KONTRON
LOGIC ANALYZER
DIAGNOSTIC PROGRAM
(LDP)

SMK-LA-1010-01

NOVEMBER 1985

KONTRON ELECTRONICS
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MOUNTAIN VIEW, CA 94039-7230

PREFACE

The Kontron Logic Analyzer Diagnostic Program (LDP) is primarily intended to be used by engineers and technicians to test the high-speed component boards (TBQ, SEQ, DMB) of the logic analyzer. To test the KDT6 and LA INT boards, see the Service Manual: Kontron LA, Volume 1 (SMK-LA-1001). The basic operating text is the Kontron Logic Analyzer Series III Operations (LA-5000).

This manual contains the following chapters and appendices:

Chapter 1 - Introduction
Chapter 2 - Test Setup
Chapter 3 - Memory Tests
Chapter 4 - TBQ Tests
Chapter 5 - SEQ Tests
Chapter 6 - DMB Tests
Appendix A - LDP Menu Input Fields
Appendix B - LDP Test Failures

For easy reference, additional schematics are provided at the end of this manual that are also duplicated in SMK-LA-1001 and LA-5000.

REVISION HISTORY

Title	Number	Date	Notes
Kontron Logic Analyzer Diagnostic Program (LDP)	SMK-LA-1010-01	11/85	Preliminary

RELATED PUBLICATIONS

Kontron Logic Analyzer Series III Operations	LA-5000-03	9/85
Service Manual: Kontron LA, Volume 1	SMK-LA-1001-01	3/85
Kontron LA Universal Probe Rack	CAN-175	10/84

WARNING

This equipment generates, uses and can radiate radio frequency energy. If it is not installed and used in accordance with this instruction manual, it may cause interference to radio communications. Kontron has constructed this equipment in accordance with good engineering design and practice, in order to minimize such interference. Because it is classified as "commercial test equipment", the equipment is exempt from the current FCC rules. Therefore, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of the FCC rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area may cause interference, in which case the user will be required, at his own expense, to take whatever measures may be required to correct the interference.

CONTENTS

ILLUSTRATIONS

FIGURES

CHAPTER 1
INTRODUCTION

1.1 PURPOSE

Because of the complex architecture of the equipment, the Kontron Logic Analyzer (LA) is difficult to test. A special program, the Logic Analyzer Diagnostic Program (LDP), has been developed to conduct appropriate tests and report the results. The purpose of this manual is to acquaint you with the LDP tests and how to perform them.

1.2 CONTENTS

This manual contains the following chapters and appendices:

Chapter 1 - Introduction

Chapter 2 - Test Setup

Chapter 3 - Memory Tests

Chapter 4 - TBQ Tests

Chapter 5 - SEQ Tests

Chapter 6 - DMB Tests

Appendix A - LDP Menu Input Fields

Appendix B - LDP Test Failures

Information on the CPU and I/O boards (KDT6, LA INT) is found in the Kontron LA Service Manual, Volume 1 (SMK-LA-1001). The basic text for operating the LA is the Kontron Logic Analyzer Series III Operations (LA-5000) manual. There is also a Customer Application Note (CAN-175) that explains how the Universal Probe Rack (UPR) operates and specifies pinout connections.

1.2.1 ORGANIZATION OF THIS MANUAL

The LDP tests are grouped in the order the hardware is configured (i.e., TBQ, SEQ, DMB), therefore, you should follow that sequence in testing.

To enhance readability, the test material in Chapters 4 through 6 is presented as follows: flowchart (if applicable), description of test, and schematics for the board. The flowcharts describe the principle underlying each test. They are intended to help the user follow the step-by-step operation, and thus enable him to find the point where the error occurred. The test descriptions suggest the cause of possible errors.

Appendix A explains what each LDP menu does and shows the associated LA sample screen shots. Appendix B describes some possible reasons for LDP test failures and also includes sample screen shots. There are additional schematics at the end of this manual pertaining to the motherboard and the KDT6 and LA INT boards (see section 1.3).

1.2.2 QUICK REFERENCE GUIDE

This subsection is designed to give you a "hands-on" approach to locating information relevant to testing the LA. The items are listed alphabetically with the corresponding manual and chapter numbers:

What	Where
Address tests	SMK-LA-1010, Chapter 3
Back panel connections	LA-5000, Chapter 1
Computer test software	SMK-LA-1001, Chapter 9
Data tests	SMK-LA-1010, Chapter 3
Disassembly of housing/boards	SMK-LA-1001, Chapter 2 (LA-SERV)

What	Where
Disk drives	SMK-LA-1001, Chapter 5
ECL bus boards	SMK-LA-1010, Chapters 4-6
Error detection at board level	SMK-LA-1001, Chapter 2 (LA-SERV)
Front panel keys	LA-5000, Chapter 2
Hardware description	SMK-LA-1010, Chapter 1
LA equipment	SMK-LA-1010, Chapter 2
LDP test software	SMK-LA-1010, Chapter 2
Power supply	SMK-LA-1001, Chapter 8
Recording operations	LA-5000, Chapter 2
Self-test probe connections	LA-5000, Chapter 3
Service remarks	SMK-LA-1001, Chapter 2 (LA-SERV)
Test instructions	SMK-LA-1010, Chapter 2
Theory of operations	LA-5000, Chapter 7
TTL bus boards	SMK-LA-1001, Chapters 3-4
Universal Probe Rack connection	CAN-175

1.3 HARDWARE DESCRIPTION

Each Kontron LA has the following board configuration (see Figure 1-1):

- KDT6 is the Z80-based, general-purpose computer board that has 256K of memory with two serial ports, one parallel port, and a floppy disk controller.
- LA INT is the I/O board that controls the reset logic, serial/parallel ports, GPIB/RS-232 connections, interface to the front panel keyboard, and the CPU-driven TTL connection.
- TBQ is the Time Base and Clock Qualifier board that controls clock generation.
- SEQ is the Trigger Sequencer Controller board that handles triggering.
- DMB is the Data Memory Board (0 to 4) that maintains data recording. Each board supports two probes and has its own clock, either external or internal.
- TMB is the Time Measurement Board, which is an optional component that records time information during Data Qualified and Transition Recording.

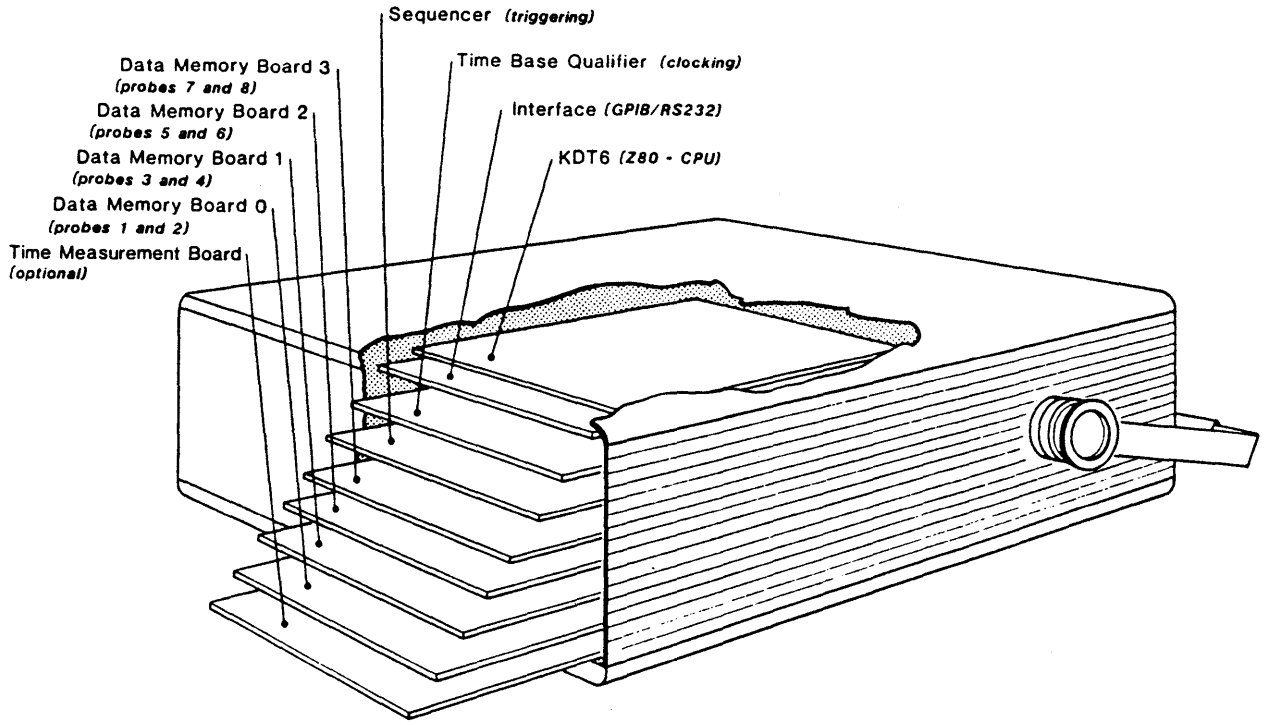

Figure 1-1. LA Board Configuration

The boards are all plugged into the LA's motherboard, which has a double Eurocard bus. There are seven pairs of 64-pin connectors; each connector pair is assigned to one of two buses:

- A-Bus

  This is a slower TTL bus used for memory access by the CPU as well as for managing other computer components.

- B-Bus

  This is a high-speed ECL bus used for communication between boards during a recording or trigger search.

See Figure 1-2 for a functional block diagram of the LA hardware.

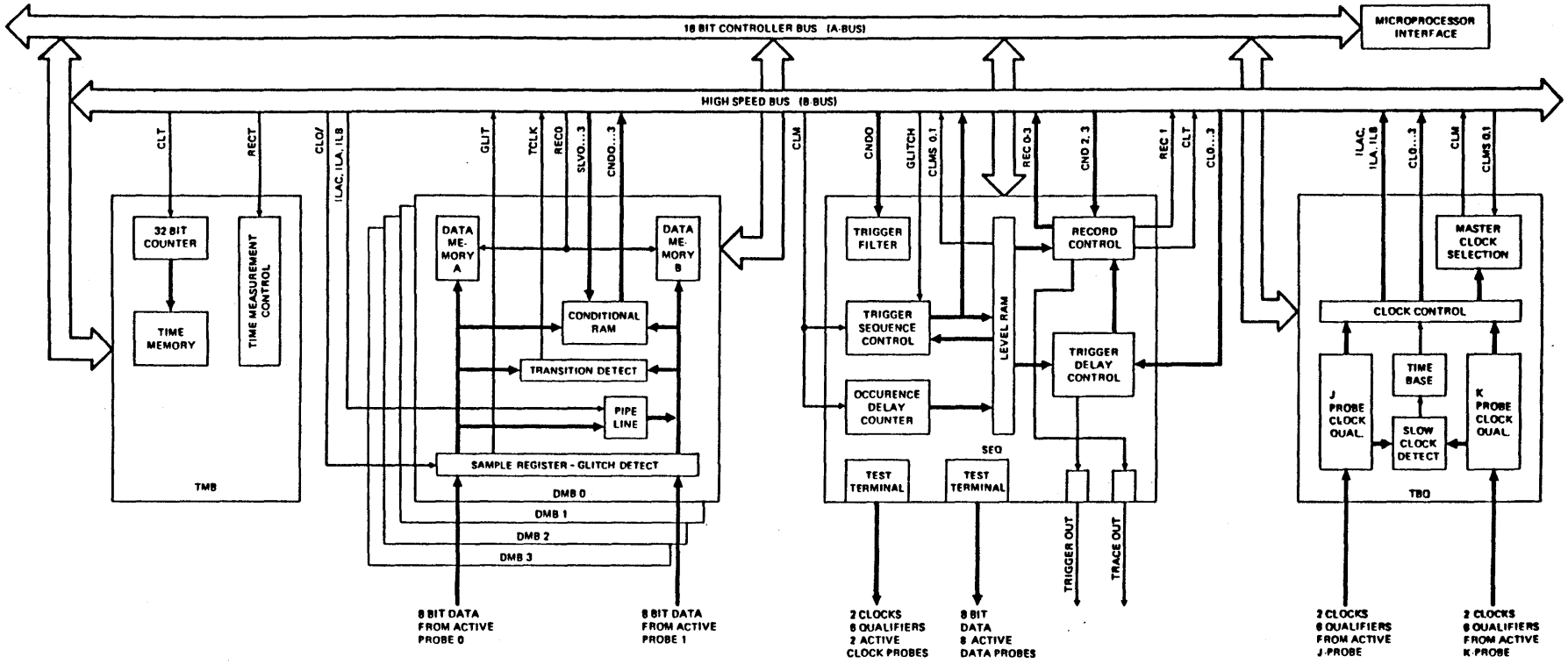

Figure 1-2. LA Hardware Functional Block Diagram

CHAPTER 2

TEST SETUP

2.1 PRE-TEST INSTRUCTIONS

Including this manual, we recommend that you have the following assembled prior to testing:

Documentation: See publications listed in section 1.2

Disks: Computer Test, SMK-LA-1001-01
KLA/KSA Diagnostic Program (LDP), SMK-LA-1010-01

Equipment: LA-32, LA-48 or LA-64

Probes (LA-SPDA):

32 channels = 6
48 channels = 8
64 channels = 10

Universal Probe Rack (LA-UPR-10)

LA test configurator with flat ribbon cables

We also suggest that you review the Quick Reference Guide in subsection 1.2.2, which identifies where supplemental testing information is located.

2.2 TEST RUN PROCEDURES

Again, we advise you to conduct your testing according to the board configuration (see section 1.3). To test the KDT6 and LA INT boards, insert the Computer Test disk into drive A, press the RESET button to automatically load the program, and follow the prompts to complete testing.

The two methods for using the LDP software to test the TBQ, SEQ and DMB boards are:

- Self-Test (with UPR and test configurator)
- Manual (without UPR and test configurator)

2.2.1 SELF-TEST METHOD

For the self-test method, perform the following steps:

1. Connect all probes into the LA-UPR-10.

2. Connect all probes to their respective positions in the rear of the LA.

3. Connect one ribbon cable of the test configurator to the front of the LA-UPR-10. Next, connect the other ribbon cable to the Data Probe/Clock Probe test terminals on the LA's back panel. These test terminals are controlled by the pattern generator circuit on the SEQ board.

4. Insert the LDP disk into drive A, press RESET to load the program, and press key 1 to start the test; follow the LDP prompts to complete testing. NOTE: If you want the test to run automatically without stopping, press the "+" key before pressing key 1, which toggles to OFF (default is ON).

2.2.2 MANUAL METHOD

If no Universal Probe Rack is available, connect the probes to the Data Probe test terminal on the LA's back panel according to the LDP operating instruction prompts. For the manual method, perform the following steps:

1. Insert LDP disk into drive A and press RESET to load the program.

2. After the Main Menu (see Figure A-1) has appeared on the screen, you can press the "+" key, which eliminates test interruption after each screen.

3. Press key 1 to start the test.

4. If the screen shows "No defective board detected", the test is finished and the equipment is in perfect working condition.

5. If, however, errors are detected and there is no indication as to which test recognizes the error, follow steps 6 through 8.

6. Push the "+" key to follow the test run on the screen.

7. Resume the test run by pressing key 1.

8. If the test indicating the presence of an error is found, press the RUBOUT key (external keyboard) or the F1 key (KLA keyboard) to get back to the Main Menu.

9. Press the "+" key again, which indicates "stop after each screen is off".

10. Press key 2 to get into the Single-Test Menu.

11. In the Single-Test Menu if you want the test to run continuously, set the flag ON by pressing key C (see Figure A-2).

12. Using the menu, select a test and then start the test by pressing the RUN/STOP key.

13. Because the audible error detection is switched ON, a "beep" will sound off during each test run when it identifies which board has an error.

    WARNING: Exchanging boards is not recommended while the power is on.

It is important to note that all data lines must go across the TBQ board and to the data bus. If one of the lines is defective, almost all tests are going to yield a negative result.

CHAPTER 3

MEMORY TESTS

In order to test the various functions of the LA boards, all RAMs located on the boards have to be in excellent working condition. Therefore, software diagnosis starts out with memory tests, followed by an operation check of the interface with the TBQ, SEQ and DMB boards. These memory tests are subdivided into data tests and address tests, which are described in the following sections.

3.1 DATA TESTS

In data tests, the same data pattern is laid down in all memory elements in order to ignore possible addressing mistakes. The data pattern itself is constructed in such a way that every bit at one point has a low and a high state. Moreover, the layout of the data pattern can indicate faulty connections between the data bits.

This kind of data test can be conducted with the following memories:

Specific RAM	Addresses*Data
TBQ Qualifier RAM	256*8 (exists 2x)
SEQ Level Address RAM	16*4
SEQ Occurrence Counter RAM low byte	16*8
SEQ Occurrence Counter RAM high byte	16*8
SEQ Level Status RAM	16*8
SEQ Trigger Filter RAM	16*4
DMB Condition RAM	256*8 (exists 4x)

Reasons for negative test results:

- Defective RAM
- Defective buffer
- Errors in the data logger

In the case of DMB Data RAM and TMB Data RAM, data cannot be written in from the computer directly; however, it is generated and written in by the DMB and TMB, respectively. The computer's task is to read the data and check it for accuracy of information.

3.2 ADDRESS TESTS

In order to find addressing errors, the RAMs are loaded with a non-repetitive pattern. This assures that each pattern is only laid down at one distinctive point in the RAM. The computer reads this pattern and checks it for accuracy of information.

Reasons for negative test results:

- Defective RAM
- Defective address counter
- Error in address logger

On the SEQ, the address counter is tested for the level address (Register 60H) in addition to the tests mentioned above. In order to yield a positive result in the test, it is not absolutely necessary that the RAMs are in perfect working condition.

Address counters located on the DMBs are also tested for data RAMs. According to the selected memory depth (2K, 4K, 8K), it is determined if the address counter can count properly all the way through the entire depth of memory. If another test is conducted, it shows whether the address counter can be precharged with any permissible value.

CHAPTER 4

TBQ TESTS

This chapter contains the tests listed below for the Time Base and Clock Qualifier (TBQ) board. The flowchart for each test (if applicable) precedes the description of the test. Schematics for the TBQ board are at the end of the chapter.

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4.1 TIME BASE TEST

Name of the test in the source listing: CLOKTS
In the Single-Test Menu of the LDP: Special Test 01

Purpose: CLOKTS determines if the time base works properly.

Reasons for negative test results:

- CL 1000 does not show up (error in clock generator or in divider chain).
- Error in the slow-clock-detection (check by means of Special Test 03, see section 4.3).

Description of the test:

The different clockings are generated in a divider chain (see page 2 of the TBQ schematics). If the slowest clocking is operating (i.e., 1000ms; hereafter referred to as CL 1000), it can safely be assumed that the divider chain is in perfect working condition.

Because CL 1000 is used in the slow-clock-detection, it is possible to test its operation via software.

The signal ENEX/ is induced and reinduced in Coil 1 (no more than 65,535 times). Thus, an external clocking rhythm is stimulated because the signals TJ0, TJ1, TK0 and TK1 toggle in the clocking rhythm of ENEX/ (see page 4 of the TBQ schematics).

Moreover, Coil 1 reads Register 73H until the date 0FH changes into 00H, which should occur when the next SYNC signal comes on. (The FLIP-FLOPs L6, K6, J5 and K5 are induced as variable cycle operations.) If the date 00H is not found within 65,535 cycles, the test result is negative.

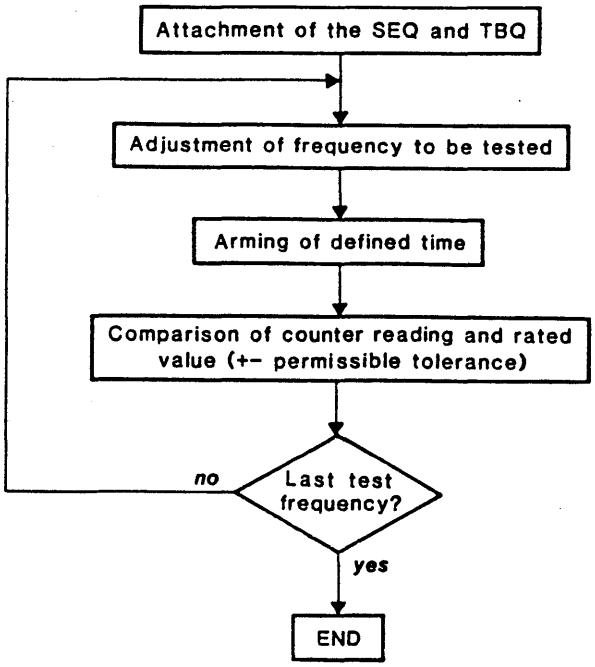

Figure 4-1. Test Loop Flowchart

4.2 ALL CLOCKS TRIGGERED BY DIVIDER CHAIN TEST

Name of the test in the source listing: CLOKT2
In the Single-Test Menu of the LDP: Special Test 02

Purpose: CLOKT2 determines if the adjustable frequencies have the proper value, and if they have been selected and processed properly.

Reasons for negative test results:

- Error detection (too fast or too slow) in all frequencies indicates a missing condition increment (Cause: DMB(s) or SEQ).

- Error detection in some frequencies indicates that there are either errors in the occurrence counter (SEQ) or in the time base (TBQ).

Description of the test:

A 16-bit wide occurrence counter is located on the SEQ. The counter uses a clock that has been selected by the TBQ. If this counter is asked to count for a specific period of time, an exactly defined counter reading has to be reached when given a precise frequency of counting. This enables the user to determine whether or not the counter readings and clockings are correct.

NOTE: A prerequisite for this test is that the counter must be in excellent working condition. Experience with this test has shown that the counter itself is imperfect rather than the clocking.

In order for the occurrence counter to work, three conditions have to be met:

1. Condition 0 (increment) has to be active. To achieve an active Condition 0, the Condition RAMs on the DMBs have to be filled with 11H. In addition, the Condition RAMs have to be enabled accordingly (load Register n2 with 30H).

2. No final trigger should have been found yet. By filling the Level Status RAMs of the sequencer with 1BH, the result is that no final trigger can be found. (Bit 4 is high at all times.)

3. The LA has to be "armed". The "arming" of the LAs is done via Register 72 on the TBQ.

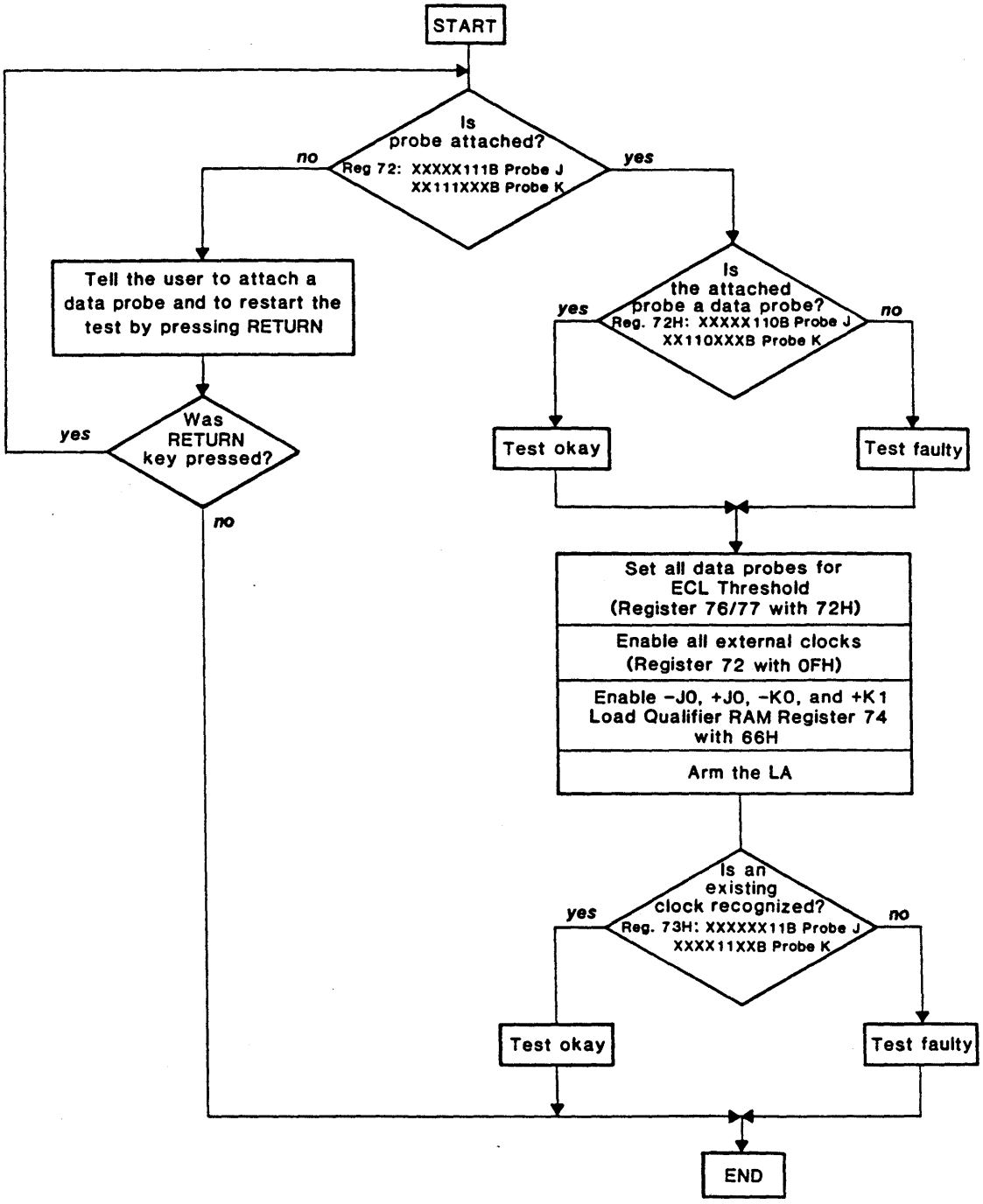

Figure 4-2. TBQ72 Flowchart

4.3 SLOW-CLOCK-DETECTION AND PROBE ID TEST

Name of the test in the source listing: TBQ72
In the Single-Test Menu of the LDP: Special Test 03

Purpose: TBQ72 determines if

a. An attached data probe is recognized properly.

b. The slow-clock-detection works properly.

Reasons for negative test results:

As per a:

- Route-marking characteristic on the probe was improperly wired or not wired at all.

- Error in the data line of Register 72.

As per b:

- Probe is not properly attached to the SEQ.

- Probe or test configurator wire defective (test has to be conducted).

- Slow-clock-detection defective (see section 4.1).

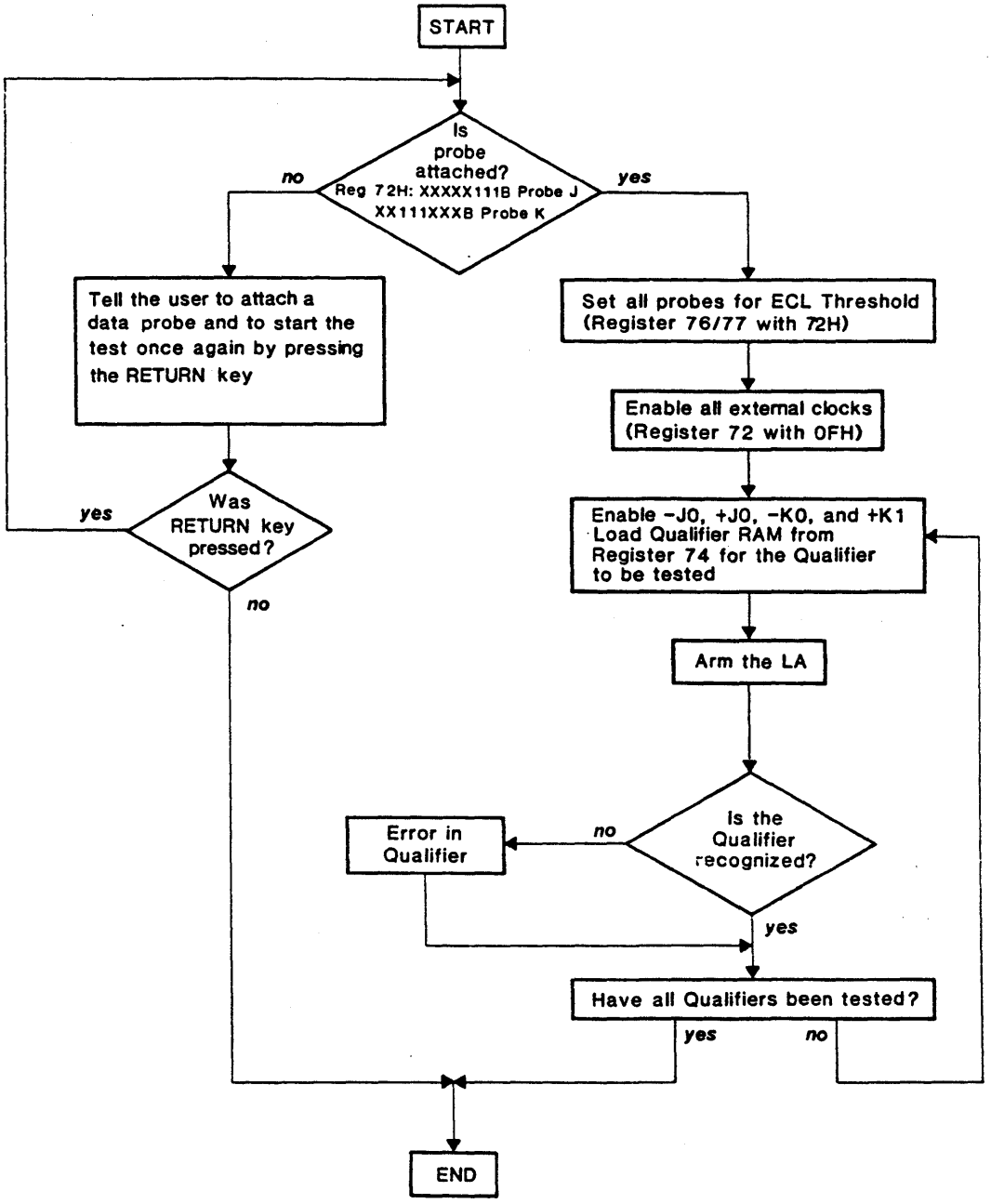

Figure 4-3. QUALTS Flowchart

4.4 QUALIFIER INPUTS TEST

Name of the test in the source listing: QUALTS
In the Single-Test Menu of the LDP: Input Tests 09 and 10

Purpose: QUALTS checks the data line from the pattern generator on the SEQ up to the Qualifier RAM on the TBQ.

Reasons for negative test results:

- Probe is not correctly attached to the SEQ.
- Probe or test configurator wire is defective (test has to be conducted).
- Pattern generator on the SEQ does not supply the right pattern.
- Input buffer on the TBQ is defective.

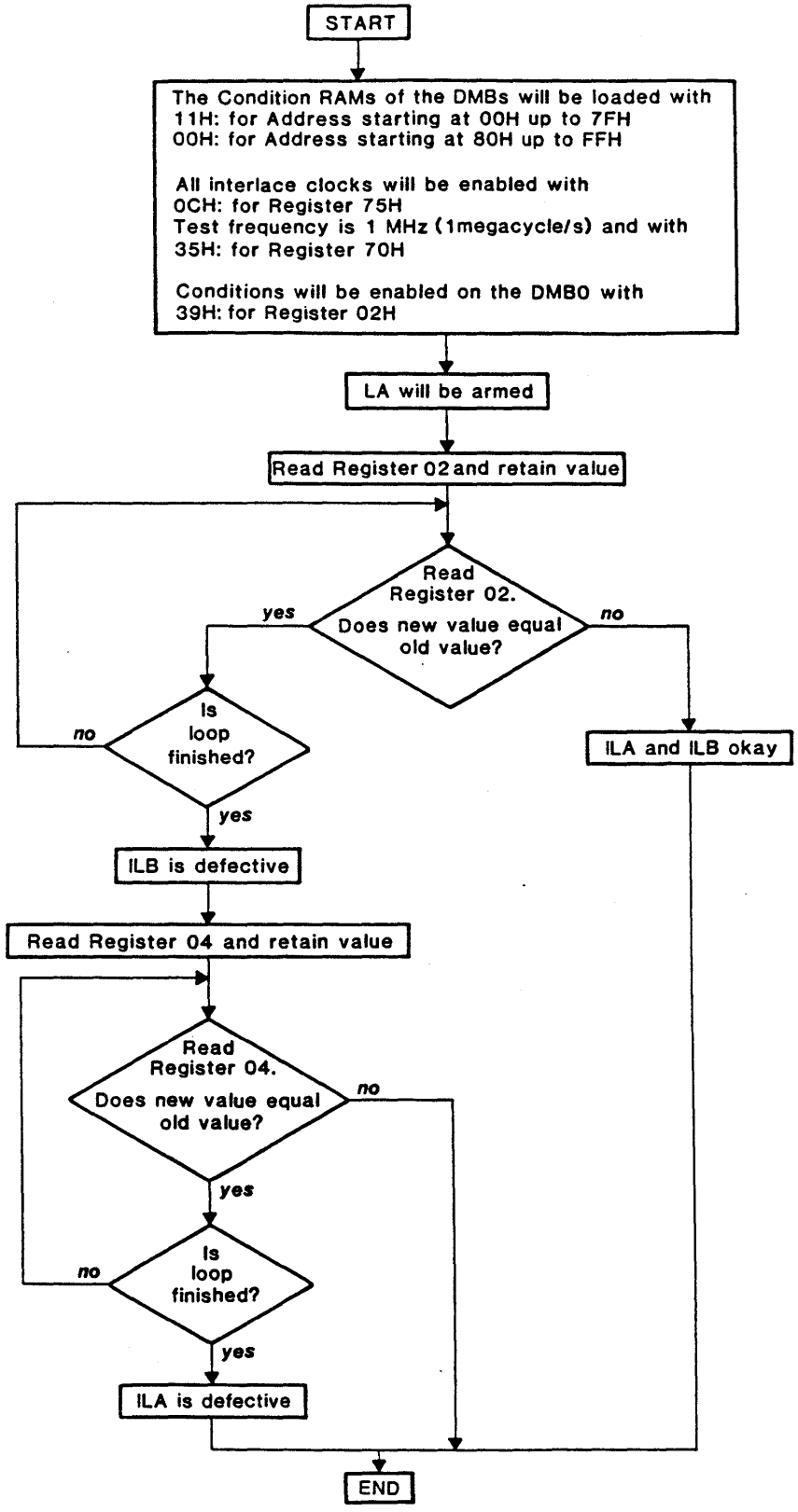

Figure 4-4. ILAB12 Flowchart

4.5 INTERLACE CLOCKS ILA1, ILB1, ILA2 AND ILB2 TEST

Name of the test in the source listing: ILABl2
In the Single-Test Menu of the LDP: Special Test 06

Purpose: ILABl2 determines if the interlace clocks are present, if they are selected properly, and indicates whether they are processed.

Reasons for negative test results:

- Control error on the TBQ (Register 75H, bits 2 and 3).
- Errors in the interlace clocks themselves.

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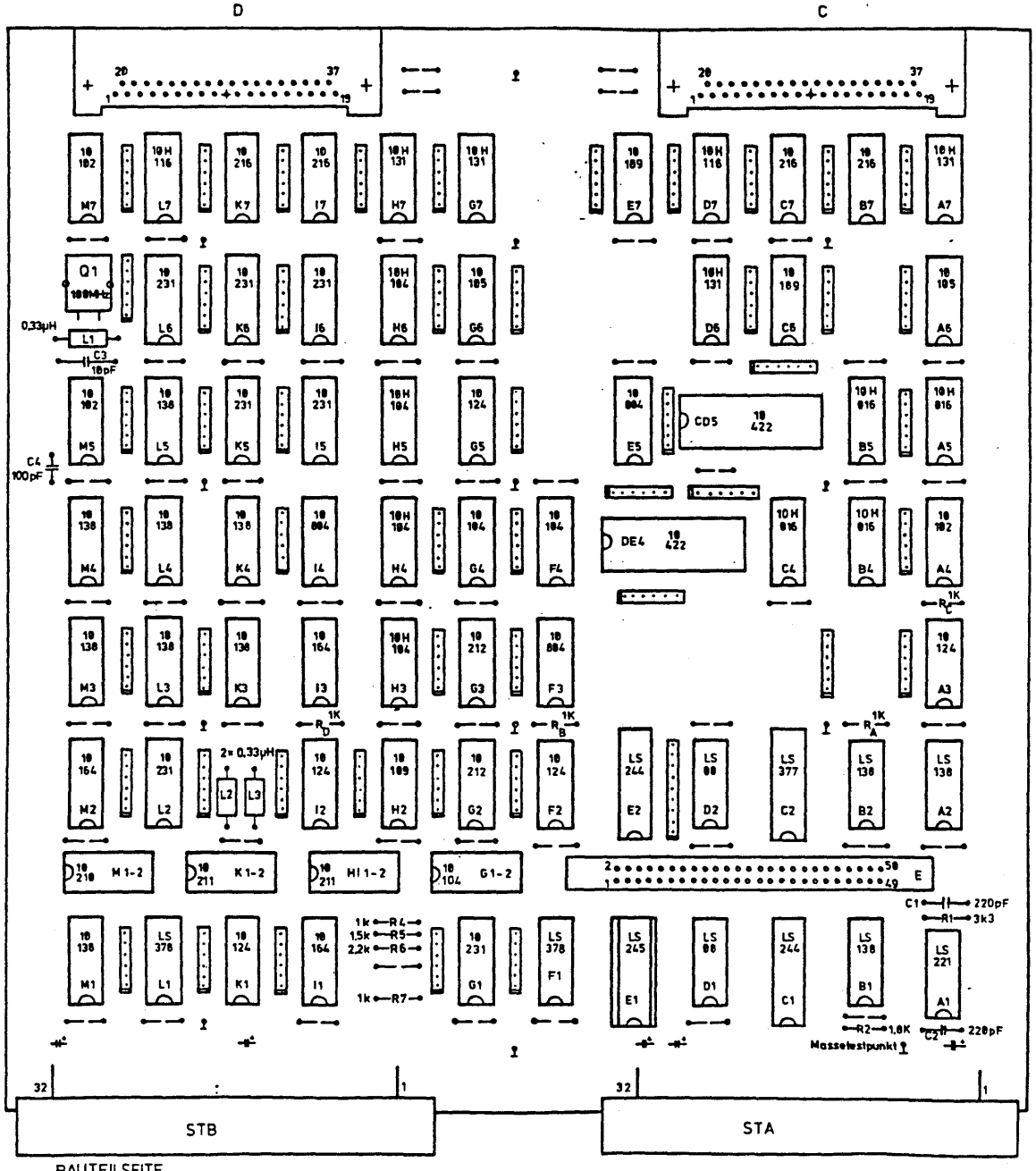

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1.4	145	20.4.82	
1.3	144	19.4.82	
	139	2.3.82	
		26.1.82	

	E.E.	Tag	Name
Bearb.		09.81	HE
Gepr.		26.1.82	

KONTRON ELECTRONIC

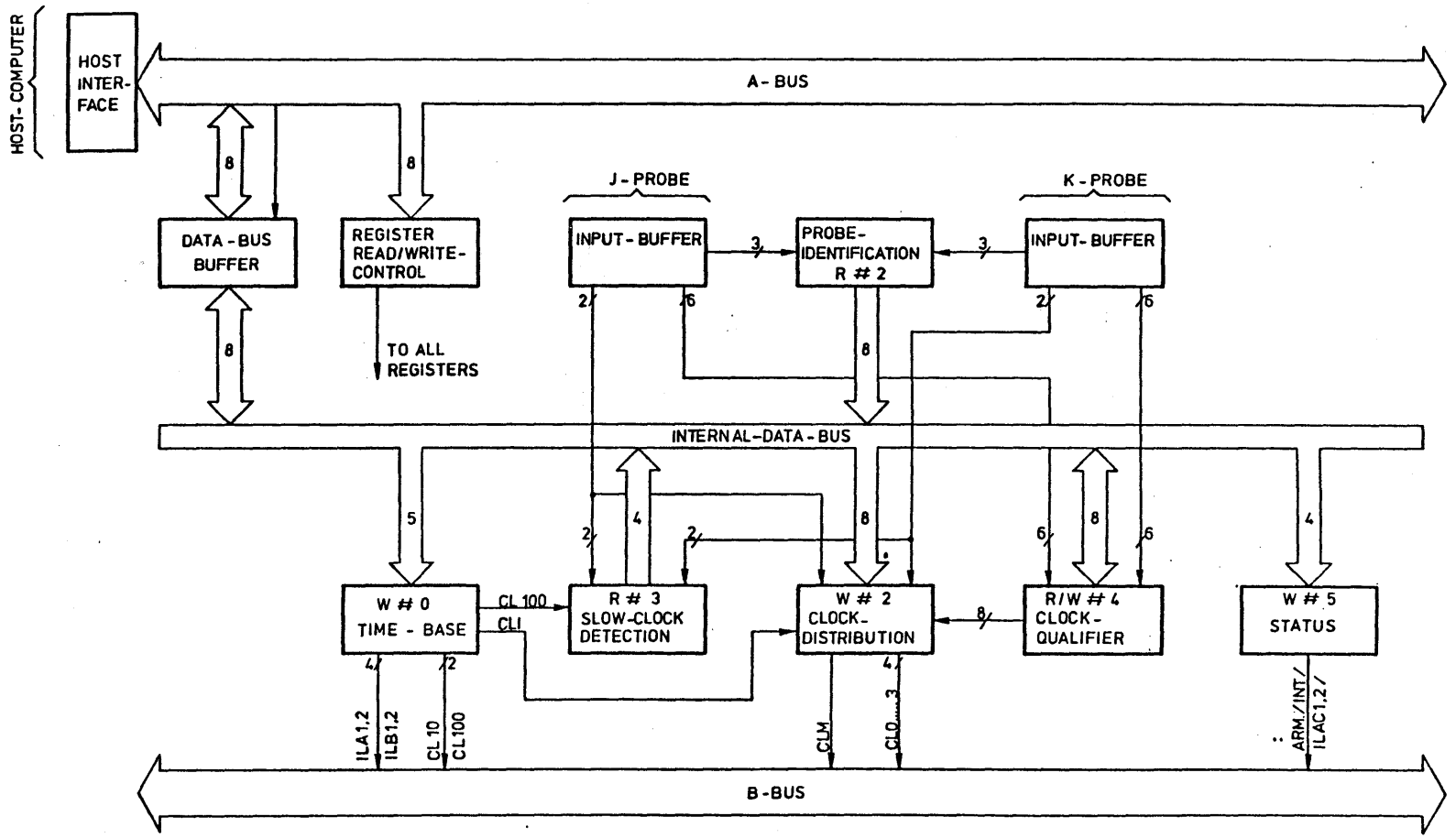
Benennung: KLA - SP-TBQ

Zu Gerät

Zeichn.-Nr. 312

Zu Anlage

Blatt Nr. v fl



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1.3	144	19.4.82	
1.2		26.1.82	

	Tag	Name
Bearb.	10.7.81	Hänsel
Gepr.	26.1.82	

KONTRON ELECTRONIC

Benennung: KLA-TBQ TIME BASE QUALIFIER

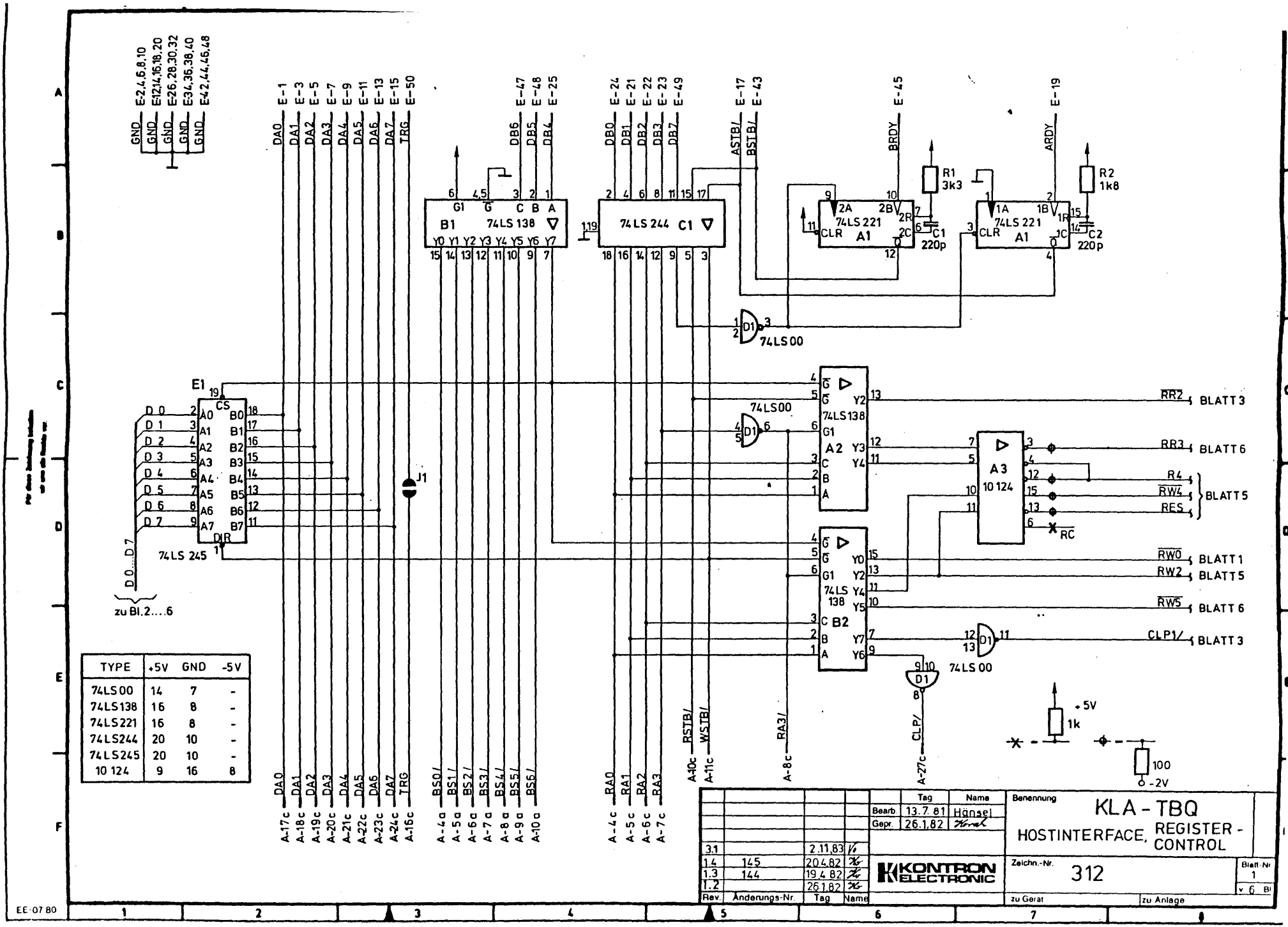
Zeichn.-Nr.: 312

Blatt-Nr.

zu Gerät

zu Anlage

EE-07.80



TYPE	+5V	GND	-5V
74LS00	14	7	-
74LS138	16	8	-
74LS221	16	8	-
74LS244	20	10	-
74LS245	20	10	-
10 124	9	16	8

Rev.	Änderungs-Nr.	Tag	Name
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1.4	145	20.4.82	
1.3	144	19.4.82	
1.2		26.1.82	

	Tag	Name
Bearb.	13.7.81	Hänsel
Gepr.	26.1.82	

KONTRON ELECTRONIC

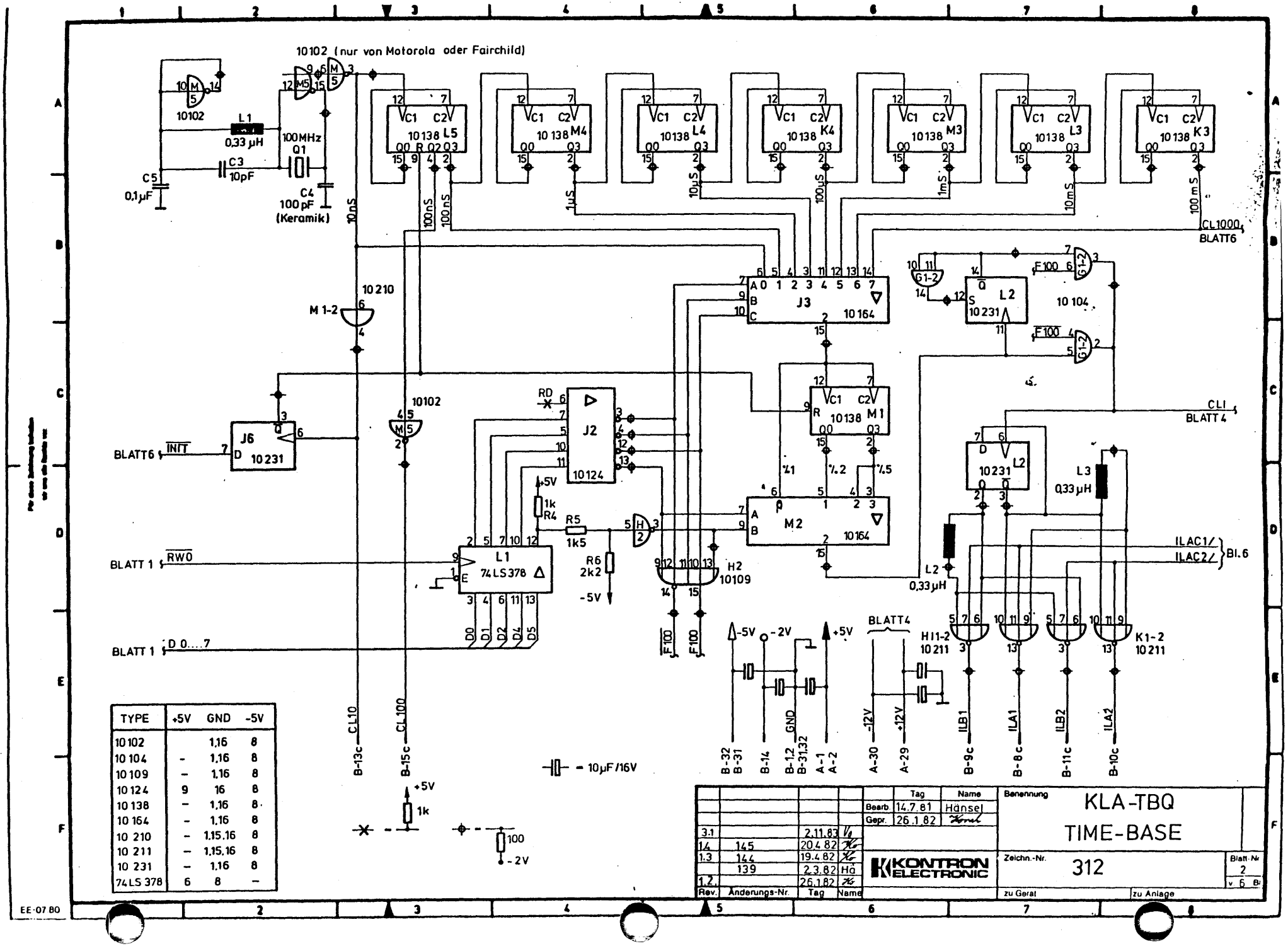
Benennung: KLA - TBQ
HOSTINTERFACE, REGISTER - CONTROL

Zeichn.-Nr. 312

Blatt-Nr. 1 v 6 Bl

zu Gerät | zu Anlage

EE-07 80



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10 104	-	1,16	8
10 109	-	1,16	8
10 124	9	16	8
10 138	-	1,16	8
10 164	-	1,16	8
10 210	-	1,15,16	8
10 211	-	1,15,16	8
10 231	-	1,16	8
74LS 378	6	8	-

Rev.	Änderungs-Nr.	Tag	Name
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1.4	145	20.4.82	
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Bearb.	14.7.81	Hänsel
Gepr.	26.1.82	

KONTRON ELECTRONIC

Benennung: KLA-TBQ TIME-BASE

Zeichn.-Nr.: 312

Blatt-Nr. 2 v 6 Bl.

zu Gerat | zu Anlage

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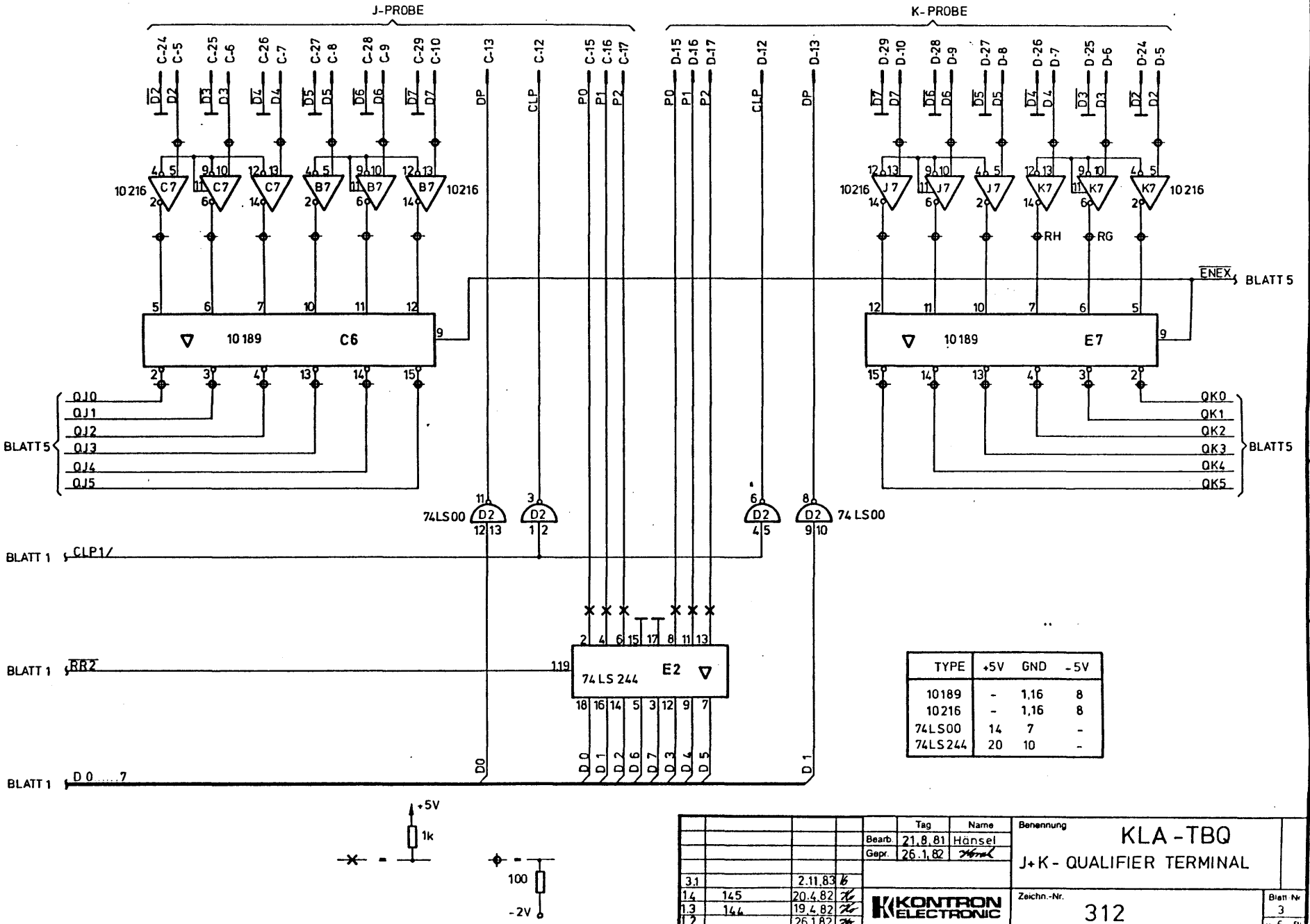

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10216	-	1,16	8
74LS00	14	7	-
74LS244	20	10	-

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Bearb.	21.8.81	Hänsel
Gepr.	26.1.82	

Benennung: KLA-TBQ
J+K-QUALIFIER TERMINAL

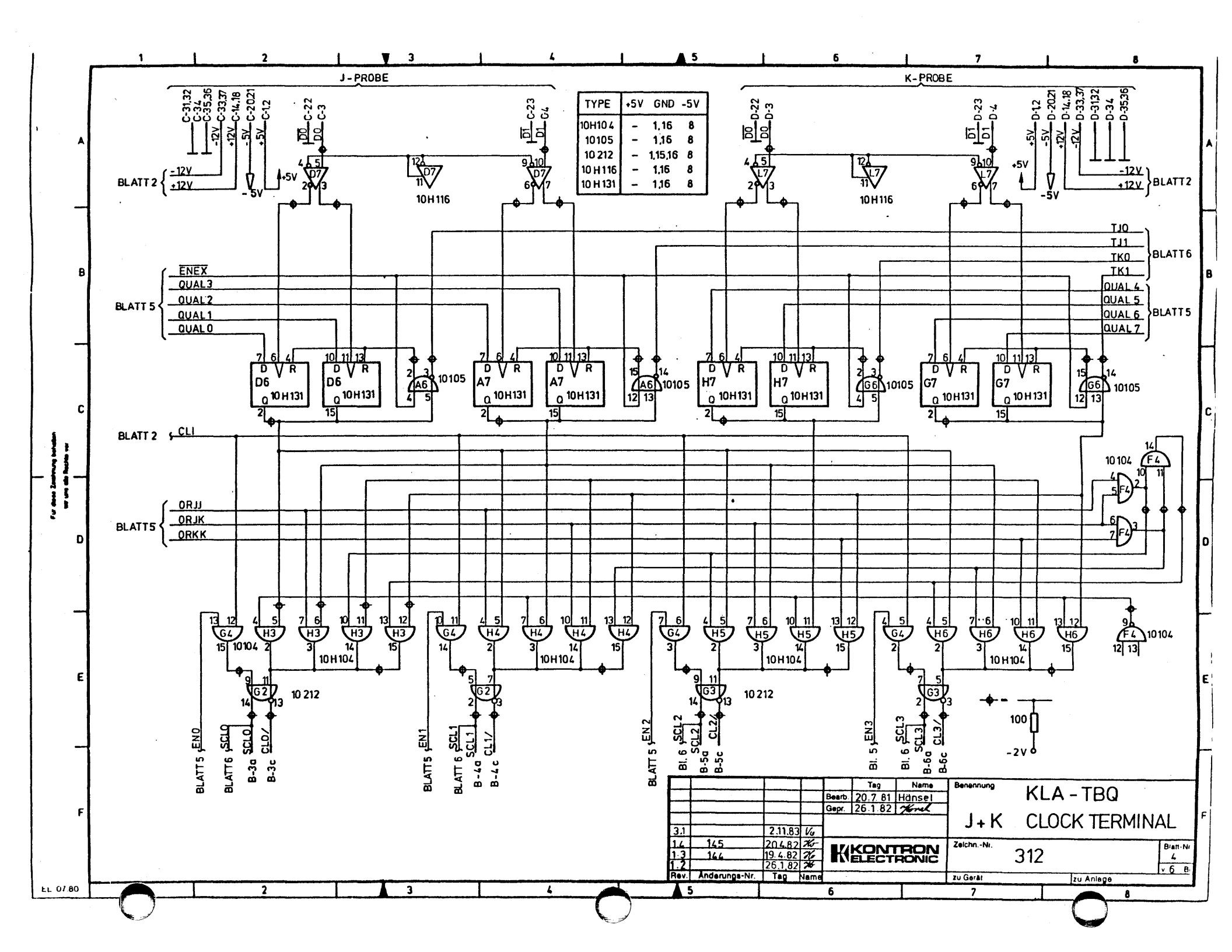
KONTRON ELECTRONIC

Zeichn.-Nr.: 312

Blatt-Nr: 3 v 6 Bl

zu Gerät | zu Anlage

EE-07 80


J-PROBE
K-PROBE
TYPE +5V GND -5V
10H104 - 1,16 8
10105 - 1,16 8
10 212 - 1,15,16 8
10 H 116 - 1,16 8
10 H 131 - 1,16 8
BLATT 2
BLATT 5
BLATT 6
ENEX
QUAL 3
QUAL 2
QUAL 1
QUAL 0
QUAL 4
QUAL 5
QUAL 6
QUAL 7
TJ0
TJ1
TK0
TK1
CLI
ORJJ
ORJK
ORKK
10H116
10105
10 H 131
10H104
10 212
10104
EN0
EN1
EN2
EN3
SCL0
SCL1
SCL2
SCL3
CL0/
CL1/
CL2/
CL3/
100
-2V
KLA - TBQ
J + K CLOCK TERMINAL
KONTRON ELECTRONIC
Bearb. 20.7.81 Hänsel
Gepr. 26.1.82
Zeichn.-Nr. 312
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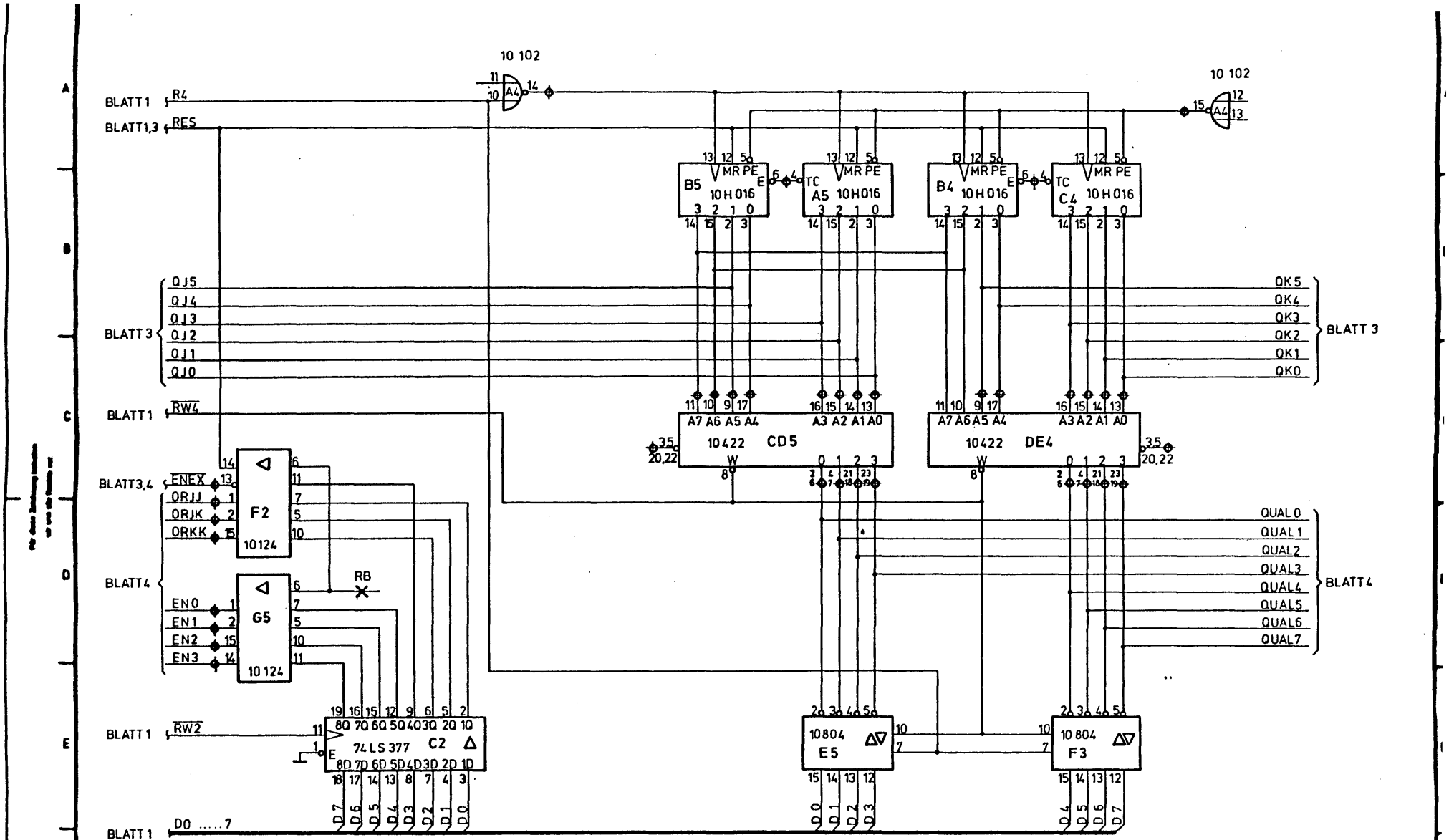
Rev. Änderungs-Nr. Tag Name
zu Gerät
zu Anlage
EL 07 80



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10102	-	1,16	8
10124	9	16	8
10422	-	1,24	12
10804	9	1,16	8
74LS377	20	10	-

Rev.	Änderungs-Nr.	Tag	Name
3.1		2.11.83	Vo
1.4	145	20.4.82	
1.3	144	19.4.82	
1.2		26.1.82	

	Tag	Name
Bearb.	16.7.81	Hänsel
Gepr.	26.1.82	

KONTRON ELECTRONIC

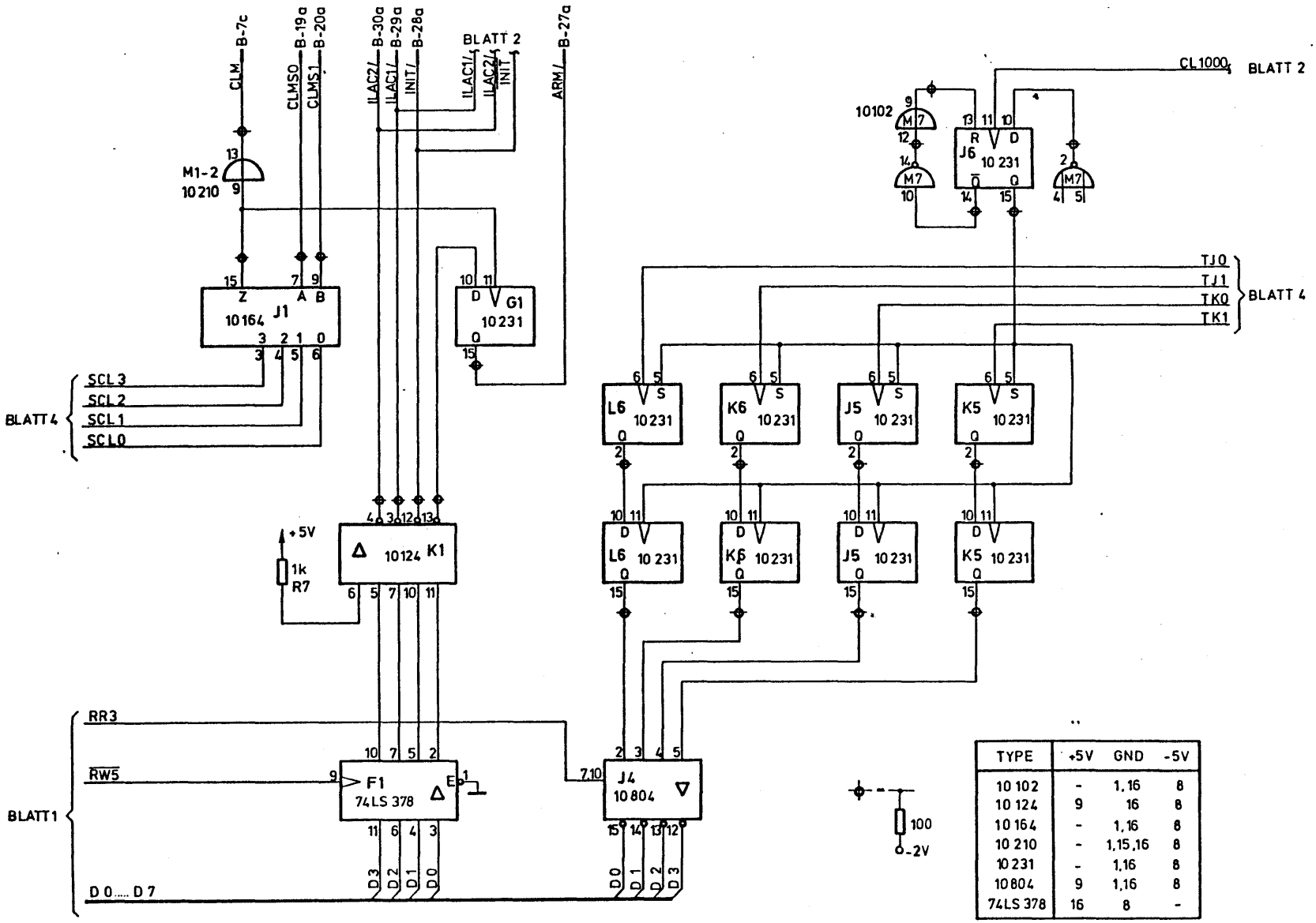
Benennung: KLA - TBQ QUALIFIER

Zeichn.-Nr. 312

Blatt Nr 5 v 6 Bl

zu Gerät | zu Anlage

EE-07 80



TYPE	+5V	GND	-5V
10 102	-	1,16	8
10 124	9	16	8
10 164	-	1,16	8
10 210	-	1,15,16	8
10 231	-	1,16	8
10 804	9	1,16	8
74LS 378	16	8	-

Rev.	Änderungs-Nr.	Tag	Name
3.1		2.11.83	
1.4	145	20.4.82	
1.3	144	19.4.82	
1.2		26.1.82	

	Tag	Name
Bearb.	16.7.81	Hänsel
Gepr.	26.1.82	

KONTRON ELECTRONIC

Benennung: KLA - TBQ
MASTER-CLOCK-SELECT
SLOW - CLOCK-DETECT

Zeichn.-Nr.: 312

Blatt Nr. 6 v 6

zu Gerät | zu Anlage

EE-07 80

CHAPTER 5

SEQ TESTS

This chapter contains the tests listed below for the Trigger Sequencer Controller (SEQ) board. The flowchart for each test (if applicable) precedes the description of the test. Schematics for the SEQ board are at the end of the chapter.

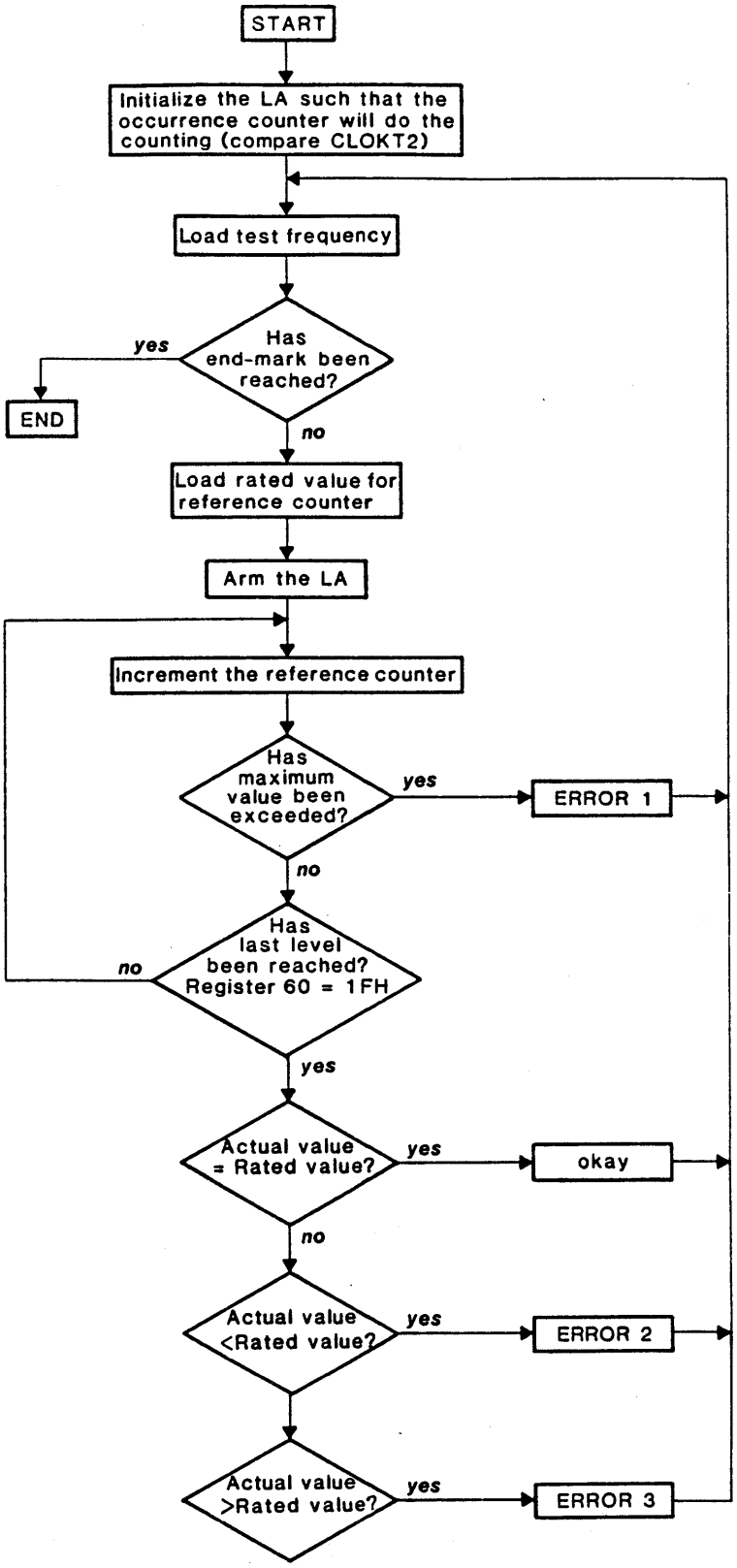


Figure 5-1. LEVINC Flowchart

5.1 LEVEL COUNTER AND OCCURRENCE COUNTER TEST

Name of the test in the source listing: **LEVINC**
In the Single-Test Menu of the LDP: Special Test 04

Purpose: LEVINC determines if the occurrence counter is loaded properly at every level, if it counts properly, and if the passage through all trigger levels takes place at the right time.

Description of errors:

Error 1:
The reference counter has reached a value of 8,000H; thus, it is safe to assume that the last level is not reached.

Possible causes:

- It is unlikely that the occurrence counter "got stuck" in one of the levels.
- The occurrence counter probably does not work at all.

Error message in the program:

"Last level was not reached"

Error 2:
The last level was reached, but too late.

Possible causes:

- The level counter does not increment.
- The occurrence counter is loaded improperly.
- The occurrence counter counts improperly.
- Errors in the data line of Register 60H.

Error message in the program:

"Last level was reached too late"

Error 3:
The last level was reached, but too early.

Same causes as in Error 2

Error message in the program:

"Last level was reached too early"

5.2 TRIGGER FILTER 0 TEST

Name of the test in the source listing: **TRGFL0**
In the Single-Test Menu of the LDP: Special Test 07

Purpose: TRGFL0 determines if the trigger filter for Condition 0 (increment) is in proper working condition.

Reasons for negative test results:

- Trigger filter is loaded improperly.
- Trigger filter does not operate properly.
- Error in the logic (which is influenced by the trigger filter).

In principle, the sequence of operation in this test is the same as in LEVINC. The differences between the two tests are:

- Only one test frequency of 100 kHz (100 kilocycles/s)
- In Level Status RAM, trigger filter 0 is enabled (1 AH)

5.3 TRIGGER FILTER 1 TEST

Name of the test in the source listing: TRGFL1
In the Single-Test Menu of the LDP: Special Test 08

Purpose: TRGFL1 determines if the trigger filter for Condition 1 (JUMP) is in proper working condition.

Reasons for negative test results:

- Trigger filter is loaded improperly.
- Trigger filter does not operate properly.
- Error in Condition 1 (JUMP).
- Error in the logic (which is influenced by the trigger filter).

In contrast to TRGFL0, the Level Status RAM is loaded with 19H (enable trigger filter 1) and the Condition RAMs are loaded with EEH (Condition 0 is not active; Condition 1 is active). Otherwise, Special Test 08 is conducted in the same way as Special Test 07.

NOTE: This is the only test that uses the condition JUMP. It checks to see that the JUMP to every level is conducted properly.

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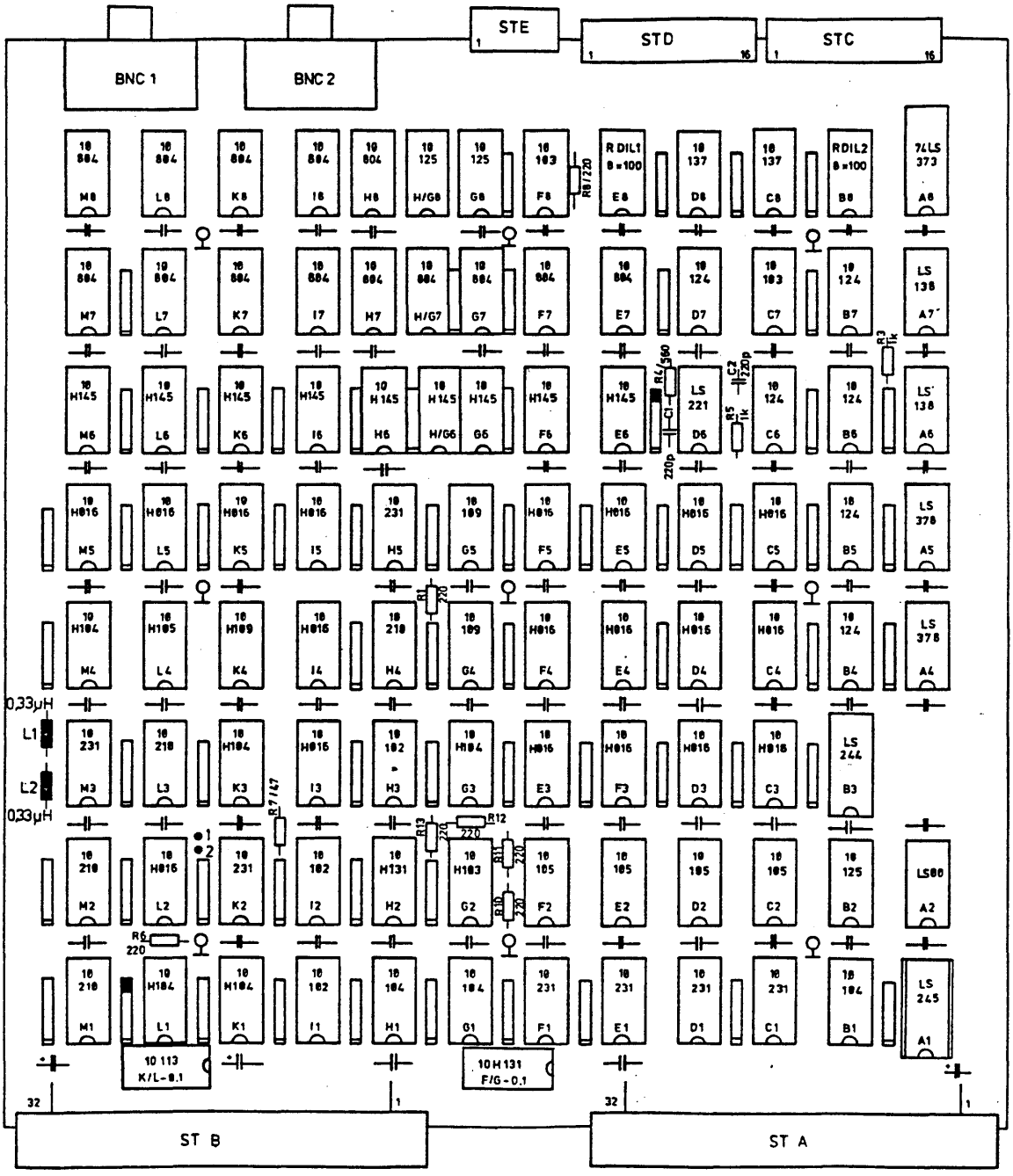


BAUTEILSEITE

= MASSETESTPUNKT

÷ = 10µF/16V

= 0,1µF DIP-C

RSIL = 100Ω

RSIL = 47Ω

= IC auf Sockel

Rev	Änderungs-Nr.	Tag	Name
1.1		27.1.82	
1.2	143	19.4.82	
1.3	146	20.4.82	
1.4	153	15.7.82	
3.1		2.11.83	

	EE	Tag	Name
Bearb.		08.81	HE
Gepr.		11.1.82	

KONTRON ELECTRONIC

Benennung: KLA - SEQ

BESTÜCKUNGSSKIZZE

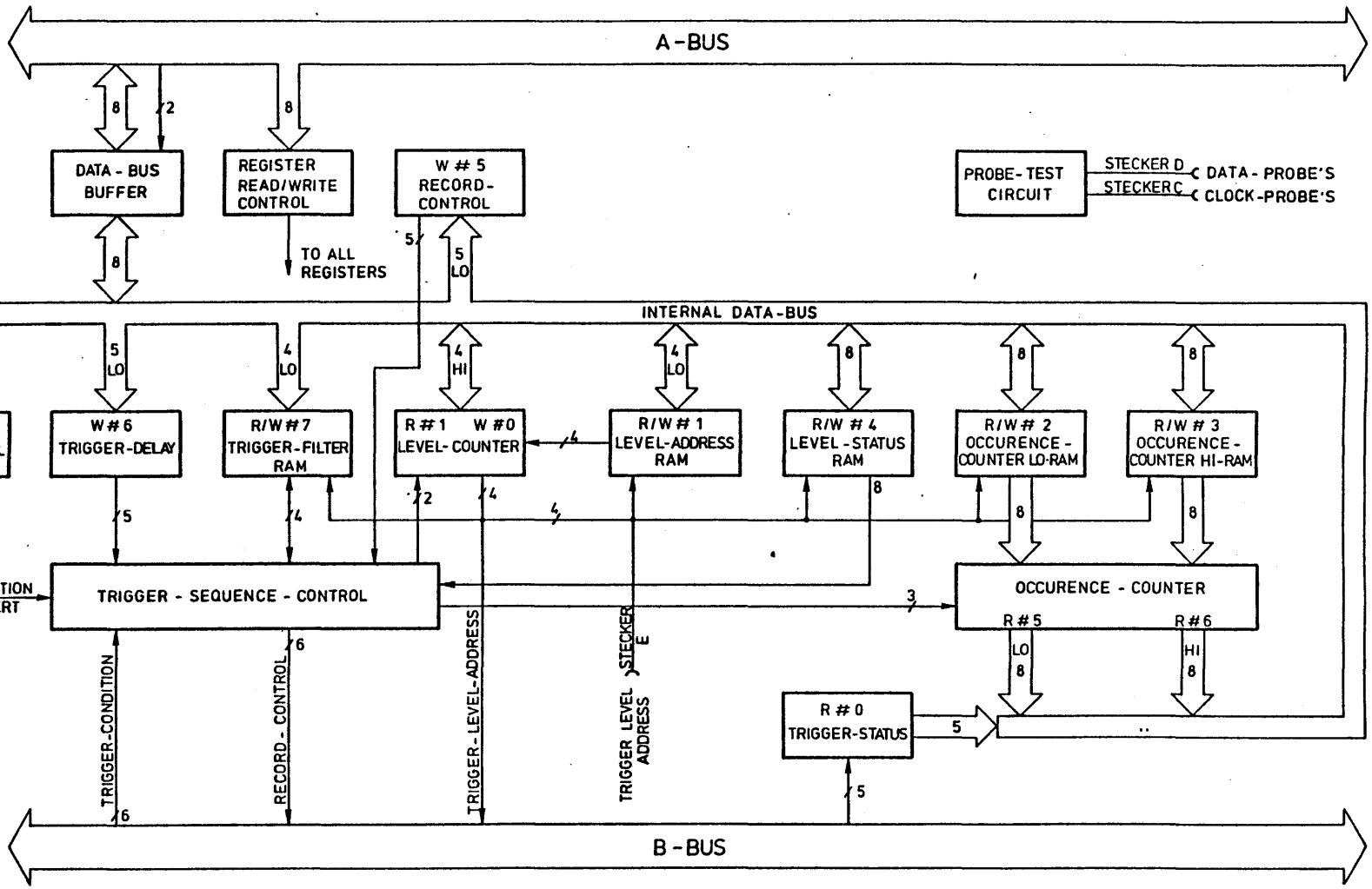
Zeichn.-Nr.: 313

Blatt Nr.: v 0

zu Gerät

zu Anlage

ET-07 80



Rev.	Änderungs-Nr.	Tag	Name
3.1		2.11.83	
1.4	153	15.7.82	
1.3	146	20.4.82	
1.2	143	19.4.82	
1.1		27.1.82	

	Tag	Name
Bearb.	20.7.81	Hansel
Gepr.	21.7.81	Hansel

KONTRON ELECTRONIC

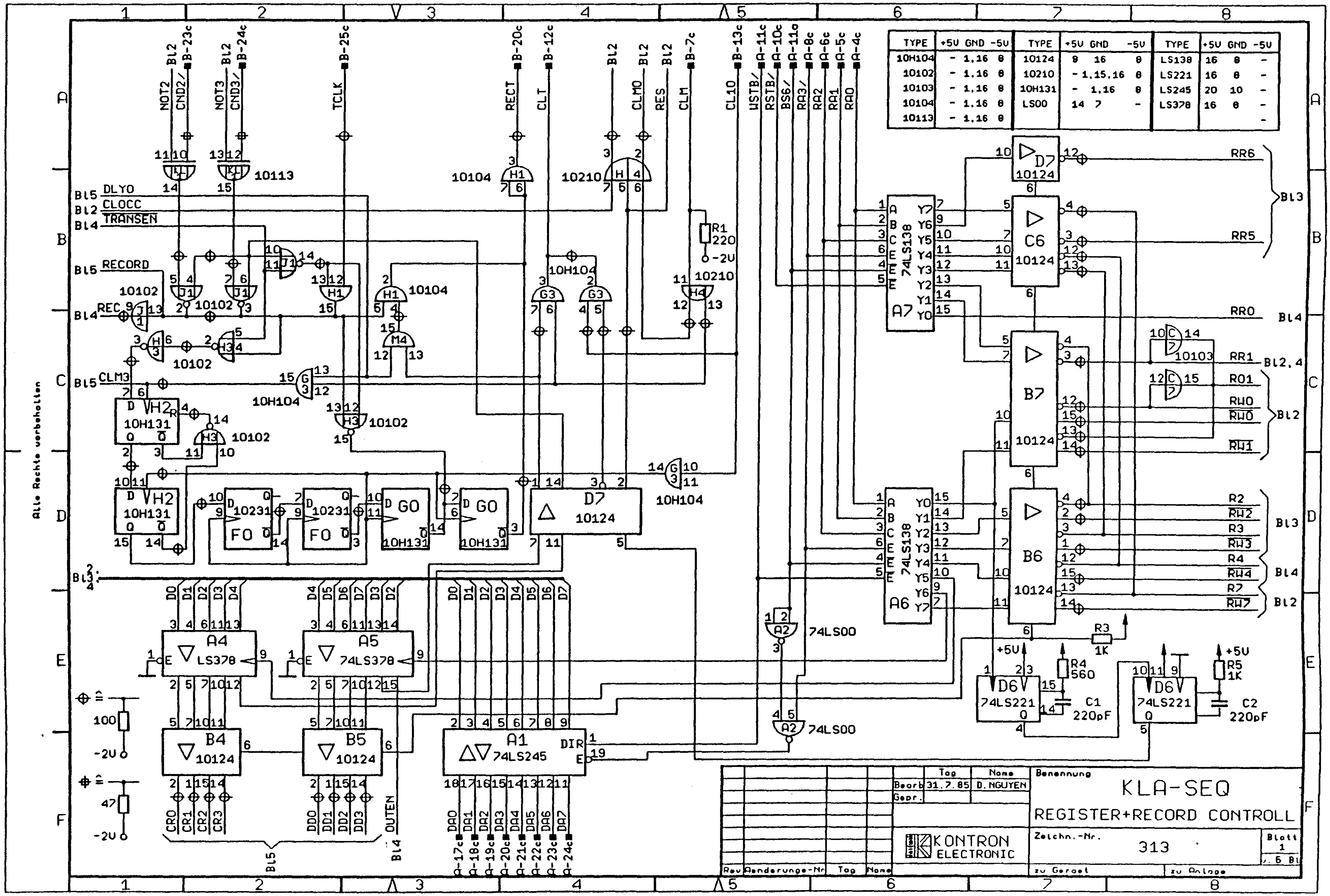
Benennung: KLA - SEQ SEQUENCE - CONTROL

Zeichn.-Nr. 313

Blatt-Nr. v Bl

zu Gerät | zu Anlage

EE 07 80



TYPE	+5V GND -5V	TYPE	+5V GND -5V	TYPE	+5V GND -5V
10H104	- 1,16 8	10124	8 16 8	LS138	16 8 -
10102	- 1,16 8	10210	- 1,15,16 8	LS221	16 8 -
10103	- 1,16 8	10H131	- 1,16 8	LS245	20 10 -
10104	- 1,16 8	LS00	14 7 -	LS378	16 8 -
10113	- 1,16 8				-

	Tag	Name
Bearb	31.7.85	D. NGUYEN
Gepr.		

Rev | Aenderungs-Nr | Tag | Name

Benennung

KLA-SEQ

REGISTER+RECORD CONTROLL

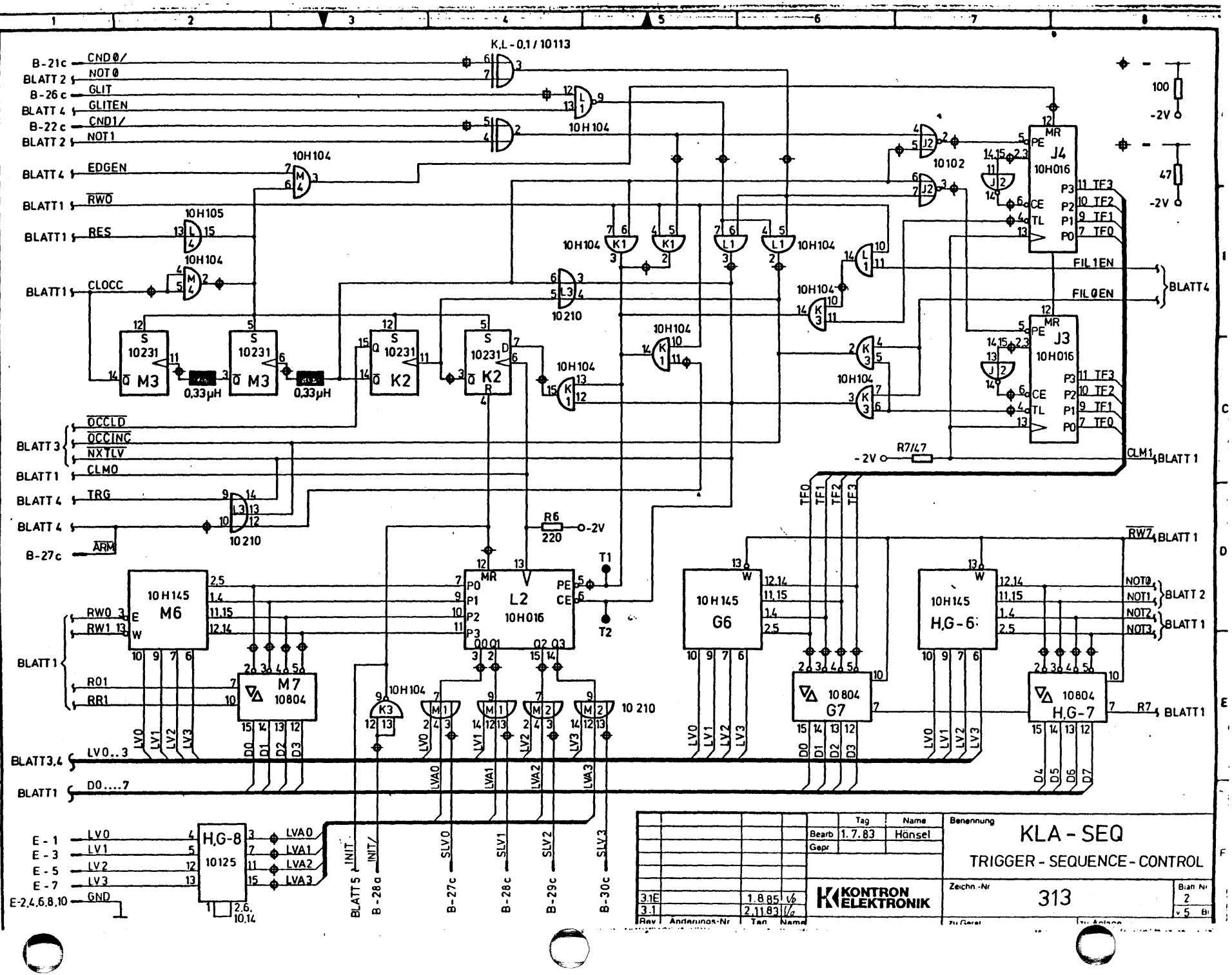
KONTRON ELECTRONIC

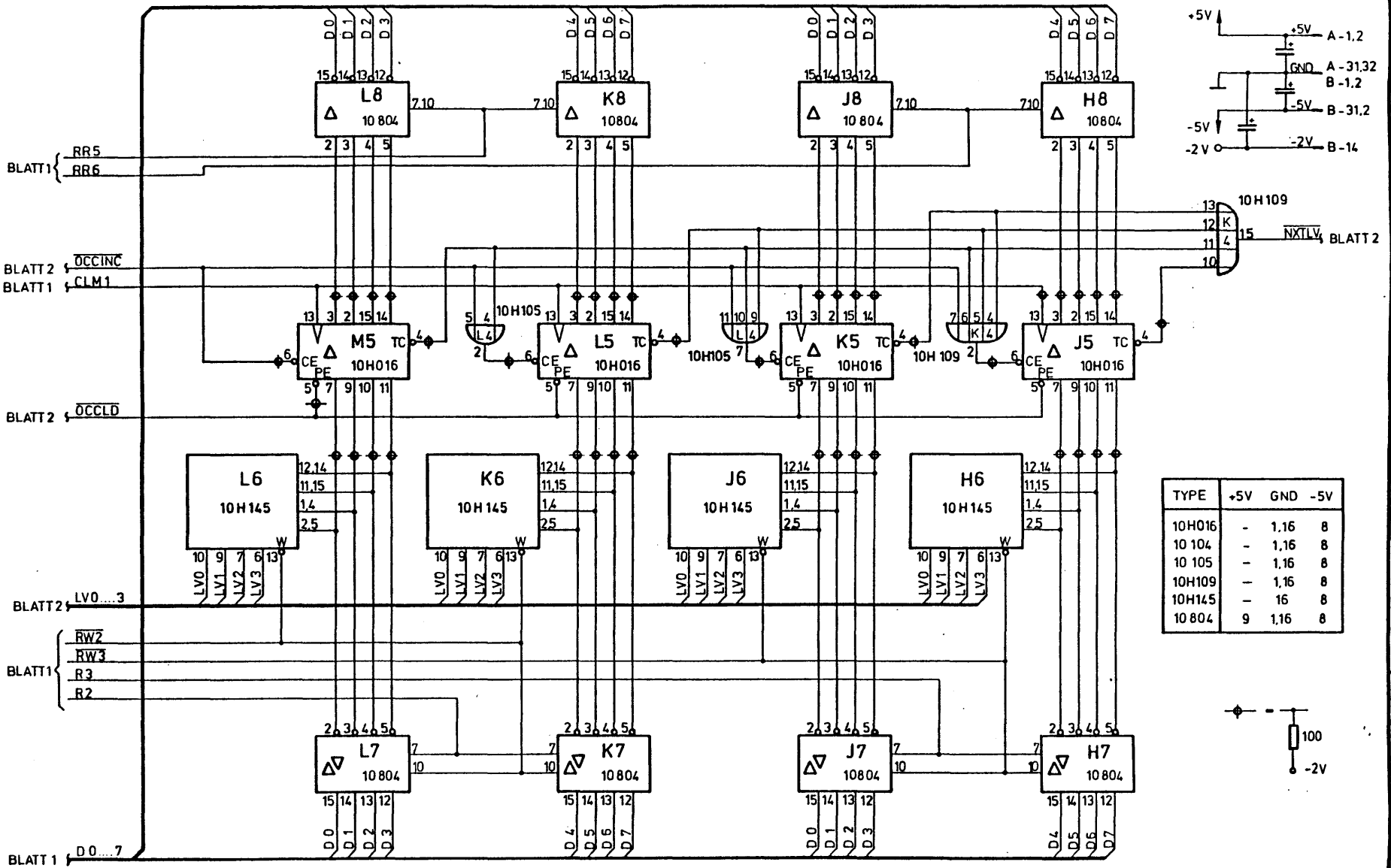
Zeichn.-Nr. 313

Blatt 1 v. 6 Bl

zu Geraet

zu Anlage


K,L - 0,1 / 10113
B-21c CND0/
BLATT 2 NOT0
B-26 c GLIT
BLATT 4 GLITEN
B-22 c CND1/
BLATT 2 NOT1
10H104
BLATT 4 EDGEN
BLATT 1 RWO
BLATT 1 RES
10H105
BLATT 1 CLOCC
10H104
10231 M3
0,33µH
10231 M3
0,33µH
10231 K2
10231 K2
10210
10H104
10102
10H016 J4
10H016 J3
FIL1EN
FILOEN
BLATT4
100
-2V
47
-2V
R7/47
-2V
CLM1 BLATT 1
OCCLD
OCCINC
NXTLV
CLMO
BLATT 3
BLATT 1
TRG
BLATT 4
BLATT 4
ARM
B-27c
10210
R6
220
-2V
T1
T2
10H016 L2
10H145 M6
10804 M7
10H145 G6
10804 G7
10H145 H,G-6
10804 H,G-7
RW0
RW1
RO1
RR1
BLATT 1
RW7 BLATT 1
NOT0
NOT1
NOT2
NOT3
BLATT 2
BLATT 1
R7 BLATT 1
LV0..3
BLATT3,4
DO....7
BLATT1
10H104
10 210
E-1 LV0
E-3 LV1
E-5 LV2
E-7 LV3
E-2,4,6,8,10 GND
H,G-8 10125
LVA0
LVA1
LVA2
LVA3
INIT
INIT/
BLATT 5
B-28a
B-27c
B-28c
B-29c
B-30c
SLV0
SLV1
SLV2
SLV3
Tag Name
Bearb 1.7.83 Hänsel
Gepr
Benennung
KLA - SEQ
TRIGGER - SEQUENCE - CONTROL
KONTRON ELEKTRONIK
Zeichn.-Nr
313
3.1E 1.8.85
3.1 2.11.83
Änderungs-Nr
Tag Name



TYPE	+5V	GND	-5V
10H016	-	1,16	8
10 104	-	1,16	8
10 105	-	1,16	8
10H109	-	1,16	8
10H145	-	16	8
10 804	9	1,16	8

Rev.	Änderungs-Nr.	Tag	Name
3.1E		1.8.85	Ho
3.1		2.11.83	Ho
1.4	153	15.7.82	Ho
1.3	146	20.4.82	Ho
1.2	143	19.4.82	Ho
	Nr. 138	3.2.82	Ho
1.1		27.1.82	Ho

	Tag	Name
Bearb.	21.7.81	Hensel
Gepr.	29.1.82	Hensel

KONTRON ELECTRONIC

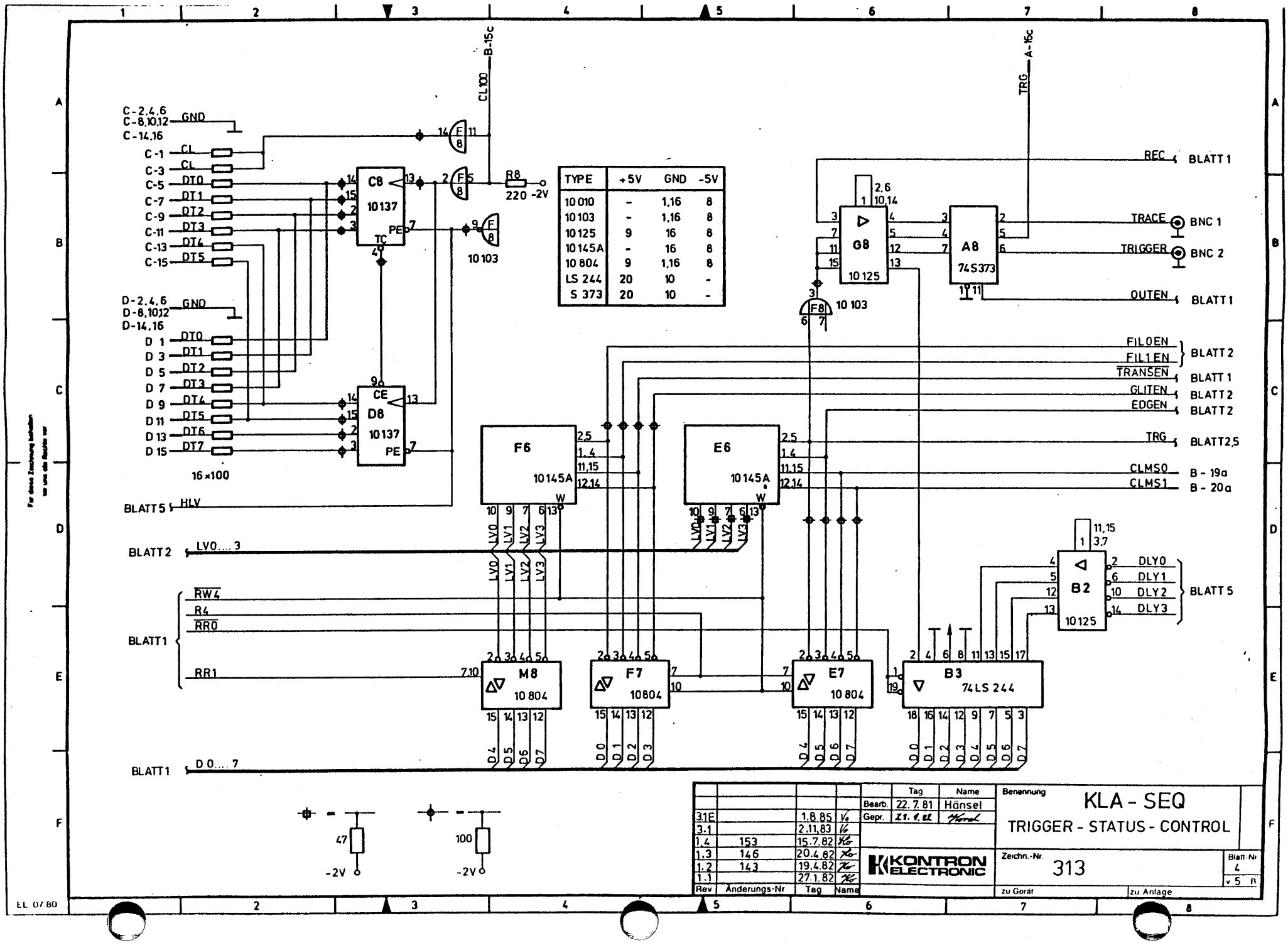
Benennung: KLA - SEQ
OCCURENCE - COUNTER

Zeichn.-Nr. 313

Blatt Nr. 3 v. 5 Bl.

zu Gerat | zu Anlage

EL 07 80



Rev	Änderungs-Nr	Tag	Name
3.1E		1.8.85	
3.1		2.11.83	
1.4	153	15.7.82	
1.3	146	20.4.82	
1.2	143	19.4.82	
1.1		27.1.82	

	Tag	Name
Bearb.	22.7.81	Hänsel
Gepr.	23.7.81	

KONTRON ELECTRONIC

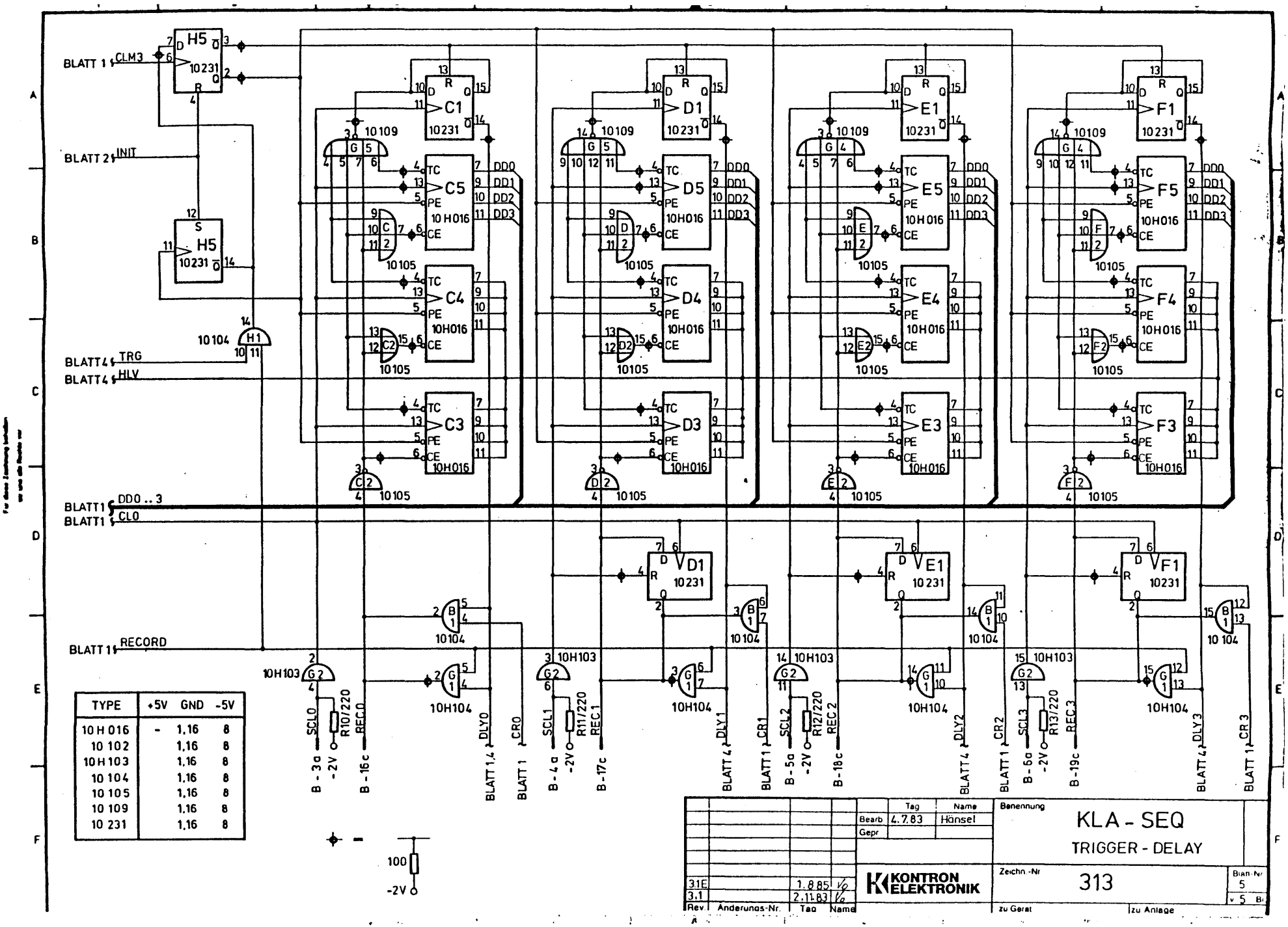
Benennung: KLA - SEQ
TRIGGER - STATUS - CONTROL

Zeichn.-Nr. 313

Blatt-Nr. 4 v 5 B

zu Gerät | zu Anlage

EL 07 80



TYPE	+5V	GND	-5V
10 H 016	-	1,16	8
10 102		1,16	8
10 H 103		1,16	8
10 104		1,16	8
10 105		1,16	8
10 109		1,16	8
10 231		1,16	8

	Tag	Name
Bearb	4.7.83	Hänsel
Gepr		

Rev.	Änderungs-Nr.	Tag	Name
3.1E		1.8.85	Ho
3.1		2.11.83	Ho

KONTRON ELEKTRONIK

Benennung: KLA - SEQ
TRIGGER - DELAY

Zeichn.-Nr: 313

Blatt-Nr: 5
v 5 Bl

zu Gerät | zu Anlage

CHAPTER 6

DMB TESTS

This chapter contains the tests listed below for the Data Memory Board (DMB). There can be up to four of these boards, which are numbered 0 through 3. The flowchart for each test (if applicable) precedes the description of the test. Schematics for the DMB board are at the end of the chapter.

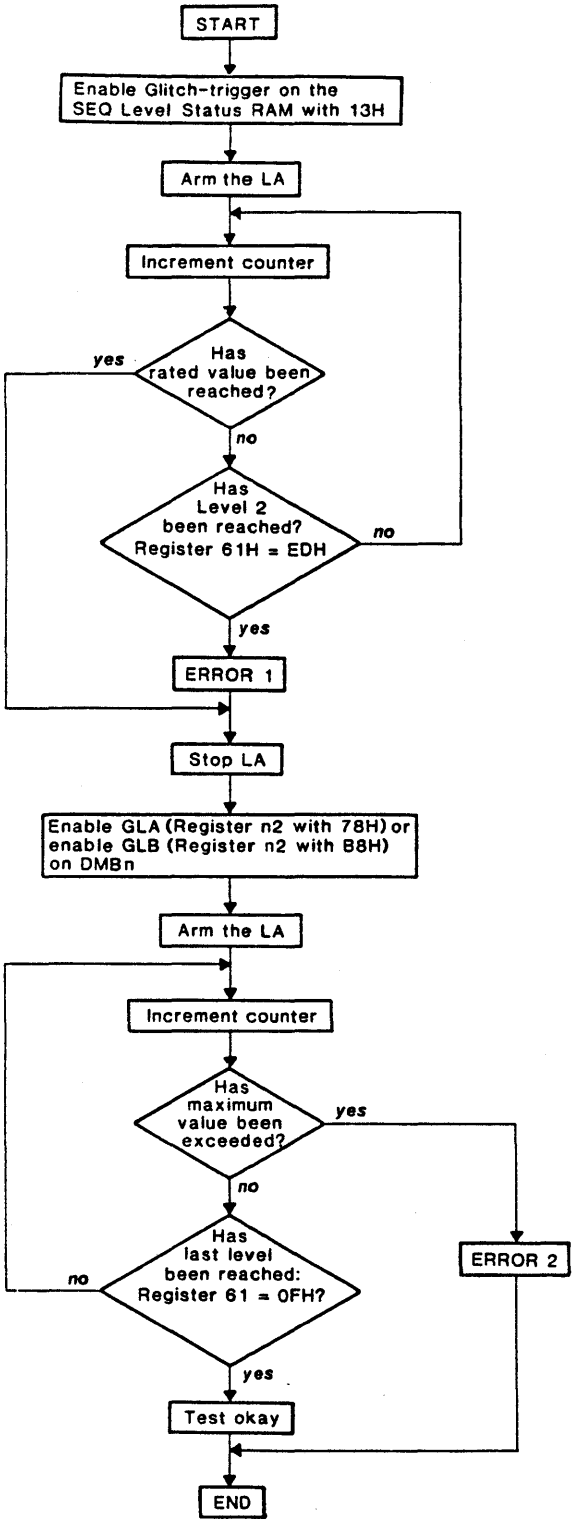


Figure 6-1. GLAGLB Flowchart

6.1 CONDITION GLIT TEST

Name of the test in the source listing: **GLAGLB**
In the Single-Test Menu of the LDP: Glitch Tests Condition

Purpose: GLAGLB determines if Condition GLIT is selected properly by each DMB, if Condition GLIT is received properly by the SEQ, and if it is processed.

Description of errors:

Error 1:
Although glitch was not enabled on the DMBs, Level 2 was reached on the SEQ. As a result, Condition GLIT is always active.

Possible causes:

- If errors occur in all eight tests, the cause for the errors is probably found on the SEQ.

  Example: Line GLIT, short circuit on low

- If errors occur only in some of the tests, the cause for the errors is probably found on the respective DMB.

  Example: Control error in Register 2 on the respective DMB

Error message in the program:

"Condition glit error"

Error 2:
The last level was not reached, probably due to a missing Condition GLIT.

Possible causes:

- If errors occur in all eight tests, the cause for errors is probably found on the SEQ.

  Examples: Line GLIT, short circuit on high
  Line GLIT interrupted

Possible causes (continued):

- If errors occur in only some of the tests, the cause for the errors is probably found on the respective DMB.

  Example: Control error in Register 2 on the respective DMB

Error message in the program:

"Condition glit is missing"

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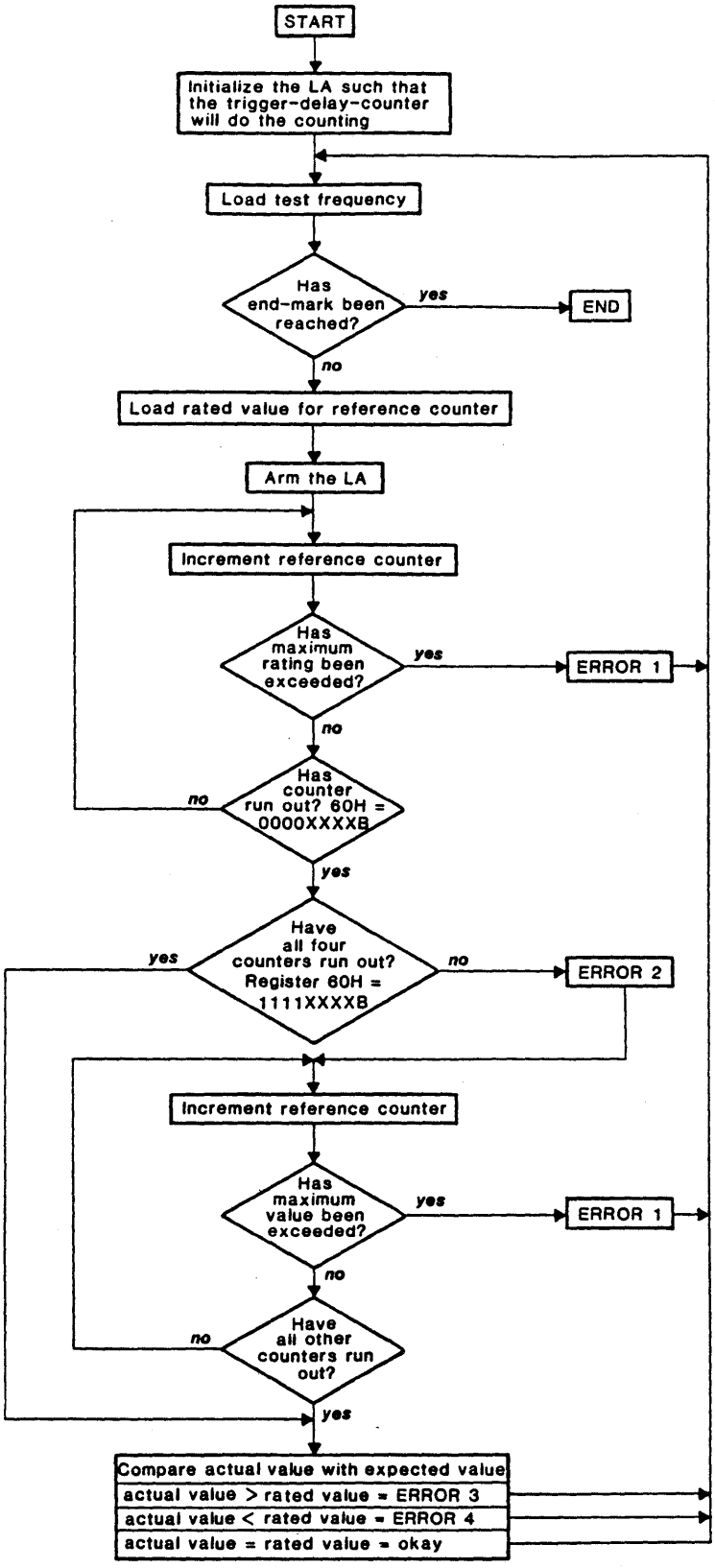

Figure 6-2. DELCNT Flowchart

6.2 ALL TRIGGER-DELAY-COUNTERS TEST

Name of the test in the source listing: **DELCNT**
In the Single-Test Menu of the LDP: Special Test 05

Description of errors:

Error 1:
The maximum value (8,000H loops) of the reference counter was reached. As a result, no trigger-delay-counter ran out.

Error 2:
At least one trigger-delay-counter has run out. However, not all four trigger-delay-counters have completed the run.

By now, all trigger-delay-counters have run out, but the timing of the work cycle was wrong.

Error 3:
Trigger-delay-counter ran out too late.

Error 4:
Trigger-delay-counter ran out too early.

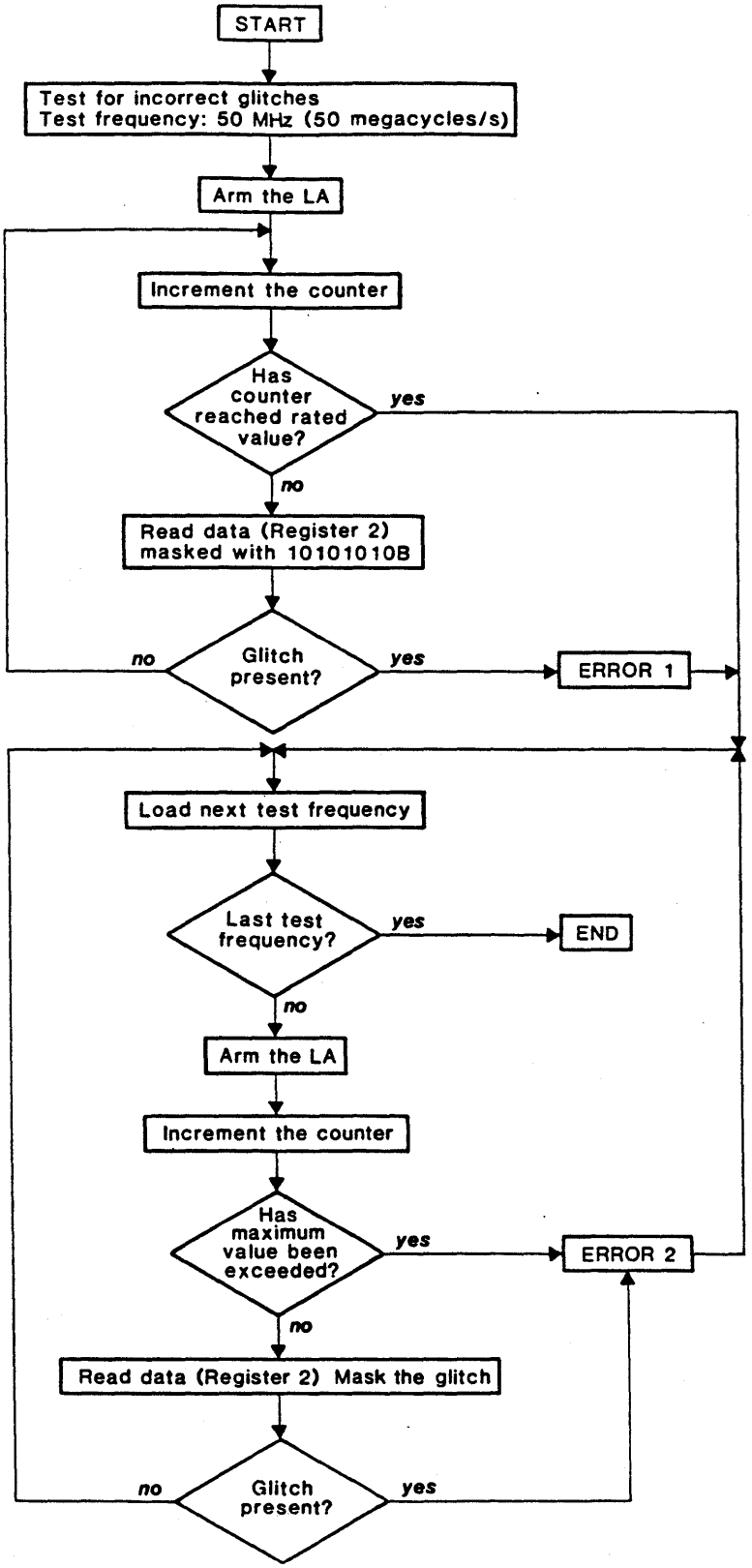

Figure 6-3. GLIT Flowchart

6.3 GLITCH-LATCH TEST

Name of the test in the source listing: **GLIT**
In the Single-Test Menu of the LDP: Glitch-Latch Tests

Purpose: GLIT determines if all glitch-latches on the DMBs are working properly.

Description of errors:

Error 1:
Glitches were detected, although no glitches should appear at a test frequency of 50 MHz (50 megacycles/s).

Possible causes:

- Defective FLIP-FLOP at respective input.
- Control error in Register 2 on the respective DMB.

Error message in the program:

"Test of false occurring glitches":

```
Glitch-latch 01     error/ok
Glitch-latch 03     error/ok
Glitch-latch 05     error/ok
Glitch-latch 07     error/ok
```

Error 2:
No glitch appeared, although the respective glitch-latch at this particular test frequency should recognize the input signals as glitches.

Possible causes:

- Defective FLIP-FLOP at respective input.
- Control error in Register 2 on the respective DMB.

Error message in the program:

"Test of false missing glitches":

```
Glitch-latch 01     error/ok
Glitch-latch 03     error/ok
Glitch-latch 05     error/ok
Glitch-latch 07     error/ok
```

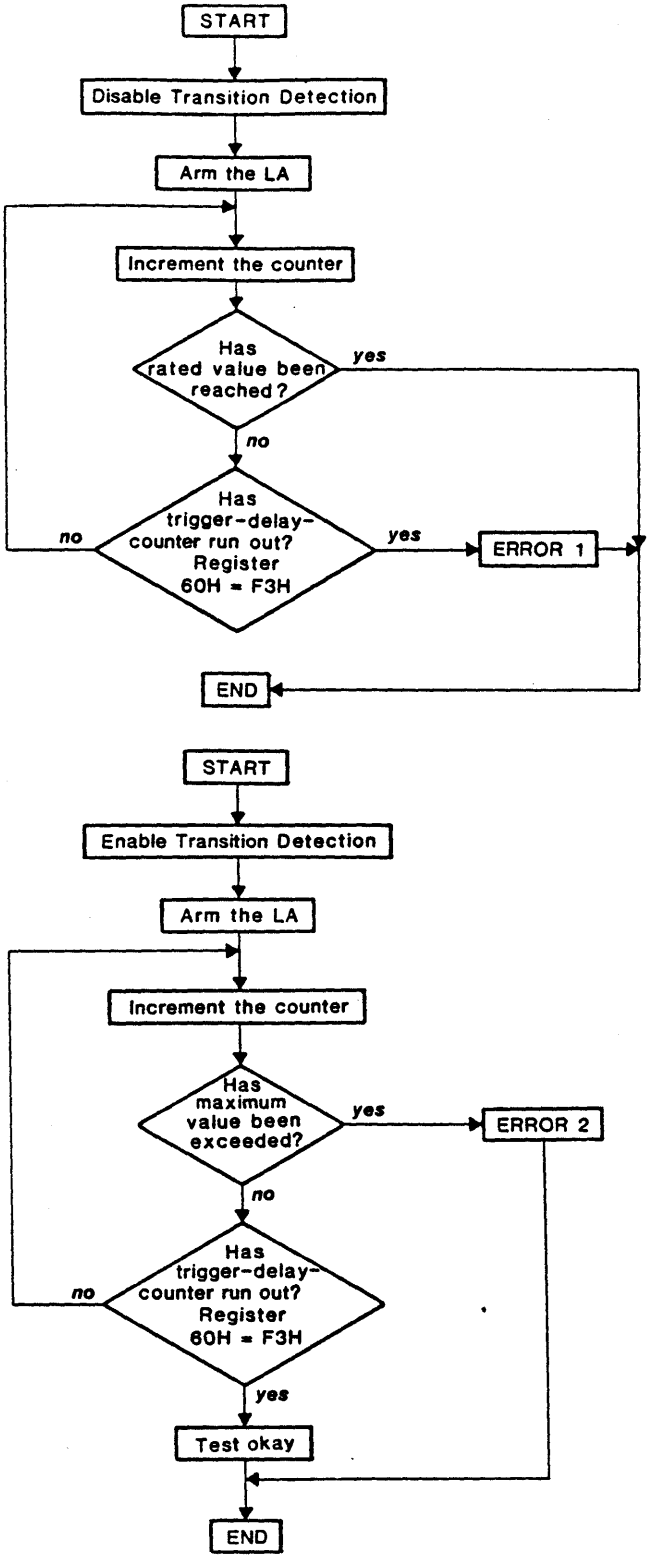

Figure 6-4. TRANS Flowchart

6.4 TRANSITIONAL CLOCKING SIGNAL (TCLK) TEST

Names of the test in the source listing: TRANS
In the Single-Test Menu of the LDP: Transition Tests

Purpose: TRANS determines if the transitional clocking signal (TCLK) is triggered by the DMBs and processed by the SEQ.

Description of errors:

Error 1:
The trigger-delay-counters on the SEQ have run out, although the TRANSITION DETECTION command on the DMBs was disabled. As a result, the transitional clocking signal (TCLK) is permanently active.

Possible causes:

- TCLK short circuit on high.
- Control error in Register 2 on the respective DMB (TRANSITION DETECTION cannot be disabled).

Error message in the program:

"Test of false occurring transitions error"

Error 2:
Trigger-delay-counters on the SEQ did not run out within the maximum time allowed for testing, although TRANSITION DETECTION command on the respective DMB was enabled.

Possible causes:

- If errors occur in all eight tests, the cause for the errors is probably found on the SEQ.

  Example: Conductor TCLK, short circuit on low

- If errors occur only in some of the tests, the cause for the errors is probably found on the respective DMB.

  Example: Control error in Register 2 on the respective DMB

Error message in the program:

"Transitional clocking signal (TCLK) error"

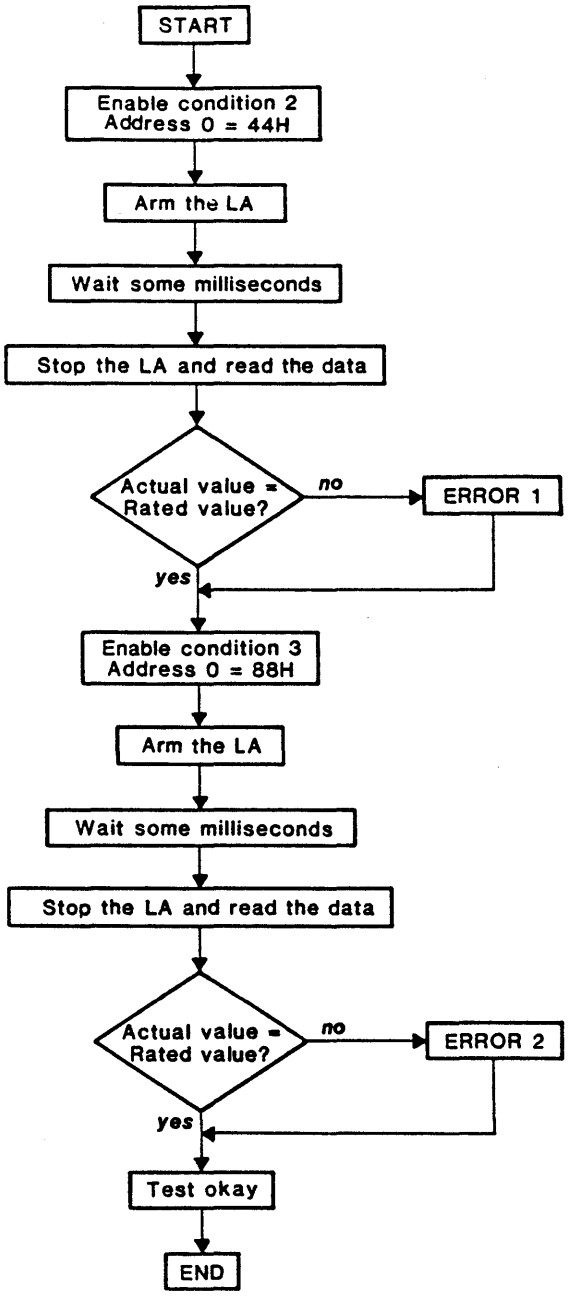

Figure 6-5. DATAQUAL Flowchart

6.5 CONDITIONS 2 AND 3 (DATA QUALIFIED RECORDING) TEST

Name of the test in the source listing: DATAQUAL
In the Single-Test Menu of the LDP: Qualified Recording Test

Purpose: DATAQUAL determines if Conditions 2 and 3 are generated properly by the DMBs and if they are properly processed by the SEQ.

Description of errors:

Error 1:
The data measured does not correspond with the rated values (01, 02, 03, 04, 05, 06, 07, 08, 09, 00, 01, etc.). Condition 2 was set for this data.

Possible cause:

- Errors on the conductor CND2.

Error message in the program:

"Condition 2 error"

Error 2:
The data measured does not correspond with the rated values (01, 02, 03, 04, 05, 06, 07, 08, 09, 00, 01, etc.). Condition 3 was set for this data.

Possible cause:

- Errors on the conductor CND3.

Error message in the program:

"Condition 3 error"

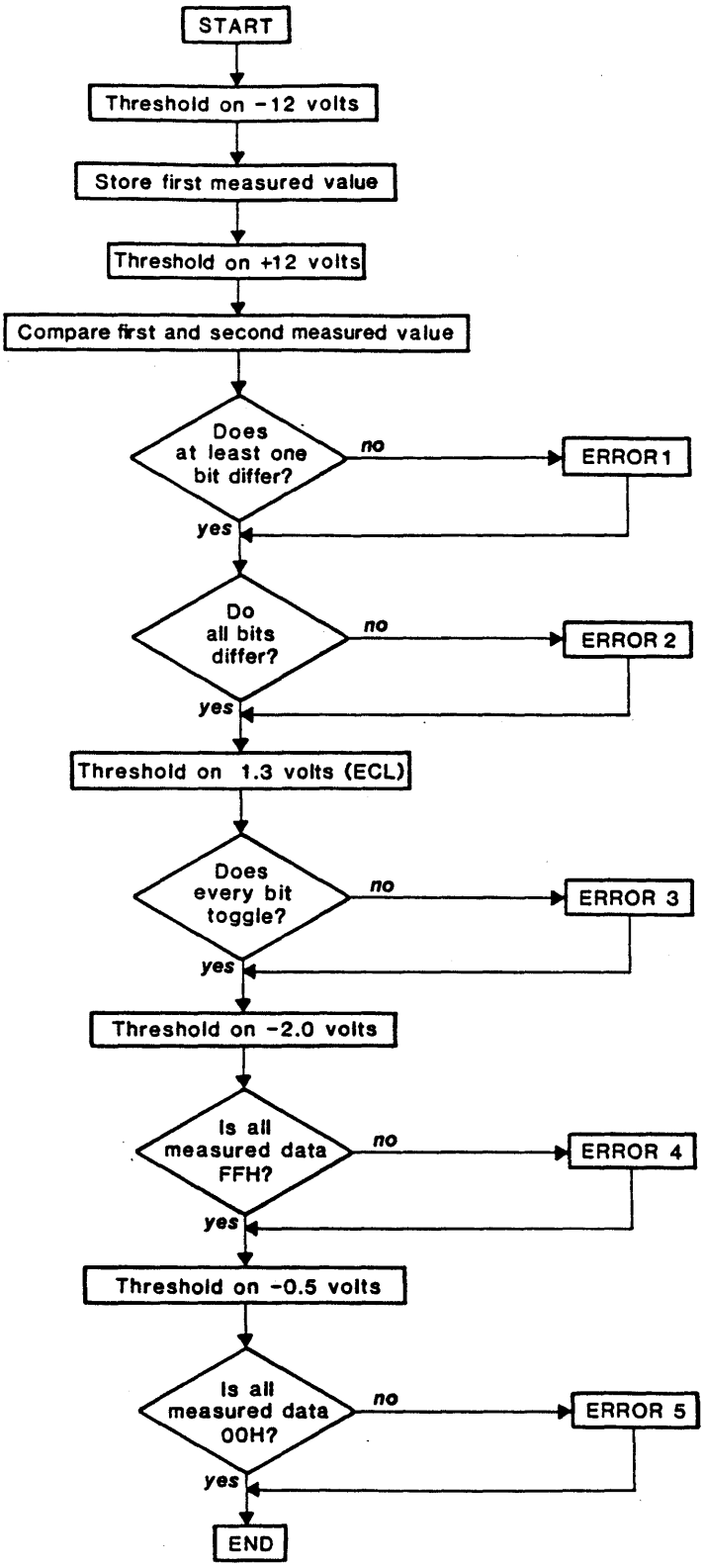

Figure 6-6. PROBETS Flowchart

6.6 PROBE TEST

Name of the test in the source listing: **PROBETS**
In the Single-Test Menu of the LDP: Probe Tests

Purpose: PROBETS determines if all data probes are working properly.

Description of errors:

Error 1:
In the first and second tests results all bits have the same value, although the threshold is adjusted to -12 volts for the first test and to +12 volts for the second test.

Possible causes:

- Errors in the data transfer from the TBQ to the probe.
- Errors in threshold hardware of the probe.

Error 2:
The first and second tests results showed that not all bits differed.

Possible causes:

- Amplifier in the probe is defective.
- ECL compactor in the probe is defective.

Error message in the program for Test 2:

"Test of all channels via changing threshold voltage"
(Error message is indicated separately for each channel.)

Error 3:
Although the threshold is adjusted to -1.3 volts (ECL threshold), some of the bits never alternate their polarity.

Possible causes:

- Test configurator wire or UPR is defective.
- Amplifier in the probe is defective.

Error message in the program for Test 3:

"Test of all channels via ECL input signal"
(Error message is indicated separately for each channel.)

Error 4:
Although the threshold is adjusted to -2.0 volts, not all data was FFH. If Error 3 did not occur, Error 4 indicates an undershoot or a negative offset.

Possible cause:

- Amplifier in the probe is defective or misaligned.

Error message in the program for Test 4:

"Test of overshoot respectively positive offset voltage"
(Error message is indicated separately for each channel.)

Error 5:
Although the threshold is adjusted to -0.5 volts, not all data is 00H. If Error 3 did not occur, Error 5 indicates an overshoot or a positive offset.

Possible cause:

- Amplifier in the probe is defective or misaligned.

Error message in the program for Test 5:

"Test of undershoot respectively negative offset voltage"
(Error message is indicated separately for each channel.)

6.7 DMB INPUTS AND ADDITIONAL DATA RAM TEST

Name of the test in the source listing: **PODTS**
In the Single-Test Menu of the LDP: Input Tests

Purpose: PODTS determines if all memory data on the DMBs supplied by the pattern generator is recorded. Possible addressing errors in the DMB Data RAMs are recognized, because the recorded pattern is induced by a decimal counter.

The pattern generator on the SEQ is tested.

The entire data line (starting from the input buffer up to and including the Data RAM) is tested.

Reasons for negative test results:

- Defective probe
- Pattern generator on the SEQ board is defective
- Test configurator wire or UPR is defective
- Error in the DMB data line
- Data RAM on the DMB is defective

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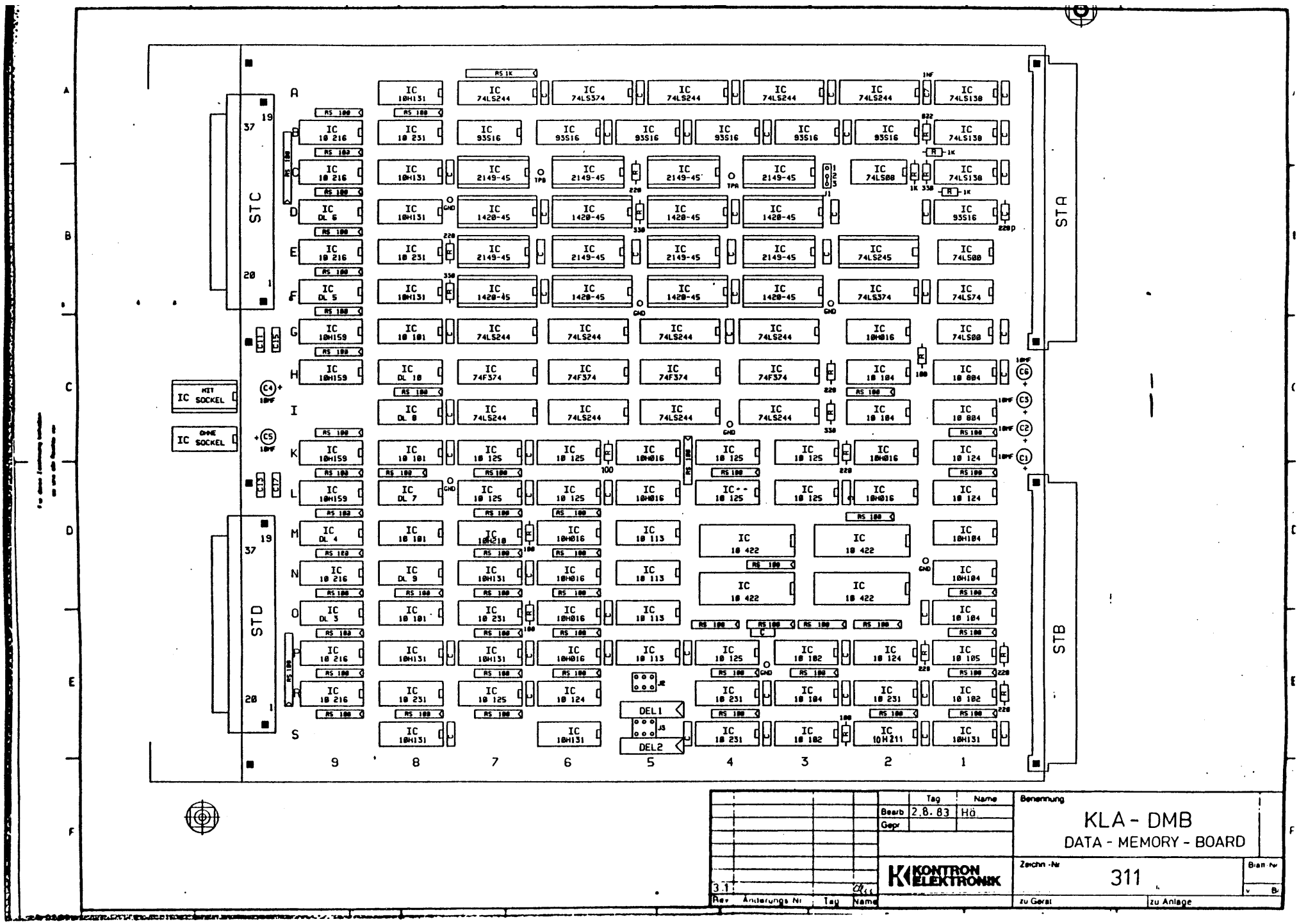
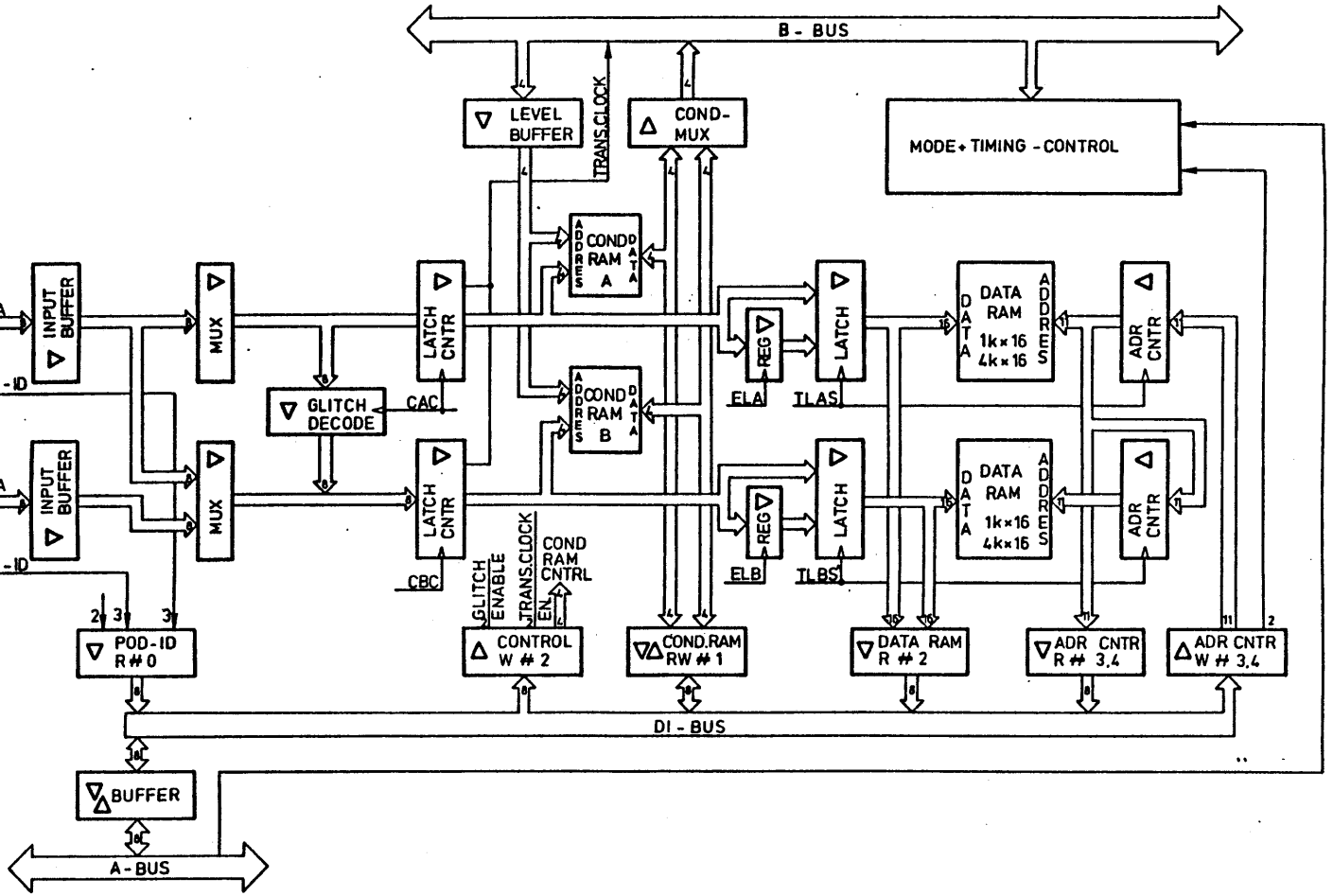


		Tag	Name	Benennung	
	Bearb	2.8.83	Hö	KLA - DMB	
	Gepr			DATA - MEMORY - BOARD	
KONTRON ELEKTRONIK				Zeichn.-Nr	Blatt-Nr
				311	
3.1				zu Gerät	zu Anlage
Rev.	Änderungs Nr.	Tag	Name		



					Tag	Name
				Bearb.	10.7.81	Hänsel
				Gepr.	27.1.82	HÜBNER
3.1						
1.5	152	16.7.82				
1.4	142	23.3.82				
1.2		27.1.82				
Rev.	Änderungs-Nr.	Tag	Name			

KONTRON ELECTRONIC

Benennung

KLA-DMB DATA-MEMORY-BOARD

Zeichn.-Nr. 311

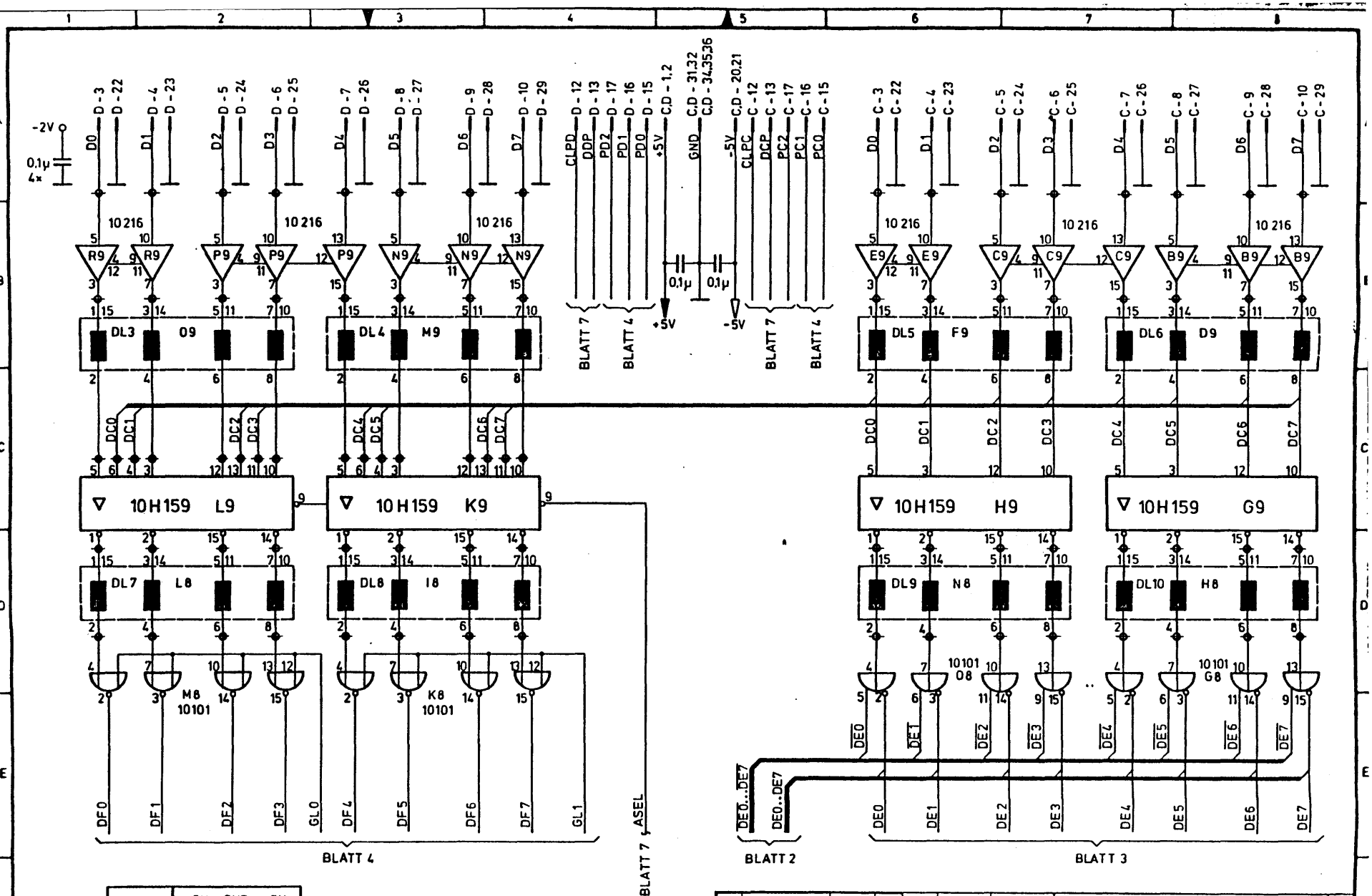
Blatt-Nr

v. Bl

zu Gerät

zu Anlage

EE-07.80



	+5V	GND	-5V
10216	-	1,16	8
10159	-	16	8
10101	-	1,16	8
DL	-	9,12,13,16	-

	Tag	Name
Bearb	20.7.83	Hänsel
Gepr		

KONTRON ELEKTRONIK

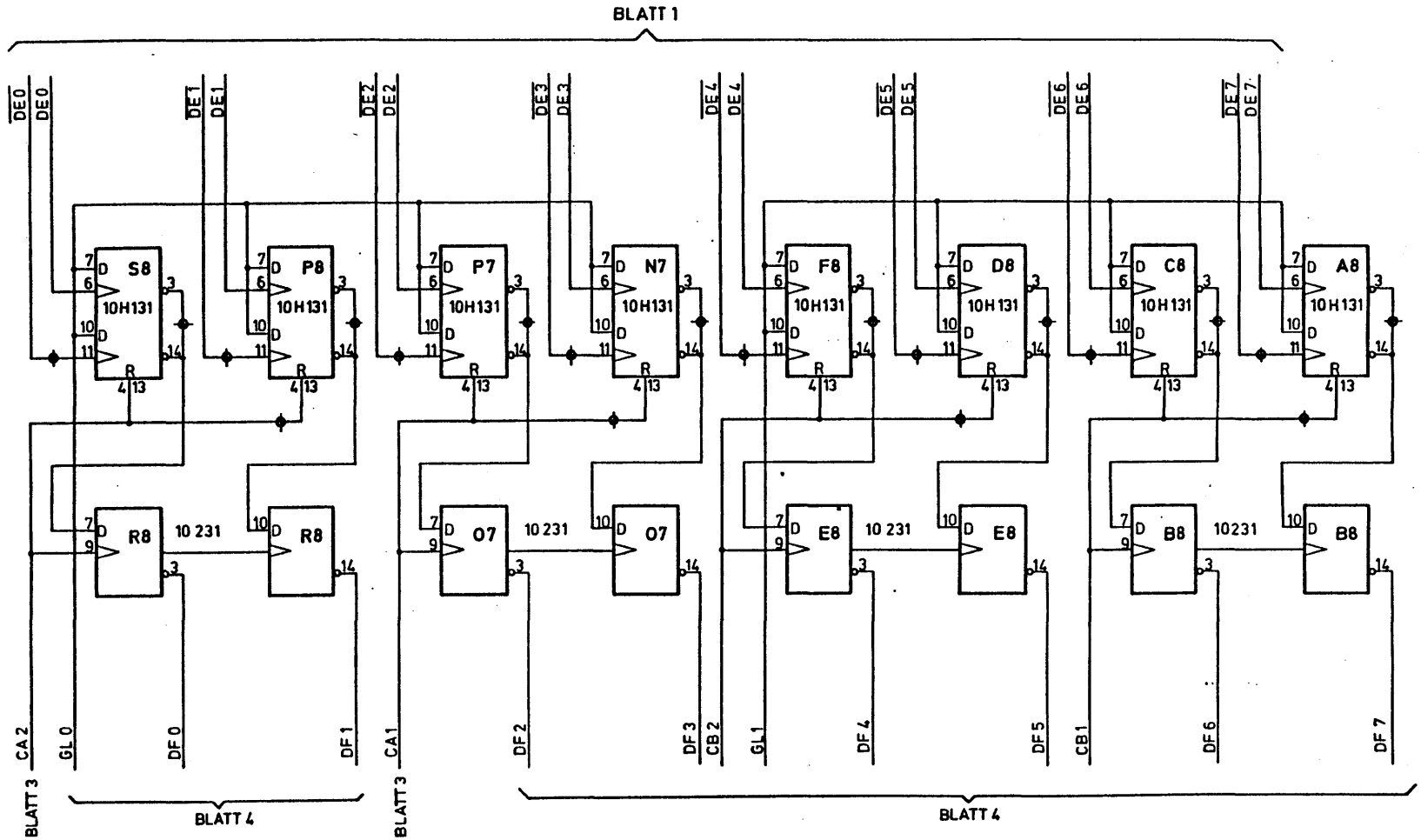
Benennung: KLA - DMB
FRONT - END

Zeichn.-Nr: 311

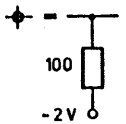
Blatt Nr: 1

3.1 Rev. | Änderungs-Nr. | Tag | Name

zu Gerät | zu Anlage



	+5V	GND	-5V
10 H 131	-	16,1	8
10 231	-	16,1	8



	Tag	Name
Bearb	25.7.83	Hänsel
Gepr		

Benennung: KLA - DMB
GLITCH - LATCH

KONTRON ELEKTRONIK

Zeichn.-Nr: 311

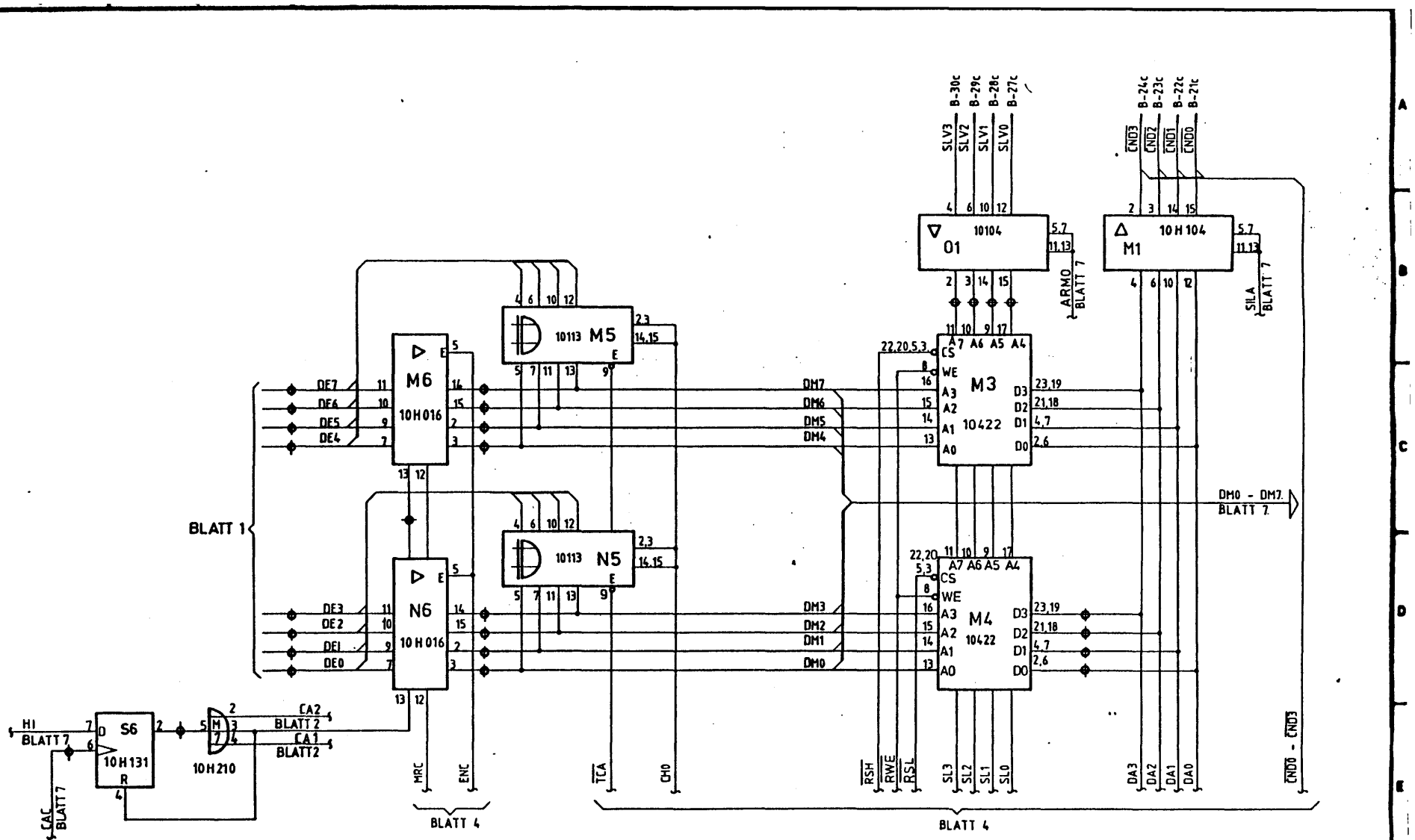
Blatt-Nr: 2 v 7 Bl

3:1

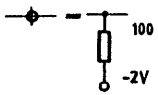
Rev.	Änderungs-Nr.	Tag	Name

zu Gerät

zu Anlage



	GND	-5V
10H016	1,16	8
10H104	1,16	8
10 113	1,16	8
10H131	1,16	8
10 422	1,24	12
10H210	1,16,15	8



Rev.	Änderungs-Nr.	Tag	Name
3.1			Hü
1.5	152	16.7.82	Hü
1.4	142	23.3.82	Hü
1.2		27.1.82	Hü

	Tag	Name
Bearb.	14.5.81	Hänsel
Gepr.	20.1.82	HÜBNER

KONTRON ELECTRONIC

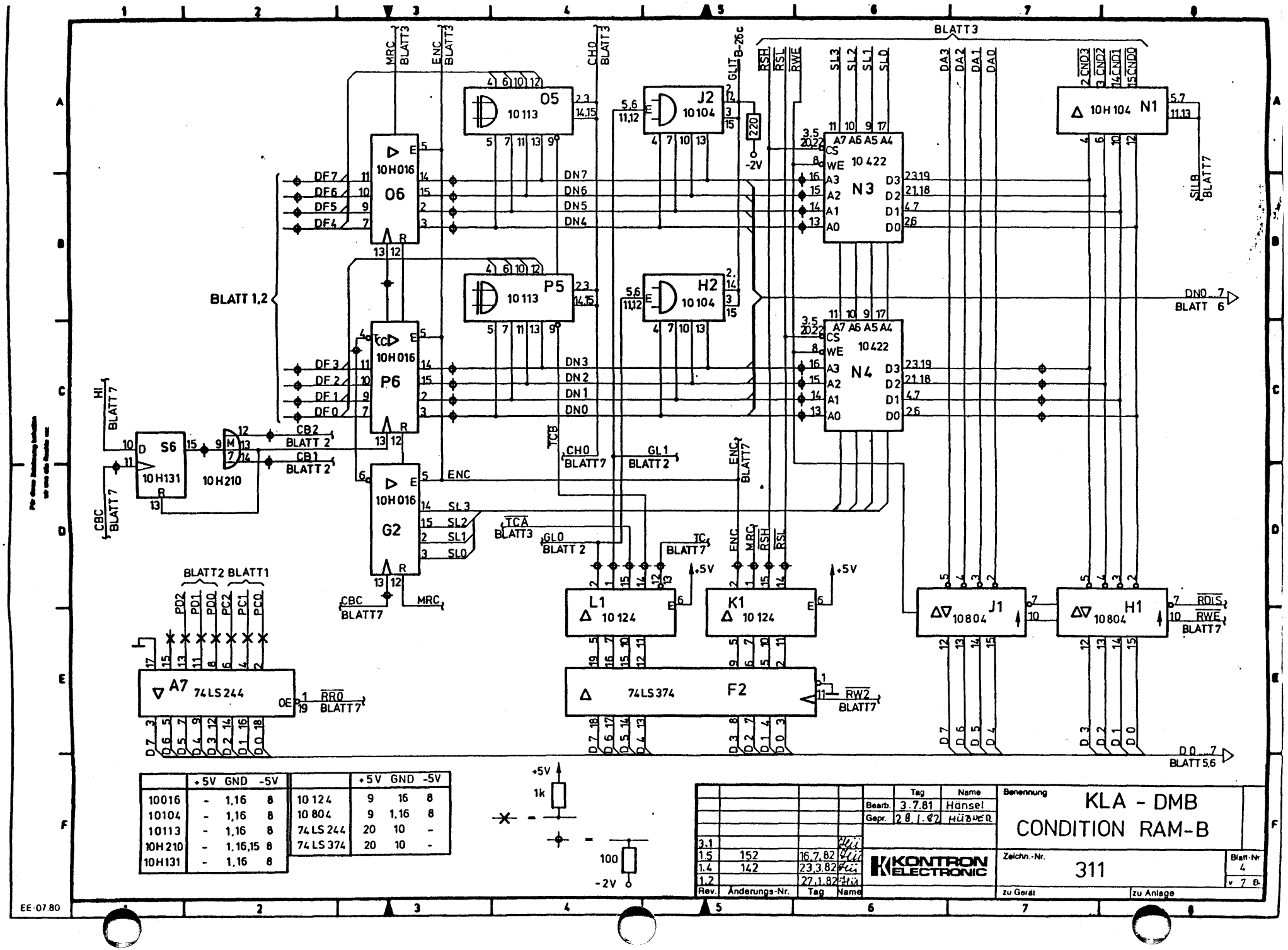
Benennung: KLA - DMB
CONDITION RAM-A

Zeichn.-Nr.: 311

Blatt-Nr. 3 v 7

zu Gerät | zu Anlage

EE-07 80



	+5V	GND	-5V	
10016	-	1,16	8	
10104	-	1,16	8	
10113	-	1,16	8	
10H210	-	1,16,15	8	
10H131	-	1,16	8	

	+5V	GND	-5V
10124	9	16	8
10804	9	1,16	8
74LS244	20	10	-
74LS374	20	10	-

Rev.	Änderungs-Nr.	Tag	Name
3.1			Hii
1.5	152	16.7.82	Hii
1.4	142	23.3.82	Hii
1.2		27.1.82	Hii

	Tag	Name
Bearb.	3.7.81	Hänsel
Gepr.	28.1.82	HÜBNER

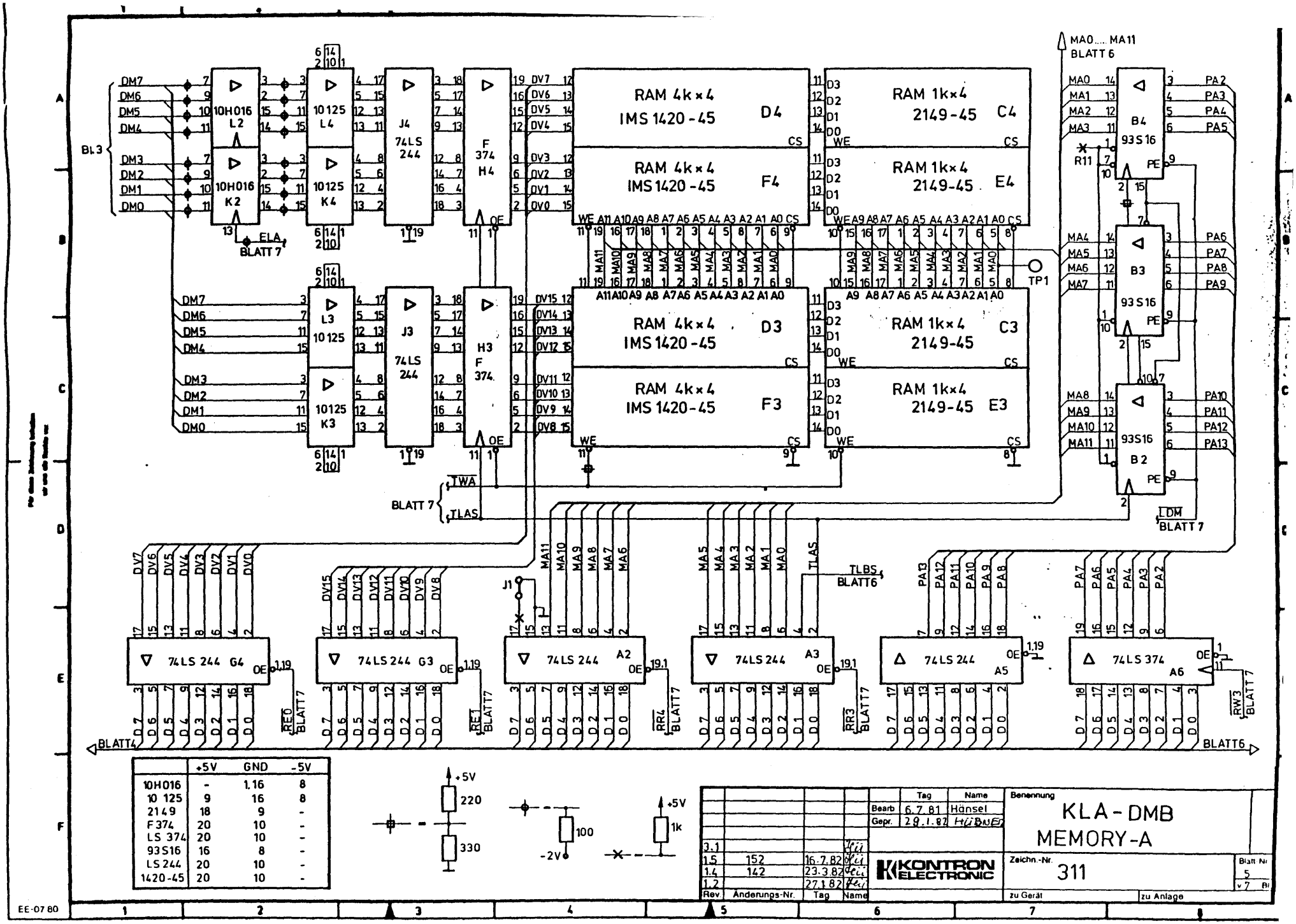
KONTRON ELECTRONIC

Benennung: KLA - DMB
CONDITION RAM-B

Zeichn.-Nr.: 311

Blatt-Nr. 4 v 7 B

zu Gerät | zu Anlage



	+5V	GND	-5V
10H016	-	1.16	8
10 125	9	16	8
2149	18	9	-
F374	20	10	-
LS 374	20	10	-
93S16	16	8	-
LS 244	20	10	-
1420-45	20	10	-

	Tag	Name
Bearb	6.7.81	Hänsel
Gepr.	29.1.82	

Rev.	Änderungs-Nr.	Tag	Name
3.1			
1.5	152	16.7.82	
1.4	142	23.3.82	
1.2		27.1.82	

KONTRON ELECTRONIC

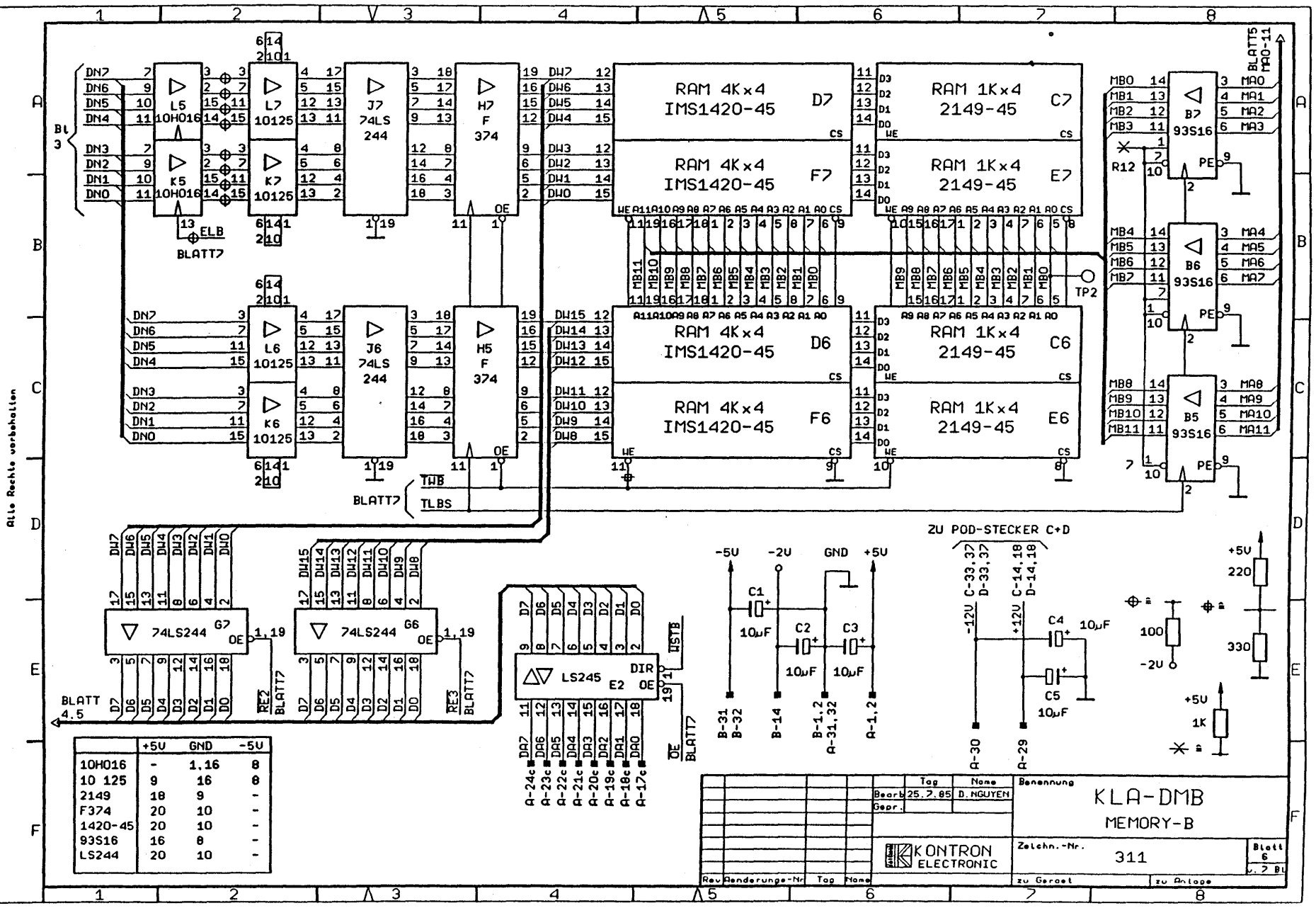
Benennung: KLA-DMB MEMORY-A

Zeichn.-Nr.: 311

Blatt Nr. 5 v 7 Bl

zu Gerät | zu Anlage

EE-07 80



	+5V	GND	-5V
10H016	-	1,16	8
10 125	9	16	8
2149	18	9	-
F374	20	10	-
1420-45	20	10	-
93S16	16	8	-
LS244	20	10	-

	Tag	Name
Bearb	25.7.85	D. NGUYEN
Gepr.		

Benennung: KLA-DMB MEMORY-B

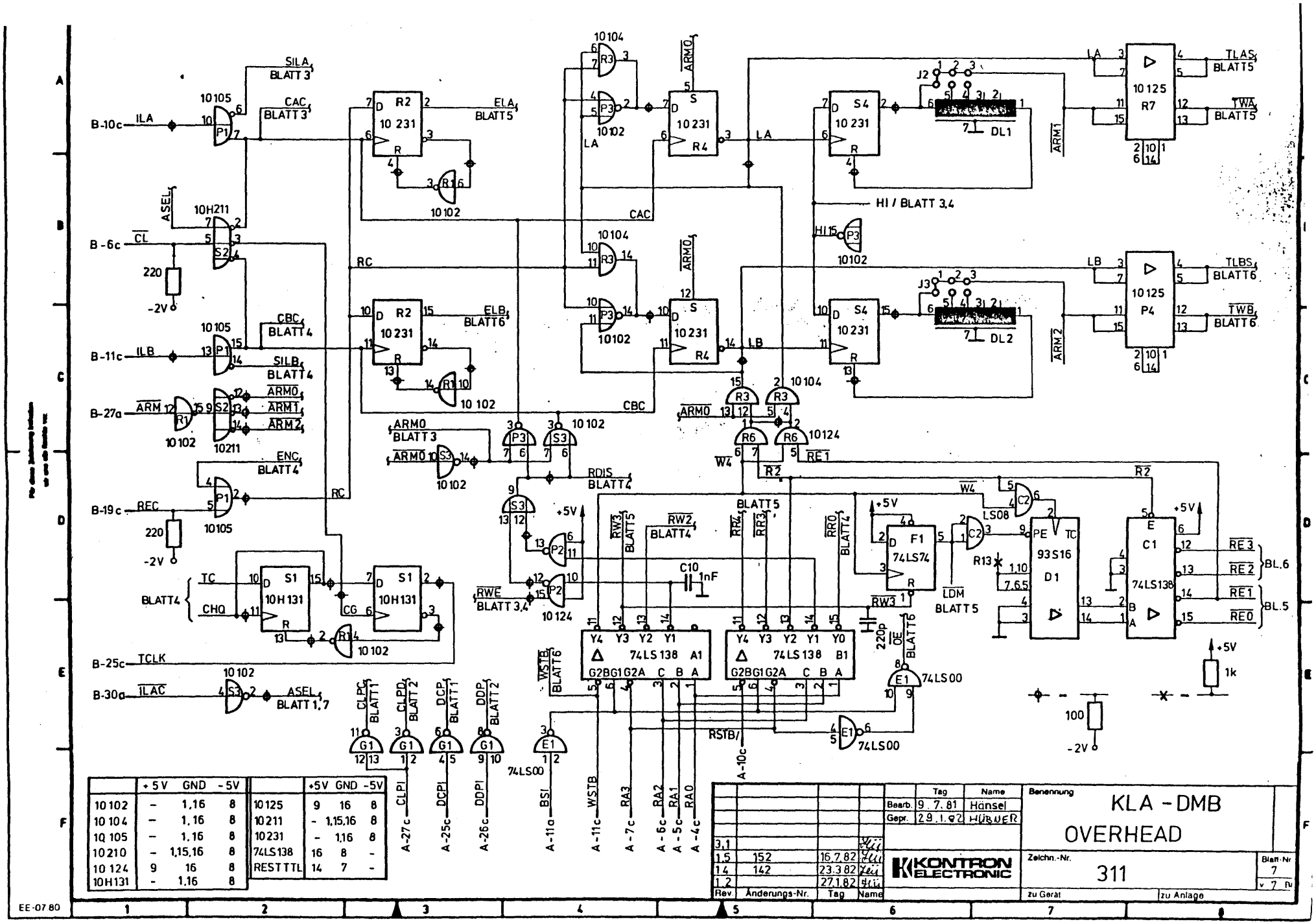
KONTRON ELECTRONIC

Zeichn.-Nr. 311

Blatt 6 v. 7 Bl.

Rev.	Aenderungs-Nr.	Tag	Name

zu Gerael | zu Anlage



	+5V	GND	-5V
10102	-	1,16	8
10104	-	1,16	8
10105	-	1,16	8
10210	-	1,15,16	8
10124	9	16	8
10H131	-	1,16	8

	+5V	GND	-5V
10125	9	16	8
10211	-	1,15,16	8
10231	-	1,16	8
74LS138	16	8	-
RESTTTL	14	7	-

Rev.	Änderungs-Nr.	Tag	Name
3,1			
1,5	152	16.7.82	
1,4	142	23.3.82	
1,2		27.1.82	

	Tag	Name
Bearb.	9.7.81	Hänsel
Gepr.	29.1.82	HÜBNER

KONTRON ELECTRONIC

Benennung: KLA - DMB OVERHEAD

Zeichn.-Nr.: 311

Blatt-Nr.: 7 v 7

zu Gerät | zu Anlage

EE-07 80

LDP MENU INPUT FIELDS

This appendix contains a list of the LDP Main Menu input fields as shown in Figure A-1 and a brief description of each. The Single-Test Menu is illustrated in subsequent pages.

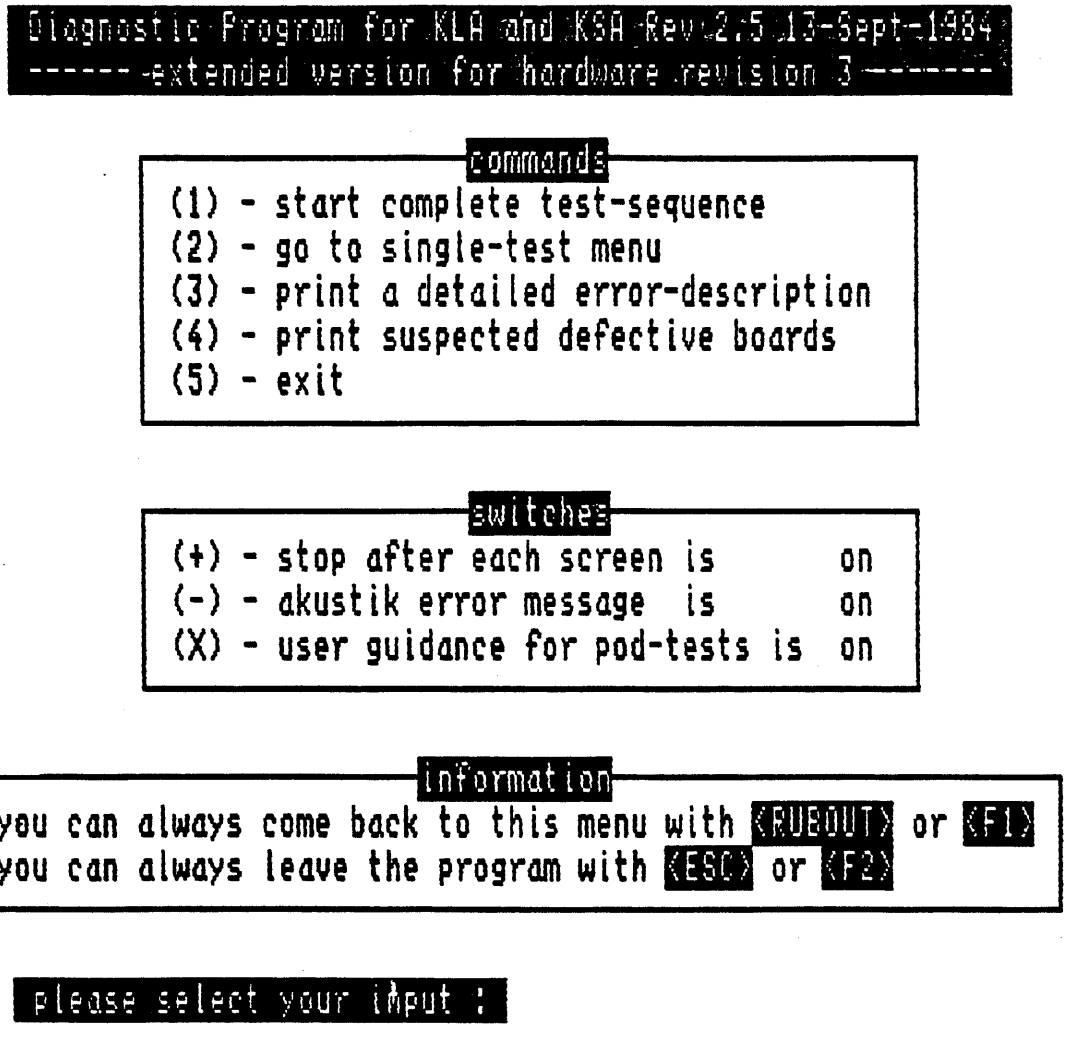


Figure A-1. LDP Main Menu

(1) start complete test-sequence

Runs through all diagnostic tests (see "+" below).

(2) user guidance for pod-test on

Displays backplane diagram, showing unconnected probes as blinking fields. If all probes are connected, this screen does not appear.

(3) go to single-test menu

If you see an error during the first run of diagnostic tests, you can choose to run individual tests. The types of tests are highlighted in reverse video; the list below allows you to select where to run that test. Individual tests are activated with the RUN/STOP key.

(4) print a detailed error-description

Displays final diagnostic test results. You must run the diagnostic tests first in order to get an accurate summary on this screen.

(5) print suspected defective boards

Displays list of suspected defective boards. You must run the diagnostic tests first in order to get an accurate summary on this screen.

(6) exit

Returns you to the Main Menu.

(+) stop after each screen is on

The LA stops after each diagnostic test. If you enter "+" in the input field, this line reads "stop after each screen is off". The LA then runs through all diagnostic tests without stopping.

(-) akustik error message is on

The LA "beeps" at every error. If you enter "-" in the input field, this line reads "akustik error message if off". Then the LA does not "beep" at every error.

The tests in the Single-Test Menu are represented in Figure A-2, which is followed by a list of test names and corresponding page numbers of the sample screen shots.

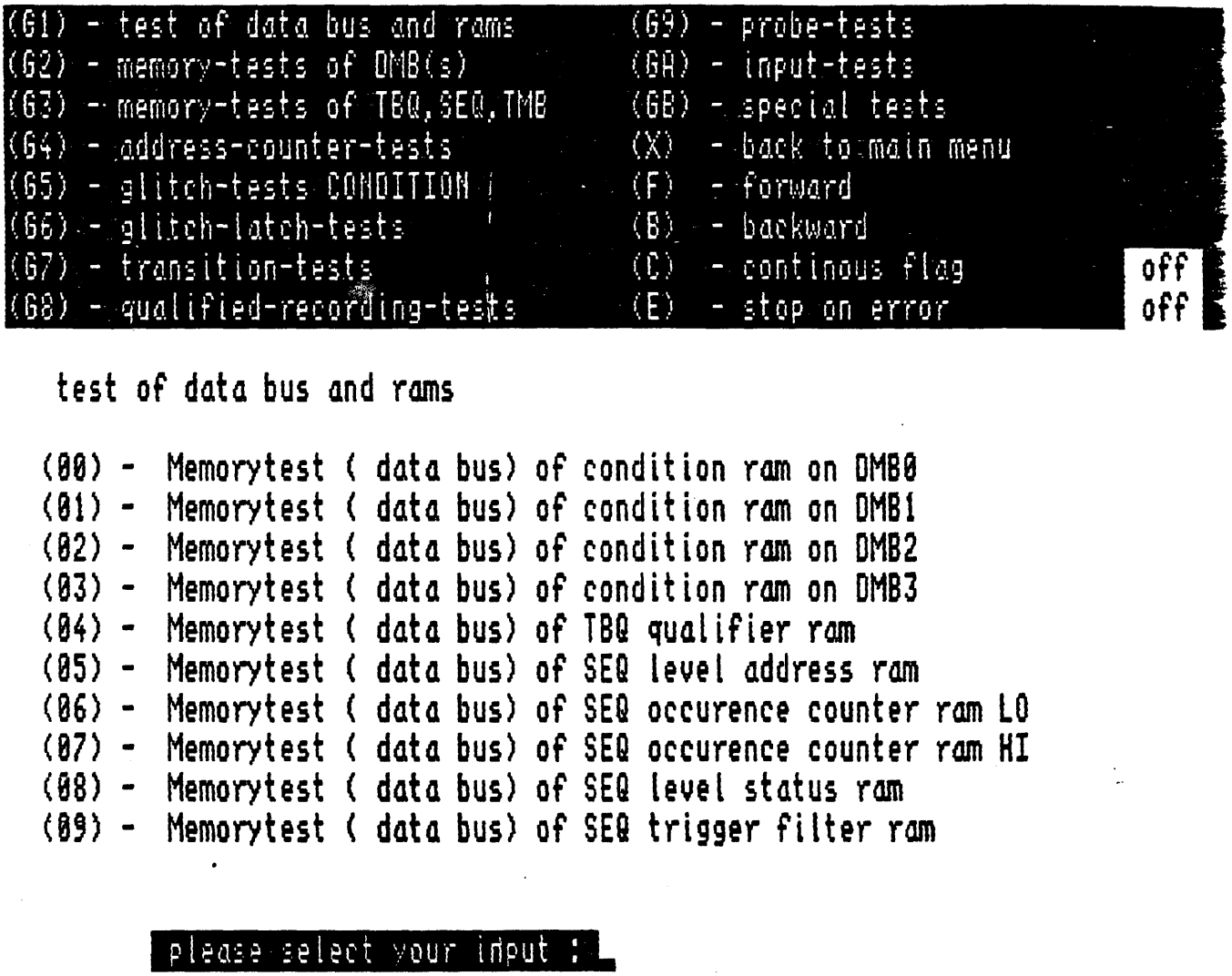


Figure A-2. Single-Test Menu

Board	Specific RAM	Data-test	Address Test
TBQ	Qualifier RAM	ok	ok
TBQ	Qualifier RAM	special Address-test	ok
SEQ	Level Address	ok	ok
SEQ	Occurence CNT	ok	ok
SEQ	Occurence CNT	ok	ok
SEQ	Status	ok	ok
SEQ	Trigger filter	ok	ok
DMB 3	Condition RAM	ok	ok
DMB 3	Data RAM	ok	ok
DMB 2	Condition RAM	ok	ok
DMB 2	Data RAM	ok	ok
DMB 1	Condition RAM	ok	ok
DMB 1	Data RAM	ok	ok
DMB 0	Condition RAM	ok	ok
DMB 0	Data RAM	ok	ok
TMB	Data RAM	ok	

test is in hold, type any key to continue

clock-tests of the TBQ-board

test of the 100ms via slow-clock-detection ok

test is in hold, type any key to continue ■

```
test of the following clocks
via occurence-counter of SEQ

100 MHz =  10 ns   jitter = + 0006 Samples      ok
 50 MHz =  20 ns   jitter = - 0001 Samples      ok
 20 MHz =  50 ns   jitter = - 0001 Samples      ok
 10 MHz = 100 ns   jitter = - 0000 Samples      ok
  1 MHz =   1 us   jitter = + 0001 Samples      ok
100 KHz =  10 us   jitter = + 0001 Samples      ok
 10 KHz = 100 us   jitter = + 0001 Samples      ok
  1 KHz =   1 ms   jitter = - 0000 Samples      ok
100  Hz =  10 ms   jitter = - 0000 Samples      ok
 10  Hz = 100 ms   jitter = - 0000 Samples      ok


     test is in hold, type any key to continue ■
```

```
probe-identifikation for  Connector C  (PROBE J)  ok
slow-clock-detection for  Connector C  (PROBE J)  ok


test is in hold, type any key to continue
```

```
probe-identifikation for  Connector D  (PROBE K)  ok
slow-clock-detection for  Connector D  (PROBE K)  ok
```

```
test is in hold, type any key to continue ■
```

Qualfier input test of pod J ok

(also runs QUALIFIER INPUT TEST OF POD K)

test is in hold, type any key to continue ■

```
level-increment-test

100 MHz =  10 ns   jitter = + 0000 Samples  ok
 50 MHz =  20 ns   jitter = + 0000 Samples  ok
 20 MHz =  50 ns   jitter = + 0000 Samples  ok
 10 MHz = 100 ns   jitter = + 0000 Samples  ok
```

test is in hold, type any key to continue

```
trigger-delay-counter-test

50 MHz =  20 ns          Trigger-delay-counter 0  ok
                         Trigger-delay-counter 1  ok
                         Trigger-delay-counter 2  ok
                         Trigger-delay-counter 3  ok

10 MHz = 100 ns          Trigger-delay-counter 0  ok
                         Trigger-delay-counter 1  ok
                         Trigger-delay-counter 2  ok
                         Trigger-delay-counter 3  ok

 1 MHz =   1 us          Trigger-delay-counter 0  ok
                         Trigger-delay-counter 1  ok
                         Trigger-delay-counter 2  ok
                         Trigger-delay-counter 3  ok

100 KHz =  10 us         Trigger-delay-counter 0  ok
                         Trigger-delay-counter 1  ok
                         Trigger-delay-counter 2  ok
                         Trigger-delay-counter 3  ok

      test is in hold, type any key to continue ■
```

```
Test of trigger filter 0 on SEQ (via condition 0)

last level was reached  in time jitter = + 0000 Samples  ok




test is in hold, type any key to continue
```

```
Test of trigger filter 1 on SEQ (via condition 1)
last level was reached  in time jitter = + 0000 Samples  ok


test is in hold, type any key to continue ■
```

Test of GLA on DMB0 via condition GLIT on SEQ

condition GLITCH ok

(also runs Test of GLB on DMB0 via condition GLIT on SEQ

Test of GLA on DMB1 via condition GLIT on SEQ

Test of GLB on DMB1 via condition GLIT on SEQ

Test of GLA on DMB2 via condition GLIT on SEQ

Test of GLB on DMB2 via condition GLIT on SEQ

Test of GLA on DMB3 via condition GLIT on SEQ

Test of GLB on DMB3 via condition GLIT on SEQ)

test is in hold, type any key to continue ■

```
glitch-latch-test of pod 1

test of false occurring glitches      test of missing glitches

Glitch-latch 01  ok                   Glitch-latch 01  ok
Glitch-latch 03  ok                   Glitch-latch 03  ok
Glitch-latch 05  ok                   Glitch-latch 05  ok
Glitch-latch 07  ok                   Glitch-latch 07  ok
```

(also runs glitch-latch-test of pods 2 - 8)

```
test is in hold, type any key to continue ■
```

test of false occurring transitions ok

test is in hold, type any key to continue ■

transition recording test of pod 1

Transitional clocking signal (TCLK) ok

(also runs transition recording test of pods 2 - 8)

test is in hold, type any key to continue

data qualified recording test pod 1 ok

(also runs data qualified recording test of pods 2 - 8)

test is in hold, type any key to continue

Test of interlace clocks ILA1.ILB1,ILA2,ILB2,(ILAC)

ILA1 ok
ILB1 ok
ILA2 ok
ILB2 ok

test is in hold, type any key to continue

```
Probe-test probe 1

Test 1 : Threshold hardware or all Inputs on Probe or DMB  ok
Test 2 : Test of all channels via changing Threshold voltage(no input nece
Test 3 : Test of all channels via ECL-input-signal (Threshold is fix)
Test 4 : Test of overshoot respectively positive offset voltage
Test 5 : Test of undershoot respectively negative offset voltage

             Test 2 :      Test 3 :      Test 4 :      Test 5 :

Channel 00   ok            ok            ok            ok
Channel 01   ok            ok            ok            ok
Channel 02   ok            ok            ok            ok
Channel 03   ok            ok            ok            ok
Channel 04   ok            ok            ok            ok
Channel 05   ok            ok            ok            ok
Channel 06   ok            ok            ok            ok
Channel 07   ok            ok            ok            ok

        test is in hold, type any key to continue
```

(also runs probe-test on pods 2 - 8)

Probe-test probe 1 ok

(also runs probe-test probe 2 - 8)

test is in hold, type any key to continue

board(s) suspected to be defective :

No defective board detected

Press RETURN or RUN/STOP to continue

APPENDIX B

LDP TEST FAILURES

This appendix describes the possible board-specific LDP test failures and includes sample screen shots.

Simulated error on: TBQ board

Possible errors detected in the following tests:

Data test, address test

Test of the following clocks via occurrence counter on SEQ

Probe identification for connector D (probe K)

Qualifier input test of pod K

Level increment test

Trigger-delay-counter test

Transition recording test of pods 1-8

Boards(s) suspected to be defective:

TBQ - Time Base and Clock Qualifier

SEQ - Trigger Sequencer Controller

DMB0 - Data Memory Board 0

DMB1 - Data Memory Board 1

DMB2 - Data Memory Board 2

DMB3 - Data Memory Board 3

Suggested correction: TBQ board replacement

Board	Specific RAM	Data-test	Address-test
TBQ	Qualifier RAM	error	error
TBQ	Qualifier RAM	special Address-test	error
SEQ	Level Address	ok	ok
SEQ	Occurence CNT	ok	ok
SEQ	Occurence CNT	ok	ok
SEQ	Status	ok	ok
SEQ	Trigger filter	ok	ok
DMB 3	Condition RAM	ok	ok
DMB 3	Data RAM	ok	ok
DMB 2	Condition RAM	ok	ok
DMB 2	Data RAM	ok	ok
DMB 1	Condition RAM	ok	ok
DMB 1	Data RAM	ok	ok
DMB 0	Condition RAM	ok	ok
DMB 0	Data RAM	ok	ok
TMB	Data RAM	ok	

test is in hold, type any key to continue

test of the following clocks
via occurence-counter of SEQ

100 MHz = 10 ns	jitter = + 0006 Samples	ok
50 MHz = 20 ns	jitter = + 19E3 Samples	*too fast*
20 MHz = 50 ns	jitter = - 0001 Samples	ok
10 MHz = 100 ns	jitter = - 0000 Samples	ok
1 MHz = 1 us	jitter = - 0000 Samples	ok
100 KHz = 10 us	jitter = + 0002 Samples	ok
10 KHz = 100 us	jitter = + 0001 Samples	ok
1 KHz = 1 ms	jitter = - 0000 Samples	ok
100 Hz = 10 ms	jitter = - 0000 Samples	ok
10 Hz = 100 ms	jitter = - 0001 Samples	ok

test is in hold, type any key to continue ■

```
probe-identifikation for  Connector D  (PROBE K)  ok
slow-clock-detection for  Connector D  (PROBE K)  error

test is in hold, type any key to continue
```

```
Qualfier input test of pod K                    error

        Qualifier input 00  error
        Qualifier input 01  error
        Qualifier input 02  error
        Qualifier input 03  error
        Qualifier input 04  error
        Qualifier input 05  error


test is in hold, type any key to continue ■
```

```
level-increment-test

100 MHz =  10 ns   jitter = + 0000 Samples  ok
 50 MHz =  20 ns   jitter = - 00A1 Samples  too fast
 20 MHz =  50 ns   jitter = + 0000 Samples  ok
 10 MHz = 100 ns   jitter = + 0000 Samples  ok
```

test is in hold, type any key to continue ■

```
   trigger-delay-counter-test

50 MHz =  20 ns          Trigger-delay-counter 0 too early
                         Trigger-delay-counter 1 too early
                         Trigger-delay-counter 2 too early
                         Trigger-delay-counter 3 too early

10 MHz = 100 ns          Trigger-delay-counter 0  ok
                         Trigger-delay-counter 1  ok
                         Trigger-delay-counter 2  ok
                         Trigger-delay-counter 3  ok

 1 MHz =   1 us          Trigger-delay-counter 0  ok
                         Trigger-delay-counter 1  ok
                         Trigger-delay-counter 2  ok
                         Trigger-delay-counter 3  ok

100 KHz =  10 us         Trigger-delay-counter 0  ok
                         Trigger-delay-counter 1  ok
                         Trigger-delay-counter 2  ok
                         Trigger-delay-counter 3  ok
probably error on preset lines
        test is in hold, type any key to continue
```

transition recording test of pod 1

Transitional clocking signal (TCLK) error

test is in hold, type any key to continue ■

board(s) suspected to be defective :

TBQ time-base and qualifier board
SEQ sequence and control board
DMB0 data-memory-board 0
DMB1 data-memory-board 1
DMB2 data-memory-board 2
DMB3 data-memory-board 3

Press RETURN or RUN/STOP to continue

Simulated error on: SEQ board

Possible errors detected in the following tests:

Data test, address test

Test of the following clocks via occurrence counter on SEQ

Level increment test

Trigger-delay-counter test

Test of trigger filter 0 on SEQ (via condition 0)

Test of trigger filter 1 on SEQ (via condition 1)

Test of GLA and GLB on DMB0 via condition GLIT on SEQ

Data qualified recording test of pods 1-8

Boards(s) suspected to be defective:

TBQ - Time Base and Clock Qualifier

SEQ - Trigger Sequencer Controller

DMB0 - Data Memory Board 0

DMB1 - Data Memory Board 1

DMB2 - Data Memory Board 2

DMB3 - Data Memory Board 3

Suggested correction: SEQ board replacement

Board	Specific RAM	Data-test	Address Test
TBQ	Qualifier RAM	ok	ok
TBQ	Qualifier RAM	special Address-test	ok
SEQ	Level Address	error	error
SEQ	Occurence CNT	error	error
SEQ	Occurence CNT	error	error
SEQ	Status	error	error
SEQ	Trigger filter	error	error
DMB 3	Condition RAM	ok	ok
DMB 3	Data RAM	ok	ok
DMB 2	Condition RAM	ok	ok
DMB 2	Data RAM	ok	ok
DMB 1	Condition RAM	ok	ok
DMB 1	Data RAM	ok	ok
DMB 0	Condition RAM	ok	ok
DMB 0	Data RAM	ok	ok
TMB	Data RAM	ok	

test is in hold, type any key to continue ■

```
test of the following clocks
via occurence-counter of SEQ

100 MHz =  10 ns   jitter = - 01FD Samples     too slow
 50 MHz =  20 ns   jitter = - 0000 Samples     ok
 20 MHz =  50 ns   jitter = - 0201 Samples     too slow
 10 MHz = 100 ns   jitter = - 0000 Samples     ok
  1 MHz =   1 us   jitter = + 0001 Samples     ok
100 KHz =  10 us   jitter = - 0001 Samples     ok
 10 KHz = 100 us   jitter = - 0001 Samples     ok
  1 KHz =   1 ms   jitter = - 0200 Samples     too slow
100  Hz =  10 ms   jitter = - 0000 Samples     ok
 10  Hz = 100 ms   jitter = - 0003 Samples     ok

     test is in hold, type any key to continue
```

level-increment-test

```
100 MHz =  10 ns   jitter = - 008C Samples too fast
 50 MHz =  20 ns   jitter = - 0118 Samples too fast
 20 MHz =  50 ns   jitter = - 02BA Samples too fast
 10 MHz = 100 ns   jitter = - 0575 Samples too fast
```

test is in hold, type any key to continue

```
   trigger-delay-counter-test

50 MHz =  20 ns          Trigger-delay-counter 0 too late
                         Trigger-delay-counter 1 too late
                         Trigger-delay-counter 2 too late
                         Trigger-delay-counter 3 too late

10 MHz = 100 ns          Trigger-delay-counter 0 too late
                         Trigger-delay-counter 1 too late
                         Trigger-delay-counter 2 too late
                         Trigger-delay-counter 3 too late

 1 MHz =   1 us          Trigger-delay-counter 0 too late
                         Trigger-delay-counter 1 too late
                         Trigger-delay-counter 2 too late
                         Trigger-delay-counter 3 too late

100 KHz =  10 us         Trigger-delay-counter 0 too late
                         Trigger-delay-counter 1 too late
                         Trigger-delay-counter 2 too late
                         Trigger-delay-counter 3 too late
probably error on preset lines
         test is in hold, type any key to continue
```

Test of trigger filter 0 on SEQ (via condition 0)

last level was not reached jitter = - 0001 Samples error

test is in hold, type any key to continue ■

Test of trigger filter 1 on SEQ (via condition 1)

last level was not reached jitter = - 0001 Samples error

test is in hold, type any key to continue ■

Test of GLA on DMB0 via condition GLIT on SEQ

condition GLITCH [redacted]

condition GLICHT is missing

test is in hold, type any key to continue ■

Test of GLB on DMB0 via condition GLIT on SEQ

condition GLITCH error

condition GLICHT is missing

test is in hold, type any key to continue ■

data qualified recording test pod 1 errors

Condition 2 errors

Condition 3 errors

test is in hold, type any key to continue ■

```
board(s) suspected to be defective :


TBQ  time-base and qualifier board
SEQ  sequence and control board
DMB0 data-memory-board 0
DMB1 data-memory-board 1
DMB2 data-memory-board 2
DMB3 data-memory-board 3
TMB  time-measurement-board
```

Press RETURN or RUN/STOP to continue

Simulated error on: DMB0 board*

Possible errors detected in the following tests:

Data test, address test

Data qualified recording test of pod 1

Probe test probe 1

Boards(s) suspected to be defective:

DMB0 - Data Memory Board 0

Suggested correction: DMB0 board replacement

* All four DMBs (DMB0 to DMB3) are identical and therefore interchangeable. The eight pods or probes, which are also interchangeable, are divided among these four boards in the following arrangement:

DMB0 = pods 1 and 2
DMB1 = pods 3 and 4
DMB2 = pods 5 and 6
DMB3 = pods 7 and 8

```
Board  Specific RAM      Data-test                    Address-test
-------------------------------------------------------------------
TBQ    Qualifier RAM     ok                           ok
TBQ    Qualifier RAM        special Address-test      ok
SEQ    Level Address     ok                           ok
SEQ    Occurence CNT     ok                           ok
SEQ    Occurence CNT     ok                           ok
SEQ    Status            ok                           ok
SEQ    Trigger filter    ok                           ok

DMB 3  Condition RAM     ok                           ok
DMB 3  Data RAM          ok                           ok
DMB 2  Condition RAM     ok                           ok
DMB 2  Data RAM          ok                           ok
DMB 1  Condition RAM     ok                           ok
DMB 1  Data RAM          ok                           ok
DMB 0  Condition RAM     ok                           ok
DMB 0  Data RAM          error!                       ok

TMB    Data RAM          ok

      test is in hold, type any key to continue
```

data qualified recording test pod 1 *error*

Condition 2 *error*

Condition 3 *error*

test is in hold, type any key to continue

```
 Probe-test probe 1                    error
Error on Address :  0004
```

test is in hold, type any key to continue ■

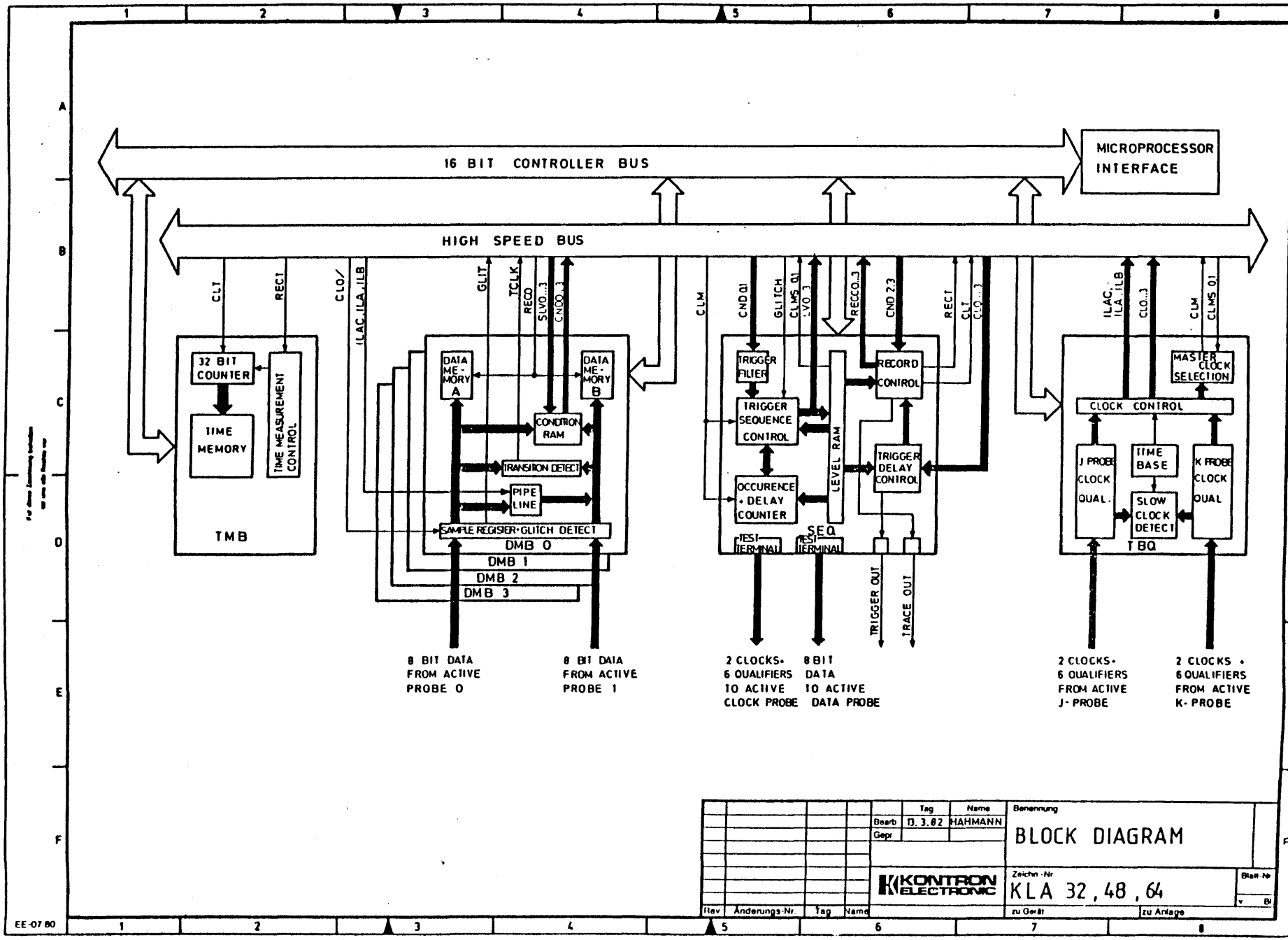
board(s) suspected to be defective :

DMB0 data-memory-board 0

Press -RETURN- or -RUN/STOP- to continue _

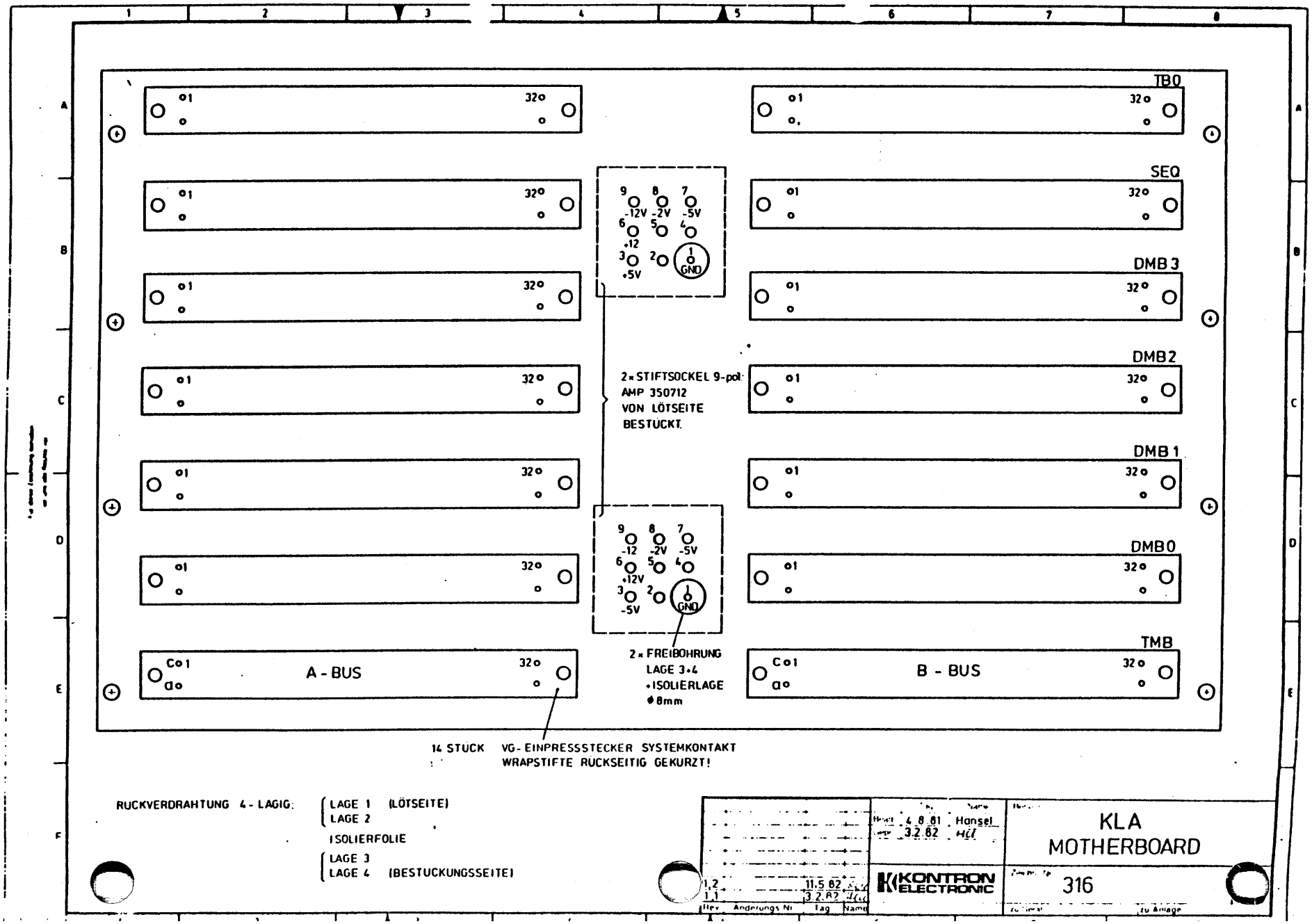
ADDITIONAL SCHEMATICS

Note: These schematics are duplicates of those found in the Service Manual: Kontron LA, Volume 1 and the Kontron Logic Analyzer Series III Operations manual; they are provided here for easy reference.



	Tag	Name	Benennung
Bearb	13.3.82	HAHMANN	BLOCK DIAGRAM
Gepr			
KONTRON ELECTRONIC			Zeichn.-Nr: KLA 32, 48, 64
Rev	Änderungs-Nr.	Tag	Name

EE-07 80


TB0
SEQ
DMB 3
DMB2
DMB 1
DMB0
TMB
A - BUS
B - BUS
2 x STIFTSOCKEL 9-pol
AMP 350712
VON LÖTSEITE
BESTÜCKT
2 x FREIBOHRUNG
LAGE 3+4
+ISOLIERLAGE
ø 8mm
14 STUCK VG-EINPRESSSTECKER SYSTEMKONTAKT
WRAPSTIFTE RÜCKSEITIG GEKÜRZT!
RÜCKVERDRAHTUNG 4-LAGIG:
LAGE 1 (LÖTSEITE)
LAGE 2
ISOLIERFOLIE
LAGE 3
LAGE 4 (BESTÜCKUNGSSEITE)
KONTRON ELECTRONIC
KLA
MOTHERBOARD
316

A-BUS (TTL)

TBQ

C		A
+5V	1	+5V
+5V	2	+5V
	3	
RA0	4	BS0/
RA1	5	BS1/
RA2	6	BS2/
RA3	7	BS3/
RA3/	8	BS4/
	9	BS5/
RSTB/	10	BS6/
WSTB/	11	
	12	GND
	13	GND
	14	GND
	15	GND
TRG	16	GND
DA0	17	GND
DA1	18	GND
DA2	19	GND
DA3	20	GND
DA4	21	GND
DA5	22	GND
DA6	23	GND
DA7	24	GND
	25	GND
	26	GND
CLP/	27	GND
	28	GND
+12V	29	+12V
-12V	30	-12V
GND	31	GND
GND	32	GND

SEQ

C		A
+5V	1	+5V
+5V	2	+5V
	3	
RA0	4	
RA1	5	
RA2	6	
RA3	7	
RA3/	8	
	9	
RSTB/	10	
WSTB/	11	BS0/
	12	GND
	13	GND
	14	GND
	15	GND
TRG	16	GND
DA0	17	GND
DA1	18	GND
DA2	19	GND
DA3	20	GND
DA4	21	GND
DA5	22	GND
DA6	23	GND
DA7	24	GND
	25	GND
	26	GND
	27	GND
	28	GND
	29	
	30	
GND	31	GND
GND	32	GND

DMB 3

C		A
+5V	1	+5V
+5V	2	+5V
	3	
RA0	4	
RA1	5	
RA2	6	
RA3	7	
RA3/	8	
	9	
RSTB/	10	
WSTB/	11	BS3/
	12	GND
	13	GND
	14	GND
	15	GND
TRG	16	GND
DA0	17	GND
DA1	18	GND
DA2	19	GND
DA3	20	GND
DA4	21	GND
DA5	22	GND
DA6	23	GND
DA7	24	GND
DA6	25	GND
DA7	26	GND
CLP/	27	GND
	28	GND
+12V	29	+12V
-12V	30	-12V
GND	31	GND
GND	32	GND

DMB 2

C		A
+5V	1	+5V
+5V	2	+5V
	3	
RA0	4	
RA1	5	
RA2	6	
RA3	7	
RA3/	8	
	9	
RSTB/	10	
WSTB/	11	BS2/
	12	GND
	13	GND
	14	GND
	15	GND
TRG	16	GND
DA0	17	GND
DA1	18	GND
DA2	19	GND
DA3	20	GND
DA4	21	GND
DA5	22	GND
DA6	23	GND
DA7	24	GND
DA6	25	GND
DA5	26	GND
CLP/	27	GND
	28	GND
+12V	29	+12V
-12V	30	-12V
GND	31	GND
GND	32	GND

DMB 1

C		A
+5V	1	+5V
+5V	2	+5V
	3	
RA0	4	
RA1	5	
RA2	6	
RA3	7	
RA3/	8	
	9	
RSTB/	10	
WSTB/	11	BS1/
	12	GND
	13	GND
	14	GND
	15	GND
TRG	16	GND
DA0	17	GND
DA1	18	GND
DA2	19	GND
DA3	20	GND
DA4	21	GND
DA5	22	GND
DA6	23	GND
DA7	24	GND
DA2	25	GND
DA3	26	GND
CLP/	27	GND
	28	GND
+12V	29	+12V
-12V	30	-12V
GND	31	GND
GND	32	GND

DMB 0

C		A
+5V	1	+5V
+5V	2	+5V
	3	
RA0	4	
RA1	5	
RA2	6	
RA3	7	
RA3/	8	
	9	
RSTB/	10	
WSTB/	11	BS0/
	12	GND
	13	GND
	14	GND
	15	GND
TRG	16	GND
DA0	17	GND
DA1	18	GND
DA2	19	GND
DA3	20	GND
DA4	21	GND
DA5	22	GND
DA6	23	GND
DA7	24	GND
DA0	25	GND
DA1	26	GND
CLP/	27	GND
	28	GND
+12V	29	+12V
-12V	30	-12V
GND	31	GND
GND	32	GND

TMB

C		A
+5V	1	+5V
+5V	2	+5V
	3	
RA0	4	
RA1	5	
RA2	6	
RA3	7	
RA3/	8	
	9	
RSTB/	10	
WSTB/	11	BS0/
	12	GND
	13	GND
	14	GND
	15	GND
TRG	16	GND
DA0	17	GND
DA1	18	GND
DA2	19	GND
DA3	20	GND
DA4	21	GND
DA5	22	GND
DA6	23	GND
DA7	24	GND
	25	GND
	26	GND
	27	GND
	28	GND
	29	
	30	
GND	31	GND
GND	32	GND

B-BUS (ECL)

TBQ

C		A
GND	1	GND
GND	2	GND
CL0/	3	SCL0
CL1/	4	SCL1
CL2/	5	SCL2
CL3/	6	SCL3
CLM	7	GND
ILA1	8	GND
ILB1	9	GND
ILA2	10	GND
ILB2	11	GND
	12	GND
CL10	13	GND
-2V	14	-2V
CL100	15	GND
	16	
	17	
	18	
	19	CLMS0
	20	CLMS1
	21	GND
	22	GND
	23	GND
	24	GND
	25	GND
	26	GND
	27	ARM /
	28	INIT /
	29	ILAC1/
	30	ILAC2/
-5V	31	-5V
-5V	32	-5V

SEQ

C		A
GND	1	GND
GND	2	GND
	3	SCL0
	4	SCL1
	5	SCL2
	6	SCL3
CLM	7	GND
	8	GND
	9	GND
	10	GND
	11	GND
CLT	12	GND
CL10	13	GND
-2V	14	-2V
CL100	15	GND
REC0	16	
REC1	17	
REC2	18	
REC3	19	CLMS0
RECT	20	CLMS1
CND0/	21	GND
CND1/	22	GND
CND2/	23	GND
CND3/	24	GND
TCLK	25	GND
GLIT	26	GND
SLV0	27	ARM /
SLV1	28	INIT /
SLV2	29	
SLV3	30	
-5V	31	-5V
-5V	32	-5V

DMB 3

C		A
GND	1	GND
GND	2	GND
	3	GND
	4	GND
	5	GND
CL3/	6	GND
	7	GND
	8	GND
	9	GND
ILA2	10	GND
ILB2	11	GND
	12	GND
	13	GND
-2V	14	-2V
	15	GND
	16	GND
	17	GND
	18	GND
REC3	19	GND
	20	GND
CND0/	21	GND
CND1/	22	GND
CND2/	23	GND
CND3/	24	GND
TCLK	25	GND
GLIT	26	GND
SLV0	27	ARM /
SLV1	28	
SLV2	29	
SLV3	30	ILAC2/
-5V	31	-5V
-5V	32	-5V

DMB 2

C		A
GND	1	GND
GND	2	GND
	3	GND
	4	GND
	5	GND
CL2/	6	GND
	7	GND
	8	GND
	9	GND
ILA2	10	GND
ILB2	11	GND
	12	GND
	13	GND
-2V	14	-2V
	15	GND
	16	GND
	17	GND
	18	GND
REC2	19	GND
	20	GND
CND0/	21	GND
CND1/	22	GND
CND2/	23	GND
CND3/	24	GND
TCLK	25	GND
GLIT	26	GND
SLV0	27	ARM /
SLV1	28	
SLV2	29	
SLV3	30	ILAC2/
-5V	31	-5V
-5V	32	-5V

DMB 1

C		A
GND	1	GND
GND	2	GND
	3	GND
	4	GND
	5	GND
CL1/	6	GND
	7	GND
	8	GND
	9	GND
ILA1	10	GND
ILB1	11	GND
	12	GND
	13	GND
-2V	14	-2V
	15	GND
	16	GND
	17	GND
	18	GND
REC1	19	GND
	20	GND
CND0/	21	GND
CND1/	22	GND
CND2/	23	GND
CND3/	24	GND
TCLK	25	GND
GLIT	26	GND
SLV0	27	ARM /
SLV1	28	
SLV2	29	
SLV3	30	ILAC1/
-5V	31	-5V
-5V	32	-5V

DMB 0

C		A
GND	1	GND
GND	2	GND
	3	GND
	4	GND
	5	GND
CL0/	6	GND
	7	GND
	8	GND
	9	GND
ILA1	10	GND
ILB1	11	GND
	12	GND
	13	GND
-2V	14	-2V
	15	GND
	16	GND
	17	GND
	18	GND
REC0	19	GND
	20	GND
CND0/	21	GND
CND1/	22	GND
CND2/	23	GND
CND3/	24	GND
TCLK	25	GND
GLIT	26	GND
SLV0	27	ARM /
SLV1	28	
SLV2	29	
SLV3	30	ILAC1/
-5V	31	-5V
-5V	32	-5V

TMB

C		A
GND	1	GND
GND	2	GND
	3	GND
	4	GND
	5	GND
	6	GND
	7	GND
	8	GND
	9	GND
	10	GND
	11	GND
CLT	12	GND
	13	GND
-2V	14	-2V
	15	GND
	16	GND
	17	GND
	18	GND
	19	GND
RECT	20	GND
	21	GND
	22	GND
	23	GND
	24	GND
	25	GND
	26	GND
	27	ARM /
	28	INIT /
	29	
	30	
-5V	31	-5V
-5V	32	-5V

			EE	Tag	Name
			Bearb	08.81	HE
			Gepr	2.12.81	
1.2		11.5.82			
1.1		2.12.81			
Rev.	Änderungs-Nr.	Tag	Name		

KONTRON ELECTRONIC

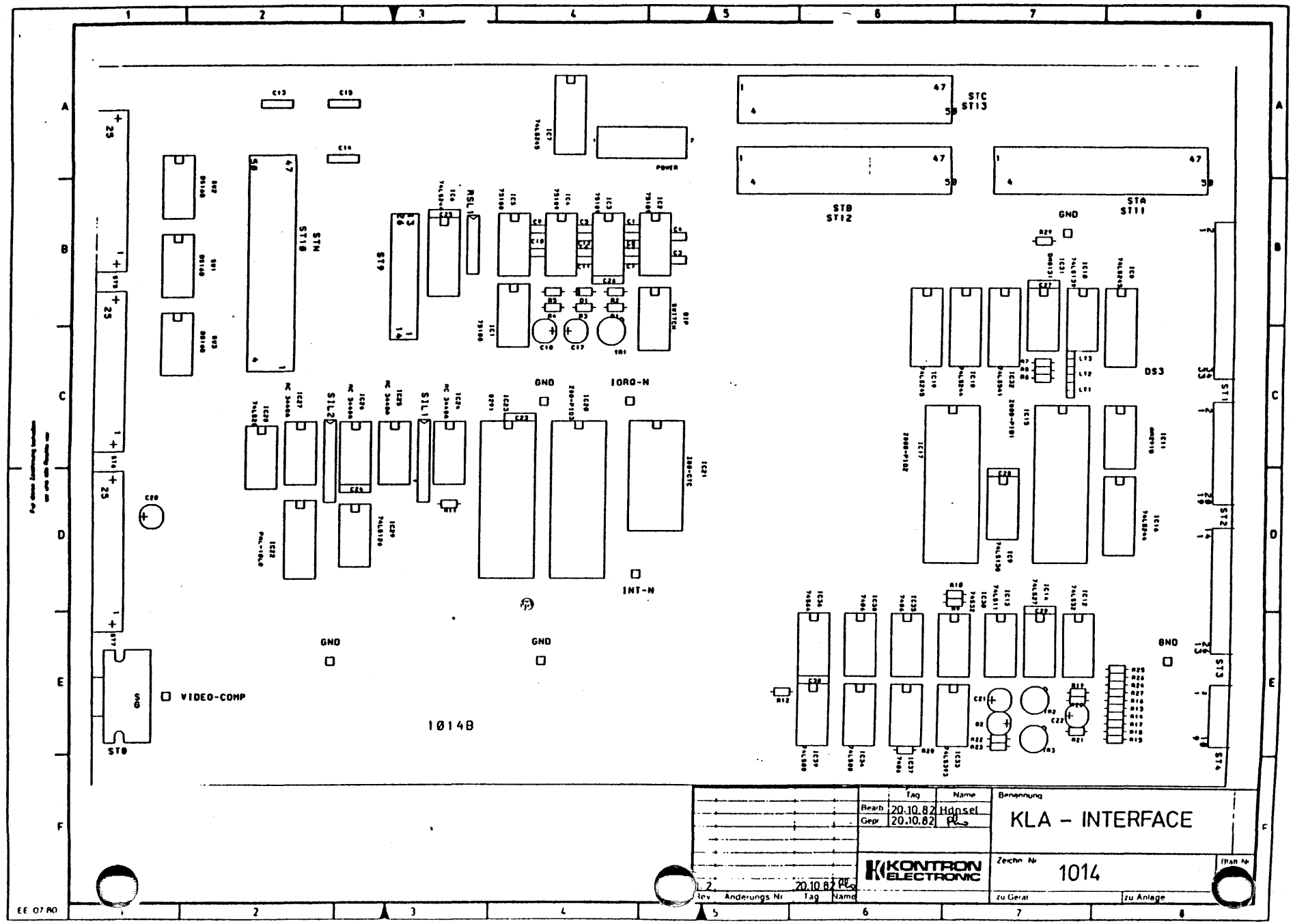
Benennung: KLA

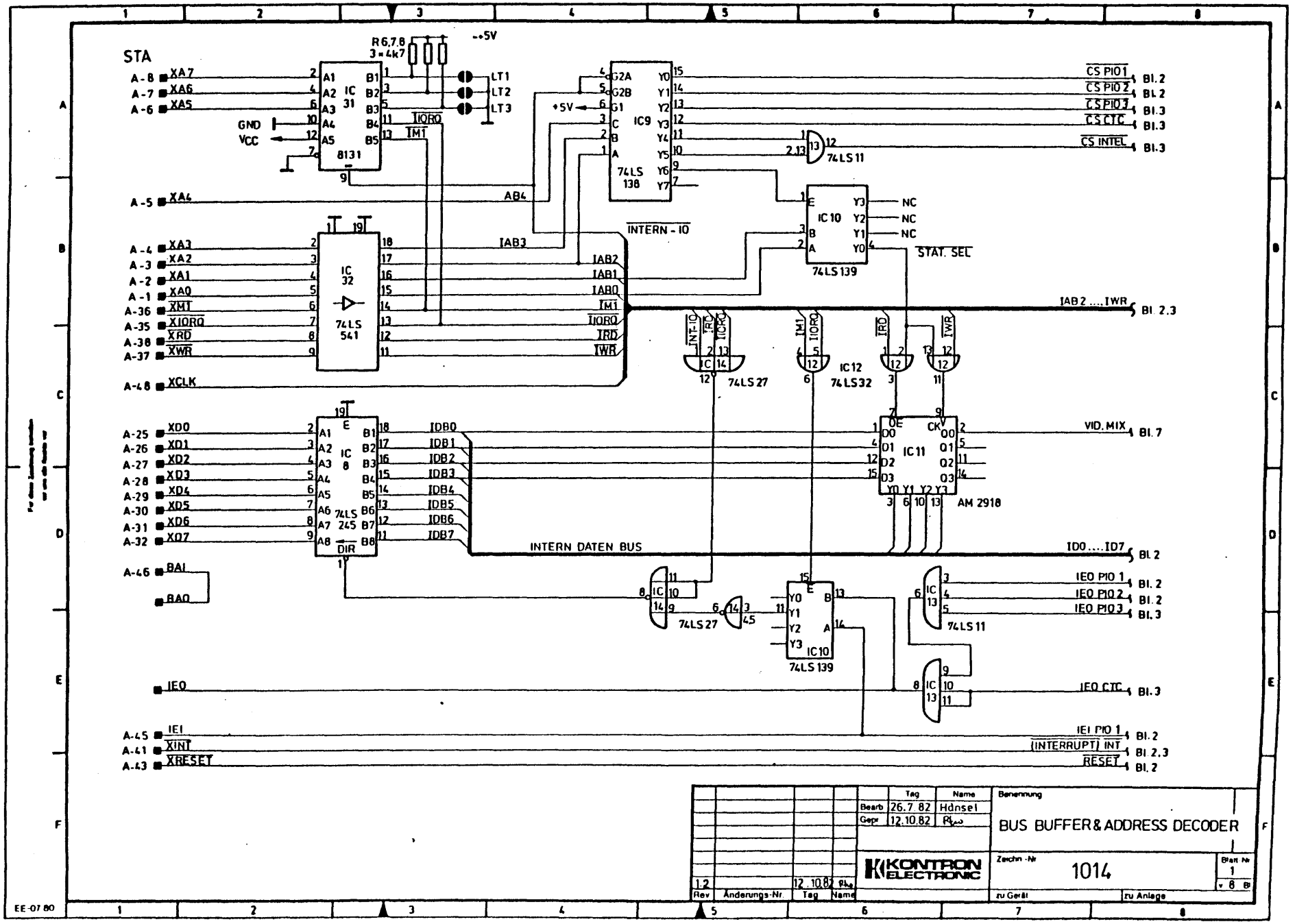
LA - MOTHERBOARD

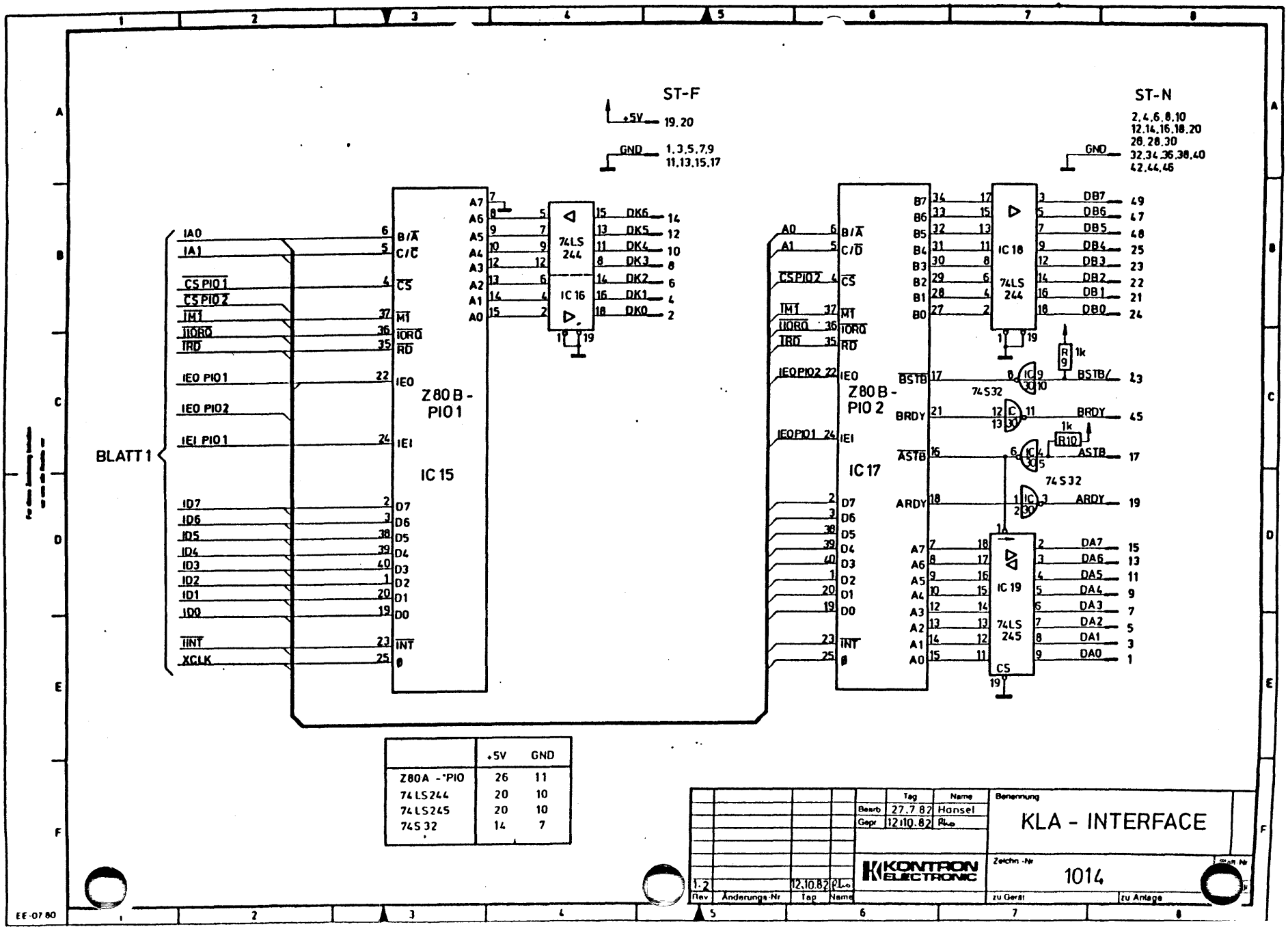
Zeichn. Nr. 316

zu Gerät

zu Anlage


STC
ST13
STB
ST12
STA
ST11
STN
ST18
ST9
MSL
POWER
GND
IORQ-N
INT-N
DS3
VIDEO-COMP
ST0
1014B
Bearb
20.10.82
Hansel
Gepr
20.10.82
Rev
Anderungs Nr
Tag
Name
Benennung
KLA - INTERFACE
KONTRON ELECTRONIC
Zeichn Nr
1014
zu Gerat
zu Anlage
EE 07 80


STA
R6,7,8
3 = 4k7
+5V
LT1
LT2
LT3
GND
VCC
IC 31
8131
IORQ
TMT
A-8 XA7
A-7 XA6
A-6 XA5
A-5 XA4
A-4 XA3
A-3 XA2
A-2 XA1
A-1 XA0
A-36 XMT
A-35 XIORQ
A-38 XRD
A-37 XWR
A-48 XCLK
IC 32
74LS 541
AB4
IAB3
IAB2
IAB1
IAB0
TM1
IIORQ
IRD
IWR
IC9
74LS 138
INTERN - IO
IC 10
74LS 139
NC
NC
NC
STAT. SEL
74LS 11
CS PIO1
CS PIO 2
CS PIO 3
CS CTC
CS INTEL
IAB2 .... IWR
INT-IO
IRC
IIORQ
IC 12
74LS 27
74LS 32
A-25 XD0
A-26 XD1
A-27 XD2
A-28 XD3
A-29 XD4
A-30 XD5
A-31 XD6
A-32 XD7
IC 8
74LS 245
DIR
IDB0
IDB1
IDB2
IDB3
IDB4
IDB5
IDB6
IDB7
INTERN DATEN BUS
IC 11
AM 2918
VID. MIX
ID0 .... ID7
A-46 BAI
BAO
IEO
IEI
XINT
XRESET
IEO PIO 1
IEO PIO 2
IEO PIO 3
IEO CTC
IEI PIO 1
(INTERRUPT) INT
RESET
Bl. 2
Bl. 2.3
Bl. 7
Bl. 3
Bearb 26.7.82 Hdnsel
Gepr 12.10.82
Benennung
BUS BUFFER & ADDRESS DECODER
KONTRON ELECTRONIC
Zeichn.-Nr 1014
Blatt Nr 1
v. 8 Bl
1.2 12.10.82
Rev Änderungs-Nr. Tag Name
zu Gerät
zu Anlage
EE-07 80



	+5V	GND
Z80A - PIO	26	11
74LS244	20	10
74LS245	20	10
74S32	14	7

	Tag	Name
Bearb	27.7.82	Hansel
Gepr	12.10.82	

Benennung: KLA - INTERFACE

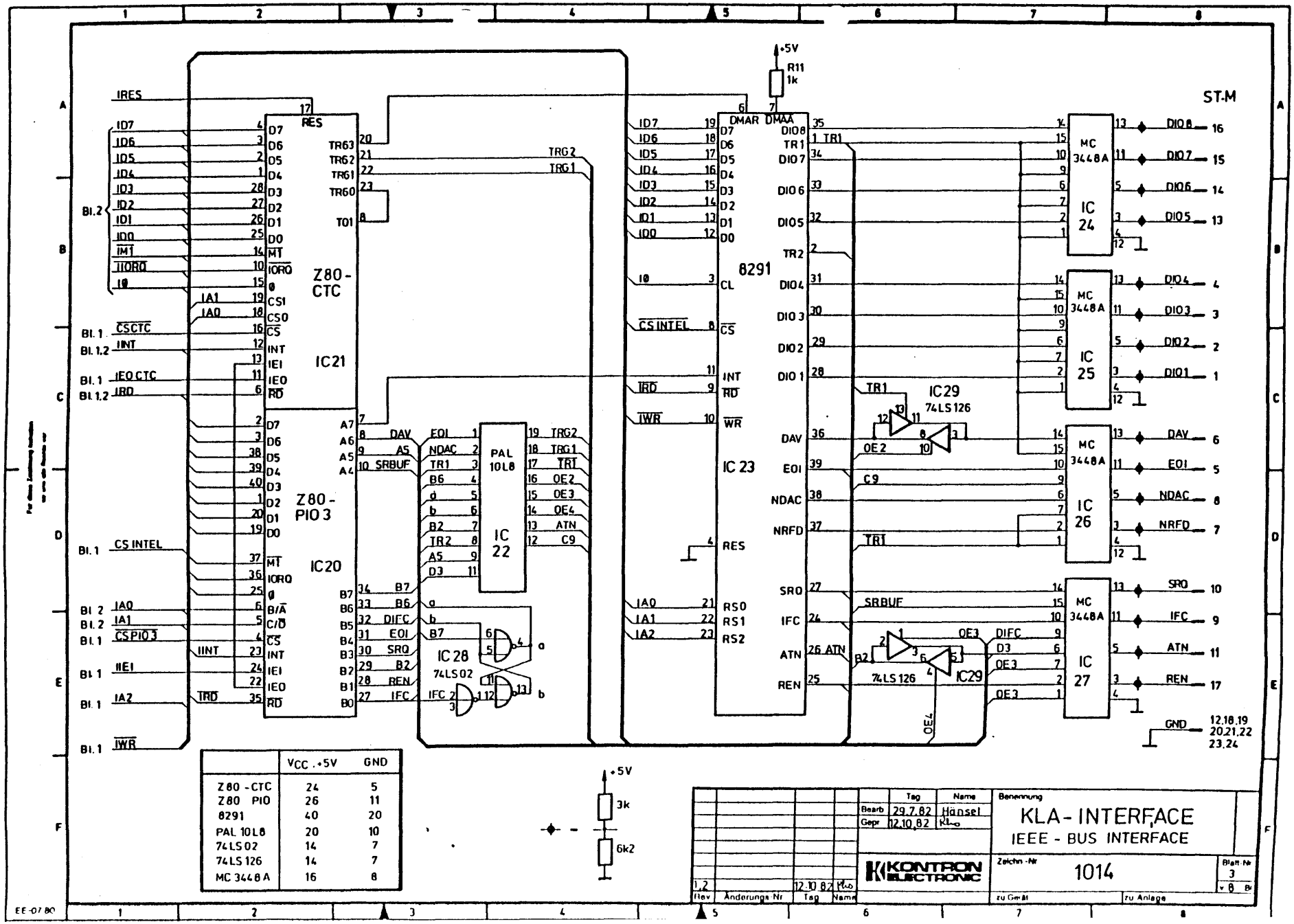
KONTRON ELECTRONIC

Zeichn.-Nr: 1014

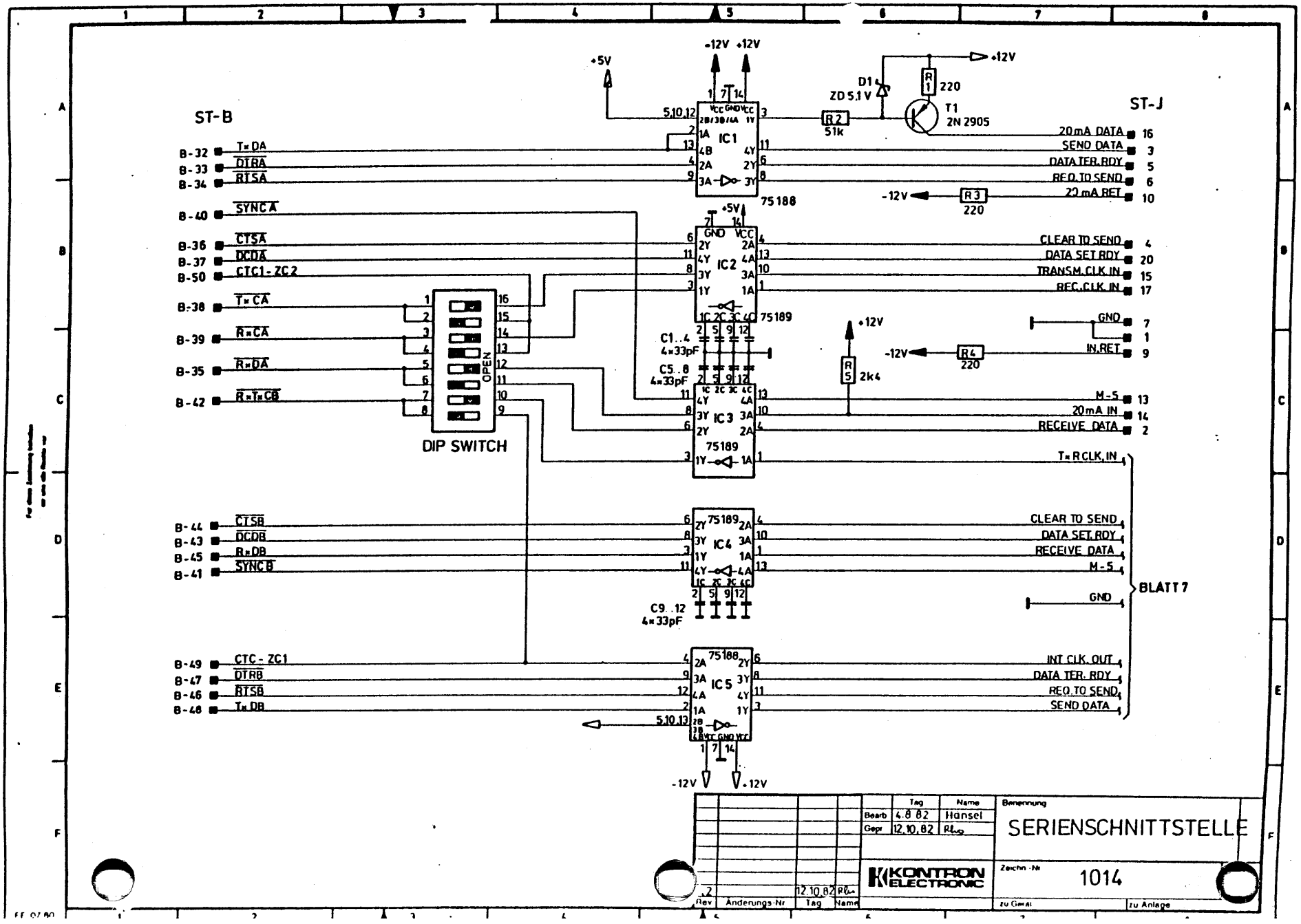
Rev	Änderungs-Nr	Tag	Name
1.2		12.10.82	

zu Gerät | zu Anlage

EE-07 80



	V_{CC} +5V	GND
Z80-CTC	24	5
Z80 PIO	26	11
8291	40	20
PAL 10L8	20	10
74LS02	14	7
74LS126	14	7
MC 3448A	16	8



	Tag	Name
Bearb	4.8.82	Hansel
Gepr	12.10.82	Rl.

Benennung: SERIENSCHNITTSTELLE

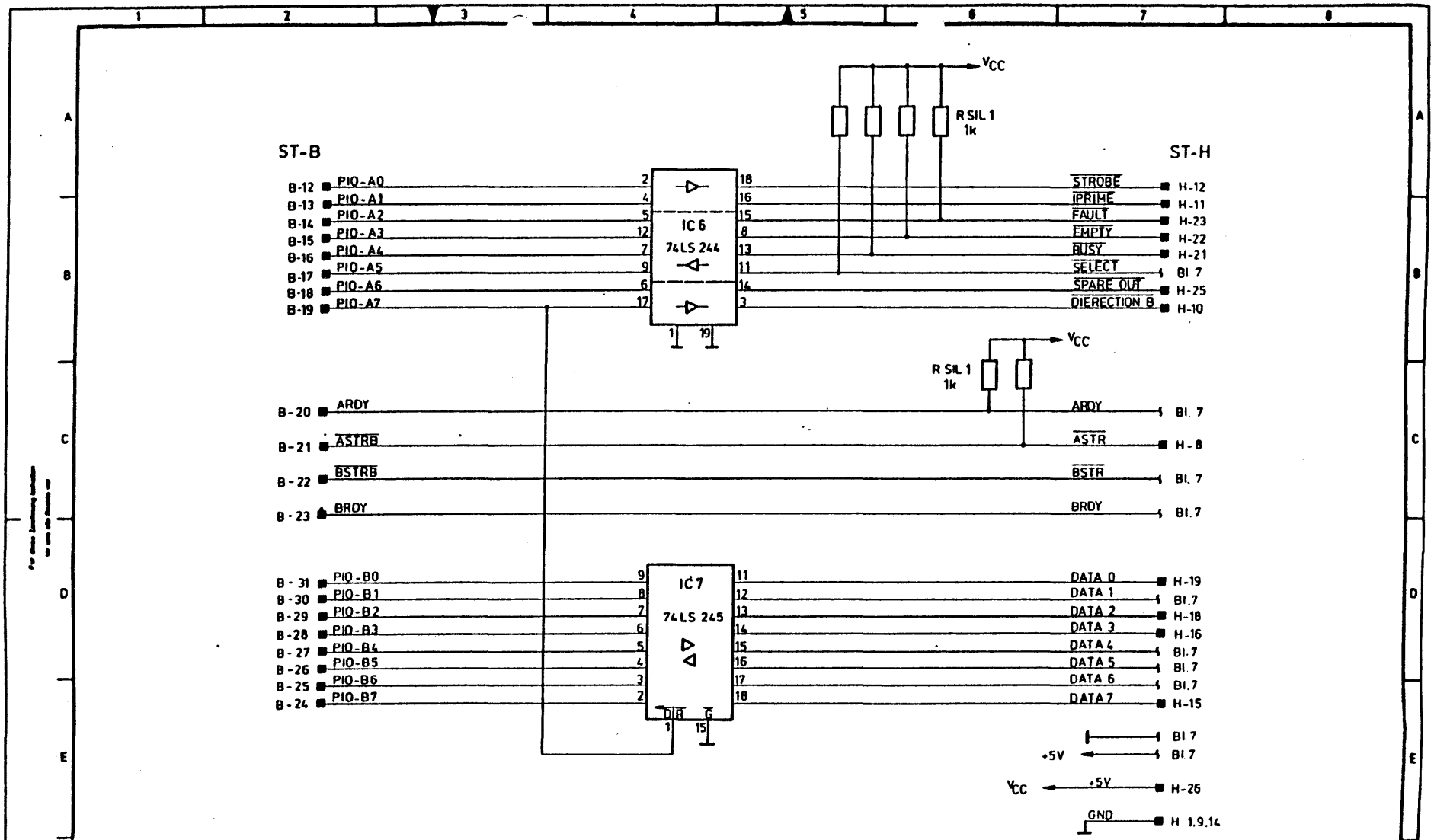
KONTRON ELECTRONIC

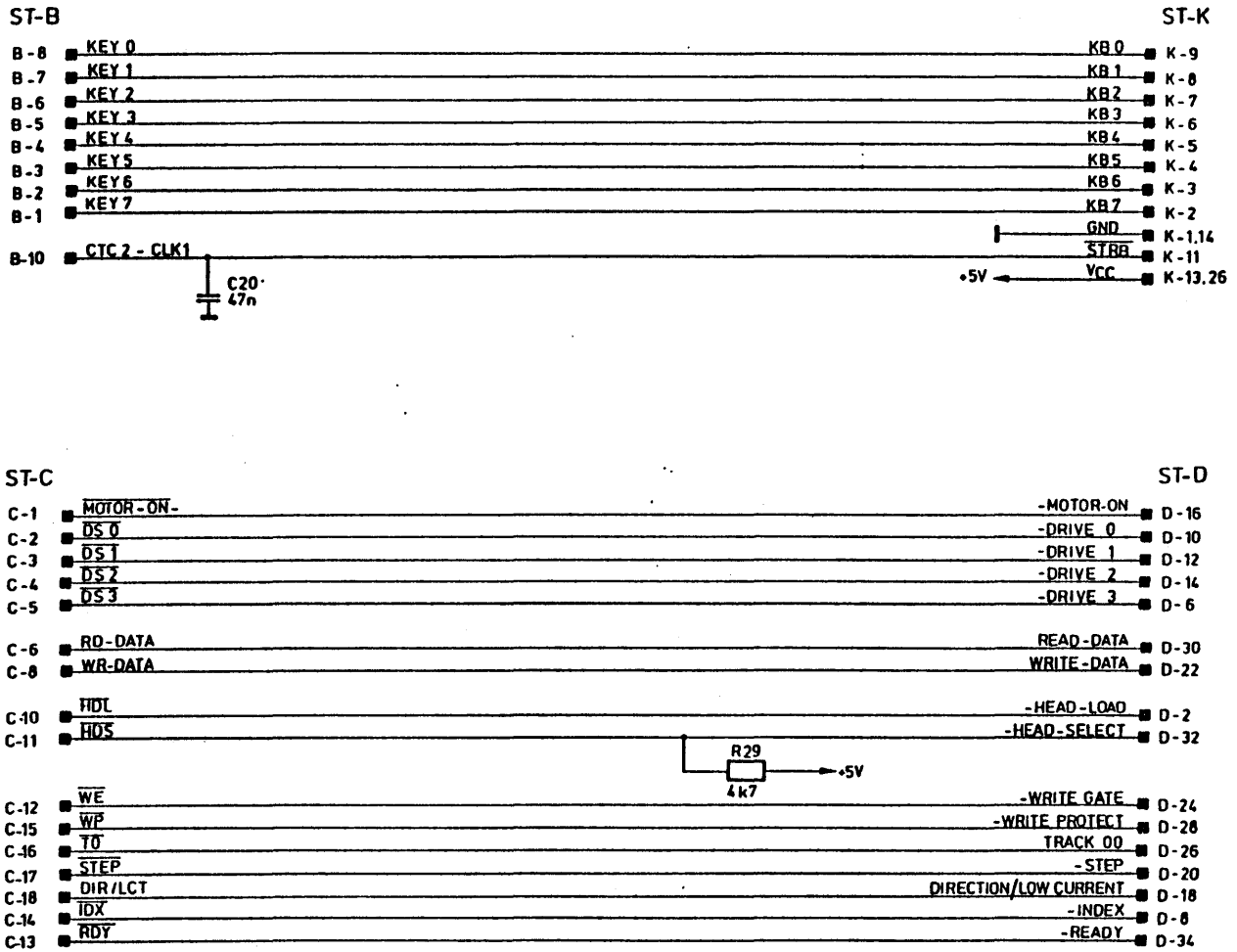
Zeichn.-Nr: 1014

Rev	Änderungs-Nr	Tag	Name
2		12.10.82	Rl.

zu Gerät | zu Anlage

EE 07.80


ST-B
ST-H
VCC
R SIL 1
1k
IC 6
74LS 244
B-12 PIO-A0
B-13 PIO-A1
B-14 PIO-A2
B-15 PIO-A3
B-16 PIO-A4
B-17 PIO-A5
B-18 PIO-A6
B-19 PIO-A7
STROBE H-12
IPRIME H-11
FAULT H-23
EMPTY H-22
BUSY H-21
SELECT BI 7
SPARE OUT H-25
DIERECTION B H-10
B-20 ARDY
B-21 ASTRB
B-22 BSTRB
B-23 BRDY
ARDY BI. 7
ASTR H-8
BSTR BI. 7
BRDY BI. 7
IC 7
74LS 245
DIR
G
B-31 PIO-B0
B-30 PIO-B1
B-29 PIO-B2
B-28 PIO-B3
B-27 PIO-B4
B-26 PIO-B5
B-25 PIO-B6
B-24 PIO-B7
DATA 0 H-19
DATA 1 BI.7
DATA 2 H-18
DATA 3 H-16
DATA 4 BI.7
DATA 5 BI.7
DATA 6 BI.7
DATA 7 H-15
BI.7
+5V BI.7
VCC +5V H-26
GND H 1.9.14
Tag Name
Bearb 5.8.82 Hänsel
Gepr. 12.10.82
Benennung
PARALLELSCHNITTSTELLE
KONTRON ELECTRONIC
Zeichn.-Nr 1014
Blatt-Nr 5
1.2 12.10.82
Änderungs-Nr Tag Name
zu Gerät
zu Anlage



	Tag	Name
Bearb	5.8.82	Hansel
Gepr	12.10.82	

KONTRON ELECTRONIC

Benennung: FLOPPY DISK&KEYBOARD INTERFACE

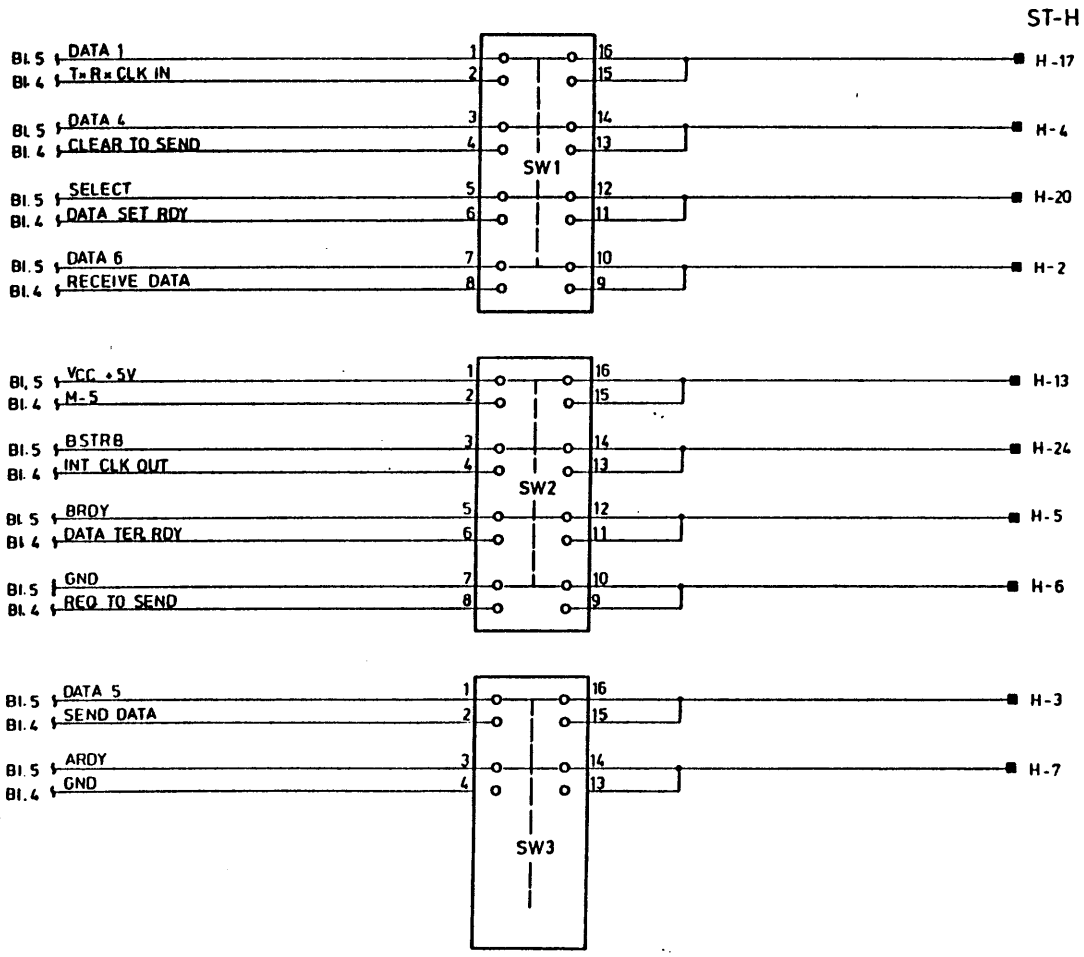
Zeichn.-Nr: 1014

Blatt-Nr

zu Gerät | zu Anlage

Rev	Änderungs-Nr	Tag	Name
1.2		12.10.82	

EE 07 80



3 = SUPER DIL DS 16B 4-2

	Tag	Name
Bearb	9.8.82	Hansel
Gepr	12.10.82	

Benennung: SERIEN - PARALLEL UMSCHALTER

KONTRON ELECTRONIC

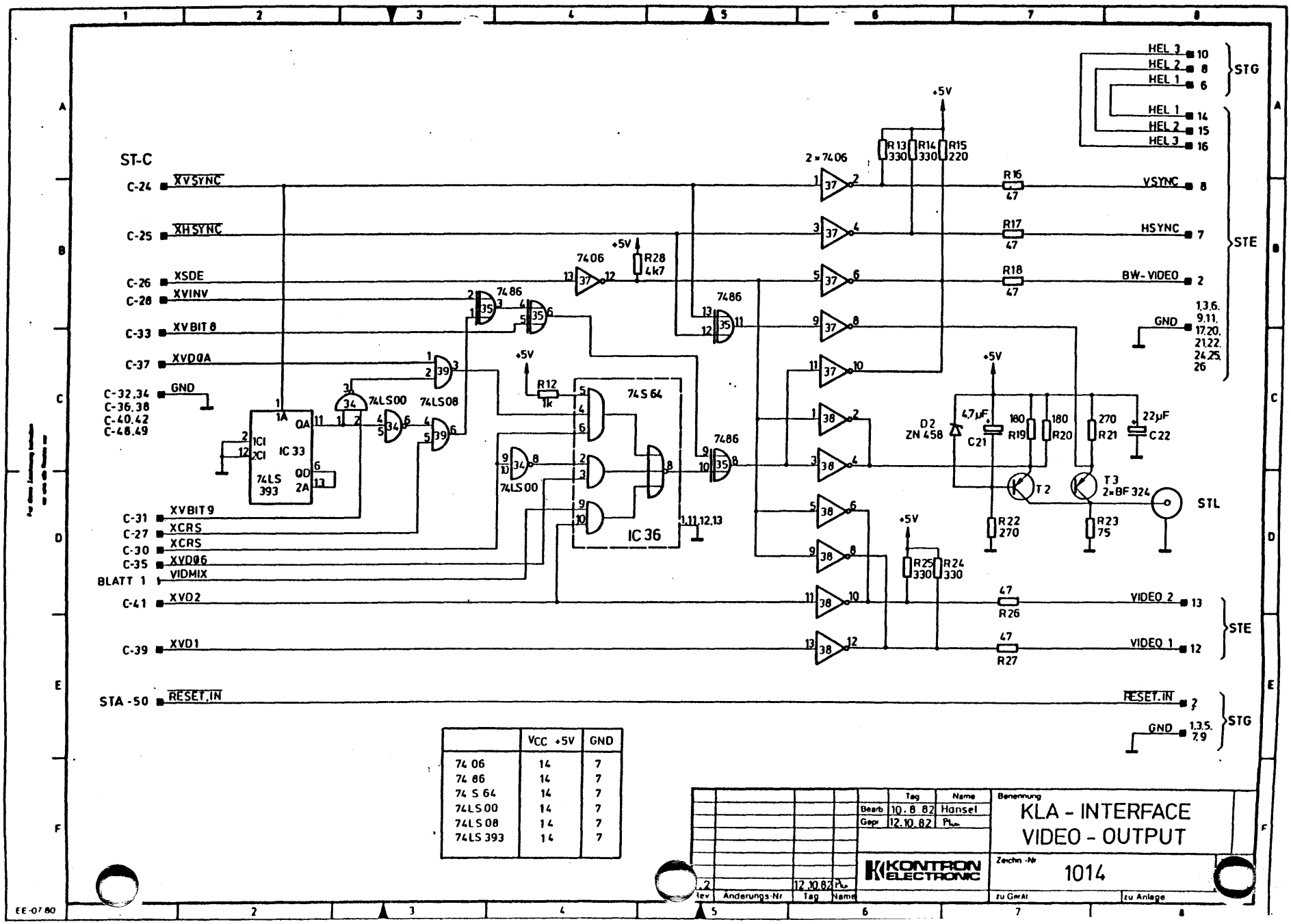
Zeichn.-Nr: 1014

Blatt Nr: 7 v. 8 Bl.

Rev	Änderungs Nr.	Tag	Name
1.2		12.10.82	

zu Gerät | zu Anlage

EE 07.80



	Vcc +5V	GND
74 06	14	7
74 86	14	7
74 S 64	14	7
74LS00	14	7
74LS08	14	7
74LS393	14	7

	Tag	Name
Bearb	10.8.82	Hansel
Gepr	12.10.82	Pl.

Benennung
KLA - INTERFACE
VIDEO - OUTPUT

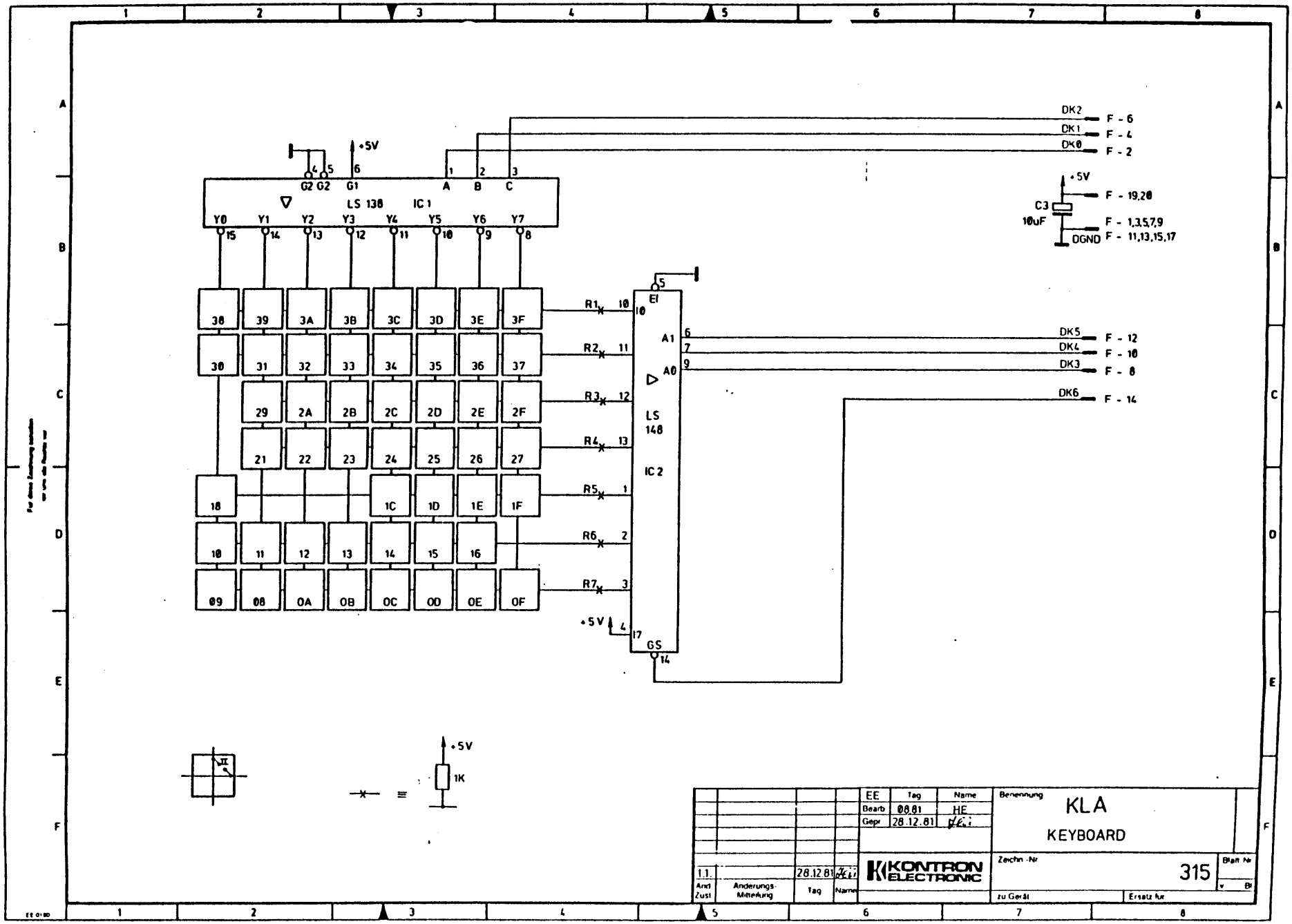
KONTRON ELECTRONIC

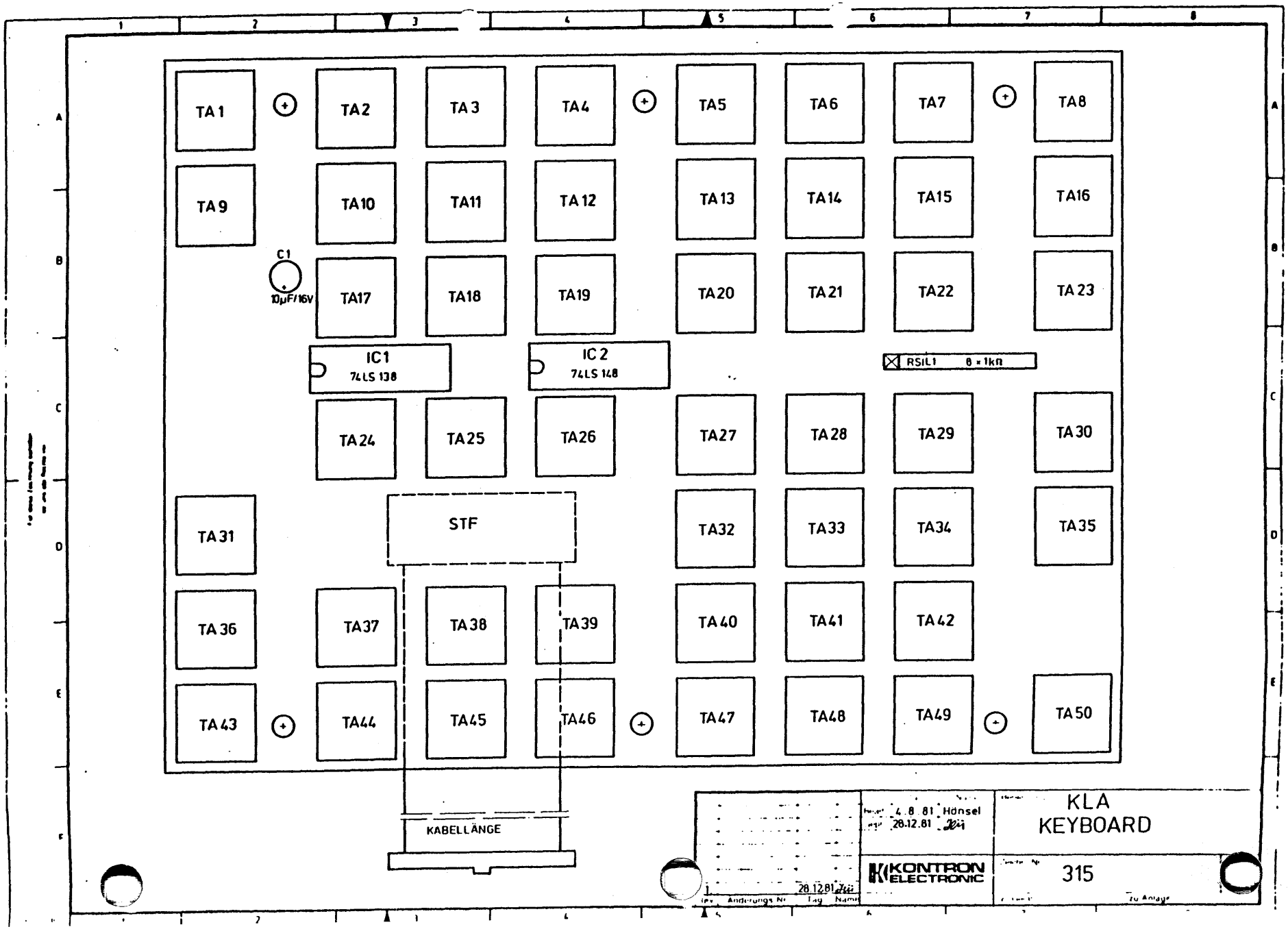
Zeichn.-Nr 1014

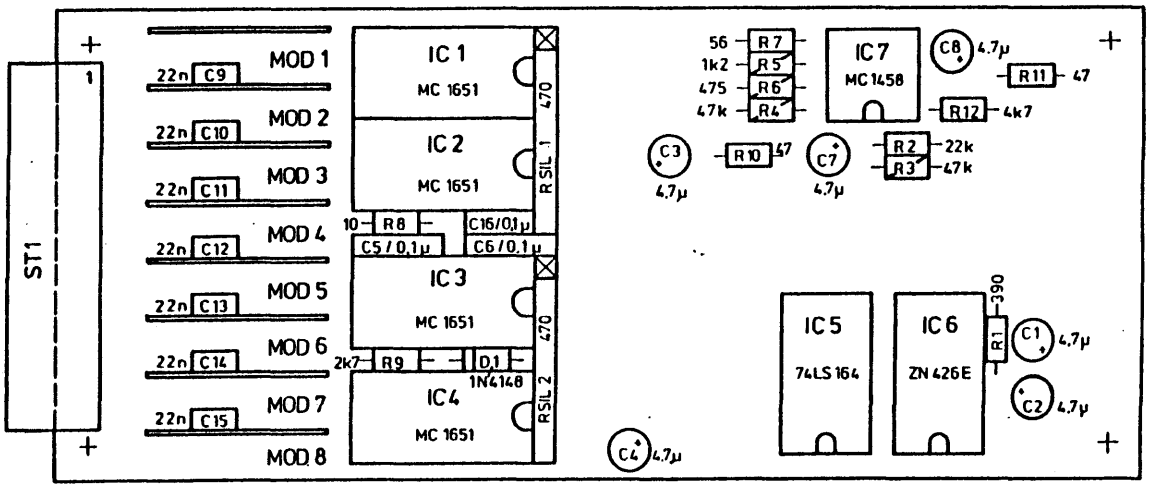
zu Gr.Bl. | zu Anlage

lev	Änderungs-Nr	Tag	Name
2		12.10.82	Pl.

EE-07 80

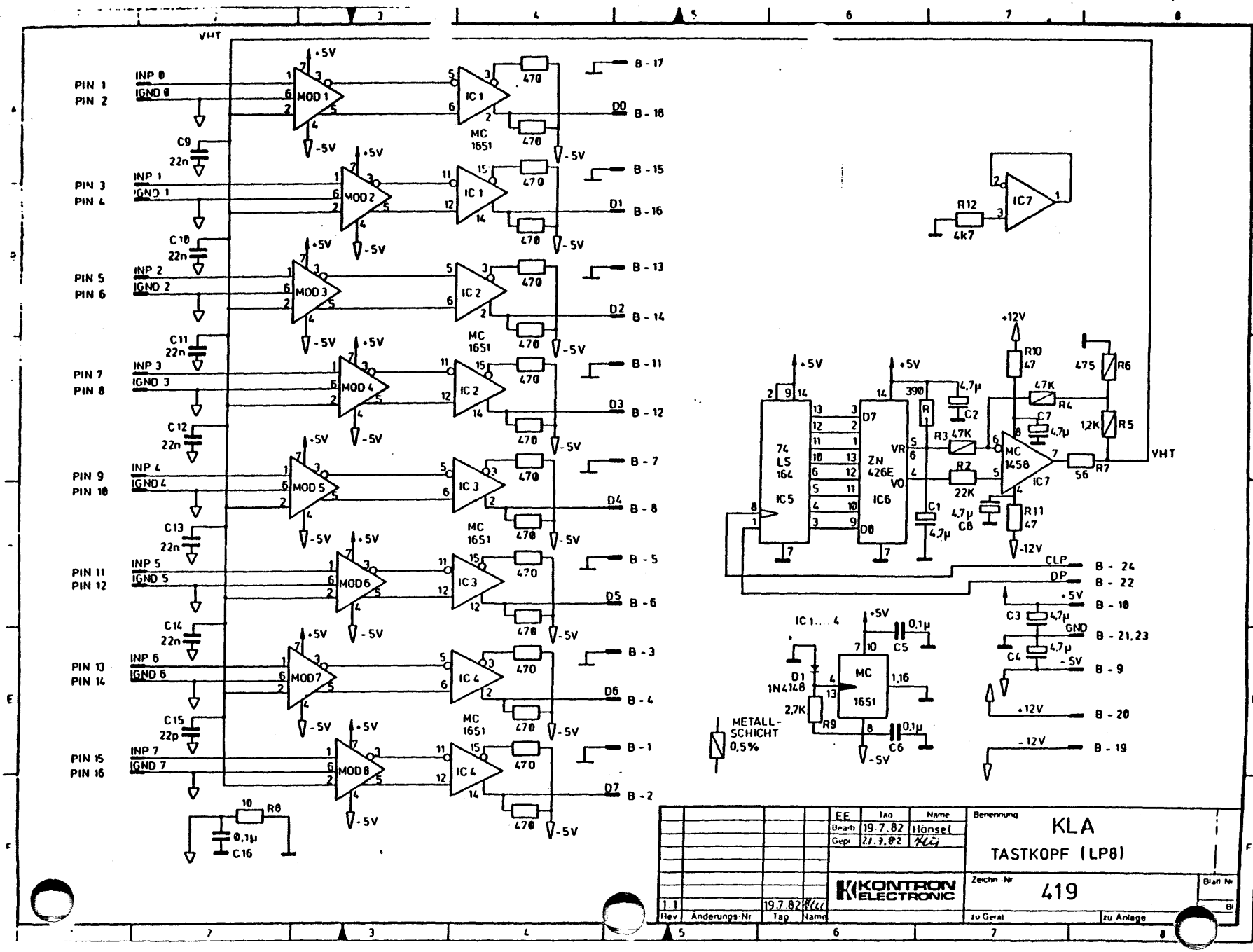

DK2
DK1
DK0
F - 6
F - 4
F - 2
+5V
C3
10uF
DGND
F - 19,20
F - 1,3,5,7,9
F - 11,13,15,17
LS 138
IC 1
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
G2 G2 G1
A B C
38 39 3A 3B 3C 3D 3E 3F
30 31 32 33 34 35 36 37
29 2A 2B 2C 2D 2E 2F
21 22 23 24 25 26 27
18 1C 1D 1E 1F
10 11 12 13 14 15 16
09 08 0A 0B 0C 0D 0E 0F
R1
R2
R3
R4
R5
R6
R7
EI
A1
A0
LS
148
IC 2
GS
DK5
DK4
DK3
DK6
F - 12
F - 10
F - 8
F - 14
1K
EE
Tag
Name
Bearb
08.81
HE
Gepr
28.12.81
Benennung
KLA
KEYBOARD
KONTRON ELECTRONIC
Zeichn -Nr
315
Blatt Nr
zu Gerät
Ersatz für
1.1.
Änd Zust
Änderungs-Mitteilung
28.12.81
Tag
Name


TA1
TA2
TA3
TA4
TA5
TA6
TA7
TA8
TA9
TA10
TA11
TA12
TA13
TA14
TA15
TA16
C1
10µF/16V
TA17
TA18
TA19
TA20
TA21
TA22
TA23
IC1
74LS 138
IC 2
74LS 148
RSIL1 8 x 1kΩ
TA24
TA25
TA26
TA27
TA28
TA29
TA30
TA31
STF
TA32
TA33
TA34
TA35
TA36
TA37
TA38
TA39
TA40
TA41
TA42
TA43
TA44
TA45
TA46
TA47
TA48
TA49
TA50
KABELLÄNGE
4.8.81 Hänsel
28.12.81
KLA
KEYBOARD
KONTRON ELECTRONIC
315
28.12.81
Änderungs Nr
Tag
Name
Zu Anlage

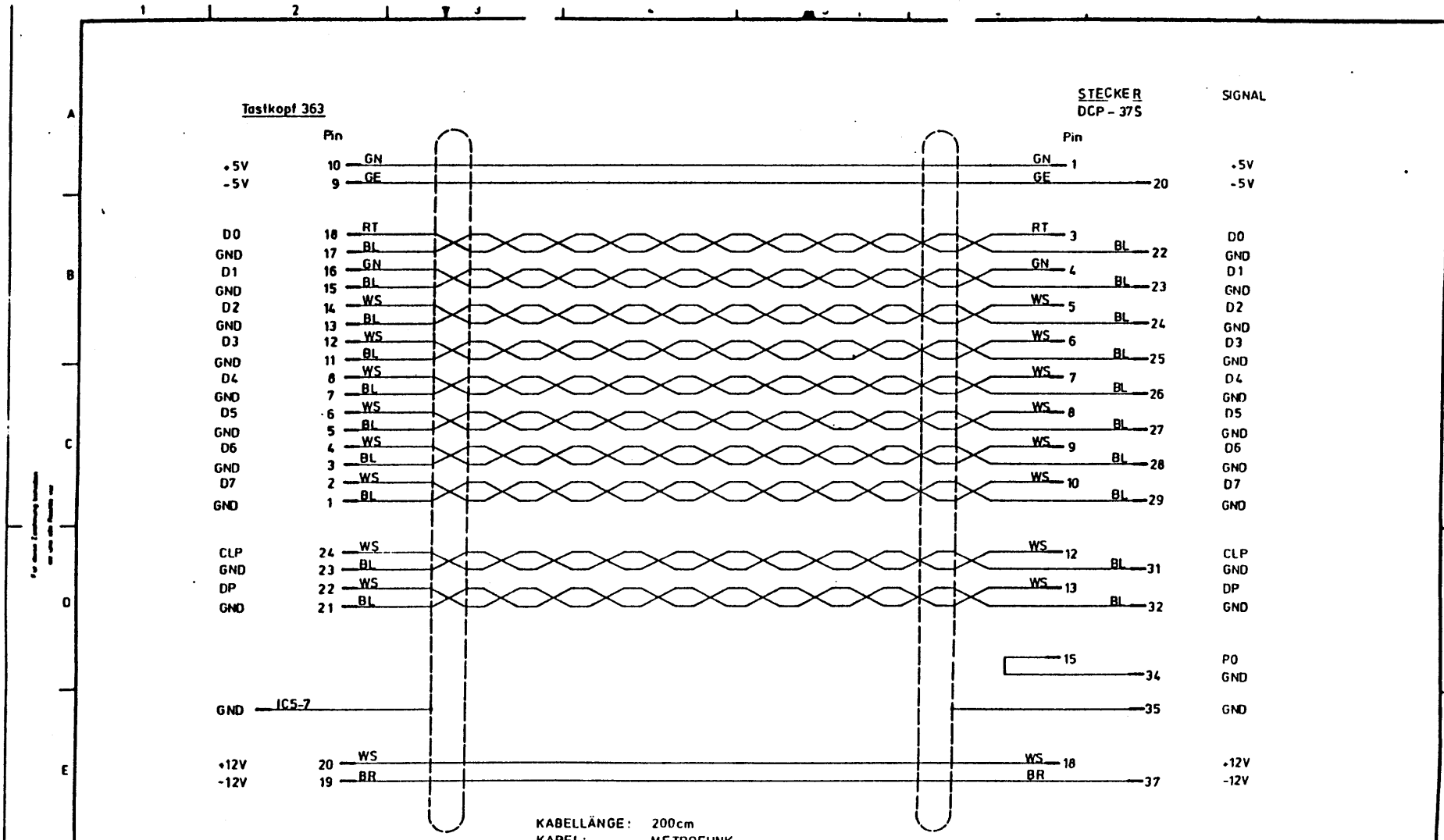


					Tag	Name	Benennung
				Bearb	19.7.82	Hansel	KLA - Tastkopf
				Gepr.	21.7.82		LP8 - HYBRID
1.1			19.7.82				
Rev.	Änderungs-Nr.		Tag	Name	KONTRON ELECTRONIC	Zeichn.-Nr 419	Blatt-Nr
						zu Gerät	zu Anlage

EE-07 80



				EE	Tag	Name	Benennung
				Bearb	19.7.82	Hänsel	KLA
				Gepr	21.7.82	Kli	TASTKOPF (LP8)
1.1		19.7.82	Kli	KONTRON ELECTRONIC			Zeichn.-Nr 419
Rev	Änderungs-Nr	Tag	Name				Blatt Nr 8
					zu Gerät		zu Anlage



	Tag	Name
Bearb	19.7.82	Hänsel
Gepr	21.7.82	Klei

Benennung: KLA
TASTKOPF - KABEL
LP8 - HYBRID

KONTRON ELECTRONIC

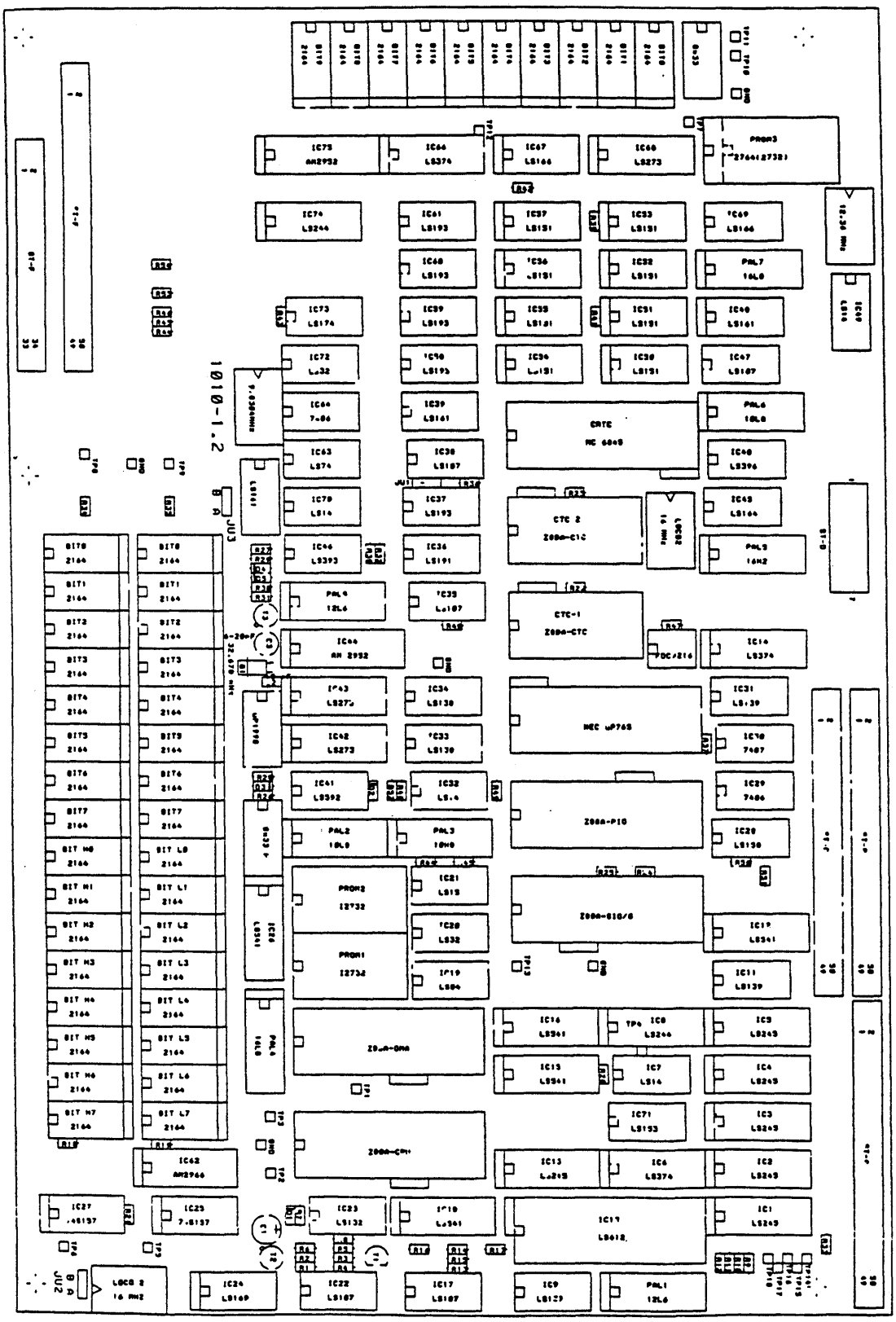
Zeichn.-Nr: 419

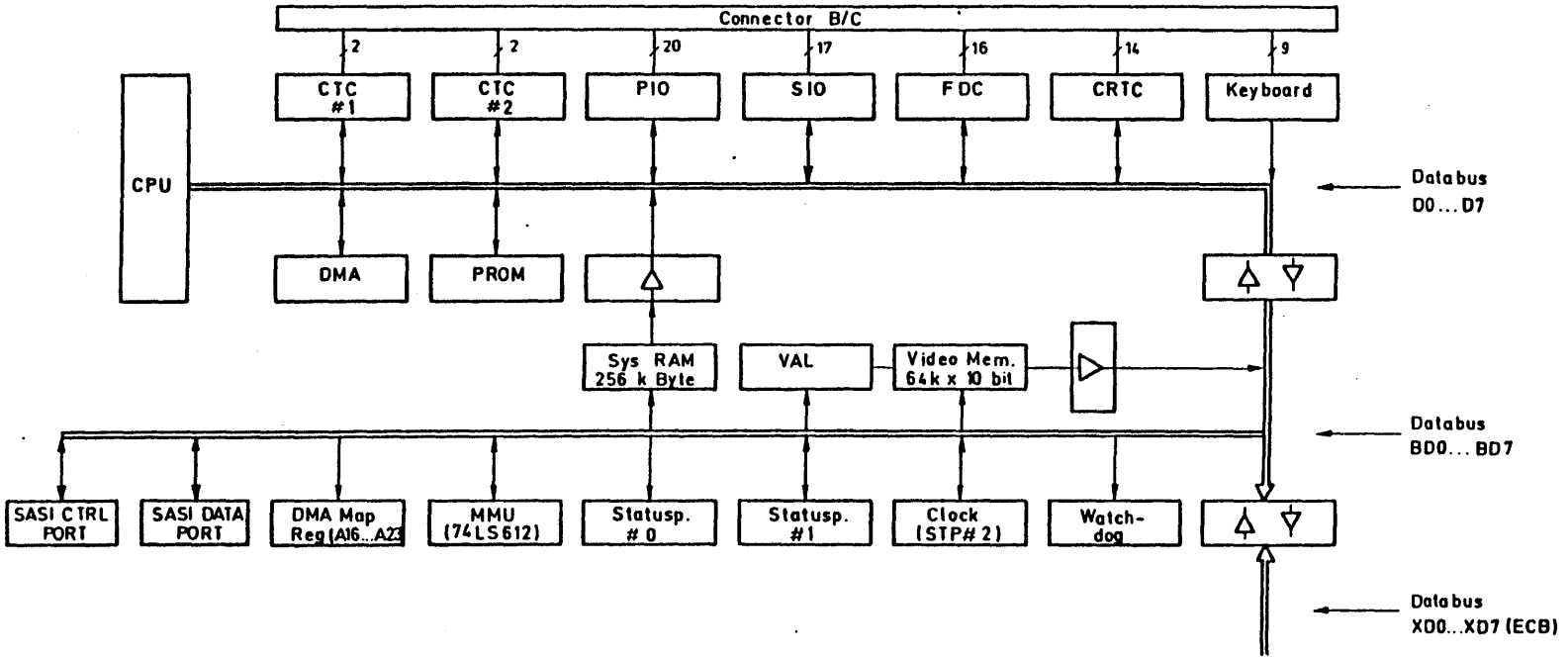
Blatt-Nr:

Rev	Änderungs Nr	Tag	Name
1.1		19.7.82	Klei

zu Gerät | zu Anlage

EE-07.80


1010-1.2
BESTUECKUNGSPLAN KDT-REV.6



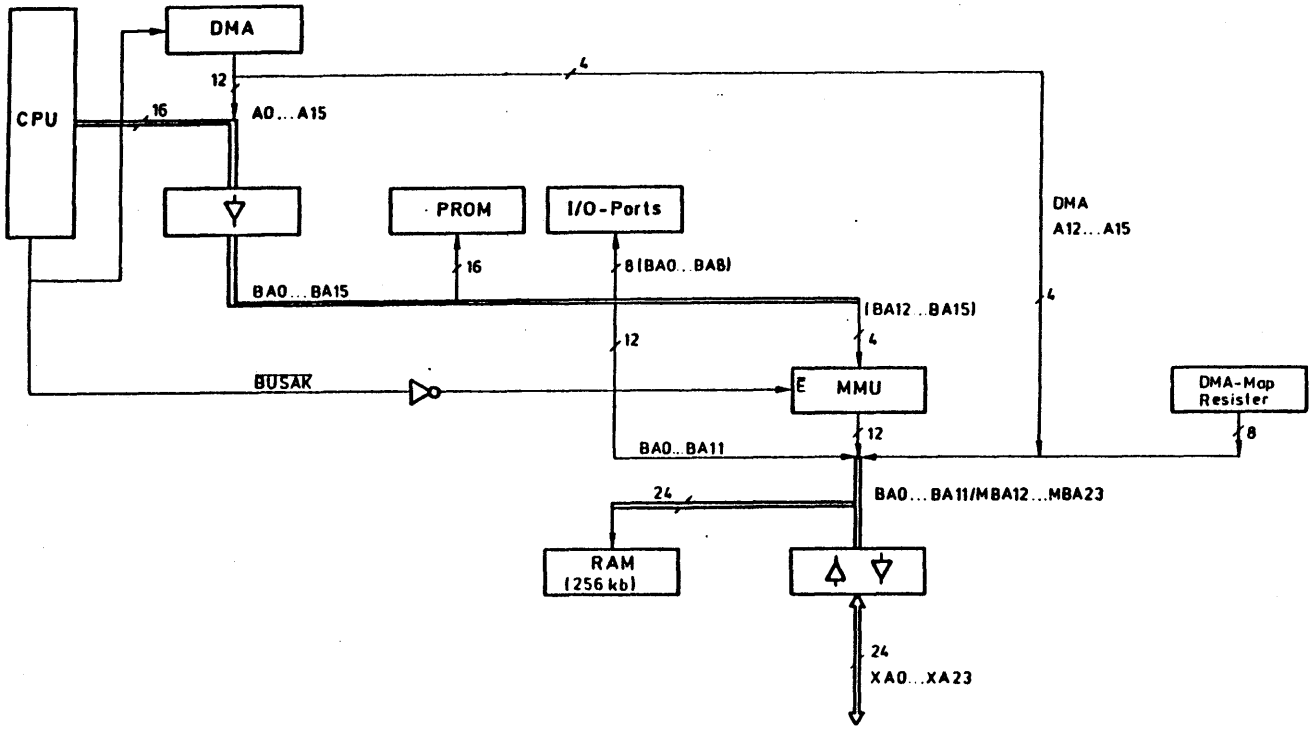
					Tag	Name	Benennung: KDT 6 Data Bus Structure
				Bearb	20.4.82	SPIES	
				Gepr.	22.4.82		
1.1		20.4.82		KONTRON ELECTRONIC	Zeichn.-Nr: 1010		Blatt-Nr:
Rev.	Änderungs-Nr	Tag	Name		zu Gerät	zu Anlage	v Bl

Ax = unbuffererd CPU address

BAx = buffered CPU address

MBAx = mapped address from MMU

XAx = buffered ECB address (external address)



	Tag	Name
Bearb	20 4 82	SPIES
Gepr	22.4.82	

Benennung: KDT 6

Address Bus Structure

KONTRON ELECTRONIC

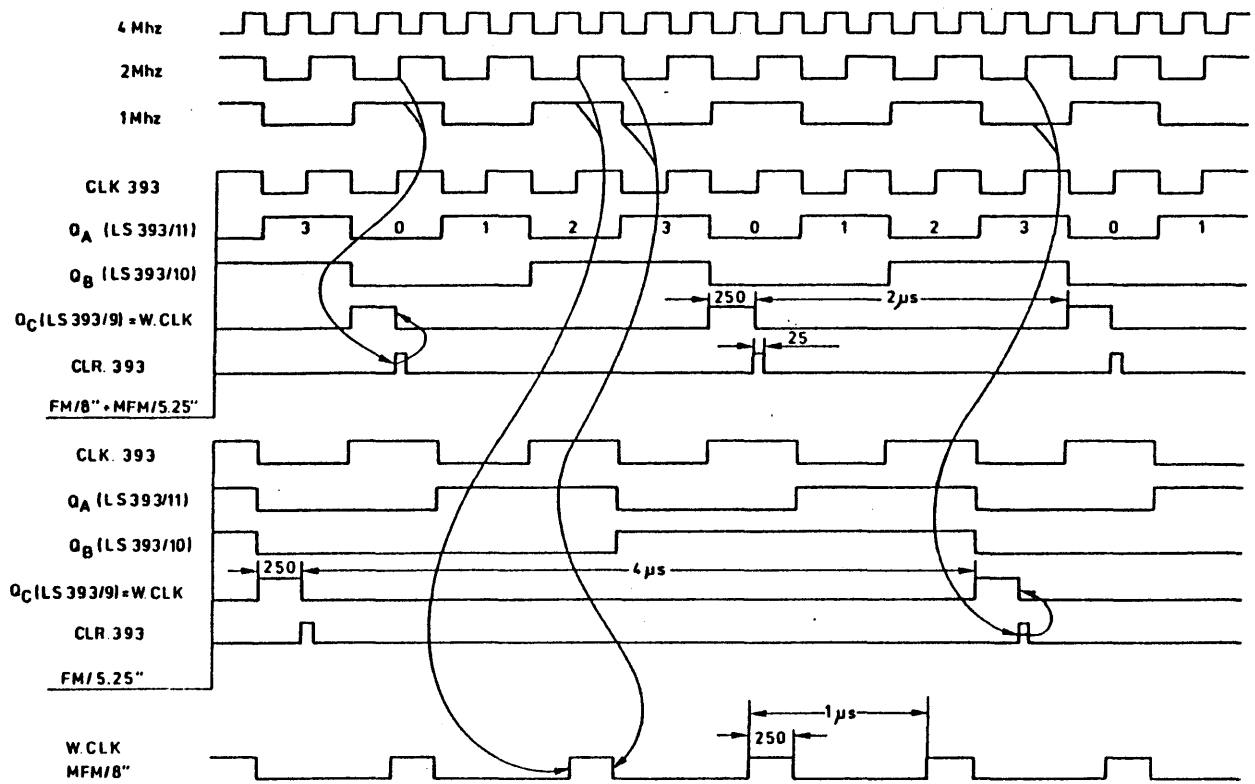
Zeichn.-Nr: 1010

Blatt-Nr

Änderungs-Nr	Tag	Name
	20.4.82	

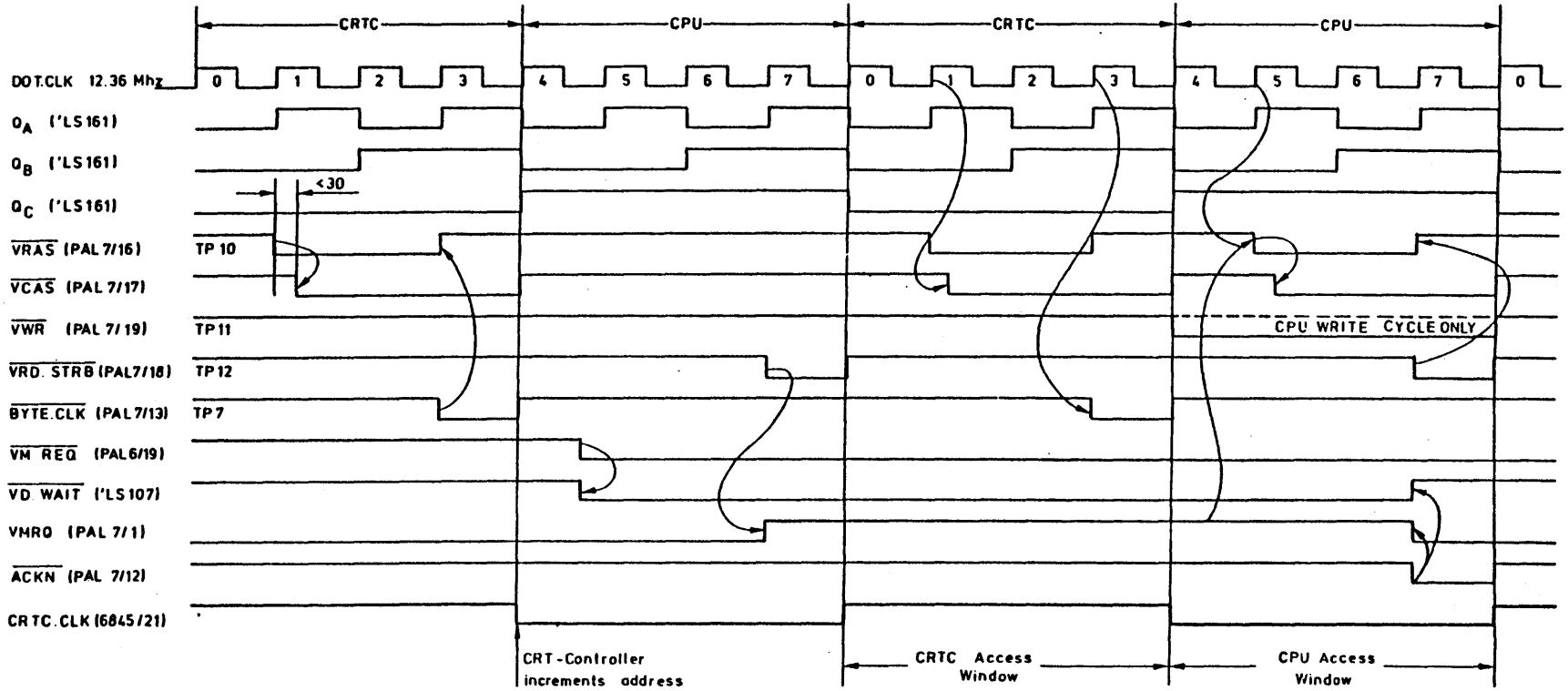
zu Gerät | zu Anlage

EE-07 80



					Tag	Name	Benennung: KDT 6
				Bearb	21.4.82	SPIES	FDC - Write Clock Generation (PAL6-12HC)
				Gepr	22.4.82		
							KONTRON ELECTRONIC
							Zeichn.-Nr: 1010
1.1		21.4.82					Blatt Nr:
Rev	Änderungs-Nr.	Tag	Name				zu Gerät / zu Anlage

FE-07.80



	Tag	Name
Bearb	21.4.82	SPIES
Gepr	22.4.82	

Benennung: KDT 6 Video Timing

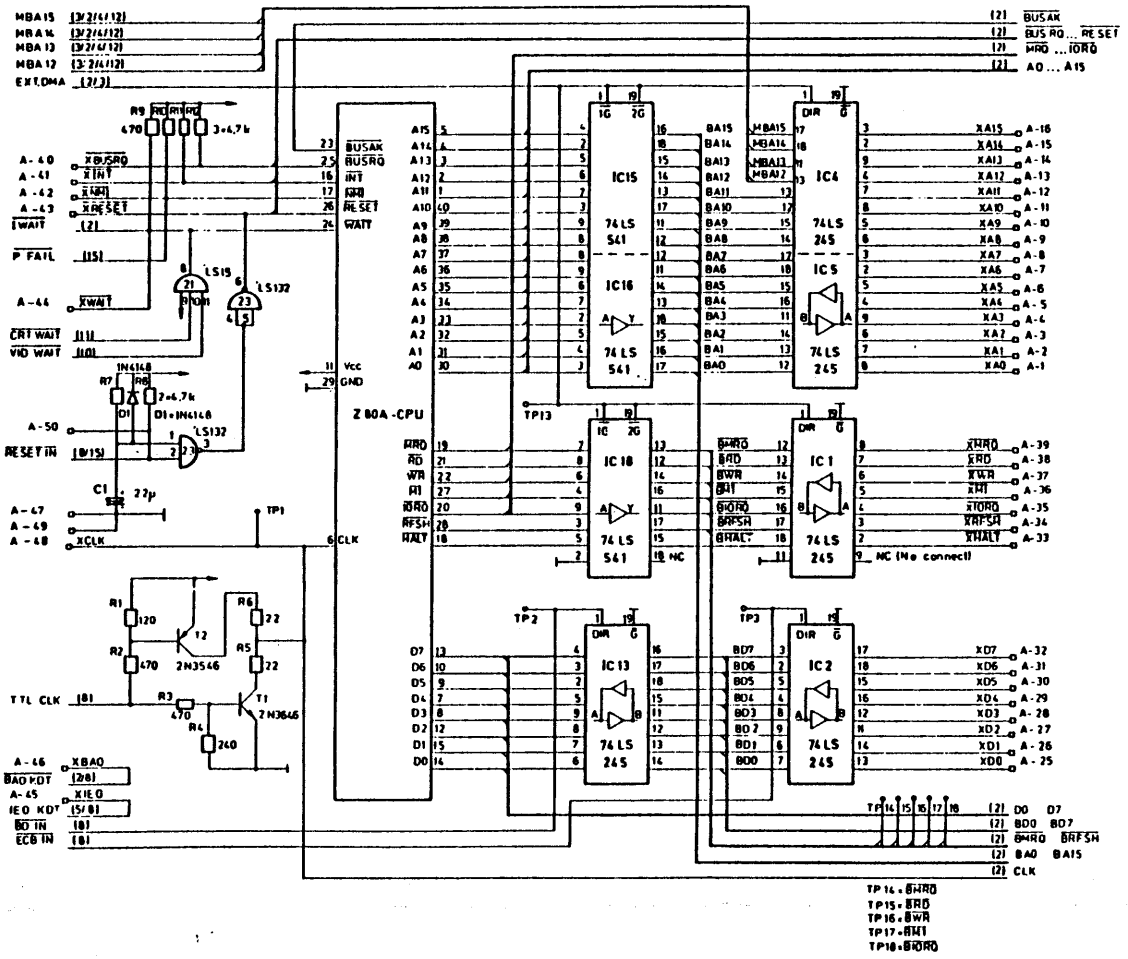
KONTRON ELECTRONIC

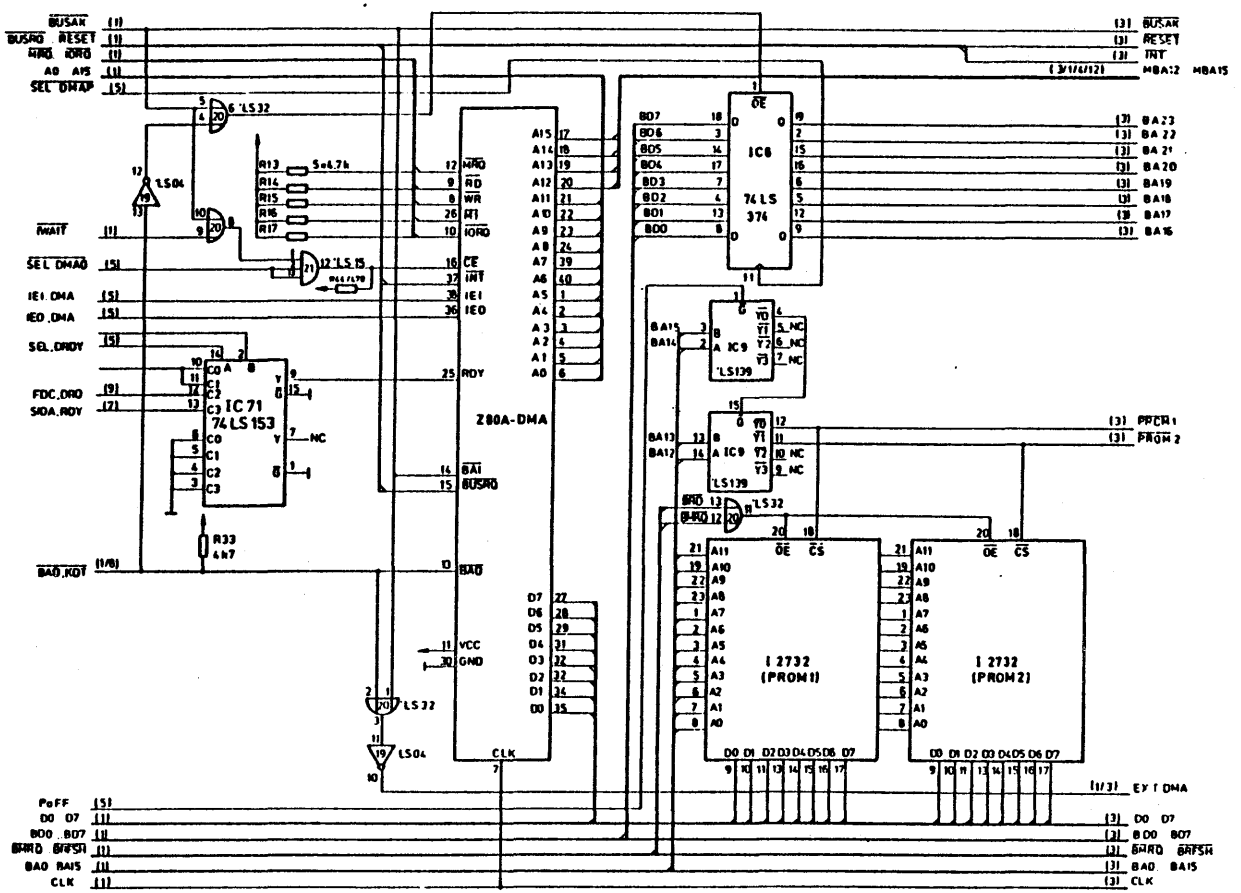
Zeichn.-Nr: 1010

zu Gerät	zu Anlage

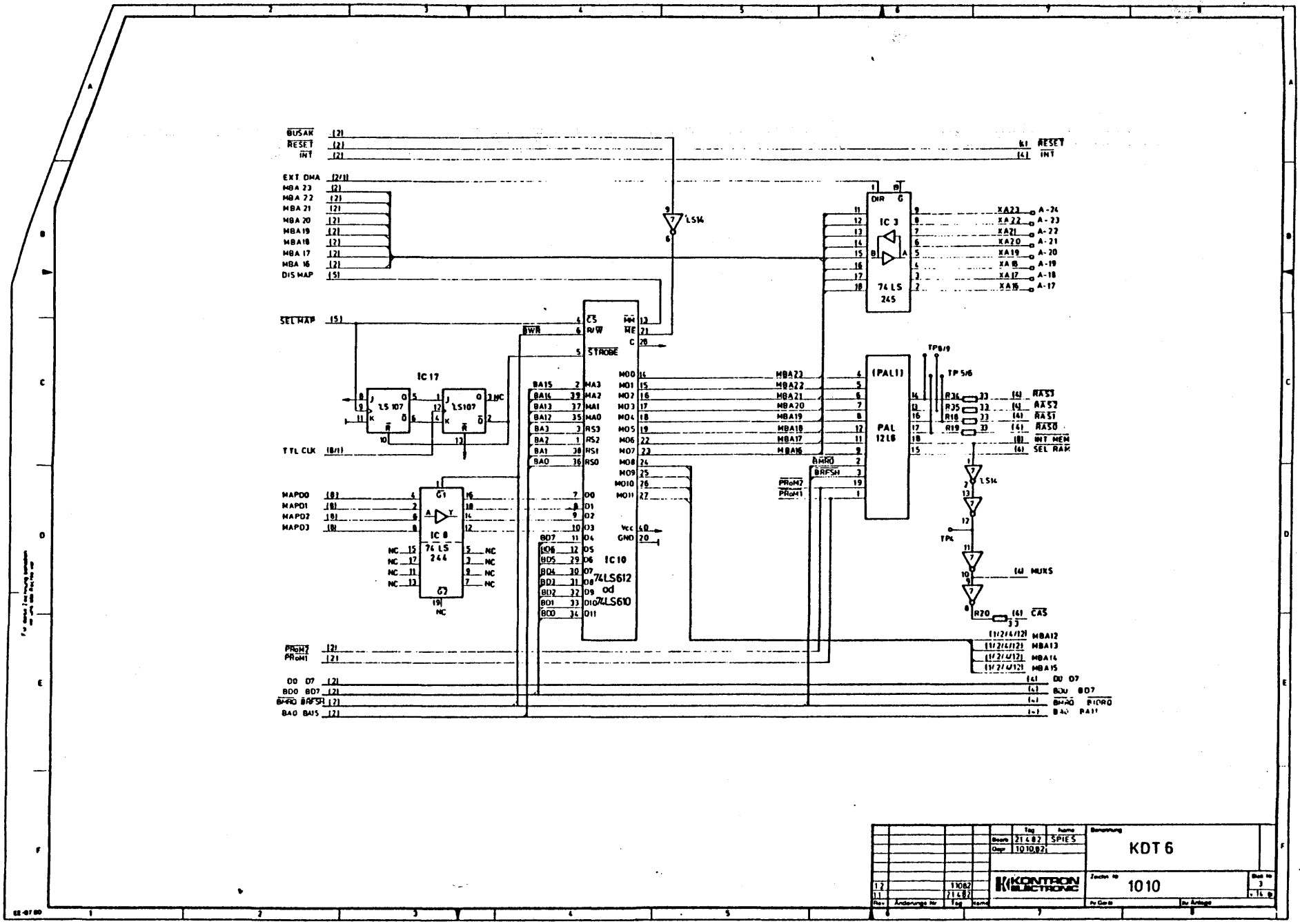
zu	Änderungs-Nr	Tag	Name
1.1		21.4.82	

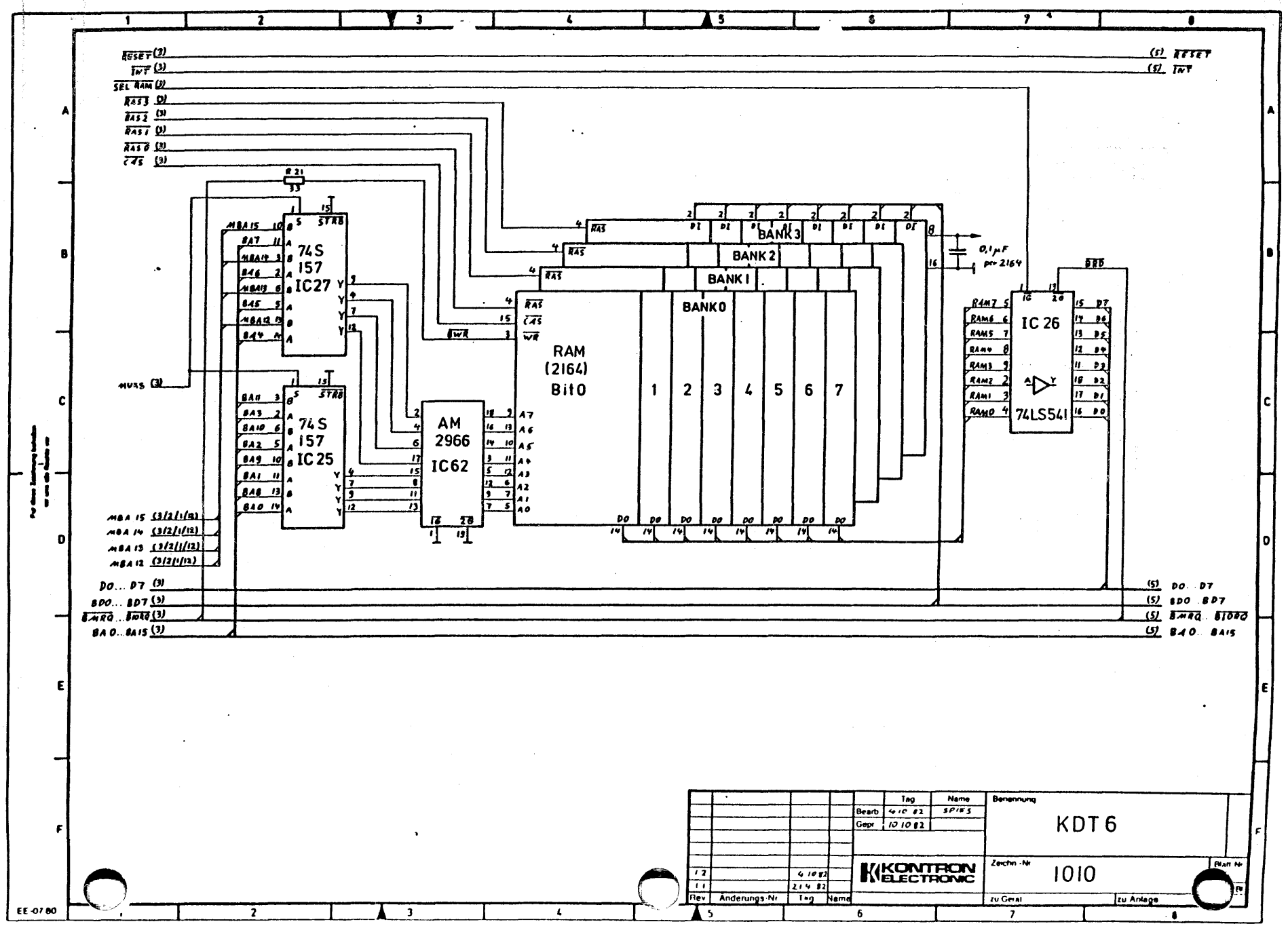
EE-07 80


MBA15
MBA14
MBA13
MBA12
EXT.DMA
BUSAK
BUSRQ ... RESET
MRQ ... IORQ
A0 ... A15
R9
470
3×4.7k
A-40
A-41
A-42
A-43
WAIT
P FAIL
A-44
CRT WAIT
VID WAIT
LS15
LS132
1N4148
R7
R8
2×4.7k
D1
D1=1N4148
A-50
RESET IN
C1 : 22µ
A-47
A-49
A-48
XCLK
TP1
Z 80A -CPU
Vcc
GND
CLK
TP13
IC15
74 LS 541
IC16
74 LS 541
IC4
DIR
74LS 245
IC5
74 LS 245
IC 18
74 LS 541
IC 1
74 LS 245
NC (No connect)
TP2
IC 13
74 LS 245
TP3
IC 2
74 LS 245
R1
120
R2
470
R6
22
R5
22
T2
2N3546
T1
2N3646
R3
470
R4
240
TTL CLK
A-46
XBAO
BAO KDT
A-45
XIEO
IEO KDT
BO IN
ECB IN
TP14=BMRQ
TP15=BRD
TP16=BWR
TP17=BM1
TP18=BIORQ
KDT 6
1010
KONTRON ELECTRONIC



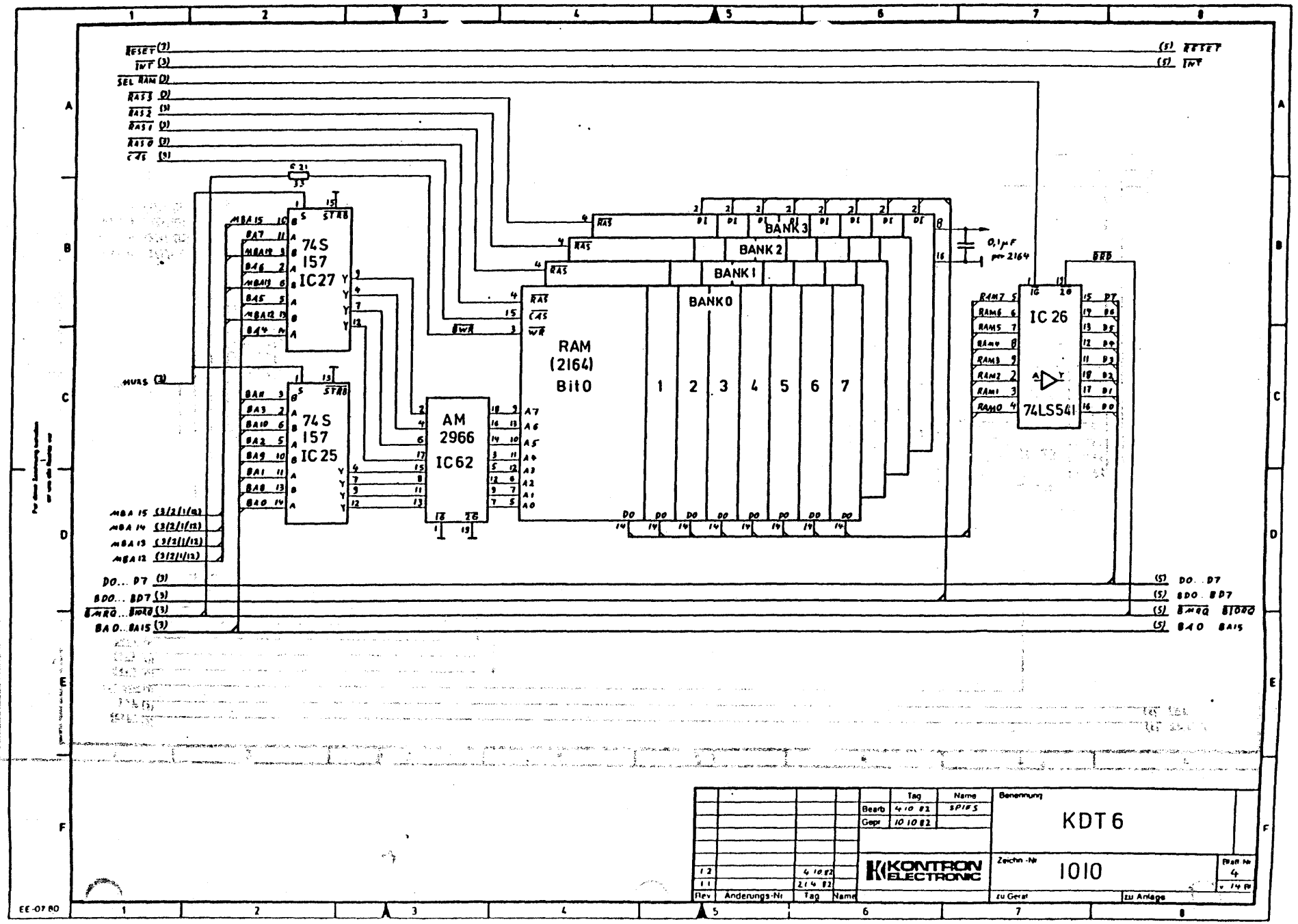
			Tag	Name	KDT 6
		Bearb	21.6.82	SPIES	
		Gepr	10.10.82		
12			11.08.82		KONTRON ELECTRONIC
11			21.6.82		1010
Nr.	Änderungen	Tag	Name		

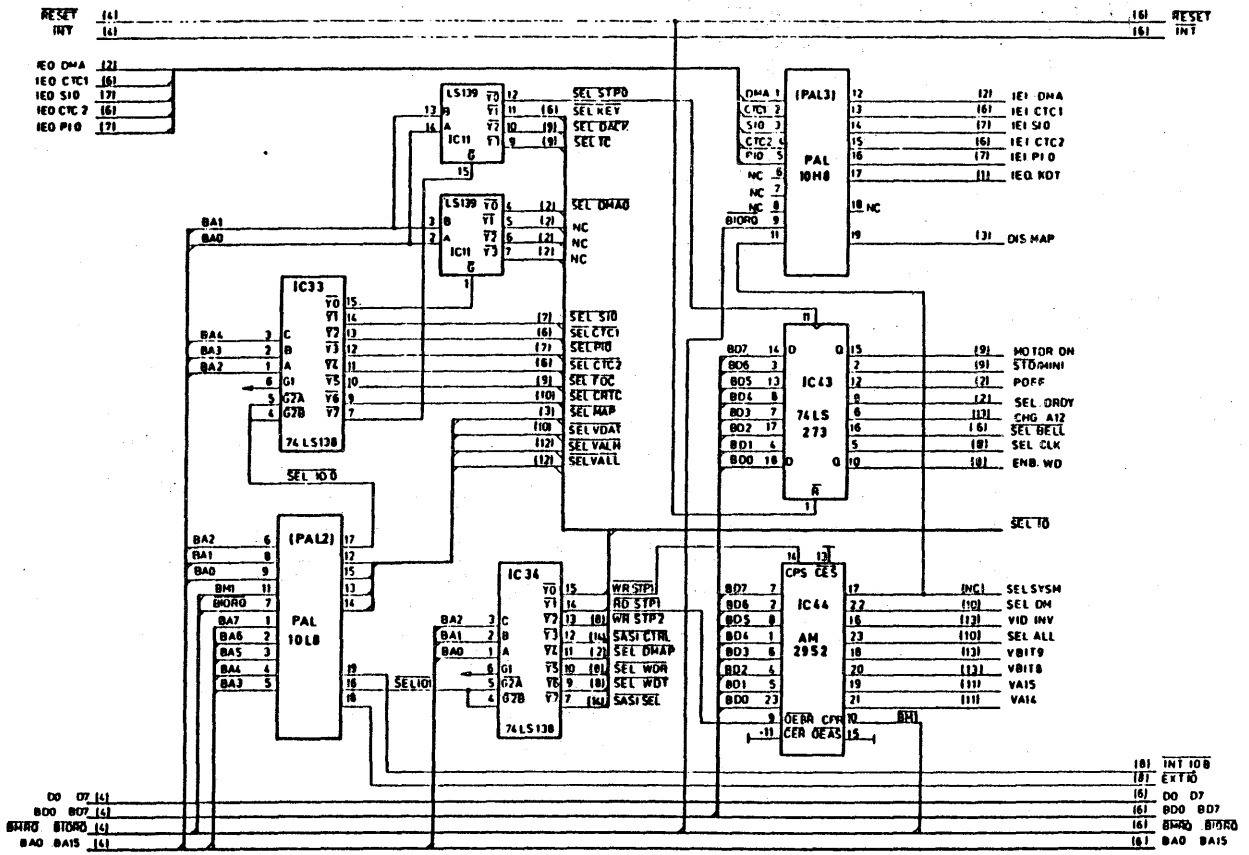

BUSAK
RESET
INT
EXT DMA
MBA 23
MBA 22
MBA 21
MBA 20
MBA 19
MBA 18
MBA 17
MBA 16
DIS MAP
SEL MAP
TTL CLK
MAP00
MAP01
MAP02
MAP03
PROM2
PROM1
D0 D7
BD0 BD7
BARQ BRFSH
BA0 BA15
IC 17
LS 107
LS107
IC 8
74 LS 244
IC 10
74LS612
od
74LS610
LS14
IC 3
74 LS 245
(PAL1)
PAL 12L6
STROBE
R/W
CS
WE
C
Vcc
GND
TP8/9
TP 5/6
TPK
R36
R35
R18
R19
R20
RAS3
RAS2
RAS1
RAS0
INT MEM
SEL RAM
MURS
CAS
MBA12
MBA13
MBA14
MBA15
XA23
XA22
XA21
XA20
XA19
XA18
XA17
XA16
A-24
A-23
A-22
A-21
A-20
A-19
A-18
A-17
KDT 6
1010
KONTRON ELECTRONIC
SPIES



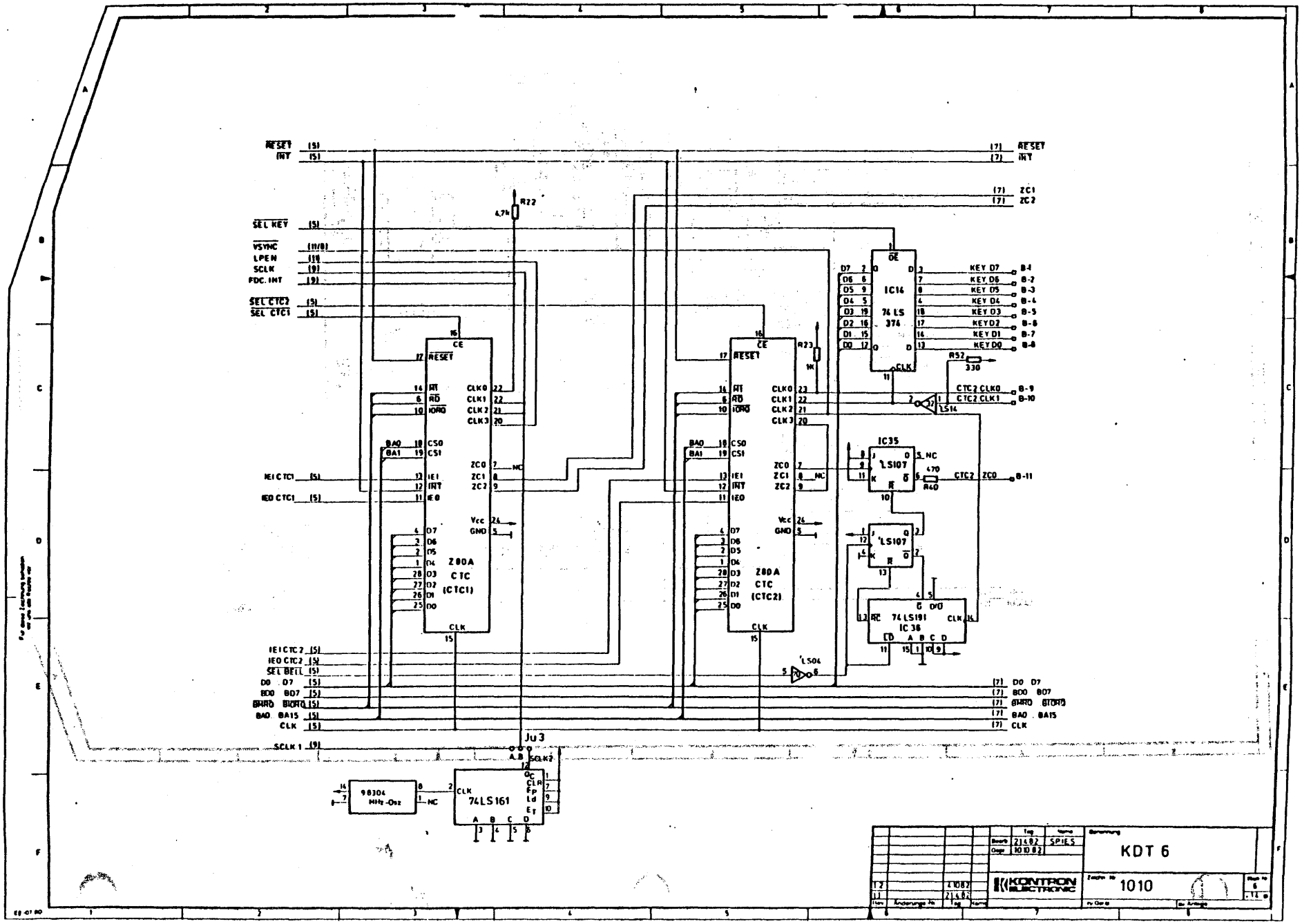
		Tag	Name	Benennung
	Bearb	4.10.82	SPIES	KDT 6
	Gepr	10.10.82		
KONTRON ELECTRONIC				Zeichn.-Nr 1010
12		4.10.82		Plan Nr
11		21.4.82		
Rev	Änderungs-Nr	Tag	Name	zu Gen.-Nr / zu Anlage

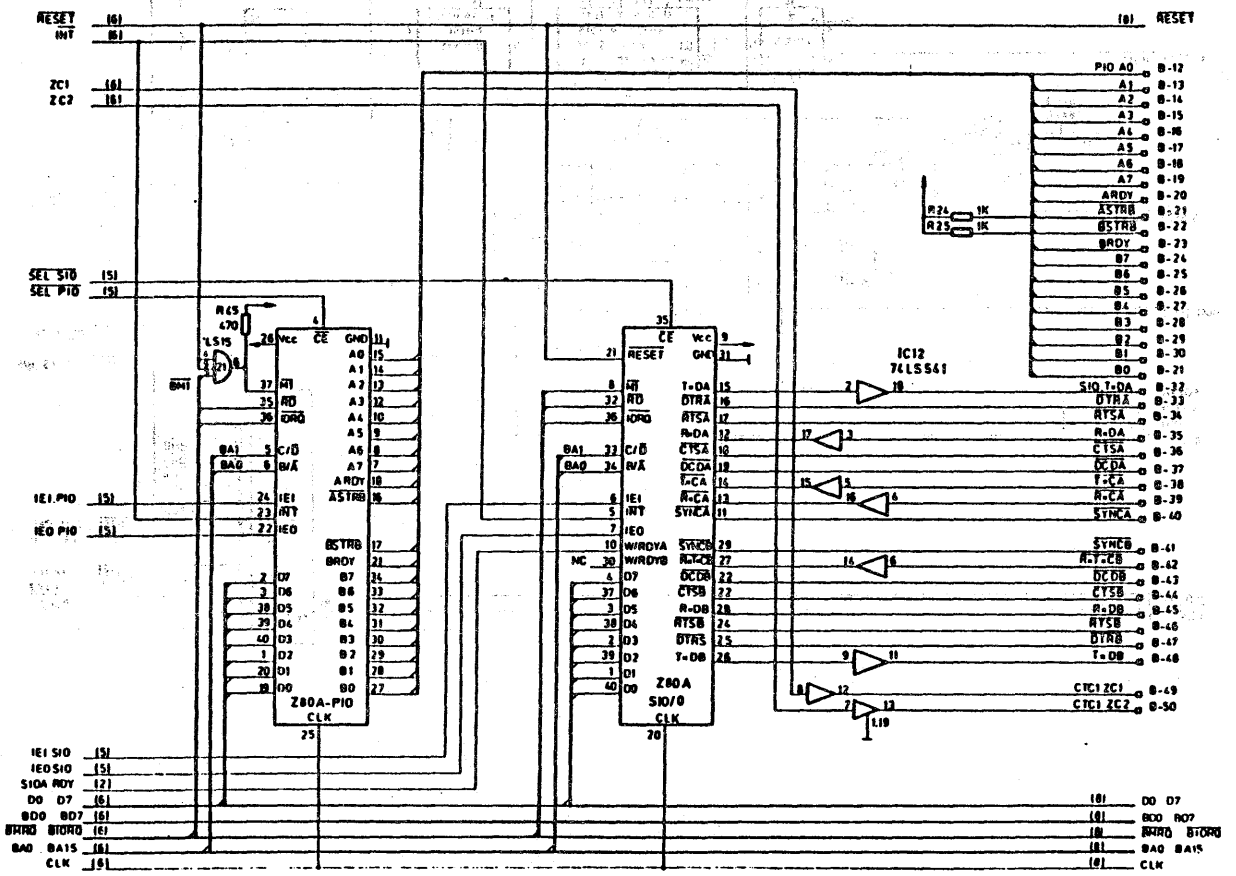
EE-07 80


RESET (3)
INT (3)
SEL RAM (3)
RAS3 (3)
RAS2 (3)
RAS1 (3)
RAS0 (3)
CAS (3)
MUX5 (3)
DO... D7 (3)
BDO... BD7 (3)
BA0... BA15 (3)
(5) RESET
(5) INT
(5) DO.. D7
(5) BDO.. BD7
(5) BA0 BA15
74S 157 IC27
74S 157 IC25
AM 2966 IC62
RAM (2164) Bit0
BANK 3
BANK 2
BANK 1
BANK 0
0,1µF pro 2164
IC 26
74LS541
KONTRON ELECTRONIC
KDT 6
Zeichn.-Nr 1010
Plan Nr 4
Bearb 4.10.82
Gepr 10.10.82
Rev Änderungs-Nr Tag Name
12 4.10.82
11 21.4.82
EE-07 80

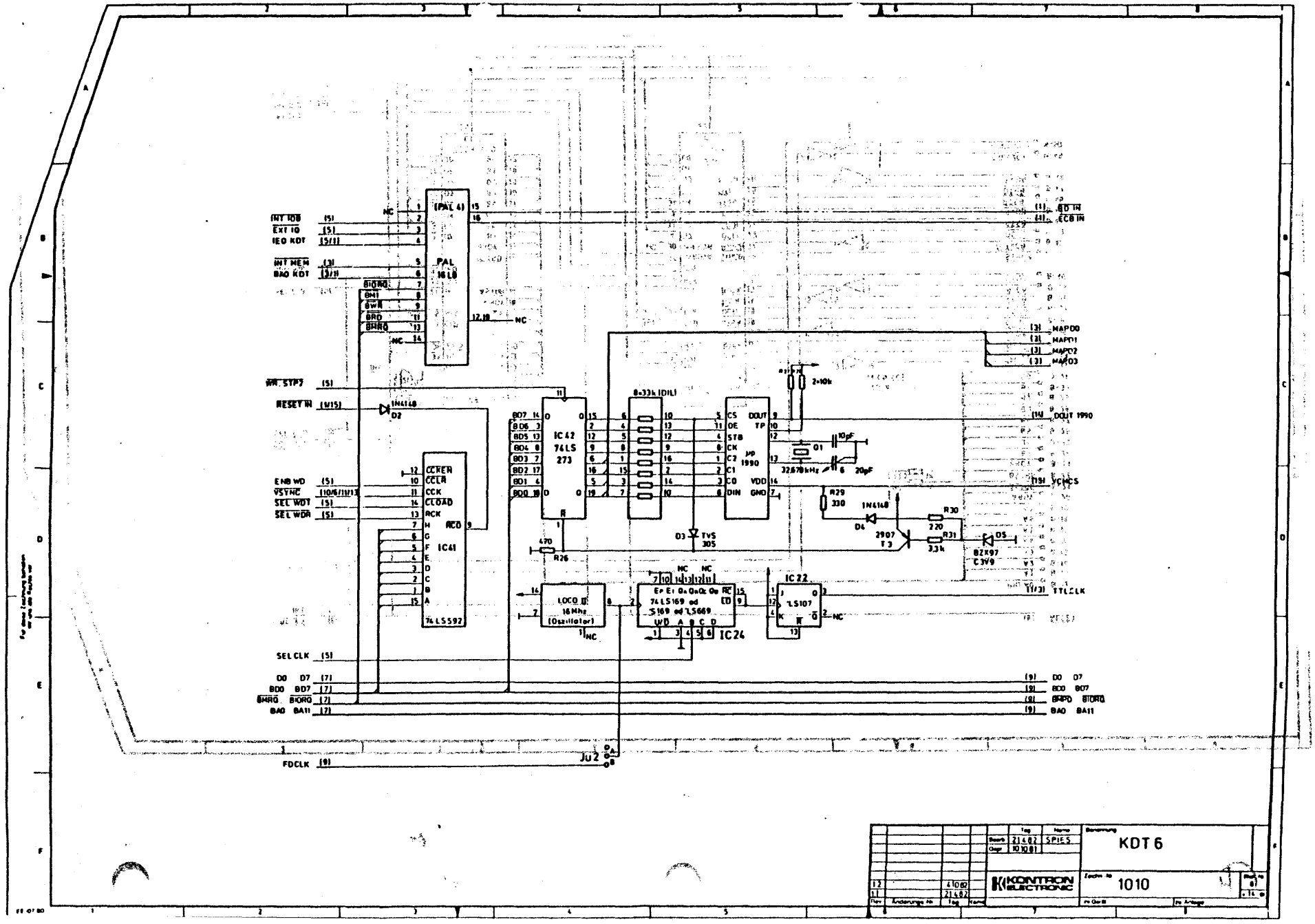


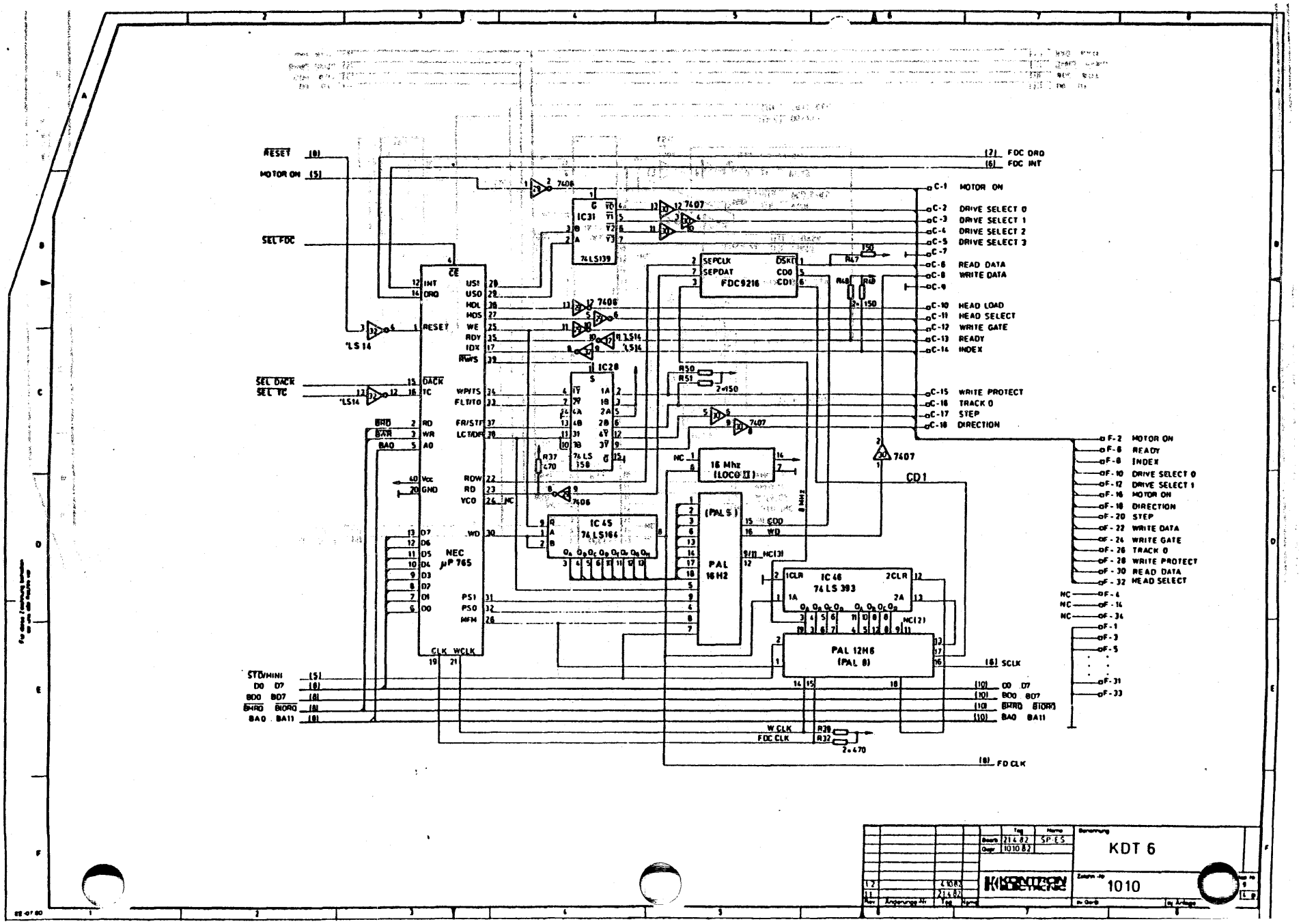
		Tag	Name	Benennung
		Bearb. 21.4.82	SPIES	KDT6
		Gepr. 30.10.82		
12	4108		KONTRON ELECTRONIC	Zeichn.-Nr. 1010
11	21.4.82			
Ind.	Änderung Nr.	Tag	Name	Ersatz für	Ersatz durch

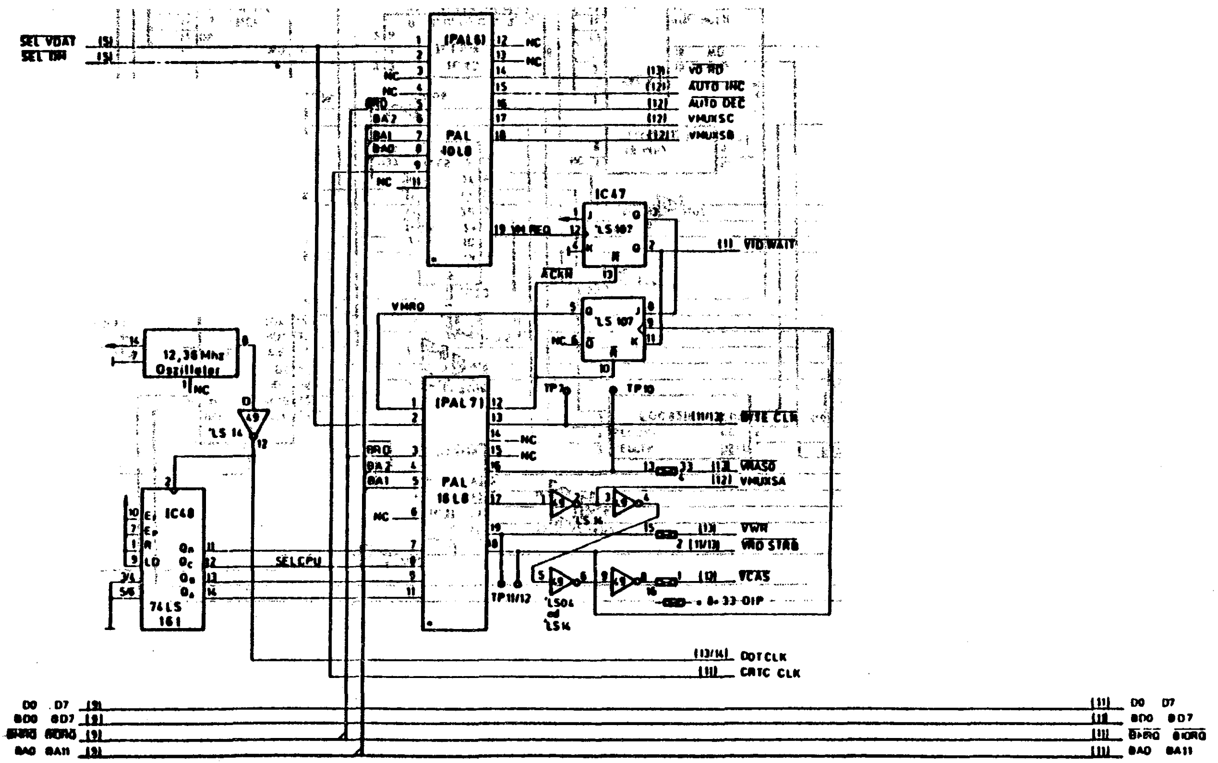

RESET
INT
SEL KEY
VSYNC
LPEN
SCLK
FDC. INT
SEL CTC2
SEL CTC1
IEI CTC1
IEO CTC1
IEI CTC2
IEO CTC2
SEL BELL
D0 D7
BD0 BD7
BWRD BDIRD
BA0 BA15
CLK
SCLK 1
R22
4,7k
R23
1k
R52
330
R40
470
Z80A CTC (CTC1)
Z80A CTC (CTC2)
IC16
74 LS 374
KEY D7
KEY D6
KEY D5
KEY D4
KEY D3
KEY D2
KEY D1
KEY D0
CTC2 CLK0
CTC2 CLK1
LS14
IC35
LS107
CTC2 ZC0
LS04
IC36
74LS191
Ju3
9,8304 MHz-Osz
74LS161
KDT 6
1010
KONTRON ELECTRONIC
SPIES



			Tag	Name	Benennung
			Bearb.	21.4.82	SPIES	KDT 6
			Gepr.	10.10.82		
12		4.10.82	KONTRON ELECTRONIC		Zeichn. Nr. 1010	Blatt Nr. 7
11		21.4.82				24
Rev.	Änderungs-Nr.	Tag	Name		Nr. Übertr.	Nr. Auftrags


INT IOB
EXT IO
IEO KDT
INT MEM
BAO KDT
BIORQ
BRD
BWR
BMRQ
PAL 16 L8
WR STP7
RESET IN
D2
IN4148
IC42 74LS 273
8=33k (DIL)
μP 1990
CS DOUT
OE TP
STB
CK
C2
C1
CO VDD
DIN GND
2=10k
10pF
32.768kHz
20pF
R29 330
R30 220
R31 33k
D4 2907 T3
D5 BZX97 C3V9
D3 TVS 30S
R26 470
ENB WD
VSYNC
SEL WDT
SEL WDR
IC41 74LS597
LOCO IO 16 MHz (Oszillator)
IC24 74LS169 od S169 od LS669
IC22 LS107
SEL CLK
D0 D7
BD0 BD7
BMRQ BIORQ
BA0 BA11
FDCLK
JU2
MAP00
MAP01
MAP02
MAP03
DOUT 1990
TTLCLK
KONTRON ELECTRONIC
KDT 6
1010

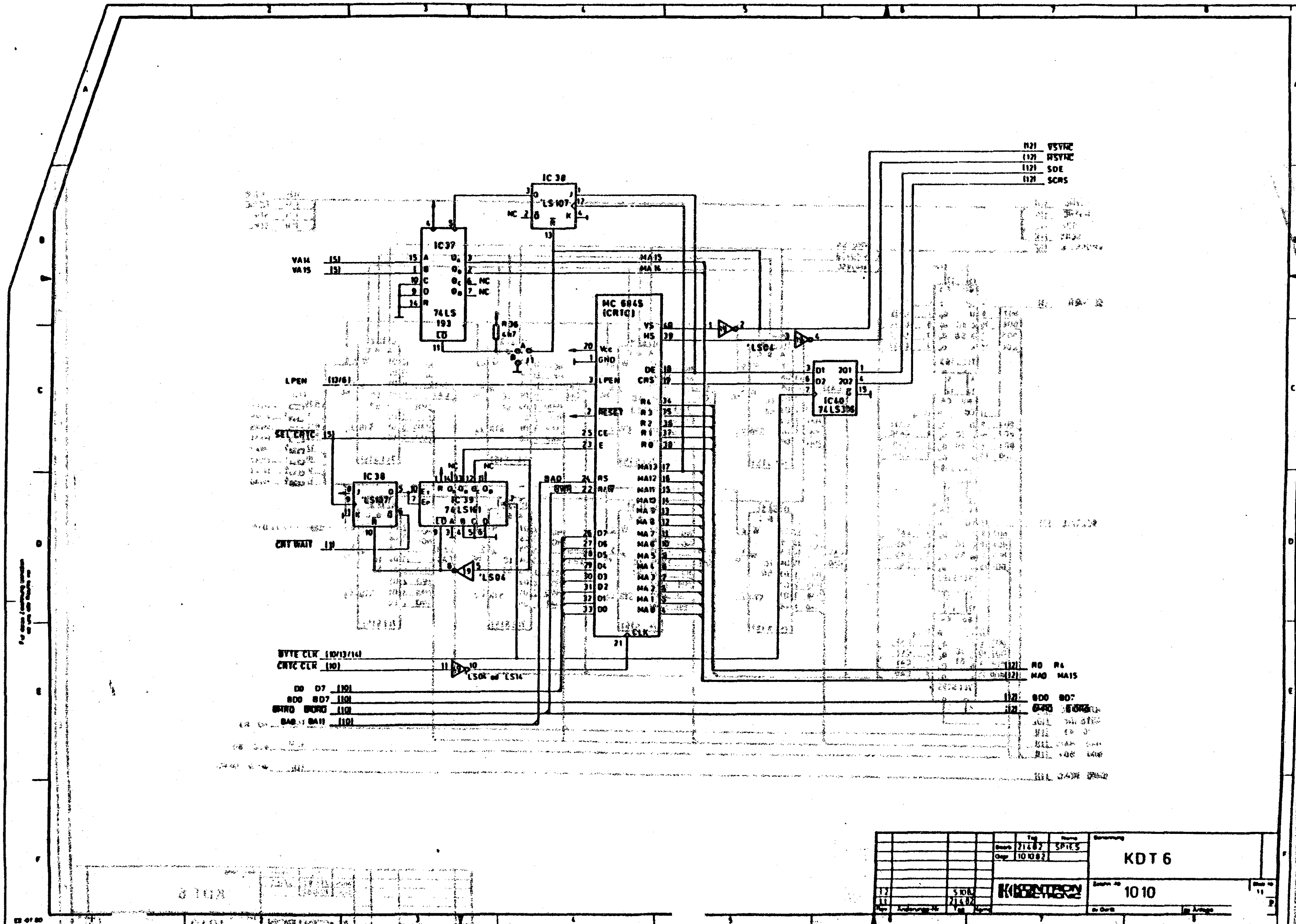

RESET
MOTOR ON
SEL FDC
SEL DACK
SEL TC
FDC DRQ
FDC INT
C-1 MOTOR ON
C-2 DRIVE SELECT 0
C-3 DRIVE SELECT 1
C-4 DRIVE SELECT 2
C-5 DRIVE SELECT 3
C-6 READ DATA
C-8 WRITE DATA
C-10 HEAD LOAD
C-11 HEAD SELECT
C-12 WRITE GATE
C-13 READY
C-14 INDEX
C-15 WRITE PROTECT
C-16 TRACK 0
C-17 STEP
C-18 DIRECTION
IC31
74LS139
IC28
74LS 158
IC45
74LS166
IC46
74 LS 393
FDC9216
NEC µP 765
PAL 16H2
PAL 12H6 (PAL 8)
16 Mhz (LOCO II)
CD1
F-2 MOTOR ON
F-6 READY
F-8 INDEX
F-10 DRIVE SELECT 0
F-12 DRIVE SELECT 1
F-16 MOTOR ON
F-18 DIRECTION
F-20 STEP
F-22 WRITE DATA
F-24 WRITE GATE
F-26 TRACK 0
F-28 WRITE PROTECT
F-30 READ DATA
F-32 HEAD SELECT
STÖRMINI
SCLK
FD CLK
W CLK
FDC CLK
KDT 6
1010



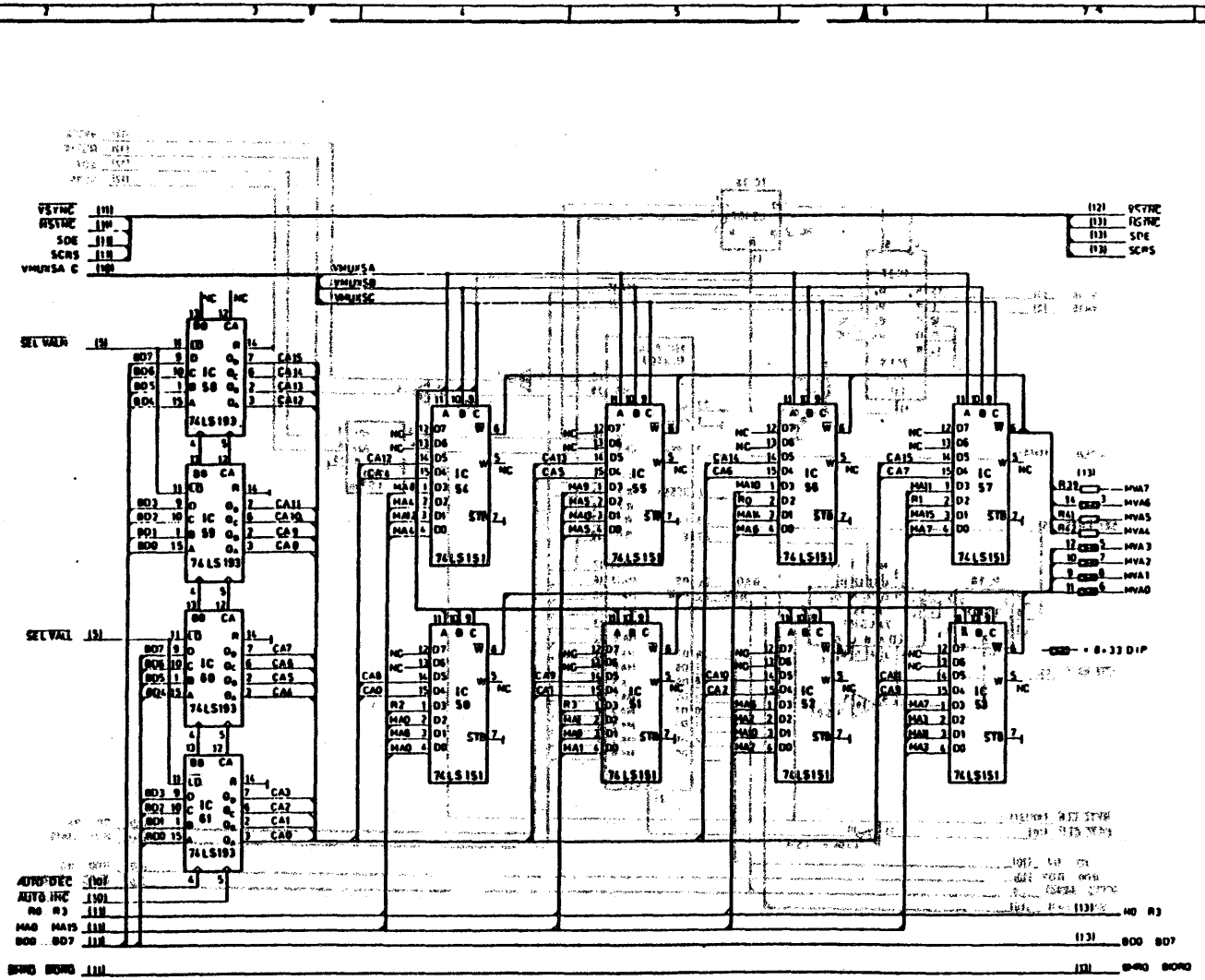
KDT 6

KONTRON ELECTRONIC

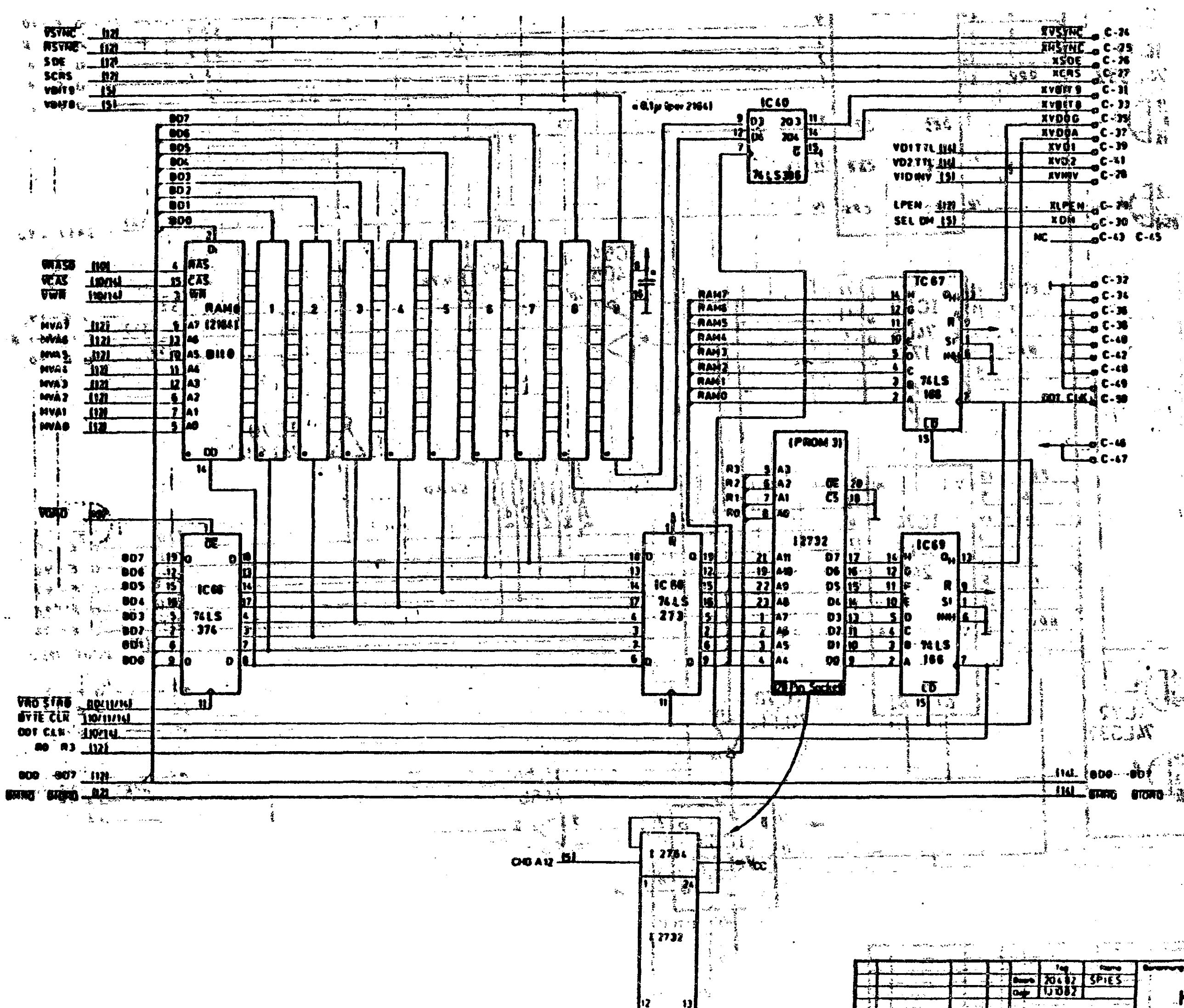
1010



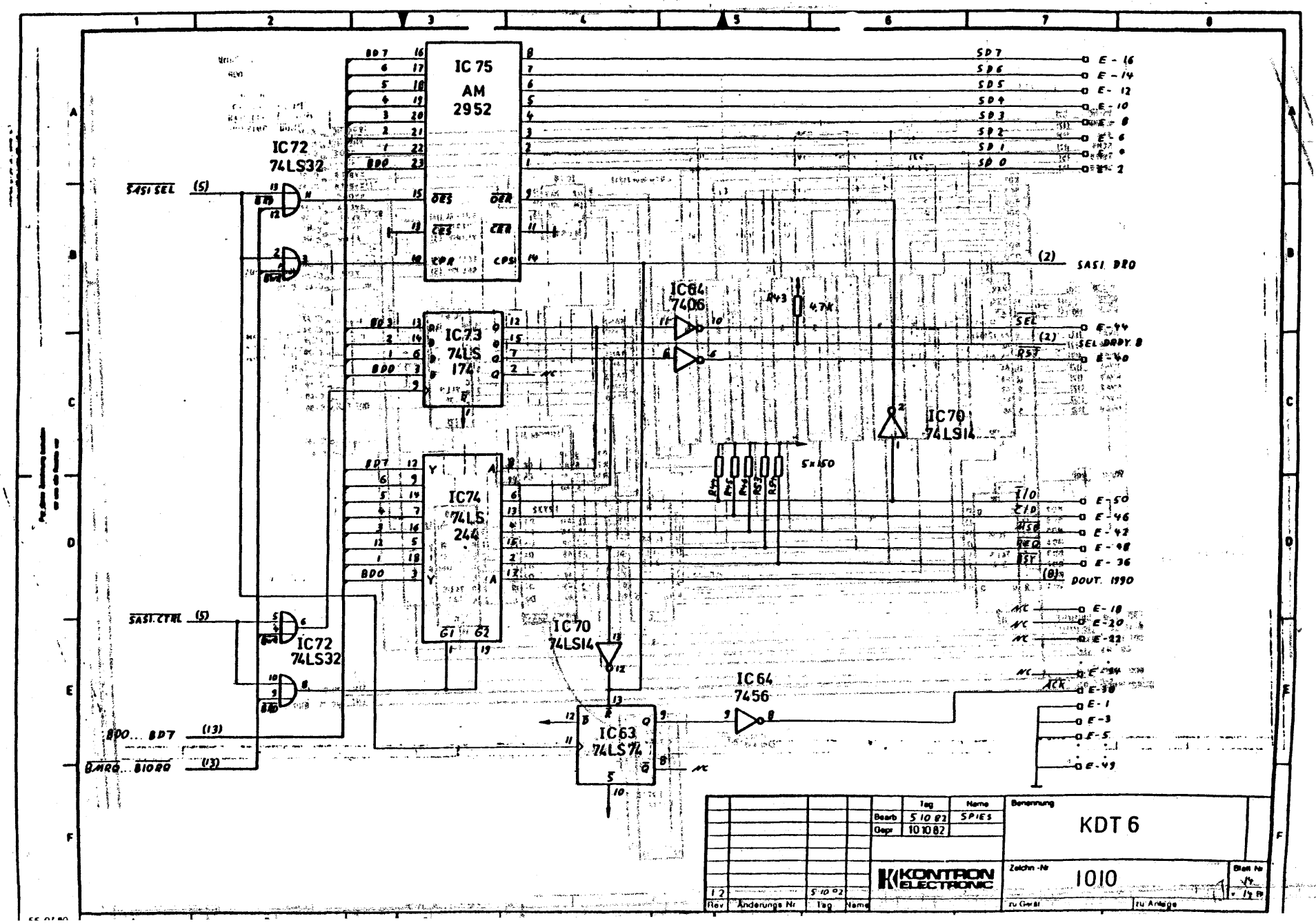
IC 38
LS107
IC37
74LS
193
VA14
VA15
R36
4k7
MC 6845
(CRTC)
LPEN
RESET
SEL CRTC
IC 38
LS107
IC 39
74LS161
CRT WAIT
'LS04
BYTE CLK
CRTC CLK
LS04 od. LS14
D0 D7
BD0 BD7
BA0 BA11
VSYNC
HSYNC
SDE
SCRS
IC40
74LS
R0 R4
MA0 MA15
BD0 BD7
KDT 6
KONTRON ELEKTRONIK
1010


VSYNC
HSYNC
SDE
SCRS
SEL VAL
74LS193
74LS151
AUTO DEC
AUTO INC
MA0 MA15
BD0 BD7
BIRQ BORQ
MVA7
MVA6
MVA5
MVA4
MVA3
MVA2
MVA1
MVA0
8-33 DIP

					KDT 6
					1010



Tag	Name	
20.4.82	SPIES	KDT 6
1.0.82		
5.10.82	KONTRON ELECTRONIC	1010
20.4.82		


IC 75
AM
2952
IC72
74LS32
IC73
74LS
174
IC74
74LS
244
IC64
7406
IC70
74LS14
IC70
74LS14
IC64
7456
IC63
74LS74
IC72
74LS32
SASI SEL (5)
SASI CTRL (5)
BDO... BD7 (13)
BMRQ... BIORQ (13)
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
(2) SASI DRQ
SEL
(2) SEL BODY B
RST
(8) DOUT 1990
ACK
5x150
KONTRON ELECTRONIC
KDT 6
1010
Bearb
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SPIES
5 10 82
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