



TRAQ
Reference Manual

Proprietary Statement

Notice is hereby given that all data contained in, revealed by, or shown on this document, whether a drawing or other writing, is proprietary and belongs to DSP TECHNOLOGY INC., Fremont, California. It is furnished and received in confidence solely for information purposes or procurement of the product to which it relates. Neither the document nor any information/data contained in it shall be used for any other purpose or duplicated or disclosed in whole or in part to anyone else without the prior written authorization of DSP TECHNOLOGY INC. in each instance. If such written authorization be given by DSPT, any disclosure or revelation by the recipient to anyone else shall be accompanied by a written statement incorporating the language and contents of this legend.

TABLE OF CONTENTS

Section 1 TRAQ System.....	1
System Description.....	1..
TRAQ Controllers.....	2...
TRAQ Memories	3...
Analog-To-Digital Converters.....	4..
Digital-to-Digital Converters	5..
Typical TRAQ Configurations.....	5..
TRAQ Current and Power Requirements.....	6.
TRAQ Installation.....	7...
System Interconnections.....	7...
Section 2 4012 and 4032 TRAQ Controllers.....	11
General Description.....	11..
Model 4012P and Model 4032P.....	12.
Models 4012 and 4032 Differences.....	13
System Diagnostics.....	13..
Section 3 Front Panel Indicators	15
Alphanumeric LED Indicators.....	15.
Front Panel LED Indicators.....	21.
Front Panel Switch Controls.....	22.
Front Panel Signals.....	23..
Model 4012P and Model 4032P Rear Panel Signals.....	24
Front and Rear Panel Flat Cable Bus Connectors.....	25

Section 4 Programming the 4012/4032 Control Registers.....	27
CAMAC Control.....	27..
Controlling Sampling and Data Readout From CAMAC.....	30
Section 5 Writing Common 4012/4032 Control Registers.....	31
Data Streamout.....	35..
Data Streamout with Auto-restart.....	36
Section 6 Model 4012 Control Registers	39
Section 7 4032 Control Registers.....	43
Section 8 Reading the 4012/4032 Control Registers	49
Model 4012 Only.....	53..
Model 4032 Only.....	53..
Section 9 Diagnostics.....	55
Section 10 Switch Options	65
CLK2 16th Bit Set.....	65..
Installation of TRAQ Firmware.....	66
Section 11 Series 5000 Memory Modules.....	67
General Description.....	67..
Front Panel Indicators and Controls.....	67
LED Indicators.....	67..
Module ID Switches	68..
Module Switch Settings.....	69..
Input Signal (5200 Series Only).....	69
Write Lock.....	70..
Section 12 TRAQ Digitizer Modules.....	71

TRAQ Digitizer Module Specifications.....	72
Temperature Range.....	72
Front Panel Description.....	73
LED Indicators.....	73
Module ID Switches.....	73
Input Signal Connectors.....	74
Bipolar/Unipolar Input Option.....	74
Input Signal Connection.....	75
2812M.....	76
Signal Conditioning.....	76
Section 13 Data Acquisition Module.....	79
Model 2812 12 bit/100 kHz/8 Channel ADC.....	79
Bipolar/Unipolar Signal Input Options.....	79
Bipolar Calibration and Alignment.....	79
Unipolar Calibration and Alignment.....	80
Common Mode Rejection.....	81
Model 2814 14 bit/100 kHz/4 Channel ADC.....	81
Bipolar Calibration and Alignment.....	81
Model 2840 14 bit/1 mHz/4 Channel ADC.....	81
Bipolar Calibration and Alignment.....	81
Model 2824 12 bit/2 mHz/1 Channel ADC.....	82
Bipolar Calibration and Alignment.....	82
Unipolar Calibration and Alignment.....	83

Model 2860 12 bit/1 mHz/4 Channel ADC.....	83
Bipolar/Unipolar Signal Input Options	83
Bipolar.....	83..
Unipolar	83..
Calibration and Alignment.....	83.
Bipolar Mode Calibration.....	83.

Appendices

Schematics

Index



SECTION 1

TRAQ SYSTEM

System Description

DSP Technology's TRAQ system is a modular product which acquires analog or digital data from multiple input channels and stores the information in local memory at rates up to 8 million data samples per second. Modular memory and analog digitizing (or digital interface) units allow easy system field expansion or reconfiguration.

Each TRAQ system is defined by one controller (4012 A or P; 4032 A or P), at least one memory module (5003, 5004, 5200..5032) and at least one digitizer module or input channel (2812, 2824, 2814, 2860...).

Data transferred from the digitizer modules to memory is initiated by a clock pulse which the controller generates from an internal crystal or an external signal. There are actually two selectable internal clocks (CLK1, CLK2) which can be controlled by the user. This allows selected portions of the data to be sampled at different rates. There are many instances where some portions of the data which has higher frequency components needs to be sampled at faster rates. The 4012/4032 will accept an external control signal which causes the unit to switch between the two clock frequencies. There is also available a mode which enables the controller to switch to the second frequency after detecting a "stop trigger." When the controller is sampling with the second clock (CLK2) the 16th bit of the data (MSB) can be set to a binary one. This allows the user to differentiate data sampled at the two clock rates.

NOTE

This option can be defeated by a jumper strap if the 16th bit is used by the digitizer unit. (See Section 10.)

Once the digitizer units receive the clock pulse (conversion command) all analog data is sampled simultaneously and digital data is stored in local digitizer buffer memories. Analog data is captured by sample & hold circuits which hold the signals constant as the analog to digital converters (ADCs) operate. Each sample & hold feeds directly into its own ADC. At the end of the conversion cycle, a signal is sent back to the controller

signaling that data is ready for readout. The controller then sequentially reads data for all required channels. The user can select the Number Of Channels (NOC) that are actively converting. As NOC is decreased the controller will allocate more memory storage for the active channels. Data is transferred sequentially as 16-bit words to the controller at a 8 Megasample/second rate. The controller double buffers the digitizer data, forming a 32-bit word which is stored in memory. When sampling is started the first data sample is stored at address zero of the memory and subsequent data at the next incremental memory location. After the memory is filled, new data is written over the previous data starting at address zero. This continues in a "round robin" fashion until a "stop trigger" is received. The "stop trigger" is either an external TTL signal, a front panel switch, or a computer command. This trigger initiates the "post trigger" sampling sequence which determines how much data is recorded before the trigger versus after the trigger. If "PTS" is set to "8/8" then all data is post trigger and sampling will stop once the entire memory is filled one more time. (i.e., if the memory size/channel is 32 K samples; another 32 K samples of data is recorded). If "PTS" = "0/8" then recording stops immediately and all the data was recorded before the time of the trigger. The controller allows the user not only to select the amount of memory per data channel, but also to divide this memory in 1/8th segments of post and pre-trigger data. The controller keeps track of where the earliest recorded sample resides in memory. All data read, or displayed starts from this sample.

After recording is complete the controller will display the data (through a digital-to-analog converter) or read it out to the computer. Data can be read starting at any 1024 block in the record. Also data readout can terminate at any point in the record and immediately go to another channel for readout.

TRAQ Controllers

The system controller is in command of all data acquisition. It communicates with the computer or user (through front panel controls) to determine the required sampling rate, pre/post trigger information, number of active data channels, memory allocation, data display and data readout. All control settings can be saved in a non-volatile memory to be restored on power-up. Communication with the computer is via the CAMAC bus; however, all data acquisition is passed through two private busses. Data from the input units is sequentially passed to the controller and then out to memory. The data is sequentially retrieved by the controller for display and readout.

The controller also executes a set of diagnostic routines on command or power up. These routines will usually catch and isolate any fatal system problem.

There are presently four controllers available for the TRAQ system:

Controller	TRAQ Memory Limitations	Comments
4012A	16 MegaSamples total; 4 MegaSamples/Channel	Standard Controller
4012P	16 MegaSamples total; 4 MegaSamples/Channel	Data retention on power down. (Requires battery backed-up TRAQ memory modules)
4032A	256 MegaSamples total; 256 MegaSamples/Channel	Standard Controller
4032P	256 MegaSamples total; 256 MegaSamples/Channel	Data retention on power down. (Requires battery backed-up TRAQ memory modules)

The 4012P/4032P units are used in environments where data retention upon loss of power is critical and they have extra control signals to protect acquired data. The 4012P has an optional reserved memory section for calibration data. These controllers are used with 5204 memory modules (internal batteries) or 5008 Bs, 5432 Bs (using external batteries).

TRAQ Memories

The amount of data storage in a TRAQ system depends on the selected controller and memory module.

Model	Memory Size (MegaSamples)	Max Modules/System	Comments
5004B	1	8	4012 or 4032 Controller
5005	2	4	4012 or 4032 Controller
5006	4	4	4012 or 4032 Controller
5007	6	1	4012 or 4032 Controller
5008	8	4	4012 or 4032 Controller
5408	8	8	4032 Controller
5416	16	8	4032 Controller
5424	24	8	4032 Controller

5432	32	8	4032 Controller
5204	0.5	8	4012 or 4032 Controller; Internal Battery Retention

 **NOTE**

5005..5008 and 5408..5432 are also available in B version for external battery backup.

All memory modules on a system should be of the same type. If modules are mixed, consult the factory for configuration information.

Analog-To-Digital Converters

A variety of analog to digital conversion units are currently available for the TRAQ system. A maximum of 256 digitizer channels can be run on one system but the total throughput rate cannot exceed 8 million samples per second. The total throughput is calculated as the product of the number of active digitizer channels times the sampling rate.

Presently the following units are available:

Model	Number of Channels/Module	Maximum Conversion Rate/Channel	Resolution
2812	8	100 KiloSamples/Sec	12
2814	4	100 KiloSamples/Sec	14
2824	1	2 MegaSamples/Sec	12
2840	4	1 MegaSamples/Sec	14
2860	4	1 MegaSamples/Sec	12

Digital-to-Digital Converters

Two modules, 2932 and 2904, are available for inputting digital information. The 2904 is used to record encoder signals from rotating devices and is not covered in this manual (see 2904 manual). The 2932 is a general purpose digital input module which will record two 16-bit TTL channels (32-bits) into TRAQ simultaneously with ADC data from the analog-to-digital channels. It also contains spare wire wrap socket space and a CAMAC interface for user customization.

Typical TRAQ Configurations

Controller	Memory	Allowable Memory Sizes	Max Number of ADC channels	
			2812	2860
4012 A/P	5004B	1 to 8 Meg	80	8
4032 A/P	5432	32 to 256 Meg	80	8

NOTE

This assumes that each channel of the

2812 is sampling at 100 kHz

2860 is sampling at 1 MHz

TRAQ Current and Power Requirements

Model	Current (amps)				Power (avg.)
	+6	-6	+24	-24	(Watts)
Controllers					
4012 (A/P)	4.0	0.05	0.05	0.05	27
4032 (A/P)	4.0		0.05	0.05	27
Memories					
5004B	2.5				15
5005	1.25				7.5
5006	1.5				9
5007	1.75				10.5
5008	2.0				12
5408	1.25				7.5
5416	1.5				9
5424	1.75				10.5
5432	2.25				13.5
Digitizers					
2812	1.5	0.55	0.150	0.150	20
2814	1.3		0.150	0.250	18
2824	1.0	0.70	0.100	0.100	15
2840	1.0		0.600	0.600	35
2860	1.7		0.250	0.270	20
2932	1.0				6
2904	2.0				12

TRAQ Installation

The minimum system configuration consists of one signal conversion channel (ADC), one controller, and 1 Megasample of memory. A CAMAC crate is also required and usually a crate controller to allow the TRAQ system to communicate with a computer. (Only one crate controller is required for each CAMAC crate).

System Interconnections

- 1) The memory modules are connected to the controller via a 50 pin flat cable. This cable plugs into the front panel TRAQBUS connectors. The memory modules usually reside to the left of the controller in the crate. This keeps the flat cable from interfering with the other controller signal cables. TRAQ systems are delivered with flat cables built for the system configuration ordered. If the system configuration is not specified, the cables will correspond to an equal distribution of ADC modules and memories.
- 2) During power-up diagnostics the controller will determine how much memory is on the bus. There must be at least 1024K words. The diagnostic routines will fail at the MEM1 test if no memory is found. Memory modules must have their I.D. switches set so that one module has ID=0, another ID=1, etc., (see Section 11, Memory Modules).
- 3) The modules can be located in any order in the crate relative to the controller. The 50-pin flat cable connector should be as short as possible to reduce bus noise and crosstalk. Refer to the memory module sections and the diagnostic section of this manual for further information regarding memory configurations.
- 4) The digitizer modules are connected to the controller through a 40 pin flat cable at the rear of the modules. This cable is also built for the system configuration originally ordered. The digitizer modules are usually installed to the right of the controller in the crate. The first digitizer module must have its ID. switch set to zero, the second to one, etc. The modules can be located in any order relative to the 4012/4032. For DSP digitizers (ex: 2812 ,8 channel ADC), channel 1 will correspond to channel 1 of the module with ID. switch set to zero; channel 9 will correspond to channel 1 of the module with ID. switch set to 1, etc.
- 5) After installing the units in the crate and connecting the two flat cable connectors, turn on the crate power. The controller will now sequence through a set of

diagnostics. If any problem is found the controller will display a "FAIL" message at the current diagnostic. Refer to the diagnostic part of the controller section.

 **NOTE**

The controller is not able to check the connection to the digitizer units. This can be checked by setting NOC to the maximum number of channels and CLK1 to the maximum conversion rate. Depress the "start" sampling switch and check that the "CVT" and "SEL" LEDs on the digitizer modules are on. Also the "DACV" LEDs on the memory modules should be on. If more than one memory module is present the "SEL" LEDs should be blinking on/off at a rate dependent on the sampling speed. If this fails check the cable interconnection between the controller and the digitizers.

- 6) A failed digitizer or memory can usually be determined without removing the interconnection cable. To locate a failed memory just change the ID to a number out of the contiguous memory address range (and the other memory IDs to fill in for the removed module), and repower the system.

EXAMPLE

Consider a four module memory system where the third module is suspected to have failed:

Module Number	ID Before	ID After
1	0	0
2	1	1
3	2	15
4	3	2

When the system is re-powered the controller will find only 3 modules in the system (the controller assumes that an empty address space means the end of the memory chain). If the system is now functional, module 3 has failed.

The digitizers can be checked in the same fashion except that it is not necessary to re-power the system. A failed digitizer can also be isolated by changing NOC. This will reduce the number of active channels and not address the modules with higher IDs.

- 7) When using the TRAQ system for transient recording there are several parameters that must be set carefully:
- a) NOC (number of active ADC channels) must be equal to or less than the number of actual digitizer channels. The 4012/4032 expects a "handshake" signal from each channel when transferring data and if no channel is present the controller will wait indefinitely for the handshake.
 - b) CLK1 or CLK2 must not be greater than the maximum conversion speed of the channels or else erroneous data will be recorded. Also, the user must be careful not to select a combination of NOC and CLK1, CLK2 which exceeds the maximum TRAQBUS speed of 8 megasamples/second. For instance,

$$\text{CLK1 (FREQUENCY)} \leq 8 \text{ MHz/NOC}$$

$$\text{CLK2 (FREQUENCY)} \leq 8 \text{ MHz/NOC}$$

EXAMPLE

Using 50 active channels of 2812 modules, each channel converting at 100 kHz gives:

$$(50 \text{ channels}) \times (100 \text{ KHz}) = 5000 \text{ kilo samples/second} \\ (5 \text{ megasamples/second})$$

which therefore does not exceed the maximum bus rate.

- c) Since the controller accommodates a large amount of memory/channel the user should be careful that "stop triggers" are not generated before sufficient

samples have been recorded or old and new data will be intermixed. This is especially true when $PTS = 0$ (all pre trigger information).

EXAMPLE

Consider using one active channel at 1 MHz ($NOC=1$, $CLK1 = 1$ MHz) and one megaword of memory. With these parameters it requires one second to sample all of memory. If $PTS=0$ and the "stop trigger" is received 1/2 second after sampling begins the last 1/2 of memory is never written into and will contain old data. If $PTS=8/8$ there is no problem as all the data (and all of memory) will be recorded after the "stop trigger" arrives.

SECTION 2

MODEL 4012 AND MODEL 4032 TRAQ CONTROLLERS OPERATIONAL DESCRIPTION

General Description

The DSP models 4012(A and P) and 4032 (A and P) TRAQ system controllers direct the flow of data between signal conversion units such as analog to digital converters (ADCs), scalars, etc. and memory storage units (Models 5004B, 5008). Up to 256 signal conversion channels can be controlled by one controller with a maximum TRAQBUS transfer rate of 8 million samples per second. Up to 16 megasamples of 16 bit data can be stored using a 4012 Controller and 256 megasamples using a 4032.

As the number of active channels are decreased the controller will allocate more memory to each channel. Also the controller allows the user to increase the number of active channels (NOC) in increments of two (except for NOC=1), i.e. NOC can be 1, 2, 4, 6, 8, 10..256. The memory size (record size) allocated to each channel is set by the controller and depends on the number of active channels and the total memory size. The user may select record sizes from the maximum memory/channel allowed down to 1024 samples. Once data acquisition is initiated the memory is written into continuously until a "**stop trigger**" is received which causes the controller to stop sampling after the correct number of post trigger samples have been recorded. The number of post-trigger samples is set in increments of 1/8 of the record size (0, 1/8, 2/8....8/8). The "**stop trigger**" is either an external TTL signal, front panel switch, or computer command.

After completion of sampling, data is either displayed (through a digital-to-analog converter) or read to the computer. The controller has an internal 12 bit digital-to-analog converter which allows the user to view a reconstructed analog waveform on an oscilloscope. A trigger is also provided to synchronize the display. Data is displayed or read starting at the earliest sample recorded. The user can select which channel to display or read. The controller displays all of the recorded data; however, data can be read by the computer starting at any 1K (1024) block.

Signal conversion units are DSP units such as Models 2812 and 2824. Two clock frequencies are available to accommodate switchable sampling rates and are controlled by either:

- 1) An external control signal "**CLK SWI**" which activates the first clock (CLK1) when the signal is at TTL low and the second clock (CLK2) when "**CLK SWI**" is TTL high.
- 2) The "**TRIG**" signal which causes the controller to start counting down the preset number of post-trigger samples. In this mode all pre-trigger samples are recorded using CLK1 and all post-trigger samples using CLK2.

The controller can also be clocked using an external user supplied signal. The sampling clock is available to synchronize other controllers.

All controller parameters can be set from front panel switches and through CAMAC from a computer. These parameters can be stored in nonvolatile memory and automatically reloaded on power-up. Also on power-up, the controller sequences through a series of diagnostics and notifies the user if a problem is detected (see DIAGNOSTIC section).

Models 4012P/4032P

The 4012P and 4032 P are special versions of the 4012A and 4032A. The systems differ from the standard units in that:

- 1) There is a "**LOCKOUT**" signal which can force the controllers to always be in the **LOCAL** control mode and lockout the remote computer.
- 2) There are two signals which if received in the correct order will start the controller digitizing:
 - a) "**MASTER ARM**"
 - b) "**MASTER ENABLED**"
- 3) The controllers record the memory address of the first sample digitized in a non-volatile memory chip. After power-up this address is restored and data can be displayed/read from the battery backed-up memory modules.
- 4) The 5204 memory modules used in these systems have an input signal "**WRITE LOCK**" which prohibits the controllers from overwriting the memories.

An additional calibration data block is available only for the 4012:

A 128K sample section of memory can be reserved for calibration data. If enabled, the 4012 will display a total memory size which is 128K less than on the TRAQBUS as this memory is reserved for calibration data only. When the unit is in the acquisition calibration mode, "ACQ CAL", data is digitized as usual, however, after recording is complete the last 2048 samples of data for each channel are transferred to the reserved memory section (approximately 1/2 second is required to transfer data for each channel). The only time data is ever written into the reserved memory section is during this transfer time. The acquisition mode "ACQ DATA" is the standard mode. Data can be read from both the calibration and data sections of memory depending which acquisition mode is enabled. This feature requires a minimum memory size of 256K samples and can be enabled or disabled from the front panel (MCAL function) or by the computer.

The 4012P and 4032P users must be sure that "4012 P" (or "4032 P") has been saved in the non-volatile RAM. On power-up the unit checks this control setting and aborts the memory diagnostics if "4012 P" is set, otherwise the data will be rewritten. The firmware also checks for a valid control setting; detection of an invalid control word forces a default setting to the "4012 A" mode but no memory diagnostics.

Model 4012 and Model 4032 Differences

The 4032 is an upgraded version of the 4012 and is able to read/write larger memory sizes. The 4012 is limited to 16 megasamples of storage while the 4032 is able to address 256 megasamples. The only functional differences are in the CAMAC control commands. (See **Programming the Control Registers Section**).

System Diagnostics


Whenever the controller's microprocessor is reset, either by the front panel reset button or a CAMAC Z (or C) command a series of diagnostic tests are performed. Failure to pass any of these test indicates the system is not functional (**refer to Diagnostic Test section**).



SECTION 3

FRONT PANEL INDICATORS AND CONTROLS



Alphanumeric LED Indicators



The controller has two alphanumeric LED displays which are controlled by two corresponding rotary switches. The **function** switch selects a control to be set and the **value** switch selects the control parameter to be used. As the **value** switch is incremented/decremented the new values are used by the internal processor to set control registers. Once sampling is initiated the values are locked-in and changing the switch values will only affect the next recording. If the controller is in remote mode only the local/remote control and the display channel can be changed. When the controller is initialized by a CAMAC clear (Z or C) or the front panel reset a series of diagnostic tests are performed (see diagnostic section). If any of these tests fail, a "FAIL" message will be displayed on the value LED with the corresponding test on the function LED. Failure to complete these tests indicates that the unit is not functional.


Function	Value	Description
ACQ	DATA	The unit is enabled to take data in the standard recording mode.
	CAL	The unit is enabled to take data for calibration recording. After calibration is complete the last 2048 samples for each channel are transferred to the reserved calibration memory. (4012 only)
CLKC	NONE	Both internal clocks (CLK1 & CLK2) and the external clock input are disabled.
	EXT	The external clock input is enabled and the internal clocks, CLK1 & CLK2, are disabled.
	INT	The internal clocks (CLK1 & CLK2) are enabled and the external clock input is disabled.
CKSW	NONE	Switching between CLK1 and CLK2 is disabled.
	FTRG	CLK1 is enabled when the SWI front panel input is TTL low. CLK2 is enabled when SWI is TTL high.  NOTE CLK1 is the normal sampling clock. When CLK2 is active the 16th bit of the data is set to 1.
	STRG	CLK2 is enabled after receipt of a stop trigger. (All post-trigger samples are taken with CLK2)

CLK1	5 MHz-10 Hz	Selects the sampling frequency for CLK1
		<p> NOTE</p> <p>Do not select a sampling speed greater than the maximum ADC conversion rate.</p>
CLK2	5 MHz-10 Hz	Selects the sampling frequency for CLK2
		<p> NOTES</p> <p>1) Do not select a sampling speed greater than the maximum ADC conversion rate.</p> <p>2) Whenever CLK2 is active the 16th bit (MSB) of the data is set to 1. (see DATA FORMAT section)</p>

Function	Value	Description
DISP	1..NOC	Displays recorded data from the selected channel through the "Display Out" front panel connector to an attached oscilloscope. NOC (number of active channels) is selected by the NOC control. The display is active only after sampling is complete and if there is no CAMAC readout. All data is displayed except when NOC = 1 which displays every other data sample.
INCR	1,10,100,1000	Selects the increment/decrement value used by MSCH.

MSCH	1..	<p>Displays the memory/channel (record size) in 1k blocks. Changing the value switch will increment or decrement the memory/channel by the amount selected in INCR. The minimum memory/channel is 1024 samples and the maximum is determined by the following algorithm:</p> $\text{MSCH}(\text{MAX}) = \text{INTEGER}(\text{MSTO}/\text{NOC})$ <p>NOC = NUMBER OF ACTIVE CHANNELS</p> <p>MSTO = TOTAL MEMORY SIZE</p> <hr/> <p><input checked="" type="checkbox"/> EXAMPLE</p> <p style="text-align: center;">MSTO = 256k : NOC = 6</p> <p style="text-align: center;">MSCH = INT(256k/6)</p> <p style="text-align: center;">= 42k</p> <p> NOTE</p> <p>The Total Memory Size (MSTO) Is Determined During The Power-Up Test Sequence.</p>
MSTO	Not Adjustable	<p>Displays the total memory size (1k blocks) which is determined during the power-up diagnostic test sequence.</p> <hr/> <p> NOTE</p> <p>The 4012P will display 128K less memory for MSTO than actually present if enabled for calibration memory ("MCAL YES") since 128K is the required memory to store the calibration data.</p>

Function	Value	Description
MODE	LOCL	Front panel controls are enabled and computer control is locked-out.
	RMOT	Computer control is enabled and front panel controls are locked-out.  NOTE The computer can override the LOCL control and change to RMOT. Also the front panel can override RMOT and change to LOCL. The display control can be set in RMOT mode.
4012 or 4032	A	Sets control firmware to run 4012A or 4032A code.
	P	Sets control firmware to run 4012P or 4032P code.
MCAL	NO	All TRAQ memory is used for data acquisition. (required for 4032 & 4032P units)
	YES	A 128K data block is reserved for calibration data.  NOTE Only available for 4012 units.

NOC	1,2,4,6..	Sets the number of active ADC channels.
	256	NOC can be set from one to the total number of available ADC channels. <hr/>  NOTE Do not set NOC greater than the total number of available ADC channels.
PREV	xxxx	Displays the current revision level of the microprocessor firmware. This message is only displayed after power-up diagnostics are completed.
PTS	0/8,1/8..	Sets the number of post-trigger samples in 1/8 intervals.
	8/8	0/8 : all data is recorded before the trigger. 1/8 : 1/8 of the data is recorded after the trigger , 7/8 before. 4/8 : 1/2 of the data will be recorded after the stop trigger; 1/2 before the trigger 8/8: all of the channel's data will be recorded after the stop trigger.


SAVE	[blank] or DONE	<p>Saves the control parameters in the non- volatile RAM memory. Turning the value switch one position forward or backwards causes the control parameters to be stored and the message "DONE" to be displayed. On power-up the unit will use these settings for the control registers.</p> <p>If on power-up the non-volatile RAM containing the control settings has incorrect settings, the Controller will default to the following control values:</p> <p>ACQ : DAT</p> <p>CLKC : INT</p> <p>CKSW : NONE</p> <p>CLK1 : 100 KHz</p> <p>CLK2 : 100 KHz</p> <p>MSCH : Full record size</p> <p>4012 : A</p> <p>MCAL : NO</p> <p>MODE : LOCAL</p> <p>NOC : 1</p> <p>PTS : 8/8</p>
-------------	--------------------	--

Front Panel LED Indicators

N	Momentary LED. On for approximately 1/2 sec when the Controller is addressed by the CAMAC dataway.
MST	Not Used

LOC	On when the controller is in local mode off when in remote mode.
CVT	On when the controller is recording data.

Front Panel Switch Controls

START/ STOP	<p>Two position momentary switch. The "START" position starts sampling, and the "STOP" position generates a stop trigger (equivalent to the front panel trigger input). The controller will initiate or reinstate sampling any time "START" sampling is depressed. After "STOP" sampling is depressed, no further stop triggers will be acknowledged (until sampling is restarted.)</p> <hr/> <p> NOTE</p> <p>This switch is not active in the remote mode.</p>
RST	Resets the microprocessor and initiates the power-up diagnostic sequences.

Front Panel Signals

(The following signals use LEMO, single pin, coax connectors)

DISPLAY OUT	<p>Analog output, approximately ± 10 Volts max into 1 Kohm minimum. Displays a reconstructed 12 bit waveform of the recorded data. ADC data is shifted by 2 LSBS (divided by 4) before displaying. Data from 14-bit converters only displays the upper 12 bits; data from 12 bit converters displays only the upper 10 bits. The full scale display ranges for these ADCs are:</p> <p>1) 14 bit converters:</p> <p style="padding-left: 40px;">+10V = ADC +full scale.</p> <p style="padding-left: 40px;">-10V = ADC -full scale.</p> <p>2) 12 bit converters :</p> <p style="padding-left: 40px;">+2.5V = ADC +full scale.</p> <p style="padding-left: 40px;">-2.5V = ADC -full scale.</p> <p>The channel to be displayed is controlled by the front panel switches or CAMAC. At the beginning of each sweep there is approximately a 100 μsec. dead time during which no data is displayed. When there is only one active channel (NOC=1) every other data point is displayed. For all other cases all of the data is displayed.</p>
SYNCH	<p>TTL signal out, into 1 Kohm minimum. The positive edge is synchronized to the beginning of the display sweep.</p>
TRIG	<p>Stop trigger which initiates post-trigger sampling, positive edge sensitive. After receipt of the first positive edge all further transitions are ignored until sampling is re-initiated. Optically isolated, protected to ± 300 Volts, requires approximately 1 ma. of current at 3 Volts to activate.</p>

CLK IN	External clock which initiates sampling of all active ADC channels, positive edge sensitive, TTL, 1 Kohm impedance. The clock frequency may change arbitrarily but the user must insure glitch free transitions.
CLK OUT	TTL signal at the same frequency as the selected clock frequency (internal or external). Will drive one 50 ohm load.
CLK SWI	TTL signal which causes the sampling rate to change from CLK1 to CLK2 if enabled. 1 Kohm impedance, TTL low enables CLK1, TTL high enables CLK2.
BUS REG	Not Used

Model 4012P and Model 4032P Rear Panel Signals

(The following signals use LEMO, single pin, coax connectors)

ARM	Optically isolated, TTL signal, protected to ± 300 Volts. A high TTL level must be detected by the controller followed by MASTER ENABLE before digitizing will be initiated. There should be at least a 100 μ sec. time delay between assertion of MASTER ARM and MASTER ENABLE . Requires approximately 1 mA to activate at 3 Volts.
MASTER ENABLE	Optically isolated, TTL signal, protected to ± 300 Volts. A high TTL level must be detected after assertion of MASTER ARM before digitizing will be initiated. Requires approximately 1 mA to activate at 3 Volts.
MASTER LOCKOUT	Optically isolated, TTL signal, protected to ± 300 Volts. A low TTL (or absence of) signal forces the controller into the local control mode. A high TTL level allows the remote control level to be activated. Requires approximately 1 mA to activate at 3 Volts.

Front and Rear Panel Flat Cable Bus Connectors

TRAQBUS	50-pin connector, TTL signals. 32 bits of multiplexed data/address and 12 control signals. Transfers data from the TRAQ controller to memory modules or slave controllers.
ADCBUS	Rear panel, 40 pin, connector, TTL levels. Transfers data from signal conversion units to the TRAQ controller.



SECTION 4

PROGRAMMING THE 4012/4032 CONTROL REGISTERS

CAMAC Control

The following list describes the response of the 4012/4032 to the CAMAC dataway commands. All commands require N(station number) and return X=1 and Q=1 unless stated.

F(0)*A(0)	Read data from the requested command register (see READING the 4012 CONTROL REGISTERS).
F(2)*A(0)	Read data for the selected channel number. Each F(2)*A(0) command reads one data sample and increments TRAQ memory to read the next sample. Data transfer rates up to the maximum CAMAC rates. Before data readout can proceed the correct CAMAC commands must be issued.
F(3)*A(0)	Read module ID. ("4012" or "4032")
F(8)*A(0)	Returns Q=1 if the internal LAM is on, regardless if the LAM was enabled by F(26)*A(0) or not.
F(9)*A(0)	Start sampling. (Only in remote control mode). There is, approximately, a 500 μ sec delay from receipt of the F(9)*A(0) command to the actual start of sampling.
F(10)*A(0)	Reset LAM Turns the internal and external(CAMAC dataway) LAM off.
F(17)*A(0)	Selects a command register for reading/writing.(see WRITING the 4012 CONTROL REGISTERS, this section).
F(24)*A(0)	Disables the LAM (look-at-me) signal from the CAMAC dataway. However the internal status can be monitored by the F(8)*A(0) command (Q=1 returned if the internal LAM is on).

F(25)*A(0)	<p>Stop sampling (equivalent to then front panel" stop trigger").</p> <hr/> <p> NOTE</p> <p>The controller will respond to this command in both local and remote control modes.</p>
F(26)*A(0)	<p>Enables the internal LAM (look-at-me) signal onto the CAMAC dataway.</p>
Z/C	<p>Initializes the controller, resets the microprocessor, and starts power-up diagnostics.</p> <hr/> <p> NOTE</p> <p>The controller will respond to this command in both local and remote control modes.</p>
LAM	<p>LAM, look-at-me is generated when sampling is complete and when data is ready for readout (if in remote mode.)</p>

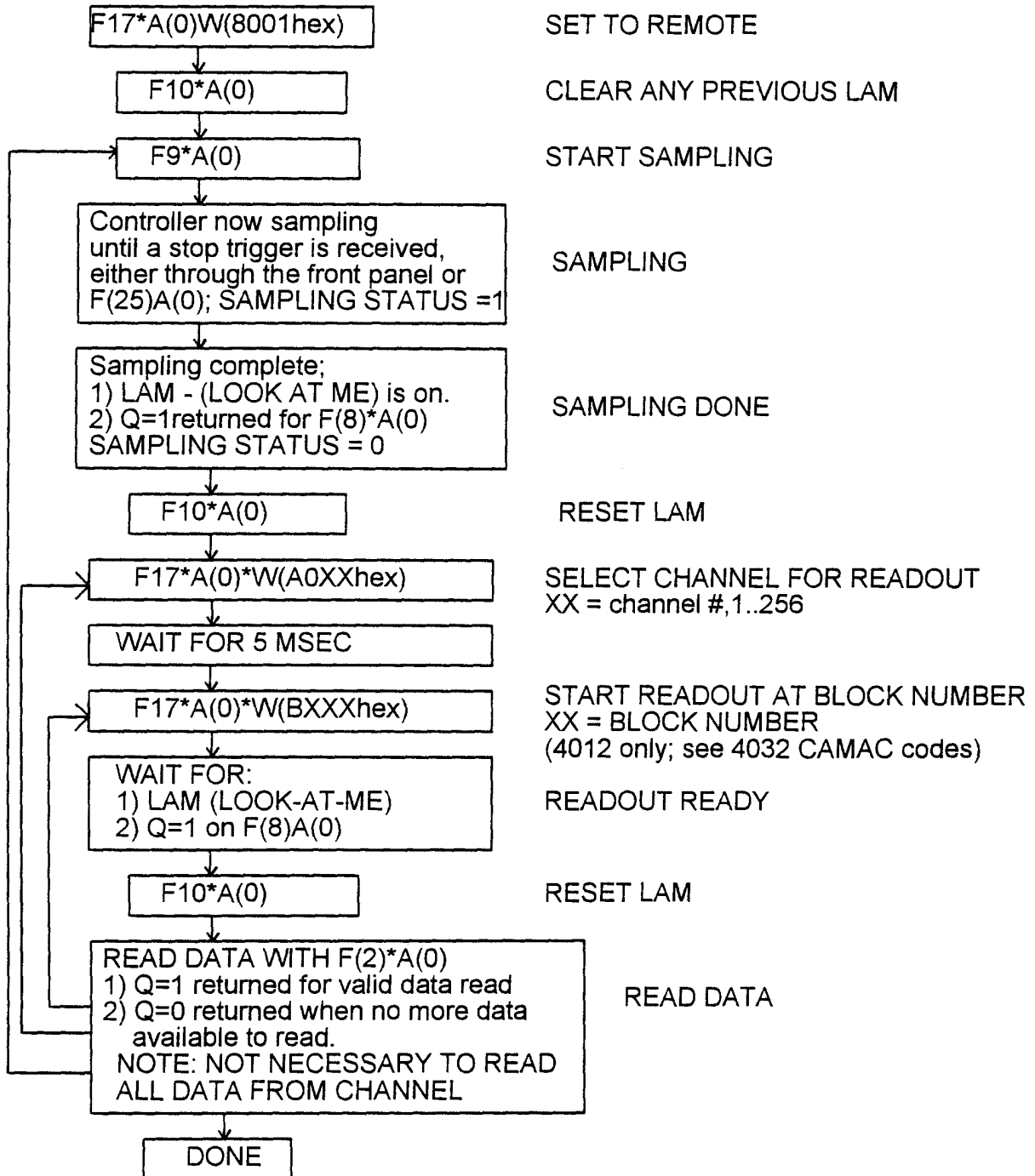
Control registers are programmed using the F(17)*A(0) command and W16-W1 CAMAC write lines. The W16-W13 lines address the control registers and W12-W1 contain the data to be loaded.

If the 4012/4032 controller is in the local control mode, only the local/remote (see 8 below) register can be changed. After commanding the unit to the remote mode all registers can be changed. As new values are programmed into the controller, the new values/functions are displayed on the front panel LEDs.

Since all command registers are read/written through the microprocessor there is a response time of approximately several hundred microseconds. The controller will respond with a Q=1 on F17*A(0) [F(0)*A(0)] if the unit is ready to accept (read) the command (data), otherwise a Q=0 is generated. When reading the control registers, which requires F(17)*A(0) to be followed by F(0)*A(0), both commands must be executed before the next F(17)*A(0) can be generated. It is recommended that a minimum of 500

μ sec delay be inserted between all commands which address the 4012 control registers. This applies for F (17), F(0), and F(9) commands.

Controlling Sampling and Data Readout From CAMAC



SECTION 5


WRITING COMMON 4012/4032 CONTROL REGISTERS

F(17)*A(0)*[(W16..W13 = Command) (W12..W1 = Data)]

 **NOTE**


COMMAND = upper 4 write bits (W16..W13) in hex



DATA = lower 12 write bits (W12..W1) in decimal


Function	Command	Data	Description
SET NUMBER OF ACTIVE CHANNELS	1	1, 2, 4,... 256	1=1 active ch. 2=2 active ch. : 256= 256 active ch.
			<p> NOTE</p> <p>Do not program more active channels than the total number of ADC channels, otherwise the controller will always be waiting for a "conversion complete" signal from the erroneous channels</p>

SET NUMBER OF POST-TRIGGER FRACTION SAMPLES	2	0,1,2,...8	<p>0 = No post-trigger samples -sampling , stops immediately after receipt of the "stop trigger".</p> <p>1 = 1/8 of the channels memory is sampled after receipt of "stop trigger"</p> <p>2 = 2/8 of the channels memory is</p> <p>3 = 3/8.</p> <p>...</p> <p>8 = all data is recorded after receipt of "stop trigger"</p>
--	---	------------	--

SET CLK1 FREQUENCY	4	0,1,...17	<p>0 = 5 MHz 1 = 2 MHz 2 = 1 MHz</p> <p>3 = 500 Khz 4 = 200 Khz 5 = 100 Khz</p> <p>6 = 50 Khz 7 = 20 Khz 8 = 10 Khz</p> <p>9 = 5 Khz 10 = 2 Khz 11 = 1 KHz</p> <p>12 = 500 Hz 13 = 200 Hz 14 = 100 Hz:</p> <p>15 = 50 Hz 16 = 20 Hz 17 = 10 Hz</p> <hr/> <p>NOTES</p> <ol style="list-style-type: none"> 1. If using FTRG and FTRIG is TTL high or a "stop trg" has been detected using STRG then CLK2 will be active. 2. Do not set CLK1 frequencies higher than the maximum conversion rate of the ADC modules.
---------------------------	---	-----------	--

SET CLK2 FREQUENCY	5	0,1,..17	<p>Same as CLK1</p> <hr/> <p> NOTES</p> <ol style="list-style-type: none"> 1. The W16 data bit is set to 1 (if enabled) for data sampled when CLK2 is active- see DATA FORMAT section 2. Do not set CLK2 frequencies higher than the maximum conversion rate of the ADC modules or the maximum transfer rate of the bus
SET CLOCK SWITCHING CONTROL	6	0,1,2	<p>0 = No switching from clock 1 to clock 2</p> <p>1 = Switch from clock 1 to clock 2 when front panel input signal "CLK SWI" is high [FTRG]</p> <p>2 = Switch from clock 1 to clock 2 when "STOP TRG" received [STRG]</p>
SET CLOCK CONTROL	7	0,1,2	<p>0 = Both external and internal clocks are disabled.</p> <p>1 = External clock (front panel input signal) is enabled; internal clocks are disabled.</p> <p>2 = Internal clocks are enabled and the external clock input is disabled.</p>

<p>SET LOCAL REMOTE CONTROL</p>	<p>8</p>	<p>0,1</p>	<p>0 = Set to local control mode</p> <p>1 = Set to remote control mode</p> <hr/> <p> NOTE</p> <p>If the controller is in the local control mode the computer may override and set to remote mode. This is required in order to set any other control registers or read data. Also, the LOCAL/REMOTE can be changed from the front panel</p>
<p>SET THE D/A OUTPUT DISPLAY CHANNEL</p>	<p>9</p>	<p>1, 2, 3, 4,5, ... 256</p>	<p>[Data(decimal):]</p> <p>1 = display channel 1</p> <p>2 = display channel 2</p> <p>...</p> <p>256 = display channel 256</p> <p>Displays data from the selected channel, (see "DISPLAY OUT," SIGNALS section).</p> <hr/> <p> NOTE</p> <p>Do not program a display channel greater than the number of active channels. If the controller is in the data readout mode then the display can be reactivated by reading out the last block of data in a channel until Q=0 is returned on the 1025th read cycle.</p>

SELECT A CHANNEL FOR READOUT 1,2,3,4,5...256	A	1, 2, 3, 4,5, ... 256, 512... 514	[Data(decimal):] 1 : Select channel 1 for readout 2 : Select channel 2 for readout . 256 : Select channel 256 for readout 512 : DATA STREAMOUT 513 : DATA STREAMOUT WITH AUTO RESTART 514 : MEMORY DUMP
	<div style="border-top: 1px solid black; padding-top: 5px;">  NOTE This command must be executed at least once before data readout can begin. It is not necessary to re-issue the command if the channel readout number is not changed. Do not program a channel number greater than the active number of channels. </div>		

Data Streamout

If the channel number = 512 then the controller will immediately enter the data streamout mode. Data is ready to read approximately 1.5 msec after issuing the command. This mode is useful for users who wish to read all TRAQ data without the overhead of setting up each channel and starting address (app. 3 msec). This mode reads data out in the following the following sequence:

Channel(NOC), Sample(1)

Channel(NOC-1), Sample(1)

Channel(1), Sample(1)
 Channel(NOC), Sample(2)
 Channel(NOC-1), Sample(2)
 .
 .
 .
 Channel(1), Sample(2),
 etc.

Data Streamout with Auto-restart

This mode allows the controller to continuously sample/read/sample... data. After the controller is commanded into this mode it will automatically enter the data readout mode after sampling is complete. The data is read in the same format as above. After the last data sample + 1 is read the Controller will automatically restart sampling. This mode is enabled until the channel readout number is changed from 513.

Data Dump: The entire memory is readout starting at address 0.

SET MODE 1 REGISTER	C	1,2,4,... 128	1 = ACQUISITION MODE = DATA 2 = ACQUISITION MODE = CALIBRATE (4012P only) 4 = ARM UNIT (P units only) 8 = STOP SAMPLING 16 = RUN 4012A CODE 32 = RUN 4012P CODE 64 = ENABLE CALIBRATION MEMORY 128= DISABLE CALIBRATION MEMORY (64,128 only for 4012P)

NOTES

Acquisition mode = data is the standard transient capture mode and is the default on power-up.

Acquisition mode = calibrate will transfer 2k samples/channel to the reserved memory after data is acquired.

Arm is the computer equivalent of the front panel MASTER ARM and must be (if in remote mode) before the Controller will accept the F(9) command start digitizing.

Stop Sampling - This command will cause the controller to stop sampling immediately; executing the following:

- a) The internal or external clock is immediately stopped.
- b) The controller waits approximately 100 μ sec after disabling the clocks to allow all ADC converters to finish converting data.
- c) The number of post-trigger samples is read by the controller.

If there have been no post-trigger samples (no stop trigger) then the earliest sample digitized is assumed to reside at the beginning of memory. The total number of samples converted is equal to the memory address of the last sample stored.

 **NOTE**

This will not be true if the memory address counters have wrapped around one time. It is advisable to use the forced stop mode only in all post-trigger mode. The user should be sure that a trigger is received before issuing this command.

If a stop trigger was received the total number of samples converted is equal to the number of programmed pre-trigger samples plus the number of post-trigger samples actually converted.

- a) The number of samples converted is stored in registers for readout. (see W=16, W=17 under READING THE CONTROL REGISTERS)

- b) If no post-trigger samples were recorded then a flag bit is stored to notify the user that no stop trigger was received. (see W=14 under READING THE CONTROL REGISTERS)

Run 4012A (4032A) code assumes the unit is a 4012A controller, 4012P a 4012P controller.

Enable/disable calibration memory reserves a 128K memory block for the calibration data.

SECTION 6

MODEL 4012 CONTROL REGISTERS ONLY

Function	Command	Data	Description
SET MEMORY/ CHANNEL	3	1...4095	<p>Set memory/channel in 1024K sample increments.</p> <p>The minimum memory/channel is 1K and the maximum is determined by the number of active channels(NOC) and the total memory size or 4095 increments (4,193,280 samples/channel).</p> <p>Maximum memory/channel = NOC * integer(MSTO/NOC) where:</p> <p>NOC = NUMBER OF ACTIVE CHANNELS (1,2,4,6...256)</p> <p>MSTO = TOTAL MEMORY SIZE (128K,256,...)</p> <p>MSTO is determined during the power-up diagnostic sequence. The 4012 will default to the maximum memory/channel for any value out of bounds.</p>

START DATA READOUT ADDRESS	B	1...4095	[Data(decimal):] 0= Start readout at earliest sample digitized 1 = " " " " " +1024 2 = " " " " " +2048 . N-1 " " " the last 1K memory block (N= MEMORY/CHANNEL ,1K BLOCKS; N(max) = 4095 blocks (sample 4,193,280).

 **NOTE**

The 4012 will not respond to this command unless the unit is both in the remote mode and sampling is complete. Data readout will start approximately 500 μ sec. after receipt of this command. A LAM will be generated when data is ready for readout.

The LAM should be reset ,F(10)*A(0), before readout begins. A Q=1 on F(2)*A(0) will be generated for valid read data. A Q=0 on F(2)*A(0) will be generated after all data from the selected channel has been read. Also, the 4012 will be in the display mode (front panel "DISPLAY OUT" active) until this command is received and will return to the display mode after the last 1K block of data has been read from the channel. It is not necessary to read all data from the channel before reading another channel or skipping to some other 1K data block.

SAVE CONTROL REGISTERS	D	0	All control settings are saved in the non-volatile memory and used as control parameters on power-up. The 4012 contains a non-volatile memory chip. The chip will retain the control parameters indefinitely but has a limited number of SAVE cycles (approximately 1000).
RESTORE CONTROL REGISTERS	E	0	Restores the control settings using the values stored in non-volatile memory. This is done automatically on power-up.
INITIATE POWER-UP DIAGNOSTIC TESTS	F	0	Allow approximately 3 seconds to execute. This test will reset the system (same as power-up). If using the 4012P firmware mode (see SET MODE REGISTER (12)) this test will NOT exercise TRAQ memories which would write overwrite data.

SECTION 7

4032 CONTROL REGISTERS ONLY

SET MEMORY/ CHANNEL LOWER	3	1...4095	Set lower 12 bits of the total Memory/Channel.
SET MEMORY/ CHANNEL UPPER	D	1...4095	Set upper 12 bits of the total Memory/Channel.

To set the 4032's MEMORY/CHANNEL requires using both:

- a) **SET MEMORY/CHANNEL LOWER**
- b) **SET MEMORY/CHANNEL UPPER**

SET MEMORY/CHANNEL UPPER and **SET MEMORY/CHANNEL LOWER**
combine to form the full MEMORY/CHANNEL (1k blocks) .

- 1) Use **SET MEMORY/CHANNEL UPPER** to set the upper 12 bits of
MEMORY/CHANNEL

- 2) Use **SET MEMORY/CHANNEL** to set the lower 12 bits of **MEMORY/CHANNEL**

 **NOTE**

SET MEMORY/CHANNEL UPPER must always be programmed first and always followed by **SET MEMORY/CHANNEL LOWER**

 **EXAMPLE**

Set **MEMORY/CHANNEL** to 8,389,632 Samples/Channel

- 1) $8,389,632/1024 = 8193$ (hex 2001) blocks of 1024 samples
 - 2) $\text{Int}[8193/4096] = 2$ (Data for **SET MEMORY/CHANNEL UPPER**)
 - 3) $8193 - 2 * 4096 = 1$ (Data for **SET MEMORY/CHANNEL LOWER**)
-

 **NOTE**

Maximum memory/channel = $\text{NOC} * \text{integer}(\text{MSTO}/\text{NOC})$
where:

NOC = NUMBER OF ACTIVE CHANNELS
(1,2,4,6...256)

MSTO = TOTAL MEMORY SIZE (128K,256,...)

MSTO is determined during the power-up diagnostic sequence. The 4032 will default to the maximum memory/channel for any value out of bounds.

START DATA READOUT ADDRESS LOWER	B	1.. 4095	Set lower 12 bits of the data channel readout block.
START DATA READOUT ADDRESS UPPER	E	1.. 4095	Set upper 12 bits of the data channel readout block.

To set the starting readout block number requires using both the

- a) **START DATA READOUT ADDRESS LOWER**
- b) **START DATA READOUT ADDRESS UPPER**

START DATA READOUT ADDRESS UPPER and **START DATA READOUT ADDRESS LOWER** combine to form the full start of data readout address (1k blocks) .

- 1) Use **START DATA READOUT ADDRESS UPPER** to set the upper 12 bits of the start address.
- 2) Use **START DATA READOUT ADDRESS LOWER** to set the lower 12 bits of start address.

 **NOTE**

START DATA READOUT ADDRESS UPPER must always be programmed first and always followed by **START DATA READOUT ADDRESS LOWER**.

EXAMPLE

Set start of readout to sample 8,389,632..

1) $8,389,632/1024 = 8193$ (hex 2001) blocks of 1024 samples

2) $\text{Int}[8193/4096] = 2$ (Data for **START DATA READOUT ADDRESS UPPER**)

3) $8193 - 2 * 4096 = 1$ (Data for **START DATA READOUT ADDRESS LOWER**)

NOTE

The 4032 will not respond to this command unless the unit is both in the remote mode and sampling is complete. Data readout will start approximately 500 $\mu\text{sec.}$ after receipt of this command. A LAM will be generated when data is ready for readout.

The LAM should be reset ,F(10)*A(0) before readout begins. A Q=1 on F(2)*A(0) will be generated for valid read data. A Q=0 on F(2)*A(0) will be generated after all data from the selected channel has been read. Also, the 4012 will be in the display mode (front panel "DISPLAY OUT" active) until this command is received and will return to the display mode after the last 1K block of data has been read from the channel. It is not necessary to read all data from the channel before reading another channel or skipping to some other 1K data block.

SET MODE 2 REGISTER	F	1,2,3	1 = SAVE CONTROL REGISTERS 2 = RESTORE CONTROL REGISTERS 3 = INITIATE POWER-UP DIAGNOSTIC TESTS
----------------------------	---	-------	---

SAVE CONTROL REGISTERS: All control settings are saved in the non-volatile memory and used as control parameters on power-up. The 4012 contains a non-volatile memory chip. The chip will retain the control parameters indefinitely but has a limited number of SAVE cycles (approximately 1000).

RESTORE CONTROL REGISTERS: Restores the control settings using the values stored in non-volatile memory. This is done automatically on power-up.

INITIATE POWER-UP DIAGNOSTIC TEST: Allow approximately 3 seconds or more to execute. This test will reset the system (same as power-up). If using the 4012P firmware mode (see **SET MODE REGISTER (12)**) this test will NOT exercise TRAQ memories which would write overwrite data.

SECTION 8

READING THE 4012/4032 CONTROL REGISTERS

F(0)*A(0)*R(R16..R1)

Control registers can be read at any time, either in remote or local control mode. The registers are read using a two step command process:

- 1) Address the register with **F(17)*A(0)*W(register address)** which causes the TRAQ processor to fetch the register data.
- 2) Read the register data with **F(0)*A(0)*R(register data)**.

If the TRAQ controller is available to accept the **F(17)*A(0)** command, a **Q=1** will be returned. The data to be read will be available within 500 μ sec and should be read by the **F(0)*A(0)** command within 1 sec after **F(17)*A(0)**. The controller will not respond for one second to any other CAMAC command while waiting for **F(0)*A(0)** to read the control register.

NOTE

In the table below:

W corresponds to the **W** data (decimal) in the **F17** command: **F(17)A(0)W(W16-W1)**

R corresponds to the **R** data (decimal) in the **F0** command: **F(0)A(0)R(R16-R1)**

CMD corresponds to the previous sections **COMMAND** value (hex).

Description	W	R	CMD
READ NUMBER OF ACTIVE SIGNAL CHANNELS	1	1,2..256	1
READ POST-TRIGGER SAMPLES	2	0,1,2..8	2
READ CLOCK 1 FREQUENCY	4	0,1,2,,17	4
READ CLOCK 2 FREQUENCY	5	0,1,2,,17	5
READ CLOCK CONTROL	6	0,1,2	6
READ CLOCK SWITCH. REG.	7	0,1,2	7
READ LOCAL/REMOTE STATUS	8	0,1	8
READ DISPLAY CHANNEL	9	1,2,,256	9
READ DATA CHANNEL TO BE READ	10	1,2..256	A
RESERVED	13		

READ STATUS	14							
	READ(R8-R1) (BINARY)							
Description	8	7	6	5	4	3	2	1
4012 NOT sampling	x	x	x	x	x	x	x	0
4012 sampling	x	x	x	x	x	x	x	1
Data acquisition mode	x	x	x	x	x	x	0	x
Calibration acquisition mode	x	x	x	x	x	x	1	x
4012P/4032P not master armed	x	x	x	x	x	0	x	x

4012P/4032P master armed	x	x	x	x	x	1	x	x
4012P/4032P not master enabled	x	x	x	x	0	x	x	x
4012P/4032P master armed enabled	x	x	x	x	1	x	x	x
Stop trigger received before EOC	x	x	x	0	x	x	x	x
Stop trigger not received before EOC	x	x	x	1	x	x	x	x
4012 (4032) not triggered	x	x	0	x	x	x	x	x
4012 (4032) triggered	x	x	1	x	x	x	x	x
4012P (or 4032P) code running	x	0	x	x	x	x	x	x
4012A (or 4032) code running	x	1	x	x	x	x	x	x
Calibration memory not enabled	0	x	x	x	x	x	x	x
Calibration memory enabled	1	x	x	x	x	x	x	x

NOTE

- 1) The 4012 will turn the LAM on when sampling is complete in the remote mode.

 - 2) In calibration mode the 4012 will store 2k/samples per channel in the reserved calibration section of memory after data acquisition.

 - 3) Stop trigger received before EOC: This status flag should be monitored when using the Stop Sampling Command. (See 12 under Writing the 4012 CONTROL REGISTERS.)
-

Reserved	15
Read Number of Samples Converted, Lower Word R16-R1	16
Read Number of Samples Converted, Upper Word R16-R1	17

Read the total number of samples converted. This command is used when sampling has been forced to stop (see **WRITING CONTROL REGISTERS**). Returns the **TOTAL** number of samples converted:

TOTAL samples converted = NOC * samples

therefore if 1000 samples have been taken and Number Of Channels = 6 then the total samples converted is 6000.

TOTAL samples converted = 65536 * (UPPER WORD) + LOWER WORD

O NOTE

TOTAL samples converted can be greater than (record length * NOC) if no stop - trigger was received and the samples converted are greater than the record length.

Reserved	15
Read Number of Samples Converted, Lower Word R16-R1	16
Read Number of Samples Converted, Upper Word R16-R1	17

Read the total number of samples converted. This command is used when sampling has been forced to stop (see **WRITING CONTROL REGISTERS**). Returns the **TOTAL** number of samples converted:

TOTAL samples converted = NOC * samples

therefore if 1000 samples have been taken and Number Of Channels = 6 then the total samples converted is 6000.

TOTAL samples converted = 65536 * (UPPER WORD) + LOWER WORD

 **NOTE**

TOTAL samples converted can be greater than (record length * NOC) if no stop - trigger was received and the samples converted are greater than the record length.

Model 4012 Only

Read Memory/Channel (1k Blocks)	3	1,2..	3
Read Start ADDR OF DATA (1k Blocks)	11	1..4095	B
Read TRAQ Total Memory Size	12	128=128K 256=256K, etc.	C

Model 4032 Only

(UPM) Upper Read Memory/Channel	18		D
(LPM) Lower Read Memory/Channel	19		

NOTE

Total Memory/Channel (1k blocks) = $65536 * UPM + LPM$

(TTMSU) : Read Total TRAQ Memory Size Upper	20		
(TTMSL) : Read Total TRAQ Memory Size Lower	21		

NOTE

Total TRAQ Memory Size (1k blocks) = $65536 * TTMSU + TTMSL$

(SADU): Read Start Addr of Data Upper	22		E
(SADL): Read Start Addr of Data Lower	23		B

 **NOTE**

Start Address for Data Readout (1k blocks) =

$$65536 * SADU + SADL$$

SECTION 9

DIAGNOSTICS

During the power-up sequence the TRAQ microprocessor runs a series of diagnostic tests. Failure to pass these tests implies the system is not functional. If a test does not pass a message will be displayed on the "value" LED display while the "function" LED displays the TEST being performed. For most of the test, the controller will continually loop through the failed test to facilitate oscilloscope probing of the failed circuitry. To restart the testing sequence hit the reset button or issue CAMAC Z (or C) commands. The tests are performed sequentially as listed below.

NOTE

In the following discussions the 4012-01 board is on the left side (as viewed from the front) and the 4012-02 (processor board) is the board on the right. The 4012-03 is the front panel board. Also, 4012P units do not use the MEM2 and MEM4 tests as stored data would be erased after power-up.

Value LED:	Function LED:
No Display	
Test Description:	
Either the 4012-02 board has no +6V power, the 4012-03 is not connected to the 4012-02, or there is some failure on the 4012-02 (such as a bad PROM, RAM, etc.) that is inhibiting the processor from initializing.	
Check:	
Check 4012-02 and 4012-03 connections, 4012-02 fuses. Or generate repetitive CAMAC Z(or C) cycles and probe the T.I. 9995 address/data lines for correct logic states. Immediately after reset, the processor will access the RAM memory (starting at location A000, hex) - check for memory access signals.	

Value LED:	Function LED:
RAM	Fail
Test Description:	
The processor writes an alternating 1010... and 0101... pattern into the onboard static RAM and attempts to read it back.	
Check:	
The processor writes an alternating 1010... and 0101... pattern into the onboard static RAM and attempts to read it back.	

Value LED:	Function LED:
INTP	Fail
Test Description:	
The processor sets-up the 9519 interrupt control chip, fires interrupt #7 (internally) and checks the 9519's interrupt status register for interrupt #7.	
Check:	
Failure implies either a bad 9519 IC or bad connections to the chip. Since a message is being displayed, the processor and associated bus circuitry are probably O.K. Probe pin 1 of 1L (9519) for chip select. Also, check for wr(write) and rd(read).	

Value LED:	Function LED:
L646	Fail
Test Description:	
<p>This is the first test that checks board interconnections, the state of the 4012-01 board and the TRAQBUS. The processor loads a pattern (AAAA 5555, hex) into the LS646s (6H-9H) on the 4012-01 board and then reads the pattern back.</p>	
Check:	
<ol style="list-style-type: none"> 1) Remove the cable from the 50 pin TRAQBUS connector and restart the test. If the test passes, the problem is either a bad TRAQBUS cable or a bad memory module which is generating data on the bus when not addressed. 2) Check all fuses on the 4012-01 board and the interconnection cable between the 4012-01 and 4012-02 3) If the test still fails, this indicates a component failure on the 4012-01 or 4012-02 board. The 4012-01 has three data busses: <ol style="list-style-type: none"> 4) A 32-bit data bus (IB31-IB0); main data bus 5) A 16-bit data bus (MD15-MD0); CAMAC data bus 6) A 8-bit data bus (PD7-PD0); μ-processor data bus 	
<p>Communication between the microprocessor the IB bus is through the CAMAC MD bus; i.e., μ-processor - CAMAC - data bus</p>	
<p>After data bytes are latched into the LS646 B latches they are transferred to the A latches and then read back through the same data paths. Any problems on the TRAQBUS will show up during the LS646 B to A transfer. To check the data in the LS646 latches, trigger a scope on pin 9H(1), the signal which transfers the data in the latches. Check 6H(4 to 11), 7H(4-11), etc. for the AAAA 5555 pattern. Failure of the pattern at this point implies either bad signal levels on the PD, MD, or IB bus, defective ICs or bad enable, latch signals to the data path chips.</p>	

Value LED:	Function LED:
LPTS	Fail
Test Description:	
Loads a 32-bit pattern (AAAA 5555, hex) into the 32-bit PTS counter and reads the pattern back.	
Check:	
Since the "L646" test passed the data bus, connections between the 4012-01 and 4012-02 board are OK. Also, the IB, MD, and PD bus are OK. The transfer of data bytes to/from the microprocessor is the same as the "L646" test except data is latched into the PTS counters, not the LS646s. Data is transferred to internal 8-bit latches by strobing the LO-DMA-CNT line. Data is then read when RD-PTS-CNT line goes low (4 times to read 4 bytes).	

Value LED:	Function LED:
ADDR	Fail
Test Description:	
Loads a 32-bit test pattern (AAAA 5555) into the 32-bit address counter. This counter can auto-skip address in increments of 1 to 255 under hardware control only. It is used to readout the data for display or CAMAC.	
Check:	
The previous tests have checked the IB and other data busses. Therefore, any problems are probably associated with internal chip problems.	

Value LED:	Function LED:
ADIN	Fail
Test Description:	
Loads a 1 into the address counters, increments the address counters 8 times and reads the resulting address back. Then repeats the test starting at address FF (hex), FFFF (hex) and FF FFFF (hex)..	
Check:	
Failure of this test usually implies a problem with the address auto-incrementer.	

Value LED:	Function LED:
ADAU	Fail
Test Description:	
<p>Loads zero into the address counters, 128 into the auto-skip register and checks for correct auto-incrementing of the address counters after generating address strobes. The test is performed 32 times (addresses 0 to 4096, in increments of 128). The addresses are read and checked after each of the 32 address strobes.</p>	
Check:	
<p>Since test "ADDR" has passed, this test should only fail due to a faulty auto-increment register or faulty overflow logic from counters.</p>	

Value LED:	Function LED:
ADOV	Fail
Test Description:	
<p>Loads FFFF FFFE (hex) into the address counters, increments two times and checks for overflow reset (address =0). The address overflow counter is used to reset the memory modules' internal address counters to zero after the end of memory has been reached during writing or reading. This counter is incremented each time counter (counts in 64K increments) and reaches its terminal count when the memory space is exhausted. The overflow triggers a 50 nsec. reset pulse, which resets the controller and memory module internal address counters. On the first address cycle the addresses increment to FF FFFF, hex, and the next address cycle causes the overflow to reset the address counters and reload.</p>	
Check:	
<p>Since the address counters have passed the three previous tests, any problems should be associated failed ICs.</p>	

Value LED:	Function LED:
PTIN	Fail
Test Description:	
Loads a 1 into the PTS counters, increments the counters 8 times and reads back the data. Repeats the same test starting with an initial count of FF, FFFF, and FF FFFF (hex).	
Check:	
Since the "LPTS" test passed this test should only fail due failed ICs.	

Value LED:	Function LED:
PTOV	Fail
Test Description:	
Loads FFFF FFFE (hex) into the PTS counters, increments one time and checks for interrupt #3 on. When the PTS counters reach the terminal count of FFFF FFFF(hex), the DMARCO goes low which in turn generates interrupt #3 to the 4012-02 board.	
Check:	
Since the PTS counters have passed the "LPTS" and "PTIN" tests the only problems should be due to faulty overflow circuitry.	

Value LED:	Function LED:
MEM1	Fail
Test Description:	

This is the first test for the memory modules. At this point all of the 4012-01 diagnostics have passed. This test performs the following functions:

- 1) Determines how much memory is on the TRAQ bus.

Checks that interrupt #6 is generated when the memory module returns the DARDY signal.

The 4012 assumes that there is at least 128K words of memory on the bus and will fail the test if no memory module responds with a DARDY, when address FFFF (hex) is addressed. The modules are organized as 32-bit words and each module's internal address counters range from FFFF-0000, hex. This is equivalent to 64 K, 32-bit words or 128K of 16-bit words. The test proceeds as:

- 1) Address 0000 FFFF is loaded into the memory modules.
- 2) A data cycle (DACYC) is generated.
- 3) The processor looks for interrupt #6 on.

If interrupt #6 is not on after the first DACYC, the test fails as either no memory is present or there are logic problems.

If interrupt #6 is on, the address is incremented by 64K (i.e. to 1 FFFF, hex) and loaded into the memory module, which generates a DACYC. This continues unless a DARDY is not returned signifying no more memory is present.

Check:

Check the I.D. switches on the memory modules. One of the units must have I.D. = 0. Also check the TRAQ bus cable. If the test still fails, set another module on the bus to I.D. = 0 (set the original modules' I.D. = 7) and rerun the test. If the test now passes, the original module was faulty. If the test still fails, probe the DARDY signal on the 4012, sheet 2. DARDY is an open collector signal so if any module is faulty, the line could be held down.

Value LED:	Function LED:
MEM2	Fail
Test Description:	
<p>This test writes the address of the first word in each 32 bit, 64k memory block on the TRAQ bus, i.e. the word at location 0000 is loaded with 0000 and then checked. The word at address 1 0000 (hex) is loaded with 1 0000 and then checked, etc. This is a very rough memory test to quickly see if there are any gross memory failures. This test will usually pickup any bad memory chips that are totally failing.</p>	
Check:	
<p>Check which memory module has it SEL LED on. This is where the failure is occurring. Probe the data lines (synchronizing with DARDY to locate the bad memory chip).</p>	

Value LED:	Function LED:
MEM4	0,1,2,....
Test Description:	
<p>This is the final diagnostic test and tests all the memory on the TRAQ bus in 1k block increments. Data is written into memory using the address counters in the 4012-01. A 1 MHz clock is used to write the data. After the memory block is written, the processor reads and checks every 64th memory location. If the test fails, the processor will remain in a loop writing/reading at the block that failed. The value displayed on the LEDs is the block being tested.</p>	
Check:	
<p>Check that the 1 MHz clock is working. If no clock is present, check the clock circuitry on the 4012-02 board. Otherwise, check the module for faulty logic or a bad memory locations.</p>	

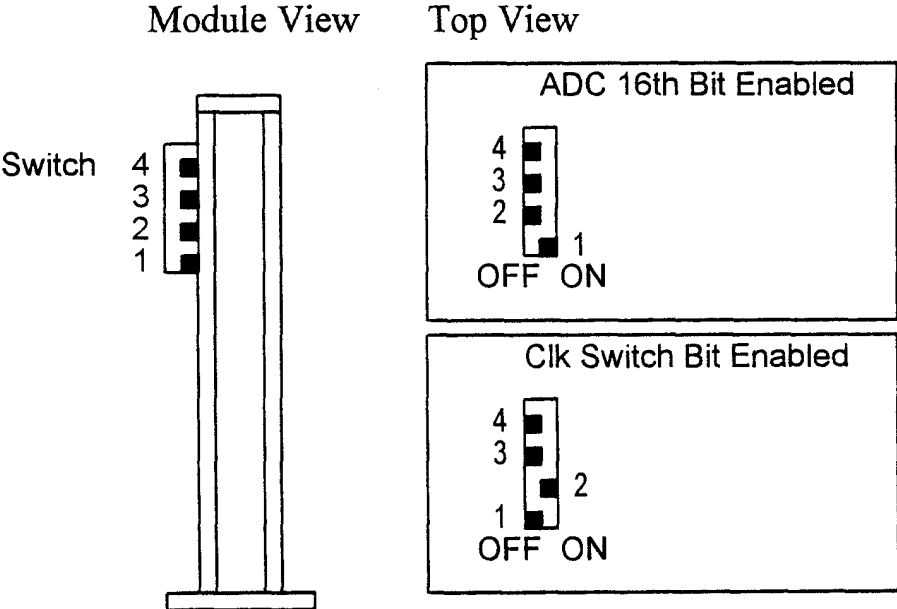
SECTION 10

SWITCH OPTIONS

CLK2 16th Bit Set

The 4012/4032 is normally delivered with the 16th data bit set to the CLK2 status detect line. Whenever CLK2 is active the 16th bit of the data will be set to one (1). This option can be defeated by changing the switch settings on the 4012-01 board. This switch is accessible at the top of the module, left side.

This allows the 16th data bit from the signal channels to be stored in memory.



Installation of TRAQ Firmware

Firmware for the 4012/4032 is programmed into two 64k EPROMs which can be field upgraded by installing new EPROM chips into the control board. Occasionally DSP may send out new revisions of this software. To install the new EPROMs place the unit on a table with the front panel facing you and:

- 1) Remove the back panel and open the unit (it may be necessary to remove the right side panel).
- 2) Remove the 28-pin integrated circuits in sockets E1 and E2 which are located at the top of the right side printed circuit board. The I.C. will have a revision number on it such as REV 1.10. Be sure to note the orientation which has pin 1 facing the rear of the module.
- 3) Install the new EPROMs in the same sockets with the same orientation.
- 4) Close the unit and remount the rear panel.
- 5) Install the unit in the crate and turn the power on. After diagnostics are complete the new revision number should be displayed.
- 6) If the unit does not power-up properly check for bent pins or incorrect installation of the EPROMs.

SECTION 11

SERIES 5000

MEMORY MODULES


General Description

Models 5004,...5432 and up are high density memory modules which store data from the TRAQ 4012/4032 controllers.

Memory in the units is organized as 32-bit words. The units can write/read data at a maximum rate of 8.0 Megasamples/second (a sample is a 16 bit data word). The maximum number of modules on the bus is limited to 8 or the maximum allowed memory size (16 Megasamples for 4012 controllers; or 256 Megasamples for 4032 controllers). All communication with the memory module is through the front panel TRAQBUS connector; the CAMAC connector supplies power only. The TRAQBUS is a multiplexed address/data bus with the ability to write/read data up to 8.0 Megasamples/second. The memory consists of dynamic RAMS with on board refresh control or static rams (Model 5200 only).

Front Panel Indicators and Controls

LED Indicators

ADCY	Momentary LED. Indicates that an address cycle has been generated.
DACY	Momentary LED. Indicates that a data cycle has been generated.
RFCY	Momentary LED. Indicates that memory refresh cycles are being generated.
RFEN	Indicates that refresh cycles are enabled
	 NOTE RFCY & RFEN should be on when the module is not connected to the TRAQBUS

WRITE	Indicates that the module is enabled for writing data to memory (when the LED is on) or reading to the Controller (when the LED is off).
SEL	Indicates that the module is selected for reading/writing. Only one memory module is selected at a time
ID3-ID0	Indicates the position of the module ID switches.
WRITE LOCK	Indicates that the memory cannot be over-written. (5200 series only)

Module ID Switches


ID3, ID2, ID1, ID0:

NOTES

- 1) Some 500x module have only 2 or 3 ID switches
 - 2) The following discussion assumes:
 - a) Only one type of memory module used (for example - multiple 5004 modules); consult the factory for ID switch settings if you need to mix different types of modules (example - 5005 and 5004).
 - b) Memory modules are installed immediately to the left of the controller.
-

Four switches which set the module identification number. The ID LEDs are on when the switch is in the "on" position. Up to 8 memory modules can be installed on the TRAQBUS and these switches determine which module will be "module 0," "module 1," etc. The ID switches must be set so that one module has ID zero, one module ID one, (up to the number of installed modules -1).

Module Switch Settings

ID	ID3	ID2	ID1	ID0	Use this setting for module:
0	off	off	off	off	Module directly to left of controller
1	off	off	off	on	2nd memory module to left of controller
2	off	off	on	off	3rd memory module to left of controller
3	off	off	on	on	4th memory module to left of controller
4	off	on	off	off	5th memory module to left of controller
5	off	on	off	on	6th memory module to left of controller
6	off	on	on	off	7th memory module to left of controller
7	off	on	on	on	8th memory module to left of controller
8	on	off	off	off	 NOTE Following ID's are used when mixing different memory model types (consult factory)
9	on	off	off	on	
10	on	off	on	off	
11	on	off	on	on	
12	on	on	off	off	
13	on	on	off	on	
14	on	on	on	off	
15	on	on	on	on	

Anytime modules are added to the TRAQ system or ID numbers changed, the controller should be reset or re-powered to initiate diagnostics.

Input Signal (5200 Series Only)

Write Lock

TTL signal, LEMO type input connector, internally pulled-up to 5 Volts by a 10 Kohm resistor. Whenever the Write Lock input signal (WLIS) is driven to a TTL low, the memory cannot be overwritten with new data. When power is applied to the module an internal signal generates a write lock. As the controller starts its power-up diagnostics it will reset the internal write lock unless the WLIS signal is present. The presence of the WLIS will always prohibit overwriting the memory.

SECTION 12

TRAQ DIGITIZER MODULES

TRAQ data acquisition is performed by modular Analog-to-Digital Converters (ADCs). These modules include the 8 channel, (100 KHz DSP 2812), 4 channel (1 MHz DSP2860) and others. Multiple modules may be connected to form a multichannel (256 maximum) system. Features common to all DSP data acquisition modules are:

- 1) High Resolution
- 2) Simultaneous Sampling
- 3) Fully Independent Channels
- 4) Modularity

Each channel is fully independent, incorporating an individual fully differential amplifier, track and hold, and ADC. This allows any or all channels to be used simultaneously at a constant data acquisition rate.

TRAQ Digitizer Module Specifications

Model	2812	2814	2840	2860	2824
Sampling Rate (KiloSamples/Sec)	100	100	1000	1000	2000
Number of Channels	8	4	4	4	1
Maximum Channels/Controller at maximum Sampling Rate	80	80	8	8	4
Resolution (bits)	12	14	14	12	12
Input Voltage Range (Volts)	± 5	± 10	± 10	± 5	± 5
Input Impedance (ohm)	100K	100K	100K	100K	100K
Bandwidth (0.5dB)(Hz)	50K	50K	500K	500K	500K
Bandwidth (3dB)(Hz)	100K	100K	1M	1M	1M
CMRR (dc-100 Hz)dB	80	80	94	72	80
CMVR (Volts)	± 12	± 12	± 20	± 12	± 12
Input Protection (dc) (Volts)	± 50	± 50	± 100	± 50	± 50
DC Gain Error (%)	± 0.1	± 0.1	± 0.1	± 0.1	± 0.1
DC Offset Error (% of FS)	± 0.1	± 0.1	± 0.1	± 0.1	± 0.1
Integral Non-Linearity (LSB)	± 0.5	± 0.5	± 0.5	± 0.5	± 0.5
Differential Non-Linearity (LSB)	1	1	1.5	1	1
Aperture Delay (Nsec)	<15	<15	<15	<15	<15
Channel-Channel Time Skew	<100	<100	<100	<100	<100

Temperature Range

Operational: 10 - 55°

Storage: -5 - 85°

Front Panel Description

LED Indicators

ADCY	Momentary LED. Indicates that an address cycle has been generated.
CVT	Indicates module is performing analog to digital conversions. The indicator will appear to be continuously on for sampling rates greater than 10 samples per second.
SEL	Indicates module is currently selected for data transfer from the internal data buffer. The indicator will appear to be continuously on for rates greater than 10 samples per second.
ID3-ID0	Indicates module identification number (module address) as determined by MODULE ID switches.

Module ID Switches

Four switches which set the module identification number. The ID LEDs are on when the switch is in the "on" position. Up to 16 ADC modules can be installed on the ADCBUS and these switches determine which module will be "module 0," "module 1," etc. The ID switches must be set so that one module has ID zero, one module ID one, (up to the number of installed modules -1).

Data Acquisition module IDs must be set according to the following rules:

1)

Module ID Switch Settings:					Channel Numbers:				
ID	ID3	ID2	ID1	ID0	2812	2814	2840	2860	2824
0	0	0	0	0	1-8	1-4	1-4	1-4	1
1	0	0	0	1	8-16	5-8	5-8	5-8	2
2	0	0	1	0	17-24	9-12	9-12	9-12	3
15	1	1	1	1	120-128	60-64	60-64	60-64	16

- 2) A module with an ID = 0 must be present in the system.
- 3) Module IDs must be contiguous (i.e., no gaps in channel numbers are allowed).
- 4) Module IDs must be unique (i.e., no modules with identical channel numbers are allowed).

 **NOTE**

The physical placement of modules on the TRAQ bus is not restricted.

Input Signal Connectors

Differential input signal connectors mate with:

LEMO - F0.302 NYL U/3.7 or equivalent.

Bipolar/Unipolar Input Option

All digitizer modules are delivered and calibrated in the bipolar input mode. Some modules have internal jumpers for unipolar mode.

 **NOTE**

Internal jumpers are not computer readable.

Model	2812	2814	2840	2860	2824
BIPOLAR MAX VOLTAGE	+4.998	9.9988	9.9988	+4.998	+4.998
BIPOLAR MIN VOLTAGE	-5.000	-10.000	-10.000	-5.000	-5.000
BIPOLAR ADC ZERO CODE	2048	8192	8192	2048	2048
UNIPOLAR MAX VOLTAGE	+9.998			+9.998	+9.998
UNIPOLAR MIN VOLTAGE	0.0			0.0	0.0
UNIPOLAR ADC ZERO CODE	0			0	0

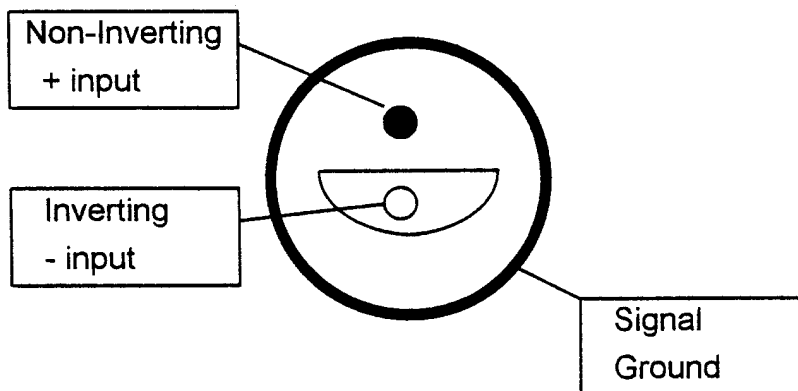
Independent mode selection is available for each channel. Selection is made via jumpers within the module. Refer to the MODULE INFORMATION section of the manual for their locations.

Input Signal Connection

Each ADC channel has a high impedance, wide bandwidth differential amplifier input.

Connector compatibility:

LEMO RA0.302NYL dual pin connector mates with LEMO F0.302NYLU/3.7



2812M

The 2812M is a special version of the 2812 with a multipin cable input which is compatible with the 1008 amplifiers; this module uses an AMP 204731-1 w/ 205172-8 Female Pins which mates with AMP 204744-1 w/ 203816-3. The pin-out for this connector is:

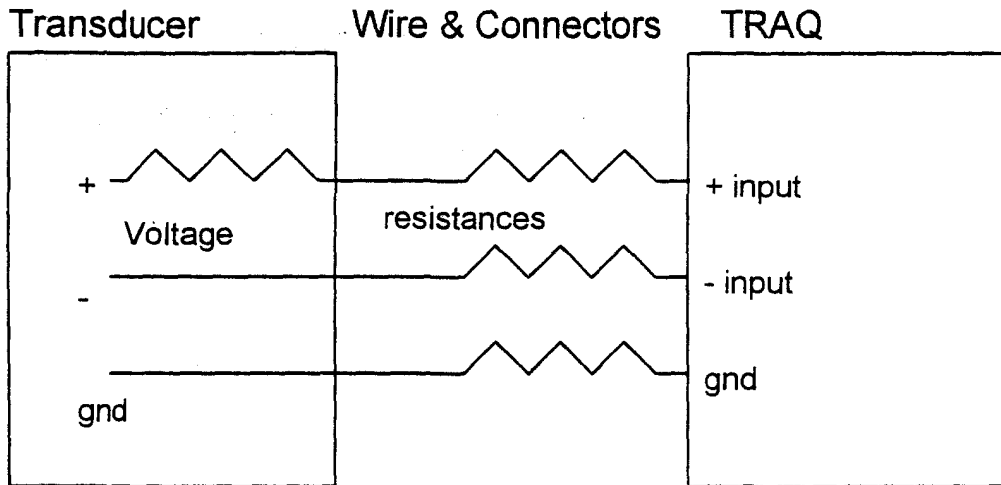
CHANNEL	+IN	-IN	SIG GND
1	1A	2A	1B
2	1C	2C	2B
3	4A	5A	4B
4	4C	5C	5B
5	8A	9A	8B
6	8C	9C	9B
7	11A	12A	11B
8	11C	12C	12B

Signal Conditioning

In order to maintain signal quality and, therefore, digitizer accuracy, certain signal conditioning procedures must be observed when connecting the TRAQ system to a signal source.

- 1) Use differential connections for analog signals. If the source is single ended, connect one side of the differential pair to the source ground.
- 2) Use twisted pair shielded cables.
- 3) Shield all analog signals to minimize inter-channel coupling and noise pickup. Ground all shields at a single, common ground to avoid ground loops.

- 4) Use low impedance sources, cabling, and connections. The DSP ADCs can resolve a milliVolt Voltage changes. The signal source impedance, as measured at the TRAQ channel input, must be less than 200 Ohms in order to maintain system accuracy.



SECTION 13

DATA ACQUISITION MODULE

SPECIFIC INFORMATION

The following sections describe in detail each of the TRAQ Data Acquisition modules. This includes information on selecting available options and calibration procedures.

Model 2812 12 bit / 100 kHz / 8 Channel ADC

Bipolar/Unipolar Signal Input Options

- 1) To select BIPOLAR input option remove jumper labeled "UNI" next to R21 component at desired channel.

- 2) To select UNIPOLAR option, install jumper at position labeled "UNI" next to R21 component at desired channel.

NOTES

- 1) Make sure R19 is 10 Kohms at the desired channel. On some early units R19 was 51.1 Kohms.

 - 2) Signal input is connected to inverting channel input.
Ground is connected to non-inverting channel input .
-

Bipolar Calibration and Alignment

Each channel of the DSP 2812 has an individual set of calibration adjustments. Access to the offset, gain, and common mode rejection trims is achieved by removing the left-hand side cover. Drawing 2812A-01-AD indicates the location of each channel and the adjustments for each.

- 1) Set channel to bipolar mode.

- 2) Set digitizer sampling clock to 100 KHz.
- 3) Connect +ve channel input to gnd.
Connect -ve channel input to gnd
- 4) Digitize and average over 10 data samples.
Adjust R21 for averaged reading of 2048.
- 5) Connect +ve channel input to gnd.
Connect -ve channel input to +4.900 Volt reference.
- 6) Digitize and average over 10 data samples.
Adjust R22 for averaged reading of 41.
- 7) Connect +ve channel input to +4.900 Volt reference.
Connect -ve channel input to +4.900 Volt reference.
- 8) Digitize and average over 10 data samples.
Adjust R25 for averaged reading of 2048.

Unipolar Calibration and Alignment

- 1) Perform BIPOLAR MODE calibration first.
- 2) Set channel to unipolar mode.
- 3) Set digitizer sampling clock to 100 KHz.
- 4) Connect -ve channel input to +5.000 Volt reference.
Connect +ve channel input to gnd.

- 5) Digitize and average over 10 data samples.
Adjust R21 for averaged reading of 2048.

Common Mode Rejection

- 1) Set channel to bipolar mode.
- 2) Connect +ve channel input to 10 v pk-pk 25 KHz sinewave.
- 3) Digitize and display reconstructed data.
Adjust R25 for minimum amplitude display.

Model 2814 14 bit / 100 kHz / 4 Channel ADC

Bipolar Calibration and Alignment

- 1) Set digitizer sampling clock to 100 kHz.
- 2) Connect both inputs of the unit under test to system ground. Adjust R19 until the digital data from the unit under test reads 8188 (decimal).
- 3) Connect the non-inverting input of the unit under test to the precision DC source. Set the source output Voltage to 9.990 Volts. Adjust R18 until the digital data from the unit under test reads 16302.

Model 2840 14 bit / 1 mHz / 4 Channel ADC

Bipolar Calibration and Alignment

- 1) Set digitizer sampling clock to 100 kHz.
- 2) Connect both inputs of the unit under test to system ground. Adjust
Channel 1 R51

Channel 2 R69

Channel 3 R14

Channel 4 R32

until the digital data from the unit under test reads 8188 (decimal).

- 3) Connect the non inverting input of the unit under test to the precision DC source. Set the source output Voltage to 9.990 Volts. Adjust

Channel 1 R53

Channel 2 R21

Channel 3 R16

Channel 4 R34

until the digital data from the unit under test reads 16302.

Model 2824 12 bit / 2 mHz / 1 Channel ADC

Access to the DSP 2824 gain, offset, and common-mode rejection adjustments is achieved by removing the left hand side cover. Drawing 2824-01-AD indicates the locations of these adjustments.

Bipolar Calibration and Alignment

- 1) Connect both inputs of the unit under test to system ground. Adjust R30 until the digital data from the unit under test reads 2048 (decimal).
- 2) Connect the non-inverting input of the unit under test to the precision DC source. Set the source output voltage to 4.974 Volts. Adjust R9 until the digital data from the unit under test reads 4085.
- 3) Repeat step 1. If no adjustment is necessary, continue to step 4; otherwise repeat steps 1 and 2 until there is no change when step 1 is repeated.
- 4) Connect both inputs of the unit under test to the precision voltage source. Adjust R10 until the digital data from the unit under test reads 2048.

Unipolar Calibration and Alignment

- 1) Select BIPOLAR MODE* and perform BIPOLAR MODE calibration.
- 2) Select UNIPOLAR MODE*.
- 3) Connect both non-inverting and inverting inputs to ground. Adjust R30 until a digital reading of between 0 and 1 is recorded.

NOTE

See sheet 1 of 2824 schematic for selecting UNIPOLAR or BIPOLAR MODES.

Model 2860 12 Bit / 1MHz / 4 Channel ADC

Bipolar/Unipolar Signal Input Options

Bipolar

Install jumper at position labeled "BI" for the desired channel(s). (factory setting)

Unipolar

Install jumper at position labeled "UNI" for the desired channel(s).

Calibration and Alignment

Each channel of the DSP 2860 has an individual set of calibration adjustments. Access to the offset, gain, and common mode rejection trims is achieved by removing the left hand side cover. Drawing 2860-01-AD indicates the location of each channel and the adjustments for each.

Bipolar Mode Calibration

- 1) Set channel to bipolar mode according to the previous section
- 2) Set digitizer sampling clock to 1MHz.

- 3) Connect 0.000 Volt reference to + input of channel.
Connect 0.000 Volt reference to - input of channel.
- 4) Adjust R12 (Offset) so that the digitized readout from the Controller (averaged over 10 samples) reads 2047.5 (± 0.5).
- 5) Connect +4.900 Volts reference to + input of channel.
Connect 0.000 Volts reference to - input of channel.
- 6) Digitize and average over 10 data samples.
Adjust R27 (+Gain) for averaged reading of 4054 (± 0.5).
- 7) Connect +4.900 Volt reference to + input of channel.
Connect +4.900 Volt reference to - input of channel.
- 8) Digitize and average over 10 data samples.
Adjust R34 (-Gain) for averaged reading of 2047.5 (± 0.5).

APPENDICES

ORDERING INFORMATION AND WARRANTY

Ordering

When ordering, please specify the complete Model Number along with any options, product description, and quantity. Orders may be placed by written order, telephone, TWX/Telex or FAX. Telephone orders must be confirmed in writing. All orders are subject to the approval of DSP Technology's Credit Department which is indicated by confirming sales order issued by the Company. The minimum order is one hundred (\$100) dollars, excluding transportation charges.

Customers should send their orders to:

DSP Technology Inc.
Order Processing Department
48500 Kato Road
Fremont, CA 94538
Telephone: (415) 657-7555
Telex: 283608
FAX: 415-657-7576

Pricing

Published prices cover standard packing only and do not include shipping, insurance, taxes, or any customs charges. All prices are subject to change without notice. All prices are F.O.B. Fremont, California. Please contact factory for volume discounts.

Payment Terms

Unless otherwise indicated, terms of payment for domestic orders, except for turn-key module/system, are net thirty (30) days from date of shipment. Terms of payment for turn-key systems are 40% of the written contracted price

submitted with the purchase order, 40% due net 30 days after shipment, 20% due net 30 days after acceptance of the system at the customer's facility (which must be completed within 30 days after shipment). A turn-key system is defined as customized hardware and software combination for which performance specifications are written that communicate how the system will perform for a specific application. Terms for orders outside the U.S. are cash in advance or irrevocable letter of credit, unless other terms have been previously arranged.

All orders placed with DSP Technology are binding and are subject to a cancellation charge of twenty five (25) percent of the selling price if cancelled.

Shipping

Domestic shipments are made by UPS, air freight, or truck. Shipping charges for UPS services are prepaid and charges added to the invoice, while other shipping methods are on a freight-collect basis. Overseas shipments are made by air freight.

Claims for shipping damages must be reported and confirmed in writing to the delivering carrier no later than fifteen (15) days after date of receipt. Claims for shortages of material must be made to DSP Technology within thirty (30) days after receipt of shipment.

Returns

DSP Technology must be notified before any product is returned for any reason. The Customer Service Department must

issue a Returned Material Authorization (RMA) number before any product can be accepted for credit, exchange or repair.

All returns for credit or exchange are subject to DSP Technology's approval and will incur a restocking charge of twenty five (25) percent, as well as any incoming transportation charges or other fees incurred by DSP Technology Inc.

Other Services

Contact DSP Technology for details regarding the following services: On-site consultation, Service contracts, System integration, and Installation.

PRODUCT WARRANTY¹

DSP TECHNOLOGY ("DSPT") warrants its products to be free from defects in material and workmanship and to meet DSPT's performance specifications. The warranty period which begins from the date of shipment to the buyer, is 90 days for ODAS products and one year for all other products. The warranty is limited by the paragraphs below.

Return to Factory

If a buyer discovers a defect in a DSPT product covered by this agreement, buyer's exclusive remedy is to ship the product back to DSPT's Fremont factory, where DSPT will, at its option, either repair or replace the product. This remedy applies if DSPT receives the returned product on or before the tenth day after the expiration of the warranty period and the buyer notifies DSPT of the defect before returning the product.

Cost of Repairs or Replacement

Buyer must prepay freight charges to DSPT. DSPT will pay standard return freight to buyer. Buyer will be charged for premium freight if that method of transport is requested by buyer. There is no other charge for repair or replacement of during warranty period.

Transferable Warranties

In addition to the foregoing warranty, DSPT also provides the buyer the transferable warranty, if any, provided to DSPT by the manufacturers of other products such as terminals and disk systems supplied by DSPT as part of a total system.

Limitation

The foregoing constitutes DSPT's entire warranty, expressed, implied, and/or statutory (except as to title), ad to any other party for any breach of such warranty and for damages, whether direct, special, incidental, or consequential.

¹Excludes Software and ODAS Products

Other than as expressly provided in this document, no warranties expressed or implied, including any warranty of merchantability or fitness for a particular purpose are made. No employee, representative, or agent or seller has any authority expressed or implied to alter or supplement the terms of this warranty.

SCHEMATICS

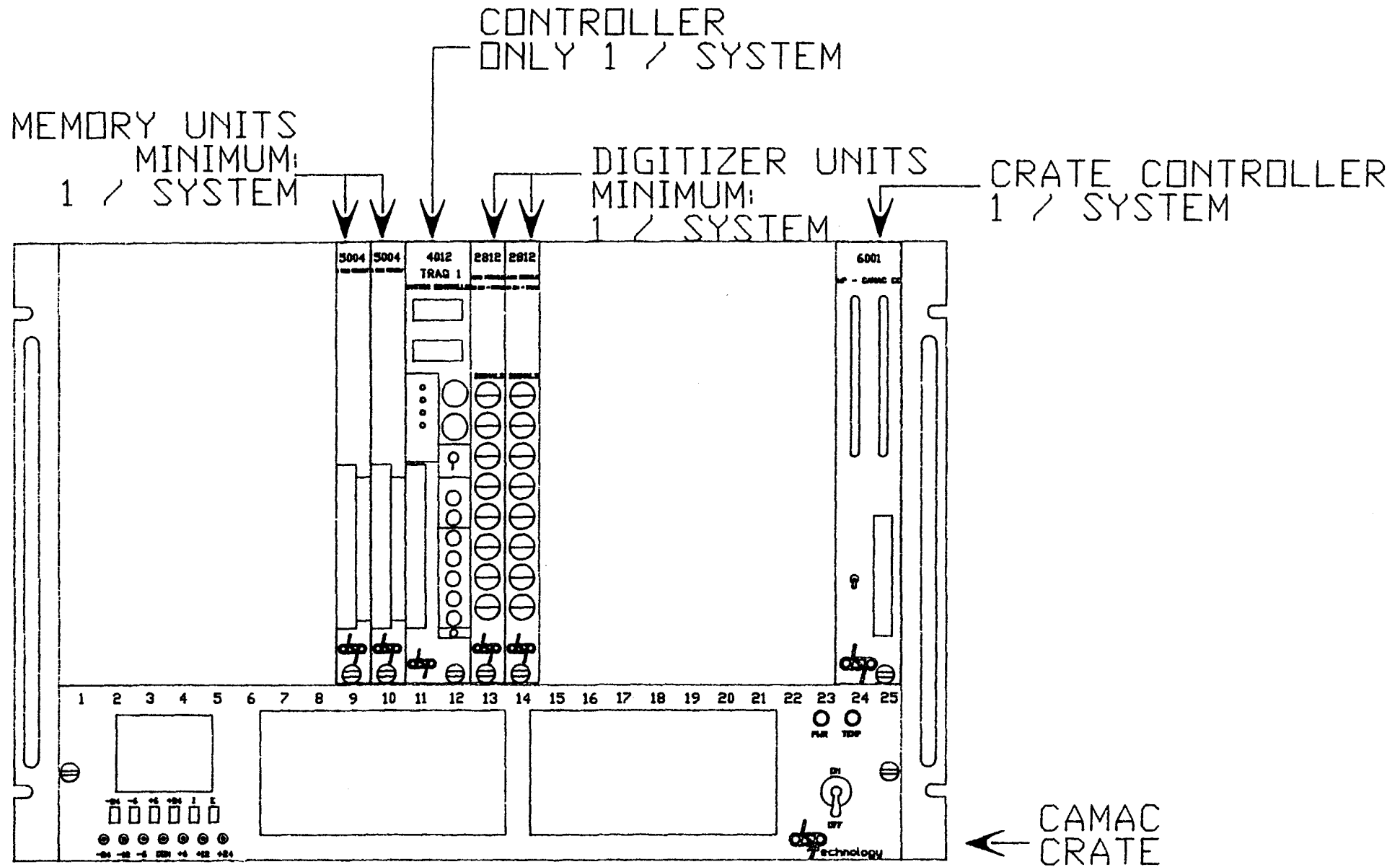


DIAGRAM 1
TRAQ CONFIGURATION DRAWING

40 PIN DAISY CHAINED CONNECTOR
CONNECTS TO:
REAR OF 4012 CONTROLLER
& REAR OF EACH DIGITIZER MODULE

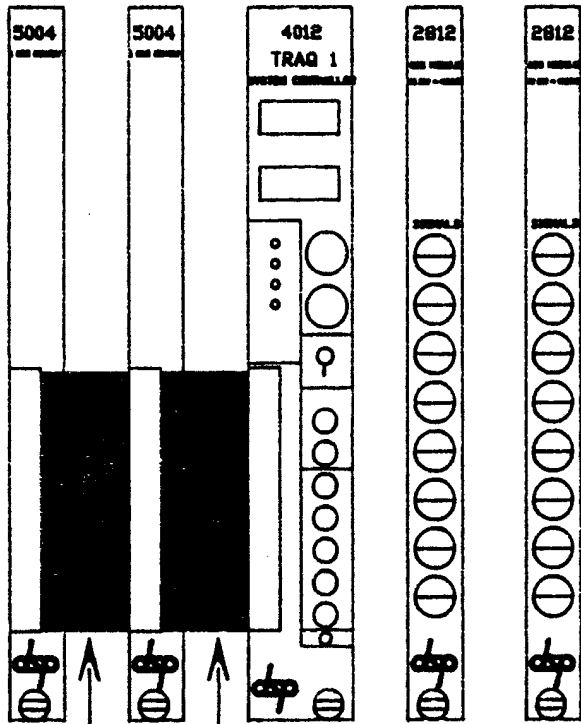










DIAGRAM 2
TRAQ
SYSTEM
INTERCONNECT

50 PIN DAISY CHAINED CONNECTOR
CONNECTS FROM 4012 CONTROLLER
TO EACH MEMORY MODULE

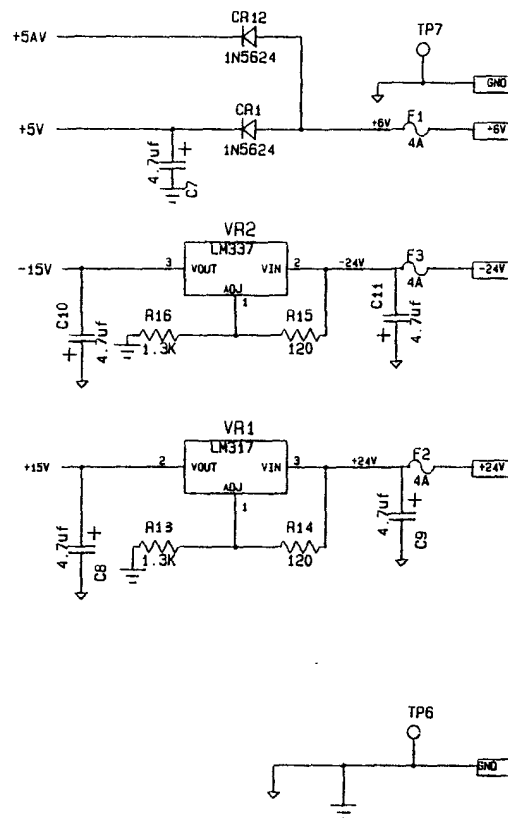
SYMBOLS:

-  CAMAC EDGE CONNECTOR
-  CONNECTOR (TO OUTSIDE WORLD)
-  CONTINUE ON SAME SHEET
-  CONTINUE ON DIFFERENT SHEET
-  UNUSED PIN
-  JUMPERS

NOTES: (UNLESS OTHERWISE SPECIFIED)

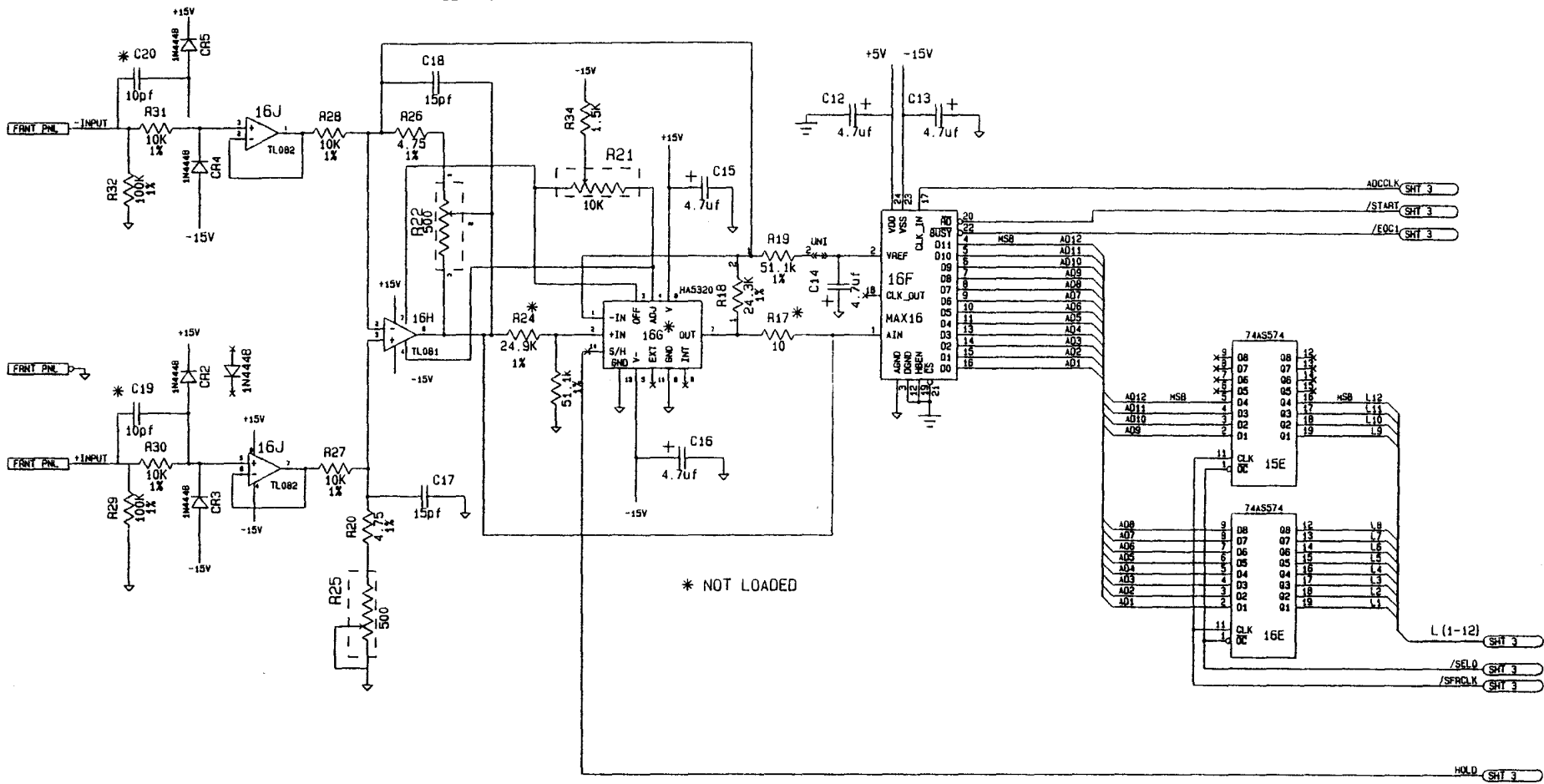
1.  DENOTES DIGITAL GROUND.
2.  DENOTES ANALOG GROUND.
3. ALL CAPACITORS ARE IN uF.
4. ALL RESISTORS ARE 5% 1/4WATT AND OHMS.
5. "*" DENOTES FACTORY OPTIONAL LOAD.

STANDARD JUMPERS	OPTIONAL JUMPERS LOADED AT TEST
"TRAQ II" "B1" (8 PLCS)	"TRAQ I" E1-E2 } ON LAST E3-E4 } UNIT IN E5-E6 } SYSTEM



SIGNATURES		DATE	D S P TECHNOLOGY INC	
DESIGNED			4800 RAY RD., FREDRICK, CA 94302-7200 (415) 857-7200	
DRAWN	PERALTA	12/85	SCHEMATIC, 2812A	
CHECKED			SIZE	PTRCH NO.
APPROVED			ISSUED	DRAWING NO.
B ECO1004-1009	JR	6/90	REVISED	REVISION
A PROD. RELEASE		12/86		
REV	DESCRIPTION	BY	DATE	
REVISIONS				
SCALE	NONE	SHEET	1	OF 3

CHANNEL ONE OF EIGHT

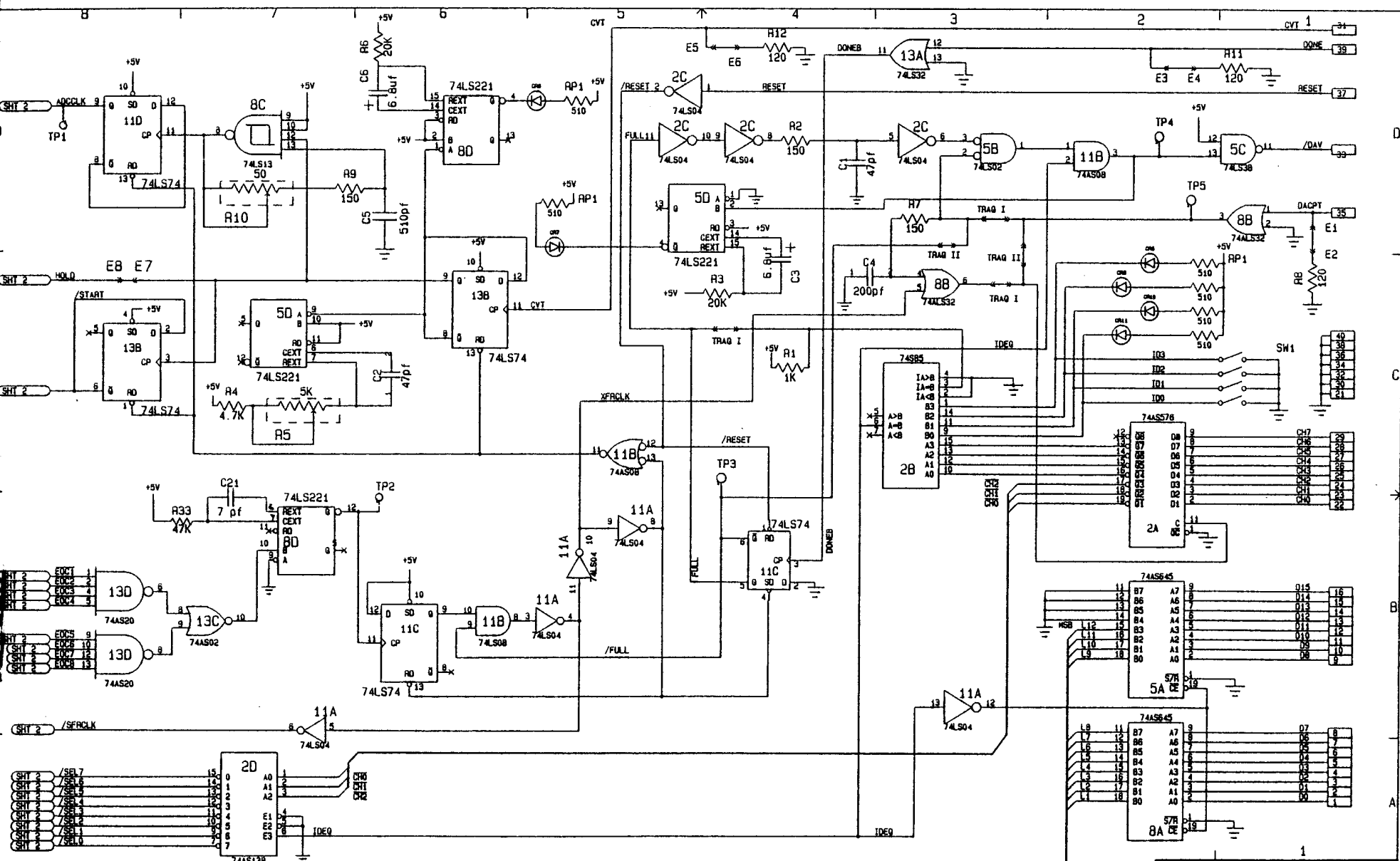


1

D S P TECHNOLOGY INC
4820 BAYVIEW RD., FORTWORTH, TX 76103-7206 (817) 627-7206

SCHEMATIC, 2812A

DATE	REVISED	DRAWING NO.	REVISION
		2812A-01-SD	C
SCALE	NONE	SHEET	2 OF 3

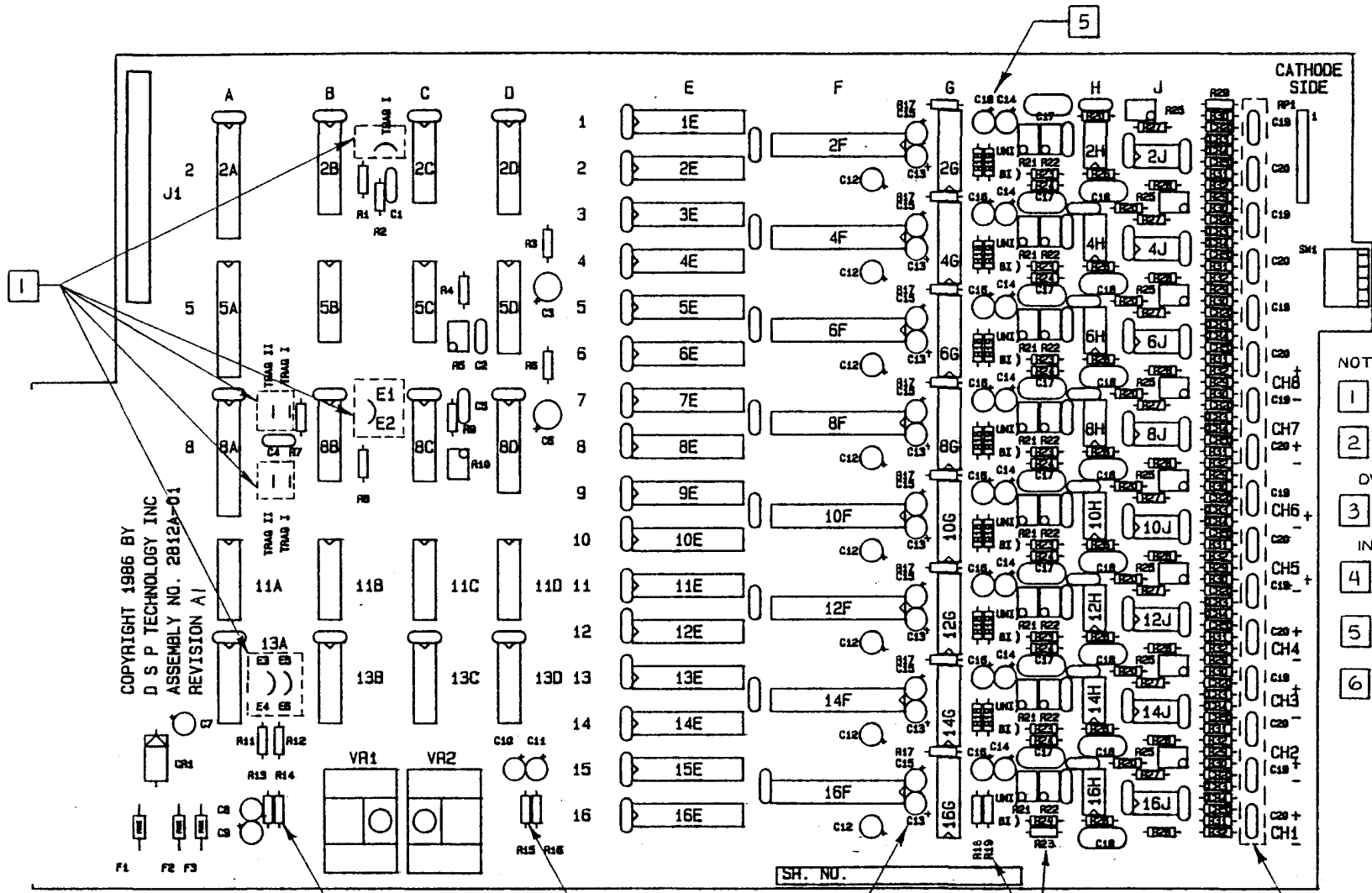


1

D S P TECHNOLOGY INC
9080 RAY RD., FREDRICK, CA 94520-7200 (415) 887-7800

SCHEMATIC, 2812A

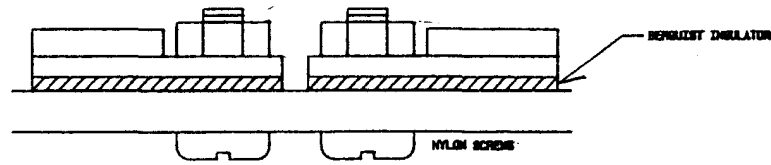
SIZE	FIG. NO.	DRAWING NO.	REVISION
03		A-2812A-01-SD	C
SCALE	NONE	SHEET	3 OF 3



COPYRIGHT 1986 BY
 D S P TECHNOLOGY INC
 ASSEMBLY NO. 2812A-01
 REVISION A1

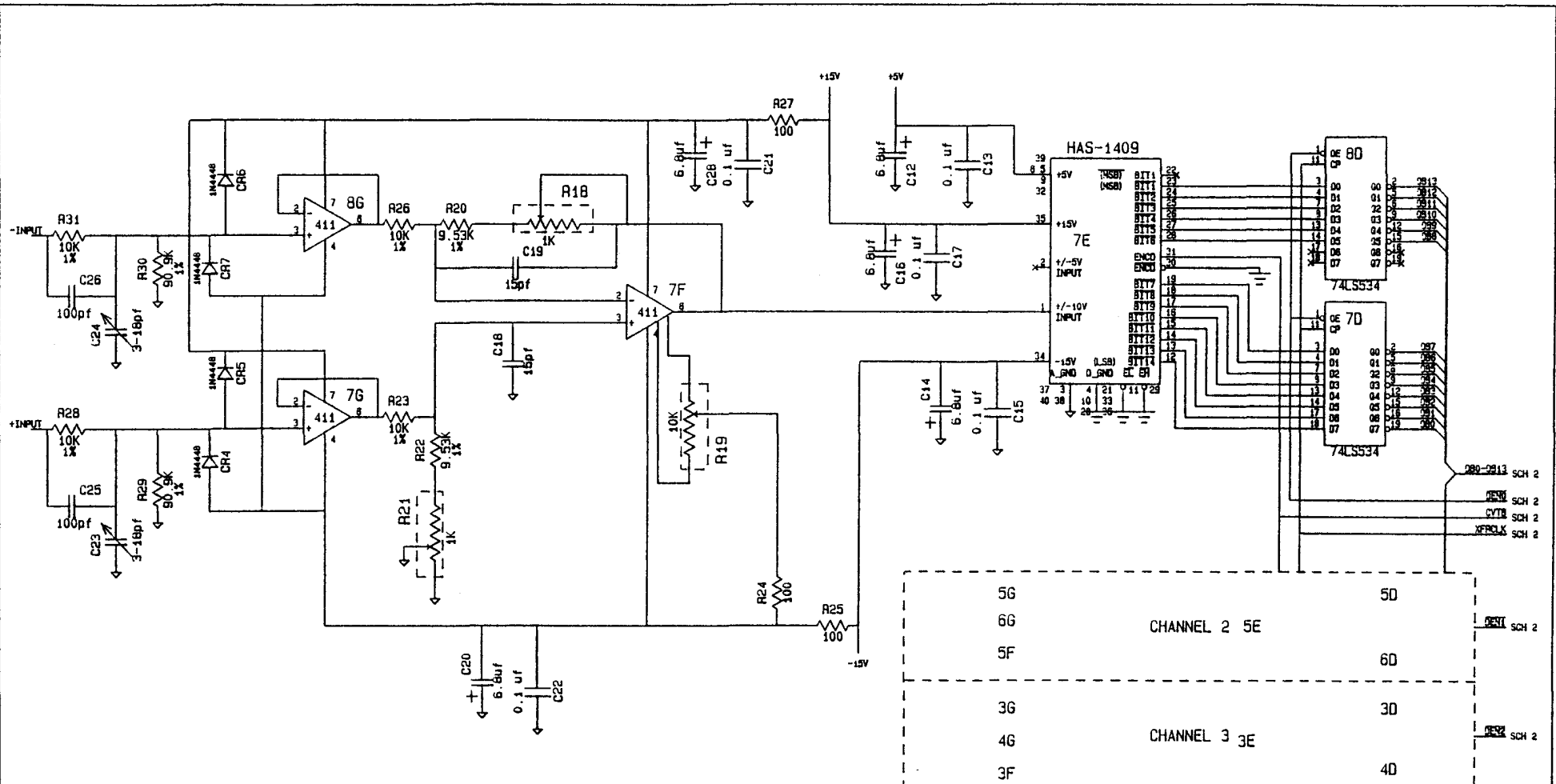
- NOTES:
- 1 MASK FOR WAVE
 - 2 INSTALL R14, R15 AFTER WAVE PER DWG # 2812A-01-CD
 - 3 C13 POLARITY SILKSCREEN INCORRECT (8 PLCS)
 - 4 C19 & C20 NO LOADS
 - 5 C18 3/8 C16 (1 PLC)
 - 6 SILKSCREEN INCORRECT

STANDARD JUMPERS	OPTIONAL JUMPERS TO BE INSTALLED AT TEST
BI (8 PLCS) *TRAQ II*	*TRAQ I* E1-E2 E3-E4 E5-E6 ON LAST UNIT IN SYSTEM

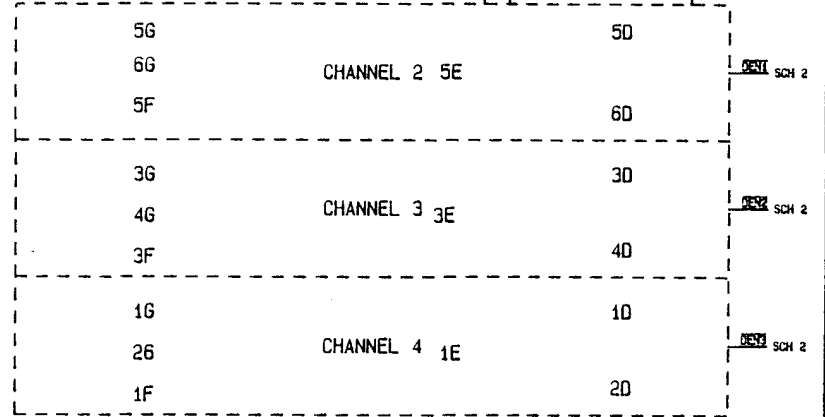


SIGNATURES		DATE	D S P TECHNOLOGY INC ASSEMBLY, 2812A
[Signature]		4/86	
REV		DESCRIPTION	DATE
A1	ECOP 1003	OK 1/77	
A	ECOP 1001	OK 1/77	
A	PROD RELEASE	4/86	
REV	DESCRIPTION	DATE	REV APPROVED
REVISIONS			

REV	FORM NO.	ISSUE NO.	ASSEMBLY
C		2812A-01-AD	AI
PAGE FULL		PAGE 1 OF 1	



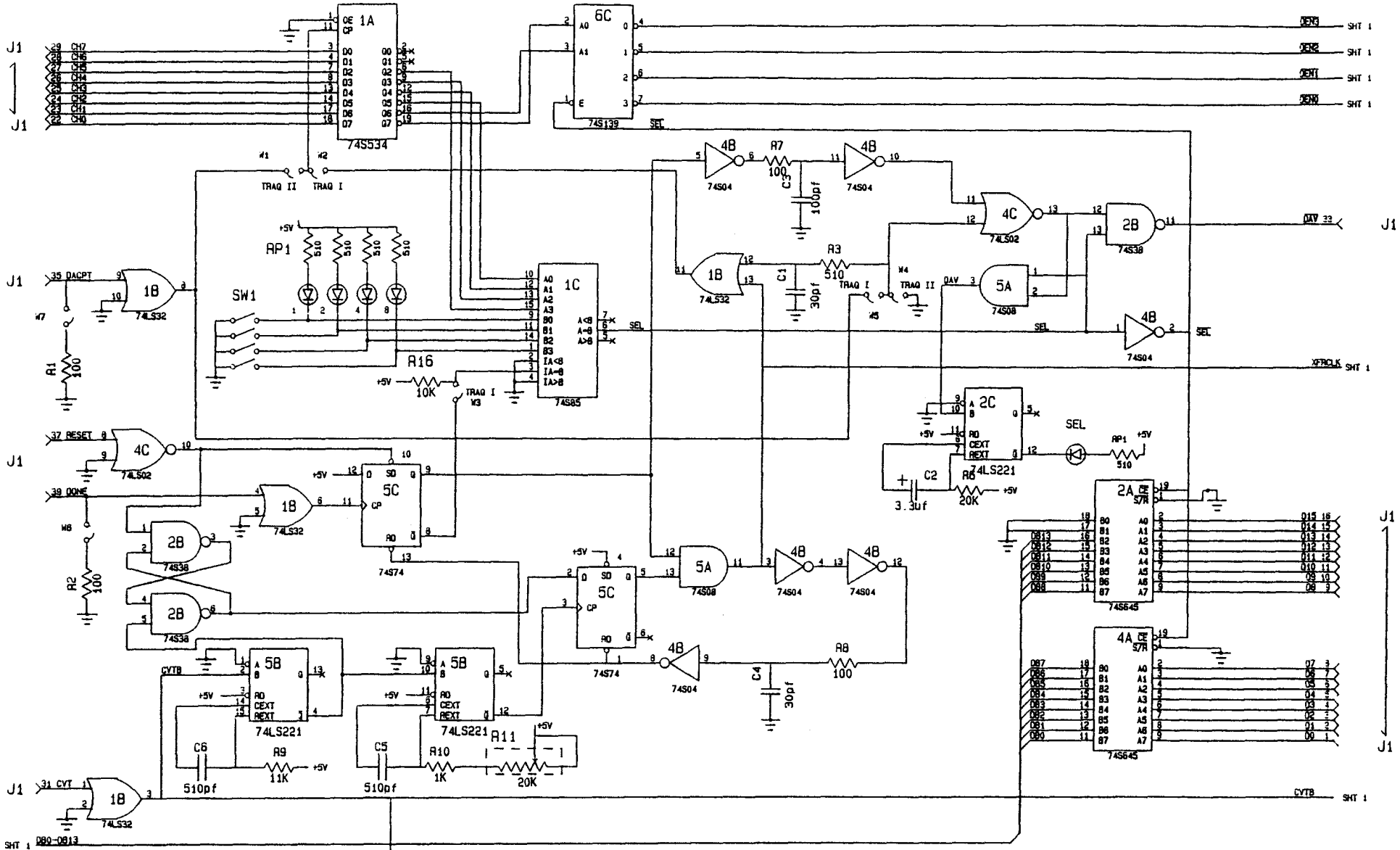
1 OF 4 IDENTICAL CHANNELS



NOTES. (UNLESS OTHERWISE SPECIFIED)

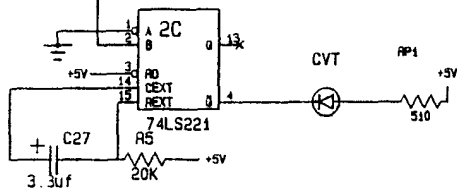
1. DENOTES DIGITAL GROUND.
2. DENOTES ANALOG GROUND.
3. ALL CAPACITORS ARE IN uF.
4. ALL RESISTORS ARE IN OHMS.

SIGNATURES		DATE	D S P TECHNOLOGY INC 4000 BAY RD. FRENCH CREEK, CA 94520-7200 415.827-1200
DESIGNED			
DRAWN	M. PERALTA	3/86	
CHECKED	P. M.	11/86	
APPROVED			
A1	ECO 028148	11/91	SCHEMATIC, 2814
A	ECO 119111	3/96	
REV	DESCRIPTION	DATE	SCALE
	REVISIONS		NONE
		DESIGN NO.	2814-01-SD
		REVISION	A1
		SHEET	1 OF 3



NOTES: (UNLESS OTHERWISE SPECIFIED)

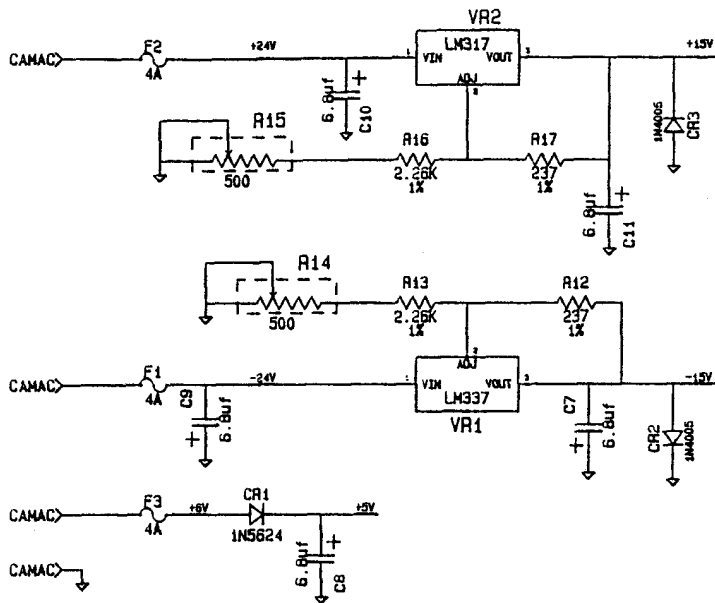
1. \perp DENOTES DIGITAL GROUND.
2. \downarrow DENOTES ANALOG GROUND.
3. ALL CAPACITORS ARE IN μ F.
4. ALL RESISTORS ARE IN OHMS.



SIGNATURES		DATE	D S P TECHNOLOGY INC		
DESIGNED BY	PERALTA	3/88	4800 KATE RD. PHOENIX, CA 84000-7300 (48) 800-7300		
CHECKED			SCHEMATIC, 2814		
APPROVED					
DATE			SIZE	PAGE NO.	REVISION
			02	2814-01-SD	A1
SCALE			NONE	SHEET	2 OF 3

TRAQ I (ONE CARD PER SYSTEM ONLY)
 W2, W3, W5, W6, W7

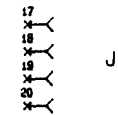
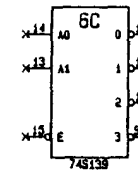
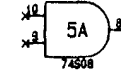
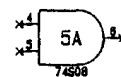
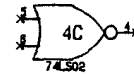
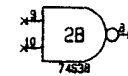
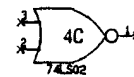
TRAQ II OPT A
 W1, W4 INSTALLED



NOTES. (UNLESS OTHERWISE SPECIFIED)

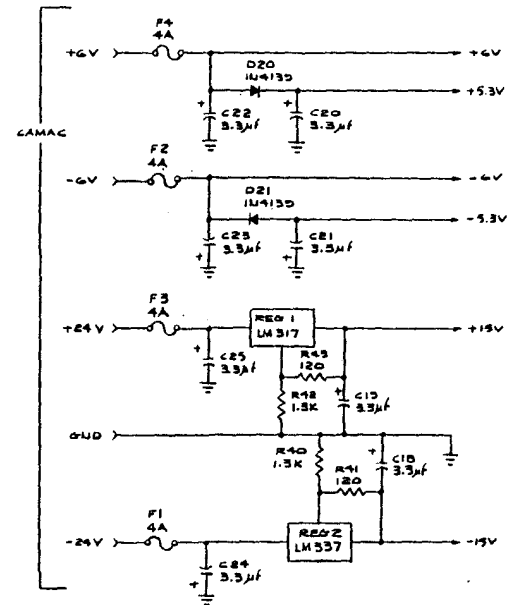
1. DENOTES DIGITAL GROUND.
2. DENOTES ANALOG GROUND.
3. ALL CAPACITORS ARE IN uF.
4. ALL RESISTORS ARE IN OHMS.

SPARES



SIGNATURES		DATE	D S P TECHNOLOGY INC	
DESIGNED BY		3/86	4000 BAY BLVD., FREDERICK, CA 95501-7200 (408) 867-7200	
DRAWN BY PERALTA			SCHEMATIC, 2814	
CHECKED BY				
APPROVED BY				
SIZE	FORM NO.	DRAWING NO.	REVISED	
	03	2814-01-SD	A1	
SCALE	NONE	SHEET	3	OF 3

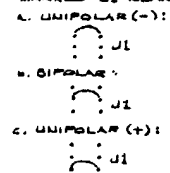
REV. NO.		REV.	REVISIONS	
REV.	NO.	DESCRIPTION	DATE	APPROVED
C	ECO 1003		3-21-84	
D	ECO 1012		10-22-84	
D	ECO 1014, 1015	ADDED COVER BIT	11-2-88	JWC
D	ECO 1017, 1018, 1019		6-1-90	JWC
D	ECO 035133, 035145		2-20-92	JWC



NOTES: OPTIONS

- FOR 2824 OPTION "A"
 - R37 = 0Ω (JUMPER)
 - C17 IS NOT LOADED
 - INSTALL TRAPEZ JUMPERS.
- FOR 2824
 - R37 = 510Ω
 - C17 = 100PF
 - INSTALL THE FOLLOWING JUMPERS.

TRAP Z
E4 - E5 (ONLY ON ONE UNIT IN THE SYSTEM)
E6 - E7 (ONLY ON ONE UNIT IN THE SYSTEM)
- FULL SCALE INPUT OPTIONS:
REFER TO COMPONENT SIDE OF PCB AT GROUP OF JUMPER SOCKETS MARKED "UI" NEAR FRONT PANEL.



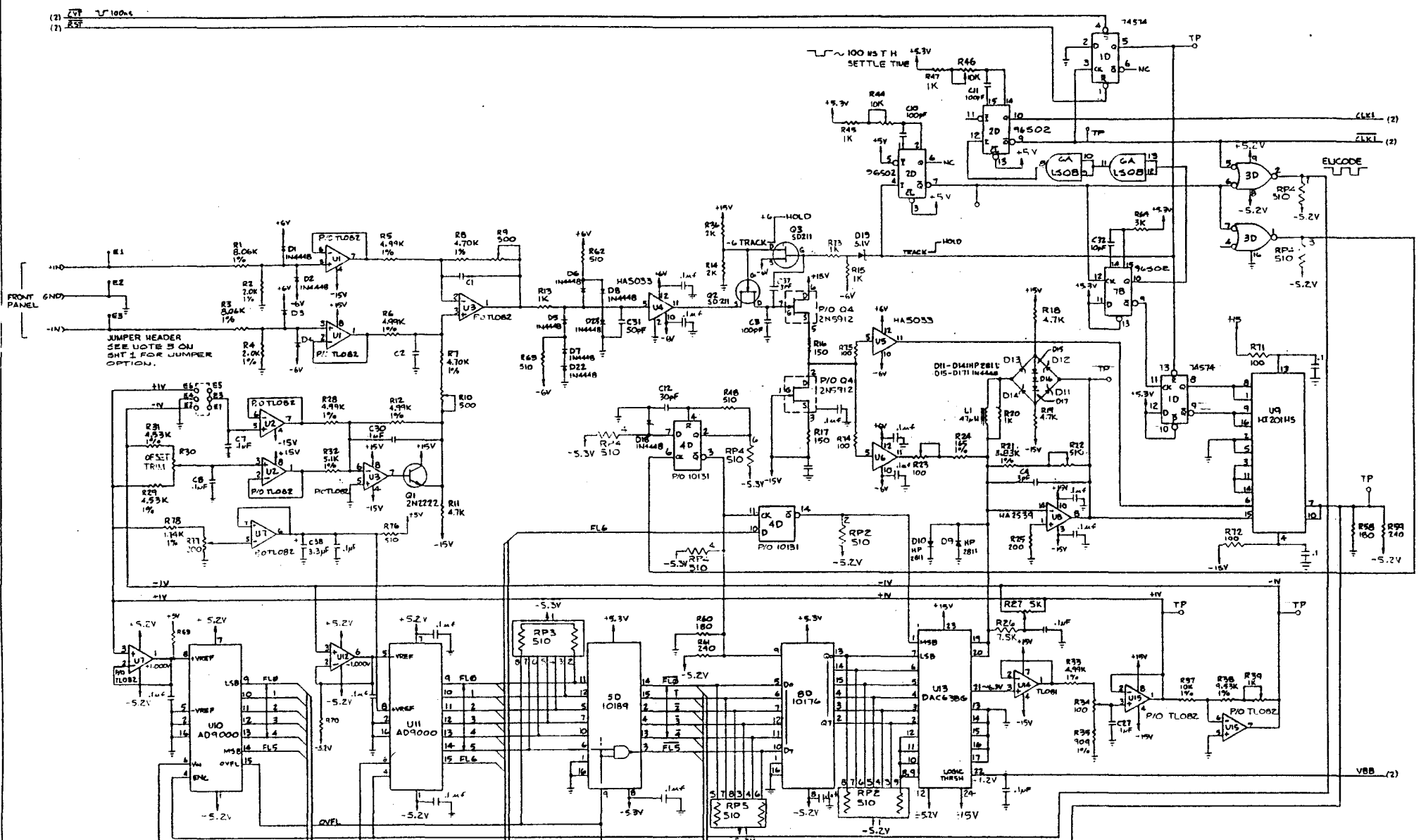
REV. NO.	REV.	DESCRIPTION	DATE	APPROVED
C	ECO 1003		3-21-84	
D	ECO 1012		10-22-84	
D	ECO 1014, 1015	ADDED COVER BIT	11-2-88	JWC
D	ECO 1017, 1018, 1019		6-1-90	JWC
D	ECO 035133, 035145		2-20-92	JWC

DATE	2/8/80
DESIGNER	JWC
CHECKED	
DATE	
DESIGNER	
CHECKED	

CONTRACT NO.	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES FRACTIONS DECIMALS ANGLES 32 1/2 1	
NATIONAL	
FORM	
DATE	
DESIGNER	
CHECKED	
DATE	
DESIGNER	
CHECKED	

APPLICATION	DO NOT SCALE DRAWING
SCALE	
SHEET 1 OF 3	

(2) V₁ 1/100k
 (7) R57



JUMPER HEADER
 SEE NOTE 3 ON
 SH1-1 FOR JUMPER
 OPTION.

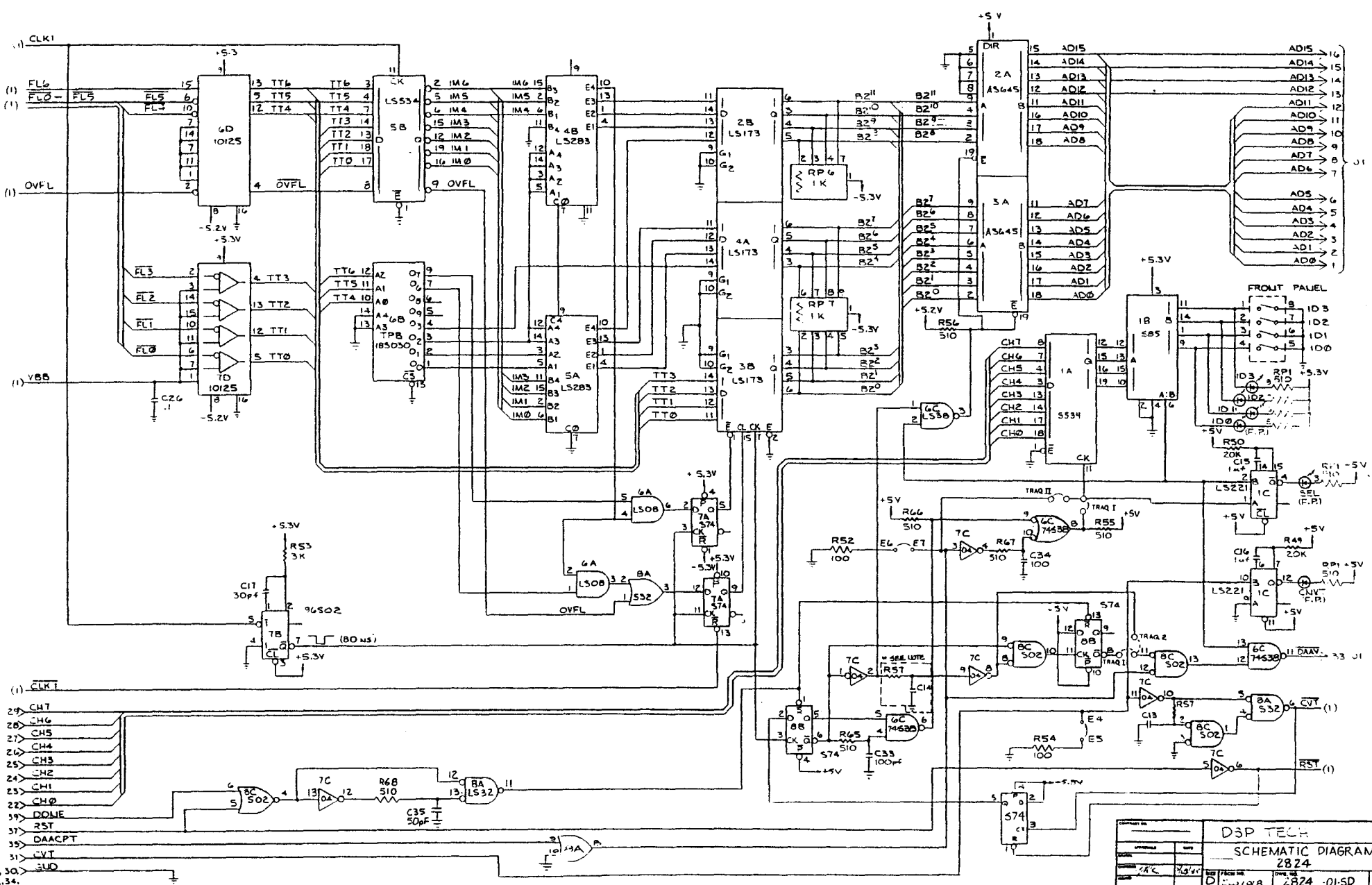
100 MS T H
 SETTLE TIME

(2) CLK1
 (2) CLK2

VBB (2)







FL6 (2)
 OVFL (2)
 FL5 - FL3 (2)

DSP TECH SCHEMATIC DIAGRAM 2824		DATE: 7/11/85 DRAWN BY: D. G. WILSON CHECKED BY: J. W. HARRIS SCALE: 1:1 SHEET: 1 OF 1
---------------------------------------	--	--

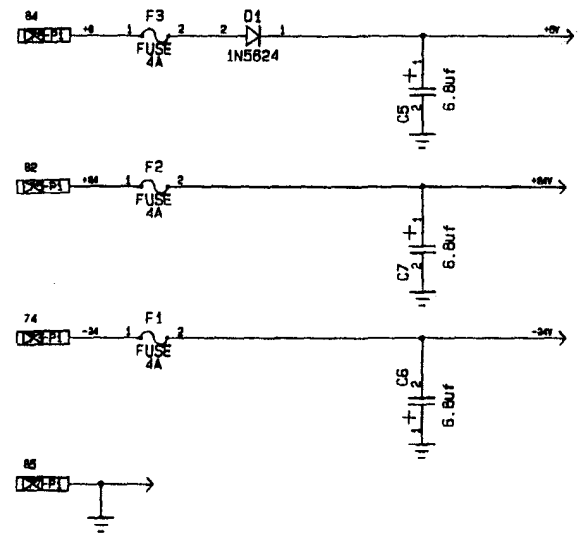


DSP TECH			
SCHEMATIC DIAGRAM			
2824			
DESIGNED BY	DATE	REV	NO.
CHK'D BY	DATE	REV	NO.
SCALE	2824-01-SD		1/1
SCALE			SHEET 3 OF 3

SYMBOLS:

-  DAMAC EDGE CONNECTOR
-  EXTERNAL CONNECTOR
-  CONTINUE ON SAME SHEET
-  CONTINUE ON DIFFERENT SHEET
-  UNUSED PIN
-  JUMPERS

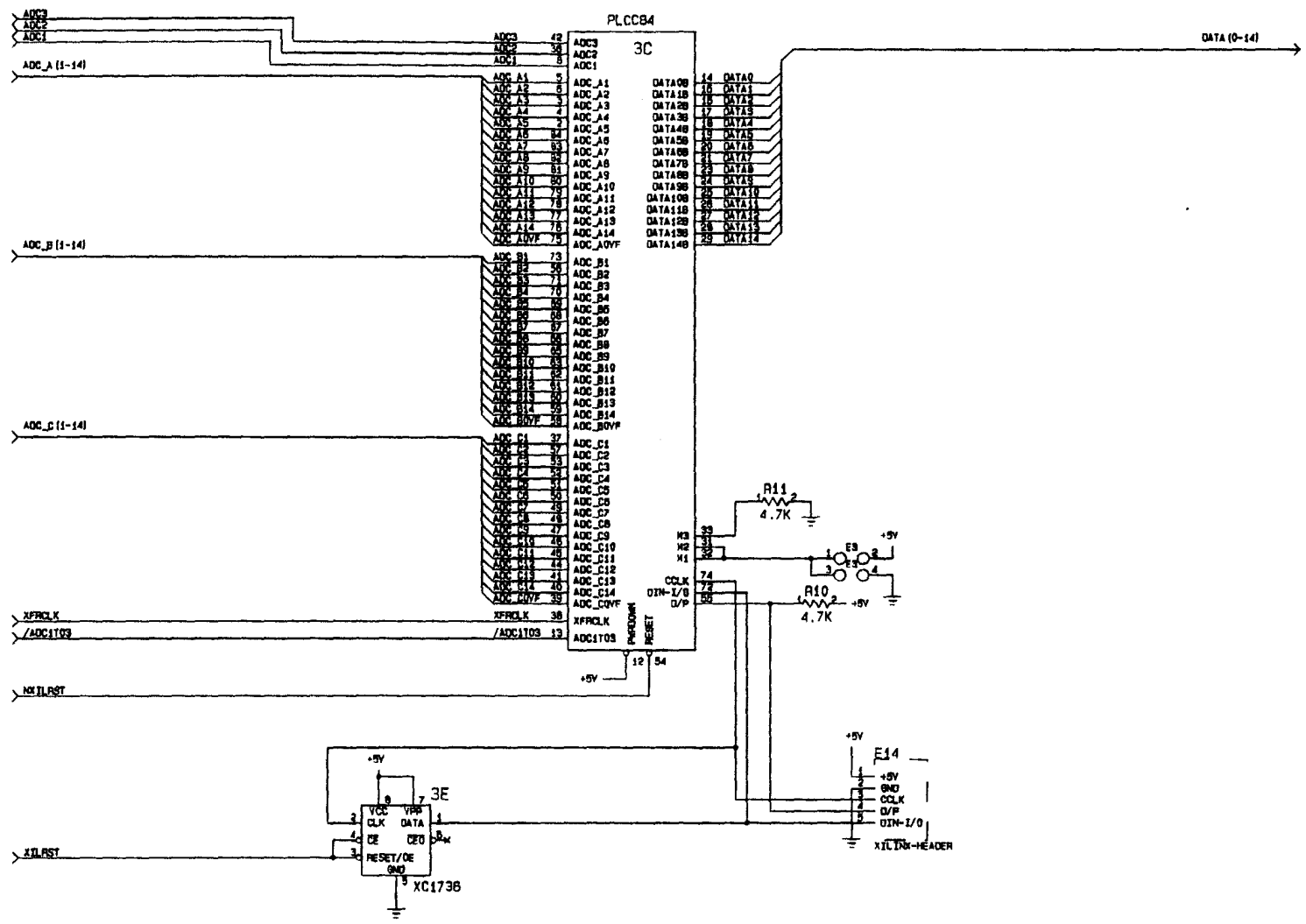
REVISIONS						
ECOM	REV	BY	DATE	DESCRIPTION	APPROV	DATE



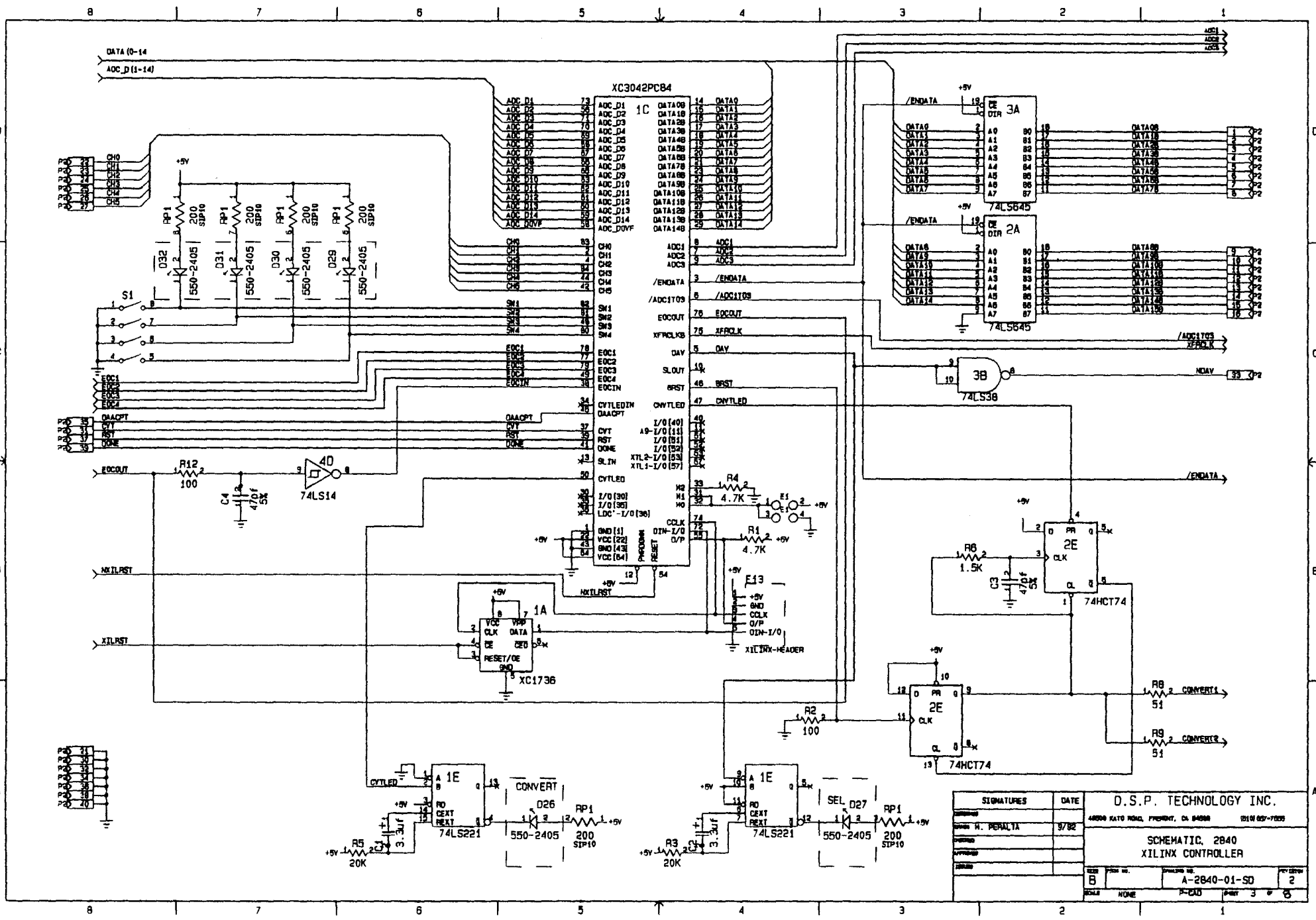
NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE IN UF.
2. ALL RESISTORS ARE 1/4W 5% AND IN OHMS.

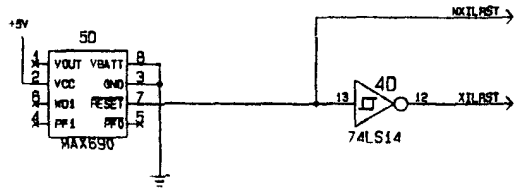
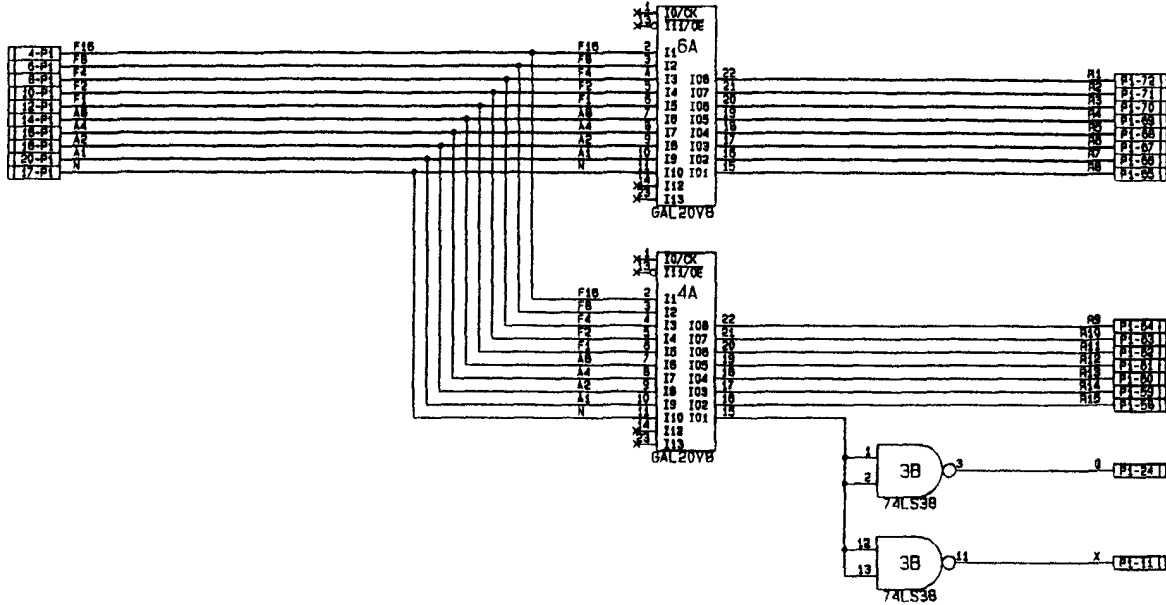
SIGNATURES		DATE	D.S.P. TECHNOLOGY INC	
DESIGNED		9/92	4800 KATO ROAD, FRENCH, CA 94508 (510) 807-7000	
DRAWN			SCHEMATIC, 2840	
CHECKED			POWER	
APPROVED			REV	REV DATE
DATE			B	2
SCALE		NONE	P-CAD	REV 1



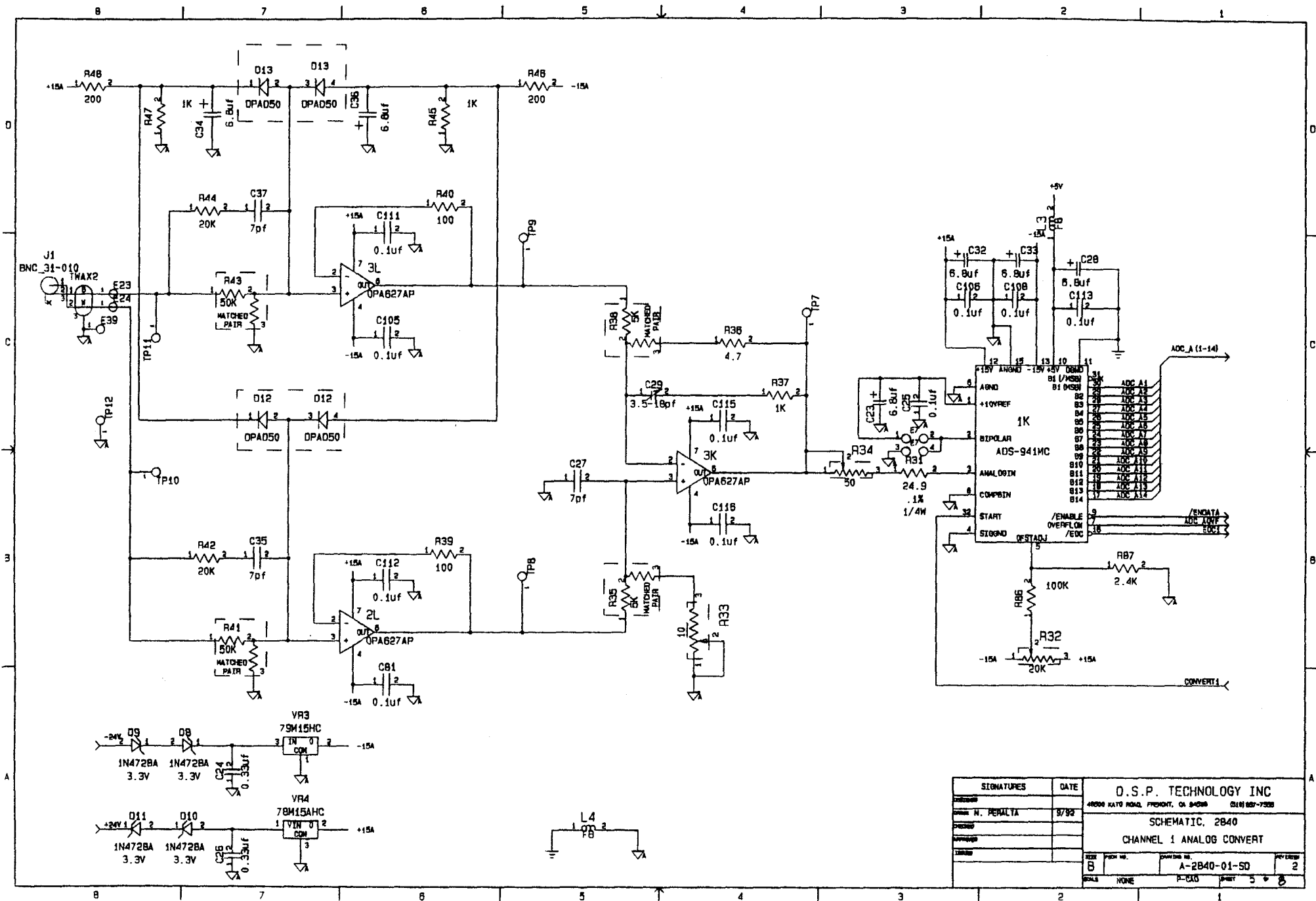
SIGNATURES	DATE		
DESIGNED BY			
DRAWN BY N. PENALTA	3/92	SCHEMATIC, 2840	
CHECKED BY		XILINX BUS DRIVER	
APPROVED BY			
DATE		REV	FROM FILE
		B	A-2840-01-SD
		SCALE	1:1 NONE
		PLANT	2



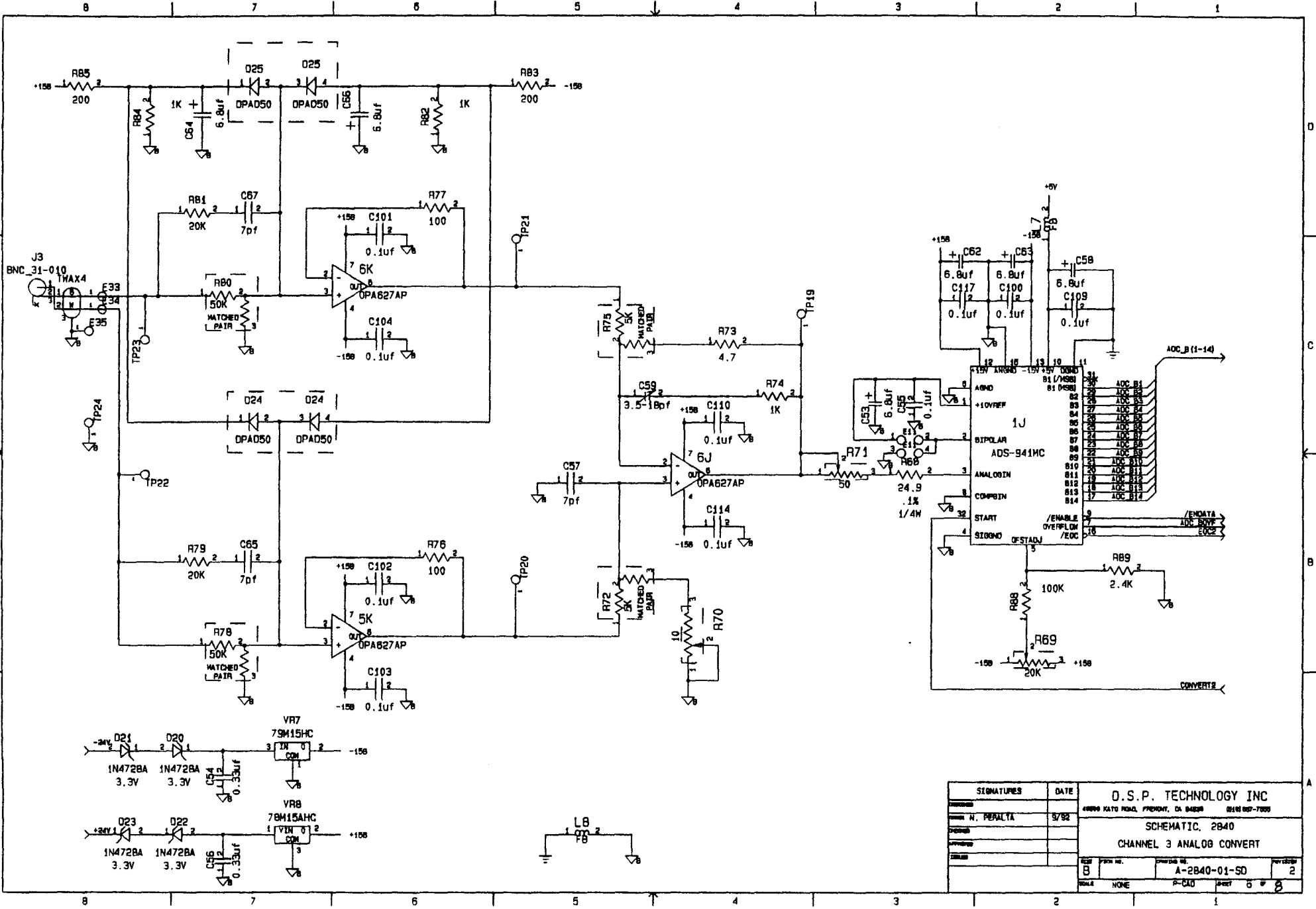
SIGNATURES		DATE	D.S.P. TECHNOLOGY INC.	
DESIGNED BY	H. PENALTA	9/92	4800 KATO ROAD, FREMONT, CA 94538 (510) 627-7000	
SCHEMATIC, 2840			XILINX CONTROLLER	
SIZE	B	FORM NO.	REV. NO.	A-2840-01-SD
SCALE	NONE	PAGE	3	OF 3



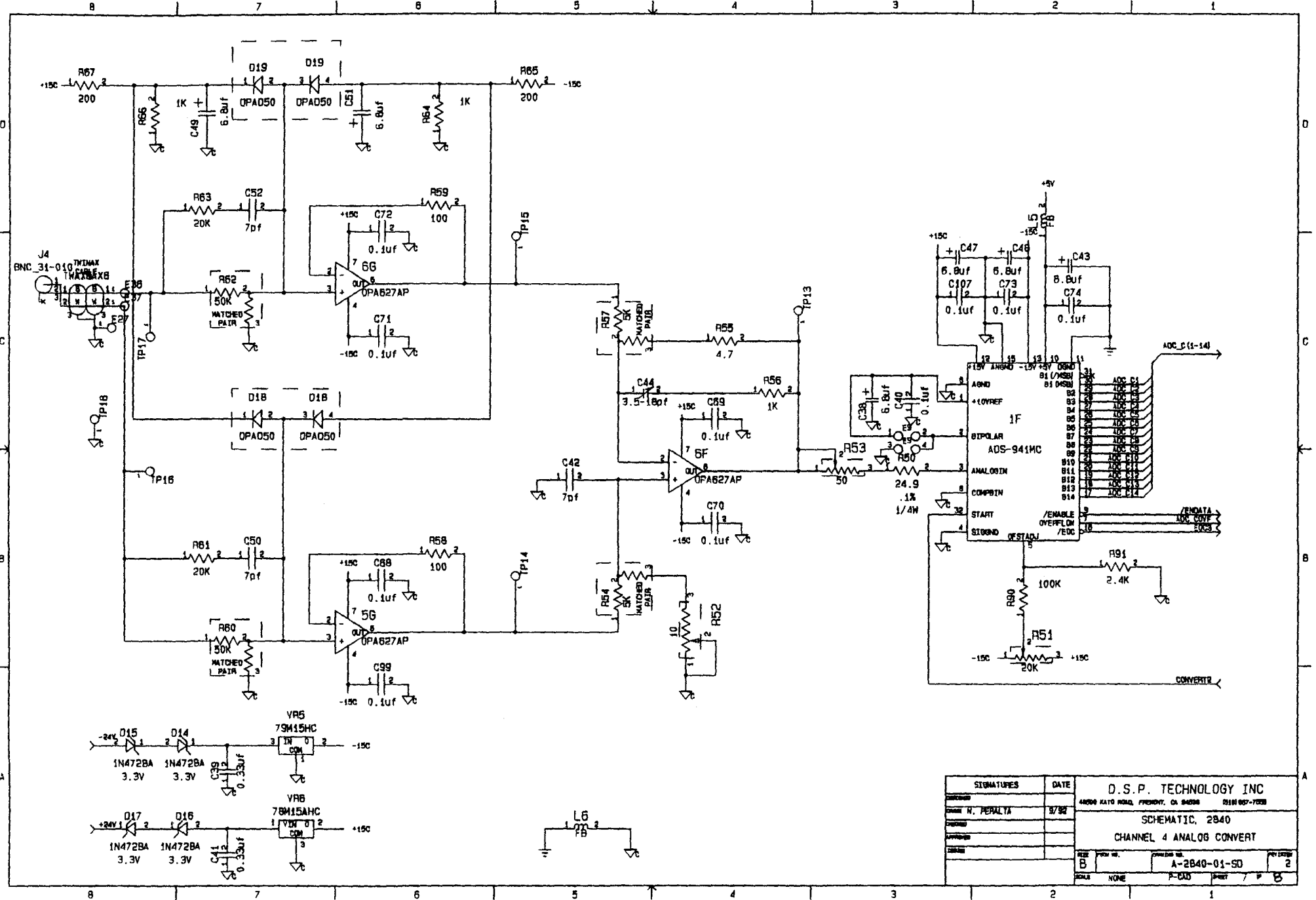
SIGNATURES	DATE	D.S.P. TECHNOLOGY INC	
DESIGNED BY		4800 KATO ROAD, FRESNO, CA 93726 (209) 687-1000	
DESIGNED BY	9/92	SCHEMATIC, 2840	
DESIGNED BY		CAMAC	
DESIGNED BY		SIZE	PAGE NO.
DESIGNED BY		B	A-2840-01-SD
DESIGNED BY		SCALE	SHEET #
DESIGNED BY		NONE	8



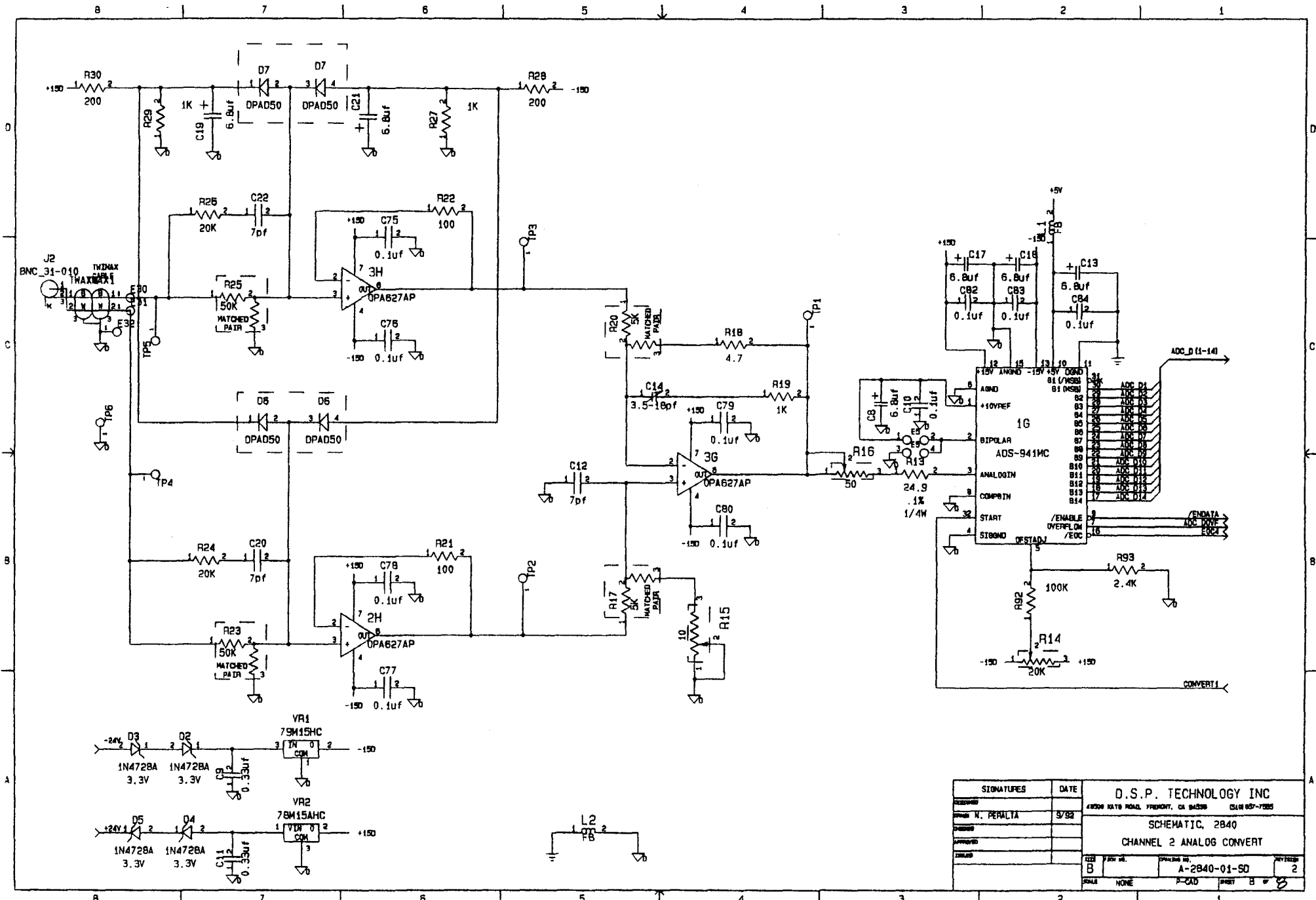
SIGNATURES		DATE	D.S.P. TECHNOLOGY INC	
DESIGNED BY		9/92	4000 KATO ROAD, FRENCH, CA 94508 (916) 837-7300	
CHECKED BY			SCHEMATIC, 2840	
APPROVED BY			CHANNEL 1 ANALOG CONVERT	
DATE			REV. FROM NO.	REV. DATE
REV. NO.			B	A-2840-01-50
SCALE		NONE	P-CAD	SHEET 5 OF 5



SIGNATURES		DATE	D.S.P. TECHNOLOGY INC	
DESIGNED BY	N. PEALTA	5/82	4800 KATO ROAD, FREDRICK, CA 94502 925/927-7000	
			SCHEMATIC, 2840	
			CHANNEL 3 ANALOG CONVERT	
REV	B	DATE	REV	2
BY	NONE	DATE	REV	2









SIGNATURES		DATE	D.S.P. TECHNOLOGY INC	
DESIGNED BY		9/82	4800 KATO ROAD, FREMONT, CA 94538 (916) 867-7000	
DRAWN BY			SCHEMATIC, 2840	
CHECKED BY			CHANNEL 4 ANALOG CONVERT	
APPROVED BY				
DATE				
REV	REV NO.	ISSUE NO.	REVISED	
B		A-2840-01-S0	2	
SCALE	NONE	F-CAD	SHEET	8



SIGNATURES		DATE	D.S.P. TECHNOLOGY INC	
DESIGNED			4850 WAYS ROAD, FORTUIT, CA 94539 (415) 957-7325	
DRAWN	N. PERALTA	5/92	SCHEMATIC, 2B40	
CHECKED			CHANNEL 2 ANALOG CONVERT	
ISSUED			REV. NO.	REVISED
			B	A-2B40-01-50
SCALE	NONE	A-CAD	SHEET	2

SYMBOLS:

-  CAMEC EDGE CONNECTOR
-  EXTERNAL CONNECTOR
-  CONTINUE ON SAME SHEET
-  CONTINUE ON DIFFERENT SHEET
-  UNUSED PIN
-  JUMPERS

STANDARD CONFIGURATION

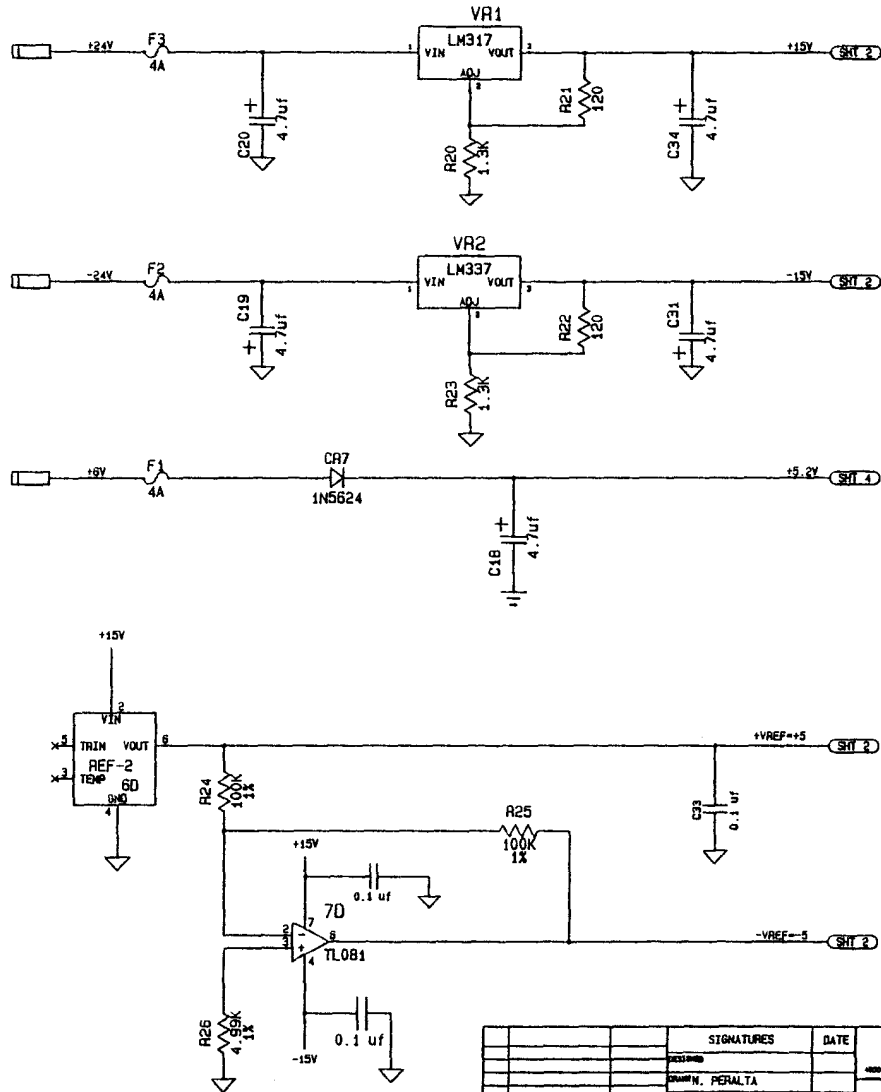
MODE	INSTALL
BIPOLAR	BT* (4 PLACES)
4012A	TRAQ II (2 PLACES)
10VFS	E7 - E8 (4 PLACES)
	E9 - E10 (4 PLACES)

OPTIONAL CONFIGURATION

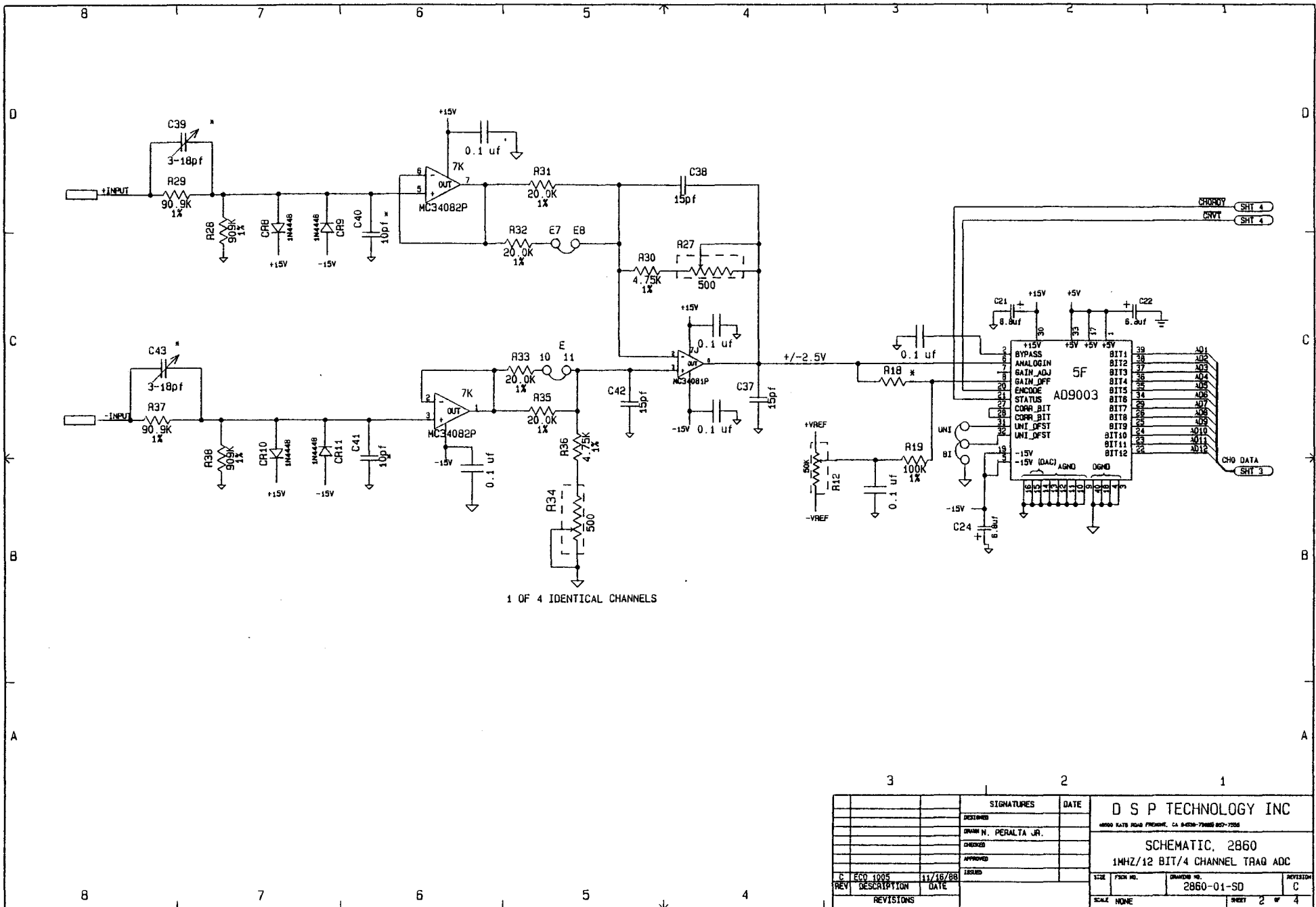
MODE	INSTALL
UNIPOLAR	UNI (4 PLACES)
20VFS	E7 - E8 NOT INSTALLED
	E9 - E10
4012	TRAQ I (3 PLACES)
	E1 - E2 ONLY ON ONE UNIT
	E3 - E4 IN THE SYSTEM
	E5 - E6

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE IN uF.
2. ALL RESISTORS ARE IN OHMS.
3. ↓ DENOTES ANALOG GROUND
4. ⊥ DENOTES DIGITAL GROUND
5. * NOT USED

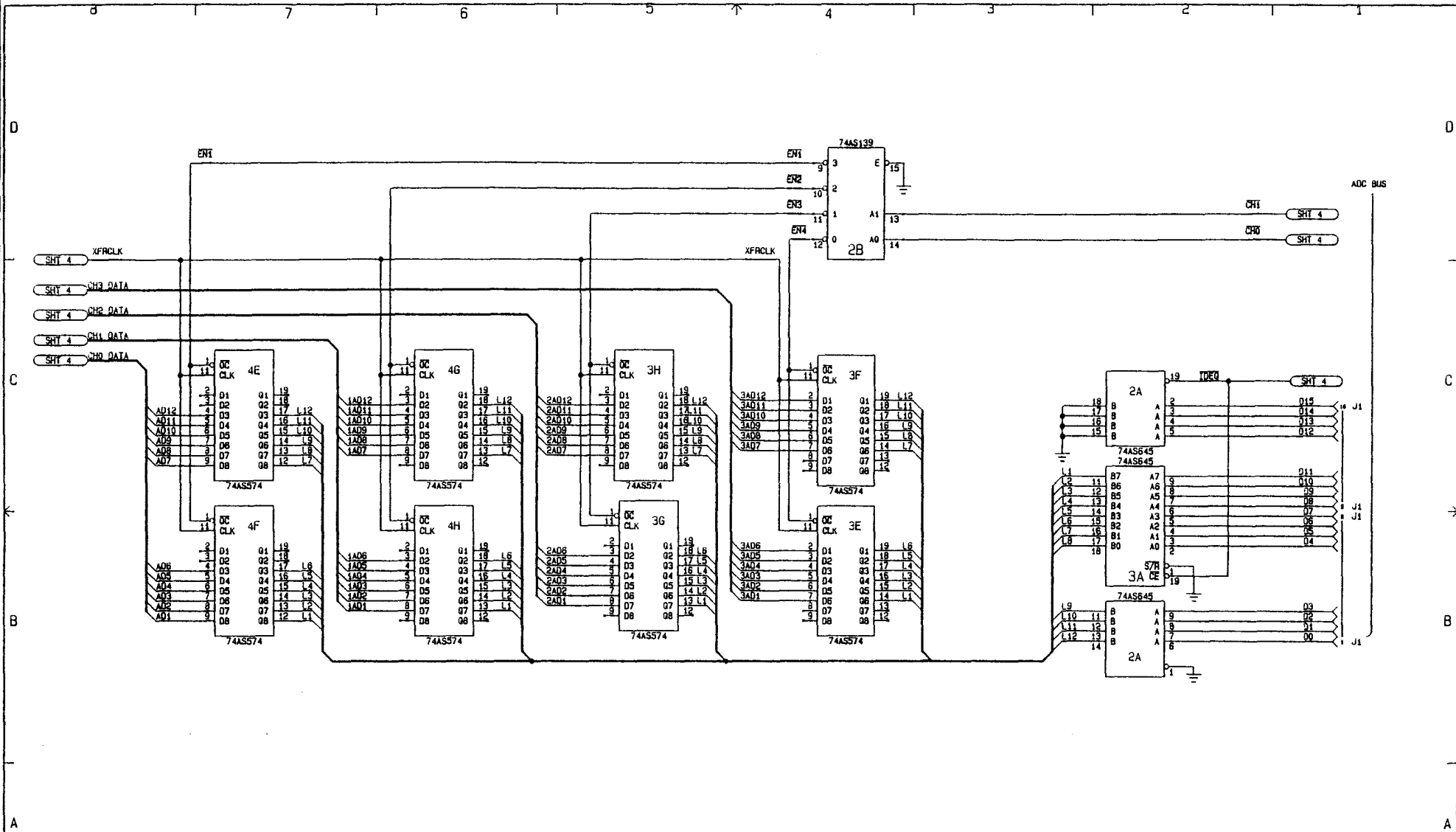


SIGNATURES		DATE	D S P TECHNOLOGY INC 4000 RALTO RD. FORTMCD, CA 94539-7200 (415) 857-7000
DESIGNED			
CHECKED			
APPROVED			
DATE			
REV	DESCRIPTION	DATE	
REVISIONS			
SIZE	TECH. NO.	PACKAGE NO.	REVISION
SCALE	HONE	2860-01-SD	C
SHEET 1 OF 4			

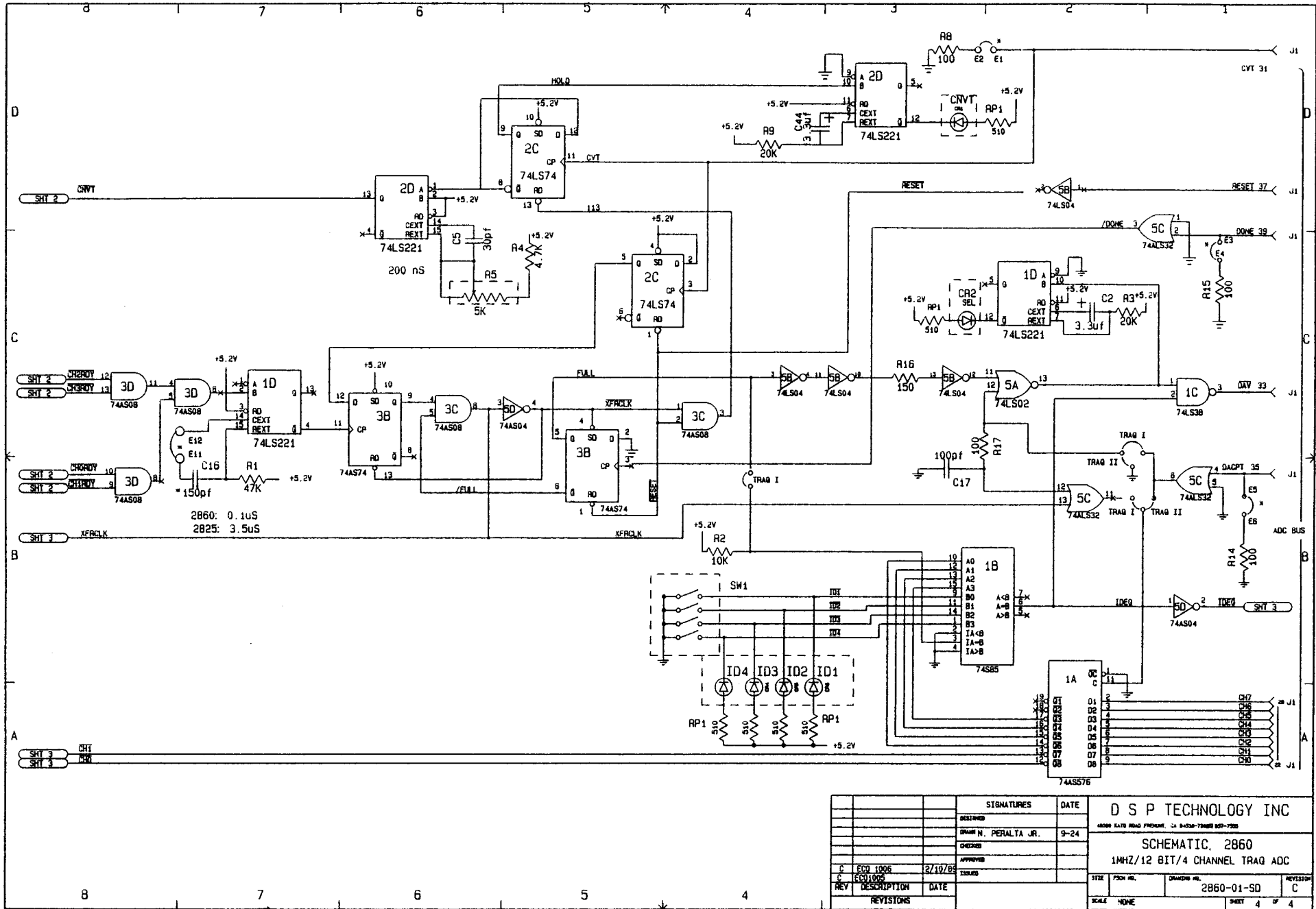


1 OF 4 IDENTICAL CHANNELS

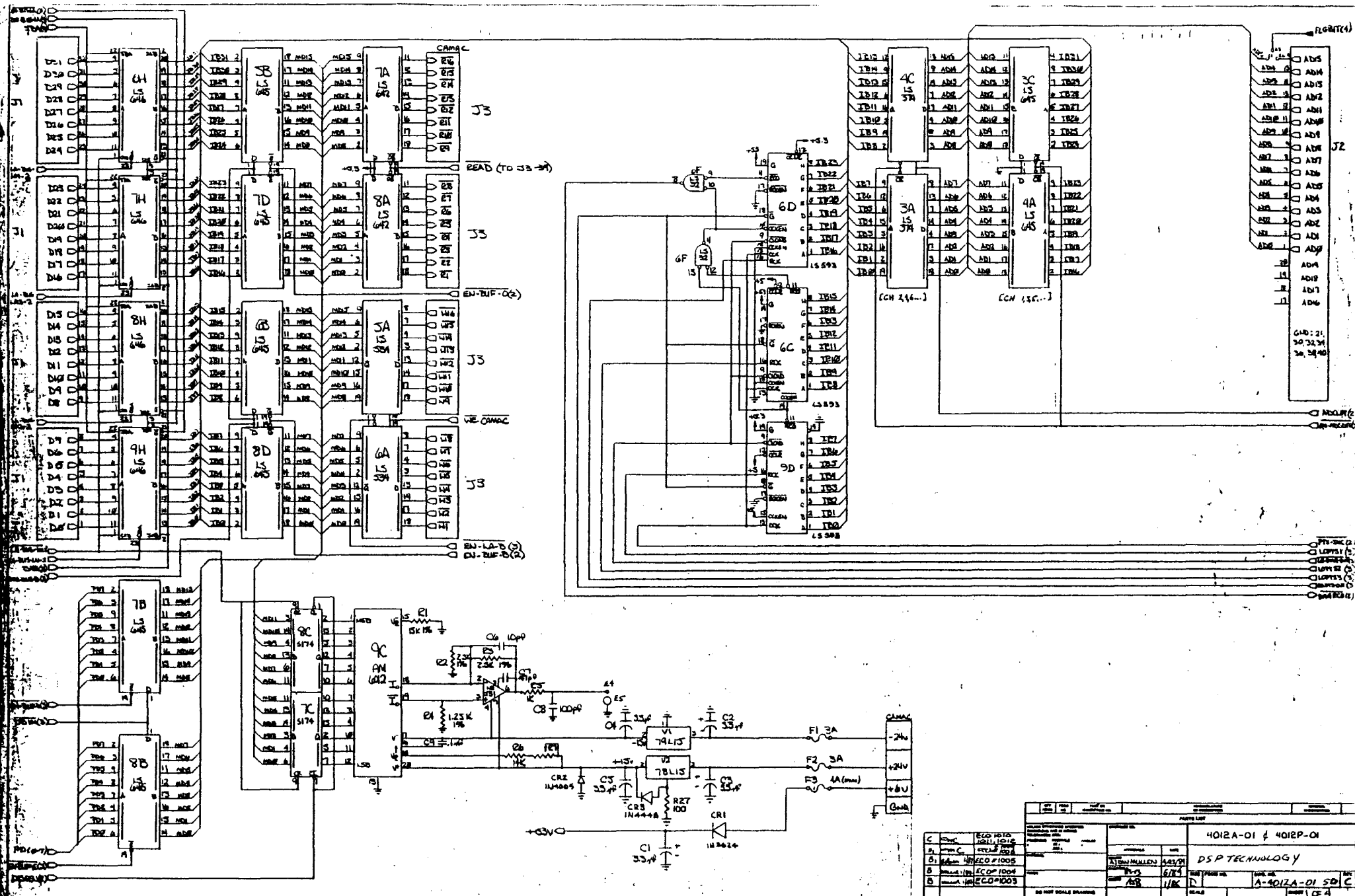
		SIGNATURES		DATE	D S P TECHNOLOGY INC		
		DESIGNED			4850 KATE ROAD FORTMCD, CA 94539-7988 857-7556		
		DRAWN N. PERALTA JR.			SCHEMATIC, 2860		
		CHECKED			1MHZ/12 BIT/4 CHANNEL TRAQ ADC		
		APPROVED			SIZE	PAGE NO.	REVISION
		ISSUED					
C	ECO 1005	11/16/88			2860-01-SD	C	
REV	DESCRIPTION	DATE			SCALE	NONE	SHEET 2 OF 4
REVISIONS							



		SIGNATURES		DATE	D S P TECHNOLOGY INC	
		DESIGNED		9-24	4000 KATE ROAD FREDONT, CA 94508-7286 (916) 758-7588	
		DRAWN N. PERALTA JR.			SCHEMATIC, 2860	
		CHECKED			1MHZ/12 BIT/4 CHANNEL TRAQ ADC	
		APPROVED			SITE FROM NO. DRAWING NO. REVISION	
		ISSUED			2860-01-SD C	
ECO 1004		11/16/88			SCALE NONE SHEET 3 OF 4	
REV DESCRIPTION		DATE				
REVISIONS						



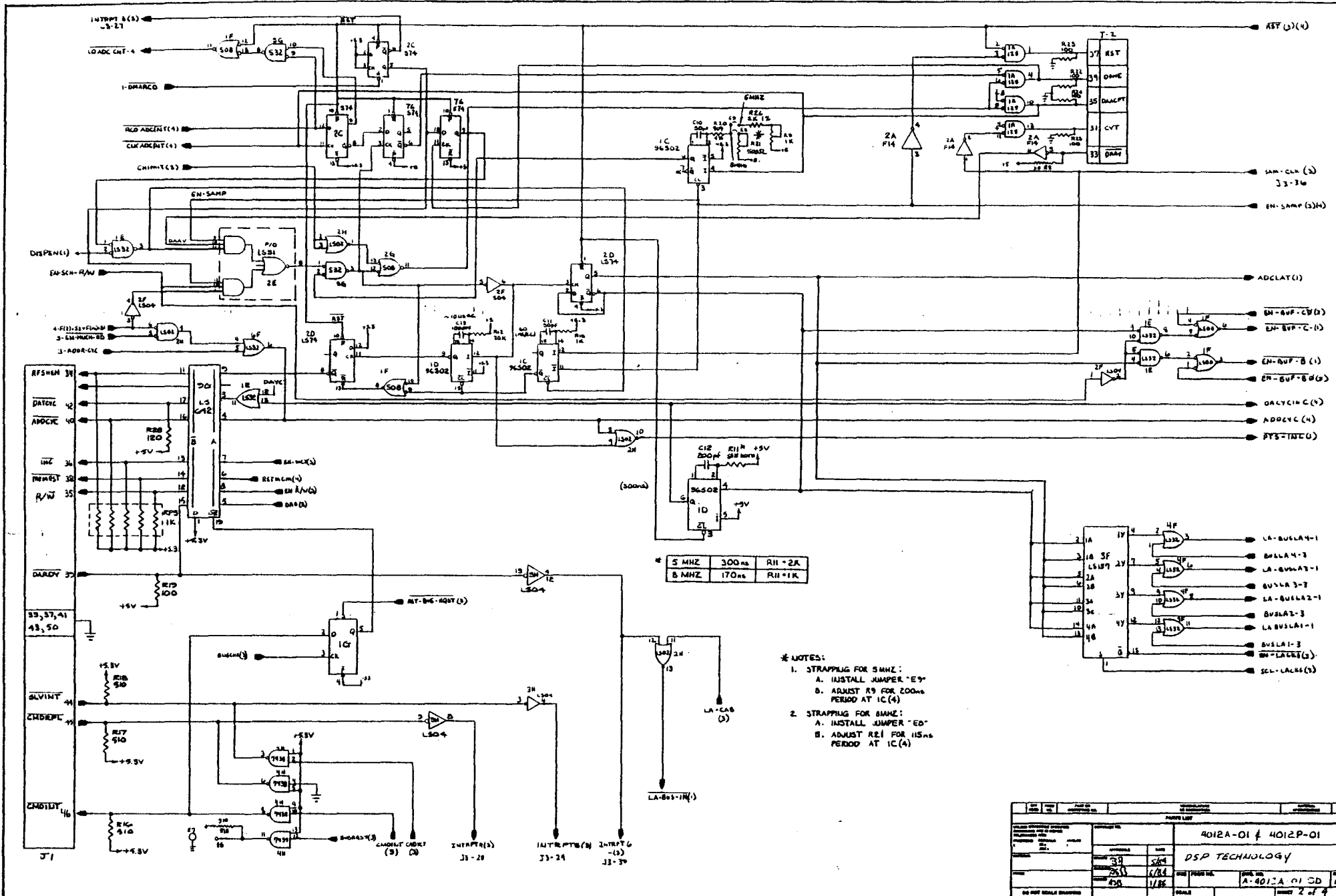
SIGNATURES		DATE	D S P TECHNOLOGY INC	
DESIGNED		9-24	4850 EAST ROAD, FRODOCT, CA 94533-7888 907-750-7500	
DRAWN N. PERALTA JR.			SCHEMATIC, 2860	
CHECKED			1MHZ/12 BIT/4 CHANNEL TRAQ ADC	
APPROVED			SIZE	FRON. NO.
C	EDJ 1006	2/10/95	13040	DRAWING NO.
C	ECJ 1005			2860-01-SD
REV	DESCRIPTION	DATE	SCALE	SHEET
	REVISIONS		NONE	4 OF 4



REVISIONS		PARTS LIST		DESCRIPTION	
NO.	DATE	BY	CHKD.	QTY.	UNIT
C	1/15/82	ECO	MSD	1	PCB
B	1/15/82	ECO	MSD	1	PCB
A	1/15/82	ECO	MSD	1	PCB

PARTS LIST		DESCRIPTION	
QTY.	UNIT	DESCRIPTION	REVISION
1	PCB	4012A-01 & 4012P-01	
		DSP TECHNOLOGY	
		DESIGNED BY	MSD
		DATE	1/15/82
		APP'D BY	MSD
		DATE	1/15/82
		REV. NO.	1
		REV. DATE	1/15/82

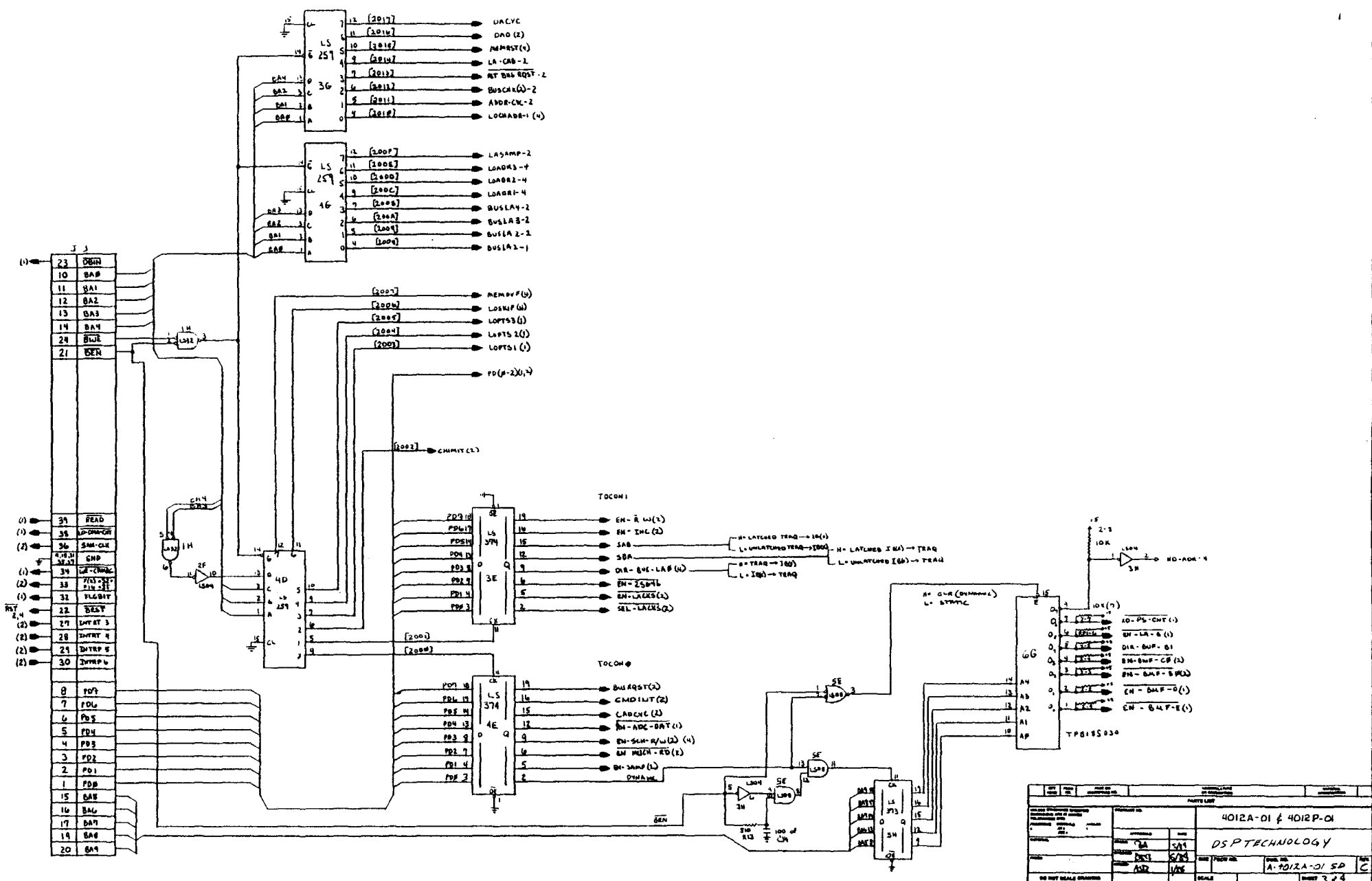
© 1982 DSP



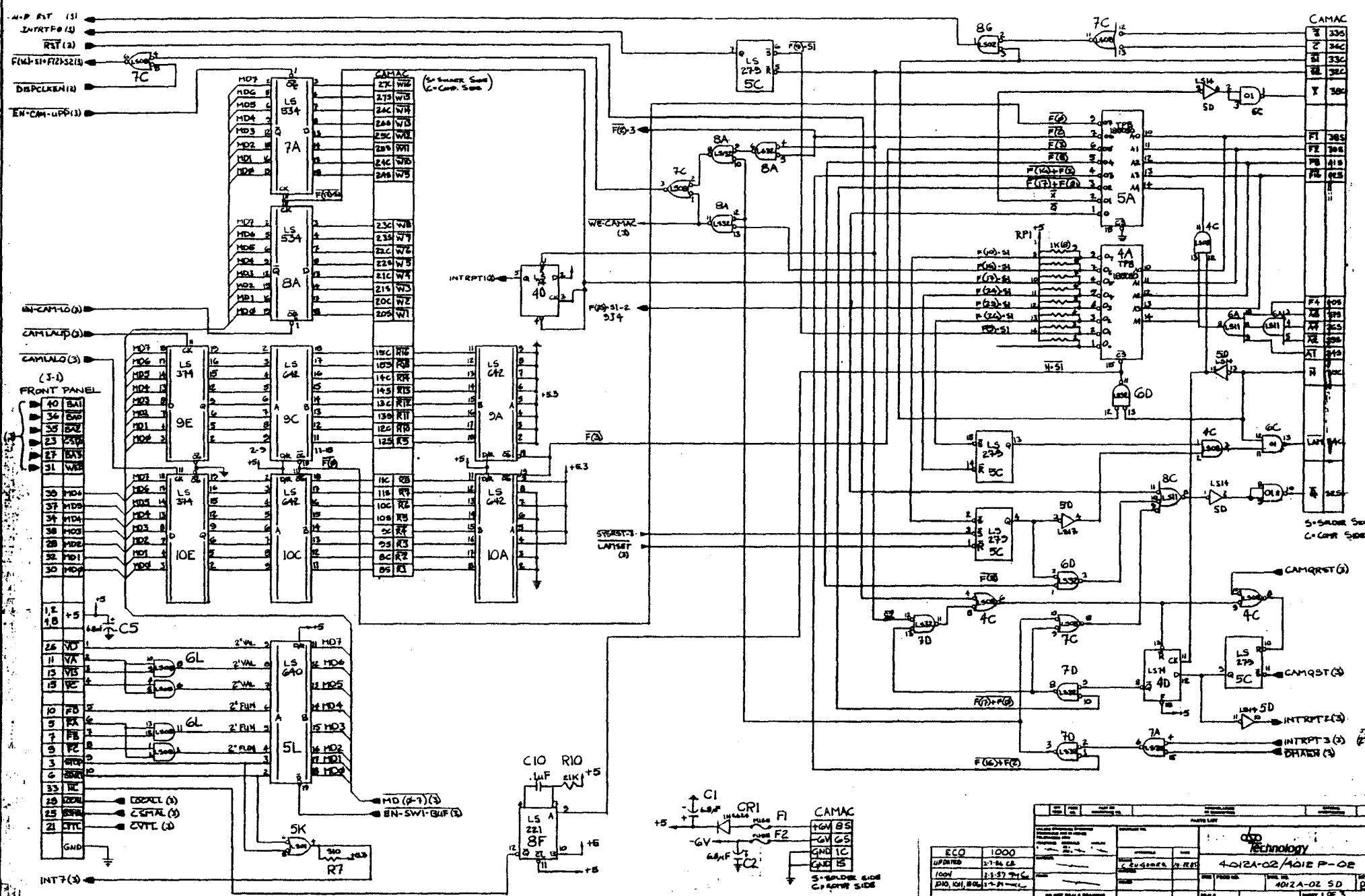
5 MHz	300ns	R9 = 2K
8 MHz	170ns	R2 = 1K

- * NOTES:
- STRAPPING FOR 5MHZ:
 - INSTALL JUMPER "E"
 - ADJUST R9 FOR 300ns PERIOD AT IC(A)
 - STRAPPING FOR 8MHZ:
 - INSTALL JUMPER "ED"
 - ADJUST R2 FOR 175ns PERIOD AT IC(A)

PARTS LIST		REVISIONS	
QTY	DESCRIPTION	NO.	DATE
1	4012A-01 & 4012P-01	1	1/84
1	DSP TECHNOLOGY	2	1/88
1	LA-4012A-01-01	1	1/88
1	LA-4012P-01-01	1	1/88



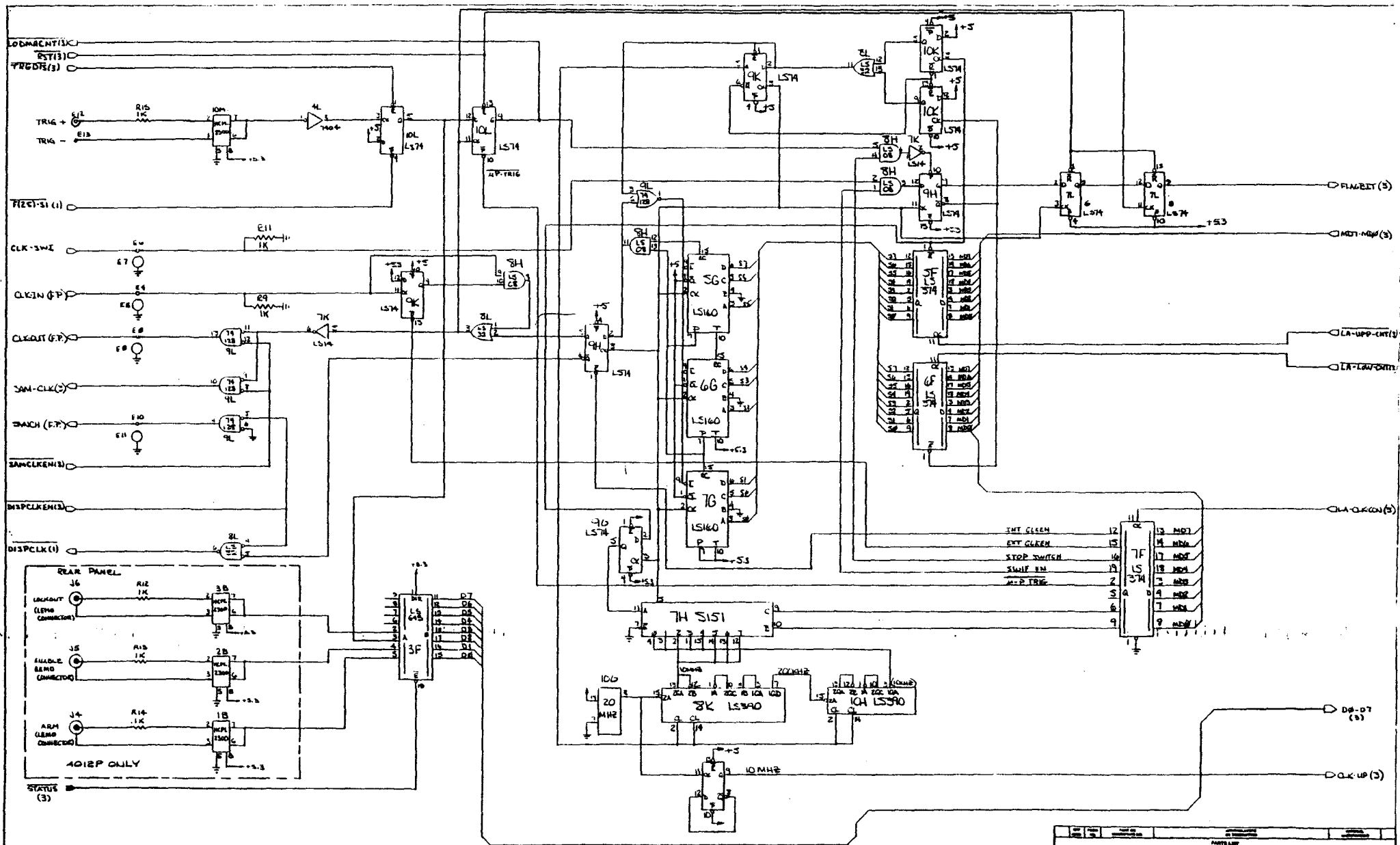
REV		DATE		DESCRIPTION	
1					
PARTS LIST					
4012A-DI & 4012P-DI					
DSPT TECHNOLOGY					
Part No.	QTY	Part No.	QTY	Part No.	QTY
4012A	1	4012P	1	4012A-DI SP	1
4012B	1	4012Q	1		
SCALE					
Sheet 3 of 4					



ECO		1000		4012A-02/4012P-02	
UPDATED	2-7-84 CE	DESIGNED BY	CE	DATE	11-27-76
100N	11-27-76	DESIGNED BY	CE	DATE	11-27-76
210, 101, 201	11-27-76	DESIGNED BY	CE	DATE	11-27-76

S-SOLDER SIDE
C-CAPACITOR SIDE

S-SOLDER SIDE
C-CAPACITOR SIDE

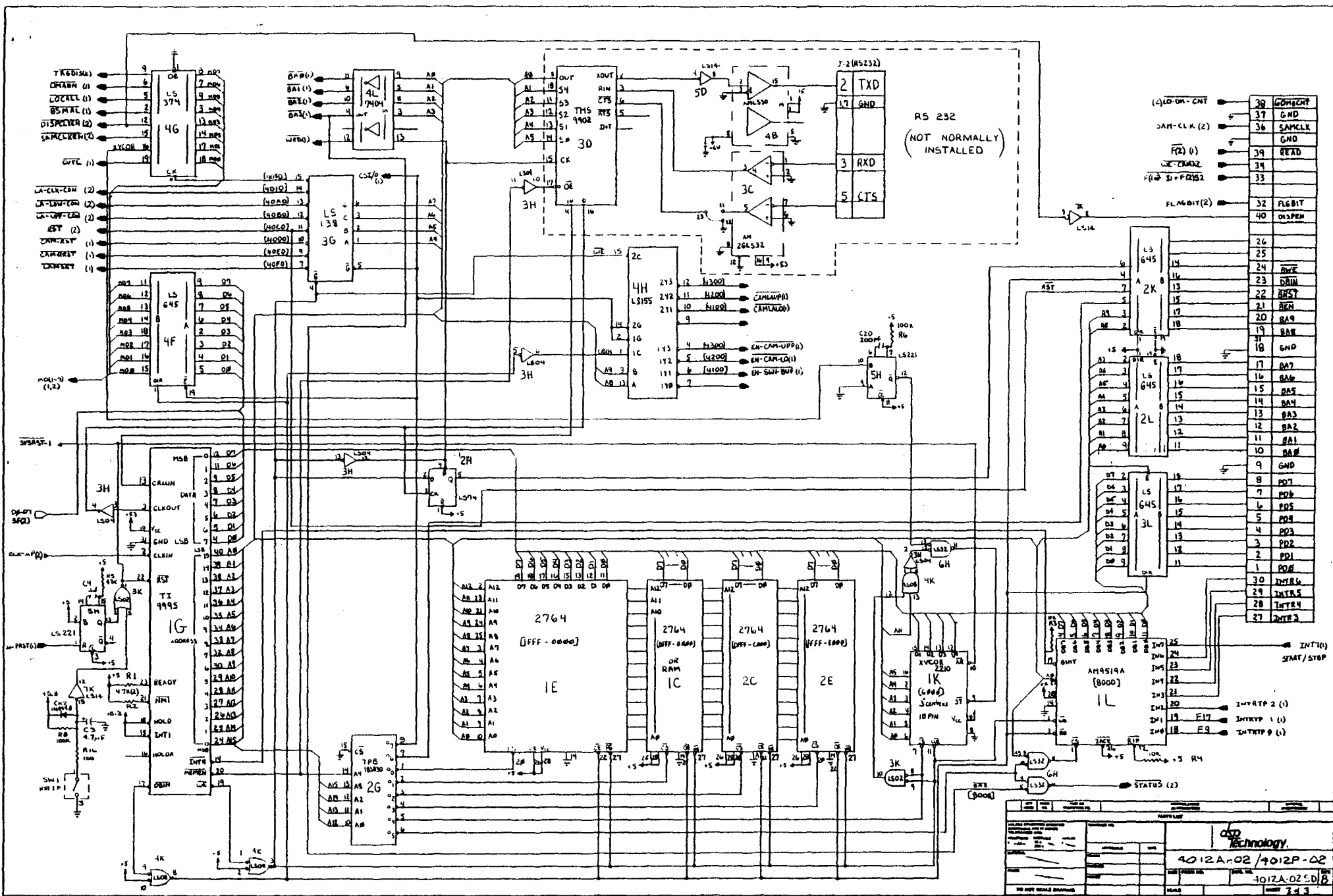


PARTS LIST	
74LS151	1
74LS155	1
74LS160	3
74LS158	1
74LS10	1
74LS00	1
74LS04	1
74LS08	1
74LS02	1
74LS01	1
74LS03	1
74LS05	1
74LS07	1
74LS09	1
74LS11	1
74LS12	1
74LS13	1
74LS14	1
74LS16	1
74LS17	1
74LS18	1
74LS19	1
74LS20	1
74LS21	1
74LS22	1
74LS23	1
74LS24	1
74LS25	1
74LS26	1
74LS27	1
74LS28	1
74LS29	1
74LS30	1
74LS31	1
74LS32	1
74LS33	1
74LS34	1
74LS35	1
74LS36	1
74LS37	1
74LS38	1
74LS39	1
74LS40	1
74LS41	1
74LS42	1
74LS43	1
74LS44	1
74LS45	1
74LS46	1
74LS47	1
74LS48	1
74LS49	1
74LS50	1
74LS51	1
74LS52	1
74LS53	1
74LS54	1
74LS55	1
74LS56	1
74LS57	1
74LS58	1
74LS59	1
74LS60	1
74LS61	1
74LS62	1
74LS63	1
74LS64	1
74LS65	1
74LS66	1
74LS67	1
74LS68	1
74LS69	1
74LS70	1
74LS71	1
74LS72	1
74LS73	1
74LS74	1
74LS75	1
74LS76	1
74LS77	1
74LS78	1
74LS79	1
74LS80	1
74LS81	1
74LS82	1
74LS83	1
74LS84	1
74LS85	1
74LS86	1
74LS87	1
74LS88	1
74LS89	1
74LS90	1
74LS91	1
74LS92	1
74LS93	1
74LS94	1
74LS95	1
74LS96	1
74LS97	1
74LS98	1
74LS99	1
74LS100	1
74LS101	1
74LS102	1
74LS103	1
74LS104	1
74LS105	1
74LS106	1
74LS107	1
74LS108	1
74LS109	1
74LS110	1
74LS111	1
74LS112	1
74LS113	1
74LS114	1
74LS115	1
74LS116	1
74LS117	1
74LS118	1
74LS119	1
74LS120	1
74LS121	1
74LS122	1
74LS123	1
74LS124	1
74LS125	1
74LS126	1
74LS127	1
74LS128	1
74LS129	1
74LS130	1
74LS131	1
74LS132	1
74LS133	1
74LS134	1
74LS135	1
74LS136	1
74LS137	1
74LS138	1
74LS139	1
74LS140	1
74LS141	1
74LS142	1
74LS143	1
74LS144	1
74LS145	1
74LS146	1
74LS147	1
74LS148	1
74LS149	1
74LS150	1
74LS151	1
74LS152	1
74LS153	1
74LS154	1
74LS155	1
74LS156	1
74LS157	1
74LS158	1
74LS159	1
74LS160	1
74LS161	1
74LS162	1
74LS163	1
74LS164	1
74LS165	1
74LS166	1
74LS167	1
74LS168	1
74LS169	1
74LS170	1
74LS171	1
74LS172	1
74LS173	1
74LS174	1
74LS175	1
74LS176	1
74LS177	1
74LS178	1
74LS179	1
74LS180	1
74LS181	1
74LS182	1
74LS183	1
74LS184	1
74LS185	1
74LS186	1
74LS187	1
74LS188	1
74LS189	1
74LS190	1
74LS191	1
74LS192	1
74LS193	1
74LS194	1
74LS195	1
74LS196	1
74LS197	1
74LS198	1
74LS199	1
74LS200	1
74LS201	1
74LS202	1
74LS203	1
74LS204	1
74LS205	1
74LS206	1
74LS207	1
74LS208	1
74LS209	1
74LS210	1
74LS211	1
74LS212	1
74LS213	1
74LS214	1
74LS215	1
74LS216	1
74LS217	1
74LS218	1
74LS219	1
74LS220	1
74LS221	1
74LS222	1
74LS223	1
74LS224	1
74LS225	1
74LS226	1
74LS227	1
74LS228	1
74LS229	1
74LS230	1
74LS231	1
74LS232	1
74LS233	1
74LS234	1
74LS235	1
74LS236	1
74LS237	1
74LS238	1
74LS239	1
74LS240	1
74LS241	1
74LS242	1
74LS243	1
74LS244	1
74LS245	1
74LS246	1
74LS247	1
74LS248	1
74LS249	1
74LS250	1
74LS251	1
74LS252	1
74LS253	1
74LS254	1
74LS255	1
74LS256	1
74LS257	1
74LS258	1
74LS259	1
74LS260	1
74LS261	1
74LS262	1
74LS263	1
74LS264	1
74LS265	1
74LS266	1
74LS267	1
74LS268	1
74LS269	1
74LS270	1
74LS271	1
74LS272	1
74LS273	1
74LS274	1
74LS275	1
74LS276	1
74LS277	1
74LS278	1
74LS279	1
74LS280	1
74LS281	1
74LS282	1
74LS283	1
74LS284	1
74LS285	1
74LS286	1
74LS287	1
74LS288	1
74LS289	1
74LS290	1
74LS291	1
74LS292	1
74LS293	1
74LS294	1
74LS295	1
74LS296	1
74LS297	1
74LS298	1
74LS299	1
74LS300	1

Technology
4012A-02/4012P-02

SEE SHEET 1

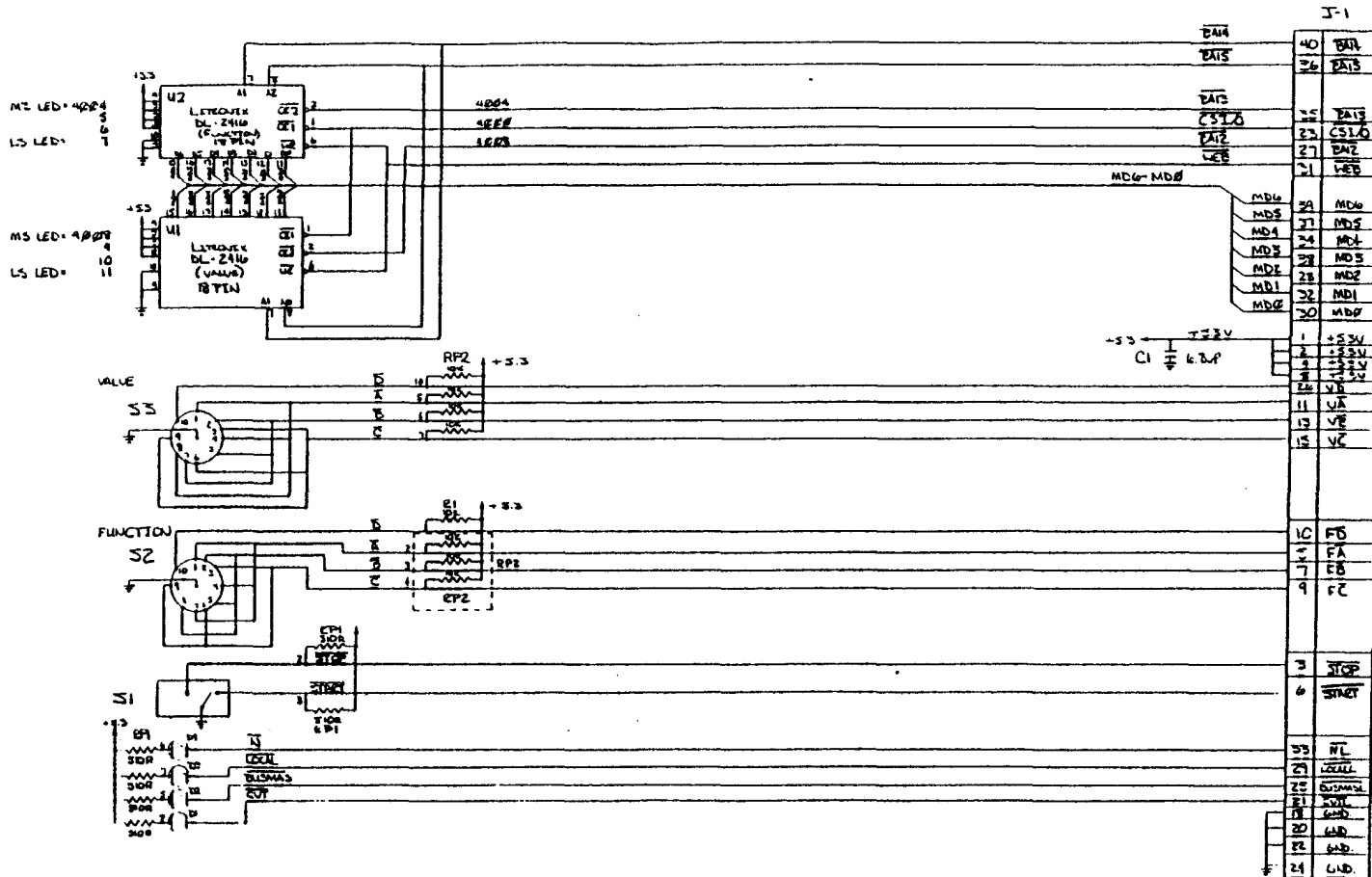
DATE	DESIGNED BY	CHECKED BY	APPROVED BY



RS 232
(NOT NORMALLY
INSTALLED)







PARTS LIST	
U1	INTEL 80286
U2	2764 EPROM
U3	2764 EPROM
U4	2764 EPROM
U5	2764 EPROM
U6	2764 SRAM
U7	2764 SRAM
U8	2764 SRAM
U9	2764 SRAM
U10	L645
U11	8255 PPI
U12	8250 UART
U13	8254
U14	374
U15	7404
U16	7404
U17	7404
U18	7404
U19	7404
U20	7404
U21	7404
U22	7404
U23	7404
U24	7404
U25	7404
U26	7404
U27	7404
U28	7404
U29	7404
U30	7404
U31	7404
U32	7404
U33	7404
U34	7404
U35	7404
U36	7404
U37	7404
U38	7404
U39	7404
U40	7404
U41	7404
U42	7404
U43	7404
U44	7404
U45	7404
U46	7404
U47	7404
U48	7404
U49	7404
U50	7404
U51	7404
U52	7404
U53	7404
U54	7404
U55	7404
U56	7404
U57	7404
U58	7404
U59	7404
U60	7404
U61	7404
U62	7404
U63	7404
U64	7404
U65	7404
U66	7404
U67	7404
U68	7404
U69	7404
U70	7404
U71	7404
U72	7404
U73	7404
U74	7404
U75	7404
U76	7404
U77	7404
U78	7404
U79	7404
U80	7404
U81	7404
U82	7404
U83	7404
U84	7404
U85	7404
U86	7404
U87	7404
U88	7404
U89	7404
U90	7404
U91	7404
U92	7404
U93	7404
U94	7404
U95	7404
U96	7404
U97	7404
U98	7404
U99	7404
U100	7404

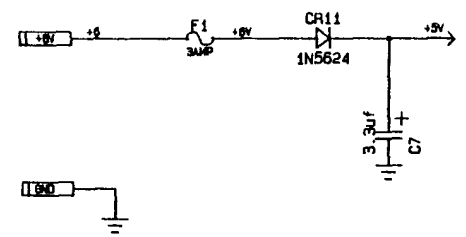
4012A-02 / 4012P-02
4012A-02-5D8



PARTS LIST		DSP Technology	
4012-03		4012-03-3D	
REV: 1.1		DATE: 10/1/88	
DRAWN: JRS		CHECKED: JRS	
APPROVED: JRS		DATE: 10/1/88	
NO COPY SHALL BE MADE		PAGE 1 OF 1	

SYMBOLS:

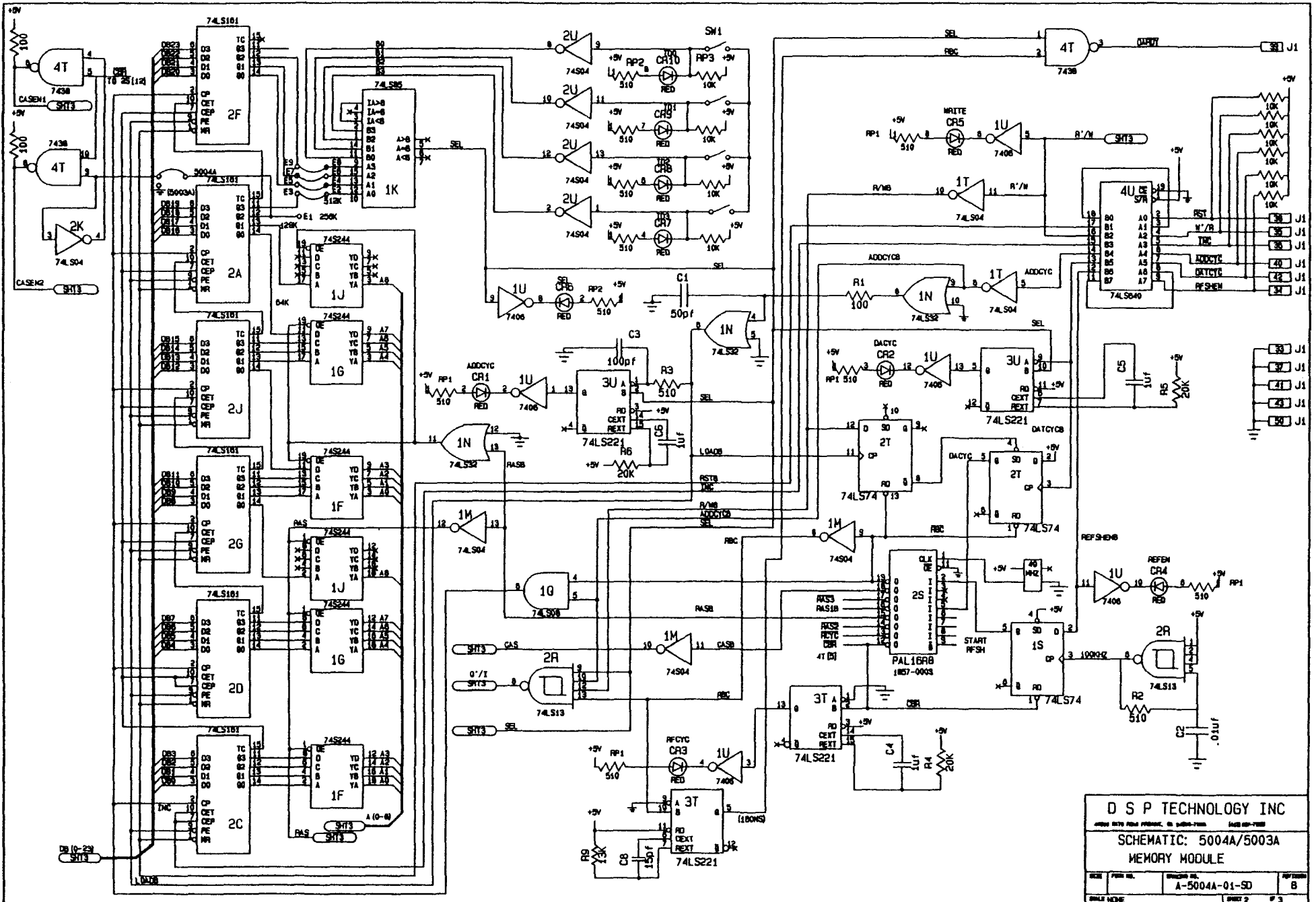
-  CAMEC EDGE CONNECTOR
-  EXTERNAL CONNECTOR
-  CONTINUE ON SAME SHEET
-  CONTINUE ON DIFFERENT SHEET
-  UNUSED PIN
-  JUMPERS
 - 5004A 5003A
 - E2 - E3 (512K) E1 - E2 (250K)
 - E4 - E5 E3 - E4
 - E6 - E7 E5 - E6
 - E8 - E9 E7 - E8
 - 4T (S) - GND



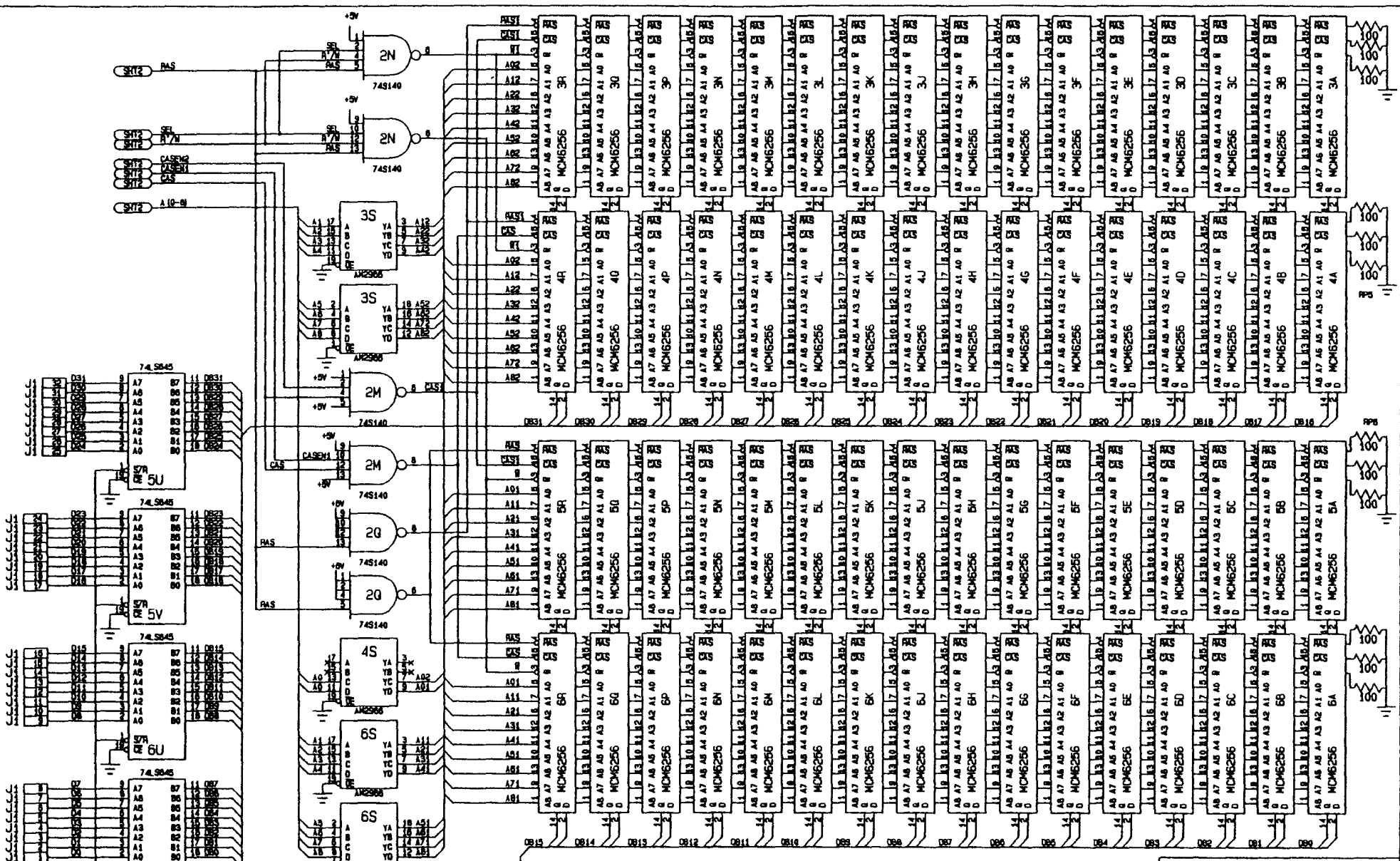
NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE IN uF.
2. ALL RESISTORS ARE 1/4W 5% AND IN OHMS.

		SIGNATURES		DATE	D S P TECHNOLOGY INC	
		DESIGNED BY		N. PERALTA	9/92	SCHEMATIC: 5004A/5003A POWER
		CHECKED BY		J. CHURCH	6/92	
		DRAWN BY				
		APPROVED BY				
		DATE				
		REV				
		DESCRIPTION				
		DATE				
		REVISITORS				
		SCALE		NONE		
		SHEET		1	OF	3

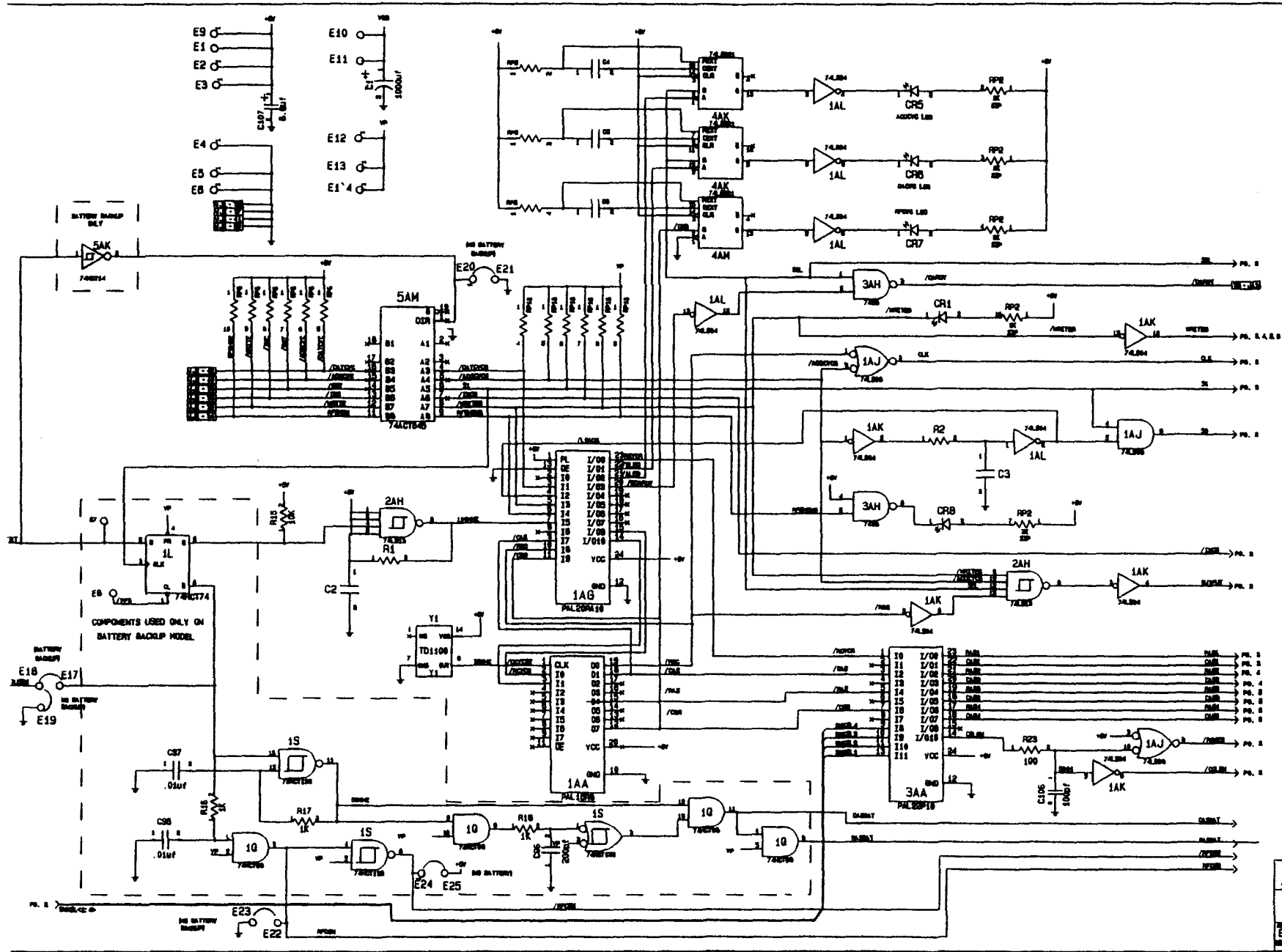


D S P TECHNOLOGY INC
 10000 10TH AVENUE, SUITE 100, DENVER, CO 80202-1000 (303) 751-1000
SCHEMATIC: 5004A/5003A
MEMORY MODULE
 SIZE: 10000 10TH AVENUE, SUITE 100, DENVER, CO 80202-1000 (303) 751-1000
 DRAWING NO. A-5004A-01-SD
 SHEET NO. 2 OF 3

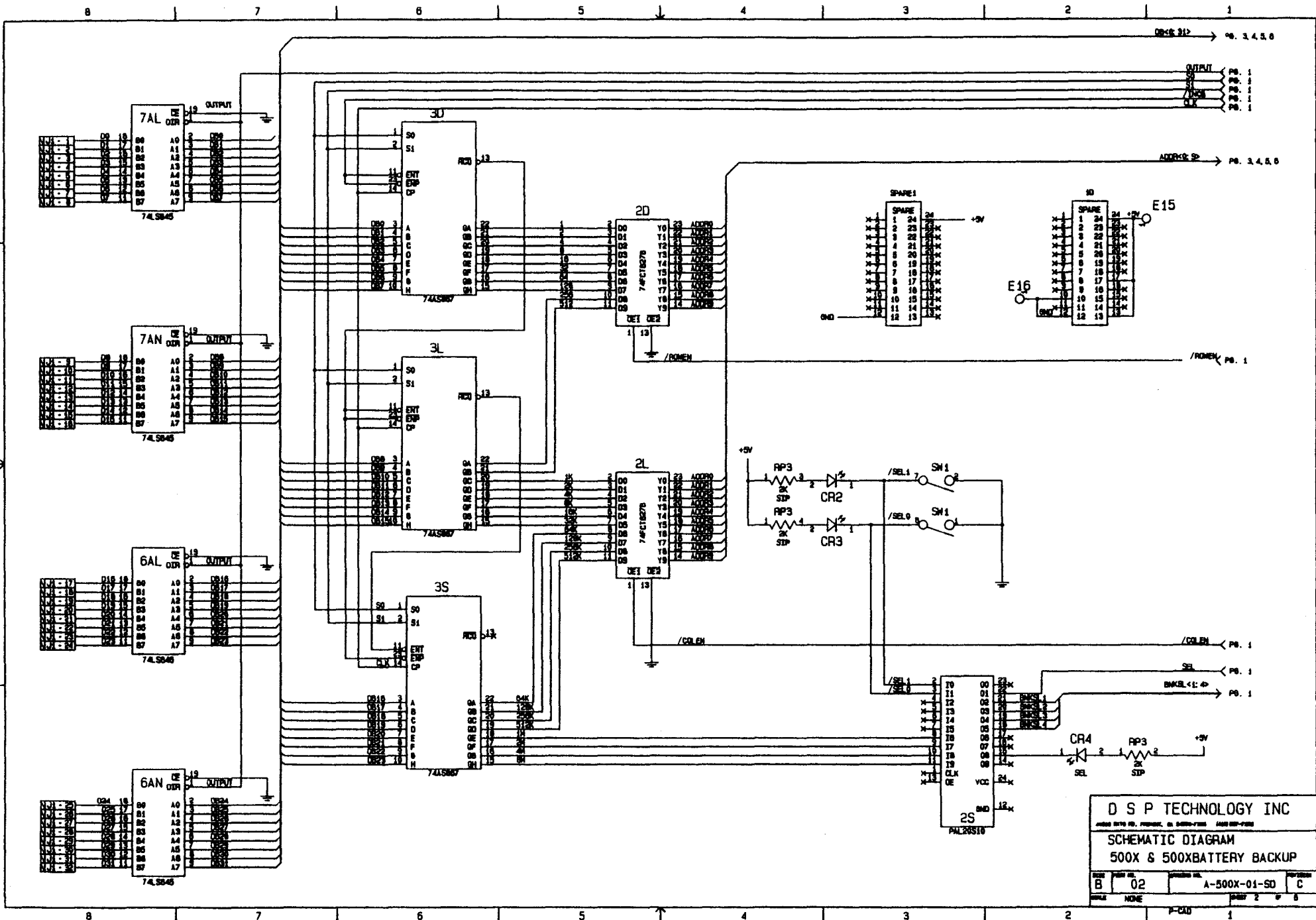


D S P TECHNOLOGY INC
 5004A / 5003A
 MEMORY MODULE

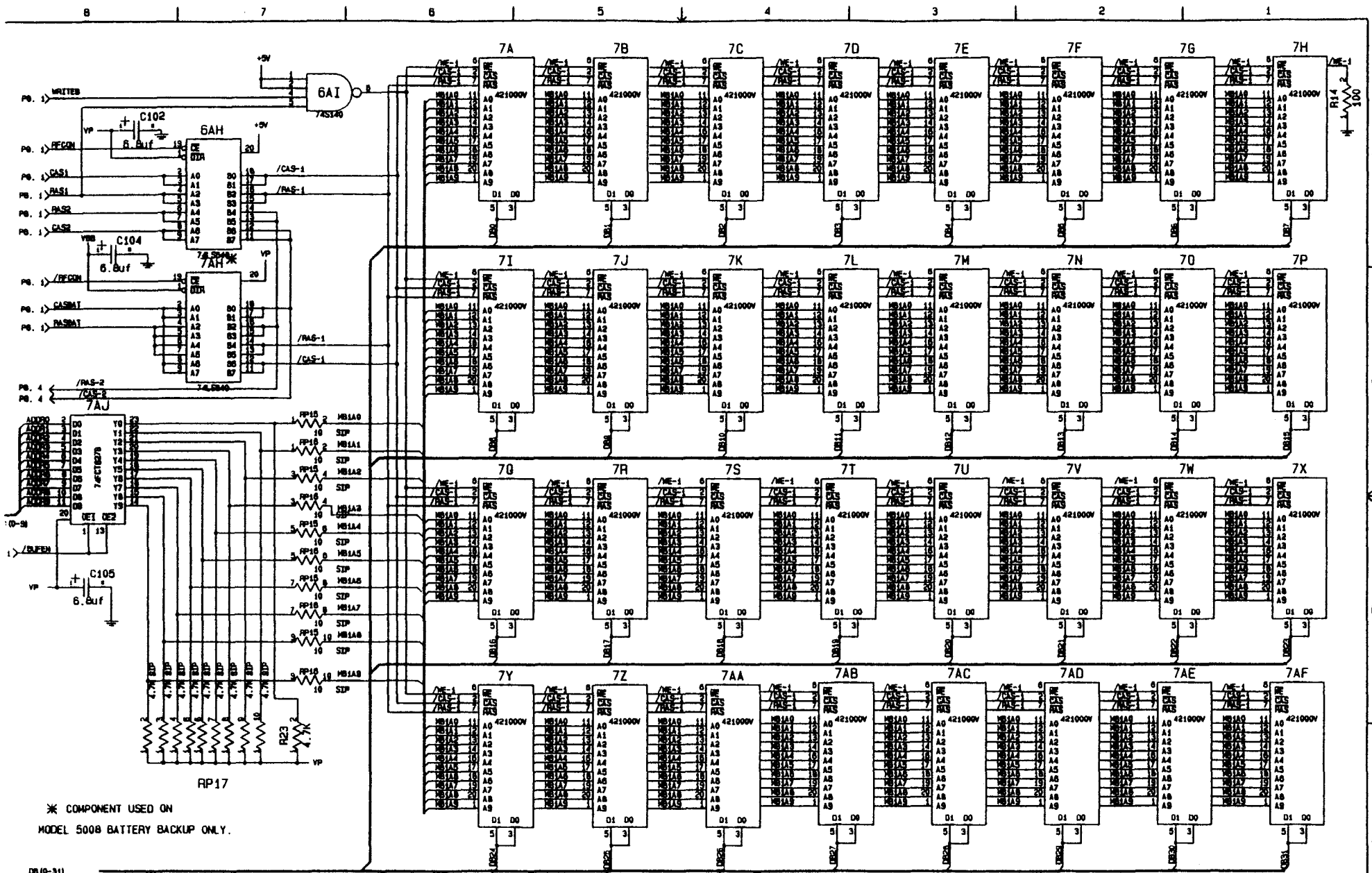
REV	FORM NO.	REVISED BY	REVISED DATE
A-5004A-01 SD		C	
PAGE 3		OF 3	



D S P TECHNOLOGY INC
 4000 W. 10th St., Suite 100
 Denver, CO 80202
 DSP TECHNOLOGY
 SCHEMATIC 5008-01
 MEMORY MODULE
 A-5008-01-50
 1-508



D S P TECHNOLOGY INC
PHONE 800-765-7766, FAX 800-765-7766, 4400 10TH AVENUE, DENVER, CO 80202
SCHEMATIC DIAGRAM
500X & 500XBATTERY BACKUP
 PART NO. 02 REVISED NO. A-500X-01-S0 SHEET NO. C
 SCALE NONE PAGE 2 OF 5



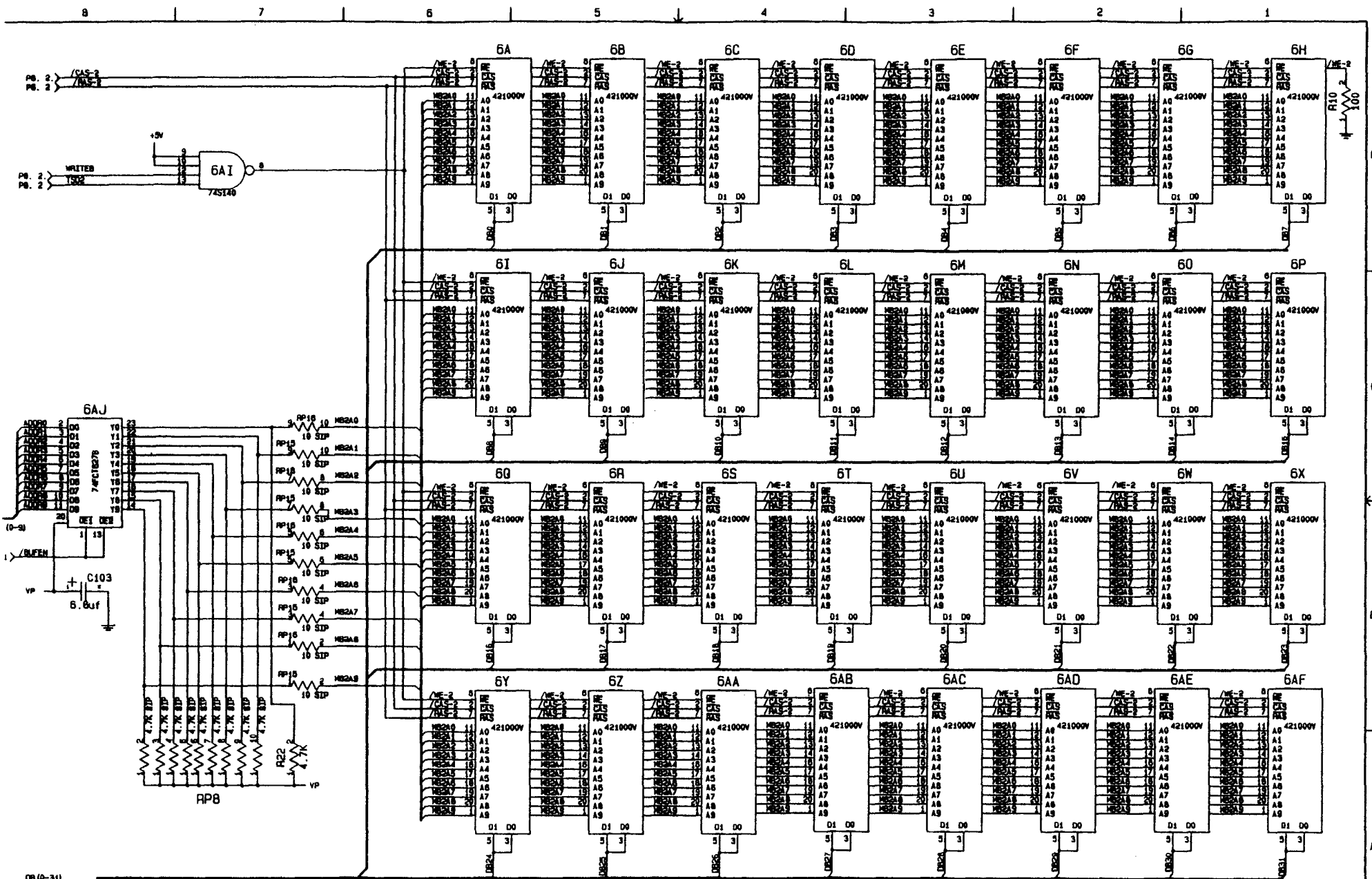
* COMPONENT USED ON
MODEL 5008 BATTERY BACKUP ONLY.

DS 10-311

MEMORY BLOCK 1

USED ON MODELS: 5005 5005BB
5006 5006BB
5007 5007BB
5008 5008BB

D S P TECHNOLOGY INC			
MEMORY BLOCK 1		5008-01	
REV B	DATE 5/88	ISSUE NO. A-500X-01-SD	DESIGNER C
APPROVED		DATE	BY

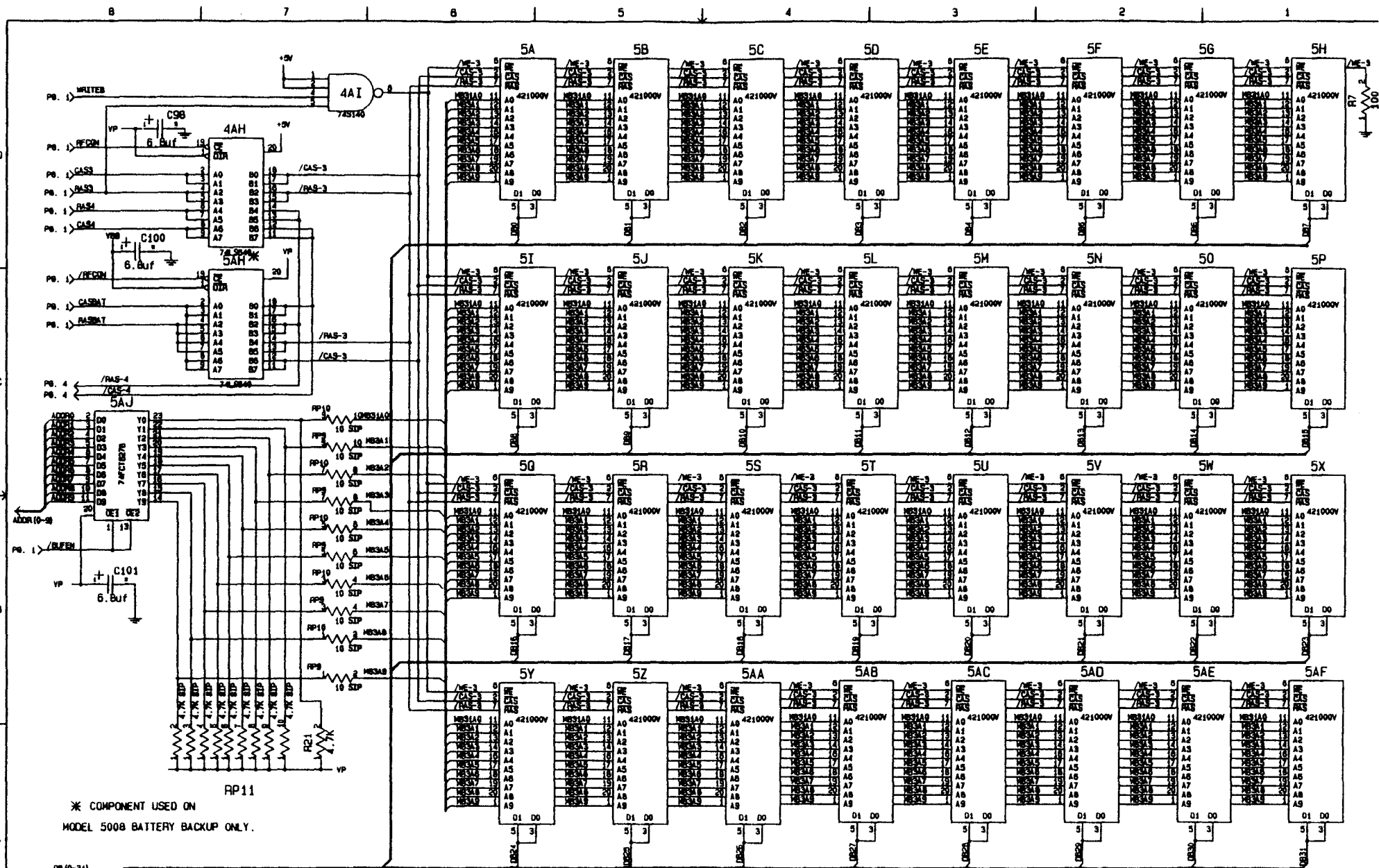


MEMORY BLOCK 2

USED ON MODELS: 5006 5006BB
5007 5007BB
5008 5008BB

D S P TECHNOLOGY INC			
MEMORY BLOCK 2: 5008-01			
REV	DATE	ISSUED BY	DESIGNED BY
B	5/88	A-500X-01-SD	C
DATE	REV	ISSUED BY	DESIGNED BY
NONE			

08 (0-31)



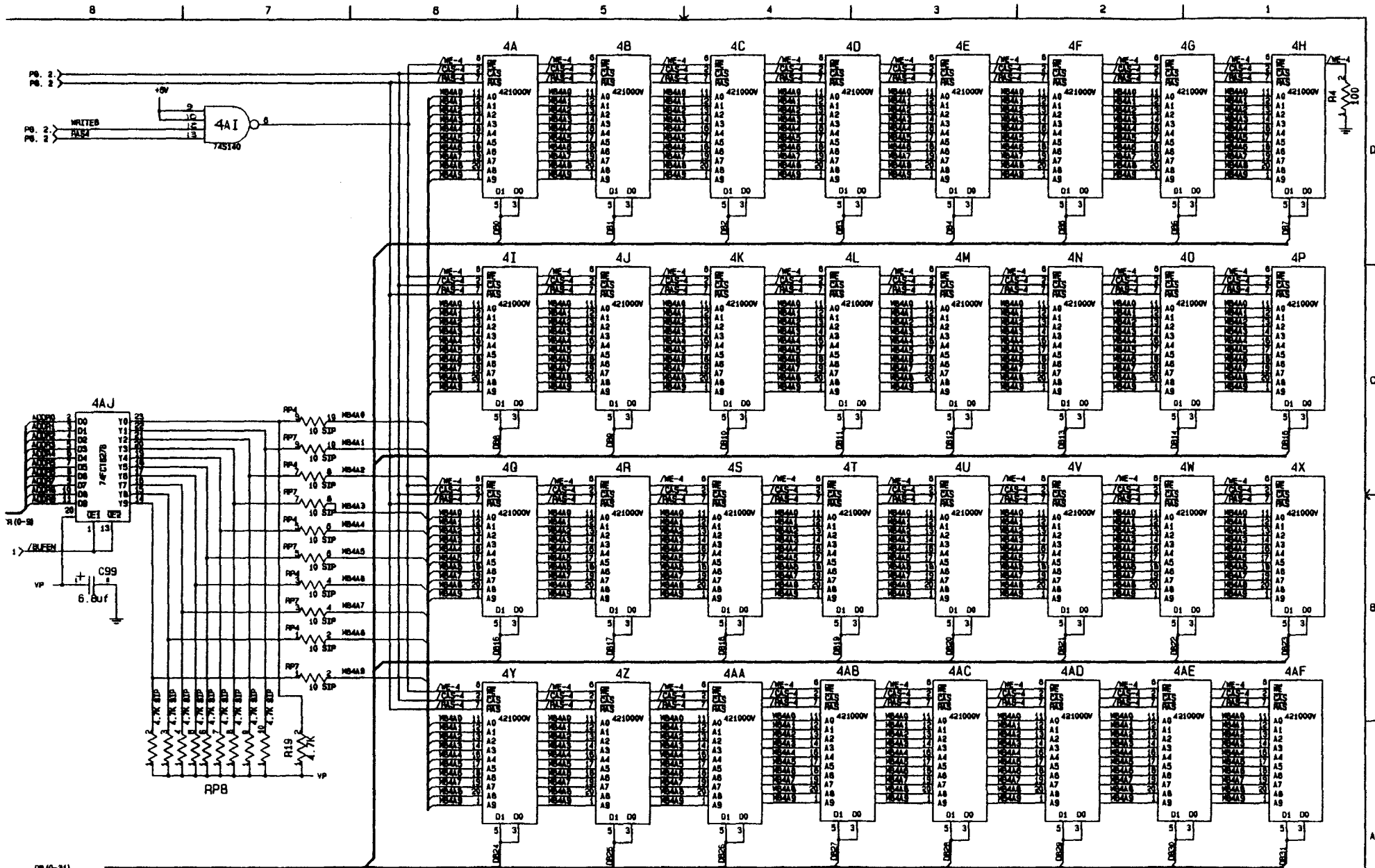
* COMPONENT USED ON
MODEL 500B BATTERY BACKUP ONLY.

DB (0-31)

MEMORY BLOCK 3

USED ON MODELS: 5007 5007BB
5008 5008BB

D S P TECHNOLOGY INC			
MEMORY BLOCK 3: 500B-01			
REV B	DATE 1/78	DESIGNER A-500X-01-SD	DRWG NO. U
SCALE NONE	SHEET 5	P-CAD	









MEMORY BLOCK 4

USED ON MODELS: 500B & 500BB

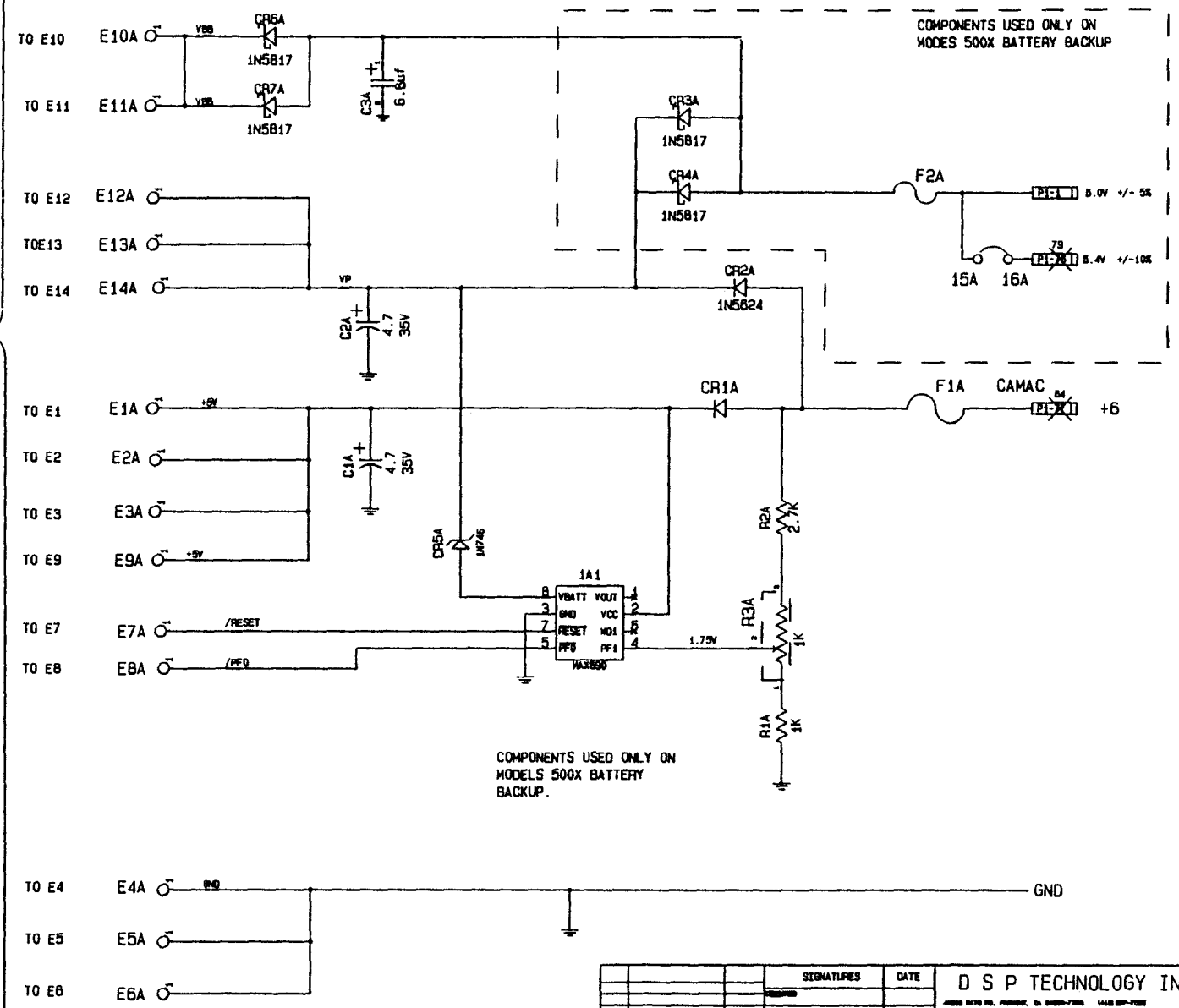
D S P TECHNOLOGY INC			
MEMORY BLOCK 4: 500B-01			
REV. B	DATE 5/88	PART NO. A-500X-01-SD	REV. C
SCALE NONE	PAGE 6	OF 6	

DB (0-31)

SYMBOLS:

-  CAMAC EDGE CONNECTOR
-  EXTERNAL CONNECTOR
-  CONT'D ON SAME SHEET
-  CONT'D ON DIFFERENT SHEET
-  UNUSED PIN
-  JUMPERS

22 AWG JUMPER
TO 5008-01 PCB









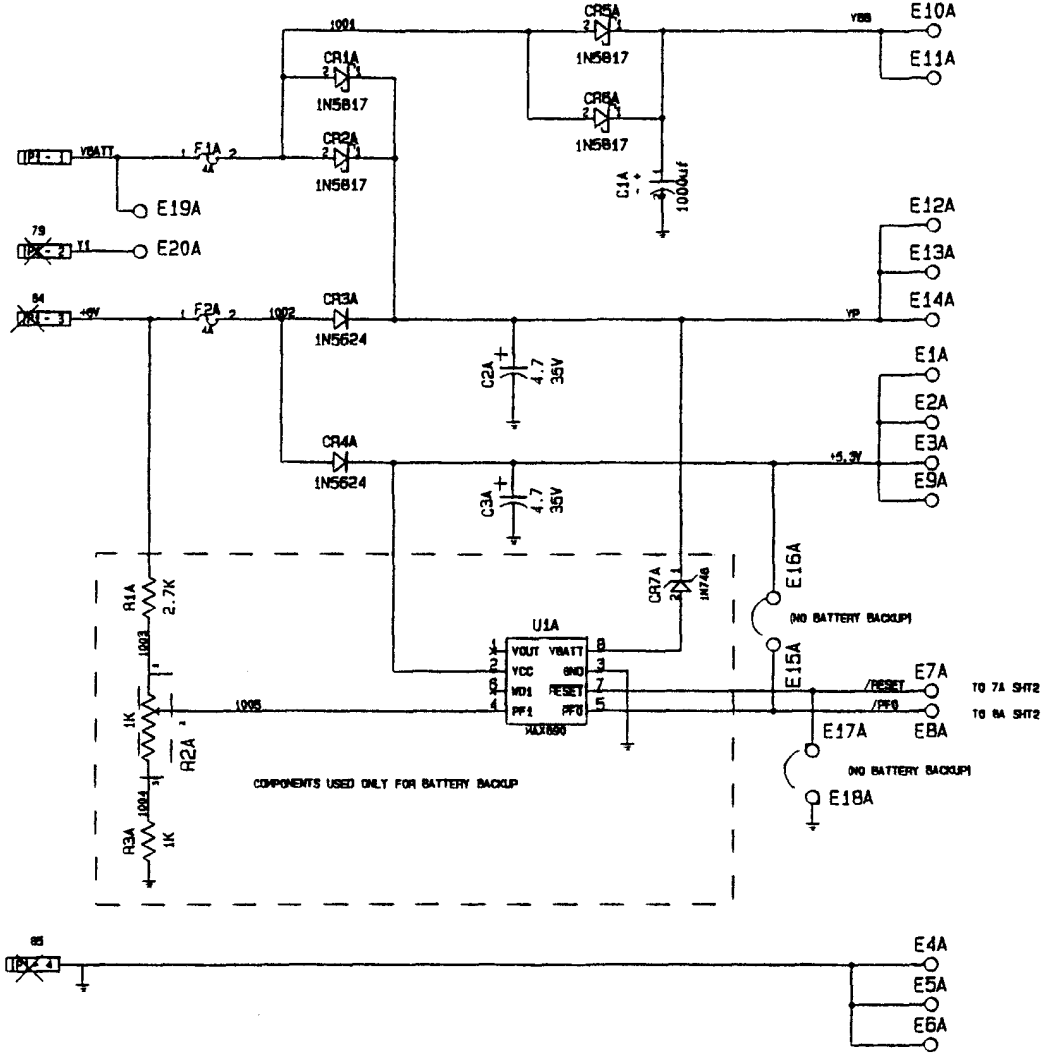
NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE IN μ F.
2. ALL RESISTORS ARE 1/4W OR AND IN OHMS.

SIGNATURES		DATE	D S P TECHNOLOGY INC 4000 BAYVIEW RD., FARMINGDALE, NY 11735-1000 (516) 339-7000
DESIGNED		5/89	
CHECKED		1/89	SCHEMATIC 500X-02 MEMORY MODULE
APPROVED			REV B PART NO. A-500X-02-SD
REV DESCRIPTION DATE			PRICE NONE SHEET 1 OF 1
REVISIONS			P-CAD 1

SYMBOLS:

-  CAMEC EDGE CONNECTOR
-  EXTERNAL CONNECTOR
-  CONTINUE ON SAME SHEET
-  CONTINUE ON DIFFERENT SHEET
-  UNUSED PIN
-  JUMPERS



COMPONENTS USED ONLY FOR BATTERY BACKUP

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE IN UF.
2. ALL RESISTORS ARE 1/4W 5% AND IN OHMS.

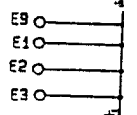
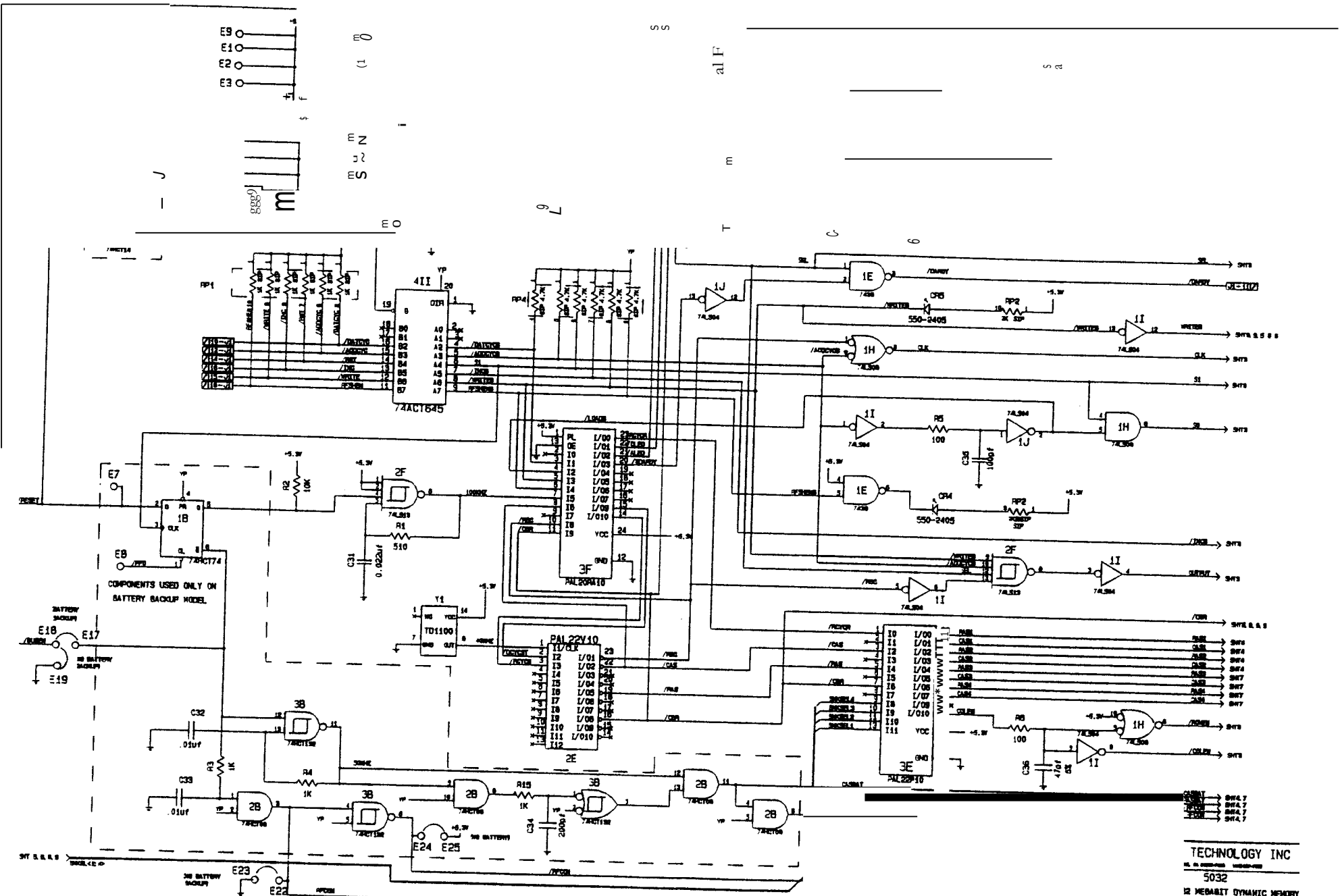
SIGNATURES		DATE	D S P TECHNOLOGY INC 32 MEGABIT DYNAMIC MEMORY POWER SUPPLY/BATTERY BACKUP
J. CHURCH		8/18/92	
SIGNATURES		DATE	5032 32 MEGABIT DYNAMIC MEMORY POWER SUPPLY/BATTERY BACKUP
NVT		6/29/93	
REV	DESCRIPTION	DATE	REV
1	PRODUCTION RELEASE	7/18/92	B
REVISIONS			SCALE NONE

B 7 6 5 4 3 2 1

B 7 6 5 4 3 2 1

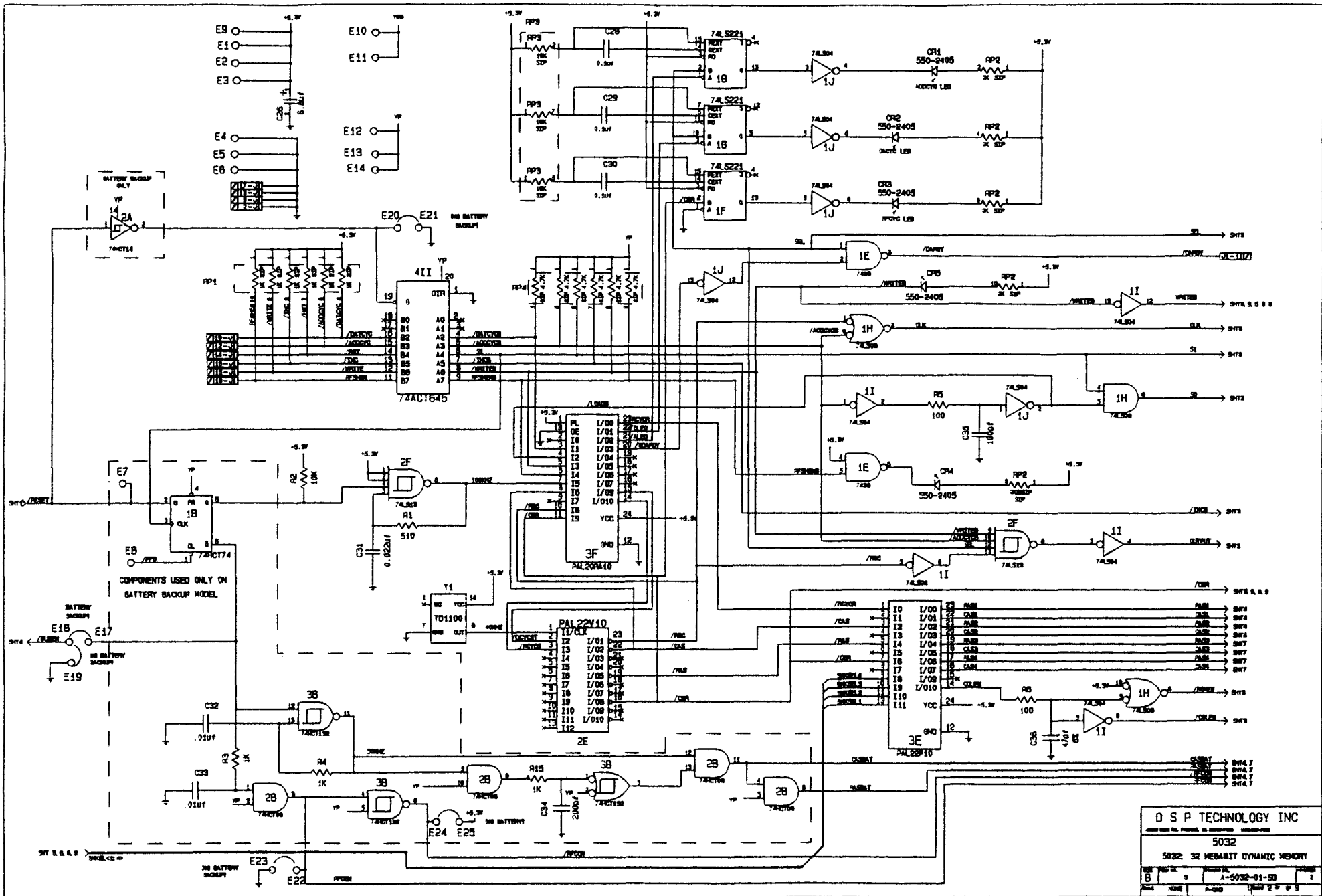
D
C
B
A

P-CAD 1

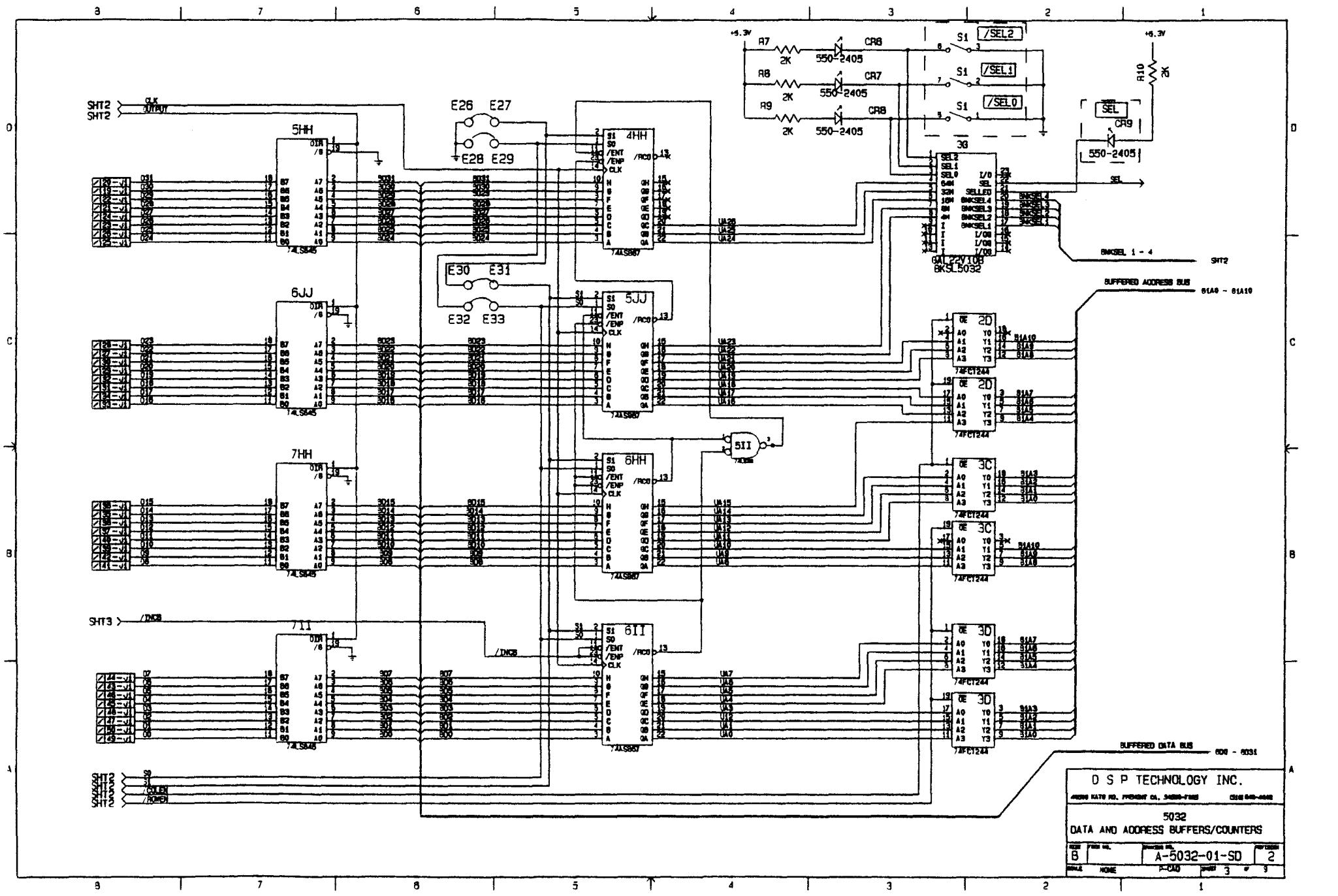


ES
E2
E1
E0

TECHNOLOGY INC
15 N. GARDEN ST. (301) 251-1000
5032
12 MEGABIT DYNAMIC MEMORY



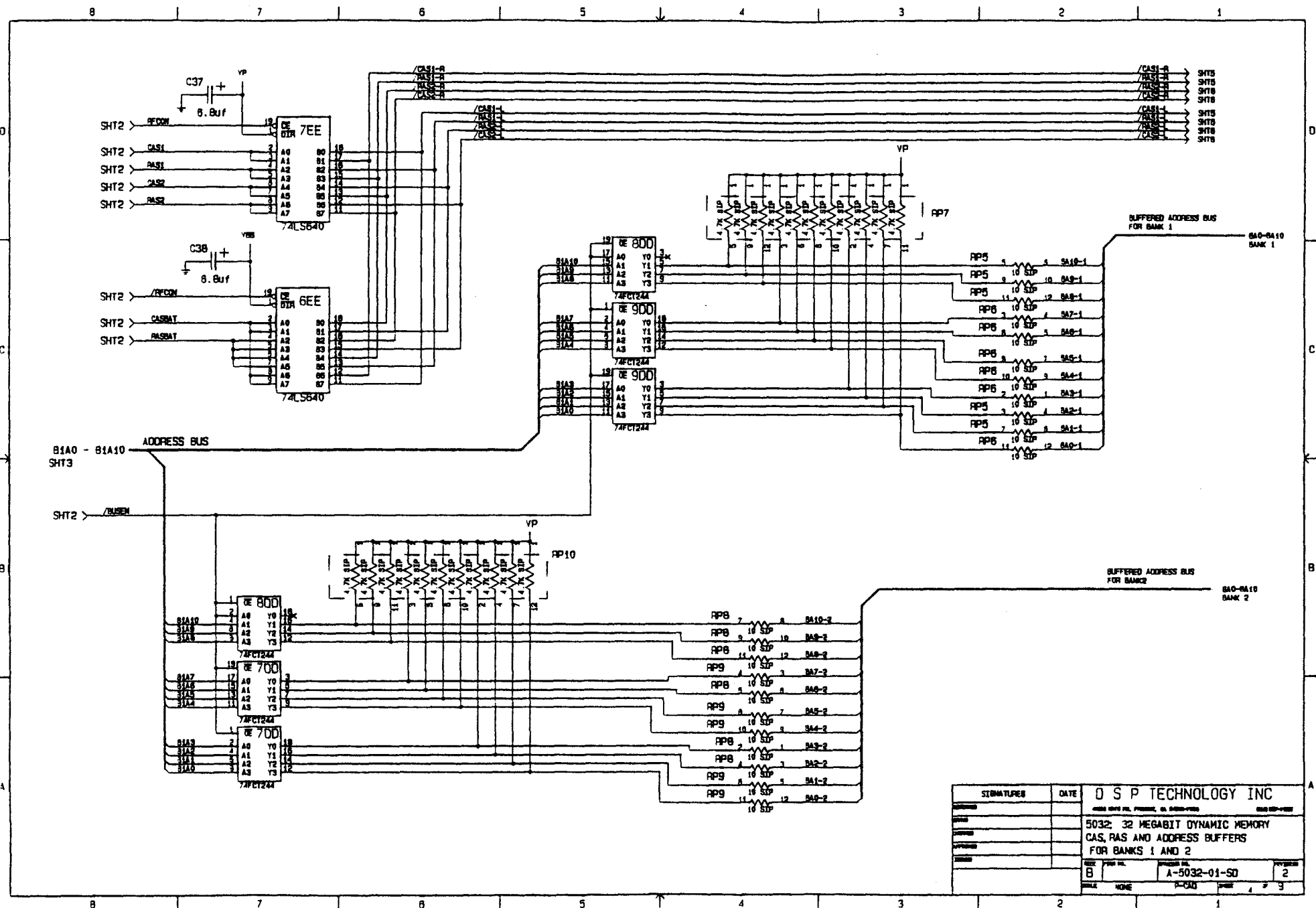
D S P TECHNOLOGY INC
 5032
 5032: 32 MEGABIT DYNAMIC MEMORY
 8 1 0 1 A-5032-01-50
 DATE NONE P-000 1987 2 F 9 9



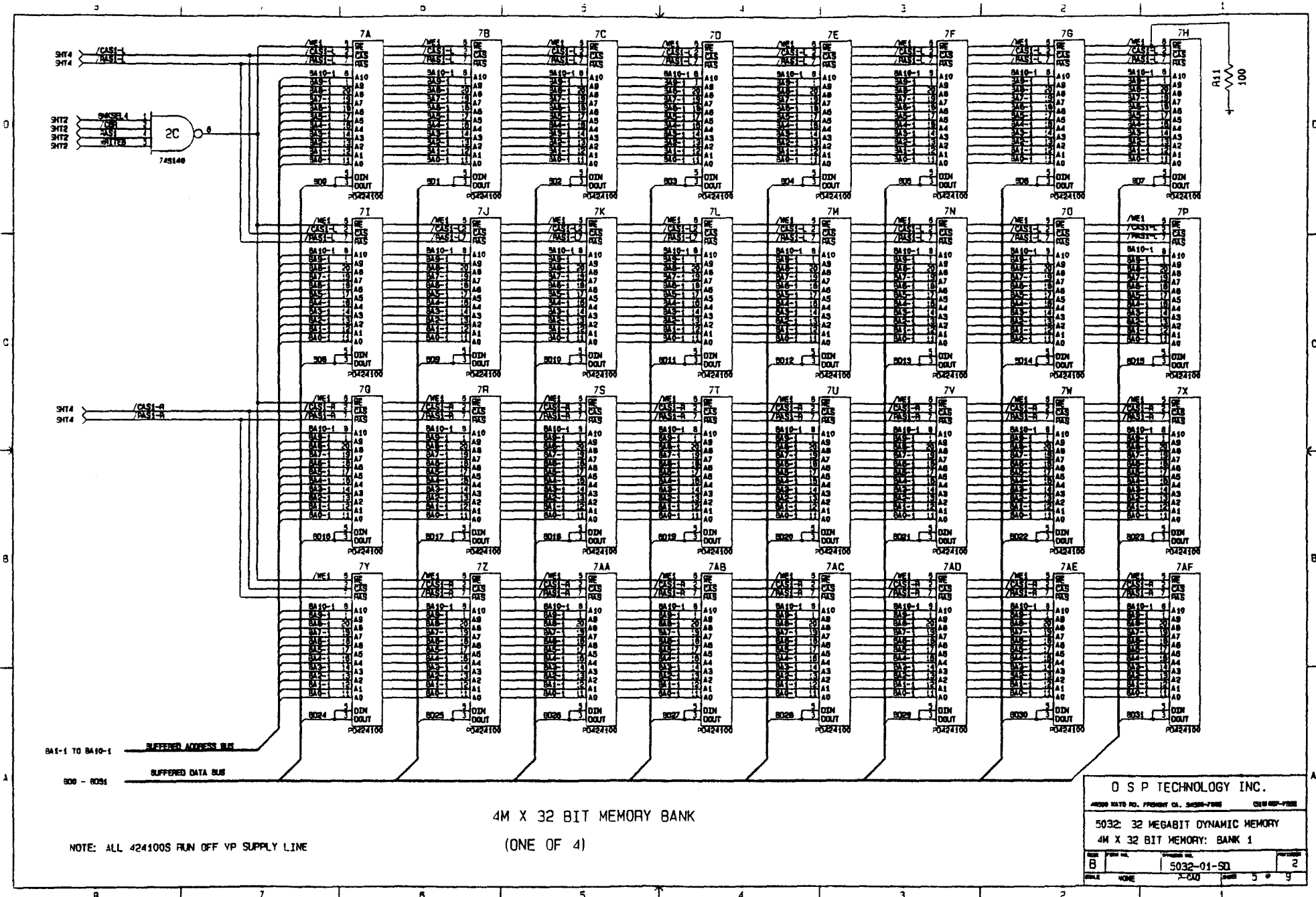
D S P TECHNOLOGY INC.
 4000 KATO RD. FRENCH CR., 34000-7100 214-640-0000

5032
 DATA AND ADDRESS BUFFERS/COUNTERS

REV	DATE	ISSUED BY	PER. CHECKED
B		A-5032-01-SD	2
SCALE	NONE	P-CAD	3 3



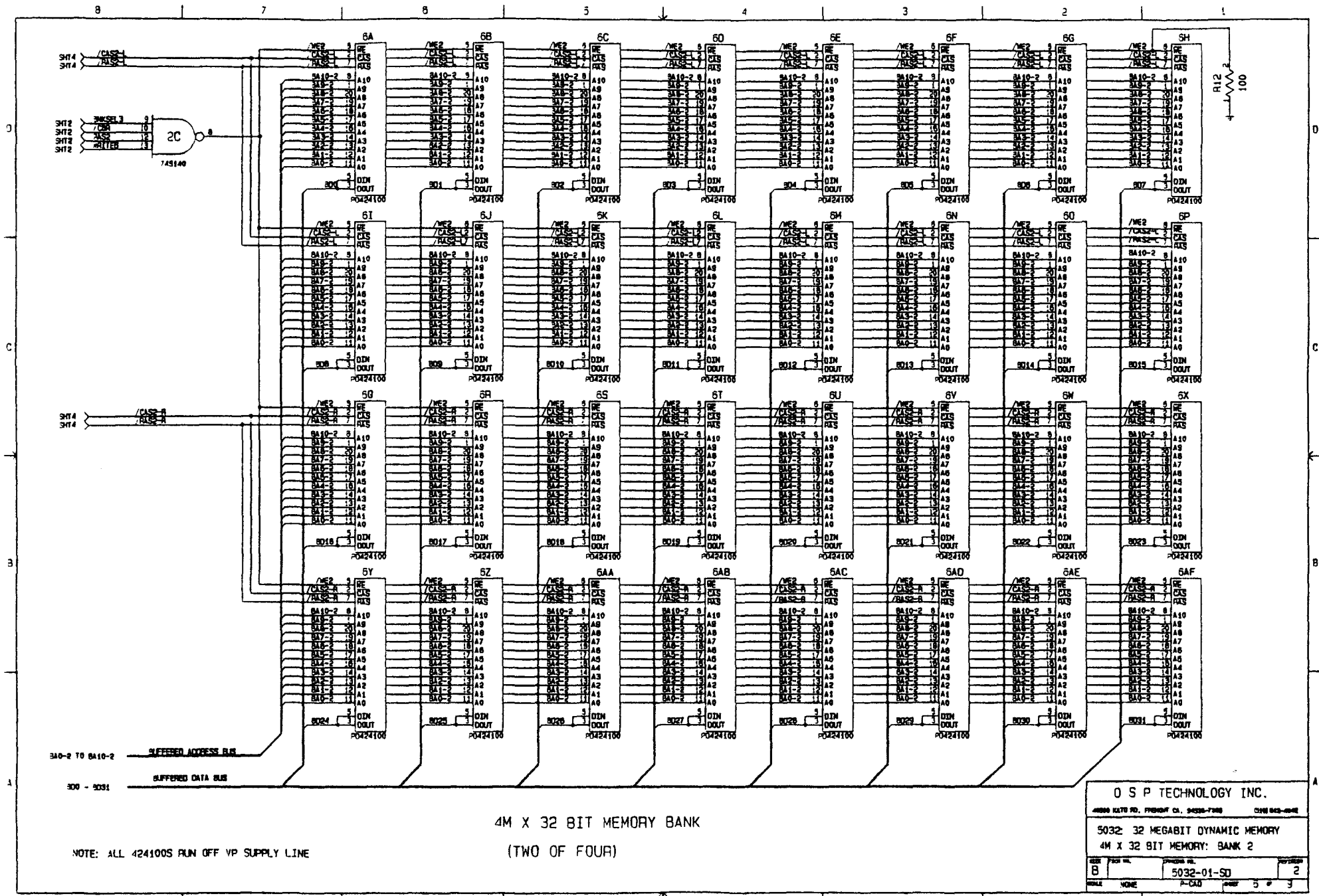
SIGNATURES		DATE	D S P TECHNOLOGY INC	
DESIGNED			5032 32 MEGABIT DYNAMIC MEMORY	
CHECKED			CAS, RAS AND ADDRESS BUFFERS	
APPROVED			FOR BANKS 1 AND 2	
REV.	1	DATE	REV. NO.	REV. NO.
B			A-5032-01-S0	2
SCALE	NONE		P-CAD	4 3



4M X 32 BIT MEMORY BANK
(ONE OF 4)

NOTE: ALL 424100S RUN OFF VP SUPPLY LINE

D S P TECHNOLOGY INC.			
4800 HATO RD., FRENCH C., SHERBORN MASS 01867-0001			
5032: 32 MEGABIT DYNAMIC MEMORY			
4M X 32 BIT MEMORY: BANK 1			
REV	PART NO.	FRONT PANEL	PAGE NO.
B	5032-01-S0		2
SCALE	NONE	1-DWG	SHEET 5 OF 9



4M X 32 BIT MEMORY BANK
(TWO OF FOUR)

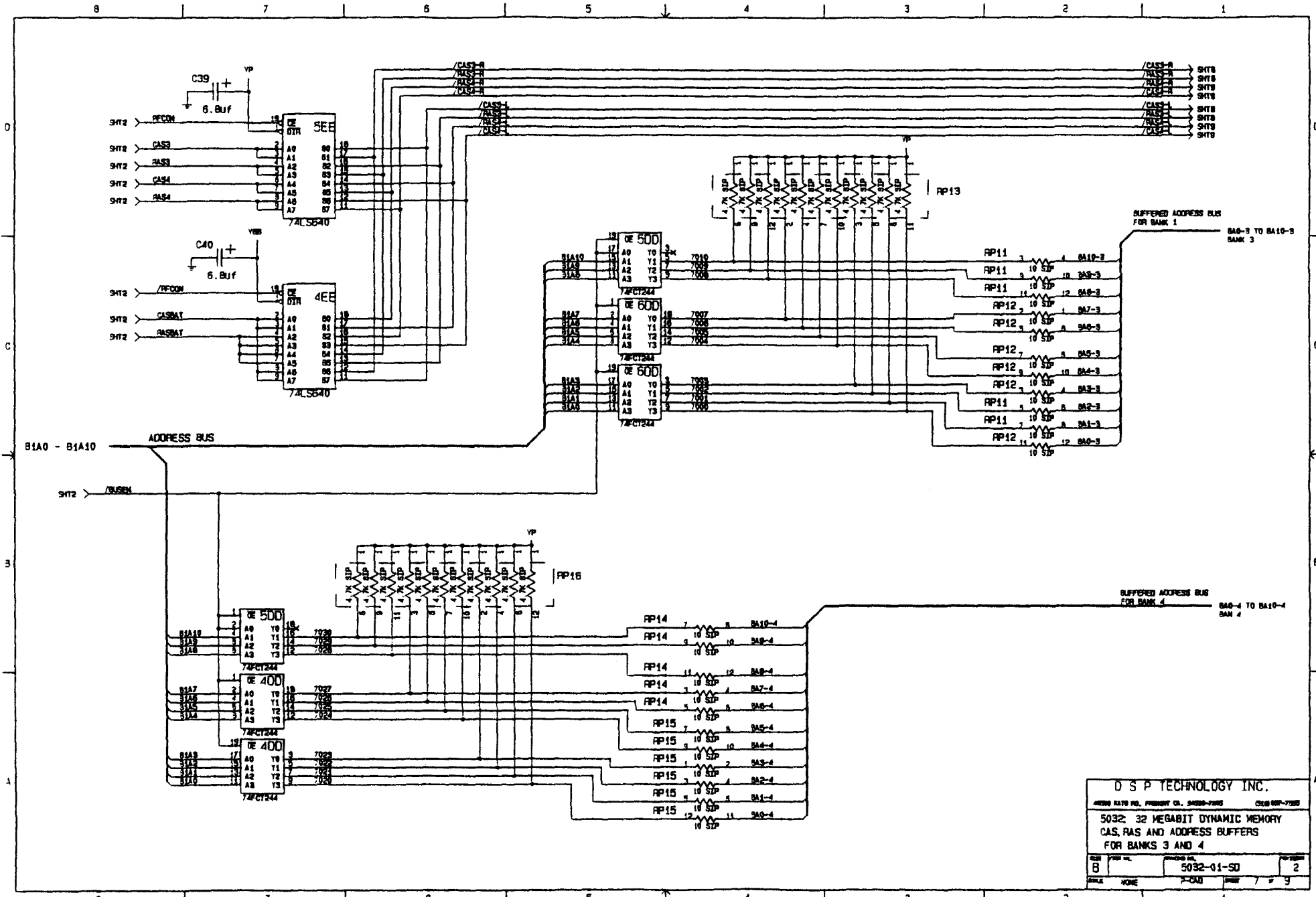
NOTE: ALL 424100S RUN OFF VP SUPPLY LINE

O S P TECHNOLOGY INC.
4000 KATO RD. FRENCH CR. 94303-7200 (415) 843-0900

5032: 32 MEGABIT DYNAMIC MEMORY
4M X 32 BIT MEMORY: BANK 2

REV	DATE	DESIGNED BY	DATE	REV
B				2

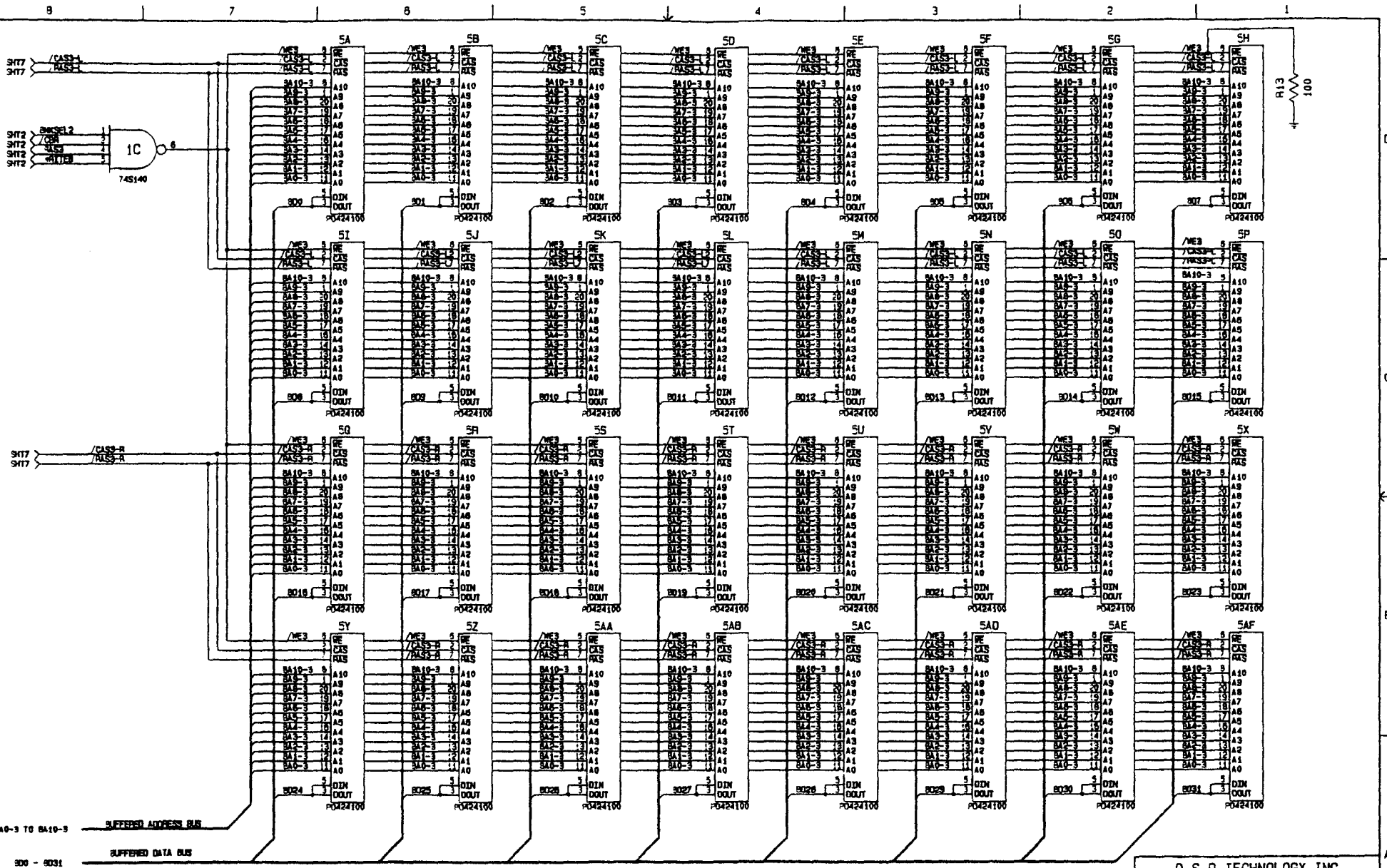
5032-01-SD



D S P TECHNOLOGY INC.
 4020 BALBO RD. FORTWORTH, TX 76104-7105 CLOSING 1995

5032: 32 MEGABIT DYNAMIC MEMORY
 CAS, RAS AND ADDRESS BUFFERS
 FOR BANKS 3 AND 4

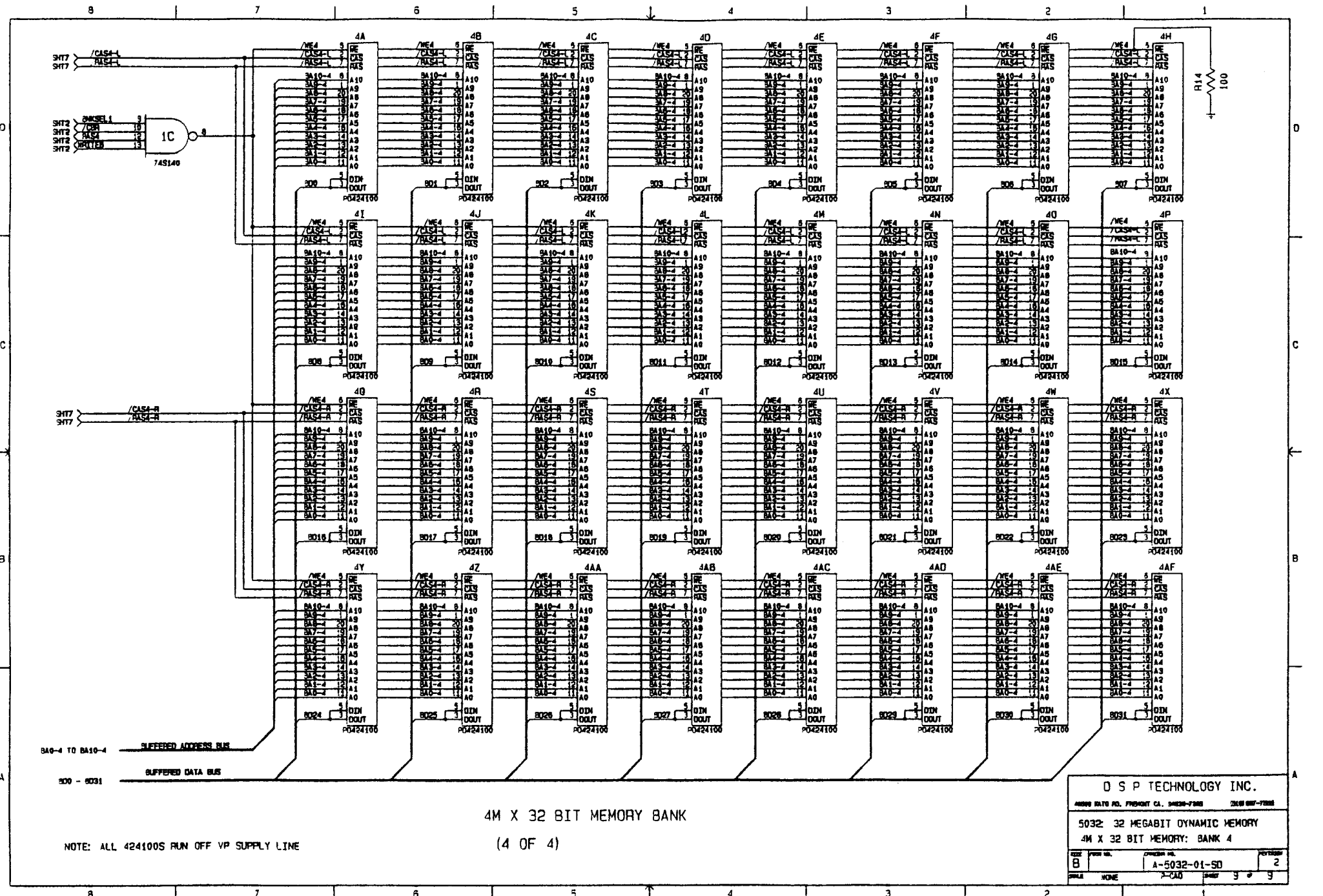
REV: B	DATE: 7-94	REVISED BY: 5032-01-S0	REVISED DATE: 7-94
DRAWN BY: NONE		SHEET 7 OF 9	



4M X 32 BIT MEMORY BANK
(3 OF 4)

NOTE: ALL 424100S RUN OFF VP SUPPLY LINE

D O S P TECHNOLOGY INC.
 4220 KATE RD., FREDERICK CO., SALES-7388 (301) 667-7388
 5032: 32 MEGABIT DYNAMIC MEMORY
 4M X 32 BIT MEMORY: BANK 3
 REV. B PART NO. 5032-01-50 PAGE 2
 SCALE NONE P-CAD PRINT 8 9



4M X 32 BIT MEMORY BANK
(4 OF 4)

NOTE: ALL 4241100S RUN OFF VP SUPPLY LINE







D O S P TECHNOLOGY INC.

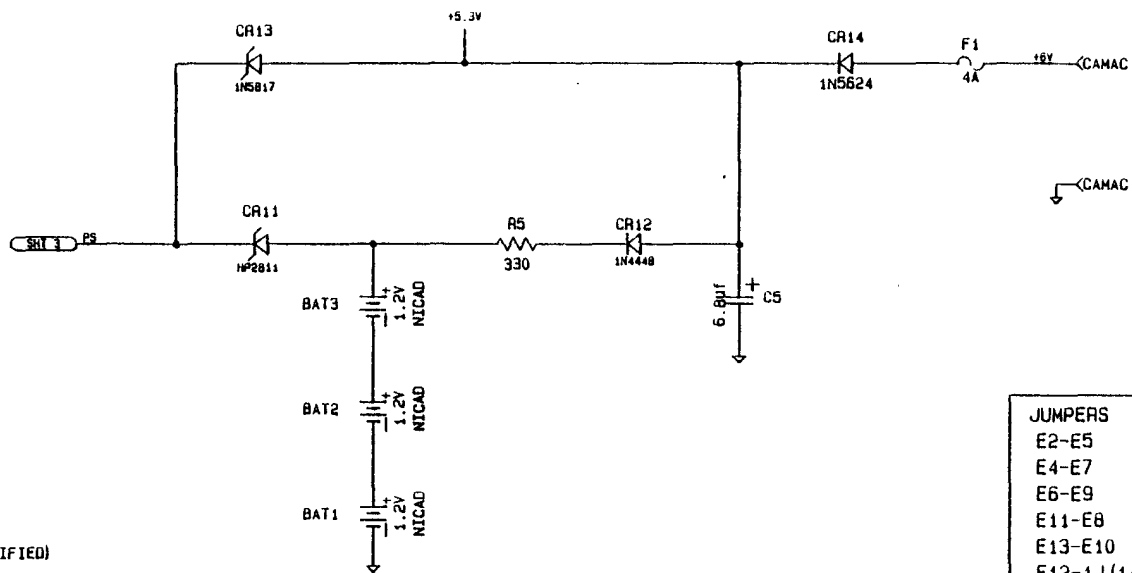
8000 BALTO RD, FREDRICK CT, DRESDEN, MD 21030-7500 (301) 887-7500

5032: 32 MEGABIT DYNAMIC MEMORY
4M X 32 BIT MEMORY: BANK 4

REV. NO.	DESIGN NO.	REV. NO.	REV. NO.
B		A-5032-01-S0	2
DATE	HOME	7-040	9 9 9

SYMBOLS.

-  CAMAC EDGE CONNECTOR
-  EXTERNAL CONNECTOR
-  CONTINUE ON SAME SHEET
-  CONTINUE ON DIFFERENT SHEET
-  UNUSED PIN
-  JUMPERS

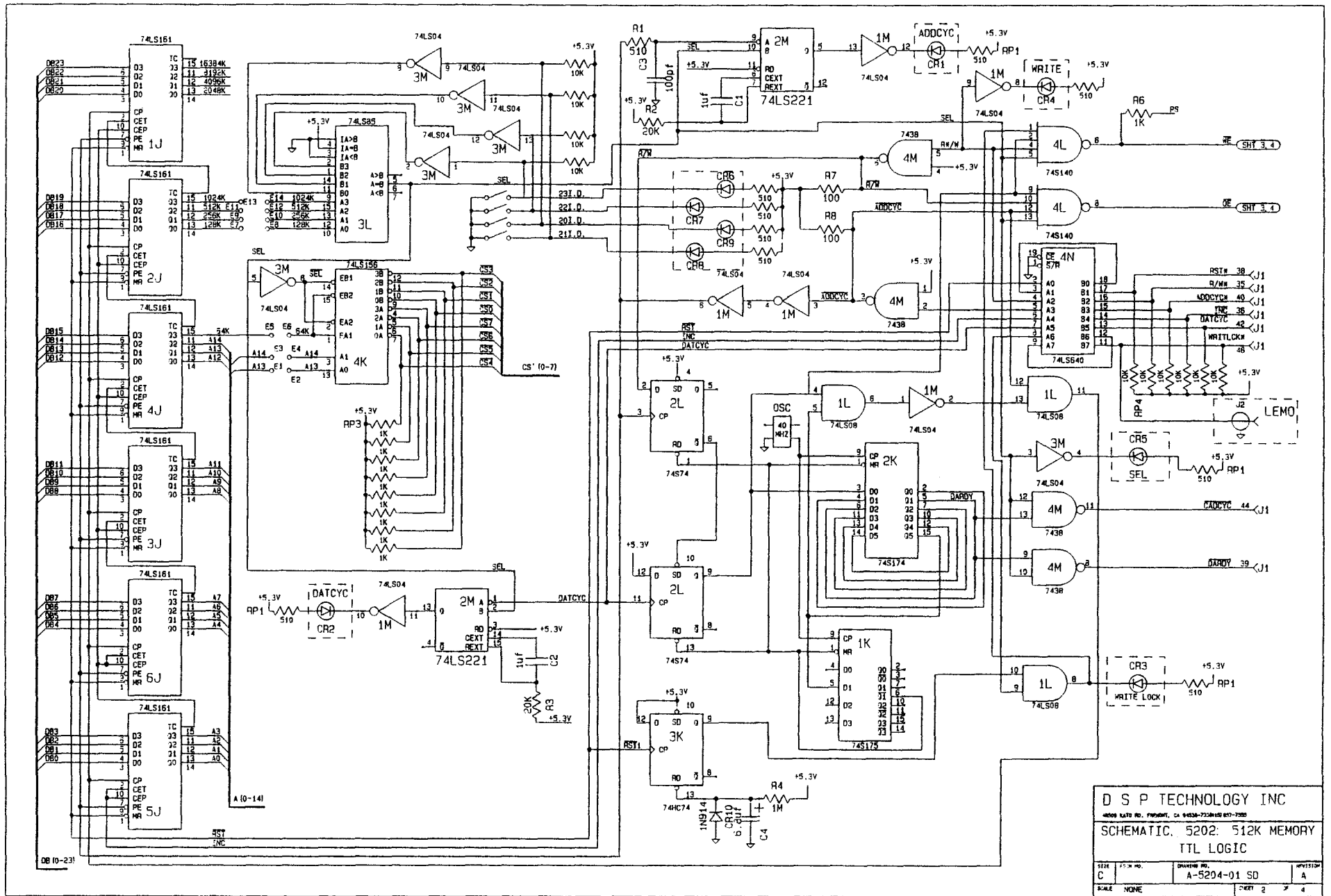


JUMPERS
 E2-E5
 E4-E7
 E6-E9
 E11-E8
 E13-E10
 E12-1J (14)
 E14-1J (13)

NOTES. (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE IN µF.
2. ALL RESISTORS ARE IN OHMS.

		SIGNATURES		DATE	D S P TECHNOLOGY INC	
		DESIGNED			4000 LOTS NO. 7000000 24 84200 7224 143 007-1000	
		DRAWN		N. PERALTA	SCHEMATIC, 5204: 512K MEMORY POWER SUPPLY	
		CHECKED				
		APPROVED			SIZE	11
		ISSUED			QUANTITY	1-5204-01 SD
PROOF RELEASE	REV	DESCRIPTION	DATE			REVISION
						A
REVISIONS				SCALE	NONE	
				SHEET	1 of 1	

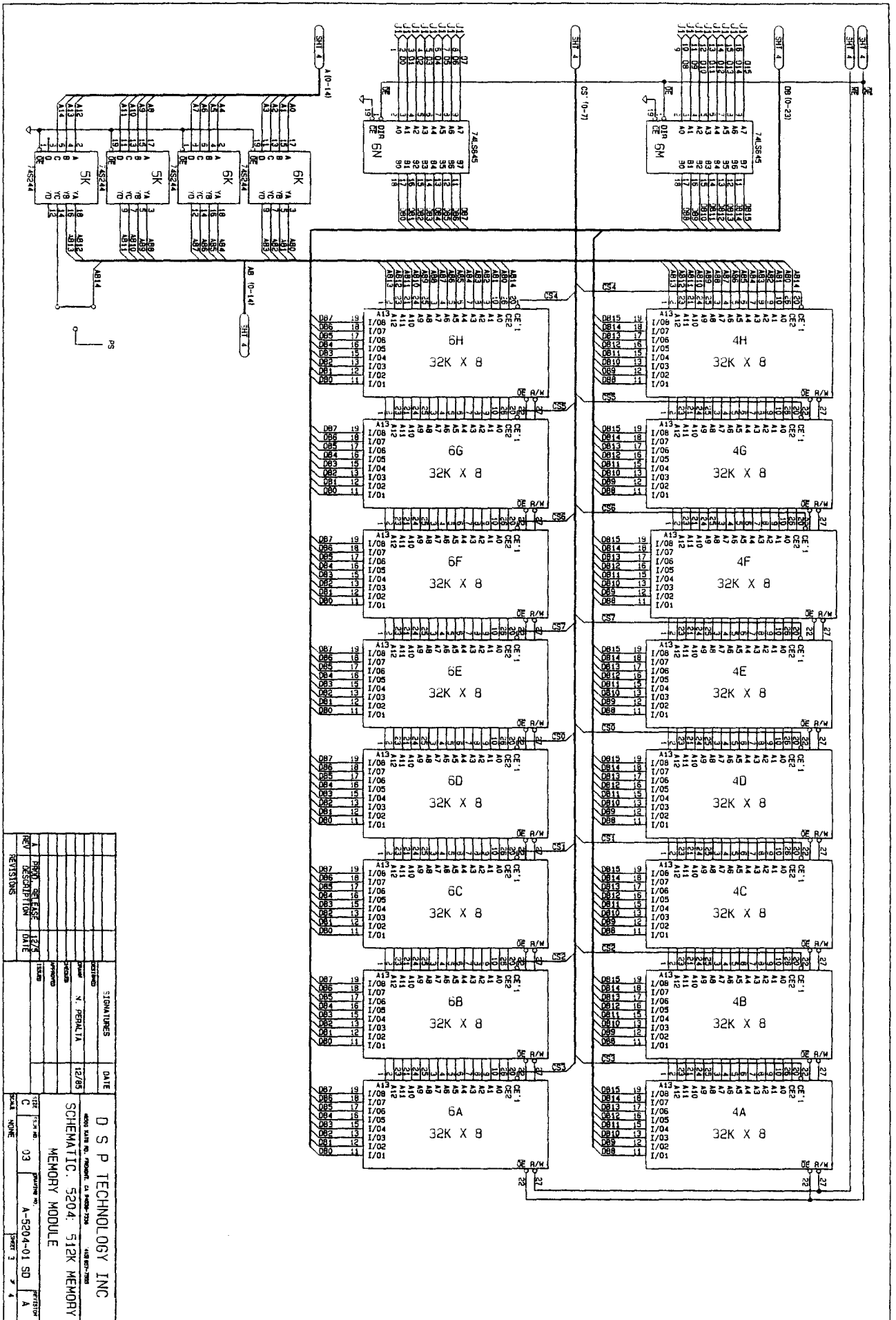


D S P TECHNOLOGY INC

4609 RATO RD., FURNERT, CA 94538-7530/US 617-7530

SCHEMATIC. 5202: 512K MEMORY
TTL LOGIC

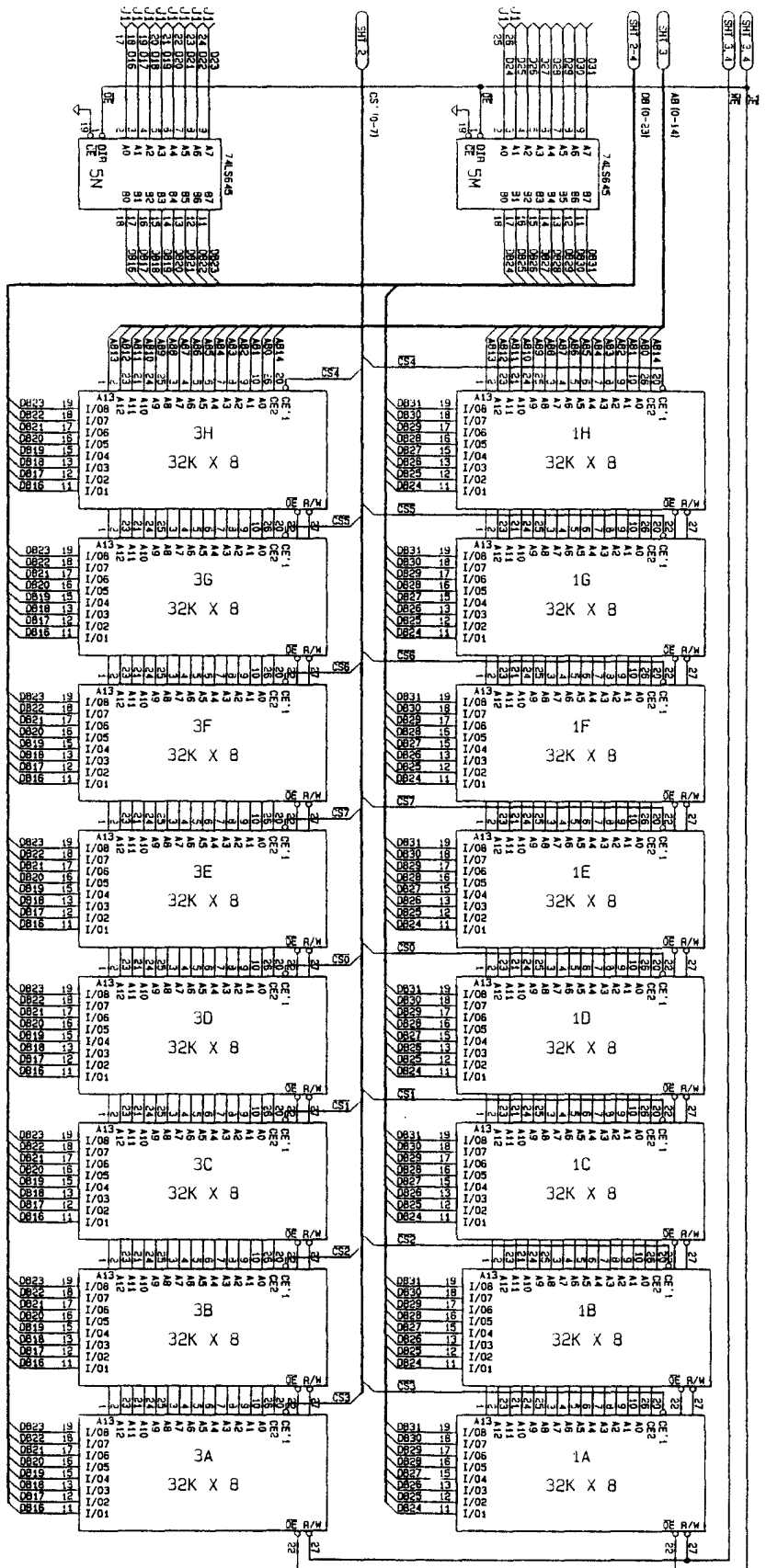
SIZE C	PAGE NO. 1	DRAWING NO. A-5204-01 SD	REVISED A
SCALE NONE		SHEET 2	OF 4



REV	DESCRIPTION	DATE	DESIGNER	DATE
1	REVISED	12/88		

SIGNALS	DATE
CS	12/88
DB	
DE	
R/W	

D S P TECHNOLOGY INC	
SCHEMATIC: 5204: 512K MEMORY	
MEMORY MODULE	
REV: 03	DATE: 12/88
SCALE: NONE	PRINTED: A



REV.	DESCRIPTION	DATE	SIGNATURES
1	ISSUE FOR FAB	12/82	
2	DESCRIPTION	12/82	
3	REVISIONS		

DESIGNED BY	DATE
DRAWN BY	DATE
CHECKED BY	DATE
APPROVED BY	DATE

DATE	04	DESIGN NO.	A-5204-01 SD
REV.	04	ISSUE NO.	1
SCALE	NONE	SHEET	4

D S P TECHNOLOGY INC

MEMORY MODULE

SCHEMATIC: 5204: 512K MEMORY

DATE: 12/82

A

Alphanumeric LED Indicators, 15

Analog-to-Digital Converters, 4

B

Bipolar

Model 2860, 83

Bipolar Calibration and Alignment, 81

Model 2812, 79

Model 2824, 82

Model 2840, 81

Bipolar Mode Calibration

Model 2860, 83

Bipolar/Unipolar Signal Input Options

Bipolar, 83

Model 2812, 79

Model 2860, 83

Bipolar Calibration and Alignment

Model 2814, 81

C

Calibration and Alignment

Model 2860, 83

CAMAC Control, 27

CLK2 16th Bit Set, 65

Common Mode Rejection

Model 2812, 81

Control Registers

Model 4012, 39

Model 4012 Only, 53

Model 4032, 43

Controlling Sampling and Data Readout From CAMAC, 30

D

Data Acquisition Module

Model 2812 12 bit/100 kHz/8 Channel ADC, 79

Data Acquisition Module, 79

Data Streamout, 35

Data Streamout with Auto-restart, 36

Diagnostics, 55

Digital-to-Digital Converters t, 5

F

Front and Rear Panel Flat Cable Bus Connectors, 25

Front Panel

LED Indicators, 21

Signals, 23

Switch Controls, 22

Front Panel Indicators and Controls, 15

Alphanumeric LED Indicators, 15

CAMAC Control, 27

Front and Rear Panel Flat Cable Bus Connectors, 25

Front Panel LED Indicators, 21

Front Panel Signals, 23

Front Panel Switch Controls, 22

LED Indicators, 67

Models 4012P/4032P Rear Panel Signals, 24

Front Panel Indicators and Controls for Model 5000 Series, 67

G

General Description

4012P/4032P, 12

Model 4012 and Model 4032, 11

Model 5000 Series, 67

I

Input Signal, 69

Installation, 7

System Interconnections, 7

TRAQ Firmware, 66

L

LED Indicators, 21

M

Memory Modules, 67

General, 67

Input Signal, 69

Write Lock, 70

Model 2812

- Bipolar Calibration and Alignment, 79
- Bipolar/Unipolar Signal Input Options, 79
- Common Mode Rejection, 81
- Unipolar Calibration and Alignment, 80
- Model 2812 12 bit/100 kHz/8 Channel ADC, 79
- Model 2814, 81
 - Bipolar Calibration and Alignment, 81
- Model 2824, 82
 - Bipolar Calibration and Alignment, 82
 - Unipolar Calibration and Alignment, 83
- Model 2840, 81
 - Bipolar Calibration and Alignment, 81
- Model 2860
 - Bipolar Mode Calibration, 83
 - Bipolar/Unipolar Signal Input Options, 83
 - Bipolar, 83
 - Unipolar, 83
 - Calibration and Alignment, 83
- Model 2860 12 bit/1 mHz/4 Channel ADC, 83
- Model 4012, 53
- Model 4012 and 4032 TRAQ Controllers, 11
- Model 4012 and Model 4032
 - Differences, 13
- Model 4012 and Model 4032 TRAQ Controllers
 - General

- System Diagnostics, 13
 - General Description, 11
 - Model 4012 Control Registers, 39
 - Model 4012/4032 Control Registers
 - Reading, 49
 - Model 4012P and Model 4032P, 12
 - Model 4032, 53
 - Model 4032 Control Registers, 43
 - Model 4032/4012 Control Registers
 - Model 4012 Only, 53
 - Model 4032 Only, 53
 - Model 5000
 - Input Signal, 69
 - Model 5000 Series, 67
 - Front Panel Indicators and Controls, 67
 - LED Indicators, 67
 - Models 4012 and 4032 TRAQ Controllers
 - General Description
 - 4012 and 4032 Differences, 13
 - 4012P/4032P, 12
 - Models 4012/4032 Control Registers
 - Data Streamout, 35
 - Writing, 31
 - Models 4012P/4032P Rear Panel Signals, 24
 - Models 5000

Module ID Switches, 68

Module Switch Settings, 69

Write Lock, 70

Models 5000 Memory Modules

General Description, 67

Module ID Switches, 68

Module Switch Settings, 69

Module Switch Settings, 69

P

Programming the 4012/4032

Controlling Sampling and Data Readout From CAMAC, 30

Programming the 4012/4032 Control Registers, 27

R

Reading 4012/4032 Control Registers, 49

S

Section 1 TRAQ System, 1, **10**

Section 2 TRAQ Controllers, 11, **10-13**

Section 3 Front Panel Indicators, 15, **13-25**

Section 4 Programming the 4012/4032 Control Registers, 27, **30**

Section 5 Writing 4012/4032 Control Registers, **31-38**

Section 6 Model 4012 Control Registers, 39, **41**

Section 7 Model 4032 Control Registers Only, **43-47**

Section 8 Reading the 4012/4032 Control Registers, **49-54**

Section 9 Diagnostics, **55-63**

Section 10 Switch Options, **65-66**

Section 11 Series 5000 Memory Modules, 67-70

Section 12 TRAQ Digitizer Modules, 71-77

Section 13 Data Acquisition Module, 79-84

Signals, 23

Switch Controls, 22

Switch Options, 65

 CLK2 16th Bit Set, 65

 Installation of TRAQ Firmware, 66

System Description, 1

System Diagnostics

 Model 4012 and Model 4032, 13

System Interconnections, 7

T

TRAQ Contollers, 2

TRAQ Controllers

 Model 4012 and Model 4032, 11

TRAQ Current and Power Requirements, 6

TRAQ Digitizer Modules, 71

 Front Panel Description, 73

 LED Indicators, 73

 Module ID Switches, 73

 Bipolar/Unipolar Input Option, 74

 Input Signal Connectors, 74

 Input Signal Connection, 75

 2812M, 76

Signal Conditioning, 76

TRAQ Digitizer Module Specifications, 72

 Temperature Range, 72

TRAQ Installation, 7

TRAQ Memories, 3

TRAQ System, 1

 Analog-To-Digital Converters, 4

 Digital-to-Digital Converters, 5

 System Description, 1

 TRAQ Controllers, 2

 TRAQ Current and Power Requirements, 6

 TRAQ Installation, 7

 System Interconnections, 7

 TRAQ Memories, 3

 Typical TRAQ Configurations, 5

Typical TRAQ Configurations, 5

U

Unipolar

 Model 2860, 83

Unipolar Calibration and Alignment

 Model 2812, 80

 Model 2824, 83

W

Write Lock, 70

Writing Common 4012/4032 Control Registers, 31

Data Streamout, 35

Data Streamout with Auto-restart, 36