Model 721
VMEbus to SCSI
Controller User's Manual

Your Partner for Performance

166-721-001
Revision A
January 22, 1990

721 Revision Level History

Revision	Description
Rev. A (1/22/90)	Initial release.

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Specifications

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Specifications

1.1. General

The Xylogics Model 721 VME to SCSI host adapter controls up to 56 SCSI target devices in any combination. Host software can set the configuration of SCSI targets via the 721 software interface. The 721 provides a single high-performance SCSI port that supports both synchronous and asynchronous transfers; it also offers an optional floppy disk drive port. Data transfers occur between the VMEbus™ and SCSI or between the VMEbus and floppy.

1.2. Using This Manual

This manual provides two software reference cards that display the IOPB structure and codes (see inserts). Section 1 describes the 721 specifications, Section 2 provides installation information, Section 3 describes the 721 registers, Section 4 describes the IOPBs, and Section 5 describes the commands. Section 6 describes error processing, Section 7 is a programming tutorial, Section 8 explains the 721's special functions, and Section 9 contains VME and SCSI interface information.

A detailed theory of operation is available on a per customer basis.

1.3. Abbreviations

AIO	Add IOPB
AIOP	AIO Pending
AIOR	AIO Response Time
AM	Address Modifier
BDID	Bus Device ID
BHT	Black Hole Transfer
CC	Command Code
CCID	Change Controller ID
CDB	Command Descriptor Block

1.3. Abbreviations (continued)

CHEN	Chain Enable
CRIO	Clear Remove IOPB
CRBS	Clear Register Busy Semaphore
CRST	Controller Reset
DRDY	Drive Ready
ERRS	Error Summary
FDMAC	DMA Controller Chip
FERR	Fatal Error
FIFO	First In/First Out Buffer
H	Notation for hexadecimal values
INTRAM	8031 Internal Random Access Memory
IOPB	Input/Output Parameter Block
IRAM	IOPB Random Access Memory
LED	Light Emitting Diode
LSB	Least Significant Byte
LSI	Large Scale Integration
LUN	Logical Unit Number
MMA	Maintenance Mode Active
MM	Maintenance Mode
MSB	Most Significant Byte
NPRM	Non-privileged Request Mode
PRIO	Priority IOPB Request
RBS	Register Busy Semaphore
REGCEL	Register Read, Write, and Interrupt
RIO	Remove IOPB
ROM	Read Only Memory
ROR	Release on Request
RSTA	Controller Reset Active
RT	Register Test
SCSI	Small Computer System Interface
SGM	Scatter/Gather Mode
SPC	SCSI Protocol Chip
SWBY	Swap Bytes
SWWD	Swap Words
TDT	Throttle Dead Time
TGT	Target Select
TMOD	Transfer Mode

1.4. Design Reliability

The following Xylogics features minimize the likelihood of product failure:

- Design for worst case voltage and temperature
- Extensive evaluation testing
- Low parts count through extensive use of custom LSI
- Buffer parity for continuous error checking
- All components burned-in
- One card in backplane or expansion chassis
- Power-cycling under thermal stress during burn-in

1.5. Programmable Features

- Interrupt or polled operations
- DMA parameters
- Drive parameters

1.6. Physical

Packaging: The 721 resides on one printed circuit board.

Dimensions: The 721 is a 2 by 2 Eurocard that measures 9.2-inches high by 6.3-inches deep (233.35 mm by 160 mm). The 721 is identical in form-factor to the standard VME (dual high-dual wide) printed circuit board.

Shipping Weight: 3 pounds (1.4 kg).

Connectors: The 721 supports two SCSI bus connector schemes: the VME P2 connector with an external cable adapter and the front panel 50-pin header.

Front Panel: Xylogics offers the 721 with an optional front panel.

1.7. Environmental

The 721 environmental requirements are 0 through 55°C, with a maximum relative humidity of 90% (non-condensing). Air flow across the board must maintain a maximum temperature differential of 7°C to prevent hot spots.

1.8. Electrical

Power: The 721 uses 4.2 amperes at +5 volts DC (VDC).

Tolerance: Power voltage must be within ±5% (4.75 to 5.25).

Grounding: Common earth ground must be established between the SCSI devices and the CPU chassis, backplane, and expansion cabinets.

1.9. System-related Specifications

Data Transfer Modes: The 721 transfers data in word or longword mode. It may use byte transfers to align subsequent transfers on word boundaries.

I/O Addressing Capability: The 721 decodes byte addresses for its on-board registers.

Data Buffering: The 721 has a 256 byte FIFO buffer. Data can be put into one end of the FIFO and simultaneously removed at the other end. There are no delays associated with filling and emptying the buffer.

Command Buffer: The 721 reads commands into a separate buffer that holds up to 14 full commands (IOPBs); this minimizes host processor intervention and optimizes controller decode overhead. The 721 can also store an additional 35 IOPB addresses.

Status LEDs: The 721 has two status LEDs. The green LED indicates the controller is active; the yellow LED indicates the on-board diagnostics did not complete successfully or a fatal error occurred.

On-board Diagnostics: The 721 runs an extensive on-board diagnostic routine upon power-up or a bus reset. If an error occurs during this test, the 721 posts the failure in a special error register.

1.9. System-related Specifications (continued)

Multiprocessor Support: The 721 has a built-in register control semaphore. This flag allows multiple processors to share the 721 register set.

Scatter/Gather: The 721 supports Scatter Read and Gather Write commands. The controller gathers data from various memory locations and transfers it to the buffer for use in a Write command. It scatters the data out from the SCSI drive to the appropriate memory locations with a Read command. To execute a scatter/gather, software issues a normal Read or Write command along with a DMA list containing a memory address and the number of 16-bit words to transfer to/from that location. The smallest granularity of scatter/gather is one 16-bit word.

Priority IOPBs: The 721 executes priority IOPBs over all IOPBs in its command buffer, except for the one in process.

Black Hole Transfers: The 721 may transfer all the DMA data into the same bus address without incrementing the address at each DMA.

Block Mode Transfers: The 721 supports block mode as per the VMEbus Specification. Block mode reduces data transfer times by allowing a DMA device to use one memory address strobe for up to 256 bytes.

1.10. SCSI-related Specifications

Small Computer System Interface: Conforms fully to the American National Standard for Information Systems (ANSI) X3.131-1986.

Data Transfer Rate: The 721 supports data transfer rates of up to 3 megabytes per second (MB/s) asynchronously and 5 MB/s synchronously.

Disconnect/Reconnect Facility: The 721 supports targets that can disconnect and reconnect at a later time.

Common Command Set: The 721 supports the SCSI Common Command Set (CCS).

SCSI Channel Controller: The 721 uses the Fujitsu MB87030 LSI SCSI Channel Controller.

SCSI Device Support: The 721 supports all SCSI devices, including magnetic and optical disks, and tape drives.

SCSI Bus Drivers: The 721 supports single-ended drivers and receivers.

1.11. Floppy Disk Drive-related Specifications
(not implemented in this version of the controller)

Data Transfer Rate: The 721 supports a floppy disk transfer rate of up to 500K-bits per second or less.

Sector Size: The 721 supports four different sector sizes: 128, 256, 512, and 1024 bytes.

Floppy Controller: The 721 uses the Western Digital 37C65 floppy controller with built-in drivers and receivers.

Number of Floppy Drives: The 721 supports up to two floppy drives in normal or PC/AT mode.

Drive Types: The 721 supports 3.5-, 5.25-, and 8-inch drives. The factory configures the 721 with connectors used on 5.25-inch form factor drives.

Drive Formats: The 721 supports IBM, PC/AT, and PC/XT formats.

1.12. VMEbus-related Specifications

VME Compliance Number: IEEE P1014/D1.0.

Transfer Mode: Direct Memory Access (DMA).

DMA Throttle Control: Each time the 721 becomes bus master, it executes DMA transfers to or from the buffer up to the maximum throttle parameter or the number of bytes/spaces available in the buffer.

DMA Data Transfer Rate: The 721 has a maximum transfer rate of 30 MB/s based on 30 nanoseconds (ns) memory response time assuming longword mode transfers.

DMA Dead Time: The 721 supports a programmable DMA dead time between throttle bursts. This prevents the 721 from taking over the bus and allows time for other DMA devices to access the bus.

Data Transfer Limit: From 0 to $2^{24}-1$ bytes.

Bus Compatibility: The 721 is compatible with the standard VMEbus (C.1).

1.12. VMEbus-related Specifications (continued)

Addressing Capability: Full 32-bit support. The 721 supports master A32, and slave A16, as per the VMEbus Specification. As a slave, the 721 responds to address modifiers 29H and 2DH. The 721 also supports block transfers.

Data Width: The 721 supports D16 and D32 as per the VMEbus Specification.

Release On Request: The 721 optionally releases the bus at the request of other VMEbus masters.

Release When Done: The 721 releases the bus after each throttle burst.

Bus Request Levels: The 721 supports four bus request levels.

Interrupt Priority: Software programmable interrupt level and vector.

1.13. Software-related Specifications

Controller IOPB Length: 36 bytes.

Controller Registers: Seven 8-bit I/O Registers; byte or word addressable. Only eight bits respond during word access.

Software Control: Software can program the 721 for use with various SCSI targets, controller parameters, and controller options

Diagnostic Support: Comprehensive set of stand-alone diagnostics written in the *C* language are available.

1.13.1. Software Interface

The software interface includes seven byte-wide registers. The first four bytes comprise the VME Address Register, the fifth byte is the Address Modifier Register, the sixth byte is the Control and Status Register (CSR), and the last byte is the Fatal Error Register (FER). The CSR includes two bits that are very important to IOPB processing: *Add IOPB* (AIO) and *Remove IOPB* (RIO).

1.13.1. Software Interface (continued)

The IOPB is a block of command and status information that includes the bus address and the type of operation. The software driver sets up the IOPB in host memory, sends the IOPB address to the VME Address Registers, and sets AIO. After receiving the IOPB address, the 721 clears AIO, DMAs the IOPB to its IRAM, executes the IOPB and, upon completion or error, updates the IOPB status, DMAs it back and sets RIO. The VME Address Registers point to the completed IOPB. The software driver reads the address and clears RIO. Software may add IOPBs to the queue, providing AIO is clear, by writing the IOPB address to the address registers and setting AIO, regardless of the 721's *Busy* status.

1.13.2. Software Drivers

Xylogics provides its customers with UNIX™ drivers for a variety of VME-based systems. Currently, Xylogics offers a full device driver and diagnostic support for Sun Microsystems' ™ Sun-3 and Sun-4 series machines. Xylogics also provides UNIX System V drivers for a variety of machines. A format utility for these drivers enables formatting, defect management, and feature tuning.

2

Installing and Testing the Controller

2

Installing and Testing the 721

2.1. General

This section describes how to unpack, configure, install, and test your 721 controller.

2.2. Unpacking and Inspection

2.2.1. Inspect the Shipping Carton and the Controller

Inspect the shipping carton. If it is damaged, do not unpack the unit. Notify Xylogics and the freight carrier immediately. If no damage is visible, carefully unpack the 721. Save the carton and other packing materials for future use.

2.2.2. Contents

The 721 is a single printed circuit board. Optional items include a manual and/or software on a ¼-inch cartridge or ½-inch magnetic tape.

If any items are missing or damaged, please contact Xylogics at one of the following telephone numbers.

United States (Burlington, MA): (617) 272-8140;
United Kingdom (Milton Keynes): 44-908-22212.

2.2.3. Handling Precautions

Observing proper handling precautions minimizes the risk of damaging the 721 with electrostatic discharge. When transporting the 721, use an antistatic bag, antistatic bin, or the original shipping carton and packing material. Personnel handling the 721 should observe proper grounding methods including, but not limited to, wrist bands, heel straps, and antistatic mats.

2.3. Configuring the 721

You can configure the 721 with several jumper options. The following subsections describe these options.

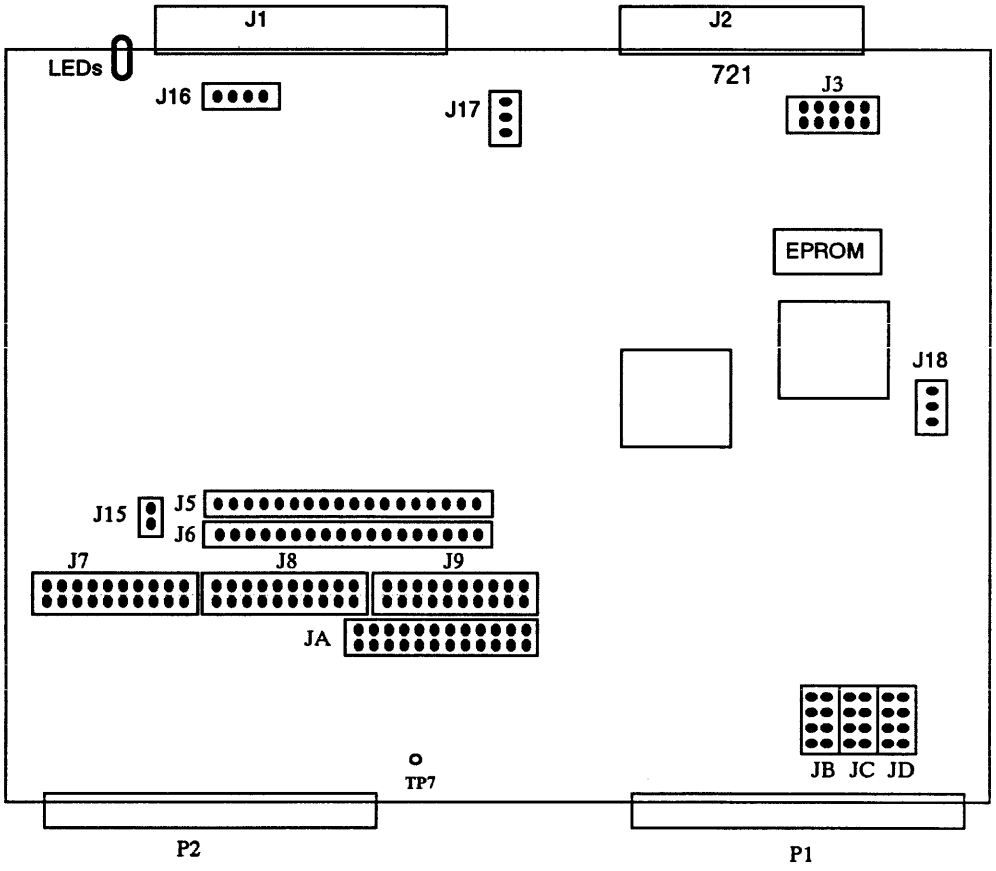


Figure 2-1. Approximate Jumper Locations

2.3.1. Base Address Selection

Jumper block JA controls the base address. Figure 2–3 shows how to set the jumpers for commonly used base addresses. Inserting a jumper makes the 721 respond to a zero on that address line; removing a jumper makes the 721 respond to a one. The 721 uses bits 1 through 3 to determine which register is being accessed. The 721 is an A16 slave, and responds to address modifier 2DH, and optionally to 29H. Factory setting: EEC0.

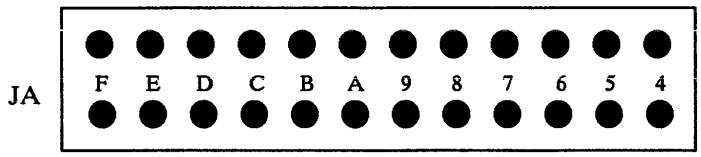


Figure 2–2. Jumper Block JA

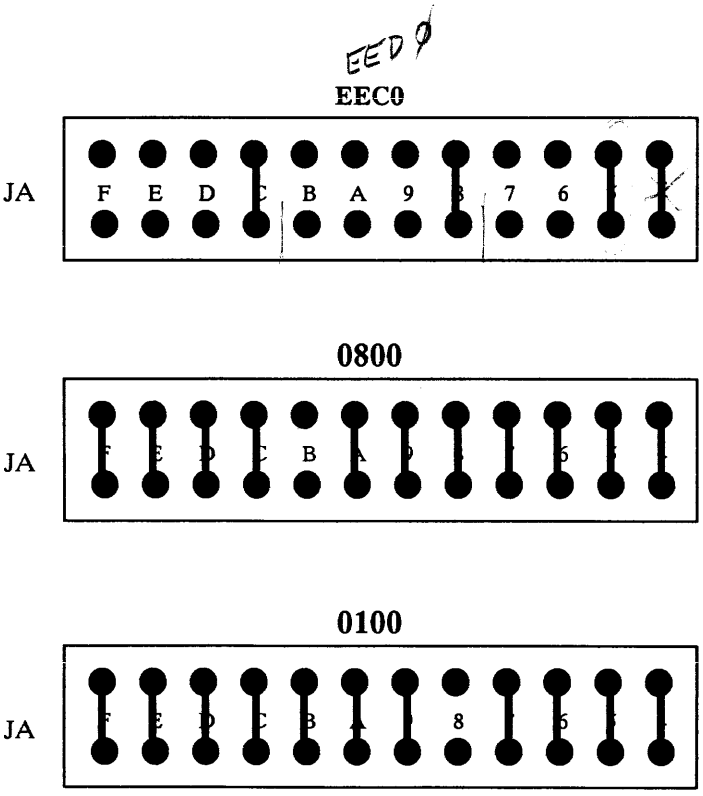


Figure 2–3. Jumpering the Base Address

2.3.2. Bus Request and Bus Grant Lines

The 721 uses the Bus Request and Bus Grant lines to become bus master. In VMEbus arbitration, there are four Bus Request/Grant levels: 0 through 3. The 721 drives one Bus Request line according to the jumper scheme you choose. The arbiter responds by driving the associated Bus Grant In line (i.e., *BG0IN* responds to *BR0*). If the 721 receives a Bus Grant on any of the Bus Grant In lines (*BG0IN* through *BG3IN*), and is not requesting the bus on that line, it passes the grant to the appropriate Bus Grant Out line: *BG0OUT* through *BG3OUT*.

Select a request level by jumpering one Bus Request (*BR0* through *BR3*), one Bus Grant In, and one Bus Grant Out line to match the selected request level. Jumper the remaining Bus Grant In/Out lines so that the incoming signal passes through the board (i.e., jumper *BGxIN* to *BGxOUT*, where x represents the remaining grant levels).

For example, Figure 2-3 shows the jumpering scheme for level 3 (the pins are numbered for this example): jumper JB4 to JB8; then jumper JC4 to JC8, and JD4 to JD8. Jumper the remaining grant levels from JC5 to JD1, JC6 to JD2, and JC7 to JD3. Factory configuration: Bus Request Level 3.

> *Some VME systems only support Bus Request Level 3.*

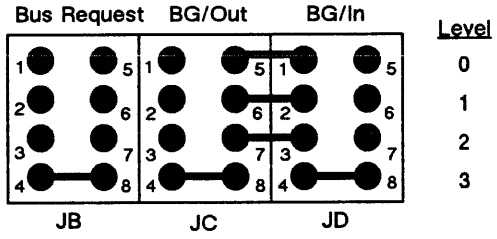


Figure 2-4. Jumpers JB, JC, and JD

2.3.3. P2 Connector

When using the P2 connector, jumper J5*n* to J6*n*, where *n* = 1 to 18. Also, install all jumpers in J7, J8 and J9. Factory setting: all jumpers *out*.

> *Do not use the front panel SCSI connector when using the P2 connector.*

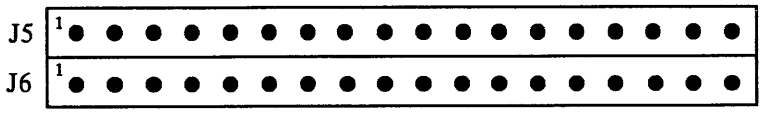


Figure 2–5. Jumper Blocks J5 and J6

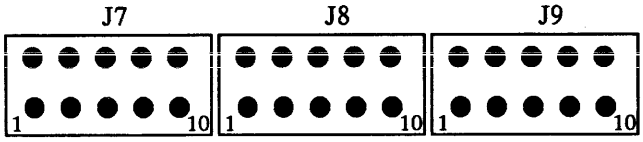


Figure 2–6. Jumper Blocks J7, J8, and J9

2.3.4. P2 Terminator Power

To supply terminator power (TERMPWR) on the P2 bus, install jumper J15. Factory setting: J15 *out*.

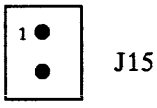


Figure 2–7. Jumper Block J15

2.3.5. Controller Terminator Power

The 721 accepts or generates terminator power, depending on J16's configuration. Factory setting: J16 3–4 *in*.

To generate terminator power locally to the 721, jumper J16 3–4 *in*.

To generate terminator power locally and to the SCSI bus, jumper J16 1–2 *in* and 3–4 *in*.

To accept terminator power from the SCSI bus, jumper J16 1–2 *in*.

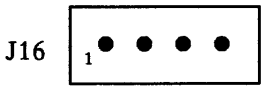


Figure 2–8. Jumper Block J16

2.3.6. SCSI Timing

To run the SCSI bus at a maximum speed of 4 MHz, jumper J18 2–3 *in*. To run the SCSI bus at a maximum speed of 5 MHz, jumper J18 1–2 *in*. Factory setting: J18 2–3 *in*.

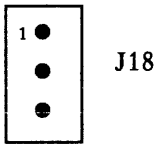


Figure 2–9. Jumper Block J18

2.3.7. Floppy Disk Jumper J3

Jumper J3 determines the floppy drive type (AT or other). Future versions of the controller will implement this feature. Factory setting: all jumpers *out*.

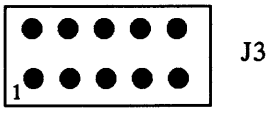


Figure 2–10. Jumper Block J3

2.3.8. Floppy Disk Jumper J17

Jumper J17 determines the floppy drive type (AT or other). Future versions of the controller will implement this feature. Factory setting: J17 *out*.

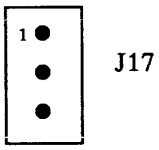


Figure 2-11. Jumper Block J17

2.4. EPROM and PAL Part Numbers

Table 2-1. PROM/PAL Part Numbers and Locations

Part Number	Location	Type
181-001-088	U31	PAL 1
181-001-089	U26	PAL 2
181-001-090	U37	PAL 3
180-002-307	U56	EPROM

2.5. Light Emitting Diodes

The 721 has two light emitting diodes (LEDs). When the green LED is lit, the 721 is active. During power-up, the yellow LED lights for a moment and then goes off. If it remains on, a fatal error or self test error occurred.

2.6. Board Labels/Revision Control

All Xylogics controllers use revision control labels. They are located on the soldered side of the board. The revision level is important when discussing configuration issues.

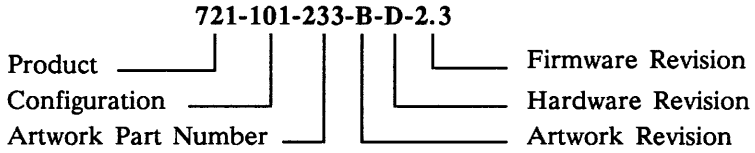


Figure 2-12. Sample Part Number

2.7. Preparing the Computer System for Installation

The backplane of your system must provide a VMEbus slot for the 721. The slot must be capable of handling a bus master, and the power source must handle the power consumption of the entire system, including the 721.

2.7.1. Backplane Jumpers

Remove any jumpers that short, or cause the Interrupt Acknowledge (*IACK IN/OUT*) and DMA Grants (*BG 0-3 IN/OUT*) to bypass the slot in which you are installing the 721.

2.7.2. Card Cage Slot

The card cage must have a slot at the proper DMA priority available for the 721. The 721 uses DMA to transfer data and IOPBs. Placement of the 721 in the DMA priority chain may be critical. The amount of bus bandwidth it uses will be high at times; this may affect other boards in the system. Likewise, other boards may not allow enough time for the 721 to DMA enough data to keep up with the SCSI; consider this when choosing a slot. For example, if the 721 does not get a high enough priority, then its DMA falls behind the SCSI requirements, and the SCSI device must wait for the 721. If the 721 priority is high, it gets enough DMA time, but other boards having smaller buffers may not receive enough data within the allotted DMA time. The priorities must be balanced for your system to work properly.

2.7.3. Power Considerations

The 721 affects the power consumption of the entire computer system. The 721 uses +5 volts (4.75 to 5.25 volts) at 4.2 amps. Make sure the power supplies can handle the entire power load. Readjust the voltages *after* plugging in the 721. A power supply that is just adequate may cause intermittent and unusual problems as it generates noise from occasional overcurrent protection.

2.8. Installing the 721

Place the 721 into the computer card cage; make sure it is firmly seated. Be careful not to dislodge any socketed ICs. Situate the SCSI device and connect it to its power source.

2.9. Cabling the Subsystem

2.9.1. Mechanical Restraint

Mechanically restraining the SCSI cable at both ends prevents it from accidentally disconnecting. Using *pull tabs* on the cable greatly reduces connector damage.

2.9.2. SCSI Device Grounds

Install a ground braid wire between the ground terminal on the SCSI device(s) and the computer system ground.

2.10. Power-up Self Test

The 721 initiates a self test upon power-up. The yellow LED lights for a moment, and then goes off. If it remains on, the board is not functioning properly or the SCSI cable is backwards. The Fatal Error Register may indicate the nature of the problem. Check the power supply voltage to ensure it is within limits (4.75 to 5.25 volts). Contact Xylogics for further assistance.

2.11. Diagnostics

When you run your diagnostics:

- Run a full pass of your diagnostic or determine that the system is working properly
- Cable and test any additional devices

2.12. Cabling Multiple SCSI Devices

If you are using multiple devices, make sure the cables are properly connected. Observe the *pin 1* markings on both the cables and the devices (see Figure 2-13 and Figure 2-14).

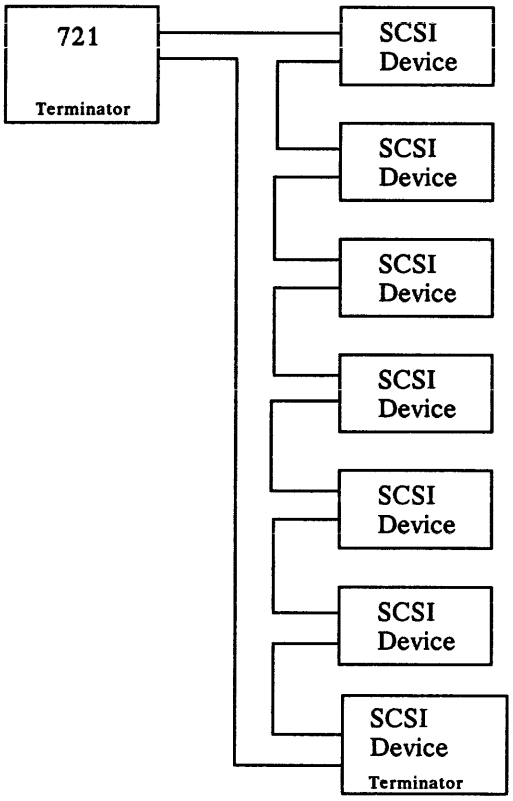


Figure 2-13. Single Initiator, Multiple Target

2.12. Cabling Multiple SCSI Devices (continued)

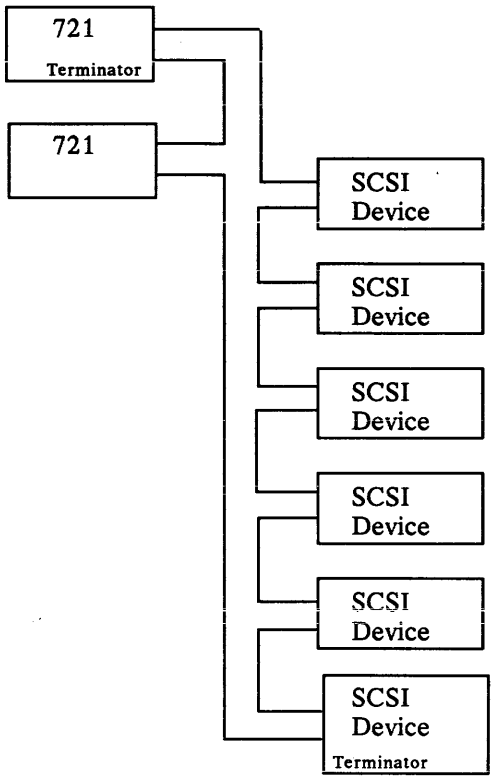


Figure 2–14. Multiple Initiators, Multiple Targets

2.12.1. Terminators

The SCSI bus requires terminators in the first and last connecting SCSI device. Since the 721 has an on-board terminator, only the last SCSI device on the bus requires a terminator. The 721 offers terminator power as a jumper option (J16) with three configurations: supply terminator power to the SCSI bus, supply terminator power locally, and accept terminator power from the bus (see Section 2.3.5.).

2.12.2. Target Select

In a single initiator, multiple target application, assign each target a unique SCSI identification (ID) number. The 721 accesses targets with ID numbers ranging from 0 through 6. ID number 7 is reserved as the 721 default (see Section 5). Each target can connect up to eight logical units having logical unit numbers that range from 0 through 7.

3

The Controller Registers

3

The 721 Registers

3.1. General

The 721 programming interface uses seven, one-byte long, I/O registers. These registers have one function when read, and another when written. The bus address jumpers define the register set's base address. Table 3-1 lists the registers and the address offset from the base address. Figure 3-1 illustrates the register map, assuming you use EEC0 as the base address.

Table 3-1. Register Offsets

Register	Offset
IOPB Address Byte 0 (Least Significant Byte)	1
IOPB Address Byte 1	3
IOPB Address Byte 2	5
IOPB Address Byte 3 (Most Significant Byte)	7
IOPB Address Modifier	9
Control and Status Register	B
Fatal Error Register	D

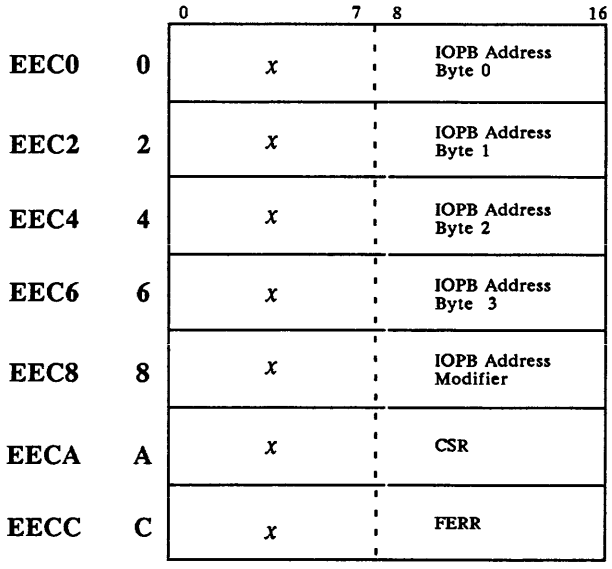


Figure 3-1. Register Map

3.2. IOPB Address Registers

The first four registers define the 32-bit address of an IOPB. When you write these registers, the 721 interprets the address of the IOPB ready for execution. When you read them, and *Remove IOPB* (RIO) is set in the Control and Status Register, the registers point to the IOPB that the 721 just completed (see Section 3.4.).

3.3. IOPB Address Modifier/Priority IOPB Register

This register defines the IOPB address modifier. Address modifiers are used for many purposes, such as memory mapping, privilege levels, and addressing range (see the VMEbus Specification).

This register also specifies whether an IOPB has priority over the current set of IOPBs in the 721 command queue. Section 3.4. defines the protocol for reading and writing this register.

7	6	5	4	3	2	1	0
Priority IOPB Request	Reserved	Address Modifier					

Bit	Mnemonic	Description
7	PRIO	**Priority IOPB Request:** When set, the IOPB, precedes all others, except the one in process, in the command queue.
6		**Reserved.**
5-0	AM	**Address Modifier:** Most systems use the standard AM code of 3DH (see the VMEbus Specification).

3.4. Control and Status Register

When written, this register provides the host with control of the 721 operation. When read, it provides the host with 721 status information. Section 3.4.1. defines the bits in this register when written; Section 3.4.2. defines the bits when read.

3.4.1. Control Register (Write)

7	6	5	4	3	2	1	0
Register Test	Reserved	Maint. Mode	Reserved	Controller Reset	Add IOPB	Clear RIO	Clear RBS

Bit	Mnemonic	Description
7	RT	**Register Test:** In maintenance mode, when RT, MM, and AIO are set, the 721 echoes back the values previously written in all of the registers (except the CSR).
6		**Reserved.**
5	MM	**Maintenance Mode:** Setting MM and AIO places the 721 in maintenance mode. Maintenance mode supports a different register protocol; use it as a diagnostic tool.
4		**Reserved.**
3	CRST	**Controller Reset:** When set, the 721 performs a *soft* reset to recover from fatal errors; it reinitializes its IOPB and AIO address storage RAM, cancelling any IOPBs in its queues, and clears the Fatal Error Register and CSR. The 721 does not generate RIOs for cancelled IOPBs. A controller reset does not affect the SCSI bus, and leaves outstanding SCSI transfers in an indeterminate state. A SCSI bus reset should follow a controller reset. *A Controller Reset takes up to one-half second to complete.*
2	AIO	**Add IOPB:** When set, the 721 executes the IOPB at the address pointed to by the IOPB Address and Address Modifier Registers. As soon as the host sets AIO, the 721 sets *AIO Pending* (AIOP) in the Status Register indicating the 721 has received AIO, but has not yet processed the new IOPB address. The 721 clears AIOP after internally storing the new address. Setting AIO while AIOP is set violates the register protocol.

3.4.1. Control Register (Write) (continued)

Bit	Mnemonic	Description
1	CRIO	**Clear RIO:** The host sets CRIO to clear RIO in the Status Register. Typically, the host sets CRIO after reading the address of a completed IOPB from the IOPB Address and Modifier Registers. Clearing RIO enables the 721 to update the IOPB Address and Modifier Registers with the address and address modifier of a newly completed IOPB. Clearing RIO, if it is not set in the Status Register, violates the register protocol.
0	CRBS	**Clear RBS:** The host sets CRBS to clear RBS in the Status Register. Clearing RBS releases the registers for use by another host. CRBS is relevant only in a multiprocessor environment.

3.4.2. Status Register (Read)

7	6	5	4	3	2	1	0
Busy	Fatal Error	Maint. Mode Active	Reserved	Controller Reset Active	AIO Pending	Remove IOPB	Register Busy Sema-phore

Bit	Mnemonic	Description
7	BUSY	**Busy:** The 721 is processing IOPBs. The 721 sets *Busy* when it clears AIOP to acknowledge the first IOPB address; it clears *Busy* after completing all the IOPBs with no new ones pending (within 500 microseconds of the host clearing RIO on the last IOPB). The 721 redefines this bit in maintenance mode.

3.4.2. Status Register (Read) (continued)

Bit	Mnemonic	Description
6	FERR	**Fatal Error:** When set, the 721 detected a fatal hardware error. A fatal error asserts *SYSFAIL*. Setting CRST clears FERR. The Fatal Error Register holds more specific information. The 721 sets FERR under the following conditions: • Maintenance mode test failure • Power-up self test failure • IOPB DMA fatal • IOPB address alignment error • Firmware error • Illegal maintenance mode test number
5	MMA	**Maintenance Mode Active:** When set, the 721 is in maintenance mode.
4		**Reserved.**
3	RSTA	**Controller Reset Active:** The host set CRST in the Control Register and the 721 is reinitializing.
2	AIOP	**AIO Pending:** When set, AIO has been set in the Control Register, but the 721 has not acknowledged its receipt. When clear, AIO may be set again.
1	RIO	**Remove IOPB:** The 721 sets RIO after completing an IOPB, and placing the address in the IOPB Address and Address Modifier Registers. After the host reads the address and modifier, it must clear RIO by writing CRIO in the Control Register.
0	RBS	**Register Busy Semaphore:** RBS allows multiple hosts to share access to the 721 registers without simultaneous access. RBS is relevant only in a multiprocessor environment.

3.5. Fatal Error Register

If a fatal error occurs, the 721 returns the appropriate completion code in this register. Table 3–2 lists the fatal error codes. Section 6.4. describes them. All codes not listed are reserved.

Table 3–2. Fatal Error Codes

Code	Description
E1	IRAM/8031 INTRAM Self Test Failure
E2	SCSI Cable Installed Backwards
E3	SPC Register Self Test Failure
E5	FDMAC Register Self Test Failure
E6	REGCEL Self Test Failure
E8	FIFO Self Test Failure
F1	IOPB DMA Fatal
F2	IOPB Address Alignment Error
F3	Firmware Error
F5	Illegal Maintenance Mode Test Number
F6	Abort Message Rejected
F9	SCSI Illegal Transfer Phase
FC	Global Timeout Error

4

IOPB Description

4

IOPB Description

4.1. General

The Input/Output Parameter Block (IOPB) passes messages between the 721 and host software. Software passes the type of transfer, target address, data address, and count to the 721; the 721 returns the transfer status and possibly the ending addresses upon command completion. Each IOPB includes 24 bytes of controller information, and 6, 10, or 12 bytes of SCSI command descriptor block (CDB).

4.2. Standard IOPB

The 721 uses the standard 36-byte IOPB for all commands.

	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM	Controller Code			
01	Completion Code							
02	SCSI Status							
03	0				CCID	0	SWWD	SWBY
04	0							
05	0			BHT	0	Target Select		
06	Link List Length					Interrupt Level		
07	Interrupt Vector							
08	0							
09	DMA Byte Count High							
0A	DMA Byte Count							
0B	DMA Byte Count Low							
0C	0							
0D	0							
0E	Data or Link Address Modifier							
0F	Next IOPB Address Modifier							
10	DMA Data or Link Address High							
11	DMA Data or Link Address							
12	DMA Data or Link Address							
13	DMA Data or Link Address Low							
14	Next IOPB Address High							
15	Next IOPB Address							
16	Next IOPB Address							
17	Next IOPB Address Low							
18 – 23	CDB Bytes 0 through 11							

4.2.1. IOPB Byte 0 (Channel Byte)

7	6	5	4	3	2	1	0
Error Summary	Done	Chain Enable	Scatter/ Gather Mode	Controller Code			

Bit	Mnemonic	Description
7	ERRS	**Error Summary:** ERRS is only valid if *Done* is set. When set, a hard or soft error occurred during IOPB processing. When clear, the 721 successfully completed the IOPB.
6	DONE	**Done:** The 721 sets *Done* after completing the IOPB.
5	CHEN	**Chain Enable:** When set, the Next IOPB Address Modifier and Next IOPB Address point to the next chained IOPB. When clear, this IOPB is not chained to another IOPB.
4	SGM	**Scatter/Gather Mode:** When set, the IOPB is either a scatter read or a gather write transfer. A link list describes the number of 16-bit words and the address to which the 721 transfers each section of the data. The link address modifier and the link address specify the link list location. When clear, this IOPB specifies the data transfer address. The data is transferred to/from contiguous memory.
3–0	CD	**Controller Code:** Always set this field to 0FH.

4.2.2. IOPB Byte 1 (Completion Code)

After the 721 executes the IOPB, it sets *Done* and posts a completion code in this byte. Completion codes are only valid if *Done* is set. A code of 00H indicates a successful completion; any other value indicates an error occurred (see Section 6.3.).

4.2.3. IOPB Byte 2 (SCSI Status)

IOPB Byte 2 is the SCSI Status byte; it is valid only if *Done* is set. The selected target returns this byte after completing each command. It is the last SCSI status that the target returns while running this IOPB or it is an equivalent byte for the floppy drives (see Table 4-1).

Vendor-unique means the American National Standards Institute (ANSI) has not defined the bit, field, or code value. SCSI device manufacturers define these fields.

7	6	5	4	3	2	1	0
Reserved	Vendor-unique		Status Code				Vendor-unique

Table 4-1. SCSI Status Codes

Value	Description
0000	Good
0001	Check Condition
0010	Condition Met/Good
0011	Reserved
0100	Busy
0101	Reserved
0110	Reserved
0111	Reserved
1000	Intermediate/Good
1001	Reserved
1010	Intermediate/Condition Met/Good
1011	Reserved
1100	Reservation Conflict
1101	Reserved
1110	Reserved
1111	Reserved

4.2.4. IOPB Byte 3 (Controller Command)

7	6	5	4	3	2	1	0
Reserved				Change Controller ID	Reserved	Swap Words	Swap Bytes

Bit	Mnemonic	Description
7–4		**Reserved.**
3	CCID	**Change Controller ID:** When set, you can change the 721 SCSI ID with a Write Controller Parameters command.
2		**Reserved.**
1	SWWD	**Swap Words:** When set, the 721 swaps the significance of the two words in a data longword. Swapping does not occur on IOPB transfers, scatter/gather lists, or 721 mode sense/select data, and is independent of setting TMOD. Swap word is not restricted to longword aligned data.
0	SWBY	**Swap Bytes:** When set, the 721 swaps the significance of the two bytes in a data word. Swapping does not occur on IOPB transfers, scatter/gather lists, or 721 mode sense/select data, and is independent of setting TMOD. Swap Byte transfers are illegal and cause an error if the data address (IOPB Byte 13) is an odd number. Swap bytes is not restricted to word aligned data.

4.2.5. IOPB Byte 5 (Target Select)

7	6	5	4	3	2	1	0
Reserved			Black Hole Transfer	Reserved	Target Select		

Bit	Mnemonic	Description
7–5		**Reserved.**

4.2.5. IOPB Byte 5 (Target Select) (continued)

Bit	Mnemonic	Description
4	BHT	**Black Hole Transfer:** When set, the 721 does not increment the bus address during a data transfer; IOPB transfers occur normally. When clear, the 721 does increment the bus address.
3		**Reserved.**
2–0	TGT	**Target Select:** Contains the target device's SCSI bus ID.

4.2.6. IOPB Byte 6 (Interrupt Level)

7	6	5	4	3	2	1	0
Link List Length					Interrupt Level		

Bit	Mnemonic	Description
7–3	LLL	**Link List Length:** Bits 7 through 3 specify the length, in elements, of a link list for Scatter/Gather commands. Each element is an 8-byte block in the link list (see Table 8–2).
2–0	INTL	**Interrupt Level:** The 721 uses INTL as the VMEbus interrupt level after completing the IOPB. The 721 does not interrupt if the level is zero.

4.2.7. IOPB Byte 7 (Interrupt Vector)

IOPB Byte 7 determines the interrupt vector that the 721 uses upon command completion. This byte is not valid if the interrupt level is zero.

4.2.8. IOPB Bytes 9 through B (DMA Count)

IOPB Bytes 9 through B are the DMA Count. These bytes specify how many bytes the 721 transfers in a data transfer, Write Controller Parameters, or Read Controller Parameters IOPB. The DMA count must correspond to the transfer length in the CDB.

4.2.9. IOPB Byte E (Data or Link Address Modifier)

7	6	5	4	3	2	1	0
Reserved		Data or Link Address Modifier					

Bit	Description
7–6	**Reserved.**
5–0	**Data or Link Address Modifier:** If SGM is set, this field specifies the link list address modifier; if SGM is clear, it specifies the data address modifier.

4.2.10. IOPB Byte F (Next IOPB Address Modifier)

7	6	5	4	3	2	1	0
Reserved		Next IOPB Address Modifier					

Bit	Mnemonic	Description
7–6		**Reserved.**
5–0	NIAM	**Next IOPB Address Modifier:** This field, along with the Next IOPB Address, points to the next IOPB in the chain. NIAM must contain a valid modifier value if CHEN is set.

4.2.11. IOPB Bytes 10 through 13 (DMA Data or Link Address)

IOPB Bytes 10 and 11 are DMA Data Address High; Bytes 12 and 13 are DMA Data Address Low. These bytes comprise the data or SGM link list address pointers. The 721 uses these bytes with the data or link list address modifier to point to the data or linked list address. If SGM is set, this address points to the linked list; if SGM is clear, this address points to the data address. The 721 uses the data address when transferring both data and mode sense or select information to or from host memory.

4.2.12. IOPB Bytes 14 through 17 (Next IOPB Address)

IOPB Bytes 14 and 15 are Next IOPB Address High; Bytes 16 and 17 are Next IOPB Address Low. These bytes comprise the Next IOPB Address pointers. The 721 uses these bytes with the Next IOPB Address modifier to point to the next IOPB in the chain (if CHEN is set in Byte 0).

4.2.13. IOPB Bytes 18 through 23 (SCSI CDB)

IOPB Bytes 18 through 23 are the SCSI command descriptor block. The 721 passes the CDB to the SCSI target device (see Section 4.3.).

4.3. SCSI Command Descriptor Block

IOPB Bytes 18H through 23H comprise the SCSI command descriptor block (CDB). The CDB can be 6-, 10-, or 12-bytes long. The 721 uses the CDB to prepare its data transfer and DMA paths; it sends the complete CDB to the SCSI target. All reserved bits, fields, or bytes must equal zero. For all commands, if there is an invalid parameter in the CDB, the target terminates the command without altering the medium.

Each CDB has an operation code as its first byte, followed by a logical unit number, command parameters (if any), and a control byte. The ANSI X3.131–1986 Specification (pages 51–184) describes the SCSI CDB more fully.

4.3.1. Typical Six-byte Command Descriptor Block

The logical block address and the transfer length (specified in blocks or bytes) are not always required and depend on both the command and device type. The CDB transfer length must correspond to the IOPB DMA byte count.

Offset IOPB	Offset CDB	7	6	5	4	3	2	1	0
18	00	Operation Code							
19	01	Logical Unit Number			Logical Block Address (MSB)				
1A	02	Logical Block Address							
1B	03	Logical Block Address (LSB)							
1C	04	Transfer Length							
1D	05	Control							

4.3.2. Typical Ten-byte Command Descriptor Block

Offset IOPB	Offset CDB	7	6	5	4	3	2	1	0
18	00	Operation Code							
19	01	Logical Unit Number			0				RAD
1A	02	Logical Block Address (MSB)							
1B	03	Logical Block Address							
1C	04	Logical Block Address							
1D	05	Logical Block Address (LSB)							
1E	06	0							
1F	07	Transfer Length (MSB)							
20	08	Transfer Length (LSB)							
21	09	Control							

4.3.3. Typical Twelve-byte Command Descriptor Block

Offset IOPB	Offset CDB	7	6	5	4	3	2	1	0
18	00	Operation Code							
19	01	Logical Unit Number			0				RAD
1A	02	Logical Block Address (MSB)							
1B	03	Logical Block Address							
1C	04	Logical Block Address							
1D	05	Logical Block Address (LSB)							
1E	06	0							
1F	07	0							
20	08	0							
21	09	Transfer Length (MSB)							
22	0A	Transfer Length (LSB)							
23	0B	Control							

4.3.4. CDB Byte 0 (Operation Code)

The first byte of all CDBs is the operation code.

7	6	5	4	3	2	1	0
Group Code			Command Code				

Bit	Mnemonic	Description
7–5	GC	**Group Code:** Designates one of eight command groups. The 721 fully supports the mandatory, optional, and extended commands in Groups 0 and 1. Groups 2 through 7 are all vendor-unique or reserved commands. The 721 supports these commands by passing through software requests and transferring data or parameters according to the SCSI bus data phase.

4.3.4. CDB Byte 0 (Operation Code) (continued)

Bit	Mnemonic	Description
4–0	CC	**Command Code:** Designates one of 32 commands available in the group.

Table 4–2. Group Codes

Group	Description
0	6-byte commands
1	10-byte commands
2–4	Reserved
5	12-byte commands
6–7	Vendor-unique commands

4.3.5. CDB Byte 1 (Logical Unit Number)

The second byte of all CDBs defines the logical unit number of the peripheral device attached to the selected SCSI target to which the command applies. It also contains other information that is command- and device type-dependent (see Section 5).

4.3.6. CDB Bytes 2 through 10 (Transfer Information)

Six-byte CDBs use Bytes 2 through 4, 10-byte CDBs use Bytes 2 through 8, and 12-byte CDBs use Bytes 2 through 10. These bytes may be reserved, specify the logical block address for a command on a direct access device, or a transfer count on a sequential access device (see Section 5).

4.3.7. CDB Bytes 5, 9, and 13 (Control)

Six-byte CDBs use Byte 5, 10-byte CDBs use Byte 9, and 12-byte CDBs use Byte 13.

5

Commands

5

Commands

5.1. General

As an initiator, the 721 supports all SCSI commands for all SCSI devices (see your device manual for specific command information). The 721 also supports five controller-specific commands (see Sections 5.3. through 5.7.).

5.2. SCSI Command Codes

Table 5-1 and Table 5-2 list the SCSI Group 0 and Group 1 command codes. The directive (Dir.) column defines all the SCSI commands that transfer data between system memory and the target device. You can also use vendor-unique commands that are not listed since the 721 transfers data according to the SCSI bus requests.

Key to Table 5-1 and Table 5-2:

721 Directive:

NO = No data transfer
RD = Read data from SCSI to system memory
WD = Write data from system memory to SCSI
RP = Read parameters from SCSI to system memory
WP = Write parameters from system memory to SCSI

SCSI Command Implementation Levels:

M = Mandatory
O = Optional
R = Reserved
V = Vendor-unique
E = Extended (required for self-configuring software)

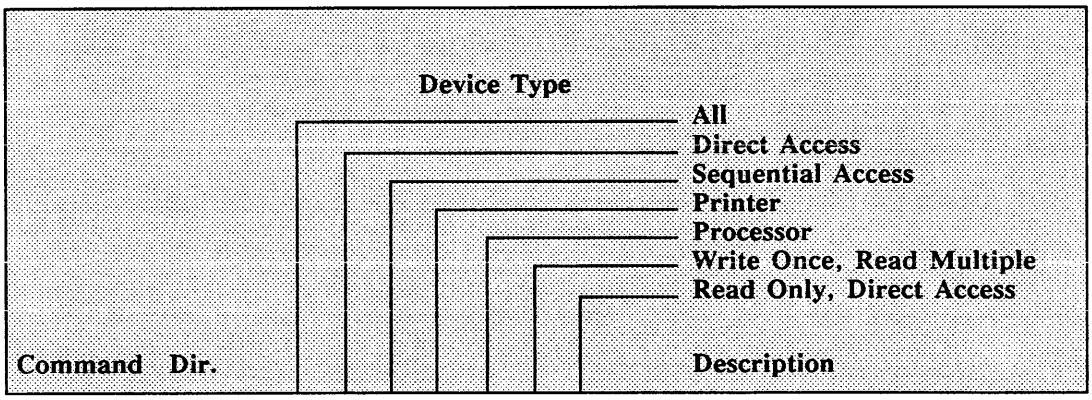
5.2.1. SCSI Group 0 Command Codes

Table 5-1. SCSI Group 0 Command Codes

Command	Dir.	All	Direct Access	Sequential Access	Printer	Processor	Write Once, Read Multiple	Read Only, Direct Access	Description
00	NO	O							Test Unit Ready
01	NO		O	M	V	V	O	O	Rezero/Rewind Unit
02		V							
03	RP	M							Request Sense
04	WP		M	R	O	V	R	R	Format Unit
05	RP		V	E	V	V	V	V	Read Block Limits
06		V							
07	WP		O	V	V	V	O	R	Reassign Blocks
08	RD		M	M	V	O	O	O	Read/Receive
09		V							
0A	WD		M	M	M	M	O	R	Write/Send
0B	NO/WD		O	O	O	V	O	O	Seek/Track Select; Slew & Print
0C-0E		V							
0F	RD		V	O	V	V	V	V	Read Reverse
10	NO		V	M	O	V	V	V	Wrt File Mks/Flush Print Buffer
11	NO		V	O	V	V	V	V	Space
12	RP	E							Inquiry
13	WT/NO		V	O	V	V	V	V	Verify
14	RD		V	O	O	V	V	V	Recover Buffered Data
15	WP		O	O	O	V	O	O	Mode Select
16	WP		O	O	O	V	O	O	Reserve Unit
17	NO		O	O	O	V	O	O	Release Unit
18	WP	O							Copy
19	NO		V	O	V	R	V	V	Erase
1A	RP		O	O	O	R	O	O	Mode Sense
1B	NO		O	O	O	R	O	O	Start-Load/Stop-Unload Unit
1C	RP	O							Receive Diagnostic Results
1D	WP	O							Send Diagnostic
1E	NO		O	O	R	R	O	O	Prevent/Allow Medium Removal
1F		R							

5.2.2. SCSI Group 1 Command Codes

Table 5–2. SCSI Group 1 Command Codes

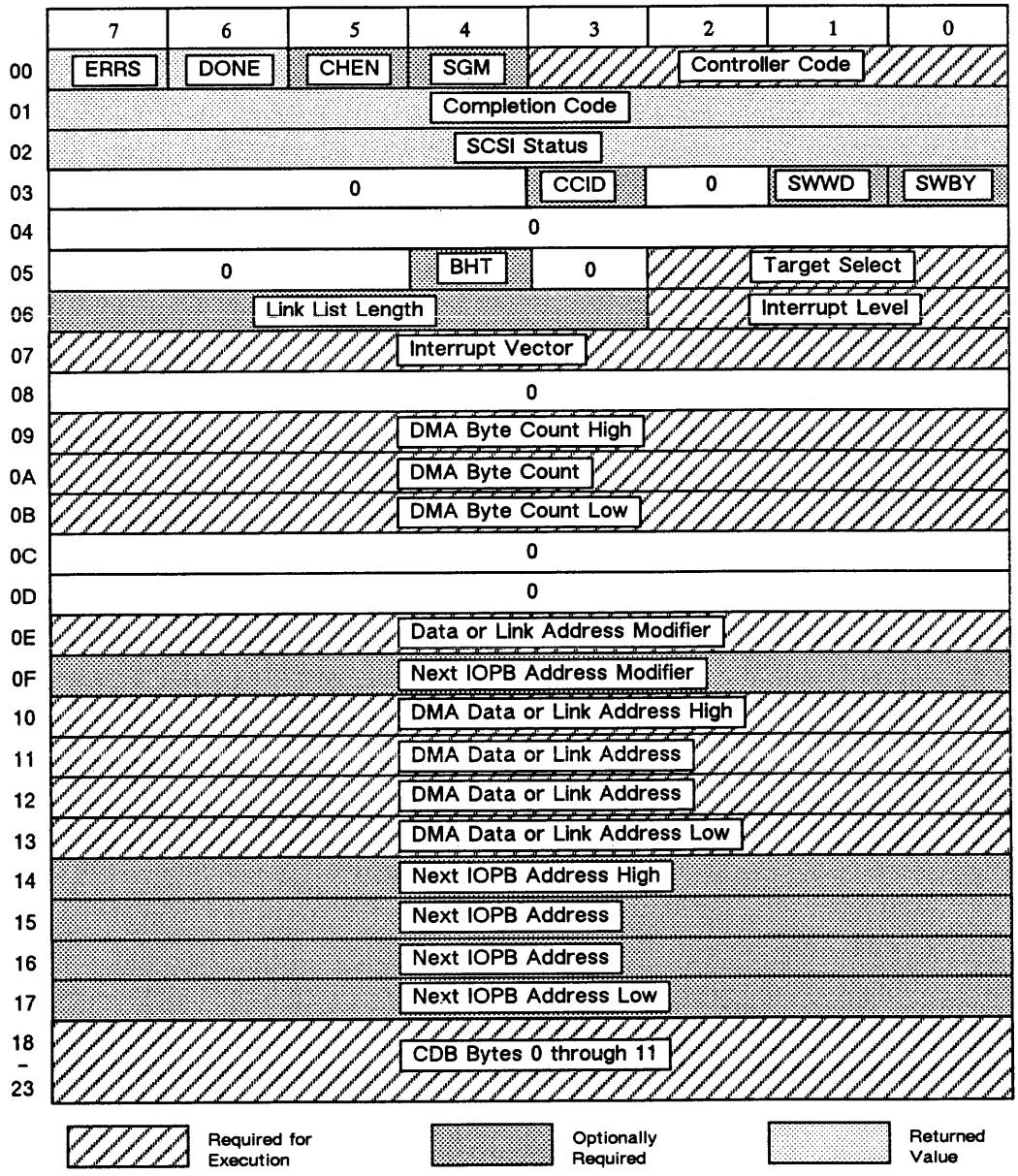


Command	Dir.	All	Direct Access	Sequential Access	Printer	Processor	Write Once, Read Multiple	Read Only, Direct Access	Description
20		V							
21									
22		V							
23		V							
24		V							
25	RP		E		E	E			Read Capacity
26		V							
27		V							
28	RD		E		M	M			Read
29		V							
2A	WD		E		M	M			Write
2B	NO		O		O	O			Seek
2C	V								
2D	V								
2E	WD		O		O	O			Write and Verify
2F	NO/WD		O						Verify
30	WP		O		O	O			Search Data High
31	WP		O		O	O			Search Data Equal
32	WP		O		O	O			Search Data Low
33	NO		O		O	O			Set Limits
34		R							
35		R							
36		R							
37		R							
38		R							
39	WP	O							Compare
3A	WP	O							Copy and Verify
3B		R							
3C		R							
3D		R							
3E		R							
3F		R							

5.3. Command Structure

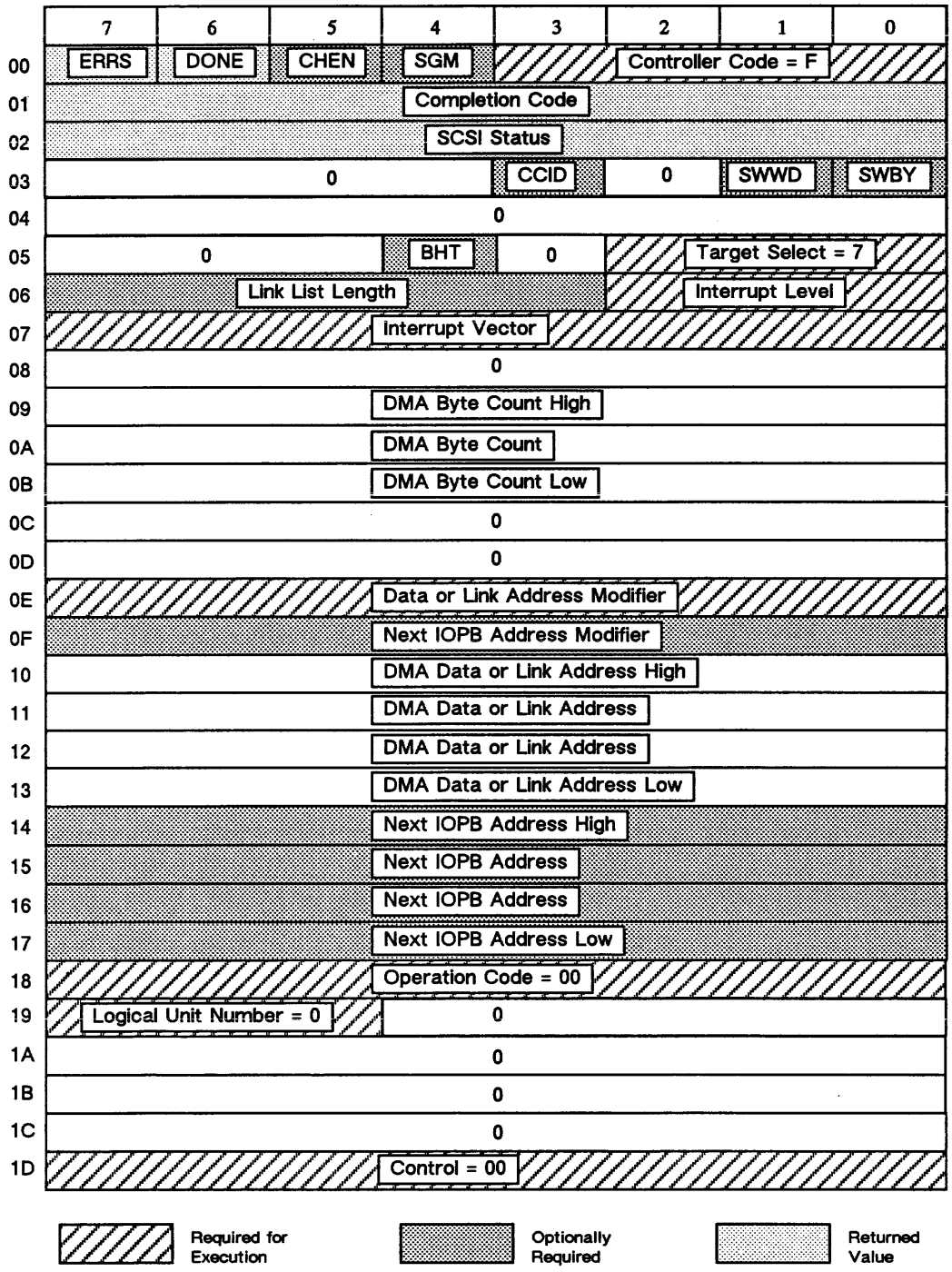
All 721 commands use the same IOPB structure. The following diagram shows which bytes the 721 absolutely requires for command execution, which bytes are optional, and which bytes it returns after execution.

Each IOPB is 36-bytes long. Reserving all 36 bytes in memory maintains IOPB integrity.



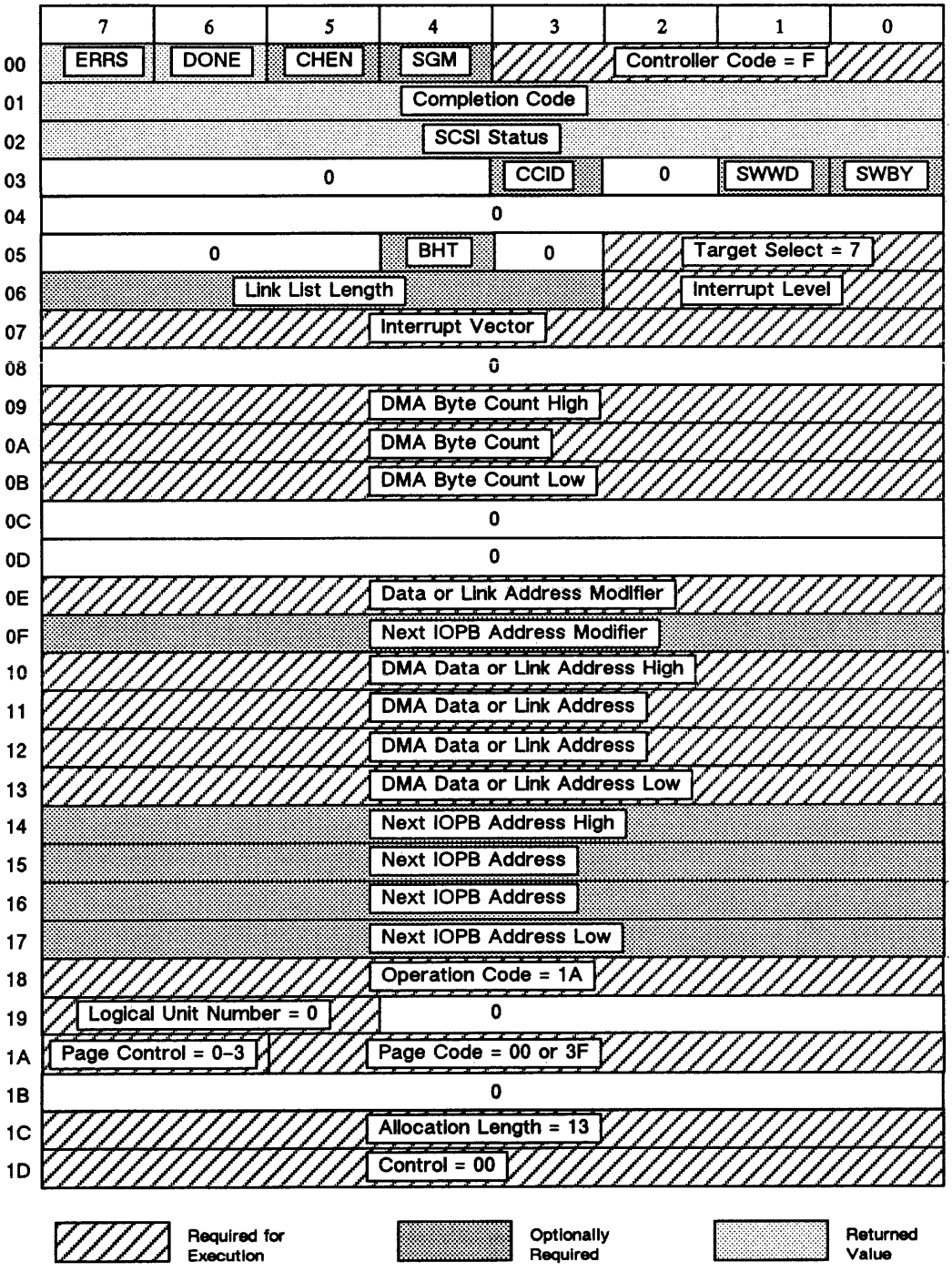
5.4. No Operation

This is an implementation of the SCSI Test Unit Ready command. Addressing the 721's target ID (seven) and logical unit zero executes a No Operation (NOP) command.



5.5. Read Controller Parameters

This is a vendor-unique implementation of the SCSI Mode Sense command. Addressing the 721's target ID (seven) and logical unit zero executes a Read Controller Parameters command. The parameter list is vendor-unique (see Section 5.5.2.).



5.5.1. Read Controller Parameters CDB

5.5.1.1. Logical Unit Number

Always address the 721 as logical unit zero.

5.5.1.2. Page Control

There are four valid page control values:

- 0H = Report Current Values
- 1H = Report Changeable Values
- 2H = Report Default Values
- 3H = Report Saved Values (same as default)

5.5.1.3. Page Code

There are two valid page code values:

- 00H = Report Page Zero
- 3FH = Report All Pages (returns only page zero)

5.5.1.4. Allocation Length

An allocation length of 13H or greater returns 19 bytes of mode sense data (all the 721's information). An allocation length of less than 13H returns that number of mode sense bytes.

5.5.2. Parameter List

All the values listed in Table 5-3 are expressed in hexadecimal. The *X* represents a programmable value in the Read Controller Parameters command.

5.5.2. Parameter List (continued)

Table 5-3. Read Controller Parameters List

Byte	Description	Page Control = 0	1	2	3
Header					
00	Sense Data Length	13	13	13	13
01	Vendor-unique Medium Type	80	80	80	80
02	Reserved	00	00	00	00
03	Block Descriptor Length	00	00	00	00
Page 0					
04	Page Code (Vendor-unique = 0)	00	00	00	00
05	Page Length	0D	0D	0D	0D
06	Controller Parameters	XX	FF	00	00
07	Throttle Dead Time and ROR	X0	D0	00	00
08	DMA Throttle	XX	FF	00	00
09	Sequential Device Types	XX	FF	00	00
0A	Host BDID	0X	07	07	07
0B	Inhibit Probe for Sync	XX	FF	00	00
0C-0D	Reserved	00	00	00	00
0E	EPROM Number High	NN	00	NN	NN
0F	EPROM Number Low	NN	00	NN	NN
10	Firmware Release	NN	00	NN	NN
11	Firmware Revision	NN	00	NN	NN
12	Firmware Subrevision	NN	00	NN	NN
13	Reserved	00	00	00	00

5.5.2.1. Controller Parameters

7	6	5	4	3	2	1	0
Auto-update	Transfer Mode	Disable Timers	SCSI Parity	Enable DMA Timeout	Non-privileged Request Mode	AIO Response Time	

5.5.2.1. Controller Parameters (continued)

Bit	Mnemonic	Description
7	AUD	**Auto-update:** When set, the 721 updates the IOPB to the transfer's ending parameters; it updates the DMA count data address after completing the transfer or detecting an error. When clear, the 721 only updates the IOPB if an error occurs. The update includes the DMA count and the final data address plus one transfer. Default: *set*.
6	TMOD	**Transfer Mode:** When set, the 721 executes data transfers in longword mode. When clear, it executes transfers in word mode. IOPB transfers are always in word mode. If a transfer starts on an improper address boundary, the 721 transfers a byte and/or a word, as necessary to align boundaries, and continues the transfer in the selected mode. The 721 may end the transfer with a byte and/or a word. Default: *clear*.
5	DT	**Disable Timers:** Setting DT disables global timeouts. Clearing DT enables global timeouts. Default: *clear*.
6	SP	**SCSI Parity:** When set, the SPC checks/generates parity on SCSI data. When clear, the 721 ignores SCSI parity. Default: *clear*.
3	EDT	**Enable DMA Timeout:** When set, the 721 enables an on-board DMA bus error timer. When clear, the 721 relies on the external VMEbus transfer timer. The timeout period is one millisecond. Default: *clear*.
2	NPRM	**Non-privileged Request Mode:** When set, the 721 responds to address modifiers 2DH and 29H. When clear, the 721 only responds to 2DH. The VMEbus Specification describes address modifiers. Default: *set*.
1-0	AIOR	**AIO Response Time:** This is the maximum time from setting AIO to the time the 721 clears it. The shorter the response time, the greater the 721 overhead. Default: *00*.

Table 5-4. AIO Response Times

Value	Time
00	100 microseconds (µs)
01	75 µs
02	62 µs
03	50 µs

5.5.2.2. Throttle Dead Time and Release on Request

7	6	5	4	3	2	1	0
Throttle Dead Time		Reserved	Release on Request	Reserved			

Bit	Mnemonic	Description
7–6	TDT	**Throttle Dead Time:** TDT selects one of four minimum time periods that determines the time the 721 remains off the bus between throttle bursts (see Section 8.4.). Default: *00*.
5		**Reserved.**
4	ROR	**Release on Request:** When set, the 721 releases the bus at the request of other bus masters; otherwise, it continues with the next throttle burst. The 721 monitors the bus request lines and releases *Bus Busy* only if another bus request is pending. It completes the specified throttle burst before releasing the bus due to a pending request. When clear, the 721 releases the bus at the end of each throttle burst and rearbitrates if more data transfers are pending. Default: *clear*.
3–0		**Reserved.**

5.5.2.3. DMA Throttle

Bits 0 through 7 are the *Throttle* (THRO) bits. The throttle is the maximum number of transfers allowed each time the 721 becomes bus master. The throttle value determines the maximum DMA burst length for both data and IOPB DMA transfers. This byte allows a throttle setting from 1 to 256. Default: *10H*.

Table 5–5. Throttle Values

Setting	Transfer Count
0	256
1	1
2	2
3	3
:	:
255	255

5.5.2.4. Sequential Device Types

The timeouts for direct access and sequential devices are different. The bit settings indicate the device type so the 721 can implement the appropriate timeout.

Each bit position represents a target device, i.e., bit 7 represents target 7, bit 6 represents target 6, etc. When bit *n* is set, the target *n* is sequential; when clear, the target is direct access. Default: *clear*.

5.5.2.5. Host BDID

By changing the values of bits 0 through 2 during a Mode Select/Write Controller Parameters (CCID *must* be set), you can change the 721's SCSI ID. Default: *seven*.

5.5.2.6. Inhibit Probe for Synchronous Transfers

Each bit position represents a target device, i.e., bit 7 represents target 7, bit 6 represents target 6, etc. When bit *n* is set, the 721 will not issue a synchronous transfer request message; when clear, the 721 will issue a synchronous transfer request message. Default: *clear*.

5.5.2.7. EPROM Part Number

The 721 returns a portion of the EPROM part number on a Read Controller Parameters command. The four nibbles in these two bytes refer to the part number's last four digits. For example, if the part number is 2307, Byte E is 23H and Byte F is 07H.

5.5.2.8. Firmware Release Level

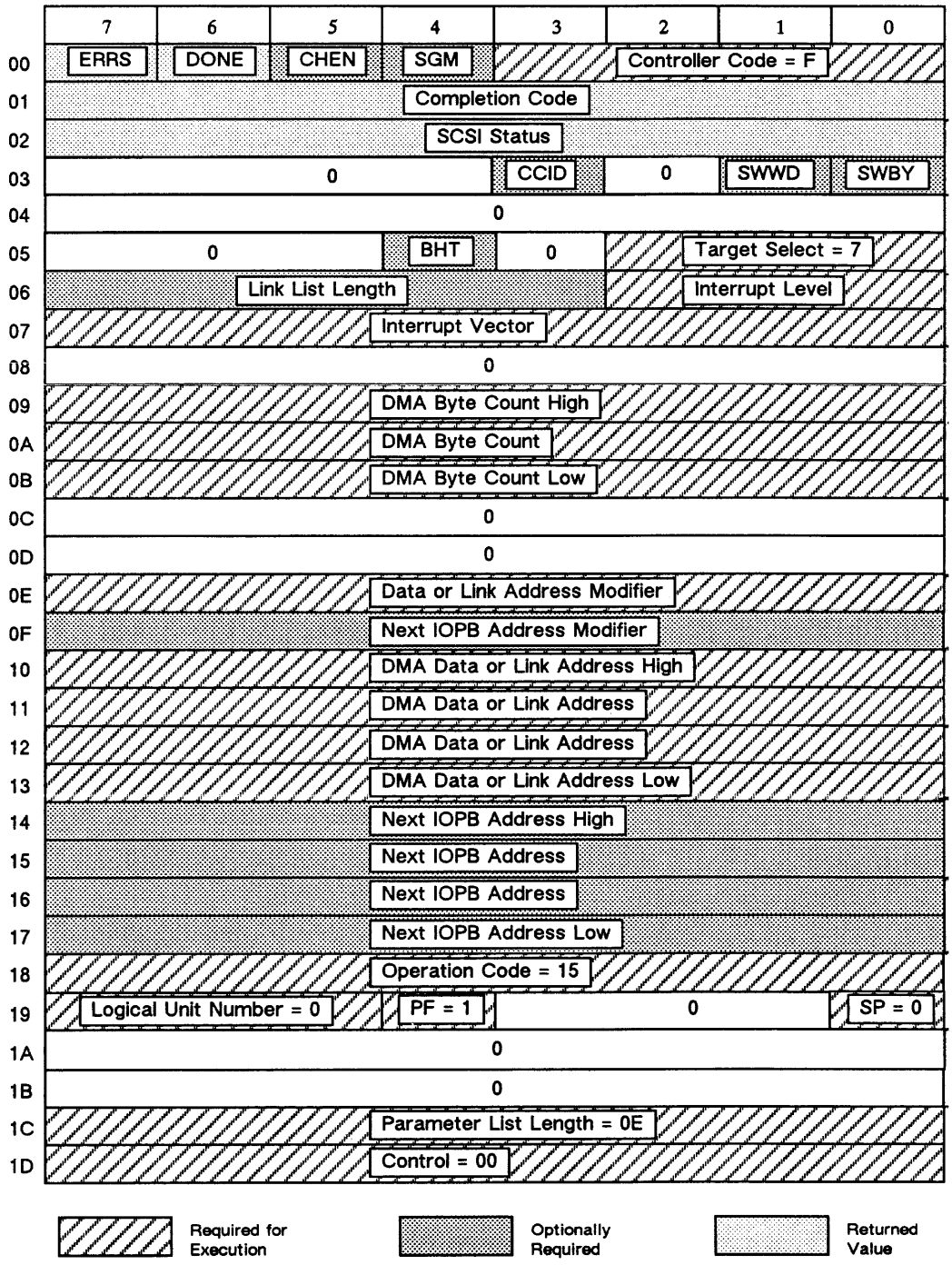
Byte 10 contains the release level of the 721 firmware.

5.5.2.9. Firmware Revision Level

Byte 11 contains the revision level of the 721 firmware; Byte 12 contains the subrevision level.

5.6. Write Controller Parameters

This is a vendor-unique implementation of the SCSI Mode Select command. Addressing the 721's target ID (seven) and logical unit zero executes a Write Controller Parameters command. The parameter list is vendor-unique (see Section 5.6.2.).



5.6.1. Write Controller Parameters CDB

5.6.1.1. Page Format

Setting *Page Format* (PF) indicates the data sent to the 721 complies with the page format.

5.6.1.2. Save Parameters

Clear *Save Parameters* (SP); the 721 cannot permanently save any parameters.

5.6.1.3. Parameter List Length

A paramter list length of 0EH delivers the complete mode select parameter list. A paramter list length of less than 0EH delivers that number of bytes; the current settings of the remaining parameters remains unchanged.

5.6.2. Parameter List

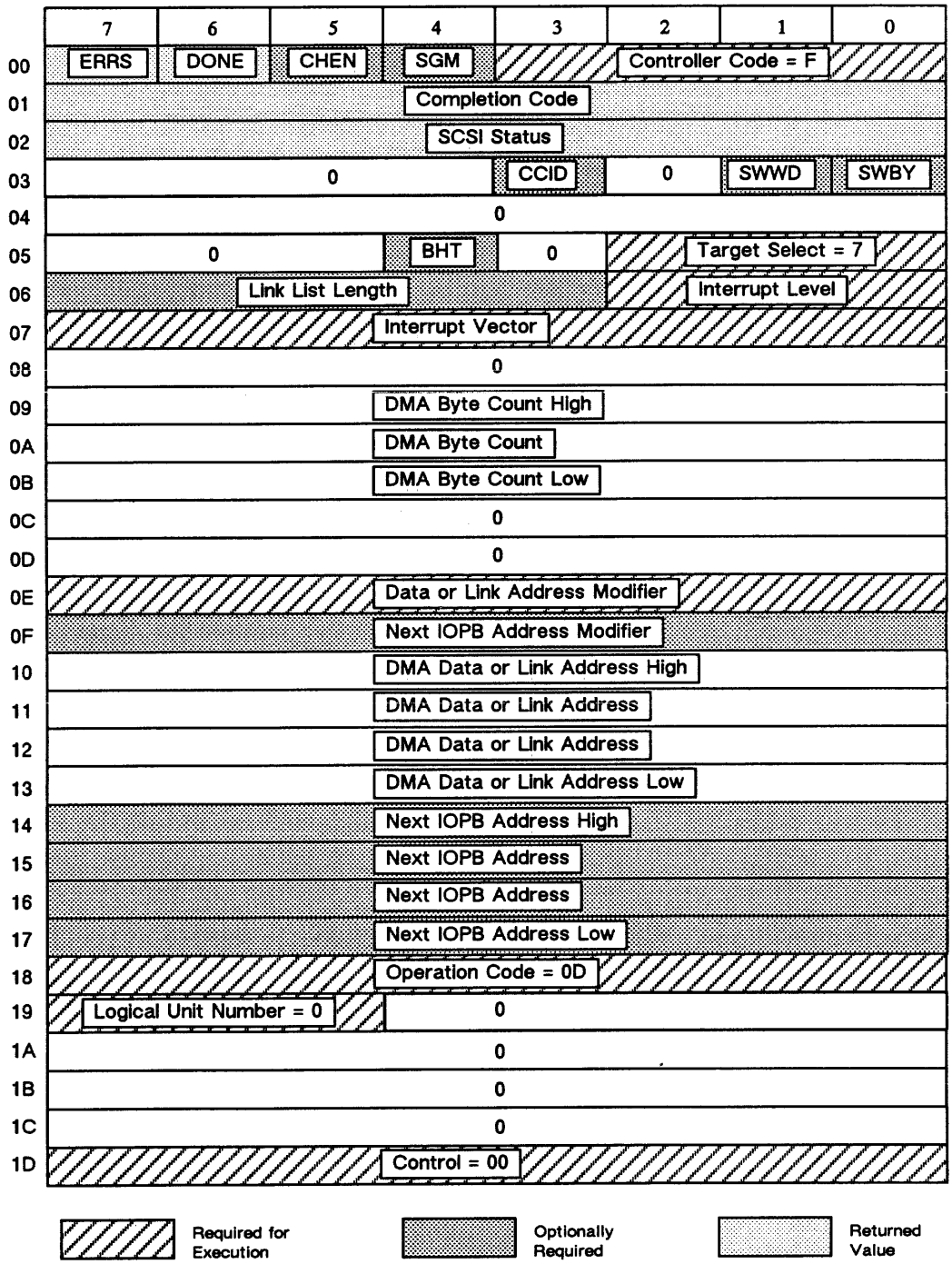
Write Controller Parameters and Read Controller Parameters use a similar parameter list. Sections 5.5.2.1. through 5.5.2.9. describe the bytes that comprise the parameter list. All the values listed in Table 5–6 are expressed in hexadecimal; the *X* represents a programmable value in the Write Controller Parameters command.

Table 5–6. Write Controller Parameters List

Byte	Description	Value
Header		
00	Reserved	00
01	Vendor-unique Medium Type	80
02	Reserved	00
03	Block Descriptor Length	00
Page 0		
04	Vendor-unique Page Zero	00
05	Page Length	08
06	Controller Parameters	XX
07	DMA Dead Time and ROR	XX
08	DMA Throttle	XX
09	Sequential Device Types	XX
0A	Host BDID	0X
0B	Inhibit Probe for Sync	XX
0C–0D	Reserved	00

5.7. SCSI Bus Reset

The 721 asserts the *RST* line on the SCSI bus. This vendor-unique command clears all SCSI devices from the bus.



6

Error Processing

6

Error Processing

6.1. General

The IOPB completion code, *Error Summary* (ERRS) bit, *Fatal Error* (FERR) bit, and Fatal Error Register represent the 721's status after command execution. FERR indicates the transfer failed and the 721 requires a *Controller Reset* before continuing (the IOPB address is not valid). ERRS affects only a specific IOPB. The completion code informs software that the 721 successfully completed a command, failed to complete a command, or encountered and corrected a problem with one of its internal recovery procedures.

The 721 sets FERR, ERRS, the completion code, and the Fatal Error Register. The SCSI target supplies the SCSI status after completing a command. A *good* status requires no further action. A *check condition* status requires that the host issue a Request Sense command (which gathers more information from the target regarding the failure).

6.2. SCSI Request Sense Data

A target can implement two formats for sense data: extended or non-extended. The vendor-unique *Error Class* field determines the sense data's format. Error Classes 0 through 6 use the non-extended sense data format. The *Address Valid* (AdVal) bit indicates that the *Logical Block Address* field contains valid information pertaining to the vendor-unique *Error Code* field.

	7	6	5	4	3	2	1	0
00	AdVal	Error Class			Error Code			
01	Vendor-unique				Logical Block Address (MSB)			
02	Logical Block Address							
03	Logical Block Address (LSB)							

Figure 6-1. Non-extended Sense Data Format

6.2. SCSI Request Sense Data (continued)

Error Class 7 and Error Code 0 use the extended sense data format (see Figure 6-2). The *Information Byte* field is not defined if *Valid* is clear. If *Valid* is set, the *Information Byte* field contains the following information:

1. The unsigned logical block address associated with the sense key for direct access, write once-read multiple and read only direct access devices.

2. The difference between the requested length minus the actual length in either bytes or blocks, as determined by the command, for sequential access, printer, and processor devices (negative values are indicated by two's compliment notation).

3. The difference between the requested number of blocks minus the actual number of blocks copied or compared for the current segment descriptor of a Copy, Compare, or Copy and Verify command.

The *Segment Number* contains the number of the current segment descriptor if the extended sense is responding to a Copy, Compare, or Copy and Verify command. SCSI supports up to 256 segments beginning with segment zero.

The *Filemark* bit indicates the current command detected a file mark. Only sequential access devices use *Filemark*.

	7	6	5	4	3	2	1	0
00	Valid	Error Class = 7			Error Code = 0			
01	Segment Number							
02	Filemark	EOM	ILI	0	Sense Key			
03	Information Byte (MSB)							
04	Information Byte							
05	Information Byte							
06	Information Byte (LSB)							
07	Additional Sense Length (n)							
08 – n+7	Additional Sense Bytes							

Figure 6-2. Extended Sense Data Format

6.2. SCSI Request Sense Data (continued)

The *End of Medium* (EOM) bit indicates that an *end of medium* condition (end of tape [EOT], beginning of tape [BOT], out of paper, etc.) exists on a sequential access or printer device. For sequential access devices, EOM indicates that the unit is at or past the early warning EOT in the forward direction, or that the target could not complete the command because it detected BOT in the reverse direction. Direct access devices do not use EOM; they report access attempts beyond EOM as an *Illegal Request* via the *Sense Key* field (which provide target status information; see Section 6.2.1.).

The *Incorrect Length Indicator* (ILI) bit indicates that the requested logical block length did not match the logical block length of the data on the medium.

The *Additional Sense Length* specifies the number of *Additional Sense Bytes* that follow. If the CDB's allocation length is too small to transfer all of the *Additional Sense Bytes*, the target does not adjust the *Additional Sense Length* to reflect the truncation.

The *Additional Sense Bytes* hold command- and peripheral device-specific data (or both) that further define the nature of the *check condition* status. The Copy, Compare, Copy and Verify, and Search Data commands define a standard purpose for some of these bytes. Except where otherwise noted, the *Additional Sense Bytes* are vendor-unique.

6.2.1. Sense Key Descriptions

Key(H)	Description
0	*No Sense:* The target has no specific *Sense Key* information for the designated logical unit. This is true for a successful command or a command with a *check condition* status because *Filemark*, EOM, or ILI is set to one.
1	*Recovered Error:* The target successfully completed the last command with some recovery action. The *Additional Sense* and *Information Byte* fields may have more information.
2	*Not Ready:* The target cannot access the selected logical unit; operator intervention may be required to correct this condition.
3	*Medium Error:* The target terminated the command with a *non-recovered error* condition that was probably caused by a flaw in the medium or an error in the recorded data.

6.2.1. Sense Key Descriptions (continued)

Key(H)	Description
4	*Hardware Error:* The target detected a fatal hardware failure (i.e., target controller or device failure, parity error, etc.) during command processing or the self test.
5	*Illegal Request:* There was an illegal parameter in the CDB or in the additional parameters supplied as data for some commands (Format Unit, Search Data, etc.). If the target detects an invalid parameter in the CDB, it terminates the command without altering the medium. If the target detects an invalid parameter in the additional parameters supplied as data, it may have already altered the medium.
6	*Unit Attention:* The removable medium may have been changed or the target has been reset (see the ANSI Specification for more information).
7	*Data Protect:* A command that reads or writes the medium was attempted on a block that is protected from this operation. The target does not execute the read or write.
8	*Blank Check:* A write once, read multiple or sequential access device encountered a blank block while reading, or a write once, read multiple device encountered a non-blank block while writing.
9	*Vendor-unique:* Reports vendor-unique conditions.
A	*Copy Aborted:* The target aborted a Copy, Compare, or Copy and Verify command because of an error in the source or destination device (or both).
B	*Aborted Command:* The target aborted the command. The host may recover from the error by trying the command again.
C	*Equal:* A Search Data command satisfied an equal comparison.
D	*Volume Overflow:* A buffered peripheral device reached EOM and data remains in the buffer that was not written to the medium. A Recovered Buffered Data command can read the unwritten data from the buffer.
E	*Miscompare:* The source data did not match the data read from the medium.
F	*Reserved.*

6.3. The Completion Code

The 721 posts a completion code in IOPB Byte 1. A completion code is only valid if *Done* is set. Table 6–1 lists the completion codes; all codes not listed in this table are reserved. The following subsections describe these codes along with any required corrective action.

Table 6–1. Summary of Completion Codes

Action	Code (Hex)	Description
No Action – Status Only	00	Successful Completion
Non-retryable Programming Errors	11	Illegal Logical Unit Address
	12	Mode Sense or Mode Select Error
	14	Illegal Command
	1C	Illegal Scatter/Gather Length
	1E	Next IOPB Address Alignment Error
	1F	Scatter/Gather Address Alignment Error
	21	Illegal Black Hole Transfer Address
	22	Illegal Priority IOPB
	23	DMA Count Size Error
Hard Errors – Retry	41	Reselection Timeout
	42	Device Selection Timeout
	43	Operation Timeout
	44	FDMAC Timeout
	45	Illegal Address Boundary
	46	FIFO Buffer Parity Error
	4A	FDMAC Error
	4B	VMEbus Error
Hard Error – Reset and Retry	60	Target Returned Invalid SCSI Status
	62	Residual Error
Fatal Hardware Errors	71	Firmware Failure
	72	Synchronous Protocol Error
	73	Illegal Phase Change During Transfer
	74	Synchronous Data Transfer Request Error
	75	Illegal Message Reject
	76	Drive Interface Fault
	77	Drive Requested Data after Count Zero
Miscellaneous Errors	81	IRAM Checksum Failure
	83	IOPB Aborted by Error

6.3.1. Completion Code Descriptions

6.3.1.1. No Action - Status Only

The following completion code usually requires no action; the 721 returns it for status only.

Code(H)	Description
00	*Successful Completion:* The 721 completed the IOPB without error.

6.3.1.2. Non-retryable Programming Errors

This group of errors is usually encountered while debugging drivers; they should not occur in a normal operating system environment.

Code(H)	Description
11	*Illegal Logical Unit Address:* The host specified a logical unit address greater than seven.
12	*Mode Sense or Mode Select Error:* The allocation length for a floppy command was incorrect.
14	*Illegal Command:* The command code in the CDB is invalid for the controller or target command.
1C	*Illegal Scatter/Gather Length:* The linked list specified a number of words to transfer that does not agree with the amount of data contained in the requested number of sectors for transfer.
1E	*Next IOPB Alignment Error:* The Next IOPB address did not start on a 16-bit boundary; the 721 does not execute the Next IOPB.
1F	*Scatter/Gather Address Alignment Error:* A scatter/gather address did not start on a 16-bit boundary.
21	*Illegal Black Hole Transfer Address:* During a black hole transfer, the data address did not start on a word boundary when the 721 was in word mode, or it did not start on a longword boundary when the 721 was in longword mode.

6.3.1.2. Non-retryable Programming Errors (continued)

Code(H)	Description
22	*Illegal Priority IOPB:* Only Request Sense and controller commands can be priority IOPBs.
23	*DMA Count Size Error:* The DMA count was greater than 16 megabytes.

6.3.1.3. Hard Errors – Retry

These errors indicate the transfer failed; retry the operation. If several retries fail, you must intervene or the operating system may crash.

Code(H)	Description
41	*Reselection Timeout:* The target did not reconnect with the 721 within the device-dependent time limit.
42	*Device Selection Timeout:* The device did not respond to the 721 within the 250 ms timeout.
43	*Operation Timeout:* The 721 did not complete the IOPB within the two second timeout period.
44	*FDMAC Timeout:* The FDMAC did not complete its task within the 1 ms time limit. Possibly, host memory did not respond in time.
45	*Illegal Address Boundary:* Following a reselect, the target tried to resume a data transfer to/from an odd address with SWBY set (see Section 4.2.4.).
46	*FIFO Buffer Parity Error:* The transfer failed; the 721 detected a FIFO buffer parity error.
4A	*FDMAC Error:* The FDMAC failed during the self test.
4B	*VMEbus Error:* The VME *BERR** signal was asserted while the 721 was bus master (see the VMEbus Specification).

6.3.1.4. Hard Error - Reset and Retry

This error indicates the transfer failed.

Code(H)	Description
60	*Target Returned Invalid SCSI Status:* The target detected a problem during command processing. The 721's reaction depends on the returned SCSI status.
62	*Residual Error:* The number of bytes DMAed differs from the number of bytes requested.

6.3.1.5. Fatal Hardware Errors

These errors indicate the hardware failed. Manual intervention or a *Controller Reset* may be the only recovery approaches that work.

Code(H)	Description
71	*Firmware Failure:* An unexpected IOPB DMA overflow occurred (fatal during write operations).
72	*Synchronous Protocol Error:* The SCSI chips are incompatible.
73	*Illegal Phase Change During Transfer:* Device changed transfer phase illegally.
74	*Synchronous Data Transfer Request Error:* The target does not respond to a synchronous data request with the correct information, i.e., data rate.
75	*Illegal Message Reject:* The target rejected a valid message, i.e., an identify message.
76	*Drive Interface Fault:* There is a problem with the acknowledge/request handshake, i.e., the drive does not remove the request.
77	*Drive Requested Data after Count Zero:* The DMA count in the IOPB did not match the transfer count in the CDB.

6.3.1.6. Miscellaneous Errors

Code(H)	Description
81	*IRAM Checksum Failure:* The calculated checksum from the IRAM and its stored value did not match during the self test. A soft bit in the IRAM, static, or probing the board with the power on can cause this error.
83	*IOPB Aborted by Error:* The 721 aborted the IOPB because a previous command returned a *check condition* status. It discards all subsequent commands, having non-zero interrupt levels, for the affected target/LUN until it receives a Request Sense or Test Unit Ready command.

6.4. Fatal Error Codes

If a fatal error occurs, the 721 sets FERR and posts the error code in the Fatal Error Register. The following error codes appear only in the Fatal Error Register. The only way to clear a fatal error is by issuing a *Controller Reset* (CRST). All codes not listed are reserved.

Code(H)	Description
E1	*IRAM/8031 INTRAM Self Test Failure:* The 721 writes the IRAM/8031 INTRAM with an incrementing data pattern, then reads it with a decrementing pattern. An error indicates a bad IRAM.
E2	*SCSI Cable Installed Backwards:* The SCSI cable is connected backwards on either the 721 or one of the devices.
E3	*SPC Register Self Test Failure:* The 721 writes the SPC registers and then reads them. An error indicates a bad SPC.
E5	*FDMAC Register Self Test Failure:* The 721 writes the FDMAC registers and then reads them. An error indicates a bad FDMAC.
E6	*REGCEL Self Test Failure:* There is a problem with the REGCEL chip.

6.4. Fatal Error Codes (continued)

Code(H)	Description
E8	*FIFO Self Test Failure:* The 721 fills the FIFO with sequential data and then reads it. An error indicates a problem with the FIFO.
F1	*IOPB DMA Fatal:* The 721 did not complete the DMA within the prescribed timeout period. The memory could be defective or not present, or the 721 may not have been able to become bus master.
F2	*IOPB Address Alignment*: The IOPB address did not start on a 16-bit boundary. Change the address and retry.
F3	*Firmware Error*: Flag settings or counter values are inconsistent with the firmware routines; the 721 cannot DMA the appropriate error status. The 721's state is indeterminate. Issue a *Controller Reset*.
F5	*Illegal Maintenance Mode Test Number*: The command is invalid.
F6	*Abort Message Rejected*: The 721 sent an *abort* message to the drive after an IOPB timed out and the drive responded with *message reject*. Issue a *Controller Reset* and a *SCSI Bus Reset*.
F9	*Illegal SCSI Transfer Phase*: The SCSI bus signals indicate some phase other than command, message, selection/reselection, status, information transfer, or bus free.
FC	*Global Timeout Error*: The operation did not complete within the two minute timeout period.

7

Programming Tutorial

7

Programming Tutorial

7.1. General

This section includes flow charts that illustrate the basic 721 programming procedures.

7.2. Programming the Controller

The first programming step involves setting up the 721 so that the system driver can execute Inquiry, Mode Sense, Mode Select, Read Controller Parameters, and Write Controller Parameters commands.

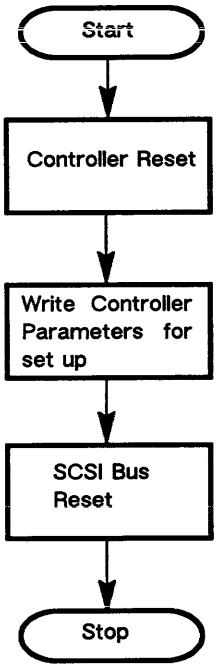


Figure 7-1. Initial Controller Values

7.3. Programming the Controller and the Driver

This sequence programs the 721 on a per device basis and sets up the block size between the software driver and the device.

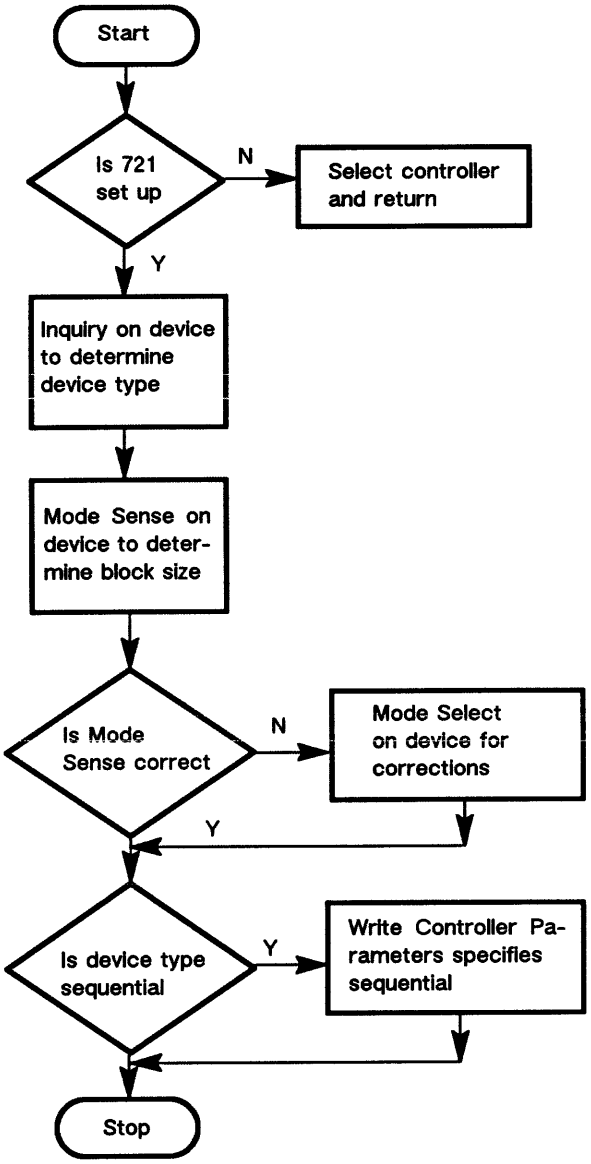


Figure 7-2. Programming the Controller and the Driver

7.4. Executing a Read or Write Operation

This flow chart illustrates a read or write operation.

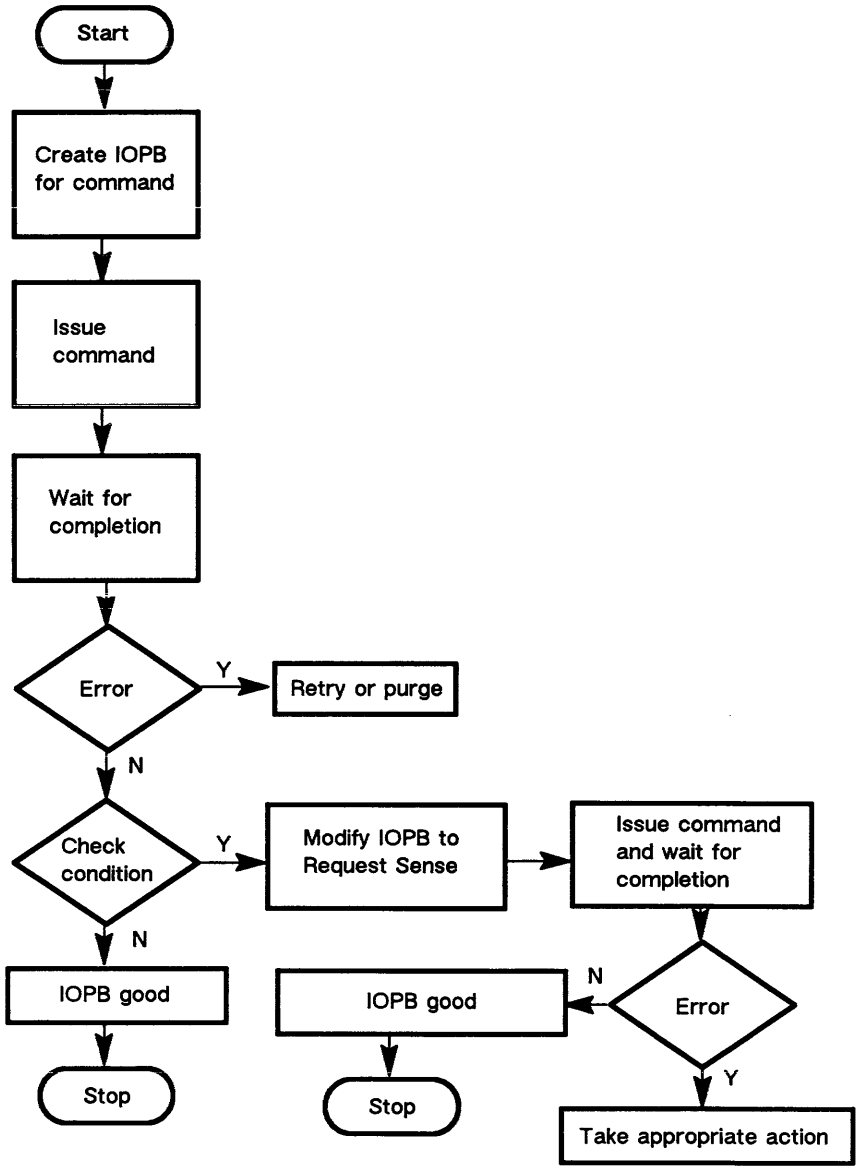


Figure 7-3. Read/Write

8

Special Functions

8

Special Functions

8.1. General

This section describes how to implement the 721's special functions.

8.2. Maintenance Mode

Firmware supports a non-IOPB driven maintenance mode. Scripts containing maintenance mode commands are useful debugging tools. They allow you to perform basic testing within the 721 by setting control bits in the Control and Status Register (CSR) and entering the desired test number and data through the address registers. Maintenance mode also provides a window through which you can examine or modify internal registers.

8.2.1. Register Use in Maintenance Mode

Table 8-1 lists the registers in maintenance mode. The CSR controls maintenance mode operations.

Table 8-1. Register Use in Maintenance Mode

Register	Description
1	Test Number or Function Code
3	Input Address Low
5	Input Address High
7	Input Data Byte (If Required)
9	Output Data Byte (If Required)
B	Control and Status Register
D	Fatal Error Register

8.2.2. Maintenance Mode Protocol

8.2.2.1. Entering the Maintenance Mode

First, familiarize yourself with the CSR; *Busy* does not have to be clear before entering maintenance mode. Simultaneously set the *Maintenance Mode* (MM) and *Add IOPB* (AIO) bits. The 721 responds by setting the *Remove IOPB* (RIO) and *AIO Pending* (AIOP) bits. Then set the *Clear RIO* (CRIO) bit. The 721 sets the *Maintenance Mode Active* (MMA) bit and clears AIOP.

8.2.2.2. Testing in the Maintenance Mode

Xylogics has developed a series of diagnostics that test the 721 microprocessor, ASICs, and RAM. For example, the Register Test can verify the operation of the 721 registers:

Load arbitrary bit patterns into all the maintenance mode registers, except the CSR (see Table 8–1). Then simultaneously set RT, MM, and AIO. After the 721 clears AIOP, the host can read the registers and compare their contents with the patterns written. *Busy* remains set; setting RT clears *Busy*.

Contact Xylogics for information regarding additional maintenance mode functions.

8.2.2.3. Exiting the Maintenance Mode

To exit the maintenance mode, the host simultaneously sets AIO and clears MM. The 721 sets AIOP and RIO, and clears *Busy* if it was set. Then the host sets CRIO.

8.3. Scatter/Gather

Scatter/gather reduces software's workload in mapped memory systems. Data that is contiguous on the SCSI device can be transferred to or from pages and page fragments scattered throughout the physical address space. Pages can contain up to 64K bytes, but must be an even length and start on a word boundary. A scatter/gather IOPB can service up to 32 such pages.

8.3.1. Scatter/Gather Link List

The *DMA Data or Link Address* in IOPB Bytes 10 through 13 points to a list of DMA page descriptors. Each 8-byte descriptor includes a byte count field and an address field, and transfers one page or page fragment. The list can have up to 32 descriptors.

The *Link List Length* in IOPB byte 6 must contain the number of descriptors in the list; a value of zero indicates the link list has 32 descriptors. The *DMA Byte Count* in IOPB Bytes 9 through B must contain the sum of the page descriptors' byte count fields. See Table 8-2 and Table 8-3.

Table 8-2. Scatter/Gather Link List

Link Number	Byte	Description
1	00-01	Byte Count (Multiples of 2)
	02	Reserved
	03	Data Address Modifier
	04-07	Data Address (Word boundaries only)
2	08-09	Byte Count
	:	
	:	
n	xx	

Table 8-3. Link List Field Values

Link List Length	Decimal Equivalent
0	32
1	1
2	2
:	:
9	9
A	10
B	11
:	:
1E	30
1F	31

8.3.2. Setting Up a Scatter/Gather Transfer

Elements of memory descriptors comprise the link list. Each element describes the starting address and the length, in bytes, of the memory block. The sum of the byte counts of all the elements in the link list must equal the SCSI logical block count times the block size (in bytes); this sum must appear in IOPB Bytes 9 through B.

The IOPB and link list in Figure 8-1 illustrate a read transfer to 6 blocks of memory. The block size in this case is 528-bytes per block; we are transferring 3 blocks of information. The 721 transfers the first 16 data bytes from each block to a separate buffer. It scatters the bulk of the data, 512-bytes per block, into memory as 3 blocks having 512 bytes each. Set SGM and execute the IOPB in Figure 8-1.

8.3.3. 721 Operation

The 721 proceeds as if doing a normal read until it starts the data transfer into memory. The contents of the link list controls the DMA processor. It gives the processor the byte count and address for each element on the list. The processor takes the data out of the FIFO and transfers it to memory as described in each element on the list.

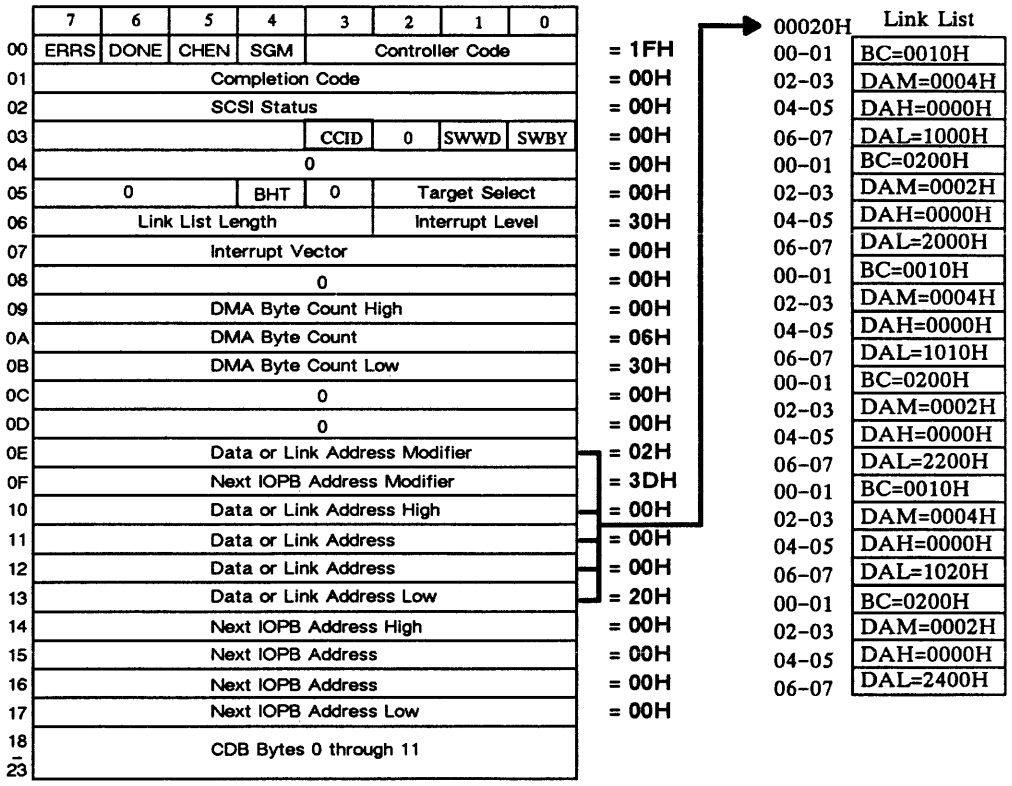


Figure 8-1. Scatter/Gather Transfers

8.4. IOPB DMA Throttle/Throttle Dead Time

The 721 always transfers IOPBs in word mode; it uses the latest specified values for the throttle and throttle dead time.

Host software can set the throttle dead time (TDT) field in the controller parameters IOPB. This value defines the time that the 721 waits before attempting to regain control of the bus between throttle bursts. There are four valid TDT values (see Table 8–4). Default: *zero*.

Table 8–4. Throttle Dead Time Values

TDT Value	Time
0	0 microseconds
1	3.2 microseconds
2	6.4 microseconds
3	12.8 microseconds

8.5. Black Hole Transfers

The normal DMA mode increments the bus address for each transfer so that the data is put into contiguous memory space. During black hole transfers, the 721 does not increment the bus address between each data transfer. Any transfer that DMAs data to a permanent memory location should have BHT set in IOPB Byte 5. The data address must be properly aligned: word aligned for word transfers and longword aligned for longword transfers.

8.6. Block Mode Transfers

Block mode reduces data transfer times by allowing a DMA device to use one memory address strobe for up to 256 bytes. Each time the transfer crosses a 256-byte memory address boundary, the device generates another address and address strobe. Block mode does not affect DMA throttling. IOPB DMA can also occur in block mode, but it is not practical since the IOPBs are relatively small. For more detailed information see the VMEbus Specification. To put the 721 into block mode, use one of the two address modifiers in the the IOPB's Address Modifier byte (xF or xB, where x = don't care).

9

Interface Signals

9

Interface Signals

9.1. General

This section provides useful interface information for your 721 SCSI controller.

9.2. VMEbus Interface Signals

Mnemonic	Conn.	Pin	Used By 721	Description
A01	P1A	30	Y	
A02	P1A	29	Y	
A03	P1A	28	Y	
A04	P1A	27	Y	
A05	P1A	26	Y	
A06	P1A	25	Y	
A07	P1A	24	Y	
A08	P1C	30	Y	
A09	P1C	29	Y	
A10	P1C	28	Y	
A11	P1C	27	Y	
A12	P1C	26	Y	
A13	P1C	25	Y	
A14	P1C	24	Y	
A15	P1C	23	Y	Address Bus
A16	P1C	22	Y	
A17	P1C	21	Y	
A18	P1C	20	Y	
A19	P1C	19	Y	
A20	P1C	18	Y	
A21	P1C	17	Y	
A22	P1C	16	Y	
A23	P1C	15	Y	
A24	P2B	4	Y	
A25	P2B	5	Y	
A26	P2B	6	Y	

9.2. VMEbus Interface Signals (continued)

Mnemonic	Conn.	Pin	Used By 721	Description
A27	P2B	7	Y	
A28	P2B	8	Y	
A29	P2B	9	Y	
A30	P2B	10	Y	
A31	P2B	11	Y	
AM0	P1B	16	Y	
AM1	P1B	17	Y	
AM2	P1B	18	Y	Address Modifier
AM3	P1B	19	Y	
AM4	P1A	23	Y	
AM5	P1C	14	Y	
D00	P1A	1	Y	
D01	P1A	2	Y	
D02	P1A	3	Y	
D03	P1A	4	Y	
D04	P1A	5	Y	
D05	P1A	6	Y	
D06	P1A	7	Y	
D07	P1A	8	Y	Data Bus
D08	P1C	1	Y	
D09	P1C	2	Y	
D10	P1C	3	Y	
D11	P1C	4	Y	
D12	P1C	5	Y	
D13	P1C	6	Y	
D14	P1C	7	Y	
D15	P1C	8	Y	
D16	P2B	14	Y	
D17	P2B	15	Y	
D18	P2B	16	Y	
D19	P2B	17	Y	
D20	P2B	18	Y	
D21	P2B	19	Y	

9.2. VMEbus Interface Signals (continued)

Mnemonic	Conn.	Pin	Used By 721	Description
D22	P2B	20	Y	
D23	P2B	21	Y	Data Bus
D24	P2B	23	Y	
D25	P2B	24	Y	
D26	P2B	25	Y	
D27	P2B	26	Y	
D28	P2B	27	Y	
D29	P2B	28	Y	
D30	P2B	29	Y	
D31	P2B	30	Y	
Strobes				
AS*	P1A	18	Y	Address Strobe
DS0*	P1A	13	Y	Data Strobe Zero
DS1*	P1A	12	Y	Data Strobe One
DTACK*	P1A	16	Y	Data Transfer Ack.
Clocks				
SERCLK	P1B	21	N	Serial Clock
SYSCLK	P1A	10	N	System Clock
DMA				
BBSY*	P1B	1	Y	Bus Busy
BCLR*	P1B	2	N	Bus Clear
BERR*	P1C	11	Y	Bus Error

9.2. VMEbus Interface Signals (continued)

Mnemonic	Conn.	Pin	Used By 721	Description
DMA (continued)				
BG0IN*	P1B	4	Y	
BG1IN*	P1B	6	Y	Bus Grant In
BG2IN*	P1B	8	Y	
BG3IN*	P1B	10	Y	
BG0OUT*	P1B	5	Y	
BG1OUT*	P1B	7	Y	Bus Grant Out
BG2OUT*	P1B	9	Y	
BG3OUT*	P1B	11	Y	
BR0*	P1B	12	Y	
BR1*	P1B	13	Y	Bus Request
BR2*	P1B	14	Y	
BR3*	P1B	15	Y	
Interrupts				
IRQ1*	P1B	30	Y	
IRQ2*	P1B	29	Y	
IRQ3*	P1B	28	Y	Interrupt Request Levels
IRQ4*	P1B	27	Y	
IRQ5*	P1B	26	Y	
IRQ6*	P1B	25	Y	
IRQ7*	P1B	24	Y	
IACK*	P1A	20	Y	Interrupt Acknowledge
IACKIN*	P1A	21	Y	Interrupt Acknowledge In
IACKOUT*	P1A	22	Y	Interrupt Acknowledge Out

9.2. VMEbus Interface Signals (continued)

Mnemonic	Conn.	Pin	Used By 721	Description
Miscellaneous				
ACFAIL*	P1B	3	Y	AC Failure
LWORD*	P1C	13	Y	Longword
RESERVED	P2B	3	N	Reserved
SERDAT*	P1B	22	N	Serial Data
SYSFAIL*	P1C	10	Y	System Failure
SYSRESET*	P1C	12	Y	System Reset
WRITE*	P1A	14	Y	Write
Power				
+5V	P1A,B,C	32	Y	+5 VDC
+5V	P2B	1,13,32	Y	+5 VDC
+5V STDBY	P1B	31	N	+5 VDC Standby
+12V	P1C	31	N	+12 VDC
-12V	P1A	31	N	-12 VDC
GND	P1A	9,11,15,17,19	Y	Signal Ground
GND	P1B	20,23	Y	Signal Ground
GND	P2B	2,12,22,31	Y	Signal Ground
GND	P1C	9	Y	Signal Ground

9.3. SCSI Bus Interface Signals

The SCSI bus supports up to eight devices, including any combination of initiators and targets. There are eighteen SCSI bus signals: nine for control and nine for data. Data signals include the parity signal option.

9.3.1. Single-ended Pin Assignments

Connect all odd pins, except pin 25, to ground; leave pin 25 open. The minus sign preceding the signal name indicates active low.

Signal Name	Pin Number
-DB (0)	2
-DB (1)	4
-DB (2)	6
-DB (3)	8
-DB (4)	10
-DB (5)	12
-DB (6)	14
-DB (7)	16
-DB (P)	18
Ground	20
Ground	22
Ground	24
TERMPWR	26
Ground	28
Ground	30
-ATN	32
Ground	34
-BSY	36
-ACK	38
-RST	40
-MSG	42
-SEL	44
-C/D	46
-REQ	48
-I/O	50

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Clarity	☐	☐	☐	☐
Organization	☐	☐	☐	☐
Figures (usefulness)	☐	☐	☐	☐
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