

ORDVAC MANUAL

Volume TWO

Circuit and Logical Diagrams

1952

UNIVERSITY OF ILLINOIS

for

BALLISTIC RESEARCH LABORATORIES

LIST OF DRAWINGS

<u>NUMBER</u>	<u>TITLE</u>	<u>SHORT DESIGNATION</u>
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126	Regulated Power Supply	
127	Green Gate Chassis	
129	DC Control and Distribution	
130	Clear Driver	
138	6AS7 Cathode Follower \pm 240V Supply	
155	Complement Gate	
159	Verifier Circuit Revised	
167	Input-Output Relay Circuit	V
169	Power Supply -2000V, 200MA	
171	Driver III Chassis	E
174	Modified Transmitter Distributor	X
176	Pulser Cathode Follower Chassis	
181	Shift Sequencing Chassis	A
189	Shift Control	A
190	AC Distribution	
192	Clear Driver Driver RI	
193	Clear Driver Driver RII	
194	Clear Driver Driver RIII	
195	Address Generator	Q
196	Video Amplifier and Williams Tube Control	W
198	Complement Gate Driver Chassis	K
200	Digit Resolver	
201	Gate Driver RI	
202	Gate Driver RII	
208	Modified Schematic -15 Printer Set with Keyboard	
209	Wiring -15 Type Perforator	
210	Modification of Teletype Table	
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231	Diode Chassis for Address Generator	
236	Carry Delay II	G
244	Arithmetic Control	C
245	Delay Selector Chassis	F
249	Odd Address Gate Chassis	CC
250	Odd Order Gate Chassis	BB
251	Even Order Gate Chassis	AA
252	Even Address Cathode Follower Chassis	DD
253	Counter Output Chassis	H
257	End Connection Logic	J
259	Input Gates for Input Circuit	
260	Decoding Chassis	D

261	Williams IV Pulse Cathode Followers	
265	TPR Output Connections	
266	Gating from R ₃	
271	Input-Output Start and Shift Chassis II	L
273	End Connection Circuits	J
274	Dispatch Counter	T
280	Gate Driver RIII	
288	Register Selection Chassis	P
289	Memory Control	M
290	Memory Synchronization Chassis	N
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300	Logical Diagram of Arithmetic Control	C
301	Logical Diagram of the Interplay Control	M, N, P
302	Logical Diagram of Delay Selector	F
305	Decoding Logic and Recognition Circuit	D
306	Decoding Register Code	
307	Order Register Code	
312	Green Gate Sequence	
314	Yellow Gate Sequence	
315	Black Gate RI Sequence	
316	Red Gate RI Sequence	
317	Memory Interplay Control	
318	Reversed Twitch Stagger Columns Generator	
319	Complement or Not Complement Sequence	
326	Input-Output Start and Shift Chassis I	U
327	Interconnection Chassis	Z
333	Idealized Pulses for Memory	
338	Basic Cycle Sequence	
339	Transfer Control Operation Sequence	
340	Order Pair Read-Out Sequence	
341	Store Operation Sequence	
343	Arithmetic Stop Chassis	B
344	Input-Output Schematic	
345	Start and Print Relay Chassis	
346	Interconnection Chassis II	
347	Start and Shift Chassis IA	
348	Logical Diagram - Arithmetic Stop and Start Control	B
349	Memory Sequences	
350	Memory Block Diagram	
351	Memory Regen. Logic	
352	Logical Symbols and Usual Circuit Equivalents	
353	Shift Counter Circuit	
354	Shift Control Logic	A
355	Punched Tape Showing Code Used.	
356	Low Speed Input-Output Wiring	
357	Slave Tube Cathode Followers	
358	Physical Layout Memory Chassis	
359	RI Register	
360	RII Register	

361	RIII Register	
362	RIII Register, 2^{-10} to 2^{-19}	
363	RIII Register, 2^{-20} to 2^{-29}	
364	RIII Register, 2^{-30} to 2^{-39}	
365	"A" Operation Sequence	
366	"R" Operation Sequence	
368	Memory Pulser	S
369	Pulser Supply Chassis	
370	WIV Clock	
371	Pulser Connections	
372	Slave Tube	
374	Arithmetic or Shift Operation Sequence	
375	Add Operation Sequence	
376	Multiplication Operation Sequence	
378	Mixing Circuits for Pulses on #10	
379	Loudspeaker Chassis	
380	Arithmetic Control Circological Diagram	C
382	Fast Input BC Enable	
383	Input Switch	

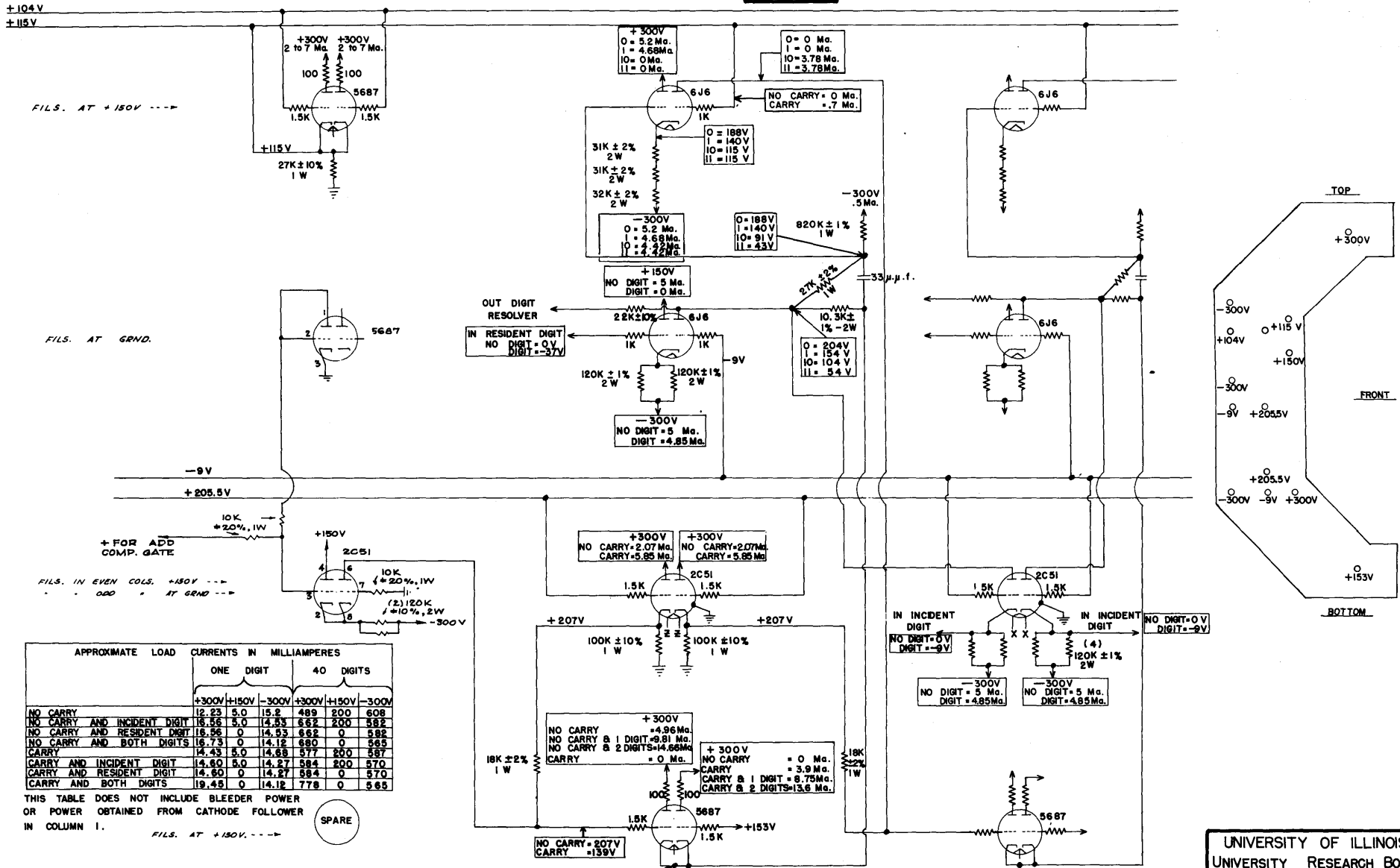
362	RIII Register 2 ⁻¹⁰ to 2 ⁻¹⁹	
363	RIII Register 2 ⁻²⁰ to 2 ⁻²⁹	
364	RIII Register 2 ⁻³⁰ to 2 ⁻³⁹	
372	Slave Tube	
357	Slave Tube Cathode Followers	
189	Shift Control	A
354	Shift Control Logic	
353	Shift Counter Circuit	
181	Shift Sequencing Chassis	A
345	Start and Print Relay Chassis	
347	Start and Shift Chassis 1A	
341	Store Operation Sequence	
265	TPR Output Connection	
339	Transfer Control Operation Sequence	
159	Verifier Circuit Revised	
196	Video Amplifier and Williams Tube Control	W
370	WIV Clock	
261	Williams IB Pulse Cathode Follower	
209	Wiring-15 Type Perforator	
314	Yellow Gate Sequence	

XS-104-2

COLUMN 1

COLUMN 2

COLUMN 3



FILS. AT +150V ---

FILS. AT GRND.

FILS. IN EVEN COLS. +150V ---
 000 --- AT GRND ---

+ FOR ADD
 COMP. GATE

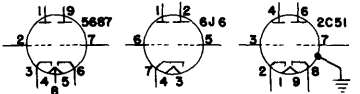
APPROXIMATE LOAD	CURRENTS IN MILLIAMPERES					
	ONE DIGIT		40 DIGITS			
	+300V	+150V	-300V	+300V	+150V	-300V
NO CARRY	12.23	5.0	15.2	489	200	608
NO CARRY AND INCIDENT DIGIT	16.56	5.0	14.53	662	200	582
NO CARRY AND RESIDENT DIGIT	16.56	0	14.53	662	0	582
NO CARRY AND BOTH DIGITS	16.73	0	14.12	680	0	565
CARRY	14.43	5.0	14.88	577	200	587
CARRY AND INCIDENT DIGIT	14.60	5.0	14.27	584	200	570
CARRY AND RESIDENT DIGIT	14.60	0	14.27	584	0	570
CARRY AND BOTH DIGITS	19.48	0	14.12	778	0	565

THIS TABLE DOES NOT INCLUDE BLEEDER POWER OR POWER OBTAINED FROM CATHODE FOLLOWER IN COLUMN 1.

FILS. AT +150V. ---



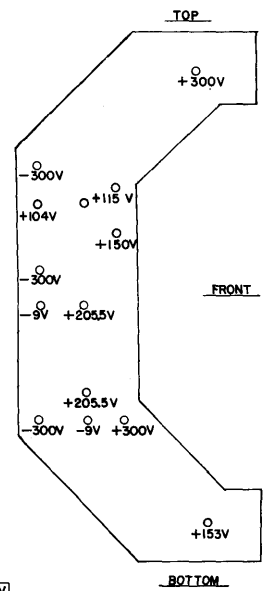
TUBE CONNECTION - DESIGNATION



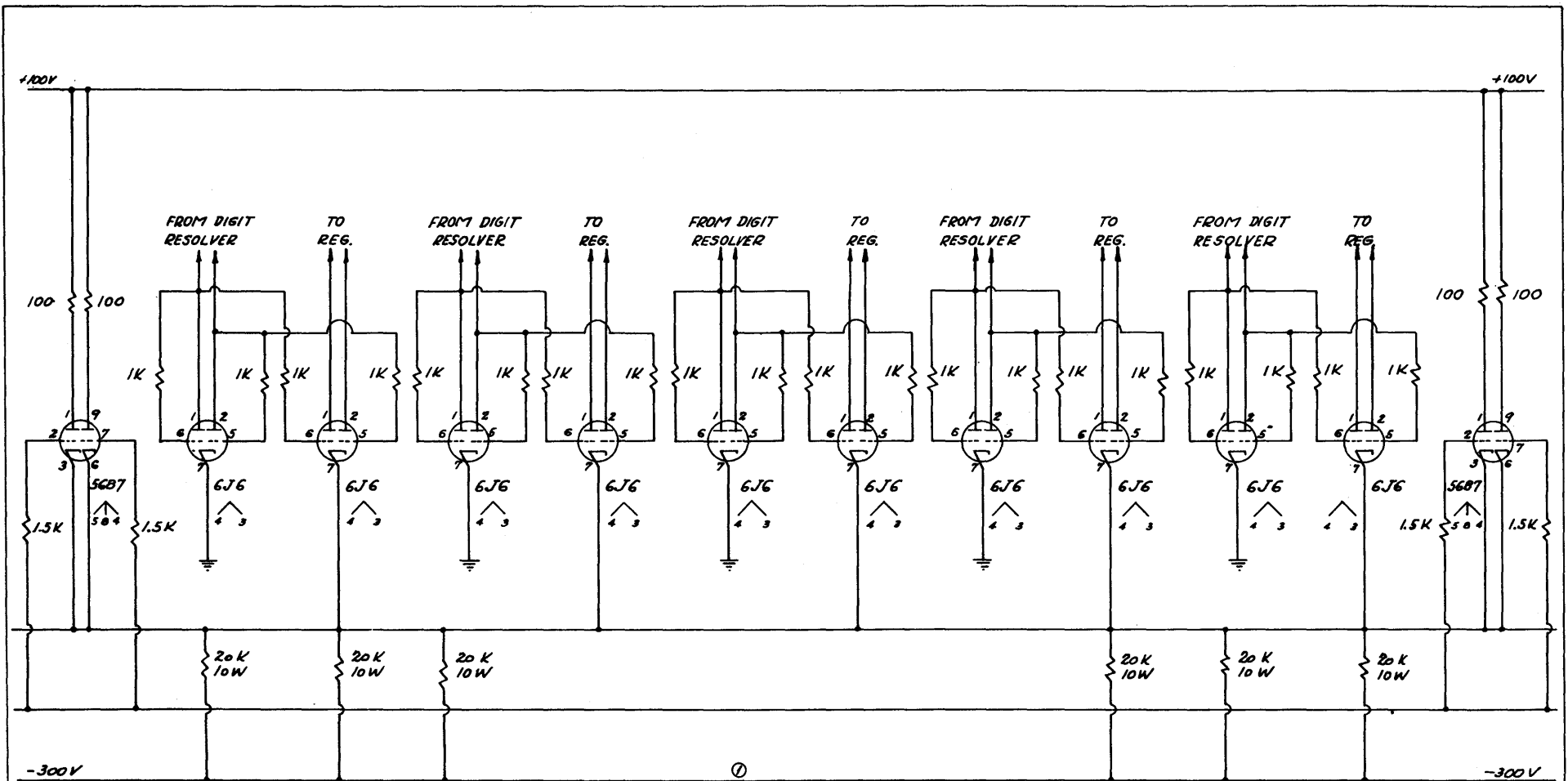
NOTE:
 COLUMNS 2-4-6-8-10 ARE IDENTICAL.
 COLUMNS 3-5-7-9-11 ARE IDENTICAL.

NOTE:
 RESISTORS — ±20%, 1/2 WATT, UNLESS SPECIFIED.
 CONDENSERS — ±20%, 600 V.

REVISED 10-24-51

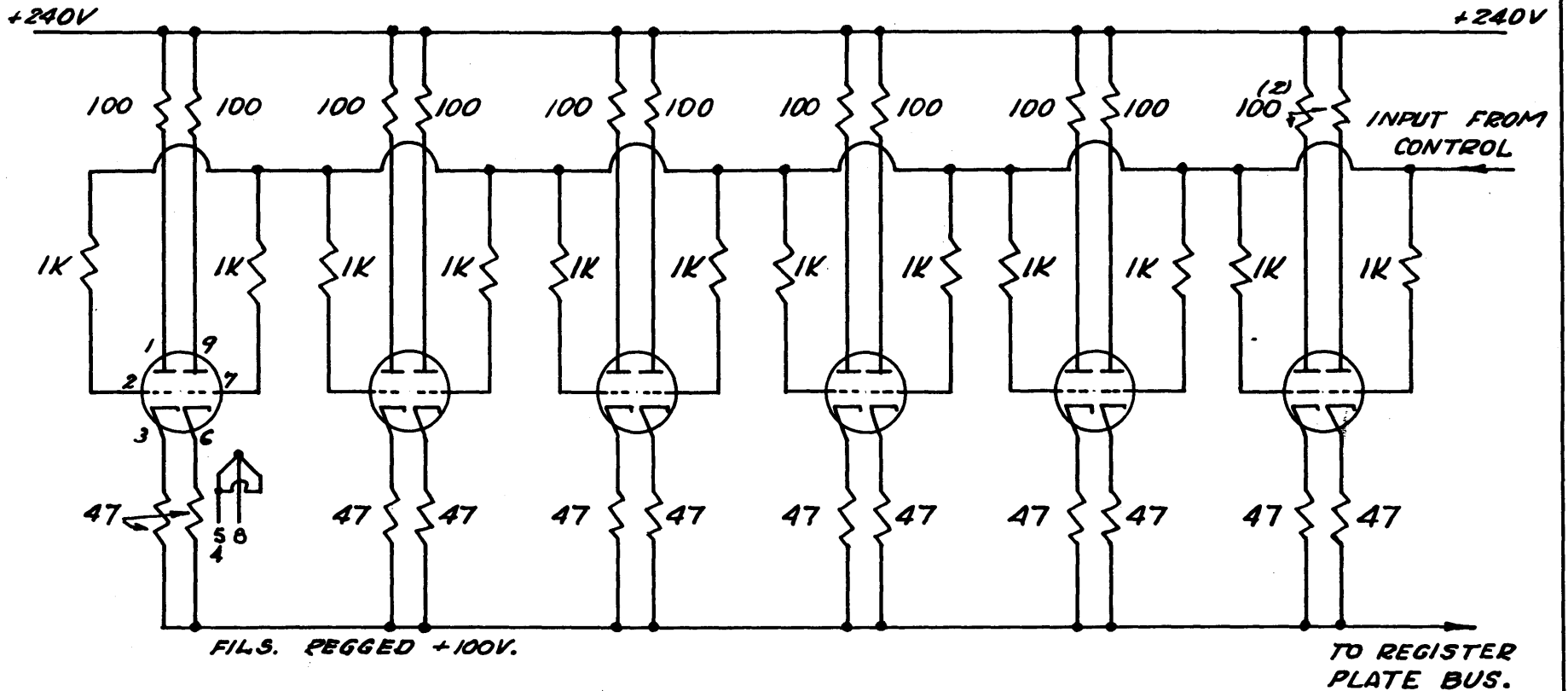


UNIVERSITY OF ILLINOIS
 UNIVERSITY RESEARCH BOARD
 ELECTRONIC DIGITAL COMPUTER
 DRAWN FOR 2-2-51 BY: [Signature]
 CHECKED BY: [Signature] APPROVED BY: [Signature]
 DATE 4/2/51 LOCATION [Signature]
 TITLE ADDER CIRCUIT
 DWG. NO. XS-104-2



- NOTE -
 ALL RESISTORS NOT SPECIFIED ARE 1/2 W, ± 20%.
 ALL FILAMENTS AT GROUND.

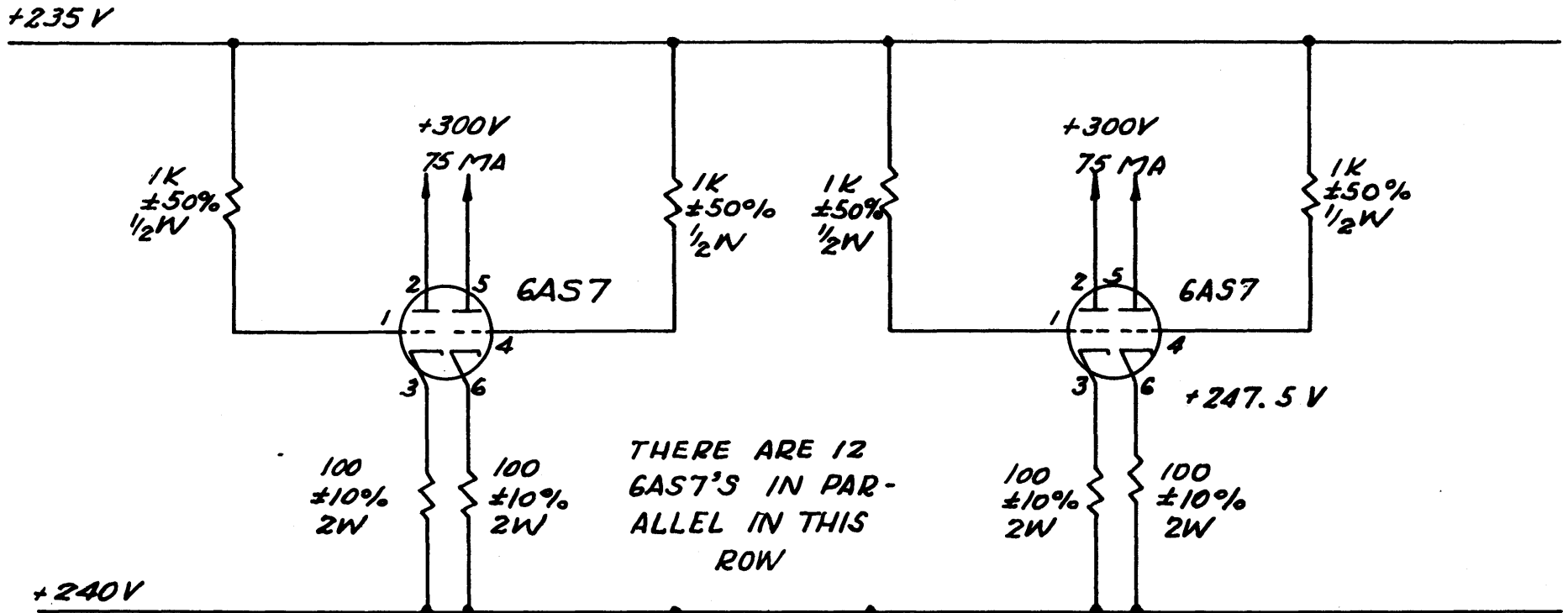
REDRAWN FROM "DRWG. 127 - 1-5-50."
UNIVERSITY of ILLINOIS
 UNIVERSITY RESEARCH BOARD
 ELECTRONIC DIGITAL COMPUTER
 DRAWN FOR W. Joyce DRAWN BY H.M.W.
 CHECKED BY W. S. 7-50 APPROVED BY R.E. W. 7-50
 TITLE GREEN GATE
CHASSIS
 DATE 8-11-50 **M-127**



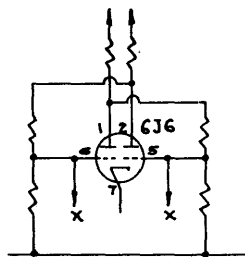
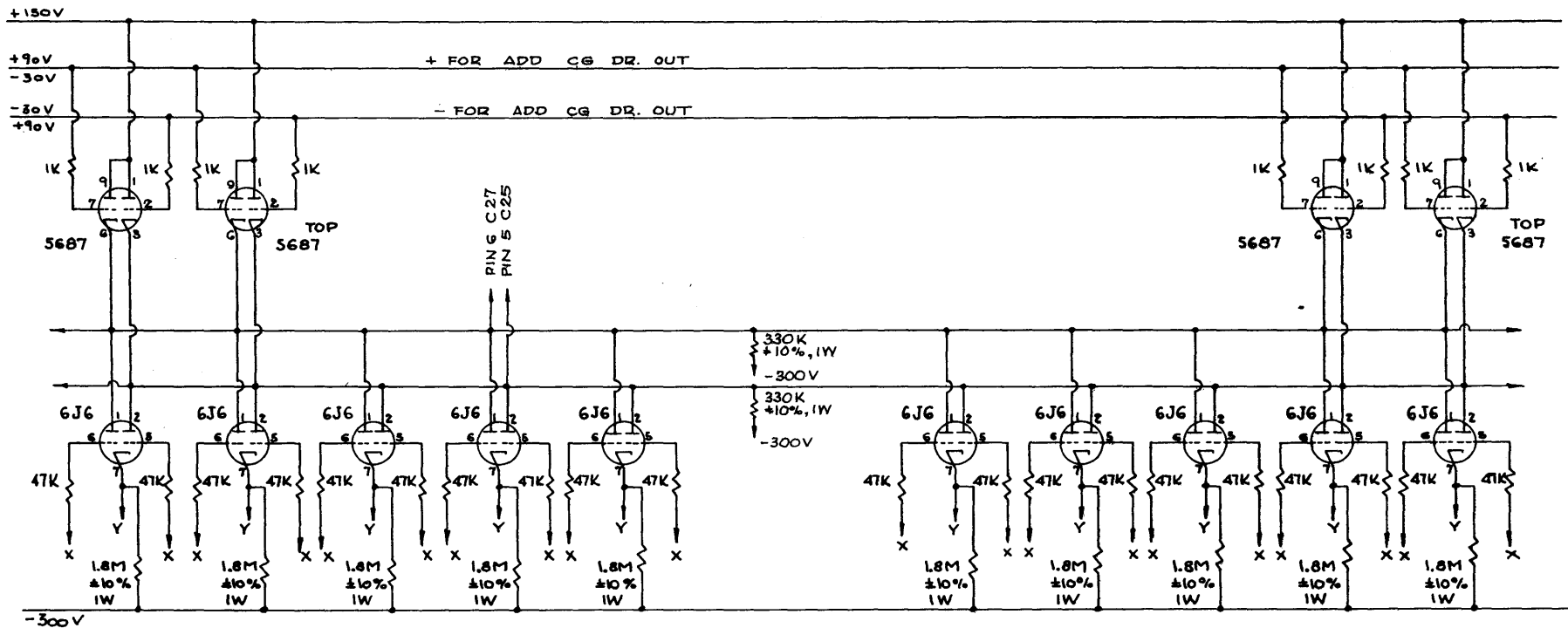
- ~NOTES~
1. ALL RESISTORS ARE $\frac{1}{2}$ W
± 5%
 2. ALL TUBES ARE 5687'S.
 3. ALL FIL. CONN. TO 6.3V
AS SHOWN ON FIRST TUBE.
- REDRAWN FROM DRWG. #130 DATED
1-9-50 BY T.B.

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 ELECTRONIC DIGITAL COMPUTER
 DRAWN FOR W.J. DRAWN BY H.V.
 CHECKED W.J. APPROVED R.E. Meagher
 TITLE CLEAR DRIVER

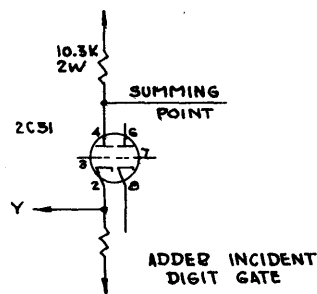
DATE 8-11-50 DRWG. No 130



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ELECTRONIC DIGITAL COMPUTER
DRAWN FOR MDS DRAWN BY HW
CHECKED M.D.S. APPROVED R.E. Wood
TITLE 6AS7 CATHODE FOL-
LOWER, ±240V SUPPLY
DATE 8-14-50 DRWG. N° - 138



REGISTER TOGGLE



ADDER INCIDENT DIGIT GATE

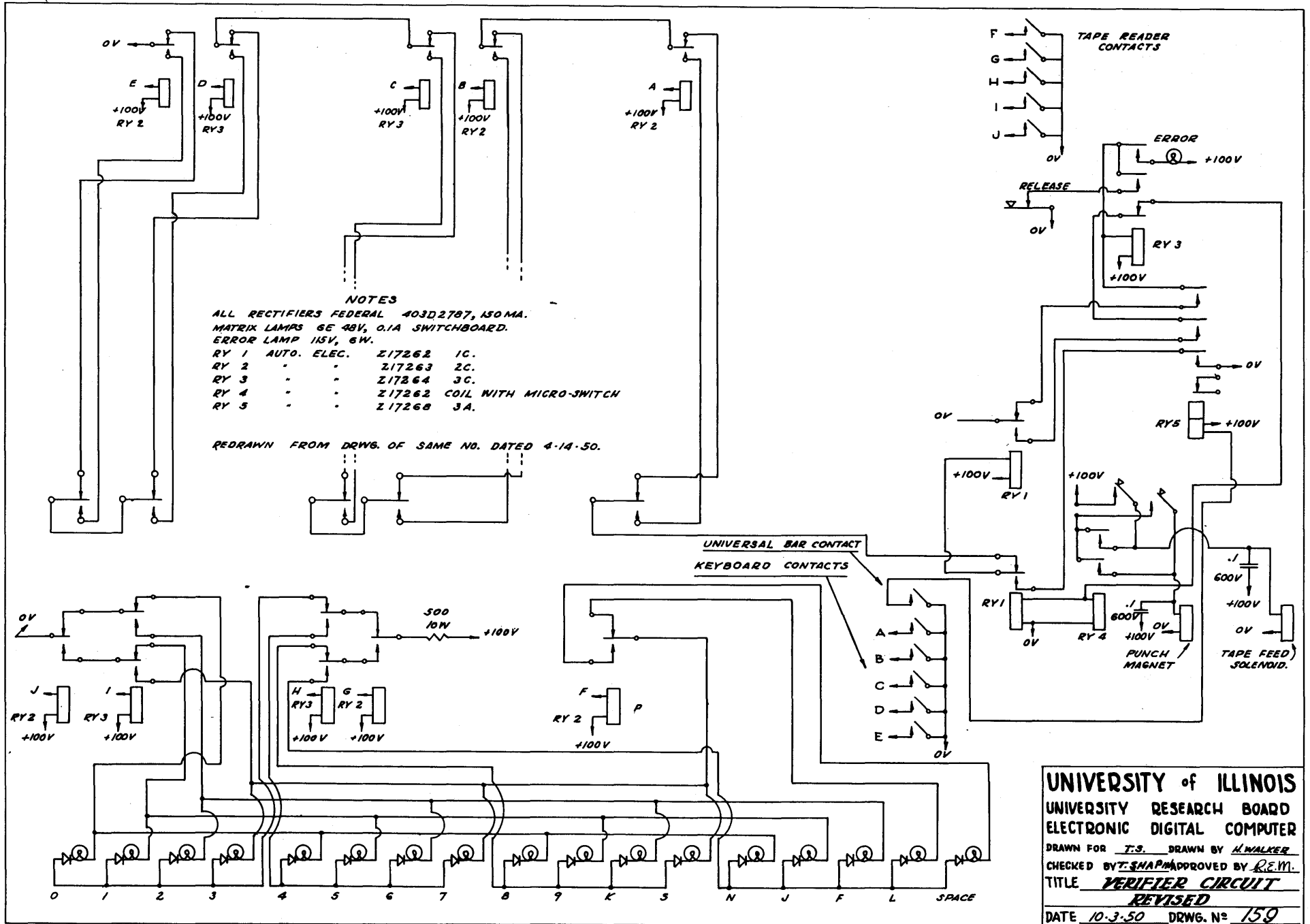
* REVISED 1-3-52

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 UNIVERSITY RESEARCH BOARD
 ELECTRONIC DIGITAL COMPUTER
 DRAWN FOR M.D.S. DRAWN BY H.W.
 CHECKED BY M.D.S. APPROVED BY R.E.W.
 TITLE COMPLEMENT GATE

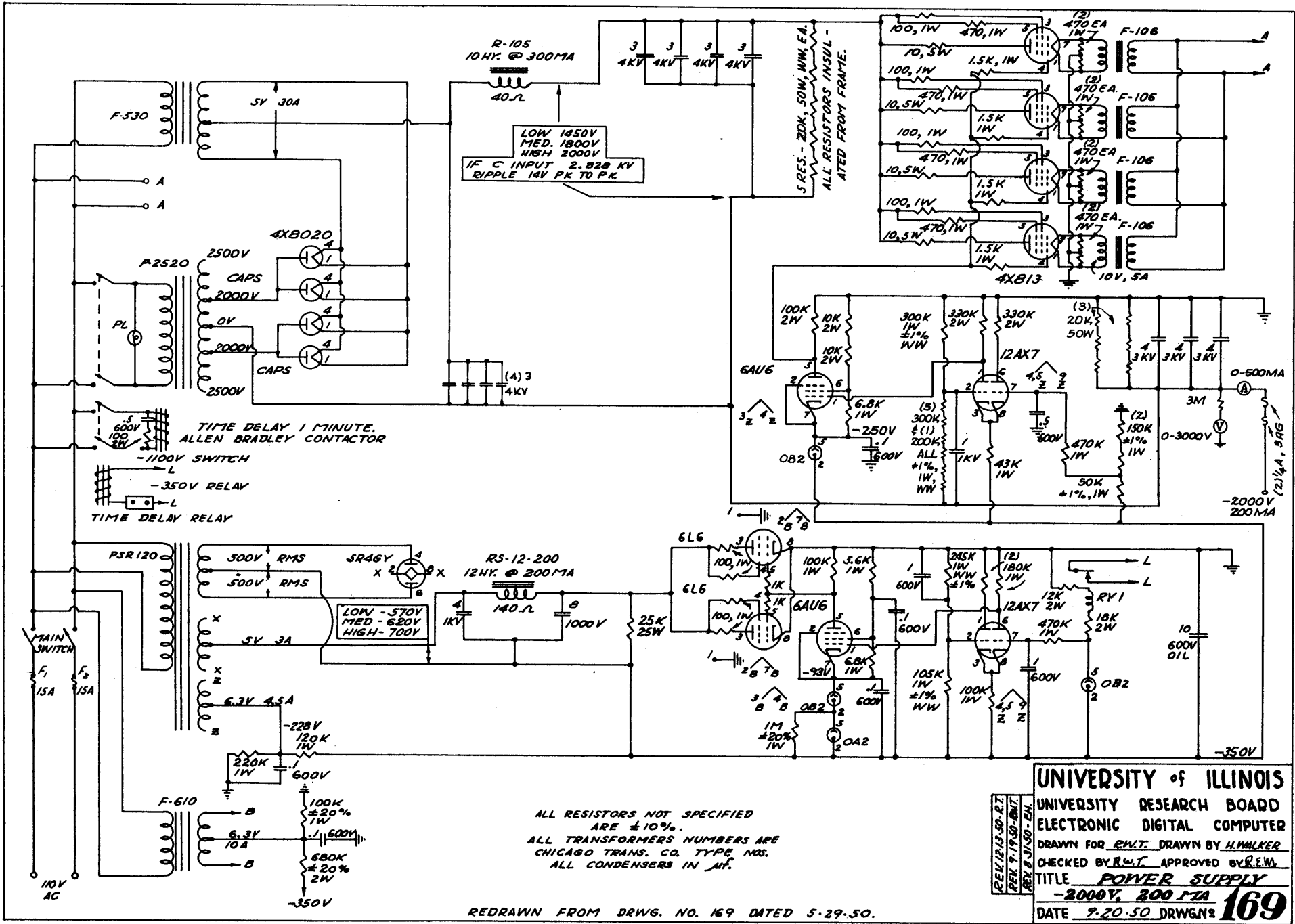
- ~NOTES~
1. RESISTORS NOT SPECIFIED ARE $\frac{1}{2}$ W, $\pm 20\%$.
 2. REDRAWN FROM DRWG. No. 155 DATED 4-12-50.
 3. ALL FILS. AT GROUND.

DATE 8-14-50

M-155



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 DRAWN FOR T.S. DRAWN BY H. WALKER
 CHECKED BY T. SNAPP APPROVED BY R.E.M.
 TITLE **VERIFIER CIRCUIT**
 REVISED
 DATE 10-3-50 DRWG. N° 159

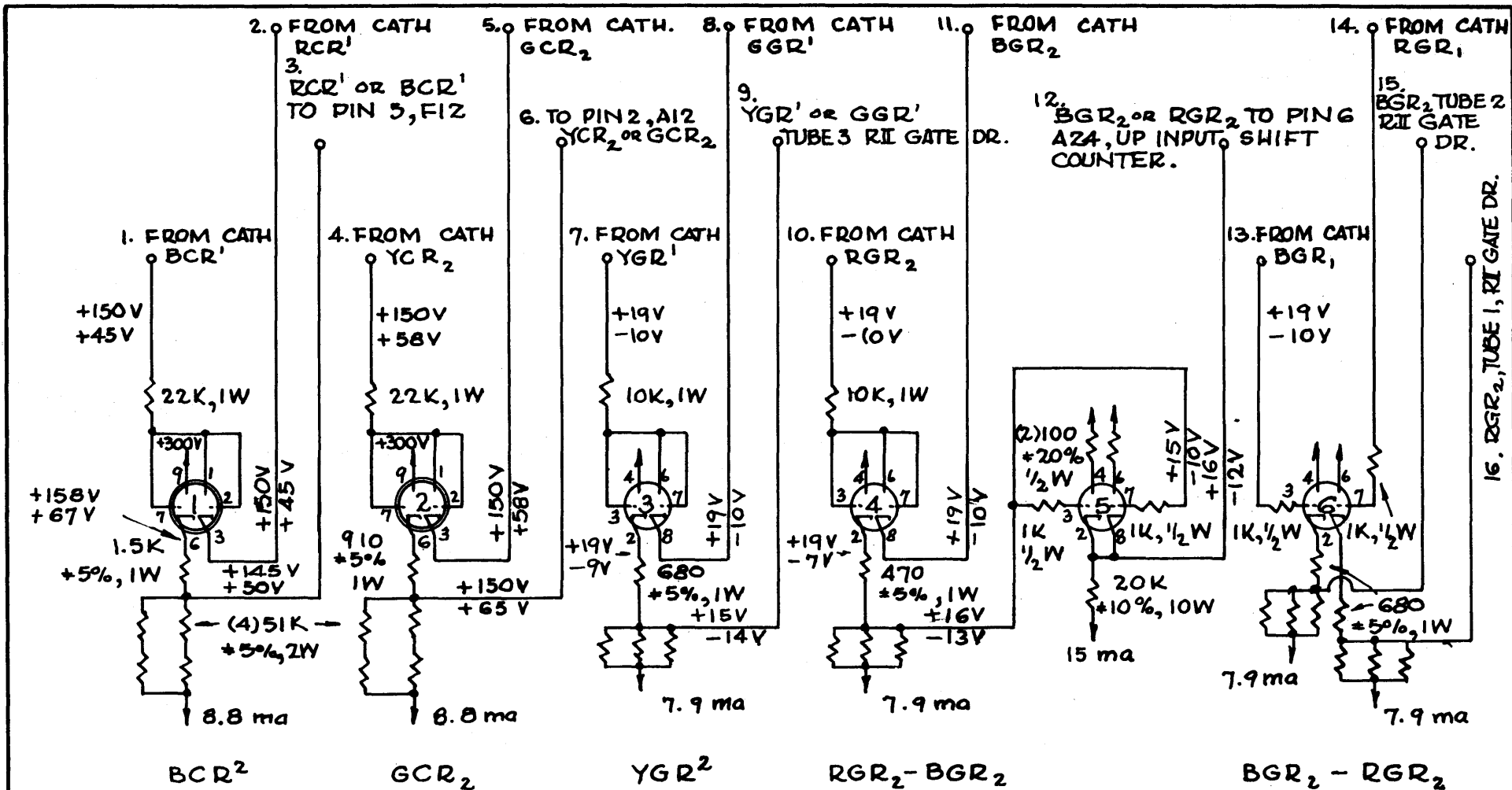


ALL RESISTORS NOT SPECIFIED ARE $\pm 10\%$.
 ALL TRANSFORMERS NUMBERS ARE CHICAGO TRANS. CO. TYPE NOS.
 ALL CONDENSERS IN μF .

REDRAWN FROM DRWG. NO. 169 DATED 5-29-50.

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 DRAWN FOR R.M.T. DRAWN BY H.MALKER
 CHECKED BY R.M.T. APPROVED BY R.E.W.
 TITLE **POWER SUPPLY**
 -2000V, 200 MA
 DATE 9-20-50 DRWG# **169**

REV 12-13-50-R.T.
 REV 9-19-50-R.M.T.
 REV 8-31-50-E.H.



WHEN NOT SPECIFIED:

1. UP VOLTAGES ARE +100V.
2. DOWN " " -300V.
3. CATH. RESISTORS ARE 120K, +5%, 2W.
4. GRID RESISTORS ARE +10%.

○ INDICATES 5687

○ INDICATES 2C51

E

- FILAMENTS OF V1 & V2 AT +100V.
- ALL OTHER FILAMENTS AT GND.

• REVISED 11-14-51.
 • REVISED & REDRAWN FROM DRWG OF SAME NO. DATED 8-3-50

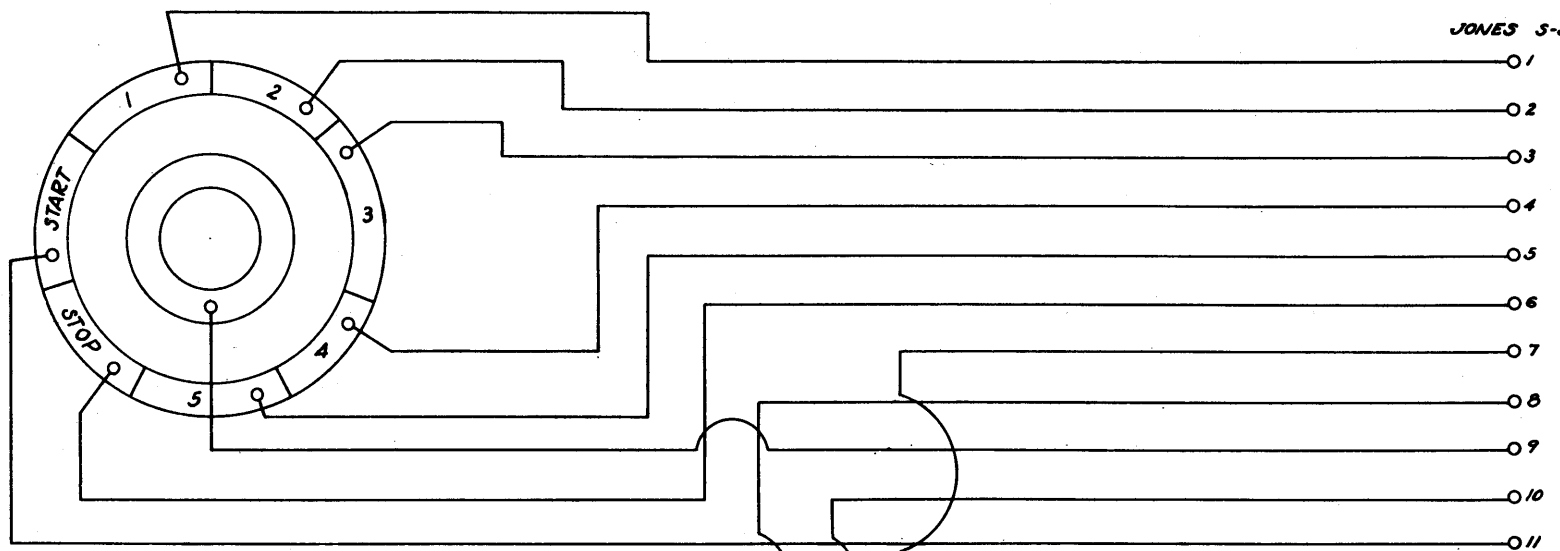
UNIVERSITY OF ILLINOIS · UNIVERSITY RESEARCH BOARD · ELECTRONIC DIGITAL COMPUTER

FOR JPN BY HMW CHECKED *Mark* APPROVED *R. E. Meagher* DATE 6-19-51

TITLE ~ DRIVER III CHASSIS

S-171

JONES S-318

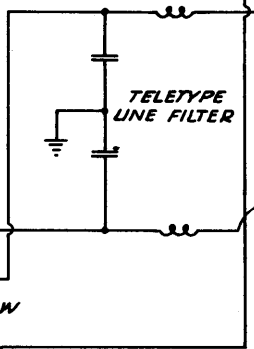


SLIP TERMINALS ON TRANSMITTER DIST.

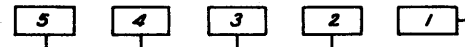
- 1 0
- 2 0
- 3 0
- 4 0
- 5 0
- 6 0
- 7 0
- 8 0
- 9 0

GND. SCREW

110AC



THIS SCREW REPLACED WITH INSULATOR FOR INPUT CIRCUIT.



MARKING LOWER CONTACTS

RELEASE MAGNET

TIGHT TAPE STOP CONTACT

REDRAWN 9-15-50 FROM DRWG. #174 DATED 6-13-50.

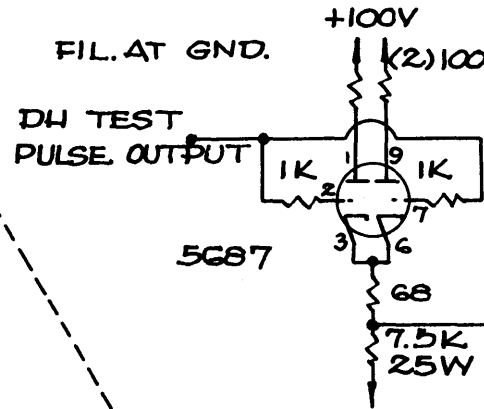
UNIVERSITY of ILLINOIS UNIVERSITY RESEARCH BOARD ELECTRONIC DIGITAL COMPUTER

DRAWN FOR T.S. DRAWN BY H.WALKER CHECKED BY T.SHAPIR APPROVED BY R.E.W.

TITLE MODIFIED TRANSMITTER DISTRIBUTER.

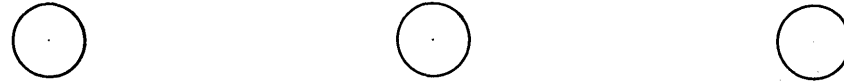
DATE 9-15-50 DRWG. NO. 174

PLATE & GRID RESISTORS ARE +20%, 1/2W.

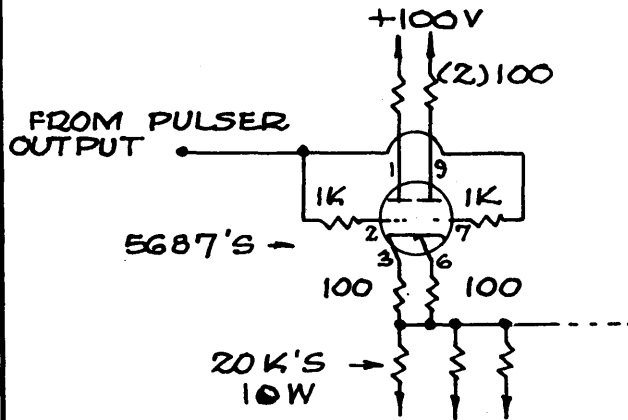


ISOLATION CATHODE FOLLOWER
FOR DASH TEST PULSE.

ALL 1K & 100 Ω RESISTORS ARE +20%, 1/2W.
ALL FILAMENTS AT GROUND.



PULSE	5687'S	20K RESISTORS
DOT	3	2
DH TEST	22	50
DH. END	10	20

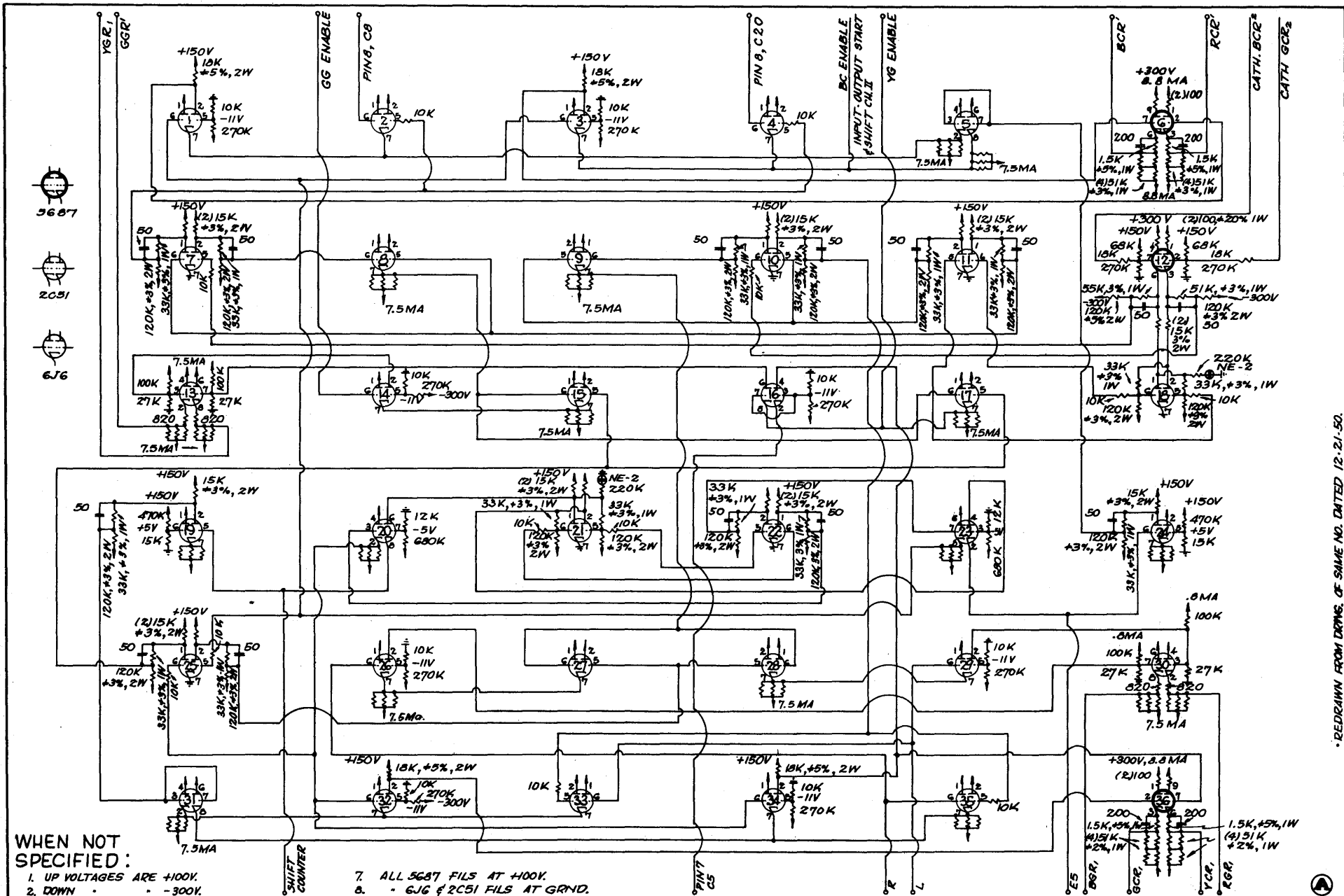


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FOR JMW BY HMW CHECKED *J. M. H.* APPROVED *R. E. Meagher* DATE 11-20-51

TITLE - PULSER CATHODE FOLLOWER CHASSIS

S-176



WHEN NOT SPECIFIED:

1. UP VOLTAGES ARE +100V.
2. DOWN - -300V.
3. CATHODE RESISTORS ARE 120K, +10%, 2W.
4. BLEEDERS ARE +5%, 1W.
5. OTHER RESISTORS ARE +20%, 1/2W.
6. CONDENSERS ARE IN μ M.

7. ALL 5687 FILS AT +100V.
8. - 6J6 & 2C51 FILS AT GRND.

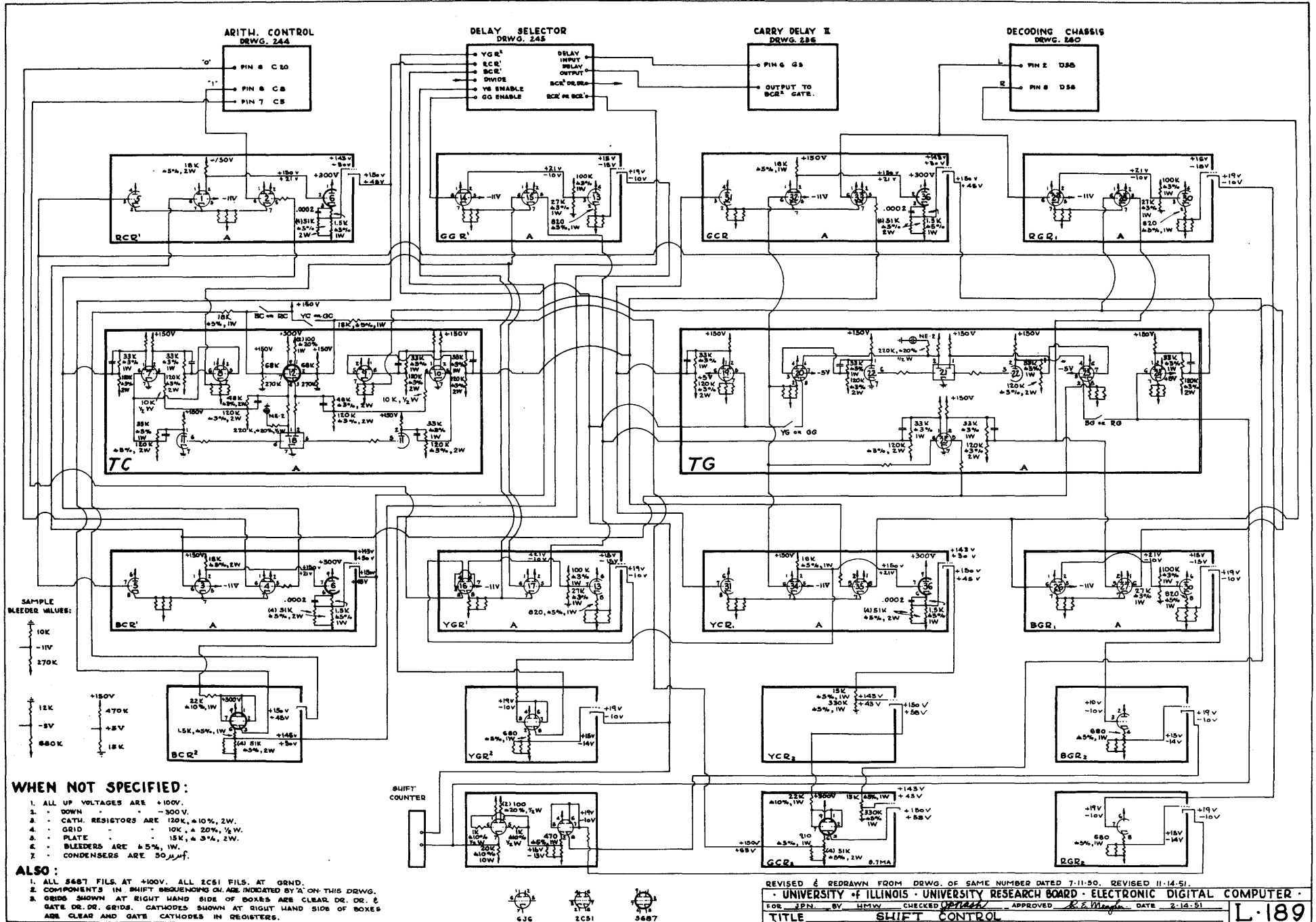
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FOR WEJ BY LIMW CHECKED *[Signature]* APPROVED *[Signature]* DATE 12-7-51

TITLE - **SHIFT SEQUENCING CHASSIS**

M-181

• REDRAWN FROM DRAWING OF SAME NO. DATED 12-21-50.



WHEN NOT SPECIFIED:

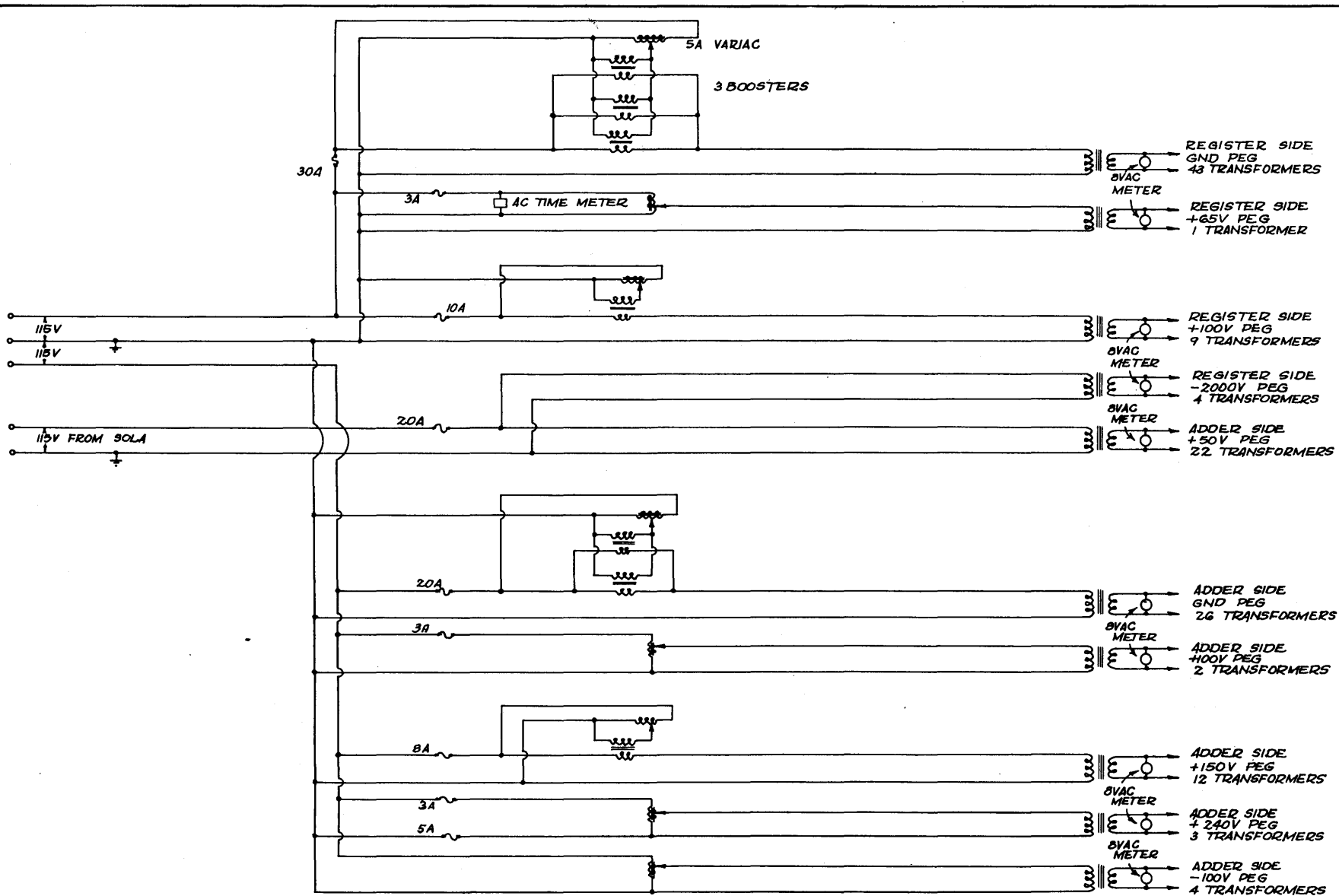
1. ALL UP VOLTAGES ARE +100V.
2. - DOWN - 300V.
3. - CATH. RESISTORS ARE 120K, ±10%, 2W.
4. - GRID - 10K, ±20%, 1/2W.
5. - PLATE - 15K, ±3%, 2W.
6. - BLEEDERS ARE ±5%, 1W.
7. - CONDENSERS ARE 50μF.

ALSO :

1. ALL 548T FILS. AT +100V. ALL 2C51 FILS. AT GRND.
2. COMPONENTS IN SHIFT SEQUENCING ARE INDICATED BY 'A' ON THIS DRWG.
3. GRID SHOWN AT RIGHT HAND SIDE OF BOXES ARE CLEAR DR. DR. & GATE DR. DR. GRIDS. CATHODES SHOWN AT RIGHT HAND SIDE OF BOXES ARE CLEAR AND GATE CATHODES IN REGISTERS.

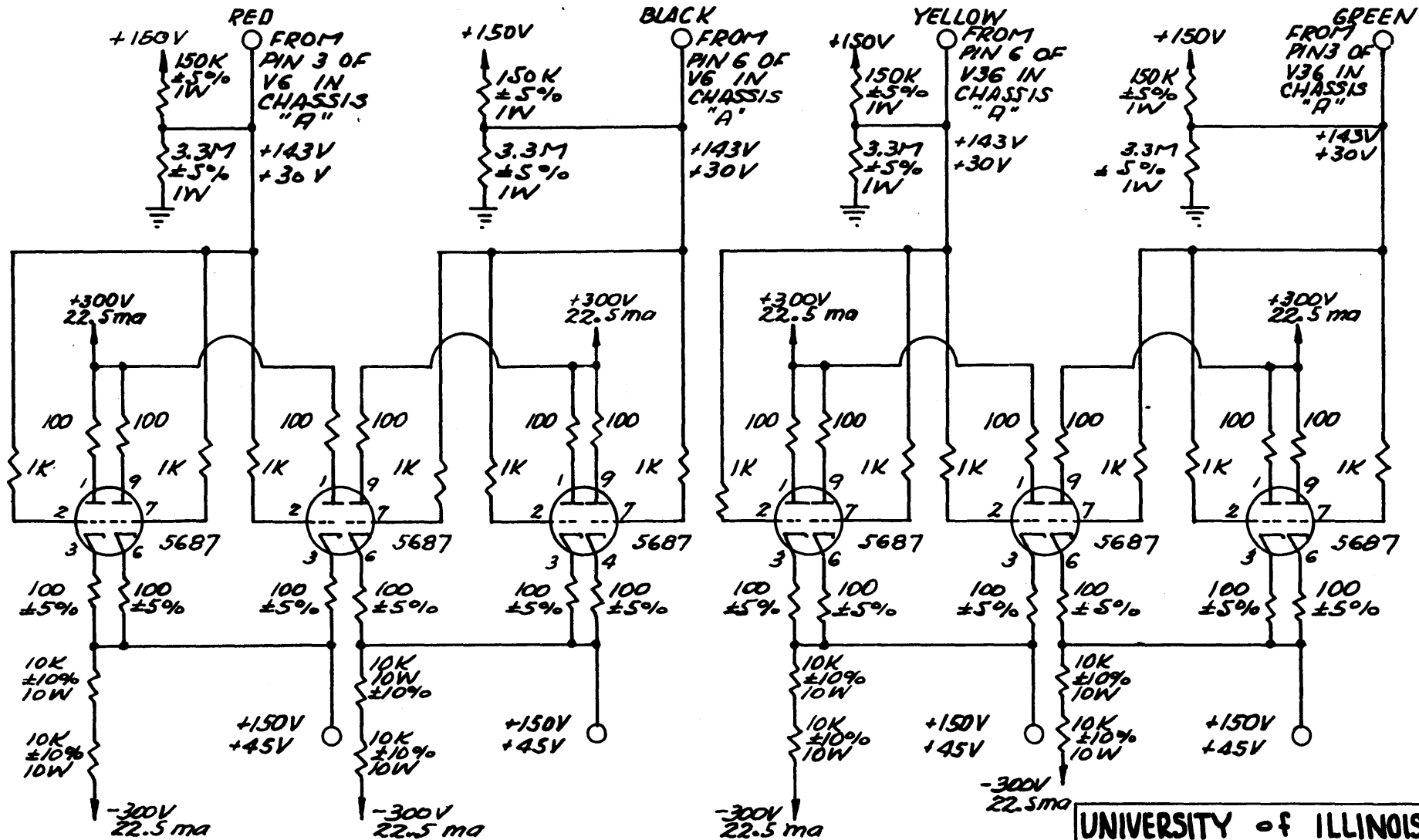


REVISED & REDRAWN FROM DRWG. OF SAME NUMBER DATED 7-11-50. REVISED 11-14-51.
 UNIVERSITY OF ILLINOIS - UNIVERSITY RESEARCH BOARD - ELECTRONIC DIGITAL COMPUTER
 FOR JEN. BY HPMV CHECKED *[Signature]* APPROVED *[Signature]* DATE 2-14-51
 TITLE SHIFT CONTROL L-189



~ NOTES ~

1. ALL 6.3V FILAMENT TRANSFORMERS ARE THORDARSON D161987.
2. ALL VARIACS GENERAL RADIO TYPE V-5MT.

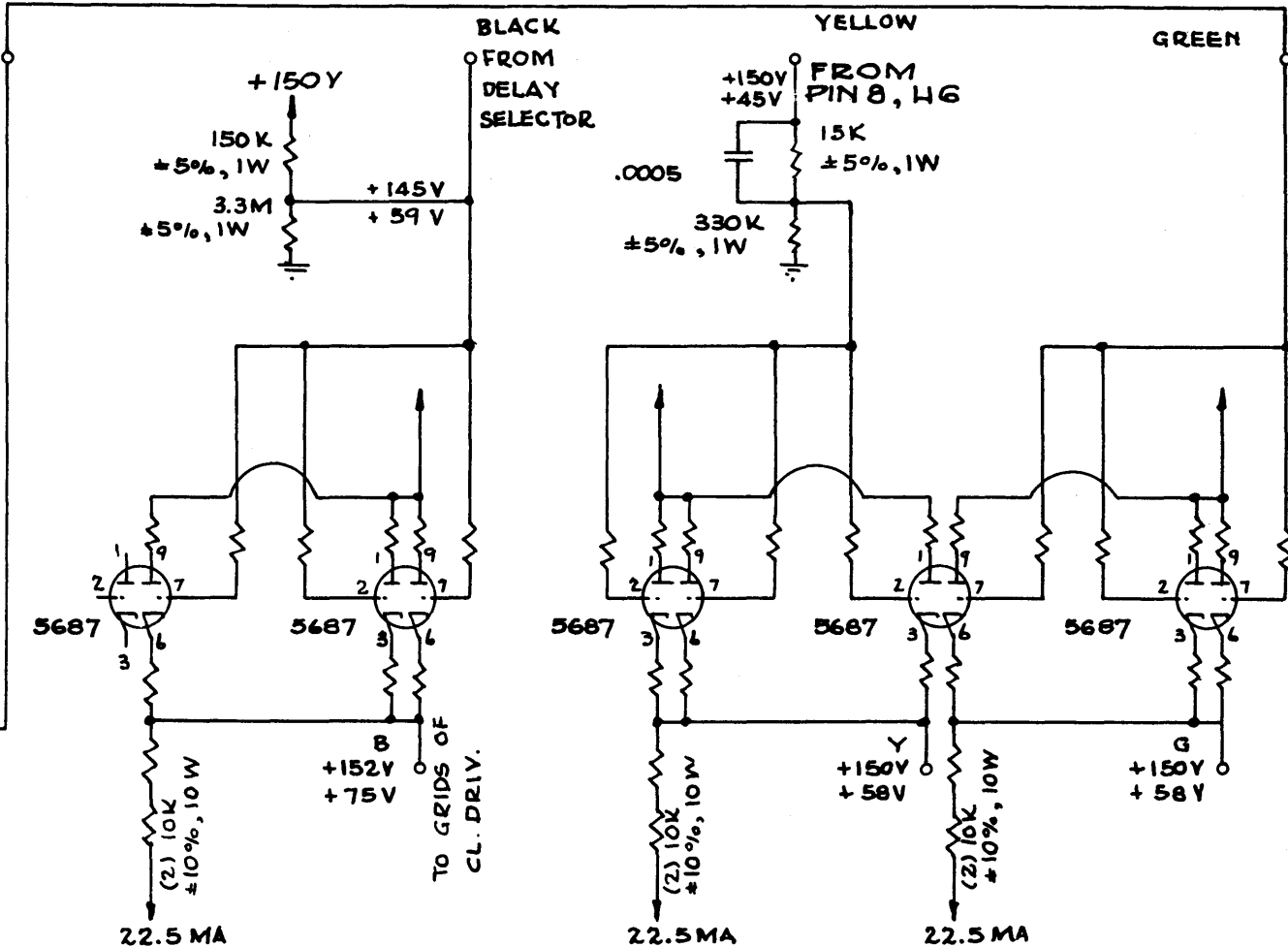
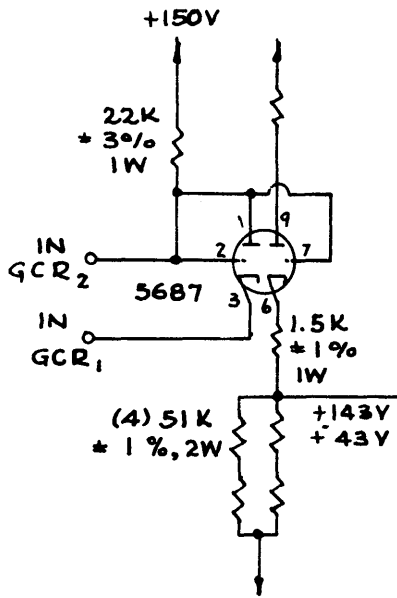


~ NOTES ~

1. UNLESS OTHERWISE SPECIFIED RESISTORS ARE 1/2W, ±20%.
2. FILAMENTS AT +100V.

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 DRAWN FOR J.P.N. DRAWN BY H.M.W.
 CHECKED Opn APPROVED R.E.M.
 TITLE CLEAR DRIVER
DRIVER RT
 DATE 7-21-50 DRWG. No. 192

FILS. AT +100V



WHEN
NOT
SPECIFIED }

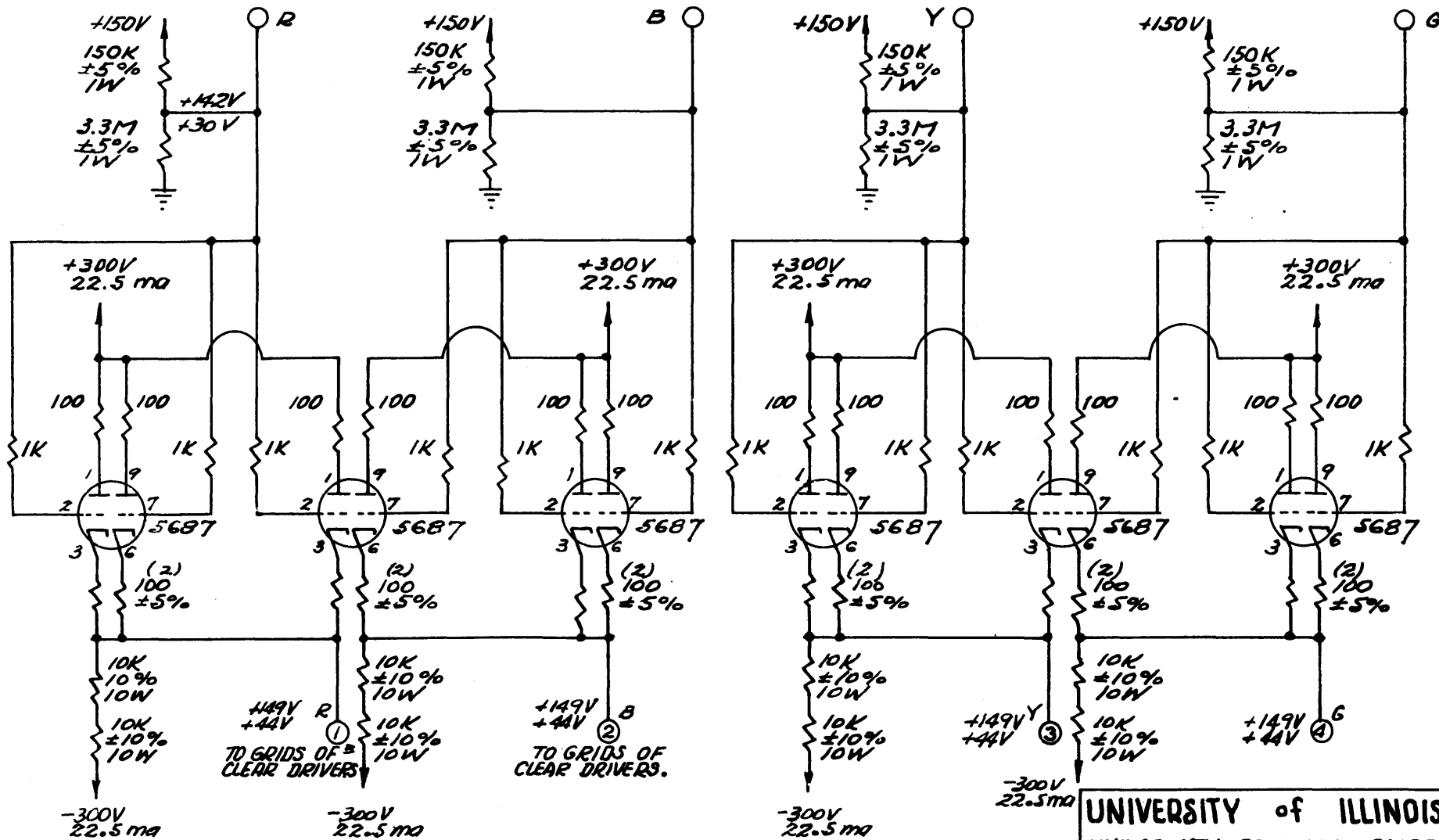
1. UP VOLTAGES ARE +500V.
2. DOWN " " - 300V.
3. PLATE RESISTORS ARE 100, ± 20%, 1/2 W.
4. GRID " " 1K, ± 20%, 1/2 W.
5. CATH. " " 100, ± 5%, 1/2 W.

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FOR ELH BY HMW CHECKED PLH APPROVED R. E. Meagher DATE 4-18-51

TITLE · CLEAR DR. DR. RII

S-193



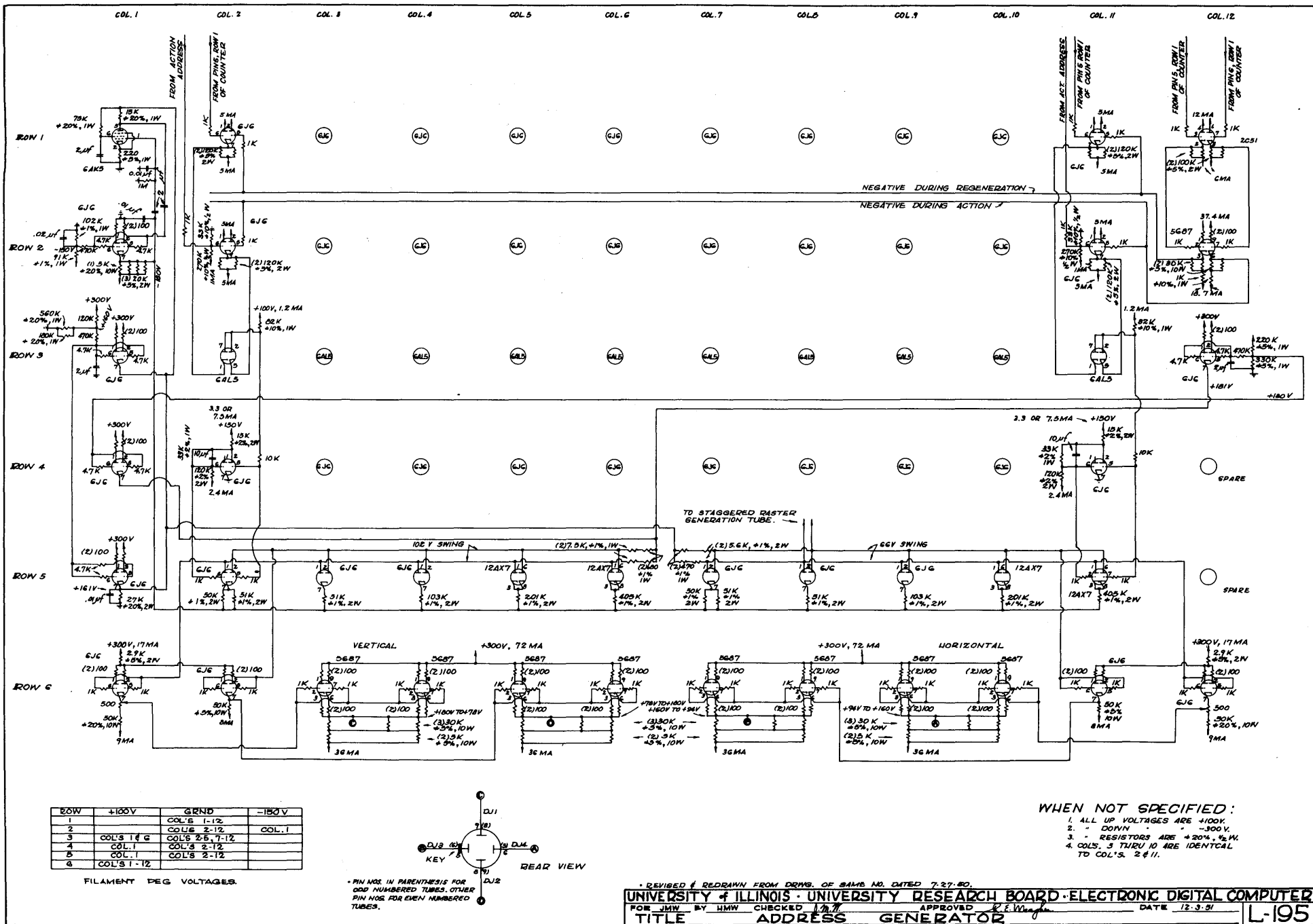
$+149V$
 $+44V$
 TO GRIDS OF
 CLEAR DRIVERS

$+149V$
 $+44V$
 TO GRIDS OF
 CLEAR DRIVERS.

NOTES

1. FILAMENTS AT +100V.
2. UNLESS OTHERWISE SPECIFIED, RESISTORS ARE $\frac{1}{2}W$, $\pm 20\%$.

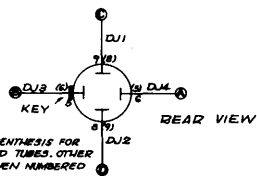
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 ELECTRONIC DIGITAL COMPUTER
 DRAWN FOR REM DRAWN BY H.M.W.
 CHECKED R.E.M. APPROVED R.E.M.
 TITLE CLEAR DR. DR. R.III
 DATE 7-18-50 DRWG. NO. 194



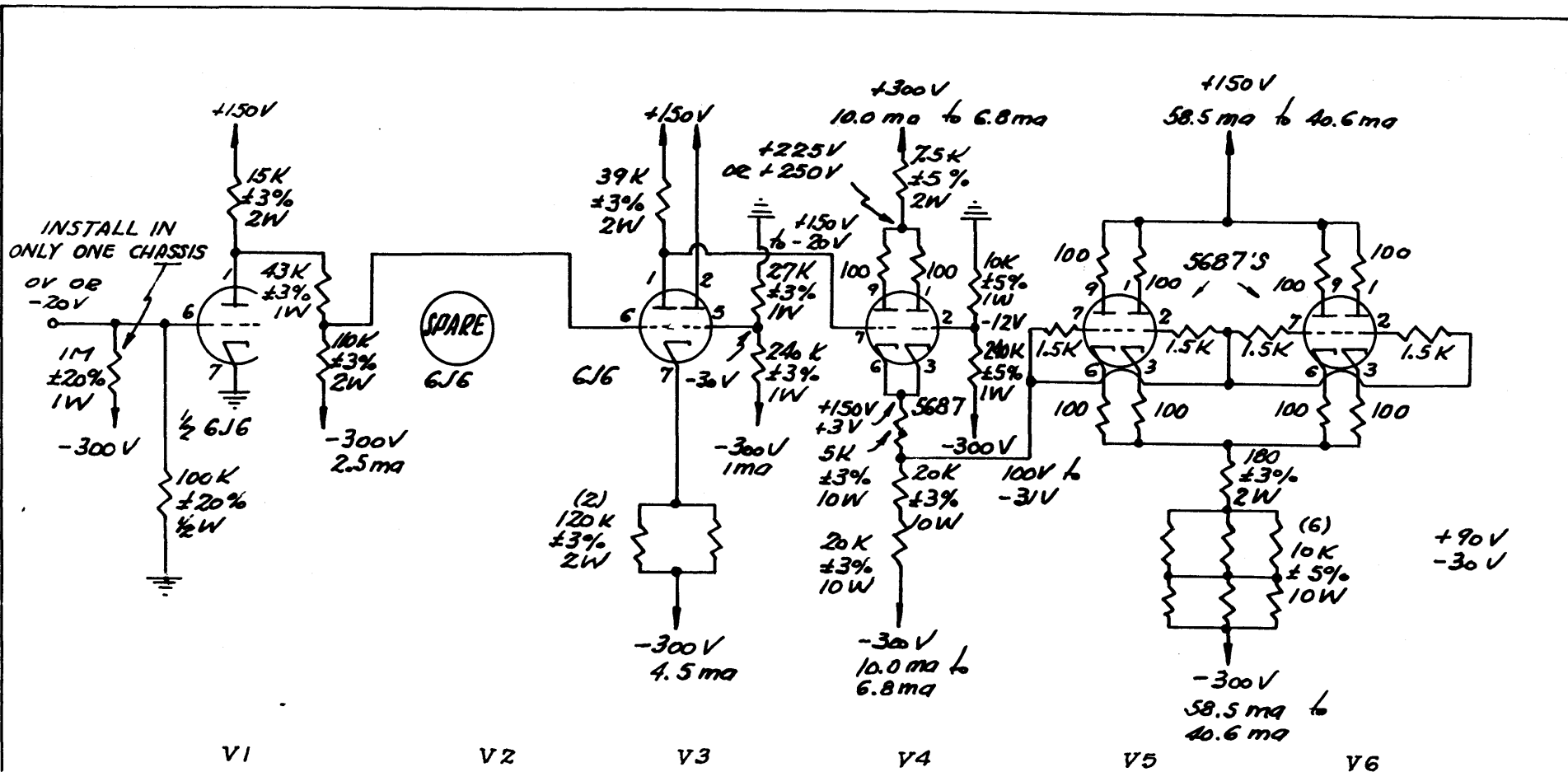
ROW	+100V	GRND	-150V
1		COL'S 1-12	
2		COL'S 2-12	
3	COL'S 1 & 6	COL'S 2, 5, 7-12	COL. 1
4	COL. 1	COL'S 2-12	
5	COL. 1	COL'S 2-12	
6	COL'S 1-12		

FILAMENT PEG VOLTAGES.

* PIN NOS. IN PARENTHESIS FOR ODD NUMBERED TUBES. OTHER PIN NOS. FOR EVEN NUMBERED TUBES.



WHEN NOT SPECIFIED:
 1. ALL UP VOLTAGES ARE +100V.
 2. - DOWN -300V.
 3. - RESISTORS ARE +20% 1/4W.
 4. COLS. 3 THRU 10 ARE IDENTICAL TO COL'S. 2 & 11.



~ NOTES ~

1. FILAMENTS OF V1 & V3 AT GRND.
2. " " V4, V5, V6 AT +65V.
3. UNLESS OTHERWISE SPECIFIED RESISTORS ARE 1/2W, ± 20%.
4. MAKE TWO PER ARITHMETIC UNIT.

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ELECTRONIC DIGITAL COMPUTER

DRAWN FOR REM DRAWN BY H-MW

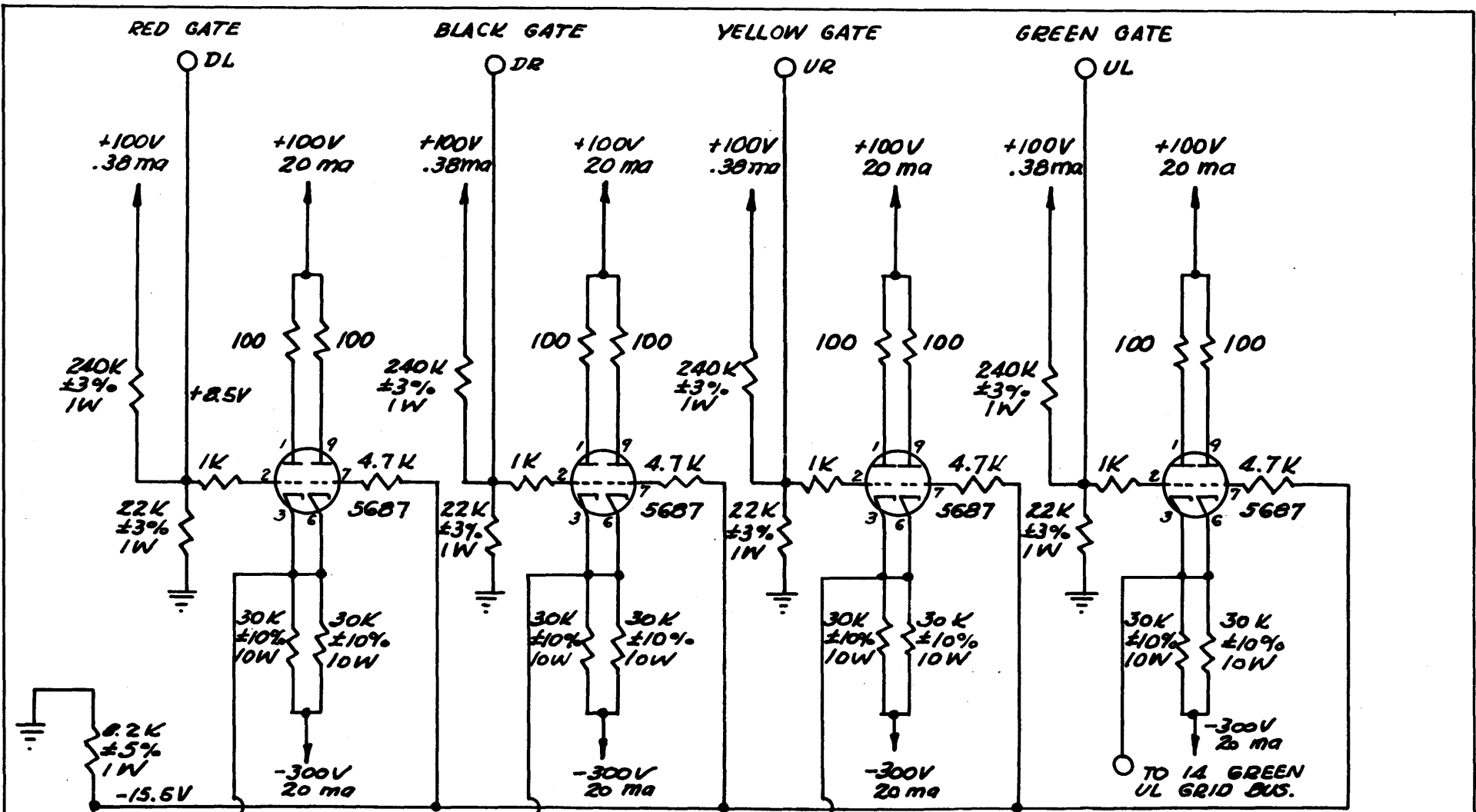
CHECKED R.E.W. APPROVED R.E. Wengler

TITLE COMPLEMENT

GATE DRIVER

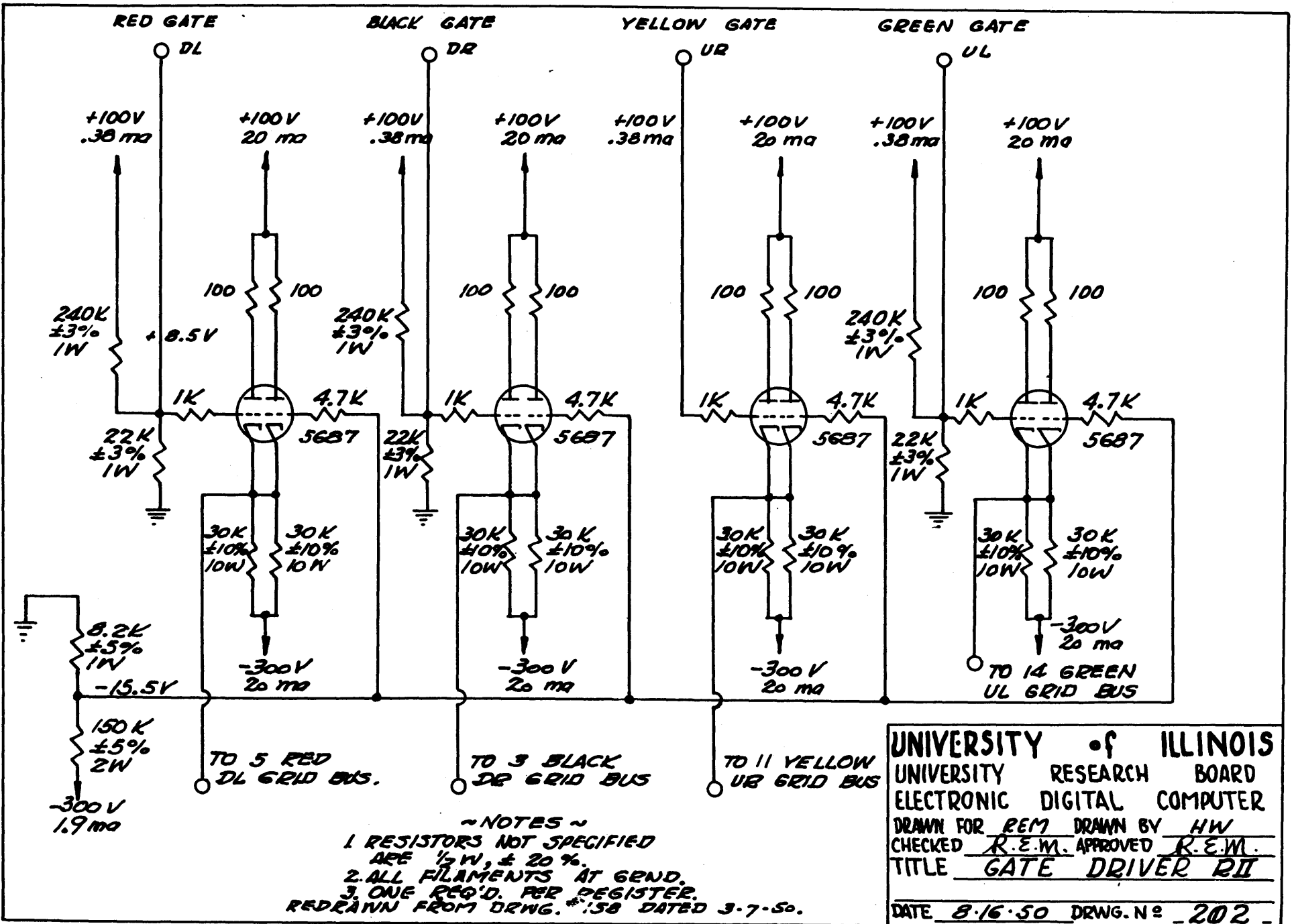
DATE 8.3.50 DRWG. N= 198





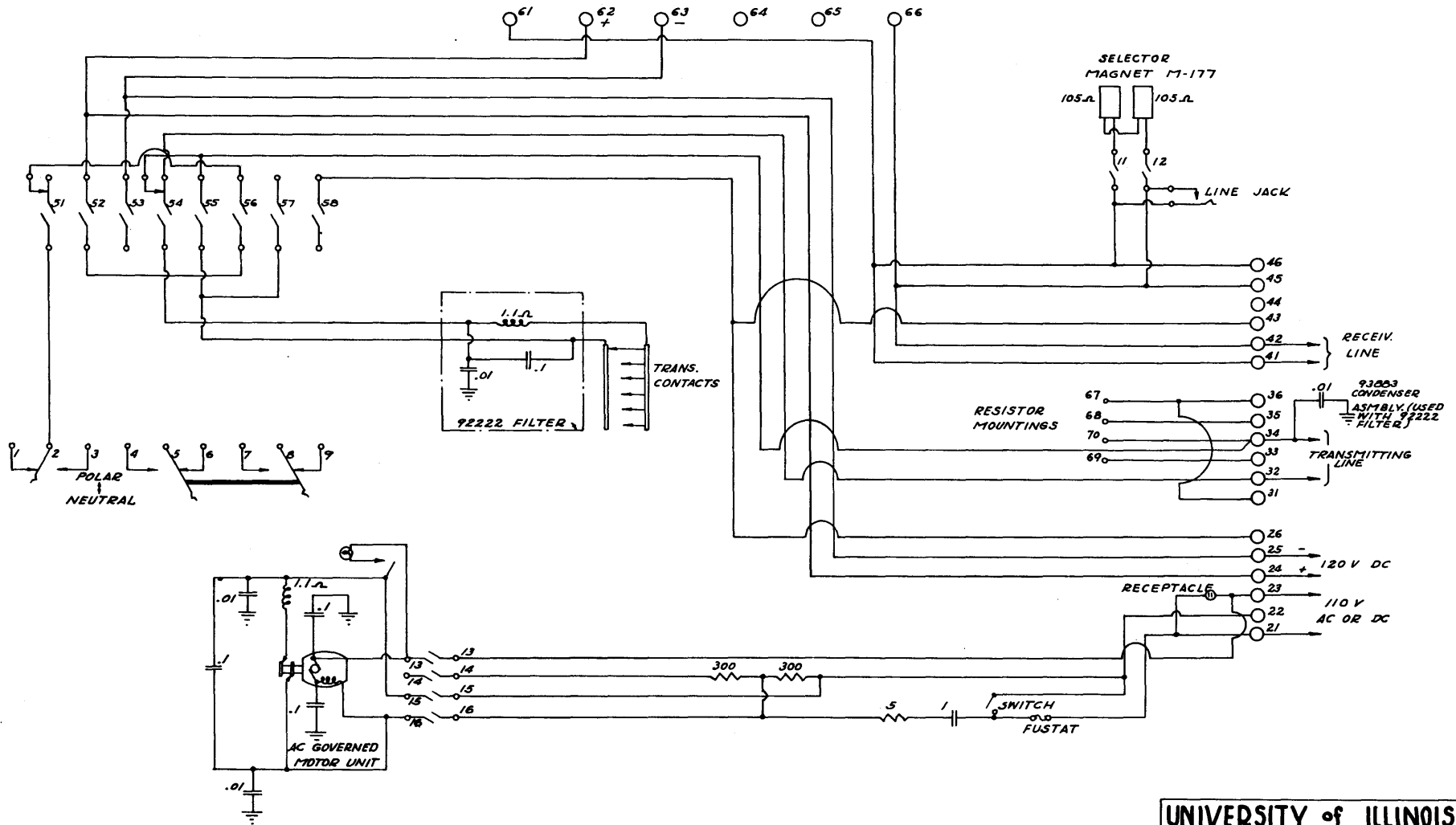
~ NOTES ~
 1. RESISTORS NOT SPECIFIED ARE 1/2W, ± 20%.
 2. ALL FILAMENTS AT GRND.
 3. ONE REQ'D. PER REGISTER.
 REDRAWN FROM DRWG. # 158 DATED 3-7-50.

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 DRAWN FOR REM DRAWN BY Hw
 CHECKED R.Z.M. APPROVED R.E.M.
 TITLE GATE DRIVER RI
 DATE 8-16-50 DRWG. N° 201

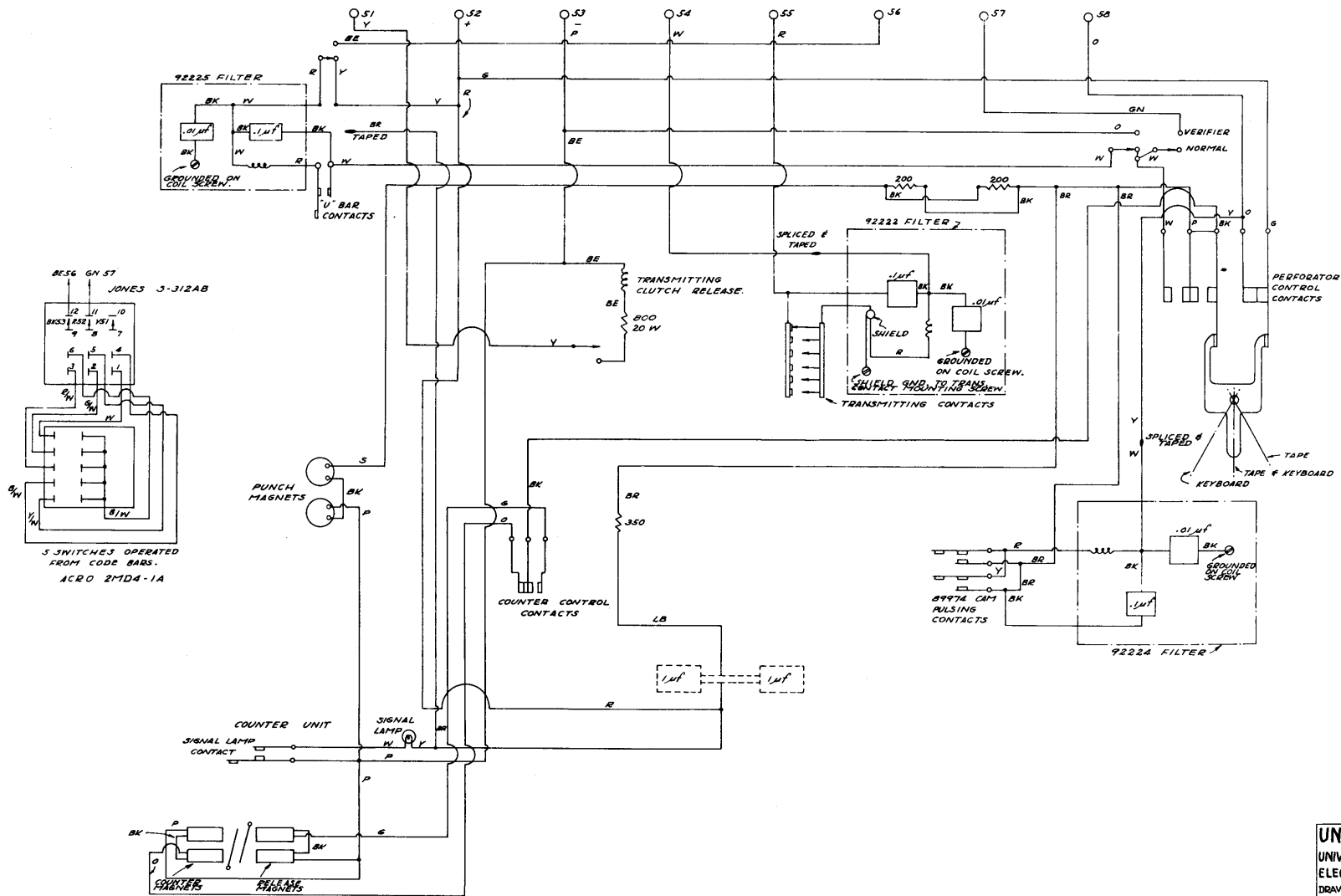


~NOTES~
 1. RESISTORS NOT SPECIFIED ARE 1/2 W, ± 20%.
 2. ALL FILAMENTS AT 6.25V.
 3. ONE REQ'D. PER REGISTER.
 REDRAWN FROM DRWG. #158 DATED 3-7-50.

UNIVERSITY of ILLINOIS
 UNIVERSITY RESEARCH BOARD
 ELECTRONIC DIGITAL COMPUTER
 DRAWN FOR REM DRAWN BY HW
 CHECKED R.E.M. APPROVED R.E.M.
 TITLE GATE DRIVER RII
 DATE 8-16-50 DRWG. No. 202



UNIVERSITY of ILLINOIS
 UNIVERSITY RESEARCH BOARD
 ELECTRONIC DIGITAL COMPUTER
 DRAWN FOR T.S. DRAWN BY H.WALKER
 CHECKED BY SHAPIN APPROVED BY R.E. WALKER
 TITLE MODIFIED SCHEMATIC -
 15 PRINTER SET WITH KEYBOARD
 DATE 7-13-50 DRWG. NO. 208



UNIVERSITY of ILLINOIS
 UNIVERSITY RESEARCH BOARD
 ELECTRONIC DIGITAL COMPUTER
 DRAWN FOR T.S. DRAWN BY H.W.
 CHECKED BY E.M. APPROVED R.E.W.
 TITLE WIRING - IS TYPE PERFORATOR
 TRANS. MOD. FOR VERIFIER
 DATE 9.14.50 DRWG. NO. 209

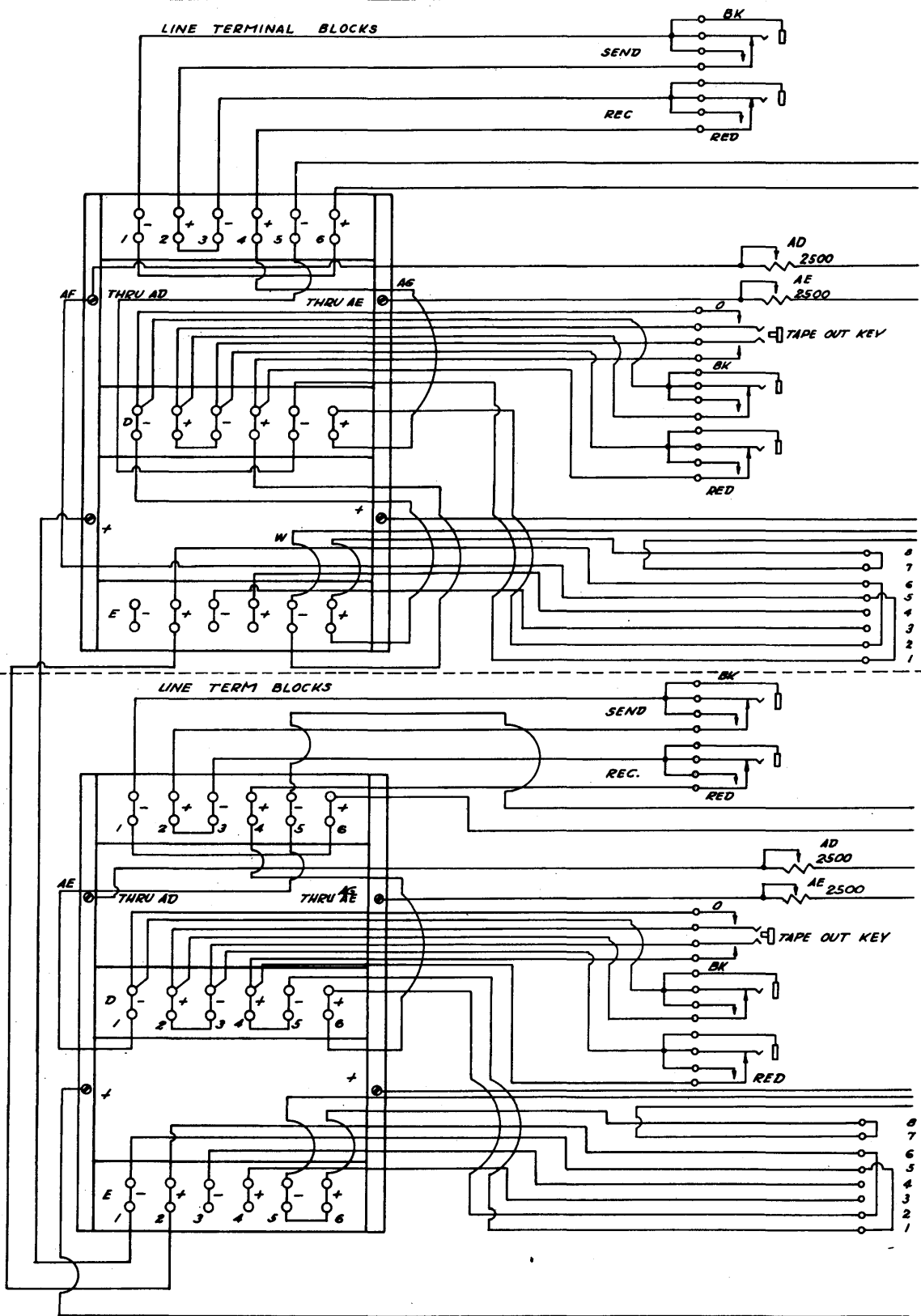
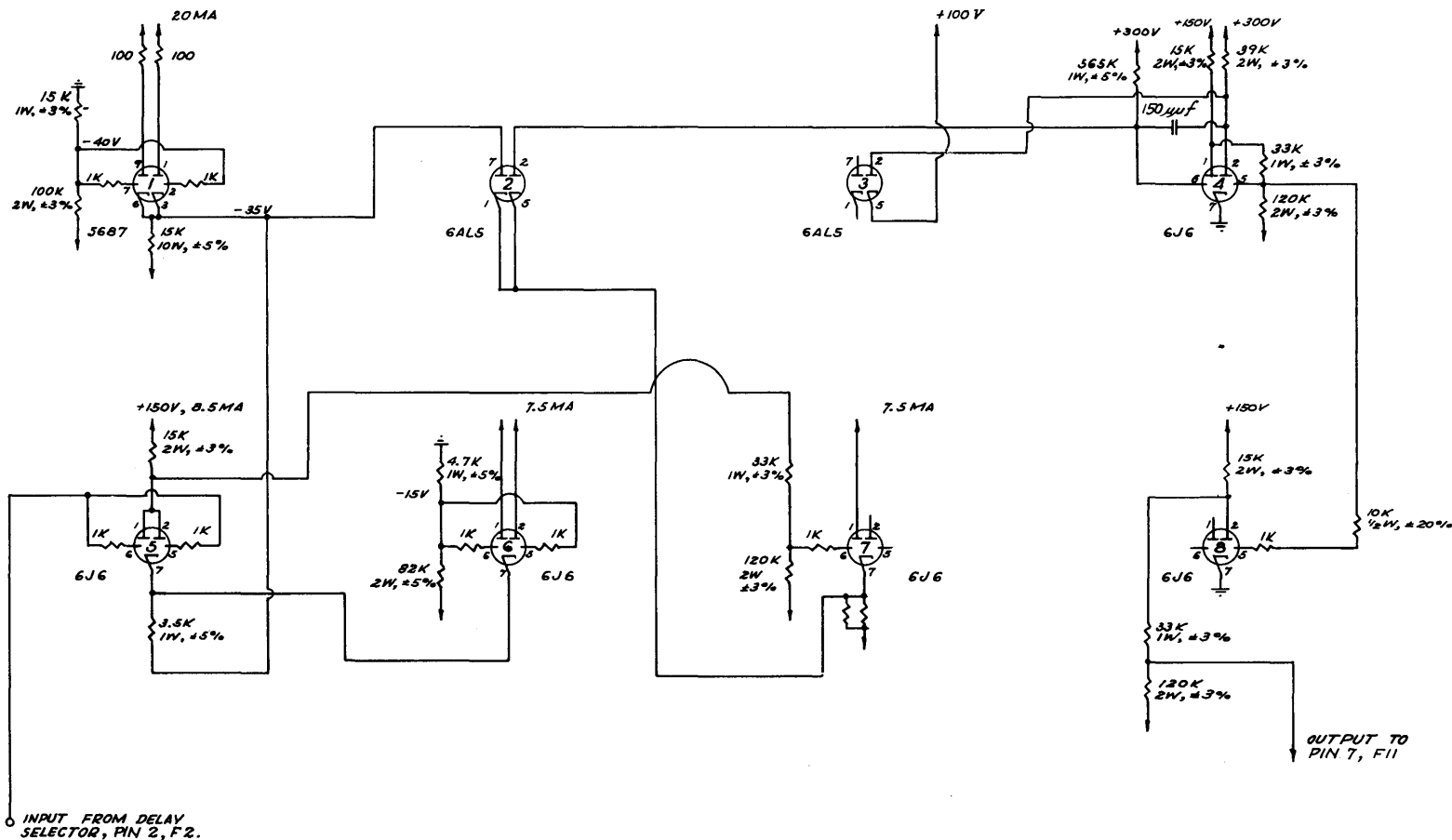


TABLE B
TABLE A

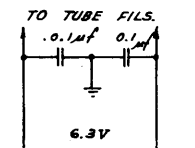
REFER TO DRWS. WD 2161-6 FOR ALL WIRING NOT SHOWN.

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UNIVERSITY RESEARCH BOARD
ELECTRONIC DIGITAL COMPUTER
DRAWN FOR T.S. DRAWN BY H. WALKER
CHECKED T. SHAPIR APPROVED R.E. WALKER
TITLE MODIFICATION OF TELETYPE TABLE DRWG. WD 2161-6
DATE 7-19-50 DRWG. N^o 210-

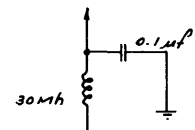


WHEN NOT SPECIFIED:

1. ALL UP VOLTAGES ARE +100V.
2. - DOWN - -300V.
3. - RESISTORS ARE 120K, 2W, ±10%.
4. - TOLERANCES ARE ½W, ±50%.
5. - FILAMENTS AT GROUND.



FILTER FOR FILAMENT VOLTAGES



FILTER FOR DC VOLTAGES.

REVISED 1.8.50 JMK



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ELECTRONIC DIGITAL COMPUTER

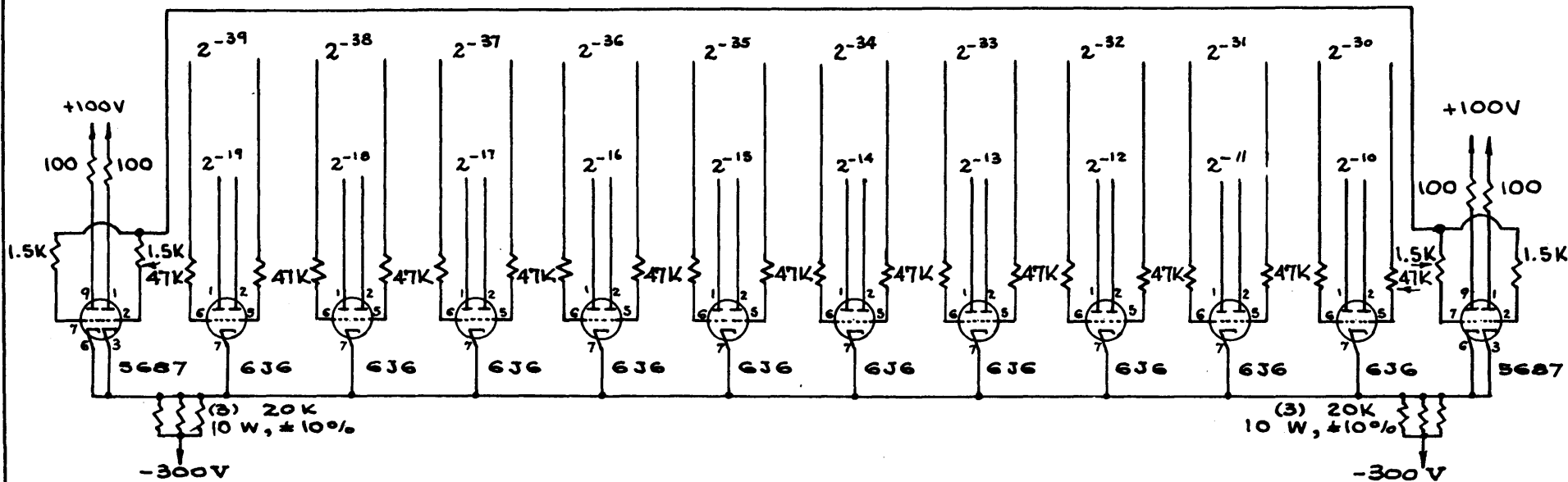
DRAWN FOR J.M. DRAWN BY HANK W.

CHECKED J.M. APPROVED R.E. Meagher

TITLE CARRY DELAY II

DATE DEC. 18, 1950

M-236



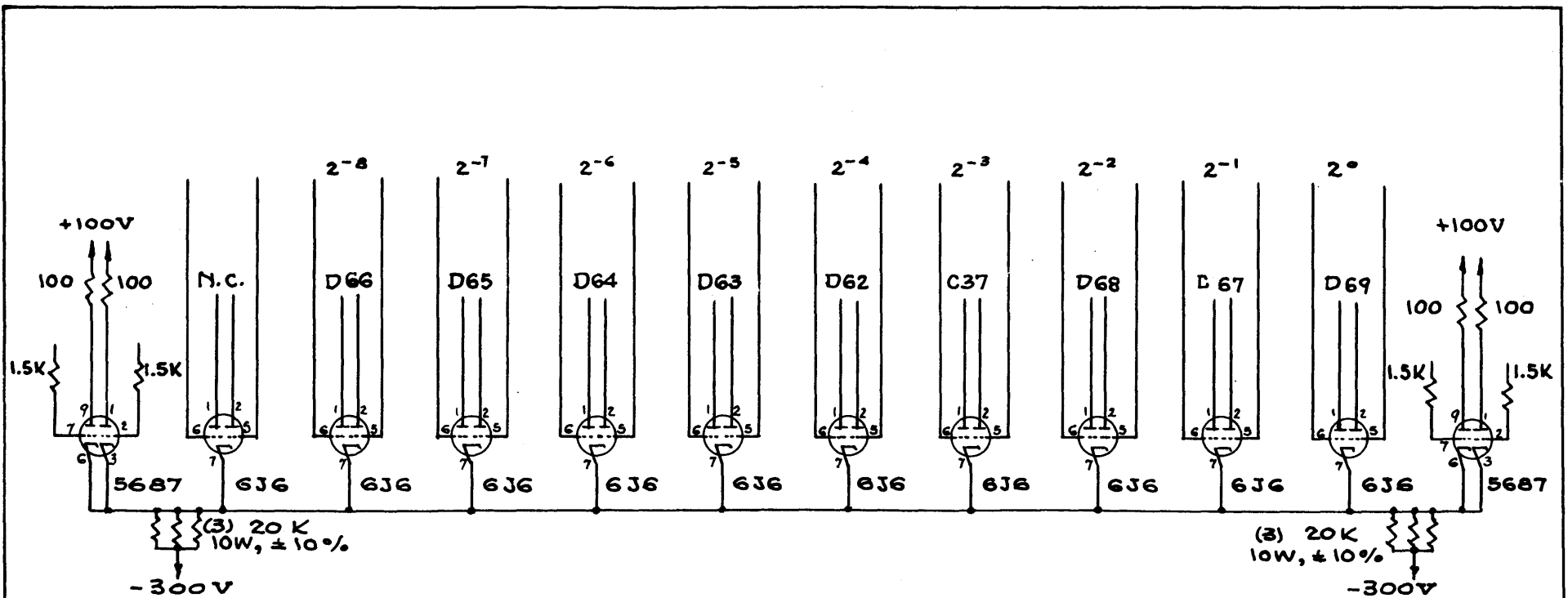
ODDVAC!

~ NOTES ~

1. PLATES CONNECT TO SAME PLATES OF R₃ FLIP-FLOPS WHOSE NUMBERS ARE SHOWN.
2. GRIDS COME FROM SAME GRIDS OF R₃ FLIPFLOPS WHOSE NUMBERS ARE SHOWN.
3. 5687 GRIDS CONNECT TO ODD ADDRESS GATE DRIVER
4. ALL FILAMENTS AT GROUND.
5. RESISTORS NOT SPECIFIED ARE 1/2W, ± 20%.

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UNIVERSITY RESEARCH BOARD	
ELECTRONIC DIGITAL COMPUTER	
DRAWN FOR	DRAWN BY
CHECKED	APPROVED
TITLE ODD ADDRESS GATE CHASSIS	
DATE 1-16-51 DRWG. N ^o 249-	





ORDVAC!

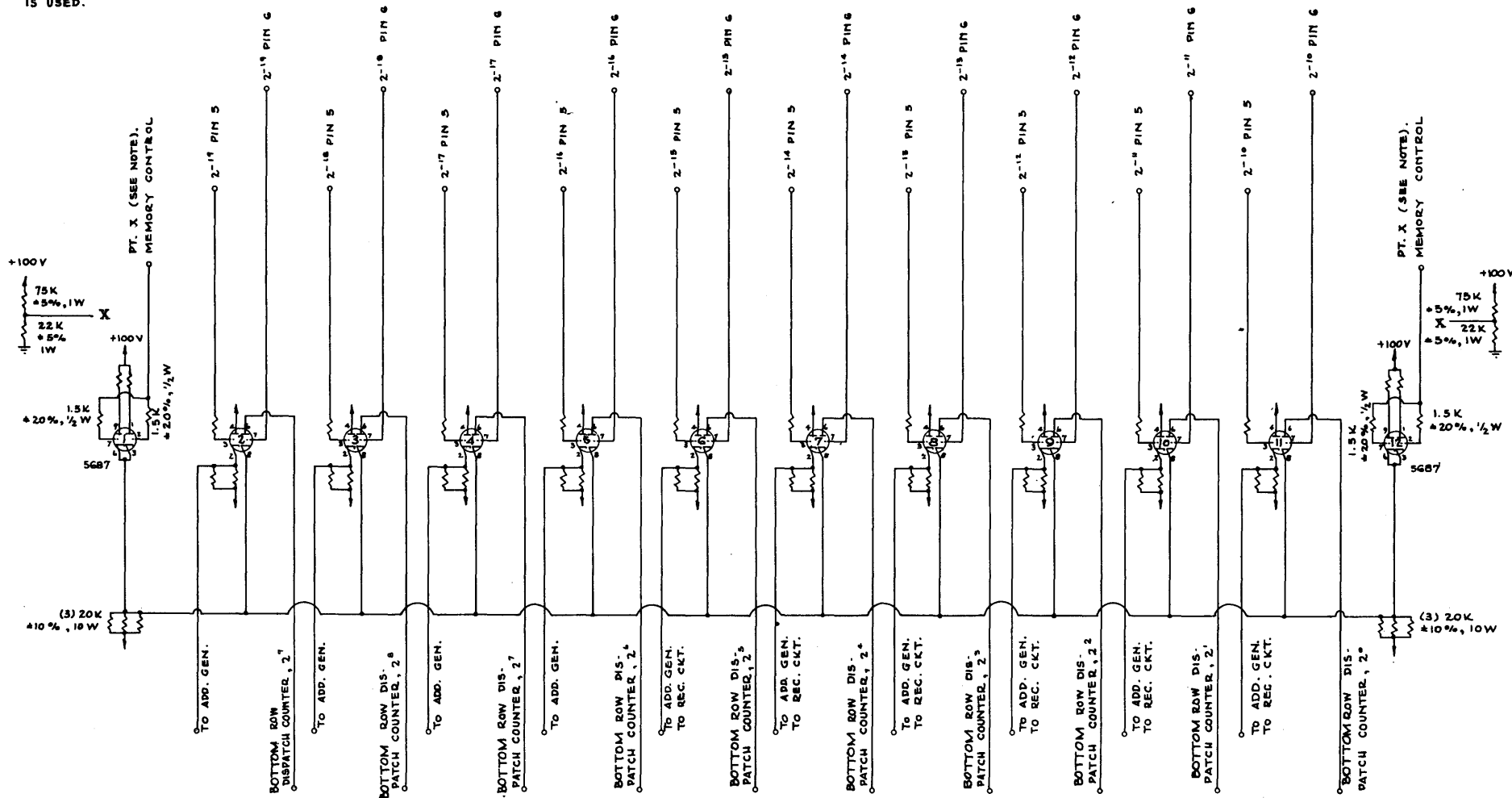
~NOTES~

1. PLATES CONNECT TO SAME PLATES OF DECODING CHASSIS FLIP-FLOPS WHOSE NUMBERS ARE SHOWN.
2. GRIDS COME FROM SAME GRIDS OF R_3 FLIPFLOPS WHOSE NUMBERS ARE SHOWN.
3. 5687 GRIDS CONNECT TO EVEN ORDER GATE DRIVER.
4. ALL FILAMENTS AT GROUND.
5. ALL RESISTORS NOT SPECIFIED ARE $\frac{1}{2}W$, $\pm 20\%$.

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UNIVERSITY RESEARCH BOARD	
ELECTRONIC DIGITAL COMPUTER	
DRAWN FOR JPN	DRAWN BY HMW.
CHECKED <i>JPN</i>	APPROVED <i>P.E. Meagher</i>
TITLE EVEN ORDER	
GATE CHASSIS	
DATE 1-16-51	DRWG. NO. 251

(A-A)

POINT X TO BE TIED IN
UNTIL MEMORY CONTROL
IS USED.



WHEN NOT SPECIFIED:

1. ALL PLATE RESISTORS ARE 100, + 20%, 1/2 W.
2. " GRID RESISTORS ARE 10K, + 20%, 1/2 W.
3. " CATHODE " 120K, + 10%, 2W.
4. " UP VOLTAGES ARE +100V.
5. " DOWN " ARE - 300V.
6. " TUBES ARE 2CD1'S.

ORDVAC!

REVISED & REDRAWN FROM DRWG. OF SAME NO. DATED 1-17-51.

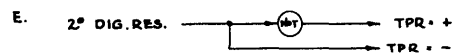
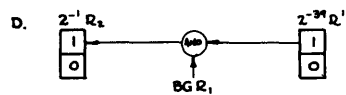
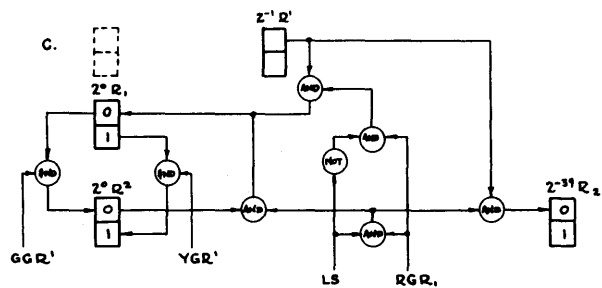
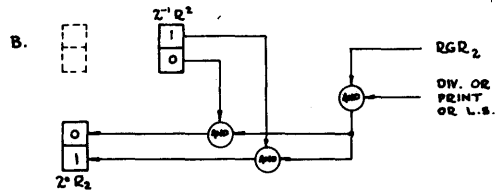
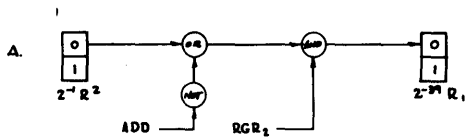
UNIVERSITY OF ILLINOIS · UNIVERSITY RESEARCH BOARD · ELECTRONIC DIGITAL COMPUTER

FOR J.F.N. BY W.M.W. CHECKED *O. P. Mack* APPROVED *E. E. Meagher* DATE 4-17-51

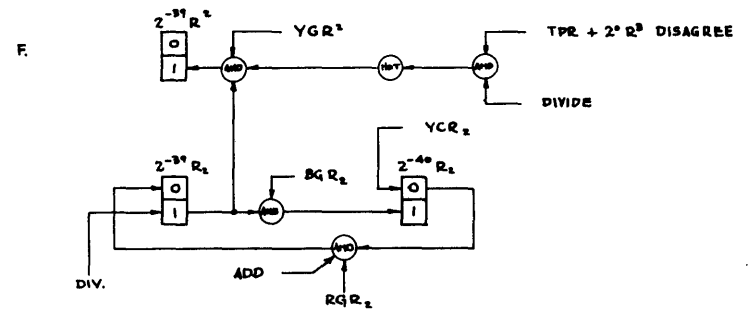
TITLE ~ EVEN ADDRESS CATHODE FOLLOWER CHASSIS

M-252

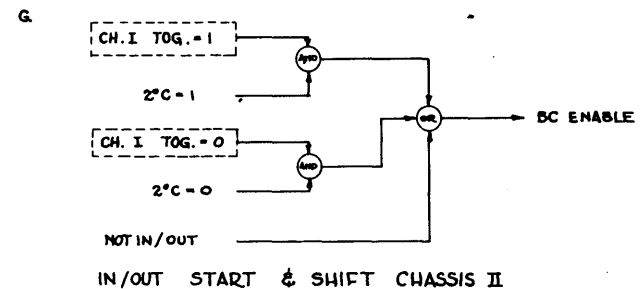
DD



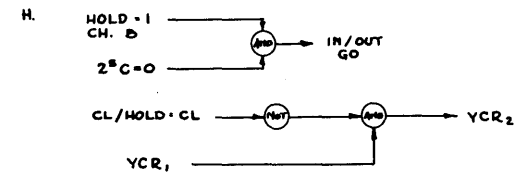
END CONNECTIONS



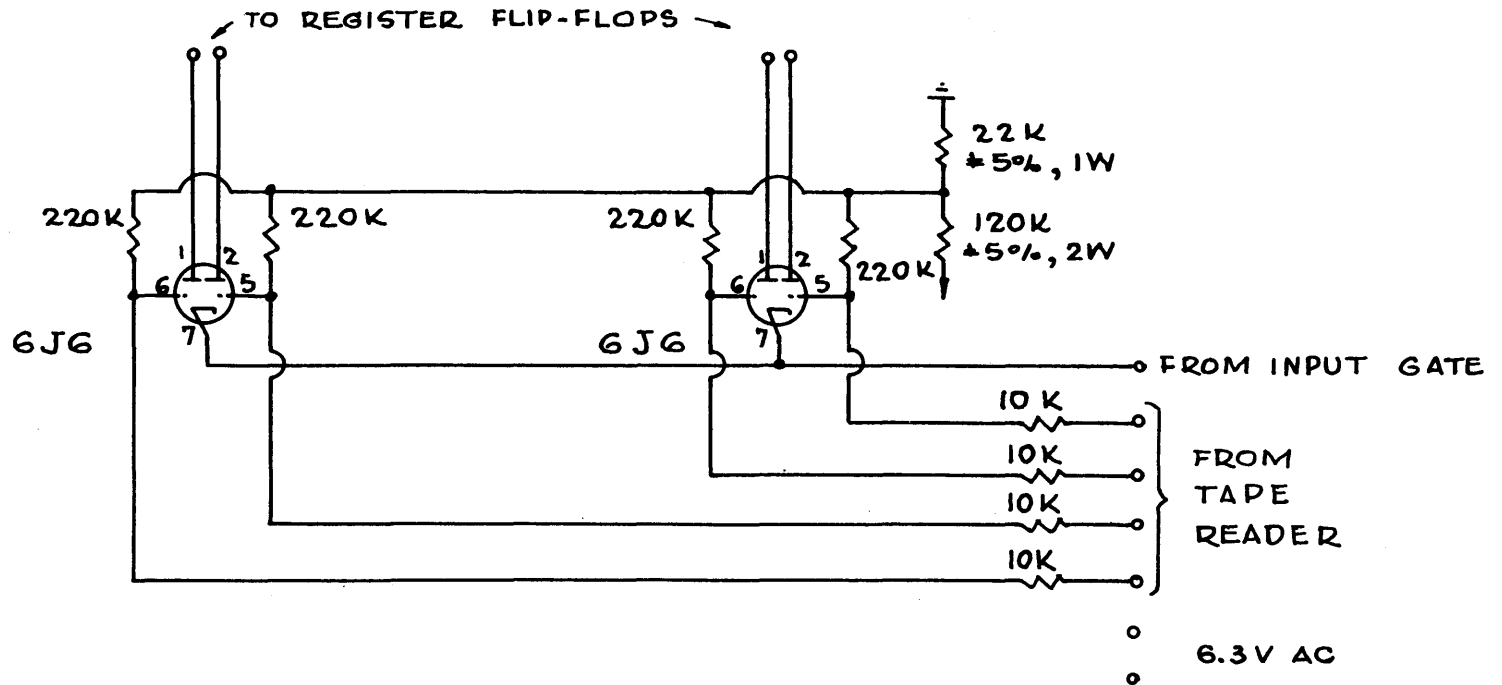
END CONNECTIONS



IN/OUT START & SHIFT CHASSIS II



COUNTER OUTPUT CHASSIS



ALL RESISTORS NOT SPECIFIED ARE ±20%, 1/2 W.

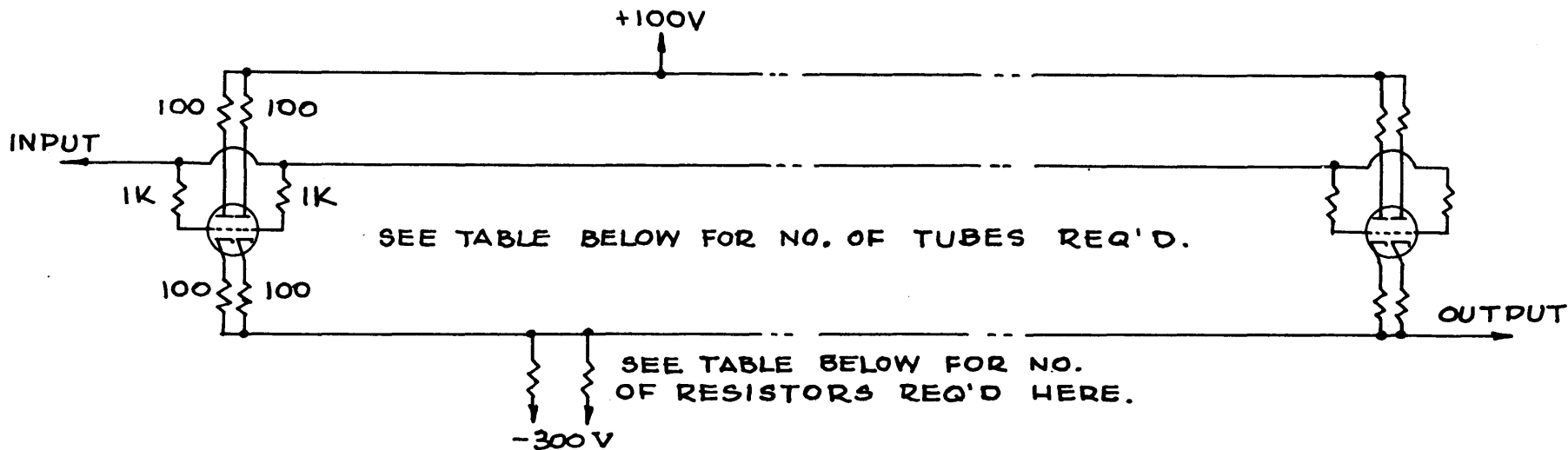
REDRAWN FROM DRWG OF SAME NO. DATED 1.22.51.

UNIVERSITY OF ILLINOIS UNIVERSITY RESEARCH BOARD ELECTRONIC DIGITAL COMPUTER

FOR T.S. BY HMW CHECKED T. SHAPIR APPROVED R. E. Mengler DATE 6.25.51

TITLE - INPUT GATES FOR INPUT CIRCUIT

S-259



THREE SECTIONS REQUIRED :

SECT I - DASH TEST	22 TUBES	50 - 20K, +10%, 10W RESISTORS
SECT. II - DASH END	10 "	20 " " " "
SECT. III - DOT	3 "	3 " " " "

ALL TUBES ARE 5687'S . RESISTORS NOT SPECIFIED ARE $\pm 20\%$, $1/2$ W.

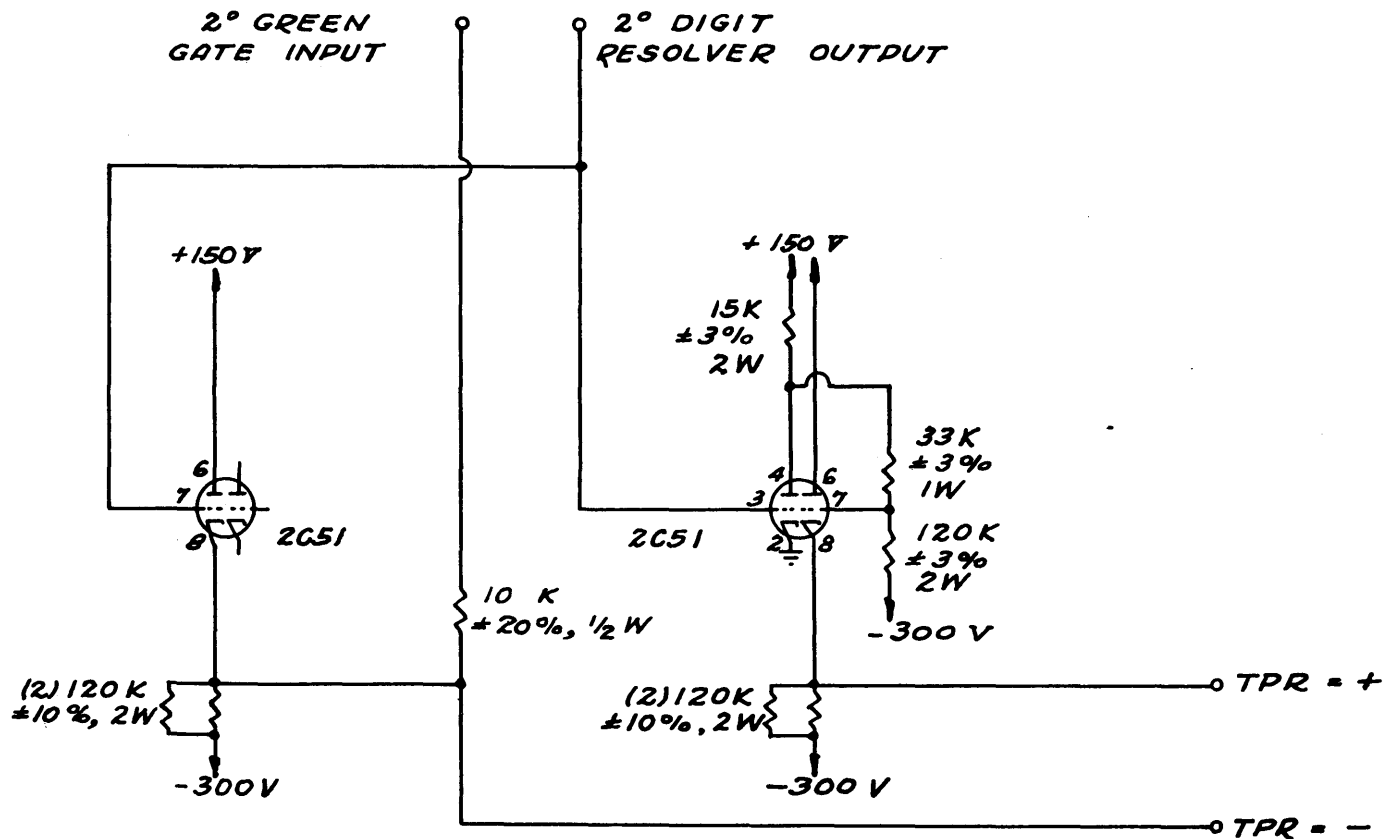
REDRAWN FROM DRWG. OF SAME NO. DATED 1-26-51.

UNIVERSITY of ILLINOIS · UNIVERSITY RESEARCH BOARD · ELECTRONIC DIGITAL COMPUTER

FOR ELH BY HMW CHECKED W. JONES APPROVED R. Z. Meagher DATE 6-25-51

TITLE ~ WILLIAMS IV PULSE CATHODE FOLLOWERS

S-261



ALL FILS. AT GROUND.

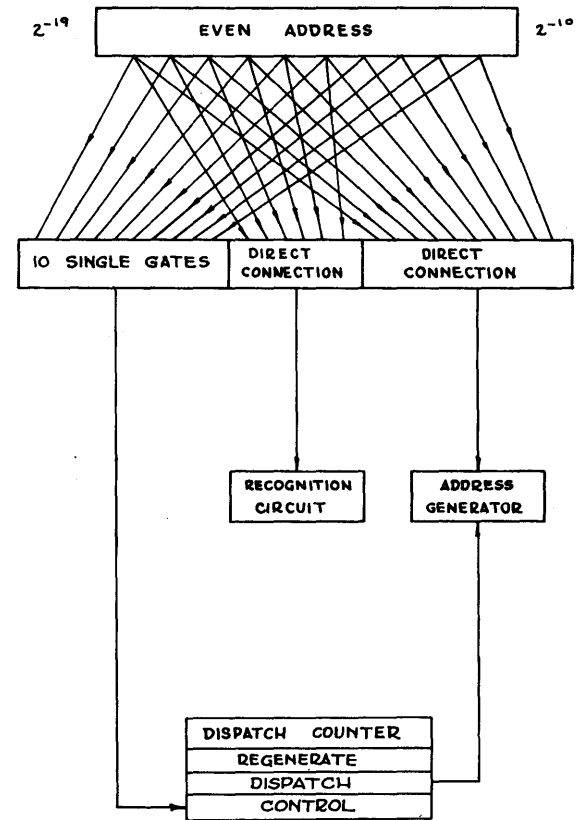
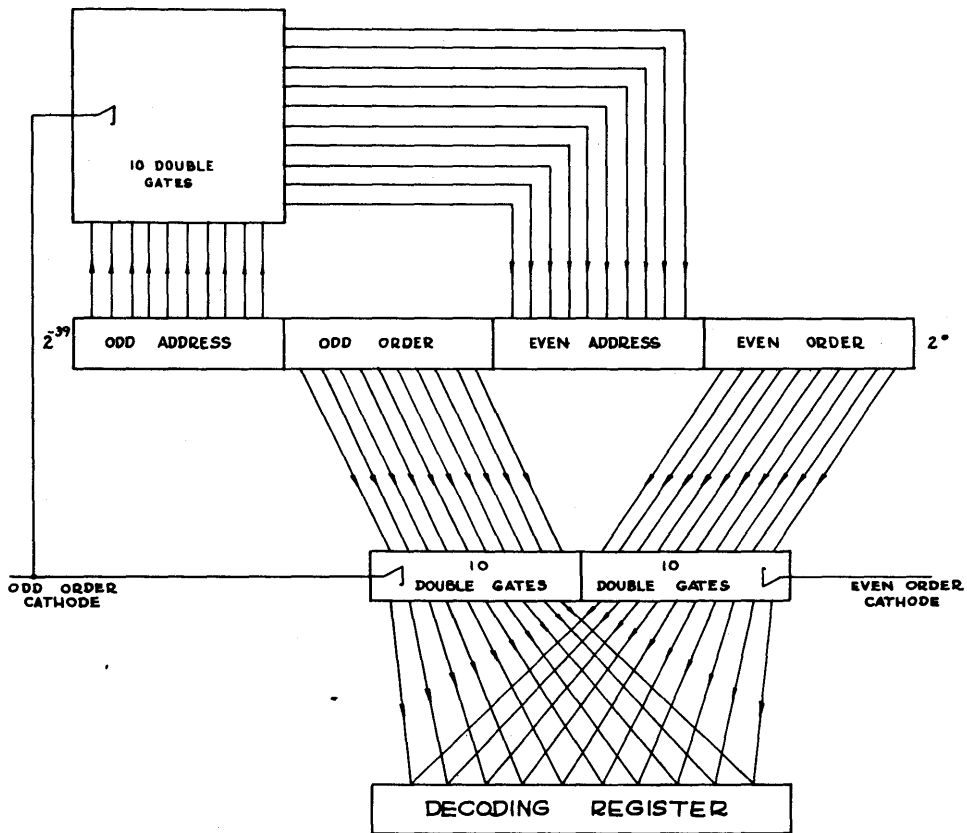
REDRAWN FROM DRAWG. OF SAME NO. DATED 2.6.51.

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FOR E.L.H. BY H.M.W. CHECKED ELR APPROVED R.E. Meagher DATE 3.19.51

TITLE TPR OUTPUT CONNECTIONS

S.265



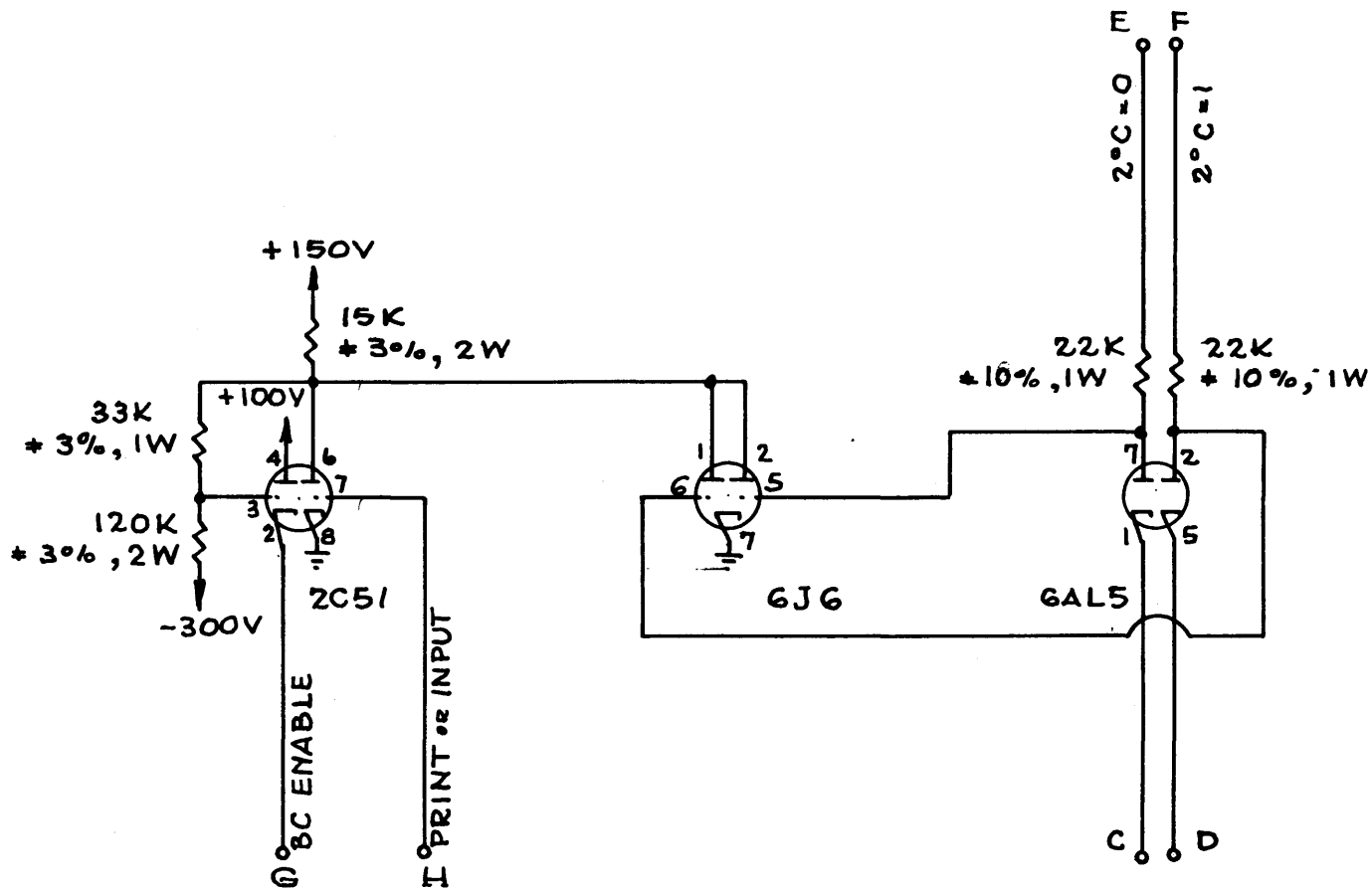
REVISED ~ 7-5-51 - JPN

UNIVERSITY of ILLINOIS · UNIVERSITY RESEARCH BOARD · ELECTRONIC DIGITAL COMPUTER

FOR JPN BY HMW CHECKED *JPN* APPROVED *R.E. Meeker* DATE 2-21-51

TITLE GATING FROM R₂

M-266



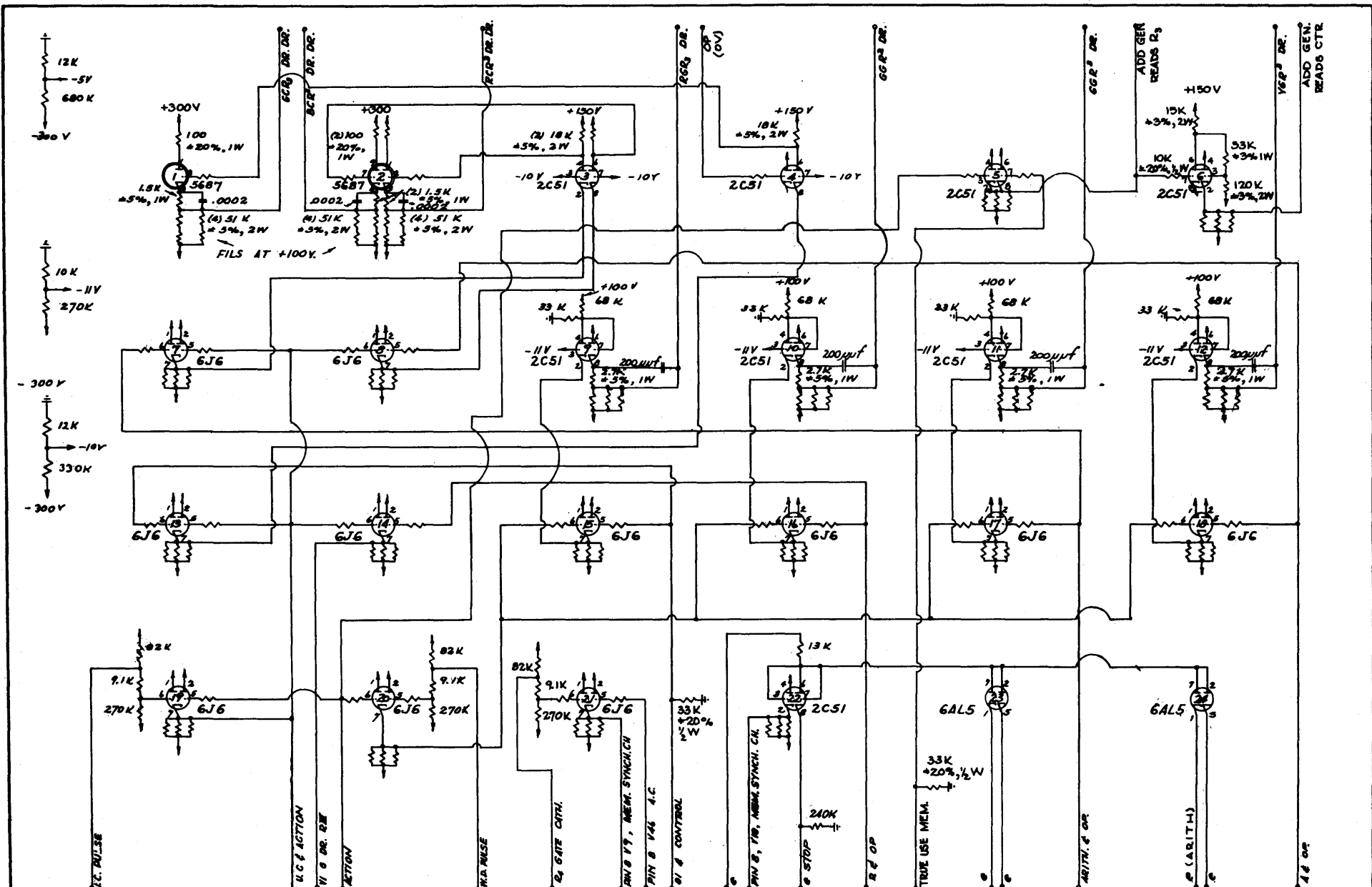
REDRAWN 6-12-51

UNIVERSITY of ILLINOIS · UNIVERSITY RESEARCH BOARD · ELECTRONIC DIGITAL COMPUTER

FOR J.P.N. BY LMW CHECKED *J.P.N.* APPROVED *R.E. Meagher* DATE 6-12-51

TITLE INPUT-OUTPUT START & SHIFT CHASSIS II

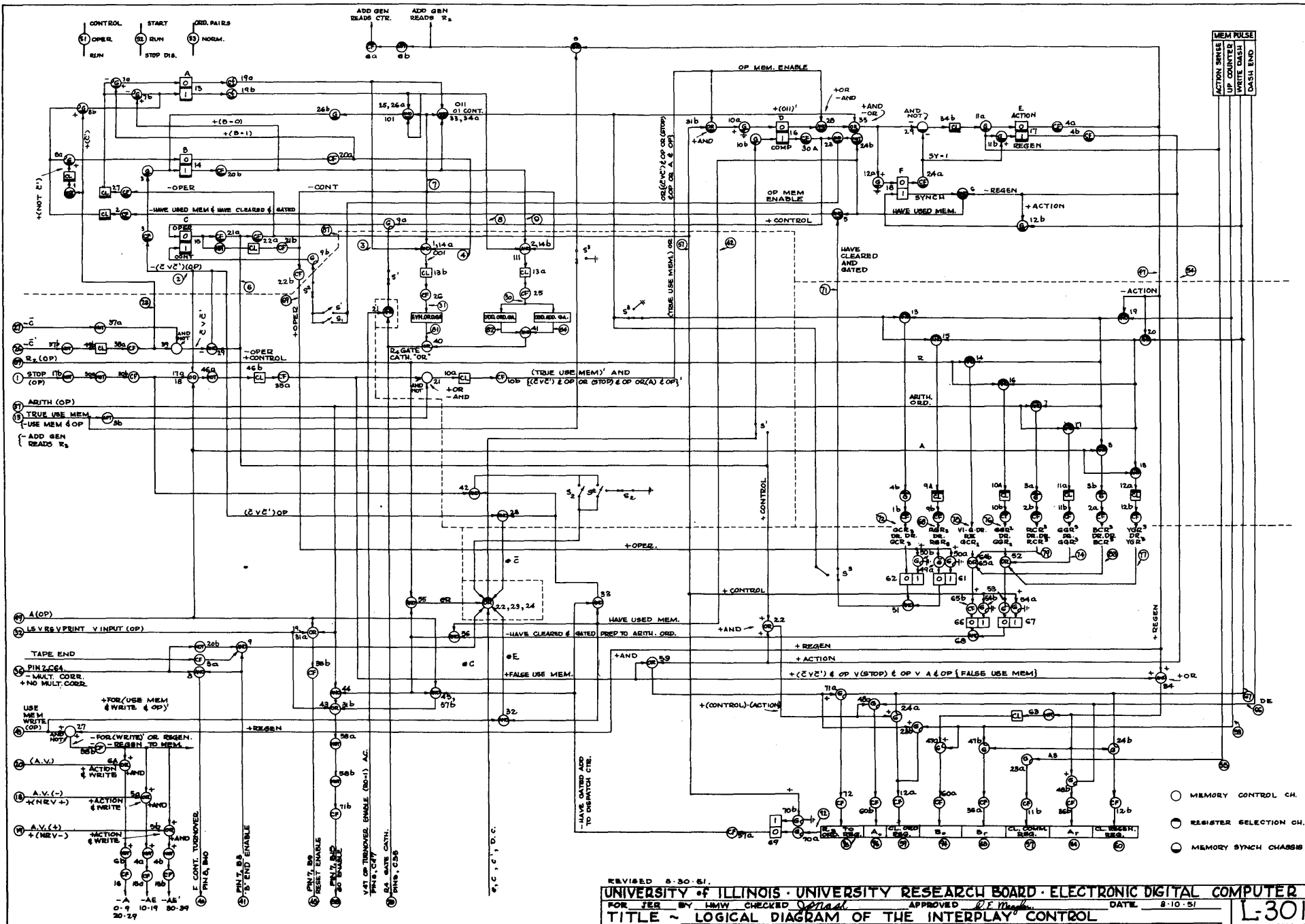
S-271

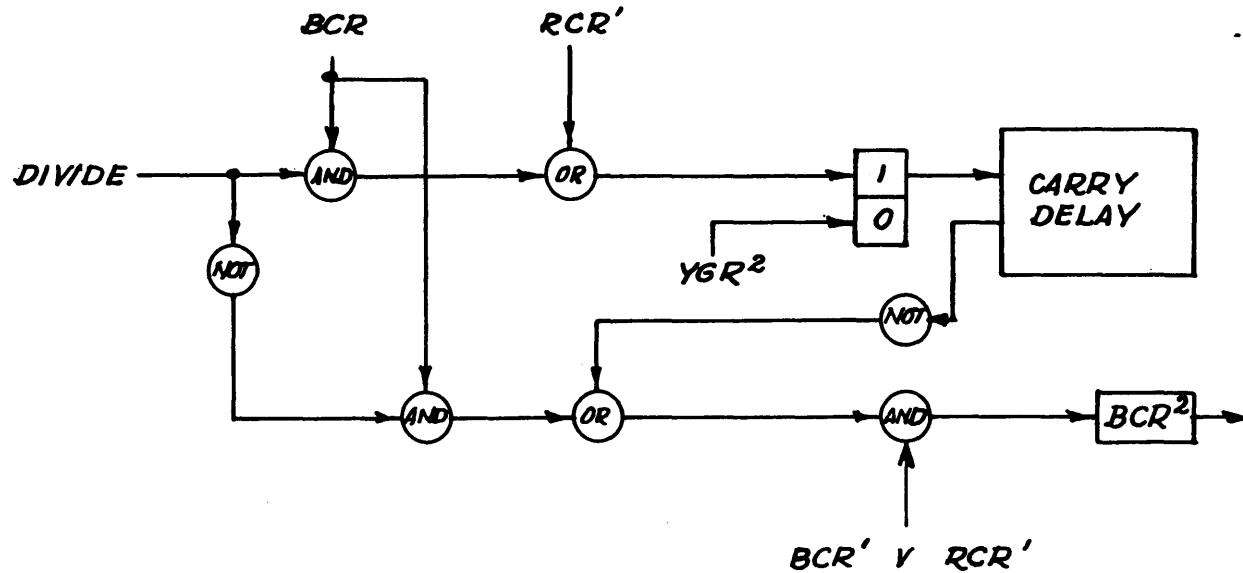
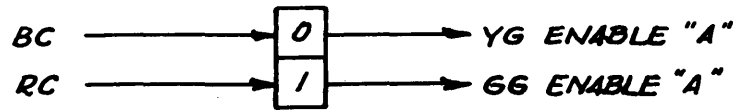


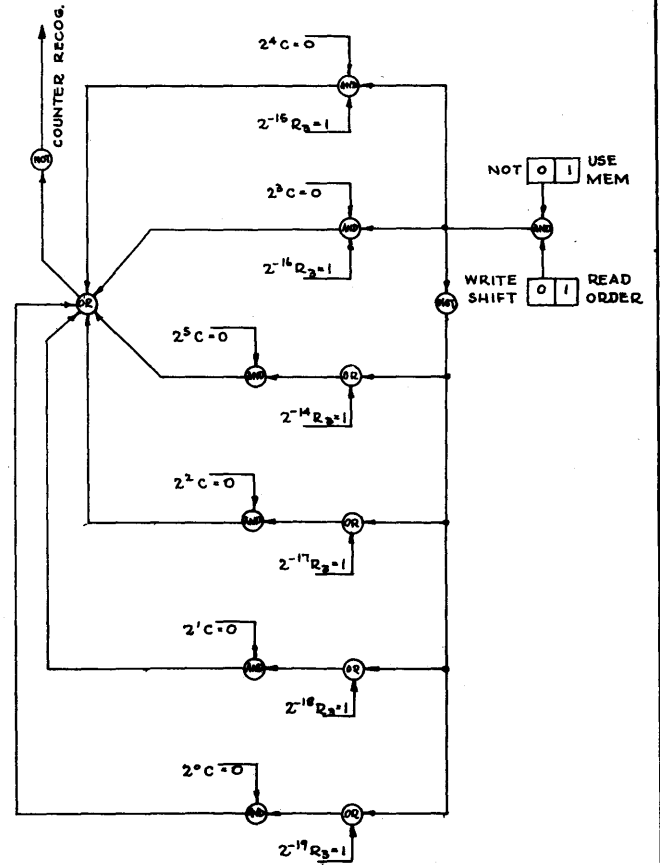
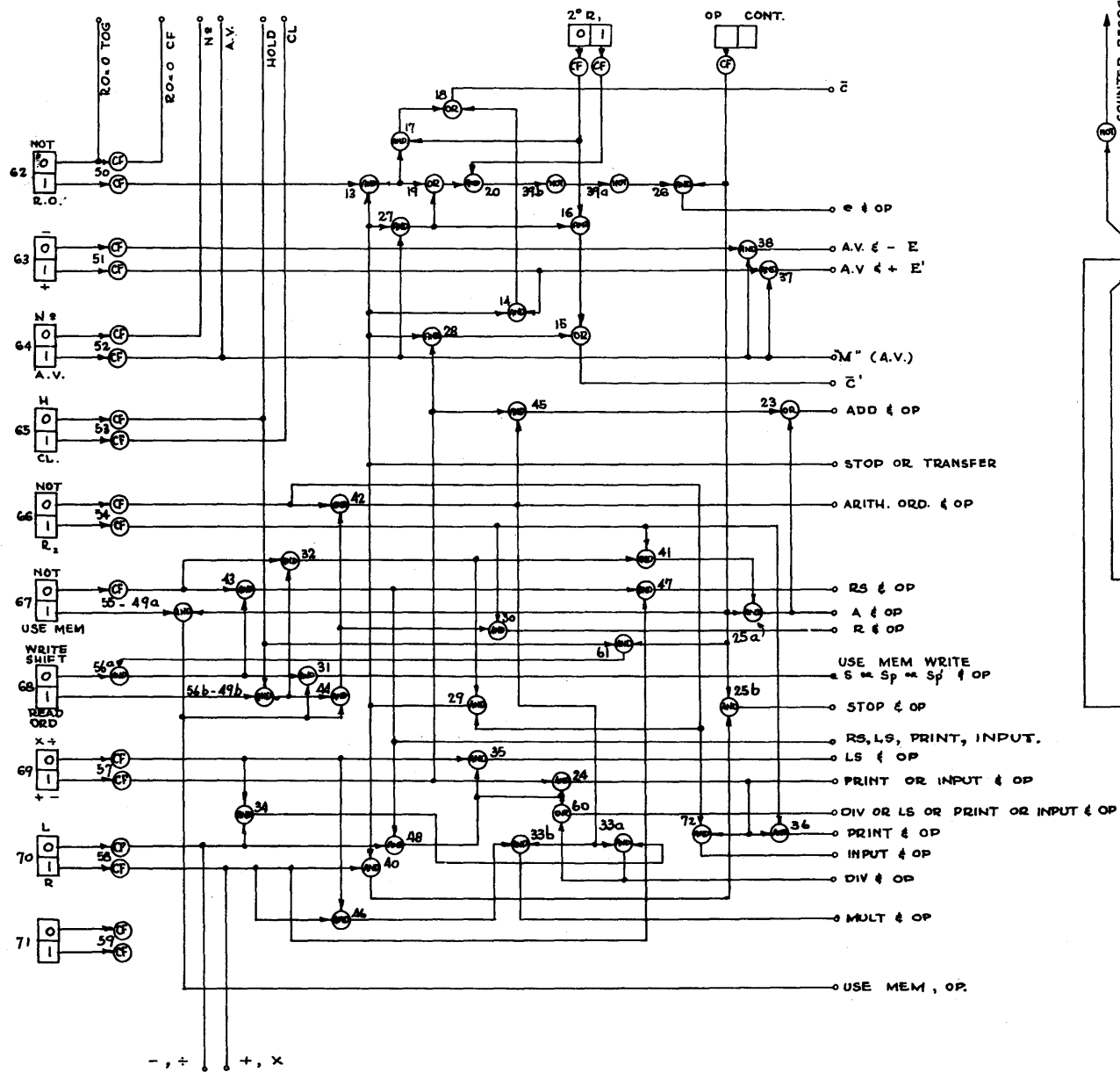
WHEN NOT SPECIFIED:

1. UP VOLTAGES ARE +100V
2. DOWN " " -100V.
3. GRID RESISTORS ARE 1.2K, ±20%, 1/2W.
4. CATH. 120K, ±10%, 2W
5. OTHER NOT SPECIFIED ARE ±3%, 1W.
6. FILS. AT GRND.

LATEST REVISION DATE ~ 8-2-51.
UNIVERSITY OF ILLINOIS · UNIVERSITY RESEARCH BOARD · ELECTRONIC DIGITAL COMPUTER
 FOR I.R.N. BY H.M.L.W. CHECKED *J.P. Nash* APPROVED *R.E. Mangan* DATE 4-30-51
TITLE REGISTER SELECTION CHASSIS **M-288**







DECODING REGISTER CODE

FLIPFLOP	62	63	64	65	66	67	68	69	70	71
I	ROUND OFF	+	A.V.	CLEAR	R ₂	USE MEM	READ ORD	+ -	R	
O	NOT	-	NO.	HOLD	NOT	NOT	WRITE SUIFT	X ÷	L	
+	0	1	1	1	0	1	1	1	1	-
X	1	1	0	1	0	1	1	0	1	-
÷	0	1	1	1	0	1	1	0	0	-
↑	1	-	-	1	-	0	0	-	1	-
↓	1	-	-	1	-	0	0	0	0	-
R	0	-	-	1	1	1	1	1	-	-
A	0	1	1	1	1	0	1	-	1	-
U'	0	0	0	1	0	0	1	1	-	-
C'	0	0	1	1	0	0	1	0	-	-
U	0	1	0	0	0	0	1	0	-	-
C	1	0	0	0	0	0	1	0	-	-
M	1	-	0	1	-	1	0	-	-	-
E	1	1	1	1	-	1	0	-	-	-
E'	0	0	1	1	-	1	0	-	-	-
Z	0	0	0	1	0	0	1	0	1	-
P	-	-	-	-	1	0	0	1	0	
T	-	-	-	-	0	0	0	1	0	

FLIPFLOPS MARKED ARE SENSED, OTHERS MERELY SET.

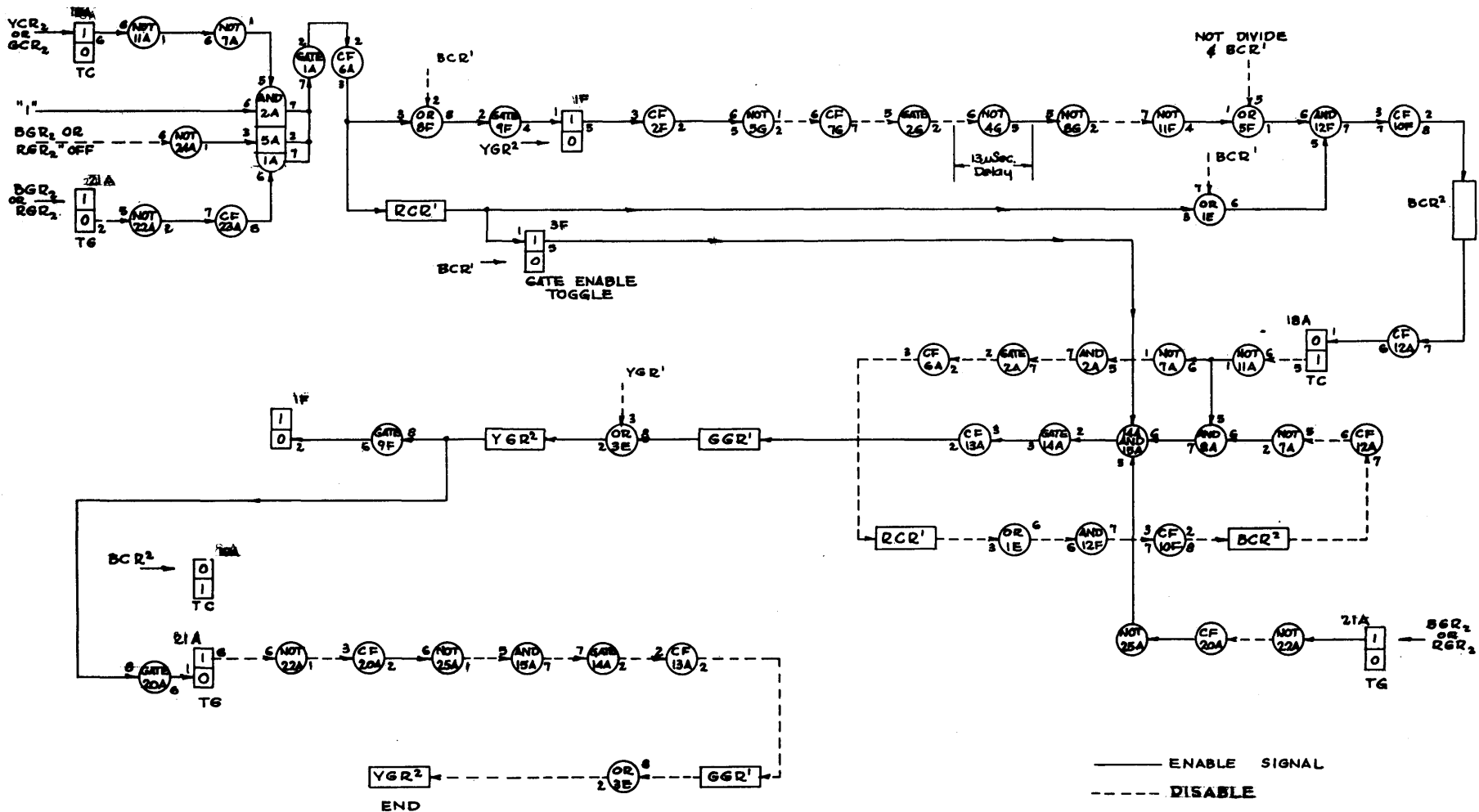
UNIV. of ILLINOIS · UNIV. RESEARCH BOARD · ELECTRONIC DIGITAL COMPUTER
 FOR JPN BY HMW CHECKED APPROVED *J. P. Nash* DATE 6-12-51
 TITLE - DECODING REGISTER CODE | S.306

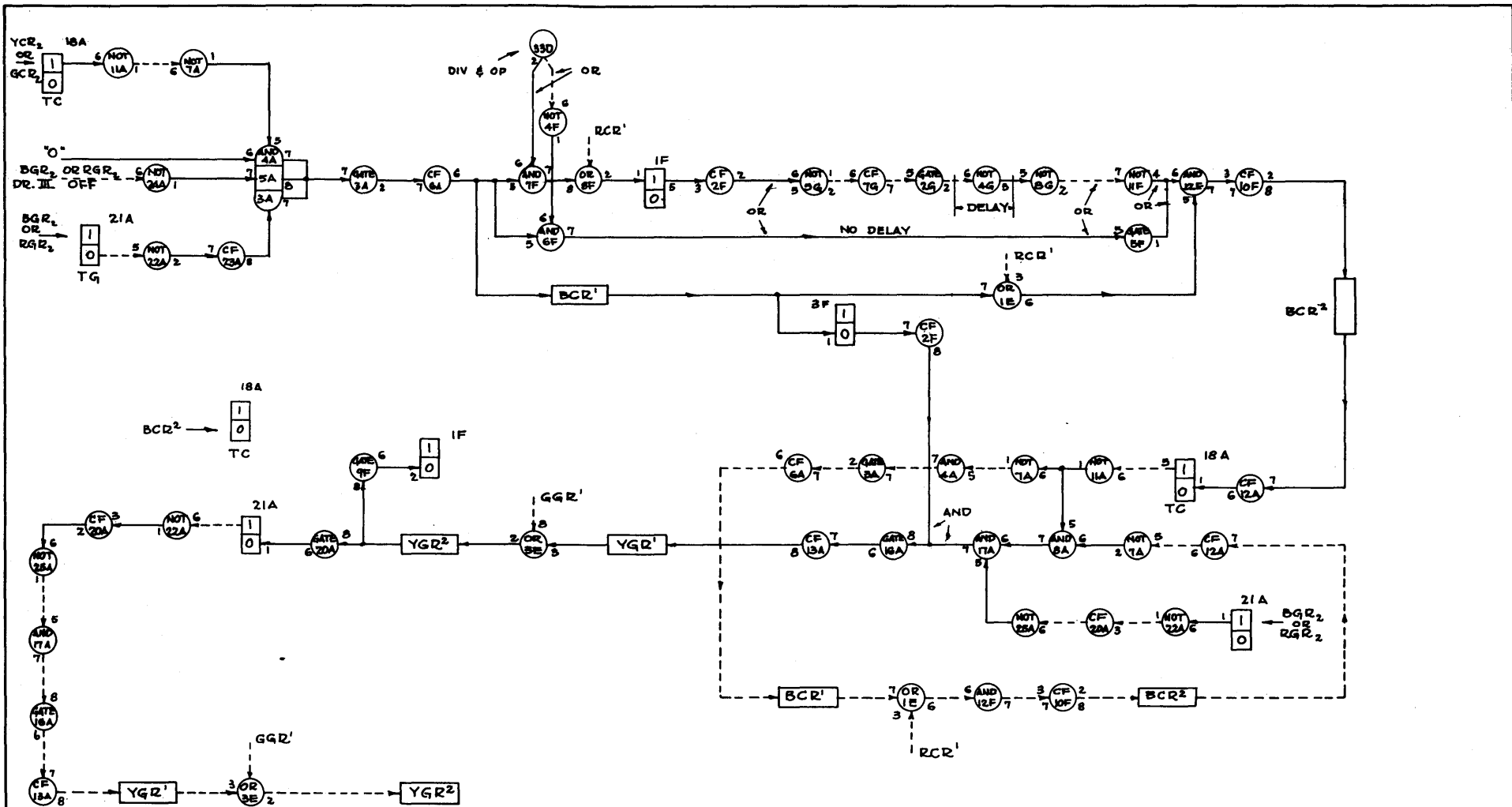
ORDER REGISTER CODE

FLIPFLOP	2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹
I	+ -	USE MEM.	READ ORD.	R	ROUND OFF	+	ABS. VAL.	CL.	R ₂	
O	X ÷	NOT	WRITE SHIFT	L	NOT	-	N ²	H	NOT	
+	1 .	1 .	1 .	1	0	0	0	0 .	0 .	
X	0 .	1 .	1 .	1 .	0	1	0	0 .	0 .	
÷	0 .	1 .	1 .	0 .	0	1	1	0 .	0 .	
→	-	0 .	0 .	1 .	0	-	-	0 .	-	
←	0 .	0 .	0 .	0 .	0	-	-	0 .	-	
R	1	1 .	1 .	-	0	-	-	0 .	1 .	
A	-	0 .	1 .	1	0	0	0	0 .	1 .	
U'	1 .	0 .	1 .	-	0	0	0	0 .	0 .	
C'	0	0 .	1 .	-	0	0	1 .	0 .	0 .	
U	0	0 .	1 .	-	0	1 .	0	0 .	0 .	
C	0	0 .	1 .	-	1 .	0	0	0 .	0 .	
M	-	1 .	0 .	-	0	-	0 .	0 .	-	
E	-	1 .	0 .	-	0	1 .	1 .	0 .	-	
E'	-	1 .	0 .	-	0	0 .	1 .	0 .	-	
Z	0	0 .	1 .	1 .	0	0	0	0 .	0 .	
P	1 .	0 .	0 .	0 .	-	-	-	0 .	1 .	
T	1 .	0 .	0 .	0 .	-	-	-	0 .	0 .	

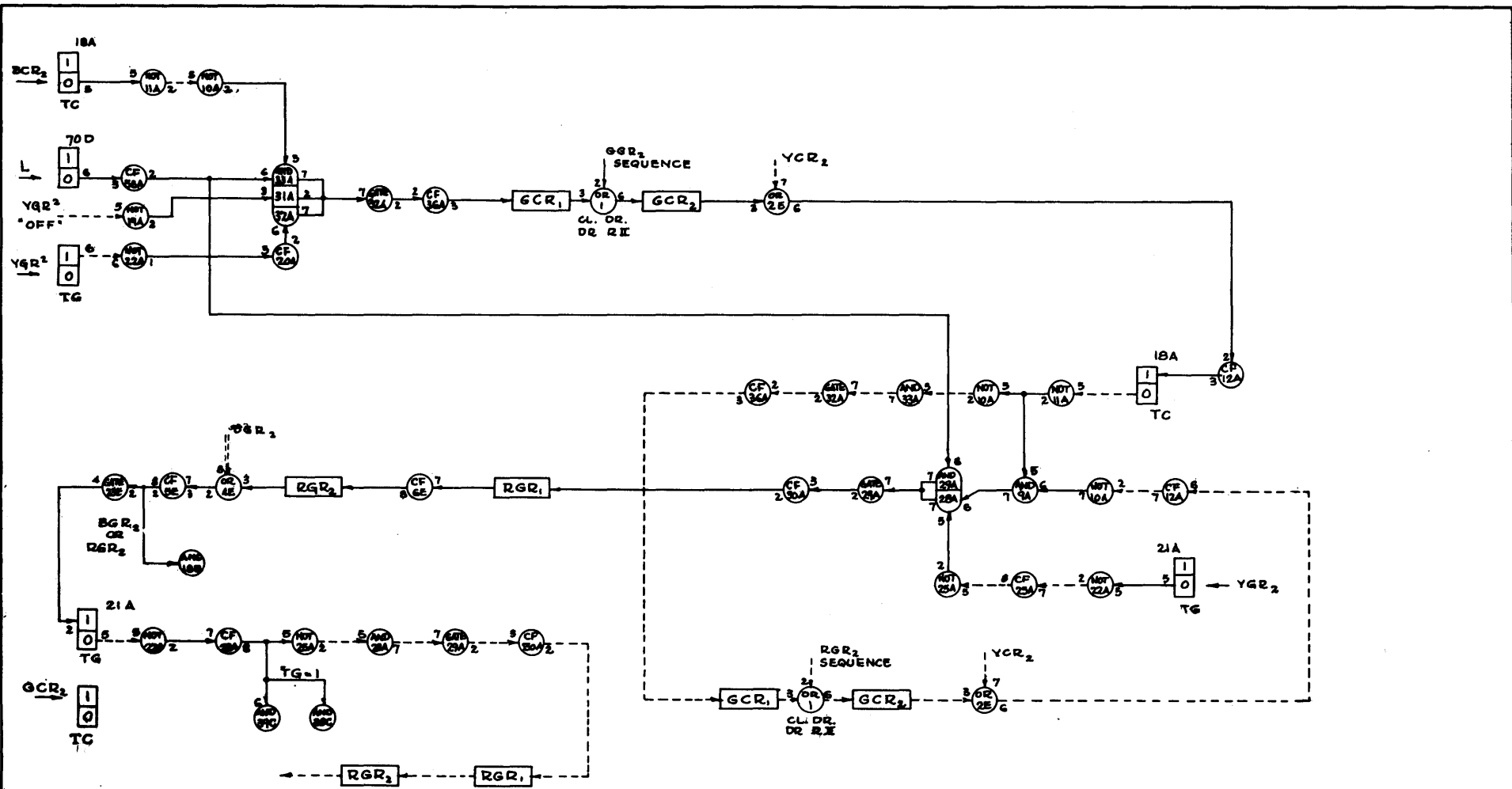
FLIPFLOPS MARKED ARE SENSED. OTHERS MERELY SET.

UNIV. of ILLINOIS · UNIV. RESEARCH BOARD · ELECTRONIC DIGITAL COMPUTER
 FOR JPN BY HMW CHECKED APPROVED *J. Prash* DATE 6-12-51
 TITLE ~ ORDER REGISTER CODE S.307.

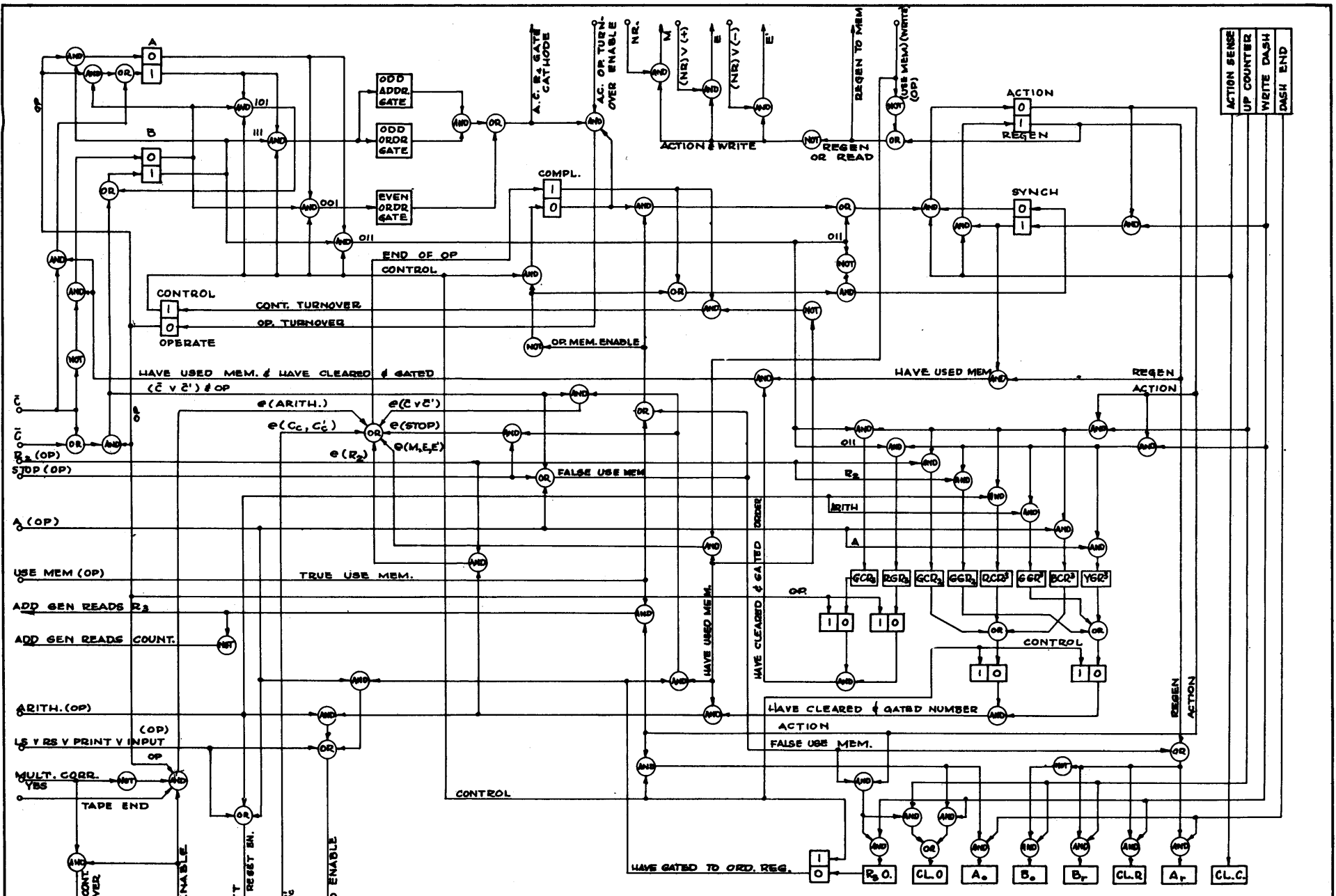


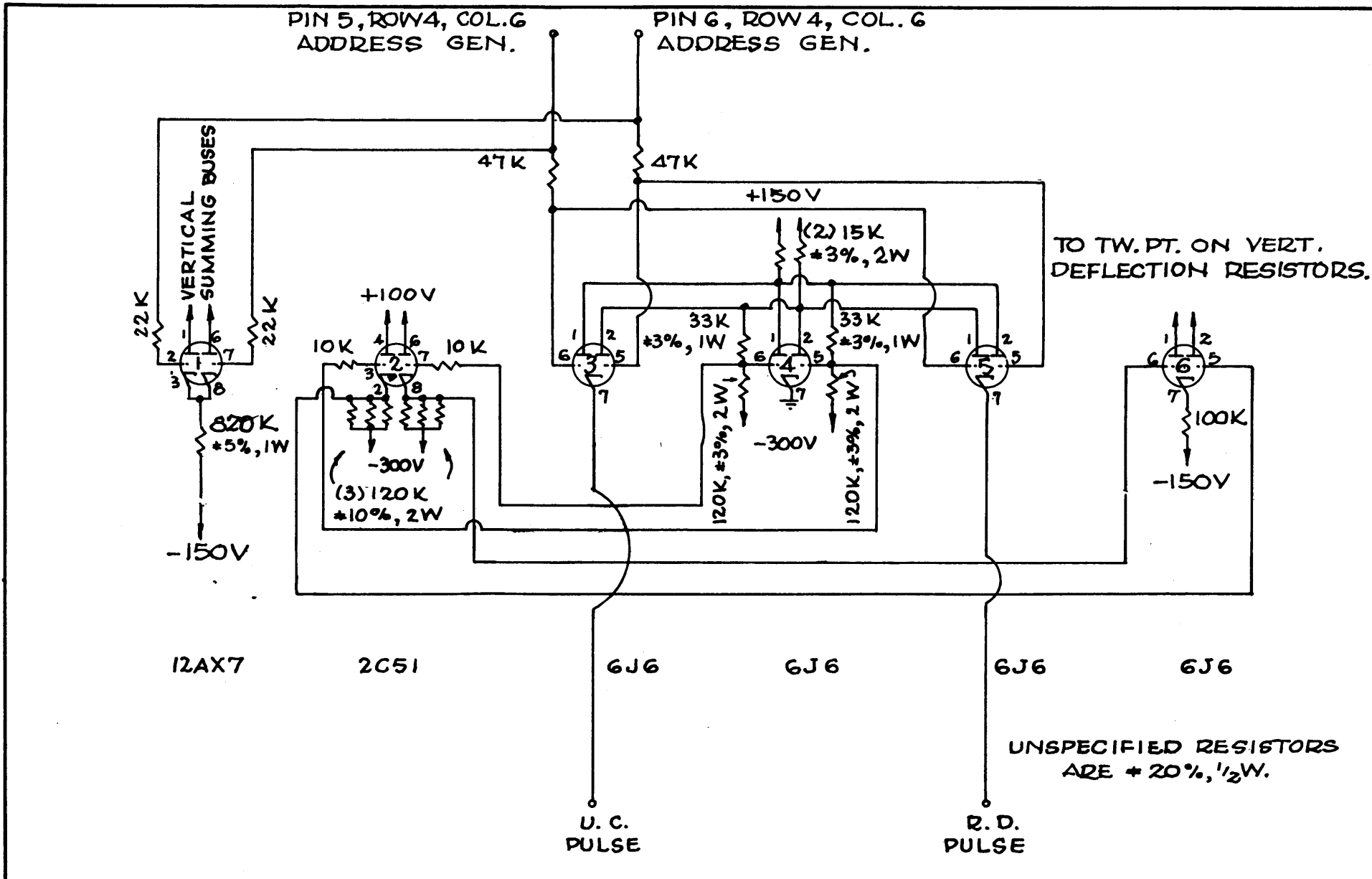


_____ ENABLE SIGNAL
 - - - - - DISABLE "



_____ ENABLE SIGNAL
 - - - - - DISABLE SIGNAL





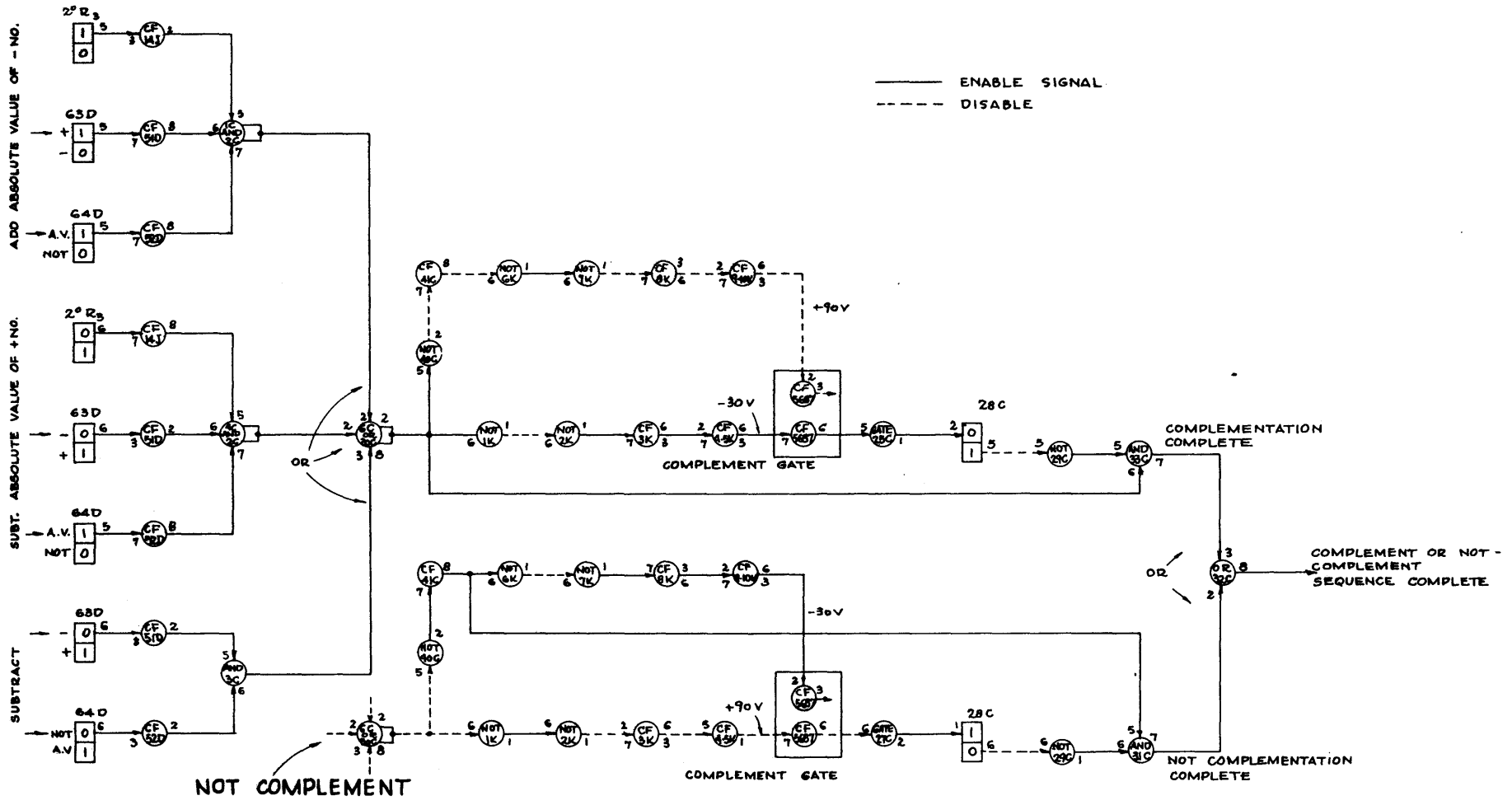
UNIVERSITY of ILLINOIS · UNIVERSITY RESEARCH BOARD · ELECTRONIC DIGITAL COMPUTER

FOR JMW BY HMW CHECKED *J.M.W.* APPROVED *J.P.Nash* DATE 7-13-51

TITLE ~ REVERSED TWITCH STAGGER COL'S. GENERATOR

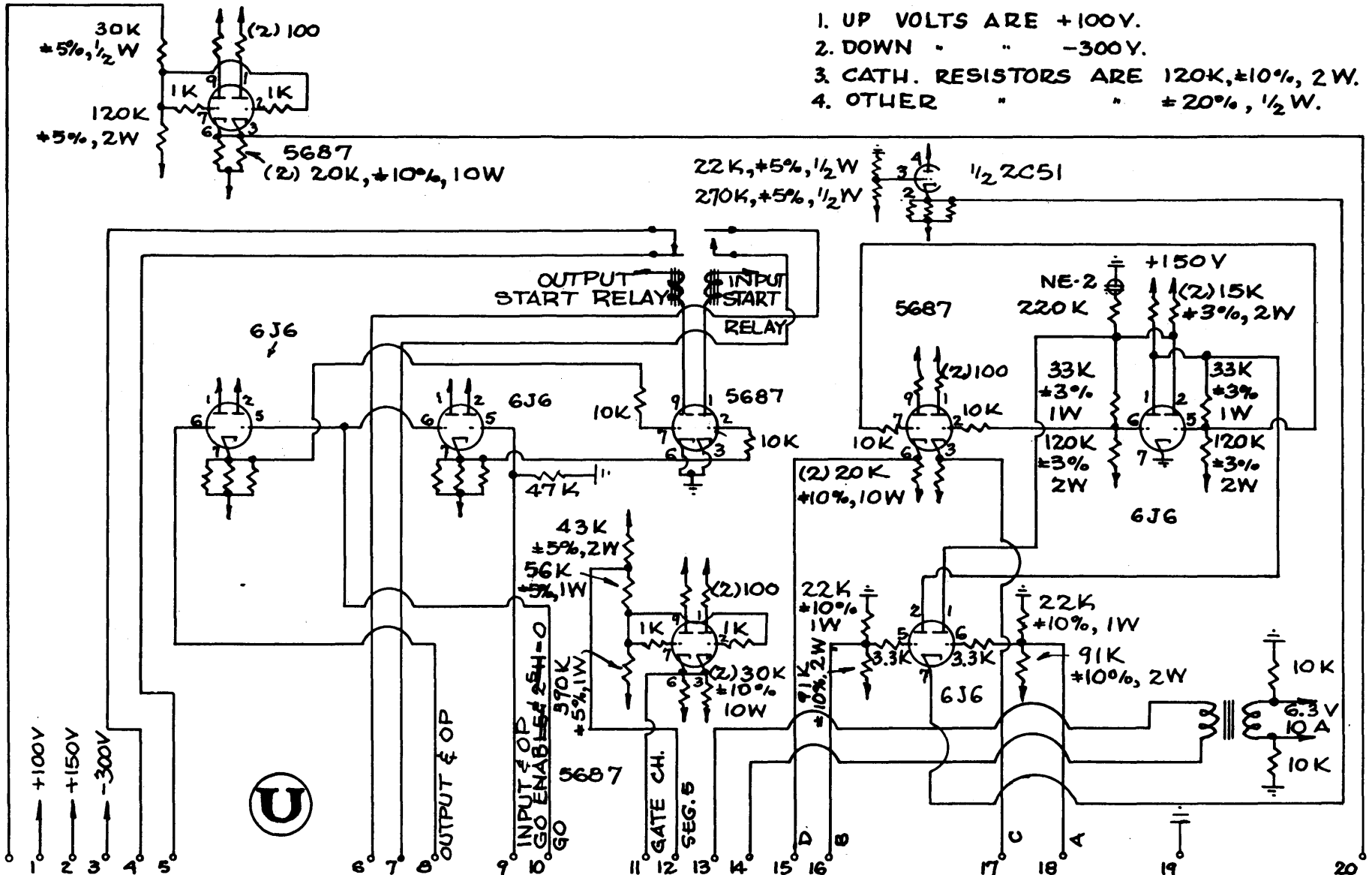
S-318

COMPLEMENT

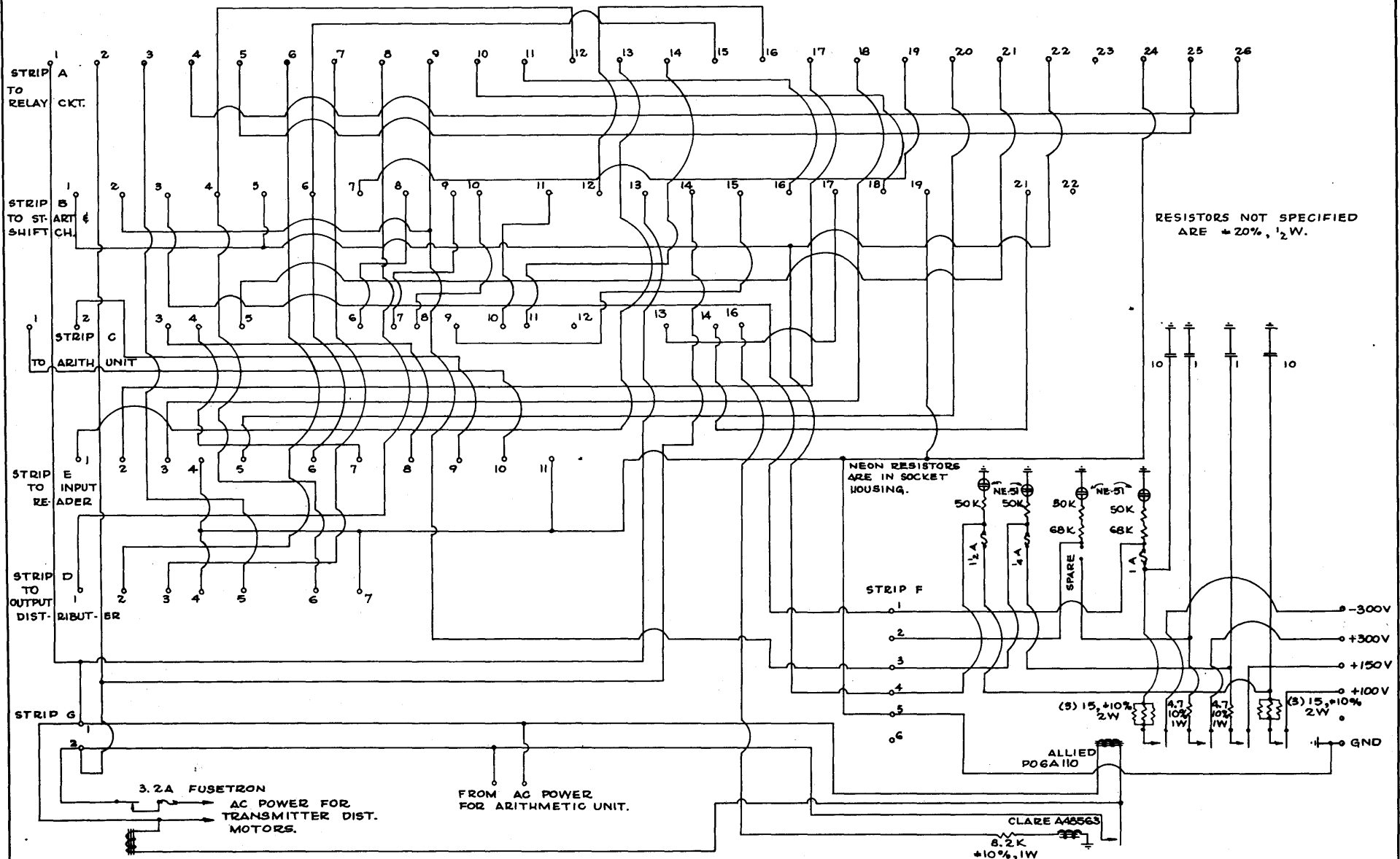


WHEN NOT SPECIFIED:

1. UP VOLTS ARE +100V.
2. DOWN " " -300V.
3. CATH. RESISTORS ARE 120K, ±10%, 2W.
4. OTHER " " ±20%, 1/2W.



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 FOR TS. BY HMW CHECKED T. SHAPIN APPROVED *R. E. Weagler* DATE 7-25-51
 TITLE - INPUT OUTPUT START & SHIFT CHASSIS I S-326



RESISTORS NOT SPECIFIED ARE ±20%, 1/2 W.

NEON RESISTORS ARE IN SOCKET HOUSING.

3.2A FUSETRON
AC POWER FOR
TRANSMITTER DIST.
MOTORS.

FROM AC POWER
FOR ARITHMETIC UNIT.

(3) 15, ±10%
2W
4.7
10%
1W
4.7
10%
1W
(3) 15, ±10%
2W

ALLIED
POGA 110

CLARE A40563
8.2K
±10%, 1W



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FOR TS BY HMW CHECKED T. SHANN APPROVED R. F. Maglieri DATE 7.27.51

TITLE ~ INTERCONNECTION CHASSIS

M-327

~ ALL PULSES GO FROM +10V TO -10V.

1.1 μ s DOT ~ TURNS THE BEAM ON TO SENSE THE INFORMATION STORED OR TO WRITE A DOT.

1.8 μ s DASH TEST ~ SELECTS THE TIME INTERVAL DURING WHICH A POSITIVE PULSE FROM THE AMPLIFIER INDICATES A DASH HAS BEEN SENSED.

3.6 μ s WRITING DASH ~ TURNS THE BEAM ON TO WRITE A DASH. GATES R_3 TO CONTROL COUNTER WHEN DESIRED. CLEARS REGENERATION COUNTER ROWS C_4A WHEN DESIRED. WHEN DESIRED R_3R_2 FROM MEM, R_2R_1 FROM MEM, G_3R_2 FROM MEM, Y_3R_2 FROM R_2 .

1.3 μ s REGENERATE DASH ~ PROVIDES A TIME DELAY FOR THE DASH END. SETS TWITCH FLIPFLOP.

2.2 μ s DASH END ~ TURNS THE BEAM OFF WHEN A DASH HAS BEEN REGENERATED. GATES ONE OF OUTSIDE ROWS OF DISPATCH COUNTER WHEN DESIRED.

2.5 μ s ACTION SENSE ~ SETS ACTION REGEN. TOGGLE WHEN DESIRED, AND CLEARS CENTER OF DISPATCH CTR. WHEN DESIRED

2.5 μ s DELAY PULSE

5 μ s SETS SYNCH TOGGLE WHEN DESIRED. GATES DISPATCH COUNTER FROM OUTSIDE TO CENTER WHEN SO ORDERED. CLEARS ORDER COUNTER SIDE OF DISPATCH COUNTER WHEN DESIRED. WHEN DESIRED IN MEMORY CONTROL, PROVIDES DRIVING PULSES FOR GCR_3 , GCR_2 , R_3R_2 & B_3R_2 . RESETS TWITCH F.FLOP.

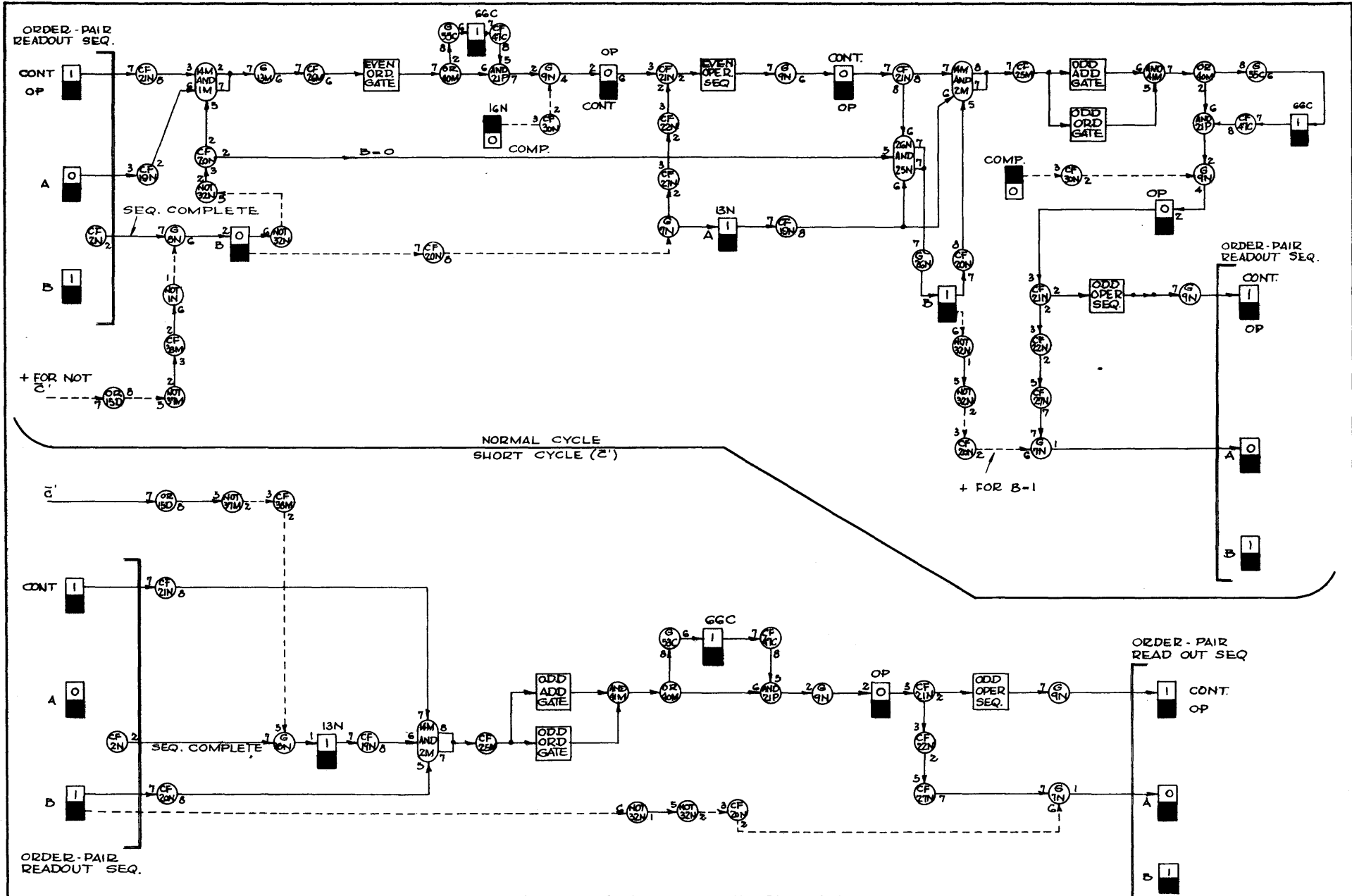
O
R
D
V
A
C

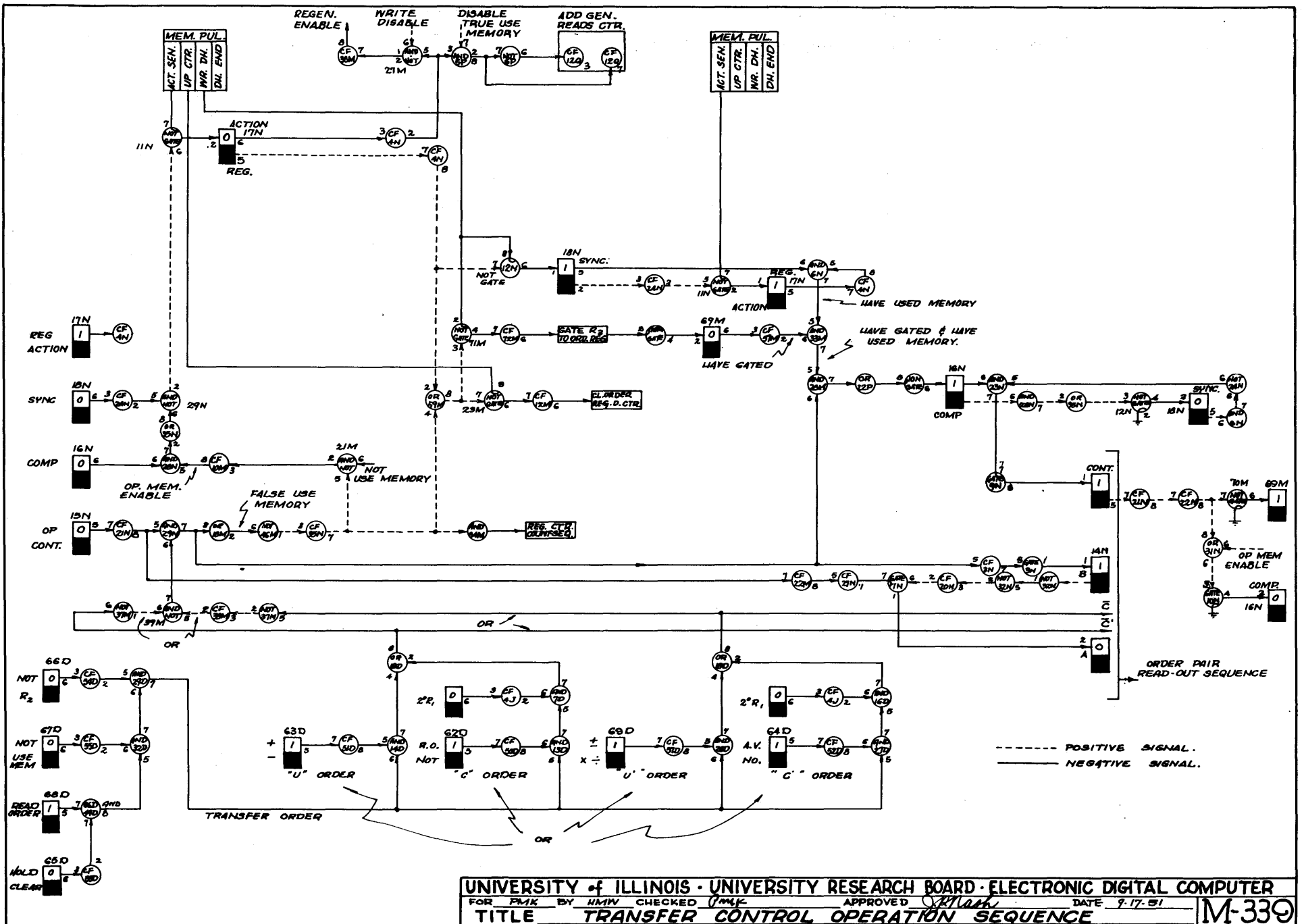
UNIVERSITY of ILLINOIS · UNIVERSITY RESEARCH BOARD · ELECTRONIC DIGITAL COMPUTER

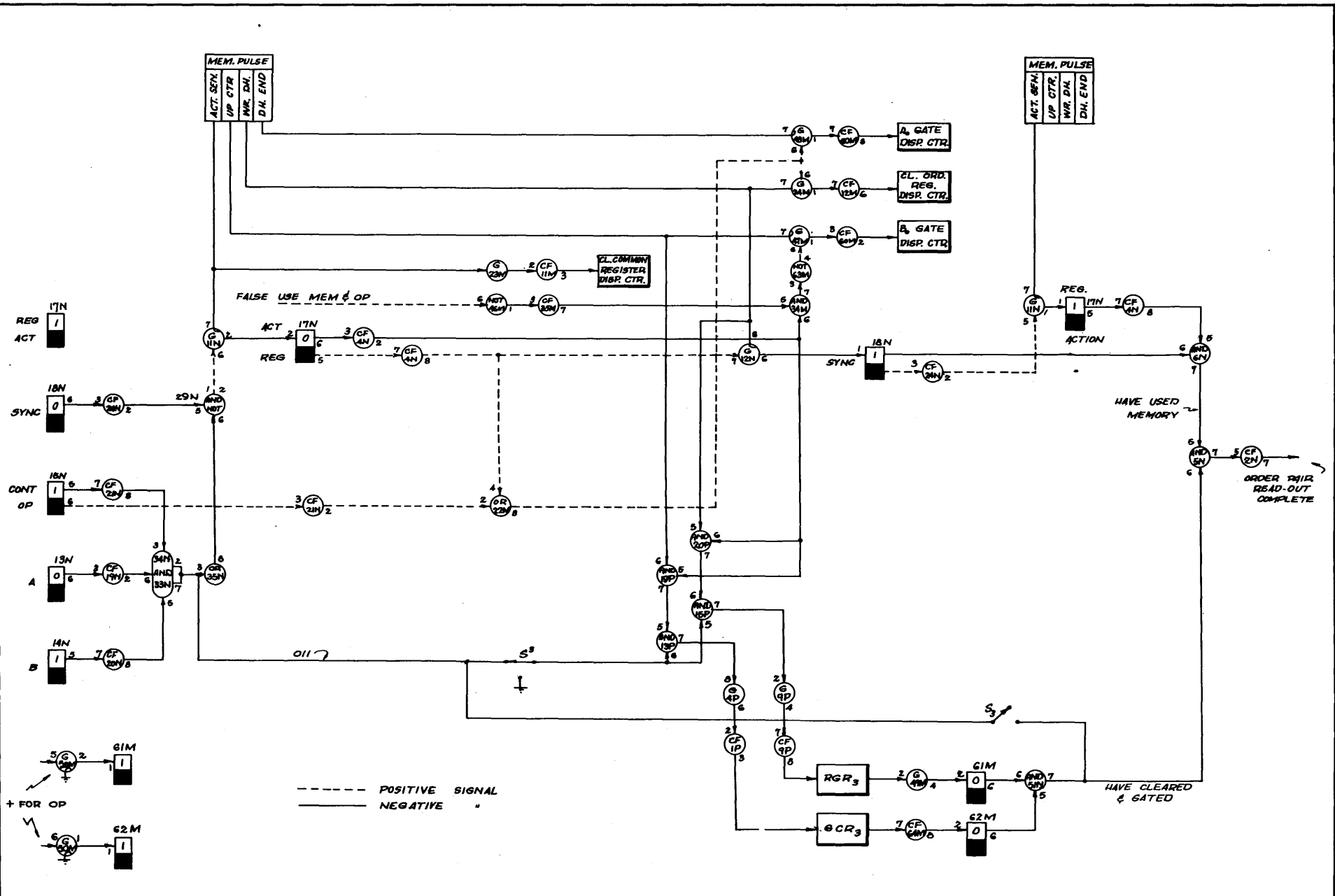
FOR JMW BY LMW CHECKED J.M.W. APPROVED R.E. Meagher DATE 8-16-51

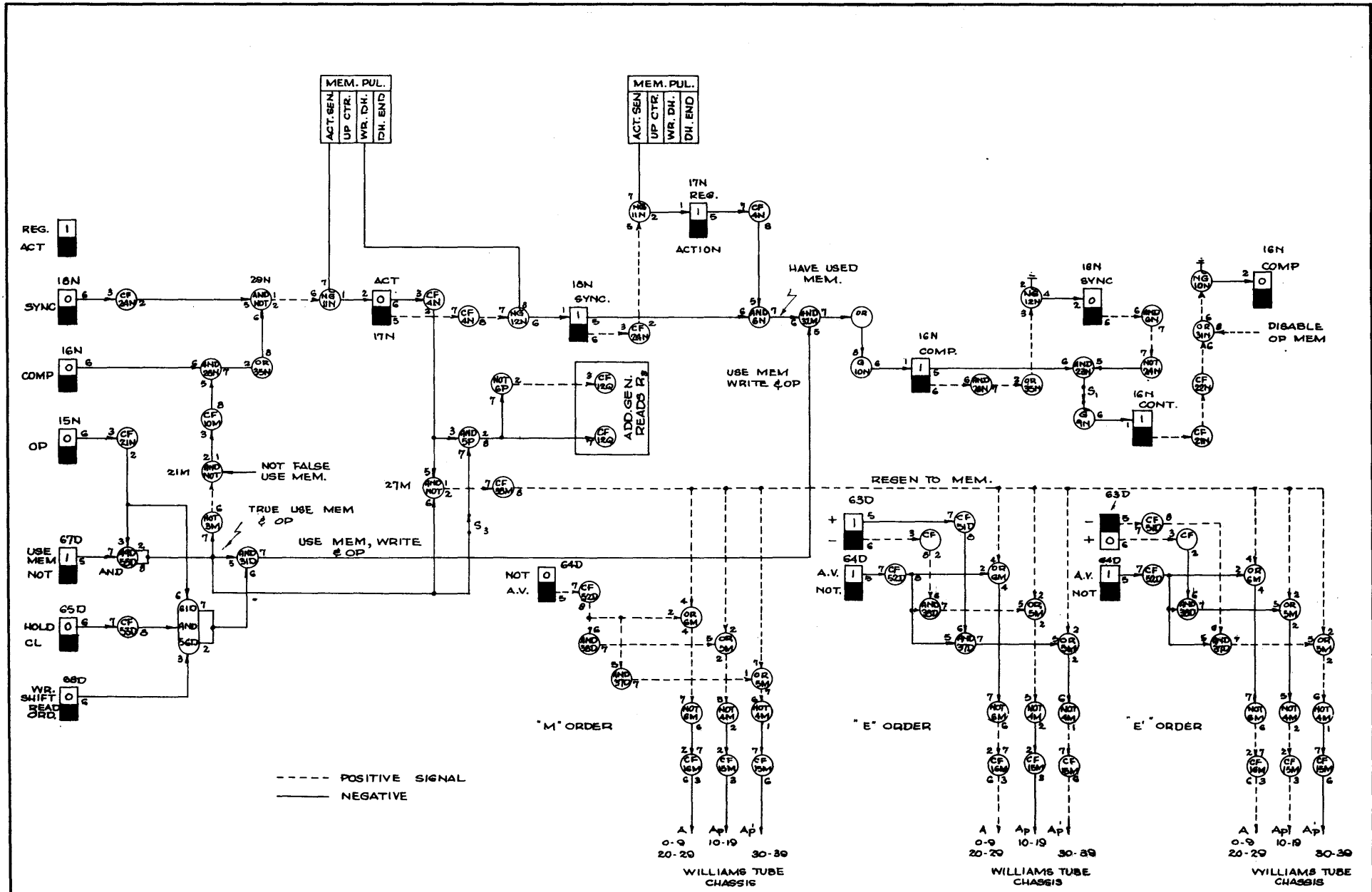
TITLE IDEALIZED PULSES FOR MEMORY

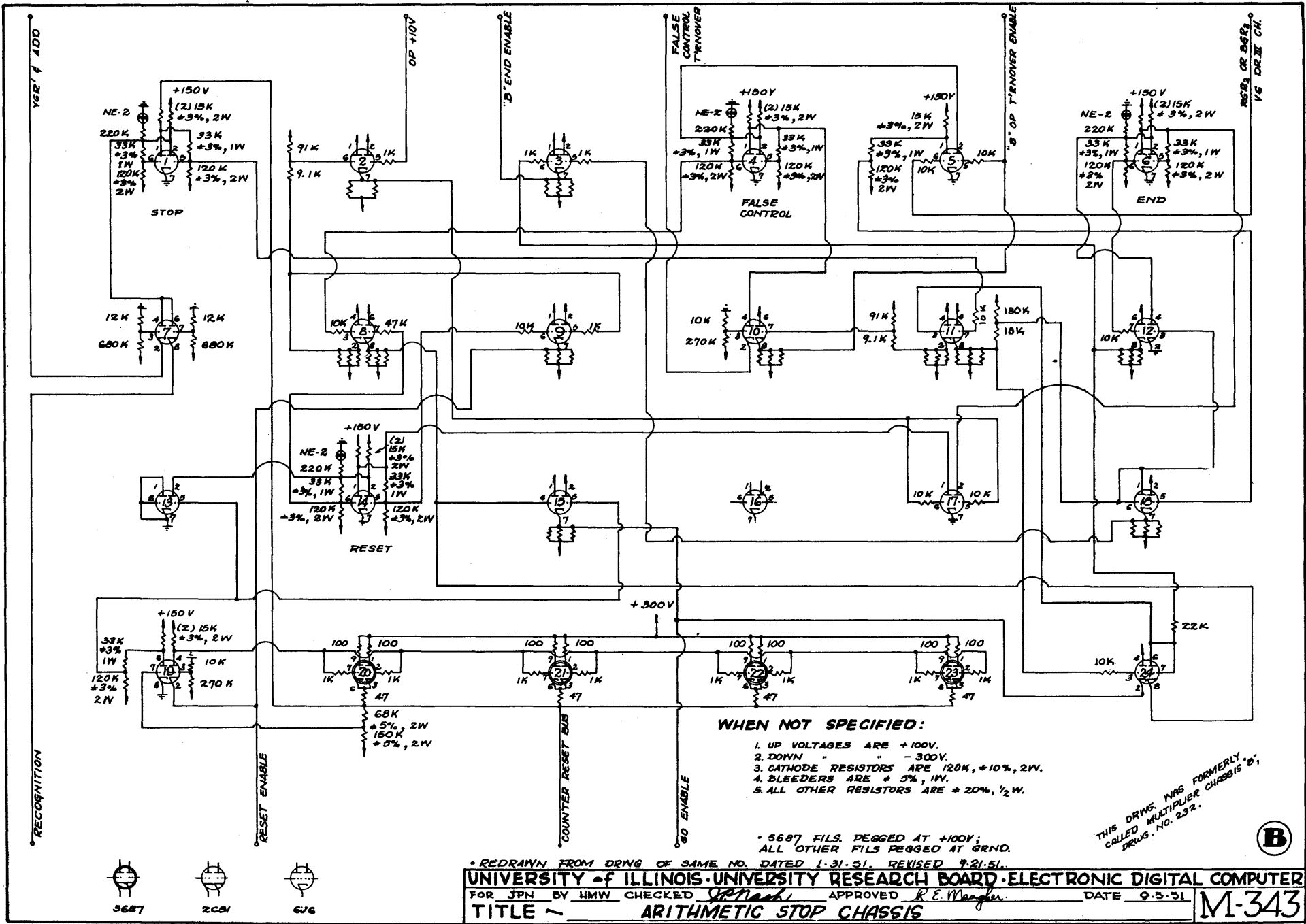
S-333











WHEN NOT SPECIFIED:

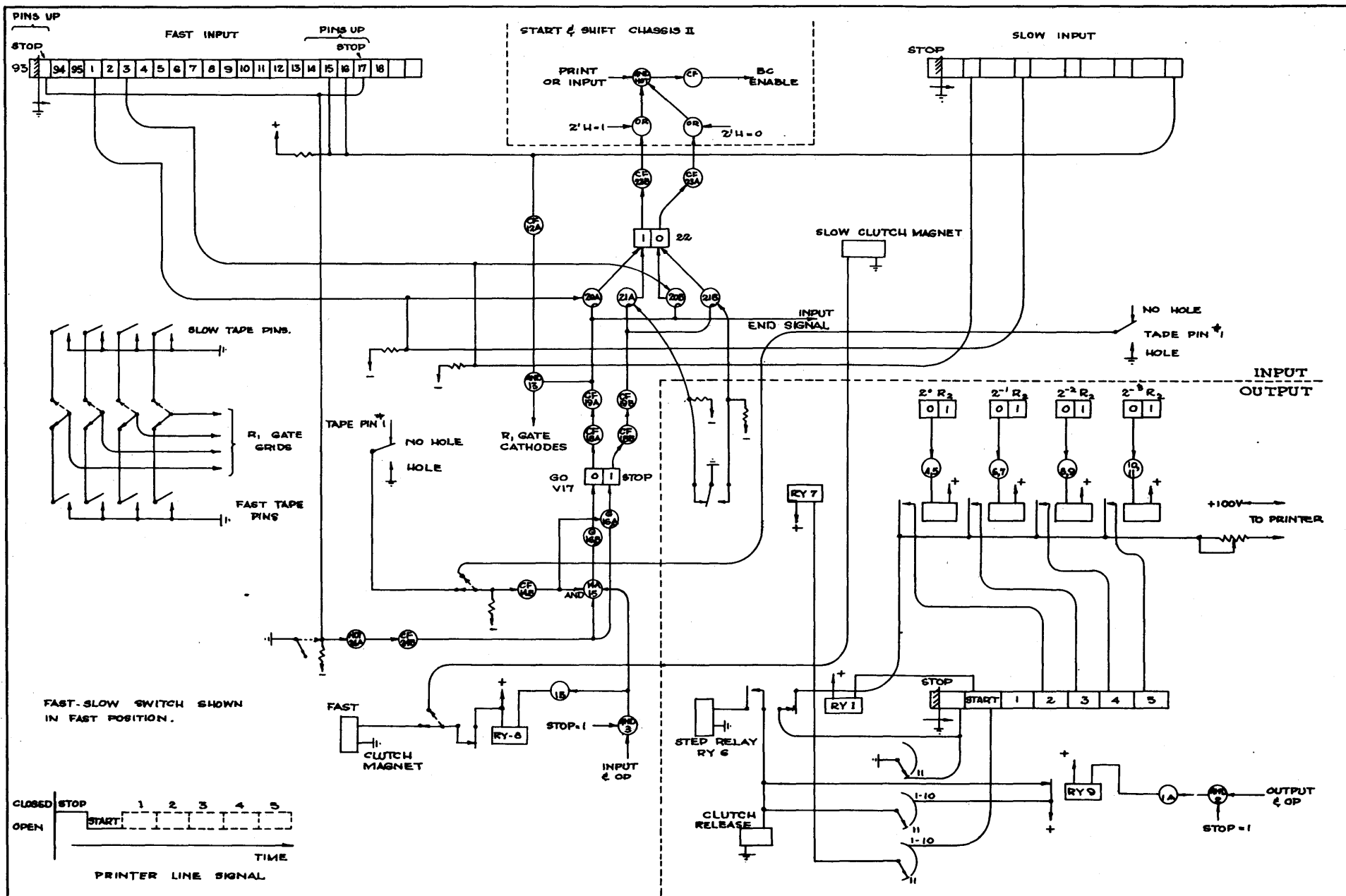
1. UP VOLTAGES ARE +100V.
2. DOWN " " - 300V.
3. CATHODE RESISTORS ARE 120K, ±10%, 2W.
4. BLEEDERS ARE ± 5%, 1W.
5. ALL OTHER RESISTORS ARE ± 20%, ½ W.

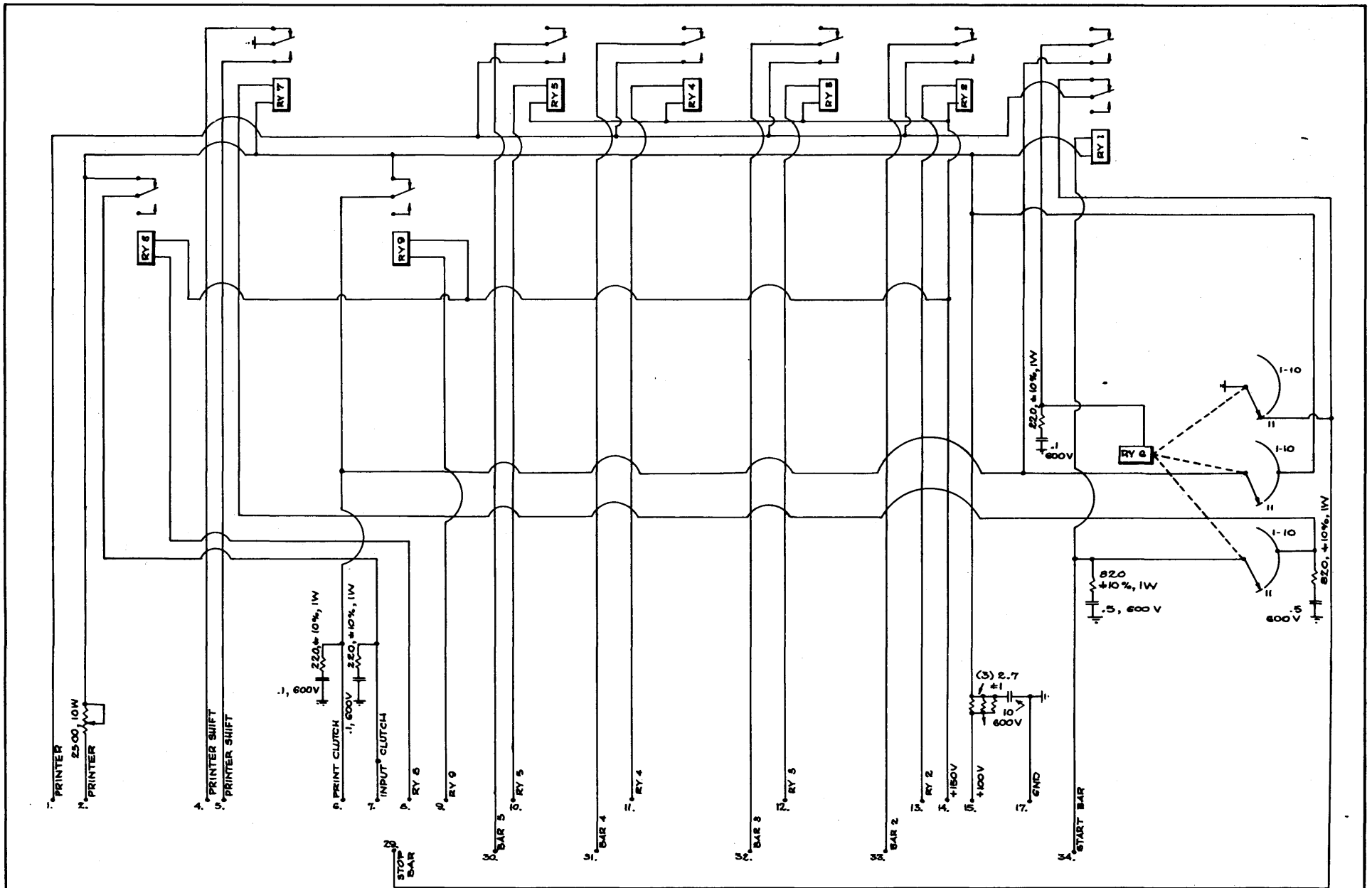
• 5687 FILS. PEGGED AT +100V;
ALL OTHER FILS PEGGED AT GRND.

• REDRAWN FROM DRWG OF SAME NO. DATED 1-31-51. REVISED 7-21-51.

THIS DRWG. WAS FORMERLY
CALLED MULTIPLIER CHASSIS 0.
DRWG. NO. 232.



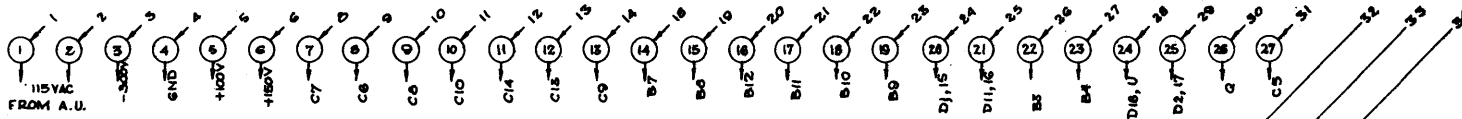




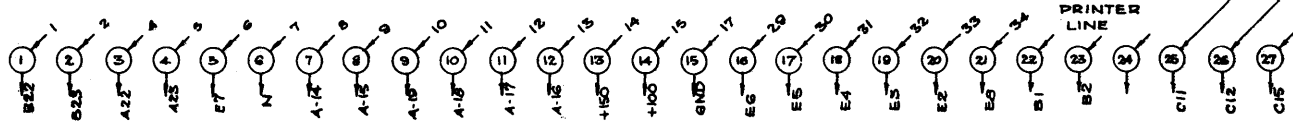
RY 1: AUTO-ELEC. Z17263 50A 100Ω 100V
 RY's 2-5-4-5 & 7:
 AUTO-ELEC. Z17262 50A 100Ω 100V
 RY 6: D87855 512 600Ω 115V
 RY's 8,9 CLARE A48568 6500Ω 10MA

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 FOR I.S. BY IDBY CHECKED T. SHAPIN APPROVED P.E. Meagher DATE 9-22-51
 TITLE ~ START & PRINT RELAY CHASSIS

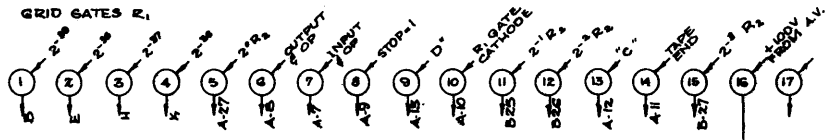
M-345



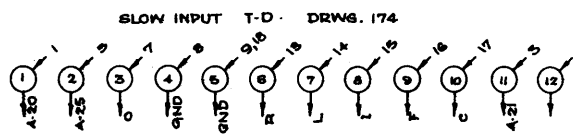
STRIP A
START & SHIFT CH. 1A - DRWG. N# 347



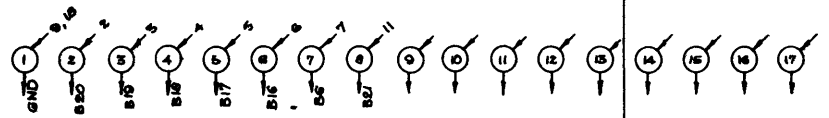
STRIP B
START & PRINT RELAY CHASSIS, DRWG N# 345

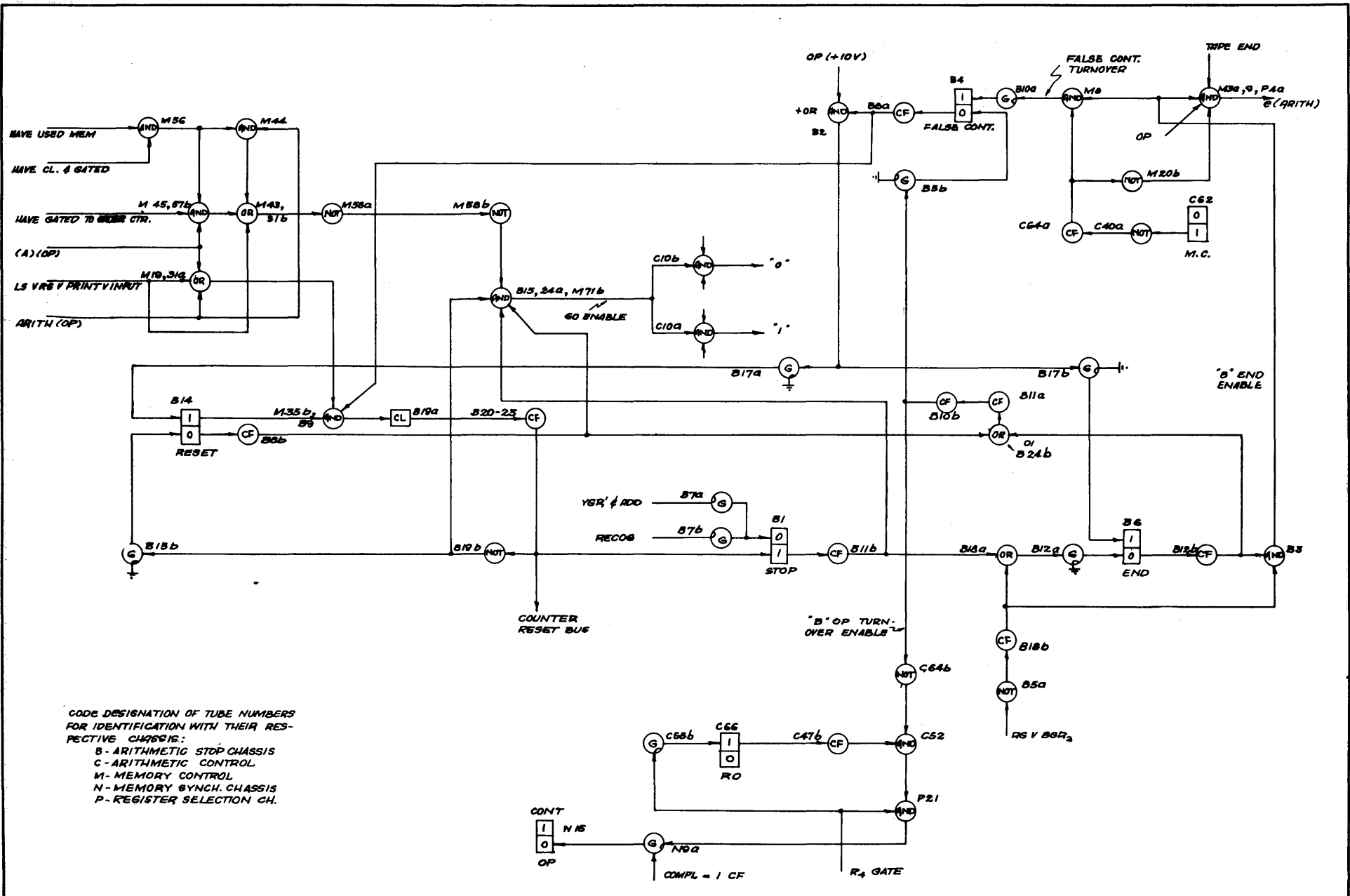


STRIP C CONNECTIONS.
ARITHMETIC UNIT



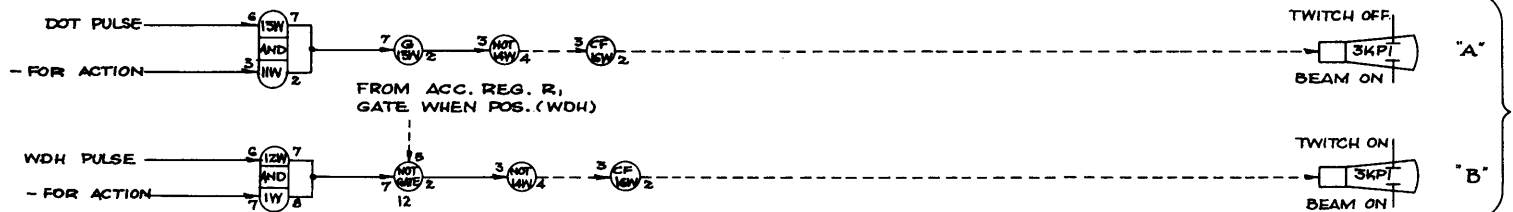
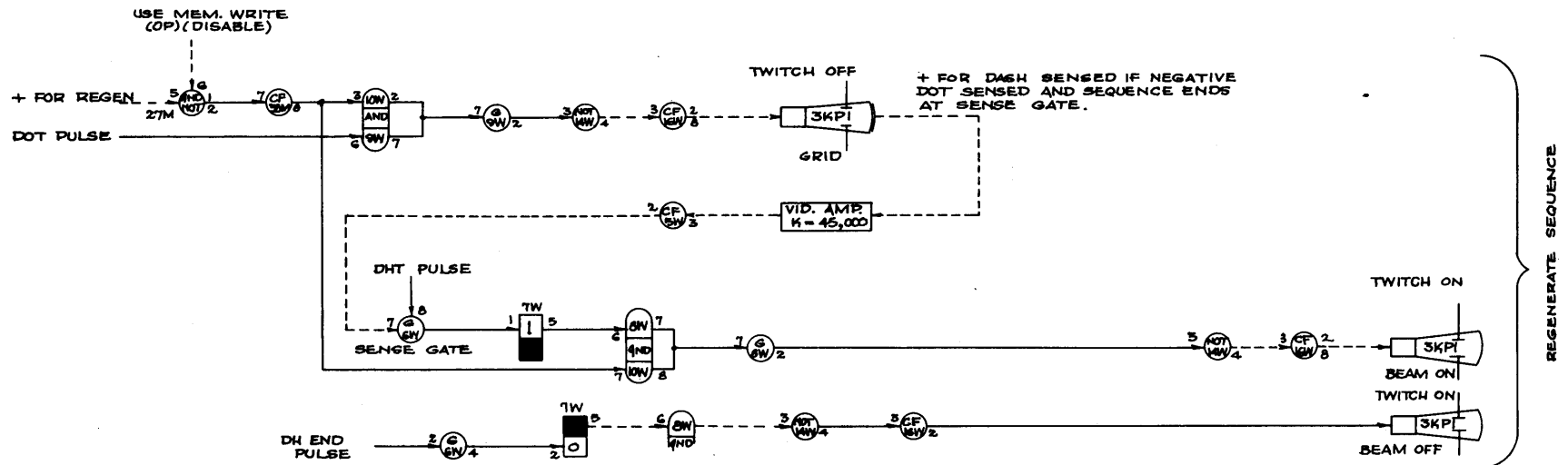
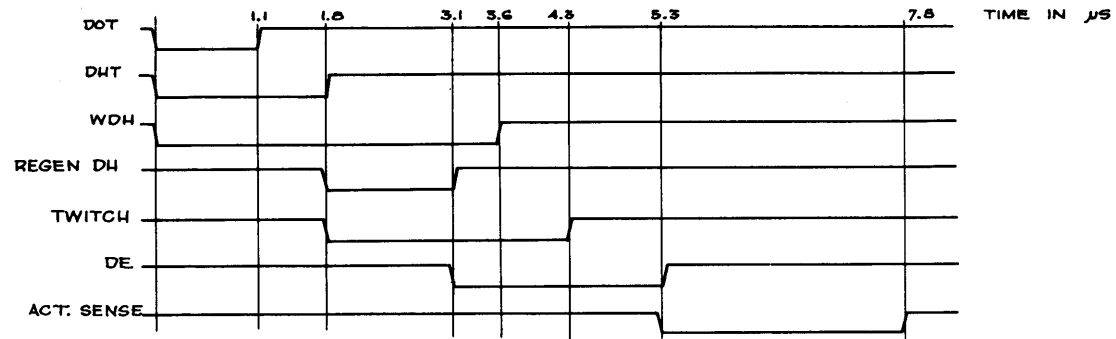
STRIP D



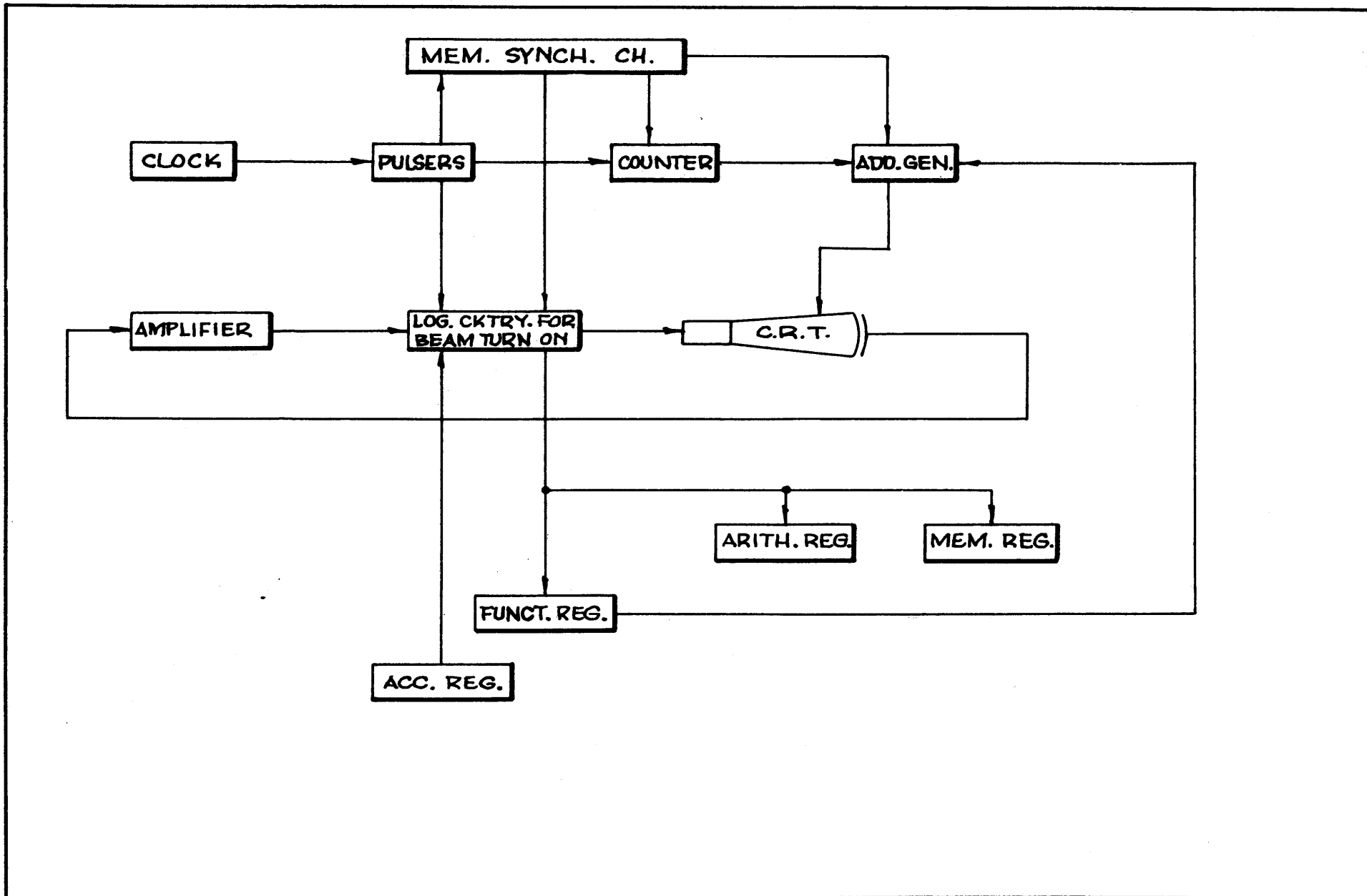


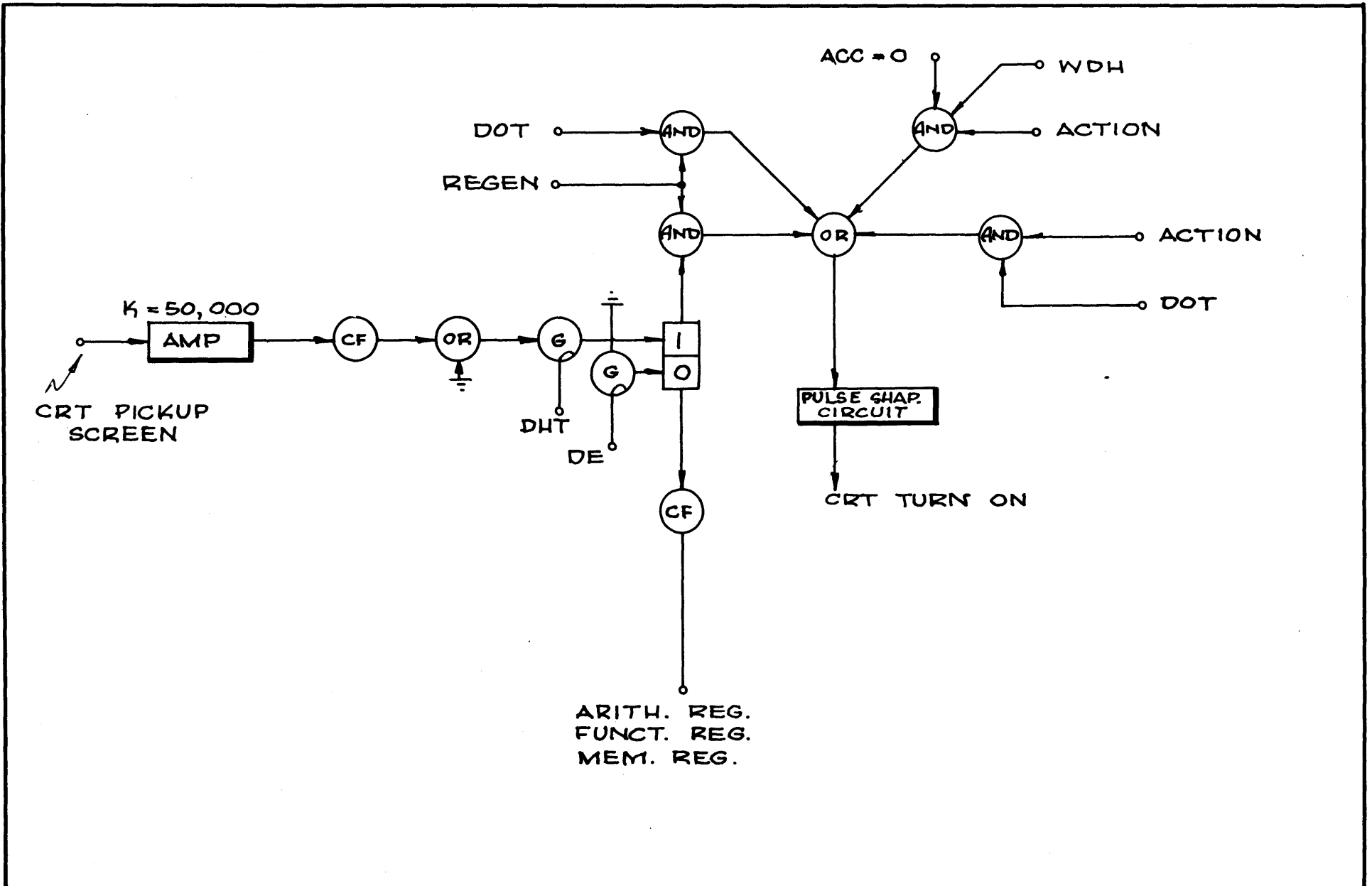
CODE DESIGNATION OF TUBE NUMBERS FOR IDENTIFICATION WITH THEIR RESPECTIVE CHASSIS:

- B - ARITHMETIC STOP CHASSIS
- C - ARITHMETIC CONTROL
- M - MEMORY CONTROL
- N - MEMORY SYNCH. CHASSIS
- P - REGISTER SELECTION CH.



————— NEGATIVE SIGNAL.
 - - - - - POSITIVE SIGNAL.

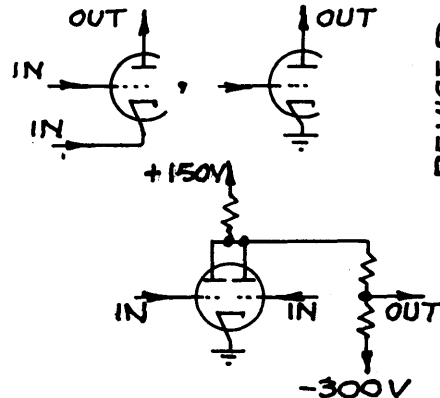
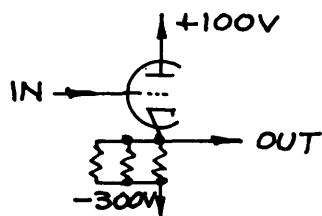
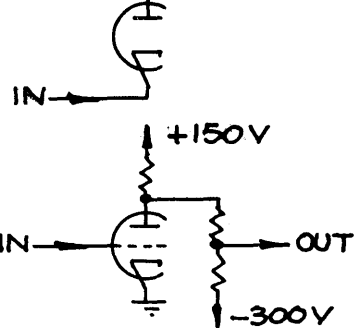
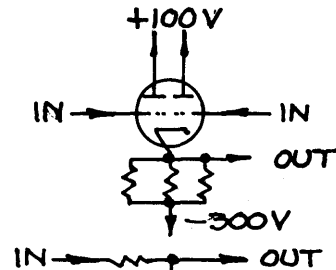
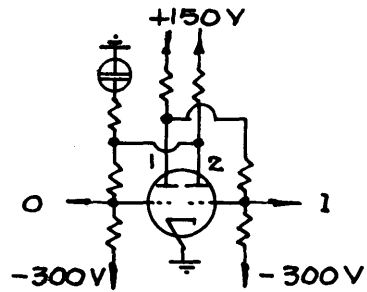
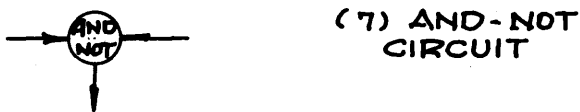
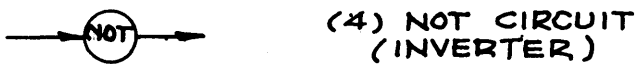
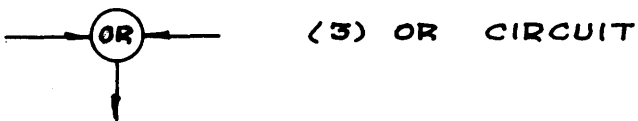
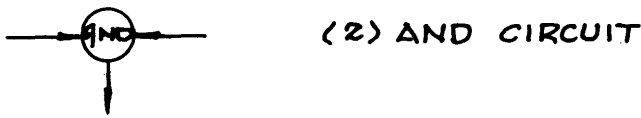
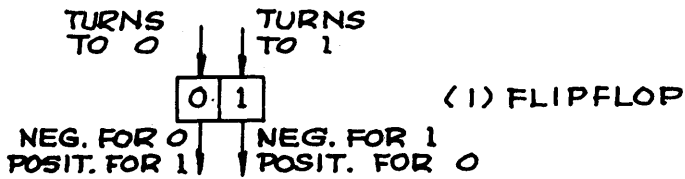




LOGICAL SYMBOL

CIRCUIT ELEMENT

(ENABLING SIGNALS ARE NEGATIVE)



~ REVISED 10.9.51.~

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 FOR JFN BY HMW CHECKED *J.P. Mack* APPROVED *R.E. Meacham* DATE 10.2.51
 TITLE ~ LOGICAL SYMBOLS & USUAL CIRCUIT EQUIVALENTS

S.352

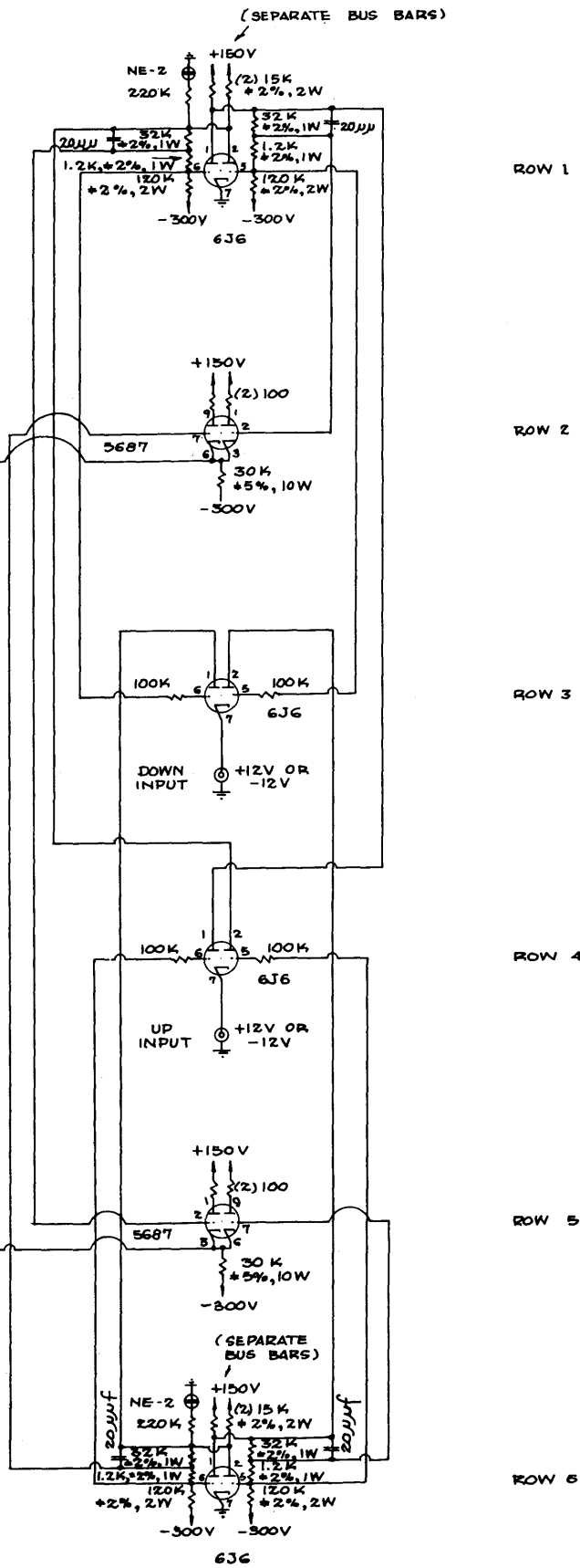
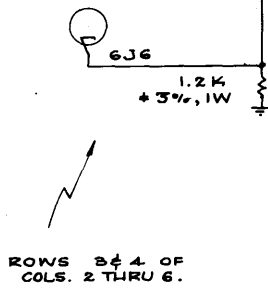
COL. 2

COL. 1

INPUT	TO NEXT STAGE			
	BOTTOM NEON LIGHT	TOP NEON LIGHT	UP SHIFT PULSE?	DOWN SHIFT PULSES?
UP PULSE	OFF	OFF	NO	NO
DOWN "	ON	"	YES	"
UP "	ON	ON	NO	"
DOWN "	OFF	"	"	YES
UP "	"	OFF	"	NO
DOWN "	ON	"	YES	"
UP "	ON	ON	NO	"
DOWN "	OFF	"	"	YES
UP "	OFF	OFF	NO	NO

TO GET A DOWN SHIFT, BOTTOM NEON LIGHT MUST BE OFF AND TOP NEON LIGHT MUST BE ON.

TO GET AN UP SHIFT BOTTOM NEON LIGHT MUST BE ON & TOP NEON LIGHT MUST BE OFF.

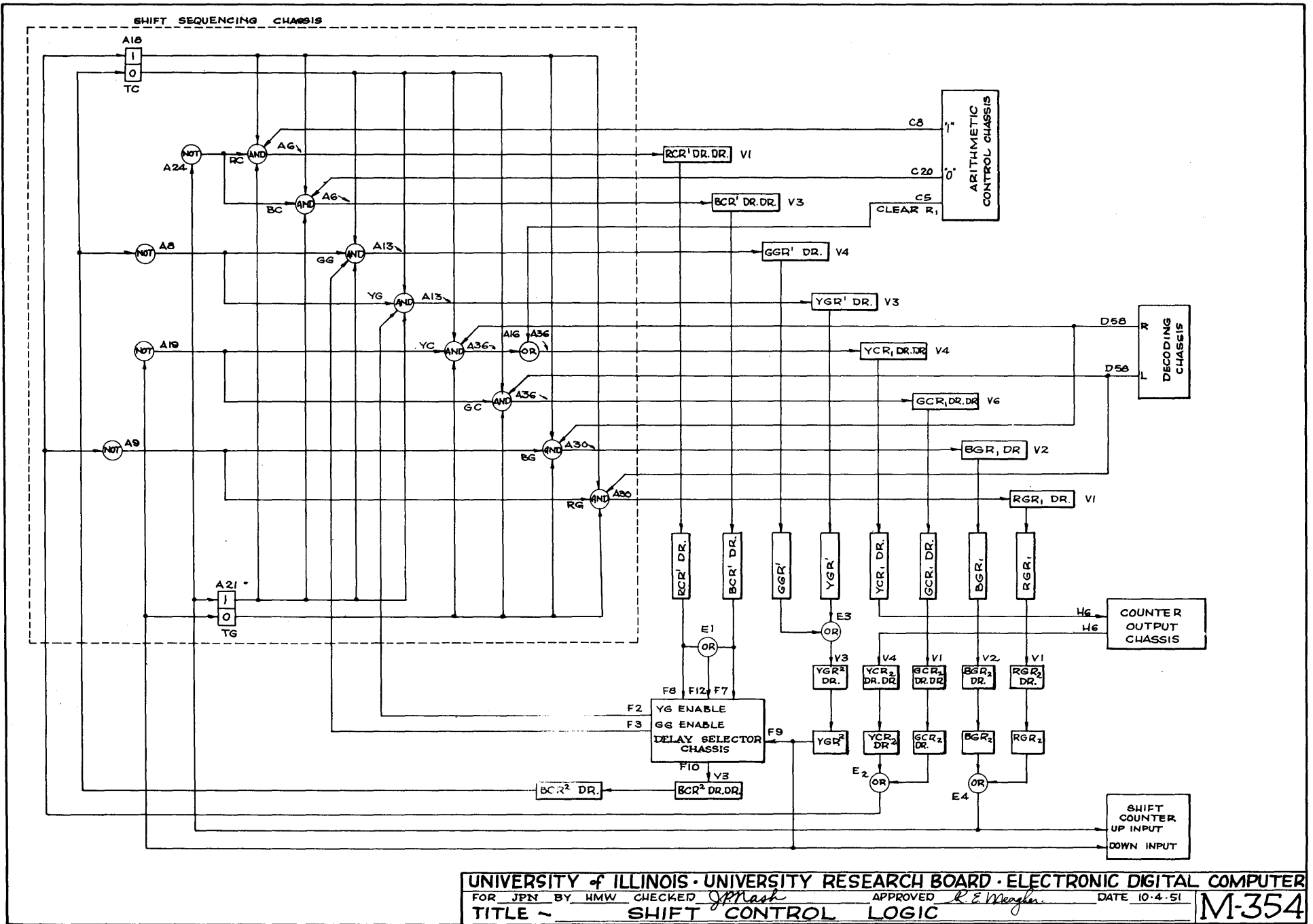


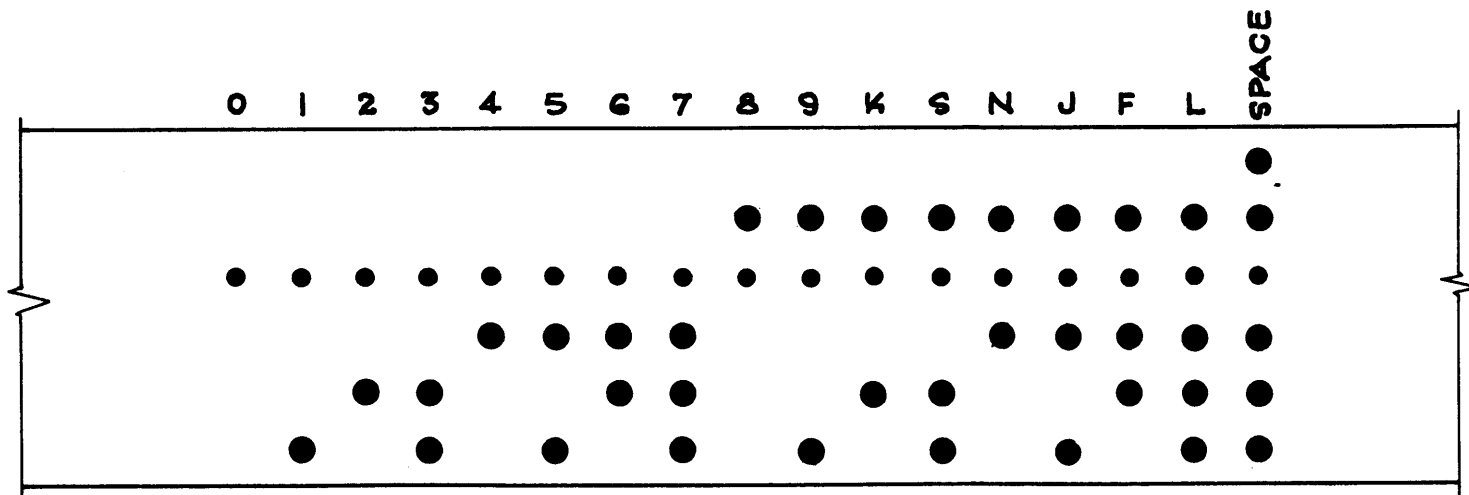
NOTES

1. RESISTORS NOT SPECIFIED ARE $\pm 20\%$, $\frac{1}{2}$ W.
2. ALL FILS. AT GROUND.
3. ALL SIX COLS. ARE IDENTICAL.
4. BOTTOM ROW OF COUNTER IS SENSED ROW.
5. DOWN PULSE IS FIRST PULSE OF PAIR.

REDRAWN FROM DRWG NO. 113 DATED 7-3-51

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 FOR JPN BY LMN CHECKED *W. E. Meigh* APPROVED *W. E. Meigh* DATE 10-1-51
 TITLE ~ SHIFT COUNTER CIRCUIT M-3553



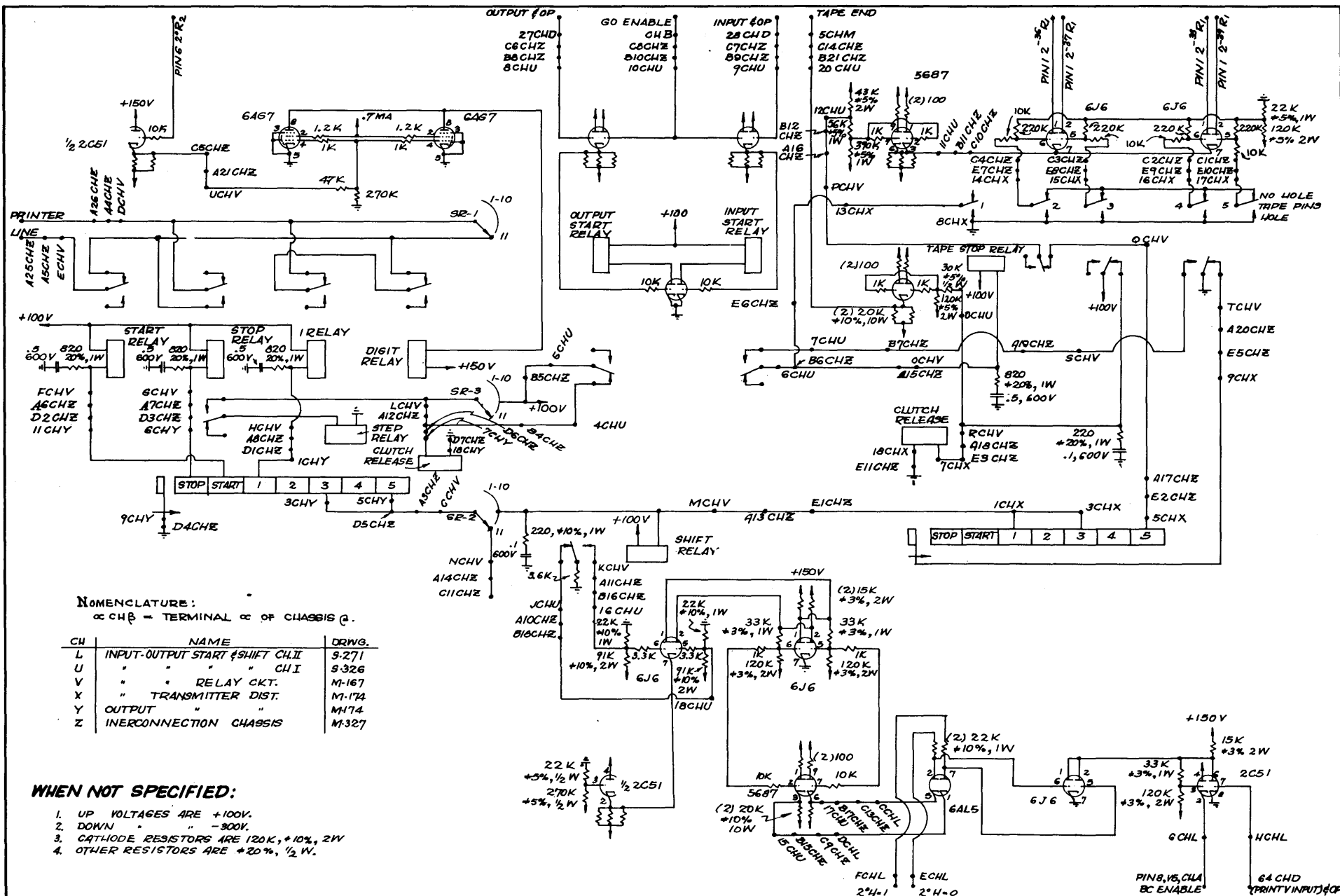


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FOR TS BY LMW CHECKED T. SHAPIN APPROVED R. E. Meagher DATE 10-8-51

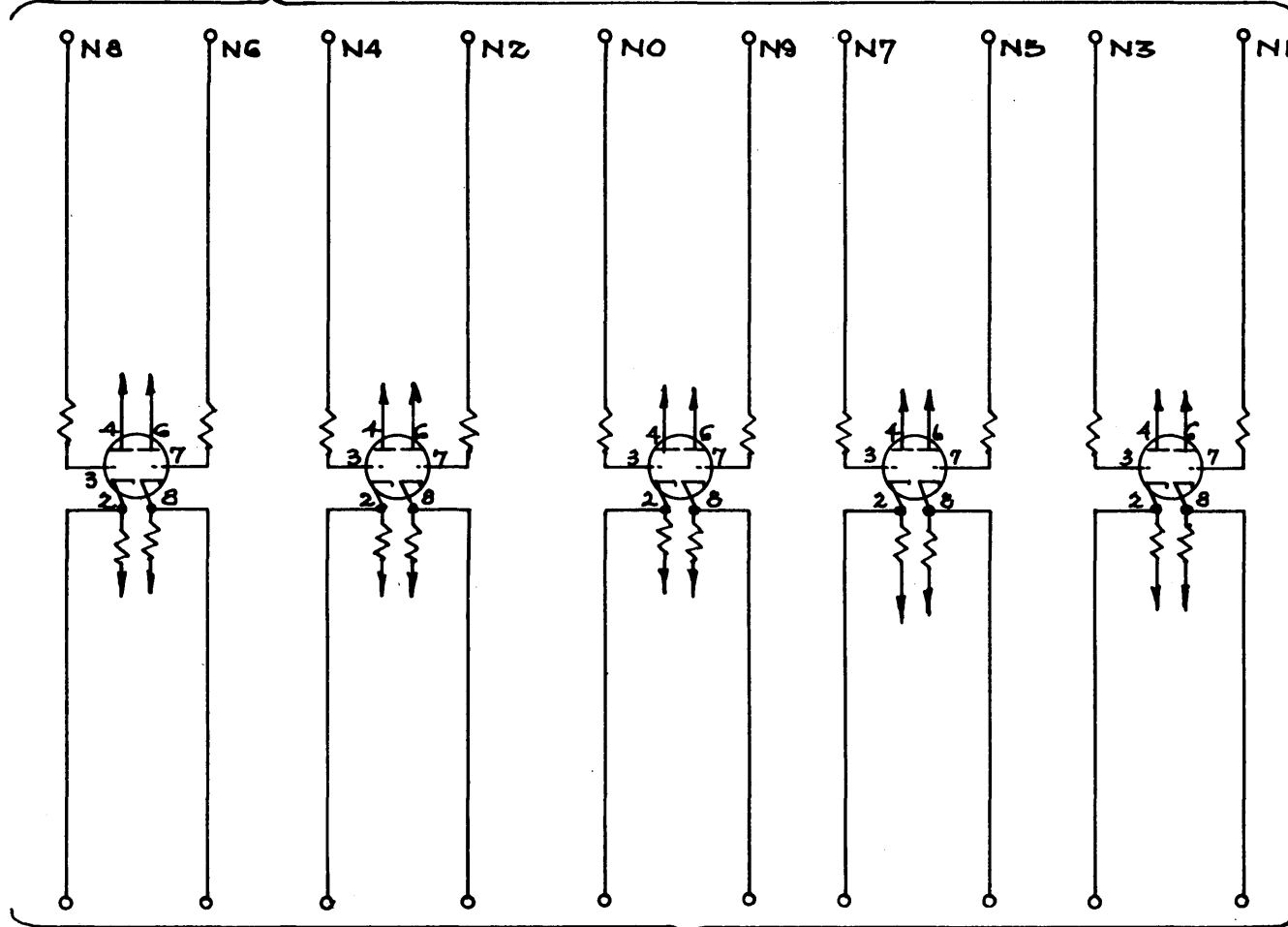
TITLE ~ PUNCHED TAPE SHOWING CODE USED

S-355



FROM PIN 8, V16, DRWG. # 196

WHERE N=0,1,2,3 POSIT. NUMBER DECADES.



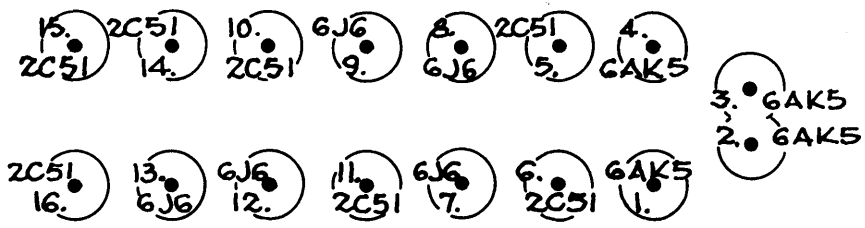
TO 40 POSITION SWITCH
TO SLAVE TUBE.

- ALL TUBES ARE 2C51'S.
- PLATE VOLTAGES ARE +150V.
- CATHODE " " -300V.
- " RESISTORS • 120K, +10%, 2W.
- GRID RESISTORS ARE 1.8K, +20%, 1/2W.

• FILS AT +50V.

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FOR JMW BY HMW CHECKED J.M.H. APPROVED R.E. Meagher DATE 10-15-51
 TITLE ~ SLAVE TUBE CATHODE FOLLOWERS S.357



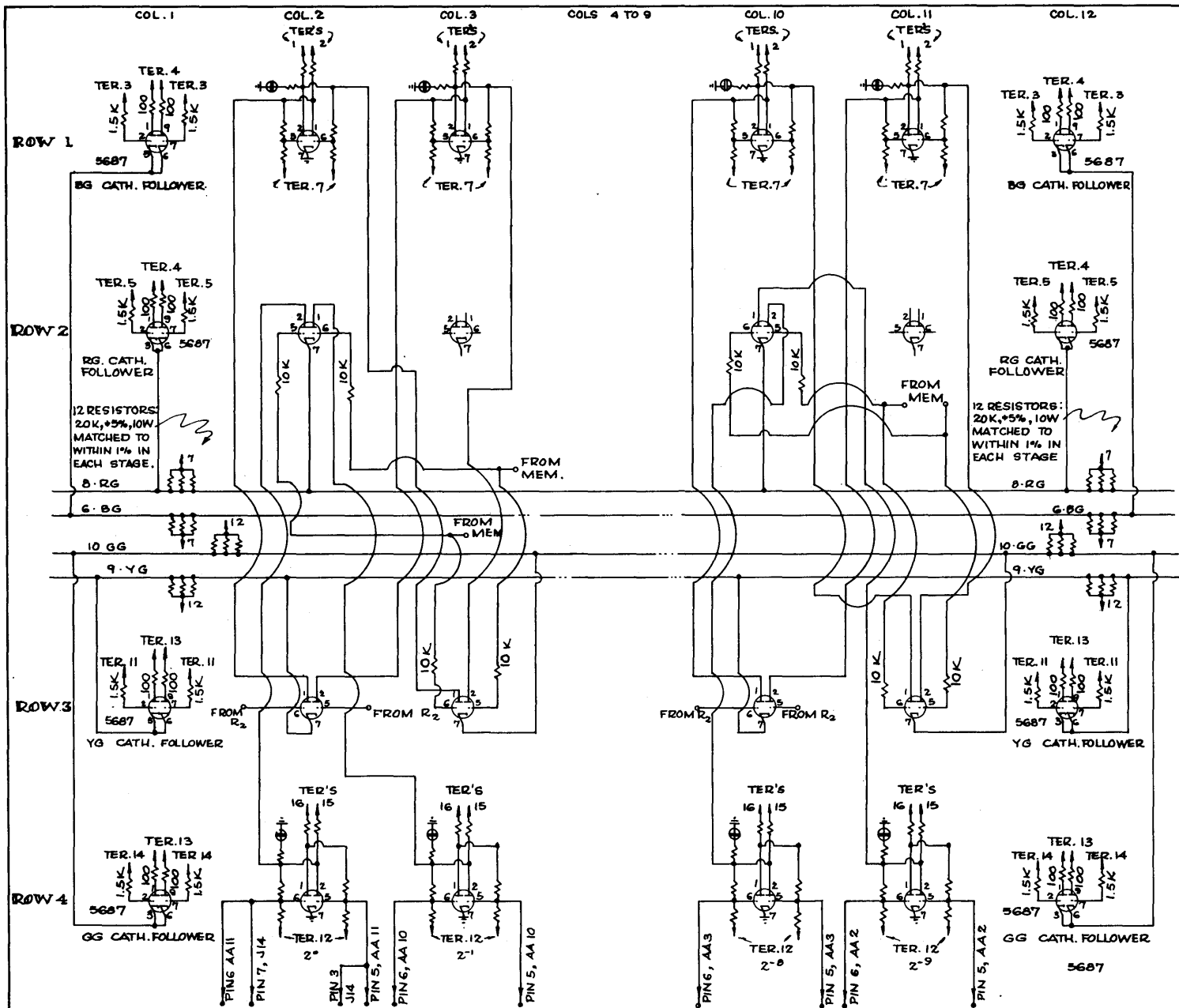
BASE DIAGRAM OF VIDEO AMPLIFIER & WILLIAMS TUBE CONTROL.

FRONT PINS OF VIDEO AMP-LIFIER & WILLIAMS TUBE CONTROL:

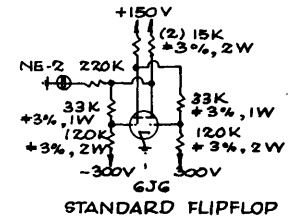
- o TEST 1
- o TEST 2
- o MEM. REG.
- o ACC. REG.
- o NO CONN.

PLUG PIN DIAGRAM FROM REAR OF MACHINE:

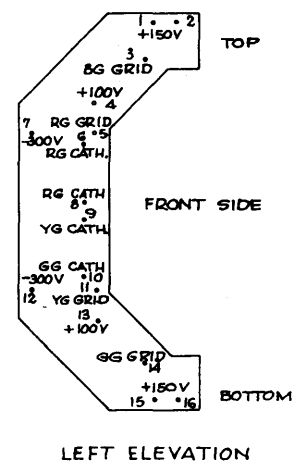
- o K FIL.
- o E FIL.
- o L -300V
- o F REGEN
- o A GRID OF SLAVE CF
- o M WHITE
- o G ACT
- o B DOT
- o N +150V
- o H WDH
- o C 3KPI GRID
- o O +300V
- o I DHT
- o D DE
- o P GND
- o J GND

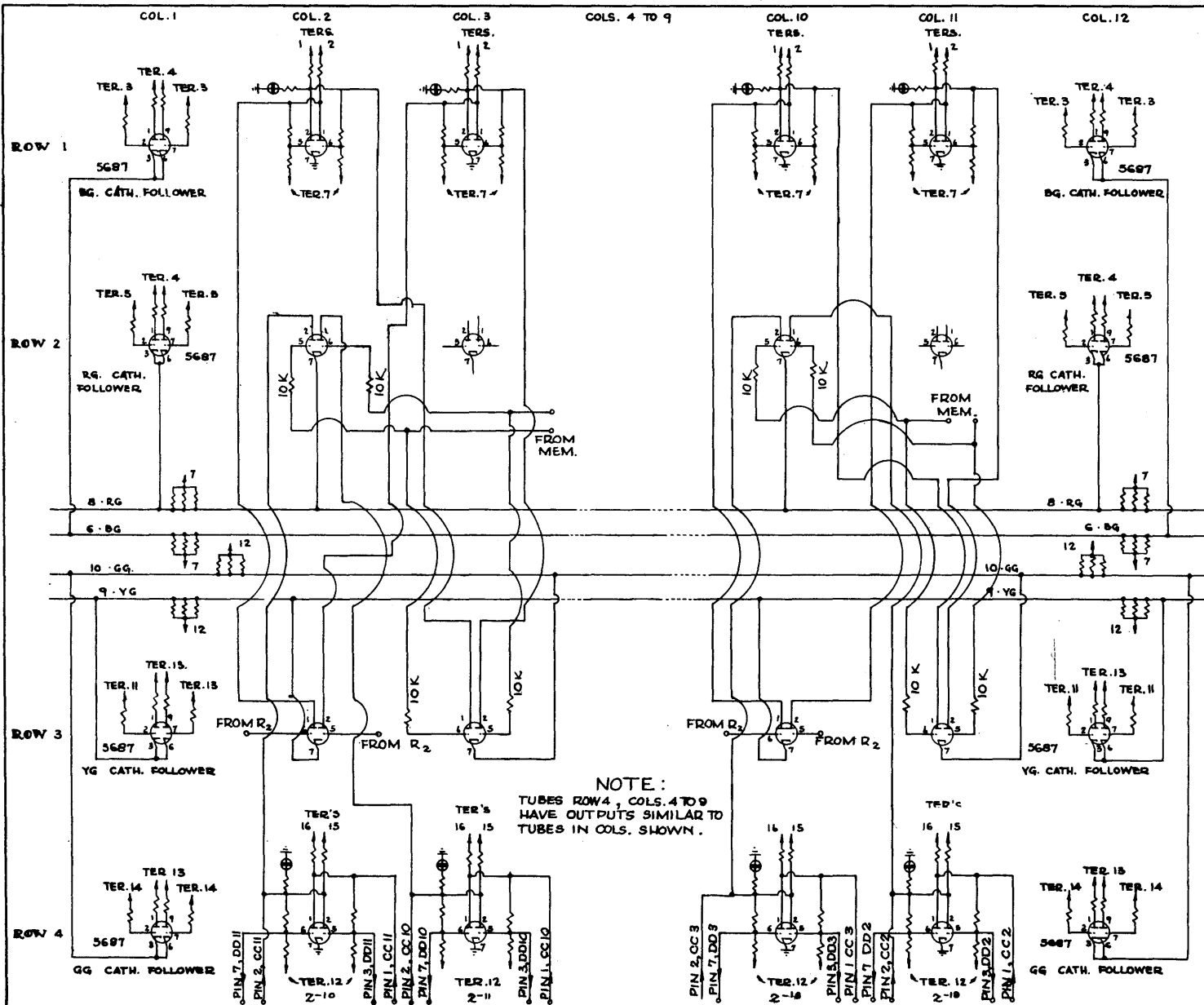


- NOTES:**
1. TUBES UNSPECIFIED ARE 6JG'S.
 2. FILAMENTS ARE AT GND.
 3. WIRING OF COLS. 4, 6, 8 IDENTICAL TO COL. 2.
 4. WIRING OF COLS. 5, 7, 9, IDENTICAL TO COL. 3.



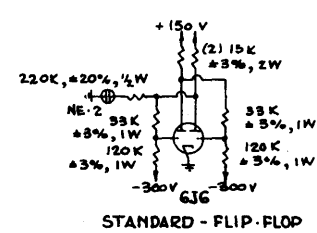
5. UNSPECIFIED RESISTORS ARE +20%, 1/4W
6. REVISED & REDRAWN FROM DRWG. NO. 279 DATED 4-15-51.





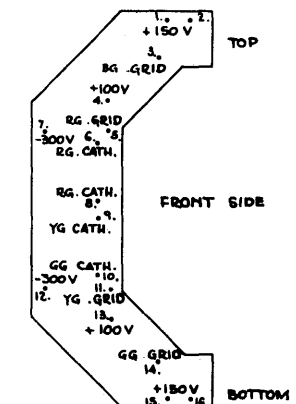
WITH EXCEPTION OF STANDARD FLIP-FLOPS, WHEN NOT SPECIFIED:

- 1. RESISTORS ARE $\pm 20\%$, $\frac{1}{2}W$.



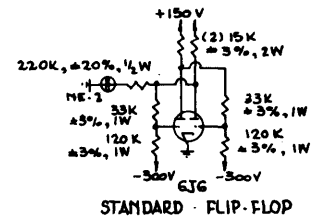
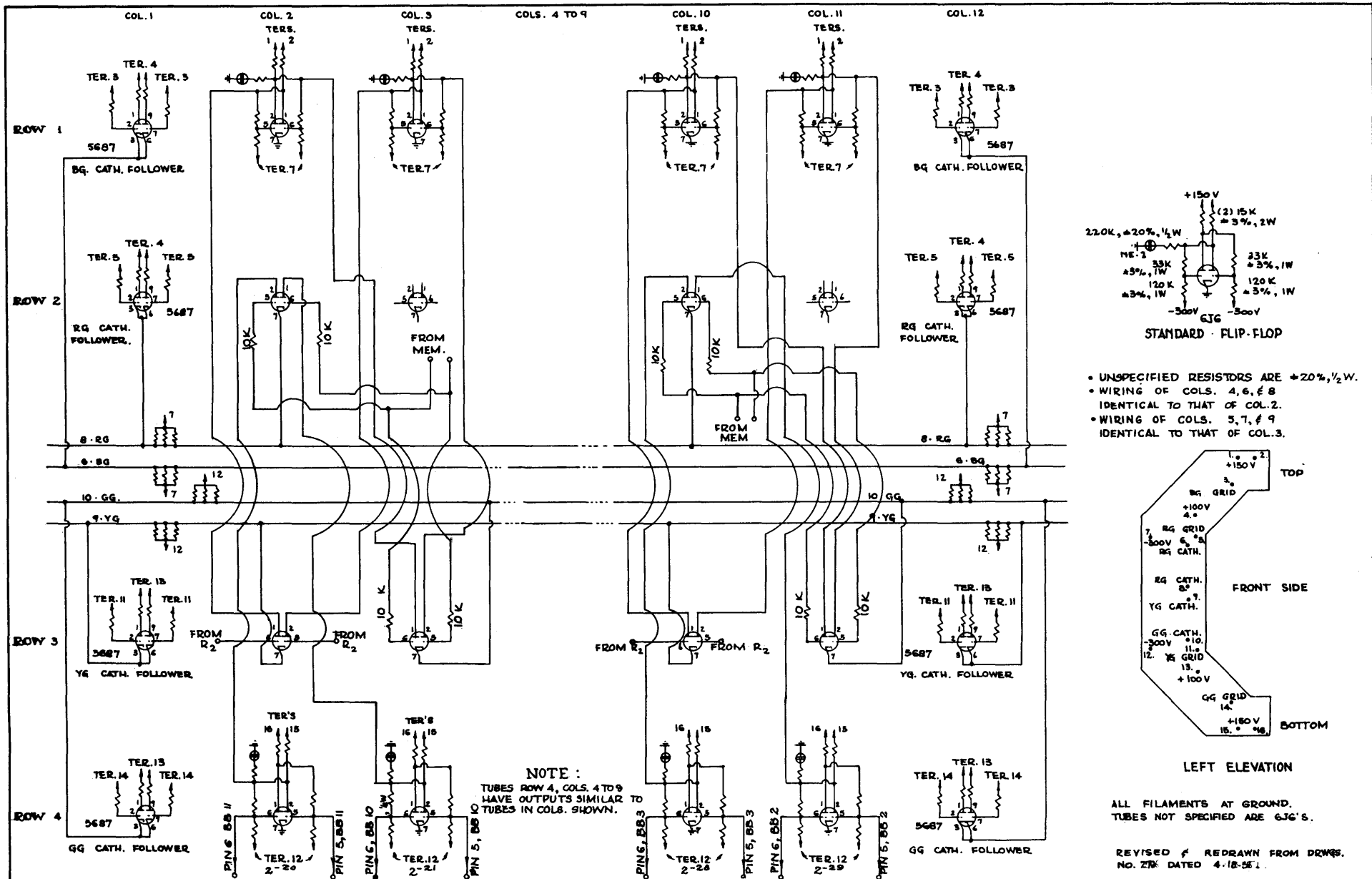
STANDARD - FLIP-FLOP

WIRING OF COLS. 4, 6, & 8 IDENTICAL TO THAT OF COL. 2.
WIRING OF COLS. 5, 7, & 9 IDENTICAL TO THAT OF COL. 3.

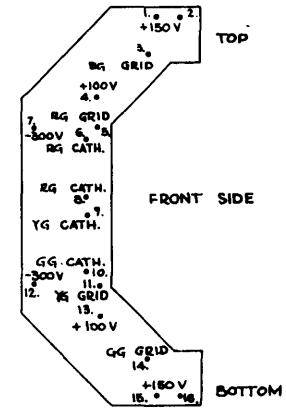


LEFT ELEVATION

ALL FILAMENTS AT GROUND
TUBES NOT SPECIFIED ARE 6J6'S.
REVISED & REDRAWN FROM DRWGS.
NO. 279 DATED 4-18-51



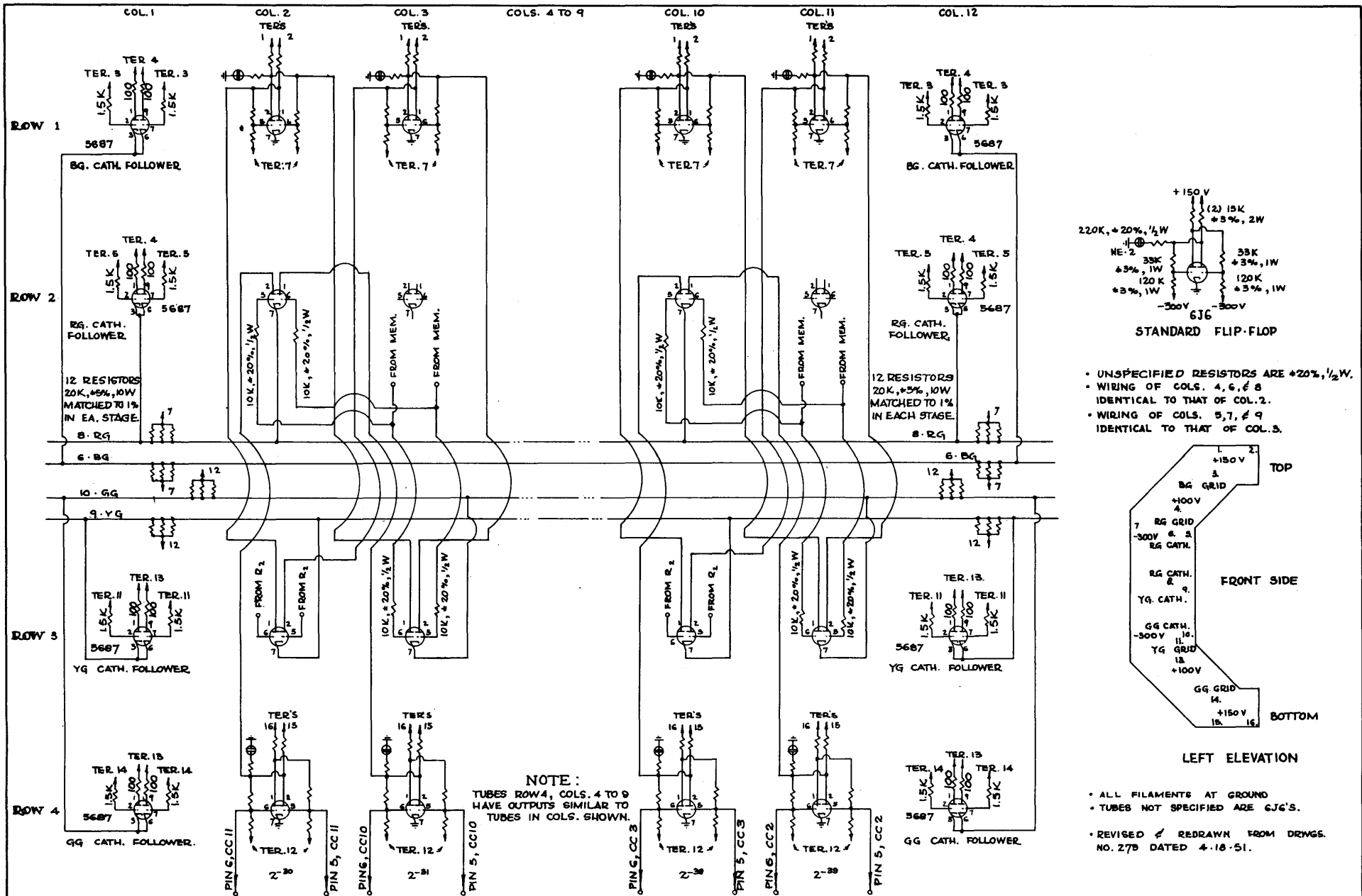
- UNSPECIFIED RESISTORS ARE $\pm 20\%$, $1/2$ W.
- WIRING OF COLS. 4, 6, & 8 IDENTICAL TO THAT OF COL. 2.
- WIRING OF COLS. 5, 7, & 9 IDENTICAL TO THAT OF COL. 3.

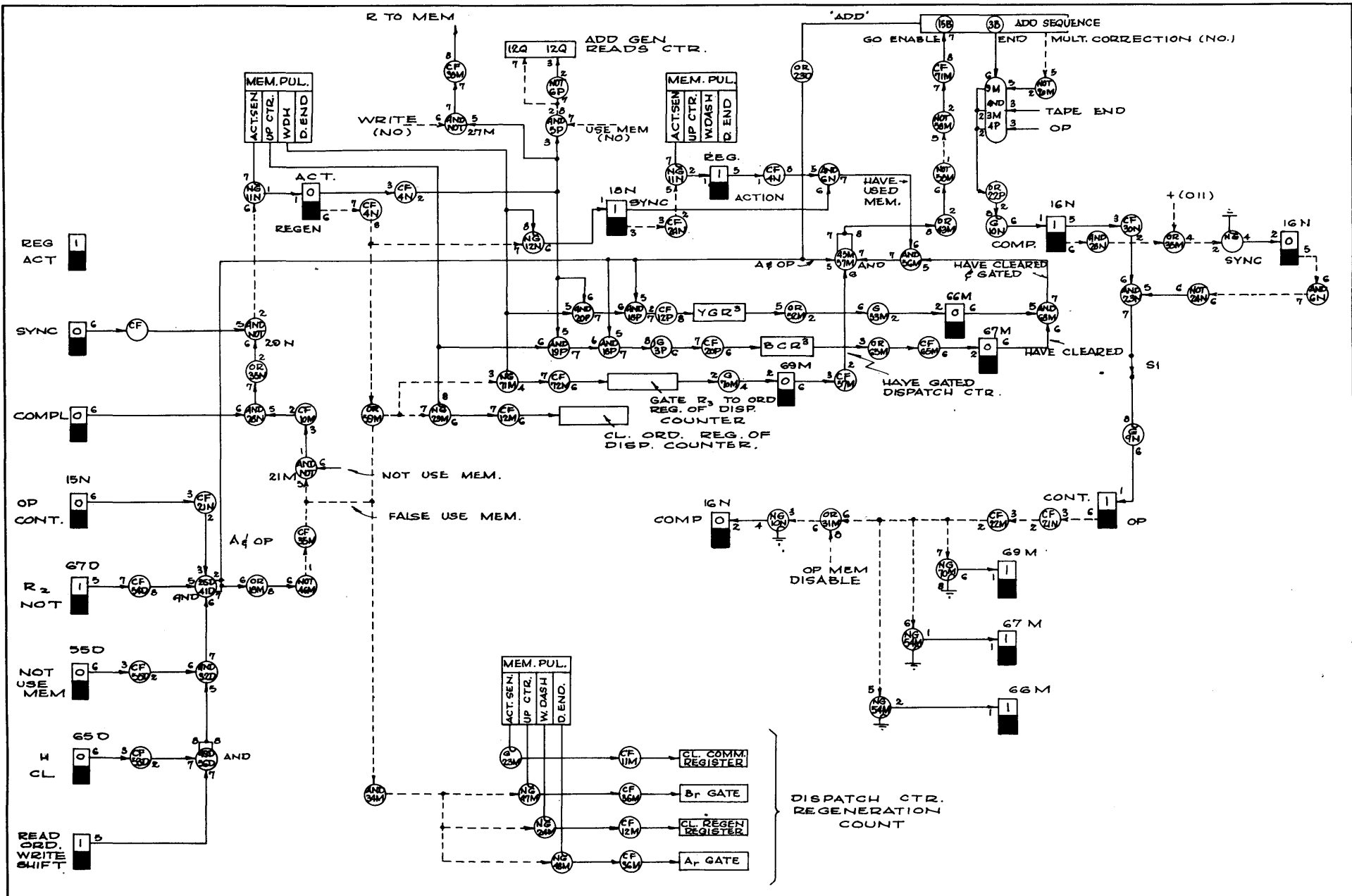


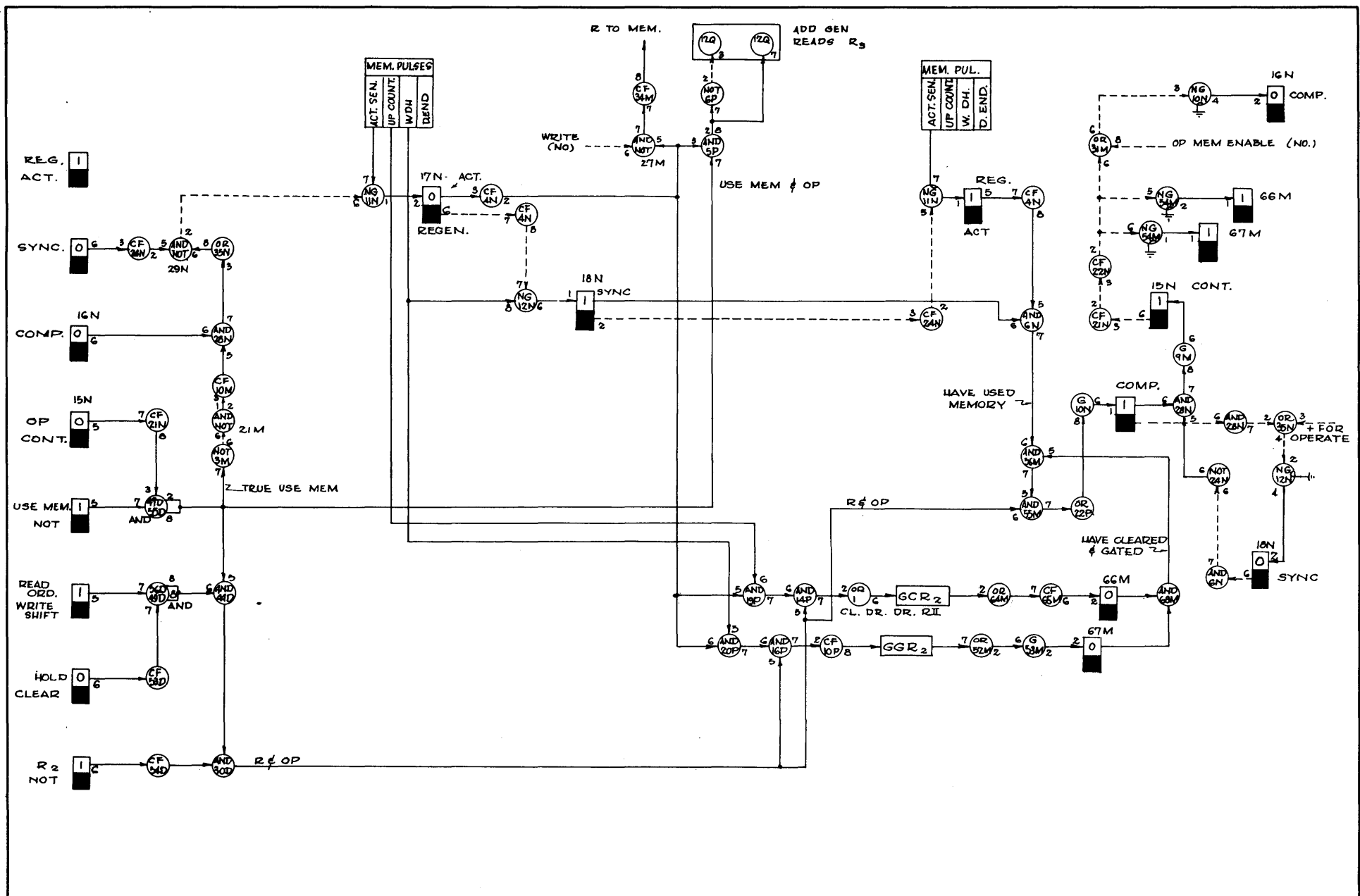
LEFT ELEVATION

ALL FILAMENTS AT GROUND.
TUBES NOT SPECIFIED ARE 6JG'S.

REVISED & REDRAWN FROM DRWS.
NO. 278 DATED 4-18-51.







GAK5

GAK5

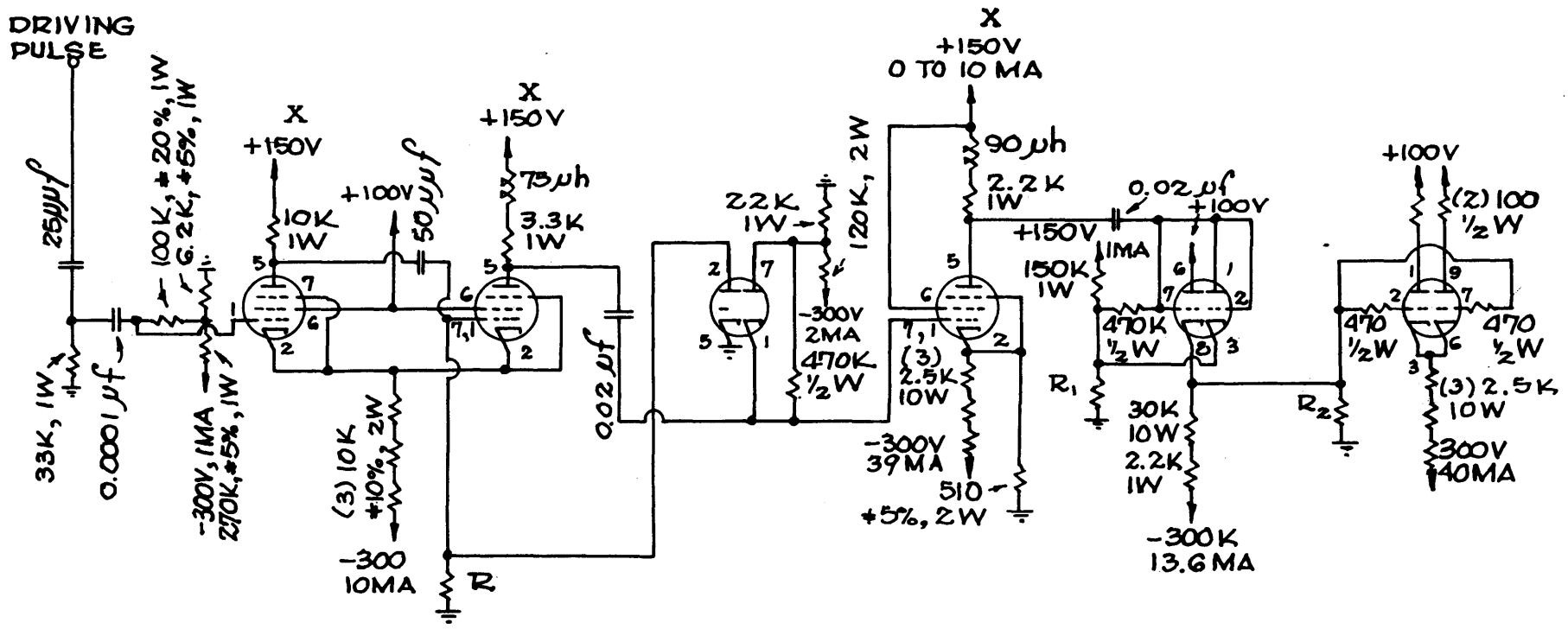
GAL5

GAQ5

12AU7

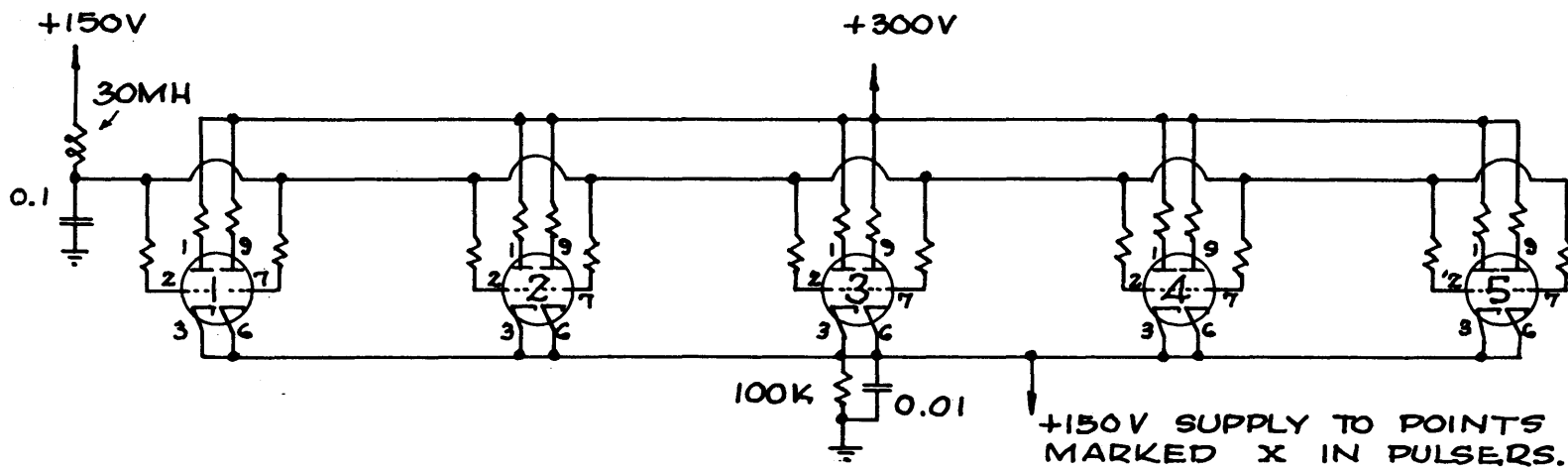
5687

DRIVING PULSE



R IS APPROXIMATELY 20K
 R₁ " " 7.5K
 R₂ " " 3K

RESISTORS NOT SPECIFIED
 ARE ±20%.
 ALL FILAMENTS AT GND.

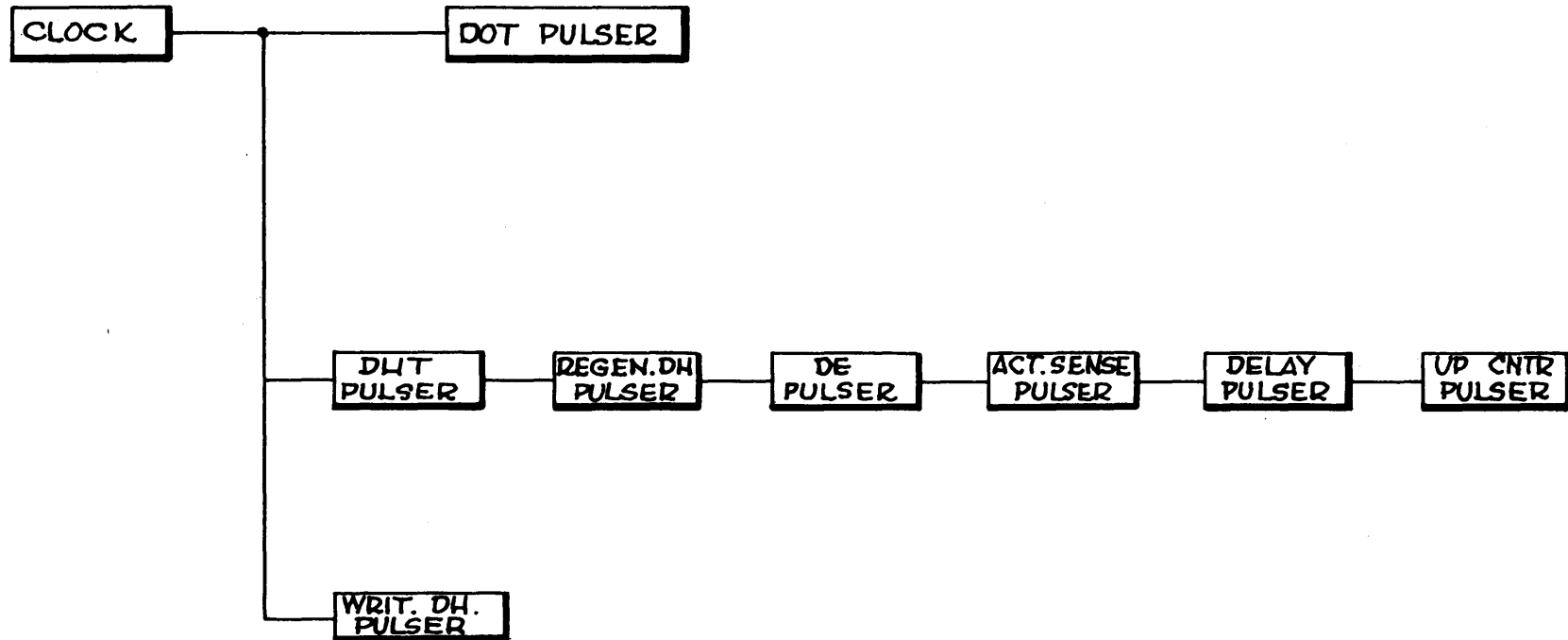


- ALL RESISTORS ARE + 20% , 1/2 W.
- " PLATE RESISTORS ARE 100 Ω .
- " GRID " " 1K .
- " TUBES ARE 5687 'S.
- " FILS. PINNED AT +150V.

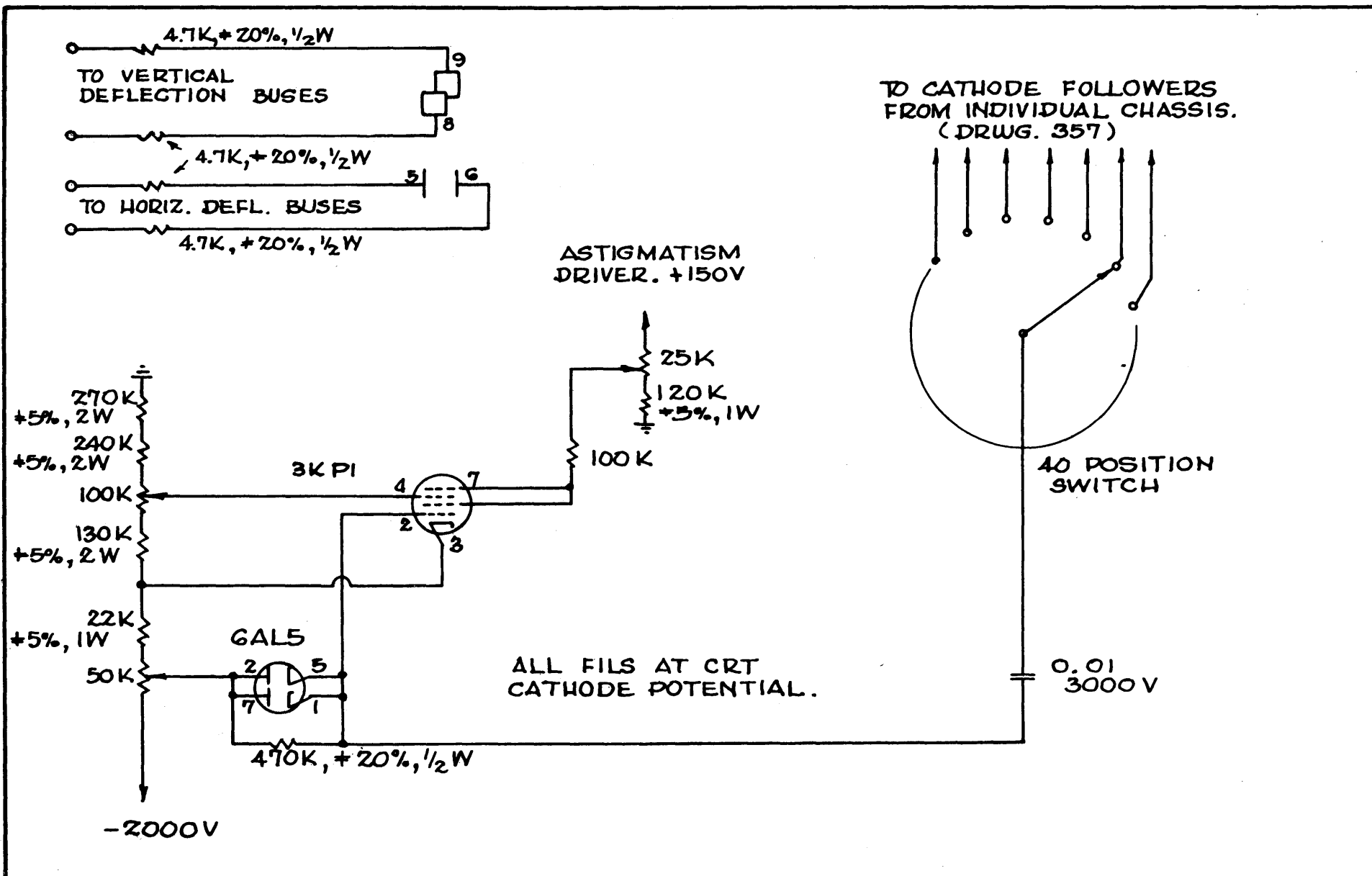
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FOR JMW BY HMW CHECKED *A.M.M.* APPROVED *R.E. Weagher.* DATE 11.13.51

TITLE ~ PULSER SUPPLY CHASSIS S.369



PULSES ARE INITIATED UPON COMPLETION OF THE TRIGGERING PULSE.

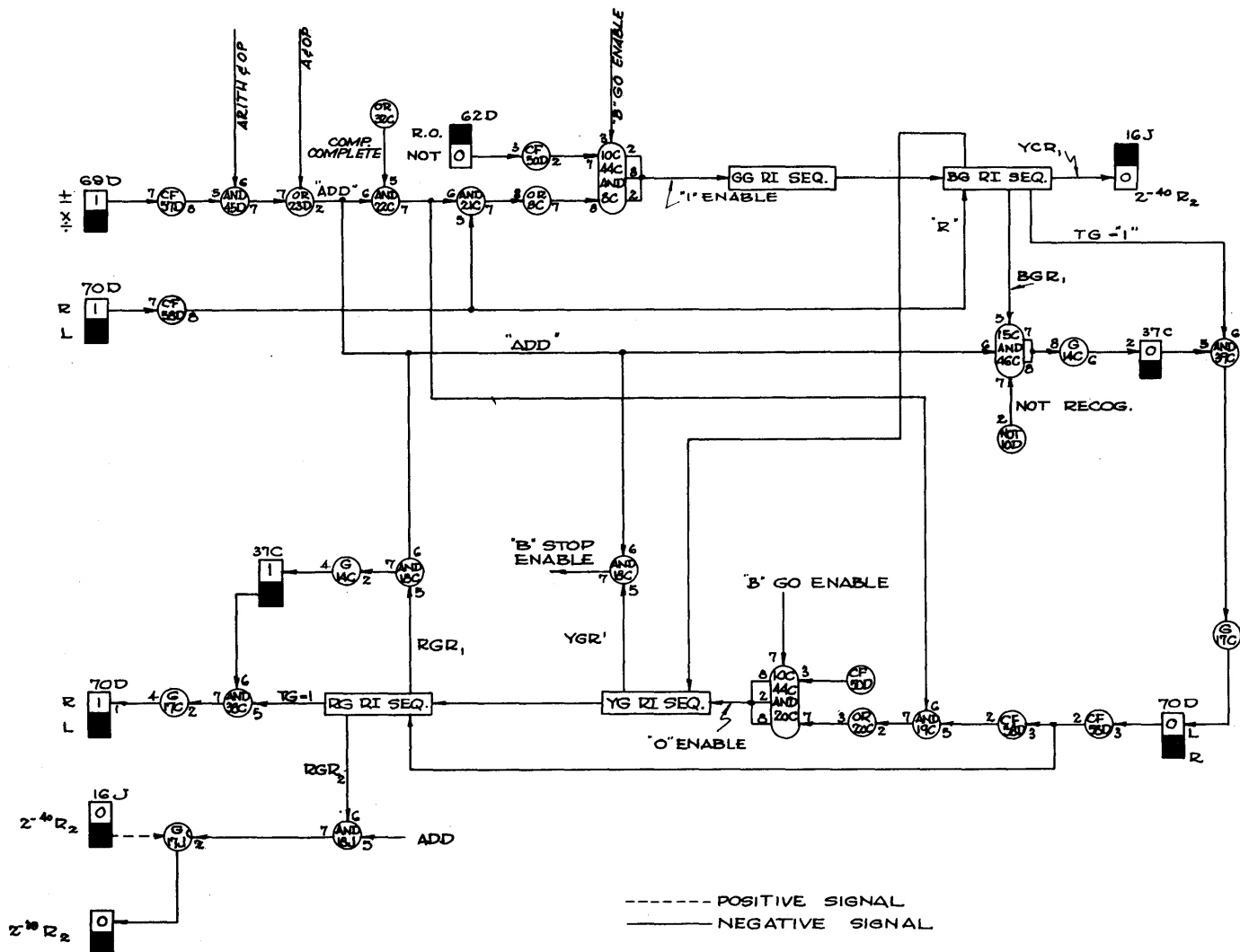


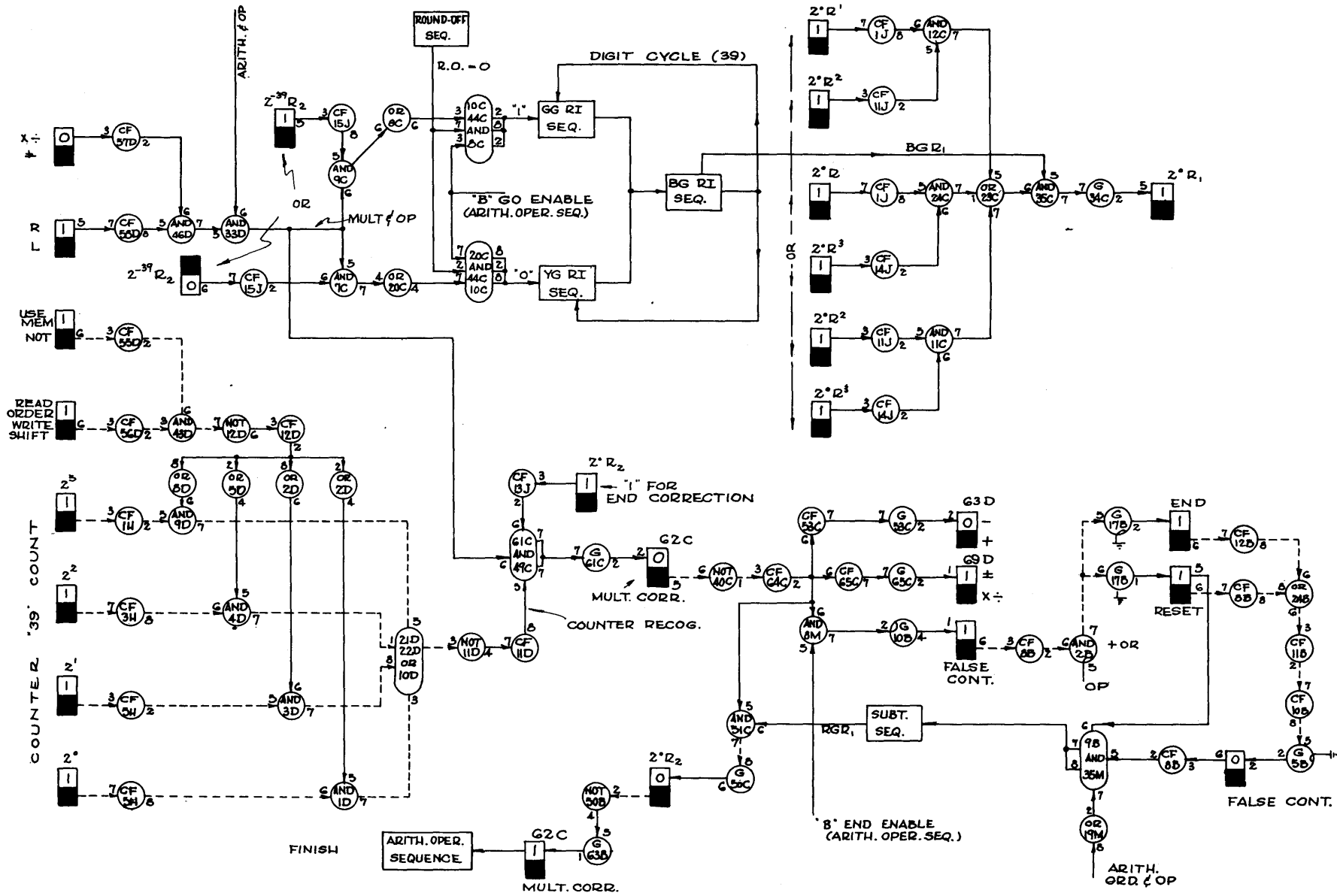
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FOR JMW BY HMW CHECKED J.M. N. APPROVED R. E. Meagher DATE 11-20-51

TITLE - SLAVE TUBE

S-372

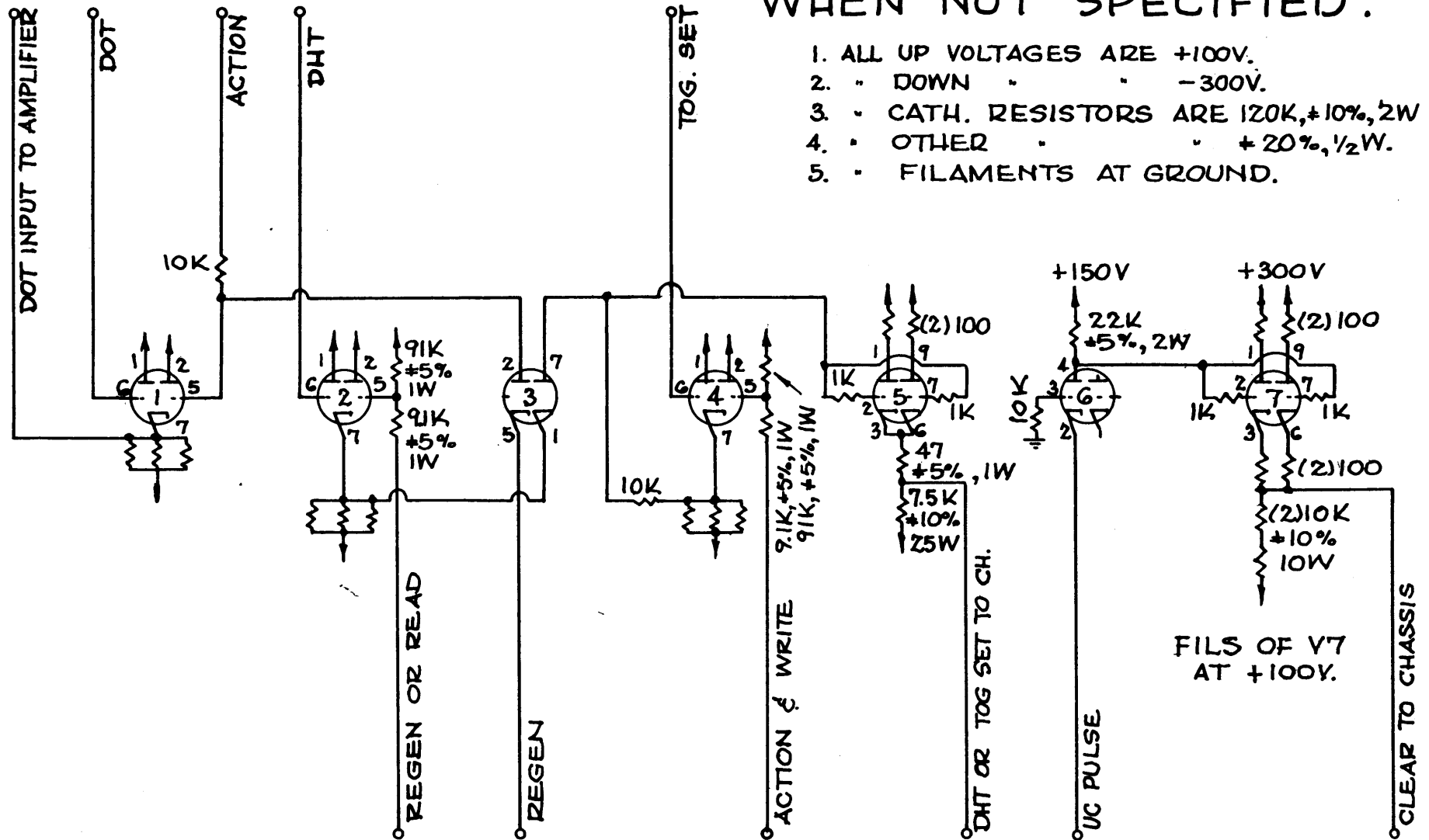




--- POSITIVE SIGNAL
 ——— NEGATIVE SIGNAL

WHEN NOT SPECIFIED:

1. ALL UP VOLTAGES ARE +100V.
2. " DOWN " " -300V.
3. " CATH. RESISTORS ARE 120K, ±10%, 2W
4. " OTHER " " +20%, 1/2W.
5. " FILAMENTS AT GROUND.



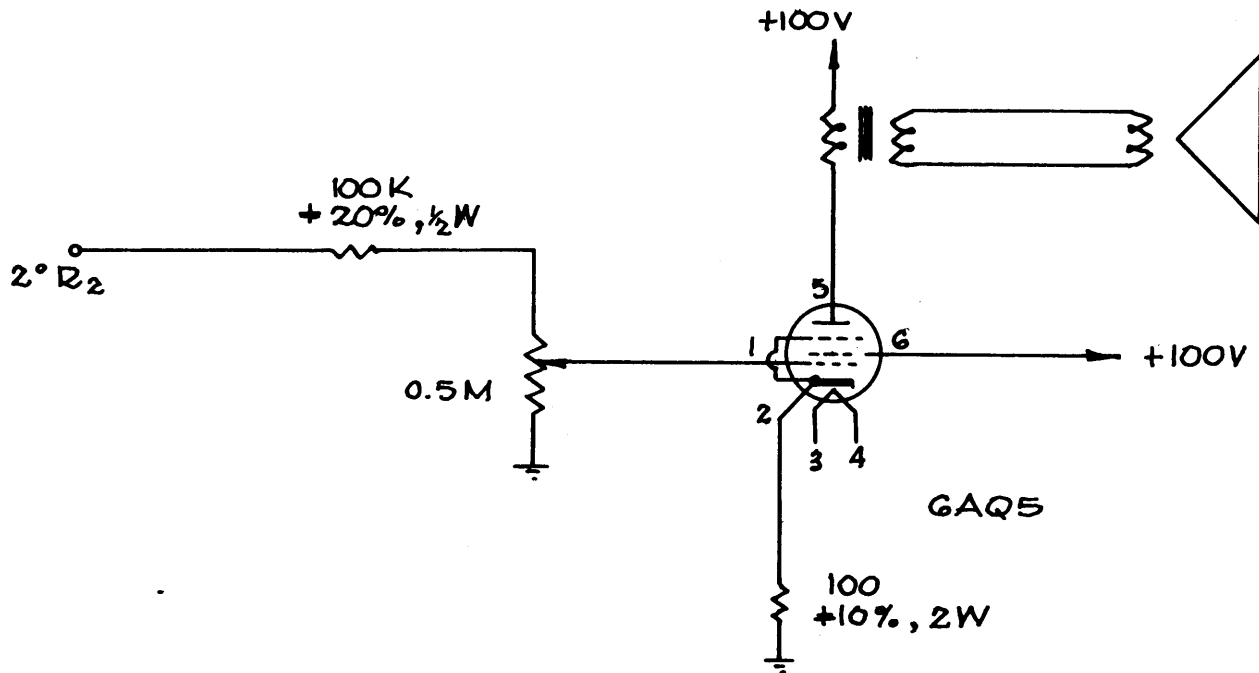
FILS OF V7
AT +100V.

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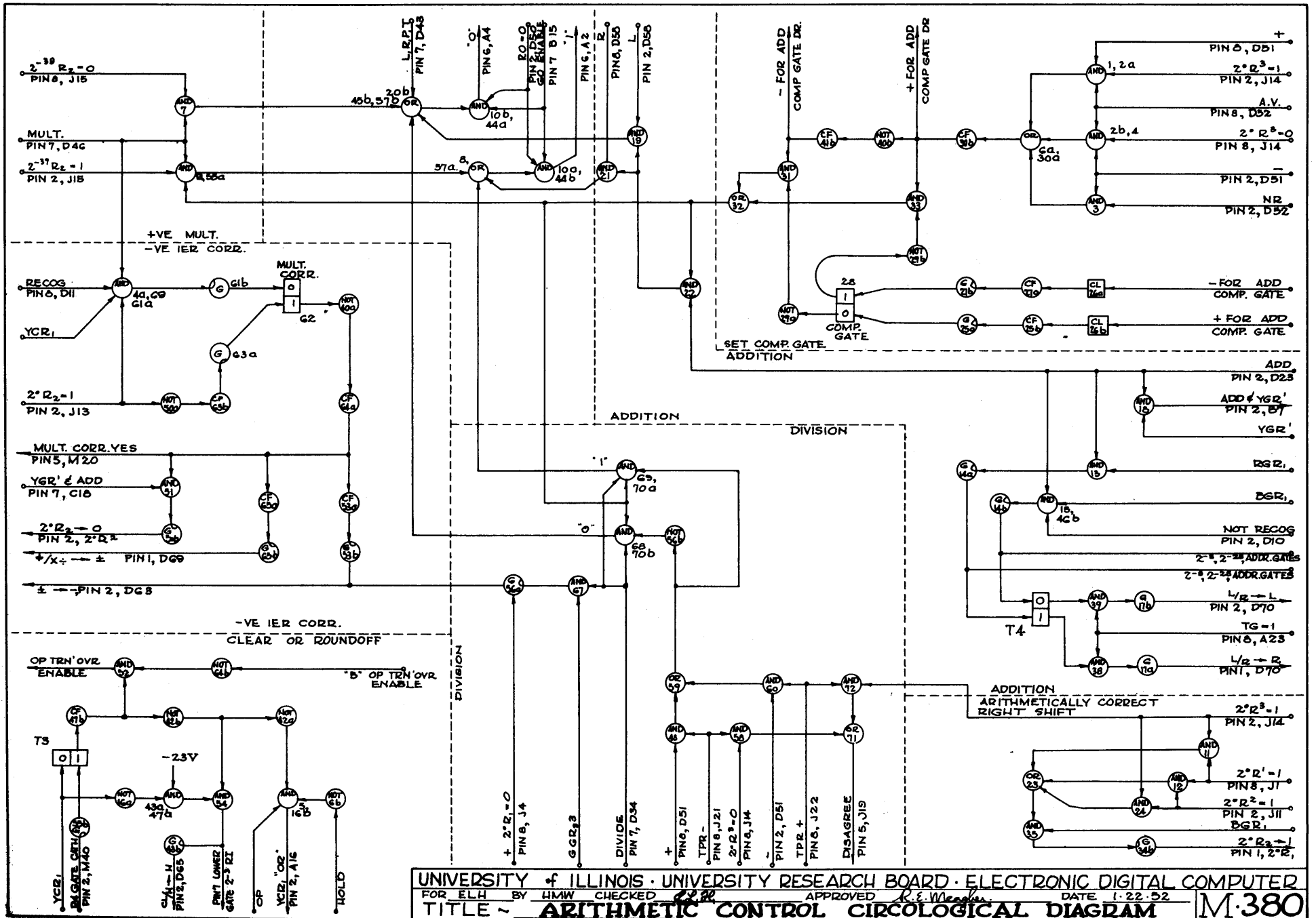
FOR JMW BY HMW CHECKED *J.M.W.* APPROVED *R.E. Meagher* DATE 1-10-52

TITLE - MIXING CKTS. FOR PULSES ON V4 #10

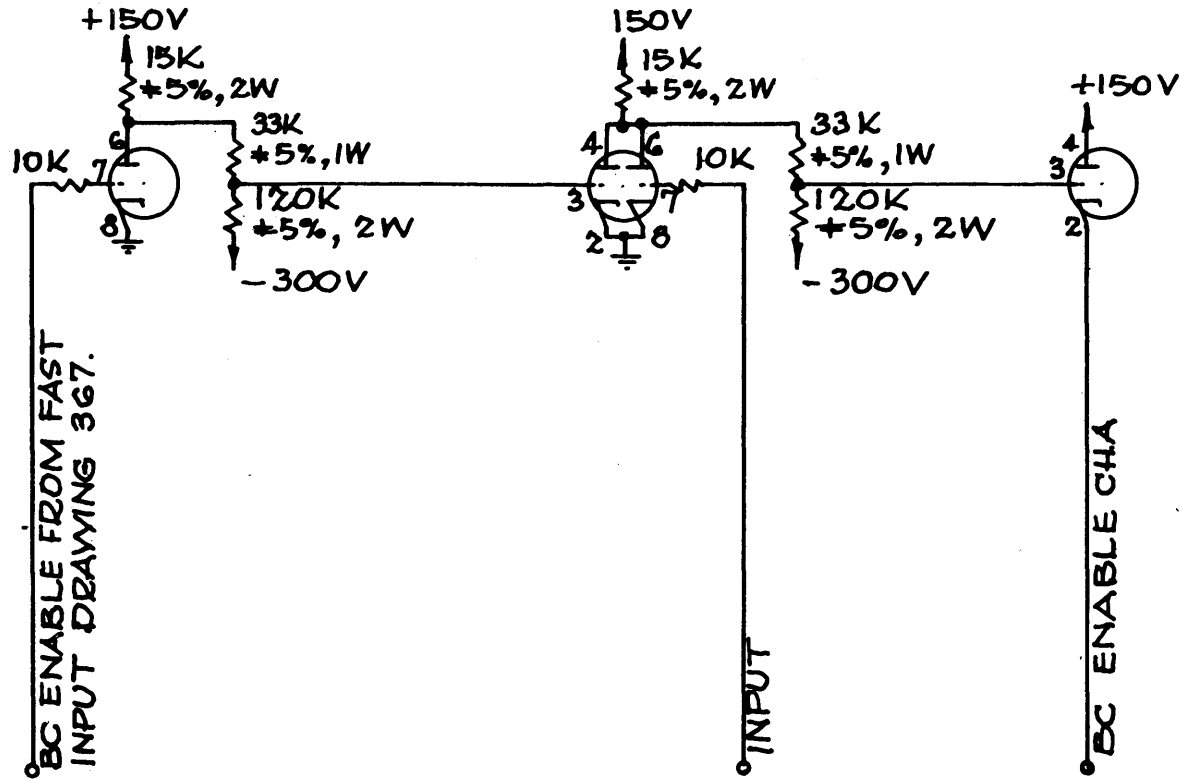
S-378



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 FOR TS BY HMW CHECKED T. SHAPIN APPROVED R. E. Weaghen DATE 1-21-52
 TITLE ~ LOUDSPEAKER CHASSIS S-379



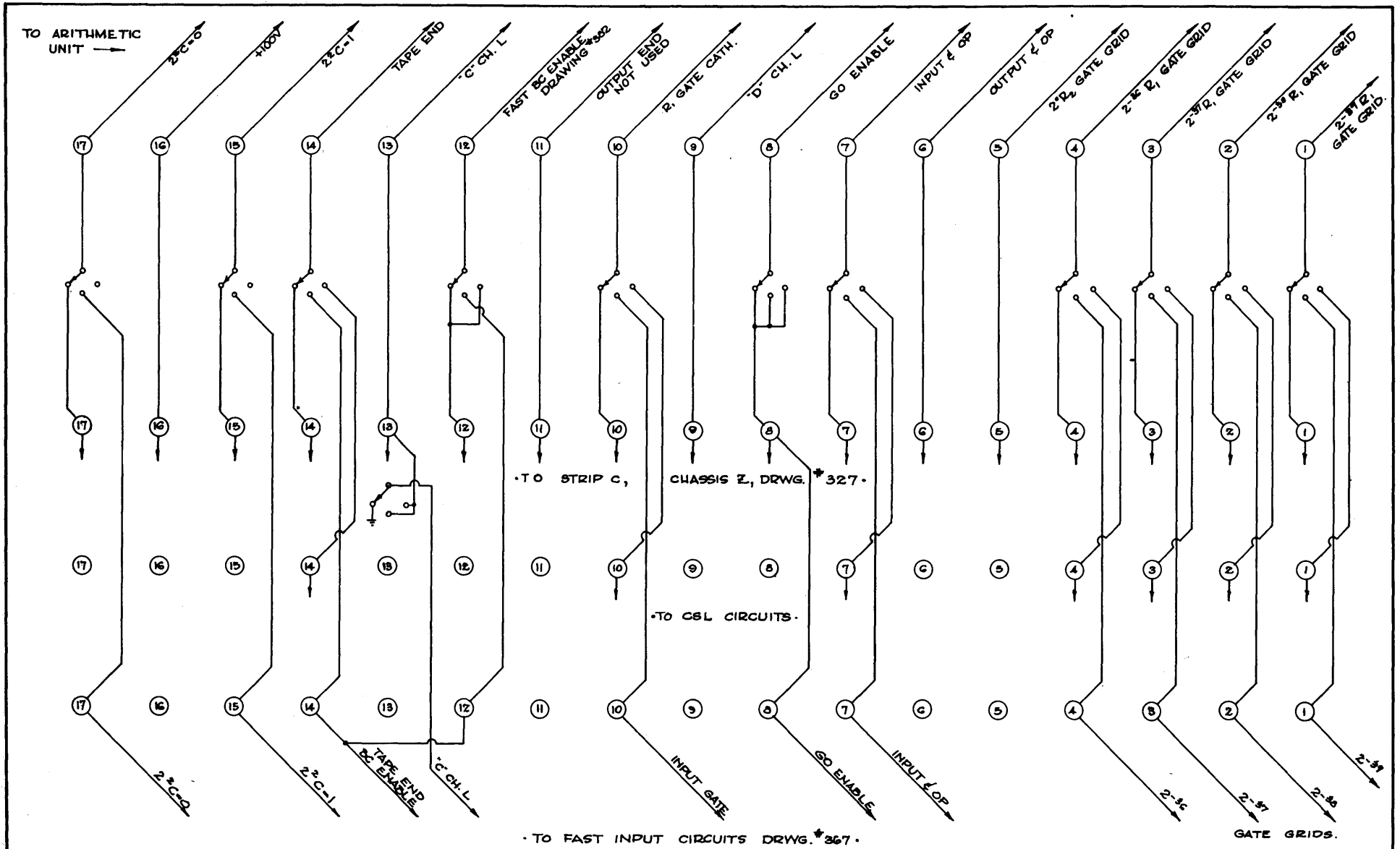
RESISTORS NOT SPECIFIED ARE +20%, 1/2W.



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FOR T.S. BY HMW CHECKED T. SHAPIN APPROVED R. E. Neaghe DATE 1-25-52

TITLE - FAST INPUT BC ENABLE S.382



SLOW INPUT
 FAST INPUT
 CSL INPUT
 • 12 POLE - 3 POSITION SWITCH •