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ILLIAC IV INTERNAL DATA FLOW

by

Theofanis Economidis

June 20, 1974

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INTRAQUADRANT DATA FLOW

I. INTRODUCTION

This document describes the data flow between the Quadrant and the Input/Output Subsystem (IOSS data), the data movement between each MLU in the Array and the Quadrant's CU (CU data) and data movement among the PE's in the Array (data via the routing logic).

The main part of this document is centered upon the Control Unit Buffer (CUB) which is the section of the ILLIAC IV computer that participates in the implementation of two major functions; routing and data transfers.

Data transfers are made via each MLU and include transfers of data from a PE to CU or READ data to CU from a PEM. Because, however, the data transfers to CU via the MLU originate either from each MLU's corresponding PE or a PEM in the Array, the reader is urged to refer to the MLU manual, IAC Doc. No. PO-I1200-0000-A, because this manual fully describes the data movement from the PE and PEM through the MLU and up to the MLU connectors (J26-J31).

For this reason, Section II of this document is devoted to the description of the data movement from the MLU connectors to the CU (ADVAST section). Because, however, the IOSS data shares the same MLU connectors with the CU data and also uses part of the Disconnect (see details in Section II) for its movement between the IOSS and the PEM's, we felt that the description of this data movement (Section III) should be part of this document even though it is not implied by the title.

The description of the implementation and function of the routing logic will be found in Section IV.

Lastly, it must be pointed out that this document is intended to be used for maintenance purposes and for this reason a great deal of care has been exercised not to spare any details that at times may seem to be rather trivial.

II. DATA TRANSFER TO CU VIA THE MLU's

A. Implementation

Figure 1 shows the data movement from a PE (TRANSFER operation) or PEM (READ operation) via the MLU to CU. The CU data from each MLU is brought to the next MLU in a "daisy-chain" fashion, where the last MLU in the PU cabinet connects directly to six connectors which constitute part of the so-called DISCONNECT. From the DISCONNECT, the data is brought into the Control Unit Buffer (CUB), which is composed of eight boards partitioned into two groups of four boards each and designated by L and K, respectively. Each of the CUB modules takes care of eight bits and its output is brought to the backplane section of the CU which is located on the third row (from top to bottom) and the third column (from left to right) and which is designated by the number 9.

The data then is brought into the ATPO2 type CU boards (eight of them) in the form of a full 64-bit word, that is, 64 bits of data in each. It must be mentioned at this point that the ATPO2 boards receive 64 bits from each processing unit. cabinet (PUC) and, therefore, it can be said that if all the PUC's are active at one time, then a word of 512 bits is received by the ATPO2's.

1. Data Movement from MLU to DISCONNECT

CU data from each of the last of the MUL's in each cabinet is brought into the DISCONNECT via belted, 25-conductor cables. These cables pick up the 64 bits of data and two strobes from the IO/CUB connectors (Figure 2), and through a daisy chain, bring it to the DISCONNECT.

On the bottom of each PU there are six logic cards called IO/CUB cards (Figure 3) which are used to take care of both the CU data and IOSS data. Each one of these six cards has a connector mounted on the right edge as we look on the component side of the card. Figure 2 shows the pin configuration of that connector. When the cards are plugged into the MLU portion of the PU (J26-J31), a paddle board is inserted into each IO/CUB connector to pick up the data and distribute it to the DISCONNECT (see Table 1).

Because at any time only one PU within each PU cabinet may transfer data to CU (via the MLU), the paddle boards (six of them) from each MLU are connected to the corresponding paddle boards of the neighboring MLU in a daisy chain fashion from right to left as shown in Figure 4. Table 2 shows the data distribution among the six connectors of the MLU and of those of the DISCONNECT.

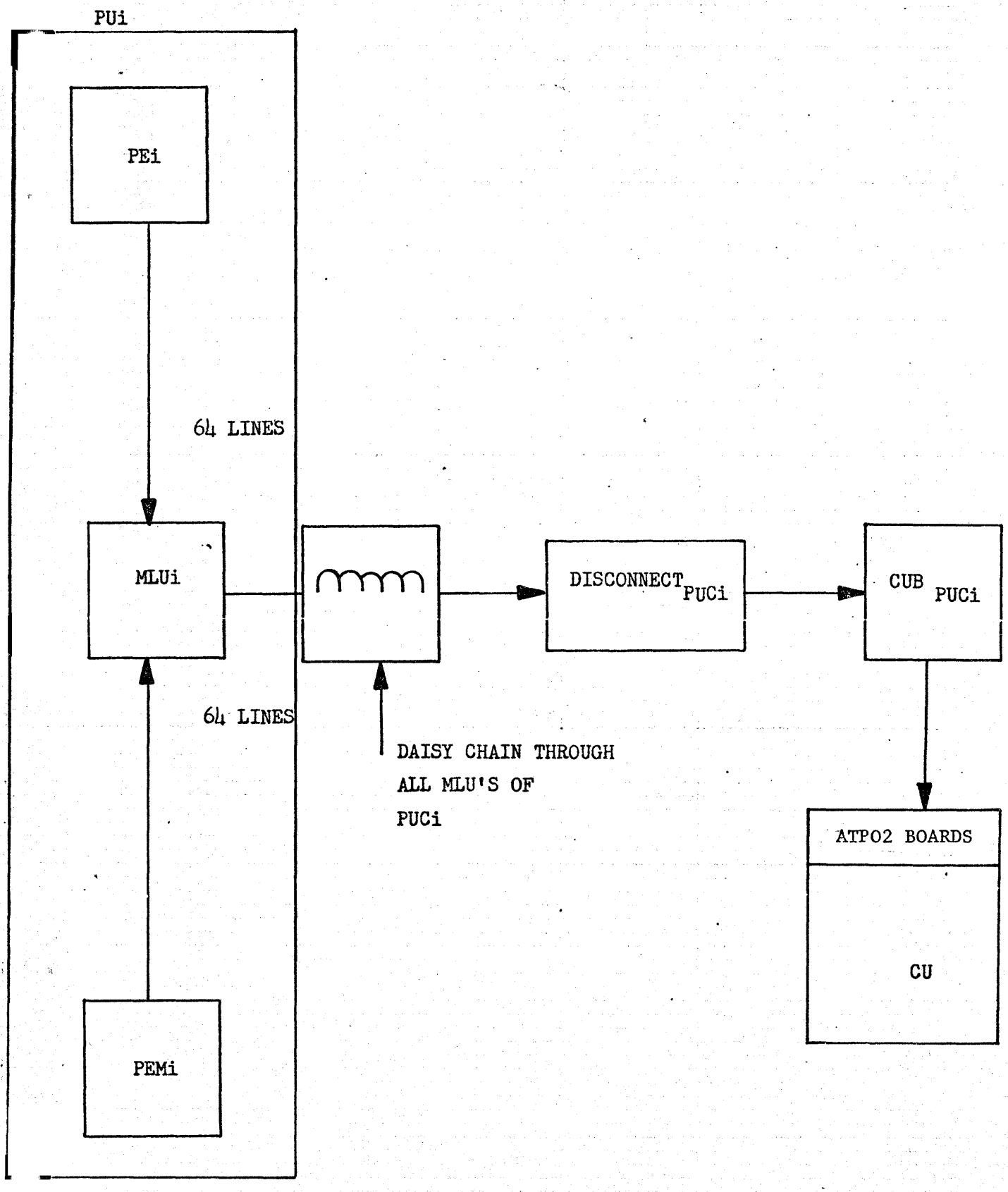

FIGURE 1. BLOCK DIAGRAM OF DATA MOVEMENT FROM PEM/PE TO CU.

TABLE 1. CU/IOSS BITS ASSIGNMENT TO MLU CONNECTORS AND IO/CUB CARDS

MLU Connector	J26	J27	J28	J29	J30	J31	Remarks
IOB/CUB Card	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	
CU	0	11	22	32	43	54	J26 through J31
or	1	12	23	33	44	55	are the MLU
IOSS	2	13	24	34	45	56	connectors which
	3	14	25	35	46	57	are used for CU
DATA	4	15	26	36	47	58	and IOSS data.
	5	16	27	37	48	59	I/01 through
BITS &	6	17	28	38	49	60	I/06 are the
	7	18	29	39	50	61	IO/CUB Cards
STROBES	8	19	30	40	51	62	(See Figure 3)
	9	20	31	41	62	63	
	10	21	CUB STROBE	42	53	CUB & I/O STROBES	

It is evident that since only the even pin numbers of each IO/CUB connector are associated with the CU data (odd pin numbers are used for IOSS data), the belted cable on the right side of the paddle board which is connected with the paddle board of the corresponding IO/CUB connector of the neighboring MLU is the one which carries the CU data. The paddle boards of the MLU which are physically located closest to the DISCONNECT (left side of the PU cabinet) are connected directly to the DISCONNECT in the fashion shown in Table 2. For an illustration (see Figures 4 and 5a), the belted cable on the right side of the paddle board plugged into the IO/CUB connector at J26 of PU00 which is housed into PUC00 is connected to the paddle board at J26 of PU70. The latter is connected to J26 of PU10 which in turn connects to J26 of PU60. J26 of PU60 is connected to J26 of PU20. J26 of PU20 connects to J26 of PU50, which connects to J26 of PU30. J26 of PU30 connects to J26 of PU40 which finally connects to connector 00-M5 of the DISCONNECT. The other five IO/CUB connectors are connected in the same fashion with their corresponding connectors of the neighboring MLU's as shown for connector J26.

Figure 5b shows the actual interconnections of all the MLU's with the DISCONNECT with in a PU cabinet.

Because each MLU in the Array is an integral part of its Processing Unit (PU) and because each PU has been assigned a two-digit octal number, it should be understood that whenever a reference is made to an MLU by its PU number this number reflects the position of the MLU with regard to the other MLU's within a PUC and subsequently within the Array. For this reason, the first octal digit (most significant digit) of the two-digit octal number represents the position of the MLU (or PU) within the PUC and the second digit (least significant digit) represents the position of the PUC within the Array. The positions of the PU's within a PUC and of the PUC within the Array have been defined in sequential order from left to right as 43526170 when looking at the ILLIAC IV Quadrant with the CU on the extreme right side (Figure 5a).

2. Data Movement from DISCONNECT to CUB Boards

The DISCONNECT is a set of 12 pairs of paddle boards and connectors used exclusively for CU and IOSS data. In other words, each belted cable from the MLU connectors (J26 through J31) is connected via its paddle board to a connector located at the DISCONNECT. Because, as shown in Table 2, the CU data (64 data bits and two strobes) are connected to six DISCONNECT connectors (M1-M6) while the other

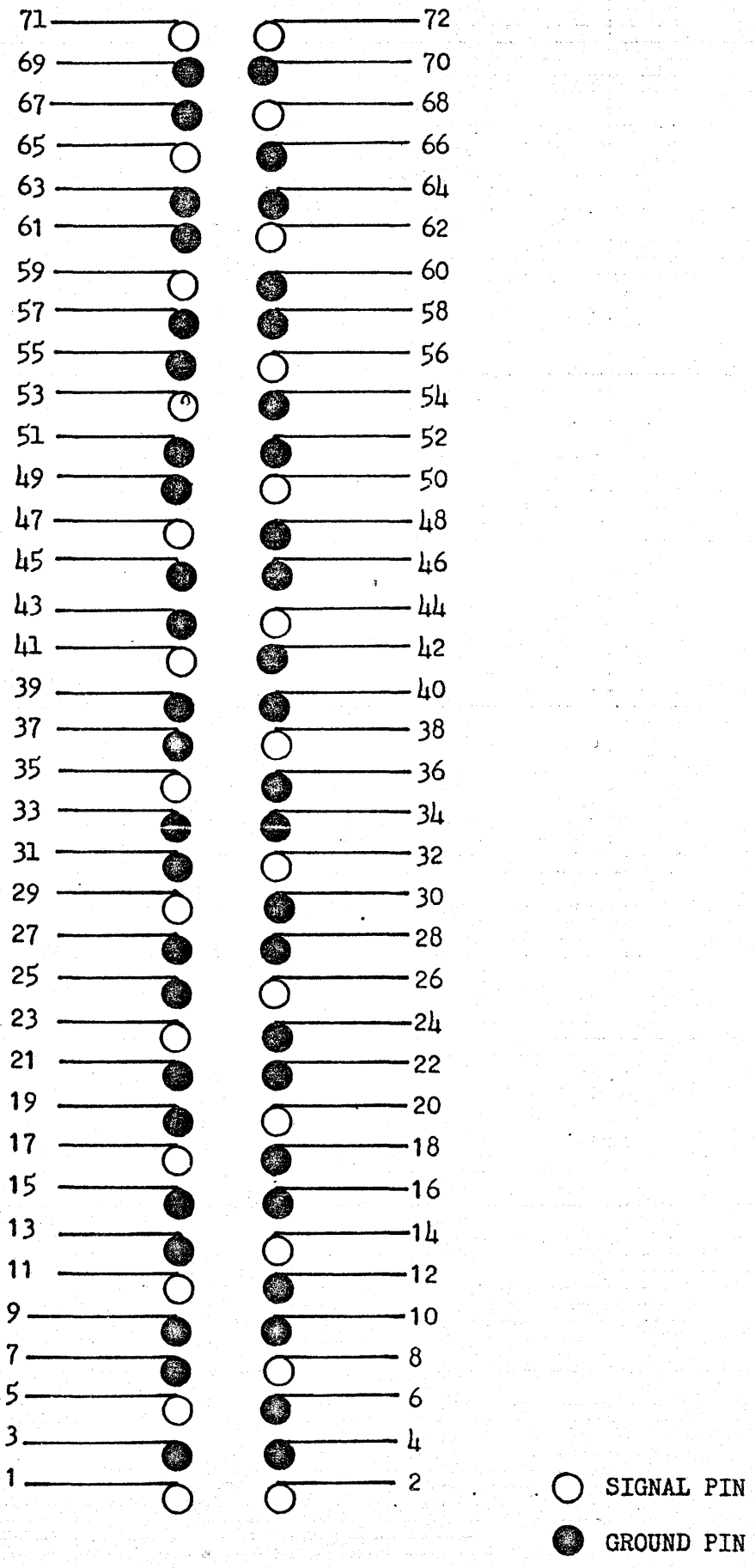

FIGURE 2. IO/CUB CONNECTOR (J26-J31)

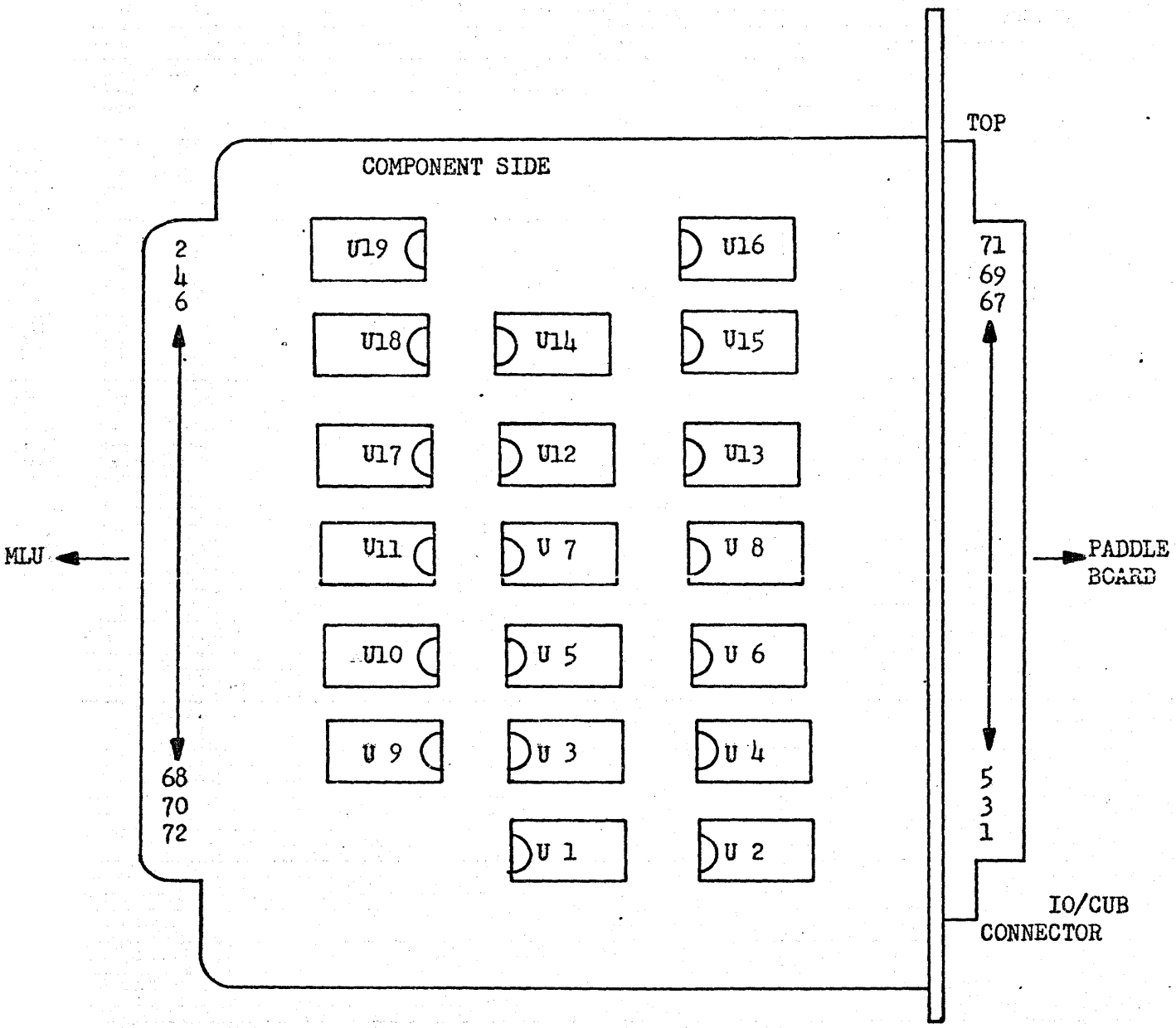

FIGURE 3. IO/CUB CARD AT MLU J26-J31 SLOTS

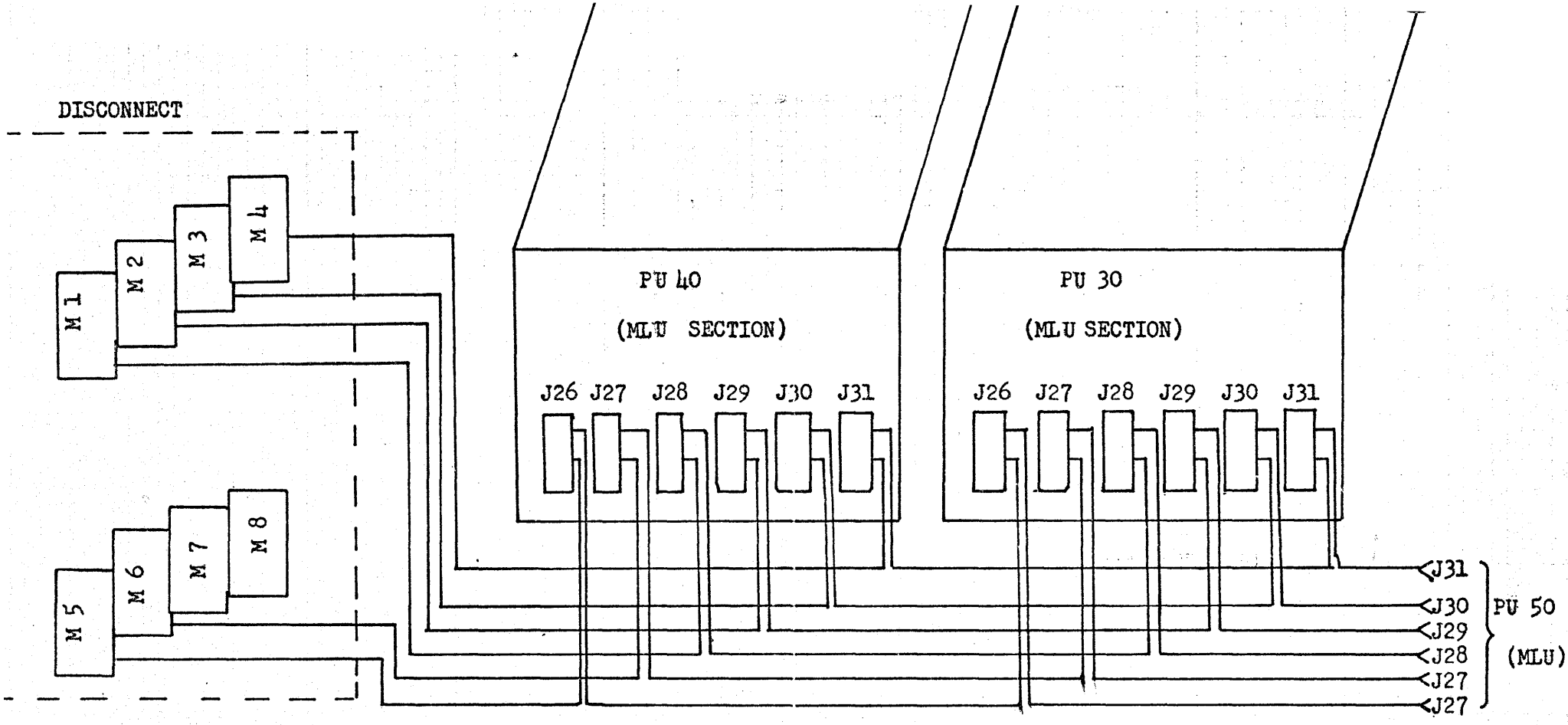

FIGURE 4: MLU INTERCONNECTIONS WITHIN A PUC FOR CU DATA

NOTE: 1. FIGURE 4 SHOWS THE MLU INTERCONNECTIONS WITHIN PUCO FOR CU DATA

2. THE DISCONNECT CONTAINS 4 MORE CONNECTORS WHICH ALONG WITH M7 & M8 TAKE CARE OF THE IOSS DATA (THEY ARE NOT SHOWN HERE).

3. THE MLU OF PU 50 IS CONNECTED IN TURN WITH PU 20,60,10,70,00.

SIGNAL NAME	MLU (SOURCE)		DISCONNECT (DESTINATION)		REMARKS
	Connector	Pin	Connector	Pin	
MOWCW 00--0	J26	08	M5	2	The data is daisy chained from each connector (J26 through J31) of one MLU to all the corresponding connectors of the MLU's of each PUC. This applies to all MOWCWxx data.
01		14		5	
02		20		8	
03		26		10	
04		32		12	
05		38		14	
06		44		16	
07		50		18	
08		56		20	
09		62		22	
10	J26	68	M5	25	
11	J27	08	M6	2	
12		14		5	
13		20		8	
14		26		10	
15		32		12	
16		38		14	
17		44		16	
18		50		18	
19		56		20	
20		62		22	
21	J27	68	M6	25	
22	J28	08	M1	2	
23		14		5	
24		20		8	
25		26		10	
26		32		12	
27		38		14	
28		44		16	
29		50		18	
30		56		20	
31		62		22	
MZTMWCW-0	J28	68	M1	25	

Table 2. Data Movement from MLU to DISCONNECT

SIGNAL NAME	MLU (SOURCE)		DISCONNECT (DESTINATION)		REMARKS
	Connector	Pin	Connector	Pin	
MOWCW 32-0	J29	08	M2	2	
33		14		5	
34		20		8	
35		26		10	
36		32		12	
37		38		14	
38		44		16	
39		50		18	
40		56		20	
41		62		22	
42	J29	68	M2	25	
43	J30	08	M3	2	
44		14		5	
45		20		8	
46		26		10	
47		32		12	
48		38		14	
49		44		16	
50		50		18	
51		56		20	
52		62		22	
53	J30	68	M3	25	
54	J31	08	M4	2	
55		14		5	
56		20		8	
57		26		10	
58		32		12	
59		38		14	
60		44		16	
61		50		18	
62		56		20	
63		62		22	
MZTMWCW-2	J31	68	M4	25	

Table 2 - continued. Data Movement from MLU to DISCONNECT

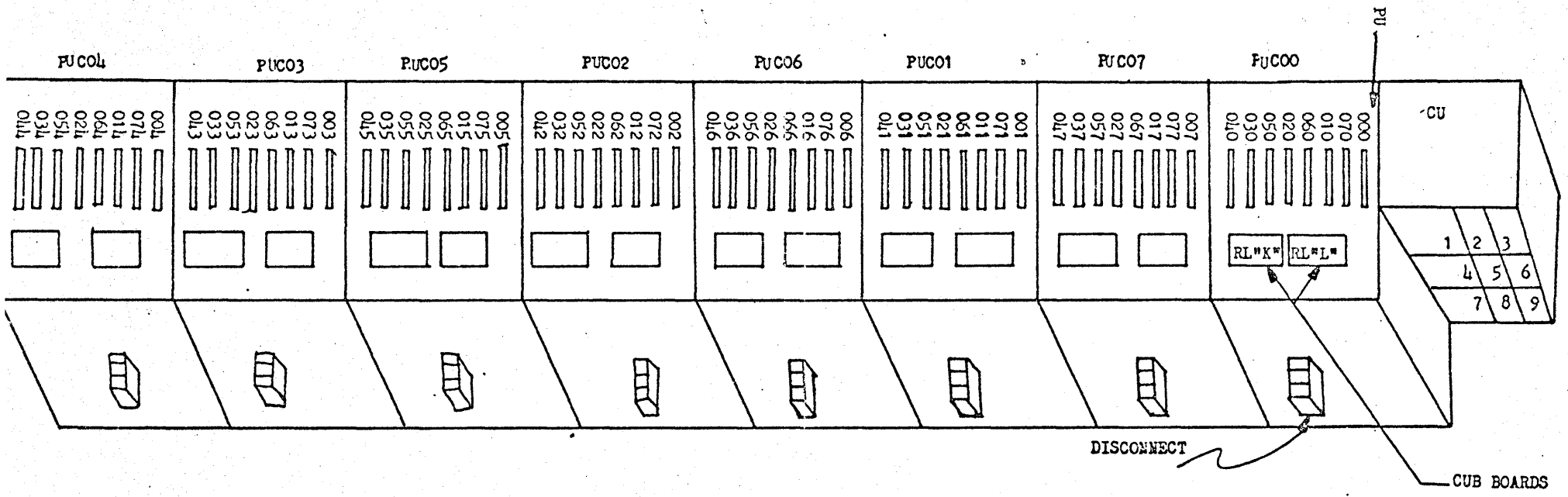

FIGURE 5(a): PHYSICAL REPRESENTATION OF PU_s, DISCONNECT AND CUB BOARDS WITHIN THE QUADRANT

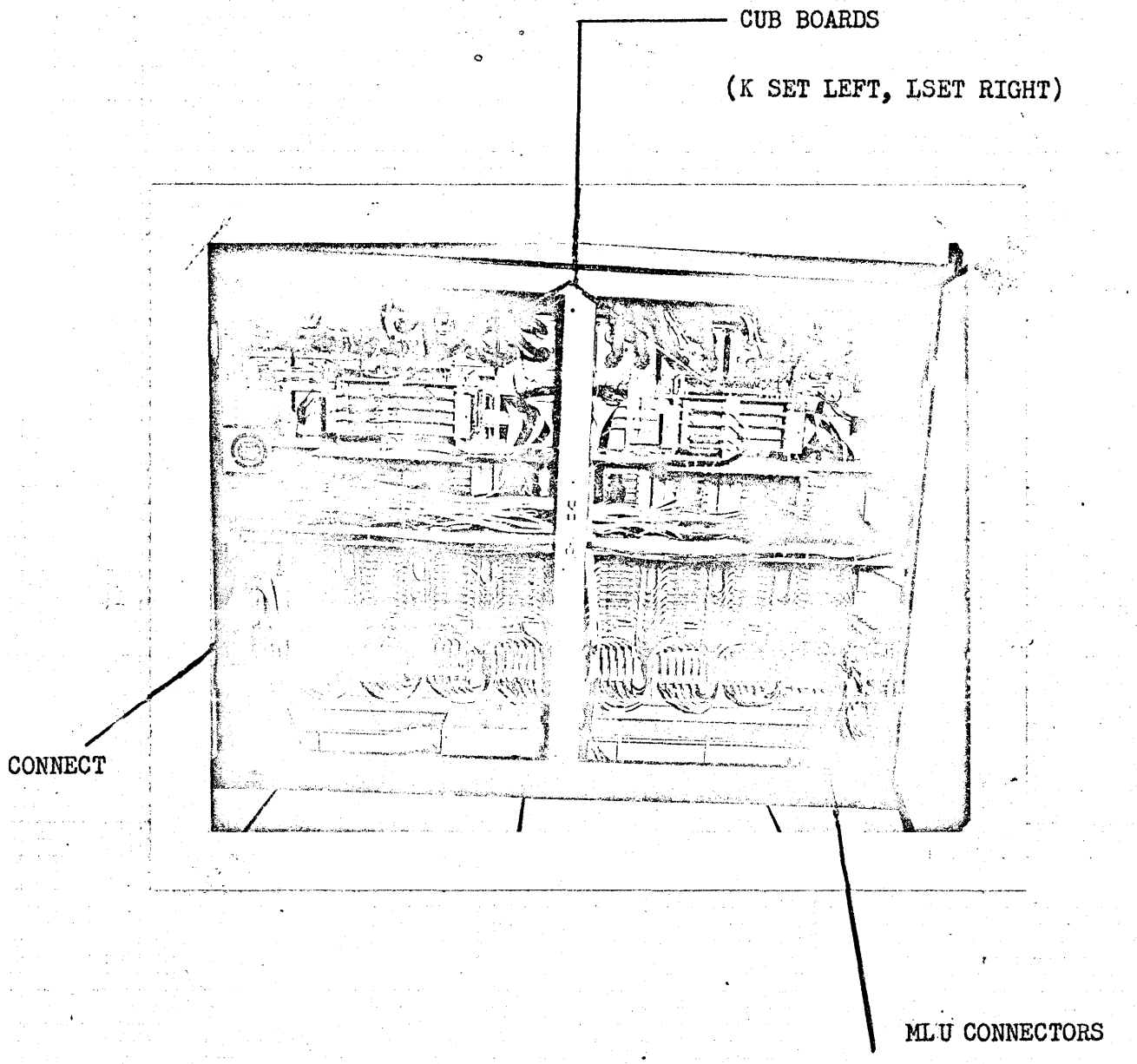

FIGURE 5(b) MLU INTERCONNECTIONS WITHIN A PUC.

six DISCONNECT connectors (M7-M12) are used for the IOSS data (128 data bits and two strobes) as explained in the section dealing with the IOSS data, the DISCONNECT may be viewed as a transparent device.

The DISCONNECT serves no other purpose but to provide flexibility in handling the belted cables connected to the CUB or input/output switch backplane. To be more specific, when a belted cable connected to the CUB backplane has to be replaced, if the Disconnect were not used and the last PU in the PUC was connected directly to the CUB board, then in order to replace the cable at the CUB backplane, all the cables for a particular connector from all PU's within the cabinet would have to be removed. By using the Disconnect, the cable is unplugged at the Disconnect and the CUB backplane can be very easily repaired on the bench or a change of the cable may be made by a special machine located away from the quadrant. From the Disconnect the six belted cables are split into two pairs of three cables each; cables from M1, M5, M6 connectors of the Disconnect are brought into the right side of four CUB boards (see Tables 2 and 3) labeled L, while the belted cables from M2, M3, and M4 connectors of the Disconnect are brought into the left set of four CUB boards (see Tables 2 and 4) labeled K. Figure 5c shows a sketch of these interconnections.

The data (32 data bits and one strobe) at each set of four CUB boards is further subdivided via the backplane CUB distribution board into four groups each of which contains eight data bits and a strobe and feeds one CUB board as Tables 3 and 4 show. The two strobes from the MLU are directed to one set of CUB boards each (L and K) and there each is split into four strobes one for each CUB board. Tables 3 and 4 show only the data in and out of the CUB boards, the reader will find on Drawing No. I1300-0100, Sheet 2 of 2, that the strobe from MLU is received at pin A58. There he will also be able to find other information which is not contained in this document.

3. Data Movement from CUB Boards to CU Backplane Connectors

In every PUC there are two sets of CUB's each of which consists of four CUB boards. The CUB boards are identical to one another and therefore interchangeable to all eight positions within the two sets is mainly partitioned into two sections, the section which takes care of the data whose origin is one of the eight PEM's or PE's (transfer of data via the MLU) of each PUC and whose destination is the CU and the other section takes care of the routing data. Because the routing function and its implementation will be described in Section IV of this document, we will restrict, at the present time, ourselves

TABLE 3. INPUT and OUTPUT data from the L set of CUB boards within a PUC

INPUT DATA INTO L SET			DATA OUT OF L SET		
BIT NO.	CUB BOARD NO.	CUB BOARD PIN NO.	BIT NO.	CUB BOARD NO.	CUB BOARD PIN NO.
0	X1	A - 45	0	X1	C - 3,5
1		A - 39	1		C - 9,11
2		A - 33	2		C - 15,17
3		A - 27	3		C - 21,23
4		A - 21	4		C - 27,29
5		A - 15	5		C - 33,35
6		A - 9	6		C - 39,41
7	X1	A - 3	7	X1	C - 45,47
8	X2	A - 45	8	X2	C - 3,5
9		A - 39	9		C - 9,11
10		A - 33	10		C - 15,17
11		A - 27	11		C - 21,23
12		A - 21	12		C - 27,29
13		A - 15	13		C - 33,35
14		A - 9	14		C - 39,41
15	X2	A - 3	15	X2	C - 45,47
16	X3	A - 45	16	X3	C - 3,5
17		A - 39	17		C - 9,11
18		A - 33	18		C - 15,17
19		A - 27	19		C - 21,23
20		A - 21	20		C - 27,29
21		A - 15	21		C - 33,35
22		A - 9	22		C - 39,41
23	X3	A - 3	23	X3	C - 45,47
24	X4	A - 45	24	X4	C - 3,5
25		A - 45	25		C - 9,11
26		A - 45	26		C - 15,17
27		A - 45	27		C - 21,23
28		A - 45	28		C - 27,29
29		A - 45	29		C - 33,35
30		A - 45	30		C - 39,41
31	X4	A - 45	31	X4	C - 45,47

NOTES: 1. The L set of four CUB boards is located on the right side of each PCU (CU on right side of Quadrant)

2. For each Data bit out of CUB we provide the true and complement form and therefore two pins for each bit.

TABLE 4. INPUT and OUTPUT Data from the K set of CUB boards within each PUC

DATA INTO THE "K" SET			DATA OUT OF THE "K" SET		
BIT NO.	CUB BOARD NO.	CUB BOARD PIN NO.	BIT NO.	CUB BOARD NO.	CUB BOARD PIN NO.
32	X1	A - 45	32	X1	C - 3,5
33		A - 39	33		C - 9,11
34		A - 33	34		C - 15,17
35		A - 27	35		C - 21,23
36		A - 21	36		C - 27,29
37		A - 15	37		C - 33,35
38		A - 9	38		C - 39,41
39	X1	A - 3	39	X1	C - 45,47
40	X2	A - 45	40	X2	C - 3,5
41		A - 39	41		C - 9,11
42		A - 33	42		C - 15,17
43		A - 27	43		C - 21,23
44		A - 21	44		C - 27,29
45		A - 15	45		C - 33,35
46		A - 9	46		C - 39,41
47	X2	A - 3	47	X2	C - 45,47
48	X3	A - 45	48	X3	C - 3,5
49		A - 39	49		C - 9,11
50		A - 33	50		C - 15,17
51		A - 27	51		C - 21,23
52		A - 21	52		C - 27,29
53		A - 15	53		C - 33,35
54		A - 9	54		C - 39,41
55	X3	A - 3	55	X3	C - 45,47
56	X4	A - 45	56	X4	C - 3,5
57		A - 39	57		C - 9,11
58		A - 33	58		C - 15,17
59		A - 27	59		C - 21,23
60		A - 21	60		C - 27,29
61		A - 15	61		C - 33,35
62		A - 9	62		C - 39,41
63	X4	A - 3	63	X4	C - 45,47

NOTES: 1. The K set of four CUB boards is located on the left side of each PUC (CU on right side of Quadrant).

2. The two pins for each data bit out of the CUB board are used for the true and complement form of each bit.

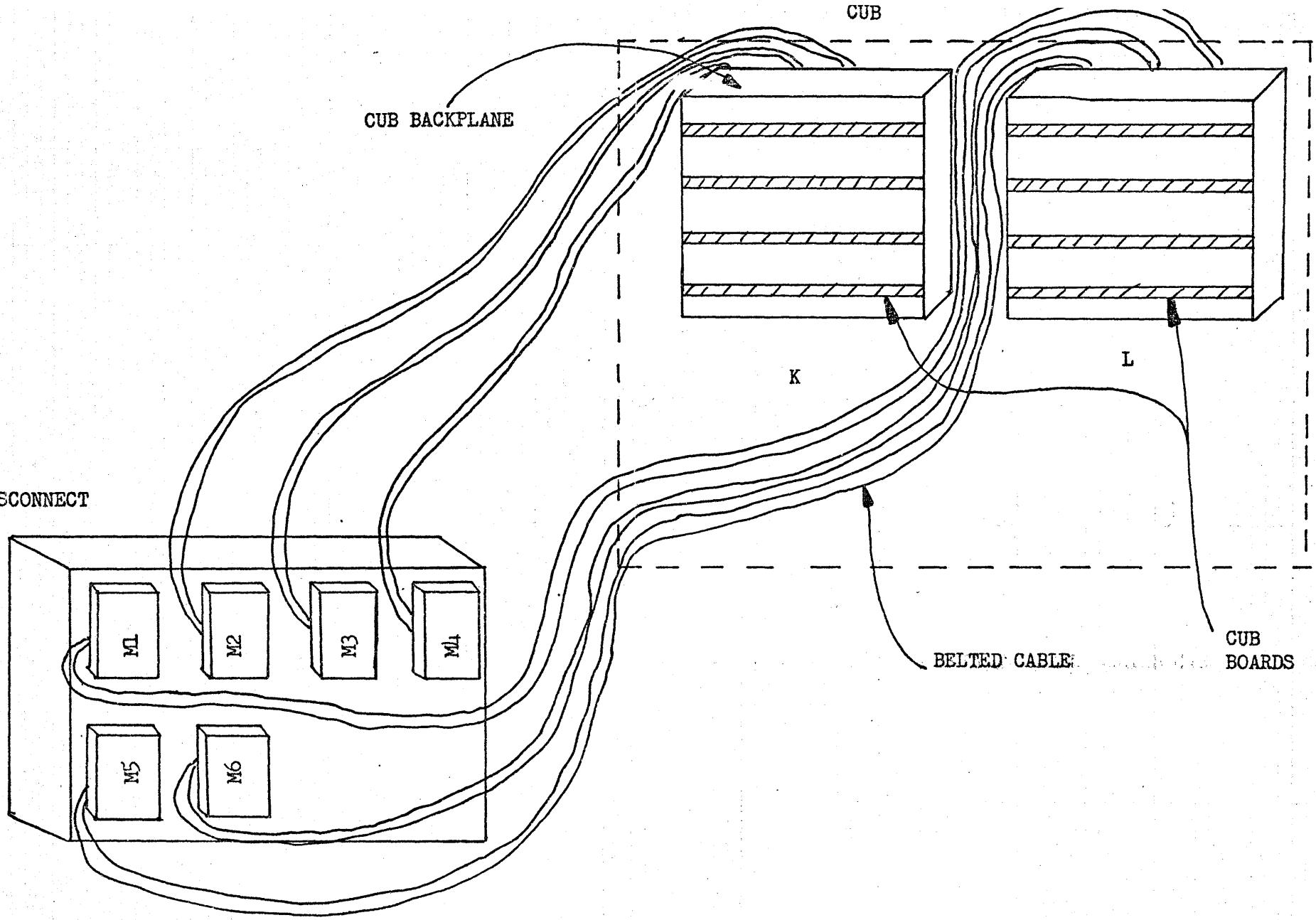

FIGURE 5(c). SKETCH OF DATA MOVEMENT FROM DISCONNECT TO CUB

to the description of the section of the CUB board which receives the data from the Disconnect and drives it to CU (ATP02 boards).

It is explained in the description of the IO/CUB card in the MLU Manual (IAC Doc. No. PO-I1200-0000-A) that signals leaving the IO/CUB card are at CTμL level (+2.5V corresponds to logical 1 and -500 mV corresponds to logical 0 when following positive logic notation).

Each CUB board receives eight data bits and a strobe (see Tables 3 and 4). The data and the strobe are down converted by the down converters; the CTμL +2.5V level is converted to +400 mV and -500 mV is converted to -400 mV. This down conversion is necessary because the data from CTμL levels have to be brought into ECL level (±400 mV) since this is the logic used by the CU.

The down converted data is strobed into the latches by the MLU strobe after the clear CUB (CLCUB) from the CU has cleared the latches and thus has prepared them to accept the data. The CLCUB signal (true and complement form) precedes the MLU strobe and MLU data by approximately 100 ns.

Approximately one CU clock after the data has been strobed into the latches, the MUPEQ signal allows the data to be driven into the CU as CU BIT(xx) and $\overline{\text{CU BIT(xx)}}$. The true and complement form of each data bit is necessary because ECL signals are less immune to noise and therefore safe data transmission via relatively long lines requires at the other end of the line the use of differential receivers. Because the CU uses negative logic notation, the reader should be aware that a low signal into the D input of the latch or out of the Q part of the latch represents a logical 1.

For more details refer to Drawing No. I1300-0100-A. Since at the present time there is no timing analysis available due to the fact that the CUB boards have been redesigned, the reader should refer to the timing diagram available at the Documentation Department which handles all the original documents concerning the ILLIAC IV hardware.

Each of the CUB paddle boards is identified by a ten character symbol. The first two numbers represent the number of the PUC, the letter K represents the left set of the CUB boards and L represents the right set of the CUB boards, the last two characters (X1 or X2 or X3 or X4) represent the position of the four boards within the set (K or L) and C represents the side of the CUB board providing the data to CU. For example, 04-L-X2C represents the paddle

board connected to the second CUB board of the right set (L) located in the last PUC (PUC4). Each CUB board provides eight data bits in true and complement form as Tables 3 and 4 show. The data is picked up from the CUB board pins by a female paddle board which is connected to a 25-conductor belted cable and whose other end connects to the backplane of the ATPO2 boards of the CU. The reader should be aware that each paddle board on every CUB board has been labeled so that using this notation and Tables 3 and 4 he will be able to identify every data bit; since each paddle board pin has been clearly numbered.

Figures 6(a) and 6(b) show the "L" and "K" sets of the CUB boards within each PUC and the CU backplane which is partitioned into nine sections numbered from 1 to 9. Before we explain how "K" and "L" sets are brought into the CU paddle boards, we refer your attention to Figure 7. This figure shows only the section of the CU backplane which is related to ATPO2 type boards. Every connector in the backplane is identified by a four character symbol. The first numeric character (number 9) indicates the section of the CU, the following alphabetic character represents one out of the twenty-one columns in the section. The second pair of alphanumeric characters represents one of the five rows in the section. For example, 9EJ5 represents the position of the fifth connector from left to right on the bottom row of the 9th section of the CU backplane.

As has been explained previously, the data which is brought into the "L" and "K" sets of CUB boards within each PUC is the data which comes from one of the eight PU's within the PUC (the eight MLU's within each PUC are daisy chained). Therefore, out of each PUC, that is, out of the CUB boards of the PUC, only 64 data bits are provided to the CU at a time. Because, however, there are instances in which the CU may receive data (64 bits) from each of the eight PUC's (see Instruction BIN(X) in the Systems Characteristics and Programming Manual: NASA CR-2159) all at one time, Figures 6a and 6b are provided to show how the "L" and "K" sets of CUB boards of each PUC are connected to the CU backplane. Figures 6a and 6b show the belted cables from each "L" and "K" sets of CUB boards to the CU backplane. The other end of each of these cables terminates at a paddle board permanently attached to the cable and which is connected to the CU backplane connectors whose positions are specified in Figures 6a and 6b. These belted cables are composed of 25 conductors each and are used to transfer the data from the CUB's in its true and complement form. Because the data is brought into the CU backplane connectors via the paddle boards, the four

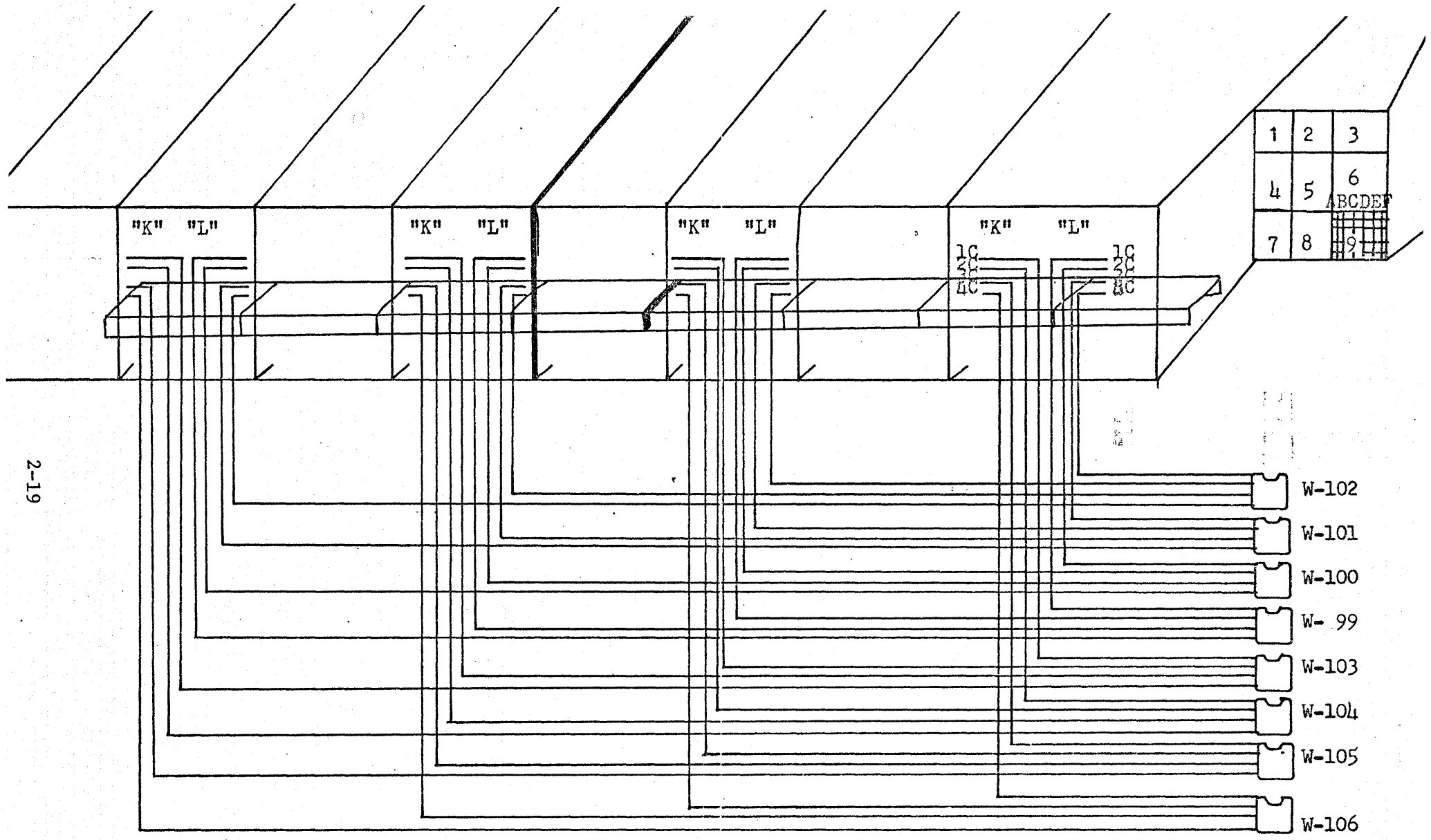

FIGURE 6(a). DATA MOVEMENT FROM CUB TO CU (ATP02 BOARDS) FOR PUC (0-3)

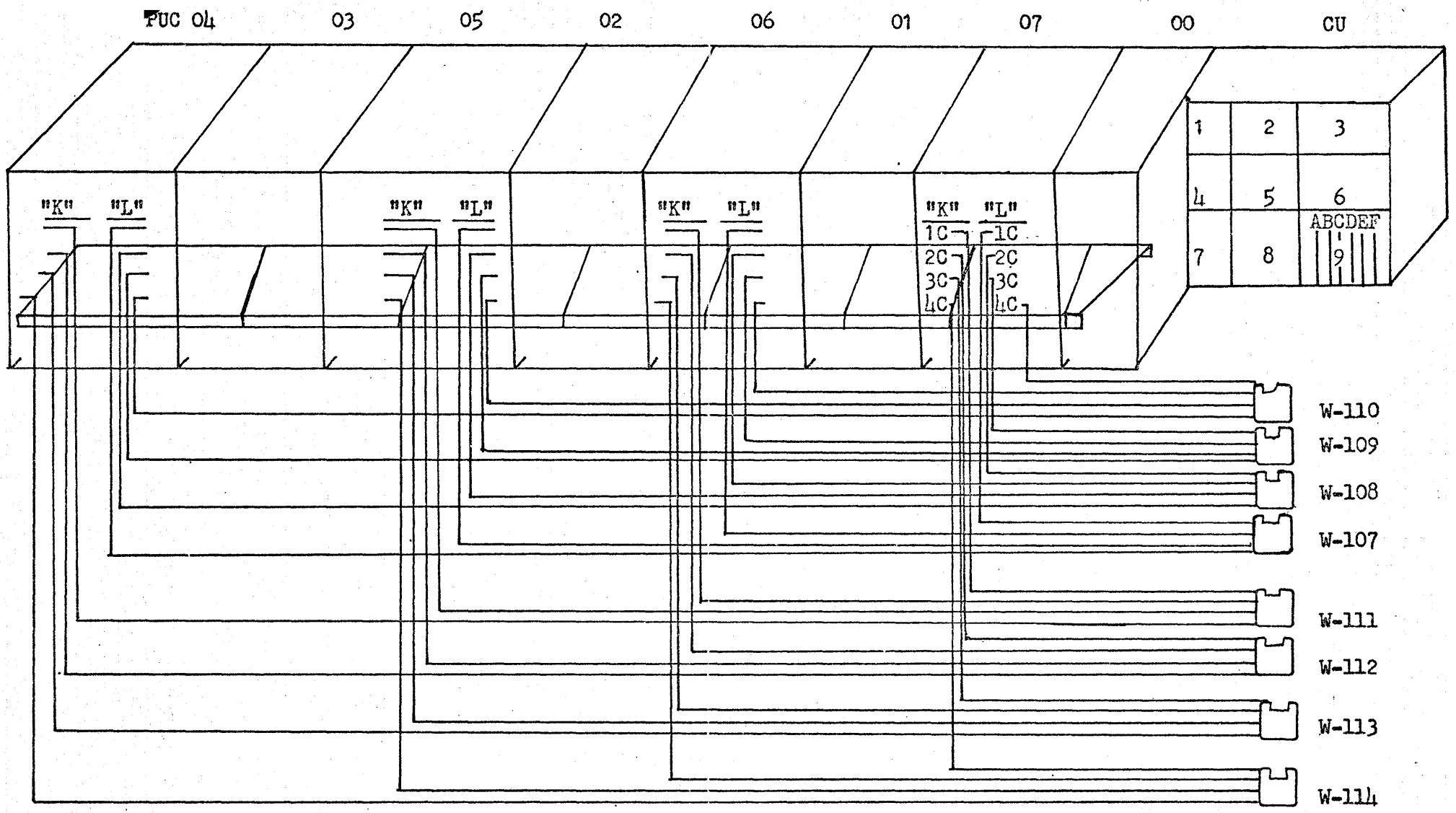

FIGURE 6(B). DATA MOVEMENT FROM CUB TO CU (A T P O 2 BOARDS) FOR PUC (4-7)

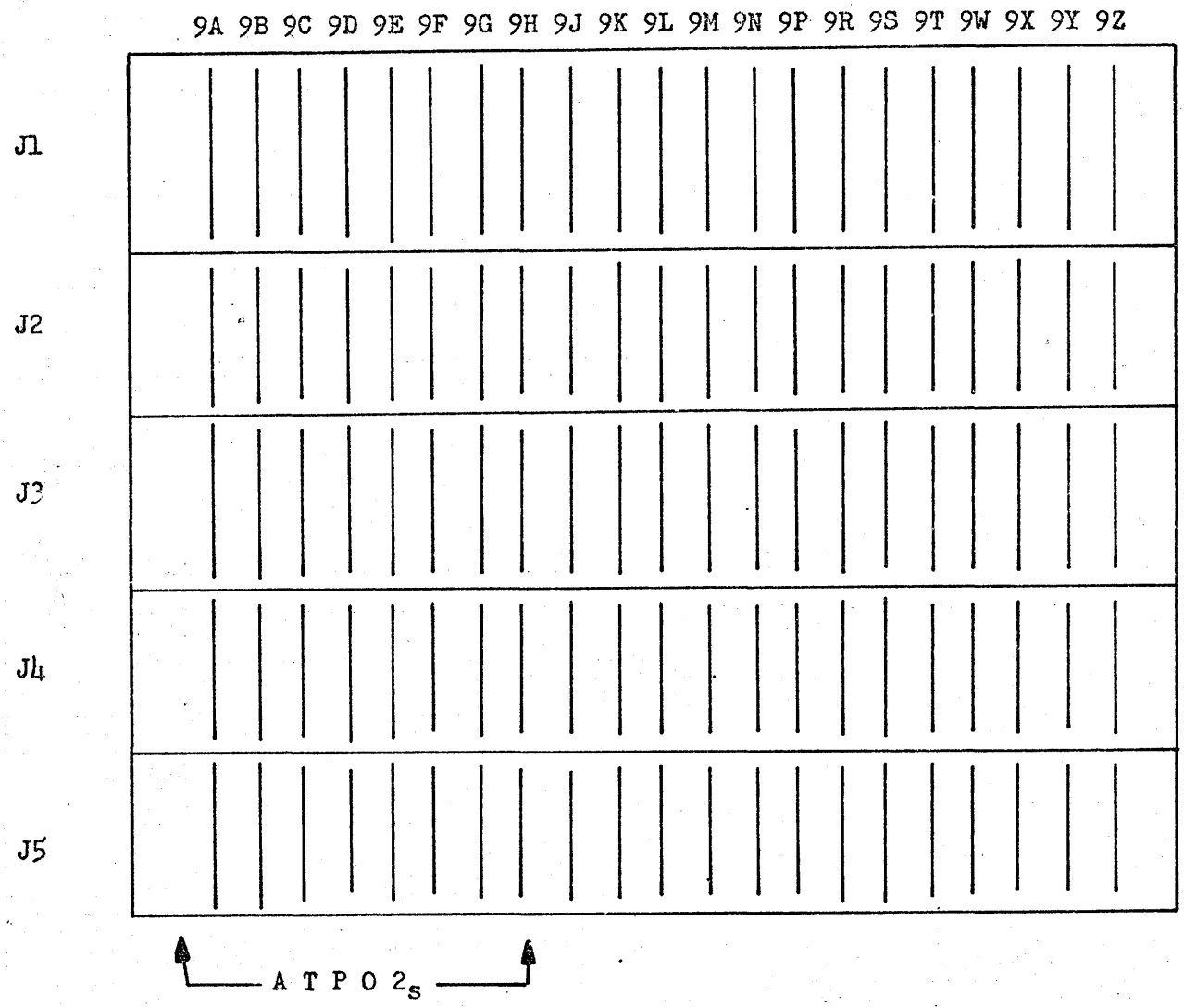

FIGURE 7. 9th SECTION OF CU BACKPLANE

character symbols on the right side of Figures 6a and 6b specify the paddle boards which are inserted into the CU backplane connectors. These paddle boards are well labeled and care should be exercised to insure that each paddle board is inserted into the position which is specified on the paddle board. Figure 8 shows the label and position of each CU backplane paddle board related to CU data from the CUB's. The symbol W-xxx specifies the CU paddle board while the four alphanumeric character symbol following W-xxx specifies the CU backplane connector into which the paddle board W-xxx is inserted.

Each paddle board, as is shown in Figures 6a and 6b , receives four belted cables from four different PUC's (L or K sets of CUB boards) in such a fashion that the same CUB board number (X1, X2, etc.) from the same set (L or K) of PUC (0-3) or PUC (4-7) connects to the same paddle board of the CU backplane.

Table 5 shows the interrelationship of each CUB paddle board in the Array with its corresponding CU backplane connector and data bit numbers accommadated by them.

4. Data Movement from the CU Backplane Connectors to ATPO2 Boards

Figure 9 shows how a paddle board with four belted cables attached to it is connected to a CU backplane connector. This figure furthermore shows the way in which the pins on an ATPO2 board are configured, so that data brought into a CU connector from four CUB boards located in four different PUC's will be distributed into the ATPO2 board via pins A, B, C, D. Because the intent of this section of this document is to describe the data flow from the MLU of each PU into the CU (ATPO2 board), we will not provide a detailed description of the ATPO2 board, but rather a brief description of the interface of the ATPO2 board with the CU backplane connectors.

In the nineth section of the CU backplane, there are eight ATPO2 boards, each of which occupies one column and five rows. This means that the CU backplane connectors J3 and J5 of a particular column (i.e., 9A, 9B, etc.) provide contact with any of the ATPO2 boards which corresponds to that particular column. It has been shown, however, that each connector (Figure 8) receives, via a paddle board, data from four CUB boards (same position number) each of which belongs to a different PUC. A very careful inspection of Table 5 reveals

	9 A	9 B	9 C	9 D	9 E	9 F	9 G	9 H
J 1								
J 2								
J 3	W-106 9A-J3	W-105 9B-J3	W-104 9C-J3	W-103 9D-J3	W-102 9E-J3	W-101 9F-J3	W-100 9G-J3	W-99 9H-J3
J 4								
J 5	W-114 9A-J5	W-113 9B-J5	W-112 9C-J5	W-111 9D-J5	W-110 9E-J5	W-109 9F-J5	W-108 9G-J5	W-107 9H-J5

FIGURE 8 LOCATION AND LABEL OF THE CU BACKPLANE PADDLE BOARDS RELATED TO CUB/CU DATA.

CUB Paddle Board No.	CU Backplane		Bit Number	Remarks
	Paddle Board Number	Connector Number		
00-LX1C	W-99	9H-J3	00	
01-LX1C				
02-LX1C				
03-LX1C	W-99	9H-J3	07	
00-LX2C	W-100	9G-J3	08	
01-LX2C				
02-LX2C				
03-LX2C	W-100	9G-J3	15	
00-LX3C	W101	9F-J3	16	
01-LX3C				
02-LX3C				
03-LX3C	W-102	9F-J3	23	
00-LX4C	W-102	9E-J3	24	
01-LX4C				
02-LX4C				
03-LX4C	W-102	9E-J3	31	

NOTE: This table contains information for data (00-31) of PUC (0-3)

Table 5. CUB to CU Backplane Connectors Data

CUB Paddle Board No.	CU Backplane		Bit Number	Remarks
	Paddle Board Number	Connector Number		
04-LX1C	W-107	9H-J5	00	
05-LX1C	↑	↑	↑	
06-LX1C	↓	↓	↓	
07-LX1C	W-107	9H-J5	07	
04-LX2C	W-108	9G-J5	08	
05-LX2C	↑	↑	↑	
06-LX2C	↓	↓	↓	
07-LX2C	W-108	9G-J5	15	
04-LX3C	W-109	9F-J5	16	
05-LX3C	↑	↑	↑	
06-LC3C	↓	↓	↓	
07-LX3C	W-109	9F-J5	23	
04-LX4C	W-110	9E-J5	24	
05-LX4C	↑	↑	↑	
06-LX4C	↓	↓	↓	
07-LX4C	W-110	9E-J5	31	

NOTE: This table contains information for data (00-31) of PUC (4-7)

Table 5 - continued. CUB to CU Backplane Connectors Data

CUB Paddle Board No.	CU Backplane		Bit Number	Remarks
	Paddle Board Number	Connector Number		
00-KX1C	W-103	9D-J3	32	
01-KX1C	↑	↑	↑	
02-KX1C	↓	↓	↓	
03-KX1C	W-103	9D-J3	39	
00-KX2C	W-104	9C-J3	40	
01-KX2C	↑	↑	↑	
02-KX2C	↓	↓	↓	
03-KX2C	W-104	9C-J3	47	
00-KX3C	W-105	9B-J3	48	
01-KX3C	↑	↑	↑	
02-KX3C	↓	↓	↓	
03-KX3C	W-105	9B-J3	55	
00-KX4C	W-106	9A-J3	56	
01-KX4C	↑	↑	↑	
02-KX4C	↓	↓	↓	
03-KX4C	W-106	9A-J3	63	

NOTE: This table contains information for data (32-63) of PUC (0-3)

Table 5 - continued. CUB to CU Backplane Connectors Date

CUB Paddle Board No.	CU Backplane Paddle Board Number	CU Backplane Connector Number	Bit Number	Remarks
04-KX1C	W-111	9D-J5	32	
05-KX1C	↑	↑	↑	
06-KX1C	↓	↓	↓	
07-KX1C	W-111	9D-J5	39	
04-KX2C	W-112	9C-J5	40	
05-KX2C	↑	↑	↑	
06-KX2C	↓	↓	↓	
07-KX2C	W-112	9C-J5	47	
04-KX3C	W-113	9B-J5	48	
05-KX3C	↑	↑	↑	
06-KX3C	↓	↓	↓	
07-KX3C	W-113	9B-J5	55	
04-KX4C	W-114	9A-J5	56	
05-KX4C	↑	↑	↑	
06-KX4C	↓	↓	↓	
07-KX4C	W-114	9A-J5	63	

NOTE: This table contains information for data (32-63) of PUC (4-7)

Table 5 - continued. CUB to CU Backplane Connectors Date

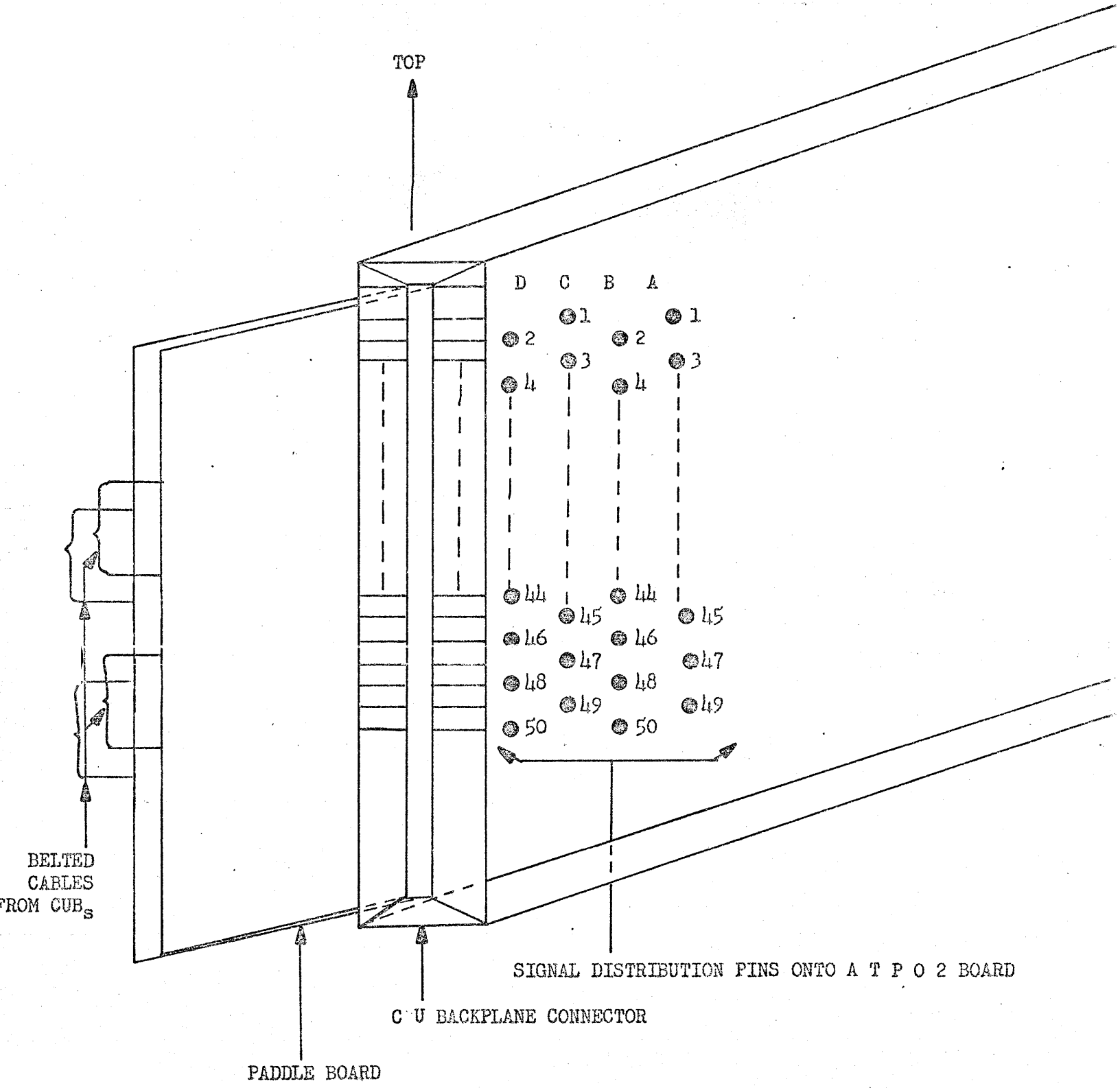

FIGURE 9 A T P O 2 BOARD CONNECTOR PIN CONFIGURATION.

that connectors J3 and J5 of any particular column take care of eight data bits (true and complement form) coming from eight different PUC's. For example, connectors at 9H-J3 and 9H-J5 accomodate bits 00 through 07 from PUC (0-7). Thus, the eight ATP02 boards (Table 6) take care of eight data bits each. The data is received by differential receivers whose outputs are brought to an OR gate via NAND gates enabled and disabled manually via eight override switches on the front panel of CU, or dynamically, via controls from the MSU. In this way, the eight ATP02 boards handle a full word of 64 bits, which may be either a single word from one of the 64 PU's (MLU's) or the result of an OR function of eight words each of which corresponds to one of the eight PUC's (BIN(X) and ILA requests select eight PUC's and one MLU within each PUC).

Table 7 provides information about the interface of the CUB paddle boards and CU backplane connectors via the belted cables of 25 conductors each. In this table, the data is defined by a signal name similar to that appearing on the AL 02 board drawings in order to make the data path easily traceable from the CUB to the ATP02 board.

CU Board Number	Location at CU	Data Bits Received	Remarks
ATPO2 A	9H	00-07	The suffix on each
ATPO2 B	9G	08-15	ATPO2 board is indepen-
ATPO2 C	9F	16-23	dent of the location
ATPO2 D	9E	24-31	of the board
ATPO2 E	9D	32-39	
ATPO2 F	9C	40-47	
ATPO2 G	9B	48-55	
ATPO2 H	9A	56-63	

Table 6. ATPO2 Board Partitioning

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU.

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
PO-00--D1	00	00-LX1C	3	J3-9H	D2
PO-00-RD1			5		C3
PO-01--D1			9		C5
PO-01-RD1			11		D6
PO-02--D1			15		D8
PO-02-RD1			17		C9
PO-03--D1			21		C11
PO-03-RD1			23		D12
PO-04--D1			27		D14
PO-04-RD1			29		C15
PO-05--D1			33		C17
PO-05-RD1			35		D18
PO-06--D1			39		D20
PO-06-RD1			41		C21
PO-07--D1	↓	↓	45	↓	C23
PO-07-RD1	00	00-LX1C	47	J3-9H	D24

P1-00--D1	01	01-LX1C	3	J3-9H	B2
P1-00-RD1			5		A3
P1-01--D1			9		A5
P1-01-RD1			11		B6
P1-02--D1			15		B8
P1-02-RD1			17		A9
P1-03--D1			21		A11
P1-03-RD1			23		B12
P1-04--D1			27		B14
P1-04-RD1			29		A15
P1-05--D1			33		A17
P1-05-RD1			35		B18
P1-06--D1			39		B20
P1-06-RD1			41		A21
P1-07--D1	↓	↓	45	↓	A23
P1-07-RD1	01	01-LX1C	47	J3-9H	B24

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P2-00--D1	02	02-LX1C	3	J3-9H	D26
P2-00-RD1			5		C27
P2-01--D1			9		C29
P2-01-RD1			11		D30
P2-02--D1			15		D32
P2-02-RD1			17		C33
P2-03--D1			21		C35
P2-03-RD1			23		D36
P2-04--D1			27		D38
P2-04-RD1			29		C39
P2-05--D1			33		C41
P2-05-RD1			35		D42
P2-06--D1			39		D44
P2-06-RD1			41		C45
P2-07--D1			45		C47
P2-07-RD1	02	02-LX1C	47	J3-9H	D48

P3-00--D1	03	03-LX1C	3	J3-9H	B26
P3-00-RD1			5		A27
P3-01--D1			9		A29
P3-01-RD1			11		B30
P3-02--D1			15		B32
P3-02-RD1			17		A33
P3-03--D1			21		A35
P3-03-RD1			23		B36
P3-04--D1			27		B38
P3-04-RD1			29		A39
P3-05--D1			33		A41
P3-05-RD1			35		B42
P3-06--D1			39		B44
P3-06-RD1			41		A45
P3-07--D1			45		A47
P3-07-RD1	03	03-LX1C	47	J3-9H	B48

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P4-00--D1	04	04-LX1C	3	J5-9H	B26
P4-00-RD1			5		A27
P4-01--D1			9		A29
P4-01-RD1			11		B30
P4-02--D1			15		B32
P4-02-RD1			17		A33
P4-03--D1			21		A35
P4-03-RD1			23		B36
P4-04--D1			27		B38
P4-04-RD1			29		A39
P4-05--D1			33		A41
P4-05-RD1			35		B42
P4-06--D1			39		B44
P4-06-RD1			41		A45
P4-07--D1			45		A47
P4-07-RD1	04	04-LX1C	47	J5-9H	B48
P5-00--D1	05	05-LX1C	3	J5-9H	D26
P5-00-RD1			5		C27
P5-01--D1			9		C29
P5-01-RD1			11		D30
P5-02--D1			15		D32
P5-02-RD1			17		C33
P5-03--D1			21		C35
P5-03-RD1			23		D36
P5-04--D1			27		D38
P5-04-RD1			29		C39
P5-05--D1			33		C41
P5-05-RD1			35		D42
P5-06--D1			39		D44
P5-06-RD1			41		C45
P5-07--D1			45		C47
P5-07-RD1	05	05-LX1C	47	J5-9H	D48

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P6-00--D1	06	06-LX1C	3	J5-9H	B2
P6-00-RD1			5		A3
P6-01--D1			9		A5
P6-01-RD1			11		B6
P6-02--D1			15		B8
P6-02-RD1			17		A9
P6-03--D1			21		A11
P6-03-RD1			23		B12
P6-04--D1			27		B14
P6-04-RD1			29		A15
P6-05--D1			33		A17
P6-05-RD1			35		B18
P6-06--D1			39		B20
P6-06-RD1			41		A21
P6-07--D1			45		A23
P6-07-RD1	06	06-LX1C	47	J5-9H	B24

P7-00--D1	07	07-LX1C	3	J5-9H	D2
P7-00-RD1			5		C3
P7-01--D1			9		C5
P7-01-RD1			11		D6
P7-02--D1			15		D8
P7-02-RD1			17		C9
P7-03--D1			21		C11
P7-03-RD1			23		D12
P7-04--D1			27		D14
P7-04-RD1			29		C15
P7-05--D1			33		C17
P7-05-RD1			35		D18
P7-06--D1			39		D20
P7-06-RD1			41		C21
P7-07--D1			45		C23
P7-07-RD1	07	07-LX1C	47	J5-9H	D24

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
PO-08--D1	00	00-LX2C	3	J3-9G	D2
PO-08-RD1			5		C3
PO-09--D1			9		C5
PO-09-RD1			11		D6
PO-10--D1			15		D8
PO-10-RD1			17		C9
PO-11--D1			21		C11
PO-11-RD1			23		D12
PO-12--D1			27		D14
PO-12-RD1			29		C15
PO-13--D1			33		C17
PO-13-RD1			35		D18
PO-14--D1			39		D20
PO-14-RD1			41		C21
PO-15--D1			45		C23
PO-15-RD1	00	00-LX2C	47	J3-9G	D24
P1-08--D1	01	01-LX2C	3	J3-9G	B2
P1-08-RD1			5		A3
P1-09--D1			9		A5
P1-09-RD1			11		B6
P1-10--D1			15		B8
P1-10-RD1			17		A9
P1-11--D1			21		A11
P1-11-RD1			23		B12
P1-12--D1			27		B14
P1-12-RD1			29		A15
P1-13--D1			33		A17
P1-13-RD1			35		B18
P1-14--D1			39		B20
P1-14-RD1			41		A21
P1-15--D1			45		A23
P1-15-RD1	01	01-LX2C	47	J3-9G	B24

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P2-08--D1	02	02-LX2C	3	J3-9G	D26
P2-08-RD1			5		C27
P2-09--D1			9		C29
P2-09-RD1			11		D30
P2-10--D1			15		D32
P2-10-RD1			17		C33
P2-11--D1			21		C35
P2-11-RD1			23		D36
P2-12--D1			27		D38
P2-12-RD1			29		C39
P2-13--D1			33		C41
P2-13-RD1			35		D42
P2-14--D1			39		D44
P2-14-RD1			41		C45
P2-15--D1			45		C47
P2-15-RD1	02	02-LX2C	47	J3-9G	D48

P3-08--D1	03	03-LX2C	3	J3-9G	B26
P3-08-RD1			5		A27
P3-09--D1			9		A29
P3-09-RD1			11		B30
P3-10--D1			15		B32
P3-10-RD1			17		A33
P3-11--D1			21		A35
P3-11-RD1			23		B36
P3-12--D1			27		B38
P3-12-RD1			29		A39
P3-13--D1			33		A41
P3-13-RD1			35		B42
P3-14--D1			39		B44
P3-14-RD1			41		A45
P3-15--D1			45		A47
P3-15-RD1	03	03-LX2C	47	J3-0G	B48

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P4-08--D1	04	04-LX2C	3	J5-9G	B26
P4-08-RD1			5		A27
P4-09--D1			9		A29
P4-09-RD1			11		B30
P4-10--D1			15		B32
P4-10-RD1			17		A33
P4-11--D1			21		A35
P4-11-RD1			23		B36
P4-12--D1			27		B38
P4-12-RD1			29		A39
P4-13--D1			33		A41
P4-13-RD1			35		B42
P4-14--D1			39		B44
P4-14-RD1			41		A45
P4-15--D1			45		A47
P4-15-RD1	04	04-LX2C	47	J5-9G	B48
P5-08--D1	05	05-LX2C	3	J5-9G	D26
P5-08-RD1			5		C27
P5-09--D1			9		C29
P5-09-RD1			11		D30
P5-10--D1			15		D32
P5-10-RD1			17		C33
P5-11--D1			21		C35
P5-11-RD1			23		D36
P5-12--D1			27		D38
P5-12-RD1			29		C39
P5-13--D1			33		C41
P5-13-RD1			35		D42
P5-14--D1			39		D44
P5-14-RD1			41		C45
P5-15--D1			45		C47
P5-15-RD1	05	05-LX2C	47	J5-9G	D48

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P6-08--D1	06	06-LX2C	3	J5-9G	B2
P6-08-RD1			5		A3
P6-09--D1			9		A5
P6-09-RD1			11		B6
P6-10--D1			15		B8
P6-10-RD1			17		A9
P6-11--D1			21		A11
P6-11-RD1			23		B12
P6-12--D1			27		B14
P6-12-RD1			29		A15
P6-13--D1			33		A17
P6-13-RD1			35		B18
P6-14--D1			39		B20
P6-14-RD1			41		A21
P6-15--D1			45		A23
P6-15-RD1	06	06-LX2C	47	J5-9G	B24
P7-08--D1	07	07-LX2C	3	J5-9G	D2
P7-08-RD1			5		C3
P7-09--D1			9		C5
P7-09-RD1			11		D6
P7-10--D1			15		D8
P7-10-RD1			17		C9
P7-11--D1			21		C11
P7-11-RD1			23		D12
P7-12--D1			27		D14
P7-12-RD1			29		C15
P7-13--D1			33		C17
P7-13-RD1			35		D18
P7-14--D1			39		D20
P7-14-RD1			41		C21
P7-15--D1			45		C23
P7-15-RD1	07	07-LX2C	47	J5-9G	D24

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
PO-16--D1	00	00-LX3C	3	J3-9F	D2
PO-16-RD1			5		C3
PO-17--D1			9		C5
PO-17-RD1			11		D6
PO-18--D1			15		D8
PO-18-RD1			17		C9
PO-19--D1			21		C11
PO-19-RD1			23		D12
PO-20--D1			27		D14
PO-20-RD1			29		C15
PO-21--D1			33		C17
PO-21-RD1			35		D18
PO-22--D1			39		D20
PO-22-RD1			41		C21
PO-23--D1			45		C23
PO-23-RD1	00	00-LX3C	47	J3-9F	D24
P1-16--D1	01	01-LX3C	3	J3-9F	B2
P1-16-RD1			5		A3
P1-17--D1			9		A5
P1-17-RD1			11		B6
P1-18--D1			15		B8
P1-18-RD1			17		A9
P1-19--D1			21		A11
P1-19-RD1			23		B12
P1-20--D1			27		B14
P1-20-RD1			29		A15
P1-21--D1			33		A17
P1-21-RD1			35		B18
P1-22--D1			39		B20
P1-22-RD1			41		A21
P1-23--D1			45		A23
P1-23-RD1	01	01-LX3C	47	J3-9F	B24

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P2-16--D1	02	02-LX3C	3	J3-9F	D26
P2-16-RD1			5		C27
P2-17--D1			9		C29
P2-17-RD1			11		D30
P2-18--D1			15		D32
P2-18-RD1			17		C33
P2-19--D1			21		C35
P2-19-RD1			23		D36
P2-20--D1			27		D38
P2-20-RD1			29		C39
P2-21--D1			33		C41
P2-21-RD1			35		D42
P2-22--D1			39		D44
P2-22-RD1			41		C45
P2-23--D1			45		C47
P2-23-RD1	02	02-LX3C	47	J3-9F	D48

P3-16--D1	03	03-LX3C	3	J3-9F	B26
P3-16-RD1			5		A27
P3-17--D1			9		A29
P3-17-RD1			11		B30
P3-18--D1			15		B32
P3-18-RD1			17		A33
P3-19--D1			21		A35
P3-19-RD1			23		B36
P3-20--D1			27		B38
P3-20-RD1			29		A39
P3-21--D1			33		A41
P3-21-RD1			35		B42
P3-22--D1			39		B44
P3-22-RD1			41		A45
P3-23--D1			45		A47
P3-23-RD1	03	03-LX3C	47	J3-9F	B48

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P4-16--D1	04	04-LX3C	3	J5-9F	B26
P4-16-RD1			5		A27
P4-17--D1			9		A29
P4-17-RD1			11		B30
P4-18--D1			15		B32
P4-18-RD1			17		A33
P4-19--D1			21		A35
P4-19-RD1			23		B36
P4-20--D1			27		B38
P4-20-RD1			29		A39
P4-21--D1			33		A41
P4-21-RD1			35		B42
P4-22--D1			39		B44
P4-22-RD1			41		A45
P4-23--D1			45		A47
P4-23-RD1	04	04-LX3C	47	J5-9F	B48
P5-16--D1	05	05-LX3C	3	J5-9F	D26
P5-16-RD1			5		C27
P5-17--D1			9		C29
P5-17-RD1			11		D30
P5-18--D1			15		D32
P5-18-RD1			17		C33
P5-19--D1			21		C35
P5-19-RD1			23		D36
P5-20--D1			27		D38
P5-20-RD1			29		C39
P5-21--D1			33		C41
P5-21-RD1			35		D42
P5-22--D1			39		D44
P5-22-RD1			41		C45
P5-23--D1			45		C47
P5-23-RD1	05	05-LX3C	47	J5-9F	D48

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P6-16--D1	06	06-LX3C	3	J5-9F	B2
P6-16-RD1			5		A3
P6-17--D1			9		A5
P6-17-RD1			11		B6
P6-18--D1			15		B8
P6-18-RD1			17		A9
P6-19--D1			21		A11
P6-19-RD1			23		B12
P6-20--D1			27		B14
P6-20-RD1			29		A15
P6-21--D1			33		A17
P6-21-RD1			35		B18
P6-22--D1			39		B20
P6-22-RD1			41		A21
P6-23--D1			45		A23
P6-23-RD1	06	06-LX3C	47	J5-9F	B24

P7-16--D1	07	07-LX3C	3	J5-9F	D2
P7-16-RD1			5		C3
P7-17--D1			9		C5
P7-17-RD1			11		D6
P7-18--D1			15		D8
P7-18-RD1			17		C9
P7-19--D1			21		C11
P7-19-RD1			23		D12
P7-20--D1			27		D14
P7-20-RD1			29		C15
P7-21--D1			33		C17
P7-21-RD1			35		D18
P7-22--D1			39		D20
P7-22-RD1			41		C21
P7-23--D1			45		C23
P7-23-RD1	07	07-LX3C	47	J5-9F	D24

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P0-24--D1	00	00-LX4C	3	J3-9E	D2
P0-24-RD1			5		C3
P0-25--D1			9		C5
P0-25-RD1			11		D6
P0-26--D1			15		D8
P0-26-RD1			17		C9
P0-27--D1			21		C11
P0-27-RD1			23		D12
P0-28--D1			27		D14
P0-28-RD1			29		C15
P0-29--D1			33		C17
P0-29-RD1			35		D18
P0-30--D1			39		D20
P0-30-RD1			41		C21
P0-31--D1			45		C23
P0-31-RD1	00	00-LX4C	47	J3-9E	D24
P1-24--D1	01	01-LX4C	3	J3-9E	B2
P1-24-RD1			5		A3
P1-25--D1			9		A5
P1-25-RD1			11		B6
P1-26--D1			15		B8
P1-26-RD1			17		A9
P1-27--D1			21		A11
P1-27-RD1			23		B12
P1-28--D1			27		B14
P1-28-RD1			29		A15
P1-29--D1			33		A17
P1-29-RD1			35		B18
P1-30--D1			39		B20
P1-30-RD1			41		A21
P1-31--D1			45		A23
P1-31-RD1	01	01-LX4C	47	J3-9E	B24

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P2-24--D1	02	02-LX4C	3	J3-9E	D26
P2-24-RD1			5		C27
P2-25--D1			9		C29
P2-25-RD1			11		D30
P2-26--D1			15		D32
P2-26-RD1			17		C33
P2-27--D1			21		C35
P2-27-RD1			23		D36
P2-28--D1			27		D38
P2-28-RD1			29		C39
P2-29--D1			33		C41
P2-29-RD1			35		D42
P2-30--D1			39		D44
P2-30-RD1			41		C45
P2-31--D1			45		C47
P2-31-RD1	02	02-LX4C	47	J3-9E	D48

P3-24--D1	03	03-LX4C	3	J3-9E	B26
P3-24-RD1			5		A27
P3-25--D1			9		A29
P3-25-RD1			11		B30
P3-26--D1			15		B32
P3-26-RD1			17		A33
P3-27--D1			21		A35
P3-27-RD1			23		B36
P3-28--D1			27		B38
P3-28-RD1			29		A39
P3-29--D1			33		A41
P3-29-RD1			35		B42
P3-30--D1			39		B44
P3-30-RD1			41		A45
P3-31--D1			45		A47
P3-31-RD1	03	03-LX4C	47	J3-9E	B48

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P4-24--D1	04	04-LX4C	3	J5-9E	B26
P4-24-RD1			5		A27
P4-25--D1			9		A29
P4-25-RD1			11		B30
P4-26--D1			15		B32
P4-26-RD1			17		A33
P4-27--D1			21		A35
P4-27-RD1			23		B36
P4-28--D1			27		B38
P4-28-RD1			29		A39
P4-29--D1			33		A41
P4-29-RD1			35		B42
P4-30--D1			39		B44
P4-30-RD1			41		A45
P4-31--D1			45		A47
P4-31-RD1	04	04-LX4C	47	J5-9E	B48
P5-24--D1	05	05-LX4C	3	J5-9E	D26
P5-24-RD1			5		C27
P5-25--D1			9		C29
P5-25-RD1			11		D30
P5-26--D1			15		D32
P5-26-RD1			17		C33
P5-27--D1			21		C35
P5-27-RD1			23		D36
P5-28--D1			27		D38
P5-28-RD1			29		C39
P5-29--D1			33		C41
P5-29-RD1			35		D42
P5-30--D1			39		D44
P5-30-RD1			41		C45
P5-31--D1			45		C47
P5-31-RD1	05	05-LX4C	47	J5-9E	D48

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P6-24--D1	06	06-LX4C	3	J5-9E	B2
P6-24-RD1			5		A3
P6-25--D1			9		A5
P6-25-RD1			11		B6
P6-26--D1			15		B8
P6-26-RD1			17		A9
P6-27--D1			21		A11
P6-27-RD1			23		B12
P6-28--D1			27		B14
P6-28-RD1			29		A15
P6-29--D1			33		A17
P6-29-RD1			35		B18
P6-30--D1			39		B20
P6-30-RD1			41		A21
P6-31--D1			45		A23
P6-31-RD1	06	06-LX4C	47	J5-9E	B24

P7-24--D1	07	07-LX4C	3	J5-9E	D2
P7-24-RD1			5		C3
P7-25--D1			9		C5
P7-25-RD1			11		D6
P7-26--D1			15		D8
P7-26-RD1			17		C9
P7-27--D1			21		C11
P7-27-RD1			23		D12
P7-28--D1			27		D14
P7-28-RD1			29		C15
P7-29--D1			33		C17
P7-29-RD1			35		D18
P7-30--D1			39		D20
P7-30-RD1			41		C21
P7-31--D1			45		C23
P7-31-RD1	07	07-LX4C	47	J5-9E	D24

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P0-32--D1	00	00-KX1C	3	J3-9D	D2
P0-32-RD1			5		C3
P0-33--D1			9		C5
P0-33-RD1			11		D6
P0-34--D1			15		D8
P0-34-RD1			17		C9
P0-35--D1			21		C11
P0-35-RD1			23		D12
P0-36--D1			27		D14
P0-36-RD1			29		C15
P0-37--D1			33		C17
P0-37-RD1			35		D18
P0-38--D1			39		D20
P0-38-RD1			41		C21
P0-39--D1			45		C23
P0-39-RD1	00	00-KX1C	47	J3-9D	D24
P1-32--D1	01	01-KX1C	3	J3-9D	B2
P1-32-RD1			5		A3
P1-33--D1			9		A5
P1-33-RD1			11		B6
P1-34--D1			15		B8
P1-34-RD1			17		A9
P1-35--D1			21		A11
P1-35-RD1			23		B12
P1-36--D1			27		B14
P1-36-RD1			29		A15
P1-37--D1			33		A17
P1-37-RD1			35		B18
P1-38--D1			39		B20
P1-38-RD1			41		A21
P1-39--D1			45		A23
P1-39-RD1	01	01-KX1C	47	J3-9D	B24

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P2-32--D1	02	02-KX1C	3	J3-9D	D26
P2-32-RD1			5		C27
P2-33--D1			9		C29
P2-33-RD1			11		D30
P2-34--D1			15		D32
P2-34-RD1			17		C33
P2-35--D1			21		C35
P2-35-RD1			23		D36
P2-36--D1			27		D38
P2-36-RD1			29		C39
P2-37--D1			33		C41
P2-37-RD1			35		D42
P2-38--D1			39		D44
P2-38-RD1			41		C45
P2-39--D1			45		C47
P2-39-RD1	02	02-KX1C	47	J3-9D	D48
P3-32--D1	03	03-KX1C	3	J3-9D	B26
P3-32-RD1			5		A27
P3-33--D1			9		A29
P3-33-RD1			11		B30
P3-34--D1			15		B32
P3-34-RD1			17		A33
P3-35--D1			21		A35
P3-35-RD1			23		B36
P3-36--D1			27		B38
P3-36-RD1			29		A39
P3-37--D1			33		A41
P3-37-RD1			35		B42
P3-38--D1			39		B44
P3-38-RD1			41		A45
P3-39--D1			45		A47
P3-39-RD1	03	03-KX1C	47	J3-9D	B48

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P4-32--D1	04	04-KX1C	3	J5-9D	B26
P4-32-RD1			5		A27
P4-33--D1			9		A29
P4-33-RD1			11		B30
P4-34--D1			15		B32
P4-34-RD1			17		A33
P4-35--D1			21		A35
P4-35-RD1			23		B36
P4-36--D1			27		B38
P4-36-RD1			29		A39
P4-37--D1			33		A41
P4-37-RD1			35		B42
P4-38--D1			39		B44
P4-38-RD1			41		A45
P4-39--D1			45		A47
P4-39-RD1	04	04-KX1C	47	J5-9D	B48
P5-32--D1	05	05-KX1C	3	J5-9D	D26
P5-32-RD1			5		C27
P5-33--D1			9		C29
P5-33-RD1			11		D30
P5-34--D1			15		D32
P5-34-RD1			17		C33
P5-35--D1			21		C35
P5-35-RD1			23		D36
P5-36--D1			27		D38
P5-36-RD1			29		C39
P5-37--D1			33		C41
P5-37-RD1			35		D42
P5-38--D1			39		D44
P5-38-RD1			41		C45
P5-39--D1			45		C47
P5-39-RD1	05	05-KX1C	47	J5-9D	D48

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P6-32--D1	06	06-KX1C	3	J5-9D	B2
P6-32-RD1			5		A3
P6-33--D1			9		A5
P6-33-RD1			11		B6
P6-34--D1			15		B8
P6-34-RD1			17		A9
P6-35--D1			21		A11
P6-35-RD1			23		B12
P6-36--D1			27		B14
P6-36-RD1			29		A15
P6-37--D1			33		A17
P6-37-RD1			35		B18
P6-38--D1			39		B20
P6-38-RD1			41		A21
P6-39--D1			45		A23
P6-39-RD1	06	06-KX1C	47	J5-9D	B24

P7-32--D1	07	07-KX1C	3	J5-9D	D2
P7-32-RD1			5		C3
P7-33--D1			9		C5
P7-33-RD1			11		D6
P7-34--D1			15		D8
P7-34-RD1			17		C9
P7-35--D1			21		C11
P7-35-RD1			23		D12
P7-36--D1			27		D14
P7-36-RD1			29		C15
P7-37--D1			33		C17
P7-37-RD1			35		D18
P7-38--D1			39		D20
P7-38-RD1			41		C21
P7-39--D1			45		C23
P7-39-RD1	07	07-KX1C	47	J5-9D	D24

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P0-40--D1	00	00-KX2C	3	J3-9C	D2
P0-40-RD1			5		C3
P0-41--D1			9		C5
P0-41-RD1			11		D6
P0-42--D1			15		D8
P0-42-RD1			17		C9
P0-43--D1			21		C11
P0-43-RD1			23		D12
P0-44--D1			27		D14
P0-44-RD1			29		C15
P0-45--D1			33		C17
P0-45-RD1			35		D18
P0-46--D1			39		D20
P0-46-RD1			41		C21
P0-47--D1			45		C23
P0-47-RD1	00	00-KX2C	47	J3-9C	D24
P1-40--D1	01	01-KX2C	3	J3-9C	B2
P1-40-RD1			5		A3
P1-41--D1			9		A5
P1-41-RD1			11		B6
P1-42--D1			15		B8
P1-42-RD1			17		A9
P1-43--D1			21		A11
P1-43-RD1			23		B12
P1-44--D1			27		B14
P1-44-RD1			29		A15
P1-45--D1			33		A17
P1-45-RD1			35		B18
P1-46--D1			39		B20
P1-46-RD1			41		A21
P1-47--D1			45		A23
P1-47-RD1	01	01-KX2C	47	J3-9C	B24

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P2-40--D1	02	02-KX2C	3	J3-9C	D26
P2-40-RD1			5		C27
P2-41--D1			9		C29
P2-41-RD1			11		D30
P2-42--D1			15		D32
P2-42-RD1			17		C33
P2-43--D1			21		C35
P2-43-RD1			23		D36
P2-44--D1			27		D38
P2-44-RD1			29		C39
P2-45--D1			33		C41
P2-45-RD1			35		D42
P2-46--D1			39		D44
P2-46-RD1			41		C45
P2-47--D1			45		C47
P2-47-RD1	02	02-KX2C	47	J3-9C	D48

P3-40--D1	03	03-KX2C	3	J3-9C	B26
P3-40-RD1			5		A27
P3-41--D1			9		A29
P3-41-RD1			11		B30
P3-42--D1			15		B32
P3-42-RD1			17		A33
P3-43--D1			21		A35
P3-43-RD1			23		B36
P3-44--D1			27		B38
P3-44-RD1			29		A39
P3-45--D1			33		A41
P3-45-RD1			35		B42
P3-46--D1			39		B44
P3-46-RD1			41		A45
P3-47--D1			45		A47
P3-47-RD1	03	03-KX2C	47	J3-9C	B48

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P4-40--D1	04	04-KX2C	3	J5-9C	B26
P4-40-RD1			5		A27
P4-41--D1			9		A29
P4-41-RD1			11		B30
P4-42--D1			15		B32
P4-42-RD1			17		A33
P4-43--D1			21		A35
P4-43-RD1			23		B36
P4-44--D1			27		B38
P4-44-RD1			29		A39
P4-45--D1			33		A41
P4-45-RD1			35		B42
P4-46--D1			39		B44
P4-46-RD1			41		A45
P4-47--D1			45		A47
P4-47-RD1	04	04-KX2C	47	J5-9C	B48
P5-40--D1	05	05-KX2C	3	J5-9C	D26
P5-40-RD1			5		C27
P5-41--D1			9		C29
P5-41-RD1			11		D30
P5-42--D1			15		D32
P5-42-RD1			17		C33
P5-43--D1			21		C35
P5-43-RD1			23		D36
P5-44--D1			27		D38
P5-44-RD1			29		C39
P5-45--D1			33		C41
P5-45-RD1			35		D42
P5-46--D1			39		D44
P5-46-RD1			41		C45
P5-47--D1			45		C47
P5-47-RD1	05	05-KX2C	47	J5-9C	D48

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P6-40--D1	06	06-KX2C	3	J5-9C	B2
P6-40-RD1			5		A3
P6-41--D1			9		A5
P6-41-RD1			11		B6
P6-42--D1			15		B8
P6-42-RD1			17		A9
P6-43--D1			21		A11
P6-43-RD1			23		B12
P6-44--D1			27		B14
P6-44-RD1			29		A15
P6-45--D1			33		A17
P6-45-RD1			35		B18
P6-46--D1			39		B20
P6-46-RD1			41		A21
P6-47--D1			45		A23
P6-47-RD1	06	06-KX2C	47	J5-9C	B24

P7-40--D1	07	07-KX2C	3	J5-9C	D2
P7-40-RD1			5		C3
P7-41--D1			9		C5
P7-41-RD1			11		D6
P7-42--D1			15		D8
P7-42-RD1			17		C9
P7-43--D1			21		C11
P7-43-RD1			23		D12
P7-44--D1			27		D14
P7-44-RD1			29		C15
P7-45--D1			33		C17
P7-45-RD1			35		D18
P7-46--D1			39		D20
P7-46-RD1			41		C21
P7-47--D1			45		C23
P7-47-RD1	07	07-KX2C	47	J5-9C	D24

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P0-48--D1	00	00-LX3C	3	J3-9B	D2
P0-48-RD1			5		C3
P0-49--D1			9		C5
P0-49-RD1			11		D6
P0-50--D1			15		D8
P0-50-RD1			17		C9
P0-51--D1			21		C11
P0-51-RD1			23		D12
P0-52--D1			27		D14
P0-52-RD1			29		C15
P0-53--D1			33		C17
P0-53-RD1			35		D18
P0-54--D1			39		D20
P0-54-RD1			41		C21
P0-55--D1			45		C23
P0-55-RD1	00	00-LX3C	47	J3-9B	D24
P1-48--D1	01	01-LX3C	3	J3-9B	B2
P1-48-RD1			5		A3
P1-49--D1			9		A5
P1-49-RD1			11		B6
P1-50--D1			15		B8
P1-50-RD1			17		A9
P1-51--D1			21		A11
P1-51-RD1			23		B12
P1-52--D1			27		B14
P1-52-RD1			29		A15
P1-53--D1			33		A17
P1-53-RD1			35		B18
P1-54--D1			39		B20
P1-54-RD1			41		A21
P1-55--D1			45		A23
P1-55-RD1	01	01-LX3C	47	J3-9B	B24

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P2-48--D1	02	02-KX3C	3	J3-9B	D26
P2-48-RD1			5		C27
P2-49--D1			9		C29
P2-49-RD1			11		D30
P2-50--D1			15		D32
P2-50-RD1			17		C33
P2-51--D1			21		C35
P2-51-RD1			23		D36
P2-52--D1			27		D38
P2-52-RD1			29		C39
P2-53--D1			33		C41
P2-53-RD1			35		D42
P2-54--D1			39		D44
P2-54-RD1			41		C45
P2-55--D1			45		C47
P2-55-RD1	02	02-KX3C	47	J3-9B	D48
P3-48--D1	03	03-KX3C	3	J3-9B	B26
P3-48-RD1			5		A27
P3-49--D1			9		A29
P3-49-RD1			11		B30
P3-50-RD1			15		B32
P3-50-RD1			17		A33
P3-51--D1			21		A35
P3-51-RD1			23		B36
P3-52--D1			27		B38
P3-52-RD1			29		A39
P3-53--D1			33		A41
P3-53-RD1			35		B42
P3-54--D1			39		B44
P3-54-RD1			41		A45
P3-55--D1			45		A47
P3-55-RD1	03	03-KX3C	47	J3-9B	B48

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P4-48--D1	04	04-KX3C	3	J5-9B	B26
P4-48-RD1			5		A27
P4-49--D1			9		A29
P4-49-RD1			11		B30
P4-50--D1			15		B32
P4-50-RD1			17		A33
P4-51--D1			21		A35
P4-51-RD1			23		B36
P4-52--D1			27		B38
P4-52-RD1			29		A39
P4-53--D1			33		A41
P4-53-RD1			35		B42
P4-54--D1			39		B44
P4-54-RD1			41		A45
P4-55--D1			45		A47
P4-55-RD1	04	04-KX3C	47	J5-9B	B48

P5-48--D1	05	05-KX3C	3	J5-9B	D26
P5-48-RD1			5		C27
P5-49--D1			9		C29
P5-49-RD1			11		D30
P5-50--D1			15		D32
P5-50-RD1			17		C33
P5-51--D1			21		C35
P5-51-RD1			23		D36
P5-52--D1			27		D38
P5-52-RD1			29		C39
P5-53--D1			33		C41
P5-53-RD1			35		D42
P5-54--D1			39		D44
P5-54-RD1			41		C45
P5-55--D1			45		C47
P5-55-RD1	05	05-KX3C	47	J5-9B	D48

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P6-48--D1	06	06-KX3C	3	J5-9B	B2
P6-48-RD1			5		A3
P6-49--D1			9		A5
P6-49-RD1			11		B6
P6-50--D1			15		B8
P6-50-RD1			17		A9
P6-51--D1			21		A11
P6-51-RD1			23		B12
P6-52--D1			27		B14
P6-52-RD1			29		A15
P6-53--D1			33		A17
P6-53-RD1			35		B18
P6-54--D1			39		B20
P6-54-RD1			41		A21
P6-55--D1			45		A23
P6-55-RD1	06	06-KX3C	47	J5-9B	B24

P7-48--D1	07	07-KX3C	3	J5-9B	D2
P7-48-RD1			5		C3
P7-49--D1			9		C5
P7-49-RD1			11		D6
P7-50--D1			15		D8
P7-50-RD1			17		C9
P7-51--D1			21		C11
P7-51-RD1			23		D12
P7-52--D1			27		D14
P7-52-RD1			29		C15
P7-53--D1			33		C17
P7-53-RD1			35		D18
P7-54--D1			39		D20
P7-54-RD1			41		C21
P7-55--D1			45		C23
P7-55-RD1	07	07-KX3C	47	J5-9B	D24

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P0-56--D1	00	00-KX4C	3	J3-9A	D2
P0-56-RD1			5		C3
P0-57--D1			9		C5
P0-57-RD1			11		D6
P0-58--D1			15		D8
P0-58-RD1			17		C9
P0-59--D1			21		C11
P0-59-RD1			23		D12
P0-60--D1			27		D14
P0-60-RD1			29		C15
P0-61--D1			33		C17
P0-61-RD1			35		D18
P0-62--D1			39		D20
P0-62-RD1			41		C21
P0-63--D1			45		C23
P0-63-RD1	00	00-KX4C	47	J3-9A	D24
P1-56--D1	01	01-KX4C	3	J3-9A	B2
P1-56-RD1			5		A3
P1-57--D1			9		A5
P1-57-RD1			11		B6
P1-58--D1			15		B8
P1-58-RD1			17		A9
P1-59--D1			21		A11
P1-59-RD1			23		B12
P1-60--D1			27		B14
P1-60-RD1			29		A15
P1-61--D1			33		A17
P1-61-RD1			35		B18
P1-62--D1			39		B20
P1-62-RD1			41		A21
P1-63--D1			45		A23
P1-63-RD1	01	01-KX4C	47	J3-9A	B24

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P2-56--D1	02	02-KX4C	3	J3-9A	D26
P2-56-RD1			5		C27
P2-57--D1			9		C29
P2-57-RD1			11		D30
P2-58--D1			15		D32
P2-58-RD1			17		C33
P2-59--D1			21		C35
P2-59-RD1			23		D36
P2-60--D1			27		D38
P2-60-RD1			29		C39
P2-61--D1			33		C41
P2-61-RD1			35		D42
P2-62--D1			39		D44
P2-62-RD1			41		C45
P2-63--D1			45		C47
P2-63-RD1	02	02-KX4C	47	J3-9A	D48

P3-56--D1	03	03-KX4C	3	J3-9A	B26
P3-56-RD1			5		A27
P3-57--D1			9		A29
P3-57-RD1			11		B30
P3-58--D1			15		B32
P3-58-RD1			17		A33
P3-59--D1			21		A35
P3-59-RD1			23		B36
P3-60--D1			27		B38
P3-60-RD1			29		A39
P3-61--D1			33		A41
P3-61-RD1			35		B42
P3-62--D1			39		B44
P3-62-RD1			41		A45
P3-63--D1			45		A47
P3-63-RD1	03	03-KX4C	47	J3-9A	B48

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P4-56--D1	04	04-KX4C	3	J5-9A	B26
P4-56-RD1			5		A27
P4-57--D1			9		A29
P4-57-RD1			11		B30
P4-58--D1			15		B32
P4-58-RD1			17		A33
P4-59--D1			21		A35
P4-59-RD1			23		B36
P4-60--D1			27		B38
P4-60-RD1			29		A39
P4-61--D1			33		A41
P4-61-RD1			35		B42
P4-62--D1			39		B44
P4-62-RD1			41		A45
P4-63--D1			45		A47
P4-63-RD1	04	04-KX4C	47	J5-9A	B48
P5-56--D1	05	05-KX4C	3	J5-9A	D26
P5-56-RD1			5		C27
P5-57--D1			9		C29
P5-57-RD1			11		D30
P5-58--D1			15		D32
P5-58-RD1			17		C33
P5-59--D1			21		C35
P5-59-RD1			23		D36
P5-60--D1			27		D38
P5-60-RD1			29		C39
P5-61--D1			33		C41
P5-61-RD1			35		D42
P5-62--D1			39		D44
P5-62-RD1			41		C45
P5-63--D1			45		C47
P5-63-RD1	05	05-KX4C	47	J5-9A	D48

TABLE 7. DATA DISTRIBUTION BETWEEN CUB - CU (Continued)

SIGNAL NAME	SOURCE			DESTINATION	
	PUC No.	CUB Paddle Board No.	Pin No.	CU Conn.No.	Pin No.
P6-56--D1	06	06-KX4C	3	J5-9A	B2
P6-56-RD1			5		A3
P6-57--D1			9		A5
P6-57-RD1			11		B6
P6-58--D1			15		B8
P6-58-RD1			17		A9
P6-59--D1			21		A11
P6-59-RD1			23		B12
P6-60--D1			27		B14
P6-60-RD1			29		A15
P6-61--D1			33		A17
P6-61-RD1			35		B18
P6-62--D1			39		B20
P6-62-RD1			41		A21
P6-63--D1			45		A23
P6-63-RD1	06	06-KX4C	47	J5-9A	B24

P7-56--D1	07	07-KX4C	3	J5-9A	D2
P7-56-RD1			5		C3
P7-57--D1			9		C5
P7-57-RD1			11		D6
P7-58--D1			15		D8
P7-58-RD1			17		C9
P7-59--D1			21		C11
P7-59-RD1			23		D12
P7-60--D1			27		D14
P7-60-RD1			29		C15
P7-61--D1			33		C17
P7-61-RD1			35		D18
P7-62--D1			39		D20
P7-62-RD1			41		C21
P7-63--D1			45		C23
P7-63-RD1	07	07-KX4C	47	J5-9A	D24

III. DATA MOVEMENT BETWEEN IOSS AND MLU

A. Implementation

Figure 10 shows the data movement between the IOSS and the MLU in a fashion different from that shown in Figure 1 related to the CU data movement. As explained in the MLU Manual, the flow of data between the Input/Output Subsystem (IOSS) and the MLU is referred to as IOSS data to differentiate it from the other two types of data movement to CU (READ or TRANSFER operation). For this reason, we will use the term IOSS data from now on since this path is composed of bidirectional lines and the direction of data flow is not important when describing the physical interface of these transmission lines.

There are only two types of occasions in which IOSS data is moved between the IOSS and MLU, that is data is moved into the MLU from the IOSS when a WRITE operation is requested and from MLU to IOSS when a READ operation has been performed. WRITE and READ operations, however, are performed by the PEM via controls which are furnished to the PEM by its corresponding MLU (see MLU Manual for more details). When a WRITE operation is requested, the IOSS data leaves the Input/Output Switch (IOS) and via the Disconnect arrives in the MLU. From the MLU the data is brought into the PEM via the separate "write data lines", where it is stored as described in PEM Manual #PO-I1600-0000-A. When a READ operation is requested, the data is available to the MLU by the PEM via the separate "read data lines" and from there using the bidirectional lines, it is brought into the Disconnect and finally into the Input/Output Switch (IOS).

Since the IOSS data does not involve the PE at all with regard to the data movement, it may be said that while the IOSS is doing "business" exclusively with the PEM via the MLU, the only role of the PE in that transaction is to provide the path for the control signals and address to the MLU which originate from the CU.

From the system's point of view, IOSS data movement involves all the PUC's and two MLU's per PUC, which amounts to transfers of data to/from sixteen MLU's at a time. For this reason, the complete MLU-IOS path will be broken into two with the Disconnect used as a common point. Figure 11 is a sketch of the cabling involved and of the way these cables are interconnected from one end to the other.

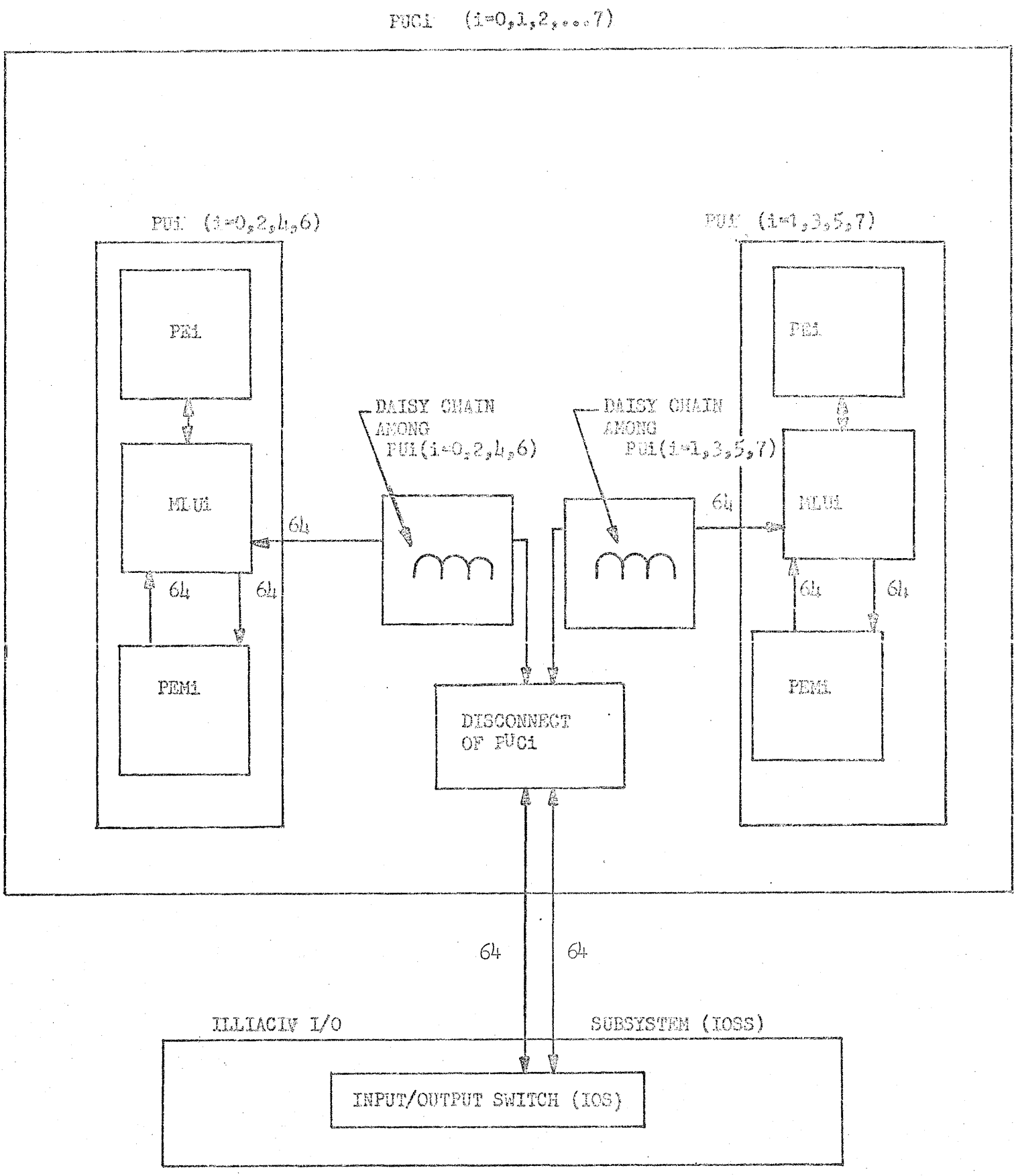

FIGURE 10. BLOCK DIAGRAM OF DATA MOVEMENT BETWEEN IOSS & MIU.

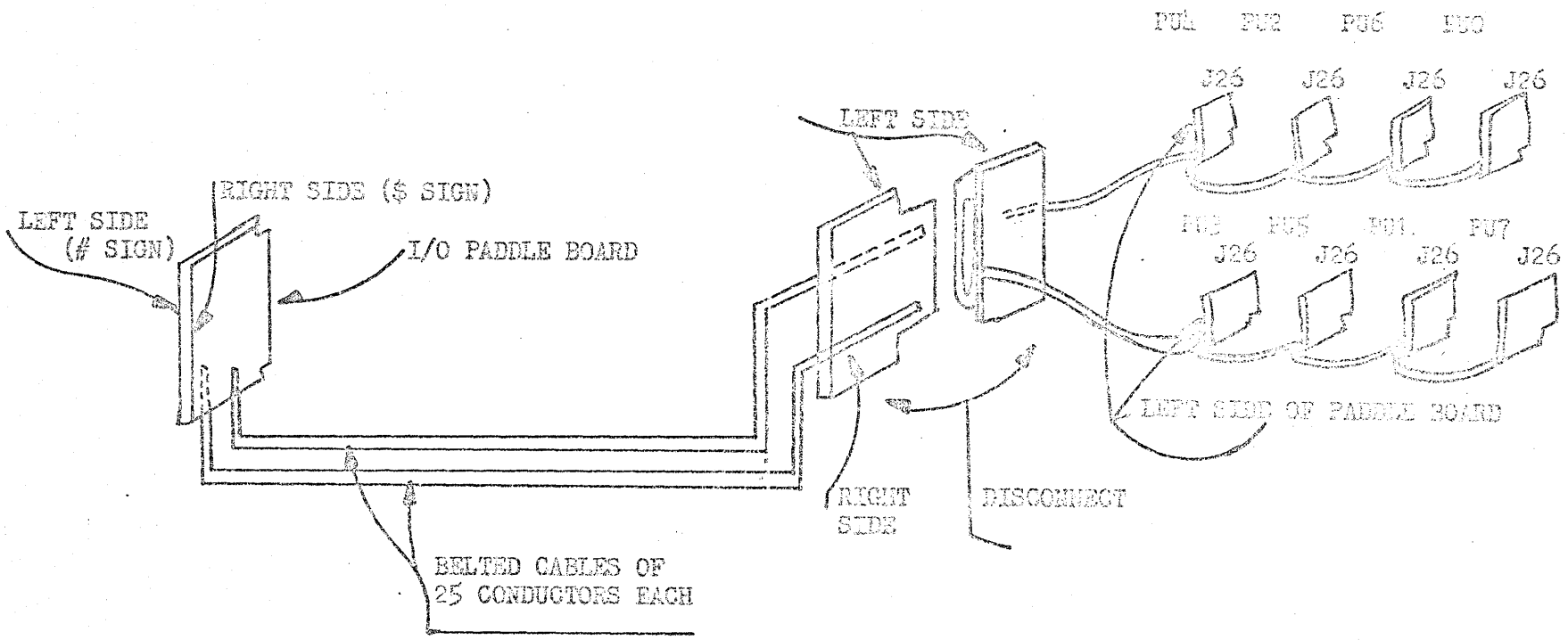

FIGURE 11. . SKETCH OF DATA MOVEMENT BETWEEN MLU AND IOS

NOTES:
1. EACH PADDLE BOARD BELONGS TO THE MLU PART OF EACH PU
2. PADDLE BOARDS OF EVEN PU NUMBERS CONNECT TO THE LEFT SIDE OF THE DISCONNECT CONNECTOR WHILE PADDLE BOARDS OF ODD PU NUMBERS CONNECT TO THE RIGHT SIDE OF THE DISCONNECT CONNECTOR
3. THE DAISY CHAINED BELTED CABLES CONNECT TO THE LEFT SIDE OF EACH MLU PADDLE BOARD BECAUSE THE RIGHT SIDE IS FOR THE CU DATA.

1. Data Movement Between MLU and Disconnect

In Section II, it was mentioned that each MLU has six IO/CUB connectors each of which is used for both CU and IOSS data. Figure 12 shows that these connectors are connected via paddle boards with each of the connectors of the Disconnect. In other words, comparison of Figures 4 and 12 reveals that the right side of each paddle board inserted into the MLU connector is connected with all the paddle boards of the MLU's (eight of them) within the PUC for CU data. For the IOSS data, however, the left side of each paddle board of MLU's belonging to even PU numbers is daisy chained and connected to the left side of the Disconnect connector, while the left side of each paddle board of MLU's belonging to odd PU numbers is daisy chained and connected to the right side of the Disconnect connector (see Figures 11 and 12). The breaking of the daisy chained PU's into two groups is dictated by the fact that IO requests select eight PUC's and two PU's within each PUC at a time. This means that any time an IO request is to be implemented, two PU's within the same PUC are selected. By breaking the PU's into two groups (even PU numbers constitute one group, while odd PU numbers constitute the other group), the selected PU's by IO requests should belong to different groups. For example, if PU-4 is one of the selected PU's, one should expect that another PU with odd number should also be selected at the same time, but never a PU which belongs to the same group that PU-4 does (even PU number).

Figure 2 shows the pin configuration of the IO/CUB connector. The odd pin numbers (left side of the connector) are used for the IOSS data, while the even pin numbers are used for the CU data. Each IO/CUB connector accomodates approximately 11 data bits; there are six IO/CUB connectors to take care of 64 data bits and one strobe. The distribution of the IOSS data between the MLU and the Disconnect is shown in Table 8. It must be remembered that the Disconnect accomodates 64 data bits and one strobe for each of the two PU groups and even though the pin numbers of the Disconnect connectors for both sides are numbered identically, one should be able to locate the proper pin corresponding to a certain data bit by using Figures 11 and 12 and Table 8 as a reference.

2. Data Movement Between Disconnect and IOSS

As explained in Section II, the Disconnect plays no other role in the system than to provide flexibility in handling the belted cables between the MLU and the Input/Output Switch (IOS).

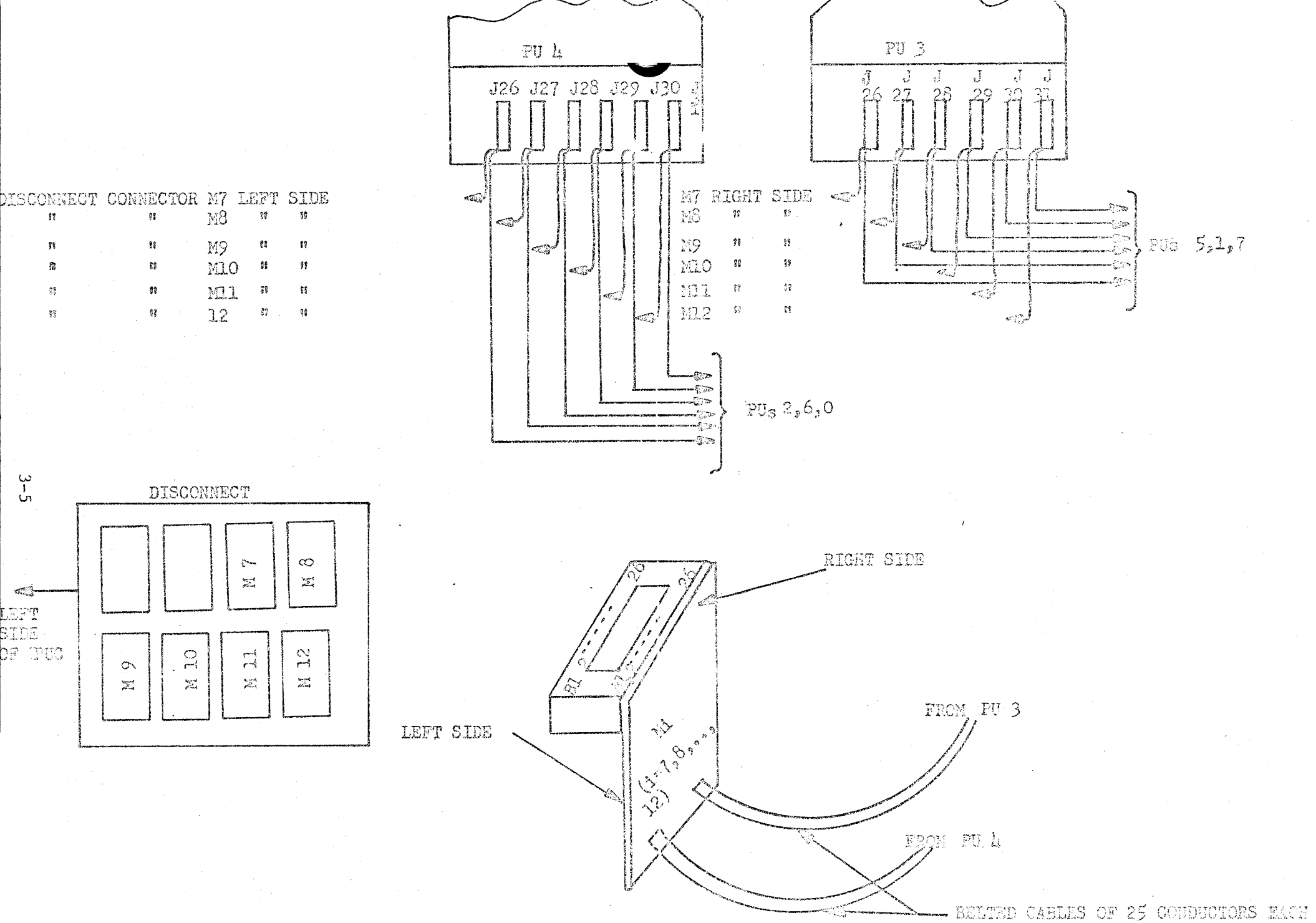

FIGURE 12. SKETCH OF MLH-DISCONECT CONNECTORS FOR LOSS DATA

TABLE 8. Data Movement Between MLU and Disconnect

SIGNAL NAME	MLU		DISCONNECT		REMARKS
	Connector	Pin	Connector	Pin	
MOWIWOO--0	I/06 or J26	5	M7	2	For PU-0, 2, 4,
01		11		5	6, refer to the
02		17		8	left side of the
03		23		10	Disconnect (see
04		29		12	Figures 11 and 12)
05		35		14	
06		41		16	
07		47		18	For PU-1, 3, 5,
08		53		20	7, refer to the
09		59		22	right side of the
MOWIW10--0	I/06 or J26	65	M7	25	Disconnect (see
MOWIW11--0	I/05 or J27	5	M8	2	Figures 11 and 12)
12		11		5	
13		17		8	
14		23		10	
15		29		12	
16		35		14	
17		41		16	
18		47		18	
19		53		20	
20		59		22	
MOWIW21--0	I/05 or J27	65	M8	25	
MOWIW22--0	I/04 or J28	5	M9	2	
23		11		5	
24		17		8	
25		23		10	
26		29		12	
27		35		14	
28		41		16	
29		47		18	
30		53		20	
MOWIW31	I/04 or J28	59	M9	22	

TABLE 8. Data Movement Between MLU and Disconnect (Continued)

SIGNAL NAME	MLU		DISCONNECT		REMARKS
	Connector	Pin	Connector	Pin	
MOWIW32--0	I/05 or J29	5	M10	2	
33		11		5	
34		17		8	
35		23		10	
36		29		12	
37		35		14	
38		41		16	
39		47		18	
40		53		20	
41		59		22	
MOWIW42--0	I/05 or J29	65	M10	25	
MOWIW43--0	I/02 or J30	5	M11	2	
44		11		5	
45		17		8	
46		23		10	
47		29		12	
48		35		14	
49		41		16	
50		47		18	
51		53		20	
52		59		22	
MOWIW53	I/02 or J30	65	M11	25	
MOWIW54	I/01 or J31	5	M12	2	
55		11		5	
56		17		8	
57		23		10	
58		29		12	
59		35		14	
60		41		16	
61		47		18	
62		53		20	
63		59		22	
MSTMWIW--0	I/01 or J31	65	M12	25	

Figure 11 shows that the paddle boards of the Disconnect connect to the IOS paddle boards via two 25-conductor belted cables. At this point, a new numbering convention is introduced. That is the IOS connector pins are assigned alphabetic characters with the # sign preceding the character for those signals distributed via the belted cables connected to the left side of the IOS paddle board and with the $ sign preceding the character for those signals distributed via the belted cables connected to the right side of the I/O paddle board.

Each I/O paddle board is defined by its location in the IOS as follows: The IOS is distributed into two panels (AC and AD) as it is shown in Figure 13. Each panel is subdivided into eleven columns (A to K) and six rows (B, D, F, H, J, L). Each column contains five slots each one to be used for an IOS paddle board. The paddle boards have been marked so that one can very easily identify a paddle board in terms of bits that this board accommodates by simply referring to Table 10.

Because the IOS occupies panels AC and AD, in Table 10 in the column specifying the location of I/O paddle board, we omit A since A is common to both panels. The location of an IOS paddle board is given by four characters. The first specifies the panel, the second specifies the row in the panel, the third specifies the column within the panel, and the fourth specifies the slot number.

For example, the notation A000 CLA8 $U reads as follows "This is bit 0 found on the U pin of the IOS paddle board located on the side which is marked 'right' and the paddle board is plugged into slot 8 of row L and column A of panel AC". It was said that each time the IOS and MLU's exchange data, sixteen MLU's participate in that action simultaneously. This means (see Table 9) that in order to access one word in all 64 PEM's of the Array that requires four IO requests. From Table 9, one can derive the conclusion that the selection of two PU's in all eight PUC's follows the PU grouping (even, odd) which was explained previously. In this fashion, PU-0 and 1 or PU-2 and 3 or PU-4 and 5 or PU-6 and 7 are selected simultaneously in all eight PUC's. Thus, data transfers to or from sixteen PEM's at a time is a normal mode of operation and it cannot be changed unless a change in the hardware is implemented.

TABLE 9. Data Distribution between MLUs and IOs

SIGNAL NAME	A000-A127				A128-A255				B000-B127				B128-B255				C000-C127				C128-C256				D000-D127				D128-D255			
BIT #	Bits 0-63		Bits 0-63		Bits 0-63		Bits 0-63		Bits 0-63		Bits 0-63		Bits 0-63		Bits 0-63		Bits 0-63		Bits 0-63		Bits 0-63		Bits 0-63		Bits 0-63		Bits 0-63		Bits 0-63		Bits 0-63	
IO WORD #	PU	PUC	PU	PUC	PU	PUC	PU	PUC	PU	PUC	PU	PUC	PU	PUC	PU	PUC	PU	PUC	PU	PUC	PU	PUC	PU	PUC	PU	PUC	PU	PUC	PU	PUC	PU	PUC
0	0	0	0	1	0	2	0	3	0	4	0	5	0	6	0	7	1	0	1	1	1	2	1	3	1	4	1	5	1	6	1	7
1	2	0	2	1	2	2	2	3	2	4		5	2	6	2	7	3	0	3	1	3	2	3	3	3	4	3	5	3	6	3	7
2	4	0	4	1	4	2	4	3	4	4		5	4	6	4	7	5	0	5	1	5	2	5	3	5	4	5	5	5	6	5	7
3	6	0	6	1	6	2	6	3	6	4		5	6	6	6	7	7	0	7	1	7	2	7	3	7	4	7	5	7	6	7	7

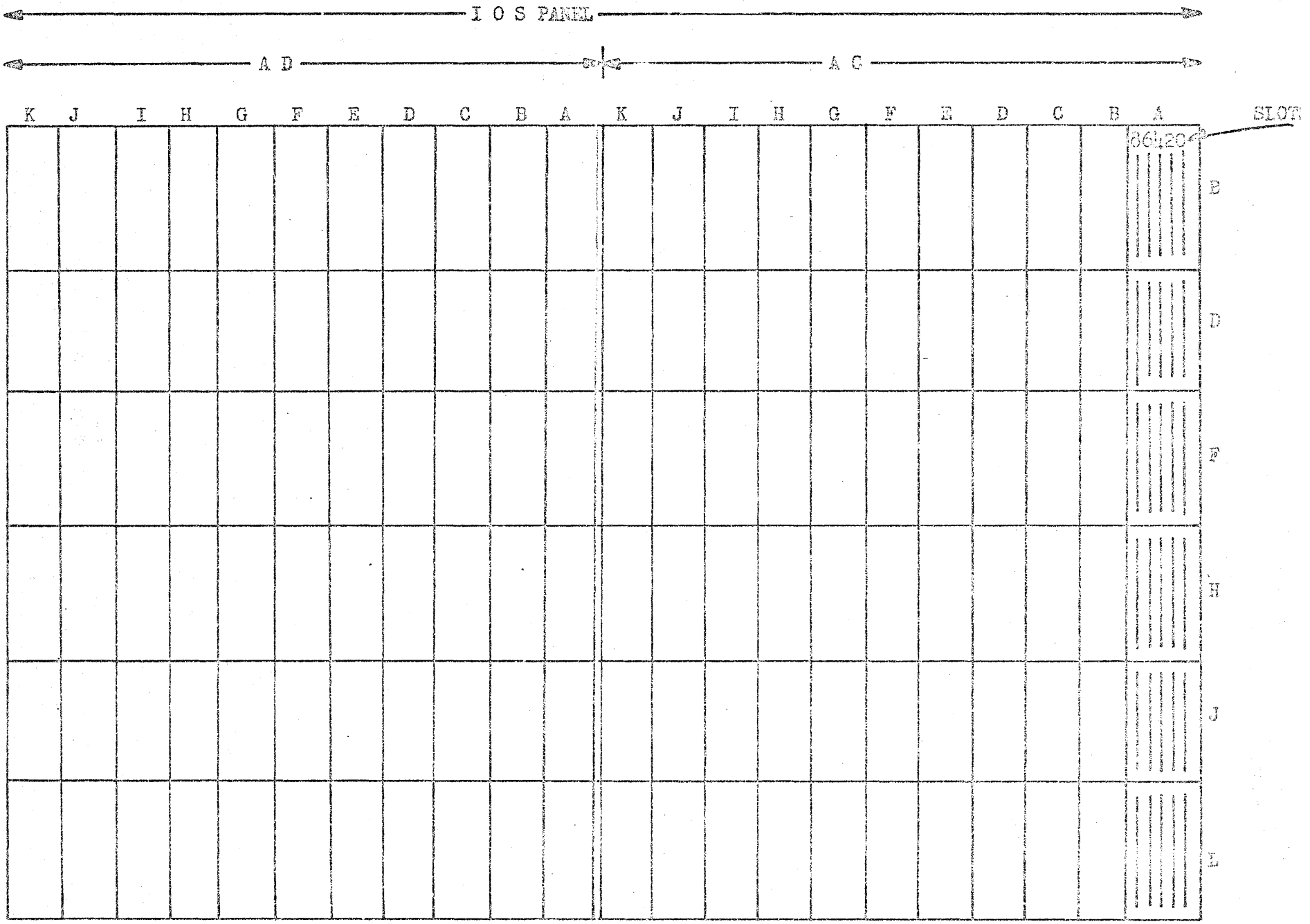

FIGURE 13. INPUT/OUTPUT SWITCH PANEL CONFIGURATION

In Table 9, in the column "Signal Name", there are four letters (A, B, C, D) used as prefixes corresponding to 256 data bits each. This distinction has no significance as far as IOSS-Array (MLU's) transfer are concerned, but indicates the four different data transfers between IOSS-DFC (256 bits each transfer) which correspond to one IOSS-Array data transfer.

Even though the scope of this document is not the description of the IOS, we feel that a typical data line configuration within the IOS could be helpful in demonstrating the flow of data in and out of the IOS.

Figure 14 shows that data is transferred between IOSS-Array via bidirectional lines whereas there is only one unidirectional line for the strobe which corresponds to 64 bits of each MLU. If a READ operation has been requested, data from the Array will be available to the Bus receiver of the "HA" Card of the IOS. The Array to Disk Enable will allow the data to pass through and arrive at Gate 2. In the meantime, the STROBE will have been received at the "HA" Card and after it has been redistributed (for fan-out purposes), it arrives at Gate 1. Gate 1 is enabled by the Array to Disk Enable and subsequently its output (STROBE) triggers Gate 2 whose output brings the data into the S-R Flip Flop. At this point, the IOSS-Array transfer has terminated. The data (output of the S-R Flip Flop) is available to be sent to the DFC.

If a WRITE operation is to take place, the data is brought to S-R Flip Flop from the DFC. The output of the Flip Flop is brought to Gate 3 which is enabled by the DISK to Array Enable. The output of Gate 3 is brought into the Bus driver ("HA" Card). The Disk to Array Enable allows the Bus driver to put the data on the bidirectional data line which, via the paddle board and the 25-conductor belted cable, allows the data to be brought to the Array.

Figure 14 shows only the basic path and controls for a data line. For more detail, the reader should consult the "HA" and "M" Cards Drawings where he will also find the signal names, controls and timing and logic for the DFC-IOSS transfers.

Figure 15 shows the IOS hardware (IOS panels) and paddle boards which are used for data transfers between IOS and Array (MLU's).

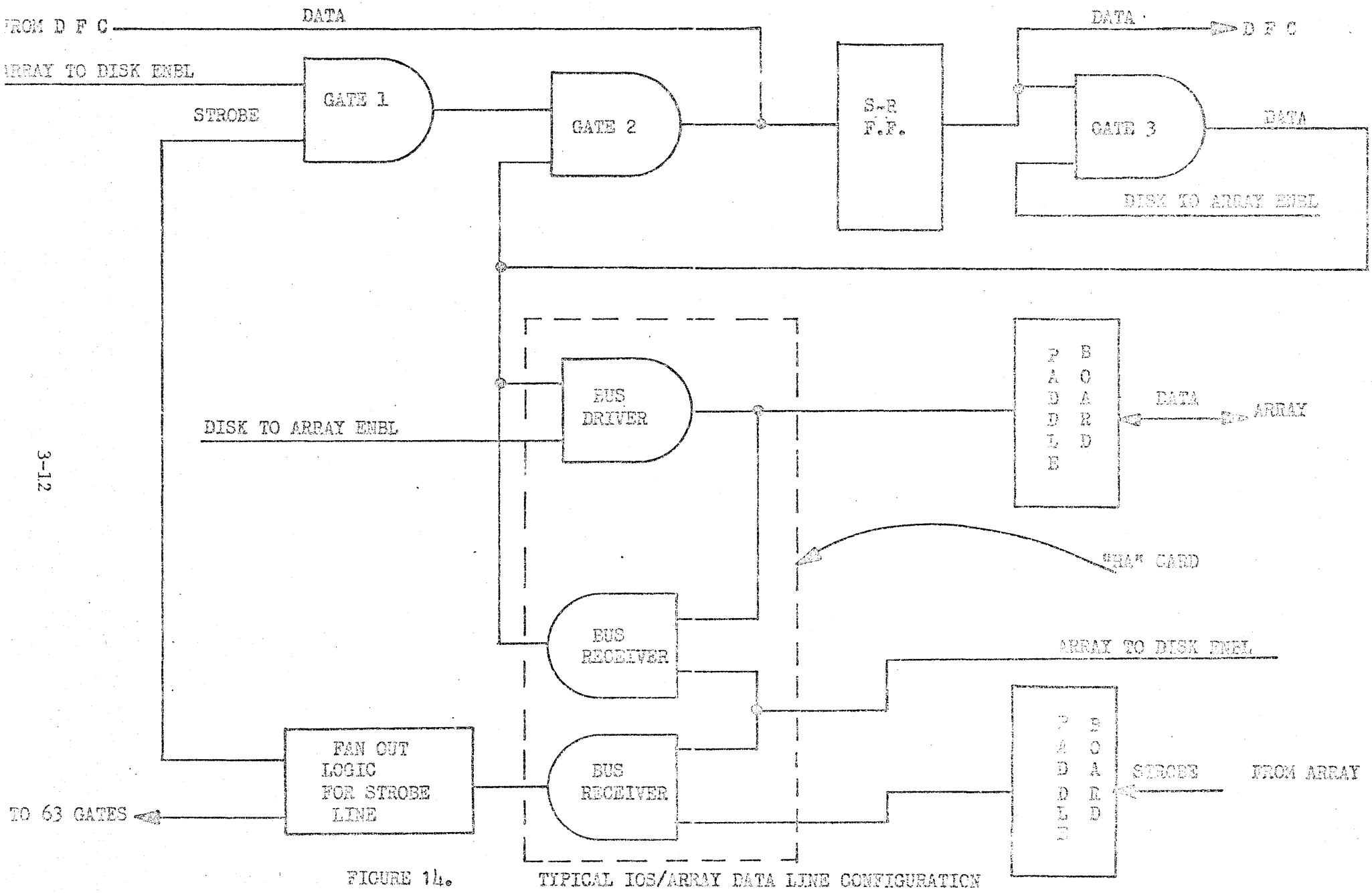

FIGURE 14. TYPICAL IOS/ARRAY DATA LINE CONFIGURATION

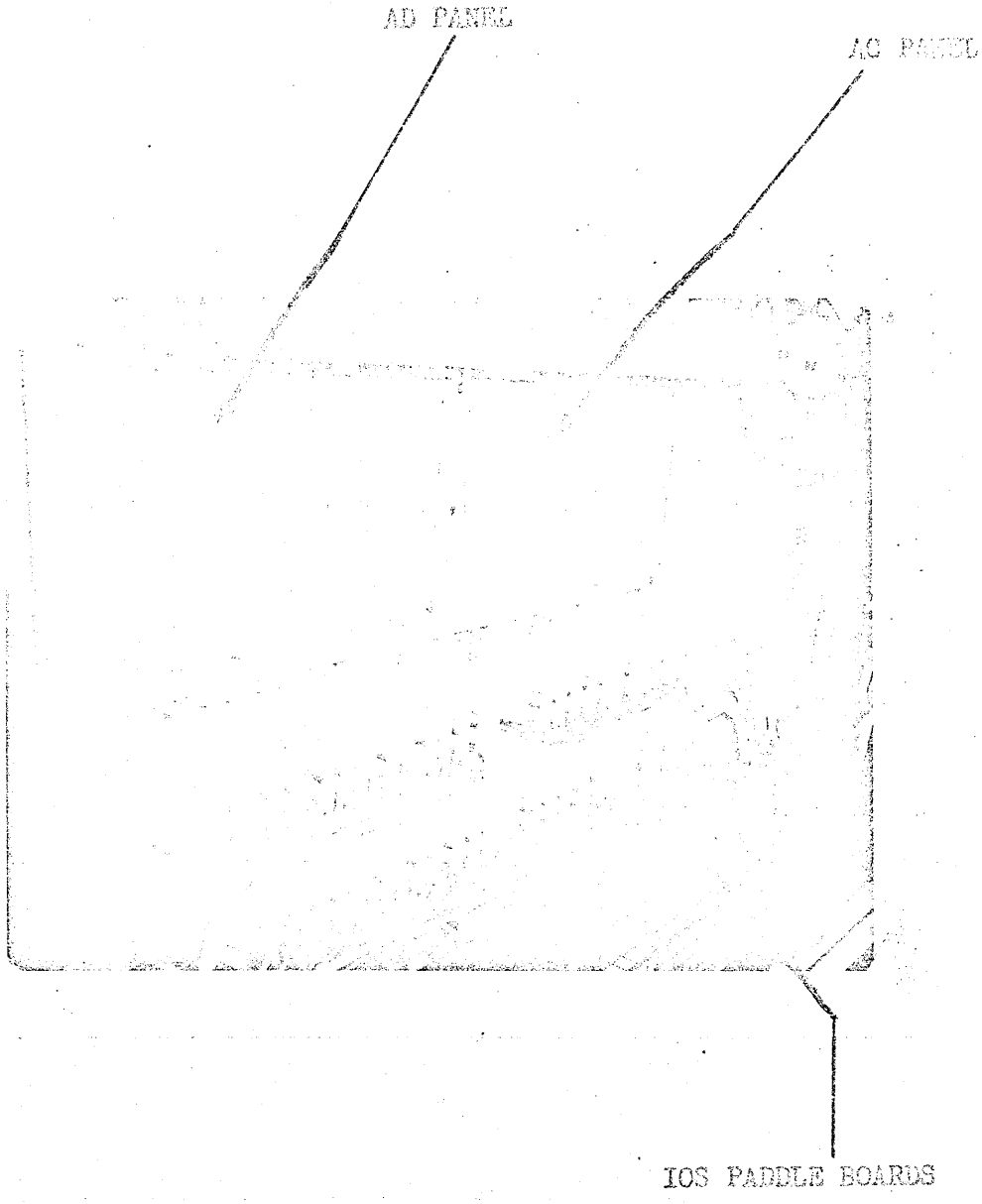

FIGURE 15. IOS HARDWARE(AC & AD PANELS)

Table 10. PU/IOS Bit-by-Bit Correspondence

PUC-0				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	0	A000	CLA8	$U
	1	1		T
	2	2		R
	3	3		Q
	4	4		N
	5	5		M
	6	6		K
	7	7		J
	8	8		H
	9	9		G
	10	10	CLA8	E
	11	11	CLB6	U
	12	12		T
	13	13		R
	14	14		Q
	15	15		N
	16	16		M
	17	17		K
	18	18		J
	19	19		H
	20	20		G
	21	21	CLB6	E
	22	22	CLC4	U
	23	23		T
	24	24		R
	25	25		Q
	26	26		N
	27	27		M
	28	28		K
	29	29		J
	30	30		H
PU 0,2,4,6	31	A031	CLC4	G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-0				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	32	A032	CLD2	$U
	33	33		T
	34	34		R
	35	35		Q
	36	36		N
	37	37		M
	38	38		K
	39	39		J
	40	40		H
	41	41		G
	42	42	CLD2	E
	43	43	CLEO	U
	44	44		T
	45	45		R
	46	46		Q
	47	47		N
	48	48		M
	49	49		K
	50	50		J
	51	51		H
	52	52		G
	53	53	CLEO	E
	54	54	CLE8	U
	55	55		T
	56	56		R
	57	57		Q
	58	58		N
	59	59		M
	60	60		K
	61	61		J
	62	62		H
	63	63		G
PU 0,2,4,6		Strobe	CLE8	E

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-1				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	0	A064	CLF6	$U
	1	65		T
	2	66		R
	3	67		Q
	4	68		N
	5	69		M
	6	70		K
	7	71		J
	8	72		H
	9	73		G
	10	74	CLF6	E
	11	75	CLG2	U
	12	76		T
	13	77		R
	14	78		Q
	15	79		N
	16	80		M
	17	81		K
	18	82		J
	19	83		H
	20	84		G
	21	85	CLG2	E
	22	86	CLH2	U
	23	87		T
	24	88		R
	25	89		Q
	26	90		N
	27	91		M
	28	92		K
	29	93		J
	30	94		H
PU 0,2,4,6	31	A095		G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-1				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	32	A096	CLI2	$U
	33	97		T
	34	98		R
	35	99		Q
	36	100		N
	37	101		M
	38	102		K
	39	103		J
	40	104		H
	41	105		G
	42	106	CLI2	E
	43	107	CLJO	U
	44	108		T
	45	109		R
	46	110		Q
	47	111		N
	48	112		M
	49	113		K
	50	114		J
	51	115		H
	52	116		G
	53	117	CLJO	E
	54	118	CLJ8	U
	55	119		T
	56	120		R
	57	121		Q
	58	122		N
	59	123		M
	60	124		K
	61	125		J
	62	126		H
	63	127		G
PU 0,2,4,6		Strobe	CLJ8	E

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-2				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	0	A128	DLA2	$U
	1	129		T
	2	130		R
	3	131		Q
	4	132		N
	5	133		M
	6	134		K
	7	135		J
	8	136		H
	9	137		G
	10	138	DLA2	E
	11	139	DLA8	U
	12	140		T
	13	141		R
	14	142		Q
	15	143		N
	16	144		M
	17	145		K
	18	146		J
	19	147		H
	20	148		G
	21	149	DLA8	E
	22	150	DLB6	U
	23	151		T
	24	152		R
	25	153		Q
	26	154		N
	27	155		M
	28	156		K
	29	157		J
	30	158		H
PU 0,2,4,6	31	A159	DLB6	G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-2				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	32	A160	DLC4	$U
	33	161		T
	34	162		R
	35	163		Q
	36	164		N
	37	165		M
	38	166		K
	39	167		J
	40	168		H
	41	169		G
	42	170	DLC4	E
	43	171	DLDO	U
	44	172		T
	45	173		R
	46	174		Q
	47	175		N
	48	176		M
	49	177		K
	50	178		J
	51	179		H
	52	180		G
	53	181	DLDO	E
	54	182	DLE4	U
	55	183		T
	56	184		R
	57	185		Q
	58	186		N
	59	187		M
	60	188		K
	61	189		J
	62	190		H
	63	A191		G
PU 0,2,4,6		Strobe	DLE4	E

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-3				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	0	A192	DLF4	$U
	1	193		T
	2	194		R
	3	195		Q
	4	196		N
	5	197		M
	6	198		K
	7	199		J
	8	200		H
	9	201		G
	10	202	DLF4	E
	11	203	DLG0	U
	12	204		T
	13	205		R
	14	206		Q
	15	207		N
	16	208		M
	17	209		K
	18	210		J
	19	211		H
	20	212		G
	21	213	DLG0	E
	22	214	DLG6	U
	23	215		T
	24	216		R
	25	217		Q
	26	218		N
	27	219		M
	28	220		K
	29	221		J
	30	222		H
PU 0,2,4,6	31	A223	DLG6	G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-3				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	32	A224	DLH6	$U
	33	225		T
	34	226		R
	35	227		Q
	36	228		N
	37	229		M
	38	230		K
	39	231		J
	40	232		H
	41	233		G
	42	234	DLH6	E
	43	235	DLI2	U
	44	236		T
	45	237		R
	46	238		Q
	47	239		N
	48	240		M
	49	241		K
	50	242		J
	51	243		H
	52	244		G
	53	245	DLI2	E
	54	246	DLJ2	U
	55	247		T
	56	248		R
	57	249		Q
	58	250		N
	59	251		M
	60	252		K
	61	253		J
	62	254		H
	63	A255		G
PU 0,2,4,6		Strobe	DLJ2	E

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-4				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	0	B000	CJA8	$U
	1	001		T
	2	002		R
	3	003		Q
	4	004		N
	5	005		M
	6	006		K
	7	007		J
	8	008		H
	9	009		G
	10	010	CJA8	E
	11	011	CJB6	U
	12	012		T
	13	013		R
	14	014		Q
	15	015		N
	16	016		M
	17	017		K
	18	018		J
	19	019		H
	20	020		G
	21	021	CJB6	E
	22	022	CJC4	U
	23	023		T
	24	024		R
	25	025		Q
	26	026		N
	27	027		M
	28	028		K
	29	029		J
	30	030		H
PU 0,2,4,6	31	B031	CJC4	G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-4				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	32	B032	CJD2	$U
	33	033		T
	34	034		R
	35	035		Q
	36	036		N
	37	037		M
	38	038		K
	39	039		J
	40	040		H
	41	041		G
	42	042	CJD2	E
	43	043	CJEO	U
	44	044		T
	45	045		R
	46	046		Q
	47	047		N
	48	048		M
	49	049		K
	50	050		J
	51	051		H
	52	052		G
	53	053	CJEO	E
	54	054	CJE8	U
	55	055		T
	56	056		R
	57	057		Q
	58	058		N
	59	059		M
	60	060		K
	61	061		J
	62	062		H
	63	063		G
PU 0,2,4,6		Strobe	CJE8	E

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-5				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	0	B064	CJF6	$U
	1	065		T
	2	066		R
	3	067		Q
	4	068		N
	5	069		M
	6	070		K
	7	071		J
	8	072		H
	9	073		G
	10	074	CJF6	E
	11	075	CJG2	U
	12	076		T
	13	077		R
	14	078		Q
	15	079		N
	16	080		M
	17	081		K
	18	082		J
	19	083		H
	20	084		G
	21	085	CJG2	E
	22	086	CJH2	U
	23	087		T
	24	088		R
	25	089		Q
	26	090		N
	27	091		M
	28	092		K
	29	093		J
	30	094		H
PU 0,2,4,6	31	095	CJH2	G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-5				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	32	B096	CJI2	$U
	33	097		T
	34	098		R
	35	099		Q
	36	100		N
	37	101		M
	38	102		K
	39	103		J
	40	104		H
	41	105		G
	42	106	CJI2	E
	43	107	CJJO	U
	44	108		T
	45	109		R
	46	110		Q
	47	111		N
	48	112		M
	49	113		K
	50	114		J
	51	115		H
	52	116		G
	53	117	CJJO	E
	54	118	CJJ8	U
	55	119		T
	56	120		R
	57	121		Q
	58	122		N
	59	123		M
	60	124		K
	61	125		J
	62	126		H
	63	B127		G
PU 0,2,4,6		Strobe	CJJ8	E

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-6				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	0	B128	DJA4	$U
	1	129		T
	2	130		R
	3	131		Q
	4	132		N
	5	133		M
	6	134		K
	7	135		J
	8	136		H
	9	137		G
	10	138	DJA4	E
	11	139	DJA8	U
	12	140		T
	13	141		R
	14	142		Q
	15	143		N
	16	144		M
	17	145		K
	18	146		J
	19	147		H
	20	148		G
	21	149	DJA8	E
	22	150	DJB6	U
	23	151		T
	24	152		R
	25	153		Q
	26	154		N
	27	155		M
	28	156		K
	29	157		J
	30	158		H
PU 0,2,4,6	31	B159	DJB6	G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-6				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	32	B160	DJC4	$U
	33	161		T
	34	162		R
	35	163		Q
	36	164		N
	37	165		M
	38	166		K
	39	167		J
	40	168		H
	41	169		G
	42	170	DJC4	E
	43	171	DJDO	U
	44	172		T
	45	173		R
	46	174		Q
	47	175		N
	48	176		M
	49	177		K
	50	178		J
	51	179		H
	52	180		G
	53	181	DJDO	E
	54	182	DJE4	U
	55	183		T
	56	184		R
	57	185		Q
	58	186		N
	59	187		M
	60	188		K
	61	189		J
	62	190		H
	63	B191		G
PU 0,2,4,6		Strobe	DJE4	E

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-7				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	0	B192	DJF4	$U
	1	193		T
	2	194		R
	3	195		Q
	4	196		N
	5	197		M
	6	198		K
	7	199		J
	8	200		H
	9	201		G
	10	202	DJF4	E
	11	203	DJG0	U
	12	204		T
	13	205		R
	14	206		Q
	15	207		N
	16	208		M
	17	209		K
	18	210		J
	19	211		H
	20	212		G
	21	213	DJG0	E
	22	214	DJG6	U
	23	215		T
	24	216		R
	25	217		Q
	26	218		N
	27	219		M
	28	220		K
	29	221		J
	30	222		H
PU 0,2,4,6	31	B223	DJG6	G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-7				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 0,2,4,6	32	B224	DJH6	$U
	33	225		T
	34	226		R
	35	227		Q
	36	228		N
	37	229		M
	38	230		K
	39	231		J
	40	232		H
	41	233		G
	42	234	DJH6	E
	43	235	DJI2	U
	44	236		T
	45	237		R
	46	238		Q
	47	239		N
	48	240		M
	49	241		K
	50	242		J
	51	243		H
	52	244		G
	53	245	DJI2	E
	54	246	DJJ2	U
	55	247		T
	56	248		R
	57	249		Q
	58	250		N
	59	251		M
	60	252		K
	61	253		J
	62	254		H
	63	B255		G
PU 0,2,4,6		Strobe	DJJ2	E

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-0				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	0	C000	CLA8	$U
	1	001		T
	2	002		R
	3	003		Q
	4	004		N
	5	005		M
	6	006		K
	7	007		J
	8	008		H
	9	009		G
	10	010	CLA8	E
	11	011	CLB6	U
	12	012		T
	13	013		R
	14	014		Q
	15	015		N
	16	016		M
	17	017		K
	18	018		J
	19	019		H
	20	020		G
	21	021	CLB6	E
	22	022	CLC4	U
	23	023		T
	24	024		R
	25	025		Q
	26	026		N
	27	027		M
	28	028		K
	29	029		J
	30	030		H
PU 1,3,5,7	31	C031	CLC4	G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-0				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	32	C032	CLD2	$U
	33	033		T
	34	034		R
	35	035		Q
	36	036		N
	37	037		M
	38	038		K
	39	039		J
	40	040		H
	41	041		G
	42	042	CLD2	E
	43	043	CLEO	U
	44	044		T
	45	045		R
	46	046		Q
	47	047		N
	48	048		M
	49	049		K
	50	050		J
	51	051		H
	52	052		G
	53	053	CLEO	E
	54	054	CLE8	U
	55	055		T
	56	056		R
	57	057		Q
	58	058		N
	59	059		M
	60	060		K
	61	061		J
	62	062		H
	63	063		G
PU 1,3,5,7		Strobe	CLE8	E

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-1				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	0	C064	CLF6	$U
	1	065		T
	2	066		R
	3	067		Q
	4	068		N
	5	069		M
	6	070		K
	7	071		J
	8	072		H
	9	073		G
	10	074	CLF6	E
	11	075	CLG2	U
	12	076		T
	13	077		R
	14	078		Q
	15	079		N
	16	080		M
	17	081		K
	18	082		J
	19	083		H
	20	084		G
	21	085	CLG2	E
	22	086	CLH2	U
	23	087		T
	24	088		R
	25	089		Q
	26	090		N
	27	091		M
	28	092		K
	29	093		J
	30	094		H
PU 1,3,5,7	31	095	CLH2	G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-1				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	32	C096	CLI2	$U
	33	097		T
	34	098		R
	35	099		Q
	36	100		N
	37	101		M
	38	102		K
	39	103		J
	40	104		H
	41	105		G
	42	106	CLI2	E
	43	107	CLJO	U
	44	108		T
	45	109		R
	46	110		Q
	47	111		N
	48	112		M
	49	113		K
	50	114		J
	51	115		H
	52	116		G
	53	117	CLJO	E
	54	118	CLJ8	U
	55	119		T
	56	120		R
	57	121		Q
	58	122		N
	59	123		M
	60	124		K
	61	125		J
	62	126		H
	63	C127		G
PU 1,3,5,7		Strobe	CLJ8	E

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-2				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	0	C128	DLA2	$U
	1	129		T
	2	130		R
	3	131		Q
	4	132		N
	5	133		M
	6	134		K
	7	135		J
	8	136		H
	9	137		G
	10	138	CLA2	E
	11	139	DLA8	U
	12	140		T
	13	141		R
	14	142		Q
	15	143		N
	16	144		M
	17	145		K
	18	146		J
	19	147		H
	20	148		G
	21	149	DLA8	E
	22	150	DLB6	U
	23	151		T
	24	152		R
	25	153		Q
	26	154		N
	27	155		M
	28	156		K
	29	157		J
	30	158		H
PU 1,3,5,7	31	C159	DLB6	G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-2				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	32	C160	DLC4	$U
	33	161		T
	34	162		R
	35	163		Q
	36	164		N
	37	165		M
	38	166		K
	39	167		J
	40	168		H
	41	169		G
	42	170	DLC4	E
	43	171	DLDO	U
	44	172		T
	45	173		R
	46	174		Q
	47	175		N
	48	176		M
	49	177		K
	50	178		J
	51	179		H
	52	180		G
	53	181	DLDO	E
	54	182	DLE4	U
	55	183		T
	56	184		R
	57	185		Q
	58	186		N
	59	187		M
	60	188		K
	61	189		J
	62	190		H
	63	C191		G
PU 1,3,5,7		Strobe	CLE4	E

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-3				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	0	C192	DLF4	$U
	1	193		T
	2	194		R
	3	195		Q
	4	196		N
	5	197		M
	6	198		K
	7	199		J
	8	200		H
	9	201		G
	10	202	DLF4	E
	11	203	DLGO	U
	12	204		T
	13	205		R
	14	206		Q
	15	207		N
	16	208		M
	17	209		K
	18	210		J
	19	211		H
	20	212		G
	21	213	DLGO	E
	22	214	DLG6	U
	23	215		T
	24	216		R
	25	217		Q
	26	218		N
	27	219		M
	28	220		K
	29	221		J
	30	222		H
PU 1,3,5,7	31	C223	DLG6	G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-3				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	32	C224	DLH6	$U
	33	225		T
	34	226		R
	35	227		Q
	36	228		N
	37	229		M
	38	230		K
	39	231		J
	40	232		H
	41	233		G
	42	234	DLH6	E
	43	235	DLI2	U
	44	236		T
	45	237		R
	46	238		Q
	47	239		N
	48	240		M
	49	241		K
	50	242		J
	51	243		H
	52	244		G
	53	245	DLI2	E
	54	246	DLJ2	U
	55	247		T
	56	248		R
	57	249		Q
	58	250		N
	59	251		M
	60	252		K
	61	253		J
	62	254		H
	63	C255		G
PU 1,3,5,7		Strobe	DLJ2	E

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-4				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	0	D000	CJA8	$U
	1	001		T
	2	002		R
	3	003		Q
	4	004		N
	5	005		M
	6	006		K
	7	007		J
	8	008		H
	9	009		G
	10	010	CJA8	E
	11	011	CJB6	U
	12	012		T
	13	013		R
	14	014		Q
	15	015		N
	16	016		M
	17	017		K
	18	018		J
	19	019		H
	20	020	CJB6	G
	21	021	CJC4	E
	22	022		U
	23	023		T
	24	024		R
	25	025		Q
	26	026		N
	27	027		M
	28	028		K
	29	029		J
	30	030		H
PU 1,3,5,7	31	D031	CJC4	G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-4				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	32	D032	CJD2	$U
	33	033		T
	34	034		R
	35	035		Q
	36	036		N
	37	037		M
	38	038		K
	39	039		J
	40	040		H
	41	041		G
	42	042	CJD2	E
	43	043	CJE0	U
	44	044		T
	45	045		R
	46	046		Q
	47	047		N
	48	048		M
	49	049		K
	50	050		J
	51	051		H
	52	052		G
	53	053	CJE0	E
	54	054	CJE8	U
	55	055		T
	56	056		R
	57	057		Q
	58	058		N
	59	059		M
	60	060		K
	61	061		J
	62	062		H
	63	D063		G
PU 1,3,5,7		Strobe	CJE8	E

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-5				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	0	D064	CJF6	$U
	1	065		T
	2	066		R
	3	067		Q
	4	068		N
	5	069		M
	6	070		K
	7	071		J
	8	072		H
	9	073		G
	10	074	CJF6	E
	11	075	CJG2	U
	12	076		T
	13	077		R
	14	078		Q
	15	079		N
	16	080		M
	17	081		K
	18	082		J
	19	083		H
	20	084		G
	21	085	CJG2	E
	22	086	CJH2	U
	23	087		T
	24	088		R
	25	089		Q
	26	090		N
	27	091		M
	28	092		K
	29	093		J
	30	094		H
PU 1,3,5,7	31	D095	CJH2	G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-5				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	32	D096	CJI2	$U
	33	097		T
	34	098		R
	35	099		Q
	36	100		N
	37	101		M
	38	102		K
	39	103		J
	40	104		H
	41	105		G
	42	106	CJI2	E
	43	107	CJJ0	U
	44	108		T
	45	109		R
	46	110		Q
	47	111		N
	48	112		M
	49	113		K
	50	114		J
	51	115		H
	52	116		G
	53	117	CJJ0	E
	54	118	CJJ8	U
	55	119		T
	56	120		R
	57	121		Q
	58	122		N
	59	123		M
	60	124		K
	61	125		J
	62	126		H
	63	D127		G
PU 1,3,5,7		Strobe	CJJ8	E

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-6				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	0	D128	DJA4	$U
	1	129		T
	2	130		R
	3	131		Q
	4	132		N
	5	133		M
	6	134		K
	7	135		J
	8	136		H
	9	137		G
	10	138	DJA4	E
	11	139	DJA8	U
	12	140		T
	13	141		R
	14	142		Q
	15	143		N
	16	144		M
	17	145		K
	18	146		J
	19	147		H
	20	148		G
	21	149	DJA8	E
	22	150	DJB6	U
	23	151		T
	24	152		R
	25	153		Q
	26	154		N
	27	155		M
	28	156		K
	29	157		J
	30	158		H
PU 1,3,5,7	31	D159	DJB6	G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-6				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	32	D160	DJC4	$U
	33	161		T
	34	162		R
	35	163		Q
	36	164		N
	37	165		M
	38	166		K
	39	167		J
	40	168		H
	41	169		G
	42	170	DJC4	E
	43	171	DJDO	U
	44	172		T
	45	173		R
	46	174		Q
	47	175		N
	48	176		M
	49	177		K
	50	178		J
	51	179		H
	52	180		G
	53	181	DJDO	E
	54	182	DJE4	U
	55	183		T
	56	184		R
	57	185		Q
	58	186		N
	59	187		M
	60	188		K
	61	189		J
	62	190		H
	63	D191		G
PU 1,3,5,7		Strobe	DJE4	E

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-7				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	0	D192	DJF4	$U
	1	193		T
	2	194		R
	3	195		Q
	4	196		N
	5	197		M
	6	198		K
	7	199		J
	8	200		H
	9	201		G
	10	202	DJF4	E
	11	203	DJGO	U
	12	204		T
	13	205		R
	14	206		Q
	15	207		N
	16	208		M
	17	209		K
	18	210		J
	19	211		H
	20	212		G
	21	213	DJGO	E
	22	214	DJG6	U
	23	215		T
	24	216		R
	25	217		Q
	26	218		N
	27	219		M
	28	220		K
	29	221		J
	30	222		H
PU 1,3,5,7	31	D223	DJG6	G

Table 10. PU/IOS Bit-by-Bit Correspondence (Cont.)

PUC-7				
PU Number	PU Bit Number	IOS Bit Number	IOS Paddleboard Location	IOS Paddleboard Pin Number
PU 1,3,5,7	32	D224	DJH6	$U
	33	225		T
	34	226		R
	35	227		Q
	36	228		N
	37	229		M
	38	230		K
	39	231		J
	40	232		H
	41	233		G
	42	234	DJH6	E
	43	235	DJI2	U
	44	236		T
	45	237		R
	46	238		Q
	47	239		N
	48	240		M
	49	241		K
	50	242		J
	51	243		H
	52	244		G
	53	245	DJI2	E
	54	246	DJJ2	U
	55	247		T
	56	248		R
	57	249		Q
	58	250		N
	59	251		M
	60	252		K
	61	253		J
	62	254		H
	63	D255		G
PU 1,3,5,7		Strobe	DJJ2	E