TOSHIBA

Functional Specification

T200 / T250

東京芝浦電気株式会社
TOSHIBA CORPORATION
TOKYO JAPAN

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FUNCTIONAL SPECIFICATION

ON DATA PROCESSING SYSTEM T200/T250

Revision A Sept. 9, 1981

TOSHIBA CORPORATION

PREFACE

This hardware specification of the T200/T250 is divided into two parts: Part I and Part II.

Part I describes the hardware specification of the CPU board (T2CPU).

Part II describes the hardware specification of the CCM board (ETCCM).

The T200/T250 has an extended memory version on which 63 K CP/M can run. The memory configuration of the extended memory version will be discussed in APPENDIX C.

ABBREVIATIONS

The following abbreviations are used in this documents.

ACK	:	ACKNOWLEDGE
CCM	:	Communication Control Module
CRTC	:	CRT Display Controller
FDC	:	Floppy Disk Controller
dec	:	Decimal expression
H	:	Hexadecimal expression
KBC	:	Keyboard Controller
REG.	:	REGISTER

NOTICES

Notel: In this document, the followings are assumed.

(1) "0" means electrically low level of signal lines.
(2) "1" means electrically high level of signal lines.
(3) $\overline{XXX}$ means that signal $\overline{XXX}$ is true when it is in electrically low level.
(4) XXX means that signal XXX is true when it is in electrically high level.
(5) XXX;100 means that signal XXX is true when it is in electrically high level.
(6) XXX;000 means that signal XXX is true when it is in electrically low level.

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Part I

1. GENERAL INFORMATION

1.1 Scope

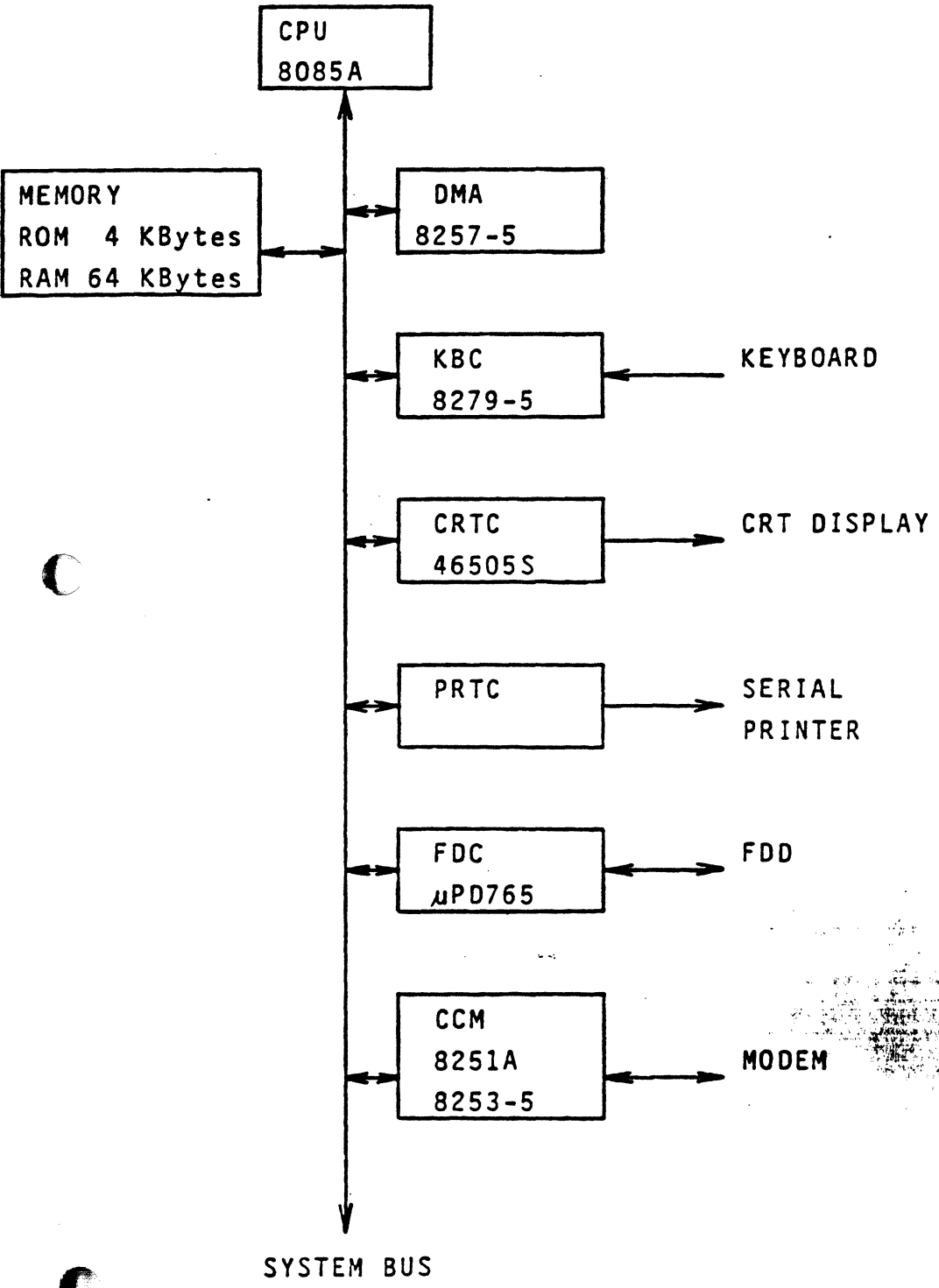
This part describes the hardware specification of the T200/T250 CPU board (T2CPU).

1.2 Features

The CPU board is composed of the followings:

microprocessor	8085A
memory address space	64 KBytes
keyboard interface	BP100 (Toshiba business personal computer) compatible
printer interface	parallel interface
floppy disk interface	FDC (Floppy Disk Controller) on the daughter board can control up to two four? 5.25-inch or 8-inch floppy disk drives, respectively. An analog type of VFO circuit is used.
CRT interface	reverse function that can be realized by hardware. EWP (Toshiba English Word Processor) compatible.
CCM interface	CCM is mounted on the CCM board that is compatible with the above EW-100. RS-232-C interface.

ARDWARE CONFIGURATION



3. CPU AND MEMORY

The Toshiba TMP8085A, 8-bit microprocessor (intel 8085A compatible), is used as a CPU. The clock cycle of the CPU is 375 ns (about 2.66 ~~2.67~~ MHz).

The memory capacity is 64 KBytes in which 4 KBytes are ROM area and others are RAM area. The program, however, can select either ROM area or RAM area for the first 4 KBytes of the memory address space (0000H-0FFFH). The last 2 KBytes of the memory address space can be used as either the refresh memory (video RAM) of 2 KBytes for a CRT display or the character generator (Video Pattern Generator ... VPG) of 2 KBytes by using memory bank selection.

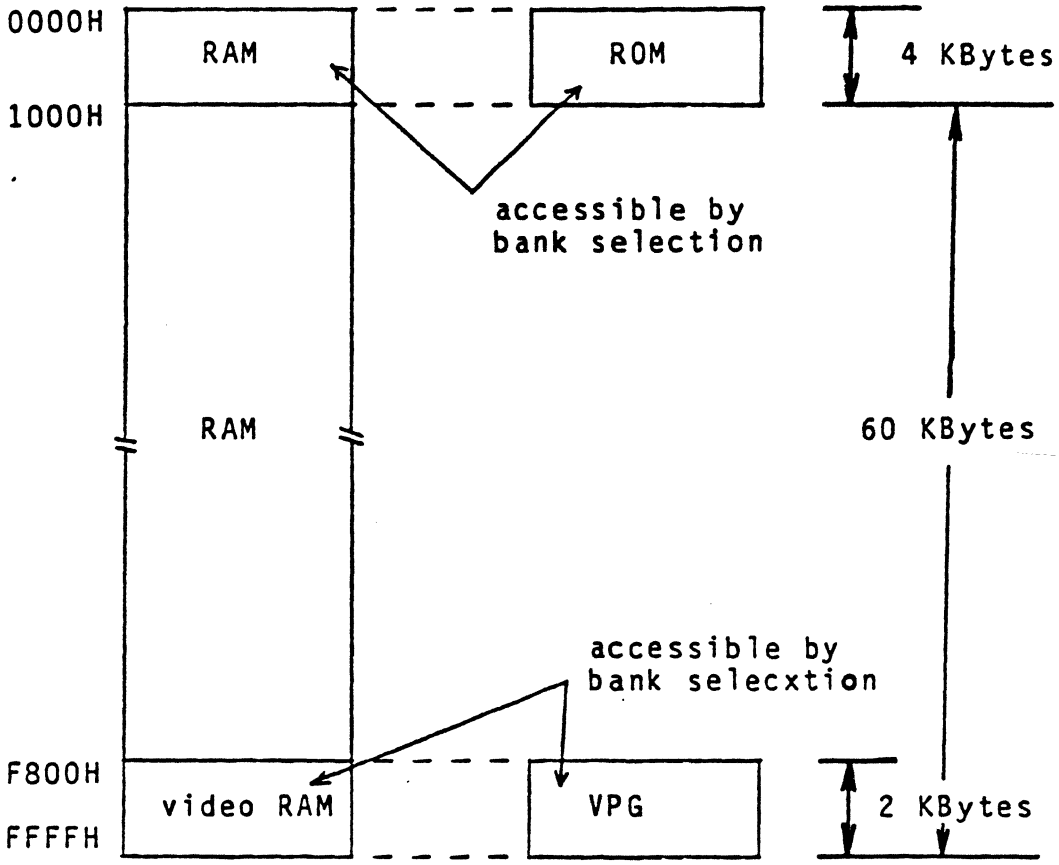
The 4Kx8 bit E-PROM (intel 2732 compatible) and 16Kx1 bit D-RAM (Toshiba TMM416D compatible) can be used as ROM and RAM, respectively. The 2Kx8 bit S-RAM (Toshiba TMM2016P compatible) can be also used as video RAM and VPG.

The refresh cycle of D-RAM is 2.0 ms/128 cycles, which is executed during T3 and T4 of the instruction fetch cycle.

The access to S-RAM needs 2 wait cycles to avoid the conflicts with CRT refresh.

Memory configuration is shown in Fig. 3.1.

Fig. 3.1. Memory Configuration



3.1 Interrupts

The followings are used as interrupts.

IRO ---- highest priority
TRAP
RST7.5
RST6.5
RST5.5 ---- lowest priority

The priority of these interrupts is ordered as shown above.

1. IRO — Jump to the memory location 0000H. This interrupt is generated by the reset signal from either power up or the console.

2. TRAP — Jump to the memory location 0024H. This interrupt is generated by the interrupt signal from the console.

3. RST7.5 — Jump to the memory location 003CH. This is the timer interrupt which is generated by 20 Hz clock divided the horizontal sync. signal for the CRT display by three.

4. RST6.5 — Jump to the memory location 0034H. This is generated by any interrupt request signal other than that from the FDC. The interrupt request is tested by reading the I/O port (D0H).

5. RST5.5 — Jump to the memory location 002CH. This is the interrupt from the FDC. It is generated by the termination of command execution and the status change of disk drives.

4. I/O ADDRESS

I/O ADDRESS	NAMES	I/O PORT
8XH	DMAC	D M A CONTROLLER
9XH	KBC	KEYBOARD CONTROLLER
AXH	CCM	C C M INTERFACE
BXH	CCM	Reserved
CXH	I/O W	I/O WRITE REGISTER
DXH	I/O R	I/O READ REGISTER
EXH	CRTC	C R T CONTROLLER
FXH	FDC	F D D CONTROLLER

X means 0 through F.

4.1 DMAC (8XH) 8257-5

REGISTER SELECTION

I/O ADDRESS	R/W	REGISTER
80H	R/W	CH0 DMA ADDRESS REG.
81H	R/W	CH0 TERMINAL COUNT REG.
82H	R/W	CH1 DMA ADDRESS REG.
83H	R/W	CH1 TERMINAL COUNT REG.
84H	R/W	CH2 DMA ADDRESS REG.
85H	R/W	CH2 TERMINAL COUNT REG.
86H	R/W	CH3 DMA ADDRESS REG.
87H	R/W	CH3 TERMINAL COUNT REG.
88H	W	MODE SET COMMAND
	R	STATUS REG.

CH0 is used for Memory block transfer (Memory Read)
CH1 Memory block transfer (Memory Write)
CH2 FDD data transfer
CH3 Reserved

4.1.1 DMA Address Register (80H, 82H, 84H)

This register specifies the memory address from which the data transfer starts. The memory address of 16 bit is loaded to the register separately, that is, upper half address and lower half address.

	MSB							LSB
F/L=0	A7	A6	A5	A4	A3	A2	A1	A0
F/L=1	A15	A14	A13	A12	A11	A10	A9	A8

NOTE : F/L means First/Last flip flop.
F/L=0 can be performed by the mode set command. After then, F/L=0 and 1 can be selected alternatively every register selection.

4.1.2 Terminal count register (81H, 83H, 85H)

This register specifies the byte counts of transfer data and the transfer mode. The data of 16 bit is loaded to the register separately, that is, upper half byte data and lower half byte data.

	MSB							LSB
F/L=0	C7	C6	C5	C4	C3	C2	C1	C0
F/L=1	Rd	Wr	C13	C12	C11	C10	C9	C8

If the TC STOP bit is set to "1", a channel is disabled after the Terminal Count (TC) output goes true ("0"), thus automatically preventing further DMA operation on that channel. Namely, DMA operation neglects the unexpected DMA request from peripheral devices.

In the ROTATING PRIORITY mode, the priority of the channels has a circular sequence. After each DMA cycle, the priority of each channel changes. The channel which had just been serviced will have the lowest priority. In the memory block transfer, the ROTATING PRIORITY must be set to "1".

ENABLE CH0 to CH3 enables DMA transfer for each channel.

Mode set command are shown as follows:

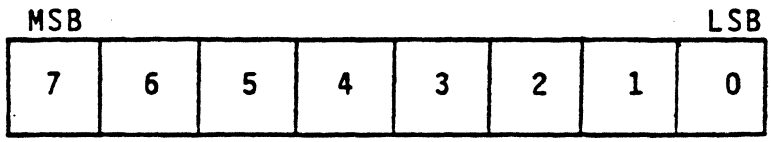
Memory Block Transfer	73H
FDD Data Transfer	64H
Memory from/to FDD Transfer	77H

The Rd and Wr specify the transfer mode as follows.

Rd	Wr	
0	0	Verify mode
0	1	Memory Write mode
1	0	Memory Read mode
1	1	Illegal

C0 through C13 specifies (the transfer byte counts -1).

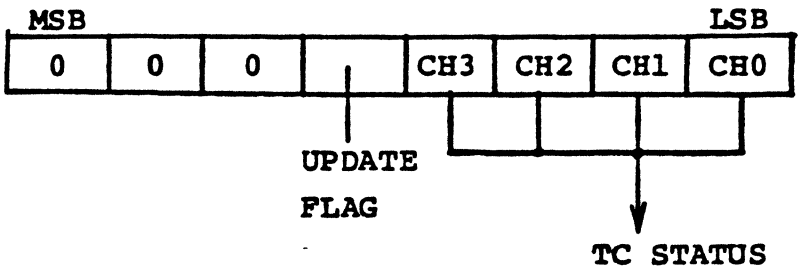
4.1.3 Mode Set Command (88H)



Bit 7 : AUTO LOAD (must be set to "0")
6 : TC STOP
5 : EXTENDED WRITE (must be set to "1")
4 : ROTATING PRIORITY
3 : ENABLE CH3
2 : ENABLE CH2
1 : ENABLE CH1
0 : ENABLE CH0

4.1.2 Status Register (~~86H~~ C8)

The status register indicates whether the data transfer has terminated or not.



If a TC STATUS bit has been set to "1", it indicates that the data transfer for that channel has already terminated.

.2 KBC (9XH) 8279-5

Register selection

I/O ADDRESS	R/W	REGISTER
90H	W	Reserved
	R	Key input data
91H	W	Control command
	R	Status

.2.1 Control Command (91H)

(1) MODE SET

MSB							LSB
0	0	0	0	0	0	1	0

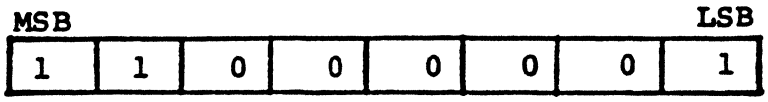
This indicates the coded N-key rollover mode.

(2) INTERNAL CLOCK SET

MSB							LSB
0	0	1	1	1	1	1	0

This indicates that the internal clock (100KHz) is generated by dividing the external clock input (2.66MHz) of the 8279-5 (Keyboard Controller).
2.67

(3) CLEAR COMMAND



This indicates to clear the key-input data which remains in the FIFO* of the 8279-5. Then, the keyboard interrupt is also reset.

* FIFO : First-In, First-Out register.

4.2.2 STATUS (91H)

MSB							LSB
		O	U	F	N	N	N

O = "1" (ERROR OVER RUN)
This occurrs by the next key-input when the FIFO is full.

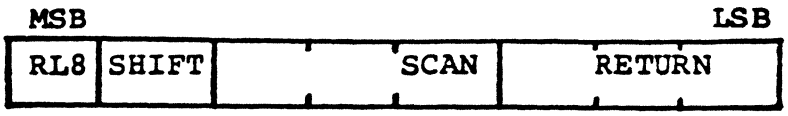
U = "1" (ERROR UNDER RUN)
This occurs when the CPU reads the empty FIFO.

F = "1"
This means the full FIFO.

NNN This means the number of characters in the FIFO.

The FIFO consists of 8-byte register.

4.2.3 Key Input Data (90H)



When reading this key input data, the keyboard switch status register (D1H) must be simultaneously read to check if the CTRL key or REPT key has been depressed or not.

This reading operation must be performed only when the interrupt from the keyboard is generated. In other cases, all the data will be "0" and the status becomes ERROR UNDER RUN.

Since the number of return lines is eleven, the return code (RETURN 000, 001, 010) for RL0, RL1, and RL2 may be the same as that for RL8, RL9, and RL10. To discriminate them, if the RL8 of the key input data (MSB) is "0", it means the return code for RL0, RL1, and RL2. Otherwise, it means that for RL8, RL9, and RL10.

SHIFT : This bit is "1" when the SHIFT key has been depressed.

RL8 : This bit is "1" when the keys, which are located within the block controlled by the line RL8, have been depressed.

4.3 CCM (AXH)

Register selection

I/O ADDRESS	R/W	REGISTER
A0H	R/W	8253-5 COUNTER #0
A1H	R/W	8253-5 COUNTER #1
A2H	R/W	8253-5 COUNTER #2
A3H	W	8253-5 CONTROL
A4H	R/W	8251A DATA
A5H	R/W	8251A CONTROL/STATUS
A6H	R/W	CCM MODE REG.
A7H	R	CCM STATUS REG.

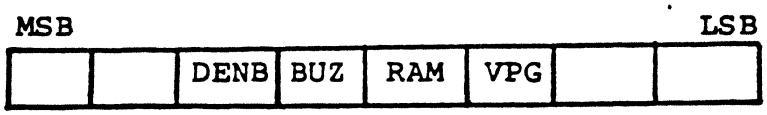
For the usage of each register, refer to the Part II in this document.

4.4 I/O W (CXH)

Register selection

I/O ADDRESS	R/W	REGISTER
C0H	W	MODE REGISTER
C1H	W	DATA REGISTER
C2H	W	COMMAND REGISTER
C3H	W	PRINTER ACK INTERRUPT RESET

4.4.1 Mode Register (C0H)



DENB(bit5) DISPLAY ENABLE

Setting this bit to "1" enables the display. The blink operation for the display message is performed by setting this bit to "1" or "0" alternatively.

BUZ (bit4) BUZZER ON

If this bit is set to "1", the buzzer on the keyboard sounds at about 2KHz.

RAM (bit3) RAM SELECT

If this bit is set to "1",the RAM area is selected for the memory address 0000H through 0FFFH. This bit is set to "0" at turning on the power switch.

VPG (bit2) VPG SELECT

If this bit is set to "1", the VPG area is selected for the memory address F800H through FFFFH. This bit is set to "0" at turning on the power switch.

4.4.2 Data Register (C1H)

MSB							LSB
DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0

The print-out data to the printer is set in this register.

4.4.3 Command Register (C2H)

MSB							LSB
		0		STEP INT. ON		PRT STB	PRT RESET

STEP INT. ON (bit3) — The interrupt request of RST6.5 can be generated by setting this bit to "1".

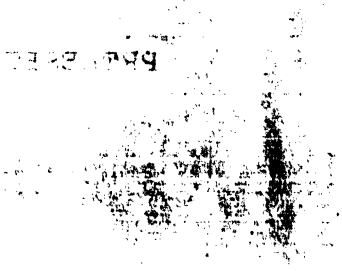
(bit2) — Reserved

PRTSTB (bit1) — This bit is set to "1" to generate the STROBE PULSE to the printer. Thus, this bit must have been set more than 1 microsecond.

PRTRESET (bit0) — This bit is set to "1" to generate the internal reset signal to the printer.

4.4.4 PRINTER ACK INTERRUPT RESET (C3H)

PRT ACK (Printer acknowledge signal) is set at the falling edge of the ACK signal from the printer and generates the interrupt. This port resets the interrupt request of the PRT ACK signal.



4.5 I/O R (DXH)

Register selection

I/O ADDRESS	R/W	REGISTER
D0H	R	INTERRUPT REGISTER
D1H	R	KB SWITCH STATUS REGISTER
D2H	R	SWITCH REGISTER
D3H	R	I/O STATUS REGISTER

4.5.1 INTERRUPT REGISTER (D0H)

MSB							LSB
$\overline{\text{KBI}}$	$\overline{\text{Tx RDY}}$	$\overline{\text{Rx RDY}}$	$\overline{\text{PRT ACK}}$	1	1	1	$\overline{\text{STEP CONT}}$

$\overline{\text{KBI}}$ (bit7) KEYBOARD INTERRUPT
This bit is set to "0" when the data is stored in the FIFO of KBC and reset by reading the data.

$\overline{\text{TxRDY}}$ (bit6)
$\overline{\text{RxRDY}}$ (bit5)
} INTERRUPT from the CCM

This bit is set to "0" when the USART (8251A) requests the data transfer.

$\overline{\text{PRT ACK}}$ (bit4) PRINTER ACK
This bit is set to "0" by the falling edge of PRTACK and reset by writing the I/O port (C3H). Since the status of this bit is uncertain at turning on the power switch, this bit should be reset before the first EI (Enable Interrupt) instruction is executed.

$\overline{\text{STEPCONT}}$ (bit0) STEP CONTROL
This interrupt request can be generated when setting the bit 3 of the port (C2H) by the software. At turning on the power switch, This bit is always "0".

4.5.2 KB SWITCH STATUS (D1H)

MSB LSB

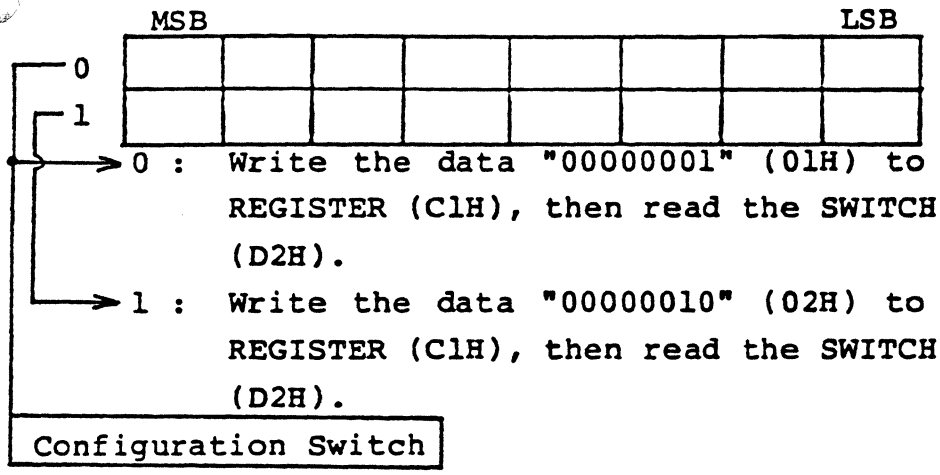
$\overline{KRP}$	1	$\overline{CTRL}$	1	$\overline{KB3}$	$\overline{KB2}$	$\overline{KB1}$	$\overline{KB0}$

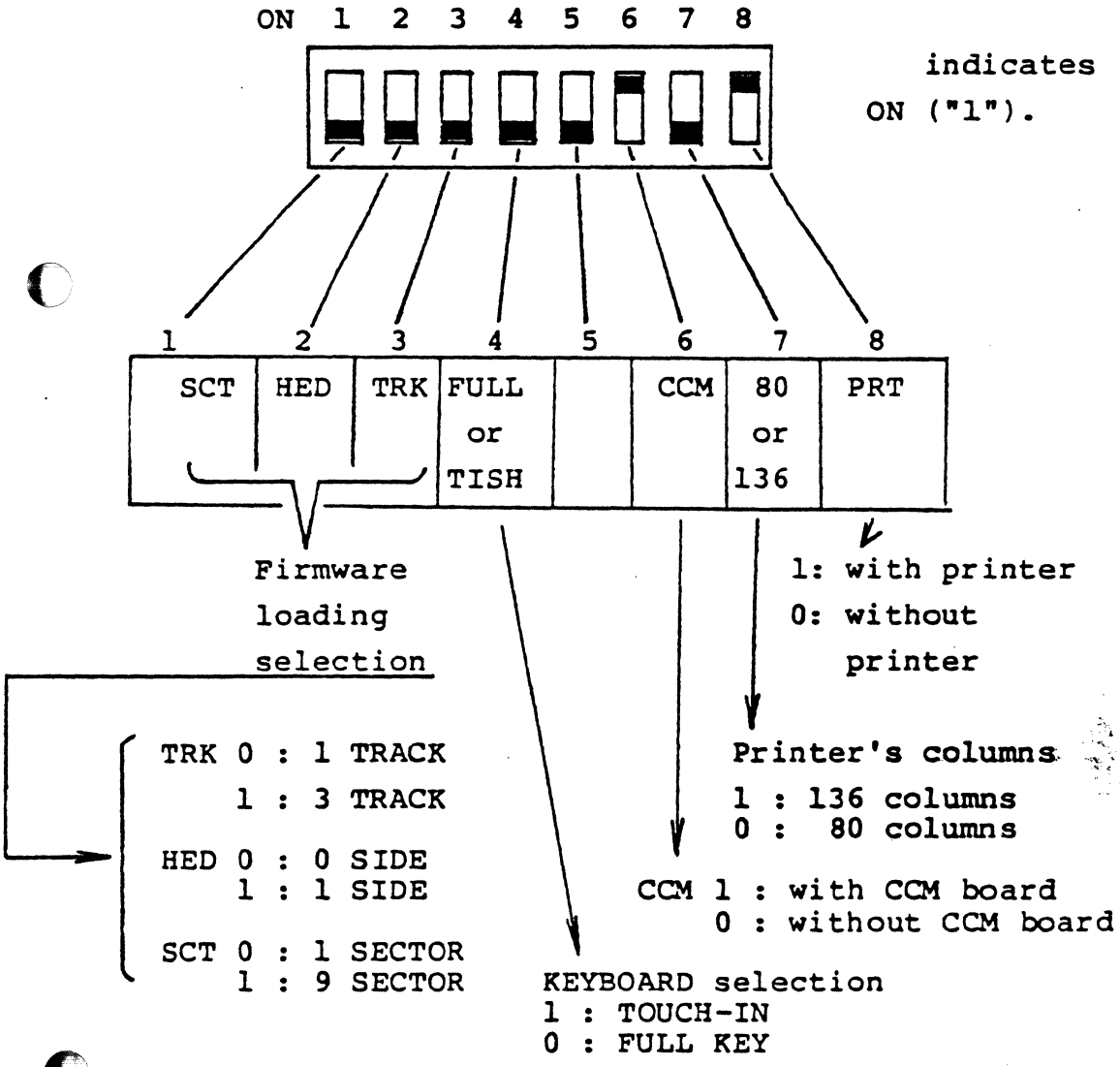
$\overline{KRP}$ (bit7) KB PEPEAT REQUEST
This flag bit can be set to "0" when the both REPEAT KEY and DATA KEY have been being depressed together. This can be reset by a status read operation.

$\overline{CTRL}$ (bit5)
This flag bit is set to "0" when the CTRL KEY has been depressed.

$\overline{KB0}$ - $\overline{KB3}$ (bit0 - 3)
KB status (Reserved for the future use)

4.5.3 SWITCH REGISTER (D2H)





5.4 I/O STATUS REGISTER (D3H)

MSB							LSB
$\overline{CI}$	$\overline{CTS}$		PRT SLCT	PRT BSY	PRT LD	PRT PE	PRT $\overline{FAULT}$

$\overline{CI}$	(bit7)	CI signal of CCM status
$\overline{CTS}$	(bit6)	CTS signal of CCM status
	(bit5)	Reserved
PRT SLCT	(bit4)	SELECT signal of the printer (selected state)
PRT BSY	(bit3)	BUSY signal of the printer (busy state)
PRT LD	(bit2)	LD signal of the printer (printer clock stop) NOT USE
PRT PE	(bit1)	PAPER ALART signal of the printer (almost paper empty of the printer)
PRT $\overline{FAULT}$	(bit0)	FAULT signal of the printer (error status) If both bit2 and bit4 is "1", this bit becomes "0".

4.6 CRTC (EXH) 46505S

Register selection

I/O ADDRESS	R/W	REGISTER
E0H	W	ADDRESS REGISTER
	R	NOT USE
E1H	W	CONTROL REGISTER (R0 - R17)
	R	CONTROL REGISTER (R14 - 17)

R0 - R17 means the register number in the CRTC.
For the details on the CRTC, refer to the APPENDIX. A "CRT DISPLAY CONTROLLER"..

4.6.1 ADDRESS REGISTER

MSB							LSB
			2^4	2^3	2^2	2^1	2^0

In the above register (bit 0 - 4) should be set the address (0 - 17dec) of the internal control registers. If the address (18 - 31dec) is set, it is neglected. The address of the prespecified control register should be written in the above register before writing/reading the data to/from that register (R0 - R17).

4.6.2 CONTROL REGISTER

The control register is used to specify the parameters that controls the CRT display timing and so on as shown in Table 4.1. In that register, R0 through R13 should be set before starting display. R14 and R15 are used to specify the cursor display position, so the initial setting for them are not necessarily required. If both R14 and R15 are set to 00H, the cursor is displayed at the upper-left corner on the screen.

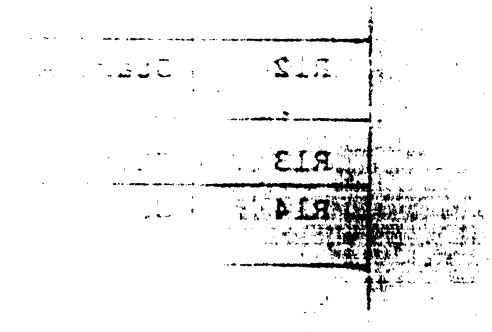


Table 4.1 CRTC Control Register

REGISTER	NAME	DESCRIPTIONS	DATA BIT(HEX)
R0	Total Number of Horizontal Characters		65
R1	Number of Horizontal Displayed Characters	80 characters	50
R2	Horizontal Sync. Position		52
R3	Horizontal Sync. Pulse Width		0A
R4	Total Number of Vertical Characters		19
R5	Total Raster Adjust		02
R6	Number of Vertical Displayed Characters	24 lines	18
R7	Vertical Sync. Position		18
R8	Interlace mode and Skew set		50
R9	Maximum Raster Address	10	09
R10	Cursor Start Raster		09
R11	Cursor End Raster		09
R12	Start Address(H)	0000H	00
R13	Start Address(L)		00
R14	Cursor(H)	any value	
R15	Cursor(L)		
R16	Light Pen(H)	NOT USE	
R17	Light Pen(L)	NOT USE	

4.7 FDC (FXH)

Register selection

I/O ADDRESS	R/W	REGISTER
F0H	R	FDC STATUS REGISTER READ
	W	FDD CONTROL COMMAND
F1H	R	FDC DATA REGISTER READ
	W	FDC DATA REGISTER WRITE

For the details on the FDC, refer to the APPENDIX. B "FLOPPY DISK CONTROLLER".

4.7.1 FDD CONTROL COMMAND (F0H)

(1) In case of 5.25-inch floppy disk drive,

MSB							LSB
RST	MON	PC1	PC0				

RST : FDC RESET at "1"
MON : FDD MOTOR ON at "1"
PC1 : W.DATA 500ns precompensation at "1"
PC0 : W.DATA 250ns Precompensation at "1"

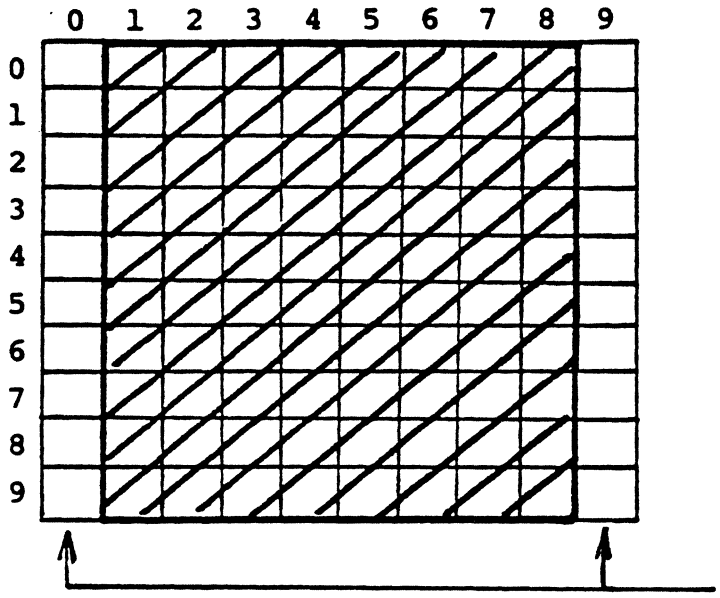
(2) In case of 8-inch floppy disk drive,

MSB							LSB
RST			SFL				

RST : FDC RESET at "1"
SFL : SWITCH FILTER ON at "1"

5. HARDWARE FUNCTION

5.1 Display Character Font



Character matrix 10x10 dots
Display area 8x10 dots

Since the character generator (VPG) is composed of S-RAM, any character can be displayed within the display area (8x10 dots).

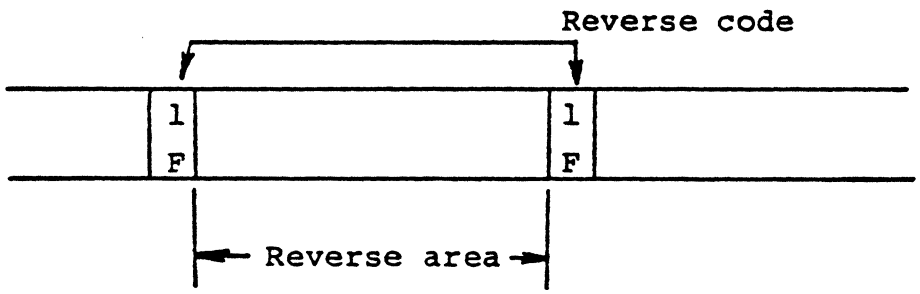
The number of display character fonts : 128 fonts

5.2 Reverse Function

The reverse function is effective from the first data 1FH to the next 1FH or to the last column of the last row.

Reverse code(1FH) cannot be displayed.

All characters and cursor can be displayed reversed within the reverse area.



Part II

6. GENERAL INFORMATION

6.1 Scope

This part describes the hardware specifications of the T200, T250 and EW-100 CCM boards, which conform to the EIA RS-232-C standard.

6.2 Features

The CCM board consists of the following components:

* Intel 8251A compatible USART(Universal Synchronous/Asynchronous Receiver/Transmitter)
* Intel 8253 compatible Timer
* Additional electronic circuits

(1) Modem interface: RS-232-C

(2) Communication mode: ASYNC(including direct connection)
SYNC(modem clock)
SYNC(internal clock)
SYNC(direct connection)

(3) Data transmission rate:

ASYNC: 110, 150, 300, 600, 1200, 2400, or 4800bps

SYNC(Modem clock, direct connection): 1200, 2400, 4800, or 9600bps

SYNC(Internal clock): 1200bps

(4) Half-duplex transmission:

In case of ASYNC, ASCII code system(7-bit data + 1-bit parity) is used.

(5) Physical specifications:

* PCB(Printed Circuit Board) 5.45 x 6.75 inches

* Connector CPU side:
  40 PIN Header(EW-100)
  50 PIN Header(T200/T250)

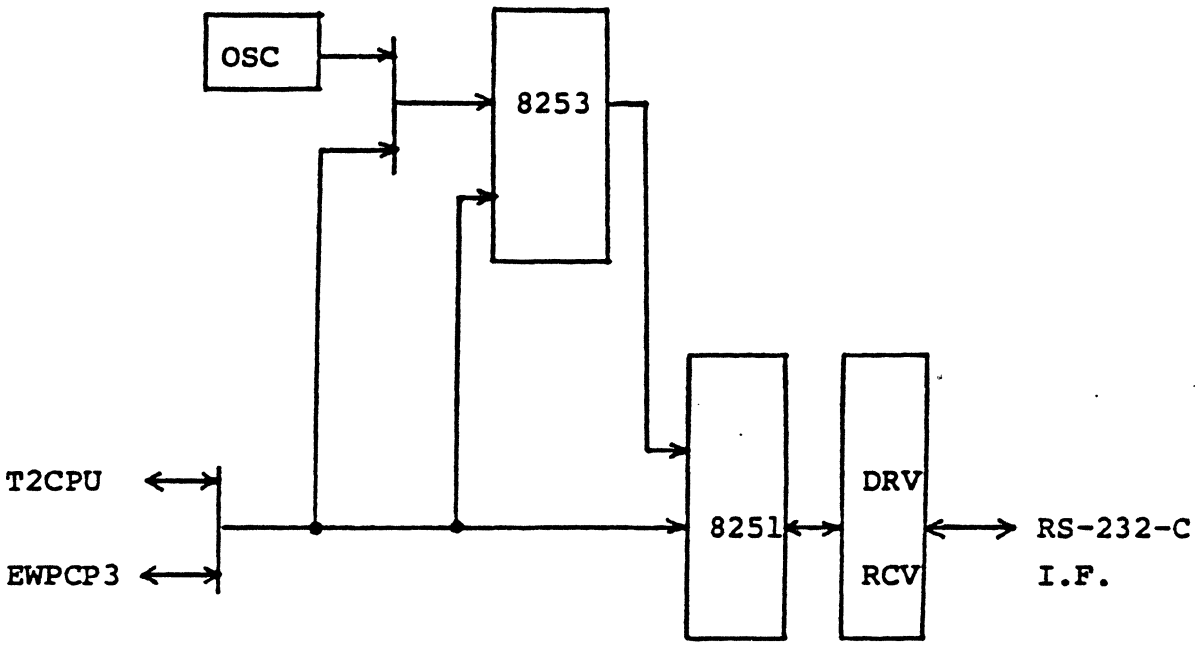
  Modem side: 26 PIN Header

* Power supply: DC +12V 0.1A max
  -12V 0.1A max
  + 5V 0.5A max

* CCM cable: 3m cable for the standard
  (15m cable for direct connection)

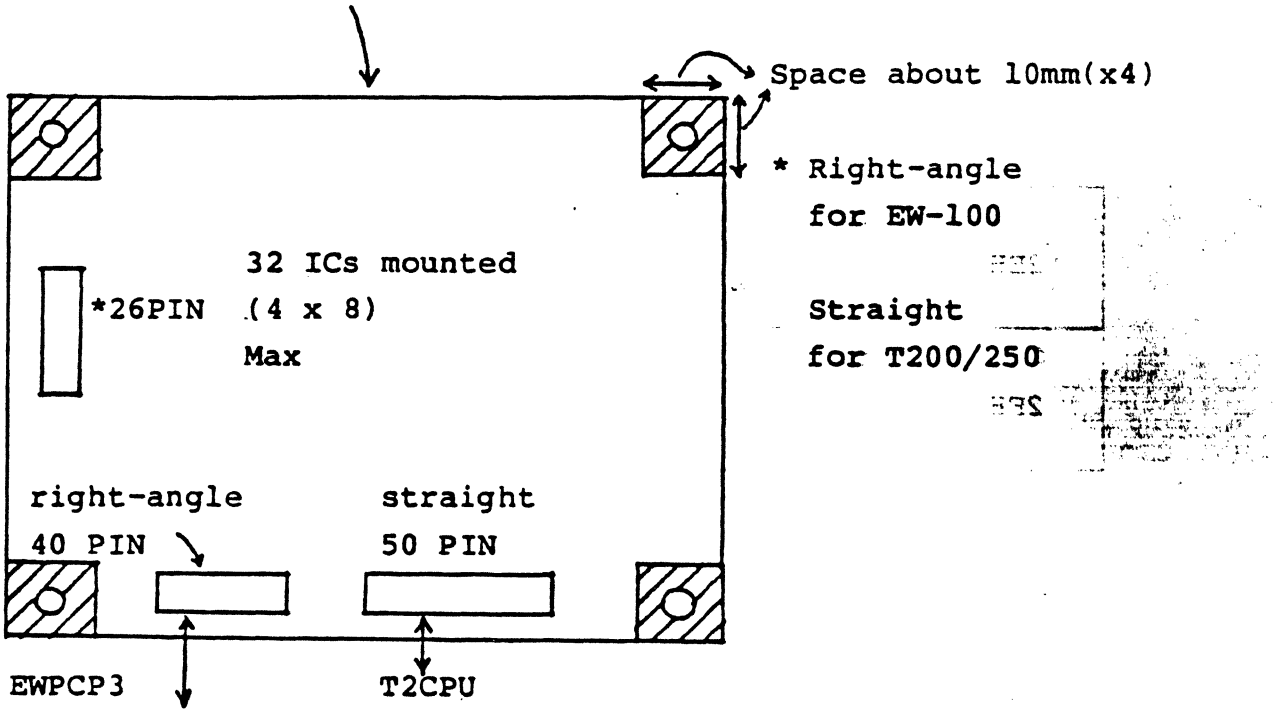
(6) This board can be used to connect I/O devices such as Modem, OCR-V100, and serial printer(serial interface) which have the RS-232-C interface.

6.3 Block Diagram



6.4 Physical Requirements

34P778221G01 for T200/T250
34P778221G02 for EW-100



7. SOFTWARE INTERFACE SPECIFICATION

.7.1 I/O Port Address

EW-100	T200/T250	R/W	Function
28H	A0H	R/W	8253-5 COUNTER #0
29H	A1H	R/W	8253-5 COUNTER #1
2AH	A2H	R/W	8253-5 COUNTER #2
2BH	A3H	W	8253-5 CONTROL
2CH	A4H	R/W	8251A DATA
2DH	A5H	R/W	8251A CONTROL/STATUS
2EH	A6H	R/W	CCM MODE REG.
2FH	A7H	R	CI/CTS

Note 1: I/O ports(A8 - BFH) of T200/T250 must not be used.

Note 2: TxRDY(Transmitter ready) and RxRDY(Receiver ready) signals generated by 8251A USART cause I/O interrupt RST6.5 for the CPU.

-5 (Timer)

COUNTER #2 only is used in ASYNC mode.

CONTROL Mode 3 and binary count should be specified(Square wave rate generator).

DATA

Baud rate bps	Decimal value to be set
110	1135
150	832
300	416
600	208
1200	104
2400	52
4800	26

In ASYNC mode, the clock input of 8253-5 is the same one as that in SYNC mode.

Baud	Value
50	2497
75	1665
134.5	928
450	277
9600	13
19,200	6

(2) SYNC

Programs are not required in SYNC(modem clock) mode.

(3) In SYNC(internal clock; direct connection) mode, the internal registers of 8253-5 should be set as follows.

CONTROL

COUNTER #0	Mode 1 should be specified (programmable one-shot)
COUNTER #1	ditto
COUNTER #2	Mode 2 should be specified (Square wave rate generator).

In either case, the binary count should be specified.

DATA

Baud rate (bps)	Decimal value to be set		
	COUNTER #0	COUNTER #1	COUNTER #2
1200	624	728	104
2400	312	364	52
4800	156	182	26
9600	78	91	13

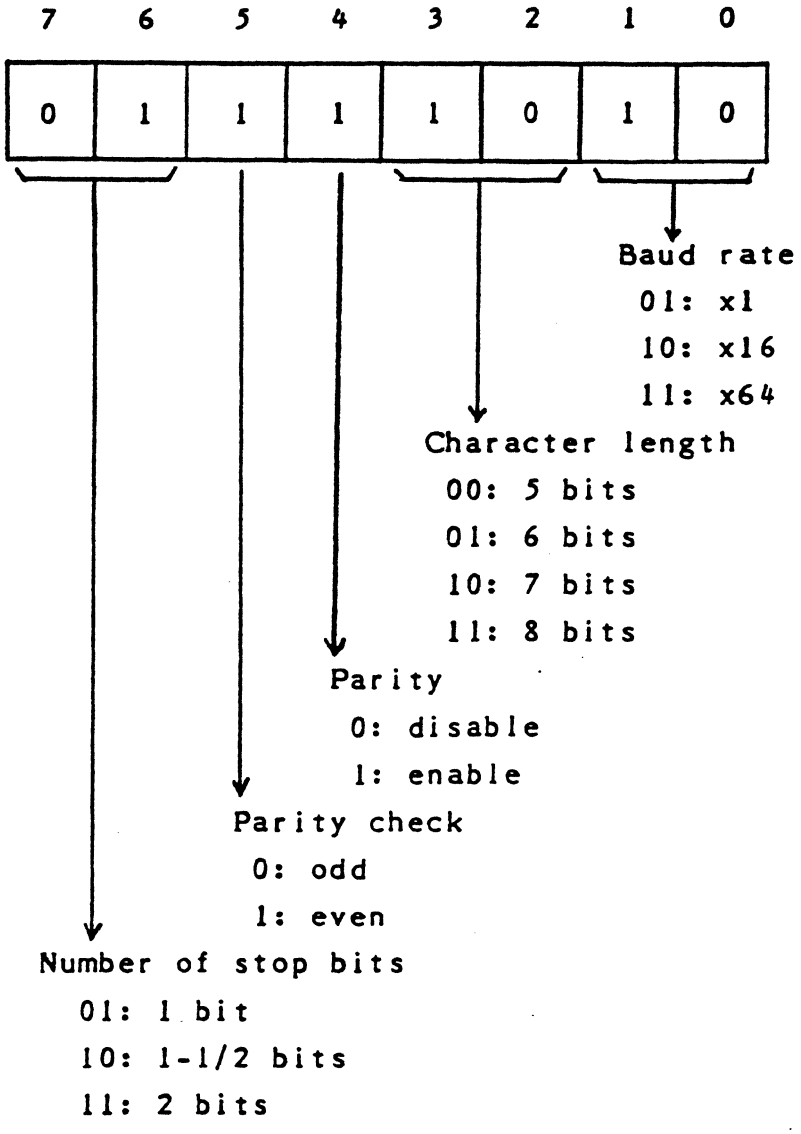
Note 1: In SYNC mode, the clock input to 8253-5 is 1.9968 MHz(divided the output of oscillator 15.9744 MHz by eight).

Note 2: COUNTER #0: N x 3/8,
COUNTER #1: N x 7/16,
COUNTER #2: N x 16,
where N means transmission rate.

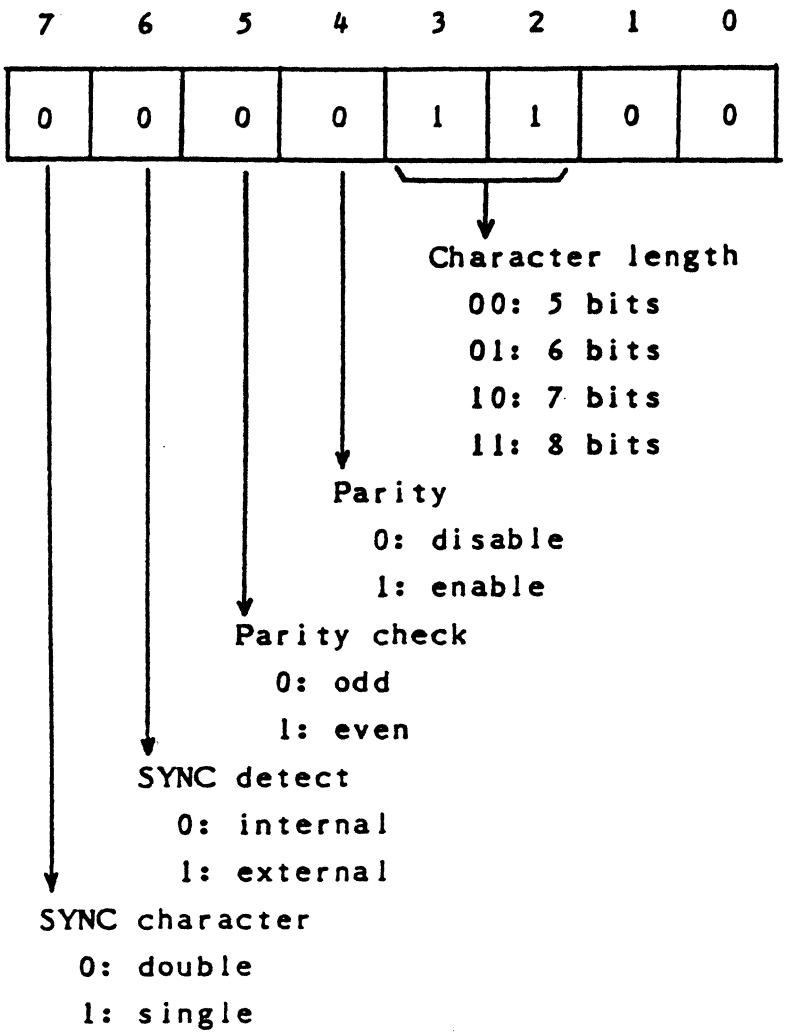
7.3 8251A (USART)

(1) MODE Instruction

ASYNC



SYNC


7 6 5 4 3 2 1 0
0 0 0 0 1 1 0 0
Character length
00: 5 bits
01: 6 bits
10: 7 bits
11: 8 bits
Parity
0: disable
1: enable
Parity check
0: odd
1: even
SYNC detect
0: internal
1: external
SYNC character
0: double
1: single

(2) COMMAND Instruction

7	6	5	4	3	2	1	0
EH	IR	RTS	ER	SBRK	RxE	DTR	TxEN

EH Enter Hunt mode
1 : Serching for SYNC character

IR Internal Reset
1 : initial setting

RTS Request To Send
1 : $\overline{RTS}$ = 0

ER Error Reset
1 : reset the error flag(PE, OE, FE)

SBRK Send Break
1 : TxD = LOW

RxE Receive Enable
1 : enable
0 : disable

DTR Data Terminal Ready
1 : $\overline{DTR}$ = 0

TxEN Transmit Enable
1 : enable
0 : disable

(3) STATUS

7	6	5	4	3	2	1	0
DSR	SYN DET	FE	OE	PE	TxE	Rx RDY	Tx RDY

DSR Data Set Ready

SYNDET SYNC Character Detect

FE Framing Error(ASYNC only)

OE Overrun Error

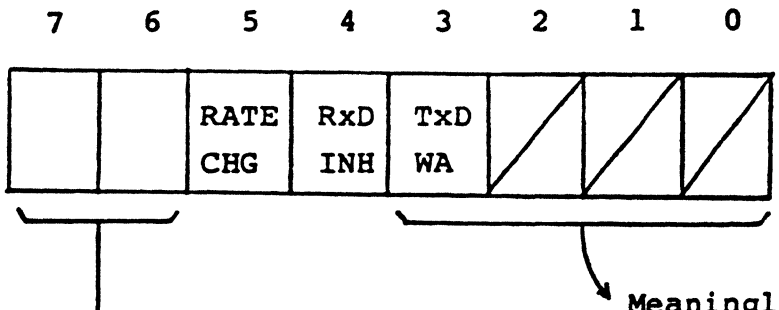
PE Parity Error

TxE Transmitter Empty

RxRDY Receiver Ready

TxRDY Transmitter Ready

7.4 CCM MODE REG.



00: ASYNC
In ASYNC and half-duplex,
when sending, RxDINH should be set to "1" and then TxDWA should be set to "1".
when receiving, TxDWA should be set to "0" and then RxDINH should be set to "0".

01: SYNC(modem clock)

10: SYNC(internal clock)

11: SYNC(direct connection)

RATE CHG: Change the modem speed.
0: NORMAL
1: HALF

RxDINH: inhibit RxD input.

TxDWA: send back internally the transmission data.

7.5 CI/CTS

7	6	5	4	3	2	1	0
$\overline{CI}$	$\overline{CD}$	$\overline{CTS}$	Tx DWA				

CI: Call Indicator

CD: Carrier Detect

CTS: Clear to Send

TxDWA: TxDWA bit of CCM MODE REG.

8. HARDWARE INTERFACE SPECIFICATION

CPU SIDE INTERFACE CONNECTOR (PJ1: EW-100, PJ2: T200)

PJ1	SIGNAL NAME	PJ1	SIGNAL NAME
01	N/C	21	CCMSEL;000
02	GND	22	CCMRD;000
03	+12V	23	CCMWR;000
04	+12V	24	GND
05	+5V	25	GND
06	+5V	26	(NOT USED)
07	GND	27	CCMRST;000
08	CCMD7;100	28	CCMOPI;000
09	CCMD6;100	29	CTXRDY;000
10	CCMD5;100	30	CRXRDY;000
11	CCMD4;100	31	CCLK;000
12	CCMD3;100	32	(NOT USED)
13	CCMD2;100	33	GND
14	CCMD1;100	34	+5V
15	CCMD0;100	35	+5V
16	GND	36	GND
17	GND	37	-12V
18	CCMA02;100	38	-12V
19	CCMA01;100	39	GND
20	CCMA00;100	40	GND

PJ2	SIGNAL NAME	PJ2	SIGNAL NAME
01	N/C	26	CCOMSL;000
02	GND	27	COMCI;100
03	+12V	28	CA02;100
04	+12V	29	COMCTS;100
05	+5V	30	CA01;100
06	+5V	31	GND
07	GND	32	CA00;100
08	CAD0;100	33	GND
09	GND	34	CIOR;000
10	CAD1;100	35	GND
11	GND	36	CRST;000
12	CAD2;100	37	GND
13	GND	38	CIOW;000
14	CAD3;100	39	GND
15	GND	40	CCLK;000
16	CAD4;100	41	GND
17	GND	42	CRXRDY;000
18	CAD5;100	43	GND
19	GND	44	CTXRDY;000
20	CAD6;100	45	+5V
21	GND	46	+5V
22	CAD7;100	47	-12V
23	GND	48	-12V
24	CSYNSL;000	49	GND
25		50	GND

MODEM SIDE CONNECTOR (PJ3, CCM MARK needed)

PJ3	SIGNAL NAME	MODEM D-SUB	
01	N/C	—	
02	TXD;000	02	
03	GND	*07	
04	RXD;000	03	
05	GND	*07	
06	RTS;100	04	
07	GND	*07	
08	CTS;100	05	
09	GND	*07	
10	DTR;100	20	
11	GND	*07	
12	(NOT USED)	—	
13	GND	*07	
14	ST2;100	15	
15	GND	*07	
16	RT;100	17	
17	GND	*07	
18	CD;100	08	
19	GND	*07	
20	DSR;100	06	
21	GND	*07	
22	CI;100	22	
23	GND	*07	(* altogether to 7 PIN)
24	SDS;000	23	
25	GND	*07	
26	ST1;100	24	
		01	Frame GND
		09	NOT USED
		10	
		11	
		12	
		13	
		14	
		16	
		18	
		19	
		21	
		25	

NDIX A

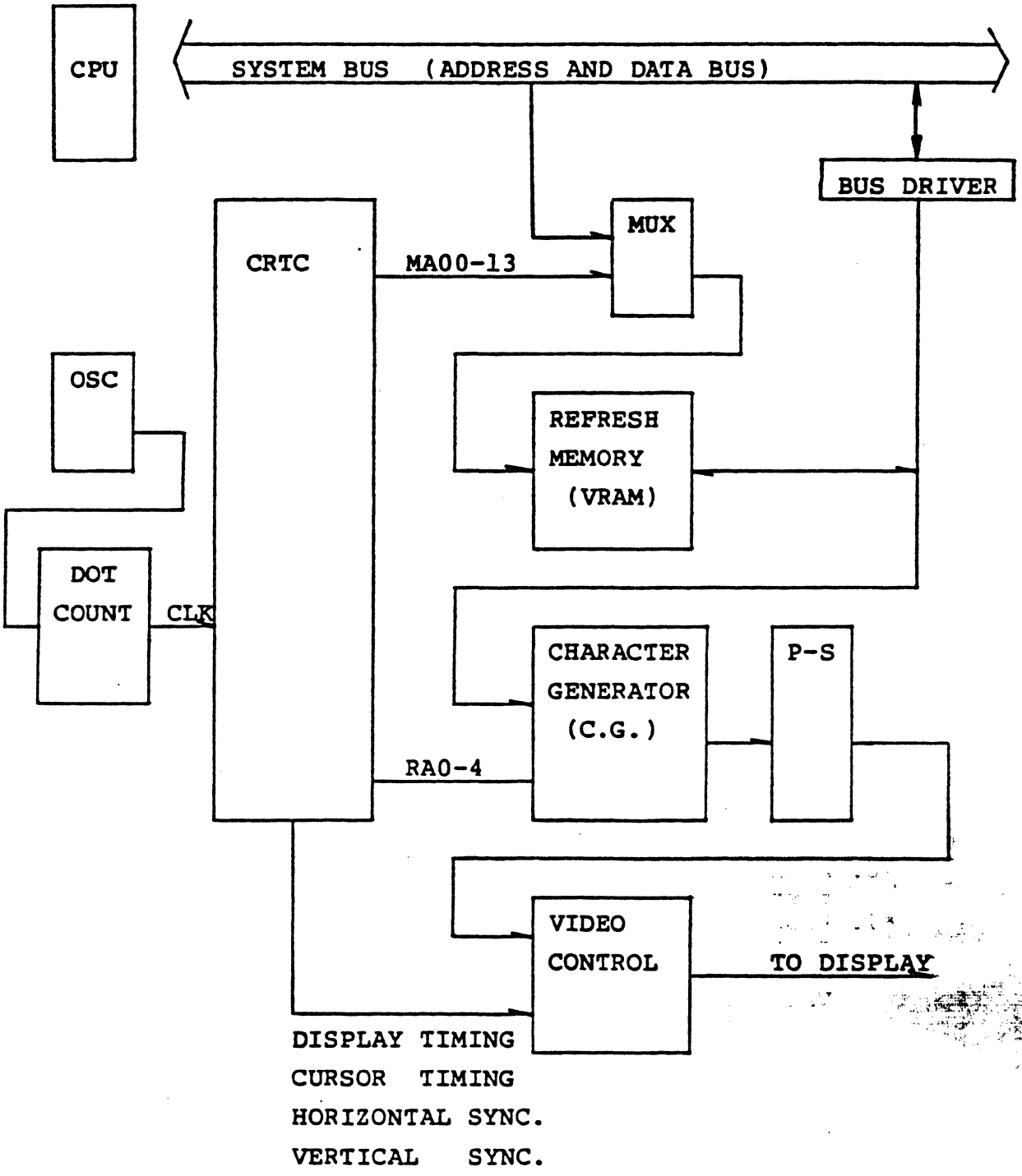
CRT DISPLAY CONTROLLER

DESCRIPTION

HD46505 (CRTC) is a LSI controller which is designed to provide an interface for microprocessor to raster scan type CRT displays.

CRTC is also designed as a programmable controller, so applicable to wide range CRT display from small low-functioning character display up to raster type full graphic display as well as large high-functioning limited graphic display.

SYSTEM CONFIGURATION



INTERNAL REGISTERS

CS	RS	Address Reg. 4	3	2	1	0	Register	R/W	Data Bit 7	6	5	4	3	2	1	0	
1	X	X	X	X	X	X		-	-	-	-	-	-	-	-	-	
0	0	X	X	X	X	X	AR	W	-	-	-						
0	1	0	0	0	0	0	R0 *7	W									*1
0	1	0	0	0	0	1	R1	W									
0	1	0	0	0	1	0	R2 *7	W									
0	1	0	0	0	1	1	R3	W	-	-	-	-					
0	1	0	0	1	0	0	R4 *7	W	-								
0	1	0	0	1	0	1	R5	W	-	-	-						
0	1	0	0	1	1	0	R6	W	-								*2
0	1	0	0	1	1	1	R7 *7	W	-								
0	1	0	1	0	0	0	R8	W	-	-	-	-	-	-	V	S	*3
0	1	0	1	0	0	1	R9 *7	W	-	-	-						*4
0	1	0	1	0	1	0	R10	W	-	B	P						*5
0	1	0	1	0	1	1	R11	W	-	-	-						*6
0	1	0	1	1	0	0	R12	W	-	-							
0	1	0	1	1	0	1	R13	W									
0	1	0	1	1	1	0	R14	R/W	-	-							
0	1	0	1	1	1	1	R15	R/W									
0	1	1	0	0	0	0	R16	R	-	-							
0	1	1	0	0	0	1	R17	R									

Note: *1. When R8 is 1 or 3 (Interlace Mode), programmed data must be odd.

*2. When R8 is 3, N/2 (N: total number of lines)

*3. When S is 1, V specifies video mode. S specifies interlace sync. mode.

*4. When R8 is 3, programmed data must be odd.

*5. B specifies the cursor blink. P specifies the cursor blink period.

16 or 32 Field Period

I Light I Dark I Light I Dark I

*6. When R8 is 3, the cursor start and the cursor end raster registers must be both even or both odd.

*7. Programmed Value = Specified Value - 1
In the following explanation, for instance, total number of horizontal characters means "Specified Value".

INTERNAL REGISTERS

AR: Address Register

This is a 5-bit register used to select 18 internal control registers (R0-R17). It is contents are the address of one of 18 internal control registers. Programming the data from 18 to 31 produces no results. Access to R0-R17 requires, first of all, to write the address of corresponding control register into this register. When RS and CS are at low level, this register is selected.

R0: Total Number of Horizontal Character Register

This is a register used to program total number of horizontal characters per line including the fly back period. The data is 8-bit and its value should be programmed according to the specification of CRTC. When M is total number of characters, (M-1) shall be programmed to this register. When programming for interlace mode, M must be even.

R1: Number of Horizontal Displayed Characters Register

This is a register used to program the number of horizontal displayed characters per line. Data is 8-bit and any number that is smaller than that of total horizontal characters can be programmed.

INTERNAL REGISTERS

R2: Horizontal Sync. Position Register

This is a register used to program horizontal sync. position in unit of horizontal character time. Data 8-bit and any number that is under the following condition (Horizontal Sync. Position + Horizontal Pulse Width $\leq$ Total Number of Horizontal Characters) can be programmed. When H is character number of horizontal sync. position, (H-1) shall be programmed to this register. When programmed value of this register is increased, the display position on the CRT screen is shifted to the left. When programmed value is decreased, the position is shifted to right. Therefore, the optimum horizontal position can be determined by this value.

R3: Horizontal Sync. Pulse Width Register

This is a register used to program horizontal sync. pulse width from 1 to 15 in unit of horizontal character time. Note that when 0 is programmed, HSYNC is not provided.

R4: Total Number of Vertical Characters Register

This is a register used to program total number of lines per frame including vertical fly back period. The data is within 7-bit and its value should be programmed according to the specification of CRTC. When N is total number of lines, (N-1) shall be programmed to this register.

R5: Total Raster Adjust Register

This is a register used to program the optimum number from 0 to 31 to adjust total number of raster per frame. This register enables to decide the number of vertical deflection frequency more strictly.

R6: Number of Vertical Displayed Characters Register

This is a register used to program the number of displayed character rows on the CRT screen. Data 7-bit and any number that is smaller than that of total vertical characters can be programmed.

R7: Vertical Sync. Position Register

This is a register used to program the vertical sync. position on the screen in unit of horizontal character time. Data 7-bit and any number that is equal to or less than total number of vertical characters (V-1) shall be programmed to this register. When programmed value of this register is increased, the position is shifted down. Therefore, the optimum vertical position may be determined by this value.

R8: Interlace Mode Register

This is a 2-bit register used to control the raster scan mode.

2^1	2^0	Mode
0	0	Non-Interlace Mode
0	1	Non-Interlace Mode
1	0	Interlace Sync. Mode
1	1	Interlace Sync. and Video Mode

In non-interlace mode, the rasters of even number field and odd field are scanned in the middle of even number field. Then it is controlled to display the same character pattern in two fields. In interlace sync. video mode, the raster scan method is the same as that in interlace sync. mode, but it is controlled to display different character pattern in two fields.

R9: Maximum Raster Address Register

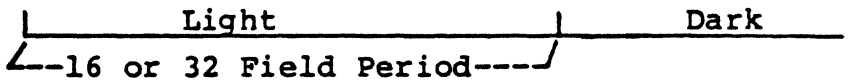
This is a register used to program maximum raster address within 5-bit. This register defines total number of rasters per character including spacing. When total number of rasters is RN, (RN-1) shall be programmed to this register. Moreover, when programmed value of R8 is 3, RN must be even.

R10: Cursor Start Raster Register

This is a register used to program the cursor start raster address by lower 5 bits (2^0 -2^4) and the cursor display mode by higher 2 bits (2^5, 2^6).

2^6	2^5	Cursor Display Mode
0	0	Non-Blink
0	1	Cursor Non-Display
1	0	Blink, 16 Field Period
1	1	Blink, 32 Field Period

Blink Period



R11: Cursor End Raster Register

This is a register used to program the cursor end raster address. When programmed value of R8 is 3 (Interlace sync. and video mode), both the cursor start raster register and the cursor end raster register must be even or odd.

R12: Start Address Register (H)
R13: Start Address Register (L)

00 00

These are used to program initial address of refresh memory to read out. Changing the contents of these registers dynamically enables paging and scrolling easily.

R14: Cursor Register (H) FF3F
R15: Cursor Register (L)

3F FF

These are used to program the cursor display address and R/W operation from the CPU is possible. When R14 is read, the higher 2 bits (2^6, 2^7) are always "0".

R16: Light Pen Register
R17: Light Pen Register

T200/T250 system are not used.

OPERATION OF CRTC

Time Chart of CRT Interface Signals

The following example shows the display operation in which values of Table. X-1 are programmed to CRTC internal registers. Fig. X-1 shows the CRT screen format. Fig. X-4 shows the time chart of signals put out from CRTC.

The relation between values of Refresh Memory Address (MA0-MA13) and Raster Address (RA0-RA4) and the display position on the screen is shown in Fig. X-10.
Fig. X-10 shows the case where the value of Start Address is 0.

Table. X-1 Programmed Values into CRTC Registers

Reg. Number	Value	Reg. Number	Value
R0	Nht	R9	Nr
R1	Nhd	R10	
R2	Nhsp	R11	
R3	Nhsw	R12	0
R4	Nvt	R13	0
R5	Nadj	R14	
R6	Nvd	R15	
R7	Nvsp	R16	
R8			

Note: Nhd < Nht , Nvd < Nvt

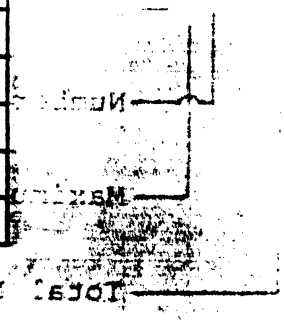
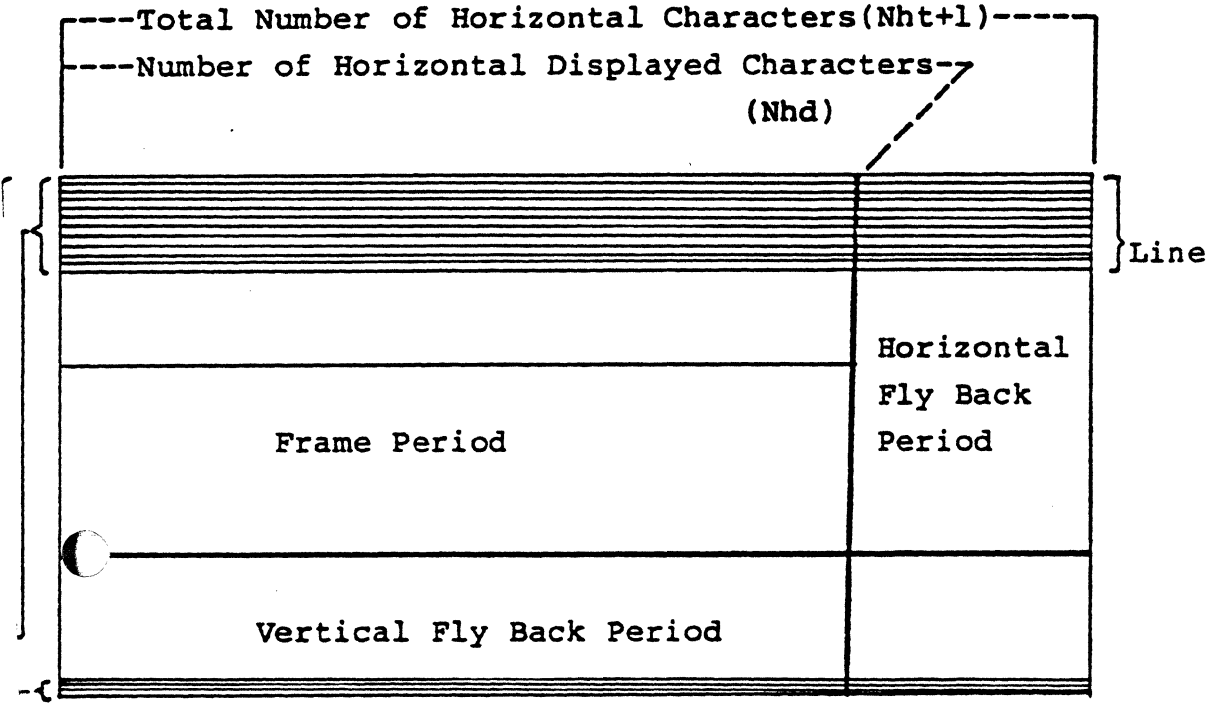


Fig. X-1 CRT Screen Format



—Total Raster Adjust (Nadj)

—Number of Vertical Displayed Characters (Nvd)

—Maximum Raster Address (Nr + 1)

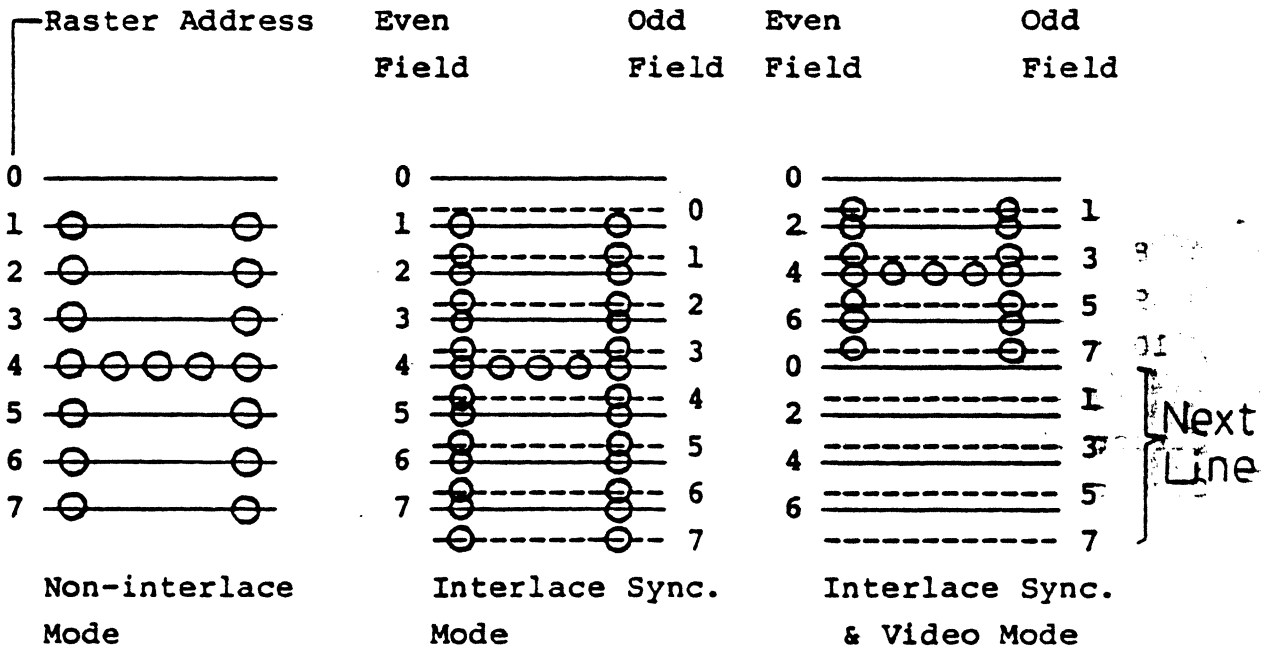
—Total Number of Vertical Characters (Nvt + 1)

Interlace Control

Fig. X-2 shows an example where the same character is displayed in non-interlace mode, interlace sync. mode, and interlace sync. & video mode.

In interlace sync. mode, the raster address of even number field and odd number field are the same and display the same character pattern. In interlace sync. and video mode, the character pattern of even number raster address is displayed in even number field. The character pattern of odd number raster address is displayed in odd number field. Therefore, compared with the characters in non-interlace mode and interlace sync. mode, the size is one-half of them vertically. Fig. X-7 shows the output wave form of vertical sync. in interlacing.

Fig. X-2 Interlace Control



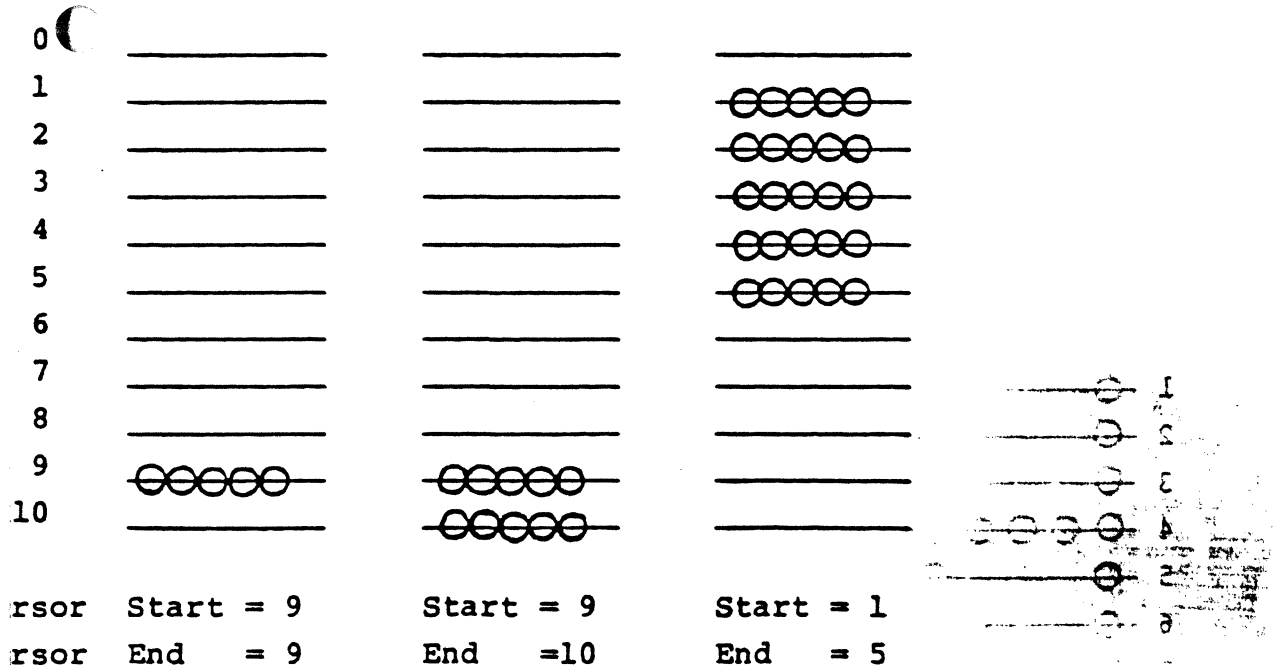
Cursor Control

Fig. X-3 shows the display patterns where each value is programmed to the cursor start raster register and the cursor end raster register. Programmed values to the cursor start raster register and the cursor end raster register need to be under the following condition.

Cursor Start Raster Register _ Cursor End Raster Register _ Maximum Raster Address Register

Time chart of CUDISP (Cursor Display) output signal is shown in Fig. X-8 and Fig. X-9.

Fig. X-3 Cursor Control



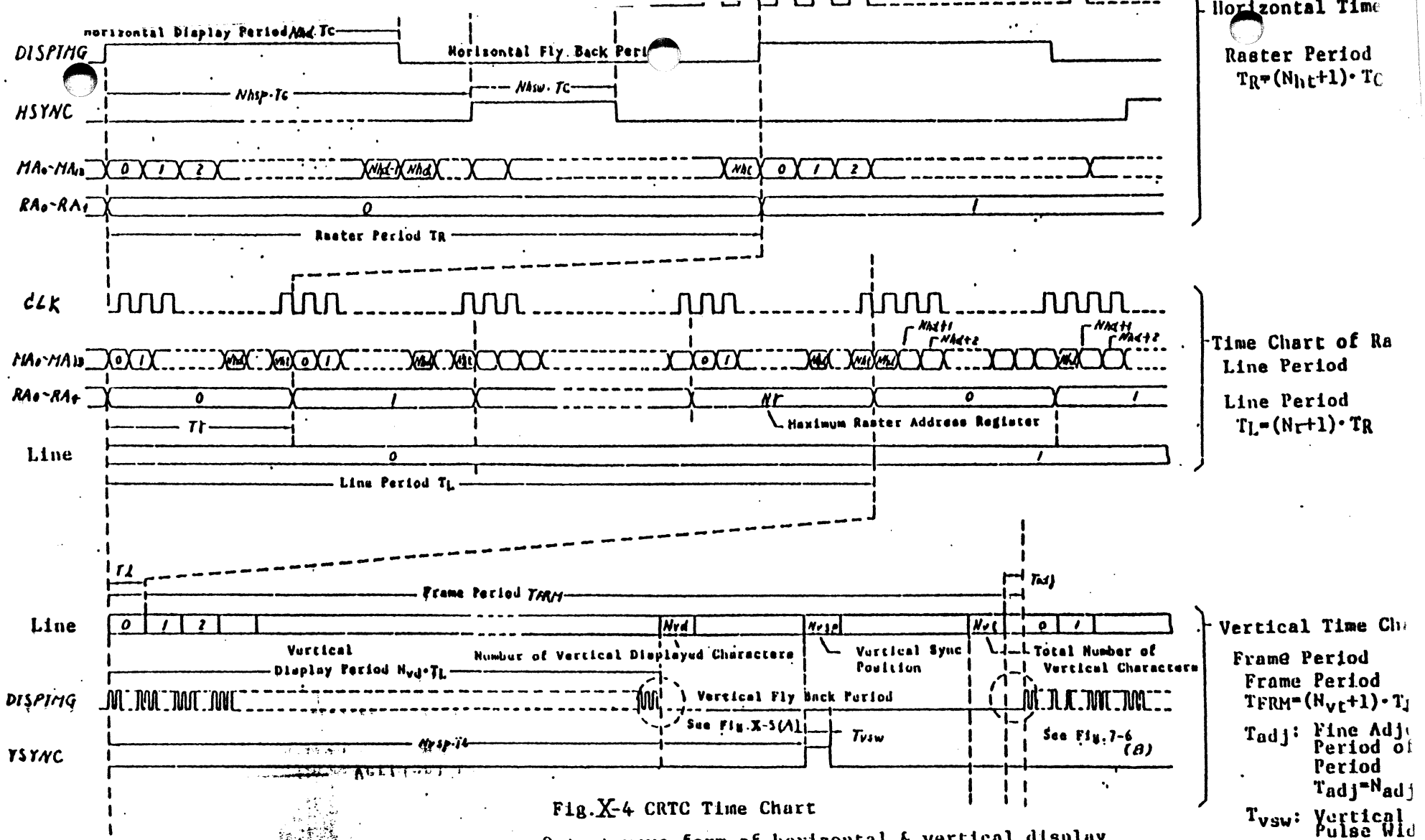


Fig.X-4 CRTC Time Chart

Output wave form of horizontal & vertical display in the case where values shown in Table.7-1 are programmed to each register.

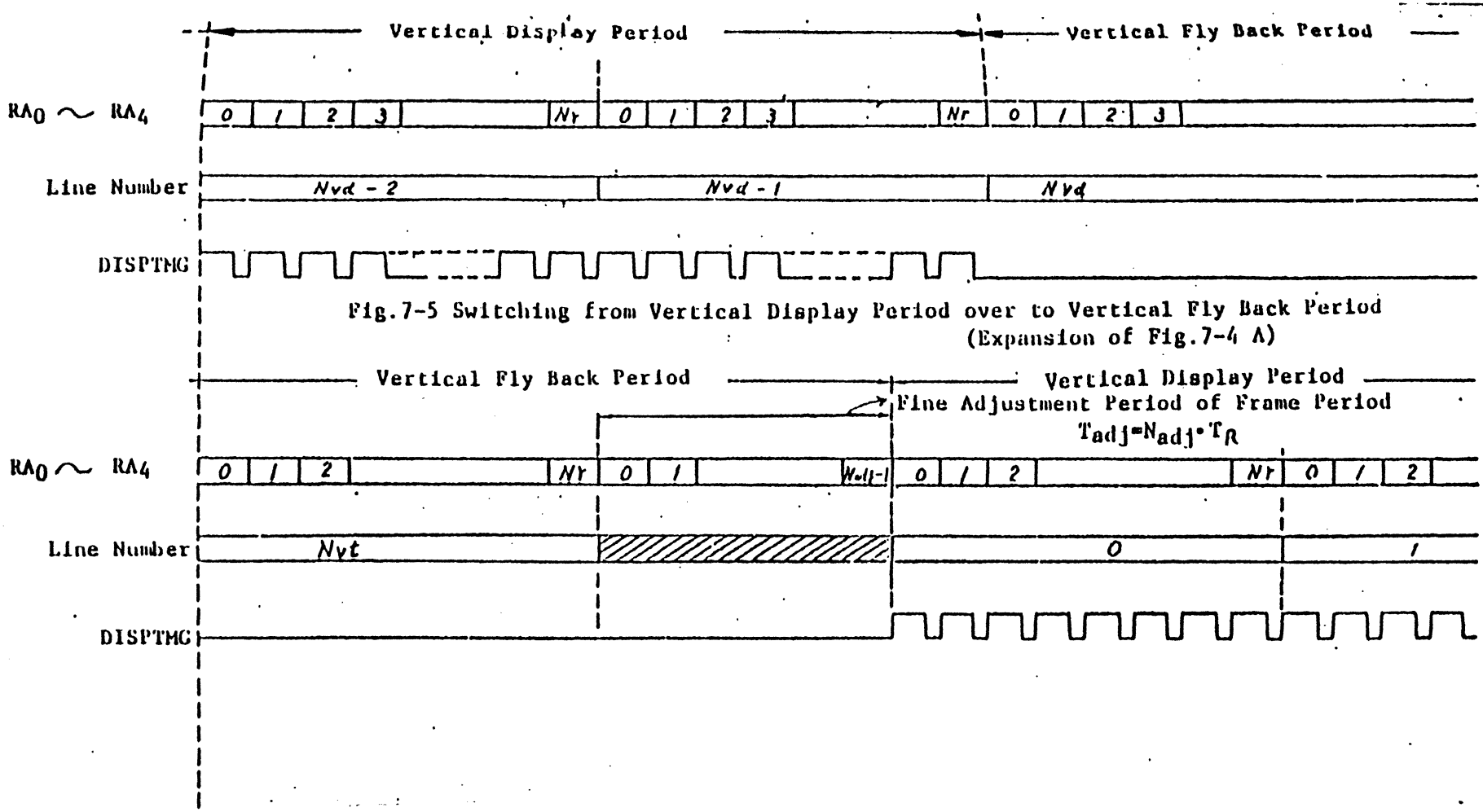


Fig.7-5 Switching from Vertical Display Period over to Vertical Fly Back Period
(Expansion of Fig.7-4 A)

Fig.X-6 Fine Adjustment Period of Frame Period in Vertical Display
(Expansion of Fig.X-4 B)

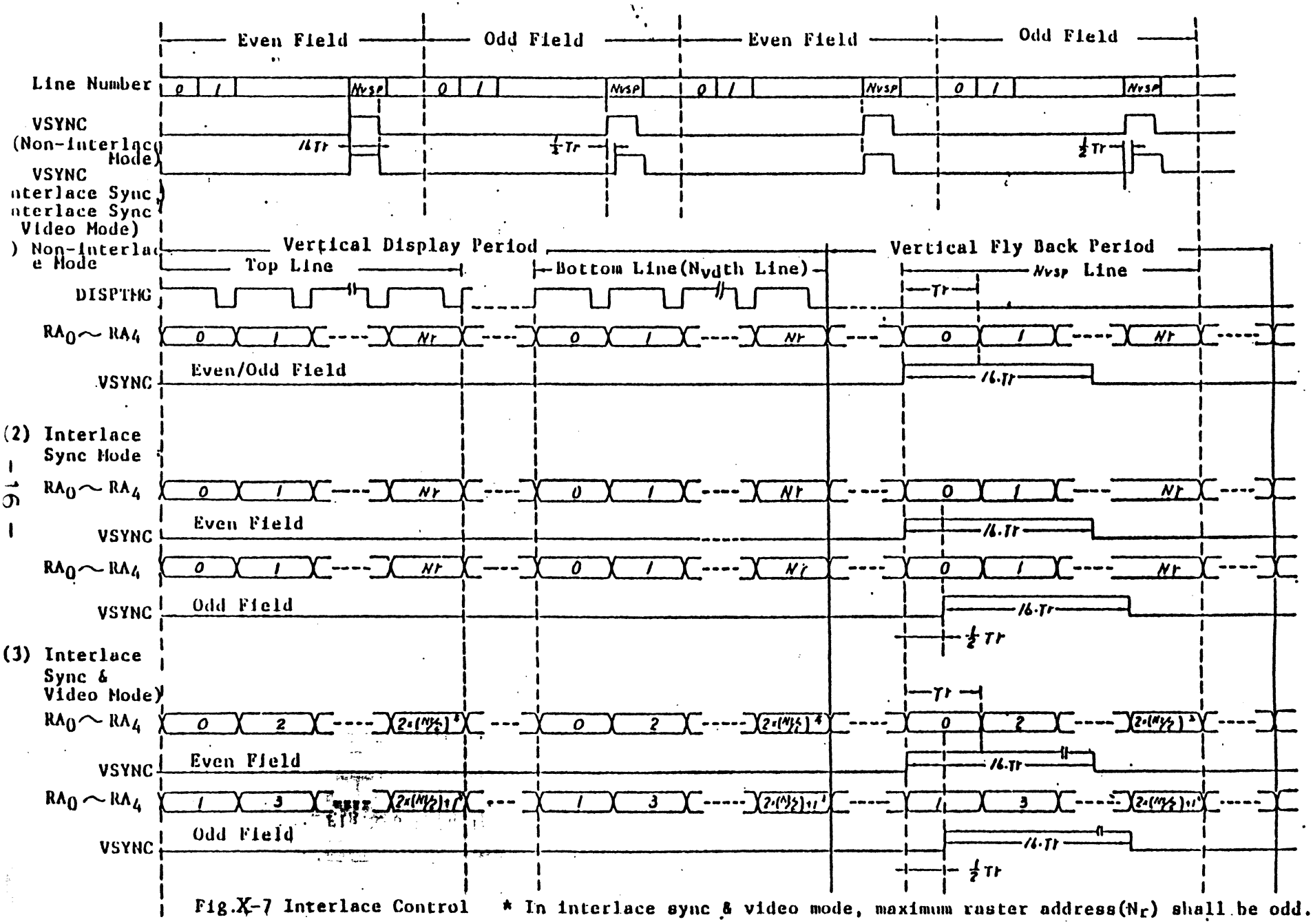


Fig.X-7 Interlace Control * In interlace sync & video mode, maximum raster address(N_r) shall be odd.

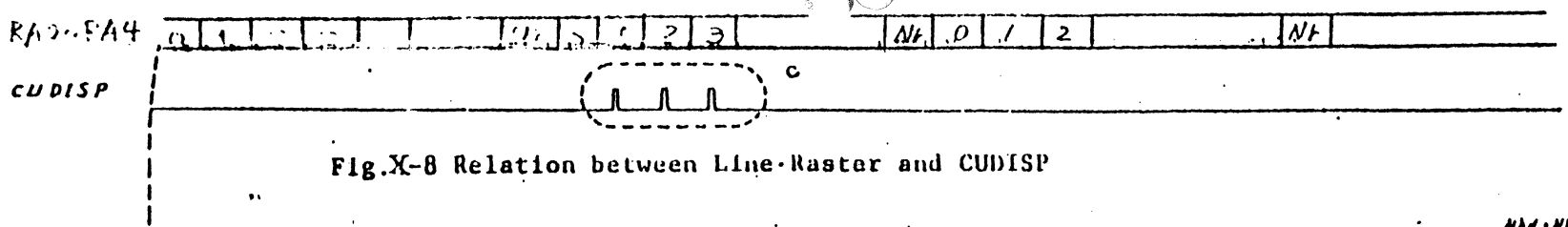


Fig.X-8 Relation between Line·Raster and CUDISP

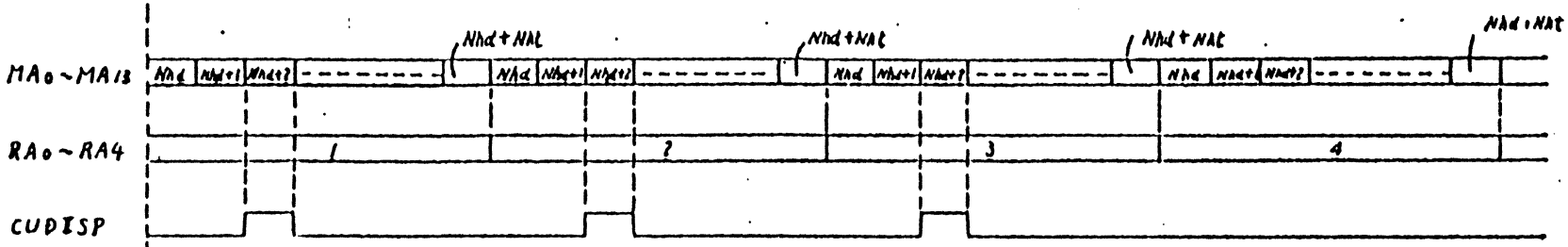


Fig.X-9 CUDISP Output Timing (Expansion of Fig.7-8 c)

NOTE: (Cursor Register=N_{hd}+2
Cursor Start
Raster Register=1
Cursor End
Raster Register=3

are programmed in cursor displ

In blink mode, it is changed int mode when frame period is 16 or period.

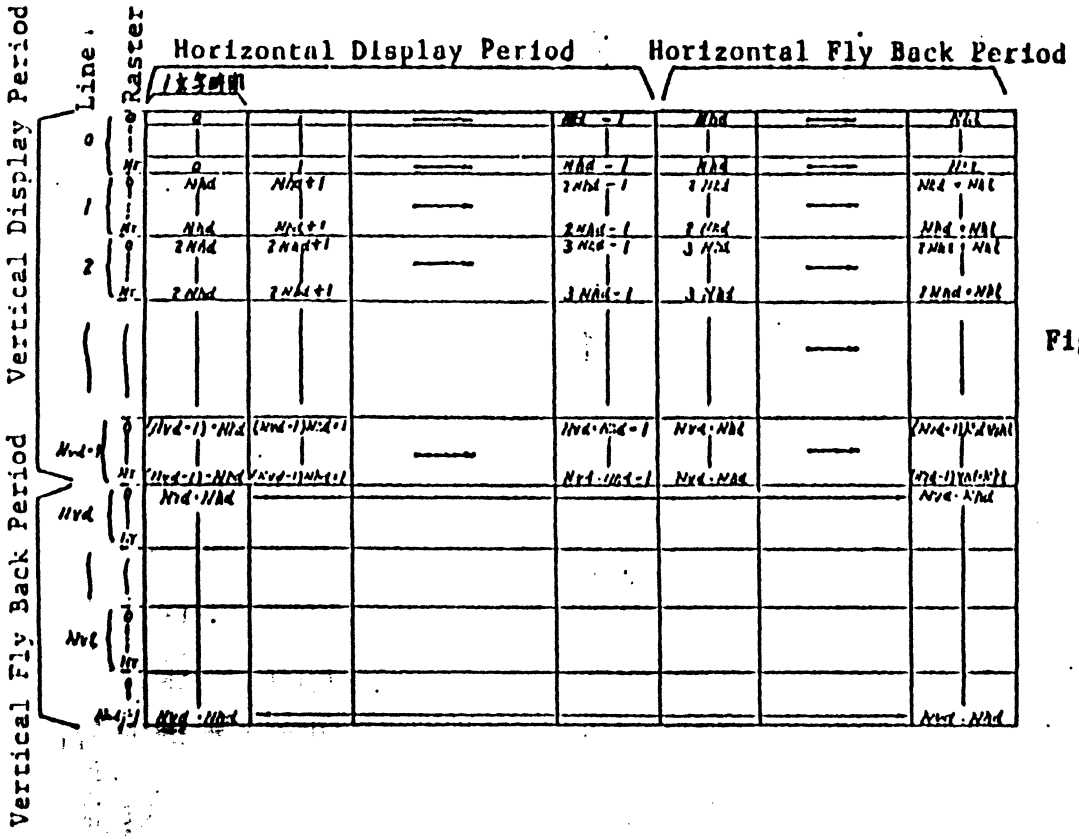


Fig.X-10 Refresh Memory Address(MA0~M

Valid refresh memory addres ~ $N_{vd}\cdot N_{hd}-1$) are shown wit the thick-line square.

Refresh memory address are out even during horizontal display period.

Refresh memory address are at N_{vd} N_{hd} during vertical period.

This is an example in the ca programmed value of start ad register is 0.

APPENDIX. B

SINGLE/DOUBLE DENSITY

FLOPPY DISK CONTROLLER

DESCRIPTION

The μPD765 is an LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of suppoting either IBM3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The FDC provides control signals which simplify the design of an external phase locked loop, and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Interface.

Hand-shaking signals are provided in the FDC which make DMA operation easy to incorporate with the aid of an external DMA Controller chip, such as the D8257. The FDC will operation in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC and DMA controller.

There are 15 separate commands which the FDC will execute. Each of these commands require multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform.
The following commands are available:

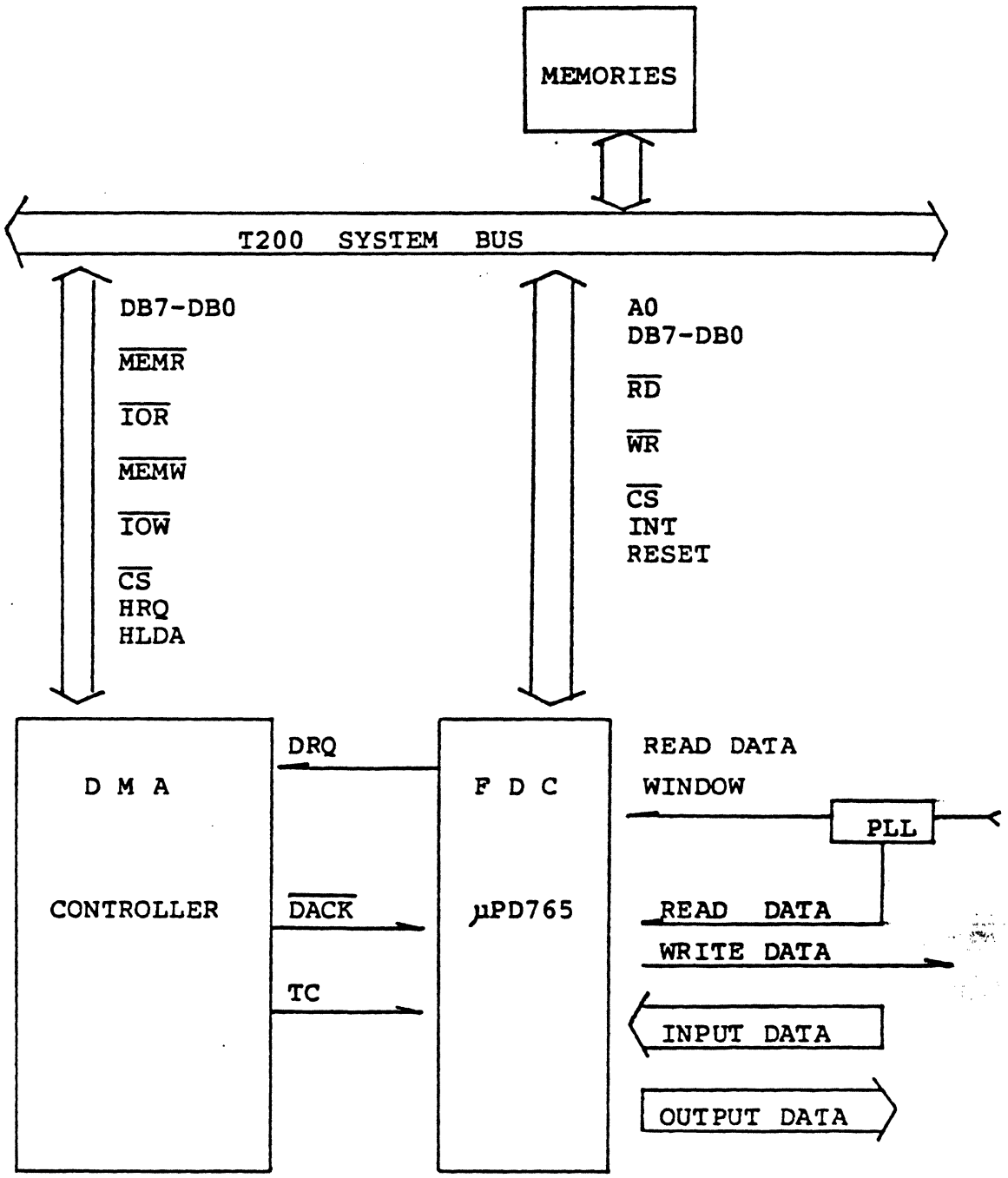
Read Data	Scan High Equal	Write Deleted Data
Read ID	Scan Low Equal	Seek
Read Deleted Data		Specify
Read a Track	Recalibrate	Write Data
Scan Equal	Format a Track	
Sense Interrupt Status		Sense Dive Status

FEATURES

Address mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The FDC offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both signal and double density modes.

* IBM compatible in both Single and Double Density Recording Formats
* Programmable Data Record Lengths: 128, 256, 512, or 1024 bytes/Sector
* Multi-Sector and Multi-Track Transfer Capability
* Drive Up to 4 Floppy Disks
* Data Scan Capability - Will Scan a Single or an Entire Cylinder's Worth of Data Fields, Comparing on a Byte by Byte Basis, Data in the processor's Memory with Data Read from the Floppy Disk
* Data Transfers in DMA or Non-DMA Mode
* Parallel Seek Operations on up to Four Drives
* Compatible with Most Microprocessors including 8080A, 8085A
* Single Phase 8 MHz clock

SYSTEM CONFIGURATION



INTERNAL REGISTERS

The FDC (μPD765) contains two registers which may be accessed by the CPU; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), which stores data, commands, parameters,and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The Status Register may only be read and is used to facilitate the transfer of data between the CPU and FDC.

The bits in the Main Status Register are defined as follows:

D7							D0
RQM	DIO	NDM	CB	D4B	D3B	D2B	D1B

RQM: Request for Master
Indicates Data Register is ready to send or receive data to or from the CPU. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the CPU.

DIO: Data Input/Output
Indicates direction of data transfer between FDC and Data Register.
DIO = "1", then transfer is from Data Register to the CPU.
DIO = "0", then transfer is from the CPU to Data Register.

NDM: Non-DMA mode
The FDC is in the non-DMA mode.

CB : FDC Busy
A read or write command is in process.

D4B: FDD number 4 is in the seek mode.
D3B: FDD number 3 is in the seek mode.
D2B: FDD number 2 is in the seek mode.
D1B: FDD number 1 is in the seek mode.

COMMAND SEQUENCE

The FDC is capable of performing 15 different commands. Each command is intiated by a multi-byte transfer from the CPU, and the result after execution of the command may also be a multi-byte transfer back to the CPU. Because of this multi-byte interchange of information between the FDC and the CPU, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the CPU.
Execution Phase:	The FDC performs the operation it was instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information are made available to the CPU.

INSTRUCTION: READ DATA

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	----------C----------								Secter ID information
	W	----------H----------								prior to Command
	W	----------R----------								execution
	W	----------N----------								
	W	----------EOT----------								
	W	----------GPL----------								
	W	----------DTL----------								
Execution										Data-transfer between the FDD and main-system
Result	R	----------ST0----------								Status information
	R	----------ST1----------								after Command execution
	R	----------ST2----------								
	R	----------C----------								Secter ID information
	R	----------H----------								after Command execution
	R	----------R----------								
	R	----------N----------								

Note: Symbols used in this table are described at the end of this section.

X = don't care. usually made to equal binary 0.

A_0 should equal binary 1 for all operations.

INSTRUCTION: READ DELETED DATA

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	----------C----------								Secter ID information
	W	----------H----------								prior to Command
	W	----------R----------								execution
	W	----------N----------								
	W	----------EOT----------								
	W	----------GPL----------								
	W	----------DTL----------								
Execution										Data-transfer between the FDD and main-system
Result	R	----------ST0----------								Status information
	R	----------ST1----------								after Command execution
	R	----------ST2----------								
	R	----------C----------								Secter ID information
	R	----------H----------								after Command execution
	R	----------R----------								
	R	----------N----------								

Note: Symbols used in this table are described at the end of this section.

X = don't care. usually made to equal binary 0.

A_0 should equal binary 1 for all operations.

INSTRUCTION: WRITE DATA

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	----------C----------								Secter ID information
	W	----------H----------								prior to Command
	W	----------R----------								execution
	W	----------N----------								
	W	----------EOT----------								
	W	----------GPL----------								
	W	----------DTL----------								
Execution										Data-transfer between the main-system and FDD
Result	R	----------ST0----------								Status information
	R	----------ST1----------								after Command execution
	R	----------ST2----------								
	R	----------C----------								Secter ID information
	R	----------H----------								after Command execution
	R	----------R----------								
	R	----------N----------								

Note: Symbols used in this table are described at the end of this section.

X = don't care. usually made to equal binary 0.

A_0 should equal binary 1 for all operations.

INSTRUCTION: WRITE DELETED DATA

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	----------C----------								Secter ID information
	W	----------H----------								prior to Command
	W	----------R----------								execution
	W	----------N----------								
	W	----------EOT----------								
	W	----------GPL----------								
	W	----------DTL----------								
Execution										Data-transfer between the FDD and main-system
Result	R	----------ST0----------								Status information
	R	----------ST1----------								after Command execution
	R	----------ST2----------								
	R	----------C----------								Secter ID information
	R	----------H----------								after Command execution
	R	----------R----------								
	R	----------N----------								

Note: Symbols used in this table are described at the end of this section.

X = don't care. usually made to equal binary 0.

A_0 should equal binary 1 for all operations.

INSTRUCTION: READ A TRACK

PHASE	DATA BUS R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	----------C----------								Secter ID information
	W	----------H----------								prior to Command
	W	----------R----------								execution
	W	----------N----------								
	W	----------EOT----------								
	W	----------GPL----------								
	W	----------DTL----------								
Execution										Data-transfer between the FDD and main-system. FDC reads all of cylinders contents from index hole to EOT.
Result	R	----------ST0----------								Status information
	R	----------ST1----------								after Command execution
	R	----------ST2----------								
	R	----------C----------								Secter ID information
	R	----------H----------								after Command execution
	R	----------R----------								
	R	----------N----------								

Note: Symbols used in this table are described at the end of this section.
X = don't care. usually made to equal binary 0.
A_0 should equal binary 1 for all operations.

INSTRUCTION: READ ID

PHASE	DATA BUS R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the cylinder is stored in Data Register
Result	R	----------				ST0			----------	Status information
	R	----------				ST1			----------	after Command execution
	R	----------				ST2			----------	
	R	----------				C			----------	Secter ID information
	R	----------				H			----------	during Execution Phase
	R	----------				R			----------	
	R	----------				N			----------	

Note: Symbols used in this table are described at the end of this section.
X = don't care. usually made to equal binary 0.
A_0 should equal binary 1 for all operations.

INSTRUCTION: FORMAT A TRACK

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	----------N----------								Bytes/Sector
	W	----------SC----------								Sectors/Track
	W	----------GPL----------								Gap3
	W	----------D----------								Filler Byte
Execution										FDC formats an entire cylinder
Result	R	----------ST0----------								Status information
	R	----------ST1----------								after Command execution
	R	----------ST2----------								
	R	----------C----------								In this case, the ID
	R	----------H----------								information has
	R	----------R----------								no meaning.
	R	----------N----------								

Note: Symbols used in this table are described at the end of this section.

X = don't care. usually made to equal binary 0.

A_0 should equal binary 1 for all operations.

INSTRUCTION: SCAN EQUAL

PHASE	DATA BUS R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	----------C----------								Secter ID information
	W	----------H----------								prior to Command
	W	----------R----------								execution
	W	----------N----------								
	W	----------EOT----------								
	W	----------GPL----------								
	W	----------STP----------								
Execution										Data-compared between the FDD and main-system
Result	R	----------ST0----------								Status information
	R	----------ST1----------								after Command execution
	R	----------ST2----------								
	R	----------C----------								Secter ID information
	R	----------H----------								after Command execution
	R	----------R----------								
	R	----------N----------								

Note: Symbols used in this table are described at the end of this section.

X = don't care. usually made to equal binary 0.

A_0 should equal binary 1 for all operations.

INSTRUCTION: SCAN LOW OR EQUAL

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	----------C----------								Secter ID information
	W	----------H----------								prior to Command
	W	----------R----------								execution
	W	----------N----------								
	W	----------EOT----------								
	W	----------GPL----------								
	W	----------STP----------								
Execution										Data-compared between the FDD and main-system
Result	R	----------ST0----------								Status information
	R	----------ST1----------								after Command execution
	R	----------ST2----------								
	R	----------C----------								Secter ID information
	R	----------H----------								after Command execution
	R	----------R----------								
	R	----------N----------								

Note: Symbols used in this table are described at the end of this section.

X = don't care. usually made to equal binary 0.

A_0 should equal binary 1 for all operations.

INSTRUCTION: SCAN HIGH OR EQUAL

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	----------C----------								Secter ID information
	W	----------H----------								prior to Command
	W	----------R----------								execution
	W	----------N----------								
	W	----------EOT----------								
	W	----------GPL----------								
	W	----------STP----------								
Execution										Data-compared between the FDD and main-system
Result	R	----------ST0----------								Status information
	R	----------ST1----------								after Command execution
	R	----------ST2----------								
	R	----------C----------								Secter ID information
	R	----------H----------								after Command execution
	R	----------R----------								
	R	----------N----------								

Note: Symbols used in this table are described at the end of this section.

X = don't care. usually made to equal binary 0.

A_0 should equal binary 1 for all operations.

INSTRUCTION: RECALIBRATE

PHASE	DATA BUS R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
Execution										Head retracted to Track zero

INSTRUCTION: SENSE INTERRUPT STATUS

PHASE	DATA BUS R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	----------ST0----------								Status information at the end of seek operation about the FDC
	R	----------PCN----------								

INSTRUCTION: SENSE DRIVE STATUS

PHASE	DATA BUS R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Result	R	----------ST3----------								Status information about FDD

INSTRUCTION: SPECIFY

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	<---SRT--->				<----HUT------>				
	W	<----------HLT---------->							ND	

INSTRUCTION: SEEK

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	----------NCN----------								
Execution										Head is positioned over proper Cylinder on Floppy Disk

INSTRUCTION: INVALID

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	-------Invalid Codes----------								Invalid Command Codes (NoOp - FDC goes into Standby State)
Result	R	----------ST0----------								ST0 = 80 HEX

SYMBOL	NAME	DESCRIPTION
A0	Address Line 0	A0 controls selection of Main Status Register (A0 = 0) or Data Register (A0 = 1).
C	Cylinder-Number	C stands for the current selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D7-D0	Data Bus	8-bit Data Bus where D7 stands for a most significant bit, and D0 stands for a least Significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
EOT	End of Track	EOT stands for the final sector number on a cylinder.
GPL	Gap Length	GPL stands for the length of GAP 3 (spacing between Sectors excluding VCO Sync. Field).
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 (H = HD in all command words)

SYMBOL	NAME	DESCRIPTION
HLT	Head Load Time	HLT stands for the head load time in the FDD. This timer can be programmed from 2ms to 254ms by 2ms (00=DON'T USE, 01=2ms, 02=4ms, and so forth) for 8-inch floppy disk drives. It can be also programmed from 4ms to 508ms by 4ms for 5.25-inch floppy disk drives.
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred. This timer can be programmed from 16ms to 240ms by 16ms (00=NOT USE, 01=16ms, 02=32ms, and so forth) for 8-inch floppy disk drives. It can be also programmed from 32ms to 480ms by 10ms (00=NOT USE, 01=32ms, 02=64ms, and so forth) for 5.25-inch floppy disk drives.
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi Track	If MT is high, a multi-track operation is to be performed. (A cylinder under both HD0 and HD1 will be read or written)

SYMBOL	NAME	DESCRIPTION
N	Number	N stands for the number of data bytes written in a sector.
NCN	New Cylinder Number	NCN stands for a new cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for Cylinder number at the completion of SENSE INTERRUPT STATUS command. Position of Head at present time.
R	Record	R stands for the sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SC	Sector	SC indicates the number of sector per Cylinder.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. This timer can be programmed from 1ms to 16ms by 1ms (F_{HEX}=1ms, E_{HEX}=2ms, D_{HEX}=3ms, and so forth) for 8-inch floppy disk drives. It can be also programmed from 2ms to 32ms by 2ms for 5.25-inch floppy disk drives.

SYMBOL	NAME	DESCRIPTION
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST0-3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected A_0 = 0). ST0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the CPU (or DMA); and if STP = 0, then alternate sectors are read and compared.
US0 US1	Unit Select	US stands for a selected drive number 0 or 1.

PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the μPD765. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the μPD765. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the μPD765 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the μPD765 is in the NON-DMA Mode, then the receipt of each data byte (if μPD765 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) will reset the Interrupt as well as output the Data onto the Data Bus. If the processor cannot handle Interrupts fast enough (every 13 μs) then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the $\overline{WR}$ signal performs the reset to the Interrupt signal.

If the μPD765 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The μPD765 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The μPD765 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The μPD765 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after successfully completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the μPD765 to form the Command Phase, and are read out of the μPD765 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the μPD765, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the μPD765 is ready for a new command. A command may be truncated (prematurely ended) by simply sending a Terminal Count signal to pin 16 (TC = 1). This is a convenient means of ensuring that the processor may always get the μPD765's attention even if the disk system hangs up in an abnormal manner.

ATA

ame (9 e words are required to place the FDC into the Read Data Mode. After the Read Data s has b issued the FDC loads the head (if it is in the unloaded state), waits the specified head ime (d d in the Specify Command), and begins reading ID Address Marks and ID fields. When nt sector number ("R") stored in the ID Register (IDR) compares with the sector number read off ette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data

ompletion of the read operation from the current sector, the Sector Number is incremented by one, r data from the next sector is read and output on the data bus. This continuous read function is called lti-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal signal. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue d data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of ector terminate the Read Data Command.

amount of data which can be handled with a single command to the FDC depends upon MT (multi- k), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 1. Transfer Capacity

Th ulti-track" function (MT) allows the FDC to read data from both sides of the diskette. For a pa r cylinder, data will be transferred starting at Sector 0, Side 0 and completing at Sector L, Side 1 (Se L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

Status Register 2 to a 1 (high), and terminates the Read Data Command.

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the DM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 µs in the FM Mode, and every 13 µs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the values for C, H, R, and N, when the processor terminates the Command.

MT	EOT	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				
1	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	NC	LSB	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	LSB	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				

Notes: 1 NC (No Change): The same value as the one at the beginning of command execution.

2 LSB (Least Significant Bit): The least significant bit of H is complemented.

Table 2: ID Information When Processor Terminates Command

WRITE DATA

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Fields. When the current sector number ("R"), stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 31 μs in the FM mode, and every 15 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

READ DELETED DATA

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field (and SK = 0 (low)), it will read all the data in the sector and set the MD flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

TRACK

mand is similar to READ DATA Command except that this is a continuous READ operation
ie entire contents of the track are read. Immediately after encountering the INDEX HOLE, the
rts reading all data on the track. Gap bytes, Address Marks and Data are all read as a continuous
eam. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data
e track. The FDC compares the ID information read from each sector with the value stored in the
d sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip
ions are not allowed with this command.

ommand terminates when EOT number of sectors have been read ($EOT_{max} = FF_{hex} = 255_{dec}$).
FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the
d time, then it sets the MA (missing address mask) flag in Status Register 1 to a 1 (high), and termi
the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively).

D ID

READ ID Command is used to give the present position of the recording head. The FDC stores the
es from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette,
re the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in
tus Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status
ister 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0
1 respectively.

ORMAT A TRACK

he Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is
ritten on the Diskette; Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double
ensity) or System 3740 (Single Density) Format are recorded. The particular format which will be written
s controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap
Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data
Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor;
that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number),
R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with non-
sequential sector numbers, if desired.

After formatting each sector, the processor must send new values for C, H, R, and N to the μPD765 for each sector on the track. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R + 1 when it is read during the Result Phase. This incrementing and formatting continues for the whole cylinder until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes:

FORMAT	SECTOR SIZE	N	SC	GPL ①	GPL ②	REMARKS
FM Mode	128 bytes/Sector	00	$1A_{(16)}$	$07_{(16)}$	$1B_{(16)}$	IBM Diskette 1
	256	01	$0F_{(16)}$	$0E_{(16)}$	$2A_{(16)}$	IBM Diskette 2
	512	02	08	$1B_{(16)}$	$3A_{(16)}$	
FM Mode	1024 bytes/Sector	03	04	–	–	
	2048	04	02	–	–	
	4096	05	01	–	–	
MFM Mode	256	01	$1A_{(16)}$	$0E_{(16)}$	$36_{(16)}$	IBM Diskette 2D
	512	02	$0F_{(16)}$	$1B_{(16)}$	$54_{(16)}$	
	1024	03	08	$35_{(16)}$	$74_{(16)}$	IBM Diskette 2D
	2048	04	04	–	–	
	4096	05	02	–	–	
	8192	06	01	–	–	

Table 3

Note: ① Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections.

② Suggested values of GPL in format command.

SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system (Processor in NON-DMA mode, and DMA Controller in DMA mode). The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 = SN	BIT 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} \geq D_{Processor}$

Table 4

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

SEEK

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)
PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

RECALIBRATE

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 1 (high) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulse have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. However, interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

SEEK END	INTERRUPT CODE		CAUSE
BIT 5	BIT 6	BIT 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Table 5

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 0 to 240 ms in increments of 16 ms (00 = 0 ms, 01 = 16 ms, 02 = 32 ms, etc.). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 256 ms in increments of 2 ms (00 = 2 ms, 01 = 4 ms, 02 = 6 ms, etc.).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information.

INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

STATUS REGISTER IDENTIFICATION

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
STATUS REGISTER 0 - ST0 -			
D_7	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			$D_7 = 0$ and $D_6 = 1$ Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid Command issue, (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit Number at Interrupt
D_0	Unit Select 0	US 0	
STATUS REGISTER 1 - ST 1 -			
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.

BIT NAME	SYMBOL	DESCRIPTION
STATUS REGISTER 1 (CONT.)		
...t ...itable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
...issing ...ddress ...Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
		If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
STATUS REGISTER 2 -ST2-		
		Not used. This bit is always 0 (low).
Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
Scan Equal ...it	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
...can Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
STATUS REGISTER 3 -ST3-		
Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

APPENDIX C

EXTENDED MEMORY VERSION OF THE T200/T250 SYSTEM

DESCRIPTION

The data processing system T200/T250 has an extended memory version on which 63 K CP/M can run. This memory extension can be done by the memory bank selection.

For the memory bank selection, MODE REGISTER (C0H) should be used as follows (See Fig. C.1)

MODE REGISTER (C0H)

MSB							LSB
X	X	X	X	ROM	VPG	RAM1	RAM0

X: conforms to the bit definition in MODE REGISTER(section 4.4.1)

EXAMPLES

(1) Initial Setting

MSB							LSB
X	X	X	X	0	0	0	0

In this case, BANK 0(ROM) and BANK I(D-RAM) can be selected.

(2) Video-RAM(BANK III) Select/Deselect

MSB							LSB
X	X	X	X	X	0	1	0

This operation selects the video-RAM(BANK III).

(3) VPG(BANK IV) Select/Deselect

MSB							LSB
X	X	X	X	X	1	1	0

This operation selects the VPG(BANK IV).

(4) D-RAM(BANK I) Select

MSB							LSB
X	X	X	X	1	0	0	0

This operation selects D-RAM(BANK I).

(5) S-RAM(BANK II) Select/Deselect

MSB							LSB
X	X	X	X	X	0	1	0

This operation selects S-RAM(BANK II).

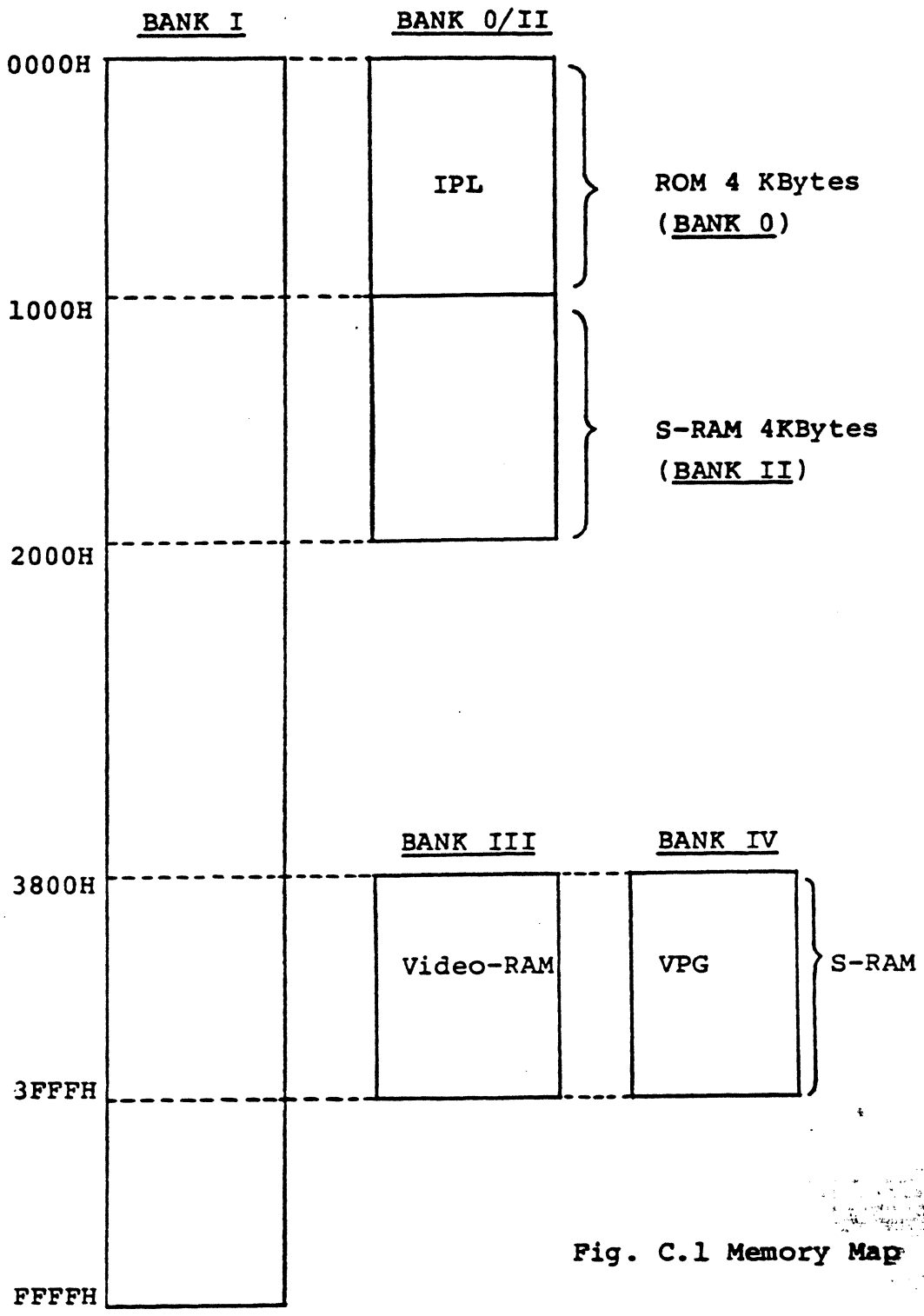


Fig. C.1 Memory Map

MEMORY BANK SELECTION

MEMORY MODE REGISTER(C0H)

For the memory bank selection, MODE REGISTER should be specified as follows.

	3	2	1	0
	ROM	VPG	RAM1	RAM0

(Note 1)

	"0"	"2"	"4"	"6"	"8"	"A"	"C"	"E"	HEX
ROM	0	0	0	0	1	1	1	1	
VPG	0	0	1	1	0	0	1	1	
RAM1	0	1	0	1	0	1	0	1	
RAM0	0	0	0	0	0	0	0	0	
ADDRESS									
0000H ↓ 0FFFH	ROM								
1000H ↓ 1FFFH		S-RAM		S-RAM		S-RAM		S-RAM	
2000H ↓ 37FFH					D-RAM				
3800H ↓ 3FFFH		V-RAM		VPG		V-RAM		VPG	
4000H ↓ FFFFH									

Note 1: RAM0 should be always set to "0".

Note 2: V-RAM means Video-RAM.

PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the μPD765. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the μPD765. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the μPD765 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the μPD765 is in the NON-DMA Mode, then the receipt of each data byte (if μPD765 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) will reset the Interrupt as well as output the Data onto the Data Bus. If the processor cannot handle Interrupts fast enough (every 13 μs) then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the $\overline{WR}$ signal performs the reset to the Interrupt signal.

If the μPD765 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The μPD765 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The μPD765 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The μPD765 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after successfully completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the μPD765 to form the Command Phase, and are read out of the μPD765 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the μPD765, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the μPD765 is ready for a new command. A command may be truncated (prematurely ended) by simply sending a Terminal Count signal to pin 16 (TC = 1). This is a convenient means of ensuring that the processor may always get the μPD765's attention even if the disk system hangs up in an abnormal manner.

TA

ne (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data has b issued the FDC loads the head (if it is in the unloaded state), waits the specified head ne (d in the Specify Command), and begins reading ID Address Marks and ID fields. When it sector number ("R") stored in the ID Register (IDR) compares with the sector number read off rte, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data

mpletion of the read operation from the current sector, the Sector Number is incremented by one, data from the next sector is read and output on the data bus. This continuous read function is called "Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal signal. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of tor terminate the Read Data Command.

mount of data which can be handled with a single command to the FDC depends upon MT (multi-), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 1. Transfer Capacity

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a pa r cylinder, data will be transferred starting at Sector 0, Side 0 and completing at Sector L, Side 1 (Se L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

Status Register 2 to a 1 (high), and terminates the Read Data Command.

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the DM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 µs in the FM Mode, and every 13 µs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the values for C, H, R, and N, when the processor terminates the Command.

MT	EOT	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				
1	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	NC	LSB	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	LSB	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				

Notes: 1 NC (No Change): The same value as the one at the beginning of command execution.

2 LSB (Least Significant Bit): The least significant bit of H is complemented.

Table 2: ID Information When Processor Terminates Command

WRITE DATA

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Fields. When the current sector number ("R"), stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 31 µs in the FM mode, and every 15 µs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

READ DELETED DATA

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field (and SK = 0 (low)), it will read all the data in the sector and set the MD flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

TRACK

mand is similar to READ DATA Command except that this is a continuous READ operation e entire contents of the track are read. Immediately after encountering the INDEX HOLE, the rts re[illegible] all data on the track, Gap bytes, Address Marks and Data are all read as a continuous ram. [illegible] FDC finds an error in the ID or DATA CRC check bytes, it continues to read data e track. The FDC compares the ID information read from each sector with the value stored in the id sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip ons are not allowed with this command.

ommand terminates when EOT number of sectors have been read ($EOT_{max} = FF_{hex} = 255_{dec}$). FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the d time, then it sets the MA (missing address mask) flag in Status Register 1 to a 1 (high), and termi the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively).

D ID

READ ID Command is used to give the present position of the recording head. The FDC stores the as from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, re the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in tus Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status ister 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 1 respectively.

ORMAT A TRACK

e Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is ritten on the Diskette: Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double ensity) or System 3740 (Single Density) Format are recorded. The particular format which will be written s controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with non-sequential sector numbers, if desired.

After formatting each sector, the processor must send new values for C, H, R, and N to the μPD765 for each sector on the track. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R + 1 when it is read during the Result Phase. This incrementing and formatting continues for the whole cylinder until the FDC encounters the INDEX HOLE for [illegible] cond time, whereupon it terminates the command.

[illegible] a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes:

FORMAT	SECTOR SIZE	N	SC	GPL ①	GPL ②	REMARKS
FM Mode	128 bytes/Sector	00	$1A_{(16)}$	$07_{(16)}$	$1B_{(16)}$	IBM Diskette 1
	256	01	$0F_{(16)}$	$0E_{(16)}$	$2A_{(16)}$	IBM Diskette 2
	512	02	08	$1B_{(16)}$	$3A_{(16)}$	
FM Mode	1024 bytes/Sector	03	04	–	–	
	2048	04	02	–	–	
	4096	05	01	–	–	
MFM Mode	256	01	$1A_{(16)}$	$0E_{(16)}$	$36_{(16)}$	IBM Diskette 2D
	512	02	$0F_{(16)}$	$1B_{(16)}$	$54_{(16)}$	
	1024	03	08	$35_{(16)}$	$74_{(16)}$	IBM Diskette 2D
	2048	04	04	–	–	
	4096	05	02	–	–	
	8192	06	01	–	–	

Table 3

Note: ① Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections.

② Suggested values of GPL in format command.

SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system (Processor in NON-DMA mode, and DMA Controller in DMA mode). The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 = SN	BIT 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} \geq D_{Processor}$

Table 4

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 µs (FM Mode) or 13 µs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

SEEK

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)
PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.