CLUSTOR
USER GUIDE

PB2500-9001-011

SYSTEM INDUSTRIES

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WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions in this manual may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J or Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which the user at his own expense will be required to take whatever measures may be required to correct the interference.

This digital apparatus does not exceed the Class A limits for radio noise emissions from a digital apparatus as set out in the Radio Interference Regulations of the Canadian Department of Communications.

Le present appareil numerique n'est pas de bruits radioelectriques depassant les limtes applicables aux appareils numeriques de Class A, prescrites dans le reglement sur le brouillage radioelectrique edicte par le Ministere des Communicatios du Canada.

PROPRIETARY STATEMENT

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1
INTRODUCTION

CLUSTOR User Guide explains how to install, operate, and maintain System Industries CLUSTOR Mass Storage Subsystem. It contains nine chapters and seven appendixes, listed in Table 1-1.

Table 1-1. CLUSTOR User Guide Sections

SECTION	DESCRIPTION
Section 1: Introduction	Contains the manual audience, related publications, conventions, terms list, and materials needed
Section 2: CLUSTOR Subsystem	Describes subsystem features and options, components, indicators, and CLUSTOR subsystem controls
Section 3: Configuration	Lists the configuration considerations, configuration examples, and necessary settings
Section 4: Preinstallation	Discusses technical specifications, site concerns, and initial unpacking
Section 5: Installation	Explains subsystem, options, and upgrade installation
Section 6: Maintenance	Includes subsystem maintenance routines, removal and replacement procedures
Section 7: System Verification and Troubleshooting	Discusses subsystem verification and approaches for troubleshooting
Section 8: Illustrated Parts List	Lists Field Replaceable Units within the CLUSTOR Controller
Section 9: Ready Reference	Provides a quick reference for configuration requirements and board settings used during installation
Appendix A: Disk Drive Settings	Gives settings for disk drives used with the CLUSTOR Controller
Appendix B: SBI CPA Installation	Gives installation procedures for SBI CPA
Appendix C: Qbus CPA Installation	Provides the installation procedures for Qbus CPA
Appendix D: UNIBUS Installation	Gives installation procedures and register information for UNIBUS CPA
Appendix E: BI Bus CPA Installation	Provides installation information for BI Bus CPA
Appendix F: Qbus CPA/M Installation	Provides installation information for Qbus CPA/M (MSCP).
Appendix G RM Register Sets	Lists the RM-compatible register sets for SBI, UNIBUS, and QBus CPA

1.1 Manual Audience

CLUSTOR User Guide is intended for System Industries customer service engineers, system users, and self-maintenance customers. Familiarity with VMS and UNIX operating systems, along with understanding the fundamentals of DEC networks, computers, and disk drive operations, is required.

1.2 Related Publications

Additional information on the CLUSTOR Subsystems and its related configurations is provided in the publications listed in Table 1-2.

Table 1-2. Related Publications

PUBLICATION NUMBER	TITLE
PB5000-9211	ULTRIX USER GUIDE
PB8700-9200	5.25-INCH DISK DRIVE INSTALLATION GUIDE
PB6005-9100	8-INCH QUICK RELEASE CHASSIS USER GUIDE
PB6005-9210	5.25-INCH QUICK RELEASE CHASSIS USER GUIDE
PB9900-9036	VAX 11-780/750/730 V4.4 — 4.7 SBI/CMI USER GUIDE
PB9900-9047	VAX 11-780/750/730 V4.4 — 4.7 UNIBUS USER GUIDE
PB9900-9070	VAX/VMS V5.X SOFTWARE MODIFICATION GUIDE
PB9900-9310	UNIX BSD 4.3 UTILITY GUIDE
PB9900-9992	8600/8650 SBI FIELD SERVICE INSTALLATION
PB9901-9041	FCC DISK DRIVE USER GUIDE
PB9901-9061	SI93 DISK DRIVE USER GUIDE
PB9904-9013	SILINK USER GUIDE
PB9904-9014	SIDOS PROGRAM USER GUIDE
PB9951-9041	SI FCC-COMPLIANT 60-INCH CABINET USER GUIDE
PB6500-9001	THETA SERIES CABINET USER GUIDE
PB2500-9100	eaSIshadow USER GUIDE
PB2950-9001	SI500C SERIES DISK DRIVE USER GUIDE
PB2920-9001	SI506 DISK DRIVE USER GUIDE
PB3270-9001	SI817 CHASSIS SUBSYSTEM USER GUIDE

1.3 Manual Conventions

Refer to the following documentation conventions as a guide to using this manual.

- Typed computer entry is shown in **boldface**. Type all boldface characters exactly as they appear. For example:

  Type: **SHOW DEV**

- Screen messages are displayed in a different typestyle, as follows:

  Printer attached to terminal? (Y/N) [N]:

- Key names are in **boldface** and shown in angle brackets. For example:

  <RETURN>
  <TAB>
  <CTRL> c

- Interactive sequences that include computer input and output are shown as follows:

  Printer attached to terminal? (Y/N) [N]: **Y**
  Initializing...

- Variable typed entries, or text you must replace, are shown in *italics*. In the following example

  Type: **COPY M*xxu*:*.* *xxxxxx*::*/LOG <RETURN>**

  xx and **xxxxxx** are italicized and replaced with the actual device type and name.

- Three types of notes are used in this manual: a standard NOTE, a CAUTION note, and a WARNING note.

NOTE

The standard NOTE highlights important or additional information.

CAUTION

The CAUTION note is used for situations that are potentially dangerous or destructive to data.

WARNING

A WARNING note is required if system failure or bodily injury could be involved.

1.4 Terms List

The terms list provides definitions and usage information for System Industries and industry-standard terms and acronyms used in this manual.

BBF	Bad Block Forwarding — an SI disk sector formatting process that removes a defective sector from service, and replaces it with a designated reserved sector.
BCB	Basic Control Board — contains the main microprocessor for the CLUSTOR Controller.
CI	Computer Interface — a board in the CLUSTOR Controller.
CI/M	Computer Interface — a board in the CLUSTOR/M Controller.
CI-LLA	Computer Interface Long Line Adapter — a computer interface board requiring LLA cabling to support two CPAs.
CLUSTOR	An SI mass storage subsystem that interfaces up to 16 disk drives and up to eight DEC computers.
CLUSTOR/M	New CLUSTOR controller configuration that includes at least one MSCP-compatible Computer Interface Board.
CLUSTOR (M)	This indicates that *both or either* CLUSTOR (RM-compatible) and CLUSTOR/M (MSCP-compatible) are involved.
CMI	Computer Memory Interconnect — a DEC system bus interface.
CPA	Computer Port Adapter — the computer interface for the CLUSTOR Controller.
CPA/M	Computer Port Adapter (MSCP) — the computer interface for the CLUSTOR/M Controller.
CPU	Central Processing Unit — a computer.
CRC	Cyclic Redundancy Check — verifies header fields.
CS	Control Store — a board in the CLUSTOR Controller.
DB	Display Board — contains front panel indicators for the CLUSTOR/M Controller.
DB/PM	Display Board Performance Monitor — provides extra indicators needed to monitor the DCP function.
DCP	Disk Cache Processor.

DEC	Digital Equipment Corporation.
DI	Drive Interface — a board in the CLUSTOR/M Controller.
DIP	Dual In-line Package — a bank of switches.
DMA	Direct memory access — a method of data transfer.
DQBI	CPA for Qbus system with CLUSTOR (RM).
DQBI/M	CPA for Qbus system with CLUSTOR/M (MSCP).
DSBI	CPA for SBI system with CLUSTOR (RM).
DBBI/M	CPA for BI Bus system with CLUSTOR/M (MSCP).
DUBI	CPA for UNIBUS system with CLUSTOR (RM).
Direct Format	A disk drive format arrangement where one physical drive emulates one logical drive with a defined drive geometry that uses the large capacity of SI disk drives.
Dual Channel Disk Drives	An SI option where a dual channel disk drive is accessed by two subsystems. This CLUSTOR/M configuration allows multiple computers to communicate with the same disk drive.
Dual Disk Format	A disk drive format where two physically daisy-chained disk drives emulate one logical drive with a defined geometry that uses the larger capacity of two SI disk drives.
ECC	Error Correction Code — a means for repairing data fields.
EPROM	Erasable Programmable Read Only Memory — an integrated memory circuit.
FCC	Federal Communications Commission — the organization responsible for regulating communications.
Flush	An action by the DCP that records cached write data on the disk under a Phase condition.
FLSHINT or Flush Interval	A DCP parameter that defines the maximum amount of time a phase condition exists. When the flush interval elapses, the DCP flushes the cached data. The flush interval default value is 10 seconds.
Gbyte	Gigabyte — a billion bytes of data.
I/O	Input/Output — a data path.
LED	Light Emitting Diode — an indicator light.

LLA	Long Line Adapter — allows internal/external cable length maximum of 200 feet between CLUSTOR and the CPA at the host controller.
Mapped Format	A disk drive format arrangement where one physical drive emulates one or two logical drives of the same geometry as a DEC RM-type disk drive.
MAXREQ or Maximum Request Size	A DCP parameter that defines the maximum number of sectors cached per request. A write or a read request of more sectors than MAXREQ that is serviced by a direct write or read to the disk drive, without using cache.
MByte	Megabyte — a million bytes of data.
MINREQ or Minimum Request Size	A DCP parameter that defines the minimum number of sectors read from the disk into the cache for any host read request. The default is 8 sectors. This is a look-ahead feature that increases the hit rate in cache of sequential data reads.
MTBF	Mean Time Between Failure — a measure of device reliability.
MTTR	Mean Time To Repair — a measure of responsiveness to failures.
NEMA	National Electronic Manufacturing Association — a professional organization.
Phase	A condition occurring under Write Back in which the DCP cache holds write data that is not yet recorded on the disk.
PDU	Power Distribution Unit — a means of distributing AC power.
Read-Check	A DCP operation where the DCP compares every read from disk with its cache data. Read-Check slows overall functioning because of the time involved in verification and is not recommended for normal operations.
SBI	Synchronous Backplane Interconnect — a DEC system bus interface.
SI	System Industries.
SMD	Storage Module Drive — a standard disk interface.
SW*x*	Switch — *x* is a variable.
VAX	Virtual Address Extension — a DEC CPU.

Write Back	A DCP operation — write data is temporarily stored in DCP cache and successful disk-write status is returned to the host. The WBAREA defines the boundaries of the disk that allows write back operation.
WBAREA or Write Back Area	A DCP parameter that defines the boundaries of each disk drive where the DCP write back operation is allowed. Default boundaries are Cylinder 0, Head 0, Sector 0 through the last cylinder, head, and sector of each disk drive enabled for caching.
WBMAX or Write Back Maximum	A DCP parameter that defines the maximum number of write back sectors per disk drive enabled for caching before a flush occurs. The default maximum is 20 sectors per drive.
Write Check	A command to CLUSTOR causing the controller to validate the disk data.
Write-Through-With-Allocate	A DCP operation where write data is written simultaneously to the DCP cache and the disk drive. Data is then available for a read from cache and no Phase condition occurs.
Wx	(Wire) jumper — x is a variable.
ZIF	Zero Insertion Force.
2500	Refers to the CLUSTOR Controller excluding the DCP. i.e; The DCP requests the 2500 data path.

1.5 Materials Needed

Installation procedures described in this manual require a standard tool box. Verification and repair procedures require the use of SI diagnostic program SIDOS, or the ASIST formatting tool.

2
CLUSTOR SUBSYSTEM

This chapter explains features and options available with the CLUSTOR subsystem, and describes the subsystem components, controls, and configurations. The CLUSTOR family series of mass storage subsystems is available in four versions: CLUSTOR 3 and 5 and CLUSTOR/M 3 and 5.

CLUSTOR 3 and 5 provide RM-compatibility for up to eight DEC VAX computers and up to eight logical (16 physical) disk drives.

CLUSTOR/M 3 and 5 provide MSCP-compatibility for up to four DEC VAX computers and up to seven logical (14 physical) disk drives.

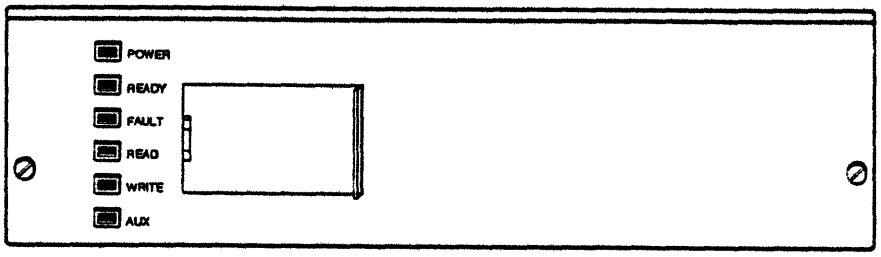
CLUSTOR/M 5 includes a Performance Monitor and cache memory in an integrated Disk Cache Processor.

The CLUSTOR subsystem also operates within an established DEC cluster. Using an Ethernet, the CLUSTOR subsystem clusters independent DEC CPUs.

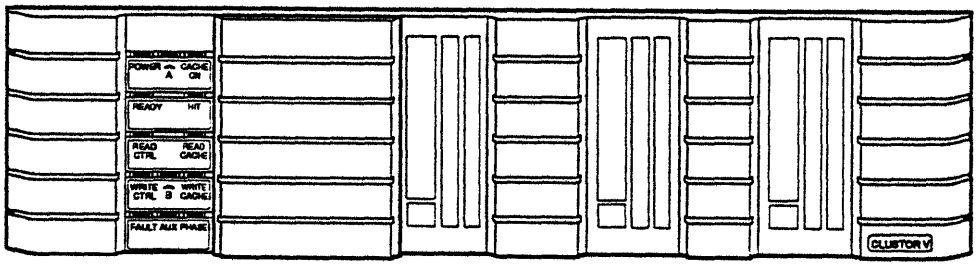
NOTE

CLUSTOR/M is used to refer to a configuration that includes at least one MSCP connection. A CLUSTOR/M configuration may be all MSCP-compatible, or may include a combination of MSCP and RM connections.

The CLUSTOR front panels in 19-inch wide formed metal and 21-inch wide molded plastic (Theta) versions are shown in Figure 2-1 and Figure 2-2.

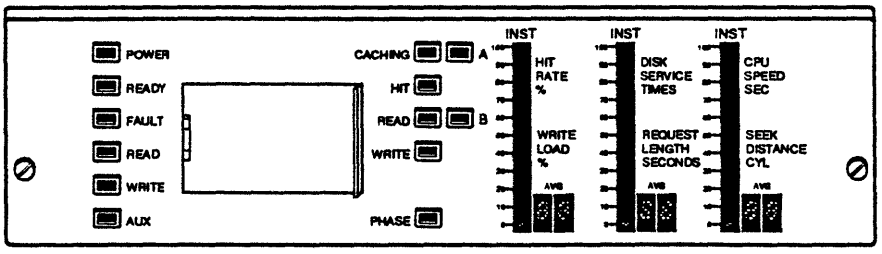


19-INCH WIDE FRONT PANEL

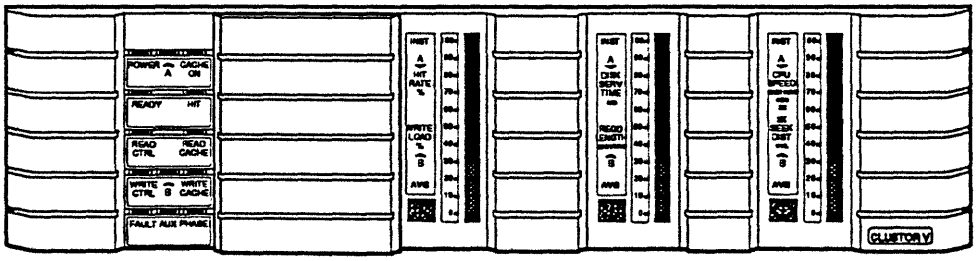


21-INCH WIDE FRONT PANEL

Figure 2-1. CLUSTOR 3(M) Front Panel



19-INCH WIDE FRONT PANEL



21-INCH WIDE FRONT PANEL

Figure 2-2. CLUSTOR 5(M) Front Panel

NOTE

A **limited** version of CLUSTOR (CLUSTOR 1) was previously produced; this configuration is **no longer available**. CLUSTOR 1 supported only 2 CI and 2 DI boards. Those with existing CLUSTOR 1 subsystems should use CLUSTOR 3 information throughout this manual.

2.1 Features

CLUSTOR controller features are described below. Refer to "Configurations" for the specific controller subsystem requirements.

- **Concurrent Command Processing**
  CLUSTOR services one to eight computers; CLUSTOR/M services one to four. It performs concurrent command processing using an interrupt driven command queue. Also, CLUSTOR and CLUSTOR/M allow multiple computer port accesses without software changes to the computer operating system. This means the computer has more than one access to the same CLUSTOR controller.
- **RM Compatibility**
  The CLUSTOR subsystem supports one to eight logical DEC RM-type disk drives. CLUSTOR uses three disk drive formats: direct, mapped, and dual disk. All formats use Bad Block Forwarding (BBF) sector scheme and incorporate Cyclic Redundancy Check (CRC) bytes in the header field and Error Correction Code (ECC) bytes in the data field.
- **MSCP Compatibility**
  The CLUSTOR/M subsystem supports one to seven logical MSCP-type disk drives. Drive formats, Bad Block Forwarding (BBF), Cyclic Redundancy Check (CRC), and Error Correction Code (ECC) are also supported.
- **Controller Operation**
  Controller processing is based on the MC68010 architecture. The controller utilizes a high-speed Direct Memory Access (DMA) sequencer and a data buffer of 64 sectors (16 Kilo-words) that allows multiple data block reads or writes. CLUSTOR (M) performs data buffer parity checks and header verification on nonformat write or read operations. The controller directs overlapped seeks during multiple disk accesses, implied seeks, and automatic head switches. Additionally, CLUSTOR (M) has resident diagnostics, power fail detection, and error code maintenance indicators.

- **Data Caching (CLUSTOR 5 and CLUSTOR/M 5 Only)**
  The CLUSTOR 5 and CLUSTOR/M 5 Controllers have an integrated Disk Cache Processor (DCP) and performance monitor (PM) that supply over 8 Mbytes of high-speed cache memory. The DCP reduces overhead by storing data from frequently accessed areas in its memory. The PM monitors DCP activity and provides real-time information used to optimize the caching parameters to suit the application. CLUSTOR 5 and CLUSTOR/M 5, with its DCP/PM, significantly improves the efficiency of data retrieval from disks.

2.2 Options

The options available with the CLUSTOR subsystems are discussed below.

- **Dual Channel Disk Drive**
  The dual channel disk drive option allows two CLUSTOR (or CLUSTOR/M) subsystems to communicate with the same disk drive. Both CLUSTORs can interface with the same computer for redundant configurations or separate computers for dual-CPU access. An additional disk drive board or other minor modification to the disk drive is required for this option. Also, both CLUSTORs and all drives must be contained in the same cabinet.

- **Long Line Computer Interface Adapter (RM-emulation only)**
  The Long Line Adapter (LLA) allows a total internal and external cable length of 200 feet (60 m) between CLUSTOR and the CPA at the host computer. High-speed, differential, tri-state bus/line drivers and receivers provide a terminated and balanced transmission system for the LLA. The adapter has its own chassis with power supply and can stand alone, mount in the computer cabinet, or mount in an expansion cabinet.

NOTE

The Long Line Adapter is not available with MSCP-emulation. Total cable length in a CLUSTOR/M configuration cannot exceed 80 feet (25 m).

- **CLUSTOR Upgrades**
  Any CLUSTOR can be upgraded in the field to a higher level CLUSTOR controller. Refer to "CLUSTOR Upgrade Installation" for more information.

2.3 Subsystem Components

This section describes the CLUSTOR subsystem components and its indicators and controls. The CLUSTOR subsystem consists of six major component groups:

- Controller chassis
- Controller boards
- Computer port adapters (CPA)
- Disk drives
- Cabling
- Cabinets

CLUSTOR Chassis

The chassis mounts on slide rails in a standard EIA 19-inch equipment rack. Chassis dimensions are 19 x 20 x 5.19 inches (48.3 x 50.8 x 13.2 cm) and requires 5.25 inches (13.3 cm) of vertical rack space. The CLUSTOR (M) chassis consists of three items:

- Power supply
- Fan
- Controller boards

The CLUSTOR (M) chassis contains the controller boards and supporting components. Its front panel has a door providing access to the firmware EPROMs, activity lights, and control switches on the Control Store (CS) board. A label on the inside of the front panel door shows locations and functions of the indicators and switches. The AC power receptacle is at the rear of the chassis, along with the I/O cable access.

The CLUSTOR (M) chassis is shown in Figure 2-3.

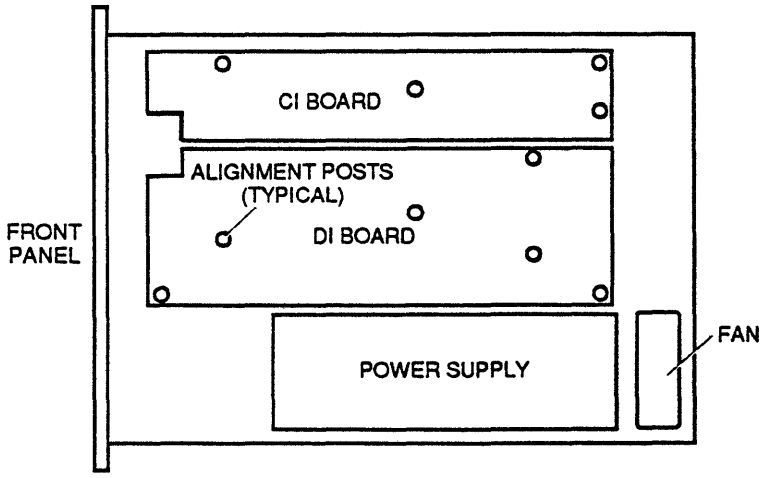


Figure 2-3. CLUSTOR (M) Chassis Components

Power Supply

The power supply is a nonlinear (switching) unit located on the right side of the chassis. A switch at the top rear of the power supply selects the input AC voltage, either 90 — 132 VAC or 180 — 264 VAC. The unit supplies the necessary DC power to the fan and boards in the CLUSTOR chassis. There are no field level power adjustments for this unit.

Fan

The fan is located at the rear of the chassis, directly behind the power supply. It is a DC cooling fan that draws air from the chassis.

CLUSTOR 3 and CLUSTOR/M 3

Cabling and direct connections between the CLUSTOR 3 and CLUSTOR/M 3 subsystem boards are described below. Block diagrams are shown in "Configurations."

- The BCB contains the main microprocessor for the CLUSTOR 3 or CLUSTOR/M 3 controller.
- The CS board connects directly to the BCB and contains the EPROM firmware that provides the microprocessor with operating instructions. The CS board interfaces with each CI or CI/M board, passing interrupt information to the BCB.
- The DB displays status information on the front panel.
- The CI or CI/M board connects the Computer Port Adapter (CPA or CPA/M) to the BCB. The CI or CI/M connects directly to the BCB through a zero-insertion-force (ZIF) connector. Each CI or CI/M also connects to the CS through a cable.
- The DI boards connect the disk drives to the BCB. The DI connects directly to the BCB through a ZIF connector.

CLUSTOR 5 and CLUSTOR/M 5

CLUSTOR 5 and CLUSTOR/M 5 include the same controller boards as CLUSTOR 3 plus the following boards. Block diagrams are shown in "Configurations."

- A DB/PM board that provides the extra indicators needed to monitor the DCP function.
- A DCP board that caches data for faster throughput.

  The DCP board connects directly to the BCB and CIs through a ZIF connector, and to the CS board through a cable. The DCP passes the DI ZIF bus for DI boards stacked above the DCP. The DCP does not use the DI ZIF bus. CLUSTOR 5 and CLUSTOR/M 5 use 8 Mbytes of cache

2.4 CLUSTOR (M) Subsystem Boards

CLUSTOR board links are consistent throughout the CLUSTOR family. CLUSTOR 3 and CLUSTOR/M 3 boards make up the basic system. CLUSTOR 5 incorporates CLUSTOR 3 along with the DCP and the PM boards; CLUSTOR/M 5 incorporates CLUSTOR/M 3 along with the DCP and PM boards. Controller interface boards for the computers and the disk drives stack above the basic control board on alignment posts of the main chassis inner bottom plate.

CLUSTOR and CLUSTOR/M controllers consist of the following boards:

- Basic Control Board (BCB)
- Display Board (DB) - CLUSTOR 3 and CLUSTOR/M 3, or Display Board/Performance Monitor (DB/PM) - CLUSTOR 5 and CLUSTOR/M 5
- Control Store (CS) board
- Computer Interface (CI or CI/M) board
- Computer Interface — Long Line Adapter (CI-LLA) Board
- Disk Interface (DI) board
- Disk Cache Processor (DCP) board - CLUSTOR 5 and CLUSTOR/M 5

Basic Control Board

The BCB mounts on the base of the chassis with the components facing the bottom cover plate. BCB dimensions are approximately 18 x 19 inches (45.7 x 48.3 cm). The BCB is shown in Figures 2-4 and 2-5.

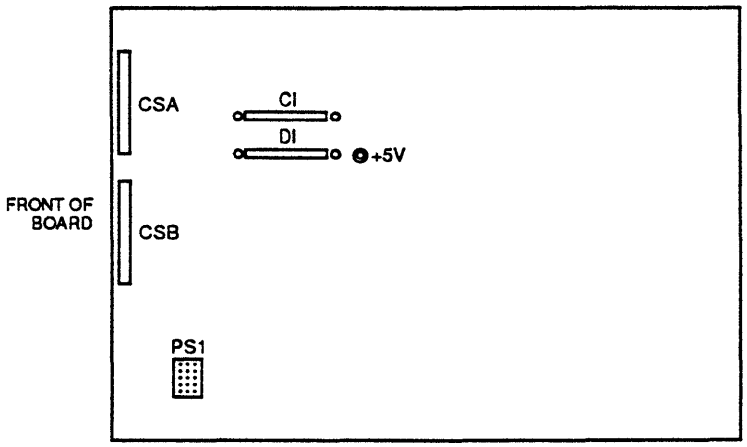


Figure 2-4. Basic Control Board, Top View

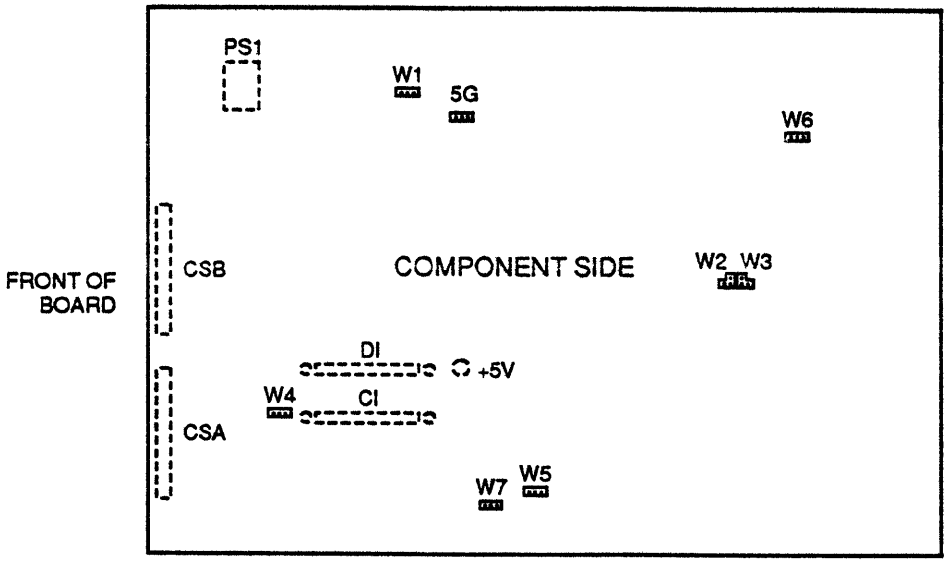


Figure 2-5. Basic Control Board, Bottom View

The BCB contains the microprocessor that directs the controller operation. The BCB gets operational memory information and host interrupt information from its direct connection to the CS board. The BCB directs the use of the common bus (represented by the ZIF connectors) between the BCB, the CIs, and the DIs.

The BCB receives power from the power supply through the PS1 connector and then routes it to all boards. Two alignment pins are near the ZIF connector. The alignment pin closest to pin 1 of the DI ZIF connector carries +5V from the BCB to all DI boards.

The BCB contains five connectors:

- CI ZIF and DI ZIF — Two 60-pin ZIF connectors connect the BCB to the CI and DI board stacks. The DCP of a CLUSTOR 5 also connects to the BCB through the ZIF connectors.
- CSA and CSB — Two 96-pin connectors plug the CS board into the BCB.
- PS1 — Connects the power supply to the BCB.

BCB jumpers define the board's configuration. Refer to "Ready Reference" for jumper settings.

Display Board

The DB contains the front panel indicators and mounts on the rear of the chassis front panel. There are two versions: the DB used with CLUSTOR 3 and CLUSTOR/M 3 and the DB/PM used with CLUSTOR 5 and CLUSTOR/M 5. The board dimensions are 18.94 x 5.19 in. (44.11 x 13.18 cm).

The DB has a 40-pin connector, P3, that cables to the CS board to receive information displayed on its indicators. The DB display supplies the operator with current information on controller activities.

Both versions have a space (4.5 x 2.5 inches) located near the left side. This space allows the user to get to the CS board indicators and switches.

Both versions of the DB panels are shown in Figure 2-6.

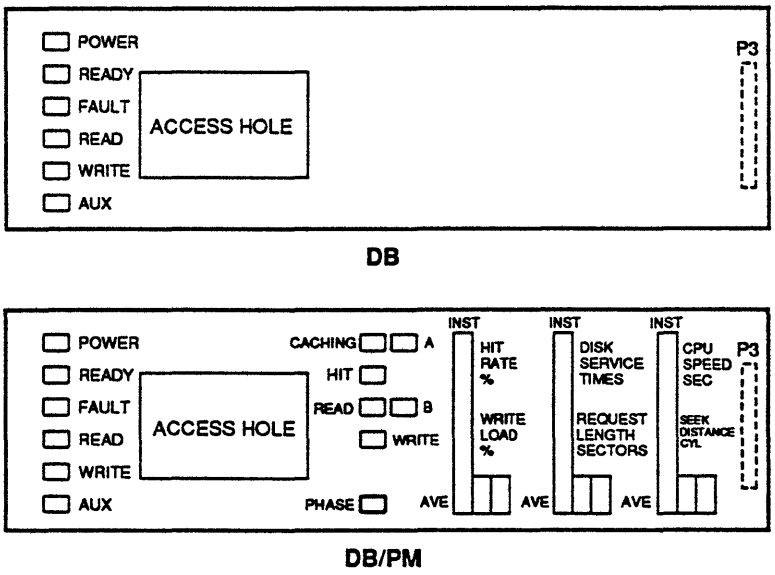


Figure 2-6. Display and Display/Performance Monitor Panels

DB Indicators for CLUSTOR 3 and CLUSTOR/M 3

The DB for CLUSTOR 3 and CLUSTOR/M 3 contain a column of indicator LEDs for these functions:

POWER	Controller is powered on
READY	Successful completion of controller power-on diagnostics
FAULT	Controller (BCB) microprocessor fatal error
READ	Disk read operation
WRITE	Disk write operation
AUX	ECC error, CRC error, or host computer powered down (non-fatal error)

DB/PM Indicators for CLUSTOR 5 and CLUSTOR/M 5

The DB/PM for CLUSTOR 5 and CLUSTOR/M 5 contain the same basic indicators discussed for the DB. Additionally, it contains the PM indicator LEDs for these functions:

CACHING	Caching is enabled; blinks when idle; solid when cache is processing a request.
HIT	Cache contains the requested read data
READ	Disk read request from host
WRITE	Disk write request from host
PHASE	Cache contains write data not written to the disk
A or B	A or B parameters display on the bar graph indicators

To the right of the LED indicators, the DB/PM displays three bar graphs. These are dual-function 101 segment LEDs that indicate the average value of the parameter over the last 32 requests. Each bar graph contains a peak indicator that is cleared every 60 seconds (default setting).

Next to each bar graph are two hexadecimal displays. Once per second, these displays are updated with the average value of the parameter since the last reset. The CS board display select switch selects either the A or the B parameters for display. The parameters are:

A Parameters

Hit Rate (%)	Percentage of read requests found in cache.
Disk Service Time (ms)	Actual time, in milliseconds, the disk system used from the moment the host posted the disk request until completion of that request, including data transfer time.

CPU Speed (Disk Requests/Sec.)	Disk requests per second being serviced. The display value is half the actual speed. CPU speed is inversely proportional to the sum of the time the CPU waits for disk completion plus the time between disk requests.

B Parameters

Write Load (%)	Percentage of write requests to total requests.
Request Length (Sectors)	The request length in sectors.
Seek Distance (Cylinders)	The seek distance, in cylinders, that the disk drives seek. The actual number of cylinders is 10 times the displayed value.

Control Store Board

The CS board has two 96-pin connectors that plug into the front of the BCB. The CS board stands vertical to the BCB and parallel behind the DB. The CS board dimensions are 10.5 x 3.5 inches (26.67 x 8.9 cm). It contains the firmware EPROMs, activity lights, and control switches accessible through the front panel door. The CS board is shown in Figure 2-7.

The CS board supplies the BCB with operating information from the CS EPROMs. The CS provides interrupts to the BCB from the CIs and the DCP of a CLUSTOR 5 or CLUSTOR/M 5. Also, the CS provides the indicator LED bank and control switches.

The CS board contains seven connectors:

CSA and CSB	Two 96-pin connectors that plug the CS board into the BCB.
J1	A 60-pin connector that cables to the DCP board.
J2	A 26-pin connector that cables to all CI or CI/M boards.
J3	A 40-pin connector that cables to the DB.
J4	A 6-pin connector that cables to the RS232-C port at the rear of the chassis.
J5	Not used.

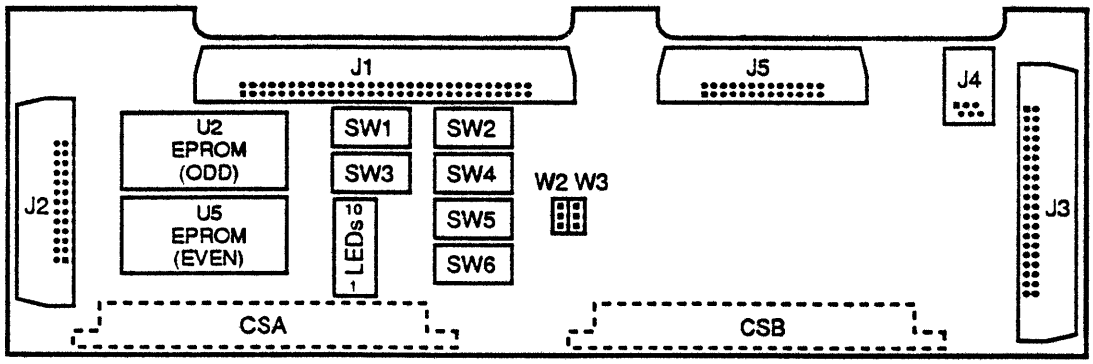


Figure 2-7. Control Store Board

The CS board has a vertical bank of 10 LEDs that indicate controller functions. While the BCB microprocessor is operating, the LED bank indicates if a command is active or waiting, and disk drive address.

LED 1 lights to indicate a microprocessor halt, with the other LEDs displaying the error code. LED 1 is at the bottom of the bank. Refer to "Subsystem Troubleshooting" for more error code information. The CS board has seven switches that are defined below:

Format (SW1)	Enable/Disable formatting. In the Enable position, the controller allows disk formatting (header write functions).
Display Select (SW2)	Selects the A or B parameters for display on the DB/PM indicators (CLUSTOR 5 and CLUSTOR/M 5 only).
Controller Reset (SW3)	This momentary switch initializes the controller. The DCP of a CLUSTOR 5 or CLUSTOR/M 5 sends cached write data to the drive and then reinitializes.
Caching (SW4)	Enable/Disable caching. In the Enable position, the DCP caches data (CLUSTOR 5 or CLUSTOR/M 5 only).
Cache Reset (SW5)	This momentary switch initializes the DCP by causing power-on diagnostics to run.
Com Port (SW6)	Selects the RS232-C port connection to either the DCP or the CLUSTOR Controller (BCB) (CLUSTOR 5 or CLUSTOR/M 5 only).

CS board jumpers define the com port signal pin configuration. Refer to "Ready Reference" for jumper settings.

Located near the LED bank, the three test points on the CS board are:

TP1	+5V
TP2	Ground
TP3	-5V

The firmware EPROMs, U2 and U5, are in sockets to facilitate update changes. Pin 1 of each chip is at the upper right.

Computer Interface Board

There are three types of CI boards. The SI-proprietary CI board provides RM-compatibility and supports up to two SI host CPA boards. This CI board is available in either Standard or Long Line options.

The CI/M board provides MSCP-compatibility and supports one SI host CPA/M board each. This CI/M board is available in the Standard option only.

As you are facing the chassis, the CI and CI/M boards stack on the left side of the chassis. Board dimensions are 4 x 18.5 inches (10.2 x 47 cm).

SI Computer Interface Board (RM)

The SI CI board provides host interface logic for two independent CPAs. J1 carries the CLUSTOR controller signals and J2 carries the Direct Memory Access (DMA) data and control signals for the even CPA. J3 carries the controller signals and J4 the DMA signals for the odd CPA.

The CI board sends interrupts via J5 and the CS board to the BCB. The ZIF connector provides the data and control communication path between the CI and the BCB. The Computer Interface-Long Line Adapter (CI-LLA) board is used with the Long Line Adapter (LLA) option. The SI CI board is illustrated in Figure 2-8.

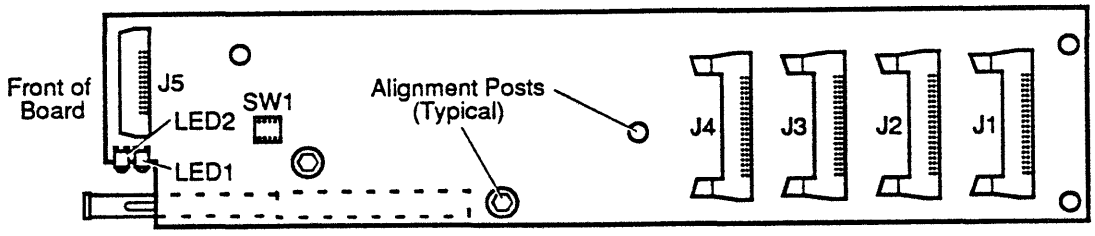


Figure 2-8. SI Computer Interface Board

The SI CI board has six connectors:

J1 and J2	Two 40-pin connectors that cable to the even CPA supported.
J3 and J4	Two 40-pin connectors that cable to the odd CPA supported.
J5	A 26-pin connector that cables to the CS board.
ZIF	A 60-pin ZIF connector that matches with the BCB ZIF connector.

Each CI board is addressed by a unique port address for each supported CPA. The CI board switch SW1 determines the board's port addresses. The two on-board LEDs, LED1 and LED2, light to indicate the board's port address selection. Refer to "Ready Reference" for switch settings and LED indications.

SCSI Computer Interface Board (MSCP)

The SCSI CI board provides interface logic for one MSCP host adapter connection. The CLUSTOR/M can look like seven logical units, each with a unique ID. J1 provides for a connection of up to eight feet. J2 provides for a connection of up to 80 feet. The ZIF connector provides the data and control communication path between the CI/M and the BCB. PC1 provides power and ground. J3 provides for interrupts between the CS board and the CI/M board.

Each CI/M board is addressed by a unique port address. Switch SW1 determines the board's port address. Two of the three LEDs on board, LED2 and LED3 (both red), light to indicate the board's port address selection. LED1 lights up to indicate successful completion of power-up diagnostics. Refer to "Configuration Settings" for switch settings and LED indications. The SCSI CI board is shown in Figure 2-9.

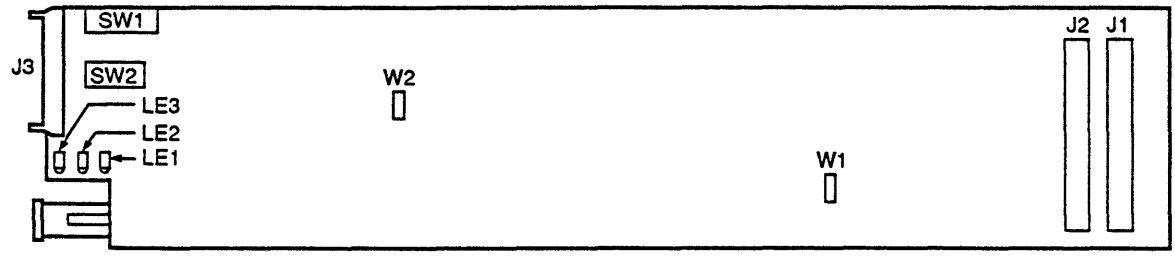


Figure 2-9. MSCP Computer Interface Board

Drive Interface Board

The DI board stacks in the center of the chassis, between the CI or CI/M board and power supply. Its dimensions are 6.5 x 18.5 in. (16.5 x 47 cm). The DI board is shown in Figure 2-10.

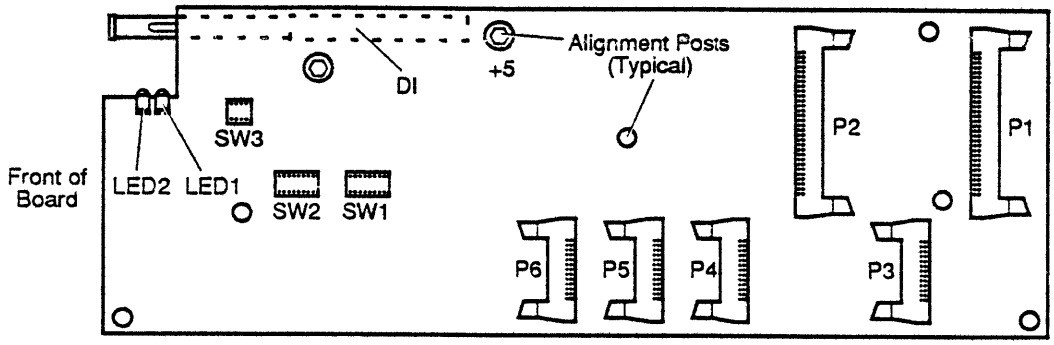


Figure 2-10. Drive Interface Board

The DI communicates with the disk drives through standard SMD cables. The DI uses the ZIF connector as the communication path with the BCB.

Two alignment pins are near the ZIF connector. The alignment pin closest to pin 1 of the ZIF connector on the DI board carries +5V from the BCB to all DI boards.

The DI board has seven connectors:

P1	A 60-pin SMD A-connector, with P3 and P4, cables to the even disk drive circuit.
P2	A 60-pin SMD A-connector, with P5 and P6, cables to the odd disk drive circuit.
P3	A 26-pin SMD B-connector cables to drive 0 of the even disk drive circuit.
P4	A 26-pin SMD B-connector cables to drive 1 of the even disk drive circuit.
P5	A 26-pin SMD B-connector cables to drive 0 of the odd disk drive circuit.
P6	A 26-pin SMD B-connector cables to drive 1 of the odd disk drive circuit.
DI ZIF	A 60-pin ZIF connector matches with the BCB ZIF connector.

Each DI board has two independent disk drive circuits. Each circuit can support one radially connected disk drive, or two daisy-chained disk drives. Daisy-chained disk drives are formatted in the dual drive format and appear as one logical drive. SW1 and SW2 specify the drive format and other parameters. SW1 identifies the even drive circuit; SW2 identifies the odd drive circuit.

Each DI board is addressed by a unique port address for each of its supported disk drive circuits. The DI board switch SW3 determines the board's port addresses. The two LEDs on the board, LED1 and LED2, light to indicate the board's port address selection.

See "Ready Reference" for the switch settings and the LED indications.

Disk Cache Processor Board

The DCP board stacks over both the CI and DI board stacks of CLUSTOR 5 or CLUSTOR/M 5. The DCP is always placed as the top board in the CI or CI/M stack. If there are fewer DI boards than CI or CI/M boards, the DI board stack is evened out by excess DI boards to maintain the +5 Volt power source. If there are more DI boards than CI, or CI/M then the excess are stacked above the DCP.

The DCP board dimensions are 19.5 x 8.5 inches (49.53 x 21.59 cm). The DCP board is shown in Figure 2-11.

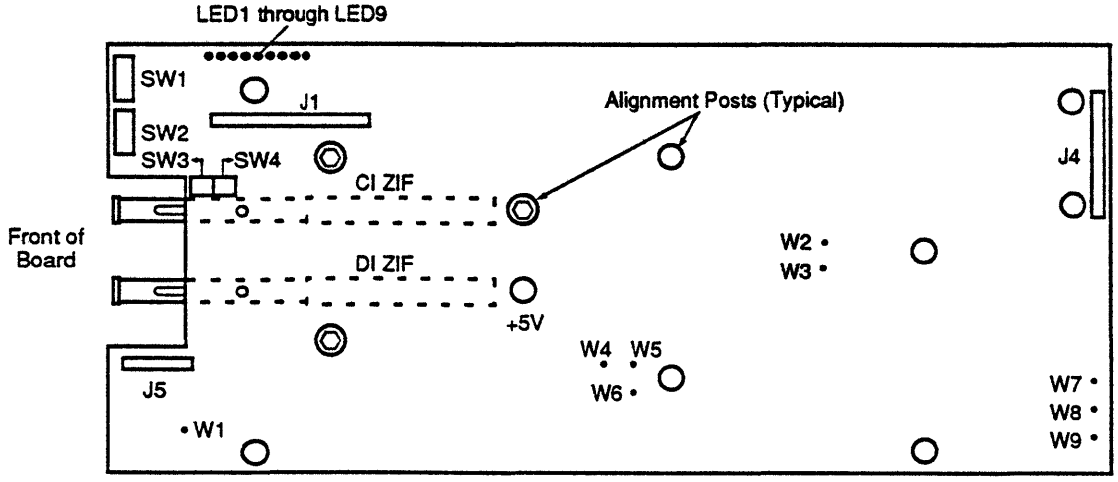


Figure 2-11. Disk Cache Processor Board

The DCP board in CLUSTOR 5 or CLUSTOR/M 5 provides a microprocessor controlled data cache. The DCP connects directly to the CS board and to the BCB, DIs, and CIs through the ZIF connector. A host request from a CPA goes to the CS board by means of the CI or CI/M board. In CLUSTOR 3, the CS board then interrupts the BCB.

In CLUSTOR 5 or CLUSTOR/M 5, the DCP receives the interrupt and responds to the request for any disk drive that is enabled for caching. If enabled for write backs, the DCP caches write data as it is transferred from the host and writes it to disk later. For a read request, the DCP reads the minimum number of sectors and caches the read data as it is read from the disk. Only the requested sectors transfer to the host. Subsequent read requests are serviced by the DCP from its cached data.

The DCP has five connectors:

J1	A 60-pin connector cables to the CS board J1.
J2	A 60-pin ZIF connector matches to the CI ZIF.
J3	A 60-pin ZIF connector matches to the DI ZIF.
J4	A 50-pin connector reserved for factory use.
J5	A 26-pin connector — not used

On the DCP, the nine LEDs indicate DCP operations and internal diagnostics tests. LED1 lights to indicate a DCP processor halt. Refer to "Ready Reference" for LED indications.

The DCP parameters, including enabling the cache, are defined by DIP switch SW1. Each logical disk drive is individually enabled or disabled for caching by the DIP switch SW2. The two momentary switches on the DCP each initiate a DCP only reset. SW3 initiates a firmware reset. SW4 initiates a hardware reset and a firmware restart.

When LED1 indicates a DCP processor halt, use SW4 or the cache reset switch on the CS board, to reset the DCP and restart the firmware on the board. Refer to "Ready Reference" for the switch settings.

Jumpers W1 through W9 define the DCP installed memory size and similar characteristics. Jumpers W10 through W17 are configured at the factory. Refer to "Ready Reference" for the jumper settings.

2.5 Computer Port Adapters

The CPA interfaces the DEC computer with the CLUSTOR controller at the CI board. The type of adapter depends on the computer and bus used. The CPA mounts in the CPU backplane, expansion area, or UNIBUS or SBI expansion cabinet. The following CPAs are available with the CLUSTOR controller:

- **UNIBUS (RM-compatible)**
  A single board CPA that mounts in the UNIBUS of the following DEC CPUs: 11/725, 11/730, 11/750, 11/780, 11/782, 11/785, 8200, 8250, 8300, 8350, 8600, 8650.
- **QBUS (RM-compatible)**
  A single board CPA that mounts in the QBUS of the DEC MicroVAX II, MicroVAX 3300-3900, and VAX 4000.
- **QBUS (MSCP-compatible)**
  A single-board CPA that mounts in the QBUS of the DEC MicroVAX II, MicroVAX 3300-3900, and VAX 4000. It supports MSCP transparently through DUDRIVER.
- **SBI (RM-compatible)**
  A multiple board CPA with its own card cage that mounts in a MASSBUS slot of the following DEC CPUs: 11/780, 11/782, 11/785, 8600, 8650.
- **BI BUS (MSCP-compatible)**
  A single board CPA that mounts in the BI Bus of the following DEC CPUs: VAX 6xxx, VAX 8xxx except for 8600 and 8650.

The RM-compatible CPA works with the CLUSTOR subsystem; the MSCP-compatible CPA/M works with the CLUSTOR/M subsystem. Each CPA has switches and jumpers that define operational parameters. Specific switch and jumper values for the CPAs are given in Appendixes B through F.

The computer operating systems supported with these CPAs and CPA/Ms are listed in Table 2-1.

NOTE

Verify operating system support with the configuration guide, since this manual is not updated after every software release.

Table 2-1. Computer Operating Systems Supported

TYPE	RELEASE LEVEL
VMS	4.4 through 4.7, 5.0 through 5.4-2
ULTRIX	2.0 through 3.1
UNIX BSD	4.3
AT&T UNIX	5.2

2.6 Disk Drives

The disk drives mount in the same cabinet assembly with the CLUSTOR controller. The disk drives vary in size and mounting methods. All the disk drives use SMD or SMD-compatible interfaces. In CLUSTOR/M, the drives remain SMD. All SCSI conversion takes place on the SCSI Computer Interface PCB.

Disk drives and mounting types are listed in Table 2-2.

Table 2-2. Disk Drive Size and Mounting Type

DRIVE	DISK SIZE	MOUNTING TYPE
SI56* SI57* SI506	5.25-inch	Two Drive Quick Release
SI510	5.25-inch	Two Drive Fixed Tray
SI83* SI817	8-inch	Two Drive Quick Release
SI85* 9733* SI92* SI95*		Two Drive Fixed Tray
SI93	9-inch	Two Drive Fixed Tray
9751* 9761*	10.5-inch	Cabinet Mount
SSD67 SSD130 SSD260 SSD452	19-inch	Cabinet Mount

* Not available for new system orders.

Depending on the drive type and application, disk drives are configured in one of the following formats:

Mapped — One physical drive emulates one or two logical drives of the same geometry as a DEC RM05 disk drive.

Direct — One physical drive emulates one logical drive with a defined drive geometry that uses the larger capacity of SI disk drives.

Dual Disk — Two physical disk drives are daisy-chained and emulate one logical drive with a defined drive geometry that uses the larger capacity of two SI disk drives. Dual disk format is not available with the SI56, SI57, and SI506 disk drives.

When formatted as direct or mapped, a single disk drive attaches radially to the DI board and the drive SMD address is 0. When formatted dual disk, two disk drives attach through a daisy-chained control cable to the DI board. The first drive is SMD address 0 and the second drive, with the control cable terminated, is SMD address 1.

Dual disk configurations require identical drive models for the daisy-chain. Daisy-chained drives must be in the same quick release chassis, the same dual tray, or nearby in the same cabinet for cabinet mounted drives. The supported disk drives and their formatted capacities are listed in Table 2-3.

Table 2-3. Supported Disk Drive Capacities

DRIVE	UNFORM CAP	FORMAT	LOGICAL UNIT PARAMS				RATIO OF PHYS/LOG	RM DEV DRIVER REQ
			CYL	HEAD	SEC	CAP		
9733*	337MB	Mapped	823	19	32	256MB	1 to 1	No
9751*	474MB	Direct	840	20	47	405MB	1 to 1	Yes
		Dual Disk	1680	20	47	810MB	2 to 1	Yes
9761*	689MB	Direct	840	20	64	551MB	1 to 1	Yes
		Dual Disk	1680	20	64	1102MB	2 to 1	Yes
SI56*	384MB	Direct	1222	15	32	300MB	1 to 1	Yes
SI57*	768MB	Direct	1630	15	48	601MB	1 to 1	Yes
SI83*	690MB	Direct	622	27	64	552MB	1 to 1	Yes
		Mapped	823	19	32	256MB	1 to 2	No
		Dual Disk*	1244	27	64	1.10GB	2 to 1	Yes
SI85*	823.9MB	Direct	743	27	64	659MB	1 to 1	Yes
		Mapped	823	19	32	256MB	1 to 2	No
		Dual Disk*	1486	27	64	1.31GB	2 to 1	Yes
SI92*	1.1GB	Direct	1633	15	70	878MB	1 to 1	Yes
		Dual Disk*	3266	15	70	1.75GB	2 to 1	Yes
SI93*	1173MB	Direct	1022	27	64	900MB	1 to 1	Yes
		Dual Disk*	2044	27	64	1.8GB	2 to 1	Yes
SI95*	2.2GB	Direct	1633	30	70	1.75GB	1 to 1	Yes
		Dual Disk*	3266	30	70	3.5GB	2 to 1	Yes
SI506	776MB	Mapped	823	19	32	256MB	1 to 2	No
		RM05	823	19	32	256MB	1 to 1	No
		Direct	1656	15	47	597MB	1 to 1	Yes
SI510	1200MB	Direct	2099	17	52	950MB	1 to 1	Yes
		Dual Disk	4198	17	52	1.9GB	2 to 1	Yes
SI817	2272MB	Direct	2609	19	70	1.77GB	1 to 1	Yes
		Dual Disk	5218	19	70	3.55GB	2 to 1	Yes
SSD67		Direct*	823	5	32	67MB	1 to 1	No
SSD130		Direct*	797	10	32	130MB	1 to 1	Yes
SSD260		Direct*	590	27	32	260MB	1 to 1	Yes
SSD452		Direct*	1023	27	32	452MB	1 to 1	Yes

* Not available after Dec. 1, 1990.

Bad Block Forwarding

BBF begins with the basic format of the disk drive. The disk drive is formatted into a set number of sectors. Each user-available sector is assigned a logical sector number in its header area. The host computer requests a sector by this logical sector number. More physical sectors are formatted per cylinder than logical sectors used in the emulation. The unused sectors are designated as spare or replacement blocks. As a drive is formatted, its replacement blocks are grouped together at the end of each cylinder.

Any bad sector found during formatting is marked and its logical designation is moved to the next sector. The logical designation of that sector is moved to the next sector. This "sector rippling" moves each following logical sector to the next physical sector until the last logical sector of the cylinder is moved into a replacement sector. CLUSTOR reports no bad sectors to the host computer for a newly formatted drive as *every* logical sector number is available to the computer.

Over time, a disk drive can develop bad sectors. CLUSTOR reports these bad sectors to the host computer. BBF occurs when the SIDOS diagnostic or the ASIST tool is used for a cylinder or a complete disk drive format.

The type of disk drive and its format determines the number of replacement blocks. When all the available replacement sectors of one cylinder are used, the cylinder, or the entire drive, must be reformatted, as BBF does not cross cylinder boundaries.

2.7 Cabling

The subsystem cabling forms the physical connections between the major assemblies of disk drive, controller, and CPA.

Internal Cabling

Internal cabling is contained within the cabinet. Internal cabling consists of cables connecting the disk drive to the DI board and the CI or CI/M board to the cabinet transition panel. CLUSTOR 3 and 5 use unshielded cables for these connections. Also considered internal cabling are the cables between the CPU cabinet transition panel and the CPA.

External Cabling

External cabling is exterior to the cabinet. External cabling consists of shielded cables that connect the SI cabinet transition panel to the CPU cabinet transition panel.

Disk Drive Cabling

The cabling between the disk drive and DI board consists of a pair of SMD cables: a 60-pin control cable and a 26-pin data cable. The drive cables are limited in length to 50 feet; this limit is never exceeded since the drives are in the same cabinet as the controller.

The two configurations for drive cables are radial for direct and mapped formats; and daisy-chain for dual-drive formats. In the radial arrangement, each drive has its own control and data cables with a terminator for the control cable.

In daisy-chain configurations, each drive has its own data cable, but the drives share the control cable. The first drive in the daisy-chain is unit 0 and has no terminator for the control cable. The control cable continues to unit 1 where it is terminated. Daisy-chained drives must be adjacent to each other.

Computer Interface Board Cabling

The cables from the CI or CI/M board to the internal cabinet transition panel connect through the cabinet transition panel to the external cabinet cables. The external cables connect through the CPU cabinet transition panel to the CPA internal cables. This path of CI to CPA cables consists of two 40-pin cables for CLUSTOR and one double-ended 50-pin cable for CLUSTOR/M. All external cabling is shielded and meets FCC requirements.

Long Line Adapter Cabling

The cables in an LLA option have a total cable length of 200 feet maximum. Up to 150 feet of external cables connect the SI cabinet transition panel to the LLA itself. From the LLA, 20 feet of external cables extend to the CPU cabinet transition panel. Cabinet internal cabling is the same for regular or LLA applications.

Cabinets

Due to space requirements, some CLUSTOR 3 and 5 configurations require more than a single cabinet. For these configurations, single and dual-bay cabinets are available. As you face the front of the cabinet on dual-bay cabinet arrangements, the left bay contains the transition panel.

3
CONFIGURATIONS

This chapter describes CLUSTOR configuration requirements and examples. The CLUSTOR subsystem configuration depends on the CLUSTOR controller, the computers serviced, the disk drives used and options selected. The number of disk drives, for example, affects the type of disk drive format used.

3.1 Configuration Requirements

These configuration requirements must be met to ensure CLUSTOR subsystem function:

- **Computer Port Adapters**
  Minimum of one, maximum of eight per CLUSTOR 3 or 5 controller.
  Minimum of one, maximum of four per CLUSTOR/M controller.
  In a multiport configuration, if the disk drive is mounted through both CPAs, two different device names have the same volume label. The CPU does not allow the same volume label on different device names. Thus, multiport configurations mount the disk drive on only one CPA and reserve the second CPA path until needed.
- **CPA to CLUSTOR Cabling**

  RM — Regular: 33 feet external to the cabinet, maximum of 50 feet total. Long Line Adapter Option: 150 feet external, maximum of 200 feet total. Requires a Long Line Adapter Computer Interface (CI-LLA) board.

  MSCP — Maximum total cable length is 80 feet between the CPA/M and CLUSTOR CI/M, including both internal and external cables.
- **Computer Interface Board**
  Minimum of one, maximum of four per CLUSTOR (M) controller. Each CI supports two CPAs. The CI-LLA requires LLA option for both of the CPAs it supports. Each CI/M supports one CPA/M.

- **Drive Interface Board**
  Minimum of one, maximum of four per CLUSTOR (M) controller. Each DI board has two independent disk drive interface circuits. Each independent interface circuit connects to one disk drive for both mapped and direct configurations, or to two daisy-chained disk drives for the dual-disk configuration. Dual disk configurations require identical model disk drives in the daisy-chain. Also, daisy-chained drives must be near to each other.
- **Disk Drive**
  Minimum of one, maximum of 16 per CLUSTOR 3 or 5 controller.
  Minimum of one, maximum of 14 per CLUSTOR/M 3 or 5 controller.

  RM emulation: The number of disk drives depends on the format type. The disk drive formats can be mixed, but cannot emulate more than eight logical disk drives. Configured as dual-disks only, CLUSTOR supports a maximum of 16 physical disk drives. Configured as mapped or direct only, CLUSTOR supports a maximum of eight physical disk drives. The controller(s) and all drives must be housed in the same single-bay or dual-bay cabinet.

  MSCP emulation: Disk drive formats can be mixed, but cannot emulate more than seven logical disk drives. Configured as dual-disks, CLUSTOR/M supports a maximum of 14 physical disk drives. Configured as mapped or direct, CLUSTOR/M supports a maximum of seven physical disk drives. The controller(s) and all drives must be housed in the same single-bay or dual-bay cabinet.
- **Dual Channel Disk Drive Option**
  Any disk drive configuration supports this option. The drive format must be maintained by definition on each DI connected to the disk drive. The second CLUSTOR controller must be housed in the same single-bay or dual-bay cabinet as the drives and the first controller. In redundant applications, one primary channel through the controller and CPA normally accesses the disk.

CAUTION

The second channel through the second controller is not mounted or used until the primary drive fails. This is mandatory when using CLUSTOR 5 or CLUSTOR/M 5 because the second channel path could access or cause stale data on the disk drive.

- **Cabinets**
  A single-bay or a dual-bay cabinet is used to house the CLUSTOR or CLUSTOR/M controller(s), and all disk drives. The cabinet type selected depends on the amount and type of equipment used. The physical cabinet restrictions must not be exceeded.

3.2 Configuration Examples

The CLUSTOR subsystem with external cables and CPAs can vary extensively, but always adheres to the configuration requirements.

CLUSTOR 3 and 5

CLUSTOR 3 and 5 support up to eight CPAs. Each CI interfaces with up to two CPAs. CLUSTOR 3 and 5 allow up to 16 disk drives in the dual-drive format. Each DI supports two independent drive interfaces, each controlling a single disk drive, or two drives daisy-chained in the dual-drive format.

An example of a CLUSTOR 3 configuration with 8 logical disk drives and eight CPAs is shown in Figure 3-1.

CLUSTOR 5

Subject to the same configuration requirements, CLUSTOR 5 differs from CLUSTOR 3 in the following ways:

- Display Board with Performance Monitor (DB/PM) replaces the DB.
- Disk Cache Processor (DCP) is added.

The CLUSTOR 5 subsystem in a 12-drive, 8-CPA configuration is shown in Figure 3-2.

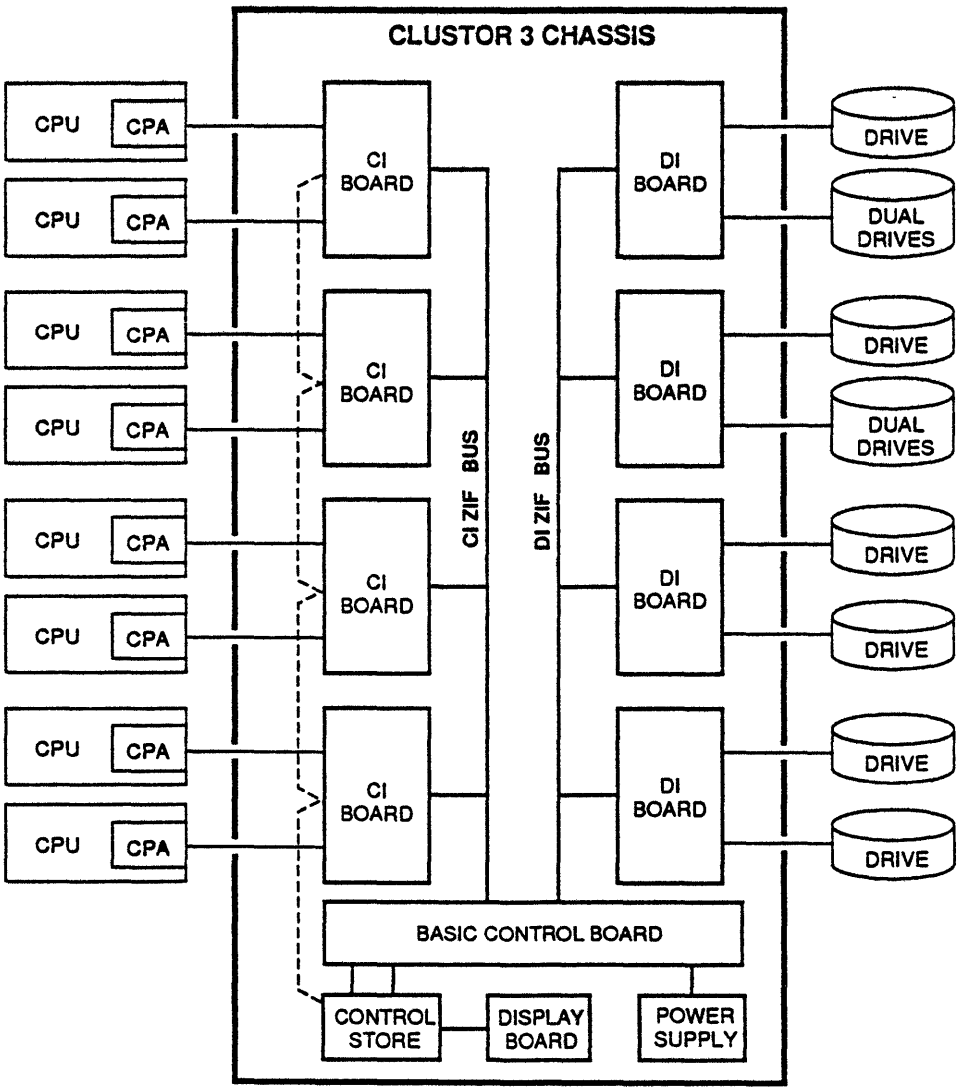


Figure 3-1. CLUSTOR 3 Subsystem (Maximum) Configuration (RM-compatible)

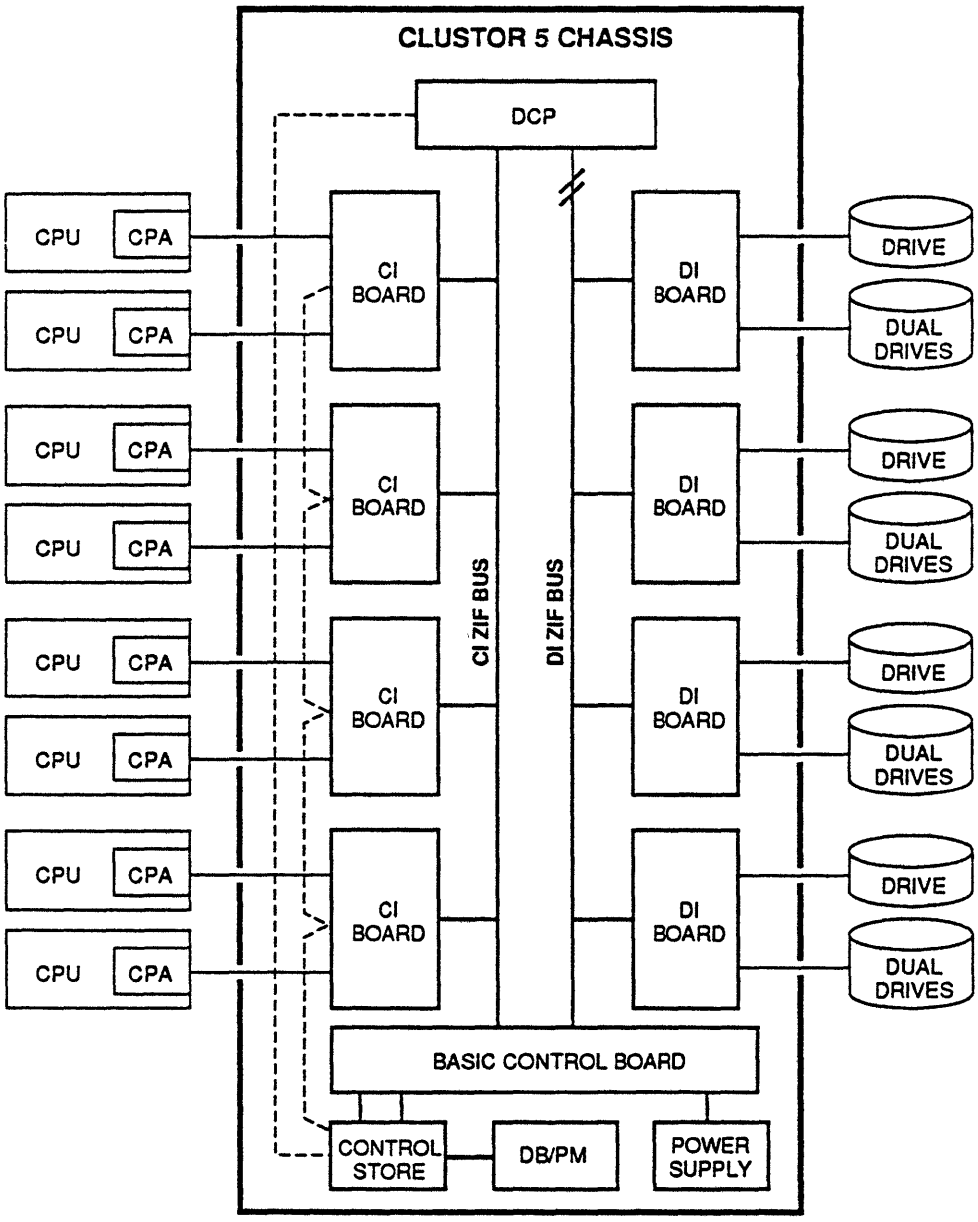


Figure 3-2. CLUSTOR 5 Subsystem (Maximum) Configuration (RM-compatible)

CLUSTOR/M 3 and 5

CLUSTOR/M 3 and 5 support up to four CPAs. Each CI/M interfaces with one CPA/M. CLUSTOR/M 3 and 5 allow up to 14 disk drives in the dual-drive format. Each DI supports two independent drive interfaces, each controlling a single disk drive; the top DI board in the stack supports only one drive.

An example of a CLUSTOR/M 3 configuration with 7 logical disk drives and four CPAs is shown in Figure 3-3.

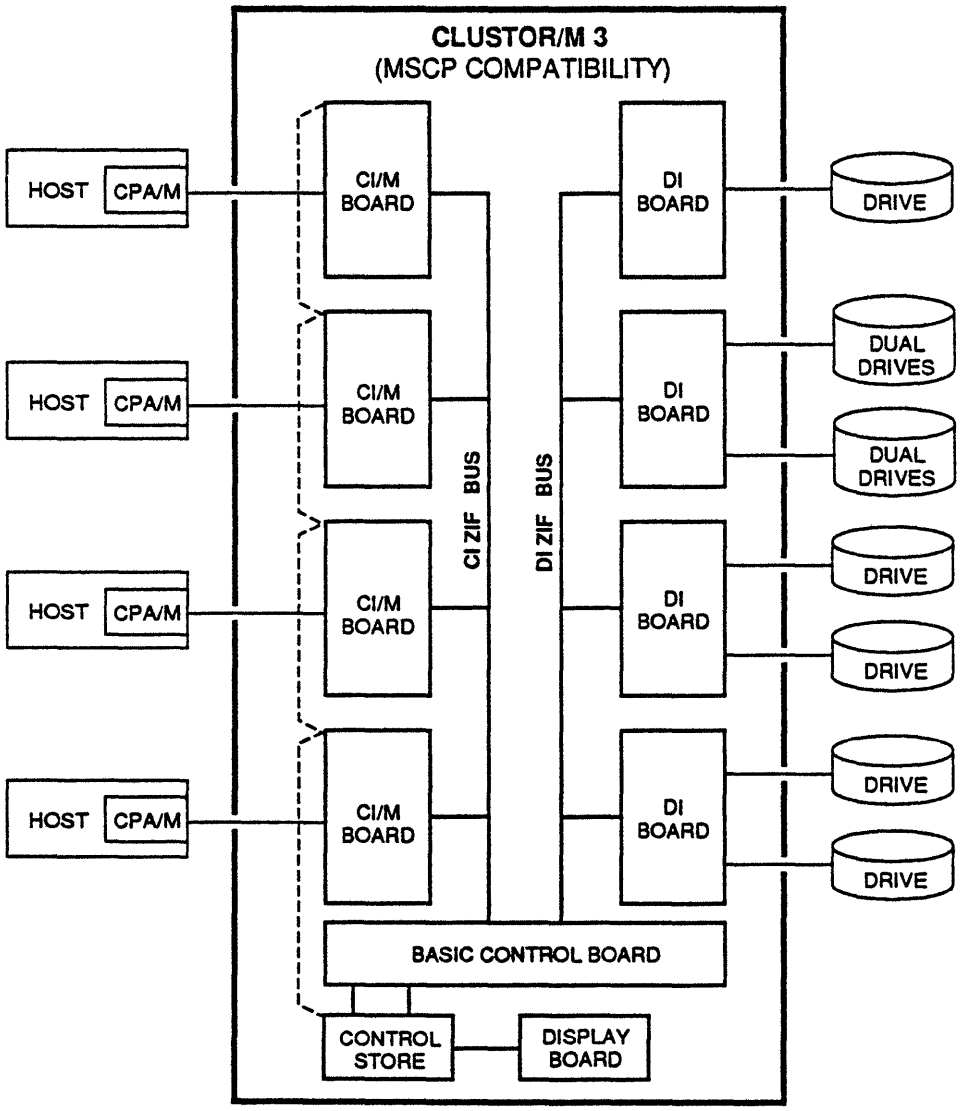


Figure 3-3. CLUSTOR/M 3 Subsystem (Maximum) Configuration

CLUSTOR/M 5

Subject to the same configuration requirements, CLUSTOR/M 5 differs from CLUSTOR/M 3 in the following ways:

- Display Board with Performance Monitor (DB/PM) replaces the DB.
- Disk Cache Processor (DCP) is added.

The CLUSTOR/M 5 subsystem in a 7-drive, 4-CPA configuration is shown in Figure 3-4.

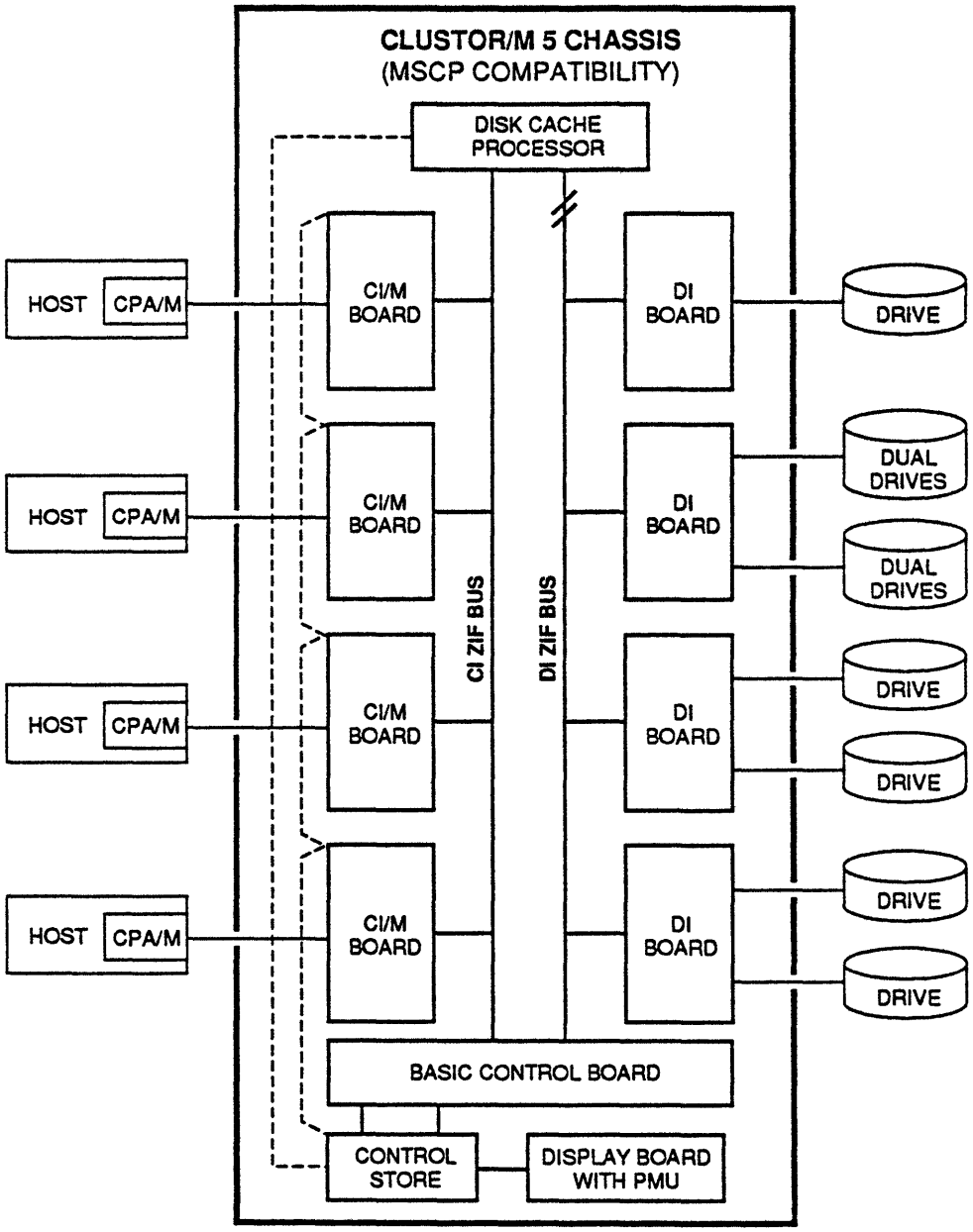


Figure 3-4. CLUSTOR/M 5 Subsystem (Maximum) Configuration

Multiport CPU

CLUSTOR 3 or 5 with the multiport CPU access feature is shown in Figure 3-5. The illustrated CLUSTOR subsystem configuration includes four CPAs. The SBI CPA at port 0 and the Unibus CPA at port 2 both serve the same CPU.

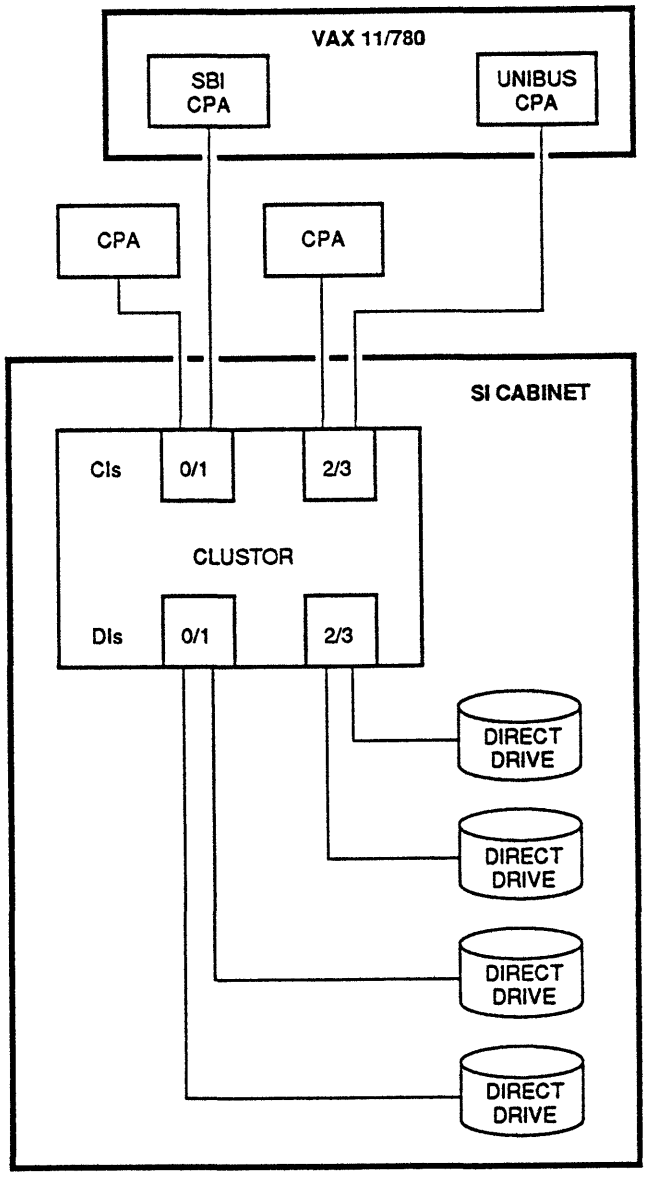


Figure 3-5. Multiport CPU

This computer multiport access requires no operating system software changes to support it. A multiport configuration mounts the disk drive on only one CPA and reserves the second CPA path until the first fails. Under VMS 5.x, using SI software application "eaSIshadow," the CPU automatically switches to the second path. Under other operating systems, this is a static redundant connection.

Dual-Channel Drive

Dual-channel configuration utilizes two CLUSTOR or CLUSTOR/M controllers, where either controller allows access to disk drives. Both CLUSTORs can interface with the same CPU for redundant configurations or separate CPUs for multiple CPU access. All CLUSTOR (M) controllers support dual-channel configurations.

The dual-channel configuration is shown in Figure 3-6. The VAX shown has two completely separate paths to the disk drives for true redundancy. The configuration includes an LLA because it is required by the CLUSTOR-B CPA at port 3 and the other CPA supported by the long line CI.

3.3 CLUSTOR Board Configuration Settings

Configuration settings include switch and jumper settings on the CLUSTOR (M) controller boards, the CPAs, and the disk drives.

Switch and jumper settings are provided in the "Ready Reference" section (Chapter 9). Refer to "CLUSTOR Subsystem" for board descriptions and illustrations.

Disk Cache Processor Board

The DCP board, used in CLUSTOR 5 only, has two configuration switches, SW1 and SW2, and 17 jumpers, W1 through W17. These define the operational board parameters. The DCP also has nine LEDs that indicate DCP operations and internal diagnostics tests. The functions for switch and jumper settings are explained in the following sections. See "Ready Reference" section (Chapter 9), for switch setting tables.

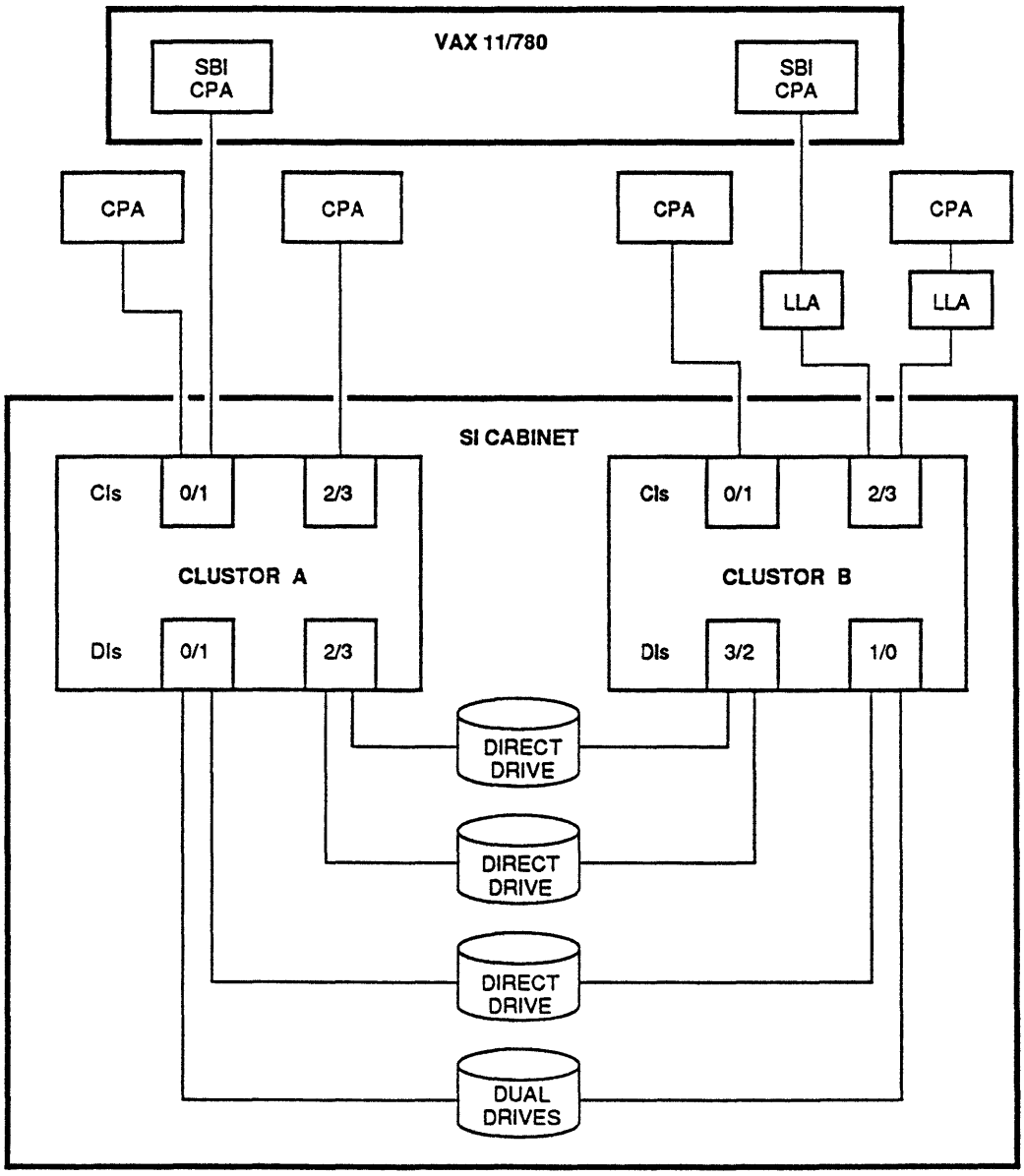


Figure 3-6. Dual Channel Disk Drive Configuration

Switch Functions

Write Back:

With Write Back enabled (OFF), the DCP executes a host write request by writing the data to the cache. Although the data is not yet written on the disk, the host receives status indicating a successful write. While the cache holds write data, the PHASE LED lights. The cache is "flushed" when the data is written to the disk. The cache flushes because:

- The flush interval time elapsed.
- The maximum number of write back sectors is reached.
- The host executes a Write Check command.
- The DCP passes on a command and data requested has not been written to the disk yet.
- There are no host requests pending (DCP) is idle.

The write back area (WBAREA) defines the boundaries of the disk where the write back operation is allowed. By default, the boundaries are Cylinder 0, Head 0, Sector 0 through the last cylinder, head, and sector of each disk drive enabled for caching.

CAUTION

It is possible for user data to be lost should a power failure occur before the cache memory is written to a disk. This should be remembered before deciding to implement the CLUSTOR 5 write back feature.

The flush interval (FLSHINT) default value is 10 seconds; the default maximum for write back sectors (WBMAX) is 20 sectors. Default definitions are altered for specific applications during DCP tuning. A write request that is fewer sectors than the maximum request size (MAXREQ) and lies within the write back area is written to cache only.

The PHASE LED lights indicate that the cache holds data not yet written on the disk. When cache flushes, the PHASE LED goes out. If a disk drive becomes write protected, or otherwise inoperable while the PHASE LED is on, the cache cannot flush to the disk.

The cache maintains the data and periodically attempts to flush. If the drive remains protected (or inoperable), CLUSTOR logs the flush errors. The controller updates the disk as soon as it is available.

Write-Through-With-Allocate:

With Write-Through-With-Allocate enabled (OFF), the controller executes a host write request by writing the data to the disk and, simultaneously, to the cache where it is available for reading. When Write Back is also enabled, Write Back prevails for write requests within the write back area. Requests outside the write back area are treated as normal write-through-with-allocate.

Read-Check:

With Read-Check disabled (ON), the DCP operates normally. Read-Check, although not recommended for normal operations, provides the important function of verifying cache operations. When enabled (OFF), Read-Check causes the DCP to compare every read from disk with its cache data. In this mode, write back is automatically disabled, but write-through-with-allocate is not affected. Read-Check slows overall functioning because of the time involved in verification.

Minimum Request Size:

The minimum request size (MINREQ) sets the minimum number of sectors read from the disk into the cache for any host read request. The default is 8 sectors. Designed as a look-ahead feature, MINREQ increases the hit rate in cache of sequential data reads. If the host requests fewer than the MINREQ, the set number of sectors is read into cache, with only the requested sectors sent to the host.

UNIX NOTE: Because the UNIX operating system internally caches read data, set the minimum request size to 1 sector.

Maximum Request Size:

The maximum request size (MAXREQ) sets the maximum number of sectors cached per request. A write or a read request of more sectors than MAXREQ is serviced by direct write or read to the disk without using cache. Default setting is 32 sectors.

Caching Enabled:

When caching enabled (OFF), the DCP operates normally (caches) from power-up. When disabled (ON) at power-up, the DCP does not cache.

Drive # Enabled for Caching:

When a drive is enabled for caching (OFF), the DCP controls all activities according to its defined parameters and caches data for the disk.

There are 17 jumpers. Jumpers W10 through W17 are for factory use only.

The nine LEDs on the DCP board indicate both operating and diagnostics status. LED 1 is closest to the front of the chassis. Refer to "Subsystem Troubleshooting" for LED indicator operating and resident definitions.

Computer Port Adapters

Each CPA has switches and jumpers that define its operational parameters. For jumper and switch locations and complete setting values, refer to Appendixes B through F.

Drives

Disk drive settings include the drive address and sector number. The drive address is 0 in single drive circuits, and 0 or 1 in dual-drive circuits. The sectors each contain 512 bytes. The sector count is the same for all formats of a particular disk drive. The drives and related sector numbers are listed in Table 3-1.

Some drives also have switches or jumpers controlling spin-up, I/O options, file protect, and other functions. Any or all disk drives can be configured dual-channel to a second CLUSTOR controller. See Appendix A for disk drive setting information. Refer to the appropriate SI or vendor manual for further information on switch and jumper locations.

Table 3-1. Actual Disk Drive Sector Counts

DRIVE	SECTOR COUNT
9733	67
9751	48
9761	67
SI83	67
SI85	67
SI56	33
SI57	49
SI92	73
SI93	66
SI95	73
SI506	48
SI510	53
SI817	73
SSD	32

4
PREINSTALLATION

This chapter provides a useful summary and is helpful for future additions. Consider the following limits when planning to install a CLUSTOR (M) subsystem. A pullout site installation checklist is provided at the end of the section.

4.1 Environmental and Physical Specifications

These specifications must be met to maximize equipment life and reliability.

Space

Space allocation includes actual physical space required by the unit and additional requirements for service clearance, as well as installation access.

Minimum service clearance is three feet in front and behind the cabinet. Connecting cables need ample slack to allow repositioning of components during service.

The single-bay Theta cabinet is available in two sizes: approximately 42 x 28 x 38 inches or approximately 60 x 28 x 38 inches. A dual-bay configuration is 60 x 55 x 38 inches.

Temperature

Ideal computer room temperature is 68° — 70° F (20° C), with a range of 65° — 75° F considered acceptable. When adding a CLUSTOR subsystem to an existing installation, determine the additional load on air conditioning.

Humidity

Humidity should be maintained in the range of 35 — 60% relative. Controlling humidity avoids the problems of static electricity or condensation.

Fire and Safety

Fire extinguishing systems should be in place. Confirm with the system manager that adequate fire precautions have been met.

Electrostatic Discharge

Static electricity is potentially dangerous to certain equipment. Static can be minimized with the use of special antistatic rugs or mats, chairs, and wrist-straps; maintaining humidity at 40 — 60%; and careful bonding of equipment frames.

Physical Specifications

The physical specifications for the CLUSTOR (M) subsystem are found in Table 4-1.

Table 4-1. CLUSTOR (M) Subsystem Physical Specifications

PHYSICAL SPECIFICATIONS			
Ambient Temperature			
Operating	60° — 90° F (15° — 32°C), 10° F/Hr Change		
Nonoperating	-32° —122° F(0° — 50°C), 26° F/Hr Change		
Relative Humidity			
Operating	8% — 80% noncondensing		
Nonoperating	5% — 90% noncondensing		
Elevation			
Operating	-500 — 7,500 Ft. (-152 — 2,286 meters)		
Nonoperating	-1,000 — 40,000 Ft. (-304 — 12,192 meters)		
Shock			
Operating (all axes)	< 2G, Half Sine Wave		
Nonoperating (all axes)	< 5G, Half Sine Wave		
Vibration			
Operating (all axes)	0.2G at 5 — 50Hz, Sinusoidal 1.0G at 50 — 500Hz, Sinusoidal		
Nonoperating (all axes)	3.0G at 2 — 200Hz, Sinusoidal		
DC Power	**+12 VDC**	**+5 VDC**	**-5 VDC**
Regulation	± 5%	± 5%	± 5%
Ripple (maximum, P-P)	100 Mv	50 Mv	50 Mv
AC Power — NEMA L15-R	**115 VAC**	**240 VAC**	
Selectable:	60 Hz	50Hz	
Fuse — Slow Blow:	4 Amps	2 Amps	
	6 Amps	3 Amps	
Mechanical Dimensions			
Height	5.25 inches (133.35 mm)		
Width	19.0 inches (482.60 mm)		
Depth	22.5 inches (571.50 mm)		
Weight	30 lbs. (13.6 kg)		
Heat Dissipation	1500 BTUs (480 Watts)		
MTBF	10,000 Power-On Hours		
MTTR	1.0 Hours		

4.2 Power Requirements

AC Power

The CLUSTOR (M) subsystem requires clean noise-free AC power. SI recommends power from a dedicated secondary of a distribution transformer. When this is not possible, use an isolation transformer to reduce the effects of conducted power line transients. If possible, attach the host computer and peripherals to the same line.

Consider total current requirements for the installation site. Check your main power panel to ensure proper and adequate power is available for the entire site. The CLUSTOR (M) power requirements are listed in Table 4-1. For power requirements of the disk drives, refer to the appropriate disk drive manual.

AC Neutral

Be careful not to confuse AC neutral with protective or frame ground. Frame ground prevents the buildup of dangerous voltages on equipment and protects personnel. It assures that any short circuit between a power phase and the cabinet draws enough current to trip the circuit's protective device immediately, rather than raising the potential of the equipment to a dangerous level. Additionally, this prevents spurious noise from entering the line. Never connect AC neutral to the frame of any equipment or the protective ground (except at the building's main electrical service entrance).

Neutral and safety ground are often connected together by the NEMA receptacles or at the circuit breaker neutral bus bar. Try to isolate neutral from safety ground in the circuit breaker box and ensure that conduit pipes are also isolated from other possible ground connections. Ideally, the equipment frame ground is isolated from neutral and other ground sources all the way back to the building main grounding rod.

AC Earth Ground

Be sure to maintain an adequate earth ground. If there is any question, perform an impedance test to ensure ground potential is less than 10 ohms. Refer to a grounding reference for measurement and grounding methods.

Typically, an earth ground suitable for computer equipment and peripherals consists of a 0.625-inch diameter copper rod driven into the earth to a depth of at least 12 feet. Since soil is quite variable in conductivity, chemicals such as salt or magnesium sulfate are added to the soil surrounding the rod to a depth of two feet. Periodic watering and chemical replenishment ensure an ongoing proper ground.

4.3 Unpacking

Inspect doorways, passageways, and elevators to verify that the shipping containers can be safely moved from the receiving dock to the computer room. Cut the metal straps and remove the shipping cartons. Unpack and inventory the contents against the shipping order.

Keep the shipping containers and packing materials. To avoid questions of liability, if a container arrives damaged, do not open it except in the presence of the shipping agent or representative. Do not sign for a container that has severe damage. After opening a container, inspect the drive for damage. If anything is damaged or missing, contact SI immediately. Return drives to SI in their SI shipping containers only. The original containers provide maximum protection during transport.

Allow the equipment to normalize to the computer room temperature before applying power. Open the cabinet(s), remove the package of extender leg parts and install them on the bottom front of the cabinet(s). Place the cabinet in position. Refer to "Installation" for more information on cabinet procedures.

The CLUSTOR (M) subsystem is shipped fully configured in the cabinet. Dual-bay configurations are separated into two cabinets before being shipped. A fully-configured CLUSTOR (M) 3 or 5 cabinet can weigh up to 2,200 pounds, excluding the shipping carton; each shipping carton measures approximately 69 x 33 x 49 inches.

4.4 Site Preparation

Use the checklist on the following page to confirm the site specifications and requirements discussed earlier in this section. The checklist pulls out for convenience.

SITE PREPARATION CHECKLIST

SITE NAME	
PREPARER'S NAME	
DATE	

CHECK (✓) EACH ITEM WHEN COMPLETED.

GENERAL REQUIREMENTS

- ☐ Notified facilities.
- ☐ Notified system manager.
- ☐ Provided access to equipment.
- ☐ Provided access to telephone.

SITE PREPARATION

- ☐ No obstacles to impede equipment delivery.
- ☐ Sufficient space for equipment and working area.
- ☐ Environmental requirements.
- ☐ Fire and safety precautions.
- ☐ Voltage and frequency requirements.
- ☐ Power routing and cable lengths.
- ☐ Static control.

Notes: _____

_____

_____

5
INSTALLATION

Procedures for the installation of the CLUSTOR (M) subsystem in a standard SI cabinet, or installing an additional disk drive are provided in this section. For removing and/ or replacing subsystem components during service, refer to "Maintenance and Troubleshooting".

5.1 General Precautions

Follow the precautions listed below to prevent injury to yourself or the equipment:

- Power-down the drive before performing any work on it.

WARNING

Never remove or install any printed circuit board or disconnect any connector, plug, or wire while power is on; doing so could cause failures.

- When removing connectors, do not pull on the cable; hold the connector firmly by its sides and pull out.
- Do not remove any parts not specified in the replacement procedure.
- When working near printed circuit boards, ground yourself with an anti-static strap.
- Package printed circuit boards in electrostatic-free envelopes.
- Read through the entire procedure before starting.

5.2 Cabinet Installation

The CLUSTOR (M) subsystem is shipped fully configured in the cabinet. A dual-bay unit is shipped with the cabinets separated. Remove the shipping material from both bays. Place the left bay in position, then move the right bay up next to it. The securing hardware is stored in the bottom of the right bay. Install the dual-bay assembly hardware using Figures 5-1 and 5-2 as a guide.

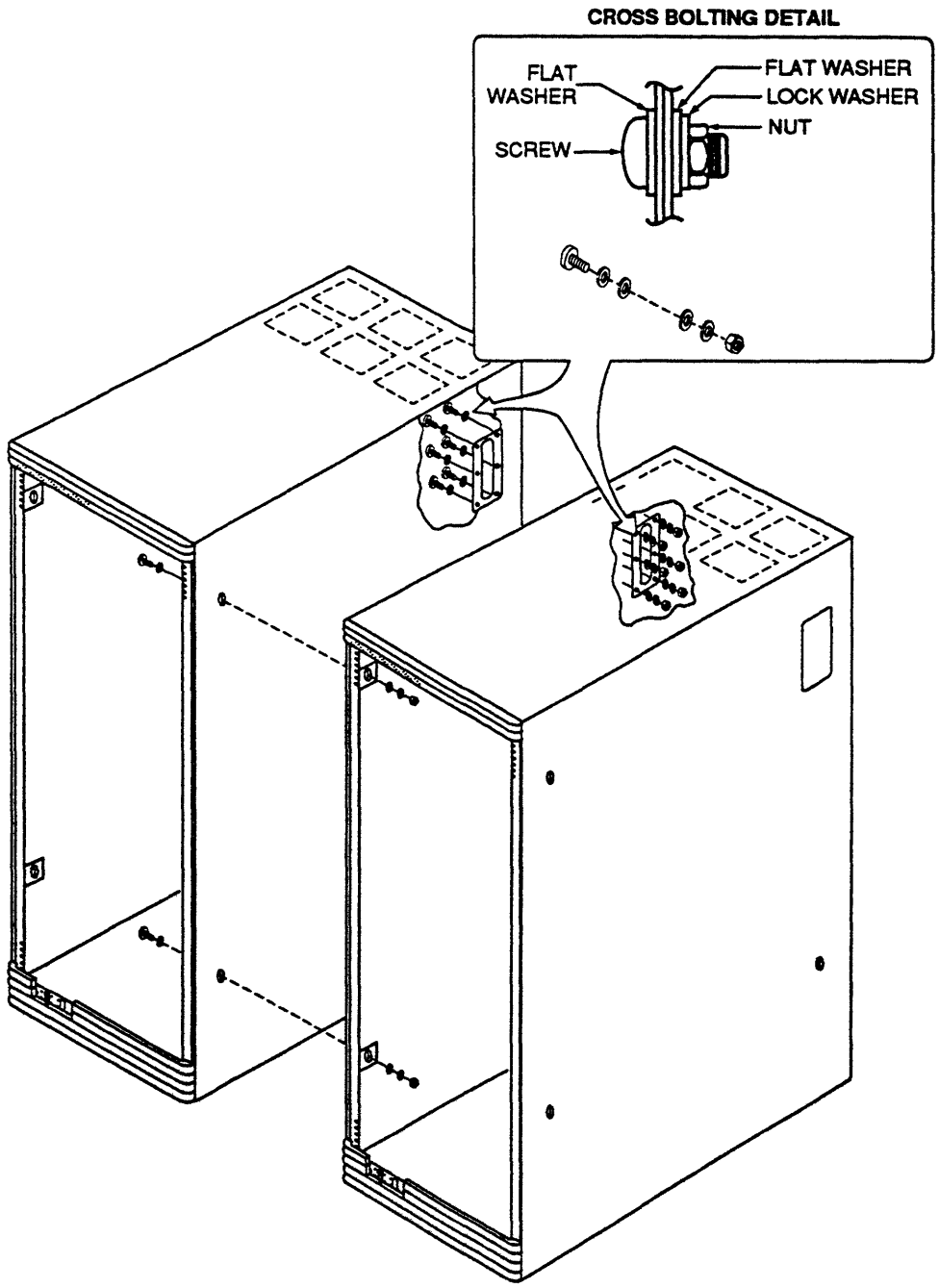


Figure 5-1. Dual-Bay Cabinet Assembly

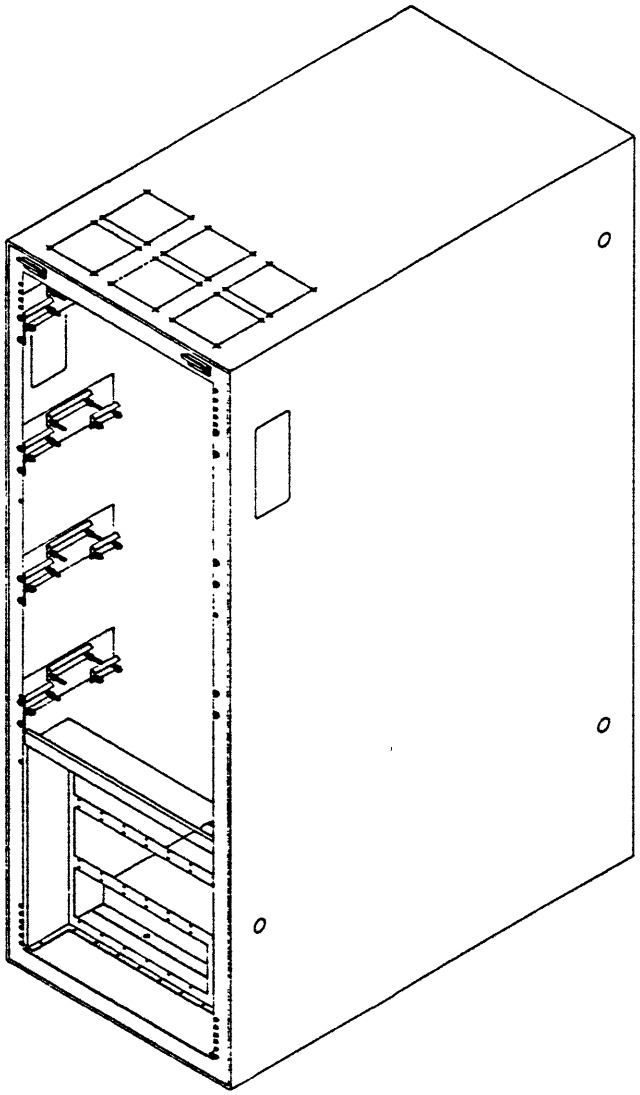


Figure 5-2. Rear View of Cabinet

5.3 Subsystem Installation

Once the cabinet(s) are positioned, the controller installation can be started. The following steps are involved in installing the CLUSTOR subsystem:

- Inspection
- Preliminary checks
- External cabling
- CPA installation
- Operating system installation
- Option and upgrade installation

Unless required by computer system equipment changes, **do not halt** the host computers until you are ready to actually install the CPAs.

Inspection and Preliminary Checks

Initial installation steps are board and cable inspection, and power-on checks. Each step is discussed in the following paragraphs.

Board and Cable Inspection

Inspect these three items to ensure all cables are seated properly:

- Drive to controller cabling
- Controller to transition panel cabling
- Device power plugs to switched power distribution unit (PDU) outlets

Dual-bay cabinets are mechanically assembled during unpacking. Disk and controller cables between the cabinets were disconnected at the drive or transition panel at the time of shipment. Reroute these cables between the cabinets and connect them according to the labels. All drive cables are labeled with the following:

Cabinet slot number
Channel
Bay side (horizontal position)
Vertical position (if necessary)

All transition panel cables are marked with a reference designator.

Power-On Checks

With the circuit breakers off at the PDUs, connect the AC power cords from the cabinet(s) to the source. Power-on the PDUs, then the drives and controller(s). Check that each attains normal ready status. Power-off the equipment and proceed with installation.

5.4 External Cabling

Label and route the external cables from the CLUSTOR cabinet transition panel to each CPA installation cabinet. Connect the cables to the CLUSTOR transition panel.

5.5 Computer Port Adapter Installation

CPAs supported by the CLUSTOR subsystem are the Unibus, Qbus, SBI and BI. Each CPA has switches and jumpers that define its operational parameters. Settings specific to CLUSTOR are listed in Appendixes B through F. Each CPA appendix covers the installation procedure, jumper and switch locations, and complete setting values.

5.6 Operating System Installation

Each host operating system user guide specifies the software modifications installation procedures. Refer to "Related Publications" for the appropriate manual.

5.7 Option and Upgrade Installation

Options available with the CLUSTOR subsystem are usually installed at the factory. This section explains how to install CLUSTOR subsystem options and how to upgrade a CLUSTOR controller to a higher level controller. There are four options available:

- Long-Line Computer Interface Adapter (CI-LLA) (RM-compatible)
- CI/M (SCSI CI) Adapter
- Dual channel disk drive
- CLUSTOR (M) 3 to 5 upgrade

To connect the frame and signal grounds together, follow the procedures below:

1. Connect all signal grounds together.
2. Connect all frame grounds together.
3. Connect the signal grounds to the frame grounds through a 500K OHM resistor at the controller.

Long Line Adapter (RM-compatible only)

The Long Line Adapter (LLA) allows a total internal and external cable length of 200 feet (60 m) between CLUSTOR and the CPA at the host CPU. High speed, differential, tri-state bus/line drivers and receivers provide a terminated and balanced transmission system for the LLA. The adapter has its own chassis with power supply and can stand alone, mount in the CPU, or mount in an expansion cabinet. Long-line adapter use requires the long-line CI board.

The LLA has an L-shaped board with a cutout area for the power supply. The approximate board dimensions are 8 x 14 in (20.3 x 35.6 cm). The LLA chassis dimensions are 3.5 x 9.5 x 19 in. (8.9 x 24.1 x 48.3 cm).

The maximum external cable length from the LLA to the controller is 150 feet (45.7 m). The maximum external cable length from the LLA to the CPA is 20 feet (6.1 m). Total internal cable length cannot exceed 30 feet (9.1 m).

The LLA has its own 6-foot power cable.

LLA Installation

1. Limit access to the subsystem and power-off the CLUSTOR chassis.
2. Extend the chassis on its rails, open the top cover and install the CI-LL board.
3. Connect the internal cables from the CI-LL to the cabinet transition panel.
4. Replace the chassis top cover and slide the chassis back into the cabinet.
5. Place the LLA and ensure the power cable reaches the AC source socket.
6. Connect the long external cables to the transition panel, route to the LLA and connect.
7. Connect the 20 foot cables to the LLA and route to the CPA.
8. Install the CPA as described in "CPA Installation."
9. Power-on the LLA and the CLUSTOR controller.
10. Have the system manager boot the systems.
11. On a VMS system, run SIDOS to verify operations.

CI/M (SCSI CI) Adapter

The CI/M (SCSI CI) presents itself to CLUSTOR as a standard CI card and CPA combination, i.e., it is 100% compatible with the existing CI boards. Therefore, with the exception of on-board switch settings and different cabling requirements, the installation of this board is identical to the installation of a standard CI card.

Important Notes Prior To Installation

1. If this is an upgrade to an existing installation, ensure that the existing 250w CLUSTOR power supply part number 122-0012 is replaced with the new 350w power supply part number 122-0006.
2. Make a note of the logical disk drive unit numbers for the disk drives that are required to be available to the host(s) connected to this SCSI CI port. This information is required for confirming the switch settings in the CI/M card.
3. If this installation is a mixed CI/M (MSCP) and standard CI (RM) configuration, it is recommended that the CI/M cards be located beneath the standard CI cards, as they draw considerably more power.

4. Standard antistatic precautions must be observed at ALL times while handling the CI/M card. High speed CMOS devices, which are extremely static sensitive, are present on this card. Also, as this is a multilayer board, care must be observed to avoid flexing the card during installation.
5. The single-ended SCSI port has on-board terminators (fixed); therefore, in these configurations the CI/M must be the last device on the SCSI bus.
6. The differential SCSI port is not terminated on the board; it requires an external terminator on the transition panel.

NOTE

The SCSI CI self-test will fail if the differential terminator is not present.

Dual-Channel Disk Drive

The dual-channel disk drive option connects two CLUSTOR or CLUSTOR/M subsystems to the same disk drive. Both CLUSTORs can interface with the same CPU for redundant configurations or separate CPUs for dual-CPU access.

Because both controllers access the same disk drive, the drive must have the same definition on the drive model switch of the DI board in each CLUSTOR. An additional disk drive board or other minor modification to the disk drive is required for this option.

Both CLUSTORs and the disk drives must be housed in the same single or dual-bay cabinet. CLUSTOR 5 applications must disable caching for dual-channel drives.

Installation depends on the subsystem configuration. Variations are:

1. Adding a second CLUSTOR (M) to a single or dual-bay cabinet and converting the disk drives to dual channel.
2. Converting a drive to dual channel in an established dual-channel subsystem.
3. Adding a dual-channel drive to an established dual-channel subsystem.

Directions for installing each variation are explained below. Specific installation directions are found in the appropriate disk drive manuals.

First Variation Installation

1. Limit access to the subsystem and power-off the controllers, drives, and cabinet.
2. Install the second CLUSTOR in the cabinet. Use slot 5 or slot 10 in the bay cabinets.
3. Install the dual-channel boards into the disk drives. Follow the procedures specified in the disk drive manual.
4. Cable the disk drives' second channel to the second CLUSTOR controller.

5. Cable the second CLUSTOR controller to the transition panel.
6. Install the external cables for the second CLUSTOR and route to the CPUs.
7. Install the CPAs and connect the external cables.
8. Power-on the subsystem and verify ready status for each device.
9. Have the system manager boot the systems.
10. On a VMS system, run SIDOS to verify operations.

Second Variation Installation

1. Limit access to the subsystems and power-off the affected controller and disk drives.
2. Install the dual-channel boards into the disk drives. Follow the procedures specified in the disk drive manual.
3. Cable the disk drives' second channel to the second CLUSTOR controller.
4. Power-on the drives and controller, and verify ready status for each device.
5. Have the system manager boot the systems.
6. On a VMS system, run SIDOS to verify operations.

Third Variation Installation

1. Limit access to the subsystems and power-off the controllers, drives, and cabinet.
2. Install the dual-channel boards into the disk drives. Follow the procedures specified in the disk drive manual.
3. Install the disk drives in the cabinets.
4. Cable the disk drives' two channels to the two CLUSTOR controllers.
5. Power-on the subsystem and verify ready status for each device.
6. Have the system manager boot the systems.
7. On a VMS system, run SIDOS to verify operations.

CLUSTOR 3 to 5 Upgrade Installation

Any CLUSTOR 3 or CLUSTOR/M 3 controller can be upgraded in the field to a higher level CLUSTOR controller.

NOTE

It is not necessary to reformat the disk drives.

Upgrading An Installed CLUSTOR

1. Prepare the existing subsystem.
2. Install the hardware.
3. Perform operational checks of the CLUSTOR subsystem.

Because each upgrade is dependent on the installed configuration, proper planning is essential. Contact your SI representative for more information.

6
MAINTENANCE

This section includes preventive and routine maintenance, diagnostics tools, and removal and replacement procedures for Field Replaceable Units (FRUs) in the CLUSTOR (M) subsystem. These units, along with their part numbers, are listed in the "Illustrated Parts List" (Chapter 8).

6.1 Subsystem Maintenance

Subsystem maintenance includes normal maintenance and diagnostics for the CLUSTOR (M) subsystem.

Preventive maintenance is required every six months, or whenever a repair is accomplished. This includes:

- Subsystem verification
- Individual drive checks
- Power and fan checks

Use the SI diagnostics program SIDOS to verify normal operation and subsystem function from a system level. If SIDOS is unavailable, any SI-supplied RM subsystem diagnostic can be used. Refer to the *SIDOS User Guide* for more information. SI Disk ASIST provides disk drive verification on a stand-alone basis. Refer to the *ASIST User Guide* for more information.

6.2 Resident Diagnostics

CLUSTOR (M) has BCB-based resident diagnostics that execute at power-on and reset. Additionally, the DCP board of CLUSTOR (M) 5 has resident diagnostics that execute at power-on and reset. Refer to "Subsystem Troubleshooting" for error code indications.

NOTE

The DCP was defined on the 9900. Since CLUSTOR's DCP is different, it is displayed as DCP II on terminal screens.

6.3 Disk Cache Processor Tuning

DCP tuning involves changing operational parameters to enhance operation under use of that particular software application. The DCP automatically tunes itself based on requests by the host. These parameters are described in more detail under "DCP Functions."

DCP Functions

To obtain information from the DCP, or to change DCP parameters, type **^C** at the terminal connected to the RS232 port on the back panel of CLUSTOR. Make sure the controller/DCP switch on the front panel is set to DCP. At the **SI>** prompt, type **HELP <cr>**. The following menu appears:

.C	Shows configuration in short form
.J	Shows journal, last request first
C	Configure cache
R	Reset cache to default settings
RUN	Engage cache and start
START	Test memory, engage cache, and start
.ST	Shows statistics on caching
FE	Troubleshooting aids

C Configure System

When configuring the system, each default is shown. Type **<cr>** to use the default. If changing a number, type **<number><cr>**. If changing an ON/OFF parameter, type **X<cr>**.

READ-CHECKS ..... Off
Print error messages ..... Off
Disable read allocates ..... Off
Automatic Tuning ..... On
Display Automatic Tuning statistics ..... Off
Number of blocks in cache 15477
Cache page/swap requests ..... On
Drive enabled for caching:
- 0 ..... On
- 1 ..... On
- 2 ..... On
- 3 ..... On

4 ..... On
5 ..... On
6 ..... On
7 ..... On
Writebacks ..... Off
Writethru with allocate ..... On

Drive #0
Valid upper boundary
Cylinder ..... (maximum number of logical cylinders)
Head ..... (maximum number of logical heads)
Sector ..... (maximum number of logical sectors)
Valid lower boundary
Cylinder ..... (0)
Head ..... (0)
Sector ..... (0) repeated for each drive enabled
Read length adds ..... On
Write length adds ..... On
Peak interval in seconds 60
Panel reset interval in seconds 0
Clear cache when full ..... Off

.ST *Displaying DCP Statistics*

The following information is displayed.

DCP II Statistics
Requests 10
Hits 2
Writes 5
Reads 3
Write checks 2
Errors 0

.C *DCP Configurations*

To display the current DCP configuration information, type .C <cr> at the S1> prompt. The following display appears:

```
        DCP II Configuration
READ-CHECKS ..... Off
Writebacks ..... Off
Write Alloc ..... On
Read Alloc Inh ..... Off
Automatic Tuning ..... On
Cache Size ..... 15477
Max Req ..... 32
Min Req ..... 8
Flush Interval ..... 10
Max Wrt Bks ..... 20
```

Read-Checks

When the DCP is in the read-check mode, data is copied by the DCP when a read-miss or a write occurs. When a read-hit occurs, the data is again copied by the DCP as it goes from the disk to the host. The DCP then compares the data to data already in the cache and reports an error when a data miss-compare occurs.

Write-Backs

When the DCP is in write-back mode, all write-to-disk requests that occur within the upper and lower boundaries of the write-back area (set in C configure cache) are immediately written directly into the cache. The disk is not accessed and all overhead involving disk writes is passed. When one of several conditions occur, the data is written to the disk by the DCP. The conditions that require the DCP to "flush" the data are:

- Flush interval (number of seconds before a flush must occur) happens (set in C configure cache).
- Maximum Write-back Blocks (Max Wrt Bks) are in the cache (set in C configure cache).
- A write check request for some write-back data occurs.
- The DCP is going to pass on a command that accesses some data in the write-back list.
- The DCP is idle (no host requests).

Write-Thru With Allocate

When Write Alloc mode is enabled, the DCP copies all write data going from the host to the disk, if it is within the upper and lower boundaries of the caching area (set by C configure cache). If write-backs are enabled, the data must be outside of the write-back boundaries and within the caching boundaries to be copied.

Read-Allocate-Inhibit

When the DCP is in this mode, data read from the disk to the host is not copied by the cache.

Automatic Tuning

When the DCP is in Automatic-Tuning mode, it compares the caching parameters to the run-time performance of the cache every 60 seconds, even if no data transfer occurs. It has the optional ability to monitor the statistics gathered during real-time operation, not just display them, on an individual drive basis.

DCP Auto-Tuning Functions

- Evaluates statistics for one drive per activation, on a round-robin schedule.
- Modifies caching parameters to increase the overall system performance, and monitors its changes to ensure it didn't actually degrade performance.
- If necessary, makes adjustments to parameters to improve performance.
- Enables and/or disables certain modes of operation when that mode is not performing at maximum for the type of requests being received.
- (Optional) Disables caching functions when errors occur that slow down the system unnecessarily.
- If performance declines, switches back to the previous parameters.
- Checks each drive for the amount of errors that have occurred.
- (Optional) If a drive is posting errors, the DCP stops caching that drive to gain the performance required for the other drives being served.

Look-Ahead Value

The DCP "looks ahead" when performing caching functions and provides a look-ahead value on a drive-by-drive basis. The look-ahead value is the number of sectors the cache tells the controller to look ahead on the disk. The look-ahead value allows the DCP auto-tuning routine to adjust the look-ahead based on the requests occurring to that one drive.

If the hit rate is below 50%, the look-ahead count (READMIN) is reduced by 2 sectors (from 8 to 6) for the next period. If the hit rate is still below 50%, the look-ahead count is again reduced by 2 sectors (from 6 to 4) for the next period. If the hit rate is still below 50%, the look-ahead count is reduced by another 2 sectors (from 4 to 2) for the next period. If the hit rate is still below 50%, the look-ahead is set back up to 8 sectors for the next period. Then the loop starts back at the top again.

The previously mentioned period varies with the number of drives being monitored, since the statistics are checked for a drive in a round-robin manner. The period equals 60 seconds times the number of drives being cached.

If the average request size is within 4 sectors of the maximum request size, the maximum request size is increased by 16 sectors, up to a maximum of 64 sectors. If the difference between the average request size and the maximum request size is greater than 16 sectors, the average request size is decremented by 16 sectors, down to a minimum of 16 sectors.

Write-Backs

If write-backs are enabled on the drive being monitored, the request types are checked. If there is at least one write check for every 2 writes, write-backs are temporarily disabled for the monitored drive only (for the next period). The requests will be checked every period. When write-checks become less than 50% of writes, write-backs will be re-enabled.

Options

If drive auto-disable is selected, whenever a particular disk drive logs more than 10 errors (since last roll-over or reset), the DCP will disable that drive from caching.

If DCP auto-disable is selected, whenever the DCP has accumulated more than 10 internal, non-drive related errors (since last roll-over or reset), the DCP will disengage itself from caching any requests.

Statistics on system operation and auto-tuning changes can be displayed on the terminal. The display will be updated when at least 8 minutes have elapsed since the last display, and the DCP is idle. When the display is enabled, the statistics display can be refreshed immediately by typing ^T (control T) at the terminal.

^T will cause the DCP to update the averages on the PMU display, and if auto-tuning display is enabled, will display the statistics.

6.4 DCP Terminal Access

There are two ways to enter into the DCP's operating system. Type a ^D (control D) to enter the DCP without disengaging it. Type a ^C (control C) to enter and also disengage from the controller. ^C allows you to work on the DCP without affecting the I/O going through the controller. Type HELP at the "S1>" prompt to list the commands available. Most of these commands are for the customer. The last command, FE, however, sets up the DCP for troubleshooting and allows access to special aids. It automatically displays a menu of available options. To redisplay this menu at any time, type FE-HELP. See Appendix H for sample displays of all the tables.

6.5 DCP Operating System Commands

The following is a list of commands available to the user after typing a ^C or ^D on the terminal.

.C	Shows the current configuration in short form.
.J	Shows the journal, most recent request first.
C	Configure, or tune, the DCP.
R	Reset the DCP to the default switch settings.
Run	Engage the DCP and start.
Start	Test memory and auto start.
.ST	Shows caching statistics.
FE	Enable diagnostic functions & display test menu.

6.6 Configuring the DCP

Below is the menu used to configure the DCP (C configure cache). Type **<cr>** to use the default. If changing an ON/OFF parameter, type **X**. If changing a number, type **<number><cr>**. To exit early, type **Q**.

Configuration Menu

READ-CHECKS ..... Off
Print error messages ..... Off
Disable read allocates (DIS-RDA) ..... Off
Automatic Tuning ..... On
Writebacks (WRBKS) ..... On

READ-CHECKS ..... Off

When the DCP is in this mode, data is always written and read between the host and the drive. The DCP simply copies the data. When a read hit occurs, the data copied from the disk is compared with the data already in the cache. If the data does not compare, an error message is displayed. This mode impedes performance, and is intended as a diagnostics tool only.

Print error messages ..... Off

When this is enabled, the DCP displays messages on the terminal when errors are detected. Regardless of this flag, the error is logged in the journal.

Disable read allocates (DIS-RDA) ..... Off

When this is enabled, read misses are not cached.

Automatic Tuning ..... On

When this is enabled, the DCP monitors its performance versus the requests processed. It then periodically modifies caching parameters to attempt to increase performance.

IF auto-tuning is **on**, these three prompts appear:

Display Auto-Tuning Statistics.....Off
Disable caching if failing DCP hardware .....On
Disable caching of failing disks.....On

Display Auto-Tuning Statistics.....Off

When this is enabled, statistics not available from the PMU are displayed at the terminal, and updated every 8 minutes.

Disable caching if failing DCP hardware .....On

When this is enabled, if the DCP detects more than 10 internal errors within the roll-over time, it will automatically disengage itself.

Disable caching of failing disks.....On

When this is enabled, if the DCP detects more than 10 errors for any one particular drive within the roll-over time, it will automatically disable caching for that particular drive.

IF auto-tuning is **off**, these two prompts appear:

Fill requests to length (LOOKAHEAD).....8
Maximum sectors per request (MAXREQ) 16

Fill requests to length (LOOKAHEAD).....8

This parameter is the minimum number of sectors the DCP will read from a drive when a read miss occurs. Maximum value is 8 and minimum value is 1.

Maximum sectors per request (MAXREQ) 16

This parameter is the maximum number of sectors in a single I/O request that the DCP will handle. Anything greater will be passed on. Maximum value is 128 and minimum value is 16.

After auto-tuning is complete the following three prompts appear:

Number of blocks in cache 15477
Cache page/swap requests.....On
Drives enabled for caching:

Number of blocks in cache 15477

This is the maximum number of blocks to cache. The maximum is 15477 and the minimum is 1.

Cache page/swap requests.....On

When this is enabled, the DCP will cache the VMS 96 sector swap requests regardless of the maximum request setting.

Drives enabled for caching:

0 .....On
1 .....On
2 .....On
3 .....On
4 .....On
5 .....On
6 .....On
7 .....On

Writebacks (WRBKS).....On

When this is enabled, write requests from the host to the drive will go directly into cache memory instead of the drive, eliminating the latency. The DCP will then write the data to the drive at a later time. The write-back data is written to the drive (flushed) when one of the following conditions occur:

1. A write check request occurs and some or all of the request is write-back data.
2. The DCP has no commands in its queue.
3. The total number of write-back sectors in the cache is greater than WBMAX.
4. The number of seconds since the last flush is greater than the flush interval.
5. If a drive is write protected or spun-down while the cache has write-back data for it, the data will remain in the cache until either the drive is able to accept write requests, the DCP reset switch is hit, or a power-fail occurs.
6. When this is enabled, each individual drive can be enabled or disabled for write-backs.

IF write-backs are **on**, these two prompts appear:

Writebacks before flush (WBMAX).....20

Flush interval in seconds.....10

Writebacks before flush (WBMAX).....20

This parameter is the maximum total number of write-back sectors in the cache allowed before a flush must occur.

Flush interval in seconds.....10

This parameter is the maximum number of seconds that can pass before a flush must occur.

IF write-backs are **on**, this prompt appears for each drive enabled for caching:

Drive # 0

Writebacks for this drive.....Off

This enables (ON) or disables (OFF) write-backs on a per-drive basis.

IF write-backs are **on** for a drive, these nine prompts appear for each drive enabled:

Drive # 0
WRBACK upper boundary (WBHI):
Cylinder (1023)
Head (17)
Sector (64)
WRBACK lower boundary (WBLO):
Cylinder (0)
Head (0)
Sector (0)

Drive # 0
WRBACK upper boundary (WBHI):

This is the highest disk address for a write request that will be handled as a write-back. Anything higher will be written through to the disk and copied by the DCP. Must be equal to or lower than VALID upper boundary.

Cylinder (1023)
Head (17)
Sector (64)

WRBACK lower boundary (WBLO):

This is the lowest disk address for a write request that will be handled as a write-back. Anything lower will be written through to the disk and copied by the DCP. The disk address must be equal to or higher than VALID lower boundary.

Cylinder (0)
Head (0)
Sector (0)

IF write-backs are **off**, this prompt appears:

Writethru with allocate (WAS).....On

When this is enabled, the DCP will copy write-request data into the cache, as well as the read requests.

Whether write-backs are ON or OFF, these nine prompts appear for each drive enabled:

Drive # 0
Valid upper boundary (VALIDHI):
Cylinder (1023)
Head (17)
Sector (64)
Valid lower boundary (VALIDLO):
Cylinder (0)
Head (0)
Sector (0)

Drive # 0
Valid upper boundary (VALIDHI):

This is the highest disk address for a request that will be handled by the DCP. Must be greater than the lower boundary.

Cylinder (1023)
Head (17)
Sector (64)
Valid lower boundary (VALIDLO):

This is the lowest disk address for a request that will be handled by the DCP. Must be less than the upper boundary.

NOTE

When set to 0, 0, 0 the drive will not cache the first sector (block 0) because the majority of systems use that sector as a boot block.

Cylinder (0)
Head (0)
Sector (0)

Read length adds .....On

This enables the inclusion of read request length statistics in the PMU display.

Write length adds.....On

This enables the inclusion of write request length statistics in the PMU display.

Peak interval in seconds (PEAK-INT).....60

This parameter is the number of seconds allowed to elapse before the PMU peak indicators are reset.

Panel reset interval in seconds.....0

This parameter is the number of seconds allowed to elapse before the PMU display and statistic tables are reset. A value of zero indicates never reset.

Clear cache when full.....Off

When this is enabled, the DCP will clear the cache memory when all the available blocks have been allocated. When disabled, the DCP will replace the blocks on a least recently used basis.

If display statistics is enabled (see C configure), every five minutes the screen (on the RS232) is updated with DCP and drive statistics. The following display is an example:

```
***** System Industries Disk Cache Processor II *****
                Auto-tuning Statistics
MinReq      8           MaxReq      32
Drive       Caching State       Errors
  0         Enabled               0
  1         Enabled               0
  2         Enabled               0
  3         Enabled               0
  4         Enabled               0
  5         Enabled               0
  6         Enabled               0
  7         Enabled               0
Writebacks are OFF
Number of changes made   0
Average requests per second   0
```

Cache Size

This is the number of 512 byte disk blocks the cache can hold.

Maximum Request

This is the largest number of blocks in one I/O request that the DCP can handle. This number can range from 8 to 128, but must be larger than the minimum request. If the VMS system disk is being cached on CLUSTOR, the PAGE/SWAP I/O requests are cached even though they are usually larger than maximum request.

Minimum Request

This is the minimum number of blocks the DCP reads from the disk. If a read request is for 2 blocks and minimum request is 8 blocks, the DCP reads the next 6 sequential past the request into the cache as well, but only transfers the 2 blocks requested to the host.

Flush Interval

This is the maximum number of seconds write-back data is held within the cache without being written to the disk.

Maximum Write-Backs

This is the maximum number of write-back data blocks that are held within the cache before it must write the data to the disk.

6.7 Component Removal and Replacement

This section explains how to remove and replace CLUSTOR components. This includes:

- Chassis
- Boards
- Computer Port Adapters
- Disk Drives

Chassis Components

The chassis mounts in a standard 19-inch (48.3 cm) FCC-Compliant equipment rack and requires 5.25 x 19 x 20 inches (13.3 x 48.3 x 50.8 cm) of rack space. Instructions on installing the chassis, and replacing the power supply and fan are listed below.

Chassis Installation

1. Mount the rail slides to either side of the chassis.
2. Mount the rails in the cabinet with the hardware supplied.
3. Place the chassis into the cabinet by inserting the slides into the rails until the locks catch. Check for binds by pushing the chassis all the way into the cabinet and then extending it all the way out on its rails.

Power Supply Replacement

1. Power-off the chassis. Extend the chassis on its rails.
2. Remove the screws that hold the top cover in place. Remove the top cover.
3. Disconnect the cables from the power supply to the BCB, the fan, and the AC input.
4. Remove the four mounting screws that secure the power supply to the chassis.
5. Remove all but the last DI board.
6. Remove the power supply.
7. Examine the replacement for correct cabling and power selection.
8. Place the replacement in the chassis and install the mounting screws.
9. Replace the DI boards.
10. Connect the power cables.
11. Power-on the chassis.
12. Check for normal indications including fan operation.
13. Power-off the chassis.
14. Replace the top cover and its screws.
15. Push the rail locks in; slide the chassis back into the cabinet; power-on the chassis.

Fan Replacement

1. Power-off the chassis. Extend the chassis on its rails.
2. Remove the screws that hold the top cover in place. Remove the top cover.
3. Disconnect the fan cable.
4. Remove the two screws that hold the fan in place, and remove the fan.
5. Place the replacement fan in the chassis and install the mounting screws.
6. Connect the fan cable.
7. Power-on the chassis.

8. Check for fan operation.
9. Power-off the chassis.
10. Replace the top cover and its screws.
11. Push the rail locks in and slide the chassis back into the cabinet. Power-on the chassis.

6.8 CLUSTOR (M) Boards

These instructions describe how to replace these boards:

- CI, DI, and DCP boards
- CS board
- BCB board
- DB or DB/PM board

NOTE

For convenience, throughout this chapter CI will be used to refer to both CI and CI/M boards.

Before starting replacement, power-off the chassis, extend it on its rails, and remove the top cover.

CAUTION

Do not use excessive force when removing boards fitted with ZIF connectors. To avoid breaking the connector, take care not to move the locking arm vertically, sideways, or to rotate it while pulling it out. If the board cannot be removed without force, verify that the connector is unlocked. Failure to fully release the connector before removing the board can result in damage.

CI, DI, and DCP Board Removal

The CI, DI, and DCP boards all stack on alignment posts and use ZIF connectors. To replace a board, you must remove the boards stacked above it. To remove a CI, DI or DCP board from the chassis, follow these steps:

1. Unfasten the knurled locking nuts at the top of the stack(s).
2. On CLUSTOR 3 or 5, remove the cable restraining clamps (not used with CLUSTOR 1). Leave the cables connected on the boards.
3. Remove the cable from the CS board to the DCP and CI boards.

4. To release the top board, carefully pull the ZIF connector locking arm straight out as far as it will go. Remove the board from the chassis with the cables still attached.
5. Repeat step 4 for each board until the desired board is exposed.
6. Remove any cables on the desired board, unlock its ZIF connector, and remove the board.

CI, DI, and DCP Board Replacement

1. Configure the replacement board(s).
2. Install the cables on the replacement board.
3. Open the ZIF connector of the replacement board and lower the board on the alignment posts.
4. Connect the cable from the CS board to the DCP and CI boards.
5. Push in the ZIF connector locking arm to lock the board in place.
6. Repeat steps 3 through 5 for each board removed.
7. Power-on the chassis and check for normal indications.
8. Install the top cover.
9. Push the chassis back into the cabinet.

CS Board Removal and Replacement

The CS board plugs into the BCB and stands behind the DB.

1. Disconnect the cables going to the CS board.
2. Remove the three screws and standoffs along the top of the CS, securing the CS to the chassis.
3. Carefully pull up on the CS board, lifting it out of its BCB connections.
4. Examine the replacement board and ensure its configuration is correct.
5. Install the replacement board into the BCB connections.
6. Install the three screws and standoffs along the top of the CB.
7. Connect the cables.
8. Power-on the chassis and check for normal indications.
9. Install the top cover.
10. Push the chassis back into the cabinet.

DB and DB/PM Removal and Replacement

The DB or DB/PM board mounts in the chassis front cover (traditional style only). For Theta series, completely replace front panel.

1. Remove the cable from the CS board at the DB.
2. Remove the three screws and standoffs along the top of the CS, securing the CS to the DB.
3. Remove the screws on either side of the chassis that hold the front panel (and the DB) to the chassis.
4. Mount the new front panel/DB on the chassis.
5. Install the 3 screws and standoffs along the top of the CS.
6. Connect the cable from the CS board.
7. Power-on the chassis and check for normal indications.
8. Install the top cover.
9. Push the chassis back into the cabinet.

BCB Removal and Replacement

The BCB mounts on the base of the chassis with the components facing the bottom cover plate.

1. Remove the power cable, PS1, from the BCB.
2. Unlock the bottom two ZIF connectors by pulling out on the locking arms.
3. Remove the bottom cover plate.
4. Remove the 11 nuts around the parameter that secure the BCB to the chassis. The bolt shows through the nut. Remove the BCB.
5. Configure the replacement board.
6. Make sure that the bottom ZIF connectors are unlocked. Mount the replacement board to the chassis and secure it.
7. Install PS1.
8. Lock the two bottom ZIF connectors.
9. Install the bottom cover plate.
10. Power-on the chassis and check for normal indications.
11. Install the top cover.
12. Push the chassis back into the cabinet.

Computer Port Adapters

For CPA replacement, refer to Appendixes B through F.

7
SUBSYSTEM VERIFICATION AND TROUBLESHOOTING

This chapter explains subsystem verification, possible error indications, and troubleshooting solutions for CLUSTOR (M) subsystems.

7.1 Subsystem Verification

Use the SI diagnostics program SIDOS to verify normal operation and subsystem function. SIDOS is a user-friendly program that provides a menu-based display for exercising and testing the subsystem.

7.2 Subsystem Troubleshooting

Subsystem troubleshooting is divided into three areas:

- Controller faults
- DCP faults
- DCP monitor
- DCP Display Examples

Controller Faults

When the controller detects a fatal hardware error, it halts and the front panel FAULT LED flashes. Inside the front panel door, the CS board LED bank displays error codes. The displayed hexadecimal error codes indicates conditions that require a reset for recovery. Record the error code before attempting a reset. Most likely, the failure is in the basic control board. The CS board LED indications are listed in Table 7-1.

Table 7-1. CS Board LED Bank Indications

LED	OPERATING INDICATIONS	HALTED INDICATIONS	
10	Command Active	Error Code, Bit 1	Least
9	Command Waiting	Error Code, Bit 2	Significant
8	Reserved	Error Code, Bit 4	Byte Of
7	Reserved	Error Code, Bit 8	Error Code
6	Reserved	Error Code, Bit 16	Least
5	Drive Address, LSB	Error Code, Bit 32	Significant
4	Drive Address	Error Code, Bit 64	Byte Of
3	Drive Address, MSB	Error Code, Bit 128	Error Code
2	(Not Used)	(Not Used)	
1	(Not Used)	Controller Halt	

The error codes displayed in hex on the CS board LED bank when the controller halts due to a failure are listed in Table 7-2.

Table 7-2. CS Board LED Error Codes

ERROR CODE	DESCRIPTION	ERROR CODE	DESCRIPTION
0B	No Available Queue	20	Timeout Recovery Not Allowed
0C	Invalid Command Decode	21	Unable to Find End of List
0D	Unable to Allocate Memory	22	Entry Not in List
0E	On-Line CPA Table Error		
0F	Off-Line CPA Table Error	28	Watchdog Timeout #2
10	State Change CPA Table Error	29	Command Timeout Invalid
11	CPA FIFO Overflow	2a	Invalid Operation Timeout
		2b	Invalid Error Type
14	Invalid Command Code	2c	Invalid Error Type
15	Invalid Drive Type	2d	Invalid Error Type
16	Invalid Status		
17	Invalid Attention Status	2f	Timeout Recovery Not Allowed
18	Disk Pointer Invalid	30	Watchdog Timeout — Illogical
19	No Pointer	31	Invalid Error Jumper Pointer
1A	Invalid Interrupt	32	Invalid Error Jumper Pointer
		33	Invalid Command
1E	CPA Configuration Error		
1F	Unable to Find End of List	3D	No Map Pointer

CONTINUED

Table 7-2. CS Board LED Error Codes (Continued)

ERROR CODE	DESCRIPTION	ERROR CODE	DESCRIPTION
3F	Invalid Duart Interrupt	F0	Unused Interrupt Vector
40	Invalid Semaphore	F1	Bus Fault Interrupt
41	Invalid Interrupt Occurred	F2	Address Fault Interrupt
42	Invalid Interrupt Occurred	F3	Illegal Instruction Interrupt
43	Invalid Interrupt Occurred	F4	Spurious Interrupt Vector
44	Invalid DEVF Flag Occurred	F5	Uninitialized Interrupt Vector
45	Invalid DOC Parameters	F6	Unused Autovector Interrupt
46	FBC DT_FORK Not Equal to CCB		
47	FBC DT_FORK Not Equal to CCB		
48	DCTB Is Not Assigned to CCB		

Disk Cache Processor Faults

Troubleshooting the DCP begins with examining the LEDs on the DCP board. The nine LEDs on the DCP board indicate both operating and diagnostics status. LED indications are listed in Table 7-3.

Table 7-3. DCP LED Indications

LED	OPERATING INDICATIONS	RESIDENT DIAG. MODE
9	Not Used	Not Used
8	DCP Read	Not Used
7	DCP Write	Not Used
6	DCP Hit	Not Used
5	DCP Phase	Bank A in Memory Testing
4	Not Used	Bank B in Memory Testing
3	Not Used	Bank C in Memory Testing
2	Not Used	Bank D in Memory Testing
1*	DCP Halt	Not Used

* LED 1 is closest to the front of the chassis.

When the DCP is reset or powered-on, it performs the resident diagnostics. If the DCP does not test all memory banks, indicated by the appropriate LED lighting, check that all DRAM chips are seated with no bent pins. Also, if DIs are installed above (on top of) the DCP, remove them and try again.

If the DCP does not engage correctly, there is probably a communications problem within the controller. See "Using the Disk Cache Processor Monitor" for debugging through RS-232 port.

During system operation, XDISK ERROR occurs on the RS-232 terminal when the CLUSTOR returned an error while processing a read request for the DCP. Run SIDOS on the disk area reported. The detection of a bad sector is usually the cause.

COPY TIMEOUT ERROR occurs when the host requests a disk block which the CLUSTOR cannot supply. Usually, the DCP timed out waiting to copy data as it is read from the disk and sent to the host. Analyze the system error log and run the appropriate diagnostics. The detection of a bad sector is usually the cause.

Almost all DCP traps indicate a bad DCP board. A trap is indicated by an EC*xx* code on the front panel in the DCP 'average' displays. Record the trap code on the board return tag. The codes are listed in Table 7-4.

Using the Disk Cache Processor Monitor

The DCP monitor is most helpful when troubleshooting an apparent DCP problem. There is no need to halt or interrupt the controller processing when using the DCP monitor.

- Connect a VT-type terminal to the RS232-C port at the rear of the CLUSTOR chassis.
- At the front panel, open the access door and set the Com Port switch to DCP. Turn on the terminal.
- To obtain the SI prompt, disable caching, and take the DCP off-line to the controller, enter:

  <CONTROL> C

Table 7-4. DCP Error Codes

ECxx*	MEANING
01	Uncorrectable parity error
04	A nonexistent ACIA is being read
48	Timeout on mailbox full
84	A trap value in SBTRAP was found
94	Memory Link Lost
AC	Verify found AQB empty
12A	Checksum fail

* Displayed in front panel 'average' displays

With the DCP on-line to the controller, the controller continues to send the DCP commands and communications. The control characters are not echoed on the screen. The prompt appears as: SI>.

- At this point, enter the help command:

  SI> **HELP <RETURN>**

  The terminal displays a list of all available commands. DCP Monitor commands (MAGIC and M) are discussed below. Other DCP commands are discussed in "SI> Prompt Commands" later in this chapter.

- Return the DCP to normal operation from the SI> prompt by entering the following:

  SI> **RUN <RETURN>**

DCP Monitor Commands

Begin the DCP Monitor by entering the following two commands:

SI> **MAGIC <RETURN>**

SI> **M <RETURN>**

The MAGIC command begins the DCP program, and the M command initiates the monitor. The asterisk (*) is the monitor prompt. Valid monitor commands are listed below.

DR <RETURN>	Display registers
AD <RETURN>	Display auxiliary memory
*D*n*/	Displays data register contents and allows changes
A*n*/	Displays address register contents, allows changes
addr/	Displays DCP memory address contents, allows changes
<RETURN>	Executes code starting at the program counter

The *n* identifies the number of the data or address registers; 0 through 7 are valid entries.

Commands that allow the user to enter changes display current contents. The program then waits for either a numeric entry or a RETURN.

If there has been no modification of the program counter (PC) the execute command (a RETURN at the asterisk prompt) displays the SI> prompt. If the PC has been changed, first set the PC to 1000, then enter G, as in this example:

* **PC/** *XXXX* **1000 <RETURN>**

* **G <RETURN>**

The *XXXX* is the current value of the PC. Reaching the SI> prompt in this way has the same effect as using the cache reset switch on the CS board.

If a trap or failure occurs while at the monitor prompt (*) the program displays a message about the error and a complete display register (DR). To reach the S|> prompt and preserve all data, enter an F:

```
* F <RETURN>

S|>
```

DR is one of several commands entered from the monitor to get more information about an error trap. This command displays the current DCP and 68000 registers, as in the following example.

```
* DR <RETURN>
                PC 00002616 (A034)          SR 2100      TRACE OFF
D0 00000006     D3 AAAA0002   A0 000004AA   A3 000045E2  D6 00000000  D7 00000000
D1 00000002     D4 AAAAAAAA   A1 00004010   A4 00004C06  A6 000009E8  A7 000001FE
D2 00000000     D5 AAAAAAAA   A2 00000200   A5 00004C06  S:  0002 0000 0006 0000
DS  0082        DC  0103      AQ FE0FFEBE   AL  0010     CW D653
*
```

Entries in the example are defined below.

PC — Program Counter: 68000 program counter value and, in parentheses, the contents of that location. This field shows where the 68000 was, and the first word of the instruction being executed when the error trap occurred.

SR — 68000 Status Register: 68000 status register value at the time of the trap. Register bit definitions are found in Table 7-5.

The trace bit (15) should be off, since the cache runs without tracing 68000 instructions. Because the cache code runs in supervisor mode, the supervisor bit (13) should be set. CPU priority bits (10, 9, 8) normally is 0, 0, 1, respectively, since most of the cache runs at priority 1. Condition codes bits (4, 3, 2, 1, 0) depend on the routine that trapped.

TRACE — Trace State: shows state of the Monitor's trace mode, either on or off. Trace mode is used during assembly debug to single step or break 68000 instructions. Trace mode is always off after an error trap since the cache runs with trace off (this field is not the same as the state of the 68000 trace bit, bit 15 of the 68000 Status Register).

D0—D7 — Data Registers 0 through 7: value in these registers depends on the trapping routine.

A0, A1 — Address Registers 0 and 1: value in these registers depends on the trapping routine.

A2 — Address Register 2: value is FORTH user area pointer and should always contain $200.

Table 7-5. 68000 Status Register Bits

BIT		DESCRIPTION
15	T	Trace Bit. If set, processor interrupts through vector at $24 on completion of each instruction
14	—	Not Used
13	S	Supervisor State. 0 = User State
12—11		Not Used
10	Priority CPU	Priority 0 — 7. Interrupts must be at a higher level to be serviced
9	Priority CPU	Priority 0 — 7. Interrupts must be at a higher level to be serviced
8	Priority CPU	Priority 0 — 7. Interrupts must be at a higher level to be serviced
7—5	—	Not Used
4	X	Extend Bit
3	N	Negative Bit
2	Z	Zero Bit
1	V	Overflow Bit
0	C	Carry Bit

A3—A5 Address Registers 3 through 5: value in these registers depends on the FORTH inner interpreter, NEXT. A5 points into the parameter field of the FORTH word currently in control of the FORTH interpreter.

A4 and A3 point into the FORTH word being called from the parameter field of the controlling word; A4 points to the top of the parameter field and A3 points to the code field. If the called word is a FORTH primitive (implemented in assembly code rather than calls to other FORTH words) A3 and A4 both point to the parameter field.

A6 Address Register 6: parameter stack pointer value, always between $800 and $A00. Normally, A6 points to a few locations below $A00 and the stack grows toward lower memory.

A7 Address Register 7: return stack pointer value, always between $100 and $200. Normally, A7 points a few locations below $200, since the top of the return stack is at $200 and the stack grows toward lower memory.

S: Parameter Stack: value is the top four words of the parameter stack. The value at the top of the stack is the right-most value listed.

DS DCP Status Register: DCP status register value at the time of the trap. Register bit definitions are listed in Table 7-6.

Table 7-6. DCP Status Register Bits

BIT		DESCRIPTION
15	DBA MODE	Data bus-to-auxiliary mode. The DCP is configured to transfer from the 2500 data bus to auxiliary memory.
14	ADB MODE	Auxiliary-to-data bus mode. The DCP is configured to transfer from auxiliary memory to the 2500 data bus.
13	PA MODE	Processor-to-auxiliary mode. The DCP is configured to transfer from the 68000 to auxiliary memory.
12—11	—	Not Used
10	AP MODE	Auxiliary-to-processor mode. The DCP is configured to transfer from auxiliary memory to the 68000.
9—8	—	Not Used
7	LAT PHI	Not Used
6	LAT PLO	Latch parity high and low. The last parity bits read. Not currently used.
5	2500 BA	2500 bus available. Not currently used.
4	OBX FULL	Out box full. The out mailbox still contains mail from the 68000 to the 2500.
3	BX FULL	In box full. The in mailbox contains mail from the 2500.
2	IAQ FULL	Address queue full. The top (2nd) location of the address queue is loaded.
1	AQ EMP	Address queue empty. The last value in the address queue has been used.
0	PAR ERR	Parity error. Value of the parity error flip-flop.

DC DCP Control Register: value in the DCP control register buffer, a software location, at the time of the trap. The buffer value should always be in the control register, since the register is always updated whenever the buffer is changed. Register bit definitions are listed in Table 7-7.

The transfer mode bits of the DCP control register bits 14, 13, 12, and 11 are connected to bits 15, 14, 13, and 10, respectively, of the DCP status register. These four bits should always be the same in both registers. Only one bit should be set at a time, since the modes are mutually exclusive.

Table 7-7. DCP Control Register Bits

BIT		DESCRIPTION
15	DMA DIR	DMA direction. Determines the direction of the DMA transfer for direct DCP to host transfers. Not currently used.
14	ADB MODE	Auxiliary-to-data bus mode. Set during transfers from auxiliary memory to the 2500 data bus.
13	DBA MODE	Data bus-to-auxiliary mode. Set during transfers from the 2500 data bus to auxiliary memory.
12	AP MODE	Auxiliary-to-processor mode. Set during transfers from auxiliary memory to the 68000.
11	PA MODE	Processor-to-auxiliary mode. Set during transfers from the 68000 to auxiliary memory.
10	DREQ ENB	Data request enable. Enables the DCP to send data request to the host for direct DCP to host transfers. Not currently used.
9	DIS PE	Disable parity errors. Prevents the parity flip-flop from being set by a parity error.
8	AQ EMP MASK	AQ-empty-mask. Prevent the AQ-empty state from interrupting the 68000.
7	CHK WD ENB	Check word enable. Enables writing the checksum into auxiliary memory after the word count rolls over. Disabled during header writes.
6—4	DCP SELECT CODE	Determines the CPA port where the DCP resides, always set to 0 by the DCP code.
3	XOR PHI	Not used.
2	XOR PLO	Exclusive-ORs the sense of the high and low parity bits during writes to auxiliary memory.
1	AQNF MASK	AQ-not-full mask. Prevents AQ-not-full state from interrupting the 68000.
0	DCP ENB	DCP enable. Read by the 68000 as bit 5 of the 68000 status register to determine if the DCP is engaged.

AQ Hardware address queue: value is at the bottom of the hardware address queue (HAQ) at the time of the trap. The lower six hex characters are the address accessed in auxiliary memory. The upper two hex characters are the word count. When the HAQ is reloaded with the beginning address and the original word count of the group of words just transferred.

A word count of FE (–2) indicates that a header link (all links are two words) was read or written last at the AQ address. A word count of FA (–6) indicates that a header preface (six words) was read at the AQ address. A zero (0) word count (–256) indicates that a block was last transferred to or from the AQ address.

Word counts other than –2, –6, or –256 indicate that the transfer did not complete. A transfer normally aborts because the DCP hardware believes it found a parity error which was not correctable.

AL Auxiliary latch: value is the last word read from or written to auxiliary memory. The DRAM column strobe clocks the auxiliary memory data bus into the auxiliary latch every memory cycle, whichever direction the data is moving.

CW Checksum register: value accumulated in the checksum register. The checksum register accumulates data for both read and write accesses to auxiliary memory.

DCP Display Examples

The following are DCP screen display examples which are displayed during maintenance and troubleshooting, configuring, and status. They include: mailbox log, journal log, command queue, drive status table, statistics, and configuration.

MAILBOX LOG (.M)

		MAILBOX				
OPCD		CPA	ID	RMDA	RMDC	RMWC
WRITE	drv 1	0	23	0	137	FF00
WRITE COPY		0	23			
START XFR		0	23			
WRTCHK	drv 1	0	24	0	137	FF00
DCP PASS		0	24			

JOURNAL LOG (.J)

RQN	TIME	CMD	WC,S	D	CYL	H	S	FCADDR	COMMENT	ID
66353	1184.5763	RD	256,1	3	417	11	22	F7C7F	* HIT	2006
66352	1184.5486	DRD	2048,8	0	411	4	17	19036	* RD DSK	2005
66351	1184.5401	RD	256,1	0	411	4	17	0	* MISS	2005
66350	1184.5378	RD	256,1	0	434	4	7	51840	* HIT	2004

COMMAND QUEUE (.Q)

CMD-QUE AT 61404
Complete

COMMAND	WTCHK	ID# 24	CPA# 0
RMDA	0	RMDC	137
RMWC	FF00	RECSIZE	1
VALID	YES	HASHTBL	68380
JOURNAL#	65BC0	SOME W/B	NO
HIT	NO	RD OR WRT	NO
WRT THRU	NO	WRITEBACK	NO
WRITE	NO	HEADER	11370000
CACHE ADR	0	SRCH LNGTH	0
DRIVE	1	ERR STATUS	
Vector:	SERVICE-WRITECHECK		
DCP Function:	PASS	XFR MODE:	
READMIN:	8	WRITEBACKS	OFF

Hit Q to abort, any other key to continue

DRIVE STATUS TABLE (.D)

DRIVE	0	1	2	3	4	5	6	7
STATUS	C00	C00	E00	000	C00	C00	C00	C00
MAX DRIVE PARAMETERS (VALID)								
MAX CYLS	823	2099	1023	1027	823	823	823	823
MAX HEADS	19	15	27	NED	19	10	10	19
MAX SCTRS	64	52	70	256	64	32	32	64
DRIVE CACHING AREA								
HIGH CYLINDER	823	2099	1023	0	823	823	823	823
HIGH HEAD	19	15	27	NED	19	10	10	19
HIGH SECTOR	64	52	70	0	64	32	32	32
LOW CYLINDER	0	0	0	0	0	0	0	0
LOW HEAD	0	0	0	NED	0	0	0	0
LOW SECTOR	1	1	1	0	1	1	1	1

STATISTICS (.ST)

*** DCP II STATISTICS ***

Requests	40
Hits	10
Writes	15
Reads	20
Write-checks	5
Errors	0

CONFIGURATION (.C)

*** DCP II CONFIGURATION ***

Read Checks	Off
Write Backs	On
Write Alloc	On
Read Alloc Inh	Off
Auto Tuning	On
Cache Size	15477
Max Req	16
Min Req	8
Flush Interval	10
Max Write Bks	20

*** Auto Tuning Statistics ***

Drive	Caching State	Writebacks	MinReq	MaxReq	Errors
0	enabled.	enabled.	8	32	0
1	enabled.	disabled.	8	32	0
2	disabled.	disabled.	0	32	0
3	enabled.	disabled.	4	32	0
4	enabled.	enabled.	8	32	0
5	enabled.	disabled.	6	32	0
6	disabled.	disabled.	0	32	0
7	disabled.	disabled.	0	32	0

Number of changes made 4

Average requests/second 120

SI> Prompt Commands

The SI> prompt commands previously discussed were HELP, RUN, MAGIC, and M. This section describes the .M, .Q, .P, .A, and .J commands.

At the SI> prompt, type **FE<cr>**. The following menu appears:

```
      ***** S.I. Field Service Tools *****

S     Test and size DRAM
.P    Show link parameters
.D    Show drive tables
.A    Show address queue
.M    Show last 80 words through the mailbox
.Q    Show command queue
SM    Scan memory for parity errors
TM    Test PMU display
TL    Test the LRU ring
M     Enter the monitor
LL    Display the LRU ring
LH    Display the hash table
LW    Display the writeback lists
TS    Test the Control Store Board switches
EM    Enable mailbox logging
DM    Disable mailbox logging
HE    Enable mailbox logging and halt on error
CE    Disable mailbox logging and halt on error
```

.M

Entering .M displays the sample mailbox, as shown in this example:

```
SI> .M <RETURN>

                              MAILBOX

OPCD                CPA  ID  RMDA  RMDC  RMWC
WRITE        drv1    0   23    0    137   FF00
WRITE COPY           0   23
START XFR            0   23
WRTCHK       drv1    0   24    0    137   FF00
PASS                 0   24
```

.Q

Entering .Q displays a sample command queue entry display. For example:

```
S1> .Q <RETURN>

CMD-QUE AT 61404
Complete
COMMAND    WTCHK      ID# 24          CPA# 0
RMDA           0      RMDC          137
RMWC/DPT    FF00      RECSIZE         1
VALID        YES      HASHTBL     68380
JOURNAL#   65BC0      SOME W/B       NO
HIT           NO      RD OR WRT      NO
WRT THRU      NO      WRITEBACK      NO
WRITE         NO      HEADER   11370000
CACHE ADR      0      SRCH LNGTH     0
DRIVE          1      ERR STATUS
Vector: SERVICE-WRITECHECK
DCP Function:   PASS   XFR Mode:
(PAUSE)
```

.P

Entering .P displays key cache parameters, as shown in this example:

```
S1> .P <RETURN>

CACHE PARAMETERS :

LHEAD    :      FFEB4
LTAIL    :         10
SHEAD    :          0
SSUCC    :          0
SPRED    :          0
HDADDR   :   3025050E   =   3   37   5   14
LSTSRCH  :          0   =   0    0   0    0
TXCTR    :          0
ERRCD    :          0

S1>
```

LHEAD and LTAIL point to the head and tail of the LRU list.

SHEAD, STAIL, SSUCC, and SPRED point to the string head, tail, successor, and predecessor, respectively, of the last string of blocks moved in the LRU list by MOVESTR.

HDADDR is the beginning disk address of the current host request, stored as a 32-bit value with the fields defined as:

Bits 31 — 29	Drive
Bits 28 — 16	Cylinder
Bits 15 — 8	Head
Bits 7 — 0	Sector

In the cache parameters printout, the disk address is expressed as a 32-bit value and in decimal after the equal sign in the sequence drive, cylinder, head, and sector.

LSTSRCH is the last disk address searched for by SEARCH. Like HDADDR, the address is expressed as a 32-bit value and in decimal after the equal sign.

TXCTR is the number of blocks the cache still had to transfer from the software AQ to the hardware AQ.

ERRCD is the last error code that trapped into the Monitor.

.A

Entering .A displays the software address queue, as shown in this example:

```
SI> .A <RETURN>
    FE65B
    FFEB4
    FEDC4
    FF63C
SI>
```

The software address queue contains the beginning addresses of the cache blocks being transferred out of cache. If the request is a miss or a write-with-allocate (write back or write-through-with-allocate) the data is transferred into cache. The maximum block address possible is $003FFEAA for an 8-Mbyte cache.

All cache blocks are $10F (271 decimal) words long. Since the first block starts at $10, dividing any block address minus $10 by $10F must result in the block number with a zero remainder, as follows:

$$\frac{\text{Block Address} - \$10}{\$10F} = \text{Block Number, with no remainder}$$

In this way, any block address with a remainder is invalid. The debug version of the cache code used by SI Engineering employs this method to check the validity of every cache address generated. The production version checks only for a zero cache address.

If the data transfer portion of the last request has finished, the AQ is empty.

.J

Entering .J to the SI> prompt displays the DCP journal. The journal holds the last 682 transactions through the DCP, as shown in this example:

```
SI> .J <RETURN>
```

RQN	TIME	CMD	WC,S	D	CYL	H	S	FCADDR	COMMENT	ID
66353	1184.5768	RD	256,1	3	417	11	22	F7C7F	* HIT	2006
66352	1184.5736	SR	0,0	3	417	11	19	0	*KILLED	2005
66351	1184.5480	DRD	2048,8	0	411	4	17	19036	*RD DISK	2004
	1184.5400	RD	256,1	0	411	4	17	19036	*MISS	2004
66350	1184.5376	SR	0,0	0	411	4	14	0	*KILLED	2003
66349	1184.5104	RD	256,1	0	434	4	7	51840	*HIT	2002

RQN is a 32-bit request number assigned sequentially as each request comes into the DCP. RQN is cleared when the cache is engaged. In the example above, the entry above 66350 is the first transaction of 66351. It is a host read request that was not in cache, thus the comment "*MISS". The next action is the DCP request to the 2500 to read eight sectors, the requested (missed) one and the next seven to make a MINREQ of eight.

TIME is the value of the DCP clock, in seconds, when the record was journalized.

CMD lists the command for the transaction. Commands beginning with a D are issued by the DCP. All others, except PK, are issued by the host. PK is issued by the 2500 to inform the DCP that a disk status has changed. DCP commands are shown in Table 7-8. Commands not listed (offset, for example) are not processed by the DCP, and so do not appear in the journal.

Table 7-8. DCP Commands

COMMAND	DESCRIPTION	RMCS1 REGISTER COMMAND VALUE
RD	Host Read	71
RHD	Host Read Header and data	73
WR	Host Write	61
FW	Host Write Header and data	63
WCH	Host Writecheck	51
SR	Host Search	31
SK	Host Seek	5
PK	Status Change	--
DRD	DCP Read Disk (fills to MINREQ)	--
DWR	DCP Write Disk (flushes Writeback data)	--

RMCS	0000C8B0	
		WRITE DATA
		DRIVE AVAILABLE
RMDS	000051C0	
		VOLUME VALID
		DRIVE READY
		DRIVE PRESENT
		MEDIUM ON-LINE
		COMPOSITE ERROR
RMER1	00002000	
		OPERATION INCOMPLETE
RMMR1	00000000	
RMAS	00000000	
RMDA	00000644	**<---- SECTOR 68.**
		SECTOR = 4. **<---- MASKED BY VMS**
		TRACK = 6.
RMDT	00002017	
		DRIVE TYPE RM05
		MOVING HEAD
RMLA	00008000	
		SECTOR COUNTER = 0.
RMSN	0000541A	
RMOF	00001800	
		ECC INHIBIT
		16-BIT FORMAT
RMDC	000005F4	**<---- CYLINDER 1524.**
		DESIRED CYLINDER = 500. **<---- MASKED**
RMHR	00000042	**<---- RMCS2 AGAIN**
RMMR2	00000000	
RMER2	00000000	
RMEC1	00000000	
RMEC2	00000000	
UCB$B_ERTCNT	07	
		7. RETRIES REMAINING
UCB$B_ERTMAX	08	
		8. RETRIES ALLOWABLE
ORB$L_OWNER	00010004	
		OWNER UIC [001,004]

WC, S is the word count and equivalent sector count. The sector count value includes a plus sign (+) if the word count spills over the number of sectors shown. For example, a word count of 514 appears as 514,2+.

D CYL H S identifies the disk address of the transaction in the form drive unit number, cylinder, head, and sector. The address shown is the logical address, not yet mapped by the 2500.

FCADDR is the cache address of the first block of data for the transaction. For a HIT, the FCADDR shows the address of the first block of data found. For a MISS, FCADDR shows the address of the first block of data stored. FCADDR is set to zero (0) when a request is first logged by the DCP and is updated while processing the command.

COMMENT shows a brief explanation of the transaction. *KILLED for the search and seek commands indicates the commands are "killed" by the DCP; it is assumed that the data is in cache and movement of the disk arm (head seek) is unnecessary. *PASS indicates the request was serviced around the cache, either because it was larger than MAXREQ, or the word count was not a multiple of 256.

ID is the 2500 command packet identification number. This number is assigned to each communication between the 2500 and the DCP.

7.3 VMS Error Log Entries

Qbus Error Log Entries

When CLUSTOR is attached to a VAX via the Qbus, there are some anomalies in the entries of the VMS error log. The following is an example of an error log entry. Items to note are bold and underlined. Comments are bold and follow an arrow.

```
ERROR SEQUENCE 9134.                                LOGGED ON:SID 0A000004
DATE/TIME 18-FEB-1991 21:40:02.02                     SYS_TYPE 01530201
SCS NODE: TOMMY                                         VAX/VMS V5.3-2

TIME STAMP      KA640      CPU REV# 5.      FW REV# 5.3

MASSBUS SUB-SYSTEM, UNIT _TOMMY$DRB2:
   'RH' REGISTER   #1FFFE0542
   'RH' REGISTER   #200000000
   'RH' REGISTER   #300420001          <--- CLUSTOR RMCS2
   'RH' REGISTER   #400000000
   'RH' REGISTER   #50000F800
   'RH' MPR #???     8000C556
```

UCB$L_CHAR	1C4DC008	
		DIRECTORY STRUCTURED
		FILE ORIENTED
		DUAL ACCESS
		SHARABLE
		AVAILABLE
		MOUNTED
		ERROR LOGGING
		CAPABLE OF INPUT
		CAPABLE OF OUTPUT
		RANDOM ACCESS
UCB$W_STS	1910	
		ONLINE
		BUSY
		SOFTWARE VALID
		UNLOAD AT DISMOUNT
UCB$L_OPCNT	0000AE54	
		44628. QIO'S THIS UNIT
UCB$W_ERRCNT	0001	
		1. ERRORS THIS UNIT
UCB$L_MEDIA	05F40644	**<--- CYLINDER, TRACK, & SECTOR**
		FUNCTION START ADDRESS,
		- CYLINDER#1524.,
		- TRACK#6.,
		- SECTOR#68.
IRP$W_FUNC	000B	
		WRITE PHYSICAL BLOCK
IRP$W_BCNT	1000	
		TRANSFER SIZE 4096. BYTE(S)
IRP$W_BOFF	0000	
		TRANSFER PAGE ALIGNED
IRP$L_PID	00010065	
		REQUESTOR 'PID'
IRP$Q_IOSB	10000001	
	00000000	IOSB, 4096. BYTE(S) TRANSFERRED

Error Log for MSCP

When CLUSTOR is attached to a VAX via MSCP, there are some anomalies in the entries of the VMS error log. The following is an example of an error log entry. Items to note are bold and underlined. Comments are bold and follow an arrow.

```
ERROR SEQUENCE 9.                                   LOGGED ON SID 02005F78
ERL$LOGMESSAGE ENTRY     20-APR-1989     10:21:55.41

KA750          REV# 120.  UCODE          REV# 95.

I/O SUB-SYSTEM, UNIT _DUA0:
   MESSAGE TYPE                0001
                                          DISK MSCP MESSAGE
   MSLG$L_CMD_REF          99730004
   MSLG$W_SEQ_NUM              0001
                                          SEQUENCE # 1.
   MSLG$B_FORMAT                 00
                                          CONTROLLER ERROR
   MSLG$B_FLAGS                  00
   MSLG$W_EVENT                00E8
                                          DATA ERROR
                                          UNRECOVERABLE ECC ERROR
   MSLG$Q_CNT_ID           00340000
                           02050000
                                          UNIQUE IDENTIFIER, 000000340000
                                          DISK CLASS DEVICE
                                          RA82
   MSLG$B_CNT_SVR                01
                                          CONTROLLER SOFTWARE VERSION #1.
   MSLG$B_CNT_HVR                01
                                          CONTROLLER HARDWARE VERSION #1.

CONTROLLER DEPENDENT INFORMATION
                                          CLUSTOR COMMAND PACKET
   LONGWORD 1.    00002008                <--- UNIT # IN 3 MOST SIG BITS
   LONGWORD 2.    00000050
   LONGWORD 3.    00000000
   LONGWORD 4.    00030070                <--- START OF CLUSTOR RESPONSE
   LONGWORD 5.    12000000
```

LONGWORD 6.	00000000	
LONGWORD 7.	00000000	<--- EXTENDED STATUS
LONGWORD 8.	10000000	
LONGWORD 9.	04000000	
LONGWORD 10.	0000E202	
LONGWORD 11.	00000000	

As shown above, the right byte containing 70 indicates the start of the response message. Sometimes this packet starts at longword 3 instead of 4, so check for the 70. Two bytes to the left (03) is an error class number. The right-most byte in longword 1 is the operation code.

The extended status bytes contain additional error information for the class and are listed with the valid option codes in Table 7-9.

Table 7-9. Valid Operation and Error Class Codes

VALID OPERATION CODES				
		08	READ	
		28	READ	
		3E	READ	
		0B	SEEK	
		2B	SEEK	
		2F	WRITECHECK	
		0A	WRITE	
		2A	WRITE	
		3F	WRITE	
ERROR CLASS AND CODES				
CLASS 0E	MISCOMPARE	CODE	001D	WRITECHECK ERROR
CLASS 02	DRIVE STATUS	CODE	003A	NON-EXISTENT DRIVE
CLASS 02	DRIVE STATUS	CODE	0004	DRIVE UNSAFE
CLASS 02	DRIVE STATUS	CODE	0204	INVALID COMMAND
CLASS 03	MEDIUM	CODE	0011	ECC ERROR / DATACHECK
CLASS 03	MEDIUM	CODE	0215	HEADER COMPARE ERROR
CLASS 03	MEDIUM	CODE	0010	HEADER CRC ERROR
CLASS 03	MEDIUM	CODE	0021	ADDRESS OVERFLOW
CLASS 04	HARDWARE	CODE	0016	DRIVE TIMING ERROR
CLASS 04	HARDWARE	CODE	0041	DATA BUFFER PARITY ERROR
CLASS 04	HARDWARE	CODE	0002	SEEK INCOMPLETE
CLASS 04	HARDWARE	CODE	0044	DEVICE CLOCK ERROR
CLASS 05	REQUEST	CODE	004E	PROGRAM ERROR
CLASS 05	REQUEST	CODE	0021	INVALID ADDRESS
CLASS 07	PROTECTION	CODE	0027	WRITE PROTECT
CLASS 0B	ABORT	CODE	0600	MISSED TRANSFER

eaSIshadow Error Log Entries

On CLUSTOR (M) systems where eaSIshadow is running, VMS cannot determine the device type when logging an error. Therefore the registers are not properly decoded. The following is an example error log for a shadowed set on CLUSTOR (M). The location of each RM is denoted to the right in bold type following an arrow.

```
ERROR SEQUENCE 275.                          LOGGED ON: SID 0A000005
DATE/TIME 18-FEB-1991 08:39:02.34                 SYS_TYPE 01530301
SCS NODE: STAVAX                                     VAX/VMS V5.3

"UNKNOWN DEVICE" ENTRY  KA655  CPU REV# 6.  FW REV# 5.3

ERROR LOG RECORD

   ERF$L_SID          0A000005
                                   SYSTEM ID REGISTER

   ERL$W_ENTRY             060
                                   ERROR TYPE ENTRY

   EXE$GQ_SYSTIME     7E65B840
                      00944684     64 BIT TIME WHEN ERROR LOGGED
   ERL$GL_SEQUENCE         0113
                                   UNIQUE ERROR SEQUENCE = 275.
   UCB$B_ERTCNT              00
                                   REMAINING RETRIES = 0.
   UCB$B_ERTMAX              CA
                                   MAXIMUM RETRIES = 202.
   IRP$Q_IOSB         08005600
                      0000022C     FINAL IOSB
   UCB$W_STS               000C
                                   DEVICE STATUS
   UCB$B_DEVCLASS            00
                                   DEVICE CLASS = 0.
   UCB$B_DEVTYPE             00
                                   DEVICE TYPE = 0.
   IRP$L_PID          00010950
                                   REQUESTING PROCESS ID
   IRP$W_BOFF              0000
                                   TRANSFER BYTE OFFSET = 0.
   IRP$W_BCNT              0200
                                   TRANSFER BYTE COUNT = 512.
   UCB$L_MEDIA        013E0034
                                   DEVICE DEPENDENT PHYSICAL
                                   ADDRESS
   UCB$W_UNIT              0000
                                   PHYSICAL UNIT NUMBER = 0.
```

UCB$W_ERRCNT	0001	UNIT ERROR COUNT = 1.
UCB$L_OPCNT	00000003	UNIT OPERATION COUNT = 3.
ORB$L_OWNER	00000000	OWNER UIC = [000,000]
UCB$L_DEVCHAR	1C41C008	DEVICE CHARACTERISTICS
UCB$B_SLAVE	00	DEVICE SLAVE CONTROLLER = 0.
IRP$W_FUNC	000C	QIO FUNCTION CODE
DDE$T_NAME	4154530A 24584156 00415244 00000000	/STAVAX$DRA/ DRIVE 0 TO BE EXACT
LONGWORD 1.	00000018	
LONGWORD 2.	FFFE0504	
LONGWORD 3.	00000000	
LONGWORD 4.	04400000	<---- RMCS2
LONGWORD 5.	00000400	
LONGWORD 6.	0000FF00	
LONGWORD 7.	00000000	
LONGWORD 8.	00000000	
LONGWORD 9.	00000879	<---- RMCS1
LONGWORD 10.	00001140	<---- RMDS
LONGWORD 11.	00000000	<---- RMER1
LONGWORD 12.	00000000	<---- RMMR1
LONGWORD 13.	00000000	<---- RMAS
LONGWORD 14.	00000034	<---- RMDA
LONGWORD 15.	00002017	<---- RMDT
LONGWORD 16.	00008000	<---- RMLA
LONGWORD 17.	00005418	<---- RMSN
LONGWORD 18.	00001000	<---- RMOF

LONGWORD 19.	0000013E	<--- RMDC
LONGWORD 20.	00000440	<--- RMHR
LONGWORD 21.	00000000	<--- RMMR2
LONGWORD 22.	00000000	<--- RMER2
LONGWORD 23.	00000000	<--- RMEC1
LONGWORD 24.	00000000	<--- RMEC2
LONGWORD 25.	FC508000	

8
ILLUSTRATED PARTS LIST

This chapter lists Field Replaceable Unit (FRU) level parts for the CLUSTOR or CLUSTOR/M controller. The chassis and boards are shown in Figure 8-1. CLUSTOR FRUs and their part numbers are listed in Table 8-1.

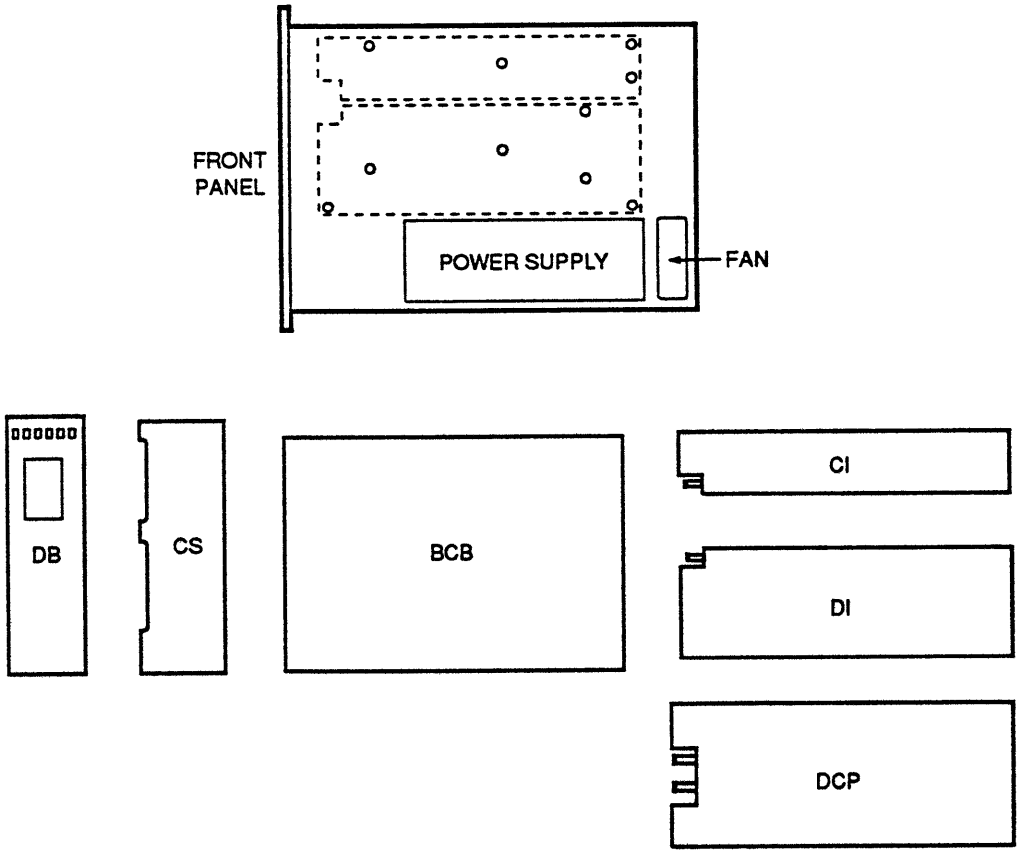


Figure 8-1. CLUSTOR Controller Field Replaceable Units

Table 8-1. CLUSTOR (M) Subsystem Field Replaceable Units

ITEM	PART NUMBER
CLUSTOR Subassembly	
Basic Control Board (BCB)	2500-6001
Control Store Board (CS)	2500-6003
Disk Interface Board (DI)	2500-6004
Computer Interface (CI-STD)	2500-6005
CI, Long Line Adapter Option (CI-LLA)	2500-6006
CI, SCSI Option (CI-SCSI)	2500-6014
CLUSTOR 5 Disk Cache Processor(DCP)	2500-6019
Power Supply	2500-7060
Fan	370-0023
CLUSTOR Front Panel Assembly (Traditional)	
CLUSTOR 3 Front Panel (with DB Board)	2500-7061
CLUSTOR 5 Front Panel (with DB/PM Board)	2500-7062
CLUSTOR Front Panel Assembly (Theta)	
CLUSTOR 3 Front Panel (with DB Board)	2500-7065
CLUSTOR 5 Front Panel (with DB/PM Board)	2500-7064
Long Line Adapter Option	
Long Line Adapter Board (LLA)	2500-7004
Host Computer Port Adapter Assemblies*	
SBI CPA (RM)	2500-7031
Qbus CPA (RM)	2500-6102
Qbus CPA (MSCP)	2500-7087
UNIBUS CPA (RM)	2500-6101
BI Bus CPA (MSCP)	2500-7088
Host Computer Transition Panels/Internal Cables	
SBI CPA Internal Cabling (RM):	
5-inch SBI Bus Cable	6000-7362
18-inch SBI Bus Cable	6000-7361
Qbus (MicroVAX II) Transition Panel/Internal Cabling (RM)	9902-7062
Qbus (MicroVAX 3300-3900 or VAX 4000) Transition Panel/Internal Cabling (RM)	9902-7149
UNIBUS (VAX 11/7XX & 86XX) Transition Panel/Internal Cabling (RM)	9902-7063
BI Bus (VAX 8XXX except 86XX) Transition Panel/Internal Cabling (MSCP)	9902-7060

* Include transition panels and internal cables

Table 8-1. CLUSTOR (M) Subsystem Field Replaceable Units (Continued)

ITEM	PART NUMBER	
External Cables (CPA to CLUSTOR)		
RM-Compatible CPAs (SBI, UNIBUS, Qbus)	MicroVAX 3300-3900 or VAX 4000 CPU	Other CPUs
10 Foot	9902-7164	9901-7915
20 Foot	9902-7148	9901-7916
33 Foot	9902-7165	9901-7917
50 Foot	9901-7918	9901-7918
100 Foot	9901-7919	9901-7919
150 Foot	9901-7920	9901-7920
MSCP-Compatible CPA/Ms (BI Bus, Qbus)		
8 Foot		9902-7330
12 Foot		9902-7331
25 Foot		9902-7360
50 Foot		9902-7361
70 Foot		9902-7362

9
READY REFERENCE

This chapter provides a quick reference of installation information on CLUSTOR configuration limits and board settings.

9.1 Configuration Requirements

1. *Computer Port Adapters:*

   Minimum of one, maximum of eight per CLUSTOR 3 or 5 controller.
   Minimum of one, maximum of four per CLUSTOR/M controller.
   Multiport configurations mount disks on only one CPA and reserve the second.

2. *CPA to CLUSTOR Cabling*

   RM Regular: 33 feet external to the cabinet, maximum of 50 feet total.
   Long Line Adapter Option: 150 feet external, maximum of 200 feet total. Requires a Long Line Adapter Computer Interface (CI-LLA) board.

   MSCP Maximum total cable length is 80 feet between the CPA/M and CLUSTOR CI/M, including both internal and external cables.

3. *Computer Interface Board*

   Minimum of one, maximum of four per CLUSTOR (M) controller.
   Each CI supports two CPAs. The CI-LLA board requires LLA option for both CPAs it supports.

4. *Drive Interface Board*

   Minimum of one, maximum of four per CLUSTOR (M) controller.
   Each DI has two independent disk drive interface circuits of 1 or 2 disk drives. Dual-disk configurations require physically adjacent, identical disk model types.

5. *Disk Drive*

   Minimum of one, maximum of 16 per CLUSTOR 3 or 5 controller.
   Minimum of one, maximum of 14 per CLUSTOR/M 3 or 5 controller.

   RM-emulation: The number of disk drives depends on the format type. The disk drive formats can be mixed, but cannot emulate more than eight logical disk drives. Configured as dual-disks only, CLUSTOR supports a maximum of 16 physical disk drives. Configured as mapped or direct only, CLUSTOR supports a maximum of eight physical disk drives. The controller(s) and all drives must be housed in the same single-bay or dual-bay cabinet.

   MSCP-emulation: Disk drive formats can be mixed, but cannot emulate more than seven logical disk drives. Configured as dual-disks, CLUSTOR/M supports a maximum of 14 physical disk drives. Configured as mapped or direct, CLUSTOR/M supports a maximum of seven physical disk drives. The controller(s) and all drives must be housed in the same single-bay or dual-bay cabinet.

6. *Dual Channel Disk Drive Option*

   The drive format must be maintained by definition on each DI connected to the disk drive. Mandatory when using CLUSTOR (M) 5 in redundant applications, only one channel accesses the disk.

7. *Cabinets*

   The physical cabinet restrictions must not be exceeded.
   CLUSTOR 3 or 5: A single-bay or a dual-bay cabinet is used to house the CLUSTOR (M) controller(s) and all the disk drives.

9.2 Disk Drive Support References

The computer operating systems supported are shown in Table 9-1.

Table 9-1. Computer Operating Systems Supported

TYPE	RELEASE LEVEL
VMS	4.4 through 4.7, 5.0 through 5.4-2
ULTRIX	2.0 through 3.1
UNIX BSD	4.3
AT&T UNIX	5.2

The disk drive size and mounting methods are shown in Table 9-2.

Table 9-2. Disk Drive Size and Mounting Methods

DRIVE	DISK SIZE	MOUNTING TYPE
SI56* SI57* SI506 SI510	5.25-inch	Two Drive Quick Release
SI83* SI817 SI85* 9733* SI92* SI95*	8-inch	Two Drive Quick Release Two Drive Fixed Tray
SI93	9-inch	Two Drive Fixed Tray
9751* 9761*	10.5-inch	Cabinet Mount
SSD80 SSD128 SSD256 SSD448	19-inch	Cabinet Mount

* Not available after Dec. 1, 1990.

The supported disk drive capacities are shown in Table 9-3.

Table 9-3. Supported Disk Drive Capacities

DRIVE	UNFORM CAP	FORMAT	LOGICAL UNIT PARAMS				RATIO OF PHYS/LOG	RM DEV DRIVER REQ
			CYL	HEAD	SEC	CAP		
9733*	337MB	Mapped	823	19	32	256MB	1 to 1	No
9751*	474MB	Direct	840	20	47	405MB	1 to 1	Yes
		Dual Disk	1680	20	47	810MB	2 to 1	Yes
9761*	689MB	Direct	840	20	64	551MB	1 to 1	Yes
		Dual Disk	1680	20	64	1102MB	2 to 1	Yes
SI56*	384MB	Direct	1222	15	32	300MB	1 to 1	Yes
SI57*	768MB	Direct	1630	15	48	601MB	1 to 1	Yes
SI83*	690MB	Direct	622	27	64	552MB	1 to 1	Yes
		Mapped	823	19	32	256MB	1 to 2	No
		Dual Disk*	1244	27	64	1.10GB	2 to 1	Yes
SI85*	823.9MB	Direct	743	27	64	659MB	1 to 1	Yes
		Mapped	823	19	32	256MB	1 to 2	No
		Dual Disk*	1486	27	64	1.31GB	2 to 1	Yes
SI92*	1.1GB	Direct	1633	15	70	878MB	1 to 1	Yes
		Dual Disk*	3266	15	70	1.75GB	2 to 1	Yes
SI93*	1173MB	Direct	1022	27	64	900MB	1 to 1	Yes
		Dual Disk*	2044	27	64	1.8GB	2 to 1	Yes
SI95*	2.2GB	Direct	1633	30	70	1.75GB	1 to 1	Yes
		Dual Disk*	3266	30	70	3.5GB	2 to 1	Yes
SI506	776MB	Mapped	823	19	32	256MB	1 to 2	No
		RM05	823	19	32	256MB	1 to 1	No
		Direct	1656	15	47	597MB	1 to 1	Yes
SI510	1200MB	Direct	2099	17	52	950MB	1 to 1	Yes
		Dual Disk	4198	17	52	1.9GB	2 to 1	Yes
SI817	2272MB	Direct	2609	19	70	1.77GB	1 to 1	Yes
		Dual Disk	5218	19	70	3.55GB	2 to 1	Yes
SSD67		Direct*	823	5	32	67MB	1 to 1	No
SSD130		Direct*	797	10	32	130MB	1 to 1	Yes
SSD260		Direct*	590	27	32	260MB	1 to 1	Yes
SSD452		Direct*	1023	27	32	452MB	1 to 1	Yes

* Not available after Dec. 1, 1990.

The disk drive sector counts are shown in Table 9-4. The CS board LED bank indications are shown in Table 9-5.

Table 9-4. Disk Drive Sector Counts (Physical)

DRIVE	SECTOR COUNT
9733	67
9751	48
9761	67
SI83	67
SI85	67
SI56	33
SI57	49
SI92	73
SI93	66
SI95	73
SI506	48
SI510	53
SI817	73
SSD	32

The CS board LED bank indications are shown in Table 9-5.

Table 9-5. CS Board LED Bank Indications

LED	OPERATING INDICATIONS	HALTED INDICATIONS	
10	Command Active	Error Code, Bit 1	Least
9	Command Waiting	Error Code, Bit 2	Significant
8	Reserved	Error Code, Bit 4	Byte Of
7	Reserved	Error Code, Bit 8	Error Code
6	Reserved	Error Code, Bit 16	Least
5	Drive Address, LSB	Error Code, Bit 32	Significant
4	Drive Address	Error Code, Bit 64	Byte Of
3	Drive Address, MSB	Error Code, Bit 128	Error Code
2	(Not Used)	(Not Used)	
1	(Not Used)	Controller Halt	

Display Board

The DB and the DB/PM have no configuration jumpers or switches.

Control Store Board

Jumpers W1, W2, and W3 are located in the CS. W1 is reserved. W2 and W3 jumper settings configure the RS232-C serial interface port signal pin selection. Jumper settings and resulting signal pin selection are listed in Table 9-6.

Table 9-6. CS Board Jumpers: RS232 Communication Port Signal Pins

CS JUMPER	RS232-C	SIGNAL	SELECTION
W2 - B W3 - B	Pin 2 Pin 3	Transmit Receive	Normal Setting
W2 - A W3 - A	Pin 3 Pin 2	Transmit Receive	Alternate

Basic Control Board

Jumpers W1 through W7 are located in the BCB. The settings for these jumpers are defined in Table 9-7.

Table 9-7. BCB Jumpers

JUMPER	LOCATION	SI SETTING	DESCRIPTION
W1	4F	W1C-A	W1-A: Normal W1-B: SI Testing Only
W2	13R	W2C-A	W2-A: 19 (hex) Sync Byte W2-B: 01 Sync Byte (not used)
W3	13R	W3C-A	W3-A: SI Media (56 bit ECC) W3-B: Removable Media (not used)
W4	19C	W4C-B	W4-A: 16 KBytes RAM W4-B: 64 KBytes RAM
W5	23J	W5C-A	W5-A: RM Emulation W5-B:non-RM emulation (not used)
W6	5P	W6C-A	W6-A: Internal ECC Correction W6-B: External ECC (not used)
W7	24H	W7C-A	Reserved (not used)
5G	pin 1 and and 2	IN	When configured with DI boards level -005 or greater
		OUT	When configured with DI boards date code 807 or less

Computer Interface Board (RM-emulation)

The port address select switch, SW1, and the port address indicators, LED1 and LED2 are located in the CI.

SW1, bits 1 and 2 define the port address. SW1, bits 3 and 4 are factory set to OFF, enabling the power fail detection circuit for the even and odd ports on the CI board. The SW1, bits 1 and 2 switch settings, resulting port numbers, and LED indications for the CI board are listed in Table 9-8.

Table 9-8. CI Port Address Values (RM-emulation)

SWITCH		PORT	INDICATORS	
SW1-1	SW1-2	ADDRESS	LED1	LED2
OFF	OFF	0 AND 1	OFF	OFF
ON	OFF	2 AND 3	ON	OFF
OFF	ON	4 AND 5	OFF	ON
ON	ON	6 AND 7	ON	ON

* OFF = Open = 0 ON = Closed = 1

Computer Interface Board (MSCP-emulation)

The CI/M board presents itself to CLUSTOR as a standard CI card and CPA combination; CLUSTOR cannot tell the difference. Switch settings for the CI/M board are shown in Table 9-9.

Table 9-9. CI/M Switch Settings

SWITCH SETTING/ LED		INDICATION
LE1		Self-test LED. LE1 turns off on successful completion of self-test. Also serves as a visual indication of SCSI activity if SW1-4 is ON.
LE2 and LE3		These LEDs give a visual indication of the selected CI port.
W1	OUT	Differential port J2 enabled (default)
W1	IN	Single-ended port J1 enabled
W2	IN	Clock enabled (default)
W2	OUT	Clock disabled

NOTE

Jumpers W1 and W2 are listed for information only. Single-ended SCSI CI cards are only available on special request.

Table 9-10. CI Port Address Values (MSCP-emulation)

SWITCH SW1-1	SW1-2	PORT ADDRESS	INDICATORS LED2	LED3
OFF	OFF	0 AND 1	OFF	OFF
ON	OFF	2 AND 3	OFF	ON
OFF	ON	4 AND 5	ON	OFF
ON	ON	6 AND 7	ON	ON

* OFF = Open = 0 ON = Closed = 1

Modes of Operation

The SCSI CI board can be configured in one of two modes:

1. MULTIPLE TARGET

   The CLUSTOR controller is presented to the SCSI bus as a multiple target device with up to seven logical units, each with its own SCSI ID. In this mode, each logical unit reserves its respective unit number as a SCSI ID, and therefore no other device on the SCSI bus can have the same ID number. This is the default configuration.

2. SINGLE TARGET with MULTIPLE LOGICAL UNITS

   The CLUSTOR controller is presented to the SCSI bus as a single target ID with up to eight logical units attached. This configuration is currently supported only on special request.

	SW1-10	SW2-8
Multiple Target Mode (Default)	OFF	ON
Single Target Multiple LUN Mode	ON	OFF

Multiple Target Mode

When multiple target mode is selected, switch bank 2 (SW2) is used to configure the required disk drives. If a disk drive is not present on CLUSTOR, the respective switch setting must be OFF in order to disable the ID. In this mode of operation the Host Adapter (Initiator) must be preconfigured to a SCSI ID of 7. The SCSI CI drive-enable switch settings for multiple target mode are listed in Table 9-11.

Table 9-11. Multiple Target Mode Switch Settings

Drive Unit ID	Switch Setting	
Enable ID/Drive unit 0	SW2-1	ON
Enable ID/Drive unit 1	SW2-2	ON
Enable ID/Drive unit 2	SW2-3	ON
Enable ID/Drive unit 3	SW2-4	ON
Enable ID/Drive unit 4	SW2-5	ON
Enable ID/Drive unit 5	SW2-6	ON
Enable ID/Drive unit 6	SW2-7	ON

Single Target Mode

If "single target with multiple LUN" mode is selected, SW2 is used to configure CLUSTOR as one SCSI ID which can present multiple logical units to the SCSI bus. Due to host adapter and some device driver limitations this mode is not currently supported. The SCSI CI drive-enable switch settings for single target mode are listed in Table 9-12.

Table 9-12. Single Target with Multiple LUN Switch Settings

Drive Unit ID	SW2-1	SW2-2	SW2-3
Enable as SCSI ID 0	OFF	OFF	OFF
Enable as SCSI ID 1	OFF	OFF	ON
Enable as SCSI ID 2	OFF	ON	OFF
Enable as SCSI ID 3	OFF	ON	ON
Enable as SCSI ID 4	ON	OFF	OFF
Enable as SCSI ID 5	ON	OFF	ON
Enable as SCSI ID 6	ON	ON	OFF
Enable as SCSI ID 7	ON	ON	ON

NOTE

SCSI ID 7 is normally reserved for the host adapter. SW2-4, 5, 6 and 7 are not used in this mode and should be set to the OFF position.

Miscellaneous Default Switch Settings

Disable Data Buffer self-test	SW1-3	OFF
Enable LE1 (self-test LED) as SCSI activity indicator	SW1-4	ON
Enable Disconnect/Reconnect	SW1-5	OFF*

* This feature will be supported shortly. The current default is OFF.

NOTE

SW1-6, 7, 8 and 9 are reserved for future use and should be set to the OFF position.

Disk Interface Board

The port address select switch; SW3, the port address indicators; LED1 and LED2, and the two drive model selection switches; SW1 for the even drive circuit and SW2 for the odd drive circuit are located on the DI board.

SW3, bits 1 and 2 define the port address. SW3, bits 3 and 4 are not used and factory set to OFF. The port address switch settings, resulting port numbers, and the LED indications are listed in Table 9-13.

Settings for each drive model selection switch depend on the drive type and format of the drive(s) supported by that circuit. The settings for each drive model are listed in Table 9-14.

Table 9-13. DI Port Address Values

SWITCH SW3-1	SW3-2	PORT ADDRESS	INDICATORS LED1	LED2
OFF	OFF	0 AND 1	OFF	OFF
ON	OFF	2 AND 3	ON	OFF
OFF	ON	4 AND 5	OFF	ON
ON	ON	6 AND 7	ON	ON

* OFF = Open = 0 ON = Closed = 1

Table 9-14. DI Board Drive Model Switch Settings

DRIVE MODEL SW1 OR SW2	DIP SWITCH NUMBERS 1*	2†	3	4	5	6	7	8	DECIMAL EQUIV.
9733 Mapped	ON	OFF	ON	ON	ON	OFF	ON	OFF	= 5
9751 Direct	ON	OFF	ON	ON	OFF	OFF	ON	ON	= 12
9751 Dual Disk	ON	OFF	ON	OFF	ON	ON	ON	ON	= 16
9761 Direct	ON	OFF	ON	ON	OFF	ON	OFF	ON	= 10
9761 Dual Disk	ON	OFF	ON	OFF	ON	ON	OFF	ON	= 18
SI56 Direct	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	= 27
SI57 Direct	ON	OFF	ON	OFF	OFF	OFF	ON	ON	= 28
SI83 Direct	ON	OFF	ON	ON	OFF	ON	ON	ON	= 8
SI83 Mapped	ON	OFF	ON	ON	ON	ON	OFF	ON	= 2
SI83 Dual Disk	ON	OFF	ON	OFF	ON	ON	OFF	OFF	= 19
SI85 Direct	ON	OFF	ON	OFF	OFF	ON	OFF	ON	= 26
SI85 Mapped	ON	OFF	ON	ON	ON	ON	OFF	ON	= 2
SI85 Dual Disk	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	= 23
SI93 Direct	ON	OFF	ON	ON	ON	OFF	OFF	OFF	= 7
SI93 Dual Disk	ON	OFF	ON	OFF	ON	OFF	ON	ON	= 20
SI92 Direct	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	= 30
SI92 Dual Disk	ON	OFF	ON	OFF	OFF	ON	ON	ON	= 24
SI95 Direct	ON	OFF	ON	ON	OFF	OFF	OFF	ON	= 14
SI95 Dual Disk	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	= 31
SI506 Direct	ON	OFF	ON	OFF	ON	ON	ON	OFF	= 17
SI506 Mapped	ON	OFF	OFF	ON	ON	ON	OFF	OFF	= 35
SI506 RM05	ON	OFF	OFF	ON	OFF	ON	ON	ON	= 40
SI510 Direct	ON	OFF	OFF	ON	ON	OFF	OFF	ON	= 38
SI510 Dual Disk	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	= 39
SI817 Direct	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	= 15
SI817 Dual Disk	ON	OFF	ON	ON	ON	ON	OFF	OFF	= 3
SSD67 Direct	ON	ON	ON	OFF	OFF	OFF	ON	OFF	= 29
SSD130 Direct	ON	ON	OFF	ON	ON	ON	ON	ON	= 32
SSD260 Direct	ON	ON	OFF	ON	ON	ON	ON	OFF	= 33
SSD452 Direct	ON	ON	OFF	ON	ON	ON	OFF	ON	= 34

OFF = Open = 1 ON = Closed = 0

* Bit 1 ON = normal, OFF = logical units daisy-chained.

† Bit 2 OFF = BBF enabled.

Disk Cache Processor Board

Near the DCP board front left side are switches SW1 and SW2. SW1 defines the DCP operational parameters. SW2 defines the disk drives enabled for caching. SW1 and SW2 values are listed in Tables 3-7, 3-8, and 3-9. DCP switch functions are described in "Configurations" (Chapter 3).

Table 9-15. DCP Switch Settings

SWITCH	SETTING	FUNCTION
SW1-8	ON	Write-Back Disabled
-7	OFF	Write-Through-With-Allocate Enabled
-6	ON	Read-Check Disabled
-5	OFF	Minimum Request Size = 8 Sectors
-4	OFF	
-3	OFF	Maximum Request Size = 32 Sectors
-2	OFF	
-1	OFF	Caching Enabled (at power-up)
SW2-8	OFF	Drive 0 Enabled for Caching
-7	OFF	Drive 1 Enabled for Caching
-6	OFF	Drive 2 Enabled for Caching
-5	OFF	Drive 3 Enabled for Caching
-4	OFF	Drive 4 Enabled for Caching
-3	OFF	Drive 5 Enabled for Caching
-2	OFF	Drive 6 Enabled for Caching
-1	OFF	Drive 7 Enabled for Caching

OFF = Open = 1 ON = Closed = 0

Table 9-16. DCP Minimum Request Size Settings

SW1-5	SW1-4	SIZE (sectors)
OFF	OFF	8*
ON	OFF	4
OFF	ON	2
ON	ON	1

OFF = Open = 1 ON = Closed = 0
* default setting

Table 9-17. DCP Maximum Request Size Settings

SW1-3	SW1-2	SIZE (sectors)
OFF	OFF	32*
ON	OFF	24
OFF	ON	16
ON	ON	8

OFF = Open = 1 ON = Closed = 0
* default setting

Table 9-18. DCP Jumpers

JUMPER	LOCATION	SI SETTING	DESCRIPTION
W1	2R	W1C-B	Boot Source: Control Store ROMs*
W2	13K	W2C-B	Cache Memory Size:
W3	13K	W3C-B	CLUSTOR 5: B, Reserved: A
W4	9N	W4C-B	Control Store Size: 128K ROMs
W5	9N	W5C-A	
W7	17R	W7C-D	
W8	17R	W8C-D	
W9	17R	W9C-A	
W6	9N	W6C-A	Static RAM Size

* Factory use only.

Table 9-19. DCP LED Indications

LED	OPERATING INDICATIONS	RESIDENT DIAG. MODE
9	Not Used	Not Used
8	DCP Read	Not Used
7	DCP Write	Not Used
6	DCP Hit	Not Used
5	DCP Phase	Bank A in Memory Testing
4	Not Used	Bank B in Memory Testing
3	Not Used	Bank C in Memory Testing
2	Not Used	Bank D in Memory Testing
1*	DCP Halt	Not Used

* LED 1 is closest to the front of the chassis.

APPENDIX A
DISK DRIVE SETTINGS

This section explains each disk drive and its settings for use in a CLUSTOR (M) subsystem. Refer to the appropriate SI or vendor manual for switch and jumper locations and further information.

NOTE

Solid State Disks do not require sector settings.

A.1 SI56 Disk Drive

The SI56 disk drive is an ESDI interface drive. The 5.25-inch Quick Release Chassis gives the drive an ESDI-SMD interface, making the SI56 Quick Release (SI56QR) an SMD-compatible disk drive.

The ESDI-SMD interface board requires a disk drive address of 0 as set by a jumper on the drive's mother board. The ESDI-SMD interface board uses the address selected by user input from the Quick Release front panel to select drive status. The ESDI-SMD interface reports the front panel address to the DI board as the drive address.

Dual-channel access is through the ESDI-SMD interface board. Channel 1 and Channel 2 controls are on the Quick Release's front panel.

Settings for the SI56 jumpers are listed in Tables A-1 and A-2.

Table A-1. SI56 and SI57 General Jumper Settings (Old - Pre-Fab #8)

JUMPER	SETTING	FUNCTION
JP1	IN	(Test)
JP2	IN	(Test)
JP3	IN	(Test)
JP4	IN	2, 7 Encoding
JP5	IN	15 MBytes/Second Transfer Rate
JP6	OUT	Spin-Up Option Enabled (Quick Release Mounting)
JP7 (DS1) JP8 (DS2) JP9 (DS3) JP10 (DS4) JP11 (DS5) JP12 (DS6) JP13 (DS7)	IN OUT OUT OUT OUT OUT OUT	Drive Address Selection If No Jumper, the Drive is Off-Line
JP14	OUT	Write Protect Disabled
JP15	OUT	Not Used
JP30	IN	Disable Programmable Sector Size (Hard Sector Only)
JP31	OUT	Hard Sector
JP32 JP33 JP34 JP35 JP36	IN IN IN IN OUT	Factory Setting for 15 Data Heads
JP37	IN	24 Byte Sync Field for SI57. Not Used for SI56
JP38-39	---	Not Used
JP40 (ABC)	B-C	Selects 27256 EPROM
JP41-42	---	Not Used

Table A-2. SI56 Sector Jumper Settings

JUMPER	SETTING	SECTOR COUNT
16	OUT	33 Sectors
17	IN	
18	OUT	
19	IN	
20	IN	
21	IN	
22	IN	
23	OUT	
24	OUT	
25	IN	
26-29	OUT	

A.2 SI57 Disk Drive

The SI57 disk drive is an ESDI interface disk drive that mounts within the 5.25-inch Quick Release Chassis. The disk drive address jumper value is 0, and the Quick Release front panel selects the address reported to the DI board. Dual channel access is through the ESDI-SMD interface board with the channel controls on the Quick Release front panel.

The SI57 presently has two manufacturer's levels; as of January 1989, the SI57 incorporates a new board layout with a new firmware level. The new SI57 is functionally identical to the previous unit. Recognize the new SI57 as Fab #8, Top Level Assembly (TLA) #1098078-3 for the standard tested unit, and TLA #1098060-3 for the quad tested unit. The new board is TLA #1015468 with firmware M.01.

The old SI57 (Pre-Fab #8) has the same mother board layout as the SI56. The old SI57 uses the same settings as the SI56 except for the sector values. Use the general jumper settings shown in Table A-1. The settings for the SI57 sector jumpers are listed in Table A-3.

The new SI57 (Fab #8) uses the same sector jumper arrangement as shown in Table A-3 above. The general jumpers settings for the new SI57 are different. Use Table A-4 for the SI57 - Fab #8.

Table A-3. SI57 Sector Jumper Settings

JUMPER	SETTING	SECTOR COUNT
16	OUT	49 Sectors
17	OUT	
18	OUT	
19	OUT	
20	OUT	
21	OUT	
22	OUT	
23	IN	
24	OUT	
25	IN	
26-29	OUT	

Table A-4. SI57 (New - Fab #8) General Jumper Settings

JUMPER	SETTING	FUNCTION
JP1	B-C	Reserved
JP2	IN	(Test)
JP3	IN	(Test)
JP4	IN	2, 7 Encoding
JP5	IN	15 Mbytes/second Transfer Rate
JP6	OUT IN	Spin-Up Option Enabled (Quick Release Mounting) Spin-Up at Power-On
DS1 DS2 DS3 DS4 DS5 DS6 DS7	IN OUT OUT OUT OUT OUT OUT	Drive Address Selection If No Jumper, the Drive is Off-Line
JP7 JP8	B-C OUT	Read Gate Delay = 0
JP9	A-B	Index Width = 3 µsec
JP10	OUT	Reserved
JP14	OUT	Write Protect Disabled
JP15	OUT	Not Used
JP16 - 29	---	Sector Size
JP30	OUT	Disable Programmable Sector Size (Hard Sector Only)
JP31	OUT	Hard Sector Mode
JP32 JP33 JP34 JP35	IN IN IN IN	Factory Setting for 15 Data Heads
JP36	OUT	Reserved
JP37	IN	24 Byte Sync Field for SI57
JP38 - 39	OUT	Not Used
JP40	OUT	Test Jumper
JP41	OUT	Test Pins
JP42	A-B	Reserved
JP43	IN	Enables Onboard ROM

A.3 9733 Disk Drive

The 9733 disk drive mounts in either an 8-inch Quick Release Chassis or an 8-inch Dual Tray. The 9733 disk drive address, sector, and option switches are located on the disk drive's interface board. Normal settings are shown in Tables A-5 and A-6.

Table A-5. 9733 Switch Settings

SWITCH 1	SETTING		FUNCTION
	UNIT 0	UNIT 1	
1	OFF	ON	Drive Address
2	OFF	OFF	
3	OFF	OFF	
4	OFF		Device Type
5	ON		Device Type
6	ON		Device Type
7	ON		Device Type
8	OFF		SMD Tag 4/5 Disabled
9	OFF		Write Enabled
10	OFF		Horizontal Mount

* Drive unit values 2 — 7 are invalid for CLUSTOR.

Table A-6. 9733 Sector Switch Settings

	SWITCH 2	SWITCH 3	SECTOR COUNT
1	ON	OFF	67 Sectors
2	OFF	ON	
3	OFF	OFF	
4	OFF	OFF	
5	ON	OFF	
6	ON	OFF	
7	OFF	OFF	

A.4 SI83 Disk Drive

The SI83 is an 8-inch disk drive. Like the 9733, the SI83 mounts in an 8-inch Dual Tray or an 8-inch Quick Release chassis, and has an add-on dual-channel interface board. Normal settings for switches SW1 and SW2 are shown in Table A-7. Settings for switches SW2 and SW3 are shown in Table A-8. Switch SW5 is normally set off.

A.5 SI85 Disk Drive

The SI85 is an 8-inch disk drive and mounts in either the 8-inch dual tray or Quick Release Chassis. The SI85 uses the same add-on, dual-channel interface board as the 9733 and SI83. SI85 switch setting information is the same as the SI83. To set the SI85, use Tables A-7 and A-8.

Table A-7. SI83 and SI85 Switch 1 and 2 Settings

SWITCH 1	SETTING		FUNCTION
	UNIT 0	UNIT 1	
1 2 3	OFF OFF OFF	ON OFF OFF	Drive Address
4	OFF		SMD Tag 4/5 Disabled
5	OFF		Write Enabled
6	OFF		Not Used
7	OFF		Hard Sector Enabled
8	OFF		Not Used
SWITCH 2			
1	OFF		Calibration Seek Disabled
2 3	OFF OFF		Horizontal Mount
4	OFF		Reserved

* Drive unit values 2 — 7 are invalid for CLUSTOR.

Table A-8. SI83 and SI85 Sector Switch Settings

	SWITCH 3	SWITCH 4	SECTOR COUNT
1	ON	OFF	67 Sectors
2	OFF	ON	
3	OFF	OFF	
4	OFF	OFF	
5	ON	OFF	
6	ON	OFF	
7	OFF	OFF	
8	OFF	OFF	Not Used

A.6 9751 Disk Drive

The 9751 is a 10.5-inch disk drive that is cabinet mounted only. The basic interface board holds the unit address switch. Switch settings are shown in Table A-9.

Drive sector and I/O option jumpers are on the drive logic board. Normal sector settings are shown in Table A-10, and I/O modification settings in Table A-11.

Table A-9. 9751 Address Switch Settings

ADDRESS SWITCH	1	2	3	4
UNIT 0	OFF	OFF	OFF	OFF
UNIT 1	ON	OFF	OFF	OFF

* Drive unit values 2 — 7 are invalid for CLUSTOR

Table A-10. 9751 Logic Board Sector Count Settings

SECTOR COUNT SETTINGS: 48 SECTORS				
GRID LOCATION (Jumper Together)	BF7	BE7	BD7	BC7
	3 — 4	3 — 4	3 — 4	2 — 3
	6 — 7	5 — 6	6 — 7	6 — 7
	10 — 11	10 — 11	9 — 10	10 —11
	13 — 14*	13 — 14	13 — 14	12 — 13

* Spare

Table A-11. 9751 Logic Board I/O Modification Settings

MODIFICATION SETTINGS		
GRID LOCATION (Jumper Together)	AE7	
	3 — 4	Disable TAG4/5
	6 — 7	Seek End After Offset
	10 — 11	Unit Not Ready During Fault

A.7 9761 Disk Drive

The 9761 is a 10.5-inch disk drive that is cabinet mounted only. Like the 9751, it requires an add-on interface board for dual-channel operation. The drive address, sector and dual-channel controls are accessible behind a small access door in the front cover. Proper settings are shown in Table A-12.

Table A-12. 9761 Sector Count and Unit Address Settings

SECTOR COUNT SETTINGS: 67 SECTORS								
SWITCH	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
B	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
A	OFF	ON	ON	OFF	OFF	OFF	ON	ON

ADDRESS SWITCH	1	2	3	4
UNIT 0	OFF	OFF	OFF	OFF
UNIT 1	OFF	OFF	OFF	ON

* Drive unit values 2 - 7 are invalid for CLUSTOR

A.8 SI93 Disk Drive

The SI93 mounts in a fixed tray that holds two disk drives. The SI93 Disk Drive parameters are set by switches accessible through the drive's front cover. The switches are on the left of the drive's display panel and recessed behind a metal cover. The drive must be configured for 66 sectors per track. The SI93 dual channel requires an additional interface board in the disk drive. Switch settings are listed in Table A-13.

Table A-13. SI93 Switch Settings

SWITCH 2	SETTING	FUNCTION
8	0	Unit Address MSB
7	0	Unit Address
6	0	Unit Address
5	x	Unit Address LSB: 0 = Unit 0, 1 = Unit 1
4	1	Enable 4 Bit Address Mode
3	0	Spindle Start Mode (Local)
2	0	Enable Offset Seek
1	1	Diagnostic Mode 1
SWITCH 3		
8	0	Spindle Delay MSB
7	0	Spindle Delay
6	x	Spindle Delay LSB: 0 = 0 Delay, 1 = 15 Second Delay
5	0	Address Mark Inhibit
4	0	Device Mode Select Standard
3	0	Device Type Select Basic
2	0	Inhibit Tag 4/5
1	1	Diagnostic Mode 2
SWITCH 4		
10	1	
9	0	
8	1	
7	1	Sector Count: 66
6	0	
5	0	
4	0	
3	0	
2	1	
1	0	

* OFF = 1, ON = 0

A.9 SI95 Disk Drive

The SI95 Drive Chassis has slots that allow the field engineer to have access to all switches located on both physical drives, as shown in Figure A-1. Switch settings for the DI board are listed in Table A-14. Switch setting for the SI-Sync board are listed in Table A-15.

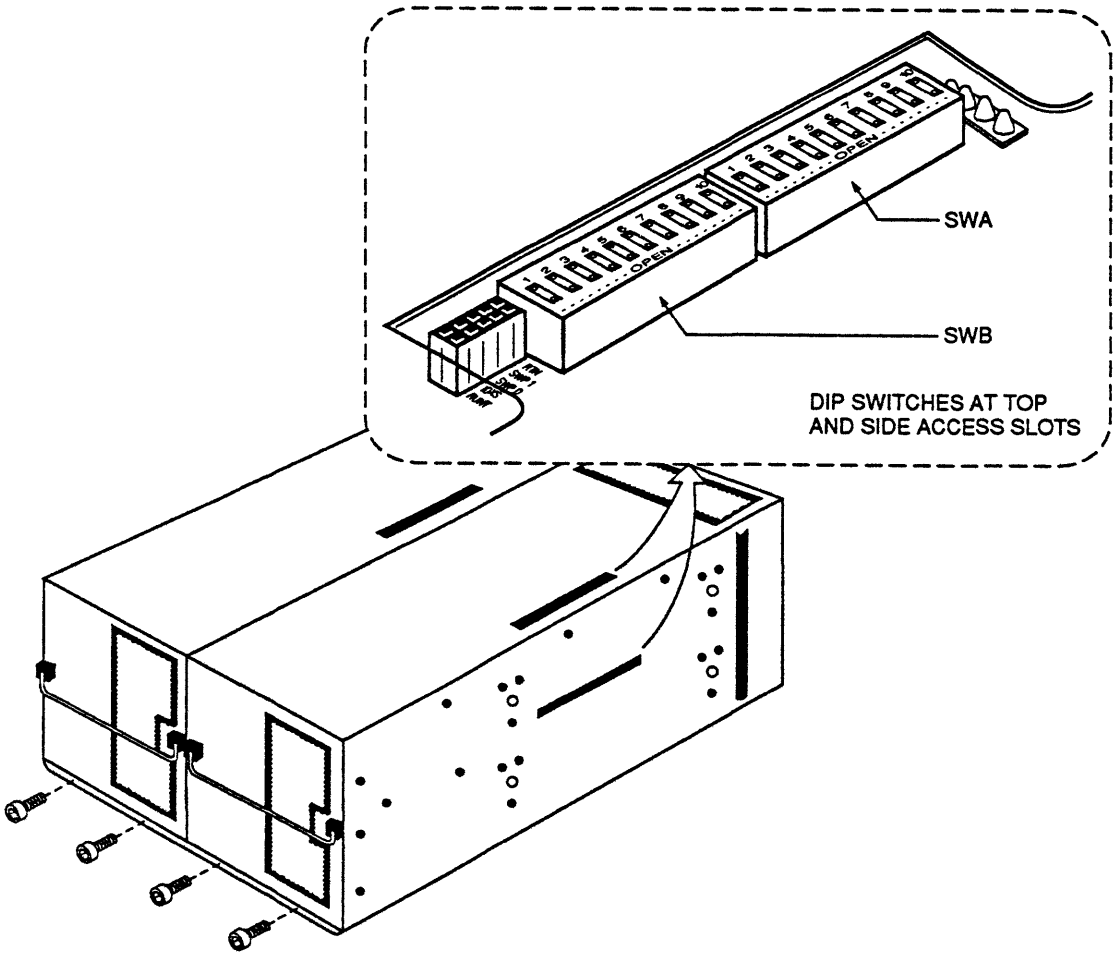


Figure A-1. SI95 Switch Locations for Top I/O Board

Table A-14. SI95 Switch and Jumper Settings (Type 3 Control Board)

SWITCH	POSITION	FUNCTION
SWA-10	Closed	2^{13} Sector Switches 73 sec, 628 bytes/sec
SWA-9	Closed	2^{12}
SWA-8	Closed	2^{11}
SWA-7	Closed	2^{10}
SWA-6	Open	2^{9}
SWA-5	Closed	2^{8}
SWA-4	Closed	2^{7}
SWA-3	Open	2^{6}
SWA-2	Open	2^{5}
SWA-1	Open	2^{4}
SWB-10	Closed	2^{3}
SWB-9	Closed	2^{2}
SWB-8	Open	2^{1}
SWB-7	Open	2^{0}
SWB-6	Closed	Write Protect Disabled
SWB-5	Closed	Clock Frequency Enabled
SWB-4	Closed	*Top I/O Board Unit Number = 0
SWB-3	Closed	
SWB-2	Closed	
SWB-1	Closed	

EXAMPLE ONLY

Refer to the appropriate User Guide for required sector settings.

* The top I/O board must be set to 0. Unit selection is made from the SI-SYNC board on the back of the drive.

JUMPER	POSITION	FUNCTION
RTN	IN	Enable Return to Original Position After Sweep
SWP1	OUT	Disable Sweep on Seeks
SWPD	IN	Enable Sweep Cycle
IDX S	OUT	Factory Set
RUNT	IN	Runt Sectors are Suppressed

Table A-15. SI-Sync Board Switch and Jumper Settings

TOP

JUMPER	POSITION
W1	IN
W2	OUT

UNIT NUMBER (SW1)

SW1-1	SW1-2	SW1-3	SW1-4	UNIT No.
Closed	Closed	Closed	Closed	= 0
Open	Closed	Closed	Closed	= 1

BOTTOM

JUMPER	POSITION	FUNCTION
W1	IN	
W2	* See Note	
W3	OUT	
W4	IN	Select Delayed for A Index
W5	OUT	Select Delayed for A Index
W6	OUT	Select Delayed for B Index
W7	IN	Select Delayed for B Index
SW1-1	Open	CH1 Index and Select Enabled
SW1-2	Open	CH1 Index and Select Enabled
SW1-3	Open	CH2 Index and Select Enabled
SW1-4	Open	CH2 Index and Select Enabled
SW1-5	Open	Normal Ready Status
SW1-6	Open	Extended Cylinder Address via TAG2
SW1-7	Open	SMD-E Mode Enabled
SW1-8	Open	Extended Cylinder Address Enabled
SW1-9	Closed	Release Timer Mode
SW1-10	Closed	Local Power ON

* W2 is IN for style one (flying lead) drives.
W2 is OUT for style two.

A.10SI92 Disk Drive

The controller disk geometry is set up for 1,635 cylinders, 15 heads, and 73 sectors. The SI92 disk is a 2.74 Mbyte transfer rate drive, spinning at 3600 RPM. Switch settings for the DI board are listed in Table A-16 and are shown in Figure A-2. Switch settings for the sync board at the back of the drive are listed in Table A-17 and shown in Figure A-3.

Table A-16. SI92 Switch and Jumper Settings (Type 3 Control Board)

SWITCH	POSITION	FUNCTION
SWA-10	Closed	2^{13} Sector Switches 73 sec, 628 bytes/sec
SWA-9	Closed	2^{12}
SWA-8	Closed	2^{11}
SWA-7	Closed	2^{10}
SWA-6	Open	2^{9}
SWA-5	Closed	2^{8}
SWA-4	Closed	2^{7}
SWA-3	Open	2^{6}
SWA-2	Open	2^{5}
SWA-1	Open	2^{4}
SWB-10	Closed	2^{3}
SWB-9	Closed	2^{2}
SWB-8	Open	2^{1}
SWB-7	Open	2^{0}
SWB-6	Closed	Write Protect Disabled
SWB-5	Closed	Clock Frequency Enabled
SWB-4	Closed	*Top I/O Board Unit Number = 0
SWB-3	Closed	
SWB-2	Closed	
SWB-1	Closed	

* The top I/O board must be set to 0. Unit selection is made from the SI-SYNC board on the back of the drive.

Table A-16. SI92 Switch and Jumper Settings (Continued)

JUMPER	POSITION	FUNCTION
RTN	IN	Enable Return to Original Position After Sweep
SWP1	OUT	Disable Sweep on Seeks
SWPD	IN	Enable Sweep Cycle
IDX S	OUT	Factory Set
RUNT	IN	Runt Sectors are Suppressed

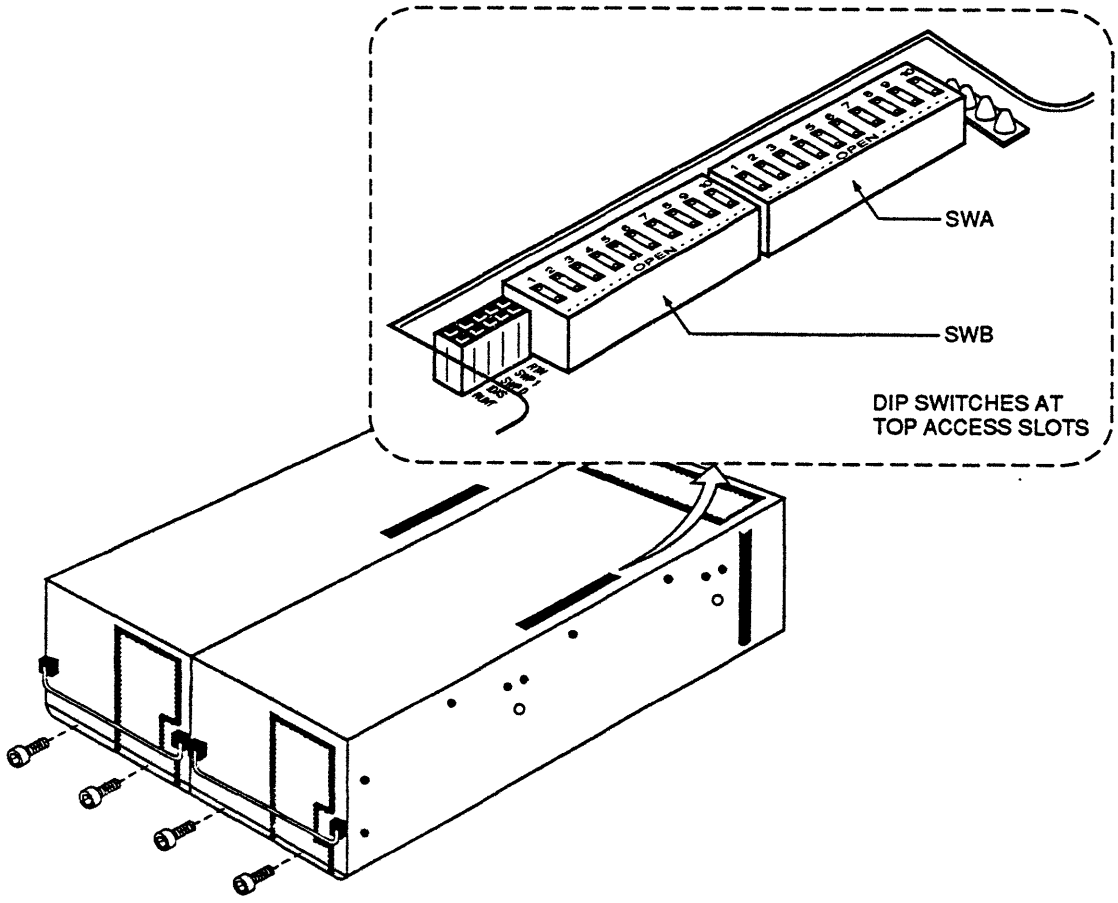


Figure A-2. SI92 Switch Locations for Top I/O Board

Table A-17. Sync Board Switch and Jumper Settings

SWITCH A213

JUMPER	POSITION	FUNCTION
SW1-1	Open	CH1 Index and Select Enabled
SW1-2	Open	CH1 Index and Select Enabled
SW1-3	Open	CH2 Index and Select Enabled
SW1-4	Open	CH2 Index and Select Enabled
SW1-5	Open	Normal Ready Status
SW1-6	Open	Extended Cylinder Address via TAG2
SW1-7	Open	SMD-E Mode Enabled
SW1-8	Open	Extended Cylinder Address Enabled
SW1-9	Closed	Release Timer Mode
SW1-10	Closed	Local Power ON

SWITCH A224

JUMPER	POSITION*	FUNCTION
SW1-1	Closed	Device ID
SW1-2	Closed	
SW1-3	Closed	
SW1-4	Closed	
SW1-5	Closed	
SW1-6	Closed	
SW1-7	Closed	
SW1-8	Closed	

* Closed = 1; Open = 0

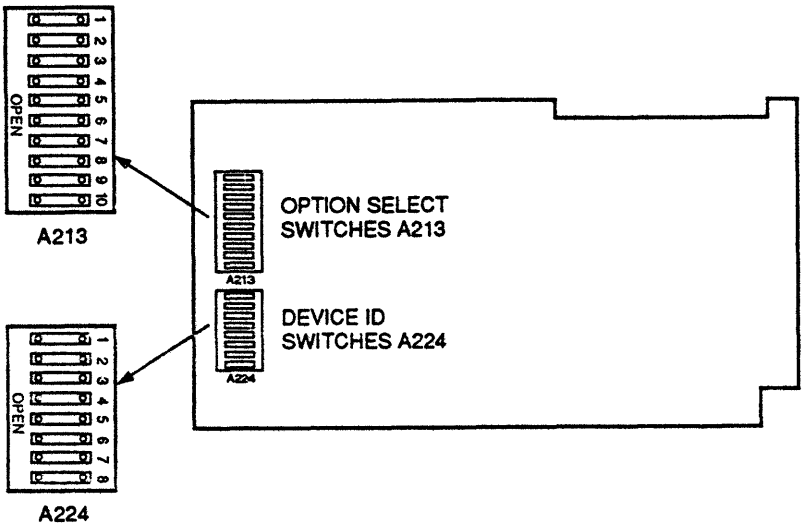


Figure A-3. SI92 Switch Locations for Sync Board

A.11 SI506 Disk Drive

Each 5.25-inch disk drive has an embedded Printed Circuit Assembly (PCA) board. The PCA board contains seven jumper blocks, four RS-232 connector blocks, and four LEDs. The drive PCA board is shown in Figure A-4. The jumper block settings are listed in Table A-18.

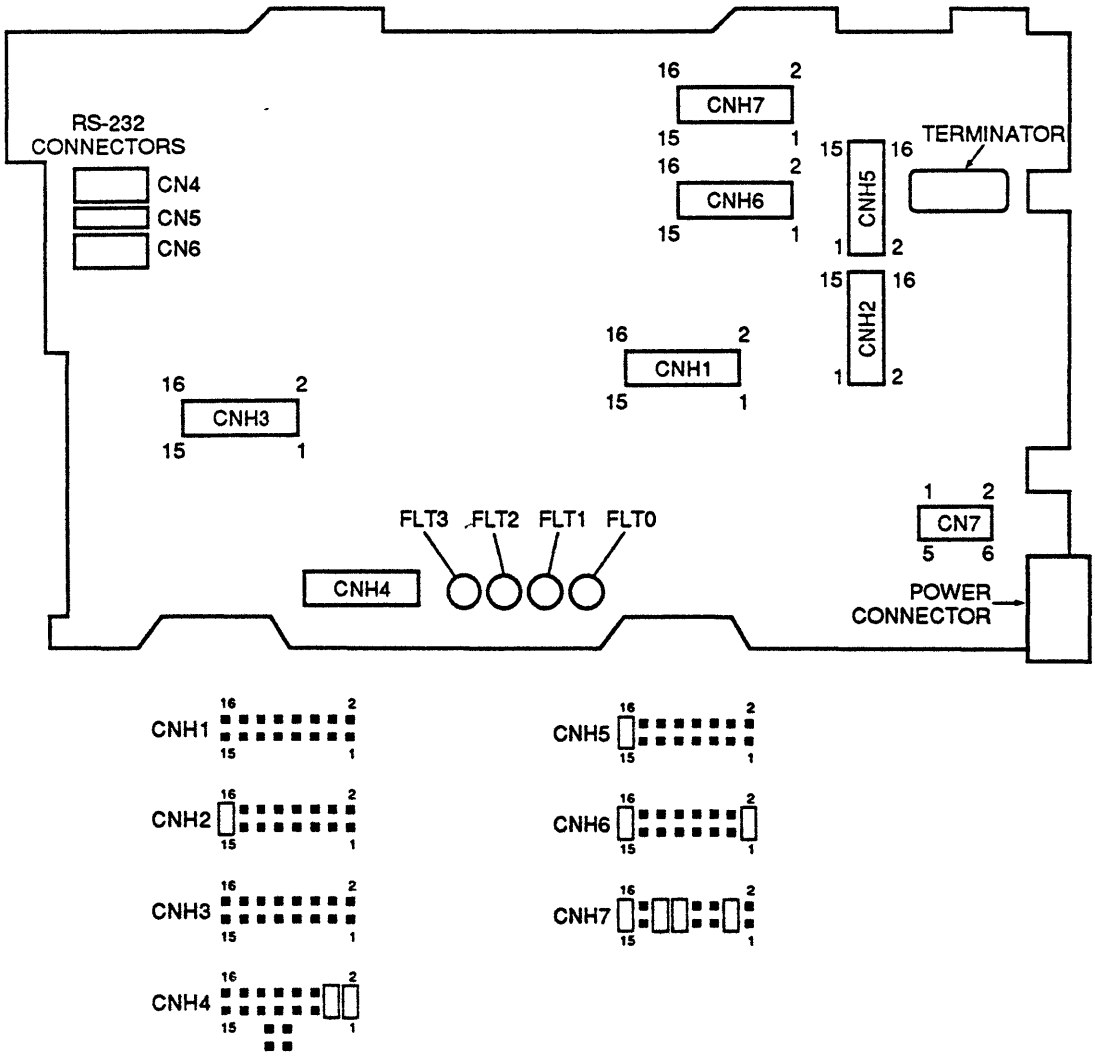


Figure A-4. SI506 Disk Drive PCA

Table A-18. SI506 Disk Drive Jumper Settings

JUMPER	SETTING	PIN
CNH1	OUT	ALL
CNH2	IN	15 — 16
CNH3	OUT	ALL
CNH4	IN	1 — 2, 3 — 4
CNH5	IN	15 — 16
CNH6	IN	1 — 2, 15 — 16
CNH7	IN	3 — 4, 9 — 10, 11 — 12, 15 — 16

A.12 SI817 Disk Drive

The SI817 Disk Drive is an industry-standard, 8-inch drive. This unit is a high-capacity, high-performance, random-access storage device using nonremovable disk platters as storage media.

Each 8-inch disk drive has an embedded printed circuit assembly (PCA) board on the top, which functions as an interface board. The top embedded interface board controls read, write, seek, and other drive control functions.

The embedded board contains two banks of switches, four jumpers, four LEDs, and three unused connectors, as shown in Figure A-5. A top plate covers the top embedded board and is attached with six allen bolts.

The switch access hole is covered by a removable, plastic window in the top plate. The default settings on the switches and jumpers are set as shown in Table A-19 and Table A-20.

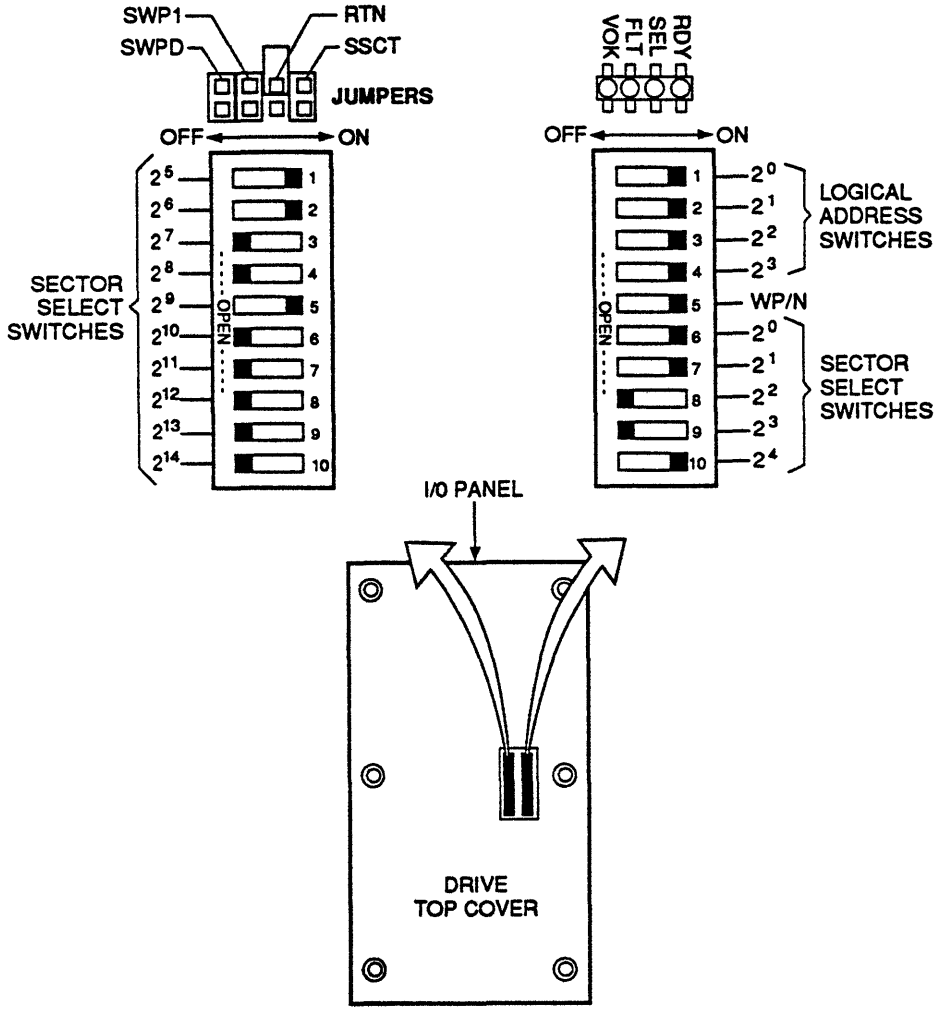


Figure A-5. SI817 Disk Drive Embedded Interface Board

Table A-19. SI817 Disk Drive Interface Board Jumper Settings

JUMPER	POSITION	FUNCTION
SWP1	IN	Disables Sweep Cycle Option on Sweeps
SWPD	IN	Disables Sweep Cycle Operation
RTN	OUT	Disables Option Returning Heads to Original Positions After Sweep Segment
SCCT	IN	Suppresses Runt Sector Pulses

Table A-20. SI817 Disk Drive Interface Board Switch Positions

SWITCH	OPEN	CLOSED
2^5		X
2^6		X
2^7	X	
2^8	X	
2^9		X
2^{10}	X	
2^{11}	X	
2^{12}	X	
2^{13}	X	
2^{14}	X	
2^0		X
2^1		X
2^2		X
2^3		X
WP/N*		X
2^0		X
2^1		X
2^2	X	
2^3	X	
2^4		X

* WP = Open: Selects write-protect mode
N = Closed: Selects normal mode

The drive rear panel controls drive selection, data formatting, and input/output (I/O) operations. The rear panel has one bank of switches that set the drive configuration and a second bank of switches, labelled "Device ID." Switch settings A213 and A224 are described in Table A-21 and shown in Figure A-6.

The drive rear panel has four 60-pin control connectors (three unused), two 26-pin data connectors (one unused), one 15-pin DC connector with 14 pins, and one unused 14-pin connector. The rear panel also has a DC ground screw.

A terminator attaches to connector 1J4 to a spade connection on the ground screw T.

Table A-21. SI817 Disk Drive Rear Panel Switches (A213)

OPEN SWITCH FUNCTIONS		CLOSED SWITCH FUNCTIONS	
1A	Channel 1, A Selected (default)	1D	Channel 1 Disabled
1B	Channel 1, B Selected (default)	1D	Channel 1 Disabled
2A	Channel 2, A Selected (default)	2D	Channel 2 Disabled
2B	Channel 2, B Selected (default)	2D	Channel 2 Disabled
RDY	Ready (default)	POK	Power OK
T2	Tag 2 (default)	T1	Tag 1
E	SMD-E	O	SMD-O (default)
XA	Extended Cylinder (default)	N	Normal Cylinder
AR	Absolute Reserve (default)	RT	Reserve Timer
R	Remote	L	Local (default)

SWITCH A224

JUMPER	POSITION*	FUNCTION
SW1-1	Open	Device ID
SW1-2	Open	
SW1-3	Open	
SW1-4	Open	
SW1-5	Open	
SW1-6	Open	
SW1-7	Open	
SW1-8	Open	

* Closed = 1; Open = 0

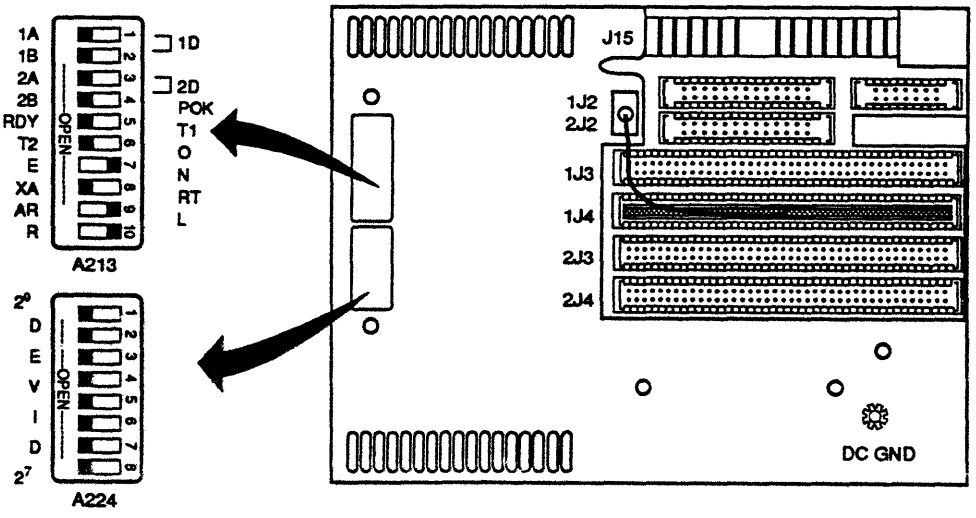
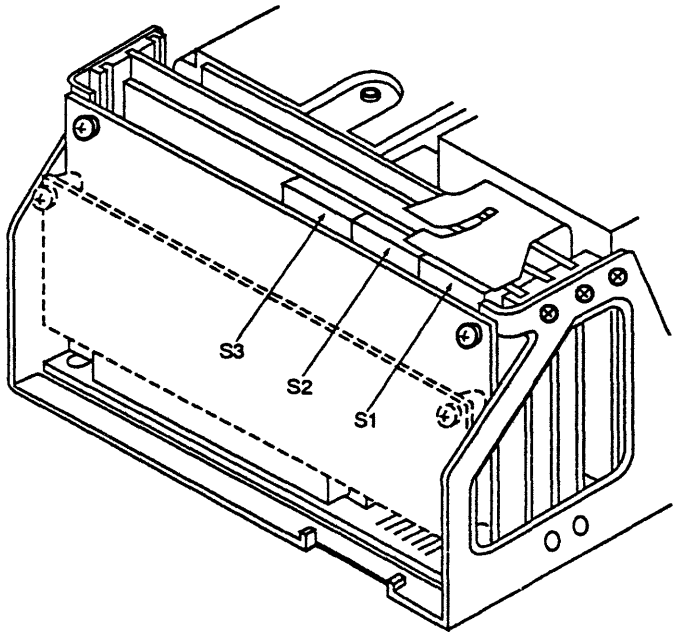


Figure A-6. SI817 Disk Drive Rear Panel

A.13 SI510 Disk Drive

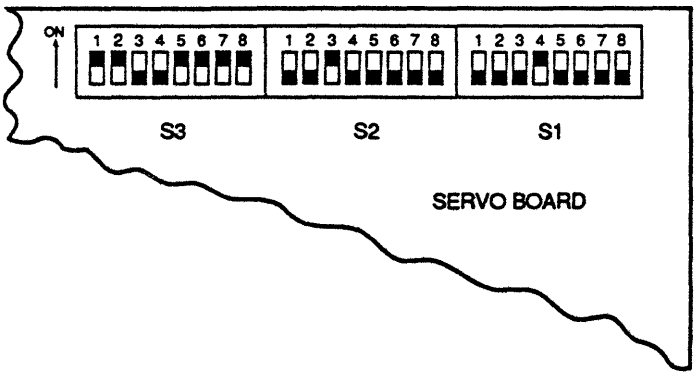


DIP SWITCH S3

1-SECTOR SWITCH	2^0	ON
2-SECTOR SWITCH	2^1	ON
3-SECTOR SWITCH	2^2	OFF
4-SECTOR SWITCH	2^3	OFF
5-SECTOR SWITCH	2^4	ON
6-SECTOR SWITCH	2^5	ON
7-SECTOR SWITCH	2^6	ON
8-SECTOR SWITCH	2^7	ON

DIP SWITCH S2

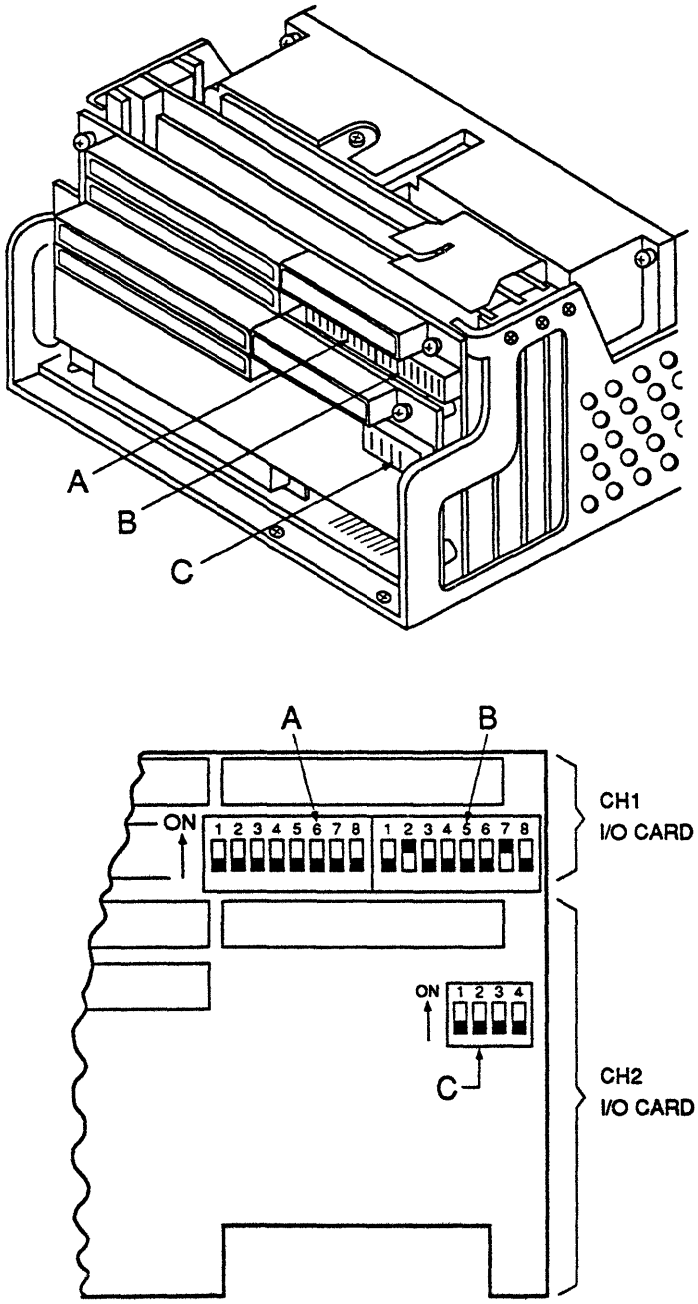
1-SECTOR SWITCH	2^8	OFF
2-SECTOR SWITCH	2^9	OFF
3-SECTOR SWITCH	2^{10}	ON
4-SECTOR SWITCH	2^{11}	OFF
5-SECTOR SWITCH	2^{12}	OFF
6-SECTOR SWITCH	2^{13}	OFF
7-SECTOR SWITCH	2^{14}	OFF
8-RUNT SECTOR		OFF



DIP SWITCH S1

1-SWEEP CYCLE ENABLE		OFF
2-ENABLE SWEEP ONLY ON SEEKS		OFF
3-MANUFACTURING TEST		OFF
4-WRITE ENABLE		ON
5-UNIT SELECT	2^0	OFF
6-UNIT SELECT	2^1	OFF
7-UNIT SELECT	2^2	OFF
8-UNIT SELECT	2^3	OFF

Figure A-7. SI510 DIP Switch Settings



A

8-POSITION DIP SWITCH

1-DEVICE ID 2^0	OFF
2-DEVICE ID 2^1	OFF
3-DEVICE ID 2^2	OFF
4-DEVICE ID 2^3	OFF
5-DEVICE ID 2^4	OFF
6-DEVICE ID 2^5	OFF
7-DEVICE ID 2^6	OFF
8-DEVICE ID 2^7	OFF

SWITCH ON MAKES THAT DEVICE ID BIT ACTIVE

B

8-POSITION DIP SWITCH (OFF SETTING/ON SETTING)

1-NOT USED	OFF
2-REMOTE/LOCAL	ON
3-1A/1D	OFF
4-1B/1D	OFF
5-T2/T1	OFF
6-XA/N	OFF
7-AR/RT	ON
8-E/O	OFF

C

4-POSITION DIP SWITCH (OFF SETTING/ON SETTING)

1-2B/2D	OFF
2-2A/2D	OFF
3-NOT USED	OFF
4-NOT USED	OFF

Figure A-8. SI510 I/O Switch Settings

Table A-22. SI510 I/O Board Switch Settings

SWITCH	SETTING*	DESCRIPTION
Device ID $2^0 - 2^7$ (DIP SW A:1 — 8)		Set according to customer requirements. Setting a switch ON makes that Device ID bit active.
Remote/ Local Switch (DIP SW B:2)	Remote (OFF) Local (ON)	Power-on sequence dependent on controller Power-on sequence independent of controller
1A/1D, 1B/1D (DIP SW B:3), (DIP SW B:4)		Enable/Disable CH 1 and select an option for sending Index & Sector to CH 1 controller. The four combinations of switch settings are as follows:
1A/1D 1B/1D	1A (OFF) 1D (ON)	This pair of switch settings enables CH 1 and sends I & S on A cable only.
1A/1D 1B/1D	1D (ON) 1B (OFF)	This pair of switch settings enables CH 1 and sends I & S on B cable only.
1A/1D 1B/1D	1A (OFF) 1B (OFF)	This pair of switch settings enables CH 1 and sends I & S on A and B cables.
1A/1D 1B/1D	1D (ON) 1D (ON)	This pair of switch settings disables CH 1.
T2/T1 (DIP SW B:5)		Selects type of extended cylinder addressing, provided that XA/N switch is set in XA position.
	T2 (OFF)	Enables Extended Cylinder Address Bits 2^{10} and 2^{11}, via Tag 2 (Head Select). Can be selected in either SMD-0 or SMD-E mode. Allows all cylinders to be accessed.
	T1 (ON)	Enables Extended Cylinder Address Bit 2^{10}, via Tag 1 (Cylinder Select). Can be selected in either SMD-0 or SMD-E mode, but Tags 4 and 6 are unusable with this selection. Allows only 2048 cylinders to be accessed.

* On = Closed; Off = Open

Table A-22. SI510 I/O Board Switch Settings (Continued)

SWITCH	SETTING*	DESCRIPTION
XA/N	XA (OFF)	Extended Cylinder Address; method set by T2/T1 switch • Allows cylinders 0 — 2109 if T2/T1 switch is set to T2 position • Allows cylinders 0 — 2047 if T2/T1 switch is set to T1 position
	N (ON)	Normal Cylinder Address (cylinders 0 — 1023); T2/T1 switch has no effect
AR/RT (DIP SW B:7)	AR (OFF)	Absolute Reserve (Dual Channel)
	RT (ON)	Reserve Timer (Dual Channel)
E/O (DIP SW B:8)	E (OFF)	SMD-E mode (Tags 1 — 6)
	0 (ON)	SMD-O mode (Tags 1 — 3)
2A/2D, 2B/2D (DIP SW C:2), (DIP SW C:1)		Enable/Disable CH 2 and select an option for sending Index & Sector to CH 2 controller (see description of CH 1 switches)

* On = Closed; Off = Open

APPENDIX B
SBI CPA INSTALLATION

This section describes SBI CPA installation procedures. Some of the installation procedures for DEC 8600 and 8650 CPUs differ from those for the 11/780. Preliminary inspection and board configuration procedures for the three CPU models are the same. All procedures are described below.

NOTE

The SBI CPA must be the version that has two interrupt lines. The MPU PCB must be a 9400-6224 or higher, and the Paddle PCB must be a 9400-6215 or higher.

The SBI CPA card cage assembly fits into a MASSBUS Adapter (MBA) slot in any VAX-11/780 Series system cabinet or SBI expansion cabinet. The system cabinet has two MBA slots. An expansion cabinet must be added if the system cabinet is full. There must also be a DEC MBA power supply or a compatible System Industries power supply with available unused capacity. The SI expansion cabinet has space for three power supplies.

SI or DEC MBA power supplies support up to two MBAs or SI SBI CPAs. If no unused power supply capacity is available, there must be a vacant power supply space in which an additional power supply can be installed. There are two optional SI power supply assemblies (115/120 VAC @ 60Hz or 220/240 VAC @ 50 Hz) available. If the CPA is replacing an existing DEC MBA or SI CPA, no additional power supply is needed.

B.1 SBI CPA Location

Where the CPA is located depends on the number of MBA devices attached to the system and whether or not the system has additional memory. Six configurations, listed below, may be encountered, each requiring a different location (A — F) for the CPA. Though the configurations cited are typical, some variation may occur.

1. No MBAs currently installed in the system.
2. One MBAs currently installed in the system.
3. Two MBAs currently installed in the system.
4. Three MBAs currently installed in the system.

5. Two MBAs and additional memory currently installed in the system.
6. Three MBAs and additional memory currently installed in the system.

For configurations 1 and 2 above (excluding 8600 or 8650), the CPA is installed in the system cabinet. For installations 3 through 6, the CPA is installed in the expansion cabinet. The MBA device locations in the VAX-11/780 cabinet and the additional SBI expansion cabinet are shown in Figure B-1.

NOTE

A case might occur where the SBI CPA is to be placed in a VAX-11/780 that does not have a UNIBUS expansion cabinet. The computer will have, instead, a UNIBUS mounting frame installed in the area normally reserved for MBAs.

Before the CPA can be installed, a DEC upgrade option H9604-BA(BB) has to be added. Once the system is upgraded, the CPA is installed as in configuration 1.

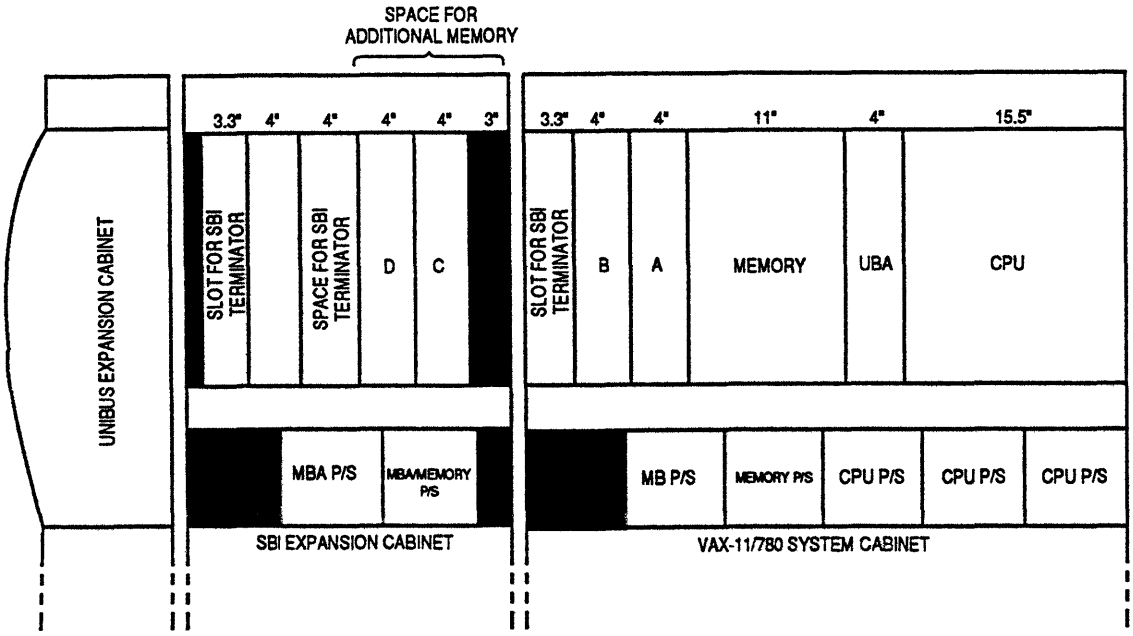


Figure B-1. MBA Device Locations in the VAX-11/780 Cabinets, Rear View

B.2 Preliminary Inspection

Unpack the SBI CPA card cage and backplane assembly, remove the printed circuit boards, and verify the following:

- All components are undamaged, in place and secure.
- Connector pins are not bent or otherwise damaged.
- Cables are not kinked or cut.

Preliminary Checkout

Verify the following:

- The SI Disk Drives and cabinets that are part of the CLUSTOR (M) subsystem have been located within acceptable cable length limits.
- The CPU has been shut down.
- Power is turned off at the power distribution panel of each cabinet in the system.
- All power to the CPU has been turned off at the MAIN POWER panel or at the 3-phase circuit breaker (CB1) located at the rear of the 11/780 system cabinet.

B.3 SBI CPA Configuration

This section details the configuration parameters of the following PCBs:

- SBI Interface Board
- Internal Registers Board
- MPU Interface Board

Transfer and Bus Request Switches

The transfer request and bus request switch pack is located at grid position 9A (Figure B-2) on the SBI interface board (9400-62X1). Transfer request and bus request levels are shown in Table B-1. BR is the same as ISR (interrupt summary request level) for the SBI.

NOTE

Nonstandard TR levels cannot be used with the UNIX or ULTRIX operating system.

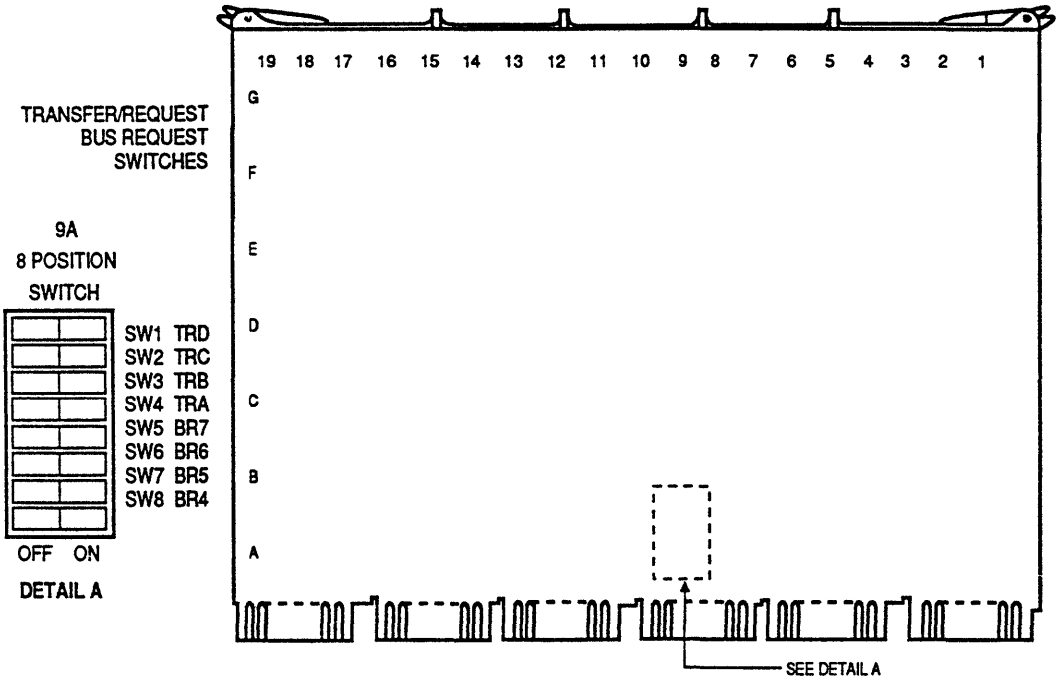


Figure B-2. SBI Interface Board

Table B-1. Transfer Request/Bus Request Switch Settings

TR LEVEL	SW1*	SW2	SW3	SW4†	BR LEVEL	SW5	SW6	SW7	SW8
8	OFF	ON	ON	ON	5	ON	ON	OFF	ON
9	OFF	ON	ON	OFF					
10	OFF	ON	OFF	ON					
11	OFF	ON	OFF	OFF					
12#	OFF	OFF	ON	ON					
13#	OFF	OFF	ON	ON					
14#	OFF	OFF	OFF	ON					
15#	OFF	OFF	OFF	OFF					

* Most Significant Bit

† Least Significant Bit

Nonstandard TR levels 8 — 11. Are standard for MBAs and SI SBI CPAs
If 8 — 11 are occupied, use alternate TR levels 12 — 15
OFF = ON = 1 ON = CLOSED = 0

Internal Registers Transfer Request Switch

This switch must be set to the same TR level as the SBI interface board. Set the transfer request switch located at grid position 17D (Figure B-3) on the internal registers board (9400-62X2). The switch settings are found in Table B-2.

Table B-2. Transfer Request Level Switch Settings

TR LEVEL	SW1†	SW2	SW3	SW4*
8	ON	ON	ON	OFF
9	OFF	ON	ON	OFF
10	ON	OFF	ON	OFF
11	OFF	OFF	ON	OFF
12#	ON	ON	OFF	OFF
13#	OFF	ON	OFF	OFF
14#	ON	OFF	OFF	OFF
15#	OFF	OFF	OFF	OFF

* Most Significant Bit

† Least Significant Bit

# Nonstandard TR levels 8 — 11. Are standard for MBAs and SI SBI CPAs If 8 — 11 are occupied, use alternate TR levels 12 — 15
OFF = ON = 1 ON = CLOSED = 0

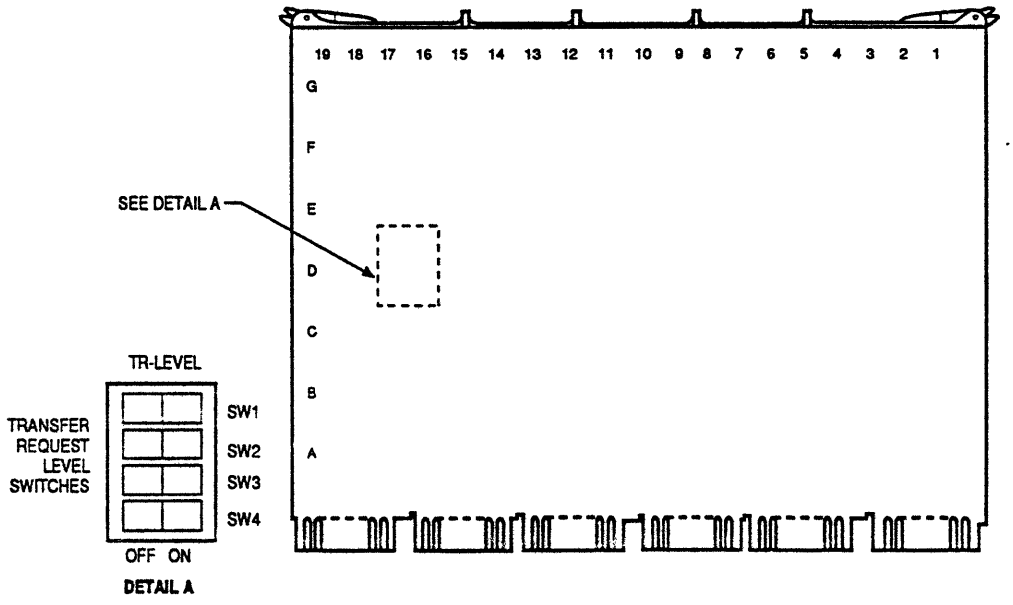


Figure B-3. Internal Registers Board

RM Emulation Jumpers

Check the MPU interface board (9400-6224) for proper installation of the RM0X jumpers. Jumper settings are listed in Table B-3. Jumper locations are shown in Figure B-4.

Table B-3. RM Emulation Jumpers (MPU Interface Board)

OPTION	JUMPER	POSITION
RM0X	W1	2

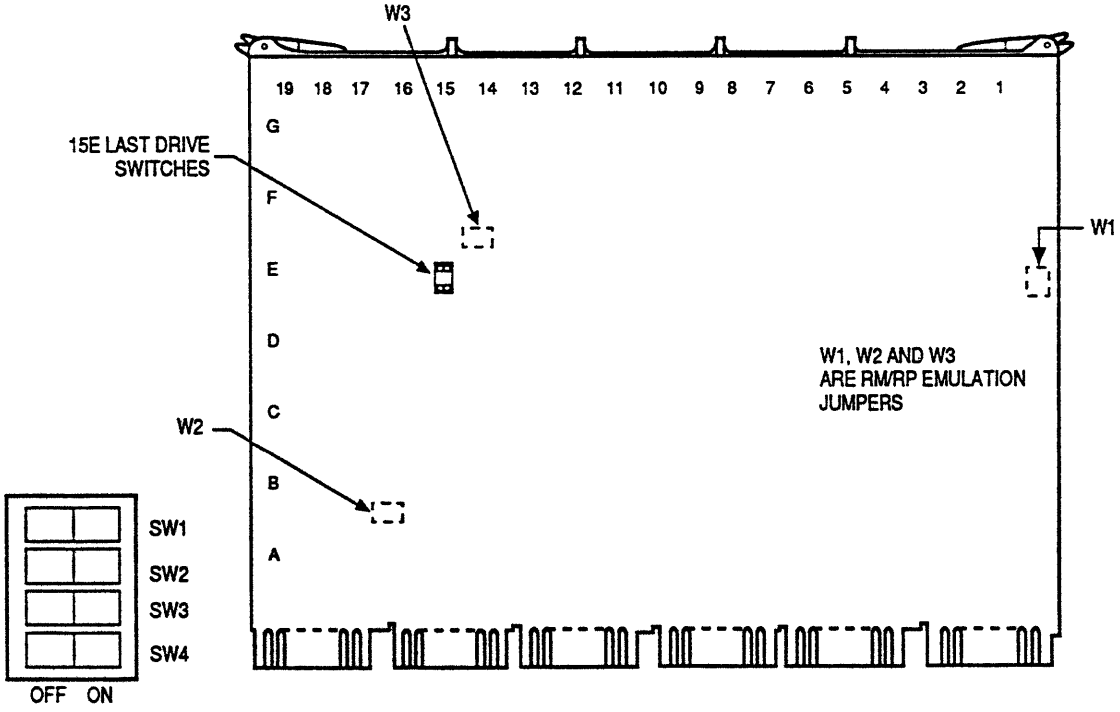


Figure B-4. MPU Interface Board

Last Drive Switches

The last drive is the highest logical unit number in the system. Set the last drive switches, located at grid position 15E (Figure B-4) on the MPU interface board to seven. The settings are listed in Table B-4.

Table B-4. Last Drive Switch Settings

LAST DRIVE NUMBER	SW1†	SW2	SW3	SW4*
0	ON	ON	ON	—
1	OFF	ON	ON	—
2	ON	OFF	ON	—
3	OFF	OFF	ON	—
4	ON	ON	OFF	—
5	OFF	ON	OFF	—
6	ON	OFF	OFF	—
7	OFF	OFF	OFF	—

* Most Significant Bit; Switch 4 not used
† Least Significant Bit

Extended Register Option

The 9400-6224 board has capacity in its register file to enable this extended register option. Jumper W2 should be removed (Table B-5).

Table B-5. Extended Register Option Jumper Setting

OPTION	JUMPER	POSITION
Disable	W2	IN
Enable	W2	OUT

Transfer Request Jumper (SBI Backplane)

This level must correspond to the level set on the SBI interface and internal registers boards. Verify that the wire-wrap jumper on the SBI backplane has been configured for the desired transfer request level. Jumper locations on the backplane are shown in Figures B-5 and B-6. The locations of the jumpers used to specify the transfer request level are listed in Table B-6.

Table B-6. TR Jumper Locations

TR ARBITRATION LEVEL WIRE-WRAP		
TR NUMBER*	**FROM**	**TO**
8	2-FF1	2-FM1
9	2-FF1	2-FN1
10	2-FF1	2-FP1
11	2-FF1	2-FP2
12	2-FF1	2-FS2
13	2-FF1	2-FT2
14	2-FF1	2-FU1
15	2-FF1	2-FU2

* NOTE: 12 — 15 are used if 8 — 11 are occupied.

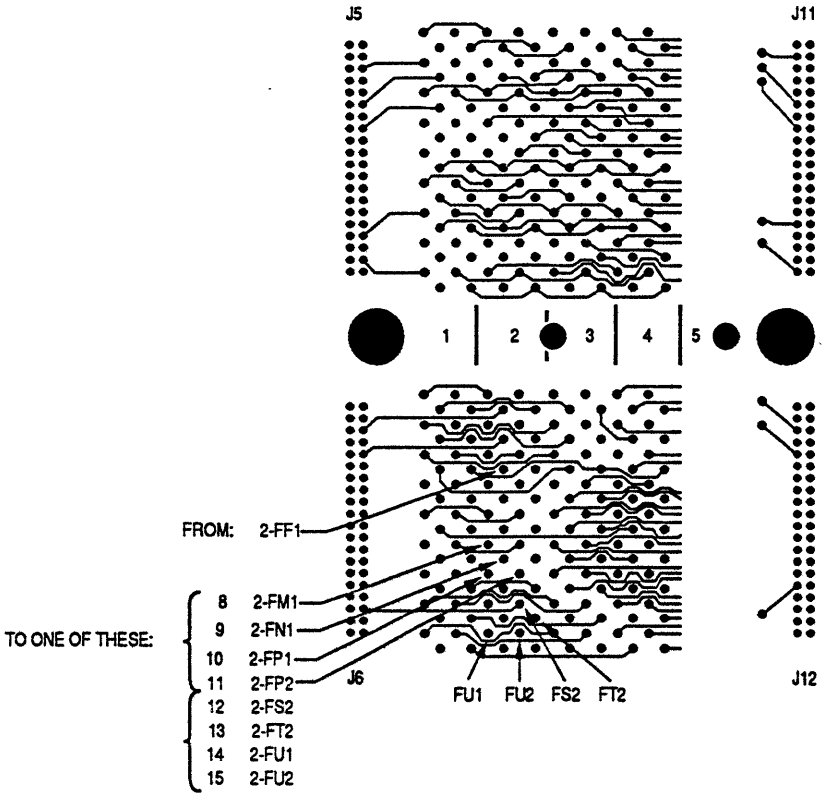


Figure B-5. SBI Backplane (old style)

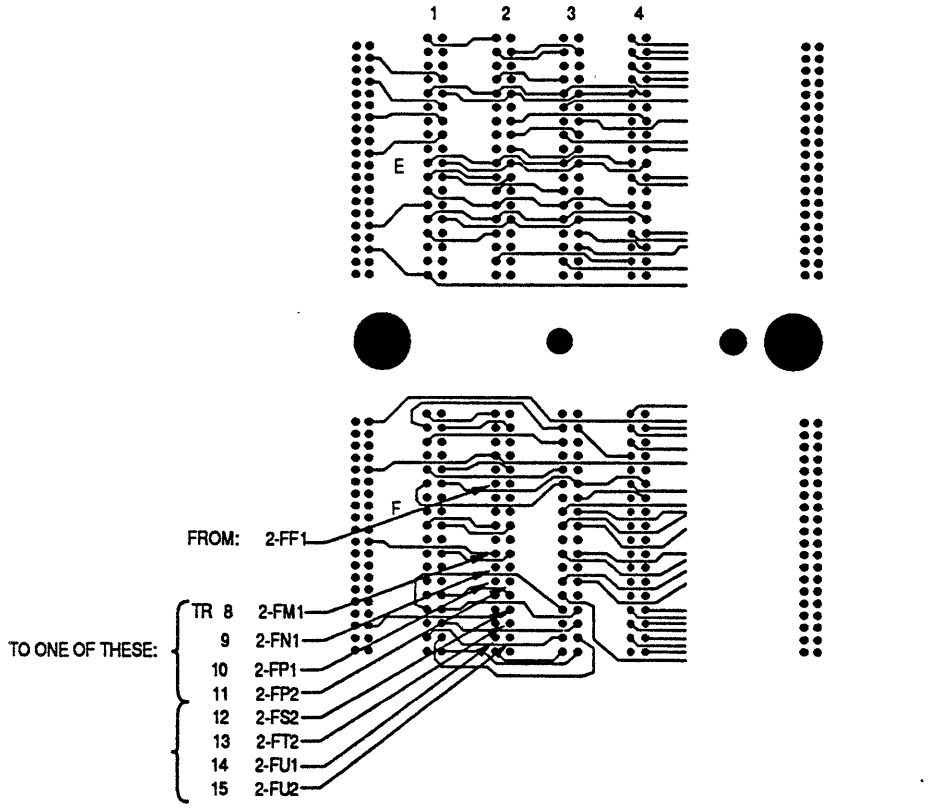


Figure B-6. SBI Backplane (new style)

Reinstall the CPA Boards

Reinstall the CPA boards in the card cage in the following order (from left to right):

1. MPU interface board
2. Data path board
3. Internal registers board
4. SBI interface board

Insert the paddleboard into the hex-high connector at the rear of the card cage; J1 and J2 connectors are on the right side of the board. Refer to "CPA and Power Cabling."

NOTE

If this is an 8600/8650 installation proceed to "Installation in a VAX 8600 or 8650."

B.4 SBI Terminator Installation

The SBI terminator is the last device on the SBI. If a vacant 4-inch (10.2-cm) slot exists between the terminator and another device, leave the terminator where it is and install the CPA in the vacant slot. If there is no vacant slot, move the terminator at least one and, if possible, two slots after the last backplane. The extra slot allows room for an additional MBA if the user wishes to install one later.

1. Remove the six 12-inch (30.5-cm) cables attached to the terminator. Set these cables aside for later use.
2. Disconnect the +5V power line, RD/BK/BLU/BK, from connector J7 on the terminator.
3. Disconnect the AC/DC LO lines, both YEL/VIO/BK. from connectors J8 and J9. J9 is connected only if the terminator board is in the system cabinet.
4. Unfasten the six screws and washers securing the terminator and backing plate assembly to the cabinet chassis and remove the assembly.
5. Remove the simulator panel from the backplane slot chosen as the new terminator location. The panel is secured with six screws and washers.
6. If the terminator's backing plate is the same size as the slot in which it is to be placed, proceed to step 7. If not, remove the terminator board from the 3.3-inch (8.4-cm) backing plate to which it is attached and install it on the 4-inch (10.2-cm) plate that was removed from the new terminator slot, or vice versa, depending on the installation requirements. Make sure that the spacers and plexiglass cover are reassembled as before.
7. Mount the terminator assembly in the 3.3-inch (8.4-cm) or 4-inch (10.2-cm) backplane slot chosen as the new terminator location.
8. Mount the old 3.3-inch (8.2-cm) or 4-inch (10.2-cm) plate in the backplane slot previously occupied by the terminator.

CAUTION

Step 8 is necessary to maintain adequate system airflow.

B.5 Power Supply Installation

Depending on the type of installation, the DEC or SI power supply can be installed in the CPU cabinet or in a DEC or SI expansion cabinet. Steps one and two are the same for either a CPU cabinet or an expansion cabinet.

1. Each available power supply space contains a simulator box, which is secured with a screw and washer at the top of the box (front) and with a snapclip at the bottom (rear) of the box. Remove the simulator box by sliding it out through the front of the cabinet.
2. Insert the Power supply so that the AC receptacles face the front of the system cabinet. Secure the power supply to the front of the cabinet with the single screw at the top of the supply and to the rear of the cabinet with the snap clip.
3. In some CPUs and DEC expansion cabinets the switch and unswitched outlets might be on the same panel of the power distribution box, which is located at the base of the cabinet. Locate a switched outlet and plug in the power supply AC power cord. The other end of the cord is plugged into the front of the power supply.
4. In an SI expansion cabinet the switched outlets are on the power strip at the rear of the power distribution box. The unswitched outlets are on the front panel of the box next to the main AC power switch.

CAUTION

Do not connect a power supply to any unswitched outlet. In FCC-compliant cabinets unswitched outlets by pass the EMI filter and have only a 5-amp breaker.

B.6 SBI CPA Card Cage Installation

1. Remove the simulator panel from the system backplane slot chosen as the SBI CPA location. This panel is secured with six screws and washers.
2. Verify that the transfer request (TR) jumper on the SBI backplane is set to the desired TR level.
3. Insert the SBI CPA card cage and backplane assembly into the VAX cabinet or expansion cabinet from the rear. Mount the assembly using four of the screws and washers removed in step 1, or use those supplied in the installation kit. Use two screws at the top rear of the assembly and two at the bottom front (Figure B-7).

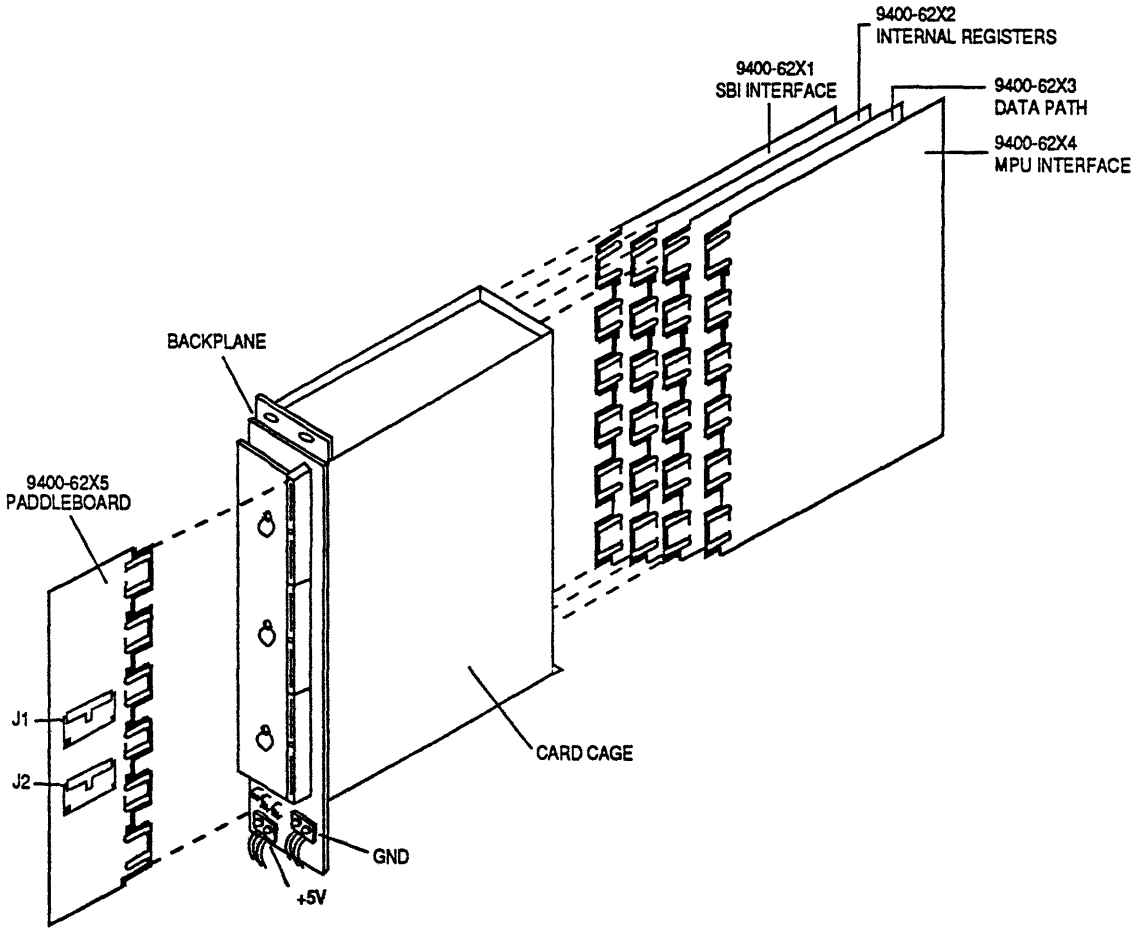


Figure B-7. SBI Card Cage and Backplane Assembly

B.7 CPA and Power Cabling

The procedures for removing the CPA and power cabling are described below. Follow these procedures before proceeding to the next section.

1. Working from the rear of the cabinet, connect six coaxial cables from the right side of the CPA backplane (J7 — J12), to the left side of the backplane located on the immediate right (J1 — J6). If the CPA backplane is the first backplane in the expansion cabinet, these will be 18-inch (45.7-cm) cables. If the CPA is installed immediately after another one, the cables will be 4 inches (10.2cm) long. Refer to Figures B-8, B-9, and B-10.

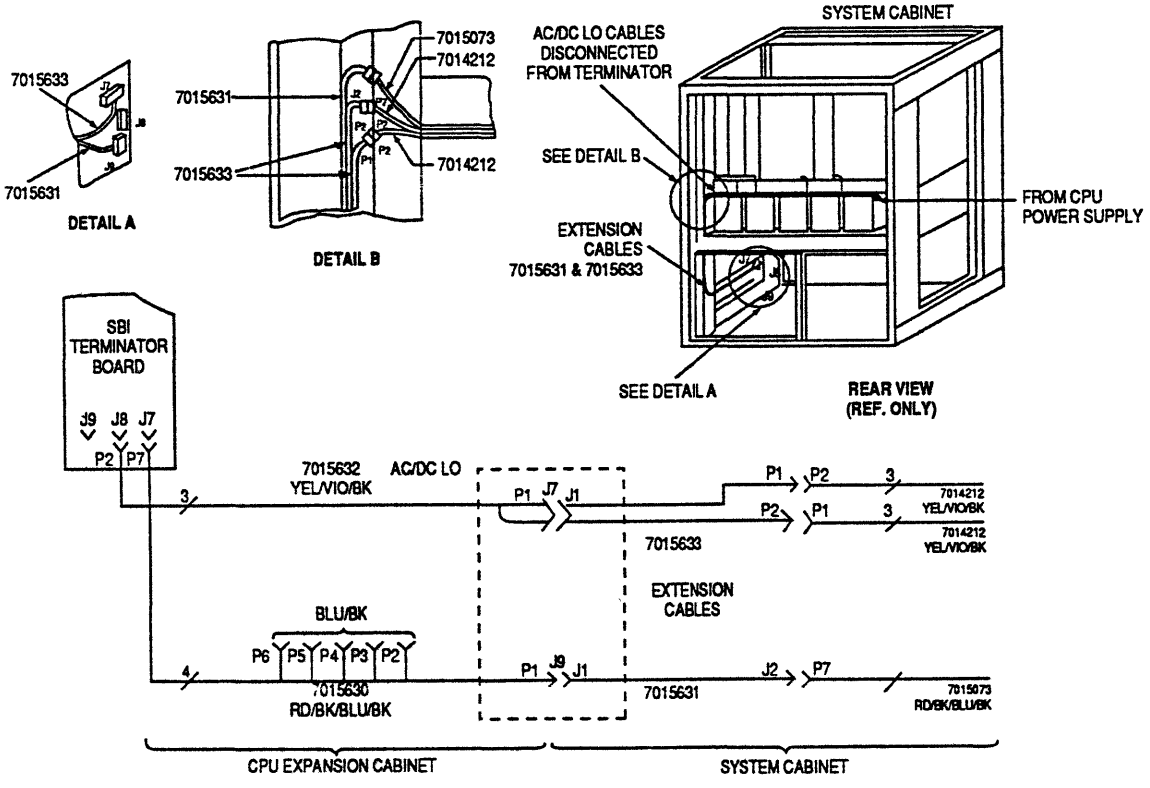


Figure B-8. SBI Cabling (Expansion Cabinet)

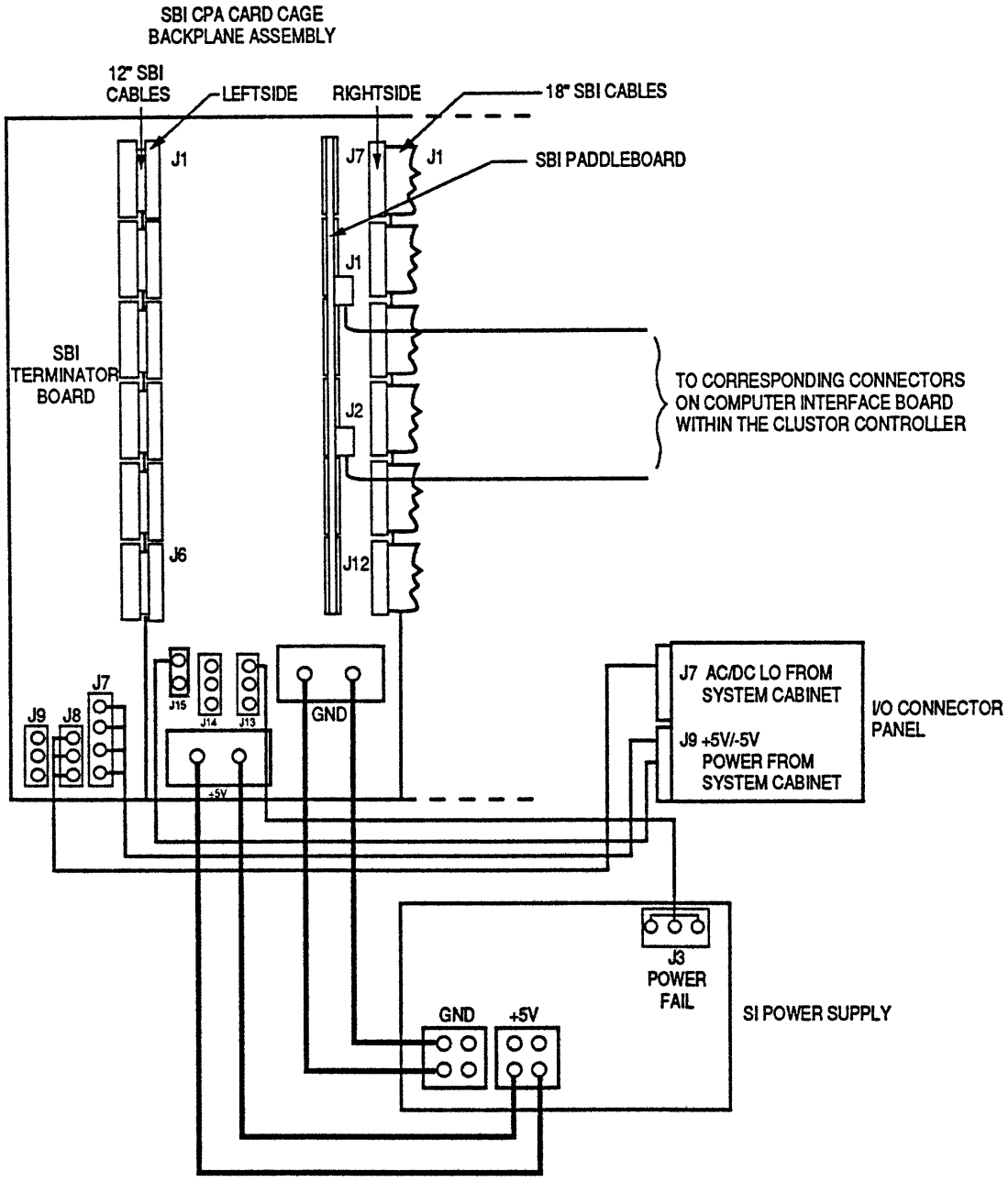


Figure B-9. SBI Cabling (System Cabinet)

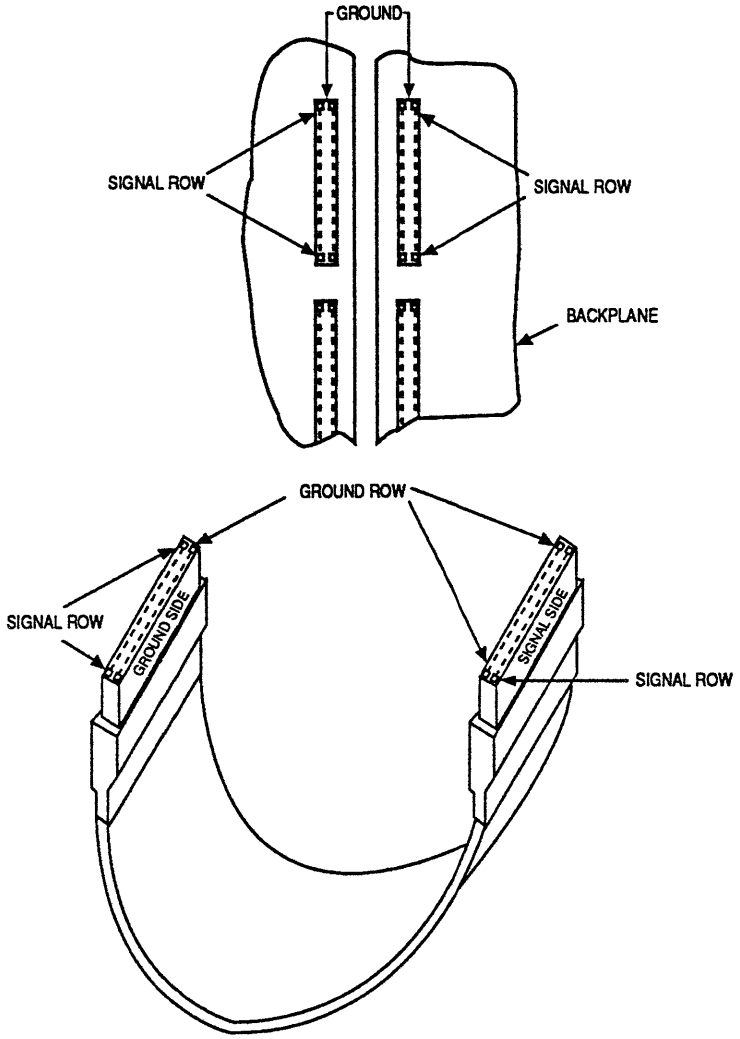


Figure B-10. SBI Signal Cable Orientation

CAUTION

Make sure that the signal side of each SBI cable is connected to the inside row of pins on each backplane connector. Refer to Figure B-11.

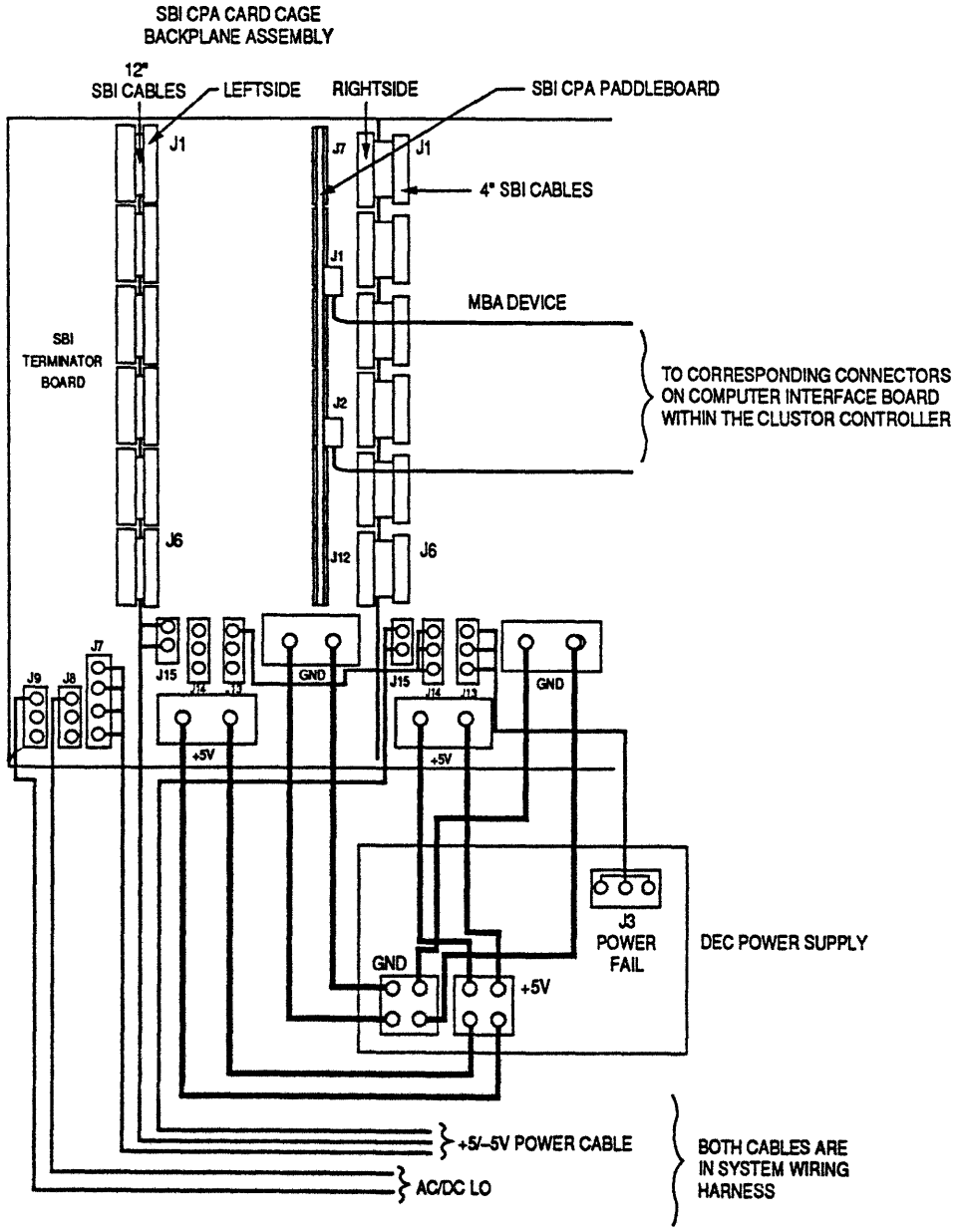


Figure B-11. Terminator Power Cables Installation

2. Connect six SBI cables from the left side of the CPA backplane (J1 — J6) to the right side of the backplane located to the immediate left. If it is the back-plane of another MBA, use 4-inch (10.2-cm) cables. If it is the backplane of the SBI terminator board, use the 12-inch (30.5-cm) cables previously removed.

3. Connect a –5V power cable (blue and black pair) to connector J15, on the interface backplane. This line is either tied into the system wiring harness or extends from the I/O connector panel. If the CPA is being installed in configuration 3 and the I/O connector panel has not been wired, refer to step 8.

4. For CPA configurations 1, 3, and 5, connect the AC/DC LO line from connector J3 on the power supply to connector J13 on the CPA backplane. The connection for CPA configuration 1 is shown in Figure B-8. It is similar for configurations 3 and 6, except it is in the system cabinet. The AC/DC LO line is color coded.

5. For CPA configurations 2, 4, and 6, connect the AC/DC LO line from connector J13 on the CPA backplane to connector J14 on the MBA backplane located to the immediate right of the interface. This connection for CPA configurations 4 and 6 is shown in Figure B-9. It is similar for configuration 2 except it is in the expansion cabinet.

6. Connect the four power supply leads from the CPA backplane to the power supply using the four 10-32 screws and washers supplied. The +5V lines are red and the ground lines are black.

7. If the terminator board is in the system cabinet, connect the +5V and the AC/DC LO lines removed previously, to connectors J7, J8, and J9, respectively, on the terminator board. If the terminator is in the expansion cabinet, its J9 connector is not used and the AC/DC LO lines are connected to J8. In the expansion cabinet the +5/–5V and AC/DC LO lines for the terminator and the –5V power cable for the CPA extend from the I/O connector panel. If this panel has not been wired, proceed to step 8.

8. When using the expansion cabinet, the AC/DC LO and +5V lines from the system cabinet are routed to the expansion cabinet via system extension cables and an I/O connector panel. The extension cables connect to the ends of the system cabinet terminator cables (The extension cable connecting to the AC/DC LO lines is a Y-cable). They extend to the I/O connector panel located near the bottom of the right panel of the system cabinet when viewed from the front (Figure B-16). To access the I/O connector panel, swing out the floppy disk subsystem.

Cable Routing

1. Insert the system cabinet AC/DC LO lines into connector J7 at the top of the I/O connector panel.
2. Insert the system cabinet AC/DC LO lines into connector J7 at the top of the I/O connector panel.
3. Insert the expansion cabinet AC/DC LO and power lines into the corresponding connectors, J7 and J9 respectively, on the I/O connector panel.

B.8 Controller to CPA Cabling

In an FCC-compliant environment the controller is housed in an SI FCC-complaint lowboy or highboy cabinet. At the base of the cabinet in the rear there is an I/O transition module for terminating 40-conductor external cables.

The SBI CPA is connected to the controller by internal and external 40-conductor cables via the transition module.

Within the VAX computer cabinet internal cables extend from J1 and J2 on the SBI paddleboard to shielded cable adapters on the VAX 11/780 IOCP. Before starting the installation, permanently identify all cables and interface panels.

CPA to controller cabling procedure is as follows (Figures B-12 and B-13):

1. Remove one of the panel units from the IOCP at the rear of the VAX 11/780 cabinet to the expansion cabinet.
2. Pass the internal J1 and J2 cables from the paddleboard through the opening.
3. Attach the J1 and J2 male connectors of the SI I/O adapter bracket.
4. Mount the bracket securely to the IOCP.

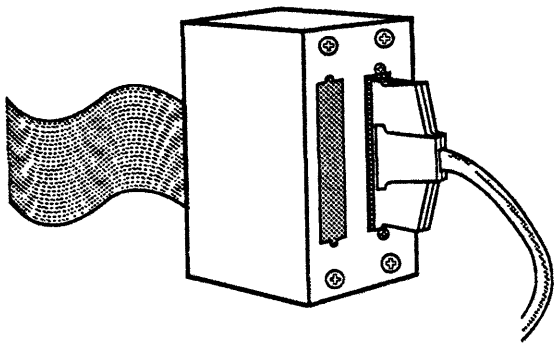


Figure B-12. 780 FCC/750 Non-FCC MASSBUS Cable

5. Run the shielded cables to the SI highboy cabinet and terminate them at the transition panel at the base of the cabinet.
6. Run the internal CPA cables from J1 and J2 on the CI board to the same paired connectors.
7. Make sure there is enough slack, 36 inches (91.4cm), in all the cables (including the drive cables and the AC power cord) to pull the controller enclosure out on its slides.

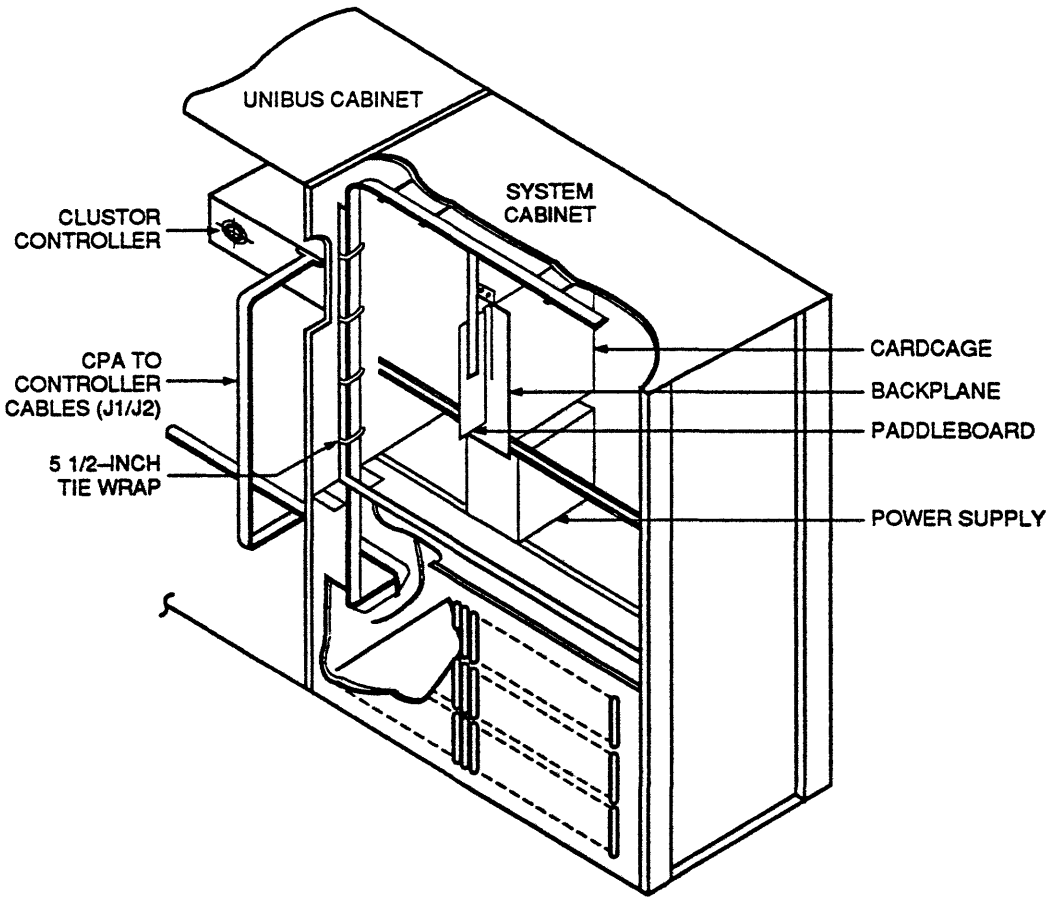


Figure B-13. Typical System Cabinet Installation

B.9 Power Requirements

The following voltages are required to operate the SBI CPA.

- +5VDC+/–.05 @ 25.0 Amps Maximum
- -5VDC+/–.05 @ 1.0 Amp Maximum

The +5VDC is obtained from the DEC or SI power supply. The –5VDC is obtained from the CPU's –5VDC power supply.

NOTE

When the system is finally powered-up, check that the switch outlet is connected by turning on and off the front panel system power ON/OFF switch. If the POWER NORMAL LED on the power supply goes on and off with the system cabinet ON/OFF switch, the switched line cord is connected.

Power Supply Check

To ensure reliable operation of the SBI CPA, check the +5VDC voltage of the DEC MBA power supply or SI power supply bus bars. It should be within the range +5.05 to +5.15 VDC. Make this check with the CPA in place. If the voltage is outside this range, and the supply is a DEC MBA power supply, consult the DEC field service representative to make the necessary adjustment or replacement. If the voltage is outside this range and an SI power supply is being used, adjust the VADJ screw at the rear of the power supply to bring the voltage within the range.

The –5VDC, which is not adjustable, is supplied by the CPU and is assumed to be operational. If this is not the case, call in a DEC field service representative.

Power Fail Circuit

The CPAs supported by the controller have power fail circuits that work in conjunction with power fail circuitry on the CI board to prevent spurious commands from being recognized by the controller when a CPA power failure occurs.

System Power-Up and Checkout

Restore power to the system and ask the user to run DEC Microdiagnostics, if he has the necessary software license. If such is not the case, boot the system up and run EXOR or SIDOS on-line to make sure the drives can be read from and written to.

B.10 Software Installation

Refer to VAX 780/750 86xx SBI/CMI Software Modifications for VMS.

B.11 Installation in a VAX 8600 or 8650

These paragraphs contain some general information about the VAX 8600 and 8650 CPUs, and the procedures for installing an SBI CPA in either of the systems.

General Information

The principal difference between VAX 780s and 8600s is that the 780 has only one SBI (SBI0), while the 8600 has two SBIs, a primary and a secondary, referred to as SBI0 and SBI1 respectively. In an 86xO system either SBI can be expanded into two cabinets to support a maximum of eight MBA devices, but they cannot be expanded into the same cabinet.

No MBA devices or other peripherals can be installed in 8600 or 8650 system cabinets. The SBI CPA must be installed in an SBI expansion cabinet. An SI expansion cabinet, which has five MBA slots, must be added if no DEC expansion cabinet is available at the site or if the existing cabinet is full.

NOTE

If the SBI CPA is going into a DEC expansion cabinet, the installation procedure is the same as the VAX-11/780 procedure.

No more than two expansion cabinets and a total of eight MBA devices can be added to the 8600. Up to four cabinets and a total of 16 CPAs could be added to the 8650, depending on cable length limitations. The total length of cable the SBI bus will support has not been determined.

If the CPA is being installed in a DEC expansion cabinet, there should be a DEC power supply in the cabinet. Each power supply (DEC or SI) can support up to two MBAs or CPAs. There are two optional SI power supply assemblies for (115/120 VAC @ 69Hz or 220/240 VAC @ 50 Hz available for this purpose. The SI expansion cabinet has space for three power supplies.

Preliminary Checkout

Verify the following:

- The 8600/8650 system has been brought down.
- Power is turned off at the power distribution panel of each cabinet in the system.
- All power to the 8600 system has been turned off. The main power switch is located in the back of the UNIBUS expansion cabinet at the base to the right of the main power cable. Other AC power switches are located in the CPU cabinet at the top and the base.
- The controller has been properly installed in the highboy cabinet(s) and the internal cabling of the disk drive has been done correctly.

Expansion Cabinet Installation

SI SBI expansion cabinets to be used with VAX 8600s or 8650s are shipped with one side panel because the VAX 8600/8650 side panels are not compatible with SI cabinets.

The expansion cabinet is positioned to the right of the CPU.

Procedure:

1. The top panel of the CPU cabinet has to be partially removed to allow the removal of the bezel at the top front the CPU cabinet. This is necessary in order to remove the CPU's right side panel.
2. To loosen the top of the cabinet open the rear doors and locate the two screws that hold the panel in place. They are located at the far left and far right of the panel. Be careful not to drop the screws.
3. Raise the panel from the rear and pull it forward a few inches.
4. The front bezel is held in place by two screws, one located at the far right and the other at the far left.
5. Set the bezel on the top panel, being careful not to disconnect any cabling. Label all the cables as a precautionary measure.
6. Remove the side panel and store it some place on site. The panel is not compatible with the SI expansion cabinet.
7. Bolt the SBI expansion cabinet to the CPU.
8. If a second cabinet is required, bolt it to the first cabinet and mount the side panel.

Installation in One SI SBI Expansion Cabinet

This section details the procedures for the installation of the CLUSTOR SBI CPA Subsystem and interfacing it with the VAX 8600. Two types of installation will be described:

- Installation in one SI Expansion Cabinet and interfacing with the VAX 8600 SBI0
- Installation in two SI Expansion Cabinets and interfacing with VAX 8600 SBIs SBI0 and SBI1

There are seven main procedures:

1. Terminator board installation
2. Power supply installation
3. Backplane and card cage installation
4. CPA to 8600 signal cabling
5. SBI CPA board installation
6. CPA power cabling
7. External cabling to the 2500 controller

The first three procedures can be done in any order, but 4, 5, 6, and 7 should be done sequentially. Normally, the SI SBI Expansion Cabinets come with the SBI card cage(s) and power supply(s) installed, in which case steps 1 — 3 can be bypassed. This procedure assumes that no other MBA devices are interfacing with the 8600 and that the CPA will interface with the 8600 SBI0.

SBI Terminator Installation

Before installing the terminator board remove the DEC SFT (system far end terminator) M9040 from the CPU. This is necessary when interfacing with SBI0.

Open the front doors of the cabinet. There are 24 I/O slots located on the right. The M9040 is in slot 5. Open the panel on the far right and remove the M9040 board. This board should be stored some place on site. Close the panel and the CPU front doors.

Position the SBI terminator board as the last device in the SBI expansion cabinet.

Procedure:

1. Remove the six 12-inch (30.5-cm) coaxial cables attached to the terminator assembly and set them aside for later use.
2. Remove the filter panel from the 4-inch backplane slot selected as the terminator location.
3. Mount the terminator assembly using the hardware supplied.

Power Supply Installation

An SI SBI Power Supply is required for every two CPAs.

Procedure:

1. Unused power supply slots contain filter boxes that are secured to the front of the cabinet with a screw and washer at the top of the box and to the rear of the cabinet with snapclip at the bottom. Remove the filter box.
2. Insert the power supply so the AC receptacles face the front of the expansion cabinet. Secure the power supply to the mounting frame with the single screw at the top of the supply.
3. Connect one end of the AC power cord to the switched outlet on the power distribution box at the base of the cabinet and the other end to the AC receptacle at the front of the supply.

CAUTION

The power distribution box has two sets of outlets:

- switched
- unswitched

The outlets are labeled and can be read from the front of the cabinet. The power supply must be connected to a switched outlet. The unswitched outlets have only a 5-amp breaker and bypass the RFI filter.

Backplane and Card Cage Installation

Procedure:

1. Remove the filter panel from the backplane slot chosen as the SBI CPA location.
2. Verify that the request (TR) jumper on the SBI backplane is set to the desired TR level.
3. Insert the SBI CPA card cage and backplane assembly into the cabinet from the rear. The assembly is held in place by two mounting brackets, one at the top of the assembly (rear of cabinet), the other at the bottom of the assembly (front). Mount the card cage using the four screws and washers removed in step 1, or use those supplied in the installation kit (Figure B-7).

CPA Signal Cabling

This procedure requires the following materials:

- Six 36-inch (91.4cm) 40-conductor coaxial cables.
- 4-inch (10.2cm) 40-conductor coaxial cables (These are insets of six, and the number of sets depends on the number of CPAs.)

Procedure:

1. Open the rear left door on the 8600 system cabinet. Remove the cover plate that is held in place by four hex bolts to expose the SBI0/SBI1 connectors. The SBI0 connectors are J41 — J46, and the SBI1 connectors are J47 — J52. They are under the left side of the cover.
2. Label each end of the 36-inch coaxial cables J41...J46.
3. Attach the cables to the J41 — J46 connectors in the SBI0 column and route them through the 8600's bulkhead to the expansion cabinet.

CAUTION

Be sure the signal side of each SBI cable is connected to the inside row of pins on each backplane connector. Refer to Figure B-10.

4. Connect the cables to the corresponding J41 — J46 connectors on the right side of the first SBI CPA backplane in the expansion cabinet.
5. Attach six 4-inch coaxial cables to connectors J47...J52 on the left side of the SBI CPA backplane.
6. Connect the cables to the corresponding J41...J46 on the right side of the next SBI backplane (J47 to J41...J52 to J46).
7. Repeat this procedure for the remaining SBI CPA backplanes except the last one in the chain.
8. On the last backplane connect the six 12-inch coaxial cables that were removed from the terminator to the J47 — J52 connectors on the last SBI CPA backplane. Connect them to the terminator board.

Installation of the CPA Boards

Installation for the CPA boards is described in the procedures below.

Procedure:

1. The boards should have been configured to the appropriate switch and jumper. Insert the CPA boards into the SBI card cage and backplane assembly from the front of the cabinet in the following order (from left to right):
   a. MPU interface board
   b. Data path board
   c. Internal registers board
   d. SBI interface board
2. Insert the paddleboard into the hex-high connector on the backplane so the J1 and J2 connectors are on the right side of the board when viewed from the rear of the cabinet (Figure B-7).

CAUTION

If for some reason the paddleboard has to be removed, take care to pull it out evenly from the top and bottom to prevent damage to the connector blocks.

Power Cabling

The +/–5VDC and AC/DC LO lines are in a wiring harness that is plugged into a connector block located near the bottom of the left side of the system cabinet when viewed from the rear. The power-fail lines come from the SI power supplies.

1. Connect the –5V lines (blue and black pair) to J15 on the SI SBI backplane.
2. Connect the AC/DC LO lines (yellow/violet/black) to J9 on the terminator backplane.
3. Connect the +5VDC lines to J7.
4. Run the harness to the system cabinet and plug into the corresponding connectors on the connector block.

CPA to Controller Cabling

In an FCC-compliant environment the 2500 controller is housed in an SI FCC-compliant 60-inch (152-cm) cabinet. At the base of the cabinet in the rear there is an I/O transition module for terminating 40-conductor shielded cables.

The SBI CPA is connected to the controller CI board by internal and external 40-conductor flat cables via the transition modules in the expansion and controller cabinets.

This procedure requires the following materials:

- One to four pairs of 40-conductor ribbon cable assemblies (internal)
- One to four pairs of shield 40-conductor cable assemblies

Procedure:

1. Label the internal and external cable pairs, e.g., J1 CPA 1, J2 CPA 1 etc.
2. Pass the internal J1 and J2 cables from the paddleboard(s) to the transition module at the base of the expansion cabinet.
3. Seat the cables in the feed through bulkhead connectors on the transition module and label the connectors.
4. Attach the shield terminators securely to the transition module.
5. Run the shielded cables to the controller cabinet and terminate them on the transition panel at the base of the cabinet.
6. Run the internal CPA cables from J1 and J2 on the CI board(s) to the paired connectors.
7. Make sure there is enough slack, 36 inches (91.4 cm), in all the cables (including the drive cables and the AC power cord) to fully extend the controller enclosure out onto its slide rails.

Installation in Two SI SBI Expansion Cabinets

This procedure is essentially the same as that for one cabinet, except for the following:

- The six cables running from the CPU to the second cabinet are about 7 feet. (2.13 m).
- It makes no difference which cabinet SBI0 or SBI1 is expanded to, but SBI0 and SBI1 cannot both be expanded to the same cabinet.
- There will be two Model 2500 controllers since more than four CPAs will be installed.
- The CPU is a VAX 8650.

Terminator, power supply, card cage, CPA boards and external cabling installation procedures are the same.

In this procedure SBI0 will be expanded to the first expansion cabinet, SBBI1 to the second. It is assumed that eight CPAs are being installed.

The procedure requires the following materials:

- Six 36-inch (91.4 cm) 40-conductor coaxial cables
- Six 7-foot (2.13 m) coaxial cables
- Two terminators
- Four SI power supplies
- Eight pairs of internal 40-conductor ribbon cables
- Eight pairs of shielded 40-conductor cables

Procedure:

1. Open the rear left door of the CPU and remove the cover plate that is held in place by four hex bolts to expose the SBI0/SBI1 connectors. SBI0 connectors are J7 — J12 (right column) and SBI1 connectors are J1 — J6 (left columns).
2. Label each end of the 36-inch coaxial cables SBI0 J7...SBI0 J12.
3. Mount the coaxial cables on the J7 — J12 connectors in the SBI0 column and route them to the first expansion cabinet.

CAUTION

Be sure the signal side of each coaxial cable is connected to the inside row of pins on each backplane connector (Figure B-7).

4. Connect the cables to the corresponding J7 — J12 connectors on the first CPA. Daisy-chain the next two CPAs with the four-inch coaxial cables, and connect the fourth CPA to the terminator in slot five with the 12-inch coaxial cables.
5. Label each end of the 7-foot cables SBI1 J6.
6. Connect them to J1 — J6 column of connectors on the CPU backplane.
7. Route them to the second expansion cabinet via the first cabinet and repeat step 4.

Power Requirements

The following voltages are required to operate the SBI CPA.

+5VDC+/−.05 @ 25.0 Amps Maximum

-5VDC+/−.05 @ 1.0 Amp Maximum

The +5VDC is obtained from the SI power supply. The −5VDC is obtained from the CPU's −5VDC power supply.

NOTE

When the system is finally powered-up, check that the switched outlet is connected by turning on and off the front panel system power ON/OFF switch. If the POWER NORMAL LED on the power supply goes on and off with the system cabinet ON/OFF switch, the switched line cord is connected.

Power Supply Check

Check the +5VDC voltage of the SI power supply bus bars. It should be within the range +5.05 to +5.15 VDC. Make this check with the CPA in place. If the voltage is outside this range, adjust the VADJ screw through the hole to the right of the bus bars (back of the power supply) to bring the voltage within this range.

The −5VDC is obtained from the existing system's −5VDC supply and is assumed to be operational.

Power Fail Circuit

The CPAs supported by the controller have power fail circuits that work in conjunction with power fail circuitry on the CI board to prevent spurious commands from being recognized by the controller when a CPA power failure occurs.

System Power-Up and Checkout

1. Restore AC power to the CPU cabinet and all peripheral cabinets.
2. Set the main circuit breakers in the CPU cabinet and in each peripheral cabinet to ON.
3. Have the system manager bring up the system.
4. Run the SI diagnostic program SIDOS.

APPENDIX C
QBUS CPA INSTALLATION

This section contains installation procedures for the Qbus CPA. Only a Qbus CPA board with part number 2500-6102, or higher, is compatible with the controller.

- Preinstallation inspection
- CPA board configuration
- Installation Materials
- Installation in a BA23 chassis
- Installation in a BA123 chassis
- Installation in a MicroVAX III
- Installation in a BA213/215 chassis.

C.1 Preinstallation Inspection

Verify the following:

- All installation materials are present and undamaged.
- All components on the CPA board(s) are in place and connector pins are not bent or otherwise damaged.
- The highboy cabinet is undamaged and its doors seal properly.
- The drives in the cabinet have been cabled and grounded correctly.
- The locking mechanisms on the drives are in the unlocked position. This does not pertain to SI 9722/33 or SI83 drives. These drives have automatic locking/unlocking mechanisms (plunger magnets).
- The elbow and cover plate on the power cable have been installed at the proper location. The portion of the power cable between the elbow and the power distribution box must be of sufficient length to allow the elbow/cover plate assembly to reach the power cable exit port at the base of the cabinet.

C.2 CPA Board Configuration

This section deals with setting the configuration switches on the CPA board. The switch locations are shown in Figure C-1. The switches determine the following:

- Control Status Register (CSR) Address
- Interrupt Vector
- Data Transfer Mode
- Interrupt Level

CAUTION

Make certain the MicroVAX system has been shut down and the AC power supply disconnected before proceeding with the installation.

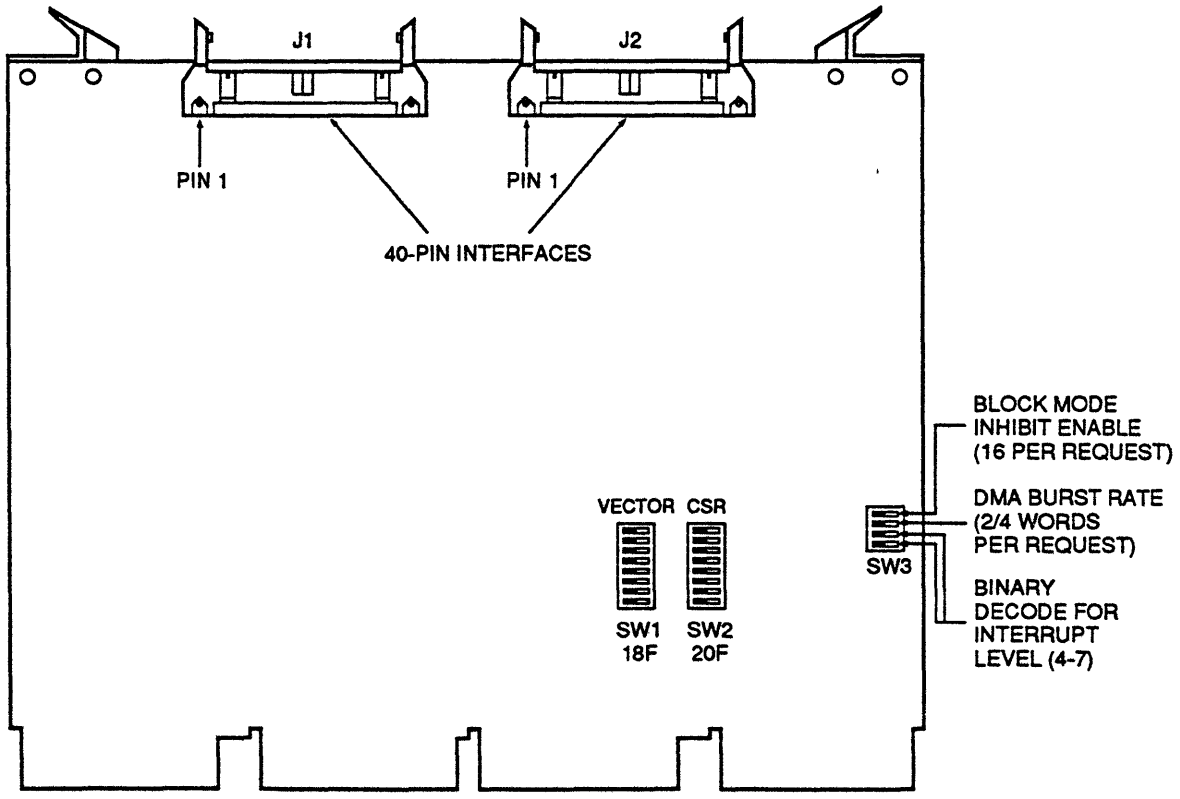


Figure C-1. Switch Locations and Functions

Control Status Register (CSR) Address

The CSR address DIP (SW2) is located at 20F. The standard primary and secondary addresses (176700 and 176300 octal, respectively) switch settings are listed in Table C-1. Nonstandard Qbus addresses can be selected by setting the appropriate Qbus address switches. A switch in the OFF position produces a logical 1 on the Qbus address line. The range is 160000 to 177700 (octal).

Table C-1. Control Status Register Address Switch Settings

QBUS ADDRESS LINES	PRIMARY ADDRESS 176700 SWITCHES 1 — 8		SECONDARY ADDRESS 176300 SWITCHES 1 — 8	
(Clustor 2500)	1	OFF*	1	OFF*
6†	2	OFF	2	OFF
7	3	OFF	3	OFF
8	4	OFF	4	ON
9	5	ON	5	ON
10	6	OFF	6	OFF
11	7	OFF	7	OFF
12#	8	OFF	8	OFF

* Standard Setting; 1 = OFF 0 = ON

† Address lines 0 — 5 are always equal to 0.

Address lines 13 — 17 are always equal to 1.

Interrupt Vector

The interrupt vector DIP (SW1) is at location 18F. The primary and secondary switch in the OFF position produces a logical 1 on the corresponding interrupt vector line. The range is 000 to 376 (octal).

Table C-2. Interrupt Vector Switch Settings

QBUS ADDRESS LINES	PRIMARY VECTOR 254 SWITCHES 1 — 8		SECONDARY VECTOR 150 SWITCHES 1 — 8	
1	1	X	1	X
2	2	ON	2	ON
3	3	OFF	3	ON
4	4	OFF	4	OFF
5	5	ON	5	ON
6	6	OFF	6	OFF
7	7	ON	7	OFF
8	8	OFF	8	ON

* X = DOES NOT CARE 1 = OFF 0 = ON

Transfer Mode

Transfer mode is determined by switches 3 and 4 in DIP SW3 located at 25E. Transfer can be either two or four words in standard mode and 16 in block mode. The block mode inhibit option is switch selectable. The settings are listed in Table C-3.

Table C-3. Transfer Mode Switch Settings (SW3)

SWITCH NUMBER	SWITCH SETTING	FUNCTION
SW3-3	ON	Two-word DMA*
SW3-3	OFF	Four-word DMA*
SW3-4	OFF	Block Mode Enable†

* OFF = 1 ON = 0

† Block Mode Disabled = SW3-4 ON

Interrupt Levels

The Qbus CPA is a position-independent device that uses a four-level interrupt scheme and monitors all higher level request lines. The default level is four. Interrupt level switch settings are listed in Table C-4. The switch pack is SW3 located at 25E.

Table C-4. Interrupt Level Switch Settings

INTERRUPT LEVEL	SW3-2*	SW3-1*
4	ON	ON
5	ON	OFF
6	OFF	ON
7	OFF	OFF

* OFF = 1 ON = 0

C.3 Installation Materials

The installation kit contains the following:

- Two 40-conductor ribbon cables per CPA, either 10 in. (25.4 cm) or 18 in. (4.57 cm) depending on the type of Micro VAX chassis.
- Two shielded 40-conductor round cables per CPA.

NOTE

Although these cables are referred to in the following procedures as being keyed. It is actually the cable shield that is keyed, not the female connector. However, the shield keys can be used to indicate pin one location.

- Mounting hardware.
- Adapter plate for the Micro VAX IOCP.
- Feed through bulkhead connector assemblies (each assembly consists of a housing and a ground plane).

C.4 Installation in a BA23

These instructions assume the BA23 is either a floorstand or tabletop unit.

1. If it is in place, remove the rear plastic cover from the BA23 by holding each end (top and bottom) of the cover and pulling it off.
2. Locate the IOCP (Figure C-2) and loosen the two captive screws at the top that hold it in place. Pull it forward and set it at the base of the cabinet. If it can be avoided, do not disconnect any internal or external cables.

NOTE

There are currently two kinds of removable panels on the IOCP: a type A panel that measures 1 x 4 in. (2.54 x 10.2 cm) and a type B measuring 2 x 3 in. (5.1 x 7.6 cm).

3. Identify the 10-inch 40-conductor ribbon cables (J1, J2). If two CPAs are being installed, label them J1-1, J1-2, J2-1, and J2-2. Connect the cables to the CPA and mount it in the first available slot from 4 through 8 in the backplane (Figure C-3).

NOTE

There can be no empty slots between the CPA and the CPU.

If an RX50 (floppy) is in the system and its controller is an RQDX1, the CPA must be placed in front of it, since the RQDX1 does not pass bus grants.

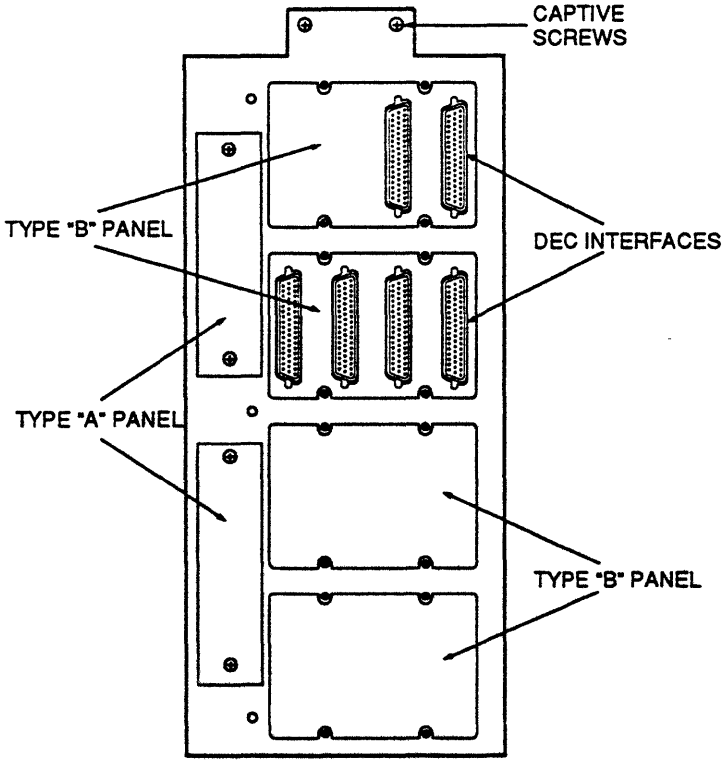


Figure C-2. BA23 IOCP

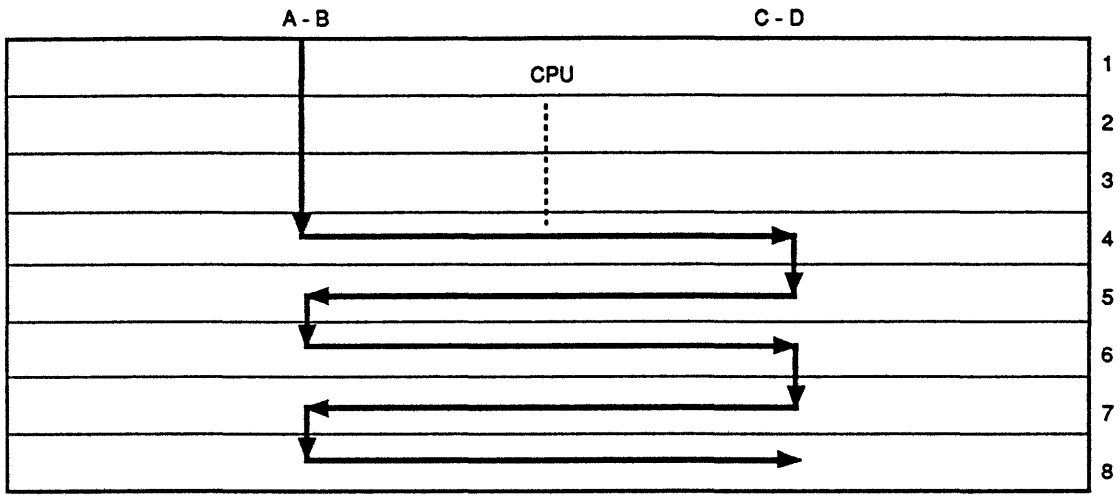


Figure C-3. BA23 Bus Continuity

4. Remove as many B panels as necessary.
5. This step references Figure C-4. Assemble the 40-pin feed through bulkhead connectors and mount them on the adapter plate as follows:
6. Mount the adapter plate/connector assembly on the IOCP.
7. Connect the CPA internal cables to the adapter/connector assembly, making sure the pin alignment is correct.

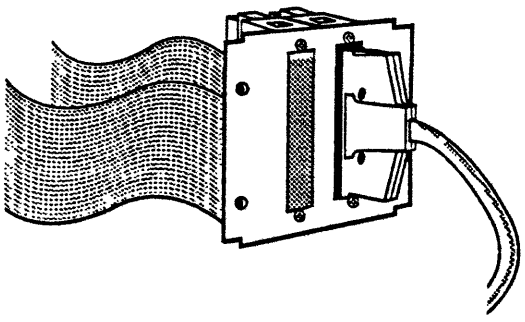


Figure C-4. BA23 Adapter Plate and Connector Assembly

8. Remount the IOCP.
9. Label the external cables and connect them to the bulkhead connectors on the adapter assembly. The feed-through bulkhead connectors and cable shields are keyed, so make sure the alignment is correct before mating them.
10. Route the cables to the drive cabinet and lay them under the cabinet.
11. Using a short-reach Phillips screwdriver, remove the transition panel cover held in place by two screws, one at each end of the panel. Check that the bulkhead connector keys are in the same relative positions as those on the IOCP adapter assembly. This is essential to maintain proper pin alignment.
12. Connect the J1, J2 external cables to the appropriate bulkhead connectors. If the connectors have not been labeled J1 and J2, it will be necessary to check the CI board in the controller to trace the cables.
13. Replace the transition panel cover.

C.5 Installation in a BA123

This procedure references Figures C-5 through C-7.

CAUTION

Make certain the MicroVAX system has been shut down and the AC power supply disconnected before proceeding with the installation.

1. Reach underneath the rear cover and pull it open to expose the IOCP and to enable the removal of the right side panel.

CAUTION

Removing the side panel (step 3) should be done very carefully to avoid damaging the RFI/EMI glue-on fingers on the inside of the panel.

2. Remove the side panel retaining bolt at the rear of the side panel. To remove the side panel pull it forward from the bottom until the two plastic locking pins on the inside of the panel at either end clear their retainer sockets. Lift it up until the two lips on the upper inside of the panel clear the slots at the top of the chassis.
3. To remove the backplane RFI cover open the two latches at the top and bottom of the cover and swing it out on its pivots.

4. Label the 40-conductor ribbon cables J1, J2. (If two CPAs are being installed, label them J1-1, J1-2 and J2-1, and J2-2). Install the board in the first available slot in the backplane. The last device on the backplane, prior to Qbus CPA board installation, will probably be the DEC RQDX2 board.

NOTE

To preserve bus grant continuity there must be **no** empty slot between the CPA board and any other device on the backplane (Figure C-6).

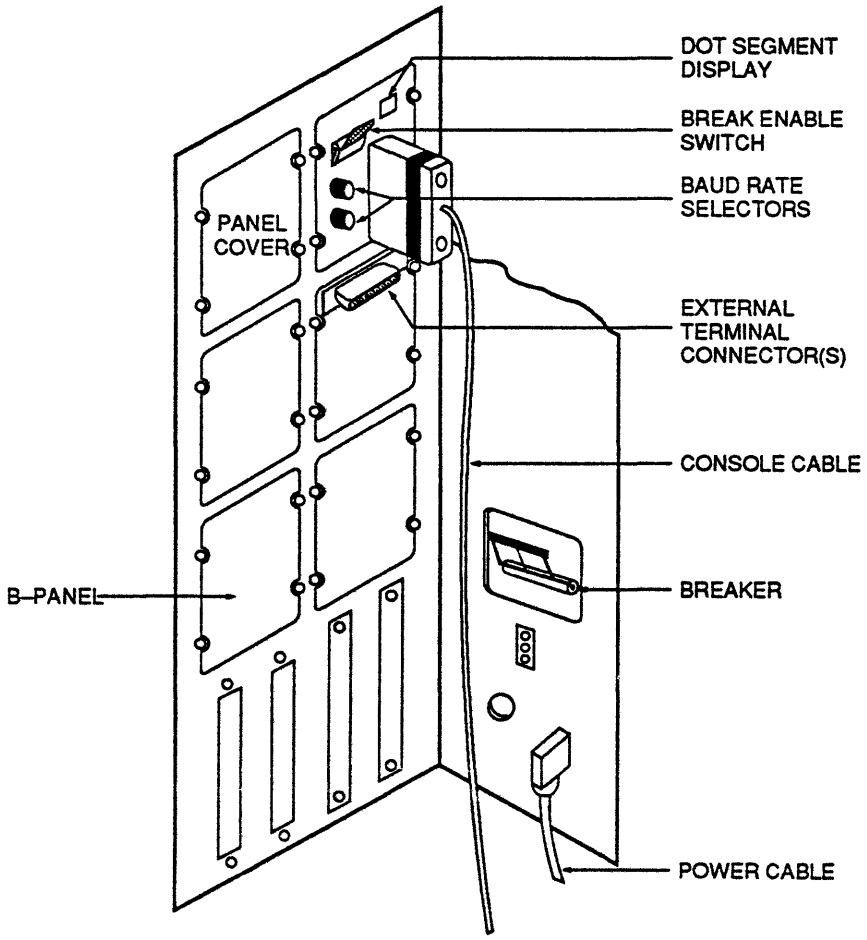


Figure C-5. BA123 IOCP

NOTE

If an RX50 (floppy) is in the system and its controller is an RQDX1, the CPA must be placed in front of it, since the RQDX1 does not pas bus grants.

There are two kinds of removable panels on the IOCP: a type A panel that measures 1 x 4 in. (2.54 x 10.2 cm) and a type B that measures 2 x 3 in. (5.1 x 7.6.cm)

5. Remove as many B panels as necessary.
6. Assemble the 40-pin feed through bulkhead connectors and mount them on the adapter plate (Figure C-7).
7. Mount the adapter plate/connector assembly on the IOCP.
8. Connect the CPA internal cables to the adapter/connector assembly, noting the location of pin one.
9. Remount the IOCP.
10. Label the shielded 40-conductor external cables and connect them to the adapter assembly. the connectors on the shielded cables are keyed, so make sure the alignment is correct before seating them.

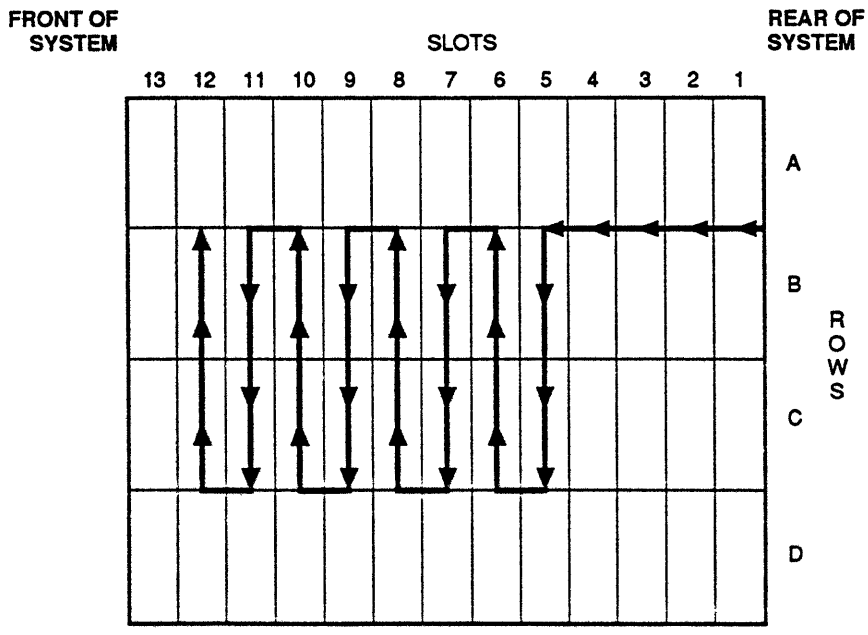


Figure C-6. BA123 Bus Continuity

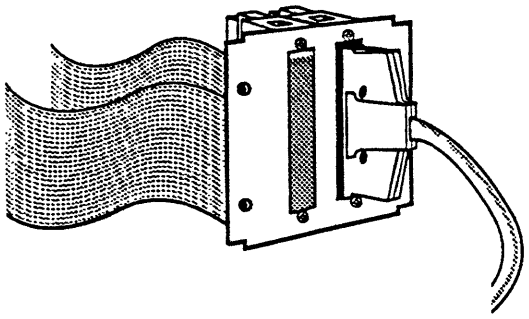


Figure C-7. BA213 Adapter Plate and Connector Assembly

11. Route the cables to the drive cabinet and lay them under the cabinet.
12. Using a short-reach Phillips screwdriver, remove the transition panel cover held in place by two screws, one at each end of the panel. Check that the bulkhead connector keys are in the same relative positions as those on the IOCP adapter assembly. This is essential to maintain proper pin alignment.
13. Connect the J1, J2 external cables to the appropriate bulkhead connectors. If the connectors have not been labeled J1 and J2, it will be necessary to check the CI board on the controller to trace the cables.
14. Replace the transition panel cover.

WARNING

Do not operate the system with the BA123 side and RFI panels removed. Doing so interferes with air flow and results in serious, if not fatal, damage to the CPU. If it is necessary to run the system for a while with these panels removed, an additional cooling means must be provided.

In newer BA123 chassis there are auxiliary fans that come on automatically when the panels are removed, so additional cooling is not required.

15. Replace the BA123 right side panel and RFI shield and close the IOCP cover.

C.6 MicroVAX III Installation

The MicroVAX III is housed in a DEC H9644 cabinet as shown in Figure C-8. The cabinet holds the RA82 disk drive and a BA213 chassis. A front door with recessed handle opens into the BA213 chassis. The cabinet door has a sliding window controlled by a three-position rotary lock. Behind the window are the controls that operate the RA70 disk drives, the TK70 tape drive, the system ON/OFF switch, and the door latch.

Power-Down the Cabinet

Follow the steps below to power-down the chassis. Refer to Figure C-9 for locations.

1. Turn the key in the rotary lock to position 3 and slide the window down.
2. Follow the shutdown procedure in the system software manuals.
3. Turn the system off by setting the ON/OFF switch to 0.

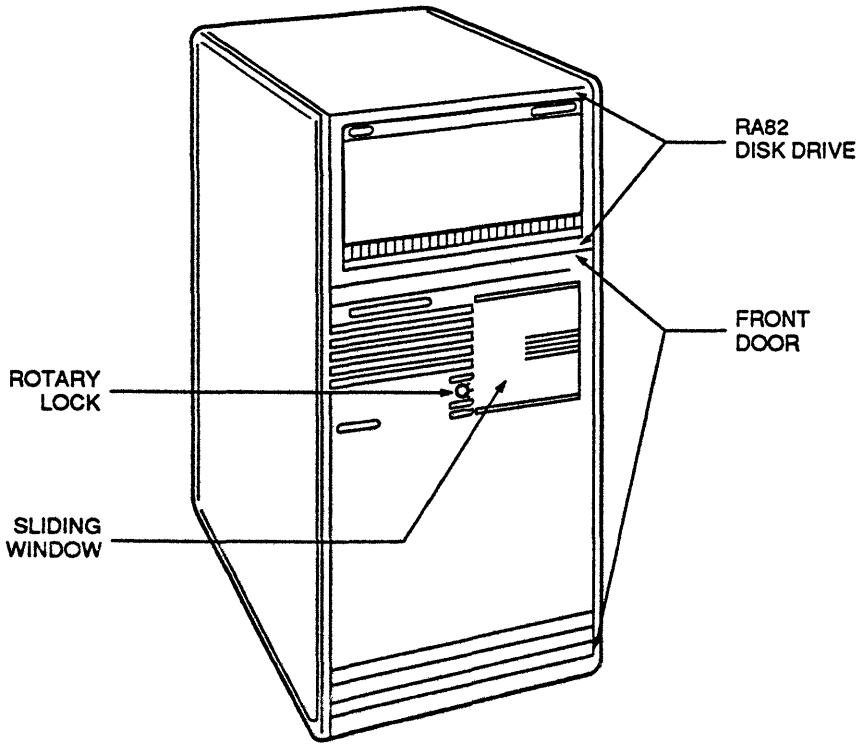


Figure C-8. MicroVAX III Cabinet

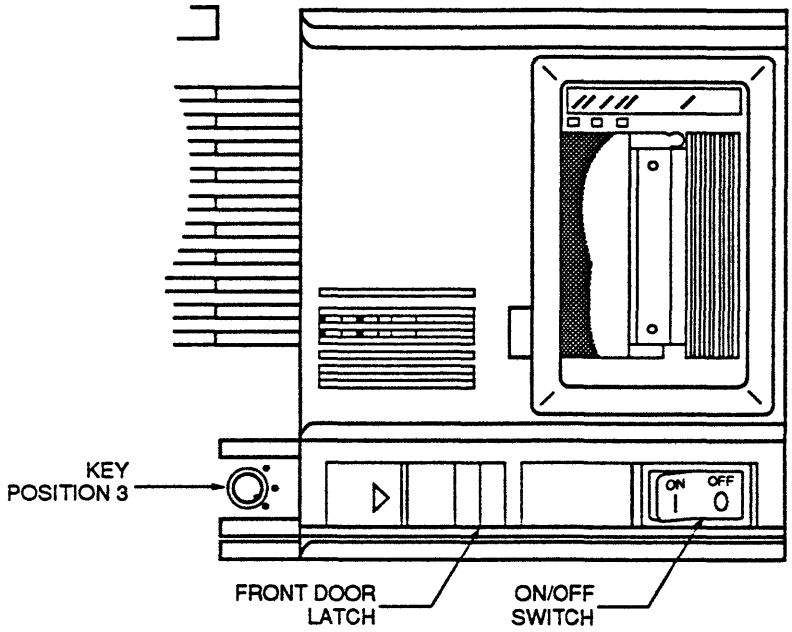


Figure C-9. Window and Control Locations

Cabinet Rear Panel Removal

The following procedure is for the removal of the rear panel. Rear panel removal is shown in Figure C-10.

1. Turn the two screws counter-clockwise a quarter turn using a 1/8-inch Allen wrench.
2. Support the top of the panel while loosening the second screw.
3. Tilt the top of the panel out about three inches.
4. Lift the panel out of the supporting bracket.

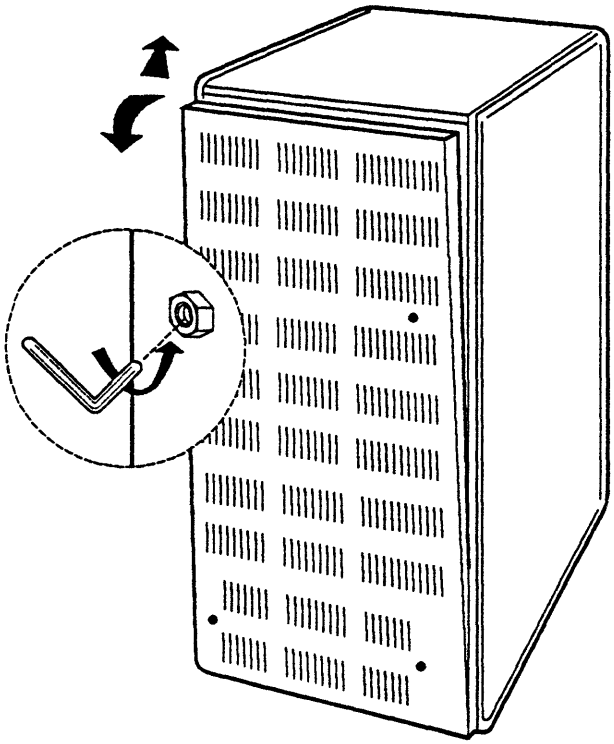


Figure C-10. Cabinet Rear Panel Removal

Open the Front Door

Perform the next steps to open the cabinet door.

1. Push the door latch to the right. The left side of the door springs open.
2. Pull the door fully open.

C.7 BA213 Chassis

Opening the front door to the MicroVAX III cabinet allows access to the components in the BA213 chassis, as shown in Figure C-11. The chassis contains:

- TK70 tape drive
- RA70 disk drives
- Card cage with the CPU, memory, controllers, communications, and mass storage controllers.
- 2 power supplies
- 2 fans

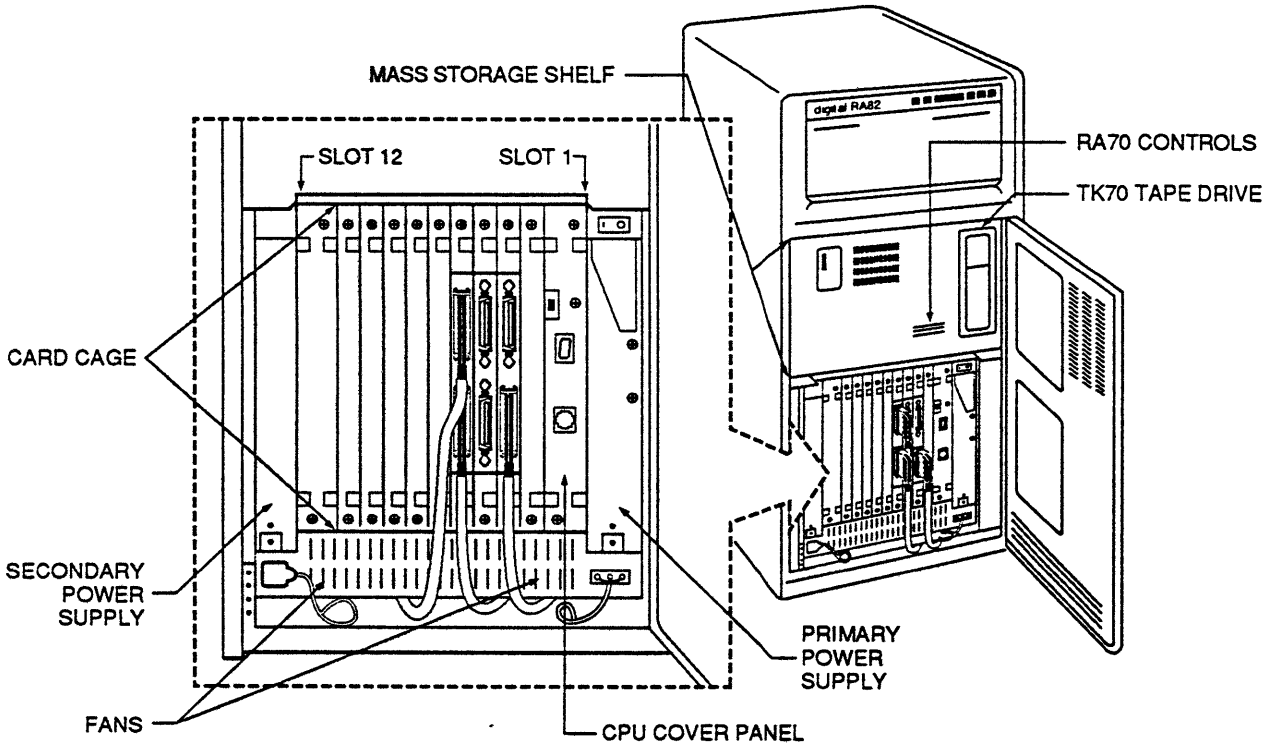


Figure C-11. BA213 Chassis

Card Cage

A 12-slot card cage under the mass storage unit houses the components. Every slot is protected by a cover panel. Do the following steps with reference to Figures C-11 and C-12.

1. Remove an empty slot cover panel using a Phillips screwdriver.
2. Slide the board into the empty slot.
3. Assemble the transition panel and connect it to the Qbus/CLUSTOR CPA.

Cable Connection

Run the cable under the fans at the bottom of the BA213 chassis, and out the back of the cabinet. Attach the shielded connector to the appropriate controller.

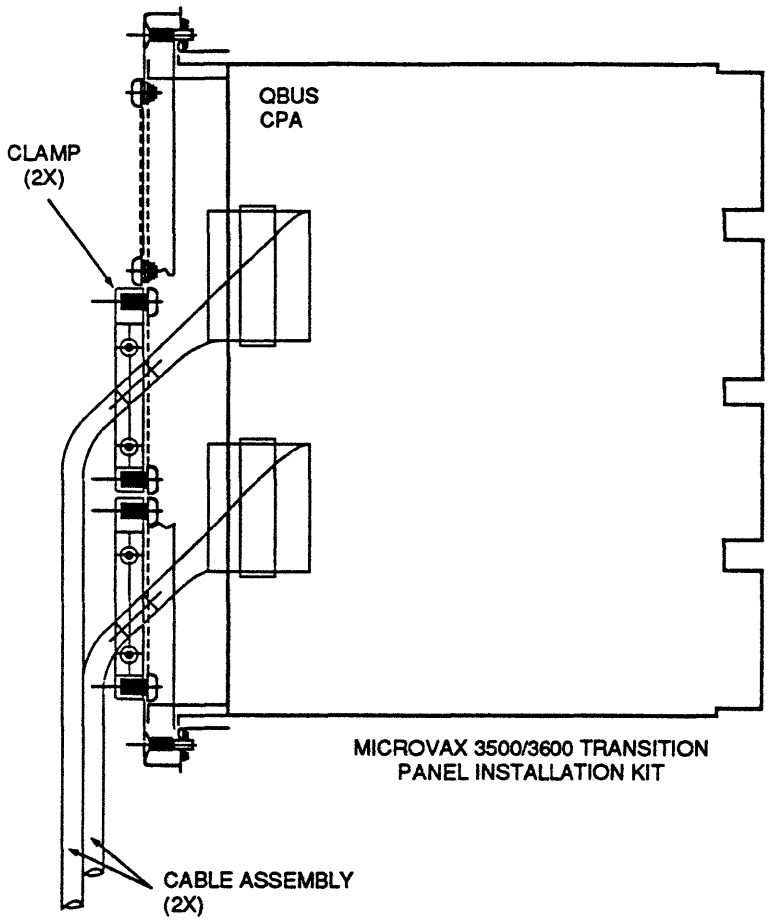


Figure C-12. Qbus/CLUSTOR CPA

APPENDIX D
UNIBUS CPA INSTALLATION

This section contains installation procedures and register information for the UNIBUS CPA. The UNIBUS CPA board must have part number 2500-6101, or higher, to be compatible with the CLUSTOR Storage System Controller.

WARNING

To avoid personal injury or equipment damage, be sure that all AC power to the system as been disconnected.

D.1 Preliminary Steps

Before installing the CPA, verify the following:

- All components are undamaged, in place, and secure.
- Connector pins are not bent or otherwise damaged.
- Cables are not kicked or cut.
- Cables shield terminators are properly installed.

D.2 Switch and Jumper Settings

Three switch settings and four jumper settings must be checked and, if necessary, set for the UNIBUS CPA to operate correctly with the controller. The following paragraphs discuss the switch and jumper settings required to configure the UNIBUS CPA. The board matrix positions for the necessary jumpers and switch positions on the UNIBUS CPA board are shown in Figure D-1.

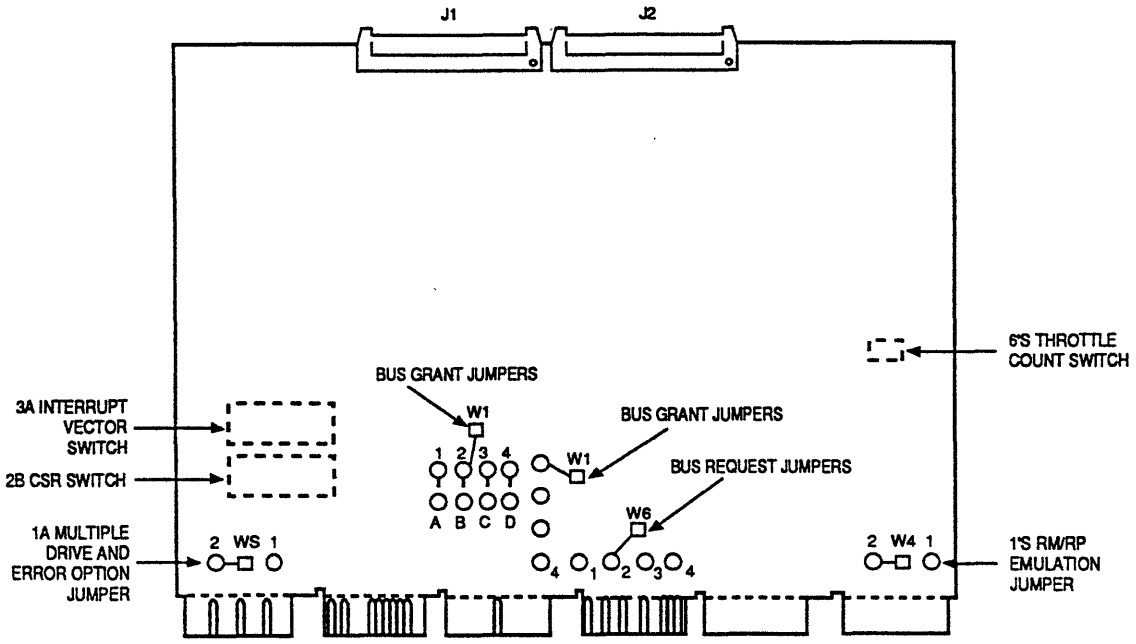


Figure D-1. UNIBUS CPA Board

Control Status Register Address

The CSR address switch is located at 2A (see Figure D-1). The switch settings are given in Table D-1. Switch 1 is OFF for all Clustor applications. Nonstandard UNIBUS addresses are selected by setting the appropriate UNIBUS address switches. A switch in the OFF position produces a logical 1 on the UNIBUS address line.

Table D-1. CSR Address Switch Settings

UNIBUS ADDRESS LINES	PRIMARY ADDRESS 776700 SWITCHES 1 — 8		SECONDARY ADDRESS 776300 SWITCHES 1 — 8	
(Clustor 2500)	1	OFF*	1	OFF*
12†	2	OFF	2	OFF
11	3	OFF	3	OFF
10	4	OFF	4	ON
9	5	ON	5	ON
8	6	OFF	6	OFF
7	7	OFF	7	OFF
6#	8	OFF	8	OFF

* Standard Setting: 1 = OFF 0 = ON

† Address lines 13 — 17 are always equal to 1.

Address lines 0 — 5 are always equal to 0.

Interrupt Vector

The interrupt vector switch is at location 3A (Figure D-1). The switch settings are given in Table D-2. Nonstandard interrupt vectors can be selected by setting the appropriate interrupt vector switch. A switch in the OFF position produces a logical 1 on the corresponding interrupt vector line.

Table D-2. Interrupt Vector Switch Settings

UNIBUS ADDRESS LINES	PRIMARY VECTOR 254 SWITCHES 1 — 8		SECONDARY VECTOR 150 SWITCHES 1 — 8	
—	1	X	1	X
7	2	OFF	2	ON
6	3	ON	3	OFF
5	4	OFF	4	OFF
4	5	ON	5	ON
3	6	OFF	6	OFF
2	7	OFF	7	ON
1	8	ON	8	ON

* X = DOES NOT CARE 1 = OFF 0 = ON

Throttle Count

The throttle count switch on the UNIBUS CPA board is located at 6S (Figure D-1). The switch settings are in Table D-3.

Table D-3. Throttle Count Switch Settings

SW1	SW2	SW3	SW4	WORDS TRANSFERRED PER BUS ARBITRATION CYCLE
OFF	OFF	OFF	ON	1
ON	OFF	ON	OFF	2
OFF	ON	OFF	OFF	4
ON	OFF	OFF	OFF	8

CPA Jumpers

The RM emulation jumper is W4 (Figure D-1) at location 7H. The jumper is connected to pin 2 for RM-emulation. The 2500-6101 CPA board has a multiple drive type and error register option. Jumper W5 is at location 5D (Figure D-1). The jumper should be in the 2 position regardless of whether the system has multiple drive types.

W6 is the CPA error clear enable. For Clustor W6 is in position 1.

Bus Request Jumper

Bus request jumper W3 on the UNIBUS CPA board is configured for BR5 priority, as shown in Figure D-1. Additional bus request settings are listed in Table D-4.

Table D-4. Bus Request Connections on the UNIBUS CPA Board

BUS REQUEST PRIORITY LEVEL	JUMPER CONFIGURATION
BR4	W3 to 1
BR5	W3 to 2
BR6	W3 to 3
BR7	W4 to 4

Bus Grant Jumpers

Any unused slots preceding the slot occupied by the UNIBUS CPA must be filled with a bus grant continuity card to insure bus continuity. Verify that the bus grant jumpers W1 and W2 on the UNIBUS CPA board are wired for BG5 priority as shown in Figure D-1. Additional bus grant settings are listed in Table D-5.

NOTE

The bus grant level and the bus request level must be the same.

Table D-5. Bus Grant Jumper Settings for the UNIBUS CPA Board

BUS GRANT PRIORITY LEVEL	JUMPERS W1	A	B	C	D	W2
BG4	to 1	OUT	IN	IN	IN	to 1
BG5	to 2	IN	OUT	IN	IN	to 2
BG6	to 3	IN	IN	OUT	IN	to 3
BG7	to 4	IN	IN	IN	OUT	to 4

Nonprocessor Grant (NPG) Jumper

The NPG line is the UNIBUS grant line for devices that perform data transfers without processor intervention. NPG line continuity is provided by wirewrap jumpers on the backplane. When an NPR device is installed into a slot, the corresponding jumper wire from pin CA1 to pin CB1 of that slot must be removed. This jumper must be removed from the slot where the CPA board is installed but must remain in place on or be added to any unoccupied SPC slots on the bus. The rear view of the SPC backplane is shown in Figure D-2.

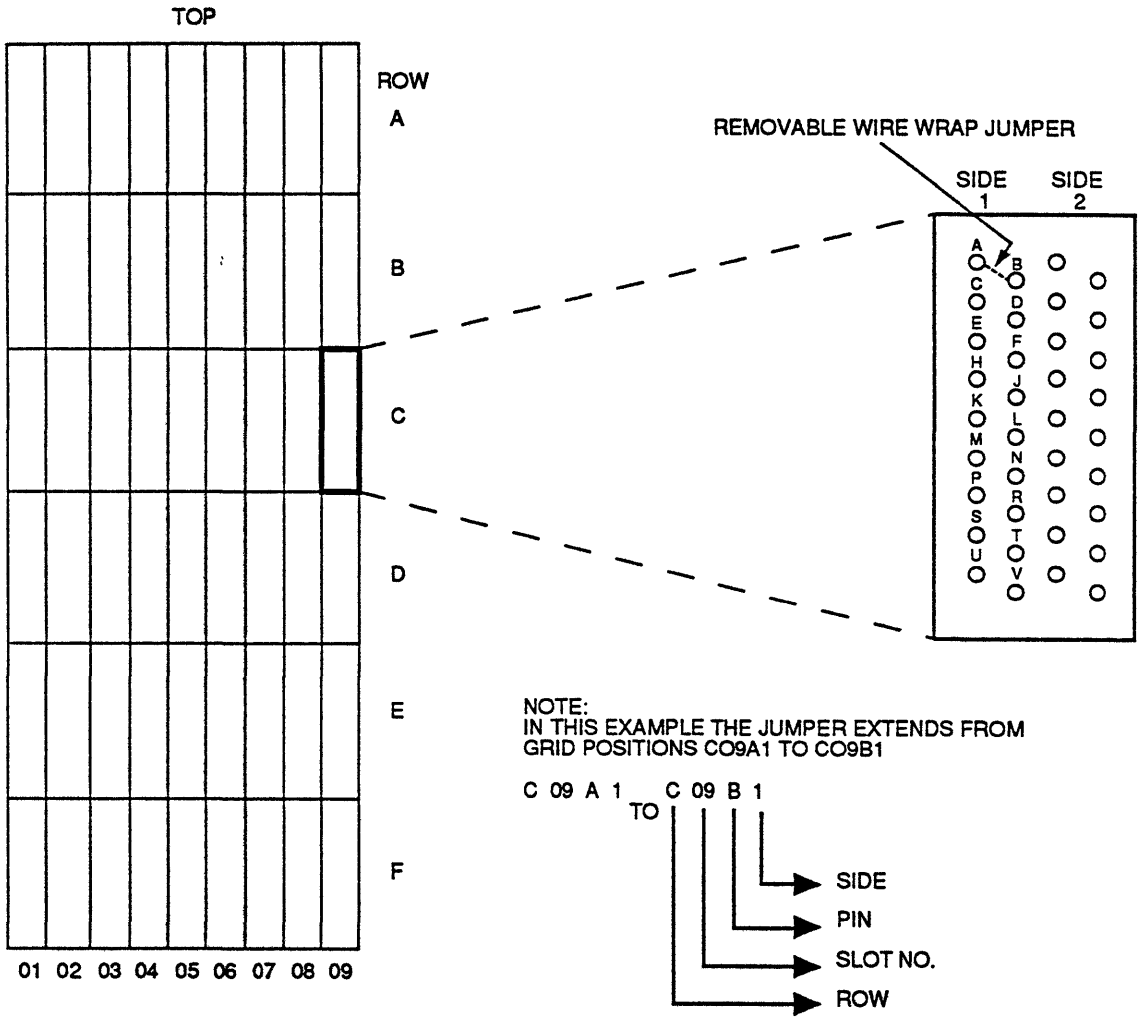


Figure D-2. SPC Backplane, Rear View

D.3 Control to CPA Cabling

The UNIBUS CPA board is connected to the controller by two 40-conductor flat ribbon cables. The cables connect J1 and J2 on the UNIBUS CPA board to J1 and J2 on the computer interface (CI) board within the controller. The cable connection is shown in Figure D-3. In most installations, the CPA and controller are in separate cabinets, requiring the installation of cabling between the cabinets and the use of transition panels to go from the internal flat cables to the shielded external cables.

To comply with FCC regulations, Part 15 subpart J, all external cables must be shielded. Restrictions imposed by cable routing or space limitations make it useful to arrange the cables before installing the CPA board in the SPC slot. The prearranged cables can be connected to the board before or after it is installed in the SPC slot.

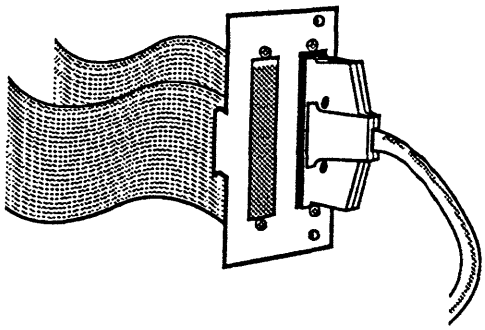


Figure D-3. UNIBUS Adapter Plate and Connector Assembly

D.4 Physical Installation

Remove the bus grant continuity card from the SPC slot selected for the CPA card, and install the UNIBUS CPA board.

NOTE

The NPG jumper must be removed from the slot where the CPA board is being installed.

D.5 Power Requirements

The UNIBUS CPA requires +5VDC at 5 Amps maximum. This is obtained from the UNIBUS backplane and is counted as one bus load.

CPA Power Fail Circuitry

CPAs supported by the controller have power-fail circuits that work in conjunction with power-fail circuitry, via SW1, on the computer interface (CI) board. This prevents spurious commands from being recognized by the controller when a CPA power failure occurs.

Boot PROM Installation

1. If a bootstrap PROM for the controller is NOT to be installed, proceed to step 5.
2. Bootstrap PROM installation. Remove the CPU memory controller module (L0011, or L0016) from slot 10 in the CPU backplane. Note that it has four 16-pin DIP sockets in which to install bootstrap PROMs. The four sockets correspond to the four boot switch positions (A, B, C, and D) on the CPU front panel. See Figure D-4.

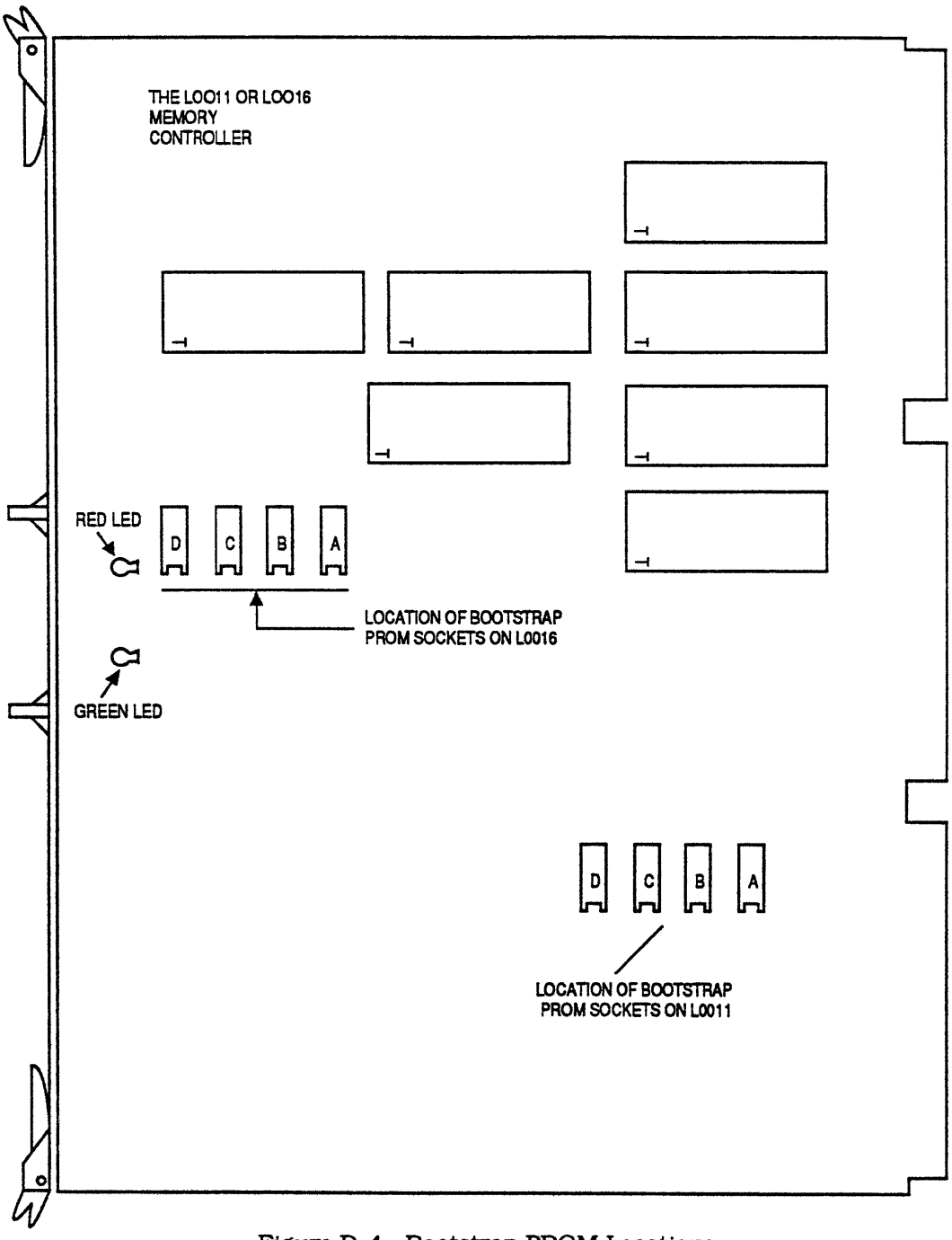


Figure D-4. Bootstrap PROM Locations

3. Plug the bootstrap PROM into any empty socket location, being sure that pin 1 of the PROM is in the proper position. If there are no empty sockets, remove one of the existing bootstrap PROMS to boot the controller from a PROM. The controller can be booted indirectly using the TU58 if desired, but the procedure is slow, and automatic reboot will not occur after a system crash.

CAUTION

The TU58 boot PROM is necessary to boot the diagnostic cartridges and must NOT be removed. This prom is usually installed in location A.

4. Attach the black and orange WARNING label that comes with the installation package to the edge of the L0011/L0016 module. The label measures about 2 3/8 by 4 inches, is highly visible, and ensures that the CPU service engineer will remove the controller boot PROM when the memory controller board is replaced. Replace the module in slot 10 of the CPU.
5. Replace the front and rear CPU card cage covers and close the CPU doors.
6. Reconnect the AC power.
7. Turn on the CBI contact breaker on the CPU power controller panel.
8. Turn the CPU front panel power-on action switch to HALT and turn the key switch to LOCAL.
9. Verify that the CPU powers-up. The following message should appear on the console screen:

```
%%  0000000  16
```

10. Spin up the disks and ask the system manager to bring up the operating system.

APPENDIX E
BI BUS CPA INSTALLATION

E.1 BI Bus CPA Jumpers and Node IDs

Each device connected to the VAX BI bus has a unique address defined by a node number. This node number is normally specified for each device by a node number plug, found on the back of the BI backplane immediately above each device slot. Numbers range from 0 to 15, and do not necessarily have to be in numerical sequence. Generally, there are more node numbers available than devices. The BI Bus CPA jumper positions and node IDs are shown in Table E-1.

NOTE

Only when the node number plug is not available for use is it necessary to define the node number by using the optional jumper plugs located on jumper bank W8 of the BI bus CPA, otherwise no jumper plugs should be located at W8.

Table E-1. CPA For BI Bus Node ID Settings

JUMPER PLUG SETTING				
W8-1	**W8-2**	**W8-3**	**W8-4**	**VAXBI NODE ID**
OUT	OUT	OUT	OUT	F hex (factory setting)
IN	OUT	OUT	OUT	E hex
OUT	IN	OUT	OUT	D hex
IN	IN	OUT	OUT	C hex
OUT	OUT	IN	OUT	B hex
IN	OUT	IN	OUT	A hex
OUT	IN	IN	OUT	9 hex
IN	IN	IN	OUT	8 hex
OUT	OUT	OUT	IN	7 hex
IN	OUT	OUT	IN	6 hex
OUT	IN	OUT	IN	5 hex
IN	IN	OUT	IN	4 hex
OUT	OUT	IN	IN	3 hex
IN	OUT	IN	IN	2 hex
OUT	IN	IN	IN	1 hex
IN	IN	IN	IN	0 hex

E.2 BI Bus CPA (SCSI Initiator) ID Selection

Each device (initiator or target) on the SCSI bus requires a unique SCSI identification address (0 — 7). SCSI ID 7 has the highest priority on the bus and SCSI ID 0 has the lowest priority. The host adapter is factory-configured to SCSI ID 7. To alter the host adapter SCSI ID, users need to change the NOVRAM setting through the on-board RS-232 utility. The SCSI IDs, settings and functions of the BI Bus CPA are listed in Table E-2. The block diagram of all BI Bus CPA LEDs and jumper banks are shown in Figure E-1.

NOTE

The connection path (computer interconnect cable) between the BI Bus CPA and the CLUSTOR CI/M board uses SCSI protocol. This does **not** indicate support for SCSI disk drives.

Table E-2. CPA for BI Bus SCSI ID Settings

JUMPER	SETTING	FUNCTION
W1	OUT	Single-ended SCSI channel terminator power disabled
W2, W4	All OUT	Differential SCSI configuration
W3	1 — 2 IN	Differential mode power protection circuit enabled
W5	OUT	SCSI controller chip's differential mode enabled
W6	OUT	Reserved
W7 — 1 W7 — 2	OUT IN	Disable Tape Support
W9	OUT	+5V for passive front panel disconnected (F)*
W10	IN	Differential SCSI channel terminator power enabled (F)*

* F denotes factory setting

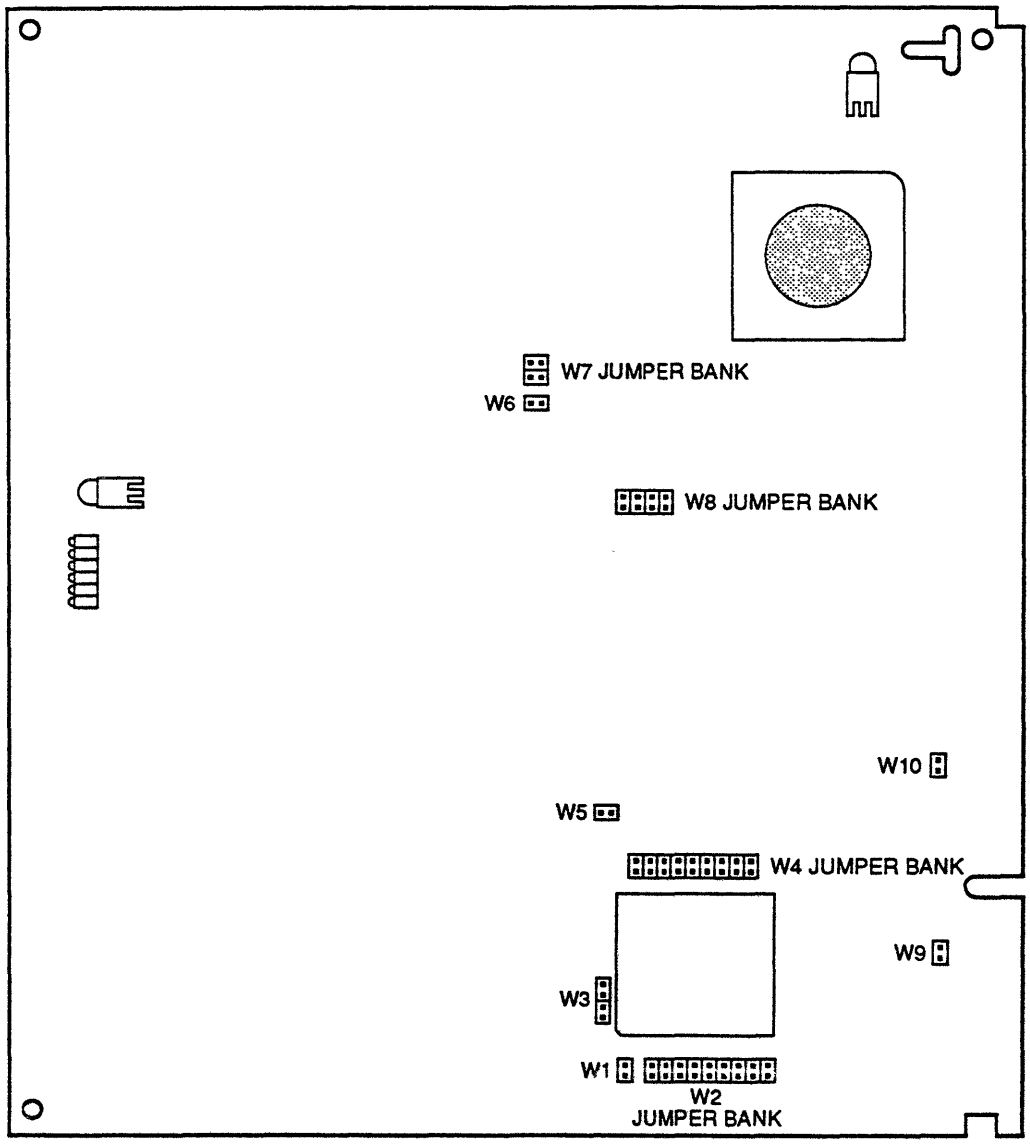


Figure E-1. BI Bus CPA Jumper Block Diagram

E.3 LED Indicators

The BI Bus CPA board has seven LEDs on the front edge and one yellow LED in the VAXBI corner area. The LEDs and indications are listed in Table E-3 and shown in Figure E-2.

Table E-3. BI Bus CPA LED Indications

LED	COLOR	INDICATION
D3	Red	Error condition occurred.
D2	Green	Power-up OK and activity indicator. Upon power-up, this LED is lit when the BI Bus CPA succeeds in the self-diagnostic testing. During normal controller operation, this LED blinks to show controller activity.
D5	Green	SCSI controller chip single-ended mode enabled.
D1	Green	JE single-ended terminator power pin is supplied with power.
D6	Green	SCSI controller chip Differential mode enabled.
D4	Green	JD differential terminator power pins are supplied with power.
Yellow LED		Self-test passed
Yellow LED (in VAXBI corner)		Also indicates self-test passed.

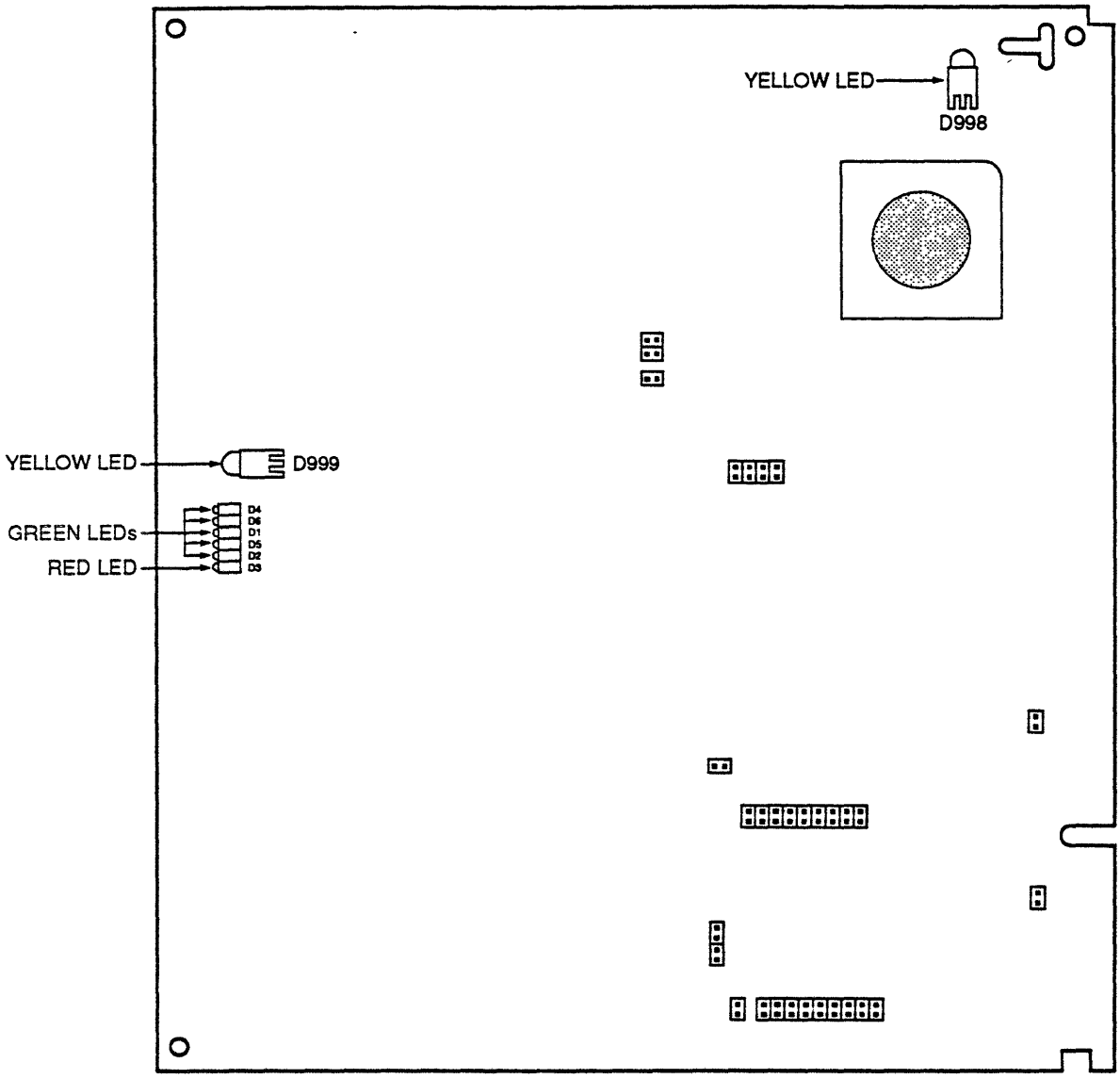


Figure E-2. BI Bus CPA LEDs, Front View

E.4 SCSI Bus Cabling

The VAXBI systems provide two 30-pin connectors in the backplane for every one of the VAXBI Zero Insertion Force (ZIF) connectors JC, JD, and JE. The 30-pin connector on the component side of the BI Bus CPA is defined as connector CON1. The 30-pin connector on the solder side of the BI Bus CPA is defined as connector CON2.

The term "VAXBI connector" will be used to refer to either the ZIF connector of the BI Bus CPA or the corresponding VAXBI backplane connector. The BI Bus CPA ZIF connectors are shown in Figure E-3. The backplane connectors are shown in Figure E-4.

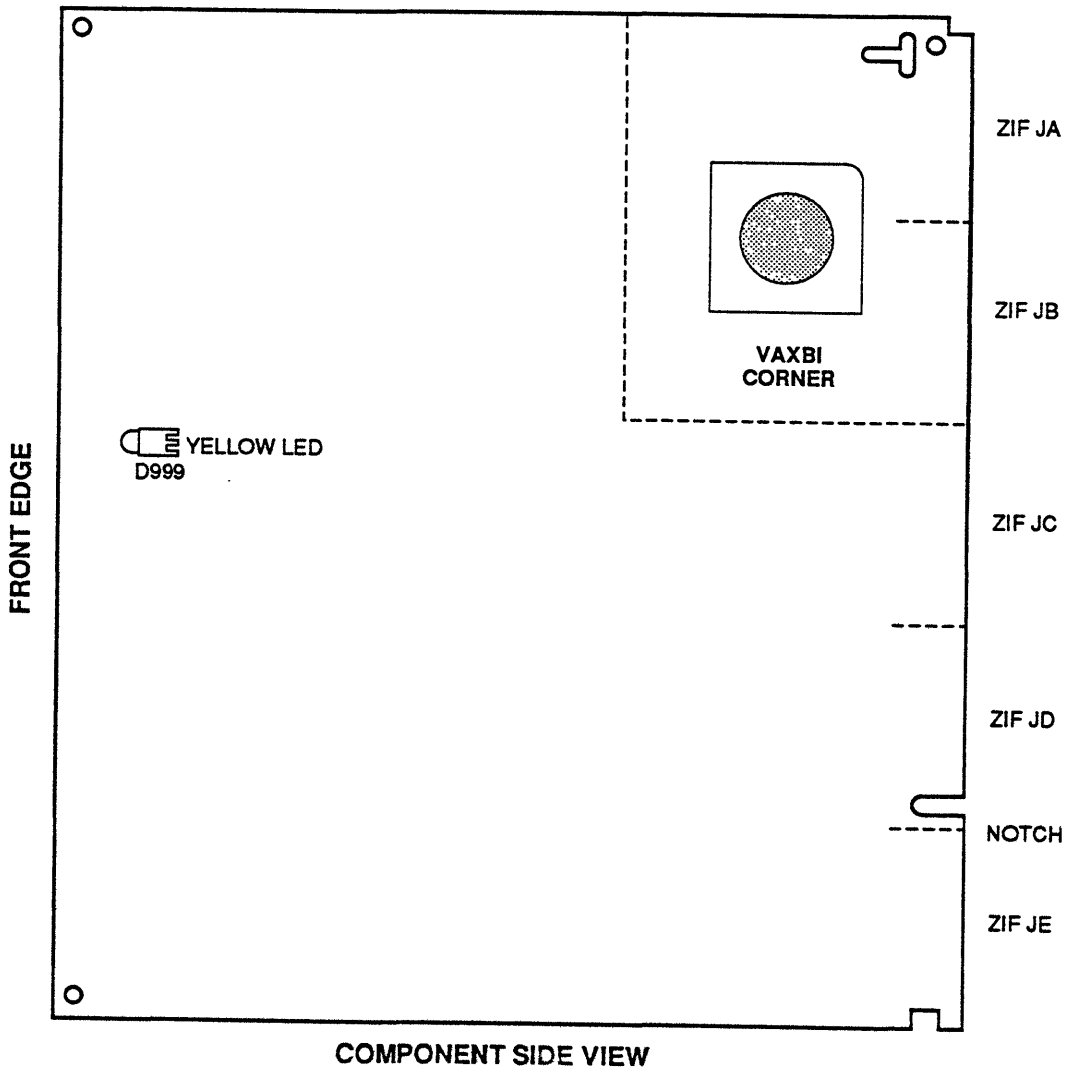


Figure E-3. BI Bus CPA ZIF Connectors

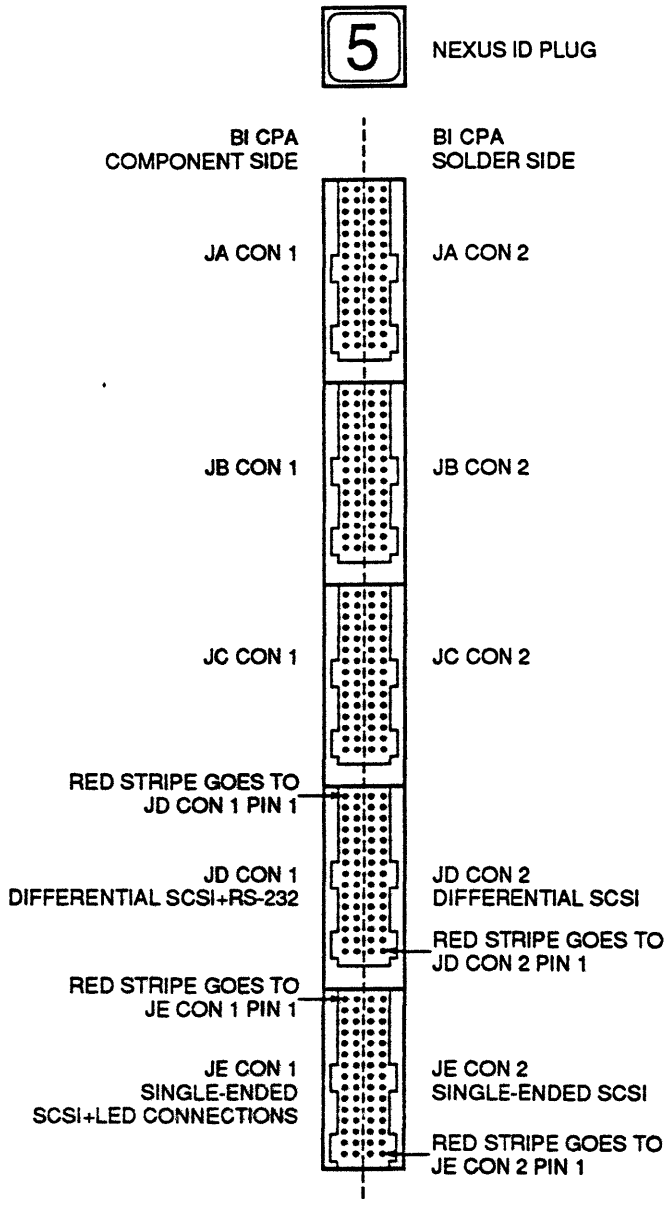


Figure E-4. BI Bus Backplane Connector (rear view)

The BI Bus CPA comes with two 8-foot SCSI I/O cables (including RS-232 utility and user front-panel interface) and system back panel adapter kit. Each SCSI I/O cable includes 60-conductor cable, two 30-pin socket connectors, one 50-pin SCSI connector, and a 10-pin socket connector. The RS-232 utility signals are designed in VAXBI Zero Insertion Force (ZIF) connector JD and the user front panel interface signals are designed in VAXBI ZIF connector JE.

One I/O cable is used for differential SCSI, the other is used for single-ended SCSI. Only one SCSI cable can be active in any particular configuration.

NOTE

Pin 1 of the SCSI I/O cable **must** match pin 1 of VAXBI connector CON1.

One SCSI I/O cable can be connected to the VAXBI backplane connector (JD) for differential SCSI devices. The 10-pin socket connector of this SCSI I/O cable carries RS-232 utility signals; it should be connected to the corresponding 10-pin RS-232 connector (J1) on the back panel adapter kit.

The other SCSI I/O cable can be connected to the VAXBI backplane connector (JE) for single-ended SCSI devices. The back panel adapter kit is shown in Figure E-4.

E.5 Differential SCSI Channel

The BI Bus CPA host adapter provides differential SCSI signals through the Zero Insertion Force (ZIF) connector JD to interface with external differential SCSI devices.

When the BI Bus CPA and the external SCSI devices are installed in one cabinet which meets EMI/RFI shielding requirements, a 50-conductor flat cable or 25-signal twisted-pair cable can be used for connecting the BI Bus CPA (JD) and the external SCSI devices. When the BI Bus CPA and the external SCSI devices are installed in separate cabinets, the shielded SCSI cable should be used to meet FCC requirements.

Every differential signal pair should be terminated with a 330 ohm resistor between the negative signal and +5 volts, 330 ohms between the positive signal and ground, and 150 ohms between the positive and the negative signal at each end of the SCSI cable. The BI Bus CPA provides on-board removable terminators (U89, U90) which are above the ZIF connector JD. Therefore, the BI Bus CPA can be installed in any location on the SCSI bus. If the BI Bus CPA is installed at either end of the SCSI cable, the on-board SCSI bus terminators should remain on the board. Otherwise, the on-board SCSI bus terminators should be removed.

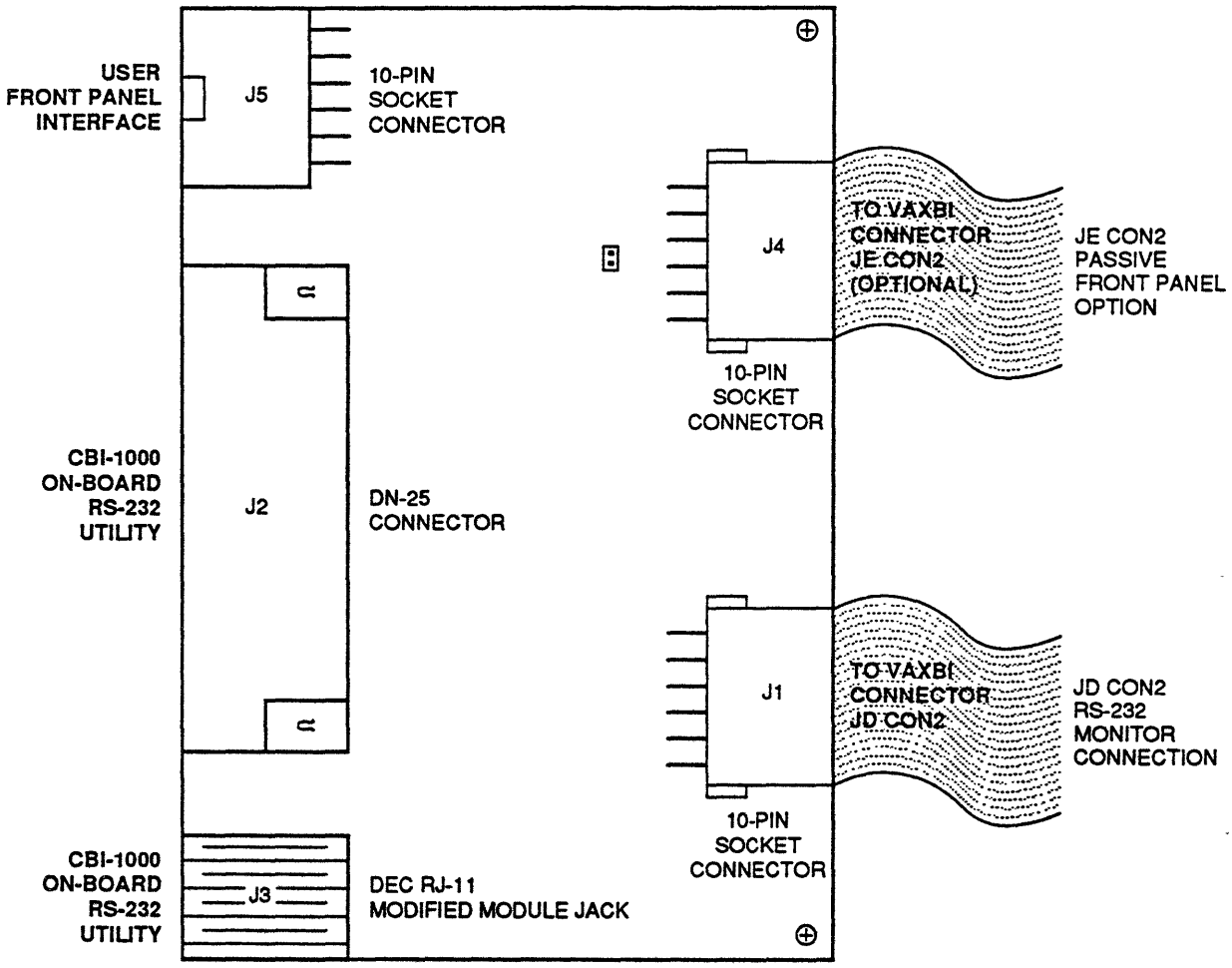


Figure E-5. Back Panel Adapter Kit

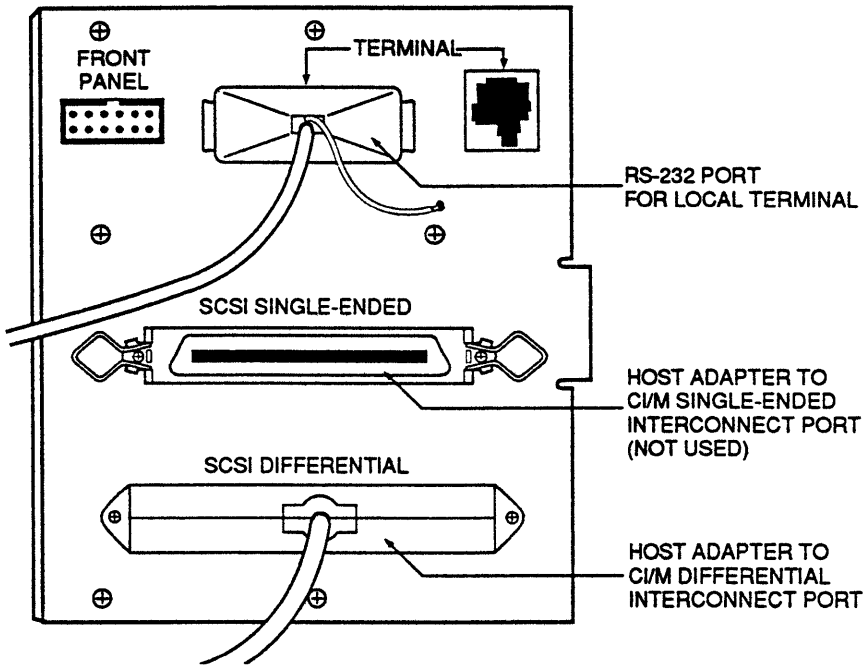


Figure E-6. Host Transition Panel

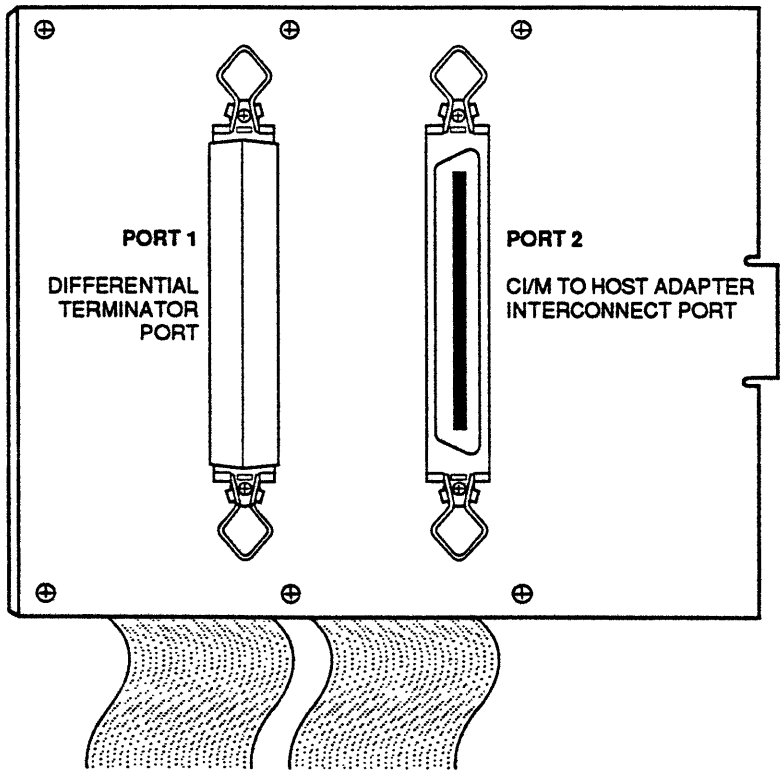


Figure E-7. CI/M Transition Panel Assembly

E.6 RS-232 Utility for BI Bus CPA

This is a general purpose on-board utility for any DEC system with VAXBI. To access the RS-232 utility, the user needs to connect a terminal and cable to the BI Bus CPA's RS-232 port (DB-25 connector or DEC-compatible RJ-11/Modified Module 423 Jack connector of the back panel adapter kit), and set the terminal baud rate to 9600 (8-bit data, no parity). Then press the system reset switch and hit carriage return on the terminal connected to the BI Bus CPA's RS-232 port. The main menu will be displayed automatically on this terminal.

Once the main utility menu appears, the user can key in the number or letter and carriage return to select the desired option. Press BREAK or CONTROL C at any time to reset the SCSI bus and return to the main menu.

The main menu of the utility will display:

```
SCSI HOST ADAPTER UTILITY (REV. XX)

[DISK]                                  [TAPE]
1 = LOGICAL UNIT NUMBER OFFSET          6 = LOGICAL UNIT NUMBER OFFSET
2 = FORMAT DRIVE                        7 = ADDITIONAL UTILITIES
3 = QUALIFY DRIVE
4 = MANUALLY REPLACE BAD BLOCKS
5 = ADDITIONAL UTILITIES

SELECT OPTION      ?
```

NOTE

Options 6 and 7 are tape functions and are **not** supported on CLUSTOR/M.

Disk Options

Option 1: Logical Unit Number Offset

This option is not used.

Option 2: Format Drive

The Format command is not supported by the SCSI CI.

Option 3: Qualify Drive

This utility is not supported by the SCSI CI. CLUSTOR/M does not support automatic bad block replacement.

Option 4: Manually Replace Bad Blocks

This utility is not supported by CLUSTOR/M.

Option 5: Additional Utilities

If option 5/Additional Utilities is selected, the following sub-menu will be displayed:

```
ADDITIONAL UTILITIES          (REV. XX)          SN = XXXX

D = DISPLAY SCSI DEVICE AND SET UP CONFIGURATION
S = SEND SCSI COMMAND TO THE DEVICE
T = TEST SCSI DEVICE
R = FORMAT RCT BLOCK

SELECT OPTION      ?
```

Display SCSI Device and Set Up Configuration

Selection D can be used to change the controller default configurations, such as:

- number of disk devices supported
- SCSI ID of the BI Bus CPA
- SCSI ID LUN assignment
- SCSI reset enable/disable
- SCSI disconnect enable/disable
- sync/async mode selection
- prevent medium removal enable/disable
- disk write with verify enable/disable
- scan/display SCSI devices attached to the BI Bus CPA.

The BI Bus CPA is shown in the following display example.

```
ADDITIONAL UTILITIES          (REV. XX)          SN = XXXX

D = DISPLAY SCSI DEVICE AND SET UP CONFIGURATION
S = SEND SCSI COMMAND TO THE DEVICE
T = TEST SCSI DEVICE
R = FORMAT RCT BLOCK

SELECT OPTION    ?    D<ret>

Current Configuration:

DEV0:        DU0, SCSI ID 0, LUN 0
             Disconnect ON, Sync MOde ON, Prevent Medium Removal ON,
             Write W/Verify OFF

DEV1:        DU1, SCSI ID 1, LUN 0
             Disconnect ON, Sync MOde ON, Prevent Medium Removal ON,
             Write W/Verify OFF

DEV2:        DU2, SCSI ID 2, LUN 0
             Disconnect ON, Sync MOde ON, Prevent Medium Removal ON,
             Write W/Verify OFF

DEV3:        DU3, SCSI ID 3, LUN 0
             Disconnect ON, Sync MOde ON, Prevent Medium Removal ON,
             Write W/Verify OFF

DEV4:        DU4, SCSI ID 4, LUN 0
             Disconnect ON, Sync MOde ON, Prevent Medium Removal ON,
             Write W/Verify OFF

DEV5:        DU5, SCSI ID 5, LUN 0
             Disconnect ON, Sync MOde ON, Prevent Medium Removal ON,
             Write W/Verify OFF
```

```
DEV6:          DU6, SCSI ID 6, LUN 0
               Disconnect ON, Sync MOde ON, Prevent Medium Removal ON,
               Write W/Verify OFF

DEV7:          SCSI ID 7, Host Adapter
               SCSI Reset ON, TMU OFF, Fast Search OFF

Change Configuration    ?    (Y/N)    Y<ret>

R = Toggle SCSI Reset                  P = Toggle Prevent Medium Removal
D = Toggle Disconnect                  B = Toggle Buffer Mode (Tape only)
S = Toggle Sync/Async                  W = Toggle Write W/Verify (Disk only)
C = Reconfigure Device                 T = Reset All Devices Mode to Default
M = Toggle TMU                         F = Toggle Fast File Search (Tape only)
```

To change the BI Bus CPA SCSI host adapter ID, the user can select option C, and the utility will display:

```
Enter Initiator ID                          7<ret>
Number of Disks? (0 — 7)                    7<ret>
    DU0 to be Reconfigured    ?    (Y/N)    N<ret>
    DU1 to be Reconfigured    ?    (Y/N)    N<ret>
    DU2 to be Reconfigured    ?    (Y/N)    N<ret>
    DU3 to be Reconfigured    ?    (Y/N)    N<ret>
    DU4 to be Reconfigured    ?    (Y/N)    N<ret>
    DU5 to be Reconfigured    ?    (Y/N)    N<ret>
    DU6 to be Reconfigured    ?    (Y/N)    N<ret>
```

The utility will display the current configuration of DEV0 to DEV7 after the last reconfiguration is made.

Send SCSI Command to the Device

Selection S from the Additional Utilities sub-menu can be used to send generic SCSI commands to the selected disk/tape drives directly.

Test SCSI Device

Selection T from the Additional Utilities sub-menu can be used to either read or write/read/verify the selected disk/tape drive continuously.

Format RCT Block

Selection R from the Additional Utilities sub-menu can be used to format the RCT blocks of the disk drive selected.

NOTE

Format RCT Block must be run on all logical disk drives attached to CLUSTOR/M prior to VMS volume initialization. This is normally performed in the factory before shipment.

APPENDIX F
QBUS CPA/M INSTALLATION

F.1 VMS Considerations

The first step to install the Qbus CPA/M host adapter under the VMS operating system is to determine the Control and Status Register (CSR) address of the Qbus CPA/M. The following procedure shows one method of determining the new CSR address of the Qbus CPA/M.

CAUTION

Do not install the Qbus CPA/M in the system until the CSR address is determined.

Qbus CPA/M CSR Address

1. First, boot the VMS system and log into the system manager account. At the DCL $ prompt, enter: **MC SYSGEN**
2. At the SYSGEN> prompt, enter: **SHOW/CONFIG**

   The SYSGEN utility will display all the device controllers installed in the system and their corresponding CSR addresses and vectors. Make a note of the list.

3. At the SYSGEN> prompt, enter: **CONFIG**
4. At the DEVICE> prompt, for Qbus CPA/M, enter: **UDA X**

   X is the number of installed UDA-type controllers plus 1 (for the new one being added).

5. At the DEVICE> prompt, enter **CTRL Z**

   The SYSGEN utility will display the CSR addresses for all the controllers. The VMS mnemonic for the MSCP disk controllers are PUA, PUB, PUC, etc. The VMS mnemonic for the TMSCP tape controllers are PTA, PTB, PTC, etc. Use the corresponding CSR address to configure the CSR jumper settings of the Qbus CPA/M.

6. At the SYSGEN> prompt, enter **CTRL Z** to exit the SYSGEN utility.

NOTE

The Qbus CPA/M will automatically program the on-board interrupt vector to match the vector assigned by the system. The vectors of other controllers might change when the Qbus CPA/M is added to the system.

An example of the SYSGEN utility procedure is provided for installing the Qbus CPA/M.

```
$ MC SYSGEN
SYSGEN>  SHOW/CONFIG
System CSR and VECTOR on 2-JUN-1989      04:10:43.30
Name:  PUA  Units:1   Nexus:0  (UBA)   CSR:772150   Vector:774   Vector2:0
Name:  PTA  Units:1   Nexus:0  (UBA)   CSR:774500   Vector:260   Vector2:0
Name:  PUB  Units:1   Nexus:0  (UBA)   CSR:760334   Vector:300   Vector2:0
SYSGEN>  CONFIG
DEVICE>  UDA 3
DEVICE>  TU81 2
DEVICE>  ^Z
Device:  UDA   Name:  PUA   CSR:  772150   Vector:154   Support: Y
Device:  TU81  Name:  PTA   CSR:  774500   Vector:260   Support: Y
Device:  UDA   Name:  PUB   CSR:  760334*  Vector:300*  Support: Y
Device:  UDA   Name:  PUC   CSR:  760340*  Vector:304*  Support: Y
Device:  TU81  Name:  PTB   CSR:  760444*  Vector:310*  Support: Y
SYSGEN>  ^Z
$
```

In this example, the CSR address of PUC should be used to configure the CSR jumpers of the Qbus CPA/M.

F.2 Jumper Settings

Normally, the user **need not change** the factory jumper settings of the Qbus CPA/M **except** the CSR address switch SW1 and SCSI terminator power option jumper W1 and W3.

CSR Address Selection

The Qbus CPA/M has jumpers to select different CSR addresses. Select the desired address by installing the jumper plugs. The standard CSR addresses for the Qbus

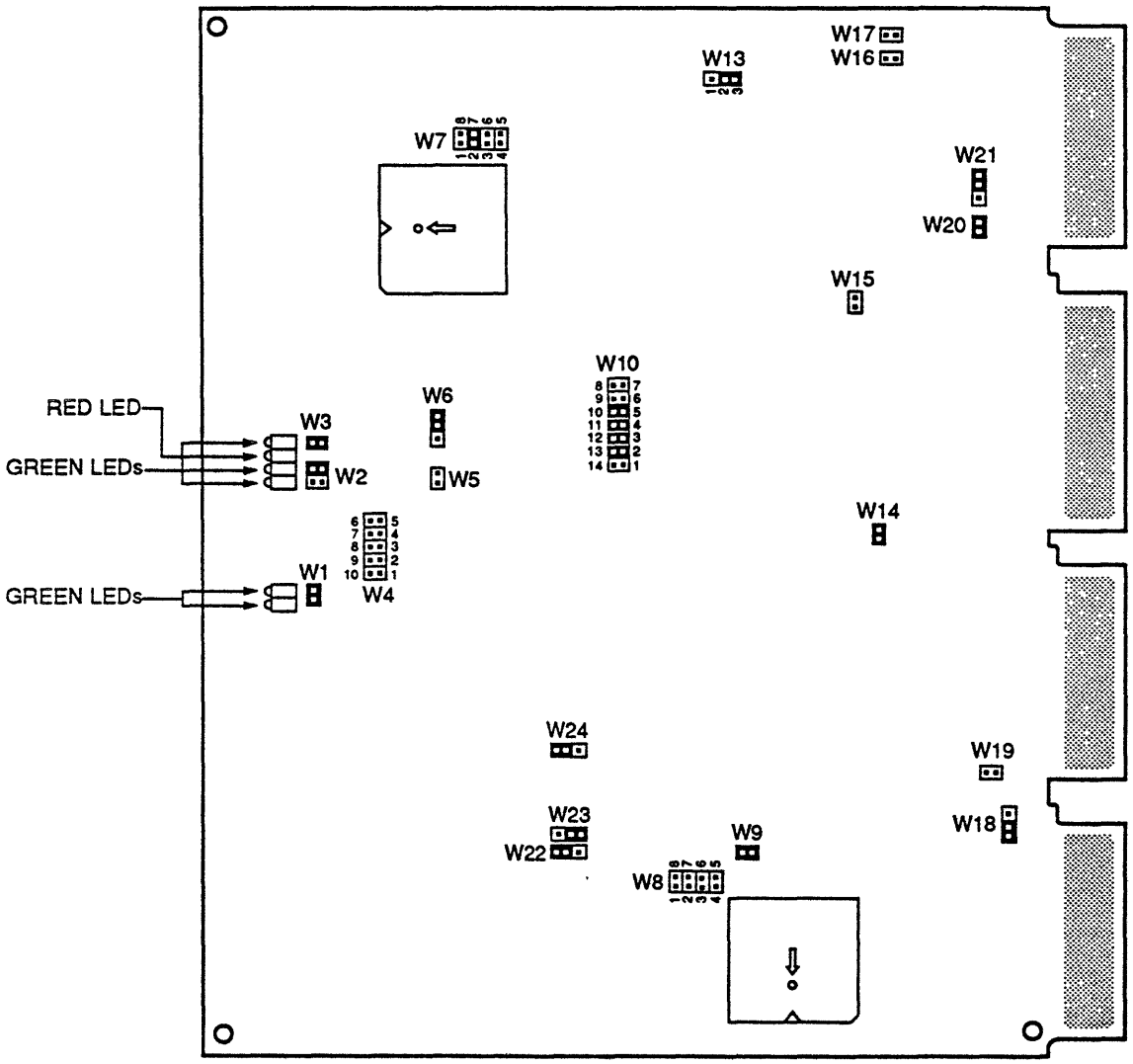


Figure F-1. MSCP Qbus CPA/M Jumper and LED Locations

NOTE

SW1-6, SW1-7, SW1-8, SW1-9, and SW1-10 **must** be set to the OFF position in order to disable tape.

The Qbus CPA/M supports 30 disk CSR addresses. Qbus CPA/M CSR addresses and switch settings are shown in the Table F-1.

Table F-1. Qbus CPA/M CSR Addresses

ADDRESS	LSI-11	MICROVAX	SW 1-1	SW 1-2	SW 1-3	SW 1-4	SW 1-5
1	17772150	20001468	ON	ON	ON	ON	ON
2	17760334	200000DC	ON	ON	ON	ON	OFF
3	17760354	200000EC	ON	ON	ON	OFF	ON
4	17760374	200000FC	ON	ON	ON	OFF	OFF
5	17760340	200000E0	ON	ON	OFF	ON	ON
6	17760344	200000E4	ON	ON	OFF	ON	OFF
7	17760350	200000E8	ON	ON	OFF	OFF	ON
8	17760360	200000F0	ON	ON	OFF	OFF	OFF
9	17760364	200000F4	ON	OFF	ON	ON	ON
10	17760370	200000F8	ON	OFF	ON	ON	OFF
11	17760400	20000100	ON	OFF	ON	OFF	ON
12	17760404	20000104	ON	OFF	ON	OFF	OFF
13	17760410	20000108	ON	OFF	OFF	ON	ON
14	17760414	2000010C	ON	OFF	OFF	ON	OFF
15	17760420	20000110	ON	OFF	OFF	OFF	ON
16	17760424	20000114	ON	OFF	OFF	OFF	OFF
17	17760430	20000118	OFF	ON	ON	ON	ON
18	17760434	2000011C	OFF	ON	ON	ON	OFF
19	17760440	20000120	OFF	ON	ON	OFF	ON
20	17760444	20000124	OFF	ON	ON	OFF	OFF
21	17760450	20000128	OFF	ON	OFF	ON	ON
22	17760454	2000012C	OFF	ON	OFF	ON	OFF
23	17760460	20000130	OFF	ON	OFF	OFF	ON
24	17760464	20000134	OFF	ON	OFF	OFF	OFF
25	17760470	20000138	OFF	OFF	ON	ON	ON
26	17760474	2000013C	OFF	OFF	ON	ON	OFF
27	17760500	20000140	OFF	OFF	ON	OFF	ON
28	17760504	20000144	OFF	OFF	ON	OFF	OFF
29	17760510	20000148	OFF	OFF	OFF	ON	ON
30	17760514	2000014C	OFF	OFF	OFF	ON	OFF
31	disable disk		OFF	OFF	OFF	OFF	OFF

Interrupt Level Selection

The Qbus CPA/M is shipped with interrupt level 4 selected. This is the standard interrupt priority for MSCP devices. The Qbus CPA/M may be jumper selected to interrupt at level 5. Jumper block locations are shown in Figure F-1.

W21	1 — 2	IN	Interrupt level 5
	2 — 3	IN	Interrupt level 4 (factory)

Block Mode DMA

In a block mode Direct Memory Access (DMA) transfer, the starting memory address is asserted, followed by data for that address, and data for consecutive addresses. Because the assertion of the address for each data word is eliminated, higher data throughput can be achieved. The Qbus CPA/M is shipped with block mode DMA enabled, with jumper shunt in W18 pin 1 and 2.

W18	1 — 2	IN	Block mode DMA enabled (factory)
	2 — 3	IN	Block mode DMA disabled

Adaptive DMA

When the adaptive DMA is enabled, the Qbus CPA/M will release the Qbus after eight words transfer if other DMA devices assert DMA request. Otherwise, the Qbus CPA/M will continue the DMA transfer for an additional eight words, then release the Qbus. The Qbus CPA/M is shipped with adaptive DMA disabled.

W19	IN	Adaptive DMA enabled
	OUT	Adaptive DMA disabled (factory)

DMA Dwell Time

If multiple DMA data transfers are performed, consideration must be given to the use of the Qbus for other system functions, such as communication multiplexer, network, etc. The Qbus CPA/M inserts DMA dwell time in between DMA data transfers. During the DMA dwell time, the Qbus CPA/M will not arbitrate for the use of the Qbus. The user can select the period of the DMA dwell time by changing the jumper W7. The default setting is W7-2 IN (4.8 uS dwell time).

W7-3	IN	1.2 uS DMA dwell time
W7-4	IN	2.4 uS DMA dwell time
W7-2	IN	4.8 uS DMA dwell time (factory)
W7-1	IN	9.6 uS DMA dwell time

SCSI Host Adapter (Initiator) ID Selection

Each device (Initiator or Target) on the SCSI bus requires a unique SCSI Identification address (0 — 7). SCSI ID 7 has the highest priority on the bus and SCSI ID 0 has the lowest priority. The Qbus CPA/M SCSI Host Adapter is factory configured to SCSI ID 7. To alter the Host Adapter SCSI ID, users need to change jumper setting of W10-3, W10-4, and W10-5.

W10-3	W10-4	W10-5		
IN	IN	IN	Host adapter ID = 7,	highest priority (f)
IN	IN	OUT	Host adapter ID = 6	
IN	OUT	IN	Host adapter ID = 5	
IN	OUT	OUT	Host adapter ID = 4	
OUT	IN	IN	Host adapter ID = 3	
OUT	IN	OUT	Host adapter ID = 2	
OUT	OUT	IN	Host adapter ID = 1	
OUT	OUT	OUT	Host adapter ID = 0,	lowest priority

Single-Ended or Differential Mode Selection

The Qbus CPA/M SCSI port comes with both single-ended and differential SCSI drivers and receivers. A jumper W2 is available for users to select the channel. When a jumper shunt is installed in the W2 pin, 1-3 location, single-ended SCSI drivers and receivers are enabled and the DS1 right green LED will be on.

NOTE

Single-ended SCSI devices should be connected to the J2 connector.

When a jumper shunt is installed in the W2 pin, 2-4 location, the differential drivers and receivers are enabled and the DS2 second-left green LED will be on.

NOTE

Differential SCSI devices should be connected to the J1 connector. The factory setting is W2 2-4 IN (differential enabled).

SCSI Terminator Power Option

When the power of the SCSI device with the SCSI terminator is turned off, the SCSI signals will be pulled down unless the terminator is powered by another SCSI device, typically an initiator (SCSI host adapter). For the same reason, when an external SCSI terminator (single-ended or differential) is installed at the other end of the SCSI cable, the terminator power option of the Qbus CPA/M needs to be enabled.

NOTE

Anytime an external SCSI terminator (instead of the on-drive SCSI terminator) is used, the SCSI terminator power option of the Qbus CPA/M has to be enabled, i.e. install jumper shunt. Remember to **turn off** the power of the system and SCSI devices while installing the SCSI cable and terminator.

The Qbus CPA/M supplies terminator power to the TERMPWR pin (pin 26) of single-ended SCSI connector (J2) through a fuse, a diode and jumper block W3. In order to prevent accidental grounding or misconnection of terminator power, make sure the pin 1 mark of the SCSI cable matches with the pin 1 mark of the SCSI device's connector before turning on the power.

W3	IN	1st single-ended SCSI channel terminator power enabled (f)
W3	OUT	1st single-ended SCSI channel terminator power disabled

The Qbus CPA/M also supplies terminator power to the TERMPWR pins (pin 25 and 26) of differential SCSI connector (J1) through a diode, a fuse and jumper block W1 for external SCSI drives. In order to prevent accidental grounding or misconnection of terminator power, make sure the pin 1 mark of the SCSI cable matches the pin 1 mark of the SCSI device's connector before turning the system power on.

W1	IN	Differential SCSI channel terminator power enabled (f)
W1	OUT	Differential SCSI channel terminator power disabled

Sync/Async Mode Selection

In general, the Sync/Async Mode for each individual drive can be selected through the on-board utility individually. The default setting is asynchronous mode.

In sync mode, the Qbus CPA/M will automatically communicate with the SCSI device to find out if the sync mode is possible, or if only the async mode is supported by the device. Then it will switch mode automatically.

CAUTION

For those devices which **do not** support this communication, async mode should be used to insure proper operation.

The following jumpers control the overall Sync/Async mode selection and will override the on-board utility sync mode set-up.

W10-2	IN	Disk sync mode disabled (factory)
	OUT	Disk sync mode enabled

The Qbus CPA/M jumper settings are listed in Table F-2.

Table F-2. Qbus CPA/M Jumper Settings

JUMPER	SETTING			DESCRIPTION
W1		IN		Differential SCSI channel terminator power enabled*
		OUT		Differential SCSI channel terminator power disabled
W2	1-3	IN		Single-ended SCSI channel enabled*
	2-4	IN		Differential channel enabled
W3		IN		Single-ended SCSI channel terminator power enabled (f)
		OUT		Single-ended SCSI channel terminator power disabled
W4	1-5	IN		Front panel interface enabled
W5		IN		
W4	1-5	OUT		Front panel interface disabled*
W5		OUT		
W6	1-2	IN		Reserved
	2-3	IN		RS-232 transmit enabled*
W7-1		IN		9.6 uS DMA dwell time
W7-2		IN		4.8 uS DMA dwell time*
W7-3		IN		1.2 uS DMA dwell time
W7-4		IN		2.4 uS DMA dwell time
W8-1 to W8-3		OUT		Reserved*
W9	1-2	IN		Reserved*
W10 — QBUS CPA/M SCSI PORT SETUP				
W10-1	IN			Tape sync mode disabled
	OUT			Tape sync mode enabled*
W10-2	IN			Disk sync mode disabled*
	OUT			Disk sync mode enabled
W10-3,	W10-3	W10-4	W10-5	
W10-4,	IN	IN	IN	Host adapter ID = 7 highest priority*
W10-5	IN	IN	OUT	Host adapter ID = 6
	IN	OUT	IN	Host adapter ID = 5
	IN	OUT	OUT	Host adapter ID = 4
	OUT	IN	IN	Host adapter ID = 3
	OUT	IN	OUT	Host adapter ID = 2
	OUT	OUT	IN	Host adapter ID = 1
	OUT	OUT	OUT	Host adapter ID = 0 lowest priority

* Factory setting
† Rev. C only

Table F-2. Qbus CPA/M Jumper Settings (continued)

JUMPER	SETTING		DESCRIPTION
W10-6		IN	Enable tape fast-search option
		OUT	Normal operation*
W10-7		IN	Tape Monitor Utility (TMU) enabled Disk SCSI format ON-LINE (FMT) enabled
		OUT	TMU disabled* FMT disabled*
W11, W12		OUT	Reserved*
W13	1-2	IN	Auto-boot enabled
	2-3	IN	Auto-boot disabled*
W14		IN	Bootstrap address 773000*
		OUT	Bootstrap address 771000
W15, W16, W17		OUT	Reserved*
W18	1-2	IN	Block-mode DMA enabled*
	2-3	IN	Block-mode DMA disabled
W19		IN	Adaptive DMA enabled
		OUT	Adaptive DMA disabled*
W20		IN	22-Bit addressing*
		OUT	18-Bit addressing
W21	1-2	IN	Interrupt level 5
	2-3	IN	Interrupt level 4*
W22	1-2	IN	Reserved*†
W23	1-2	IN	Reserved*†
W24	1-2	IN	Reserved*†
W25		OUT	Reserved*†

* Factory setting
† Rev. C only

F.3 Mounting Slot Selection

The Qbus CPA/M can be installed in any priority on the standard MicroVAX Qbus backplane as long as the Qbus interrupt acknowledge/DMA grant daisy-chain is not broken.

F.4 LED Indicators

The Qbus CPA/M has 2 LED modules in the front of the board. The LED module contains either four or two LEDs. The LED modules are labeled DS1 and DS2, and are labeled below and shown in Figure F-2.

LED	COLOR	INDICATION
DS1	green	Left LED. Power-up OK and activity indicator. On power-up, this LED is turned on when the Qbus CPA/M succeeds in the self-diagnostic testing. During normal controller operation, this LED blinks to show controller activity.
	red	Second-left LED. Error condition occurred.
	green	Third-left LED. J2 single-ended terminator power pin is supplied with power.
	green	Right LED. J2 single-ended SCSI channel enabled.
DS2	green	Left LED. J1 differential terminator power pins are supplied with power.
	green	Right LED. J1 differential SCSI channel enabled.

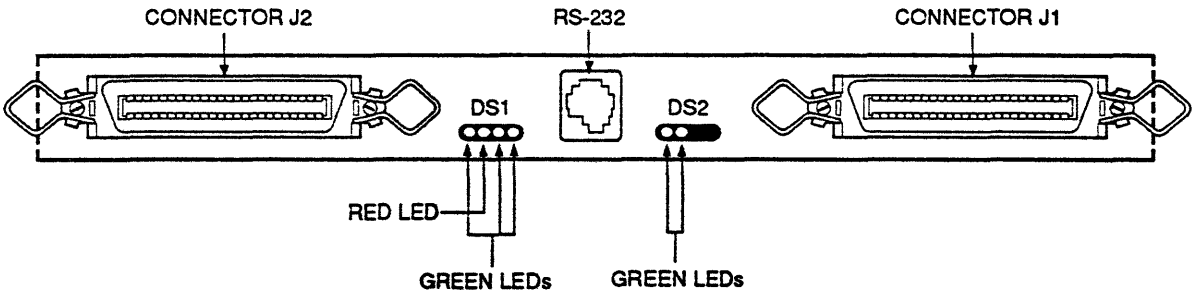


Figure F-2. Qbus CPA/M LEDs, Front View

F.5 SCSI Bus Cabling and Termination

Single-Ended SCSI Channel

The Qbus CPA/M host adapter provides a 50-pin connector (J2), to interface with external single-ended SCSI devices.

When the Qbus CPA/M and the SCSI devices are installed in the same cabinet which meets EMI/RFI shielding requirements, a 50-conductor flat cable or 25-signal twisted-pair cable can be used for connecting the Qbus CPA/M (J2) and the SCSI devices. When the Qbus CPA/M and the SCSI devices are installed in separated cabinets, the shielded SCSI cable should be used to meet the FCC requirements.

NOTE

Use a minimum conductor size of 28 AWG to minimize noise effects and ensure proper distribution of optional terminator power. The maximum cable length is 6 meters or 20 feet in single-ended channel.

The SCSI bus signals should be terminated with 220 ohms to +5 volts and 330 ohms to ground at each end of the cable. The Qbus CPA/M provides on-board removable terminators (RN9, RN10, RN11), which are next to the SCSI connector J2. Therefore, the Qbus CPA/M can be installed in any position of SCSI cable. If the Qbus CPA/M is installed in either end of the SCSI cable, the on-board terminators should remain on the board. Otherwise, the on-board terminators should be removed.

Differential SCSI Channel

The Qbus CPA/M also provides a 50-pin connector (J1), to interface with external differential SCSI devices.

When the Qbus CPA/M and the external SCSI devices are installed in the same cabinet, which meets EMI/RFI shielding requirements, a 50-conductor flat cable or 25-signal twisted-pair cable can be used for connecting the Qbus CPA/M (J1) and the external SCSI devices. When the Qbus CPA/M and the external SCSI devices are installed in separated cabinets, the shielded SCSI cable should be used to meet FCC requirements.

The Qbus CPA/M provides on-board removable terminators (RN1, RN2, RN3, RN4, RN5, RN6, RN7, RN8) which are next to the connector J1. Therefore, the Qbus CPA/M can be installed in any position of the SCSI cable. If the Qbus CPA/M is installed at either end of SCSI cable, the on-board SCSI bus terminators should remain on the board. Otherwise, the on-board SCSI bus terminators should be removed.

F.6 On-Board Utility

The Qbus CPA/M host adapter comes with four different on-board utilities which include the on-board utility for LSI-11 systems, the on-board utility for MicroVAX II, Micro 3X00 and VAX 4000 systems, the general purpose RS-232 utility for all systems, and the ODT utility. Because the formats and features of the on-board utilities for LSI-11 systems and MicroVAX systems are similar (except different start-up procedures), the MicroVAX utility only will be described.

Disk Utility for Qbus CPA/M

The Disk Utility Program provides a convenient way of formatting and configuring the drive. An example is given below:

VAX Systems

	Command	Indication
1.	Halt the CPU	
2.	>>> I <CR>	Initialize
3.	>>> U <CR>	Unlock
4.	>>> D/P/W 20001F40 20 <CR>	Enable Qbus memory access
5.	>>> D/L 20088008 80000002 <CR>	Set up Qbus map
6.	>>> D/W 2000146A A72E <CR>	Deposit to base CSR+2
7.	>>> D* 100 <CR>	Load utility to memory
8.	>>> S 400 <CR>	Start the utility

NOTE

The address shown in step 6 is equal to the CSR address (selected by the switch SW1-1 to SW1-5 of the Qbus CPA/M) plus 2.

The utility will display:

```
SCSI UTILITY PROGRAM

        Disk                    Tape

1   =   772150          A   =   774500
2   =   760334          B   =   760404
3   =   760354          C   =   760444
4   =   760374          D   =   760504
5   =   760340          E   =   760544
6   =   760344          F   =   760410
7   =   760350          G   =   760450
8   =   760360          H   =   760454

SELECT CSR ADDRESS
```

The user will then select the number which matches the CSR address Qbus CPA/M. The main menu will display:

```
1 = BOOT DRIVE
2 = CONFIGURE LUN OFFSET
3 = FORMAT DRIVE
4 = QUALIFY DRIVE
5 = MANUAL REPLACE BAD SECTORS
6 = READ, WRITE AND VERIFY TEST
7 = ADDITIONAL SCSI COMMANDS

SELECT OPTION :
```

The user now has seven options to choose from. If at any time the user types in a **<CTRL C>**, the command is aborted and the utility program returns to the main menu. If the user types in **<CR>** with no value, then the parameters will remain unchanged.

Configure LUN Offset

This option is not supported with CLUSTOR/M.

Format Drive

This option is not supported with CLUSTOR/M.

Qualify Drive

This option is not supported with CLUSTOR/M.

Manual Replace Bad Sectors

This option is not supported with CLUSTOR/M.

Read, Write and Verify Test

This option allows the user to test the integrity of the control board, drive cable and disk drive. The program will generate random data patterns for testing.

```
1 = BOOT DRIVE
2 = CONFIGURE LUN OFFSET
3 = FORMAT DRIVE
4 = QUALIFY DRIVE
5 = MANUAL REPLACE BAD SECTORS
6 = READ, WRITE AND VERIFY TEST
7 = ADDITIONAL SCSI COMMANDS

SELECT OPTION: 6
```

```
RANDOM READ WRITE TEST
DO YOU WANT READ ONLY     ?    <Y OR N>        N

DRIVE NUMBER <0 TO 6>:        0
***WILL DISTROY DATA ON THIS DRIVE, ARE YOU SURE?        Y

TEST FROM BLOCK     #     <0-XXXXX>     ?

TO BLOCK    #    <XXXXX-YYYYY>       ?

TESTING STARTED. TYPE CTRL-C TO ABORT.
```

Utility Bootstrap

To bootstrap the operating system on drive 0 to 6, select option 1 from the main menu.

```
1   =   BOOT DRIVE
2   =   CONFIGURE LUN OFFSET
3   =   FORMAT DRIVE
4   =   QUALIFY DRIVE
5   =   MANUAL REPLACE BAD SECTORS
6   =   READ, WRITE AND VERIFY TEST
7   =   ADDITIONAL SCSI COMMANDS

SELECT OPTION       :       1

BOOT DRIVE NUMBER       <0 TO 6>       0

BOOT DU0. ARE YOU SURE        ?       Y

WAIT    ...
```

Additional Utilities

The user can use this option to display the SCSI IDs of the attached SCSI devices, issue SCSI commands to the selected device, test SCSI devices and format the disk drive RCT (replacement and caching table) blocks. When this option is selected, the menu will display:

```
ADDITIONAL UTILITIES        (REV. XX)              SN = XXXX

    D = SETUP CONFIGURATION AND DISPLAY SCSI DEVICE
    S = SEND SCSI COMMAND TO THE DEVICE
    T = TEST SCSI DEVICE
    R = FORMAT RCT BLOCK

SELECT OPTION  ?
```

Selection "D" can be used to change the controller default configurations, such as the number of disk and tape devices supported, SCSI ID and SCSI LUN assignment, SCSI reset enable/disable, SCSI disconnect enable/disable, sync/async mode selection, tape buffer mode enable/disable, prevent medium removal enable/disable, disk write with verify enable/disable, etc. It will also scan/display the SCSI devices attached to the controller.

Selection "S" can be used to send generic SCSI commands to the selected disk/tape drives directly.

Selection "T" can be used to either read or write/read/verify the selected disk/tape drive continuously.

Selection "R" can be used to format the RCT blocks of the disk drive selected.

NOTE

Format RCT Block **must** be run on **all** logical disk drives attached to CLUSTOR/M prior to VMS volume initialization. This is normally performed in the factory before shipment.

F.7 RS-232 Utility for Qbus CPA/M

This is a general purpose on-board utility for any DEC system with Qbus. To access the RS-232 utility, the user needs to connect a terminal and cable to the Qbus CPA/M's RS-232 port (10-pin connector J1 of Qbus CPA/M), and set the terminal baud rate to 9600 (8-bit data, no parity). Halt the system, toggle the reset switch and hit carriage return **<CR>**. The main menu will be displayed automatically on the terminal.

Once the main utility menu shows up, the user can key in the number or letter and **<CR>** to select the desired option. Press **<BREAK>** or **<CTRL C>** at any time to reset the SCSI bus and return to the main menu.

NOTE

Pin 8 (receive data) of the Qbus CPA/M's RS-232 port is also used as a write-protect input for the front panel interface of the controller during normal operation. Remove the terminal cable from the RS-232 port after using the SCSI utility.

For the Qbus CPA/M, the main menu of the utility will display:

```
SCSI HOST ADAPTER UTILITY          (REV. XX)

    1  =  LOGICAL UNIT NUMBER OFFSET
    2  =  FORMAT DRIVE
    3  =  QUALIFY DRIVE
    4  =  MANUALLY REPLACE BAD BLOCKS
    5  =  ADDITIONAL UTILITIES

SELECT OPTION       ?
```

APPENDIX G
RM REGISTER SETS

This section describes the SBI, UNIBUS, and Qbus CPA register sets (RM-compatible only). Bits followed by an asterisk have a definition different than DEC's. The registers are summarized at the end of this appendix.

MSCP-compatible CPAs do not use register sets.

G.1 SBI CPA Register Groups

The SBI CPA contains three group of registers as follows:

1. Eight internal operation and control registers (Table G-1).
2. 256 Map registers allow transfers to and from contiguous and noncontiguous memory.

Table G-1. Internal Registers

OFFSET FROM CPA BASE ADDRESS (HEX)	REGISTER NAME	MNEMONIC
00	Configuration/Status	MBACSR
04	Control	MBACR
08	Status	MBASR
0C	Virtual Address	MBAVAR
10	Byte Count	MBABCR
14	Diagnostic	MBADR
18	Selected Map	MBASMR
1C	Command Address	MBACR

3. Sixteen external registers emulate the register located within the disk drives in a DEC MASSBUS system (Table G-3). There are 32 register addresses assigned for each drive. However, in this emulation only 16 registers are used per drive: a total of 128 registers for 8 logical drives. The registers can only be accessed by long-word references that are long-word aligned on byte 0. The internal registers and the map registers are 32 bit wide, but the following convention has been adopted:
   a. For external register writes only the low 16 of the long-word are written.
   b. For external register reads the drive register supplies the low 16 bits and the MBA status register (MBASR) the upper 16 bits (MBASAR bits 31 through 16).

c. To obtain the external (drive) register address, add the hexadecimal number under the required drive number in Table G-2 to the base address for the CPA. External (drive) address calculation is shown in Table G-3.

Table G-2. Base Addresses

TR LEVEL	CPA BASE ADDRESS MBACSR ADDRESS	
	SBI 0	SBI 1
8	20010000	22010000
9	20012000	22012000
19	20014000	22014000
11	20016000	22016000
12	20018000	22018000
13	2001A000	2201A000
14	2001C000	2201C000
15	2001F000	2201F000

Table G-3. External (Drive) Register Address Calculation (Hex)

REGISTER (RM03/05)	OFFSET FROM CPA BASE ADDRESS DRIVE NUMBER							
	0	1	2	3	4	5	6	7
RMCS1	400	480	500	580	600	680	700	780
RMDS	404	484	504	584	604	684	704	784
RMER1	408	488	508	588	608	688	708	788
RMMR1	40C	48C	50C	58C	60C	68C	70C	78C
RMAS	410	490	510	590	610	690	710	790
RMDA	414	494	514	594	614	694	714	794
RMDT	418	498	518	598	618	698	718	798
RMLA	41C	49C	51C	59C	61C	69C	71C	79C
RMSN	420	4A0	520	5A0	620	6A0	720	7A0
RMOF	424	4A4	524	5A4	624	6A4	724	7A4
RMDC	428	4A8	528	5A8	628	6A8	728	7A8
RMHR	42C	4AC	52C	5AC	62C	6AC	72C	7AC
RMMR2	430	4B0	530	5B0	630	6B0	730	7B0
RMER2	434	4B4	534	5B4	634	6B4	734	7B4
RMEC1	438	4B8	538	5B8	638	6B8	738	7B8
RMEC2	43C	4BC	53C	5BC	63C	6BC	73C	7BC

G.2 Internal Registers

The eight internal registers are described below.

Configuration and Status Register (MBACSR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PE	WS	URD	0	MT	TDF	0	0	PD	PU	OT	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit	Name	Function
31	SBI Parity Error (PE)	Set when an SBI parity error is detected. When this bit is set, the fault signal is asserted on the SBI for one cycle. Cleared by power-fail or the deassertion of fault.
30	Write Data Sequence (WS)	Set when no write data is received (neither tag = write data nor ID = write command ID) following a write command. When this bit is set the fault cycle is asserted on the SBI for one cycle. Cleared by power-fail or the deassertion of fault.
29	Unexpected Read Data (URD)	Set when read data is received but not expected. When this bit is set, the fault cycle is asserted on the SBI for one cycle. Cleared by power-fail or the deassertion of fault.
28	Not used	Always read as 0.
27	Multiple Transmitter Fault (MTF)	Set when the ID on the SBI does not agree with the ID transmitted by the CPA while it is transmitting data on the SI. The negation of the fault signal on the SBI clears all the fault status bits. Cleared by power-fail or the deassertion of fault.

Bit	Name	Function
26	Transmission During Fault (TDF)	Set when SBI fault is detected on the second cycle after the CPA has transmitted information to the SBI Cleared by power-fail or the deassertion of fault.
25 — 24	Not used	Always read as 0.
23	Adapter Power-Down (PD)	Set when the CPA detects the assertion of ACLO. When this bit is set, it causes an interrupt to the CPU if IE (MBACR bit 2) is set. Cleared when the controller power goes up or by the assertions of INIT in MBACR, DCLO, UNJAM, or by writing a 1 into this bit.
22	Adapter Power-Up (PU)	Set when the controller receives the deassertion of ACLO. When this bit is set, it also sets IE and interrupts the CPU. Cleared when the controller power goes down or by the assertions of INIT in MBACR, DCLO, UNJAM, or by writing a 1 into this bit.
21	Over Temperature (OT)	Always read as 0.
20 — 08	Not used	Always read as 0.
07 — 00	Adapter Code	Each adapter on the SBI is assigned a separate code. The CPA adapter code is always 00100000.

Controller Register (MBACR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	MM	IE	ABORT	INIT

Bit	Name	Function
31 — 04	Not used	Always read as 0.
03	Maintenance Mode (MM)	Set by writing a 1 into this bit. Setting this bit puts the CPA in the maintenance mode, which lets the programmer execute special diagnostic functions (See MBADR). Cleared by INIT, DCLO, SBI DEAD, or by writing a 0 into this bit.
02	Interrupt Enable (IE)	Set by writing a 1 into this bit or by a power-up. Allows the CPA to interrupt the CPU when certain conditions occur. Cleared by INIT, UNIJAM, DC LO, SBI DEAD, or by writing a 0 into this bit.
01	Abort Data Transfer (ABORT)	Set by writing a 1 into this bit. Setting this bit starts the data transfer abort sequences to stop sending commands and addresses, and stop the byte counter. It also sets DTA in MBASR and interrupts the CPU if IE (bit 2) is set. Cleared by INIT, DC LO or SBI DEAD, or by writing a 0 into this bit.
00	Initialization (INIT)	This bit is always read as 0. Writing a 1 into this bit will: 1. Clear status bits in MBACSR. 2. Clear MBACR, MBASA, and MBABCR. 3. Clear control bits of MBADR. 4. Cancel all pending commands except read data pending. 5. Abort data transfer. 6. Cause a PGM reset interrupt to the controller's MPU.

Status Register (MBASR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DTB	NRC	CRD	0	0	0	0	0	0	0	0	0	PGE	NED	0	ATTN

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	DTC	DTA	DLT	WCU	WCL	MXF	EXC	DPE	MPE	IVM	ECF	RDS	IST	RDT

Bit	Name	Function
31	Data Transfer Busy (DTB)	Set when a data transfer command is received. Read only. Cleared when a data transfer is terminated normally or aborted.
30	No-Response Confirmation (NRC)	This bit is set when the CPA receives a no-response confirmation for the read command or the write data command sent to the SBI. Setting this bit causes a retry of the command. Cleared by INIT or by writing a 1 into it.
29	Corrected Read Data (CRD)	Set when TAG of read data received from memory is CRC. Clear by INIT or by writing a 1 into it.
28 — 20	Not used	Always read as 0.
19	Program Error (PGE)	Set when one or more of the following conditions exists: 1. The program tries to initiate a data transfer when the controller is already doing one. 2. The program tries to load MAP, VAR, or byte counter while the controller is performing a data transfer operation. 3. The program tries to set maintenance mode during a data transfer operation. When this bit is set, it causes an interrupt to the CPU if IE (MBACR bit 2) is set. Cleared by INIT or by writing a 1 into it.

Bit	Name	Function
18	Nonexistent Drive (NED)	Set when a nonexistent drive is addressed. When this bit is set, it causes an interrupt to the CPU if IE is set. Cleared by INIT or by writing a 1 into it.
17	Not used	Always read as 0.
16	Attention (ATTN)	Asserted when any drive attention bit is asserted. The assertion of this bit causes an interrupt to the CPU if IE is set. Cleared by removing attention conditions on all drives. See ATA in RMDS.
15 — 14	Not used	Always read as 0.
13	Data Transfer Complete (DTC)	Set when a data transfer is completed normally or aborted. When this bit is set, it causes an interrupt to the CPU if IE is set. Cleared by INIT, by receipt of a valid data transfer command, or by writing a 1 into it.
12	Data Transfer Aborted (DTA)	Set when the data transfer aborts. When this bit is set, it causes an interrupt to the CPU if IE is set. Cleared by INIT, by receipt of a valid data transfer command, or by writing a 1 into it.
10	Write Check Upper Error (WCU)	Set when a compare error is detected while the controller is performing a write check operation. When this bit is set, the data transfer aborts. Cleared by INIT, by receipt of a valid data transfer command, or by writing a 1 into it.
09	Write Check Lower Error (WCL)	Set when a compare error is detected while the controller is performing a write check operation. When this bit is set, the data transfer aborts. Cleared by INIT, by receipt of a valid data transfer command, or by writing a 1 into it.

Bit	Name	Function
08	Missed Transfer Error (MXF)	Set if the controller fails to detect an end of header, or sector, or the data buffer fails to empty during a data transfer. With this bit set, it causes an interrupt to the CPU if IE is set. Cleared by INIT, by receipt of a valid data transfer command, or by writing a 1 into it.
07	Exception (EXC)	Set when the drive ERR bit (RMDS bit 14) is set. When this bit is set, the data transfer aborts. Cleared by INIT, by receipt of a valid data transfer command, or by writing a 1 into it.
06	Data Parity Error (DPE)	Set when a controller buffer parity error is detected. With this bit set, the data transfer aborts. Cleared by INIT, by receipt of a valid data transfer command, or by writing a 1 into it.
05	Page Frame Map Parity Error (MPE)	Set when a parity error is detected on the data read from the map during a data transfer. When this bit is set, the data transfer aborts. Cleared by INIT, by receipt of a valid data transfer command, or by writing a 1 into it.
03	Error Confirmation (ECF)	Set when the CPA receives error confirmation for a read or write command. When this bit is set, the data transfer aborts. Cleared by INIT, by receipt of a valid data transfer command, or by writing a 1 into it.
02	Read Data Substitute (RDS)	Set when the TAG of the read data received from memory is read data substitute. When this bit is set, the data transfer aborts. Cleared by INIT, by receipt of a valid data transfer command, or by writing a 1 into it.

Bit	Name	Function
01	Interface Sequence Time-out (IST)	Set when an interface sequence time-out occurs. An interface sequence time-out is defined as the beginning time from arbitration for the SBI until: 1. ACK is received for a command address transfer that specifies read or 2. ACK is received for a command/address transfer that specifies write data, or 3. ERR confirmation is received for any command/address transfer. The maximum time-out is 102.4 microseconds. When this bit is set, the data transfer aborts. Cleared by INIT, by receipt of a valid data transfer command, or by writing a 1 into it.
00	Read Data Time-out (RDT)	Set when a read data time-out occurs. A read data time-out is defined as the time from a completion of an interface sequence that specifies a read command to the time that the specified read data is returned to the commander. The maximum time-out is 102.4 microseconds. When this bit is set, the data transfer aborts. Cleared by INIT, by receipt of a valid data transfer command, or by writing a 1 into it.

Virtual Address Register (MBAVAR)

Before a data transfer is initiated, the program must load and initial virtual address (pointing to the first byte to be transferred) into this register. Bits 16 — 09 select one of the 256 MAP registers. The contents of the selected MAP register and the value of bits 08 — 00 are used to assemble a physical SBI address to be sent to memory.

Bits 08 — 00 indicate the byte offset into the page of the current data byte. The virtual address register must not be written to during a data transfer.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MAP

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
POINTER (16 — 09)							BYTE ADDRESS IN PAGE (08 — 00)								

Byte Count Register (MBABCR)

The program loads the two's complement of the number of bytes for the data transfer to bits 15 — 00 of this register. The controller hardware will load these 16 bits into bits 31 — 16 and bits 15 — 00 of the byte count register. Bits 31 — 16 serve as the counter for the number of bytes transferred to or from the drive and bits 15 — 00 serve as the byte count for the number of bytes transferred through the SBI interface.

A starting byte count of 16 bits of zeros is the maximum number of bytes of a data transfer (65,536 bytes). The byte count register must not be modified during a data transfer.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DISK BYTE COUNTER (READ ONLY)															

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SBI BYTE COUNTER (READ/WRITE)															

Diagnostic Register (MBADR)

The Maintenance Mode (MM) bit (MBACR bit 03) must be set to write to the diagnostic register. If the CPA is not in maintenance mode when an attempt to write to MBADR is made, the attempt is ignored.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	SLF	IMP	BSC	TDR	TDO	RW	SAT	TOB	RW	RW	0	DS	DV	AI	DUF

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MPD7	MPD6	MPD5	MPD4	MPD3	MPD2	MPD1	MPD0	RCVR7	RCVR6	RCVR5	RCVR4	RCVR3	RCVR2	RCVR1	RCVR0

Bit	Name	Function
31	Read/Write (RW)	This bit is read/write with no effect. It is used to find out if the bit can be written to. Cleared by INIT.
30	Simulate Loading FAR (SLF)	When Maintenance Mode (MM, MBACR bit 3) is set, writing a 1 followed by a 0 to this bit will simulate loading the file address register on the MPU interface board. Cleared by INIT.
29	Invert Map Parity Checking	When MM and this bit are set, the map parity check bit will be inverted, thus allowing a map parity error to be simulated.
28	Block Sending Command (BSC)	When MM and this bit are set, SBI transfer requests are blocked. This causes the missed transfer bit to be set (MXF,MBASR bit 8). Cleared by INIT.
27	Test Data Request (TDR)	When MM is set, writing a 1 and a 0 to this bit will simulate the assertion and deassertion of DATA REQ on the data path board. Cleared by INIT.

Bit	Name	Function
26	Test DOUT (TDO)	When MM is set, writing a 1 and a 0 to this bit simulates the assertion and deassertion of DMA OUTPUT (DOUT) on the data path board. Cleared by INIT.
25	Read/Write (RW)	This bit is read/write with no effect. It is used to find out if the bit can be written to. Cleared by INIT.
24	Simulate Attention (SAT)	When the MM bit is set, writing a 1 and a 0 to this bit simulates the assertion and deassertion of ATTN. Cleared by INIT.
23	Test OB Clock (TOB)	When the MM bit is set, writing a 1 followed by a 0 to this bit simulates the clocking of an output buffer on the data path board. Cleared by INIT.
22 — 21	Read/Write (RW)	These bits are read/write with no effect. They are used to find out if the bits can be written to. Cleared by INIT.
20	Not used	Always reads as 0.
19	Data Strobe (DS)	This bit is read-only and reflects the state of the data strobe signal on the data path board.
18	Data Valid (DV)	This bit is read-only and reflects the state of the data valid signal on the data path board.
17	Accept Input (AI)	This bit is read-only and reflects the state of the accept input signal on the data path board.
16	D12 Full (DIF)	This bit is read-only and reflects the state of the D12 FULL signal on the data path board.
15 — 08	Microprocessor Data Bus (MPD 7 — 0)	These bits are read only and reflect the state of the controller MPU data bus as received by the MPU interface board.
07 — 00	Receiver Bus (RCVR 7 — 0)	These bits are read-only and reflect the state of the RCVR bus on the data path board.

Selected MAP Register (MBASMR)

This register is read only and has the same format as a MAP register, but it is valid only when DT BUSY is set. These are the contents of the MAP register pointed to by bits 16 — 09 of the virtual address register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VALID	0	0	0	0	0	0	0	0	0	0	PAGE FRAME NUMBER				

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAGE FRAME NUMBER (20 — 00)															

Bit	Name	Function
31	Valid	When this bit is set to 1, it indicates that this map register contains a valid page frame number. If a data transfer attempts to use a map register with this bit set to 0, IVM (MBASR bit 04) is set.
30 — 21	Not used	Always read as 0.
20 — 00	Physical Page Frame Number	Contains physical page frame number of the map.

Command Address Register (MBACAR)

This register is read only and valid only when DTBUSY is set. It contains the value of bits 31 — 00 of the SBI during the command/address part of the CPA's next data transfer.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMMAND (31 — 28)				ADDRESS (27 — 00)											

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ADDRESS (27 — 00)															

MAP Registers

The CPA contains 256 MAP registers, which can only be written to when there is no data transfer in progress. A write to a MAP register while a data transfer in progress is ignored, causes the setting of PGE, and interrupts the CPU at the end of a data transfer if IE is set. Following are the bit assignments of the map registers:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VALID BIT				ZERO (30 — 21)						PAGE FRAME NUMBER (20 — 00)					

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAGE FRAME NUMBER (20 — 00)															

Bit	Name	Function
31	Valid	When set to 1, it indicates this map register contains a valid page frame number. If a data transfer attempts to use a map register with this bit set to 0, IVM (MBASR bit 4) is set.
30 — 21	Not used	Always read as 0.
20 — 00	Physical Page Frame Number	Contains the physical page frame number of the map. The first map register has an offset address of 800 (HEX) from the CPA base address.

UNIBUS and Qbus CPA Registers; SBI External (Drive) Registers (RM03/RM05)

NOTE

A register bit followed by an asterisk indicates that is function(s) differs from DEC's definition.

Registers are referred to by their name, UNIBUS primary address, and SBI offset for disk 0. They are summarized at the end of this appendix.

Control and Status 1 Register (RMCS1) (776700) (offset 400)

RMCS1 can be read or written by program control and is used to store the current disk command function code (Table G-4) and operational status of the controller.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	TRE	MCPE	0	DVA	PSEL	A17	A16	RDY	IE	F4	F3	F2	F1	F0	GO

Bit	Name	Function
15	Special Condition (SC)	Set when TRE or any drive's ATA bit is set. Not used on SBI, always read as 0. Cleared by clearing the TRE or ATA conditions.
14	Transfer Error (TRE)	Set when one or more of RMCS2 bits 15 — 08 (DLT,WCE,UPE,NED,NEM,PGE,MXF,MDPE) are set or a drive error occurs during a data transfer. Not used on SBI, always read as 0. Cleared by UNIBUS INIT, controller clear, by loading a data transfer command with GO set, or by writing a 1 to this bit which causes an error clear.
13*	MASSBUS Control Bus	Set to 0 by the controller. Not used on SBI.
	Parity Error (MCPE)	
12	Not used	Set to 0 by the controller.
11*	Drive Available (DVA)	Always read as 1.
10*	Port Select (PSEL)	Set to 0 by the controller. Not used on SBI.

Bit	Name	Function
09 — 08	A17 — A16 UNIBUS Address Extension Bits	Upper extension bits of the RMBA register. Not used on SBI. Cleared by UNIBUS INIT, controller clear, or by writing zeros in these bit positions.
07	Ready (RDY)	Normally RDY = 1. During data transfers, RDY = 0. When a data transfer command code (51 — 73 octal) is written into RMCS1, RDY is reset. At the termination of the data transfer, RDY is set. Not used on SBI.
06	Interrupt Enable (IE)	IE is a control bit that can be set only under program control and which enables an interrupt to occur when the following conditions are satisfied: 1. At the end of a data transfer if IE is set when RDY is asserted. 2. If SC, IE, and RDY are all asserted. 3. If the program writes 1s into IE and RDY at the same time. Cleared by UNIBUS INIT, controller clear or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled. Not used on SBI.
05 — 00	F4 — F0 and GO Bit	F4 — F0 and the GO bit (00) are function (command) code control bits. See Table G-4.

Table G-4. Function Code Control Bits

F4	F3	F2	F1	F0	GO*	HEX	OCTAL	FUNCTION
0	0	0	0	0	1	01	01	No Operation
0	0	0	1	0	1	05	05	Seek
0	0	0	1	1	1	07	07	Recalibrate
0	0	1	0	0	1	09	11	Drive Clear
0	0	1	0	1	1	0B	13	Release
0	0	1	1	0	1	0D	15	Offset
0	0	1	1	1	1	0F	17	Return to Centerline
0	1	0	0	0	1	11	21	Read-in-present
0	1	0	0	1	1	13	23	Pack Acknowledge
0	1	0	1	0	1	15	25	System Reserve (Extended Mode Only)†
0	1	0	1	1	1	17	27	System Release (Extended Mode Only)†
0	1	1	0	0	1	19	31	Search
1	0	1	0	0	1	29	51	Write Check Data
1	0	1	0	1	1	2B	53	Write Check Header and Data
1	0	1	1	0	1	2D	55	dMode Change (Extended Mode Only)†
1	1	0	0	0	1	31	61	Write Data
1	1	0	0	1	1	33	63	Write Header and Data
1	1	1	0	0	1	39	71	Read Data
1	1	1	0	1	1	3B	73	Read Header and Data
1	1	1	1	0	1	3D	75	Maintenance Function (Extended Mode Only)†

* The GO bit (RMCS1, bit 0) must be set to cause the controller to respond to a command. The controller resets GO after command.

† SI Function

Word Count Register (RMWC) 776702

The program loads RMWC with the two's complement of the number of words to be transferred. A maximum of 65,535 words can be transferred at one time.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC

Bit	Name	Function
15 — 00	Word Count (WC)	The program sets this register to specify the number of words to be transferred (two's complement form). The controller updates this register after completion of each DMA transfer. Not used on SBI. Cleared by writing zeros into it.

UNIBUS Address Register (RMBA) 776704

RMBA addresses the memory location in which a transfer is to take place. This register forms the lower 16 bits of the address that combine with bits 09 and 08 of the control register RMCS1 to create the 18-bit memory address or bits 05 — 00 of RMBAE to create the 22-bit memory address (Qbus CPA only).

The program loads the register with the staring memory address. After each DMA transfer, the register increments by 2. If BAI (bus address increment inhibit), bit 03 of RMCS2, is set, incrementing RMBA is inhibited and all transfers take place to or from the staring memory address.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	0

Bit	Name	Function
15 — 01	UNIBUS Address (BA)	Loaded by the program to specify the memory address of a transfer. RMBA increments by 2 after each transfer of a word to or from memory. Not used on SBI. Cleared by UNIBUS INIT or controller clear.
00	Not used	Always read as 0. Not used on SBI.

Desired Sector/Track Address Register (RMDA) 776706 (offset 414)

RMDA addresses the sector and track on the disk to or from which a transfer is desired. The RMDA register is associated with the drive whose unit number appears in bits 02 — 00 of the status register RMCS2 for UNIBUS and Qbus operations.

Before a transfer on the UNIBUS and Qbus CPA, the RMDA register is loaded by the program with the address of the first block to be transferred. At the end of a transfer RMDA contains the address of the block following the last block of the transfer. RMDA contains a 6-bit sector address field providing for 64 sectors per track. It also contains a 6-bit track address field providing for up to 64 data tracks per cylinder.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	TA32	TA16	TA8	TA4	TA2	TA1	0	0	SA32	SA16	SA8	SA4	SA2	SA1

Bit	Name	Function
15 — 14	Not used	Set to 0 by the controller.
13 — 08	Track Address (TA)	The program sets these bits to specify the track on which a transfer is to start. Updated by the controller at the end of the transfer. Clear by UNIBUS INIT
07 — 06	Not used	Set to 0 by the controller.
05 — 00	Sector Address (SA)	The program sets these bits to specify the sector on which a transfer is to start. Updated by the controller at the end of the transfer. Cleared by UNIBUS INIT.

Control/Status Register 2 (RMCS2) 776710

RMCS2 indicates the status of the controller and contains the drive unit number. The unit number specified in bits 02 — 00 of this register indicates which of the possible eight logical drives is selected. Not used on SBI.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0

Bit	Name	Function
15*	Data Late (DLT)	Set to 0 by the controller.
14	Write Check Error (WCE)	Set when the controller is performing a write-check operation and a word on the disk does not match the corresponding word in memory. WCE sets TRE. If a mismatch is detected during a write-check command execution, the transfer terminates and the WCE bit is set. The memory address displayed in RMBA (and extension) is the address of the word following the one that did not match, if BAI is not set. The mismatched data word from the disk is displayed in the data buffer (RMDB). Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with the GO bit set.
13	UNIBUS Parity Error (UPE)	Set if UNIBUS parity lines indicate an error while the controller is performing a data transfer command. UPE sets TRE. The RMBA contains the address plus two of the memory location with the parity error. Cleared by UNIBUS INIT, controller clear, error clear, or by loading a data transfer command with the GO bit set.
12	Nonexistent Drive (NED)	Set when the program attempts a command on a drive that does not exist, or is powered-down. NED sets TRE. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with the GO bit set.

Bit	Name	Function
11	Nonexistent Memory (NEM)	Set when the controller is performing a DMA transfer and the memory address specified in RMBA is nonexistent, i.e., does not respond to MSYN within 10 microseconds. NEM sets TRE. The RMBA register contains the address plus two of the memory location causing the error. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with the GO bit set.
10	Program Error (PGE)	Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. PGE sets TRE. Cleared by UNIBUS INIT, controller clear, or error clear.
09*	Missed Transfer (MXF)	Set if the controller fails to detect an end of header, end of sector, or the data buffer fails to empty during a data transfer. MXF sets TRE. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with the GO bit set.
08	MASSBUS Data Bus Parity Error (MDPE)	Set to 0 by the controller.
07	Output Ready (OR)	Set by the controller to indicate a word is in RMDB.
06*	Input Ready (IR)	Set to 1 by the controller.
05	Controller Clear (CLR)	When a 1 is written into CLR bit, the controller and all drives are initialized. Always read as 0.
04*	Parity Test (PAT)	PAT bit has no effect on controller operation. Cleared by UNIBUS INIT or controller clear.

Bit	Name	Function
03	UNIBUS Address (BAI)	When BAI is set, the controller will not increment the RMBA register during a data transfer. BAI bit cannot be modified while the controller is doing a data transfer (RDY negated). If set during a data transfer, all data words are read from or written into the same memory location. Cleared by UNIBUS INIT or controller clear.
02 — 00	Unit select (U2 — U0)	U2 — U0 bits are written by the program to select a drive. The program can change these bits during data transfer operations, without interfering with the transfer. Cleared by UNIBUS INIT, or controller clear.

Drive Status Register (RMDS) 776612 (SBI offset 404)

RMDS contains status indicators for the selected drive. The status indicators displayed are those of the drive that is specified by the unit select bits (02 — 00) of the RMCS2 register for the UNIBUS/Qbus CPA.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	0	0	0	0	0	OM

Bit	Name	Function
15	Attention Active (ATA)	An attention condition from a drive sets the ATA bit and the corresponding summary bit in RMAS. ATA is cleared by UNIBUS INIT, drive clear, controller clear, loading a command with the GO bit set, or, if no error conditions exist, writing a 1 in the RMAS register bit corresponding to the drive unit number. An attention condition is caused by: 1. Any error in the error register if; a. GO bits set at completion of command. b. Go bits reset at occurrence of error.

Bit	Name	Function
		2. At the completion of seek, search, recalibrate, offset, or return to centerline. 3. MOL changes state.
14	Error (ERR)	Set when one or more of the error bits in the error registers (RMER1 or RMER2) for a selected drive is set. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing zeros into the error registers.
13*	Positioning In Progress (PIP)	Always read as 0.
12	Medium On-Line (MOL)	Set for the drive upon the successful completion of the start-up cycle. This bit is asserted when the unit ready line from the drive is asserted indicating that the drive is up to speed, the heads are positioned over the recording tracks, and no fault condition exists within the drive. Cleared when the drive is spun-down or switched off.
11	Write Lock (WLRL)	Set when the write protected line from the drive is asserted (as enabled by a switch located on the drive), indicating that the drive will not accept write commands. A write command issued on a write-locked drive causes the write-lock error (WLE, bit 11 of RMER1) to be set.
10	Last Sector Transferred (LST)	Set when last addressable sector on the disk pack has been read or written.
09*	Programmable (PGM)	Always read as 0.
08*	Drive Present (DPR)	Set if the drive is powered-up.

Bit	Name	Function
07	Drive Ready (DRY)	Set at the completion of every command, data handling or mechanical motion. If this bit is reset, the program must not issue another command to this drive. When set, this bit indicates the readiness of the drive to accept a new command. DRY is the complement of the GO bit except when the drive is nonexistent. Then DRY is reset. Cleared at the initiation of a command.
06	Volume Valid (VV)	Set by the pack acknowledge or read-in preset command. When reset, VV bit indicates the drive has been spun down and then up, and that a disk pack may have been changed (RMD only). Cleared whenever the drive spins up, i.e., when MOL becomes asserted, or when the CPU powers-up.
05 — 01	Not used	Always read as 0.
00	Offset Mode (OM)	Set when offset command is issued to the drive. When set, and a read command is received, the offset is performed prior to the execution of the read. Reset by any of the following actions: 1. Power-up 2. Mid-transfer seek 3. Write data or write header and data 4. Return to centerline 5. Recalibrate

Error Register 1 (RMER1) 776714 (SBI offset 408)

RMER1 contains the error status indicators for the drive whose unit number appears in bits 02 — 00 of the RMCS2 register on UNIBUS/Qbus CPA's. The logical OR of all the error bits in the RMER1 and RMER2 registers are written into bit 14 of the RMDS register.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	BPE	RMR	ILR	ILF

Bit	Name	Function
15	Data Check (DCK)	If ECI (RMOF bit 11) is 0, this bit will be set if a correctable ECC error is detected (ECH is also set). If ECI is 1 and the ECC error is detected, no correction is attempted and this bit is set. The ECH bit will not be set. Cleared by drive clear, UNIBUS INIT, controller clear, or by writing zeros into the register.
14	Unsafe (UNS)	Indicates a drive fault has been detected. If set and DVC is not set, an ACLO condition occurs. Set when bit 7 (DVC) of RMER2 is set. Cleared by drive clear, UNIBUS INIT, controller clear, or by writing zeros into this register.
13*	Operation Incomplete (OPI)	Set to 0 by the controller.
12	Drive Timing Error	Set when more than one sector pulse occurs within a sector. Cleared by drive clear, UNIBUS INIT, controller clear, or by writing zeros into this register.
11	Write Lock Error (WLE)	Set when the operating system attempts to issue a write command to a drive which has its write-protect switch on (WRL set in RMDS). Cleared by UNIBUS INIT, drive clear, controller clear, or by writing zeros into the register.

Bit	Name	Function
10	Invalid Address Error (IAE)	Set when the address in the desired cylinder register (RMDC) or the disk address register (RMDA) is invalid and a seek, search, or data transfer operation is initiated. Cleared by UNIBUS INIT, drive clear, controller clear, or by writing zeros into the register.
09	Address Overflow Error (AOE)	Set when the desired cylinder register (RMDC) overflows during a read or write. Cleared by UNIBUS INIT, drive clear, controller clear, or by writing zeros into the register.
08	Header CRC Error (HCRC)	Set by a CRC error in the header if HCI (RMOF bit 10) is reset. Cleared by UNIBUS INIT, drive clear, controller clear, or by writing zeros into the register.
07	Header Compare Error (HCE)	If the sector counter is equal to the desired sector field, the header associated with that sector is compared with the desired header words. If the header matches the desired cylinder and desired sector/track address, the header field is the required one. If HCI (RMOF bit 10) is reset and the header does not match the desired cylinder and sector/track address, the HCE bit is set. Cleared by UNIBUS INIT, drive clear, controller clear, or by writing zeros into the register.
06	ECC Hard Error (ECH)	Set by an uncorrectable ECC error. This bit is not set if ECI (RMOF bit 11) is set. Cleared by UNIBUS INIT, drive clear, controller clear, or by writing zeros into the register.
05*	Write Clock Fail (WCF)	Set to 0 by the controller.

Bit	Name	Function
04*	Format Error (FER)	Set when the controller format switch is OFF and a write header and data command is attempted. Cleared by UNIBUS INIT, drive clear, controller clear, or by writing zeros into this register.
03*	Buffer Parity Error (BPE)	Set when a controller buffer parity error is detected. Cleared by UNIBUS INIT, drive clear, controller clear, or by writing zeros into this register.
02*	Register Modification Refused (RMR)	Set to 0 by the controller.
01	Illegal Register (ILR)	Set to 0 by the controller.
00	Illegal Function (ILF)	Set when the GO bit is set and the function code in the control register does not correspond to a valid command on this drive. Cleared by UNIBUS INIT, drive clear, controller clear, or by writing zeros into the register.

Attention Summary Register (RMAS) 776716 (SBI offset 410)

RMAS allows the program to examine the attention status of all the drives with only one register read operation. It also provides the means for resetting the attention logic in a selected group of drives.

The bit displayed in each of the eight low-order positions of this register is identical to the ATA bit displayed in the RMDS register for the corresponding drive. When fewer than eight drives are attached to the controller, the bits corresponding to the missing drives are always 0.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA	ATA	ATA	ATA	ATA	ATA	ATA	ATA

Bit	Name	Function
15 — 08	Not used	Always read as 0.
07 — 00	Attention Active (ATA)	Each ATA bit is set when the corresponding drive asserts its ATA bit. All bits are cleared by UNIBUS INIT, or controller clear. Individual bits are cleared by loading a function code with the GO bit set in the corresponding drive or by writing a 1 in the ATA bit positions of this register. Writing a zero has no effect. Each drive's ATA bit is displayed in bit 15 of RMDS. Each drive also responds in the bit position of RMAS register that corresponds to its logical unit number; e.g., drive 02 responds in bit position 02 of RMAS register.

Look-Ahead Register (RMLA) 776720 (SBI offset 41C)

RMLA is a communication register between the controller and the CPU.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
QBCPA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Function
15	Qbus CPA	1 = Qbus, 0 = UNIBUS. Software tool for bus identification.
14 — 00	—	Reserved

Data Buffer Register (RMDB) 776722

RMDB provides the bad data-word resulting from a bad data-compare operation. Not used in SBI.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB

Bit	Name	Function
15 — 00	Data Buffer (DB)	Contains the bad data-word.

Maintenance Register #1 (RMMR1) 776724 (SBI offset 40C)

RMMR1 is not emulated.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Function
15 — 00	Not Emulated	Set to 0 by the controller.

Drive Type Register (RMDT) 776726 (SBI offset 418)

RMDT allows the program to distinguish between different types of drives.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	MOH	0	DRQ	0	0	DT	DT	DT	DT	DT	DT	DT	DT	DT

Bit	Name	Function
15 — 14	Not used	Set to 0 by the controller.
13	Moving Head (MOH)	Set to 1 by the controller, since the drives are moving head devices.
12	Not used	Set to 0 by the controller.
11*	Drive Request Required (DRQ)	Set to 0 by the controller.
10 — 09	Not used	Set to 0 by the controller.
08 — 00	Drive Type (DT)	These bits contain a code indicating the drive type being emulated. This is determined by the controller firmware (RMOX) reading the model byte switch bank on the DI board (Table G-5).

Table G-5. Drive Type Code

DRIVE TYPE RM03	RM05
24*	27*

* Octal Notation

Serial Number Register (RMSN) 776730 (SBI offset 420)

The RMSN bit definitions have been changed to reflect SI device types.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	X	X	X	X	X	U2	U1	U0

Bit	Name	Function
15	Emulation	1 = RM03. 0 = RM05.
14	CLUSTOR	Set to 1 for 2500 Controller.
13	Drive Cabling	1 = daisy-chain. 0 = radial.
12	Bad Block Forwarding (BBF)	1 = BBF enabled. 0 = BBF disabled.
11 — 07	Drive Model Bytes	See Table G-6.
06	Dual-Drive	1 = dual drive. 0 = single drive.
05	Mapped/Direct	1 = mapped. 0 = direct.
04	Drive Type	1 = FMD. 0 = RMD (Fixed/Removable Media).
03	—	Reserved for SI.
02 — 00	U2 — U0	Drive unit numbers.

Offset Register (RMOF) 776732 (SBI offset 424)

RMOF contains the positioner offsetting information supplied to the drive directly by the software operating system prior to issuance of the offset command. The drive has the ability to offset the positioner approximately 200 microinches from the track centerline in either direction.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	FMT	ECI	HCI	0	0	OFD	0	0	0	0	0	0	0

Bit	Name	Function
15 — 13	Not used	Set to 0 by the controller.
12*	Format 16 (FMT)	The controller sets this bit to 1. A zero bit here is useless, since only a 16-bit format is used.
11	Error Correction Inhibit (ECI)	Set when the software inhibits error correction. If an ECC error is detected and this bit is reset, the controller performs the ECC correction process at the end of the sector, provided the W7 jumper on the controller is set for internal ECC correction. If the error is correctable, it is corrected in the controller's buffer and the transfer proceeds (software transparent — no error indication). If the error is uncorrectable, the controller sets the ECH and DCK bits in RMER1. If the ECI bit is set, however, the error correction process is inhibited, and the DCK bit in RMER1 is set (ECH bit is not set). Cleared by UNIBUS INIT, drive clear, controller clear, or by writing zeros into this bit.
10	Header Compare Inhibit (HCI)	Set when the software inhibits the reporting of header compare errors HCE and HCRC. When the controller detects this bit asserted, it ignores the header compare logic and CRC check. With HCI set, the controller depends only on the hardware sector counter comparison for identification. If the sector counter is out of sequence, the wrong sector might be affected by the data transfer.

Cleared by UNIBUS INIT, drive clear, controller clear, or by writing a zero into this bit.

Bit	Name	Function
09 — 08	Not used	Set to 0 by the controller.
07	Offset Direction (OFD)	Set when the offset direction is toward the spindle. When reset, the offset direction is away from the spindle. The offset direction bit is valid if the following conditions are met: 1. Read command is loaded into bits 0 — 5 of control register (RMCS1). 2. RMCS1 GO bit is set. 3. The offset mode bit (RMDS bit 00) is set.
06 — 00	—	Reserved

Desired Cylinder Register (RMDC) 776734 (SBI offset 428)

RMDC contains the address of the cylinder to which the drive positioner moves the heads for a seek, search, or data handling command.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC

Bit	Name	Function
15 — 13	Not used	Set to 0 by the controller.
12 — 00	Desired Cylinder (DC)	Set by the program to specify the required cylinder address. The IAE bit in RMER1 is set if, when asserting the GO bit for data transfer, seek or search command, RMDC contains an address larger than the maximum cylinder address on the drive.

Holding Register (RMHR) 776736 (SBI offset 42C)

RMHR is not emulated and is to 0 by the controller.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Function
15 — 00	Not Emulated	Set to 0 by the controller.

Maintenance Register #2 (RMMR2) 776740 (SBI offset 430)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Function
15 — 00	Not Emulated	Set to 0 by the controller.

Error Register #2 (RMER2) 776742 (SBI offset 434)

RMER2 contains detailed error status information and is primarily used for monitoring the electromechanical performance of the drive rather than the interface.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BSE	SKI	DPE	IVC	LSC	LBC	0	0	DVC	0	0	0	DPE	0	0	0

Bit	Name	Function
15	Bad Sector Error (BSE)	Set when the controller detects a 0 in bit 14 or 15 of the first header word and the HCI bit in RMOF is zero. Cleared by UNIBUS INIT, drive clear, controller clear, or by writing zeros into this register.
14	Seek Incomplete (SKI)	Set when a seek operation fails to complete within 500 ms from a seek initiation. Cleared by UNIBUS INIT, controller clear, or by writing zeros into this register.

Bit	Name	Function
13*	Drive Plug Error (DPE)	Set to 0 by the controller.
12	Invalid Command (IVC)	Set when either VV or MOL (RMDS bits 6 and 12) are reset and any command other than read-in preset, pack acknowledge, drive clear or NO-OP is received. Cleared by UNIBUS INIT, drive clear, controller clear, or by writing zeros into this register.
11*	Loss of System Clock (LSC)	Set to 0 by the controller.
10*	Loss of Bit Clock (LBC)	Set to 0 by the controller.
09 — 08	Not used	Set to 0 by the controller.
07	Device Check (DVC)	Set when drive fault line is asserted. Also sets UNS (bit 14 of RMER1).
06 — 04	Not used	Set to 0 by the controller.
03*	Data Parity Error (DPE) or Massbus Data Parity Error (MDPE)	Set to 0 by the controller.
02 — 00	Not used	Set to 0 by the controller.

ECC Position Register (RMEC1) 776744 (SBI offset 438)

RMEC1 (Read Only)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	BURST LOCATION (12 - 00)												

Bit	Name	Function
15 — 13	Not used	Set to 0 by the controller.
12 — 00	Burst Location	These bits specify the location in the record of the first bit of the error burst in the error pattern register.

ECC Pattern Register (RMEC2) 776746 (SBI offset 43C)

RMEC2 (Read Only)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	ERROR BURST (10 — 00)										

Bit	Name	Function
15 — 11	Not used	Set to 0 by the controller.
10 — 00	Error Burst	These bits are the 11-bit error correction burst that the software uses to correct bad data in the record. The ECC position register specifies the staring bit position.

Bus Address Extension Register (RMBAE) 776750

NOTE

This register pertains to Qbus CPA only.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	A21	A20	A19	A18	A17	A16

Bit	Name	Function
15 — 06	Not used	Set to 0 by the controller.
05 — 00	Address Extension Bits	These are the upper extension bits of the RMBA register. Bits 01 and 00 are echoed in bits 09 and 08 in RMCS1.

G.3 Register Summaries

The three register groups are summarized below.

Configuration and Status Register (MBACSR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PE	WS	URD	0	MT	TDF	0	0	PD	PU	OT	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Controller Register (MBACR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	MM	IE	ABORT	INIT

Status Register (MBASR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DTB	NRC	CRD	0	0	0	0	0	0	0	0	0	PGE	NED	0	ATIN

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	DTC	DTA	DLT	WCU	WCL	MXF	EXC	DPE	MPE	IVM	ECF	RDS	IST	RDT

Virtual Address Register (MBAVAR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MAP

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
POINTER (16 — 09)							BYTE ADDRESS IN PAGE (08 — 00)								

Byte Count Register (MBABCR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DISK BYTE COUNTER (READ ONLY)															

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SBI BYTE COUNTER (READ/WRITE)															

Diagnostic Register (MBADR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	SLF	IMP	BSC	TDR	TDO	RW	SAT	TOB	RW	RW	0	DS	DV	AI	DUF

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MPD7	MPD6	MPD5	MPD4	MPD3	MPD2	MPD1	MPD0	RCVR7	RCVR6	RCVR5	RCVR4	RCVR3	RCVR2	RCVR1	RCVR0

Selected MAP Register (MBASMR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VALID	0	0	0	0	0	0	0	0	0	0	PAGE FRAME NUMBER				

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAGE FRAME NUMBER (20 — 00)															

Command Address Register (MBACAR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMMAND (31 — 28)				ADDRESS (27 — 00)											

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ADDRESS (27 — 00)															

MAP Registers

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VALID BIT				ZERO (30 — 21)						PAGE FRAME NUMBER (20 — 00)					

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAGE FRAME NUMBER (20 — 00)															

Control/Status 1 Register (RMCS1) (776700) (offset 400)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	TRE	MCPE	0	DVA	PSEL	A17	A16	RDY	IE	F4	F3	F2	F1	F0	GO

Word Count Register (RMWC) 776702 (not used on SBI)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC

UNIBUS Address Register (RMBA) 776704 (not used on SBI)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	0

Desired Sector/Track Address Register (RMDA) 776706 (offset 414)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	TA32	TA16	TA8	TA4	TA2	TA1	0	0	SA32	SA16	SA8	SA4	SA2	SA1

Control/Status Register 2 (RMCS2) 776710 (not used on SBI)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0

Drive Status Register (RMDS) 776612 (SBI offset 404)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	0	0	0	0	0	OM

Error Register 1 (RMER1) 776714 (SBI offset 408)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	BPE	RMR	ILR	ILF

Attention Summary Register (RMAS) 776716 (SBI offset 410)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA	ATA	ATA	ATA	ATA	ATA	ATA	ATA

Look-Ahead Register (RMLA) 776720 (SBI offset 41C)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1/0*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

* 1 = Qbus, 0 = UNIBUS.

Data Buffer Register (RMDB) 776722 (not used on SBI)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB

Maintenance Register #1 (RMMR1) 776724 (SBI offset 40C)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Drive Type Register (RMDT) 776726 (SBI offset 418)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	MOH	0	DRQ	0	0	DT	DT	DT	DT	DT	DT	DT	DT	DT

Serial Number Register (RMSN) 776730 (SBI offset 420)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	X	X	X	X	X	U2	U1	U0

Offset Register (RMOF) 776732 (SBI offset 424)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	FMT	ECI	HCI	0	0	OFD	0	0	0	0	0	0	0

Desired Cylinder Register (RMDC) 776734 (SBI offset 428)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC

Holding Register (RMHR) 776736 (SBI offset 42C)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Maintenance Register #2 (RMMR2) 776740 (SBI offset 430)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Error Register #2 (RMER2) 776742 (SBI offset 434)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BSE	SKI	DPE	IVC	LSC	LBC	0	0	DVC	0	0	0	DPE	0	0	0

ECC Position Register (RMEC1) 776744 (SBI offset 438)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	BURST LOCATION (12 — 00)												

ECC Pattern Register (RMEC2) 776746 (SBI offset 43C)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	ERROR BURST (10 — 00)										

Bus Address Extension Register (RMBAE) 776750 (not used on SBI)

NOTE

This register pertains to Qbus CPA only.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	A21	A20	A19	A18	A17	A16