

DIGITAL MAGNETIC LOGIC

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INTRODUCTION

This book deals with a class of digital magnetic-core circuits that consist of magnetic components and interconnecting conductors, and which offer extremely high reliability, long life, and adaptability to special environments, e.g., high-intensity radiation. The history of such *core-wire circuits*, as we refer to them in this book, spans some 15 to 20 years, from the first discussions of theoretical possibility to the large array of techniques and variations at present.

Four potential areas of study for any device and circuit technology are (1) the physics of the devices, (2) the development of engineering models for use in circuit analysis, (3) the development of circuit synthesis techniques, and (4) the development of quantitative circuit-design methods. Part I is concerned with areas (3) and (4) and is based on the use of a highly abstracted magnetic-core model that greatly simplifies the discussion of basic circuit principles. The bulk of the writing in Part I covers many different core-wire techniques and represents an attempt to integrate the published work of many different authors. Parts of Chaps. 6 and 10 are concerned with circuit-design methods not previously published. Part II covers areas (1) and (2), based on use of more detailed, precise consideration of magnetic phenomena. Chapter 11 provides a condensed summary of the physics of magnetism for readers wishing some insight into the behavior of square-loop cores. Chapter 12 covers recently developed core models that permit accurate representation of flux switching in square-loop cores.

Part I is a step-by-step development of the principles of magnetic-core circuit techniques. In Chap. 1 we introduce the language of flux linkage and current linkage, and show how basically different the circuit action is when a core is loaded with resistive, inductive, or capacitive elements. In Chap. 2 we consider

flux transfer from one core to another core, in which case a change in flux linkage from the switching of a first core induces a coupling-loop current that switches the second core; the change in flux level, $\Delta\phi$, becomes our basic signal. We are primarily interested in the ratio of received flux to transmitted flux, i.e., the flux-transfer ratio G , which is generally a function of the transmitted flux level $\Delta\phi_T$. Of special interest are the conditions for $G > 1$, that is, for $\Delta\phi$ gain.

In Chap. 3 we show that in order to achieve bistable gain characteristics, G must exhibit a certain form of functional dependence on $\Delta\phi_T$. Proper balancing of flux-gain and flux-loss mechanisms permits the realization of the required functional form. To maintain this transfer characteristic between two cores embedded in a chain of similar cores, certain requirements on forward and backward isolation must be met. It is shown how diodes readily serve in this role, which is the basis of the well-known core-diode logic circuits.

In Chap. 4 we introduce several varieties of core-wire circuits. This begins as an effort to replace the diodes in a core-diode circuit by other toroidal cores. A systematic replacement procedure is developed, and we show how any core-diode circuit can in fact be realized in core-wire form, i.e., as a circuit consisting simply of toroidal cores and interconnecting wire. We then extend the class of core-wire circuits and develop new circuit forms that have no equivalent core-diode forms. We also introduce more complex core shapes, i.e., multileg cores, and show their advantages over functionally equivalent arrays of simple toroidal cores.

In Chap. 5 we show how to transform a core circuit to a magnetic-network representation in which rate of flux change is the flow variable. The network representation provides a common language for flux-transfer schemes. Many schemes that superficially appear different can be shown by the network representation to be functionally equivalent. Also, it is generally simpler to convert from one type of scheme to another after transforming to the network domain. Examples of transformations and reverse transformations are given. In particular, it is shown that any given network may often have many different forms of physical realization.

In Chap. 6 we treat a specific core-wire scheme, designated by the term MAD-R, that has been studied and applied more than any other scheme. A quantitative design method for this form of circuit is presented, and it is shown that circuits of this type can

be designed to operate with very wide tolerances on temperature and power-supply conditions.

The core-wire schemes known today were invented by many different persons and generally in a rather *ad hoc* and random fashion, a situation that characterizes the early advances in many fields. In Chap. 7, a technique is described by means of which one can search for all possible schemes for a given configuration of magnetic elements. Certain new schemes derived in this fashion, as well as a formal "re-inventing" of certain of the schemes discussed in Chaps. 4 and 5, are given by way of example. The method itself offers interesting insight into the operation of these circuits.

A comment is in order on scheme identification as generally used throughout these chapters. Because it was not easy to develop nomenclature that clearly distinguishes between various schemes (in the fashion of the terms DCTL, TRL, and the like, as applied to transistor circuits), we decided instead to identify a scheme or method of approach by the name of the person with whom it is associated, as far as we know, either by patent disclosure or publication. We depart from this policy in the case of better-known schemes when a name has been established (e.g., the MAD-R scheme).

In Chaps. 8 and 9 we introduce other methods of approach to circuit synthesis that open up whole new families of schemes, some of which offer significant potential for future practical application. Three different techniques are introduced in Chap. 8, each leading to new scheme types. Together these techniques pave the way in Chap. 9 for an important class of bipolar schemes. In the bipolar representation, the binary states (designated *one* and *zero*) are symmetrically represented; i.e., they are characterized by flux transfer of equal amplitudes but opposite polarities, as opposed to high and low levels of flux transfer in the unipolar schemes. A number of especially interesting schemes based on the use of coherent rotation of magnetization in thin films fall into the bipolar category.

Through Chap. 9 we are concerned strictly with the development of basic transfer schemes, i.e., flux transfer along a simple, iterative chain of circuits, without regard to logical fan-in or fan-out. In Chap. 10 we investigate methods of general logic synthesis with core-wire circuits.

Part II is concerned with the magnetic devices themselves. Chapter 11 is a highly condensed, step-by-step exposition of the physics of magnetism that leads to the basic square-loop

characteristic and the basic mechanisms of flux switching. It provides the reader with some background to appreciate the empirical models for flux switching that are discussed in detail in Chap. 12.

The goal of Chap. 12 is to model the static and dynamic flux properties of square-loop magnetic cores. It is shown that a pair of simple mathematical equations can model the major hysteresis loop of a typical ferrite material, from which hysteresis loops for thick-walled toroidal cores are derived and shown to fit experimental data quite accurately. Parameters derived from these static hysteresis curves are used in the dynamic switching models. From the results of basic flux-switching experiments, it is shown that the familiar elastic and inelastic components of flux switching can best be modeled in terms of two components each. The two components of elastic switching are due to rotation of magnetization and local domain-wall movements; the two components of inelastic switching relate to what are referred to as minor and major wall displacements. Mathematical equations for all four components are derived, and it is shown how these relations quite accurately model flux switching of ferrite cores over a large range of drive amplitudes, conditions of loading, and switching speed (from nanoseconds to microseconds). Computational methods for the models are also discussed. These models are presently being applied with considerable success to computer-aided analysis of complex magnetic-core circuits.

Two primary reasons can be singled out for the erratic development of core-wire logic circuits over the past fifteen years: the general lack of background, training, and understanding of magnetics by engineers who are the potential users; and the rapid growth of semiconductor technology, which has generally offered circuits with performance superior to that of core circuits under most, though not all, conditions. This book was begun over seven years before publication, and the enthusiasm for following it to completion has been similarly erratic. We finally came to the conclusion, independently of short-time variations in general interest, that core-wire or other magnetic-core logic circuits in one form or another will likely find their niche—if not based on ruggedness and reliability one year, then on radiation immunity and absence of standby power the next. This factor provided a major impetus to complete the book. But equally important, although the underlying thread of this book is the highly specialized technology of core-wire circuits, much of the material is relevant to magnetic devices and circuits in general.

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Part I

CORE-WIRE CIRCUITS

ELEMENTARY CIRCUITS

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In order to develop some background for dealing with flux transfer between cores, which is basic to any digital magnetic-core circuit, we consider in this first chapter the properties of simple circuits utilizing a single magnetic element in combination with certain of the more common electrical components. The primary intent is qualitative understanding rather than engineering detail.

1-1 Introduction

Let us first review the fundamental rules governing induced electromotive force (emf) and induced magnetomotive force (mmf). Consider a vector field B representing magnetic flux density at any point in space. If B changes with time, then an electric field E is induced, as described by one of Maxwell's equations, namely

$$\text{curl } E \equiv \nabla \times E = - \frac{\partial B}{\partial t} \quad (1-1)$$

By vector manipulation, Eq. (1-1) may be converted to the integral form

$$\oint_P E \cdot dl = - \frac{\partial}{\partial t} \int_A B \cdot dA \quad (1-2)$$

usually referred to as Faraday's law of induction, where P is any closed path, and A is any surface bounded by P . The line integral of E along P is the loop emf e , and $\int \mathbf{B} \cdot d\mathbf{A}$ is the magnetic flux linking the closed loop P . When the same quantity of flux ϕ is encircled N times by the loop P , that is, a winding of N turns, then, effectively

$$\int \mathbf{B} \cdot d\mathbf{A} = N\phi \quad (1-3)$$

and for this case, Eq. (1-2) may be rewritten as

$$e = -N \frac{d\phi}{dt} \quad (1-4)$$

The minus sign in Eq. (1-4) implies that the induced emf tends to produce current with associated flux linkage opposing the original $Nd\phi/dt$, in accordance with Lenz's law and use of a left-hand rule. Normally we will be concerned with a coupling loop, i.e., a closed path formed by an electrical conductor, in which the current that flows is such that the total voltage drop around the loop is always equal to the induced emf e .

In core circuits we are primarily concerned with magnetic fields that are concentrated within the surface boundaries of cores. In Fig. 1-1, assume that the field B is confined entirely to the two core legs A and B with total flux values of ϕ_A and ϕ_B , respectively. The flux in each of these legs closes through some external magnetic structure. If the closed path P encircles these legs N_A and N_B times, as shown, then the total flux linking the path is actually $N_A \phi_A + N_B \phi_B$.

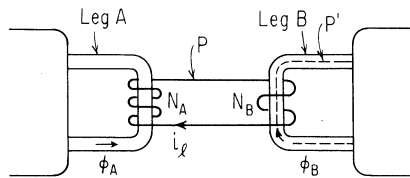


Fig. 1-1. Interconnecting two magnetic legs with a coupling loop of N_A and N_B turns; polarities are consistent with $+d\phi_A/dt$ or $+d\phi_B/dt$ inducing a positive loop current i_l .

Consider next a vector current density J that generates a magnetic field, according to another of Maxwell's equations

$$\text{curl } \mathbf{H} \equiv \nabla \times \mathbf{H} = \mathbf{J} \quad (1-5)$$

The displacement-current term $\partial \mathbf{D} / \partial t$ that normally belongs in this equation is omitted here because it is generally negligible in the circuits in which we are primarily interested. Equation (1-5) can be converted to the integral form

$$\oint_{P'} \mathbf{H} \cdot d\mathbf{l} = \oint_{A'} \mathbf{J} \cdot d\mathbf{A} \quad (1-6)$$

usually referred to as Ampere's law, where P' is a closed path and A' is any surface bounded by P' . The line integral of \mathbf{H} is the loop mmf F , and $\int \mathbf{J} \cdot d\mathbf{A}$ is the total current linkage of the closed loop P' . For a set of discrete currents i_j linking P' we can rewrite Eq. (1-6) as

$$F = \sum_j N_j i_j \quad (1-7)$$

If P' follows along Leg B, then the component of mmf generated by current i_ℓ is $N_B i_\ell$, with direction given by the familiar right-hand rule.

From Fig. 1-1 we see that any flux change in Leg A threads the electric loop N_A times and that any loop current encircles Leg A the same number of times. This illustrates that the number of *inter*linkages between a magnetic leg and an electric loop is actually independent of which one wraps around the other. It also brings out the distinction between total flux linkage through an electric loop, versus simply the flux in a magnetic leg, and similarly for total current linkage through a magnetic core versus simply the current in a conductor.

Figure 1-2 shows the general circuit configuration to be considered in the following sections, in which we analyze separately the effects of resistive, inductive, and capacitive loads on a core connected to a drive current i_d applied through N_d turns. We will assume some highly simplified core characteristics that are adequate for the purposes of this chapter, and, in fact, for most of Part I.

First we assume that the core exhibits the idealized static ϕ - F hysteresis loop shown in Fig. 1-3(a). By the term *static*, it is meant that this is the curve that would be traced out if the mmf F were changed very slowly (quasi-statistically) in time and the corresponding ϕ values plotted. The horizontal top and bottom of the loop represent positive and negative flux saturation levels and the

vertical sides imply that flux changes between negative and positive saturation with $|F|$ only slightly greater than the *threshold* value F_0 . An actual curve has finite slopes at the top and bottom, which account for an inductive component in switching, often referred to as the elastic-flux component. (The source of this component is discussed in detail in Chap. 12.) In any case, if a core is driven into saturation and the drive is then reduced to zero, that is, $F = 0$, the resulting remanent flux level is designated as ϕ_r . A core with a hysteresis loop approaching the ideal shape shown in Fig. 1-3(a) is commonly referred to as having a *square-loop* characteristic.

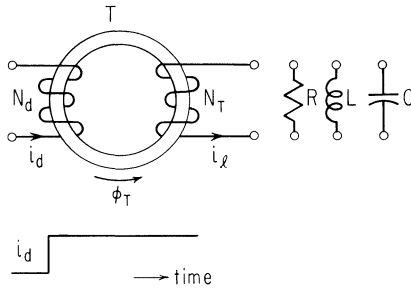


Fig. 1-2. General circuit to be analyzed with a resistive, inductive, or capacitive load connected separately.

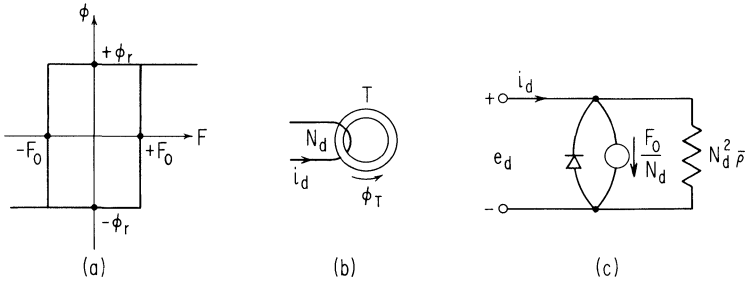


Fig. 1-3. Equivalent circuit for a core, based on an idealized $\phi - F$ loop.

In addition to this simple static model, we assume for most purposes in Part I that dynamic change of flux $\dot{\phi} \equiv d\phi/dt$ in the range $-\phi_r < \phi < \phi_r$ is governed by the relation

$$\dot{\phi} = \bar{\rho}(F - F_0) \quad \text{for } F > F_0$$

and

$$\dot{\phi} = \bar{\rho}(F + F_0) \quad \text{for } F < -F_0$$

(1-8)

where $\bar{\rho}$ (the average value of the inelastic switching parameter ρ) is a constant and where F is equal to the mmf $\sum_j N_j i_j$. According to this model, the rate of flux change is proportional to the *excess* mmf, i.e., the amount by which F exceeds the threshold F_0 . In Chap. 12 it is shown that the switching parameters are by no means constant, as assumed here for $\bar{\rho}$ and F_0 , but depend strongly on the instantaneous flux state, on how this state was reached, and also on F itself. Since the models for ρ and F_0 developed in Chap. 12 are relatively complex, we have chosen here to assume constant values of $\bar{\rho}$ and F_0 for mathematical simplicity in demonstrating principles. Curves subsequently calculated from the switching model of Eq. (1-8) are therefore accurate only in their grosser aspects.

Based on this model, there is a simple electrical equivalent circuit for a core under the conditions that $|\phi| < \phi_r$ and $F \geq F_0$. In Fig. 1-3(b) is shown a core with no coupling-load. For simplicity, the winding for i_d is drawn as if to link the core only once, but N_d linkages are assumed. The emf e_d due to switching is

$$e_d = \bar{\rho} N_d (N_d i_d - F_0) = N_d^2 \bar{\rho} \left(i_d - \frac{F_0}{N_d} \right) \quad (1-9)$$

This expression may be represented by the equivalent circuit of Fig. 1-3(c), where the diode is assumed to have zero forward resistance and infinite back resistance. This ideal diode and the current generator F_0/N_d in parallel with it together behave as a current sink accepting all input current i_d up to the value F_0/N_d , without supporting any voltage. For $i_d > F_0/N_d$, the diode is cut off and $e_d > 0$. The equivalent circuit is valid until the core saturates, i.e., until a time τ such that $\phi = +\phi_r$ or $\Delta\phi = 2\phi_r$, where

$$\int_0^\tau \dot{\phi}_T dt = \frac{1}{N_d} \int_0^\tau e_d dt = 2\phi_r \quad (1-10)$$

assuming the core starts in negative saturation $-\phi_r$. When the core saturates at $+\phi_r$, and therefore terminates switching, the equivalent switching resistance becomes zero and the core effectively represents a short circuit except for the inductance term due to the elastic-flux component, which is ignored in this chapter.

1-2 Resistive Load; $\Delta\phi$ Dissipation

Consider the case in which the coupling loop of Fig. 1-2 connects the core T , called a transmitter core, to a resistive element. The loop inductance is assumed negligible. The core is driven by a step $i_d(t)$ current pulse from an initial state $\phi = -\phi_r$. During the pulse the net mmf drop F in the core is $N_d i_d - N_T i_\ell$ and hence from Eq. (1-8)

$$\dot{\phi}_T = \bar{\rho}(N_d i_d - N_T i_\ell - F_0) \quad (1-11)$$

Current i_ℓ is equal to e_T/R , where $e_T = N_T \dot{\phi}_T$. Hence

$$i_\ell = \frac{N_T \dot{\phi}_T}{R} \quad (1-12)$$

Solution of the above two equations yields

$$\dot{\phi}_T = \bar{\rho}(N_d i_d - F_0) \frac{R}{R + N_T^2 \bar{\rho}} \quad (1-13)$$

and

$$i_\ell = \bar{\rho}(N_d i_d - F_0) \frac{N_T}{R + N_T^2 \bar{\rho}} \quad (1-14)$$

Note that the effect of the resistive loading is to reduce the rate of switching by the factor $R/(R + N_T^2 \bar{\rho})$, relative to the no-load case. If $R \rightarrow 0$, then $\dot{\phi}_T \rightarrow 0$, and the core cannot be switched in finite time. For the case $R = 0$, there is in a sense no "receiver" in the coupling loop to accept any transmitter flux-linkage change $N_T \Delta\phi_T$. This is a useful interpretation that is worth pursuing further. By integration of Eq. (1-12) with respect to time, we have

$$N_T \Delta\phi_T = \int_0^t R i_\ell dt = R q_\ell \quad (1-15)$$

where q_ℓ is the net electric charge flow in the loop. The quantity $R q_\ell$ may be viewed as an equivalent flux-linkage change $N \Delta\phi = R q_\ell$ absorbed by the resistance. It is sometimes useful to think of this process as "dissipation" of flux linkage, or alternatively as $\Delta\phi$ dissipation of an amount $R q_\ell / N_T$. When flux transfer from a transmitter core to a receiver core is considered in Chap. 2, dissipation of a $\Delta\phi$ in the coupling-loop resistance will be found to be an

important loss term subtracting from the $\Delta\phi$ otherwise available to the receiver core.

We could also derive Eqs. (1-13) and (1-14) by extending the equivalent circuit introduced in Fig. 1-3. Let Eq. (1-11) be re-written in the form

$$e_d = N_d \dot{\phi}_T = \bar{\rho} N_d^2 \left(i_d - \frac{F_0}{N_d} - \frac{N_T}{N_d} i_l \right) \tag{1-16}$$

The term $N_T i_l / N_d$ is the only one not accounted for in the previous equivalent circuit, and it may be viewed as a current in the secondary of an ideal transformer of turns ratio $N_d : N_T$, as shown in Fig. 1-4. The ideal transformer and the load R may in turn be replaced by an equivalent resistance $(N_d^2 / N_T^2) R$, and from this equivalent circuit Eqs. (1-13) and (1-14) can be derived directly.

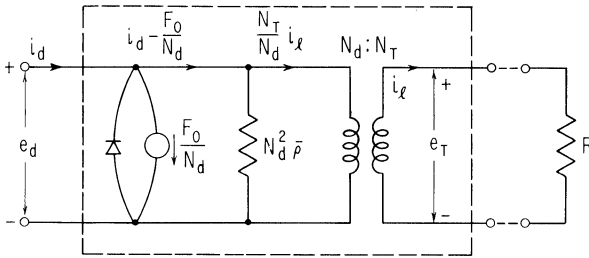


Fig. 1-4. Equivalent circuit of a core driven by current i_d through N_d turns and loaded by resistance R across N_T turns.

For the simple flux-switching model assumed here, the circuit within the dashed boundary in Fig. 1-4 is valid regardless of the nature of the excitation and load at the terminals as long as $F > F_0$ and $|\phi| < \phi_r$. In conventional transformer terms, the differential switching resistance $N_d^2 \bar{\rho}$ is just a core-loss resistance (in ferrite cores, due primarily to internal damping effects rather than eddy currents). This loss element and the current sink of value F_0 / N_d represent the departures from an ideal transformer. It should be emphasized once more that for quantitative analysis of core dynamics, it is necessary to make use of the more accurate flux-switching models described in Chap. 12.

1-3 Inductive Load; $\Delta\phi$ Storage

Let us next consider the case where the transmitter core in Fig. 1-2 is loaded only by a linear inductance. The emf $L di_l / dt$

induced in the load must be exactly balanced by the emf across the core, since we are assuming zero loop resistance. Hence

$$N_T \frac{d\phi_T}{dt} = L \frac{di_\ell}{dt} \quad (1-17)$$

or, by integration

$$N_T \Delta\phi_T = L\Delta i_\ell \quad (1-18)$$

Recalling that self-inductance is defined as the change in flux linkage per unit change of current in the same element, then $L\Delta i_\ell$ is simply the change in flux linkage for a change Δi_ℓ in loop current. This quantity represents all the flux linkage of the loop outside the core, including the contribution from wire inductance as well as any lumped inductance in the loop.

Assume now that the step $i_d(t)$ current pulse causes the core to switch, given the initial conditions $\phi = -\phi_r$ and $i_\ell = 0$. As flux switches, the load current i_ℓ increases according to $i_\ell = (N_T/L)\Delta\phi_T$. But, in accordance with Eq. (1-11), as i_ℓ increases, the rate of flux switching necessarily decreases. By substituting Eq. (1-11) into Eq. (1-17) we obtain

$$\frac{di_\ell}{dt} + \left(\frac{N_T^2 \bar{\rho}}{L}\right) i_\ell = \left(\frac{N_T \bar{\rho}}{L}\right) (N_d i_d - F_0) \quad (1-19)$$

Since i_d is constant during switching, Eq. (1-19) is simply a first-order linear differential equation whose solution is

$$i_\ell = \frac{N_d i_d - F_0}{N_T} \left(1 - e^{-(N_T^2 \bar{\rho}/L)t}\right) \quad (1-20)$$

Thus, any changes in output current i_ℓ are associated with an L/R time constant, where $R = N_T^2 \bar{\rho}$ is the equivalent resistance of the core as viewed across the N_T turns.

Equation (1-20) is valid only so long as the core flux does not reach saturation. If ϕ_T reaches the value $+\phi_r$, then $\dot{\phi} = 0$ and we see from Eq. (1-18) that i_ℓ remains constant at the value $N_T(2\phi_r)/L$. Otherwise, we see from Eq. (1-20) that i_ℓ approaches the asymptotic value

$$i_\ell^{\max} = \frac{N_d i_d - F_0}{N_T} \quad (1-21)$$

and the net current linkage of the core is then equal to the threshold value F_0 .

For a given amplitude of i_d , there exists a unique value of inductance L_c for which $\Delta\phi_T$ approaches $2\phi_r$ exactly in conjunction with i_ℓ approaching the maximum value given by Eq. (1-21). For this value of inductance, in other words, the net mmf $N_d i_d - N_T i_\ell$ drops toward threshold just as the core approaches positive saturation. From Eqs. (1-18) and (1-21) we have

$$\frac{N_T(2\phi_r)}{L_c} = \frac{N_d i_d - F_0}{N_T} \quad (1-22)$$

or

$$L_c = \frac{N_T^2(2\phi_r)}{N_d i_d - F_0} \quad (1-23)$$

For $L < L_c$, the loop current reaches its maximum value before the core saturates, and we see from Eqs. (1-18), (1-21), and (1-23) that

$$\Delta\phi_T^{\text{final}} = \frac{L}{L_c}(2\phi_r) \quad (1-24)$$

For $L > L_c$, the core saturates before the loop current reaches i_ℓ^{max} , and the final value of i_ℓ is

$$i_\ell^{\text{final}} = \frac{L_c}{L} i_\ell^{\text{max}} \quad (1-25)$$

For $L > L_c$, the time τ that it takes for the core to saturate can be found by solving Eq. (1-20) for the time required for the current to build up to i_ℓ^{final} . We find

$$e^{-(N_T^2 \bar{\rho}/L)\tau} = 1 - \frac{L_c}{L} \quad (1-26)$$

or

$$\tau = \frac{L}{N_T^2 \bar{\rho}} \ln\left(\frac{1}{1 - (L_c/L)}\right)$$

For $L = \infty$, (that is, for an open secondary), the simple result $\tau = 2\phi_r/\bar{\rho}(N_d i_d - F_0)$ can be derived from Eqs. (1-26) and (1-23).

A family of curves of load current as a function of time, for a rectangular drive pulse of duration T_1 , is shown in Fig. 1-5. Note that the load current is in a direction tending to switch the core back toward $-\phi_r$. If $i_\ell > F_0/N_T$ at $t = T_1$, then for $t > T_1$, i_ℓ decays towards a final value of F_0/N_T with the same time constant $L/N_T^2\bar{\rho}$ found in Eq. (1-20). As a result, the core switches back by the amount $(L/N_T)[i_\ell - (F_0/N_T)]$, and the net flux change is LF_0/N_T^2 , in agreement with Eq. (1-18).

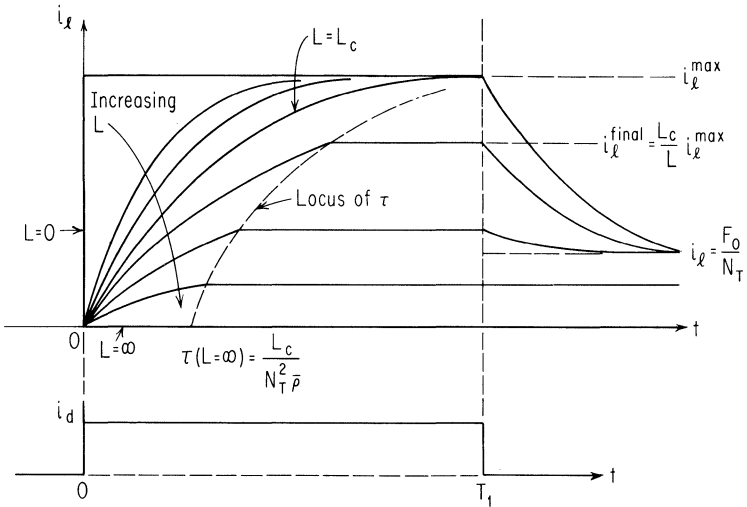


Fig. 1-5. Loop current i_ℓ as a function of time in the circuit of Fig. 1-2 with an inductive load.

It is very useful to consider the notion of a flux-linkage change Li_ℓ , or flux change $\Delta\phi = Li_\ell/N_T$, as being "stored" in the inductance. This is based on the observation that the inductor can actually drive the core, returning some flux linkage to it (the inductance being the transmitter in this case), provided the loop current exceeds the core threshold F_0/N_T after the drive i_d terminates. However, in any actual circuit where loop resistance is not zero, $\Delta\phi$ storage in inductance can only be temporary, since any flux linkage not returned to the transmitter core is eventually dissipated in the resistance.

1-4 Capacitive Load; $\Delta\phi$ Transformation

The effects of capacitive loading are qualitatively different from those for inductive loading, although one might correctly

guess that there is an RC time constant associated with the load current, where $R = N_T^2 \bar{\rho}$ is again the switching resistance of the core, as viewed from the capacitor.

Consider the circuit of Fig. 1-2 with only the capacitor attached. Assuming that the capacitor is not charged initially, the voltage across the core winding must also be zero initially, implying a starting value of load current $i_\ell = (N_d i_d - F_0)/N_T$. As the capacitor charges and its voltage increases, the load current must decrease to permit the core to switch correspondingly faster. The equation of voltage buildup can be obtained as follows. Substitution of the relations $i_\ell = C dv_C/dt$ and $v_C = e_T = N_T \dot{\phi}_T$ into Eq. (1-11) results in

$$\frac{dv_C}{dt} + \frac{v_C}{RC} = \frac{\bar{\rho} N_T (N_d i_d - F_0)}{RC} \tag{1-27}$$

with the solution

$$v_C = \bar{\rho} N_T (N_d i_d - F_0) (1 - e^{-t/RC}) \tag{1-28}$$

where $R = N_T^2 \bar{\rho}$. A family of curves of v_C versus t , with C as a parameter, is shown in Fig. 1-6. Note that all curves tend to build to the same asymptotic value of voltage, $v'_C = \bar{\rho} N_T (N_d i_d - F_0)$. This is not surprising, for if the core did not saturate, equilibrium would finally be reached with zero load current and a constant output voltage $v'_C = N_T \dot{\phi}_T$ whose value would depend only on the drive strength. Thus, with a capacitive load, a switching voltage $N_T \dot{\phi}_T$ can be sustained without any load current i_ℓ , whereas with an R or L load, a nonzero value of $\dot{\phi}$ is not possible unless a loop current i_ℓ is flowing (and changing in the latter case).

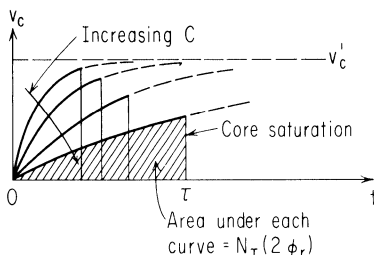


Fig. 1-6. Output voltage v_C as a function of time in the circuit of Fig. 1-2 with a capacitive load.

Integrating Eq. (1-28) in order to find the flux change, we obtain

$$N_T \Delta \phi_T \doteq \int_0^t v_C dt = v_C' RC \left[\frac{t}{RC} - (1 - e^{-t/RC}) \right] \quad (1-29)$$

From this equation we see that flux switched in the core increases monotonically with time until the core saturates. Saturation occurs at a time found by substituting $\Delta \phi_T = 2\phi_r$ into Eq. (1-29). When the core saturates at $+\phi_r$, the switching resistance of the core drops to zero, and the capacitor discharges rapidly, the discharge current driving the core still further into positive saturation. There is, of course, an abrupt drop in voltage when saturation is reached, as indicated in the family of curves of Fig. 1-6. (In actual practice, there would be a damped oscillation after saturation is reached because of the saturation inductance of the core and the parasitic inductance and resistance of the coupling loop.) The areas under the curves in Fig. 1-6 are clearly identical, since each curve represents the same magnitude of flux switching, namely, $2\phi_r$.

Here we must note a very important difference between capacitive and inductive loading. An inductive load tends to maintain the load current in the same direction after termination of drive, whereas the capacitive discharge current is opposite to that of the initial charging current. Thus, whereas the inductor discharge current tends to switch the core back toward its original state, the capacitive discharge current tends to keep the core switching in the *same* direction as originally (see the examples in Fig. 12-30).

Let us finally consider the case of terminating the drive current before saturation is reached, at time t_1 in Fig. 1-7. From the arguments above, the capacitor discharge current will keep the core switching in the same direction for some time. The pertinent equation in this case is

$$\frac{dv_C}{dt} + \frac{v_C}{RC} = -\frac{\bar{\rho} N_T F_0}{RC} \quad (1-30)$$

with the solution

$$v_C = v_C(t_1) e^{-t/RC} - \bar{\rho} N_T F_0 (1 - e^{-t/RC}) \quad (1-31)$$

where again $R = N_T^2 \bar{\rho}$, and $v_C(t_1)$ is the value of voltage reached when the drive is terminated. A typical response curve is shown in Fig. 1-7(a).

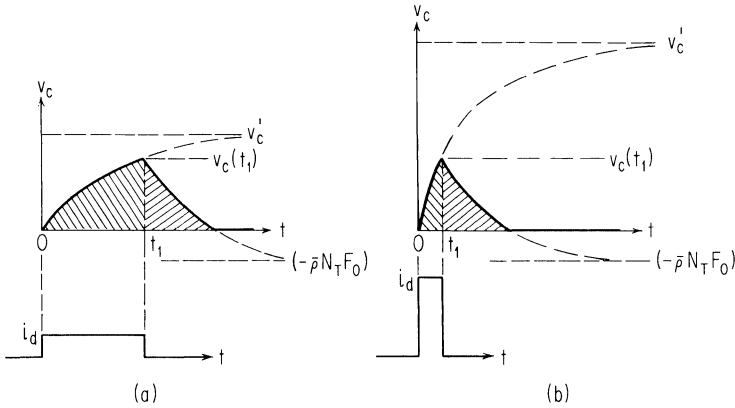


Fig. 1-7. Changing the ratio of flux switched during the drive pulse to that switched after the drive pulse from >1 in (a) to <1 in (b), by varying the magnitude of i_d .

An important observation is that the magnitude of flux switched subsequent to drive termination can actually be *larger* than that switched by the drive itself. We can see this from the following argument. With a stronger drive, the voltage builds towards a higher asymptotic value, and therefore the capacitor can be charged to the same value in shorter time. Thus, the area under the buildup portion of the curve can, in principle, be made vanishingly small, although the curve during discharge is totally unaffected by the initial drive strength. For example, compare the curves of Fig. 1-7(a) and (b). In the limit of very strong drive, we have the possibility of charging the capacitor to any specified voltage with a negligible amount of core flux being switched.

A capacitor thus offers an interesting capability of $\Delta\phi$ *transformation*, the capacitor being able to deliver to the core more, or less, flux linkage than the core delivers to the capacitor during the charging phase. There is nothing particularly mysterious about this, since there are no basic constraints on the integral of capacitor voltage, even though the voltage itself is unique for any particular charge state. Similarly, in the case of an inductor, the current is fixed for any given flux-linkage state, but there is no basic constraint on the integral of current, i.e., on charge.

1-5 Summary

Using a very simple core model, we have treated separately the cases of core switching with resistive, inductive, and capacitive

loads. With a resistive load, the loop current is simply proportional to $\dot{\phi}$, and flows, therefore, only so long as flux is switching (the flux switching is dissipative). With an inductive load, the loop current is directly proportional to the magnitude of flux change $\Delta\phi$ and this we interpret simply as flux-linkage storage, in the sense that the same magnitude of flux linkage in the core is, so to speak, regenerated in the linear inductance. We are able to define an L/R time constant, where R is the equivalent resistance of the switching core as viewed from the coupling loop winding. With a capacitive load, we find an RC time constant, where R is the same as in the inductive case, and steady state is reached when the voltage generated in the core winding exactly equals that across the capacitor, and no loop current flows. In this case, the magnitude of equivalent flux linkage stored in the capacitor during charge can be less than, equal to, or greater than the flux linkage subsequently delivered from the capacitor during discharge. This is an important property interpreted as $\Delta\phi$ transformation.

This simplified treatment is of little value in quantitative prediction, and is primarily for developing insight into manipulation of flux change as a signal parameter. It should be intuitively clear that the ability to dissipate, store, and transform this parameter is important in circuit synthesis. Quantitative analysis of core switching with various sorts of loads, using a better engineering model for the core, is treated in Sec. 12-6.

COUPLED PAIR OF CORES; $\Delta\phi$ TRANSFER

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In the previous chapter we saw that loading a core with a resistance, an inductance, or a capacitance results in $\Delta\phi$ dissipation, storage, or transformation, respectively. Now let us consider loading a core with another core, in which case we have the possibility of $\Delta\phi$ transfer, i.e., transmission of flux from a transmitter core to a receiver core.

2-1 Flux Transfer Ratio G

The flux transfer takes place through an electrical coupling loop which is assumed for the moment to be purely resistive (Fig. 2-1(a)). For such a coupled pair of cores, we are generally concerned with the $\Delta\phi$ transfer ratio

$$G(\Delta\phi_T) = \frac{\Delta\phi_R}{\Delta\phi_T} \quad (2-1)$$

where $\Delta\phi_R$ and $\Delta\phi_T$ are the flux changes in the receiver and transmitter, respectively. In contrast with conventional electronic circuits, the appropriate signal parameter here is $\Delta\phi$, rather than voltage or current, and of special concern are the conditions for achieving a transfer ratio $G > 1$.

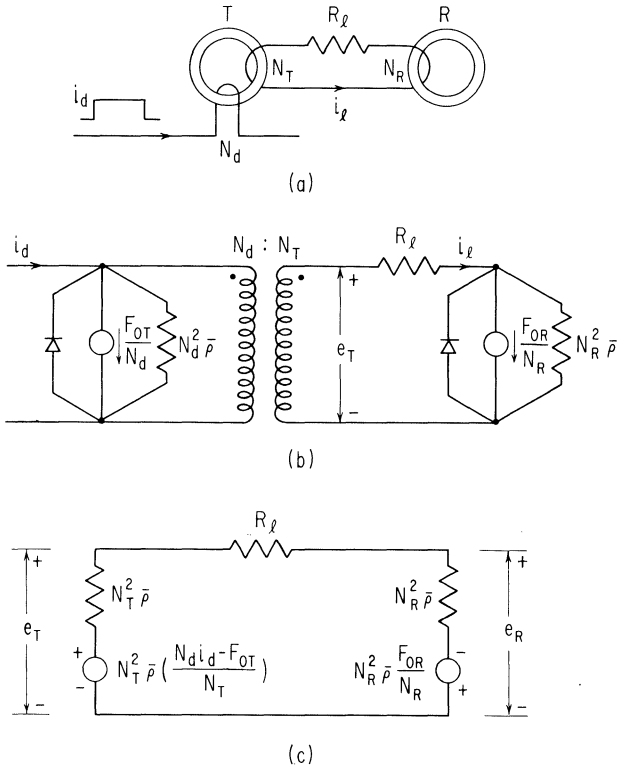


Fig. 2-1. Flux transfer from Transmitter Core T to Receiver Core R.

Assume that each of the coupled cores starts in the $-\phi_r$ flux state and switches towards the $+\phi_r$ state, as governed by the flux-switching model of Eq. (1-8). A transmitter drive pulse i_d of constant magnitude is also assumed. Under these assumptions, the rates of change of flux $\dot{\phi}_T$ and $\dot{\phi}_R$ are independent of time (as long as neither core reaches positive saturation), and the transfer ratio G is simply equal to the ratio of switching rates, or

$$G = \frac{\Delta\phi_R}{\Delta\phi_T} = \frac{\dot{\phi}_R}{\dot{\phi}_T} \tag{2-2}$$

In this chapter we are primarily concerned with the general effects on the transfer ratio of turns ratio, loop impedance, receiver threshold, and receiver loading resistance.

2-2 Requirement on Turns Ratio for $G > 1$

In the circuit of Fig. 2-1(a), the coupling loop is assumed to have a resistance R_ℓ , but negligible inductance. Equating the net emf around the loop to the voltage drop in R_ℓ , we have

$$N_T \dot{\phi}_T - N_R \dot{\phi}_R = R_\ell i_\ell \quad (2-3)$$

Integrating each term with respect to time, and rearranging, we obtain

$$N_T \Delta\phi_T = N_R \Delta\phi_R + R_\ell q_\ell \quad (2-4)$$

where $q_\ell = \int_0^t i_\ell dt$. This equation is similar to Eq. (1-15) for resistive loading except that of the transmitted flux linkage here, only part, namely, $R_\ell q_\ell$, is dissipated as a loss in R_ℓ , and the remainder $N_R \Delta\phi_R$ reaches the receiver core.

Based on Eqs. (2-1) and (2-4), we may write

$$G = \frac{N_T}{N_R} - \frac{R_\ell q_\ell}{N_R \Delta\phi_T} = n \left(1 - \frac{R_\ell q_\ell}{N_T \Delta\phi_T} \right) \quad (2-5)$$

where n is the turns ratio N_T/N_R . Thus, despite the inevitable loss of flux linkage during transfer, transfer gain $G > 1$ is nevertheless possible if $n > 1$ by an amount sufficient to overcome the effect of the subtractive term $R_\ell q_\ell/N_T \Delta\phi_T$. Note that this term is just the ratio of dissipated flux linkage to transmitted flux linkage.

2-3 Limit on Loop Resistance

Let us now assume that $n > 1$ and consider how large R_ℓ can be while maintaining $G \geq 1$. Based on our simple model, the circuit of Fig. 2-1(a) may be represented by the equivalent circuit shown in Fig. 2-1(b). The cores are assumed identical, with the same $\bar{\rho}$ and the same threshold value $F_0 = F_{0T} = F_{0R}$, though the latter symbols are kept distinct for the purpose of discussing transmitter and receiver thresholds separately.

Assuming that the drive current i_d is large enough to make $N_R i_\ell \geq F_{OR}$, the diodes in the core model are nonconducting and may be neglected. Then with current generators transformed to equivalent voltage generators, and all quantities referred to the transformer secondary, we obtain the equivalent circuit of Fig. 2-1(c) where $e_T = N_T \dot{\phi}_T$ and $e_R = N_R \dot{\phi}_R$. Under the specified condition of $G \geq 1$, it is clear that the highest upper limit on loop resistance is obtained when the effective receiver threshold is equal to zero. This condition can be approached with strong driving so that $N_d i_d \gg F_0$. Alternately, the receiver threshold can be effectively reduced by applying a bias mmf $N_b i_b = F_0$, as shown applied to both cores in Fig. 2-2. The term *bias* is used in the usual electrical engineering sense of determining an operating point, the bias signal by itself nominally not causing any flux switching. It may be either a dc bias or a constant-amplitude pulse synchronized with the current i_d .

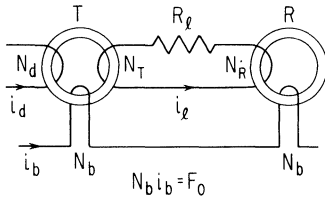


Fig. 2-2. Use of a bias mmf to overcome the switching thresholds of transmitter and receiver.

With the transmitter and receiver each biased to threshold, that is, with $N_b i_b = F_0$, we simply have

$$\dot{\phi}_R = \bar{\rho} N_R i_\ell \quad (2-6)$$

and

$$\dot{\phi}_T = \bar{\rho} (N_d i_d - N_T i_\ell) \quad (2-7)$$

Equations (2-6) and (2-3) may be solved for G in the form

$$G = \frac{\dot{\phi}_R}{\dot{\phi}_T} = n \frac{N_R^2 \bar{\rho}}{R_\ell + N_R^2 \bar{\rho}} \quad (2-8)$$

This result is also clear from the equivalent circuit of Fig. 2-1(c), where, with receiver threshold cancelled out, the emf ratio $e_R/e_T = N_R \dot{\phi}_R/N_T \dot{\phi}_T$ is readily seen to be equal to $N_R^2 \bar{\rho}/(R_\ell + N_R^2 \bar{\rho})$.

The above results may be interpreted as follows: of the total flux linkage $N_T \Delta \phi_T$ injected into the loop, a fraction G/n reaches the receiver core, and the remaining portion $1 - G/n$ is lost by dissipation in R_ℓ . The exact division of transmitted flux linkage is generally very dependent on drive magnitude $N_d i_d$, and is independent of drive here only because of our assuming idealized core properties and the biasing of the receiver core exactly to threshold.

Based on the requirement that $G \geq 1$, we obtain directly from Eq. (2-8) an upper limit on R_ℓ , namely

$$R_\ell \leq (n - 1)N_R^{2\bar{\rho}} \quad (2-9)$$

from which we see that there is no limit on the ratio $R_\ell/N_R^{2\bar{\rho}}$ so long as n can be made arbitrarily large. But by rewriting Eq. (2-9) in terms of transmitter resistance $N_T^{2\bar{\rho}}$, we find

$$R_\ell \leq \left(\frac{n - 1}{n^2}\right)N_T^{2\bar{\rho}} \quad (2-10)$$

and thus see that the upper limit on $R_\ell/N_T^{2\bar{\rho}}$ is $1/4$, which is obtained with a two-to-one turns ratio ($n = 2$), in which case $N_R^{2\bar{\rho}} = R_\ell$. In other words, for $G \geq 1$ the loop resistance can never be more than $1/4$ the transmitter resistance.

There are many other important factors relevant to choice of coupling-loop turns ratio. The simple result here is most likely to be significant where there is practical difficulty in constructing a low-resistance coupling loop. In that case, it may be helpful to specify $N_T/N_R = 2$ in order to allow as large a value of R_ℓ as possible relative to $N_T^{2\bar{\rho}}$.

2-4 Effect on G of Transmitter and Receiver Thresholds

It is not always possible, or even desirable, to eliminate the core thresholds by bias, so it is necessary to understand the effects of threshold on the transfer ratio. Let us consider the case of constant drive and no biasing at all. From the equivalent circuit of Fig. 2-1(c), we can write

$$i_\ell = \frac{N_T^{2\bar{\rho}} [(N_d i_d - F_{0T})/N_T] + N_R^{2\bar{\rho}} (F_{0R}/N_R)}{N_T^{2\bar{\rho}} + R_\ell + N_R^{2\bar{\rho}}} \quad (2-11)$$

and

$$e_T = N_T \dot{\phi}_T = N_T^{2\bar{\rho}} \left(\frac{N_d i_d - F_{0T}}{N_T} - i_\ell \right) \quad (2-12)$$

For substitution into Eq. (2-5), we obtain the ratio

$$\frac{R_\ell q_\ell}{N_T \Delta \phi_T} = \frac{R_\ell \int_0^t i_\ell dt}{N_T \int_0^t \phi_T dt} = \frac{R_\ell i_\ell}{N_T \dot{\phi}_T} \quad (2-13)$$

Substitution of this ratio, as evaluated from Eqs. (2-11) and (2-12), into Eq. (2-5) yields

$$G = n \left(\frac{n N_R^2 \bar{\rho} (N_d i_d - F_{0T}) - (R_\ell + N_T^2 \bar{\rho}) F_{0R}}{n (R_\ell + N_R^2 \bar{\rho}) (N_d i_d - F_{0T}) - N_T^2 \bar{\rho} F_{0R}} \right) \quad (2-14)$$

Equation (2-14) is valid only if $N_d i_d$ is large enough that $N_R i_\ell \geq F_{0R}$. The limiting condition $G = 0$, corresponding to $N_R i_\ell = F_{0R}$, is obtained when $N_d i_d$ has the critical value

$$(N_d i_d)_c = F_{0T} + n \left(1 + \frac{R_\ell}{N_T^2 \bar{\rho}} \right) F_{0R} \quad (2-15)$$

For any lower value of drive, $G = 0$ also.

The form of G as a function of $N_d i_d$ has been sketched in Fig. 2-3. Note that for $N_d i_d \gg (N_d i_d)_c$, G approaches asymptotically the value given by Eq. (2-8), since the threshold terms become relatively insignificant. Also note that if we view F_{0T} and F_{0R} as the effective thresholds, then for the previous case of receiver biasing, that is, $F_{0R} = 0$, Eq. (2-14) again reduces to Eq. (2-8). In this case, the transmitter threshold has no effect on the transfer ratio G , although the individual rates of switching are lower than they would be if F_{0T} were zero also. In fact, from Eq. (2-14) we see that the effect of nonzero F_{0T} on G may always be overcome simply by increasing $N_d i_d$ by the amount F_{0T} , which is equivalent to biasing the transmitter. The effect of nonzero F_{0R} in reducing G ,

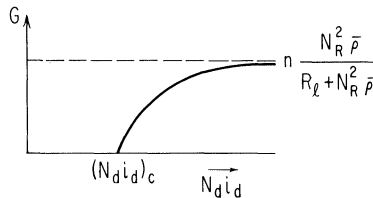


Fig. 2-3. Sketch of flux-transfer ratio as a function of drive strength, from Eq. (2-14).

however, cannot be completely overcome with any finite value of $N_d i_d$.

2-5 Effect on G of Coupling-Loop Inductance

The control of coupling-loop inductance L_ℓ is often as important as the control of the resistance R_ℓ . When L_ℓ is taken into account, the values of i_ℓ and $\dot{\phi}$ are no longer constant in time. Omitting detailed analysis here, it can be reasoned that storage of the flux linkage $L_\ell i_\ell$ in L_ℓ is at least a temporary flux loss en route to the receiver. Furthermore, if the receiver stops switching at time T_S (whether due to saturation or to lack of sufficient mmf), then a flux linkage equal to $L_\ell i_\ell(T_S)$ is left stored in L_ℓ , and this is transformed into a permanent flux-linkage loss dissipated in R_ℓ as i_ℓ decays exponentially.

2-6 Effect on G of Receiver Loading

For the circuit of Fig. 2-2, we say that $G \geq 1$ can be obtained for any value of R_ℓ by making the turns ratio n sufficiently large. However, if the receiver is also loaded, it may not be possible to obtain $G \geq 1$ for any value of n . Consider, for example, the case in Fig. 2-4(a), where the secondary winding of the receiver contains the same number of turns N_T as that of the transmitter. For

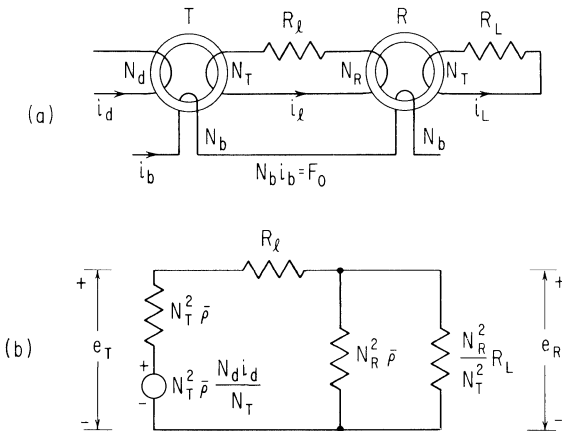


Fig. 2-4. Loading the receiver with resistance R_L through a winding of N_T turns.

the special case of $R_L = R_\ell$, this circuit may be viewed as deriving from an iterative core circuit in which the next core in the chain beyond Core R is in some manner prevented from switching.

For simplicity of analysis, and in order to minimize the effect of receiver loading, both cores are again assumed biased to threshold. The equivalent circuit of Fig. 2-1(c) may then be expanded to include the load by connecting R_L as shown in Fig. 2-4(b). Solving for the ratio e_R/e_T from this circuit and noting that

$$G = \frac{\dot{\phi}_R}{\dot{\phi}_T} = \frac{e_R/N_R}{e_T/N_T}$$

we obtain

$$G = \frac{n}{n^2(R_\ell/R_L) + (R_\ell/N_R)^{2\bar{\rho}} + 1} \quad (2-16)$$

For the case of equal loop resistances $R_L = R_\ell$, Eq. (2-16) reduces to

$$G(n, R_\ell) = \frac{n}{n^2 + (R_\ell/N_R)^{2\bar{\rho}} + 1} \quad (2-17)$$

With respect to R_ℓ , the largest value of G ,

$$G(n) = \frac{n}{n^2 + 1} \quad (2-18)$$

is obtained as $R_\ell/N_R^{2\bar{\rho}} \rightarrow 0$, and maximization of Eq. (2-18) with respect to the turns ratio $n = N_T/N_R$ yields

$$G_{\max} = \frac{1}{2} \quad (2-19)$$

for $n = 1$. Thus, with $R_L = R_\ell$ it is not only impossible to achieve $G \geq 1$ with a large turns ratio, but rather $n = 1$ results in the highest possible value of G . Furthermore, with $R_L = R_\ell$, we obtain the highest gain not by making R_L large, but rather for the heaviest possible receiver loading, i.e., as $R_L \rightarrow 0$. The latter result merely means that G is more affected by the coupling-loop resistance than by the loading resistance.

Since $G \geq 1$ cannot be obtained for $R_L = R_\ell$, let us derive the minimum value of R_L/R_ℓ for which the condition $G = 1$ can be

achieved. To emphasize the R_ℓ/R_L dependence, let us assume that R_ℓ is already small compared with $N_R^2\bar{\rho}$ so that Eq. (2-16) becomes

$$G = \frac{n}{n^2(R_\ell/R_L) + 1} \quad (2-20)$$

Hence, for $G \geq 1$

$$\frac{R_L}{R_\ell} \geq \frac{n^2}{n - 1}$$

For $G = 1$, the minimum value

$$\frac{R_L}{R_\ell} = 4 \quad (2-21)$$

is obtained for turns ratio $n = 2$. Thus, with all conditions idealized, it is necessary to have loading resistance at least four times the loop resistance to obtain $G \geq 1$. This result has considerable significance in connection with the iterative core circuits that we shall treat, beginning in the next chapter.

2-7 Flux Pumping

The use of a turns ratio greater than unity could be viewed as the gain mechanism for achieving $G \geq 1$ in the manner shown in the previous sections. We will later describe other gain mechanisms by which it is possible to achieve $G > 1$ even in cases where $N_T/N_R \leq 1$. To illustrate this possibility, let us show here that by the use of multiple transfers we can "pump" the receiver to a fully switched condition even when the transfer ratio is less than unity on any single transfer.

In the circuit of Fig. 2-4(a), suppose that both cores are initially in negative remanence and that we apply a symmetrical pattern of positive and negative currents that drive the transmitter repeatedly between $-\phi_r$ and $+\phi_r$. With $G < 1$, the receiver will then be driven repeatedly between $-\phi_r$ and some flux level lower than $+\phi_r$. The resulting history is sketched in Fig. 2-5(a). With a suitable asymmetry, however, so that the receiver switches less flux in the negative-going direction, the operating level in the receiver approaches closer and closer to positive saturation, as suggested in

Fig. 2-5(b). In other words, we can ultimately achieve a net gain ($G \geq 1$) relative to the $\Delta\phi_T$ transmitted during a single transfer. This is true even if the receiver is heavily loaded with a value of $R_L < R_\ell$.

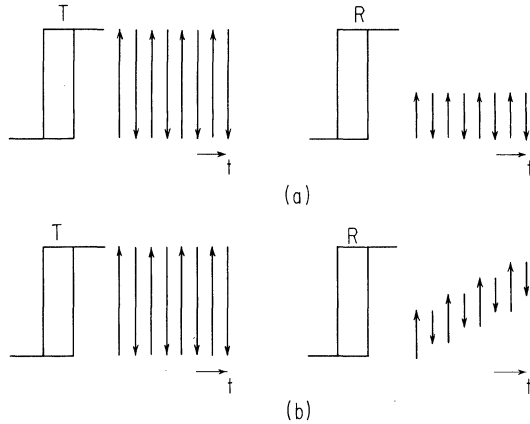


Fig. 2-5. Illustrating symmetrical switching cycles in (a), and showing receiver pumping effect with asymmetrical switching cycles in (b).

As shown by Eq. (2-14), G is a function of drive strength as long as the receiver threshold is nonzero. Hence, suitable asymmetry could be achieved merely by using different drive strengths in the two directions of switching, as in Fig. 2-6(a). A different method is shown in Fig. 2-6(b), where a dc receiver bias aids the loop current in the positive switching direction, but opposes it in the negative switching direction.

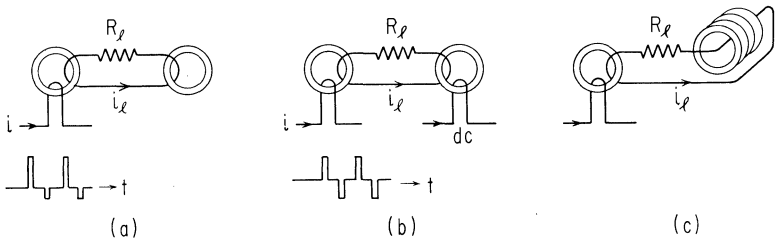


Fig. 2-6. Two different ways to apply dc bias to achieve asymmetrical switching in (a, b); pumping a single transmitter to fully switch a number of identical receiver cores in (c).

If a number of receiver cores are linked by the loop, as in Fig. 2-6(c), all could be pumped to a fully switched level with a

sufficient number of cycles. By doubling the number of pumping cycles, i.e., by doubling the time, we can double the net gain. This becomes a "gain-bandwidth" problem for digital transfer (Chap. 3), since the maximum bit rate is inversely proportional to transfer time. Even within a single cycle there is a gain-bandwidth relation. Net gain per cycle could be increased if the amount of flux switched back during the negative half cycle were reduced. In the limit, if loop current magnitude during the negative half cycle were below the effective receiver threshold, no receiver flux would switch back at all. In this case, the loop resistance would dissipate the entire flux linkage $N_T(-2\phi_p)$ injected by the transmitter, and the time for this operation would be correspondingly increased. We will see that this is an important mode of circuit operation, i.e., a transmitter slowly dissipating a flux-linkage change in loop resistance.

2-8 Direct-Current Drive; Implicit Phasing

A dc mmf less than threshold can serve as a bias source in the conventional sense of setting an operating point. A dc mmf greater than threshold can cause significant switching, however, and therefore act as a driver. For example, in Fig. 2-7 a negative dc mmf normally holds the first core in saturation. Upon application of a positive pulse large enough to overcome the dc mmf plus the core threshold, the first core can be switched to positive saturation, and flux is transmitted to the second core. Upon termination of the pulse, the dc mmf drives the first core back to its original condition. If the dc drive is less than the net positive drive, then with repeated application of the drive pulse, the second core can be pumped as shown in Fig. 2-5(b).

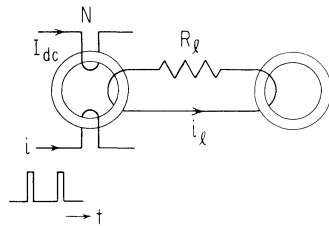


Fig. 2-7. Two-phase operation with a single pulse source and a dc mmf large enough to switch the core back to its original state.

With a dc mmf just slightly above threshold, the first core switches back slowly, and essentially all flux linkage is dissipated in loop resistance during the negative half cycle.

We see that it is possible to have more phases of circuit operation than there are explicit pulse drivers. We can think of the circuit of Fig. 2-7 as having a two-phase nature though only one clock-pulse is needed, the second phase being achieved

implicitly. The use of dc current for this purpose is not only practical but often results in considerably simplified driver systems.

There are two points to note about dc current sources in this type of application. First, there cannot be any *net* energy exchange between the dc current source and any core linked by this source. Starting at time $t = 0$, the net energy transferred from the current source I_{dc} to the core of Fig. 2-7 can be expressed simply as

$$W = \int_{t=0}^t I_{dc} e dt = I_{dc} \int_{t=0}^t N \frac{d\phi}{dt} dt = I_{dc} N (\phi_f - \phi_i) = I_{dc} N \Delta\phi$$

where e is the induced emf in the winding, and ϕ_f and ϕ_i are the final and initial values of the flux, respectively. Thus, there is as much energy delivered from the current source during one polarity of flux change as is delivered back to the source during the opposite polarity of flux change. After each complete cycle of switching, $\phi_f = \phi_i$, or $\Delta\phi = 0$, and there is no net exchange of energy, no matter how complex the circuitry attached to the core.

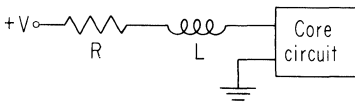


Fig. 2-8. Use of a series inductance to stabilize a dc current source of magnitude $I_{dc} = V/R$.

A current source is often synthesized with a large voltage source V and large series resistance R (where V/R is the desired current), V being large compared to the largest expected voltage drop in the driven circuitry. However, the power lost in the series resistance makes

this type of current source very inefficient. A large improvement can generally be achieved by incorporating an inductance in series with the load. Thus, for a relatively large L in Fig 2-8, a flux-linkage change $\sum N_i \Delta\phi_i$ across the core circuit can be absorbed, or balanced, by a current change on the order of $\Delta I \approx \sum N_i \Delta\phi_i / L$, which can be made arbitrarily small with a large inductance. This is similar to the result in Eq. (1-18) where a change in flux linkage results in a certain change in loop current that subsequently decays with a time constant L/R , where R is the circuit resistance. The use of a series inductance often simplifies the dc-source design and permits the use of much smaller values of V and R than would otherwise be possible. This technique is particularly useful for magnetic-core circuits that are cyclically operated because of the bipolar nature of the load voltages. With unipolar loads, it would be necessary to delay a certain number of L/R time constants

between switching operations in order to prevent cumulative current changes.

2-9 Summary

In this chapter we have treated specifically the case of a second core acting as a load on a first core. Primary interest is in the flux transfer ratio G , the ratio of flux change in the receiving core to the flux change in the transmitting core, and more particularly, in achieving transfer ratios greater than unity, i.e., actual signal gain. An important method for achieving $G > 1$ is to use a turns ratio greater than unity in the coupling loop between transmitter and receiver. We make some basic observations on the effect on the gain of various circuit and device parameters such as loop resistance, loading resistance, and the static thresholds of the transmitter and receiver elements. In particular, maximum limits on loop resistance and load resistance are derived for the condition $G \geq 1$. Another gain mechanism, namely, flux pumping, is also considered, although this is mainly of academic interest. Finally, we consider the practically important case of core switching with a dc current, which, upon termination of a switching pulse, automatically restores the core to its original state.

DIGITAL TRANSFER IN ITERATIVE CORE CIRCUITS

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We wish now to consider some of the basic requirements for synthesizing digital transfer systems. In particular, we will show how cores and diodes, or alternately cores and capacitors, can be used in combination to achieve circuits for digital transfer. Since core-diode circuits are discussed in detail elsewhere, for example, by Meyerhoff (1960), their treatment in this book is limited to the material of this section. Discussion of core-capacitor schemes is also limited to this section, since such circuits are mainly of academic interest and in any case are outside the primary interest of this book. It is considered worthwhile to introduce these schemes before starting the treatment of core-wire schemes in order to develop insight into $\Delta\phi$ gain and loss mechanisms, and into methods for achieving isolation between various parts of a magnetic core circuit. Diodes are obvious devices for achieving isolation, and it is therefore easy to illustrate the principles of digital transfer with core-diode circuits. In Chap. 4 we will use certain of these

core-diode schemes as an introduction to the general synthesis of core-wire schemes.

3-1 Binary Shift Register

A general logic network is a highly interconnected network of digital circuits through which binary variables can be stably transmitted. If we follow any one path of the network, we find many other paths merging with it (fan-in), and other paths branching off from it (fan-out). To simplify the study of digital transmission, it is convenient to concentrate on just the requirements for stable storage and transfer of binary variables along a simple path with no side branches, i.e., a common binary shift register. If a particular circuit scheme can be used to build a shift register, then the basic scheme can almost invariably be expanded for general logic realization. Thus, we can profitably evaluate and compare schemes on the basis of shift register synthesis alone, without becoming much involved in general logic techniques.

A binary shift register is basically a chain of storage elements, such as flip-flops or magnetic cores, so interconnected that the stored binary pattern can be shifted along the chain. The chain may be arbitrarily long and may be closed on itself so that a binary pattern can be continually circulated in the closed loop. We generally speak of an N -bit shift register, where N is the capacity of the register, i.e., the number of bits in the shifting pattern.

There are many ways to structure a register. Suppose, for example, that we have an N -bit binary pattern held in Cells 1 through N of a closed ring of $N + 1$ storage cells, such as in Fig. 3-1. Upon application of clock pulse C_1 , the bit stored in the first cell is advanced into Cell $N + 1$, formerly empty. Upon application of clock pulse C_2 , the bit stored in Cell 2 is advanced into Cell 1, and so on. The shifting occurs in caterpillar fashion in this case, and shifting an N -bit pattern requires $N + 1$ clock sources.

A more common method of structuring is to arrange for shifting all data simultaneously. This mode requires more storage cells but only a small, fixed number of clock drivers,

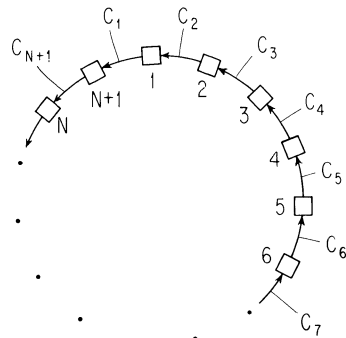


Fig. 3-1. N -bit register with $(N + 1)$ cores and $(N + 1)$ clock sources.

independent of the number of bits N . A common arrangement uses two storage cells per bit and two clock pulses, as shown schematically in Fig. 3-2, where the square boxes represent storage cells and the arrowed lines represent interconnecting circuitry. It is common to refer to the alternate cells as O (for odd) and E (for even). To shift an N -bit pattern that is stored in the O -rank, we activate the coupling circuitry between each O -cell and its right-hand E neighbor, and thereby simultaneously shift the pattern to the E -rank. This is referred to as an $O \rightarrow E$ shift. Next we activate an $E \rightarrow O$ shift, and the pattern is transferred back to the O -rank, but shifted one place to the right as required. The *shifting rate*, or *bit rate*, depends on the time it takes to complete this basic two-phase shift cycle.

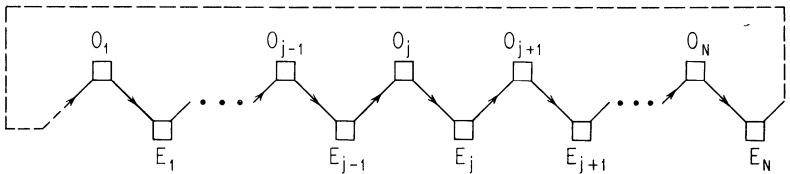


Fig. 3-2. N -bit register with $2N$ cores and two clock sources.

An important aspect of binary transfer is the isolation required between adjacent storage cells. In the transfer from Cell O_j to E_j , during an $O \rightarrow E$ transfer, the switching of E_j must be prevented from affecting the following O_{j+1} cell, i.e., *forward isolation* is required, and the switching or readout from O_j must be prevented from acting on E_{j-1} , which is acting as a receiver from Cell O_{j-1} , i.e., *back isolation* is also necessary. During an $E \rightarrow O$ transfer, the roles must be reversed, the inactivated paths becoming activated, and vice versa.

Although there are other possible shifting schemes, we concentrate primarily on this simultaneous shifting technique, which is the most common. This results in no particular loss of generality.

3-2 Digital Transfer

In the previous section, we represented bistable storage cells symbolically without specifying any particular device technology. Pursuing this symbolic approach, we can derive some important requirements for digital transfer between cells.

Δφ Gain Requirements. The register circuit of Fig. 3-2 is redrawn along a single row in Fig. 3-3(a), with cells renumbered in sequence. Let us follow just one of the bits of the pattern as it moves along the chain. Suppose that the particular bit of interest is initially stored in Cell $j - 1$. At the next shift pulse, there is a transfer from Cell $j - 1$ to Cell j with $\Delta\phi$ transfer ratio

$$G = \frac{\Delta\phi_j}{\Delta\phi_{j-1}} \tag{3-1}$$

where $\Delta\phi_j$ represents the magnitude of flux switched in Cell j , and $\Delta\phi_{j-1}$ is the magnitude of flux simultaneously switched in Cell $j - 1$. We will assume here that the value of $\Delta\phi$ when the cell is acting as a transmitter is the same as the value of $\Delta\phi$ switched when the same cell was previously a receiver (though there are important exceptions, as we shall see in later chapters).

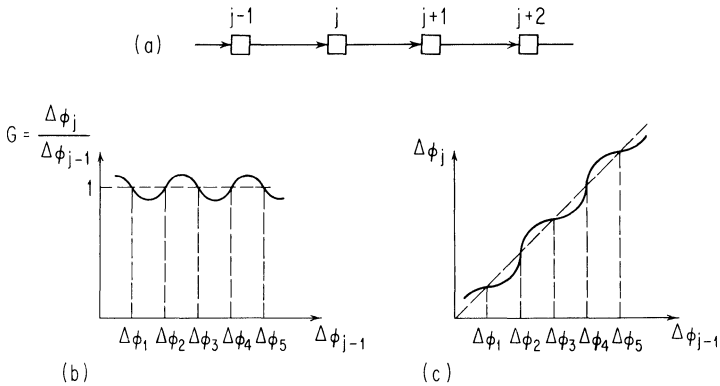


Fig. 3-3. Flux-gain requirements for multistable flux transfer.

If the transfer ratio were exactly unity in each transfer, independent of the magnitude of $\Delta\phi$, then we would have a very useful “analog delay line”; any level of $\Delta\phi$ injected at one end of the chain would emerge unchanged at the far end at a later time. However, the transfer ratio generally depends on many different circuit parameters, and it is impossible to keep these parameters sufficiently controlled to actually achieve unity transfer ratio over a range of $\Delta\phi$ levels. Instead, let us consider different ranges of signal level, and ask what form of gain characteristic $G(\Delta\phi)$ is required to ensure that an initial signal level within any one range should be maintained within that range regardless of the length of the transmission chain. A form of $G(\Delta\phi)$ characteristic that would satisfy this requirement is indicated in Fig. 3-3(b). In some regions $G > 1$, in other regions $G < 1$. At signal levels marked $\Delta\phi_1$ through $\Delta\phi_5$, the gain is exactly unity, but only levels $\Delta\phi_1$, $\Delta\phi_3$, and $\Delta\phi_5$ represent

stable levels. By this we mean the following: if initially $\Delta\phi_3 < \Delta\phi < \Delta\phi_4$, then $G < 1$, or if initially $\Delta\phi_2 < \Delta\phi < \Delta\phi_3$, then $G > 1$, so that in either case the level will monotonically approach $\Delta\phi_3$ during subsequent transfers. If the initial signal level is exactly equal to $\Delta\phi_4$, then any noise in the system will shift the signal level away from level $\Delta\phi_4$ toward either level $\Delta\phi_3$ or $\Delta\phi_5$. Thus the levels $\Delta\phi_2$ and $\Delta\phi_4$ are unstable points of unity transfer ratio.

The curve of Fig. 3-3(b) can be translated into the curve of Fig. 3-3(c), known as a $\Delta\phi$ -transfer curve, where the 45° line is the locus of the stable and unstable unity-gain points. In the case of binary transmission, the transfer curve has the form shown in Fig. 3-4(a). We define the lower stable signal level as the binary *zero* level, labeled $\Delta\phi_L$, and the upper level as the binary *one* level, labeled $\Delta\phi_U$. The intermediate, unstable unity-gain point is labeled $\Delta\phi_I$. This type of transfer curve applies to what is generally referred to as a *unipolar* representation (based on a high magnitude of signal for a *one* and a low magnitude of signal for a *zero*). An alternate data representation is shown in Fig. 3-4(b) where the two states have signal levels of equal magnitude but of opposite polarity. This is referred to as a *bipolar* data representation (which is employed in the circuits discussed in Chap. 9).

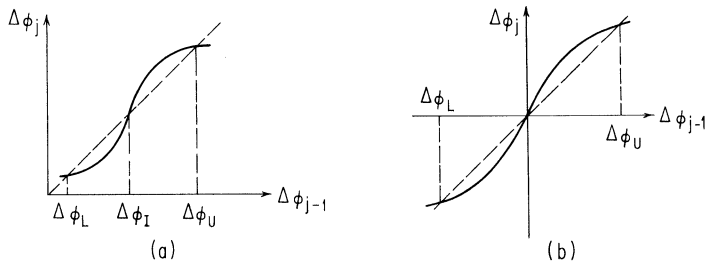


Fig. 3-4. Flux-gain requirements for stable binary transmission: (a) unipolar mode; and (b) bipolar mode.

Drive-Current Tolerances. For achieving wide operating tolerances, the objective of design is to maintain the transfer curve within proper bounds over as wide a range of drive currents as possible. Here we wish only to point out the general nature of the effect of current variations on the transfer curve.

Consider a register of the two-phase type shown in Fig. 3-2, with drive currents having magnitudes $I_{O \rightarrow E}$ and $I_{E \rightarrow O}$. Assume that one of the currents, say $I_{E \rightarrow O}$, is held at a nominal operating value, and let us consider the effect of variations in the magnitude of the

other current $I_{O \rightarrow E}$. As $I_{O \rightarrow E}$ increases, the gain ratio G normally increases for all values of $\Delta\phi_{j-1}$ because of lower percentage losses in coupling loops, as explained in Sec. 2-4 for a coupled pair of cores. Therefore, the entire transfer curve shifts upward as drive current increases. But there is a maximum permitted value of $I_{O \rightarrow E}$ which corresponds to the lower portion of the transfer curve becoming tangent to the 45° line, as indicated in Fig. 3-5. Any further increase in current results in $G > 1$ for all values of $\Delta\phi < \Delta\phi_U$ and the loss of a stable lower level. Similarly, there is a minimum permitted value of $I_{O \rightarrow E}$, below which there is no stable upper level. If we plot the permitted range in $I_{O \rightarrow E}$ for each value of $I_{E \rightarrow O}$, we obtain a two-dimensional region, or *range map*, of allowable drive values (as illustrated later).

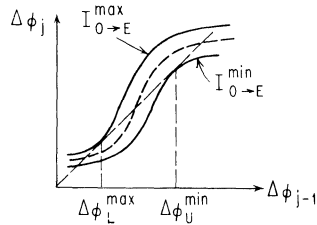


Fig. 3-5. Limits on drive pulse amplitude for bistable transfer.

3-3 Gain and Loss Mechanisms

A *gain* or *loss* mechanism tends to raise or lower the transfer curve relative to the 45° line, as shown in Fig. 3-5. Since the overall effect of all the gain and loss mechanisms operating together must be nonlinear, at least one of the individual mechanisms must be nonlinear. Gain is often obtained primarily by use of coupling-loop turns ratio $n > 1$, and this is a linear effect. Therefore, a nonlinear loss mechanism must be used if no other significant gain mechanism is present. We consider two such nonlinear loss mechanisms in this section.

Given a zero-impedance coupling loop, and turns ratio $n > 1$, then the relation between $\Delta\phi_j$ and $\Delta\phi_{j-1}$ is represented by the dashed line of Fig. 3-6(a). Note that receiver saturation causes the curve to flatten at a value of $\Delta\phi_j = 2\phi_r$. Clipping away a certain portion of the transmitted flux $\Delta\phi_{j-1}$ shifts the curve to the right (solid curve of Fig. 3-6(a)), and we then have the desired bistable form. We wish to illustrate two basic types of flux clipping, one exemplified by the use of an explicit clipping toroid in the loop (*inelastic clipping*) and the other exemplified by coupling loop inductance (*elastic clipping*).

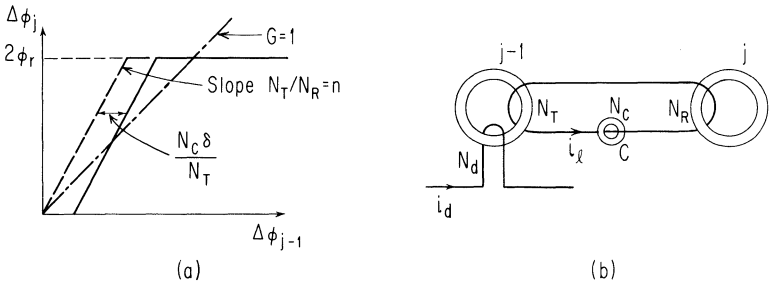


Fig. 3-6. Synthesizing a binary transfer characteristic with turns ratio $n > 1$ as the gain mechanism and a flux clipper as a nonlinear loss element.

For the inelastic method, an additional, small core C of flux capacity δ is included in the loop (Fig. 3-6(b)). Assume that the number of turns N_C of the small core is such that the flux-linkage capacity $N_C \delta$ is relatively small (perhaps 10 to 20 percent of the transmitted linkage), and that the threshold of Core C is low compared to that of the receiver. Then, when the transmitter switches, this clipper core switches first with a relatively small loop current. When it saturates, the loop current increases to the point where the receiver begins switching. For this circuit we can write

$$N_T \Delta\phi_{j-1} = N_C \delta + N_R \Delta\phi_j \quad (3-2)$$

or

$$\Delta\phi_j = \frac{N_T}{N_R} \left(\Delta\phi_{j-1} - \frac{N_C \delta}{N_T} \right) \quad (3-3)$$

Assuming that the received flux will later be transmitted as $\Delta\phi_j$, then Eq. (3-3) is indeed represented by the solid curve of Fig. 3-6(a). Note that for a transmitted flux less than $N_C \delta / N_T$, no flux at all is available to the receiver.

Elastic clipping can be achieved with loop inductance L_ℓ . As the loop current i_ℓ builds up, flux linkage equal to $L_\ell i_\ell$ is stored in the inductance. When the transmitter stops switching, current still flowing in the loop inductance causes the receiver to continue switching until i_ℓ falls to F_0 / N_R , after which the remaining flux linkage $L_\ell F_0 / N_R$ stored in the inductance is dissipated in the loop resistance. This dissipated flux is a relatively large part of the low-level loss subtracting from transferred flux.

This is a good point to summarize and preview some of the known types of gain and loss mechanisms for core-wire circuits,

exclusive of those unique to magnetic thin-film circuits, which will be described in Chap. 9. There are four main types of gain mechanisms known; two of these are the use of turns ratio and the use of "soft-threshold" properties (described in connection with the scheme of Sec. 4-5); the third is some type of flux pumping, introduced in Sec. 2-7; the fourth is flux doubling, a circuit scheme described in Sec. 5-5. There are three main types of loss mechanism, all of which subtract an amount of $\Delta\phi$ from the transmitted $\Delta\phi$ signal en route to the receiver. The first type is $\Delta\phi$ dissipation in loop resistance. Second is elastic clipping, which may be either undriven (necessarily so in parasitic loop inductance) or explicitly driven, as may be obtained either with use of a core of linear material or by driving a square-loop core into saturation. Third is inelastic clipping, which may also be driven or undriven at the time of clipping, although the clipping element must subsequently be cleared to its original state each cycle. The effect of receiver threshold (Sec. 2-4), though not a loss mechanism itself, causes the loss in loop inductance to be nonlinear. The loss in loop resistance is also nonlinear due to the actual nonlinear character of receiver resistance $N_R^2\bar{\rho}$, as shown in Chap. 12.

3-4 Forward Decoupling in a Magnetic Chain

The simplest possibility to consider for attempting to construct a shift register is merely to string together a chain of identical cores, neighboring cores being interconnected by a set of identical coupling loops, as in Fig. 3-7. In such a simple chain, however, receiver loading by adjacent cores (in the sense of Sec. 2-6) is so great that $G > 1$ cannot actually be achieved. To achieve $G > 1$, it is necessary to decouple each receiver element from the remainder of the chain. Such decoupling is readily achieved with a diode element inserted in each loop in the manner of Fig. 3-8. Assume that Core $j + 1$ is in negative remanence (clockwise flux) and that Core j has been

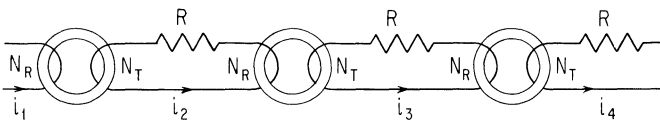


Fig. 3-7. In a simple iterative core chain with no decoupling, receiver loading results in $G < 1$.

preset to a certain flux level. When Core j is explicitly cleared to negative remanence by the current pulse i_C , a coupling-loop current i_{j+1} flows and switches a certain amount of flux in Core $j + 1$. The diode in the output circuit of Core $j + 1$ prevents receiver-loading current from flowing, and $G > 1$ can therefore be obtained.

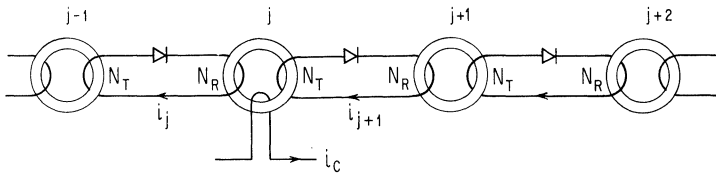


Fig. 3-8. Forward decoupling by means of a series diode in each loop.

In the transfer from Core j to Core $j + 1$, the diode in the output circuit of Core $j + 1$ not only provides the necessary loop decoupling to achieve gain but also provides a forward isolation function by assuring that the switching of Core $j + 1$ will not affect Core $j + 2$. However, we must now consider a potentially serious lack of back isolation, since the switching of Core j also results in a back-loop current i_j that might affect the switching of Core $j - 1$.

3-5 Backward Isolation; Core-Diode Transfer Schemes

Instead of assuming a drive only for the j th Core, as in Fig. 3-8, let us now consider the case of interest, namely, a simultaneous drive, first for all the O -cores, and then for all the E -cores, as in Fig. 3-9. Each drive pulse unconditionally drives its associated set of driven cores to their *zero* condition, i.e., clockwise flux. As described in Sec. 3-1, a basic shifting cycle thus consists of an $O \rightarrow E$ pulse followed by an $E \rightarrow O$ pulse. With repetitive application of clock pulses in this sequence, data is continually shifted to the right along the string of cores (and possibly back to the first core on the left via an end-around loop).

Let us now examine the potentially serious problem of backward isolation. Suppose that initially Core O_{j-1} holds a *zero* and Core O_j a *one*. During the $O \rightarrow E$ pulse, a large magnitude of flux switches in O_j , resulting in a relatively large back current i_j that tends to switch Core E_{j-1} . The latter core should nominally not be switched, except possibly for a low *zero* level of $\Delta\phi$ received from Core O_{j-1} .

Any flux switched in Core E_{j-1} due to current i_j represents *back transfer* of $\Delta\phi$. This $\Delta\phi$ would subsequently be transmitted forward during the next $E \rightarrow O$ pulse, and we see then the possibility of spurious buildup of a *zero* to a *one* as a result of this back-transfer problem. In the present case, since $N_R < N_T$, the amount of $\Delta\phi$ transmitted backwards is less than that transmitted forward, and with sufficiently careful design this circuit can actually be made to operate reasonably well. We will now consider three techniques for greatly improving backward isolation, with corresponding improvement in performance. In effect, what we wish to do is increase the directional asymmetry in the line. In contrast, if we were to set $N_T = N_R$ in Fig. 3-9, there would be no asymmetry at all, and there would be the same tendency for transfer of flux to the left as to the right.

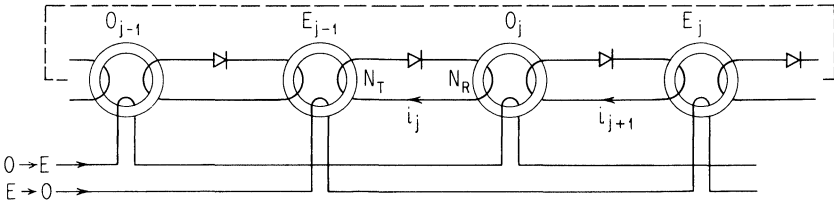


Fig. 3-9. Demonstrating the need for backward decoupling.

The first scheme for reducing back transfer is indicated in Fig. 3-10(a), where a shunt diode is introduced into each coupling loop. The polarity of the diode is such that it does not interfere with forward transfer, though it short-circuits any back transfer. The resistor R is necessary so that the shunt diode does not present a short circuit to the switching core itself. Another scheme for reducing back transfer is shown in Fig. 3-10(b). Here, back-to-back diodes in each loop prevent the flow of loop current except when one of the diodes is deliberately forward biased (by a current

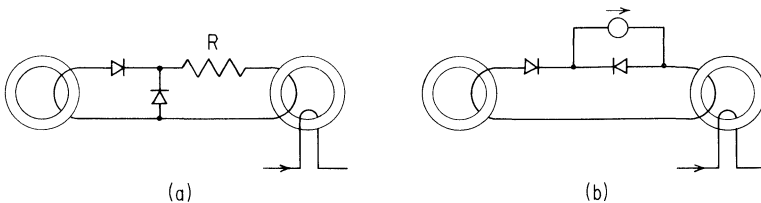


Fig. 3-10. Backward decoupling by means of: (a) a shunt diode in each loop; and (b) an additional reversed diode which is forward biased only during forward transfer.

source), so that a particular loop can be used for forward transfer. More practical circuits of this type can be arranged so that only a single extra pair of diodes is required, rather than one extra diode per loop. (Both of these techniques lead to high performance, and circuits of this type have found wide application.)

The above two methods for increasing the directional asymmetry of the line involve the addition of extra elements per loop. An equally important technique involves the use of additional loops. Returning to Fig. 3-9, we see that the back current i_j would cause no harm if Core E_{j-1} were not used as a receiver during the $O_j \rightarrow E_j$ transfer. This situation can be provided by rearranging the drive lines to the form shown in Fig. 3-11(a). Now when Core B_j is the transmitter and Core C_j the receiver, Core A_j is prevented from switching by mmf applied to the winding labeled *Hold*. The drive line shown is intended to provide simultaneous transfer from all B cores to the neighboring C cores. The coupling loops between the C and A cores are not shown completed, in order to emphasize that the diodes prevent any forward current in these loops during Clock Pulse B . If the A cores are held from switching, as shown, then there can be no back transfer either, and we therefore have achieved nominally perfect isolation during the $B \rightarrow C$ transfer. Although not shown in the figure, if two other clock lines labeled A and C are similarly provided and properly displaced along the chain, then excellent performance can be achieved by applying clock pulses in the sequence A, B, C, A, B, C, \dots

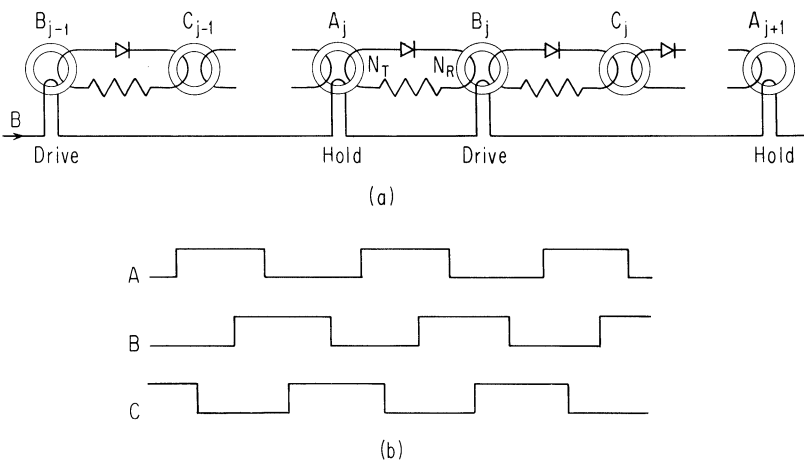


Fig. 3-11. A 3-core-per-bit register requiring a three-clock driver.

The explicit Hold windings shown in Fig. 3-11(a) can actually be eliminated if the clock pulses are made to overlap in time in the manner shown in Fig. 3-11(b). Thus, if the B pulse is applied before the A pulse terminates, then current through the A windings, which previously drove each of the A cores to its reference, or clear, state now plays the role of holding the A cores in this cleared condition.

Note in Fig. 3-11 that if N_T could be set equal to N_R , then the physical chain would be perfectly symmetrical and the direction of shifting could be reversed merely by altering the clock sequence to A, C, B, A, C, B, \dots (in the manner of reversing a three-phase motor). Although this is not possible here, because $N_T > N_R$ is required for achieving flux gain, we will next consider a transfer scheme in which bidirectional transfer can, in fact, be achieved in just this manner, due to gain being achieved by a different mechanism that allows N_T/N_R to be set equal to unity.

3-6 Transfer Schemes Using Capacitance

In this section, we consider two types of registers using capacitors, in conjunction with cores, to illustrate several basic points. The first scheme has not, to our knowledge, been put to significant use, though the second one has been applied practically and is described in detail in Chap. 14 of Meyerhoff (1960).

Core-Capacitor Scheme. This scheme, described by Dumaire, Jeudon, and Lilamand (1958), makes use of the $\Delta\phi$ -transformation effect described in Sec. 1-4. If Core A in Fig. 3-12(a) is initially in the *one* state, then Pulse A switches the core and charges the capacitor. The charging current i_c cannot switch Core B because it tends to drive Core B further into saturation. Just as Core A begins to saturate, the capacitor discharges in the direction to switch Core B . The capacitor voltage as a function of time is sketched in Fig. 3-12(b). It was shown in Sec. 1-4 that the equivalent flux linkage (measured in terms of the volt-second area under the capacitor voltage curve) can actually be greater during discharge than during charge, which may result in $G > 1$ even with unity turns ratio.

Figure 3-12(c) shows a register chain based on this transfer scheme. With unity turns ratio, we have bilateral symmetry in the structure, and there could be no directional preference with only two clock phases and two cores per bit. Therefore we use three

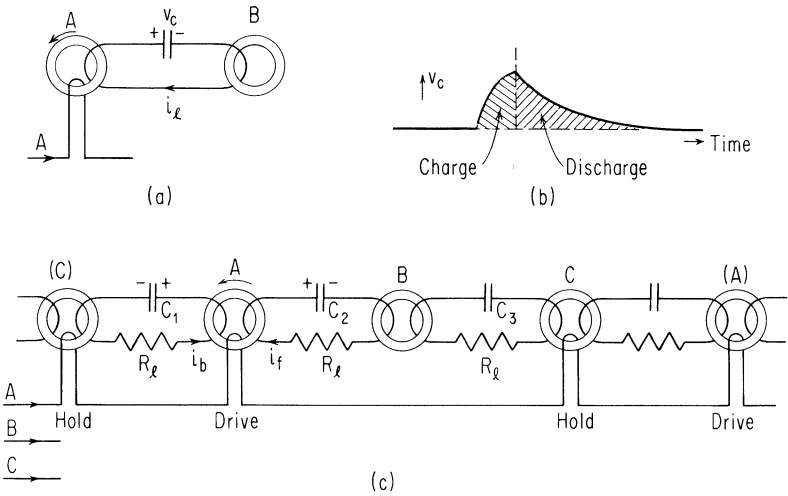


Fig. 3-12. A 3-core-per-bit symmetrical register with one capacitor per loop and a unity turns ratio.

cores per bit and employ the timing asymmetry and the same drive-hold configuration as in Fig. 3-11. In Fig. 3-12(c), as Core A switches, a back current i_b and a forward current i_f charge the respective capacitors C_1 and C_2 . As Core A begins to saturate, these capacitors start to discharge, both currents then being in a direction to drive Core A further into saturation. Capacitor C_1 discharges rapidly, the reversed current i_b being limited primarily by the coupling-loop impedance and the saturation inductance of the cores. (In order to avoid oscillations and to limit the holding mmf required, the loop resistance R_l must be larger than a certain minimum value.) Discharge current from C_2 switches Core B, as desired. But Capacitor C_3 is a load on Core B; as a result, C_2 initially discharges rapidly and C_3 charges rapidly until their voltages are equal. Then both capacitors discharge simultaneously to continue the switching of Core B. In this manner, upon application of the drive pulse A, all cores labeled A simultaneously transfer their data states to their B neighbors.

To achieve continuous shifting, we require three clocks, as in the three-phase register of Fig. 3-11. As there, we are able to achieve the holding function without special Hold windings, by overlapping the A, B, and C pulses (provided that R_l is large enough to prevent the maximum backloop mmf from overriding the drive mmf retained on the previous core for holding it clear). By thus omitting the Hold windings, and with turns ratio $n = 1$, shifting to

the left is achieved merely by reversing the order of the clock pulses, as suggested at the end of Sec. 3-5.

Core-Diode-Capacitor Scheme. Although a register for simultaneous shifting of all data must have at least two storage cells per bit, it is not necessary that each of the storage elements be capable of holding data indefinitely. It is sufficient if one set of elements provides only temporary, or dynamic, storage during the relatively brief interval in which the long-term storage elements are being cleared in order to be ready to receive the data back again, in the shifted position. A common type of register of this form is shown in Fig. 3-13, where the dynamic storage is provided by the capacitors. Such a register requires only a single-phase clock. The circuits are arranged so that during the drive pulse, data is transferred to the right from cores to capacitors, and in the interval between drive pulses the capacitors "transmit to," i.e., discharge into, the neighboring cores to the right.

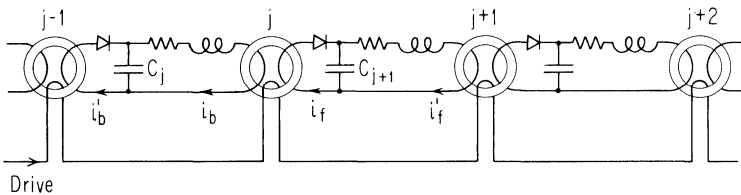


Fig. 3-13. A single-core-per-bit register requiring only a single-phase pulsing.

To follow the operation, assume that Core j is in the *one* state when the drive pulse is applied. Core j therefore switches, and forward and back loop currents i_f and i_b flow. The forward current i_f charges Capacitor C_{j+1} , but is not able to set Core $(j + 1)$ because the drive pulse is still applied to this core. When the drive pulse terminates (timing is arranged so that the drive terminates when the switching cores reach saturation), the series diode becomes cut off and the capacitor discharges through Core $(j + 1)$, setting it strongly. The backloop current i_b , resulting from Core j switching, tends to charge capacitor C_j , but because of the relatively high impedance in this charging circuit, and because of the lower number of receiver turns, C_j tends to charge to a considerably smaller voltage than C_{j+1} . Nevertheless, a current i'_b , small compared to i'_f , tends to flow through Core $(j - 1)$. The shunting thus provided by the capacitor is generally not as good as that provided by the shunt diode in the circuit of Fig. 3-10(a).

Hence, the isolation between transfers is not perfect (even ideally), but it is sufficient for obtaining good performance. Single-phase core-diode-capacitor circuits such as these have been used quite widely.

3-7 Summary

This chapter covers the basic requirements for stable binary transfer in a chain of magnetic elements. First we show that for bistability it is necessary to have the flux transfer ratio $G > 1$ for large values of $\Delta\phi$ and $G < 1$ for small values of $\Delta\phi$, where we assume that a binary *zero* state is represented by a small, ideally zero, level of $\Delta\phi$, and a *one* state by a relatively large magnitude of $\Delta\phi$. Various gain and loss mechanisms for shaping the gain curve as a function of the $\Delta\phi$ level are discussed. From the limits on coupling loop and load resistance found in Secs. 2-3 and 2-6, we see that in order to achieve $G > 1$ in an iterative chain of identical stages, it is necessary to unload each stage that is switching as a receiver element; we refer to this as forward decoupling. Backward decoupling is also required where a number of independent stages are switched together along the magnetic chain. Diodes are effective in providing these forward and backward decoupling functions, and various core-diode schemes are discussed. It is also shown how capacitors can be employed to provide the necessary flux-gain mechanism, in terms of the $\Delta\phi$ -transformation property of Sec. 1-4, and also to provide temporary storage in coupling loops. Although the capacitor schemes are of secondary interest, they provide good practice in the tracing and manipulation of flux signals and aid in the understanding of basic requirements on flux gain and loss mechanisms.

INTRODUCTION TO CORE-WIRE TRANSFER SCHEMES

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In this chapter, we first show how the combination of a toroidal core and a resistance, along with use of an extra clock phase, can replace each diode of a core-diode circuit. This replacement leads to a class of circuits generally known as *resistance-type* core-wire circuits. Every core-diode circuit has such a core-wire equivalent, although as we will see, the converse is not true. In these circuits, dissipation of flux linkage in the coupling-loop resistance during some portion of the clock cycle is a basic part of the operation.

Second, we show how the requirement for loop resistance can in turn be eliminated by the use of still other cores, leading to circuits generally known as *nonresistance-type* core-wire circuits. In these circuits, resistive flux dissipation is not required (in fact, is undesired) in any part of the cycle, though any dissipation that

does occur must be accounted for in detailed quantitative analysis. The resistance circuits are generally much slower than the non-resistance circuits but are much more tolerant to variations in circuit components and drive-pulse amplitude.

The resistance and nonresistance types of circuits can each be realized either with toroidal cores or with multileg cores. Each of the possibilities is illustrated by example in this chapter. These examples are specifically chosen to illustrate basic principles and important differences in various types of core-wire circuits. Although none of these examples represents schemes presently in practical use, all have been successfully operated in the laboratory.

The development of the various types of circuits in this chapter is somewhat tedious, but the indulgence of the reader is sought, for in this way one can better understand the very many possibilities inherent in these circuits. The general principles on flux gain and current tolerances that were introduced in Chap. 3 apply here, but the emphasis will be on qualitative details for obtaining decoupling and other basic requirements with the different circuit types. Given the essential qualitative characteristics, detailed design for bistable transfer can be accomplished by the methods discussed later.

4-1 Simulation of Diode Action

Assume that the core of Fig. 4-1 is in negative remanence $-\phi_r$. A positive current $+i$ would drive the core further into negative saturation, with small induced emf, whereas a negative current $-i$ would switch the core towards $+\phi_r$, with relatively large emf induced in the winding. In analogy to diode notation, the direction of current in which the core is driven into saturation is called the *forward* (low-impedance) direction; the other direction is referred to as the reverse direction. If a current in a separate winding (shown dashed in the figure) tends to hold the core in its $-\phi_r$ condition, then the core will exhibit low impedance to either direction of current flow as long as the mmf in the reverse direction is less than the holding mmf. The same effect is achieved with a diode by applying a current bias, in which case a

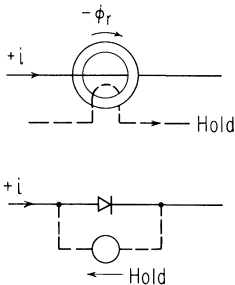


Fig. 4-1. Simulating diode action with a core; $+i$ symbolizes the forward (low impedance) direction for both the diode and its core replacement.

The same effect is achieved with a diode by applying a current bias, in which case a

“backward current” equal to the holding current can flow before the diode circuit opens.

We note, however, the following differences between a diode and its potential replacement:

1. For a constant applied current, the switching voltage is not constant in time (the constant- $\bar{\rho}$ core model noted earlier is only a rough approximation), i.e., the effective impedance of a switching core is not constant.

2. A back impedance can be sustained only so long as the core is actually switching. Once the core becomes saturated, the impedance is again essentially zero.

3. When the core reaches the opposite state of saturation, the “magnetic diode” has effectively been reversed, so that an opposite polarity current will now cause the high-impedance state.

4. The ability to use a number of electrically isolated windings on the same core, some of which may carry control currents (such as holding currents), is an important property that has no diode counterpart.

An example of diode replacement by a core is shown in Fig. 4-2. In Fig. 4-2(a), the diode prevents loop current from flowing when the left-hand core (assumed to be a receiver core) is switched by the drive mmf $N_R i_f$. The flux linkage injected by the left core is dissipated in the back resistance of the diode. (This can be achieved with very small loop current because of the high value of back resistance.) In Fig. 4-2(b), we replace the diode with a core, making use of the polarity convention of Fig. 4-1. Now the flux linkage injected by the left-hand core is balanced by flux switching in the “diode core.” If the latter has a low threshold, and does not saturate before switching in the left-hand core is completed, then the loop current i_ℓ is again very small, and no flux switches in the right-hand core.

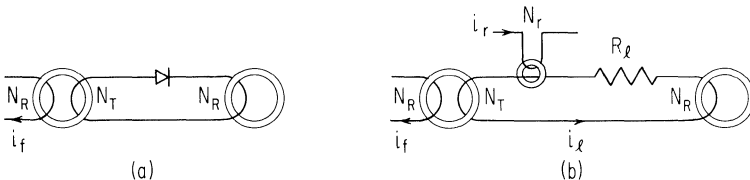


Fig. 4-2. Replacing the diode of (a) with a core and loop resistance in (b) along with the addition of a clock phase.

We see then that both the diode and its replacement core can accept flux linkages with very small current flow. An important

difference, however, is that the core must be explicitly restored to its original, or clear, state before it can play the same diode function again. This is the role of the extra clock phase. In order not to disturb either the left- or right-hand cores during the restore operation, the restoring mmf $N_r i_r$ must switch the core slowly, and, since neither of the other two cores are to switch, there must be a resistance in the loop to dissipate the injected flux linkage. Thus, we see how a core and a loop resistance, along with use of an extra clock phase, can replace the diode. In this fashion, each of the core-diode circuits of Chap. 3 could be transformed to a core-wire circuit. In the following section we consider a specific example of such a circuit.

Briggs Scheme. A direct core-wire equivalent of the circuit of Fig. 3-10(b) is shown in Fig. 4-3. For simplicity, only the $O \rightarrow E$ advance line is shown, although a similar $E \rightarrow O$ line is also necessary. During $O_j \rightarrow E_{j+1}$ transfer, the small shaded cores B and F are switched by very small loop currents and provide the required backward and forward isolation functions, respectively. (In Fig. 3-10(b), these functions are provided by the corresponding diodes.) This circuit is easily arranged with a single drive line that provides both the advance and hold functions, as indicated by the dashed line in the figure, so that only a single power source is actually needed for this phase of operation.

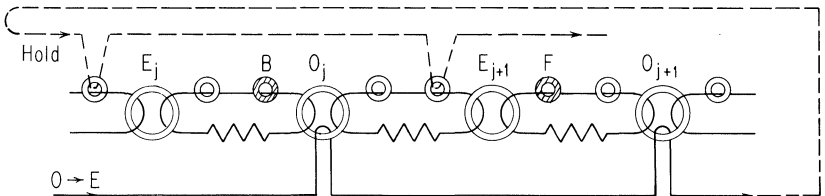


Fig. 4-3. Core-wire equivalent of the core-diode circuit of Fig. 3-10(b).

Although no windings are shown in Fig. 4-3 for the restoring function, a single line linking all of the diode cores could be used. A current pulse on this line following each advance pulse would restore all of the small cores that were switching during the advance phase and leave unaffected the cores already in their clear states. Alternatively, the restore line could be energized with direct current, which would automatically restore these cores following each advance pulse (see Sec. 2-8). In this case, the resulting circuit operation still has a four-phase rhythm ($O \rightarrow E$,

Restore, $E \rightarrow O$, Restore), even though only two explicit clock pulses are applied. The primary effect of applying the restore current continuously is that the diode cores then have somewhat poorer back resistance, in the sense that loop currents must achieve higher values before overcoming the dc mmf. The circuit of Fig. 4-3 is essentially identical to the one described by Briggs (1952).

4-2 Core-Wire Scheme with No Core-Diode Equivalent

We noted earlier that although every core-diode circuit has a core-wire equivalent, the converse is not true. To illustrate, we will now show the development of a core-wire circuit that requires only a single "diode core" per loop, but which has no operable core-diode equivalent. To start, consider the arrangement of Fig. 4-4(a) in which a diode shunts to ground between each pair of cores. Assume that Core E_j contains a *one*. During the $E \rightarrow O$ transfer, Core E_j switches to $-\phi_r$ and a forward current i_f tends to flow through Diode D_1 . Since the main objective is to switch Core O_j , we wish Current i_f to link that core, but go no

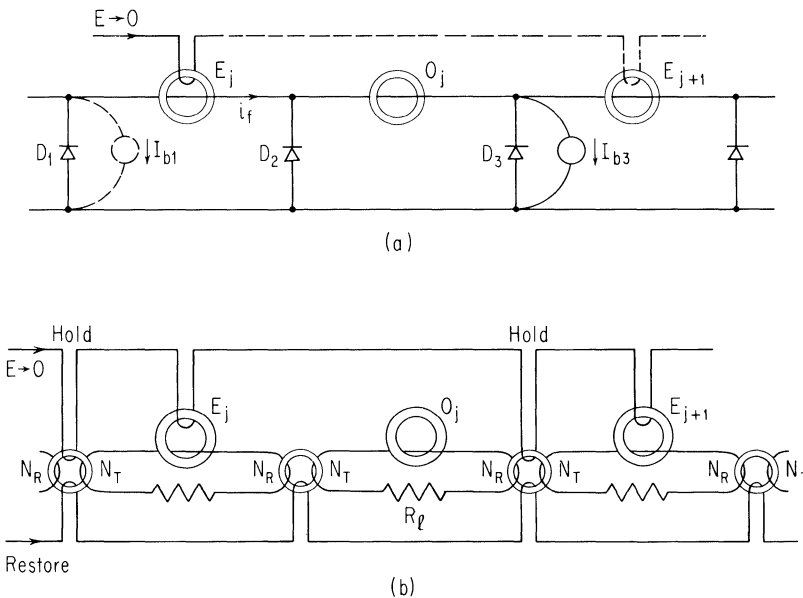


Fig. 4-4. A core-wire register with no core-diode equivalent is shown in (b). The core-diode version in (a) is inoperable because of lack of a gain mechanism.

further. This is accomplished by forward-biasing the diode D_3 , with Current I_{b3} , as shown in the figure. The diodes D_1 and D_3 in effect then establish a coupling loop between Cores E_j and O_j .

All other E cores are simultaneously driven by the same $E \rightarrow O$ pulse, and every other diode to the right of an O core is therefore similarly forward biased, as shown by the dashed parts of Fig. 4-4(a). During the alternate $O \rightarrow E$ drive periods, the other set of diodes is similarly forward biased. To this extent, the core-diode circuit appears proper. However, there is no place to obtain a turns ratio > 1 for flux gain, and no other $\Delta\phi$ gain mechanism is present, so that in fact the circuit of Fig. 4-4(a), as it stands, is inoperable as a shift register.

Russell Type-II Resistance Scheme. Simply replacing the diodes of Fig. 4-4(a) with cores (and, of course, coupling-loop resistance) offers no advantages regarding flux gain. However, by the use of a separate pair of windings of turns N_T and N_R , on each shunt core (Item 4 of Sec. 4-1), we quite easily obtain the required $\Delta\phi$ gain (Fig. 4-4(b)). Each advance-pulse line in Fig. 4-4(b) links alternate shunt cores in order to hold them clear, analogous to forward biasing on the corresponding diodes in Fig. 4-4(a). The Restore line can again be dc operated. This type of register, using one shunt core per loop, was introduced by Russell (1957) and is referred to as the Russell Type-II scheme.

Thus we see that although all core-diode circuits can be transformed to core-wire circuits, the reverse is not true; in subsequent chapters, we will treat other examples of core-wire circuits with no core-diode equivalents.

4-3 Replacement of Loop Resistance by a Core

We would like to show now how the coupling-loop resistance as a functional element may, in turn, be replaced by another core. In doing so we obtain an example of a nonresistance core-wire scheme.

Russell Nonresistance Scheme. The Russell-II scheme of the previous section has a corresponding nonresistance version (Russell, 1959) that is identical in structure and clock sequence except that the loop resistance is replaced with another core, as shown in Fig. 4-5(a). For simplicity, only the $E \rightarrow O$ drive winding is shown in the figure. For shifting a bit in from the left, during an



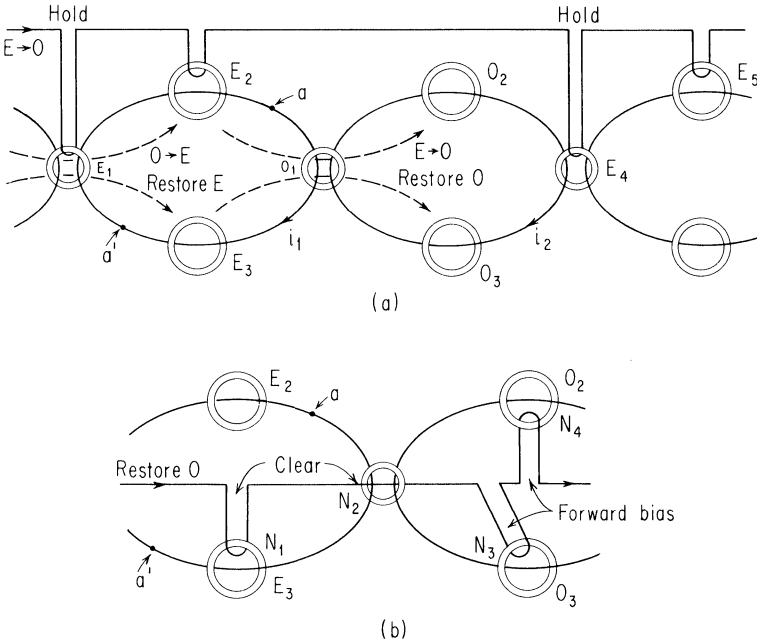


Fig. 4-5. Replacing the functional loop resistance of Fig. 4-4 with another core to obtain a nonresistance-type of core-wire circuit.

$O \rightarrow E$ transfer, the coupling core E_1 and the receiver core E_2 are both switched as before. During this transfer, the coupling-loop current i_1 is positive. The next operation is to restore the coupling core E_1 . But now the $\Delta\phi$ from Core E_1 is not dissipated in coupling-loop resistance, but rather is transferred to Core E_3 . (Let Restore- E be the operation of returning E_1 to its clear state.)

During the following $E \rightarrow O$ pulse, which clears Core E_2 , a positive loop current i_1 switches the coupling core O_1 , as a result of which the receiver O_2 is also switched (the right-hand coupling core E_4 being held clear during this operation). Assume for the moment that Core E_3 does not switch during this transfer operation.

Consider now the Restore- O phase during which the coupling Core O_1 is restored. In the resistance version, flux linkages from Core O_1 are balanced by resistive flux dissipation in both the forward and back loops. Here, however, there is no need for dissipation in the back loop, for if we clear Core E_3 simultaneously, the flux linkage earlier stored in Core E_3 can balance the flux linkage from Core O_1 . In other words, if Cores O_1 and E_3 were cleared at the same rate, then zero voltage would appear between points $a - a'$, and there would simply be no back transfer, regardless of

the rate of clearing. Now in the forward loop, a negative current i_2 tends to clear Core O_2 at the same time that it tends to set Core O_3 . To minimize switching of Core O_2 , this core can be biased (up to threshold) in a direction to hinder switching, as shown in Fig. 4-5(b), while at the same time Core O_3 is biased forward to minimize the required switching current. We might ask why Core O_3 couldn't simply be small, compared with Core O_2 , so that we would not have to forward-bias Core O_2 in this manner. To answer this, we observe that during the subsequent $O \rightarrow E$ transfer phase, Core O_3 must be prevented from switching (as was earlier noted for Core E_3 during the $E \rightarrow O$ phase). Hence, the effective backward threshold of Core O_3 must be larger than the effective forward threshold of Core E_4 (when loaded by E_5 , which is equal in size to O_2). We conclude that the two cores on each loop are preferably of comparable size.

Let us now see how it is that we can achieve higher-speed operation in this nonresistance version. Consider again the resistance version of Fig. 4-4(b). For low flux loss during transfer, the loop resistance should be as low as possible. On the other hand, for a high rate of flux dissipation during Restore, the resistance should be as high as possible. The loop resistance, of course, has the same value during each operation. By substituting a core for resistance, however, as in Fig. 4-5, we can achieve a significant difference in average core impedance during the two operations, by the selective biasing discussed above. In other words, during a restore phase, a forward-biased core has a relatively high effective impedance as seen by loop current (and hence switches rapidly), whereas during the subsequent transfer phase, the same core (still biased forward) presents a relatively low impedance to the opposite polarity of loop current, making possible a low loss of the transmitted $\Delta\phi$. Thus, at the expense of additional core components and drive complexity, we can in general achieve a considerably higher transfer speed in a nonresistance-type circuit than in its resistance-type counterpart.

4-4 Extra Isolation with Multileg Cores

Multileg Core. We now introduce a more complex core shape. One of the earliest such devices was the transfluxor (Rajchman and Lo, 1955), in which a single, small (or *minor*) aperture was added

to a simple core (Fig. 4-6(a)). Let us note some basic properties of this device.

1. A current i of large amplitude results in a clockwise flux throughout the entire core of Fig. 4-6(a), in particular in the legs on both sides of the small aperture, just as in an ordinary toroid. We refer to this clockwise flux state as the *clear* state.

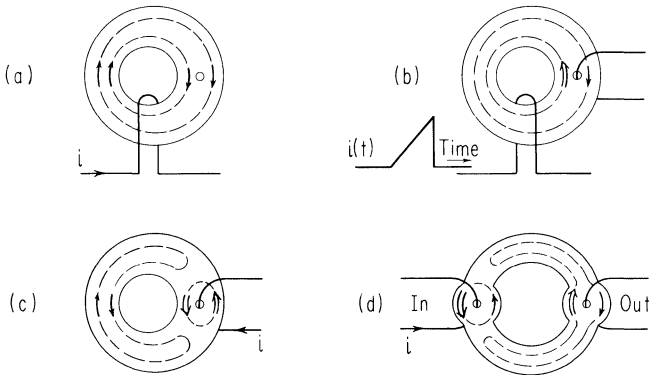


Fig. 4-6. Multileg core: (a) clear state; (b) set state; (c) driving the output aperture with a small mmf; (d) separate input aperture for digital setting.

2. Now consider a slowly increasing mmf of the opposite polarity (Fig. 4-6(b)). At some threshold value of current, flux begins switching counterclockwise along the inner wall of the toroid; as mmf increases further, flux switches to larger and larger values of radius. At some particular magnitude of current, exactly half of the flux is switched, as shown in Fig. 4-6(b). (The switched flux is indicated by the double arrow.) This state, in which the flux is in opposite directions (relative to the major aperture) in the legs adjacent to a minor aperture, is referred to as the *set* state.

3. With the core in the set state, it takes a relatively small mmf to switch flux locally about the minor aperture (Fig. 4-6(c)). The resulting flux pattern is shown by the dashed lines. The low value of mmf results from the short switching path about this aperture. In fact, in this state, flux can be switched back and forth continuously with a small current of alternating polarity applied to the minor aperture.

4. The set state can be achieved “digitally,” i.e., without requiring a precise magnitude of input current, by the use of a separate input aperture, as in Fig. 4-6(d). In this case, starting with a

cleared core, a sufficiently large input current i causes a complete switching of flux in the leg linked by the input winding. If the current i in Fig. 4-6(d) rises relatively slowly, then flux switching occurs along the shortest physical path around the major aperture, so that nominally no flux change links the output winding in this setting operation. (In this figure, shaded areas are shown around the minor apertures to suggest the desirability in general of having constant cross-sectional area everywhere around the major aperture. The subject of core shaping is discussed further in Sec. 6-9.)

With these simple notions regarding a multileg core, we can proceed to show new possibilities in core-wire circuits and to show why core-wire circuits involving multileg cores are generally superior in performance to those synthesized strictly with toroids.

Cores with more than one aperture have been called by various names: multiaperture cores, MADs, multileg cores, multipath cores. In the following chapter each leg of a core will be represented by a branch in a general magnetic network representation, and for this reason we prefer the term *multileg*. However, the acronym MAD, from MultiAperture Device, has been applied to certain schemes for a sufficiently long time that this term has been retained in the names of those schemes.

Briggs-Lo Scheme. In Fig. 4-7(a), each multileg core incorporates into one element both the storage and coupling-core functions of the Russell-II circuit of Fig. 4-4(b), and, as we will see, contributes an important new function as well. This scheme was initially discussed by Briggs and Lo (1961).

Assume that each of the E cores in Fig. 4-7(a) has been cleared, i.e., is in its *zero* state, and that binary data is stored in the O cores. The advance $O \rightarrow E$ pulse switches all of the O cores to their clear states, and transfers, in the process, the state of each O core to its right-hand E neighbor. Assume that Core O_1 is in the set state in the sense of Fig. 4-6(b). The $O \rightarrow E$ pulse clears Core O_1 , inducing a loop current i that in turn sets E_1 , accomplishing thereby the desired transfer. (If O_1 were in its clear state, no loop current would flow, and E_1 would remain in its clear state.)

In more detail, note that when O_1 is cleared, flux switches only through its inner leg; flux in the outer leg is already in the clockwise or clear direction. Therefore there is no back transfer. In the forward loop, the current i sets E_1 by switching flux in its outer leg and around the main aperture. But no flux can switch in the inner leg, which is already saturated in the direction of the

input mmf; thus unlike the case of the original Russell-II scheme, no holding current is necessary for prevention of forward transfer.

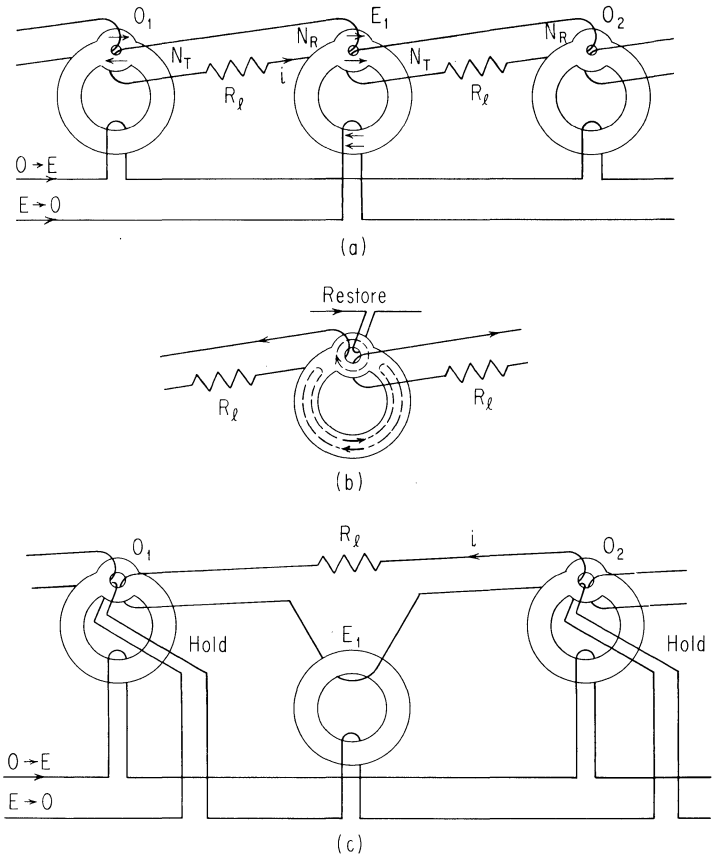


Fig. 4-7. In (a) and (b), Briggs-Lo multileg-resistance scheme similar to the Russell-II scheme of Fig. 4-4(b), but not requiring holding; (c) Engelbart reduction.

Of the three legs in each multileg core, the major one can be thought of as replacing the storage core in Fig. 4-4(b), and the outer small leg as replacing the coupling core. The inner small leg is somehow extra, and its presence happens to be the reason that the holding function of the Russell-II scheme is no longer necessary here. In terms of the network approach of the next chapter we will see more clearly the role of such "extra" circuit elements.

To continue with the cycle of operation, consider Fig. 4-7(b), where a restore current (applied to all cores) switches flux slowly

about the minor aperture of E_1 , injecting flux linkages into both the forward and back loops, which is dissipated in the loop resistances. The cycle is completed with an $E \rightarrow O$ transfer followed by another restore pulse. We thus have a four-phase cycle, though the restore line can again be energized by a single dc source, so that actually only two explicit clock pulses are required.

Engelbart Reduction. With one more step we can obtain a scheme with even one less clock phase, and only one coupling loop per bit. But we must reintroduce a holding current. This scheme is indicated in Fig. 4-7(c), where the multileg element E_1 has been replaced by a simple toroid of the same general size, and both coupling loops are merged into one. This scheme was devised by D. C. Engelbart of Stanford Research Institute (unpublished notes). (In connection with Fig. 7-7(c), we will show that this is a minimal scheme in terms of the number of elements per bit.)

To see how it is that we save a clock phase, and why holding is necessary, assume again that a *one* is initially stored in Core O_1 . During the subsequent $O \rightarrow E$ phase, a large positive loop current sets Core E_1 . Although this current is in a direction to set Core O_2 , the setting mmf is necessarily less than the simultaneous drive on Core O_2 , and so holding is not necessary during this phase.

We might have considered the restoring function in Fig. 4-7(b) to be a flux transfer, in effect, from the outer to the inner leg of Core E_1 with subsequent transfer from the inner leg. There is no equivalent function in Fig. 4-7(c), and the $E \rightarrow O$ pulse can therefore be applied immediately following the $O \rightarrow E$ pulse. A high positive loop current flows during this $E \rightarrow O$ phase, setting O_2 . This current also tends to set the inner leg of O_1 . But since this leg is now in its cleared state, it can be unconditionally held that way, as indicated in the figure. The resulting system then has only one toroid and one multileg core per bit, and a three-phase cycle $\dots, E \rightarrow O, \text{Restore}, O \rightarrow E, \dots$, but holding is again required to prevent back transfer.

4-5 Isolation of Input and Output in Separate Apertures

Having introduced multileg resistance schemes above, we wish now to treat one last circuit arrangement, namely a multileg non-resistance scheme. In the circuits of Fig. 4-7, the input and output windings connect to the same minor aperture. Functional decoupling

is achieved by a restore phase, which we noted can be considered as a local flux transfer from the input leg to the output leg (around the minor aperture), during which time we have balancing flux dissipation in the loop resistances. Let us consider more explicit isolation based on separate apertures for the input and output windings.

MAD-N Scheme. The particular circuit to be discussed here, which is shown in abridged form in Fig. 4-8, is referred to as the MAD-N scheme, N for Nonresistance type (Crane, 1959). It uses two multileg cores per bit and is based on a four-phase clock cycle. Assume that each E core is initially in its clear state and that Core O_1 stores a *one*, i.e., is in its set state. We will follow the transfer of this binary *one* through one complete clock cycle to Core O_2 . The flux states at each step are shown below the circuit, and flux changes at any particular step are shown by double arrows.

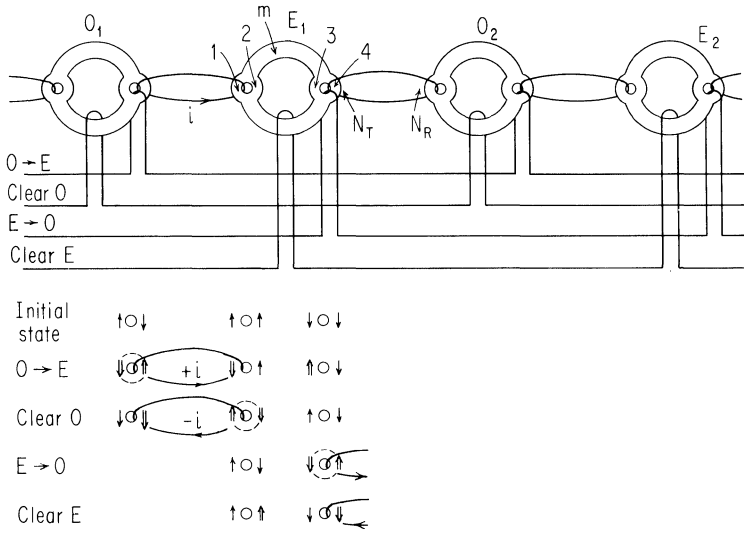


Fig. 4-8. Using separate apertures for input and output, resulting in the MAD-N scheme.

A pulse on the $O \rightarrow E$ line causes flux to switch locally around the output aperture of Core O_1 . The resultant loop current $+i$ sets receiver Core E_1 , the flux nominally switching in the shortest path that includes Legs 1, m , and 3. The output circuit is therefore effectively decoupled from the primary flux-switching path when the core acts as a receiver. Since flux switches only locally about the output aperture of the transmitter, transmission is said to be

nondestructive. Though this basic nondestructive read-out feature is very useful, it implies here that the O element must be explicitly cleared, i.e., driven to its *zero* state, before it can subsequently be used as a receiver.

Clearing of the transmitter is achieved with a pulse on the Clear O winding. The result is that flux is again reversed through the output winding, and a negative loop current $-i$ reverses flux locally around the input aperture of the receiver, Core E_1 . The significance of this operation is that the input leg of E_1 is now back to its initial (cleared) direction, so that when the E core is subsequently cleared there will be no flux linkage generated in the input winding and hence no back transfer. The full clock cycle for this register has the familiar four beat rhythm: $O \rightarrow E$, Clear O , $E \rightarrow O$, Clear E ,

For *zero* transfer, the advance pulse should cause no flux switching in the transmitter, and the receiver nominally remains in its cleared state. To ensure no flux switching, the advance mmf applied to Leg 4 of the transmitter must be limited to the threshold for switching around the major aperture. But for *one* transfer, this magnitude of drive mmf is not adequate to induce enough loop current for switching flux around the major aperture of the receiver. In other words, the circuit shown in Fig. 4-8 is not actually workable in the abridged form shown.

Exchange of Flux Gain and Excess MMF. To increase the maximum amount of drive mmf allowed, we can bias the transmitter and receiver as shown in Fig. 4-9. Let F_0 represent the threshold for major-aperture switching. In addition to applying this much mmf to Leg 4 of the transmitter, a similar amount can be applied to the receiver to bias it to threshold, as well as a similar amount in the clear direction of Leg 3 of the transmitter. The latter mmf is limited to a single threshold unit to prevent flux from being lost by

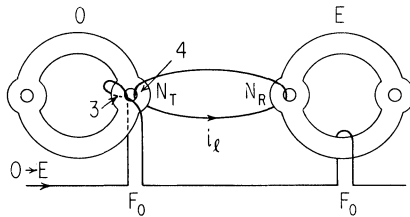


Fig. 4-9. Increasing the drive mmf and biasing the receiver.

unsettling around the transmitter major aperture in the case of *one* transmission. (Actually, because of the soft-threshold effects discussed in the next section, Leg-3 bias must generally be kept somewhat below this amount.)

With this bias arrangement, we have a drive mmf $2F_0$ available to switch flux around the transmitter output aperture, and since the receiver is biased to threshold, any loop mmf $N_R i_\ell$ is completely effective in causing switching of the receiver. An upper limit on loop current is therefore $2F_0/N_T$ (assuming zero mmf drop in the transmitter), and hence an upper limit on excess mmf that can be supplied to the receiver is $(N_R/N_T)2F_0$. But with turns ratio as the flux-gain mechanism, the maximum gain ratio is N_T/N_R . Hence an upper limit on the product of gain ratio and excess mmf ("gain-excess" product) is simply $2F_0$. This result, which is typical for many nonresistance circuits, implies that increasing flux gain by increasing N_T/N_R necessarily results in a reduction in the maximum excess mmf, and hence reduces the maximum transfer speed and potentially the drive-current range. (When actual losses are taken into account, including nonlinear loss for maintaining a stable *zero* level, there is some optimum turns ratio, typically < 2 for nonresistive circuits, at which drive-current range is a maximum.)

Soft-Threshold Gain Mechanism. We have thus far assumed that $\Delta\phi_T(j) = \Delta\phi_R(j)$, i.e., that an element starting in the clear state $-\phi_r$ is set to a certain flux level during one clock pulse (receive time) and is returned to the initial clear state during some subsequent clock pulse (transmit time). But this is not always the case. In particular, for the MAD-N scheme of this section, the advance operation and the clear operation are quite distinct. Furthermore, the main aperture mmf is in the *same* direction during both the receive and transmit phases. This creates the possibility of transmitting a larger amount of flux than was actually received.

To see how this can work, assume in Fig. 4-10(a) that only about half of the flux capacity of the input leg of the O element is switched during the input clock phase $E \rightarrow O$. During the subsequent Clear- E pulse, a negative loop current switches flux locally around the input aperture, Fig. 4-10(b). Now during the following $O \rightarrow E$ phase (Fig. 4-10(c)), an amount of flux equal to the received flux is easily switched around the output aperture. But, additional flux, labeled $\Delta\phi^*$, can simultaneously be switched around the main aperture as well, resulting in a net output flux $\Delta\phi_T(j) = \Delta\phi_R(j) + \Delta\phi^*$.

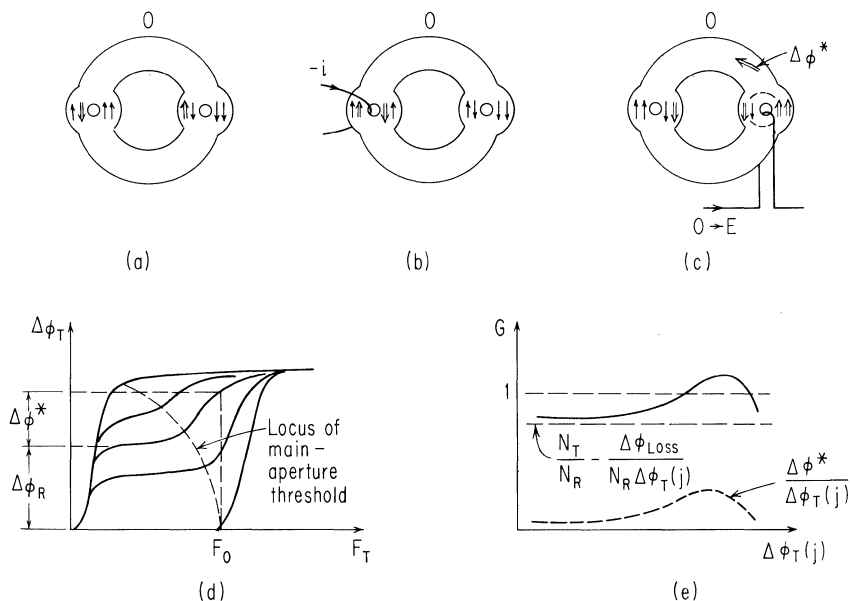


Fig. 4-10. Use of the soft-threshold flux-gain mechanism.

Although we are now discussing *one* transfer, we must keep in mind that for *zero* transfer, $\Delta\phi_T$ (and hence also $\Delta\phi^*$) should nominally be zero. To be a useful gain mechanism, therefore, we must be able to achieve a significant magnitude of $\Delta\phi^*$ during *one* transfer, but only a negligible amount during *zero* transfer. Since the strength of the advance pulse is independent of data state, this could only occur if there were a significant difference in the main aperture threshold for the two states. And this is precisely what may occur.

A typical family of output curves is shown qualitatively in Fig. 4-10(d). Note that the main-aperture threshold, shown by the dashed line, significantly decreases with the level of flux $\Delta\phi_R$ set during the input phase. Thus with an mmf F_0 applied, $\Delta\phi^*$ will be very small for $\Delta\phi_R \approx 0$, whereas a significant level of $\Delta\phi^*$ can be obtained for larger values of $\Delta\phi_R$. The transfer ratio can be written

$$G = \frac{\Delta\phi_T(j+1)}{\Delta\phi_T(j)} = \frac{\Delta\phi_R(j+1) + \Delta\phi^*}{\Delta\phi_T(j)} \quad (4-1)$$

but

$$\Delta\phi_R(j+1) = \frac{N_T \Delta\phi_T(j) - \Delta\phi_{loss}}{N_R} \quad (4-2)$$

where $\Delta\phi_{\text{loss}}$ represents the amount of flux-linkage loss in the coupling-loop resistance and inductance. Thus

$$G = \frac{N_T}{N_R} - \frac{\Delta\phi_{\text{loss}}}{N_R \Delta\phi_T(j)} + \frac{\Delta\phi^*}{\Delta\phi_T(j)} \quad (4-3)$$

With the relationship of $\Delta\phi^*/\Delta\phi_T(j)$ versus $\Delta\phi_T(j)$ suggested by the dashed line in Fig. 4-10(e), and with $[(N_T/N_R) - \Delta\phi_{\text{loss}}/N_R \Delta\phi_T(j)]$ assumed constant, as a first approximation, we see that it is possible to achieve a proper digital gain curve even with $N_T/N_R = 1$. Operation based on soft-threshold gain has in fact been verified in the laboratory with $N_T = N_R = 1$, that is, with single turn windings, though with relatively small circuit tolerances.

A potential advantage of exploiting the soft-threshold gain mechanism is that a unity turns ratio is thus allowed, and the resulting symmetry permits bidirectional shifting. It is easily verified that if the bias winding on the E -core in Fig. 4-9 is replaced by a figure-eight winding, symmetrical with the drive winding on the O -core (and similarly for the $E \rightarrow O$ drive windings), then shifting can be caused to proceed to the left instead of to the right simply by reversing the order of the two clear pulses. In any case, whether this soft-threshold effect is relied on as the primary gain mechanism or not, it contributes to the overall transfer characteristic for many types of schemes.

4-6 Summary

In this chapter we have introduced a number of basically different core-wire schemes in order to illustrate a number of different aspects of these circuits. Although all of the schemes discussed are actually operable, none are of any special practical interest. They are introduced here primarily because they have a certain direct simplicity, and through them one can quickly gain insight into the basic operations. Perhaps it is no accident that these were among the schemes reported earliest in the literature.

In Sec. 4-1 we show how a diode can be replaced by a core-resistance combination together with an extra clock phase to "restore" the core so that it can again perform its diode function. The resistance is required for $\Delta\phi$ dissipation (in the sense of Sec. 1-2) during the restore operation. The resistance thus introduced into the circuit with this replacement technique leads to

what are called resistance-type core-wire circuits. Every core-diode circuit has such a core-wire equivalent, though it is shown in Sec. 4-2 that the converse is not true.

In Sec. 4-3, we show how the resistance function can be replaced in turn by still another core, leading to the synthesis of nonresistance core-wire circuits, which are generally faster than the resistance type circuits, but also have lower operating margins. Finally, it is shown in Secs. 4-4 and 4-5 how important improvements in circuit isolation are obtained by the use of still more complex circuits, in particular by the use of multileg cores.

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In the preceding chapters, digital magnetic core circuits were evolved by matching the functional properties of cores to the requirements for digital transfer in iterative circuits. In the process, the effects of electrical elements in core circuits were considered. We also indicated a number of different ways in which cores, coupled by wire only, could provide all of the properties needed for realization of digital transfer. Later, we consider still

other ways to synthesize such circuits. As an important aid in deriving and understanding such a diversity of schemes and techniques, we introduce in this chapter a generalized magnetic-network representation for magnetic-core circuits.

As used here, a *magnetic network* is an abstract representation of a circuit. In general, such a network consists of magnetic branches and nodes and electrical mutual coupling (conductive coupling loops), just as an electric network consists of electric branches and nodes and magnetic mutual coupling (transformers). In a magnetic network it is particularly easy to trace flux switching paths, just as in an electric network it is easy to trace current flow paths. Magnetic-network concepts are primarily useful here for qualitative analysis and for derivation of new transfer schemes.

The main qualitative aspects that distinguish one form of transfer circuitry from another are: (1) the basic topology; (2) the significant flux states, and the mode of sequencing between these states; and (3) the physical types of elements involved. Item (1) is reflected in the structure of the network. Item (2) relates to the order in which network elements are switched when the circuit is cycled through a series of flux states. Item (3) involves specification of whether the flux change in some network branch is an actual flux change in a magnetic element, or whether it represents an equivalent flux-linkage change in another type of element, e.g., dissipation in a resistance (Sec. 1-2).

The transformation of circuits into network terms helps in the classification of known schemes. It is also useful for the derivation of new schemes, by means of a number of network operations that we will develop. Also, with the network notation we can more readily see how to trade off between wiring complexity, e.g., an array of toroids, and core complexity.

In the first section of the chapter, magnetic-network concepts are introduced in terms of a single multileg core linked by current-carrying windings. Then, we consider the transformation of more general core circuits into the magnetic-network domain. In Sec. 5-3 we describe a number of network operations that facilitate the derivation of variations of a given basic transfer scheme. In Secs. 5-4 and 5-5, we show how the network methods can be applied in the derivation of new schemes as well as aid in understanding the operation of relatively complex schemes. Though these last two sections are excellent exercises in deriving new schemes, and in developing facility with network methods, they may be bypassed without loss of continuity.

5-1 Network Representation

We take the view that a complex core consists of legs connected at junctions, and that each leg may be treated as a distinct magnetic element, with properties similar to those of a toroidal core. Interaction between the legs is represented by constraints on the amount of flux entering a junction and on the total mmf along a closed path in the core. Additional constraints imposed by intercoupling electric circuitry may be represented in similar fashion, thus providing a common representation for both the cores and the wiring. Several persons have contributed to the evolution of this representation to its present form, but the original impetus was provided by D. C. Engelbart (unpublished notes).

Drawing Network Structures. In Fig. 5-1, three multileg cores are shown, each of which consists of several legs and junctions, the latter indicated by dots. Assume that the minimum cross-sectional area of Legs 1, 2, 3, and 4 is the same in each of these cores and the same as that of Leg 7 in Fig. 5-1(c). Also, assume that Legs 5 and 6 each have minimum cross-sectional areas twice that of the other legs. It is helpful to consider the cores to have uniform height (in the third dimension), in which case the above statements apply to leg widths. We assume in Fig. 5-1 that all small legs are of width w .

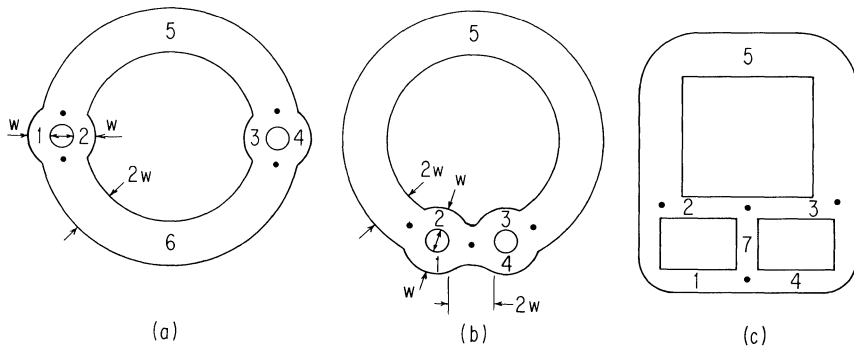


Fig. 5-1. Different forms of multileg cores having two minor apertures.

In Fig. 5-2, we show the basic magnetic-network structures of the respective cores of Fig. 5-1. Here we represent only the legs of the cores and how they are connected at junctions. Hence, it is

sufficient to represent each leg by a line and each junction by a node.

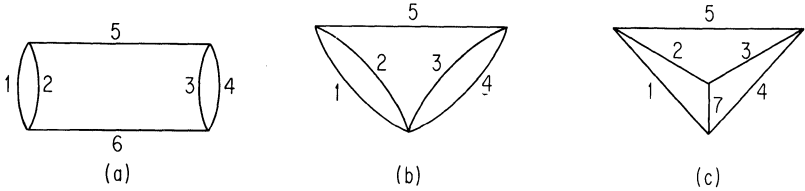


Fig. 5-2. Magnetic network representation of the multileg cores of Fig. 5-1.

The network structures of Fig. 5-2(a) and 5-2(b) may be considered equivalent because the amounts of flux in Legs 5 and 6 are constrained to be the same. In fact, we may view Fig. 5-2(b) as a reduction to *unbalanced* form of the *balanced* network of Fig. 5-2(a), and hence as a reduced network representation of the core of Fig. 5-1(a) as well as a direct representation of the core of Fig. 5-1(b).

Loop and Node Constraints. In electric circuit theory, the basic variables are voltage drop and current, the product of which is power. We consider the analogous variables for magnetic circuits to be mmf drop F , and rate of change of flux $\dot{\phi}$, the product of which is also power.

The constraint on each network node (following from Maxwell's equation $\nabla \cdot \mathbf{B} = 0$) is simply

$$\sum_i \phi_i = 0 \quad (5-1)$$

implying

$$\sum_i \dot{\phi}_i = 0 \quad (5-2)$$

where the summation is over all flux values emanating from the node. For the case of no linking currents, as in Figs. 5-1 and 5-2, the constraint on each network loop, following from Eq. (1-7), is

$$\sum_i F_i = 0 \quad (5-3)$$

where the summation is over all mmf drops around the loop.

Representation of Saturation Flux States. Considering the possibility of partial switching of cores, an unlimited number of flux states are possible; however, we are concerned primarily with digital flux states associated with nominal saturation of one or more legs of a core. With this constraint, let us consider further the network of Fig. 5-2(b), but now with orientation arrows drawn on the branches, as in Fig. 5-3, where we show all the possible flux states, assuming that each of the Legs 1, 2, 3, and 4 must be saturated one way or another. Arrows represent only the direction of flux saturation in this diagram. Though the flux states in Fig. 5-3(d), (e), and (f) are exactly the opposite of those in Fig. 5-3(a), (b), and (c), respectively, it is important, relative to schemes described later, to consider all of these possibilities.

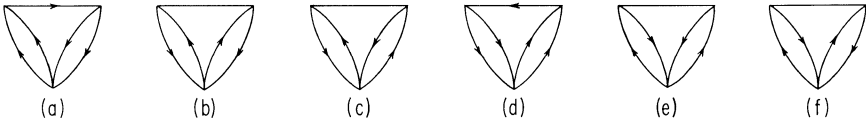


Fig. 5-3. All possible minor-leg saturation flux states for the network of Fig. 5-2(b).

The network diagrams drawn thus far give no indication of areas or length of legs, but it is apparent that cross-sectional areas are crucial relative to consideration of the saturation flux states. Also, relative mmf thresholds of legs must be taken into account when we consider whether it is possible to actually sequence through a given series of flux states. Therefore, we often want some means for suggesting the relative cross-sectional areas and lengths of legs. Where this is necessary, each branch can be drawn as a rectangle rather than a simple line, as in Fig. 5-4, where the length and width of the rectangle are suggestive of the length and cross-sectional area of the leg, respectively. Lines drawn between the rectangles and nodes represent the connections of the legs at the junctions. These lines may be thought of as ideal magnetic-flux conductors. In many cases, it is convenient to treat one node of a network as a reference or a "ground" node, as shown in Fig. 5-4.

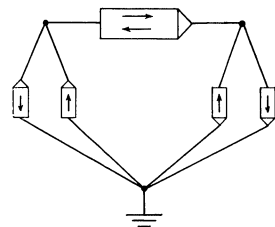


Fig. 5-4. Rectangular branch representation to indicate relative lengths and relative cross-sectional areas.

The use of rectangles also provides a convenient means for showing the present flux state of all of the branches, as is

done in Fig. 5-4 for the core state shown in Fig. 5-3(b). The fact that $\phi = 0$ in the main leg may be indicated either with opposing arrows, as in Fig. 5-4, or with no arrows at all. The clear or reference state of the core may be indicated with triangular pointers on the rectangles, as shown in Fig. 5-4 for the usual clear state of a core of this type, i.e., clockwise saturation around the major aperture.

Representation of Drive MMF. In order to sequence between flux states, it is necessary to provide electric-current excitation. A way to view currents in windings is as current linkages, analogous to rate of change of flux linkages $N\dot{\phi}$ in an electric circuit. When current linkages are present, Eq. (5-3) must be generalized to the form

$$\sum_i F_i = \sum_k N_k i_k \quad (5-4)$$

where $N_k i_k$ is the mmf due to the k th winding linking the network loop, with polarities defined such that positive values of the i_k tend to produce positive values of the F_i . This equation is just another way of writing the integral form of Ampere's law given by Eq. (1-6).

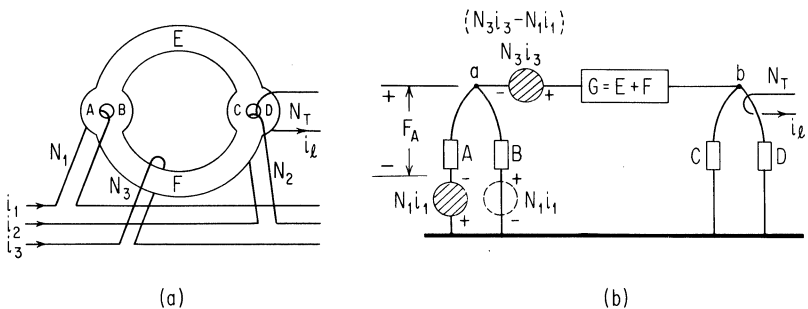


Fig. 5-5. Network representation of drive mmf.

In Fig. 5-5(a) is shown a core linked by independent source currents i_1 , i_2 , and i_3 , in windings of N_1 , N_2 , N_3 turns, respectively, and a dependent, induced loop current i_l in a winding of N_T turns. A way to represent these mmf in the network is shown in Fig. 5-5(b), where the current-linkage sources $N_1 i_1$, $N_2 i_2$, and $N_3 i_3$ are shown as mmf generators in appropriate branches of the network. The variable output current i_l is shown simply as a conventional loop since we are not yet prepared to show the representation of

dependent currents in network terms. (Note that Legs *E* and *F* are both represented by a single branch *G*.)

Though the representation of Fig. 5-5(b) is very useful, we must note that when all current linkages in a loop are transformed into discrete generators in series with certain branches, then the node potentials thus defined are artifices rather than unique physical quantities. This is so because for a given excitation pattern, only the total loop mmf are specified, in the sense of Eq. (5-4), and the assignment of particular mmf to particular branches is not unique. For example, a completely equivalent choice for representing the generators is to move the mmf $N_1 i_1$ to be in series with branch *B* (shown dashed, and with opposite polarity) instead of branch *A*, and to adjust the magnitude of the generator in series with branch *G* to $N_3 i_3 - N_1 i_1$. But the total drive mmf in every closed path is identical in the two schemes, and of course the resultant mmf drop in any leg (such as F_A in Leg *A*) is unique, and independent of the particular equivalent set of mmf generators chosen.

Sequencing between Flux States. To see how the sequencing from one flux state to another may be represented in a network, consider Fig. 5-6, where we assume the vertical branches to be identical and the clear state to be the same as shown in Fig. 5-4. On the basis of Eq. (5-2), any flux change entering a particular node through one branch must be balanced by a flux change in one or more other branches leaving the same node. In many cases, we are concerned only with flux entering a node in a single branch and leaving it in only one other branch. It is apparent that any such flux change must occur in a single closed path in the network.

In Fig. 5-6(a), the initial flux state, as indicated by the arrows within the boxes, is the *clear* state. Assume that a drive mmf $N_1 i_1$

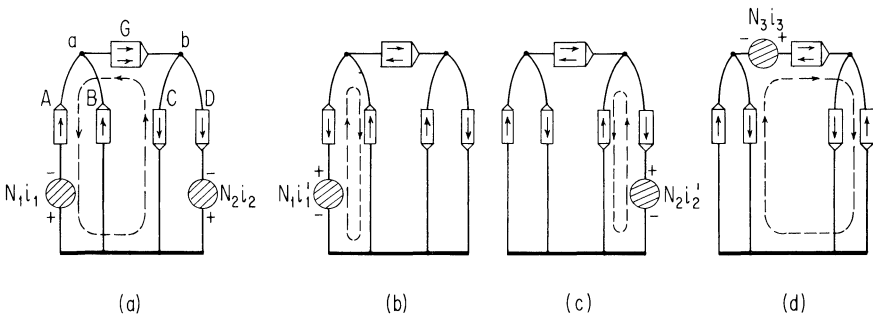


Fig. 5-6. Sequencing between flux states.

is applied, which is sufficient to produce a flux change in the path indicated by the dashed line. With this excitation alone, the flux change would tend to divide equally between the branches *C* and *D*. However, an mmf $N_2 i_2$ is applied simultaneously to Branch *D* in order to hold it in its clear state. In Fig. 5-6(b), an mmf $N_1 i_1'$ is applied to cause a local flux reversal in Branches *A* and *B*. (The arrows inside the boxes in Fig. 5-6(b) represent the flux state resulting from the switching in Fig. 5-6(a).) In Fig. 5-6(c), the mmf $N_2 i_2'$ produces a similar local change in Branches *C* and *D*. It is assumed that the mmf $N_1 i_1'$ and $N_2 i_2'$ are too low in magnitude to produce inelastic flux changes along the path including Branch *G*. In Fig. 5-6(d), mmf $N_3 i_3$ forces the core back to its clear state.

In the cycle of Fig. 5-6, each leg is switched from its clear state to a second state and then back to the clear state. Only two switching steps are required for a cycle of changes in any one branch, but note that we have used four steps in sequencing the whole network through this cycle of flux changes. Note also that this sequence of changes is exactly the one undergone by a core in the MAD-N scheme of Sec. 4-5. (The network representation for this scheme is treated further in Sec. 5-4.)

Representation of Electrical Loads. In Fig. 5-7(a), a core is shown driven by a current i_d through N_d turns and loaded with an electrical loop containing series elements *R*, *L*, and *C* across N_T turns. The network representation is shown in Fig. 5-7(b), with the drive shown as an mmf generator $N_d i_d$ inserted into Leg *B*. Since the loading current i_l through N_T turns constitutes a back mmf $N_T i_l$, it is shown as an mmf potential difference $N_T i_l$ inserted into Leg *C*. This mmf is not a fixed generator but dependent on other conditions in the core and loading circuit. It is terminated by a pair of nodes in anticipation of inserting appropriate equivalent network elements. Small circles are placed around these nodes to distinguish them from the solid-dot nodes representing physical magnetic junctions.

The equation for the electrical loop in Fig. 5-7(a) is

$$N_T \dot{\phi} = L \frac{di_l}{dt} + Ri_l + \frac{1}{C} \int i_l dt \quad (5-5)$$

which may be rewritten as

$$\dot{\phi} = C_m \frac{d(N_T i_l)}{dt} + \frac{(N_T i_l)}{R_m} + \frac{1}{L_m} \int N_T i_l dt \quad (5-6)$$

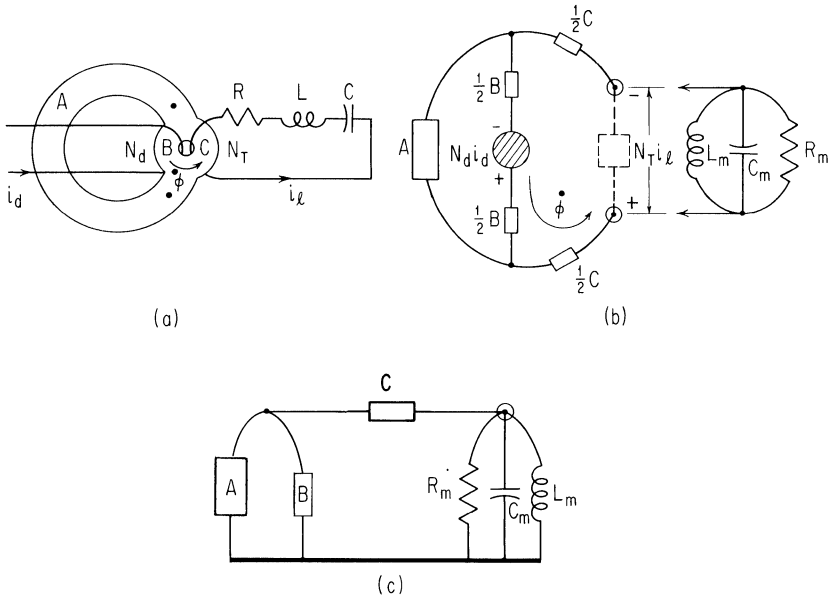


Fig. 5-7. Network representation of electrical loads.

where

$$C_m = \frac{L}{N_T^2}$$

$$\frac{1}{R_m} = G_m = \frac{R}{N_T^2} \tag{5-7}$$

$$L_m = N_T^2 C$$

The quantity $N_T i_\ell$ is the mmf drop between the pair of circled nodes. The three terms on the right of Eq. (5-6) may be interpreted as equivalent amounts of ‘‘magnetic current’’ adding up to the actual ϕ in Leg C. Three branches for carrying these ‘‘magnetic currents’’ are shown on the right side of Fig. 5-7(b). Note that the magnetic representation for the loading circuit is completely dualistic to the physical electric circuit. That is, the series combination of the linear parameters L , R , and C transforms to the equivalent parallel circuit consisting of C , G , and L , each multiplied by the appropriate scale factor as given by Eq. (5-7). The emf $N_T \phi$ transforms to ‘‘magnetic current’’ ϕ (with scale factor $1/N_T$), electric current i_ℓ transforms to the mmf drop $N_T i_\ell$

(with scale factor N_T). A voltage v inserted into the loop would transform into a magnetic current generator of value v/N_T applied across the node pair in Fig. 5-7(b).

The circled nodes associated with transformed electric circuitry will generally be termed *synthetic* nodes in order to be distinguished from physical nodes representing core junctions. The general equation for $\dot{\phi}$ continuity at a synthetic node is

$$\sum_i \dot{\phi} = 0 \quad (5-8)$$

where $\sum_i \dot{\phi}$ includes the equivalent magnetic currents corresponding to voltages in the electrical loop. (Equation (5-6) may be put into this form by transferring all terms to one side of the equation.) Integration of the terms in Eq. (5-8) results in

$$\sum_i \phi_i = K \quad (5-9)$$

where K is a general constant.

Equation (5-8) for a synthetic node is identical with Eq. (5-2) for a physical node. Equation (5-9) differs from Eq. (5-1), however, since K is not necessarily equal to zero. The reason is that the values of equivalent ϕ_i deriving from branches that represent electric elements are actually only integrals of voltages, over arbitrary lengths of time, and hence need not satisfy the flux continuity law. This fact makes it very important to distinguish synthetic nodes from physical nodes in networks.

In the network of Fig. 5-7(b), there is one physical node for each core junction and a pair of synthetic nodes in place of the electrical loop. The same $\sum_i \dot{\phi}_i = 0$ equation applies to both members of this pair of synthetic nodes. Figure 5-7(c) shows this network reduced to the equivalent unbalanced form, with boxes inserted in the branches to represent the three physical magnetic legs. The single synthetic node represents the coupling loop.

Transformation of Coupling Loops. Let us next consider the transformation of a coupling loop that links two cores, as in Fig. 5-8(a). Having previously shown how electrical elements transform, we now assume an ideal zero-impedance coupling loop, since it is a straightforward process to reintroduce electric impedance parameters into the loop. In Fig. 5-8(b), the coupling loop mmf acting on each core is represented by magnetic potentials $N_T i_\ell$ and $N_R i_\ell$ between synthetic node pairs cc' and dd' , respectively. For $N_T = N_R$ these potentials are identical and the two node pairs can be merged

directly into a single node pair, as suggested by the dashed lines. The network could then be transformed to an unbalanced form, as in the example of Fig. 5-7(c).

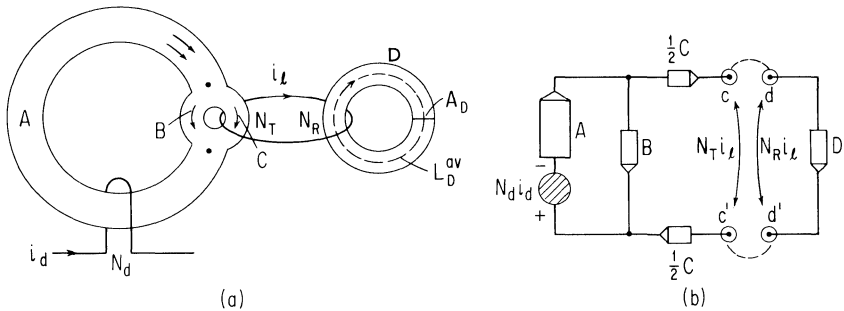


Fig. 5-8. Network representation of coupling loops.

For most purposes where network manipulations are useful, it is sufficient to assume a coupling loop with a unity turns ratio, in which case we can transform the circuit in the straightforward manner shown above. Even if a loop with a nonunity turns ratio is required in the final circuit, it may be substituted for a unity-ratio loop after reverse transformation of the desired network into the circuit domain (Sec. 5-3). Although we thus need not consider the general transformation for $N_T \neq N_R$, we shall show the nature of such a transformation.

Merging of the node pairs in Fig. 5-8(b) can be accomplished for the case $N_T \neq N_R$ by transforming to another set of mmf and ϕ variables in one network or the other while maintaining equivalent internal magnetic behavior. This transformation is performed here on the single-branch network on the right, since this is the simpler one. Referring to Fig. 5-9(a), we define an equivalent

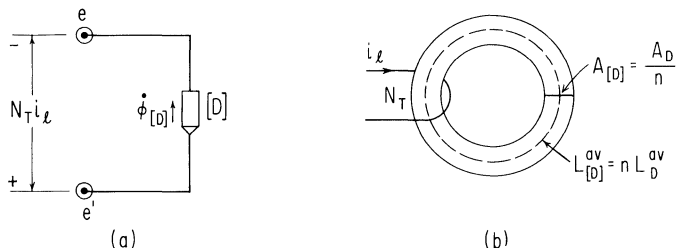


Fig. 5-9. An equivalent receiver element for Fig. 5-8 that allows substitution of a unity-turns-ratio coupling loop.

branch $[D]$, across whose terminals the mmf drop is equal to $N_T i_\ell$, matching with the left-hand network of Fig. 5-8(b). Transformed quantities are designated by square-bracketed subscripts, e.g., $\dot{\phi}_{[D]}$ in Fig. 5-9(a) replacing $\dot{\phi}_D$ in Fig. 5-8(b). The meaning of "equivalent magnetic behavior" is that the average B and H fields in the branch remain unchanged, i.e., that

$$B_{[D]}^{\text{av}} = B_D^{\text{av}} \quad \text{and} \quad H_{[D]}^{\text{av}} = H_D^{\text{av}} \quad (5-10)$$

Given the area A_D and average length l_D^{av} of Core D , we may then write

$$\frac{N_T i_\ell}{N_R i_\ell} = \frac{F_{[D]}}{F_D} = \frac{H_{[D]}^{\text{av}} l_{[D]}^{\text{av}}}{H_D^{\text{av}} l_D^{\text{av}}}$$

whence

$$l_{[D]}^{\text{av}} = \frac{N_T}{N_R} l_D^{\text{av}} = n l_D^{\text{av}} \quad (5-11)$$

and

$$\frac{N_R}{N_T} = \frac{\dot{\phi}_{[D]}}{\dot{\phi}_D} = \frac{\dot{B}_{[D]}^{\text{av}} A_{[D]}}{\dot{B}_D^{\text{av}} A_D}$$

whence

$$A_{[D]} = \frac{N_R}{N_T} A_D = \frac{A_D}{n} \quad (5-12)$$

The toroid equivalent of Branch $[D]$ is shown in Fig. 5-9(b). In effect, we have replaced the coupling loop of turns-ratio N_T/N_R by a loop of unity turns ratio N_T/N_T and scaled the area and the path length in opposite directions by the ratio $n = N_T/N_R$. Since A_D and l_D^{av} scale by reciprocal factors, the volume $A_D l_D^{\text{av}}$ remains unchanged.

With this equivalent toroid, the node pairs cc' in Fig. 5-8(b) and ee' in Fig. 5-9(a) may be directly merged and we arrive at the same simple network form as with the original core and a unity turns ratio. Processing from this point would be the same in either case. As already noted, however, we generally need not concern ourselves with this step of finding equivalent cores, but rather we assume unity turns ratio directly and make any necessary corrections as a final step.

5-2 Ladder and Lattice Networks

We have seen above how to represent both magnetic and electric circuitry in a magnetic network. Let us now apply these principles to iterative core circuits of the type introduced in Chap. 4. Our objective is to relate the nature of the circuit coupling to features of the corresponding network. An understanding of these relations in transforming from circuit to network will aid considerably in reverse transformation from network to circuit.

A stage of the MAD-N circuit of Fig. 4-8 is shown again in Fig. 5-10(a), without drive lines but with coupling-loop resistance and inductance indicated. Following the procedure outlined earlier in this chapter, the balanced network of Fig. 5-10(b) is obtained.

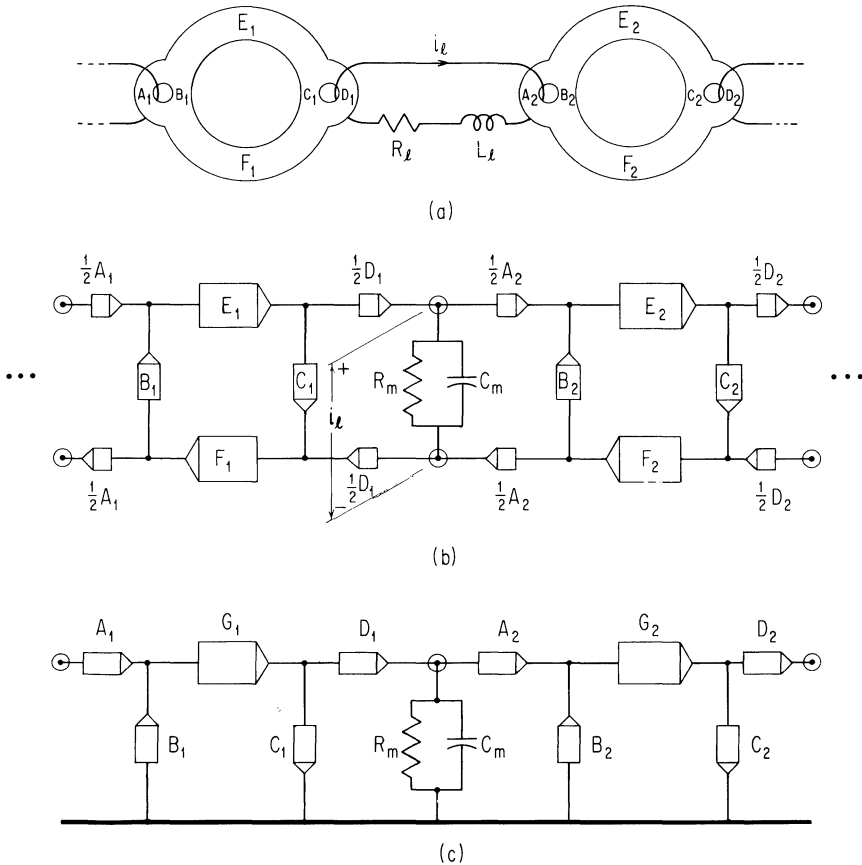


Fig. 5-10. Ladder network representation of the MAD-N scheme.

The network is in the form of a simple ladder, with two synthetic nodes per coupling loop and one physical node per core junction. By combining corresponding pairs of series branches along the two rails of the ladder, we may reduce the network to the unbalanced form of Fig. 5-10(c), in which there is one synthetic node per loop and one physical node per pair of junctions. Any balanced ladder network can be converted to such an unbalanced form in which one rail serves merely as the reference node.

A level of complexity beyond the ladder is the lattice network, shown in skeletal form in Fig. 5-11, which in iterative form is nonplanar. An example of a circuit leading to a lattice network is shown in Fig. 5-12(a). This circuit (which is treated further in Sec. 5-5) transforms to the lattice network of Fig. 5-12(b), which is even more complex than the lattice of Fig. 5-11 since it also contains transverse branches between each node pair. In order to derive this network, we may proceed, as before, by representing each loop with node pairs aa' and bb' in Fig. 5-13(a). Branches C_1 and C_2 , which represent toroids linked by only a single loop, may be immediately drawn as shown. Unlike previous examples, however, this circuit also includes cores that are linked by more than one coupling loop each. Core A_2 , which is driven by the *difference* of the two loop currents, may be represented by the two series halves shown in Fig. 5-13(b). Core B_2 , which is driven by the *sum* of the two loop currents is similarly represented by two series halves but drawn as in Fig. 5-13(c) in order to have mmf potential ($i_a + i_b$) applied to it in a closed path including both members. The final network of Fig. 5-12(b) is obtained by combining the various elements of Fig. 5-13.

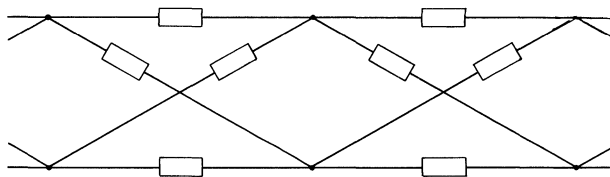


Fig. 5-11. A lattice form of magnetic network.

Quite independently of the iterative nature of the circuit here, additional discussion is needed on the type of coupling. For simplicity, consider the truncated circuit of Fig. 5-14(a), which has the balanced network representation shown in Fig. 5-14(b). If we attempt to reduce this network to unbalanced form by drawing a

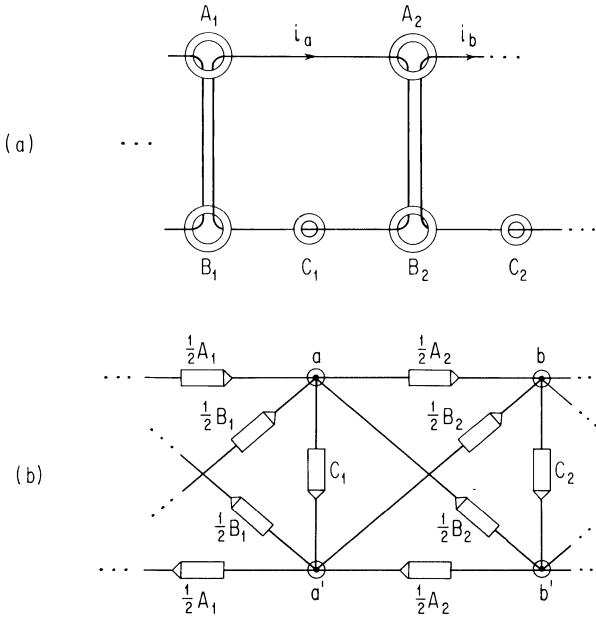


Fig. 5-12. A toroidal core circuit and its lattice network representation.

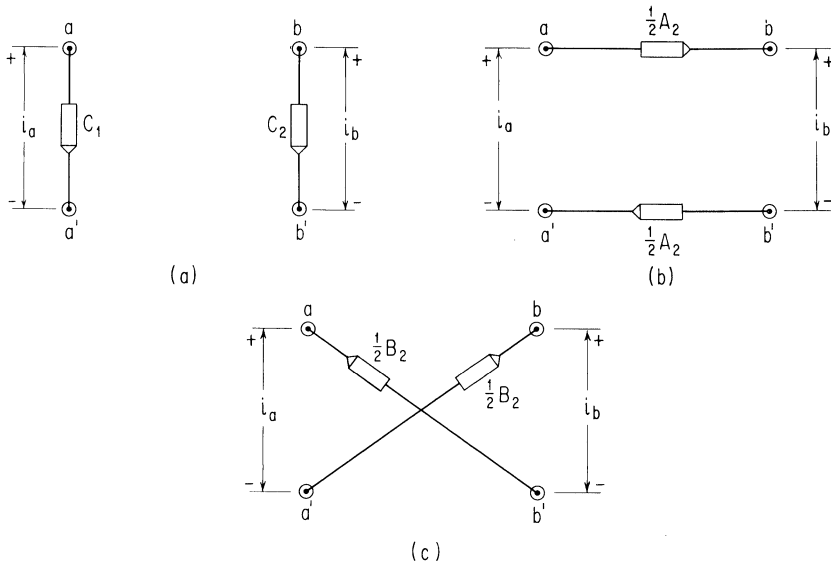


Fig. 5-13. Elements in the transformation of Fig. 5-12.

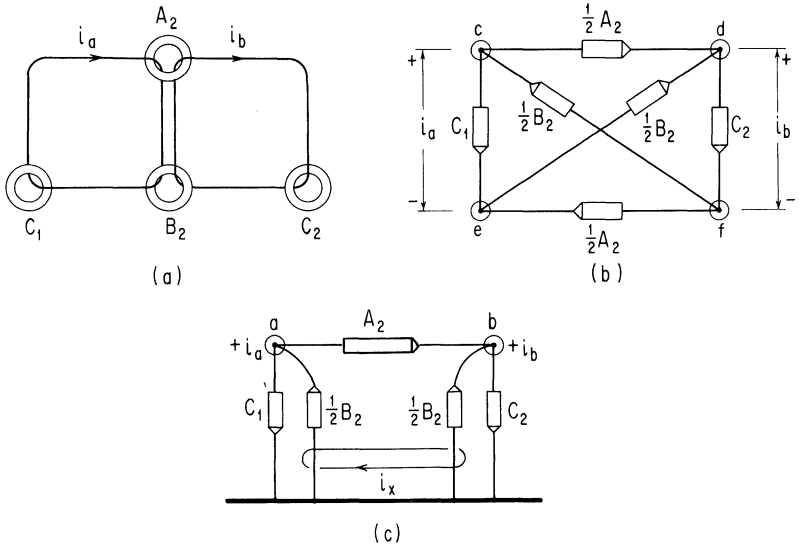


Fig. 5-14. Illustrating a case of irreducibility of a balanced lattice network to an unbalanced network having no electrical loops.

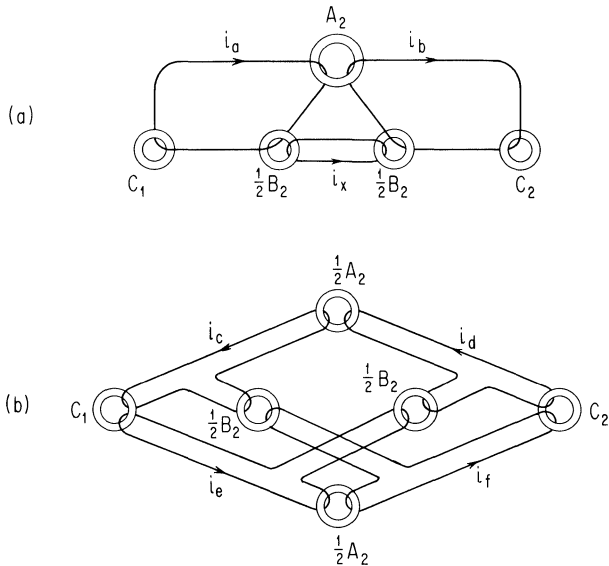


Fig. 5-15. Toroid realizations of the networks of Figs. 5-14(c) and (b), respectively.

ground rail and combining the two parts of A_2 as in Fig. 5-14(c), we find it necessary to attach an ideal coupling loop, in order to assure that identical flux switching prevails at all times in both parts of B_2 . The loop current i_x that flows will be such that $i_a - i_x$ will exactly equal $i_b + i_x$, as otherwise there would be a difference in switching rates of the two halves of B_2 .

In general, when one constructs a network using two (or more) branches to represent a single core leg, these branches must be linked by ideal coupling loops in such a way as to guarantee the same flux switching conditions in each branch representing part of a given leg. This is not necessary in the network of Fig. 5-14(b) only because of the symmetrical lattice form. By *symmetrical*, we mean that the two A branches are identical, including equal division of any drive mmf applied to A , and likewise the two B branches.

We see then that the network representation of a given circuit may validly take more than one form. (The network of Fig. 5-14(c) is a correct representation, even though it is not purely in a magnetic form.) It is also true, as we shall show now, that there is generally more than one circuit realization of a given network.

For example, if in Fig. 5-14(c), we let Nodes a and b each be replaced by a coupling loop and let each branch be replaced by a toroid, we obtain the circuit of Fig. 5-15(a). Provided the two B cores have the same initial state, this circuit must be equivalent in behavior to that of Fig. 5-14(a). Alternately, if we interpret each node in Fig. 5-14(b) as having a potential with respect to some isolated ground node, and then replace each node by a separate coupling loop, we obtain the circuit of Fig. 5-15(b). If we defined any one of the nodes in Fig. 5-14(b) as "ground," then the corresponding loop in Fig. 5-15(b) would vanish, since a zero value of current would be implied. In this way we see that any one of the four loops could be removed without changing the basic nature of the circuit. An intuitive reason for this is that only the values of current differences applied to the cores are significant, and these values are not constrained by arbitrarily fixing the value (in particular, at zero) of any one current.

We can readily deduce a set of conditions on a toroidal-core circuit in order for it to have a purely magnetic network representation on the basis of just a single branch per toroid. Any given branch is connected to exactly two nodes, and it experiences the *difference* of potential between the two nodes. Hence, with each nodal potential representing a coupling-loop current, a single branch cannot possibly represent a toroid unless: (1) that toroid is linked by no more than two coupling-loop currents; and (2) the currents (if there are two) are of oppositely defined polarity. It is

clear, from the way it was derived, that the circuit of Fig. 5-15(b) satisfies these conditions, but that the circuits of Figs. 5-14(a) and 5-15(a) do not.

5-3 Manipulation of Nodes; Reverse Transformations

Given a circuit, we have seen how to convert it to magnetic network form. The reasons for making such a transformation are that it helps us to understand the operation of known circuits, or to develop new circuits that are basically different in the transfer method, or to find variations that permit easier physical realization. We would like to consider now some manipulations that increase the scope of physical realization possibilities. First we will consider the effects of reversing node types—from a physical node to a synthetic node, and vice versa—and then possibilities arising from simply inserting new nodes into a network.

Exchange of Node Types. By reversing node types in a network, we can often obtain a pair of circuits that are magnetically equivalent but have very different physical form. For example, starting with a coupling loop that transforms into a synthetic node in the network, let us consider the effect of exchanging this node for a physical node (a physical core junction). There is actually no problem in substituting a physical node for a synthetic node in this manner, if we assume a zero impedance coupling loop and if the sum of the flux values entering the node (linking the loop) is equal to zero. Whenever this condition is not satisfied, however, as in Fig. 5-16(a), then the synthetic-to-physical exchange can be made only by the artifice of adding a dummy branch across the node-pair representing the loop, as in Fig. 5-16(b), for the purposes of proper flux closure. The flux in this new branch must remain constant at the negative of the sum of flux values in the other branches attached to the same node. To prevent a flux change in this branch, it must

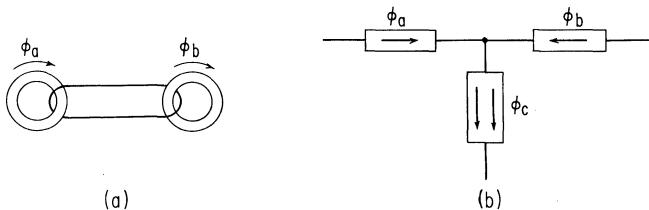


Fig. 5-16. Flux constraints at synthetic and physical nodes.

either be held in a saturated state, e.g., by applying current to a winding on it, or else it must have a large threshold so that it functions like a permanent magnet relative to the rest of the network.

There is also no problem in substituting a synthetic node for a physical node, if again we hypothesize zero-impedance coupling loops and require the initial value of total flux linking each coupling loop to be zero. If, as often occurs, some legs of a multipath element are required only for proper flux closure, as noted above, but do not otherwise switch at any time, then the toroids corresponding to these legs may be eliminated, the only effect being that $\sum_i \phi_i \neq 0$ in coupling loops that would have coupled such toroids.

The above comments on node reversals are based on the assumption of ideal coupling loops. Though generally not affecting the gross logical properties of a network structure, the finite resistance and inductance of coupling loops must be taken into account when the operation of a circuit is analyzed in detail, especially in connection with obtaining a bistable gain characteristic for a transfer circuit (see Chap. 3). In some cases of replacing a physical node by a synthetic node, one must also take care to avoid the phenomenon of "flux creep," where even small $\Delta\phi$ losses in loop resistance may accumulate over many cycles to result in a spurious first-order change of total flux in the set of cores linked by a coupling loop. The flux pumping arrangements of Fig. 2-6 make deliberate use of this creep possibility in a coupling loop with non-zero resistance. This phenomenon cannot occur at a physical node, since $\sum_i \phi_i$ in the attached branches is necessarily equal to zero.

Once we can independently choose the node type for each node in the network, we have a vast array of possibilities for the specific form of the physical realization—from all-toroid circuits, i.e., all synthetic nodes, to a single magnetic element, i.e., all physical nodes, and many possibilities between. Actually, networks with a mixture of physical and synthetic nodes are the ones most commonly dealt with, and for good reasons. Toroidal-core circuits, as in Fig. 5-12(a), require the largest number of individual cores and the largest amount of coupling wiring. A circuit consisting of only a single-core poses great fabrication problems for other than trivially simple circuits. (We consider a specific example of a single-core circuit in Sec. 5-5.) Furthermore, $\Delta\phi$ -gain is readily achieved by means of coupling-loop turns ratio, and we rely on gain by this means for most transfer schemes. (In Sec. 5-4 we illustrate some network manipulations that lead to variations in the physical form of multileg core circuits.)

Insertion of Nodes. Let us consider two specific types of network modification, namely, insertion of synthetic nodes and insertion of physical nodes. In the first case, we break certain branches by insertion of a synthetic node, usually to allow incorporation of turns ratio for flux gain, but sometimes solely for the purpose of breaking a complex structure into parts that can be more readily fabricated. For an example of this type of insertion, consider the ladder network of Fig. 5-17(a), which has no synthetic nodes and therefore would call for realization as a single magnetic component. Suppose that a synthetic node is inserted in the center of each A branch having an even subscript, as in Fig. 5-17(b). The shunt loss branches associated with the loop parameters R_ℓ and L_ℓ are shown. Although the original branch A_2 has been divided into halves, and is realized in Fig. 5-17(c) as two legs in two different cores, the change in structure is not logically significant as long as coupling-loop losses are kept minor. (Should $\Delta\phi$ storage in L_ℓ or $\Delta\phi$ dissipation in R_ℓ become significant, compared to flux changes in the cores, then the alteration is logically as well as

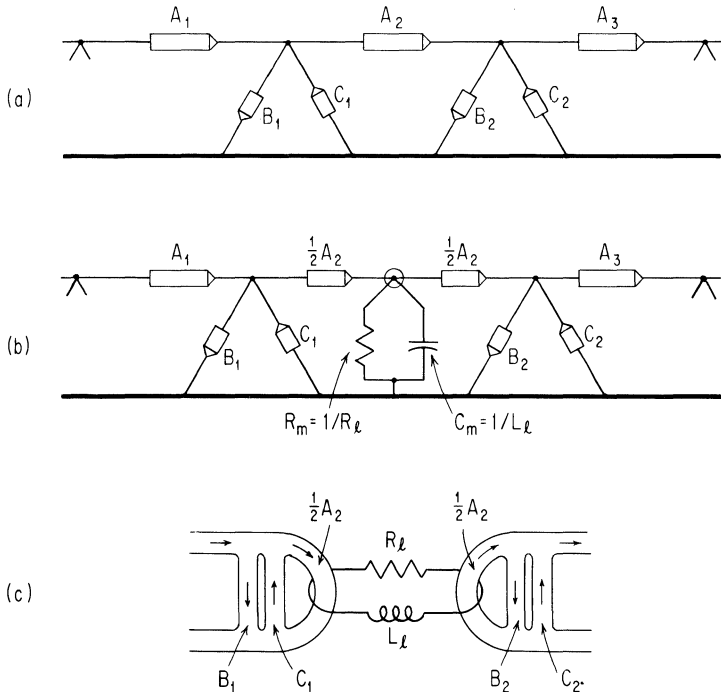


Fig. 5-17. Insertion of synthetic nodes in an otherwise all-physical-node network.

practically significant, since independent switching of the two halves of A_2 is implied.)

We see then that insertion of synthetic nodes can help divide a circuit into more manageable pieces. On the other hand, insertion of physical nodes is generally done in order to incorporate more elements of the network into a single core. For example, consider the iterative network and corresponding circuit of Fig. 5-18(a) and (b). To incorporate the toroid D_1 into one of the multileg cores, it must be associated with either the branch to the left, or with that to the right, of the synthetic node to which it is attached, as shown in Fig. 5-18(c) and (e), respectively. But in either case, an additional branch, E_1 or F_2 , must be inserted, thus generating the new physical node x_1 or y_2 , respectively. Figure 5-18(d) and (f) shows circuit realizations for incorporating the toroid to the left or right, respectively. Which of the two realizations is the more favorable depends upon the scheme in which the circuit is being

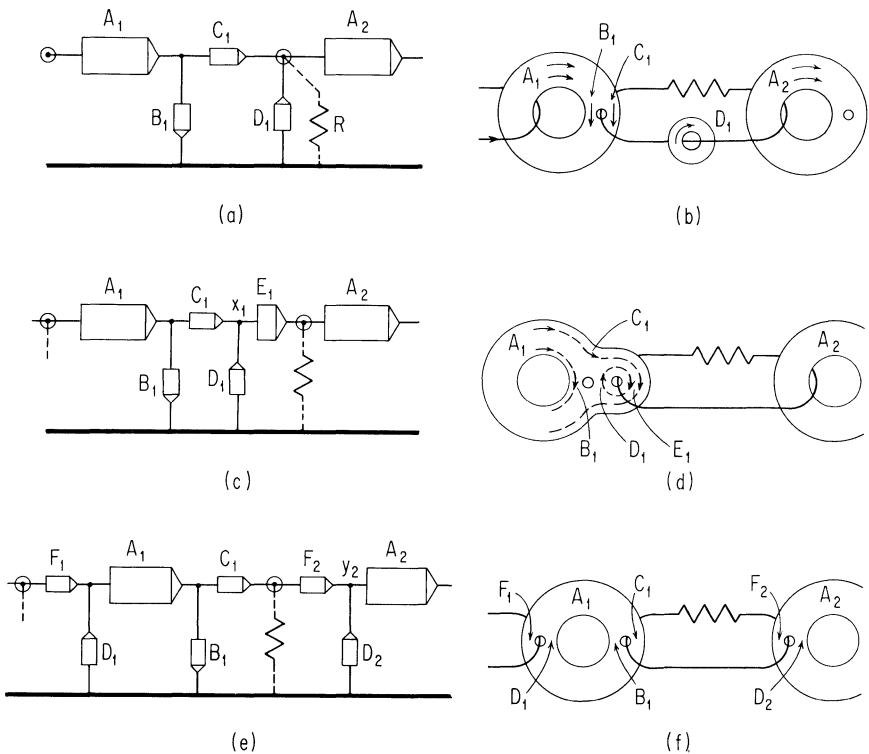


Fig. 5-18. Insertion of physical nodes to incorporate more elements of the network into a single core.

used and on practical design details. If the coupling-loop resistance is very small, then the new branch (E_1 or F_2) must switch in conjunction with A_2 in the first case and with C_1 in the second case. However, if resistance R were used in a first-order way (meaning a resistance type of scheme), then the new branch may switch independently of the mate just indicated for it, and its possible use in the two realizations might be quite different. In any case, because of the additional leg E_1 or F_2 , it can be seen that incorporation of a toroid into a multileg core may do more than just result in fewer separate cores in the circuit, but may actually augment the capabilities of the circuit due to the increased complexity of the structure. Conversion from the circuit of Fig. 4-4(b) to that of Fig. 4-7(a) may be interpreted in this sense.

5-4 Flux-State Sequencing in Magnetic Networks

In Sec. 5-1, it was shown in an abstract way how one could cycle through a sequence of flux states in a simple network. In this section, we wish to consider in more detail the sequencing of flux states in specific networks. As a first example we consider operation of the MAD-N scheme of Sec. 4-5 from the network point of view. We then show how the network representation is useful in deriving a number of variations on this scheme. One of these variations in turn is used in the derivation of the flux-doubling scheme of Sec. 5-5, an interesting scheme whose network representation is that of the lattice of Fig. 5-12(b).

MAD-N Sequencing in Network Form. In connection with Fig. 4-8, it was indicated how the pattern of flux representing a binary *one* is propagated along the structure. To increase facility with the network representation, let us follow the same flux switching in terms of the network diagram of Fig. 5-19(a), in which branches representing coupling-loop impedance are ignored. As a starting point, we assume that a *one* is introduced from the left during the first $O \rightarrow E$ pulse (Fig. 5-19(b)). (Drive generators will be indicated in later phases.) It is clear from the initial state of B_E that no flux can be switched in it during this advance operation. Flux could switch through output leg D_E , but there is no closing path of low magnetic impedance comparable to the path through C_E . The resulting flux state is shown by the arrows inside the boxes of Fig. 5-19(c), which now portray the "present" flux state just prior to application of the Clear- O pulse.

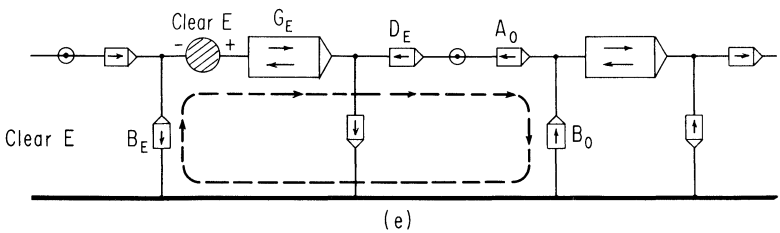
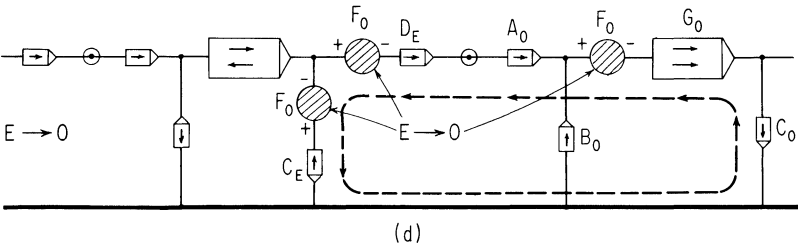
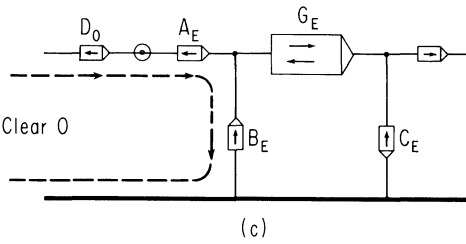
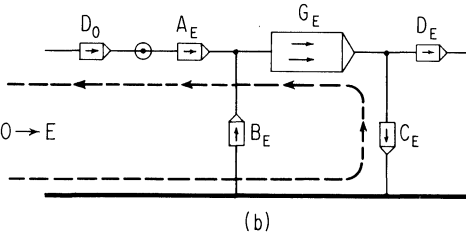
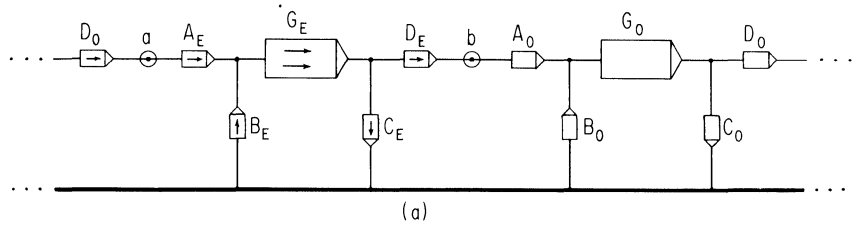


Fig. 5-19. Tracing the flux-switching sequence in the network representation of the MAD-N scheme.

In response to the Clear- O pulse, flux switches in input elements A_E and B_E , that is, locally about the input minor aperture. Flux could conceivably switch along the path $G_E C_E$ as well, but the mmf drop across Branch B_E is so small that one can assume negligible flux switching along the much longer path.

The flux switching path during the subsequent $E \rightarrow O$ pulse is indicated in Fig. 5-19(d). In accordance with the drive arrangement of Fig. 4-9, $E \rightarrow O$ drive generators are shown in series with Branches D_E , C_E , and G_O (the latter providing receiver bias). The switching path, which includes all three of the $E \rightarrow O$ generators, is the same as in Fig. 5-19(b), except for being shifted one stage along the network. The subsequent Clear- E generator appears in series with the driven leg G_E (Fig. 5-19(e)). The resulting flux switching is again as in Fig. 5-19(c), but shifted one stage to the right along the network.

We have now translated the entire shifting sequence to the magnetic network representation. Of course, nothing new was added in the process, since we simply converted from one form of representation to another. We will find in the subsequent study, however, that this network form is very useful. After a bit of practice, one may use shortcuts such as not drawing boxes at all on each branch, and so on. This permits rapid sketching of different types of shifting schemes.

Note in Fig. 5-19 that each branch is cycled once, i.e., switched two times, during a single shift cycle. This is generally true for transfer schemes, except where nonswitching branches are present solely for the sake of static flux closure. Hence, if there are n branches per bit length (excluding the static-closure type), there must be $2n$ switchings per bit length during one clock cycle, when a *one* is being transferred. Hence it is necessary that

$$m_1 + m_2 + m_3 + m_4 = 2n \quad (5-13)$$

where m_i is the number of switchings during the i th phase. From Fig. 5-19(d) and (e) it is easy to see that in this example all the m_i have the same value, namely, 5, and that indeed $n = 10$, that is, there are 10 branch elements per bit length.

The closed paths required for flux changes define the least complex structure required for any particular scheme. The structure is usually augmented in one way or another, however, with nodes and branches that are not essential to the basic scheme, but which allow certain desired types of physical realization and provide practical improvement for actual circuit design and

operation. For example, the network structure just considered is not the minimal one for this particular sequence of flux changes in the paths indicated, and thereby provides us with the opportunity to illustrate a number of different points, namely:

1. network reduction by node and branch elimination, in order to arrive at the minimal structure;
2. some advantages in the nonminimal structure; and
3. the use of exchange and addition of nodes (and branches) in order to obtain an alternate nonminimal realization.

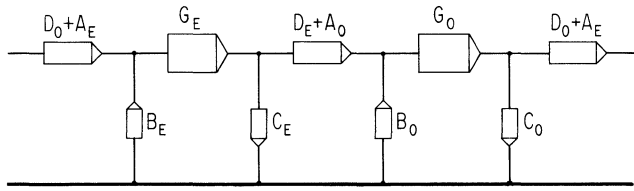
All of these variations will involve the identical sequencing of flux states, although the alternate core shapes and circuits obtained will look quite different from the original ones.

Stabler and Engelbart Variations. Suppose we first exchange all of the synthetic nodes of Fig. 5-19(a) for physical nodes, and then eliminate these nodes, as indicated in Fig. 5-20(a), on the basis that two branches of the same material and cross-sectional area connected in series are functionally identical to a single branch. Conversion of this reduced network to all synthetic nodes now leads to the toroid-wire circuit of Fig. 5-20(b), which was described by Stabler (1961).

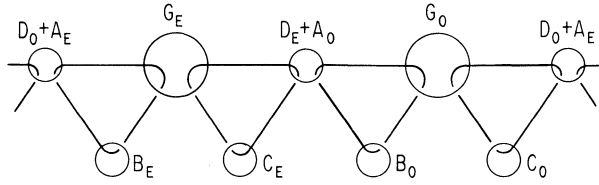
Further examination of fig. 5-20(b) shows that Branches D_E and A_O in fact serve no function necessary to the scheme of sequencing, except that the $E \rightarrow O$ drive is applied on Branch D_E (Fig. 5-19(d)). However, an equivalent drive may be achieved with generators on Branches C_E and G_E (equivalent in the sense of providing the same net drive mmf in each network loop). Branches $D + A$ may thus be eliminated and the pair of flanking nodes combined into one single node, as shown in Fig. 5-20(c). This network is minimum in the sense that no further reduction can be made for the sequence of flux-change paths involved. The toroidal-core circuit realization of this minimal network is shown in Fig. 5-20(d). This development was originally done by Engelbart (1959).

Variations Avoiding Interaction of Adjacent Bits. Although this minimum form of the scheme can be successfully operated, we would like to point out the type of difficulty that one may encounter when eliminating nonessential branches as we have done in going from the network of Fig. 5-19(a) to the network in Fig. 5-20(a) and then to the one in Fig. 5-20(c).

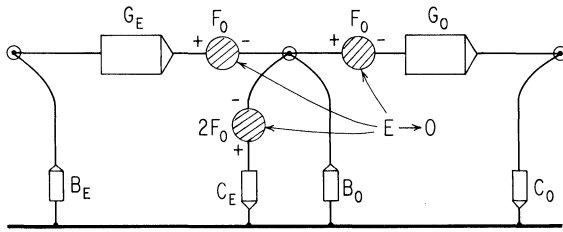
Let us consider the case of two adjacent *ones* propagating along the register. Suppose in Fig. 5-21(a) that a *one* is stored in the O



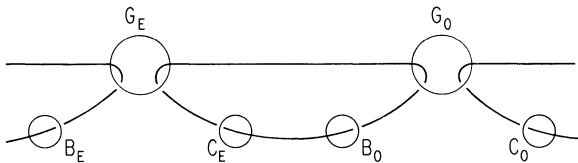
(a)



(b)

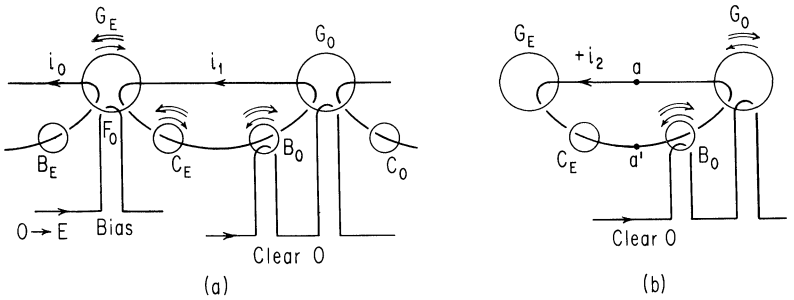


(c)

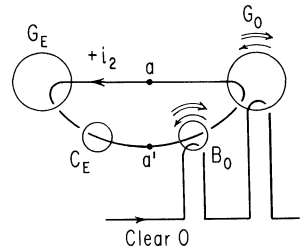


(d)

Fig. 5-20. The Stabler and Englebart reductions of the MAD-N scheme.



(a)



(b)

Fig. 5-21. Interaction of adjacent bits in the Englebart circuit.

stage, in which case Cores B_0 and G_0 are in their set states. Suppose that a *one* is also stored in the preceding O stage to the left (not shown). At the next $O \rightarrow E$ pulse, Core G_E will be switched by loop current i_0 (as indicated by the double-lined arrow), and a current i_1 will flow. Since B_0 is in a set state (due to a *one* stored in the O stage), the loop current i_1 tends to simultaneously switch some flux in both Cores C_E and B_0 , as indicated by the double-lined arrows above both of them. But, any flux switched in Core B_0 is pumped back into Core C_E during the very next Clear- O pulse, and the final flux configuration is nominally the same as though Cores G_E and C_E had switched simultaneously in the first place (as would have been the case if the right-hand O stage had held a *zero*). However, although the final flux configuration is nominally the same, it is clear that there will be slight differences in $\Delta\phi$ losses (because of the extra transfers through resistive coupling loops), depending on information states, and this may result in a problem of sensitivity to the information state. With either of the "augmented" schemes of Figs. 5-19(a) or 5-20(a), this interaction can be prevented because the "redundant" branches are in their clear states during this transfer and therefore can be unconditionally held clear. This would provide complete isolation between stages, except for small elastic flux changes induced by the holding mmf and by loop currents.

The ability to hold these redundant cores in their clear states, so as to achieve interstage isolation, is even more important with regard to back transfer. This can readily be seen in connection with Fig. 5-21(b). If during the Clear- O phase, we merely drive Core G_0 , then back current $+i_2$ tends to set output Core C_E (which could be very harmful since C_E is to be a transmitter on the next $E \rightarrow O$ pulse), in addition to clearing Core B_0 as desired. To minimize switching of Core C_E , we can drive Cores B_0 and G_0 simultaneously. If these cores could be switched at exactly the same rate, there would be zero voltage across terminals $a-a'$, and hence no back transfer. However, it is difficult to ensure that two cores switch at exactly the same rate, especially when they are of different size and when one is loaded during the switching (output circuit loading on G_0) and the other is not. Note that it is not a sure solution to deliberately drive B_0 harder than G_0 , since a current $-i_2$ then tends to clear C_E , which would be harmful in the case of C_E containing a *one*.

Isolation between bits in the nonminimal schemes is achieved by the series network branch ($D_E + A_0$) between adjacent bit storage positions. In the minimum scheme of Fig. 5-20(c), no such element

separates C_E from B_O , and it is for this reason that these branches thus become simultaneously involved with the set state patterns of two bits.

It may be noted that in the Russell scheme of Fig. 4-5(a), which has the identical circuit configuration as that of Fig. 5-20(d), the two singly linked cores in any loop are simultaneously in a set state only in connection with the *same* bit of information. (This results from setting and then immediately clearing the preceding coupling core on adjacent clock phases.) Hence the coupling cores of that circuit provide the type of isolation that is obtained for the present scheme only from the additional coupling cores occurring in an augmented version. (Still another scheme with this same circuit configuration and in which this type of isolation can be obtained in the minimal form is treated in Sec. 7-4.)

Network Variations Resulting in Major-Aperture Coupling. We wish now to show how one may depart from the minimum structure of Fig. 5-20(c) in a way that produces a nonminimum network with some potential advantages (as well as possible disadvantages) relative to the other nonminimal networks of this section, and that results in a multileg circuit realization that is quite different from the original circuit of Fig. 5-10(a).

Following the techniques of Sec. 5-3, let us introduce new nodes by dividing each G branch of Fig. 5-20(c) and inserting a new synthetic node between the halves as shown in Fig. 5-22(a). A physical realization of this network is shown in Fig. 5-22(b), with turns ratio N_T/N_R inserted, and with clear states indicated by the arrows. Note that what we have been calling an O stage or E stage no longer corresponds directly to any one given multileg element. Rather, "half of an E stage" appears on one multileg core, and the other half on the adjacent core, and similarly for the O stages. To emphasize this fact, the cores are labeled alternately as OE , EO , and OE . The flux-switching path for $O \rightarrow E$ transfer of a *one* is shown by the dashed line in Fig. 5-22(a).

The operation of both multileg versions, Figs. 5-10(a) and 5-22(b), is clearly similar. However, the geometries are very different, and thus there could be important differences in details of operation—for example, in terms of soft-threshold properties (see Sec. 4-5). An obvious advantage of the present circuit is that the coupling loops link major instead of minor apertures. This makes physical wiring easier, and also, because larger wire could

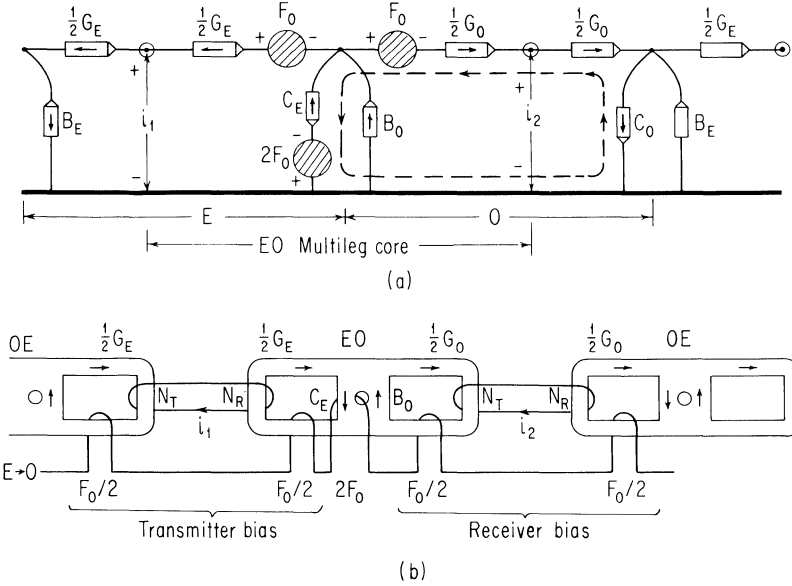


Fig. 5-22. Achieving major-aperture coupling by inserting new synthetic nodes.

be used, there would be greater flexibility in the design of the coupling-loop impedance.

One other effect must be noted in order to underline an important difference that can result from manipulation of nodes. During *one* transfer, there is a maximum net drive of $2F_0 - F_0 = F_0$ tending to switch flux in the backward direction (around the major aperture of the transmitter in Fig. 5-10(a)). Neglecting soft-threshold effects, this mmf would cause no backward major-aperture switching. In the circuit of Fig. 5-22(b), however, the drive $2F_0$ applied to the transmitter tends to switch flux about the directly coupled half of the transmitter, since the effective threshold of this leg is just $F_0/2$ plus the portion of transmitter bias applied to it. As a result, coupling-loop current $-i_1$ flows. However, the resulting mmf $N_T i_1$ acting on the left-hand part of the E stage cannot exceed its effective threshold. Hence, except for parasitic impedance, the coupling loop presents a short circuit on the left-hand side of the EO core, which is thus largely prevented from switching. But the small amount of switching that would occur represents a flux loss to be accounted for in quantitative analysis.

With careful design, any of the nonresistance circuits in this section can be made to operate reasonably well. These circuits are primarily of academic value, however, because for proper operation, the advance current pulses must be kept within too limited a range, at least in the case of existing cores. In the next section we illustrate an improved, 'flux-doubling' scheme, which has actually been used for design of a prototype system. We will see how the network representation greatly aids in understanding the basic operation of this relatively complex but very intriguing scheme.

5-5 The Flux-Doubling Scheme and Its Network Representation

We now derive a scheme whose network representation is precisely that of the lattice of Fig. 5-12(b). We will see that there is an inherent flux-doubling feature in the basic transfer scheme, which provides an important flux-gain mechanism. To derive this scheme, we return to the circuit of Fig. 5-21(b) where we noted a potential back-transfer problem during the Clear- O pulse if Cores B_O and G_O switch at different rates. As a first step towards equalizing their switching rates, we might try using identical cores in these positions, as suggested in Fig. 5-23(a). The turns N_4 and N_5 (on the Clear- O winding) are adjusted so as to equalize as much as possible the net mmf on Cores G_O and B_O during the Clear- O pulse.

Note that the drive conditions for Cores G_E and B_E are very similar, G_E being set by a counterclockwise loop current at $O \rightarrow E$ drive time and B_E by a comparable magnitude of clockwise loop current at Clear- O drive time. In fact, in order to prevent G_E from being cleared by the latter loop current, positive bias windings on G_E and B_E have been added to the Clear- O line. But output conditions for Cores G_E and B_E are still very different. Specifically, any flux switched in G_E is coupled on ahead, whereas flux switched into B_E "dead ends" there, being used merely to balance the $\Delta\phi$ from G_E to prevent back transfer during Clear- E . The question arises as to whether we can make Core B_E comparable to Core G_E relative to output as well as input, i.e., make B_E a coupling core also. Actually, all that is required is to thread the transmitting core ends of the coupling loops through the B as well as the G cores, as indicated by the dashed lines in Fig. 5-23(a) and by the solid lines in Fig. 5-23(b), where the coupling circuit is abstracted and redrawn more symmetrically. Since loop current during the

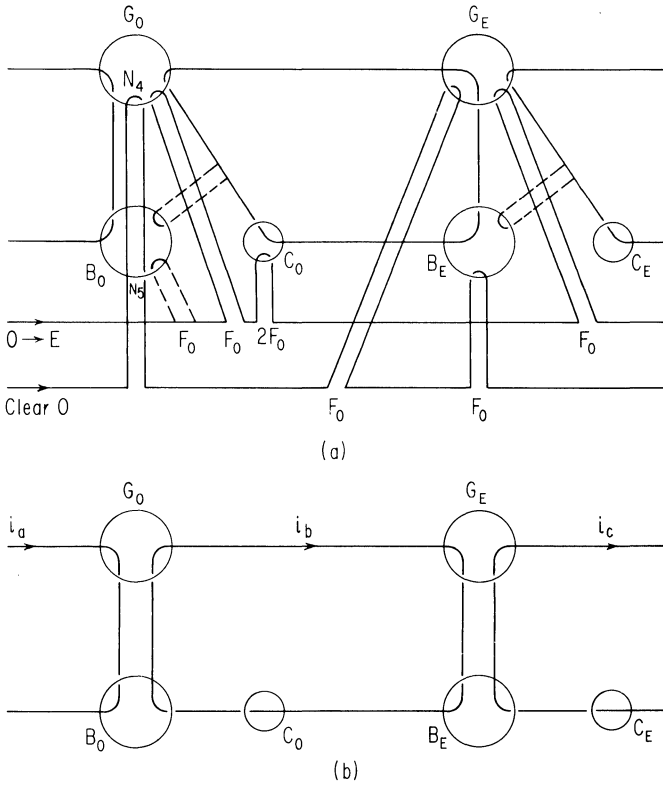


Fig. 5-23. The all-toroid flux doubler.

$O \rightarrow E$ phase now negatively links B_0 in addition to G_0 , B_0 is positively biased (dashed winding in Fig. 5-23(a)) to oppose the clearing tendency of loop current. Further, based on symmetry, we can now set $N_5 = N_4$, achieving a circuit described by Bennion, et al. (1961).

Demonstration of the Doubling Effect. The above alteration makes it much easier to switch B_0 and G_0 at approximately equal rates, but along with this we have actually achieved a much more interesting property. We wish to show that inherent doubling of $\Delta\phi$ is now achieved during transfer (and hence that we do not require $N_T/N_R > 1$ in order to achieve a transfer ratio $G > 1$). As an aid, note first that the coupling circuit of Fig. 5-23(b) is exactly that of Fig. 5-12(a), and hence the network representation is the lattice network of Fig. 5-12(b), redrawn in Fig. 5-24(a). To verify that

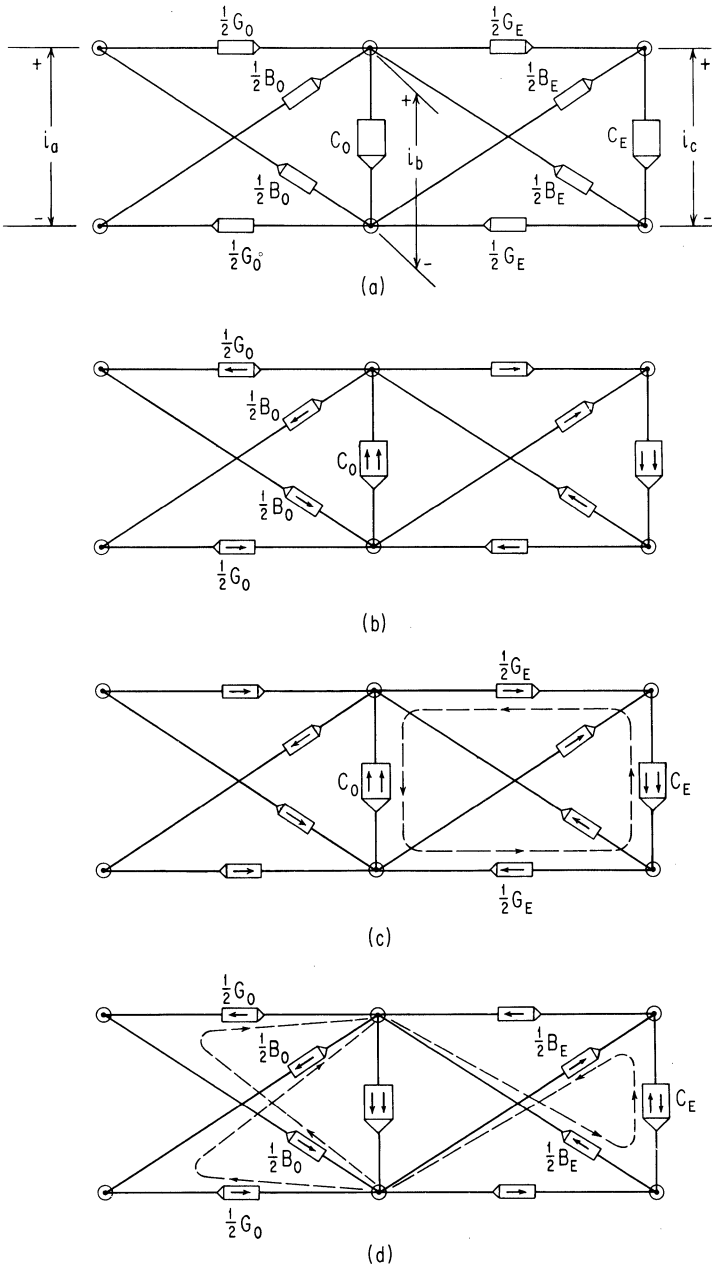


Fig. 5-24. Flux state sequencing in the flux doubler.

flux doubling actually occurs, let us review the sequence of flux transfers during a half cycle of operation. Suppose that we initially have one unit of set flux stored in each of the B_O and G_O branches and two units in Branch C_O , and suppose that these quantities represent less than half the capacities for each of the branches. Let the arrows inside the boxes of Fig. 5-24(b) represent the directions of set flux. The $O \rightarrow E$ drive causes the two units of flux in C_O to be transferred to G_E (Fig. 5-24(c)). Then the Clear- O drive causes the two units of flux stored in B_O and G_O together to be transferred to B_E (Fig. 5-24(d)). During these two phases, the flux switched into G_E and B_E is coupled additively into C_E , resulting in four units of flux being set into C_E . Thus, after this half cycle of operation, we have the E branches set comparably to the initial state of the corresponding O branches, but with twice the original amount of signal flux. These statements of course apply also to the corresponding cores of Fig. 5-23.

As the flux state is transferred along the register, the level increases until saturation of either the C cores or the B and G cores causes limiting. For steady-state register operation, this limiting effect ensures that overall unity gain is achieved, though we start with flux gain of 2:1 before losses are counted, as compared to 1:1 for any of the previous schemes, assuming the same turns ratio in each case.

Derivation of the Multileg-Core Doubler. Although the back transfer problem was reduced in converting to a doubling scheme, the toroid doubler of Fig. 5-23 still suffers from potential problems of adjacent-bit interaction. Let us now develop a much improved, multileg-core version of the doubler. We could proceed by adding branches to the network a step at a time in order to minimize interaction; instead, however, let us start on a different track and compare the results.

Suppose that we wish to utilize a double-transmitter arrangement, as in Fig. 5-25(a), in order to increase flux gain. Then we must ensure that these elements are both in the same state before transmission. One technique for accomplishing this is to transmit from one element to the other before transmitting from both together. Such an arrangement is indicated in Fig. 5-25(a), the local transmitter-to-transmitter transfer being affected by a pulse labeled TT . The sequence is: (1) read into the top element; (2) transmit to the lower element; then (3) read from both simultaneously. The TT transmission can take place during clearing of

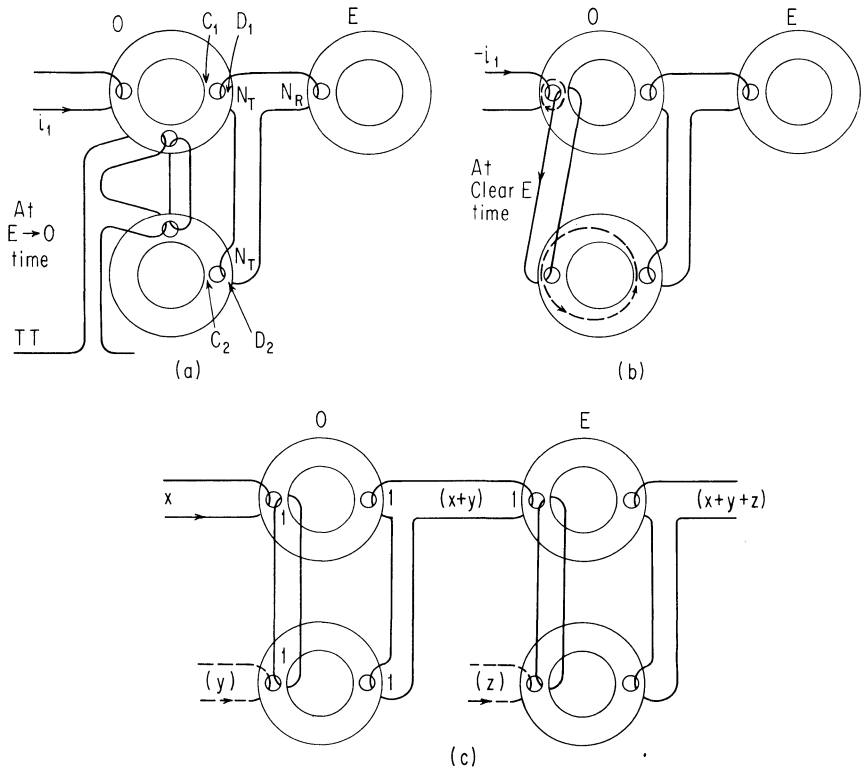


Fig. 5-25. Multileg-core flux doubler.

the previous stage, so that no extra time is actually required for this operation.)

As indicated in Fig. 5-25(b), the TT loop need not connect with a separate aperture of the upper core but in fact can connect to the same input aperture. Not only does this reduce the number of apertures required, but it improves the operation. Assuming a *one* had been received during the previous $E \rightarrow O$ transfer, then during the simultaneous Clear E and TT operation, negative input current (resulting from the clearing of the previous E element) aids in switching around this aperture.

A flux-transfer arrangement based on this scheme is indicated in Fig. 5-25(c). An N_T/N_R ratio of unity has been shown, in particular $N_T = N_R = 1$, which is convenient for such a scheme. The

TT loops have been drawn symmetrically here, and a second set of input windings have been suggested by the dashed lines. (In terms of the design example of Sec. 10-5, we will see that this doubler circuit leads naturally to the formation of a two-input OR function $x + y$, as indicated by the labeling of input and output variables in Fig. 5-25(c).)

There is a basic similarity of the toroid doubler and the multileg version. Legs C_1 and C_2 of Fig. 5-25(a) play the role of the output toroid C in Fig. 5-23. During the input operation, a unit of $\Delta\phi$ is switched in Leg C_1 , and stored there, then $\Delta\phi$ is switched in Leg C_2 , and stored there, and then both units of $\Delta\phi$ are transmitted simultaneously to the next receiver. Legs D_1 and D_2 , which are needed for static flux closure in the multileg elements, have no counterpart in Fig. 5-23, though they provide extra isolation between stages, as discussed in connection with Fig. 5-21. Thus, again, the multileg version has the advantage of decreased bit-interaction problems, as is usual when using input apertures. The multileg version also has the easy facility for adding an extra input, as in Fig. 5-25(c), which is important in general logic circuits.

Continuous Magnetic Circuit. A magnetic network with only physical nodes transforms to a continuous circuit with no coupling loops at all. Though such a circuit is conceptually simple, physical realization is very difficult. Further, with no coupling loops present in the circuit, we must obviously rely on some other $\Delta\phi$ -gain mechanism to achieve a transfer ratio > 1 . The flux-doubling effect is an ideal one for this purpose.

Assume that all synthetic nodes in the flux-doubler network of Fig. 5-24(a) are replaced by physical nodes. The nonplanar circuit realization is then as shown in Fig. 5-26, with the clear state indicated, and with the method of driving suggested by the $O \rightarrow E$ drive line. The doubling effect takes place in this structure in exactly the fashion described in connection with the network diagrams of Fig. 5-24, thus making it unnecessary to rely on any other gain mechanism to achieve $G > 1$.

One problem in designing an operating circuit in this form is the need for built-in flux clipping, or some other nonlinear loss mechanism, for making $G < 1$ for low values of $\Delta\phi$. But this problem is generally not difficult to solve so long as one has ample inherent $\Delta\phi$ gain to begin with, as is the case here. Such structures have been designed and analyzed relative to flux-clipping ratio and other parameters, and special devices have actually

been fabricated, with laboratory operation demonstrated in one case of simulation with a planar continuous structure (Van De Riet and Bennion, 1965). However, fabrication for practical use appears to be infeasible at this time.

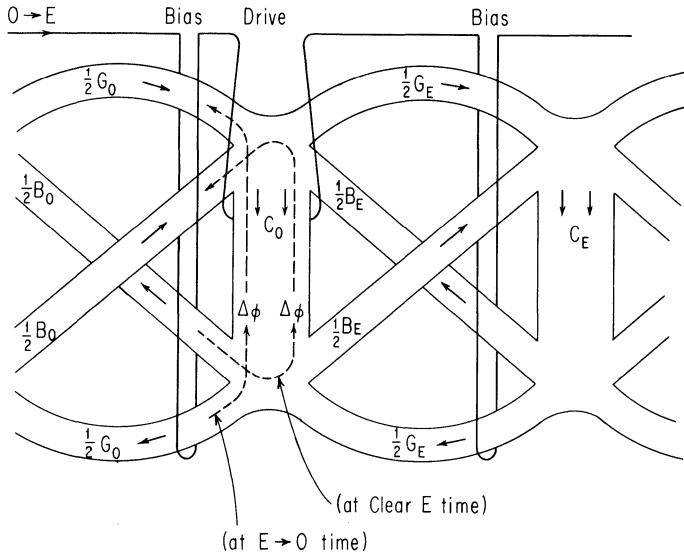


Fig. 5-26. Continuous magnetic circuit.

5-6 Summary

In an electrical diagram of a core-wire circuit, current flow can be traced simply by following the lines representing electrical conductors. It is generally not easy, however, to follow the flow of flux change. By converting to a magnetic diagram, however, where the lines now represent magnetic conductors, it is equally easy to follow flux flow. Since flux linkage is our primary signal parameter, the ability to quickly sketch magnetic equivalents of core-wire circuits is very useful.

In Secs. 5-1 to 5-3 we have shown how to convert from an electrical circuit to an equivalent magnetic network and to reconvert from a network to its corresponding circuit form. With a few basic principles, the conversion and reconversion is actually quite simple and the rewards of mastering the techniques well warrant the effort. Not only is the network representation useful in circuit analysis, but it provides a useful domain in which to vary the basic structure and derive thereby new variations and new schemes. In

other words, it is often more convenient to work in the magnetic network domain than in the electric circuit domain. By means of the network representation, it is often easy to show the equivalence between circuit forms that on the face appear to be very different. Also, it is simpler with network techniques to show how to combine various core elements, e.g., simple toroidal cores, into more complex multileg cores.

In Secs. 5-4 and 5-5, some new core-wire scheme variations are derived, partly as an exercise in network manipulation. The flux-doubling scheme of Sec. 5-5 is of particular interest in that it well illustrates the power of the network representation as an aid in understanding the basic operation of a relatively complex scheme; further, this basic scheme is utilized in construction of a core-wire logic system that is discussed in Sec. 10-5.

MAD-R SCHEME

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The term MAD-R, in which R stands for Resistance, is an abbreviated name for a particular type of scheme that has been used in the majority of core-wire logic applications up to this time.

This scheme was developed independently by Briggs and Lo (1961), Gianola (1960), Bennion (1960), and possibly others. Because of the importance of the MAD-R scheme, three different derivations of it are presented in this chapter, as summarized in Fig. 6-1. Though the reader may bypass the second and third of these without any loss of continuity, each derivation emphasizes different aspects of the circuit.

Following these derivations, the remainder of the chapter is concerned with design techniques for this type of circuit. Though the basic circuit form is quite simple in appearance and can readily be made operable, considerable care is required to obtain optimum performance. The design technique presented here is rather bulky and cumbersome (typical of highly nonlinear processes), though, in fact, it is rather simple to apply, with a little practice, and highly useful. By following this procedure, one almost invariably obtains a near-optimum design in short order. The method is a mixture of cut-and-try and rule of thumb based on empirical data, though there is plausible reasoning and purpose behind each step, which we try as much as possible to present as we go along.

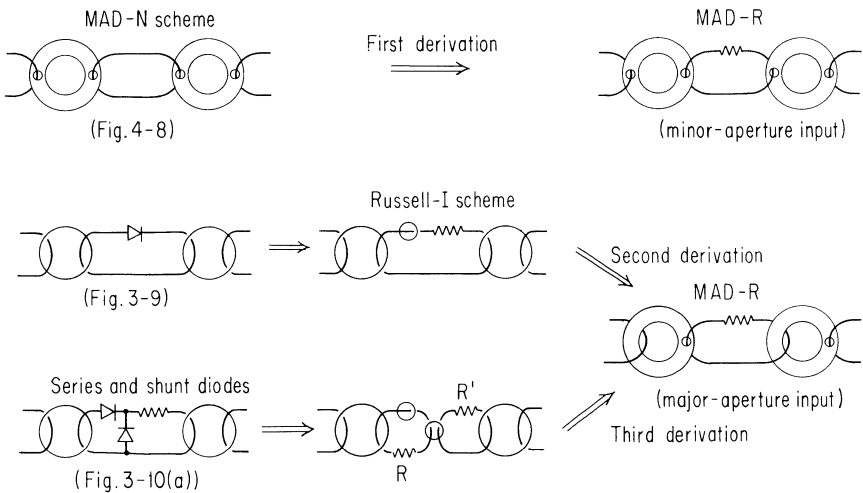


Fig. 6-1. Outline of three different derivations of the MAD-R scheme.

6-1 Derivation from MAD-N Scheme

For convenience, the circuit of the MAD-N scheme is redrawn in Fig. 6-2(a). For this circuit, recall that the advance currents

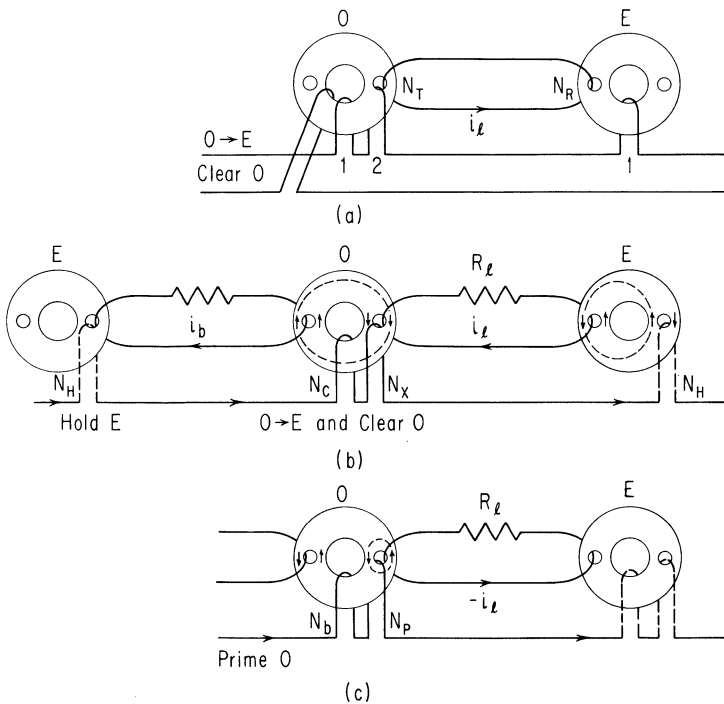


Fig. 6-2. Derivation of the MAD-R circuit from the MAD-N scheme.

must be great enough to cause transfer of flux with unity gain for the *one* state, yet are strictly "threshold-limited" at high levels in order not to cause spurious setting of a transmitter in the *zero* state. In the interest of enlarging this operating range, note that if it were possible to transfer flux to the receiver simultaneously with clearing the transmitter, then the drive current would no longer be threshold-limited, since a *zero* flux state in the transmitter could not be inelastically disturbed. To be able to operate in this manner, we must, first of all, reverse the polarity of one end of the coupling loop, as shown in Fig. 6-2(b), where the desired flux-switching paths during $O \rightarrow E$ are indicated. Second, to achieve the required transmitter state prior to $O \rightarrow E$ transfer, flux must be reversed locally around the output aperture (after still earlier setting), as indicated in Fig. 6-2(c). The polarity of induced loop current during this local flux reversal is such as not to switch the receiver (Core E), and the transmitter flux change during this phase is dissipated in loop resistance R_L . Thus a resistance type of scheme is indicated.

The operation indicated in Fig. 6-2(c) is commonly called *priming* and the associated drive current is labeled *Prime O*. This phase of operation is analogous to the "restore" phase of Secs. 4-1 to 4-3, though here the elements being restored and the elements that we must avoid disturbing in the process are legs of multiaperture cores. We will see in a moment why the prime phase, like the restore phase, is relatively slow, so that whatever advantages are to be gained by this scheme relative to the MAD-N scheme are at the expense of some loss in speed of operation.

The priming mmf in this circuit is provided by current through Winding N_p in the output minor aperture. The winding N_b is used to bias the main aperture of the core so as to increase the maximum allowable priming mmf. Since the main-aperture mmf due to priming current must always be kept below main-aperture threshold, priming current can simultaneously be applied to the receiver elements without disturbing them, as indicated by the dashed windings in Fig. 6-2(c). In fact, the priming current may even be left on continuously, as its effects during the transfer phases are readily overcome by the advance currents. Thus, priming may be achieved with a single dc current applied to all cores, as in the case of the restore currents of Secs. 4-1 to 4-3. Pulsed driving is required, therefore, for only two of the four phases of operation and is optional for the other two.

In summary, the basic clock cycle is Prime O , $O \rightarrow E$, Prime E , $E \rightarrow O$, ... The effect of priming, following an $E \rightarrow O$ transfer, is to switch flux locally about all O -core output apertures that were set during the $E \rightarrow O$ transfer. (Flux is dissipated in loop resistance during this phase.) Flux transfer during the subsequent $O \rightarrow E$ transfer, which simultaneously clears all O -elements, is indicated in Fig. 6-2(b). An important point to note is that the flux switched in a core while it is being cleared links the back loop, thereby inducing a back-loop current (i_b in Fig. 6-2(b)) in a direction to set (hence disturb a *zero* state) in the previous receiver core. To prevent such switching, a Hold- E winding of N_H turns is placed on the output leg of each receiver core.

A physical wiring arrangement for this circuit that has sometimes been used is shown in Fig. 6-3 (AMP, 1960; Sweeney, 1961), where the multileg elements are shown in cross section. Typical numbers of turns are indicated on each winding. The clear windings are each wired straight through the main apertures of each bank of cores. Because N_H , N_X , and N_p generally have equal values (in this case 3) they are realized by a single common winding

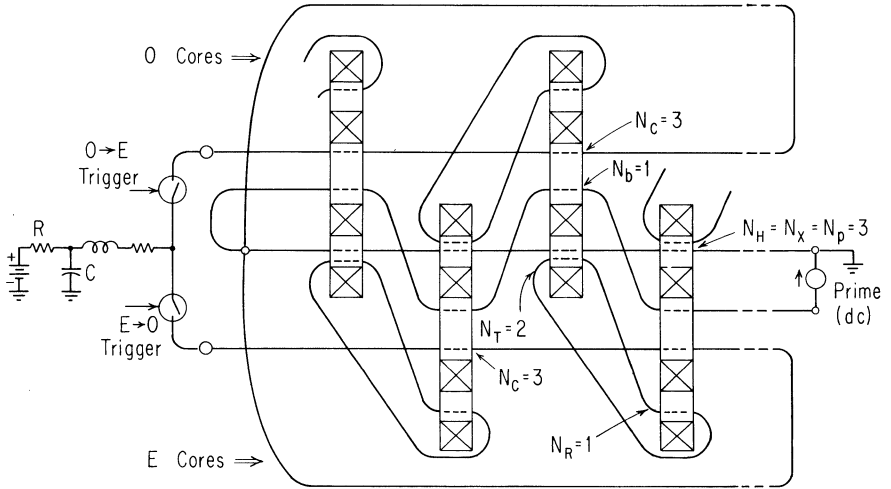


Fig. 6-3. A physical wiring arrangement for the MAD-R circuit.

wired straight through the output apertures of all the cores. The two phases of clock-pulse currents may be provided by two triggered switches (e.g., four-layer diodes, silicon-controlled rectifiers, transistors, thyratrons), discharging damped half-sinusoidal pulses from a common RC charging circuit. The dc source need not have a very large source resistance for dc current, but should be well isolated from the pulse sources (as in Sec. 2-8, for example, by the use of a series inductance). For applications in which zero standby power is desired, it is possible to arrange the wiring such that the very same current that recharges the driver capacitor C simultaneously constitutes the prime current as well.

Current Tolerances Versus Speed. We will now derive an approximate value for the upper limit on speed of this circuit, relative to the MAD-N scheme, and then consider what has been gained in terms of drive current tolerances. The clearing phase for the MAD-N scheme and the advance phase for the MAD-R scheme can both be operated at relatively high speed and high tolerances, and hence we need compare limits only on the advance phase for the former and the priming phase for the latter.

First, consider the speed of the MAD-N circuit (Fig. 6-2(a)). With the $O \rightarrow E$ current equal to its maximum value F_0 , the receiver is biased to threshold, and hence its rate of switching can be

estimated by

$$\dot{\phi}_R = \bar{\rho}(F - F_0) = \bar{\rho}(N_R i_\ell + F_0 - F_0) = \bar{\rho}N_R i_\ell \quad (6-1)$$

assuming the core model of Sec. 1-1. Assuming the transmitter minor-aperture path length to be ideally zero, so that the advance mmf $2F_0$ is fully bucked by coupling-loop mmf $N_T i_\ell$, then $i_\ell = 2F_0/N_T$, or

$$\dot{\phi}_R^{\max} = \bar{\rho}N_R \frac{2F_0}{N_T} = 2\bar{\rho}F_0 \quad (6-2)$$

as an upper limit, assuming a unity turns ratio, that is, $N_T = N_R$. The corresponding minimum value of switching time τ is equal to $2\phi_r/\dot{\phi}_R^{\max}$, that is,

$$\tau_{\min} = \frac{\phi_r}{\bar{\rho}F_0} \quad (6-3)$$

For the MAD-R scheme, the maximum current coupled into the loop during priming is also $2F_0/N_T$, but the emf $N_T \dot{\phi}_T$ must now be balanced by dissipation in R_ℓ ; hence $N_T \dot{\phi}_T = i_\ell R_\ell$ or

$$\dot{\phi}_T = \frac{2F_0 R_\ell}{N_T^2} \quad (6-4)$$

By integration of Eq. (6-4) over a priming time T , we obtain the value

$$T = \frac{N_T^2 \phi_r}{R_\ell^{\max} F_0} \quad (6-5)$$

where R_ℓ^{\max} is the largest value of R_ℓ for which $G \geq 1$ can be obtained during advance time. From Eq. (2-9), we see that even with arbitrarily large advance drive to remove the effect of receiver threshold, $G = 1$ implies

$$R_\ell^{\max} = N_R 2\bar{\rho} \left(\frac{N_T}{N_R} - 1 \right) \quad (6-6)$$

From Eqs. (6-5) and (6-6)

$$T = \frac{n^2}{n-1} \frac{\phi_r}{\bar{\rho}F_0} \quad (6-7)$$

where $n = N_T/N_R$. By minimizing T with respect to turns ratio n , we find

$$T_{\min} = \frac{4\phi_r}{\bar{\rho}F_0} \quad (6-8)$$

with $n = 2$.

Based on this highly idealized comparison, we see from Eqs. (6-3) and (6-8) that the MAD-R scheme is on the order of four times slower than the MAD-N scheme. This approximate result can be shown to be true for comparison of many other resistance and nonresistance schemes as well.

In deriving approximate current tolerances for the two schemes, we again need consider only the priming drive for the MAD-R scheme and the advance drive for the MAD-N scheme, since only these currents have strict upper, as well as lower, limits (governed by the core threshold). At the upper limits, either spurious setting in the *zero* case or spurious unsetting in the *one* case occurs. The upper limit on mmf is the same in both cases, namely, an amount related to the minimum path length l_M^{\min} around the major aperture. However, the lower limit on mmf, especially for very low-speed operation, can be much more favorable in the case of priming, since the priming mmf need be only large enough to switch flux slowly around the output aperture, whereas for the MAD-N scheme, advance mmf must switch the transmitter rapidly enough to set the receiver without undue losses in the coupling loop. The priming current ratio I_{\max}/I_{\min} is therefore directly proportional to the l_M^{\min}/l_m^{\max} path-length ratio, where l_m^{\max} is the maximum length of the flux-switching path around the output minor aperture. In contrast, as we decrease advance mmf for the MAD-N scheme, and realistically assume that receiver bias decreases along with it, enough loop current must be induced to bring the receiver up to threshold from the lowered bias point and to supply excess mmf for switching at some minimum rate. Practically speaking, an advance current ratio I_{\max}/I_{\min} of more than about 2/1 for the MAD-N scheme is difficult to obtain, even for large values of path-length ratio l_M^{\min}/l_m^{\max} . Yet with very practical values of this ratio, say about 4/1, priming current ratios I_{\max}/I_{\min} of 6/1 and even greater are obtained. (Such large current tolerances are particularly important for operation over a wide temperature range, because of the shift of threshold with temperature. A detailed analysis in Sec. 6-8 demonstrates how such large tolerances are actually achievable.)

6-2 Second Derivation, from Russell Type-I Scheme

This derivation helps to emphasize the importance of holding output legs of receivers against back transfer and also the advantages of the MAD-R circuit relative to similar schemes using only toroidal cores. The circuit of Fig. 3-9, with one series diode per loop, is redrawn in Fig. 6-4(a), and its corresponding core-wire version, referred to as the Russell Type-I scheme, is drawn in Fig. 6-4(b). This circuit tends to be marginal in operation, because of a back-transfer problem (Sec. 4-2). We find that one type of alteration to remove this problem leads naturally to the MAD-R scheme, emphasizing its advantages in the use of "holding" to avoid back transfer.

The magnetic network for this circuit is shown in Fig. 6-4(c). Flux directions within the elements are those resulting from *one* transfer during $O \rightarrow E$, that is, setting of G_E and D_E , with subsequent "priming" of Core D_E , that is, slow clearing of Core D_E , with dissipation into the shunt resistance. The back transfer problem is now obvious. During the subsequent $E \rightarrow O$ transfer, there is just as much tendency to switch the previous G_0 element as the forward G_0 element, as suggested by the dashed switching path. The forward direction is favored only because of the asymmetry resulting from $N_T > N_R$.

To eliminate the back transfer problem, it is necessary to provide an effective shunt path between the G_E branch and the left-hand G_0 branch. The shunt branch D_0 is in the desired position, but is already saturated in the intended switching direction. However, loop resistance can also serve as a shunt path. To take advantage of this fact, let us add (in each stage) a new series magnetic branch labeled H (to anticipate the fact that we will use this new branch for holding against back transfer). In Fig. 6-4(d), if the clear state of the new H_0 branch is in the direction indicated, then it can be unconditionally held during the $E \rightarrow O$ transfer, thereby eliminating any chance of back transfer. Now to provide a suitable shunt path for transfer, R'_m is added at the new coupling-loop node s . (We will see in a moment that resistance R_m is no longer needed.) To obtain proper $E \rightarrow O$ transfer, flux must be set into the corresponding new branch H_E prior to $E \rightarrow O$ drive. In this case, the flux switching path during $E \rightarrow O$ transfer, as indicated in Fig. 6-4(d), is through R'_m , G_E , and H_E , to G_0 and D_0 (not shown) in the next stage. Prior reversal of flux in branch H_E is easily achieved by altering the priming operation. In the original scheme of Fig. 6-4(b) and (c), the D_E core is primed immediately after

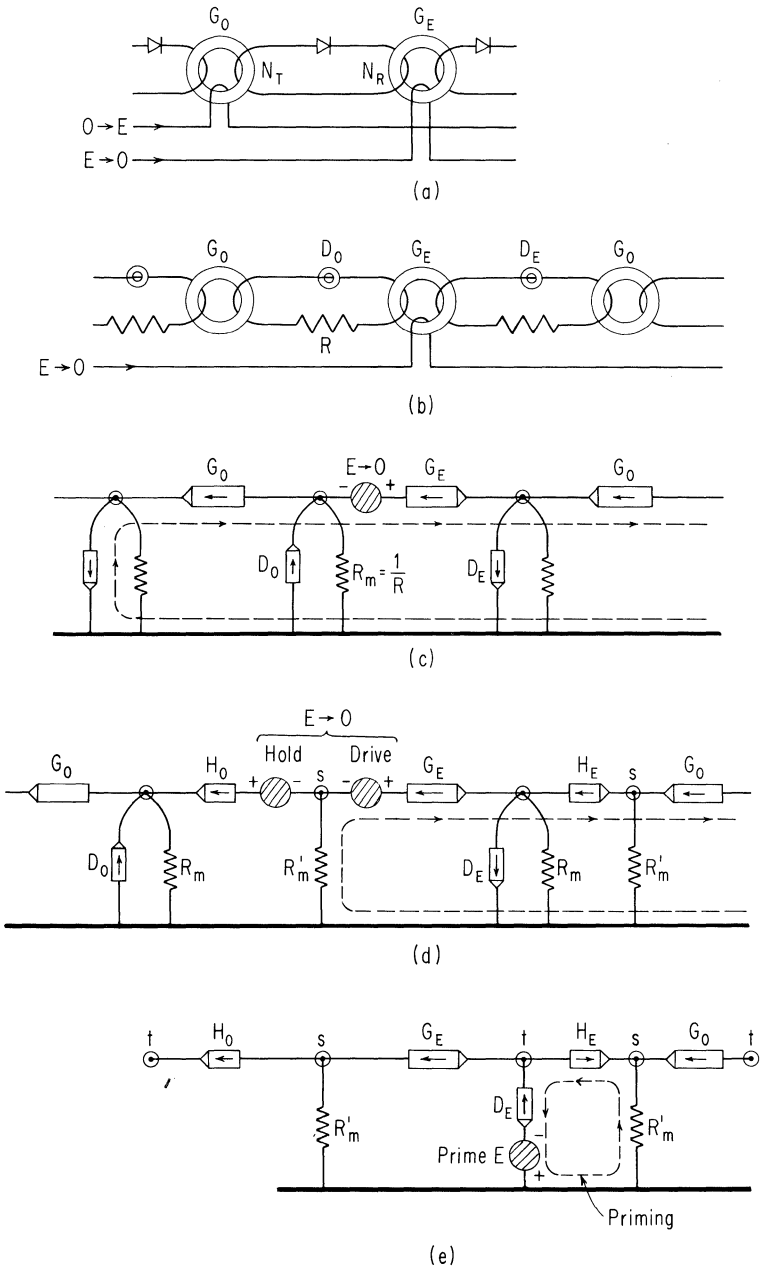


Fig. 6-4. Derivation of the MAD-R circuit from the Russell Type-I scheme.

$O \rightarrow E$ transfer, the flux being dissipated in R . If we eliminate the corresponding branch R_m , however, as in Fig. 6-4(e), then branch D_E can be restored only by simultaneously switching flux in the new element H , with an identical amount of flux being dissipated in the new resistance branch R'_m . Reverse transformation of the network of Fig. 6-4(e) with the $E \rightarrow O$ windings of Fig. 6-4(d) added, yields the circuit of Fig. 6-5(a), which has previously been described by Dick (1963). (Additional windings for priming the O cores and for the $O \rightarrow E$ transfer are of course also required.)

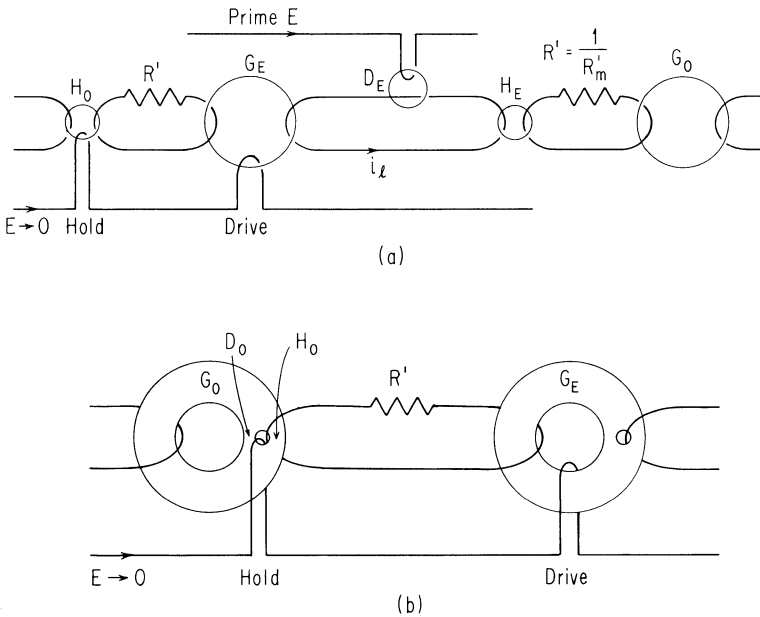


Fig. 6-5. An all-toroid version in (a), and a multileg version in (b), of the MAD-R network of Fig. 6-4(e).

Returning again to Fig. 6-4(e), now assume that the nodes labeled t are all converted to physical nodes, with the G branches doubled in width to satisfy the constraints of flux continuity. Reverse transformation leads to the circuit of Fig. 6-5(b), which is identical to that of Fig. 6-2(b) except for the use of separate input apertures. (Though the use of a minor aperture for input is not actually required for proper MAD-R operation, this practice leads to certain advantages that will be discussed in Sec. 6-4.)

The circuit of Fig. 6-5(a) is the all-toroid version of the MAD-R circuit using major-aperture input. Although this circuit is functionally equivalent to the multileg version of Fig. 6-5(b), there is

significant operational advantage, relative to the priming operation, in favor of realization with multileg cores. This results from the fact that there will always be some finite resistance R in the loop linking Cores D and H in Fig. 6-5(a), and Core H will exhibit some finite amount of switching in response to any mmf larger than its own individual threshold. To minimize the amount of this switching in the *zero* state, we could consider the following measures (though, all in all, the multileg circuit provides a much greater combination of flexibility and performance than the all-toroid version of the same scheme):

1. Bias Core H only to its own threshold or less. (Practically speaking, this may mean no bias at all since H is such a small core.) This would result in a very significant reduction in priming tolerances and speed, however, since Core H would now be driven only from the loop current resulting from the switching of Core D , and there would be a significant $\Delta\phi$ loss in any coupling resistance R . This would place a lower limit on the rate of priming. These problems can be alleviated somewhat by using a lower-threshold material for Core H only, as indicated by Dick (1963).

2. Apply dc priming to both cores (H and D), but operate the circuit near the maximum rate to minimize the time for spurious flux switching in Core H before the latter core is cleared again.

3. Employ pulsed rather than dc priming. Even here, however, there would tend to be some increase of the *zero* $\Delta\phi$ level, because of some flux switching in Core H during the relatively long priming period, as well as a reduced *one* level because of flux loss in R during priming.

6-3 Third Derivation, Based on Series-Shunt Core-Diode Circuit

Here we return to the circuit of Fig. 3-10(a) with a series and a shunt diode in each loop, redrawn in Fig. 6-6(a), followed by its equivalent core-wire circuit in Fig. 6-6(b), and its network representation in Fig. 6-6(c). Let us try to alter the circuit so as to eliminate the need for more than one loop resistance per stage. Comparing the network of Fig. 6-6(c) with that of Fig. 6-4(e), we see that the main difference is the reversed clear-state polarity of the Sh and H branches. Apparently then we can eliminate the need for one resistance, namely R_m , simply by reversing the polarity of Branch Sh in each stage.

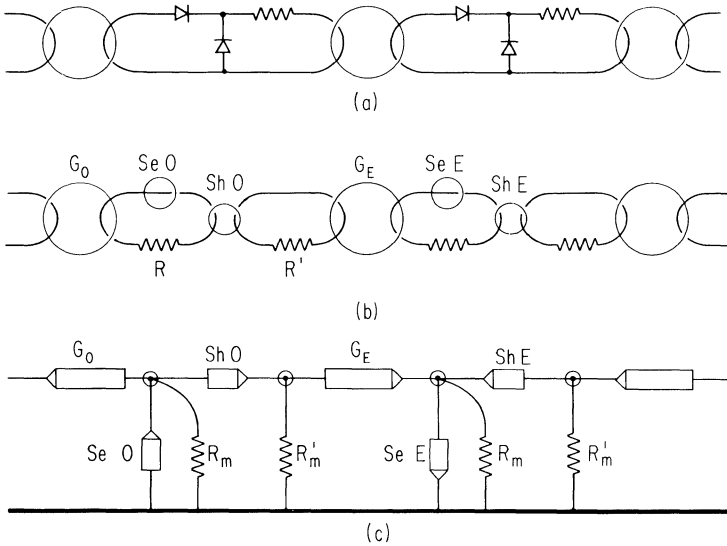


Fig. 6-6. Derivation of MAD-R from the series-and-shunt diode transfer scheme.

Let us consider why the clear state of the Sh elements must be reversed if we are to eliminate one of the loop resistances. The question is whether the circuit can be rearranged so as to eliminate the need for resistance R . If so, when the series element Se is restored by priming, a counterbalancing voltage drop in the loop must be provided either by the switching of the previous G element or the following Sh element. Since we do not wish to disturb the state of G , after having just read into it, the only alternative is to switch the Sh element simultaneously with the Se element, and it is for this reason that the clear state of the Sh element must therefore be reversed from that shown in Fig. 6-6(c).

Through this route we see that if we try to view the reversed Sh branch as a shunt "diode core" and if we were to try to draw an equivalent core-diode version, the shunt diode would point in the opposite direction from that in the original core-diode circuit of Fig. 6-6(a). This new circuit could not work, obviously, since forward transmission would be short-circuited. Furthermore, pointing in this new direction, the shunt diode would not even prevent back transmission. Thus, the core-diode circuit corresponding directly to the MAD-R circuit is not operable. Proper operation is achieved in the core-wire version only because, viewing S again as a "diode core," it is possible to effectively reverse the polarity of the core operating as a diode (recall property (3) of

Sec. 4-1). By making use of this different capability of a core versus a diode, the MAD-R circuit is actually a significant improvement over the core-wire circuit of Fig. 6-6(b), the most similar scheme that does have a core-diode equivalent.

6-4 Minor-Aperture Input and Output

Input. In the first derivation of the MAD-R scheme, minor-aperture input evolved directly from the use of a separate input aperture in the MAD-N scheme. In the two subsequent derivations, input was applied directly to the major aperture. Clearly, both methods of input are functionally identical, though the use of an input aperture affords some extra design and operational flexibility:

1. Effective clipping can be obtained with minor-aperture input, as will be described in Sec. 6-9.

2. It is possible to prime the input aperture simultaneously with the output aperture so that during subsequent advance (when the transmitter is being cleared) there is no flux switched through the input winding. This has the advantage of decreasing the required drive strength and eliminating the need for holding against back transfer. A disadvantage is a reduction in the upper prime-current limit, because mmf applied around both apertures are additive relative to major-aperture setting. If the input and output apertures are primed separately, however, then the range for each priming current is as before.

3. Several input signals can be applied to a core without first-order cross talk. If the various inputs each linked the main aperture, any flux switched in the core would link each input winding. With separate inputs applied to independent minor apertures, however, such linking is largely avoided.

Nondestructive Transfer. There are also important variations that can be applied at the output. Previously, transmission was accomplished by clearing the transmitter element. However, it is possible to effect transfer nondestructively, i.e., without clearing the transmitter core, by driving only around the output aperture. An appropriate drive arrangement in this case is the figure-eight winding indicated in Fig. 6-7, where it is assumed that after priming both output apertures, we drive one set of receivers during the $(E \rightarrow O)_1$ pulse, a second set during $(E \rightarrow O)_2$, and only

then clear the transmitter. Although this arrangement requires extra drivers, the increased flexibility obtained can be useful, for example, for high "fan out" in certain logic circuits.

AC Readout. We have seen above how nondestructive transfer within the system can be achieved by switching flux only locally around an output aperture of the transmitter. We can also apply an alternating waveform (e.g., a sine wave, typically in the range of 0.1 to 5 megacycles) to a minor aperture, to obtain continuous nondestructive readout from a core. With the drive amplitude adjusted to avoid switching around the major aperture, the output ϕ level is low and primarily elastic in nature for a *zero* output from a cleared core (Fig. 6-8(a)), but is relatively high from local inelastic switching for a *one* output (Fig. 6-8(b)). The output power obtainable from typical cores used in logic circuits is of the order of a tenth of a watt and hence may be used directly to drive incandescent bulbs or to trigger power devices such as relays. (There is some discussion in Sec. 6-9 regarding the shaping of minor apertures in order to obtain a large *one/zero* readout ratio.)

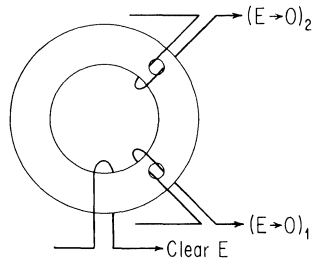


Fig. 6-7. Separating the Advance and Clear functions in the transmitter.

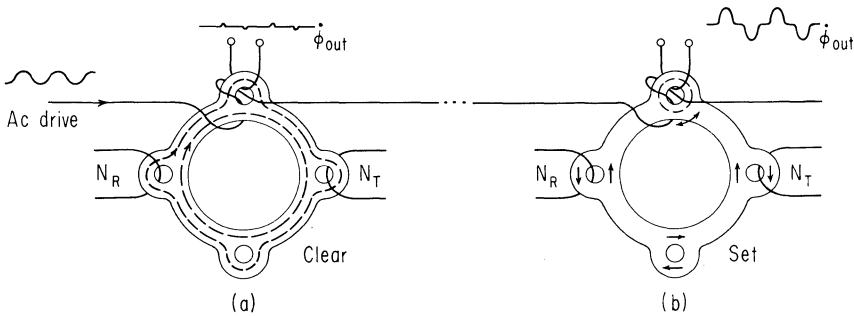


Fig. 6-8. Continuous nondestructive readout from a minor aperture.

Aside from merely indicating the internal binary state, minor-aperture output may be used for actual switching of analog signals (e.g., audio signals), with good fidelity, as described by Crane and English (1963), or for other control purposes. This on-off control capability is an important feature of systems based on unipolar schemes using multileg cores.

6-5 An Approach to Circuit Design

The constant- $\bar{\rho}$ core model of Sec. 1-1 is useful primarily in the demonstration of principles, and for obtaining rough quantitative values for switching time, drive-current levels, average switching voltages, etc. Its use in Sec. 6-1, for example, provided a ratio for limits of switching speed for the MAD-R and MAD-N schemes. In no case, however, are realistic waveforms of circuit variables, e.g., coupling-loop current, obtained analytically by using the constant- $\bar{\rho}$ model. The model is thus inadequate for detailed circuit design, which depends on transient analysis.

In Chap. 12, accurate engineering models for core switching are described, and their use in computer-aided analysis is illustrated. Though these models are quite complex, the obvious way to future analysis and design of core-wire circuits is the further development and application of such models and computer methods. In the remainder of this chapter, we wish to describe a manual method, which, though rather simple, has nevertheless been extremely useful in circuit design.

In the past, it has been found possible to design many core circuits without dependence on precise analysis, though in some cases such design amounted to nothing more than the making of educated guesses followed by laboratory testing, typically followed by several additional cycles of cut-and-try methods. Without appropriate models, it is impossible to do away with the phase of laboratory testing of circuits followed in general by some re-design. In the case of MAD-R circuits, certain methods of measurement and use of test data have been developed that make this process quite systematic, and which have resulted in consistently good design procedures with a surprisingly small amount of iteration. With well-designed cores (see Sec. 6-9), one can readily design MAD-R transfer circuits that have virtually no upper limit on advance current and with very wide prime-current range, at least for room-temperature use.

The primary objective in design of the coupling loops and advance windings is minimization of voltage and current requirements on the driver while maintaining wide drive-current tolerances. This aspect is treated in Sec. 6-6. Procedures for acquiring core data and for testing circuits in order to find and adjust values of design parameters are described in Sec. 6-7. An analysis leading to a design procedure for the priming circuit is discussed in Sec. 6-8. The implications of the circuit design procedure on those features that are desirable in the core design

itself are discussed in Sec. 6-9. (Extension of the design procedure to logic circuits is considered briefly in Sec. 10-6.)

6-6 Design of Coupling Loops and Advance Circuit

The MAD-R circuit of Fig. 6-2 is shown in more detail in Fig. 6-9. Assume that a *one* is initially stored in a primed state in the center transmitter core T . The initial states of this core and of the two adjacent receivers R and R' are designated by the row of arrows representing minor-leg flux directions. Upon application of an advance pulse i_A , loop currents i_f and i_b are induced, and the flux changes indicated by arrows within cores T and R occur. The major reversals are $\Delta\phi_{T1}$ and $\Delta\phi_{T4}$ in the transmitter, and $\Delta\phi_{R1}$ and $\Delta\phi_{Rm}$ (closing through Leg 3) in the receiver. The arrows in Legs 2 and 3 of T and Leg 2 of R represent flux changes that are of second-order magnitude, but sometimes still significant. A half cycle of operation is completed by application of the prime current i_p to each receiver core, switching the flux signal from Leg 3 to Leg 4 ($\Delta\phi_{R4} \approx \Delta\phi_{R3}$) in Core R and inducing a loop current i_r .

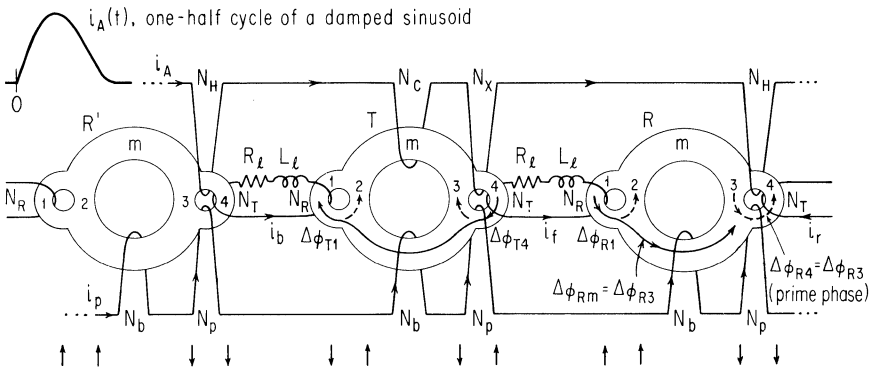


Fig. 6-9. MAD-R circuit shown in detail.

Choice of Design Point. A typical range map for a MAD-R register is shown in Fig. 6-10, where I_A and I_p represent peak advance and prime currents, respectively. The open-ended top indicates that no upper limit on I_A is detected within the region of measurement. (The top may “close in” due to either *zero* buildup or *one* dropout if poor cores or poor circuit designs are

used.) The choice of the nominal operating value of I_A is then merely a matter of how much tolerance one wishes to reserve above the minimum value. The nominal priming current might be chosen for equal plus and minus tolerances.

For aspects of design considered in this section, we choose a tentative value of priming current I_p^{nom} (the exact value not being critical), and then consider operating conditions at the corresponding value of minimum advance current I_A^{min} as indicated in Fig. 6-10. This point serves as an operational design point for the coupling loops and the advance circuit.

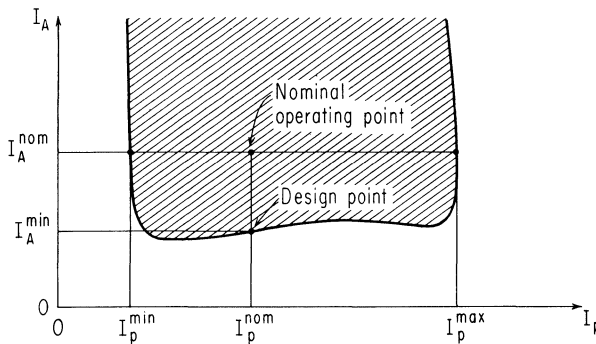


Fig. 6-10. A typical form of the range map for the MAD-R circuit (the shaded area being the allowed operating range).

We assume that advance current i_A has the form of one-half cycle of a damped sinusoid, as indicated in Fig. 6-11(a), with rise and fall times T_r and T_f . This pulse shape is easily obtained by discharging a capacitor through an L - R drive line linking the MAD-R circuit (see Fig. 6-3). A circuit designed in this fashion will also operate well when driven by pulses of other shapes, e.g., triangular, provided certain general characteristics are retained; in particular, similar pulse width and appropriate limits on rates of rise and fall. Baer and Heckler (1962) describe other practical drivers for core-wire circuits based on adaptation of Melville pulse-compression circuits, which also use nonlinear magnetic cores.

Coupling-Loop Design. The coupling-loop design problem, in greatest generality, involves the choice of coupling loop turns N_T and N_R and coupling-loop impedance in terms of wire resistance and inductance R_ℓ and L_ℓ so as to satisfy the necessary flux gain requirements during flux transfer. The basic relation can be derived by summing the emf and voltage drops in the forward

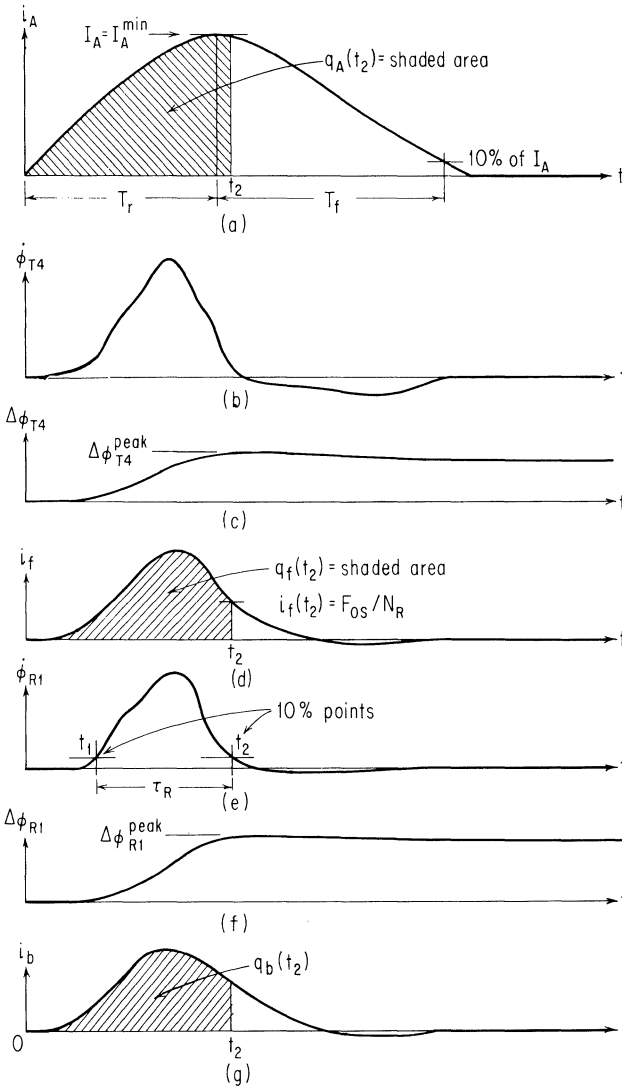


Fig. 6-11. Typical waveforms for $\dot{\phi}$ and $\Delta\phi$, for both transmitter and receiver, and for forward and backward loop currents, in response to Advance Current Pulse of amplitude I_A^{\min} .

coupling loop of Fig. 6-9 during transfer, namely

$$N_T \dot{\phi}_{T4} - N_R \dot{\phi}_{R1} = R_\ell i_f + L_\ell \frac{di_f}{dt} \tag{6-9}$$

Since $i_f = 0$ initially, integration over time from 0 to t yields

$$N_T \Delta\phi_{T4}(t) - N_R \Delta\phi_{R1}(t) = R_\ell q_f(t) + L_\ell i_f'(t) \tag{6-10}$$

where the $\Delta\phi$'s are the net flux changes and q_f is the charge flow in the loop, that is

$$q_f = \int_0^t i_f dt \quad (6-11)$$

Typical waveforms of $\dot{\phi}$ and $\Delta\phi$ for both transmitter and receiver, and of forward and back loop currents, for $I_A = I_A^{\min}$, are shown in Fig. 6-11. Note that $\dot{\phi}$ and loop-current waveforms reverse in sign toward the end of the advance pulse. This is primarily because of elastic-flux components. The peak magnitude of i_f in the negative direction is related to the rate of fall of advance current, and for this reason the rate of fall of i_A must be limited to insure against spurious unsetting of flux in the receiver. As seen in Fig. 6-11, the transmitter begins switching almost immediately after time $t = 0$ (when the advance pulse is turned on), but there is a delay in switching of the receiver until the forward loop current builds up to the threshold of the receiver. The switching time τ_R of the receiver is defined as the difference in the times t_1 and t_2 at which $\dot{\phi}_{R1}$ is 10 percent of its peak value. (In some cases, more consistent results are obtained by measuring τ_R on the main-aperture $\dot{\phi}_{Rm}$ waveform because of the absence of elastic flux clipped out by closure through Leg 2.)

We wish to consider Eq. (6-10) at the instant $t = t_2$, when the inelastic flux switching is nominally complete. For $I_A > I_A^{\min}$, the receiver would complete switching before the transmitter. As I_A is decreased, the difference in switching times decreases, until at $I_A = I_A^{\min}$, both cores complete their switching together at $t = t_2$. Thus, as implied by Fig. 6-11, both $\Delta\phi_{T4}$ and $\Delta\phi_{R1}$ reach peak values very slightly after t_2 , and following Eq. (6-10),

$$N_T \Delta\phi_{T4}^{\text{peak}} - N_R \Delta\phi_{R1}^{\text{peak}} \approx R_L q_f(t_2) + L_L i_f(t_2) \quad (6-12)$$

Figure 6-12 illustrates a ϕ - F characteristic for flux switching via the path including Legs 1, m , and 3 of the receiver in Fig. 6-9. The mmf applied to this path is simply $F = N_R i_f$ since we assume that the priming current i_p is zero during the advance pulses. (The equations to be derived can readily be modified for the case of dc priming, once the principles are understood.) The limiting cross-sectional area is usually that of Leg 3; here we assume that $2\phi_r$ in Fig. 6-12 represents the maximum flux-setting capacity of Legs 1 and 3 in series. The dashed line in Fig. 6-12 represents the

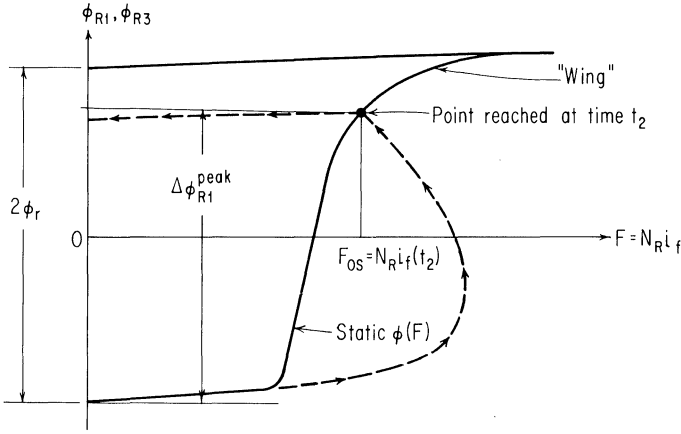


Fig. 6-12. The ϕ - F characteristic for flux switching via the path including Legs 1, m , and 3 of the receiver.

dynamic $\phi(F)$ variation during transfer. The value $N_R i_f(t_2)$, may be viewed as a “stop-switching threshold,” which we call F_{0S} . Because of the complexities of dynamic switching, this point does not necessarily fall exactly on the static $\phi(F)$ curve (as indicated in Fig. 6-12) but may be on one side or the other. The question of how to make measurements for estimating accurately just where this point F_{0S} occurs in an operating circuit is one of the crucial aspects of the design procedure, and this matter is covered in Sec. 6-7.

In most cases, we have simply a single receiver turn, that is, $N_R = 1$, but to retain flexibility for certain cases where it is desirable to scale the values of N_R and N_T , we define a parameter

$$\Pi_R = N_R q_f(t_2) \tag{6-13}$$

which represents the total charge-turns that are required for setting the receiver, up to the time t_2 . We may then rewrite Eq. (6-12) in the form

$$N_T \Delta\phi_{T4} - N_R \Delta\phi_{R1} = \frac{R_\ell \Pi_R + L_\ell F_{0S}}{N_R} \tag{6-14}$$

where, for simplicity, we have suppressed the superscript “peak,” though $\Delta\phi_{T4}$ and $\Delta\phi_{R1}$ are here understood to be peak values.

Equation (6-14) is the primary expression relating to coupling-loop design. It contains core-related parameters $\Delta\phi_{T4}$, $\Delta\phi_{R1}$, Π_R , and F_{0S} , and coupling-loop parameters N_T , N_R , R_ℓ , and L_ℓ . It turns out that Π_R is the only one of the parameters that varies significantly with coupling-loop design. Very roughly, we can write

$$\Pi_R \approx \Pi_0 + kF_0\tau_R \quad (6-15)$$

where $\tau_R = t_2 - t_1$ is the receiver switching time, where Π_0 is the value of charge-turns required for rapid switching (i.e., for $\tau_R \rightarrow 0$), and where k is an empirical constant with a value depending on other core and circuit parameters, but usually in the range of 1.0 to 2.0. (It can be shown that $\Pi_0 \approx lS_w$, where l is path length and S_w is the switching coefficient, as represented in Eq. (12-121), and also that $k \approx 1 + t_1/2\tau_R$. However, these results and Eq. (6-15) are given only to indicate roughly how Π_R varies with τ_R and will not be used further.)

The suggested coupling-loop design procedure starts with a choice of values of N_T and N_R (usually 2 and 1, respectively) and of Π_R and τ_R . Then a coupling loop is chosen with wire cross section and length to provide a combination of values of R_ℓ and L_ℓ that result in satisfaction of Eq. (6-14). Practical considerations of core and circuit dimensions may then dictate that the process be repeated for different values of N_T , N_R , and Π_R (or τ_R). This process presumes that we have already determined the quantities $\Delta\phi_{T4}$, $\Delta\phi_{R1}$, F_{0S} , and Π_R as a function of τ_R for the cores being used. The experimental determination of these quantities is the subject of Sec. 6-7.

In order to aid the choice of wire size and length, we rewrite Eq. (6-14) in the form

$$N_R^2(n\Delta\phi_{T4} - \Delta\phi_{R1}) = R_\ell\Pi_R + L_\ell F_{0S} \quad (6-16)$$

where $n = N_T/N_R$. The choice of a wire loop for satisfying Eq. (6-16) is complicated by the fact that the inductance of a loop of a given shape and wire size is a nonlinear function of the total length of wire. On the helpful side, however, it has been found empirically that loops with $N_T/N_R = 2/1$, wound loosely without controlling the shape, generally have an inductance approximately equal to $(3/4)L_C$, where L_C is the inductance of a circular loop of the same length and wire size. (To reduce the inductance substantially below this value, it is necessary to make the loop into the form of a strip-line or at least to twist the wires very closely.) Considering this fact, and also since the value $L_\ell F_{0S}$ is usually considerably smaller than

$R_\ell \Pi_R$, it has normally been found accurate enough to set

$$L_\ell = 0.75 L_C \quad (6-17)$$

for the purpose of design.

Curves of L_ℓ as well as R_ℓ may therefore be plotted as functions of wire length l_ℓ , for various wire gauges, and graphical procedures may be established for selecting wire length and gauge to yield a pair of values of R_ℓ and L_ℓ to satisfy Eq. (6-16). However, we often know approximate wire length in advance, in which case the use of a linear approximation for L_ℓ is expedient. That is, we set

$$L_\ell = \frac{3}{4} L_C = \frac{3}{4} (-a + bl_\ell) \quad (6-18)$$

where a and b are positive parameters characteristic of a given wire size. (For example, for wire of gauge AWG No. 33, with l_ℓ in the range of 1.5 inch to 3.0 inches, $a = 0.010$ microhenry and $b = 0.0295$ microhenry/inch.) We may also set R_ℓ proportional to l_ℓ , that is

$$R_\ell = \xi l_\ell \quad (6-19)$$

Substitution of the above two equations into Eq. (6-16) results in the following formula for l_ℓ

$$l_\ell = \frac{N_R^2 (n\Delta\phi_{T4} - \Delta\phi_{R1}) + 0.75 a F_{0S}}{\xi \Pi_R + 0.75 b F_{0S}} \quad (6-20)$$

If the calculated length l_ℓ for the assumed wire size turns out to be an impractically short length, there are several possibilities for adjustment. A wire of larger diameter may be considered, if the minor-aperture size allows it. Or the number of coupling-loop turns may be scaled upward (e.g., from 2/1 to 4/2), with an increase by a factor N_R^2 (for example, 4 to 1 for scaling of 2 to 1) in the allowed values of R_ℓ and L_ℓ , as can be seen from Eq. (6-16). Or, finally, it may be necessary to reduce the design value of Π_R (also reducing τ_R), in order to allow a higher-impedance loop, and then repeat the procedure to find a new value of l_ℓ .

Design of Advance Circuit. What we wish to find now are the specifications for the advance windings N_H , N_C , and N_X . In particular,

we desire a design solution in which we have small integral turns ratios so that these windings, which are driven in common, can be realized with a small number of turns.

For convenience in calculating advance-current charge (i.e., the integral of advance current to time t_2), we assume that

$$T_r = t_2 \quad (6-21)$$

although we shall see that we can allow adjustment to certain values of $T_r < t_2$ once a good circuit design has been obtained. Next, it is necessary to consider values of advance-current charge $q_A(t_2)$ and back-loop charge $q_b(t_2)$ (Fig. 6-11) in comparison to the forward-loop charge $q_f(t_2)$. First consider the N_X drive around the output leg of the transmitter, which is not essential, but nevertheless useful, for enhancement of flux gain. This winding is normally chosen to approximately cancel the loop charge-turns acting back on the transmitter (thus minimizing elastic-flux effects), i.e., such that at time t_2

$$N_X q_A \approx N_T q_f = n N_R q_f = n \Pi_R \quad (6-22)$$

In order to guarantee sufficient holding mmf with N_H , it is necessary for the back-loop charge-turns to be canceled out in Core R' in Fig. 6-9, that is

$$N_H q_A \geq N_T q_b \quad (6-23)$$

Let us assume that we can achieve the lower limit indicated by Eq. (6-23), and hence that Core R' makes no contribution of flux-linkage change to the back loop. Then the back-loop equation integrated to time t_2 yields

$$N_R \Delta\phi_{T1} = R_\ell q_b(t_2) + L_\ell i_b(t_2) \quad (6-24)$$

By dividing Eq. (6-14) by Eq. (6-24), with the definitions of Π_R and F_{0S} considered, we obtain

$$\frac{N_T \Delta\phi_{T4} - N_R \Delta\phi_{R1}}{N_R \Delta\phi_{T1}} = \frac{R_\ell q_f(t_2) + L_\ell i_f(t_2)}{R_\ell q_b(t_2) + L_\ell i_b(t_2)} \quad (6-25)$$

For simply finding the value of N_H required, it has been found empirically to be a good enough approximation to assume that the ratio of inductive flux storage to resistive flux loss is the same

in the back loop as in the forward loop at time t_2 , and also that all of the $\Delta\phi$'s on the left side of Eq. (6-25) are equal. Then Eq. (6-25) yields the approximate result

$$q_b(t_2) \approx \frac{q_f(t_2)}{n-1} \quad (6-26)$$

From Eqs. (6-26), (6-22), and the lower limit of Eq. (6-23), we obtain

$$N_H \approx \frac{N_X}{n-1} \quad (6-27)$$

The transmitter and receiver cores switch at about the same rate; hence, we can assume that the net charge-turns driving the transmitter are equal to the charge-turns $\Pi_R = N_R q_f(t_2)$ driving the receiver. That is, recalling that $N_X q_A(t_2)$ cancels $N_T q_f(t_2)$, we can write

$$N_C q_A(t_2) - N_R q_b(t_2) \approx N_R q_f(t_2) \quad (6-28)$$

From Eqs. (6-26), (6-28), and the lower limit of Eq. (6-23),

$$N_C q_A(t_2) \approx \frac{N_T}{n} [q_b(t_2) + q_f(t_2)] \approx N_T q_b(t_2) = N_H q_A(t_2)$$

whence

$$N_C \approx N_H \quad (6-29)$$

In summary, then, from Eqs. (6-27) and (6-29) we find that $N_C \approx N_H \approx N_X/(n-1)$. For the usual case of $n=2$, we see that $N_H = N_X$. A practical effect of this result is that a single line wound through all output apertures and fed in common from the two N_C lines, through the O and E sets of cores, serves the purpose of both the N_X and N_H windings, with roles alternating for the two advance pulses, as shown in Fig. 6-3.

Though Eqs. (6-27) and (6-29) are approximate, Eq. (6-27) has been found to be satisfactory over a wide range of conditions. For low-drive designs (large τ_R), however, it has sometimes been found that a value of N_C equal to N_H , as in Eq. (6-29), does not result in sufficient clearing of transmitters. In such cases, it has been

found possible to increase N_C (typically to $N_C = 4$ if $N_H = N_X = 3$) without causing insufficient holding, and such a value generally obviates any possible problem of insufficient clearing.

In specifying parameters for the advance-pulse shape, a rule of thumb for avoiding unsetting during the fall time is to set

$$T_f \approx 2T_r \quad (6-30)$$

where T_f and T_r are defined as in Fig. 6-11(a). In order to obtain a rough estimate of the peak advance current I_A (while still assuming T_r is to be set equal to t_2), we first recall from Eq. (6-22) that $N_X q_A(t_2) = N_T q_f(t_2)$. Because of the damped-sinusoid nature of the advance pulse

$$q_A(t_2) \approx \frac{2}{3} I_A t_2 \quad (6-31)$$

and from Eq. (6-22) we obtain

$$I_A \approx \frac{3}{2} \frac{N_T}{N_X} \frac{q_f(t_2)}{t_2} \quad (6-32)$$

Though we have assumed that $T_r = t_2$ until now, it has been found empirically that we may, for actual operation, scale down T_r and T_f until $T_r \approx (2/3)t_2$, without affecting transfer circuit operation significantly, but economizing on power from the advance driver approximately in proportion to the scaling. (In actual designs, t_2 is equal to about $(3/2)\tau_R$. An actual value can be measured when the first trial circuit is built, at which time the width of the advance pulse may be readjusted.)

Redesign. Once a first design has been achieved, based on estimated values of $\Delta\phi_{T4}$, $\Delta\phi_{R1}$, τ_R , and Π_R , the usual practice is to build a short closed-loop register as a test circuit. With good cores, such a circuit is always at least operable. If the circuit does not operate within specifications, however, then measurements are taken on the actual test circuit for redesign.

It is easy to obtain actual measurements of τ_R , $\Delta\phi_{T4}$, and $\Delta\phi_{R1}$ at the bottom of the range map (the design point), as will be described in Sec. 6-7. The parameter F_{0S} can be assumed unvaried from the initial measurement. One may then use Eq. (6-14) for determining an empirical value of Π_R on the basis of the circuit measurements, and this result provides an improved data point on

the empirical curve of Π_R versus τ_R , which very roughly has the form of Eq. (6-15). The design procedure may then be repeated with revised values of $\Delta\phi_{T4}$, $\Delta\phi_{R1}$, and Π_R . For simple transfer circuits, it is seldom necessary to do more than one iteration, if even that.

So far the design procedure has been based on *one* transfer. If *zero* buildup should turn out to be a problem, any specific amount of clipping may be obtained by building it into the input aperture (Sec. 6-9) or by incorporating flux-source clipping as used for logic circuits (Sec. 10-5).

Placement of Drive Windings. There are two extreme ways for making multiple-turn drive windings. By the "straight-through" method, a single turn links all cores before the next turn is started. By the "lumped-winding" method, each winding is completed in a tight coil before the next winding along the drive line is started. The straight-through method is better for quick, economical wiring, but the lumped-wiring method results in shorter drive lines of lower intrinsic impedance. In either case, return paths for lines should be bundled as closely as possible to the threading lines, because large return loops can result in air fields large enough to affect operation adversely.

6-7 Measurement of Design Parameters

If the core or circuit parameters are unknown to begin with, it is desirable to make initial measurements on a test core before attempting to build any transfer circuits. On the other hand, if these parameters are known approximately, a test circuit (typically a four-bit closed-loop register) can be designed and built immediately, and then measurements can be made under operation for adjustment of the design. One example of the latter case is the use of a new batch of cores of specified shape and material content, but suffering from typical batch-to-batch variations. Another example is a new design with a completely known core but for lowered advance-current requirements. In any case, for simplicity in measuring test parameters, we assume a coupling-loop turns ratio $N_T/N_R = 2$, which generally yields good enough initial parameter measurements even if some other ratio is eventually to be used.

Core Test Circuit for Initial Measurements. For the first measurements on a relatively unknown core, the test circuit of

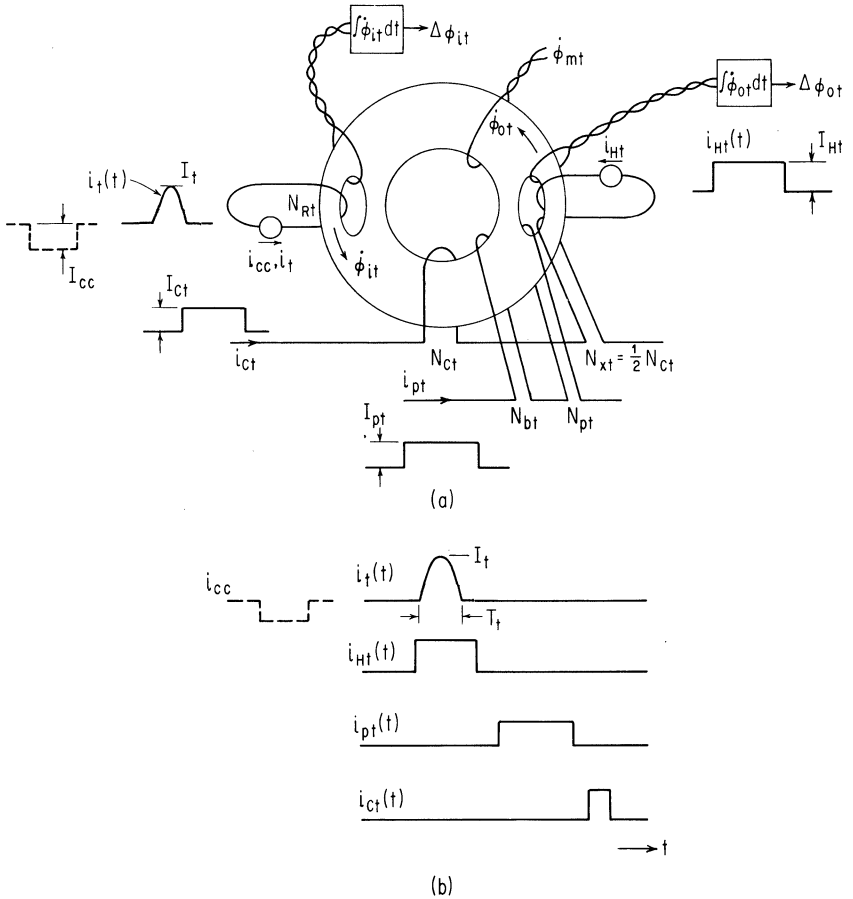


Fig. 6-13. Test circuit for obtaining design parameters.

Fig. 6-13(a) may be used. Throughout this section, we add the subscript t to designate this test circuit and results obtained from it. The prime-pulse amplitude is generally set roughly in the middle of its range, which can be estimated by taking the average between a value for switching fully around the minor aperture and a value for just reaching the major-aperture threshold. The turns N_{pt} and N_{bt} are generally set at 3 and 1, respectively. As an approximation to the coupling-loop current shape, a half-sinusoid test current i_t is used. (For the moment, ignore the precursor current i_{cc} indicated with the dashed line.) Rectangular pulses of controllable amplitude may be used for the other currents i_{ct} and

i_{Ht} required for the test. The timing sequence for applying the four required current pulses is indicated in Fig. 6-13(b). The test current i_t , of peak value I_t and width T_t , and the waveforms of the resulting $\dot{\phi}_{it}$ and $\Delta\phi_{it}$ are shown in Fig. 6-14. At the instant t_{2t} , when $\dot{\phi}_{it}$ drops to 10 percent of its peak value, we wish to make a measurement to obtain approximate values of Π_R (as a function of τ_R) as well as values of F_{0S} and $\Delta\phi_{R1}$.

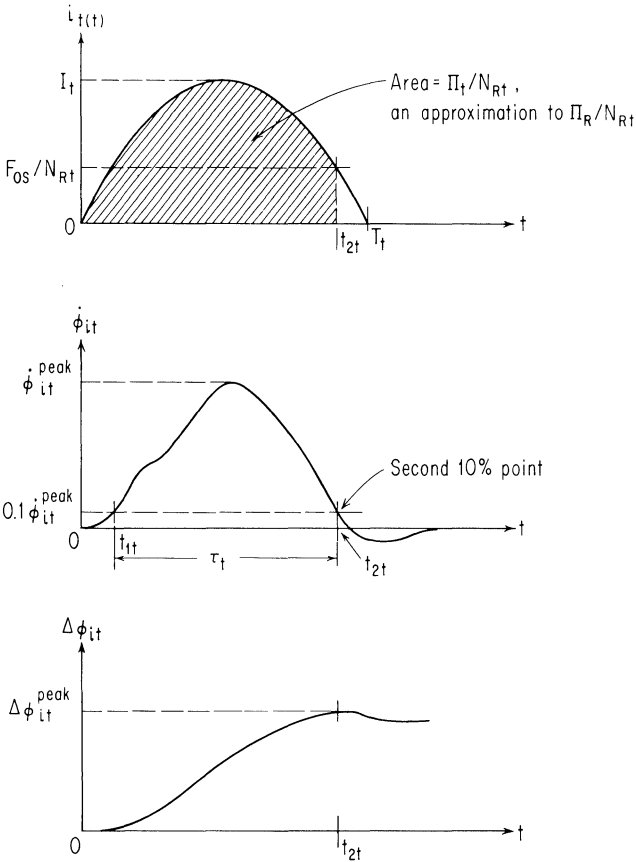


Fig. 6-14. Test current waveform i_t and resulting input waveforms $\dot{\phi}_{it}$ and $\Delta\phi_{it}$.

Experience has shown that this objective can be achieved quite satisfactorily with a procedure consisting of the following three main steps:

1. Find the amplitude I_t of test current corresponding to the design point of Fig. 6-10.

2. Simulate the relative drive mmf acting on the transfer circuit at time t_{2t} .
3. Make final adjustments and actual measurements.

These steps will be detailed below, but note first that the only remaining parameter needed for the design equations (6-15) and (6-16), namely $\Delta\phi_{T4}$, may be approximated by measurement of the output flux $\Delta\phi_{ot}$ (Fig. 6-13(a)) during the clear pulse i_{Ct} , again based on appropriate adjustment of drive mmf values.

Simulation of Design-Point Operation. The first of the three steps outlined above is the most interesting part of the test, namely, finding the critical amplitude for the test pulse relating to the design point of Fig. 6-10. The sequence of steps indicated below is suggested as a useful procedure, though the designer, with experience, may develop his own specific procedure.

Consider Fig. 6-15, where half-sine input test pulses of various amplitudes are shown together with the corresponding $\dot{\phi}_{it}$ waveforms. Assuming that a design is desired for a given transfer time τ , for example, $\tau = 1.0$ microsecond, then we proceed as follows: First, select a value of test pulse width T_t somewhat greater than τ , say 1.5τ . Second, with the test sequence of Fig. 6-13(b) and with fixed-amplitude values of i_{Ht} and i_{Ct} well above threshold, increase the test-current amplitude I_t to just above threshold, say $I_{t(1)}$ in Fig. 6-15. Third, consider the resulting $\dot{\phi}_{it(1)}$ waveform and note $t_{2t(1)}$ when $\dot{\phi}_{it(1)}$ falls to 10 percent of its peak value. In this low range, the amount of switching is not flux-limited, so that for a small increase in current, say from amplitude $I_{t(1)}$ to $I_{t(2)}$, a greater amount of flux is switched and the second 10-percent point on $\dot{\phi}_{it}$ moves to the right (from $t_{2t(1)}$ to $t_{2t(2)}$). During further increase of current amplitude, a transition is passed having the following characteristics:

1. The time of the second 10-percent point on $\dot{\phi}_{it}$ reaches a maximum value t_{2t}^* , for some specific amplitude I_t^* with corresponding $\dot{\phi}_{it}$ waveform $\dot{\phi}_{it}^*$, and then decreases steadily for higher amplitudes, e.g., to $t_{2t(3)}$ for amplitude $I_{t(3)}$ in Fig. 6-15.

2. At about this same point, i.e., where t_{2t} is maximum, the shape of the decaying portion of the $\dot{\phi}_{it}$ waveform undergoes a striking change, becoming rapidly steeper. This change in shape is related to the fact that inelastic switching terminates at about the base of the "wing" on the ϕ - F loop of Fig. 6-12, which is just about the point of operation desired for the design simulation.

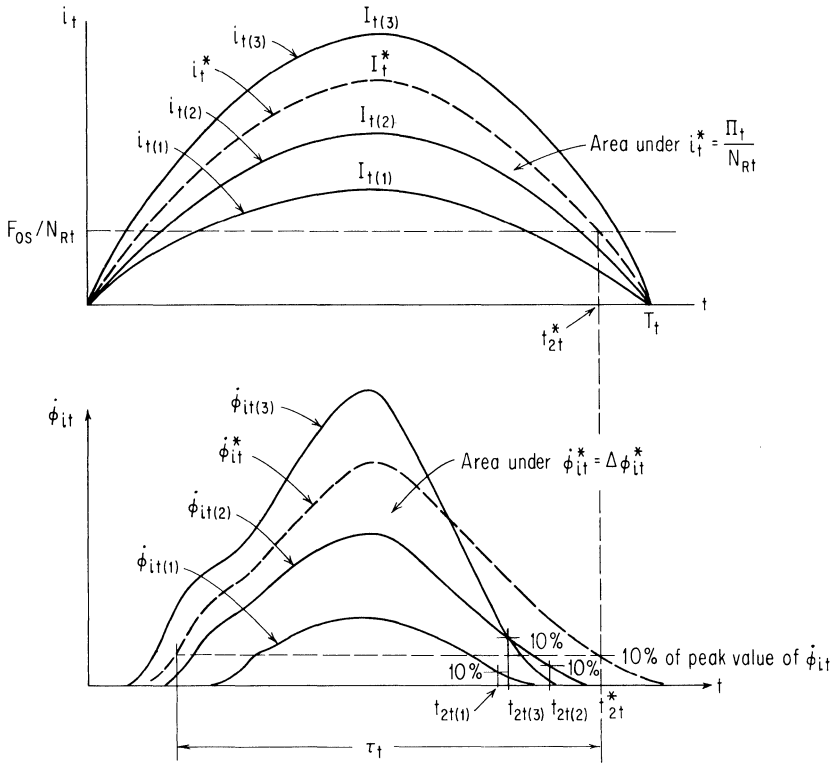


Fig. 6-15. $\dot{\phi}$ for different amplitudes of half-sinusoid test current.

3. For amplitudes of current greater than I_t^* , switching may be considered to be flux-limited; this observation fits with the fact that the width of $\dot{\phi}_{it}$ then decreases as the peak of $\dot{\phi}_{it}$ increases, whereas the area $\Delta\phi_{it}$ hardly increases further.

For test purposes, the amplitude of i_t is set to the value I_t^* found where this transition occurs.

Simulation of Drive MMF. In principle, the drive levels through Winding N_{Ht} at setting time, and through Windings N_{Ct} and N_{Xt} at clearing time should simulate transfer-circuit drive levels, correcting for the expected back mmf values in the coupling loops, which are not present in the test circuit of Fig. 6-13(a). From experience, it has generally been found sufficiently realistic to set the holding mmf about equal to the peak test mmf, that is,

$$N_{Ht}I_{Ht} \approx N_{Rt}I_t \tag{6-33}$$

This relation need be satisfied only approximately during any test sequence—say within 10 percent, since holding is a relatively non-critical function.

On a similar basis, at the time of clearing the test core with current i_{Ct} , minor-aperture drive conditions for the transfer circuit, including loading by both input and output loops, are adequately simulated by setting $N_{Ct} = 2N_{Xt}$, as indicated in Fig. 6-13(a), and adjusting i_{Ct} so as to have output-aperture mmf $N_{Xt}I_{Ct}$ equal to the test mmf $N_{Rt}I_t$ used for setting, that is

$$N_{Xt}I_{Ct} = N_{Rt}I_t \quad (6-34)$$

Greater care is required to satisfy Eq. (6-34) than Eq. (6-33), since the measurement of $\Delta\phi_{ot}$ is fairly sensitive to minor-aperture drive. It should be emphasized that the main point is one of *consistency* in how some rather arbitrary rules are adhered to, since the simulation of actual circuit conditions is approximate in any event.

Finally, in order to assure that any input-aperture flux-clipping capacity (a matter of core design discussed in Sec. 6-9) is in a "prepared" or "cleared" state, it is desirable to apply to the input aperture, prior to the test current i_t , the negative current pulse i_{cc} indicated in Fig. 6-13. The mmf value should be great enough to just switch any uncleared flux in the input leg around the input aperture. The pulse need not be rectangular and of course could be applied on a separate additional winding instead of on N_{Rt} .

Final Adjustment and Actual Measurements. After the first setting of the amplitude of i_t , as described earlier, the amplitudes of i_{Ht} and i_{Ct} are adjusted to satisfy Eqs. (6-33) and (6-34). In general, I_t will then no longer be set at the critical transition point, which will have shifted slightly, and the adjustment procedure for I_t , followed by that for I_{Ht} and I_{Ct} , may have to be iterated one or more times, but convergence to definite final values is rapid.

When the two aspects of mmf simulation have been simultaneously achieved, then a set of measurements may be made. The waveforms $\dot{\phi}_{it}$ and $\dot{\phi}_{ot}$ are integrated as indicated in Fig. 6-13(a) and we assign $\Delta\phi_R = \Delta\phi_{it}^{\text{peak}}$ and $\Delta\phi_T = \Delta\phi_{ot}^{\text{peak}}$. Referring to Fig. 6-14, the switching time τ_t is measured between 10 percent-points on $\dot{\phi}_{it}$ (or $\dot{\phi}_{mt}$ if preferred), and F_{0S} is measured as the value of $N_{Rt}i_t$ at time t_{2t} . The waveform i_t could also be integrated to time t_{2t} to obtain a value of Π_t/N_{Rt} . However, because

of the half-sine shape, the area may readily be calculated as a function of I_t , T_t , and either t_{2t} or F_{0S} .

In general, the first pair of values of Π_t and τ_t will not match the original design specification, whether the latter is in terms of Π_R or τ_R . However, the procedure may be repeated with a second trial value of T_t , resulting in a second point on the curve of Π_t versus τ_t (generally without much change in the $\Delta\phi$ and F_{0S} measurements). With two or more such measurements, we may interpolate or extrapolate to the set of parameters matching a specified switching time (or some other original specification).

Transfer-Circuit Measurement for Redesign. From the set of parameters obtained as described above, a design for coupling loops and advance windings may be obtained by the procedures of Sec. 6-6. Though design of priming circuitry will be covered in Sec. 6-8, we may build a test circuit using priming pulses and windings as specified for the test core of Fig. 6-13(a). A range map such as in Fig. 6-10 may then be plotted. (If no range of operation exists, it usually means that either the cores are very poor, e.g., they have a low degree of squareness, or that the original specification for switching time is unreasonably low or high.) The left-hand and lower boundaries are governed by *one* dropout in a single-*one* pattern of information, due to insufficient Prime current or Advance current, respectively. The right-hand boundary is governed by either *zero* buildup or *one* dropout (or preferably both simultaneously for the "matched" case discussed in Sec. 6-8) due to excessive priming current. The upper boundary (if detectable) is usually due to *zero* buildup from inelastic receiver switching induced by excessive elastic switching of the transmitter, but may also be due to *one* dropout caused by various "unsettling" effects, such as can occur from too rapid a fall of advance current.

The next step is to set a nominal value I_p^{nom} —preferably the same value used for the core tests—and then decrease I_A to the lower range boundary. Revised values of $\Delta\phi_T$, $\Delta\phi_R$ and τ_R are then measured, using sense windings on the transmitter and the receiver associated with one of the coupling loops. It is extremely difficult to measure loop current (and hence F_{0S} and Π_R), however, without affecting loop impedance. Fortunately, F_{0S} can generally be assumed unchanged from the core measurement, and hence a revised experimental value of Π_R may be calculated from Eq. (6-14).

Based on the new pair of values obtained for Π_R and τ_R , the curve of Π_t versus τ_t obtained from core measurements may be

scaled to match the new point. A new design for a different value of τ_R may then be tried in the test circuit, a further adjustment made in the $\Pi_t - \tau_t$ design curve, and so on, until design data as precise and complete as desired is obtained. If just a single good design is required, this can usually be achieved on the first or second trial after a little experience with the procedures has been obtained.

6-8 Design of Priming Circuitry

As indicated in Sec. 6-7, it is easy to design for wide priming-current range, at least for a single, constant temperature. Following Nitzan (1965), we now wish to show how priming range may in fact be greatly enhanced and operation thereby achieved even over a large range of temperature, though at the cost of a reduced speed of operation.

In Fig. 6-16, the range map of Fig. 6-10 is shown, for room temperature and for specified minimum and maximum temperatures. Due to the effect of temperature T on the threshold field of the core material, both I_p^{\min} and I_p^{\max} decrease as T increases, and vice versa. For operation within the temperature range $T_{\min} \leq T \leq T_{\max}$, the priming range is therefore reduced to a band narrower than at any single temperature.

Increased priming range at any given temperature can be achieved by use of a priming pulse with a slowly rising front, e.g., a ramp or a half-sine pulse, rather than a rectangular pulse, in conjunction with control of the ratio N_p/N_b . In this way, the overlap range between given temperature extremes can be greatly increased. In fact, an overlap range can be created with a ramp pulse for temperature extremes (e.g., over the range from -50°C to 100°C) where typically no overlap range even exists for rectangular pulse priming. An alternative (and more costly) way to obtain a wide temperature range is to design a compensated prime-driver circuit that automatically supplies decreasing current amplitude with increasing temperature, and vice versa.

We will first analyze the case of a rectangular pulse more accurately than previously, as a basis for comparison, and then show how to obtain improved designs with a slowly rising pulse—specifically a ramp function. We will present quantitative results that are useful for actual design for ramp-pulse priming. Similar results can be obtained with other slowly rising pulse shapes, such as a half-sine pulse, as described by Nitzan (1965).

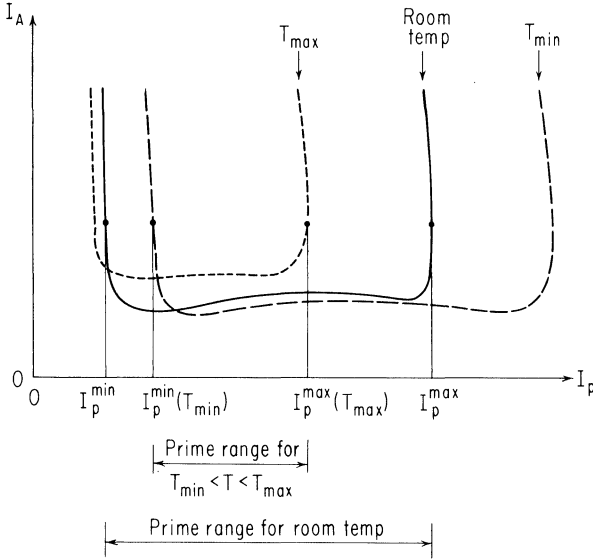


Fig. 6-16. Range maps at extreme temperatures T_{min} and T_{max} .

Rectangular Priming Current. Consider a rectangular priming current pulse of amplitude I_p and duration T_p . We wish to calculate I_p^{min} and

$$I_p^{max} = \min(I_{p\downarrow}^{max}, I_{p\uparrow}^{max}) \tag{6-35}$$

where $I_{p\downarrow}^{max}$ and $I_{p\uparrow}^{max}$ are the maximum values of I_p which cause a *one* dropout or a *zero* buildup, respectively. For flux changes received by Leg 3 and then primed into Leg 4 (Fig. 6-9), a full *one* corresponds to $\Delta\phi_3 = \Delta\phi_4 = 2\phi_r$, where ϕ_r is the maximum residual flux of a minor leg. Suppose that $\Delta\phi_3$ and $\Delta\phi_4$ are gradually reduced below $2\phi_r$ by varying I_p or I_A or both. Initially, the *one* remains stable, but when $\Delta\phi_3$ reaches a certain fraction γ of $2\phi_r$, for example, $\gamma \simeq 0.9$, the *one* drops to a *zero*, because flux gain falls below unity. The corresponding $\Delta\phi$ primed into Leg 4 is $\Delta\phi_4 = \eta\Delta\phi_3 = \eta\gamma 2\phi_r$, where $\eta < 1$ as a result of insufficient priming. Calculation of γ and η is complex, especially because of second-order effects of I_A on γ . A value of $\eta\gamma \simeq 0.8$ has been observed to be a good approximation in many cases of *one* dropout.

Interestingly enough, *one* dropout may be caused by I_p being either too small or too large. For $I_p < I_p^{min}$, $N_p I_p$ is too small to switch enough flux through Legs 3 and 4, and priming may be said to be mmf-limited. For $I_p > I_{p\downarrow}^{max}$, $N_b I_p$ causes flux to be unset

around the major aperture, so that the amount of primed flux is insufficient to sustain *one* transfer, and the priming may be said to be flux-limited.

To derive a formula for I_p^{\min} , consider Fig. 6-17. The static $\phi(F)$ curve around the minor aperture, i.e., for Legs 3 and 4 in series, is plotted as ϕ_4 versus F . The unsaturated portion of ϕ_4 versus F is approximated by a straight line that intersects the horizontal lines $\phi = -\phi_r$ and $\phi = +\phi_r$ at two points whose F values are F_1 and F_2 , respectively. Thus, in this region

$$F = \alpha + \beta\phi_4 \quad (6-36)$$

where

$$\alpha = \frac{F_2 + F_1}{2} \quad (6-37)$$

and

$$\beta = \frac{F_2 - F_1}{2\phi_r} \quad (6-38)$$

The value of ϕ_4 for which a *one* drops to *zero* is $(-\phi_r + \eta\gamma 2\phi_r)$, and the corresponding F value is denoted by F_{\downarrow} . Substitution of $\phi_4 = -\phi_r + \eta\gamma 2\phi_r$ into Eq. (6-36) gives

$$F_{\downarrow} = F_1 + \eta\gamma(F_2 - F_1) \quad (6-39)$$

For a very long priming pulse, $N_p I_p^{\min} = F_{\downarrow}$; hence

$$I_p^{\min} = \frac{1}{N_p} [F_1 + \eta\gamma(F_2 - F_1)] \quad (6-40)$$

For a rectangular pulse of duration T_p , it can be shown that Eq. (6-40) is modified to the form

$$I_p^{\min} = \frac{1}{N_p} \left[F_1 + \frac{\eta\gamma(F_2 - F_1)}{1 - e^{-(T_p/\tau)}} \right] \quad (6-41)$$

where

$$\tau = \frac{2\phi_r}{F_2 - F_1} \cdot \frac{N_T^2}{R_\ell}$$

Note that as $T_p \rightarrow \infty$, Eq. (6-41) reduces to Eq. (6-40).

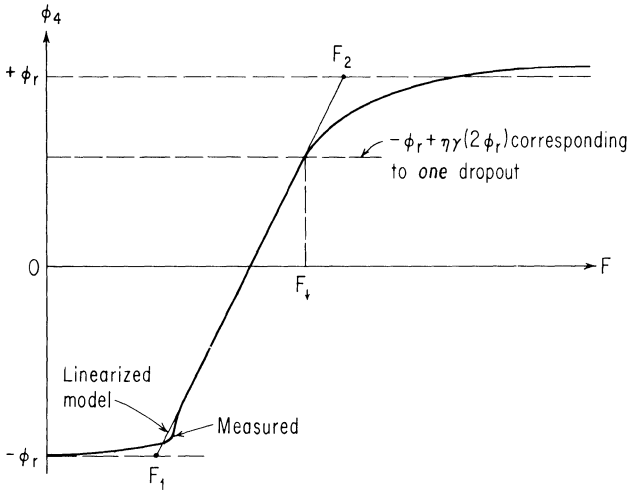


Fig. 6-17. Static $\phi(F)$ curve around the minor aperture.

Consider next the case of a *one* dropout due to excessive flux unsetting around the major aperture via Legs 3 and 1. Since the main leg is initially in a partially set state, the static $\phi(F)$ curve for unsetting around the major aperture is narrower and rounder than if the core were initially in a clear state. Let us denote by F_M^* the *soft threshold* corresponding to the critical amount of flux unsetting around the main leg. If $N_b I_p \geq F_M^*$, a *one* drops to *zero*; hence

$$I_{p\downarrow}^{\max} = \frac{F_M^*}{N_b} \tag{6-42}$$

Finally, we examine the condition for a spurious *zero* buildup. It can be seen from Fig. 6-9 that the mmf $(N_p - N_b)I_p$ acts around the major aperture along a closed path including Legs 4 and 2. Let the dc threshold of this path be denoted by F_M . Although $\Delta\phi_m$ may increase up to a certain fraction (e.g., up to about 20 percent) of $2\phi_r$ before a *zero* builds up, to be conservative we assume that, due to the sharpness of the static $\phi(F)$ curve near its threshold, a *zero* buildup occurs if $(N_p - N_b)I_p \geq F_M$. Hence

$$I_{p\uparrow}^{\max} = \frac{F_M}{N_p - N_b} \tag{6-43}$$

The function of an N_b -turn priming winding on the main leg is thus clear—namely, to increase $I_{p\uparrow}^{\max}$.

Following Eq. (6-35), we set $I_p^{\max} = I_{p\downarrow}^{\max} = I_{p\uparrow}^{\max}$ for an optimum, *matched* case. Thus, when the circuit is properly designed, Eqs. (6-42) and (6-43) give

$$\frac{N_p}{N_b} = 1 + \frac{F_M}{F_M^*} \quad (6-44)$$

For typical ferrites that have been used for MAD-R circuits, $F_M \approx 2F_M^*$; hence, if $N_b = 1$, then $N_p = 3N_b = 3$, which are the values specified in Fig. 6-3. Note that "rectangular" priming is implied when dc priming is used, since the priming current becomes fully effective immediately after the advance pulse terminates.

For the matched-case condition, and assuming a very long priming pulse, then from Eqs. (6-40), (6-42), and (6-44), the maximum value of I_p^{\max}/I_p^{\min} is found to be

$$\mathcal{R}_{\max} = \frac{F_M^* + F_M}{F_1 + \eta\gamma(F_2 - F_1)} \quad (6-45)$$

Ramp Priming Current. The maximum value of range ratio \mathcal{R} that can be obtained with a very long rectangular priming pulse is expressed in Eq. (6-45). We shall show now that much higher values of \mathcal{R} can be achieved if we let the prime drive current $i_p(t)$ rise slowly so that in the *one* case, ϕ_3 reaches $-\phi_r$ just before $N_b i_p(t)$ reaches F_M^* . Beyond this latter point, $i_p(t)$ continues to rise toward its peak without causing any switching around the major aperture, provided the peak value does not finally exceed the *zero-buildup upper-limit* $F_M/(N_p - N_b)$. In effect, what we will find is that the longer the time we allow for the ramp, the closer the optimal N_p/N_b ratio approaches unity (compared with $(N_p/N_b)_{\text{opt}} = 3$ noted above for the rectangular-pulse case); in the limit, $N_p = N_b$, and we can see from Eq. (6-43) that $I_{p\uparrow}^{\max} \rightarrow \infty$.

We assume that the ramp priming current has variable slope k and constant duration T_p , that is, $i_p = kt$ during $0 \leq t \leq T_p$, and $i_p = 0$ for $t > T_p$. The slope $k = I_p/T_p$ varies between k_{\min} and k_{\max} as the peak value I_p varies between I_p^{\min} and I_p^{\max} . Flux switching around Legs 3 and 4 starts at $t = T_0 = F_1/(N_p k)$. The resulting voltage $N_T \dot{\phi}_4$ induces a current $i_f = N_T \dot{\phi}_4/R_\ell$ in the forward loop. Since flux switching is relatively slow during priming, we assume that the net mmf follows the static curve, Fig. 6-17; furthermore, since $\Delta\phi_4$ does not exceed $\eta\gamma 2\phi_r$ in the conditions under investigation, we can equate this net mmf to the linear approximation previously given in Eq. (6-36), that is, $F = \alpha + \beta\phi_4$. Combining of these relations

results in a first-order linear differential equation whose solution is

$$\phi_4(t) = -\phi_r + \frac{N_p k}{\beta} \left\{ t - T_0 - \tau \left[1 - e^{-(t-T_0)/\tau} \right] \right\} \quad (6-46)$$

where

$$\tau = \frac{N_T^2}{\beta R_\ell} \quad (6-47)$$

is the time constant with which $\dot{\phi}_4$ rises.

Let T_S denote the time when prime switching is completed. As k is increased (from some value corresponding to a stable *one*), kT_S increases despite the decrease in T_S . For the maximum value of k , namely, k_{\max} , i_p reaches $I_{p\downarrow}^{\max} = F_M^*/N_b$ at $t = T_S$, that is, when $\phi_4(t) = -\phi_r + \eta\gamma 2\phi_r$, as we see in Fig. 6-18. (If $k > k_{\max}$, a *one* drops to a *zero*.) To find k_{\max} , we substitute the relations $t = T_S = F_M^*/(N_b k_{\max})$, $T_0 = F_1/(N_p k_{\max})$, and $\phi_4(t) = -\phi_r + \eta\gamma 2\phi_r$ into Eq. (6-46) and obtain

$$k_{\max} \left\{ 1 - \exp \frac{-\left[\left(F_M^*/N_b \right) - \left(F_1/N_p \right) \right]}{k_{\max} \tau} \right\} = \frac{1}{\tau} \left(\frac{F_M^*}{N_b} - \frac{F_\downarrow}{N_p} \right) \quad (6-48)$$

which, for given core and circuit parameters, is a transcendental equation with one and only one solution for k_{\max} .

For a value of $k = k_{\max}$, once priming is completed, $i_p(t)$ may continue to rise beyond $t = T_S$ with no effect on flux unsetting, because Leg 3 is already in negative saturation. But, in order to prevent *zero* buildup, the rise of $i_p(t)$ must terminate before reaching $I_{p\uparrow}^{\max}$, that is at $t = T_{pm}$, as shown in Fig. 6-18, where

$$T_{pm} = \frac{F_M}{k_{\max}(N_p - N_b)} \quad (6-49)$$

The resulting $i_p(t)$ waveform in this case, that is, $k = k_{\max}$ and $t = T_{pm}$, is considered to be a matched case because its slope and amplitude have upper-limit values determined by both the *one*-dropout and the *zero*-buildup criteria. (Note that the matched case cannot be realized if $I_{p\downarrow}^{\max} > I_{p\uparrow}^{\max}$.) The duration T_{pm} is the border

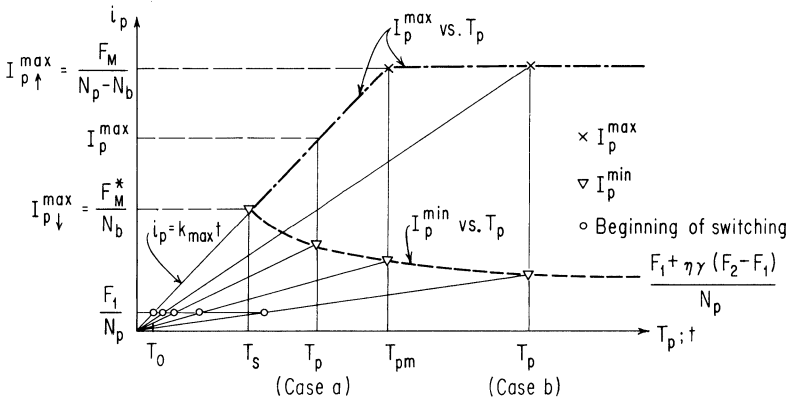


Fig. 6-18. Plot of I_p^{\max} and I_p^{\min} as a function of ramp duration T_p ; $T_p \leq T_{pm}$ in case (a), and $T_p \geq T_{pm}$ in case (b). If $k \geq k_{\max}$ or $I_p \leq I_p^{\min}$, a one drops to zero; if $I_p \geq I_{p\uparrow}^{\max}$, a zero builds up to a one.

between two cases of T_p . If

$$T_S \leq T_p \leq T_{pm} \quad (\text{Case a})$$

then

$$I_p^{\max} = k_{\max} T_p$$

and, if

$$T_p \geq T_{pm} \quad (\text{Case b})$$

then

$$I_p^{\max} = I_{p\uparrow}^{\max} = \frac{F_M}{N_p - N_b}$$

The lower limit of k , namely, k_{\min} , is calculated for both Case a and Case b by substituting the relations $t = T_p$, $T_0 = F_1/(N_p k_{\min})$, and $\phi_4(t) = -\phi_r + \eta\gamma 2\phi_r$ into Eq. (6-46). We can thus derive the relation

$$k_{\min} \left\{ T_p - \tau \left[1 - \exp \frac{-[T_p - (F_1/k_{\min} N_p)]}{\tau} \right] \right\} = \frac{F_1 + \eta\gamma(F_2 - F_1)}{N_p} \quad (6-50)$$

from which k_{\min} can be determined transcendently. As T_p increases (for given N_p/N_b), k_{\min} decreases at such a rate that $I_p^{\min} = k_{\min} T_p$ decreases, and thus the range ratio \mathcal{R} increases.

Since I_p^{\max} also increases with T_p in Case a, the increase of \mathcal{R} with T_p is faster in Case a than in Case b.

In normal operation we would set the priming duration equal to the matched value since at this duration the range ratio is already just about maximum. But the matched-value duration depends on the turns ratio N_p/N_b . In particular, we would like now to show that the longer the priming duration, the closer $N_p/N_b \rightarrow 1$ for the matched case. In the limit, $N_p/N_b = 1$, and $I_p^{\max} \rightarrow \infty$, and hence also $\mathcal{R}_{\max} \rightarrow \infty$. Recall from Eq. (6-44) that N_p/N_b typically has a value ≈ 3 for a matched case of rectangular-pulse priming.

To show this dependence on N_p/N_b let us assume a matched design in terms of Fig. 6-18, that is, $T_p = T_{pm}$, and trace the effects of a change in N_p/N_b . From the limiting relations for k_{\max} and $I_{p\uparrow}^{\max}$, we can deduce that if either N_p decreases, or N_b increases, or both, then k_{\max} decreases and $I_{p\uparrow}^{\max}$ increases. Thus, assume that we increase the prime duration T_p . For this new duration to represent a matched design, the intersection point of Fig. 6-18 must be moved to the right. But this can only be achieved by decreasing N_p/N_b , which results in an increase in $I_{p\uparrow}^{\max}$ and a decrease in k_{\max} . (Increasing N_p/N_b would move the intersection point to the left.) Thus, the larger the allowed priming time the closer $N_p/N_b \rightarrow 1$ for a matched design.

The ramp $i_p(t)$ waveform may be modified to advantage by replacing the sudden fall at $t = T_p$ by a gradual fall (such as an exponential decay) beyond $t = T_p$. The values of k_{\max} and I_p^{\max} are the same as for the simple ramp except for a minor increase in k_{\max} if T_p is slightly below T_S . On the other hand, k_{\min} and I_p^{\min} are lower, because switching may continue beyond $t = T_p$. As a result, \mathcal{R} is even higher than for a ramp $i_p(t)$. For the same reason, an even better modification than a gradual fall is to maintain i_p constant for a specified time beyond $t = T_p$. The resulting overall $i_p(t)$ waveform is then trapezoidal. Similarly, improved results can be obtained with a half-sine priming current, as shown by Nitzan (1965).

For a typical core used in MAD-R logic circuits, with minor aperture about 1/10 the diameter of the major aperture, computed and measured values of I_p^{\max} and I_p^{\min} versus T_p at room temperature are compared in Fig. 6-19 for a ramp priming current with exponential decay of time constant $\tau_f = T_p/2$. Two N_p/N_b values are shown: $6/6 = 1$ and $6/4 = 1.5$. Note that the unity-ratio case, $N_p/N_b = 6/6 = 1$, results in $I_{p\uparrow}^{\max} \rightarrow \infty$, that is, no flattening of the curve, as predicted. But note that the case of $N_p/N_b = 1$ is actually superior to the case of $N_p/N_b = 1.5$ only if $T_p > 450 \mu\text{sec}$.

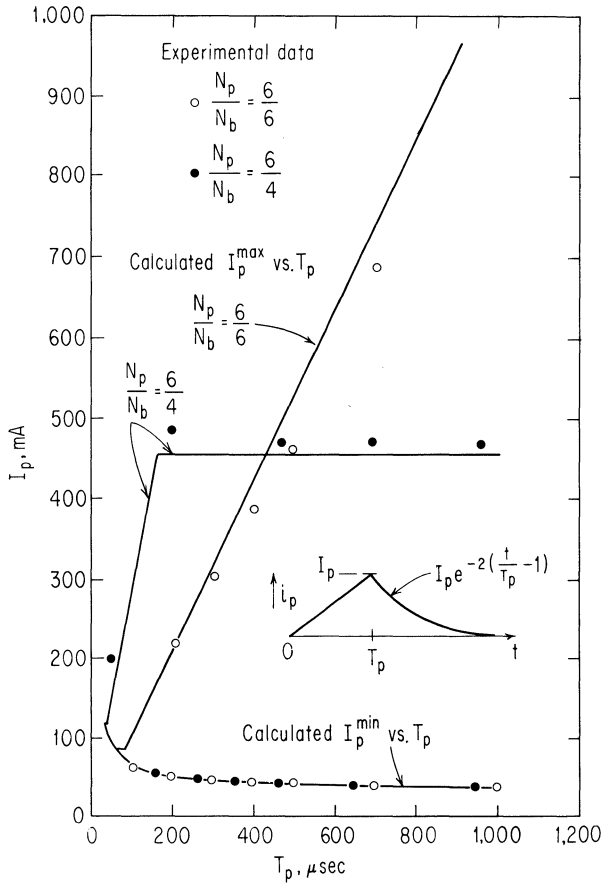


Fig. 6-19. Calculated and measured I_p^{max} and I_p^{min} vs. T_p with N_p/N_b as a parameter ($T = 25^\circ\text{C}$).

Effect on Core Designs. Enlargement of the minor apertures may be desirable in order to reduce the cost of fabrication (because wiring is easier), but this reduces priming range. With the technique of slow-rise priming just described, however, some reduction in range ratio \mathcal{R} may be tolerated. For example, with a minor aperture as much as $1/4$ the area of the major aperture, we calculate for a given core material at 25°C , $\mathcal{R}_{\text{max}} = 4.8$ with $N_p/N_b = 7/5$ for a bit rate of 500/sec., or $\mathcal{R}_{\text{max}} = 10$ for $N_p/N_b = 6/5$ for 60/sec. In comparison, we calculate $\mathcal{R}_{\text{max}} = 2.5$ for a bit rate of 60/sec. using a rectangular pulse. (This result as compared to the results in Fig. 6-19 gives an idea of how relative path lengths around major and minor apertures must be considered in conjunction with overall core design, discussed in the next section.)

6-9 Core Design

The purpose of this section is to outline the major considerations in the design of multileg cores. Though the emphasis is on aspects important to MAD-R circuitry, the underlying principles are of more general nature. We consider only the geometrical aspects of core design. The problems of designing material mixes for certain specifications, and for controlling the mixing, pressing, and firing operations are beyond the scope of this book. (It should be mentioned, however, that there is the potential of using two different ferrite materials in different sections of the same core, in order to enhance the ratio of major/minor aperture thresholds to a value greater than the ratio of major/minor aperture path lengths, as described by Heckler (1967).)

Gross Aspects of Size and Shape. Since the required drive currents are proportional to core path lengths (assuming a single material), and switching voltage is proportional to cross-sectional area, core miniaturization is important for achieving low current and low power levels. An additional factor against large size, for ferrite cores, is the press-and-die problem, since very high pressures are required during the forming process to achieve high-density uniform packing of the constituent metal-oxide powders. On the other hand, miniaturization tends to be limited by such mechanical factors as fragile elements in the core-forming dies, fragility of the cores themselves, and inadequate space for windings.

Of these factors, the size limitations based on requirements for coupling loops are the most significant and fundamental. For example, suppose we start with a well-designed circuit with $N_R = 1$ and specify that wire length and all core dimensions are to be scaled down uniformly, but that wire cross section is to be adjusted so as to maintain unchanged the ratio of loop resistance to receiver switching resistance, namely, $R_l/N_R^2\bar{\rho}$, in order to maintain a good design with transfer and priming times unchanged. The switching resistance $N_R^2\bar{\rho}$ can be rewritten as $N_R^2\Delta\phi_R/S_w l$, where l is path length and S_w is the switching coefficient of the material. (For more discussion of S_w , see Sec. 12-6.) Since $\Delta\phi_R$ is proportional to the cross-sectional area of the core, then $\bar{\rho}$ is proportional to area/length—or just to the linear scaling factor since all core dimensions are scaled uniformly. Since R_l is proportional to length/area of the wire, then with wire length scaled down with core dimensions, the wire cross section must be kept constant in order for $R_l/N_R^2\bar{\rho}$ to remain constant. This means that the ratio of

aperture area to wire cross section decreases as the square of the scale factor. For typical cores and circuits (with minor-aperture diameters of 20-30 mils), coupling-loop wires already fill a substantial portion of minor-aperture space, so in fact very little further miniaturization is possible without sacrifice in performance. (The practical lower limit on minor-aperture diameter for MAD-R circuits, depending on other details of the cores, is probably in the range of 10-20 mils.)

Path-length ratio, i.e., the ratio of switching path lengths around the major and minor apertures, affects drive tolerances for all core-wire schemes, but has a most direct affect on the priming range of MAD-R circuits (see Sec. 6-8). On the basis of the desired path-length ratio and a minimum practical minor-aperture size, an overall core size in the planar view may be selected. There is still a question of how thin to make the core (in the third dimension), the objective being to minimize voltage requirements. Aside from the question of the mechanical strength of the core, problems relating to air-flux leakage become significant if the thickness of the core is substantially reduced in proportion to the other dimensions. (The minimum practical thickness is also of the order of 10-20 mils.)

The number of minor apertures required may range from one (adequate for simple shift registers with major-aperture input) to four, five, or more, for logic-circuit cores—say, two apertures for inputs, two for outputs, and one, perhaps, for readout to a power output device, as indicated in Fig. 6-8.

Shaping to Minimize Soft-Threshold Effects. Consider the three-leg core of constant thickness shown in Fig. 6-20(a), which has one minor aperture in an otherwise purely toroidal core. In this case, after a clearing mmf $N_C i_C$ has been applied and then removed, Leg m cannot remain saturated because $w_m > w_3 + w_4$, where w represents the minimum leg width. The resulting soft threshold of Leg m is undesirable as it may cause spurious setting (for example, during the priming phase in MAD-R operation). To overcome this problem, we may design the core so that $w_m = w_3 + w_4$. This is generally accomplished by shaping Leg 4 as shown in Fig. 6-20(b). Four alternative ways for shaping a core with two minor apertures are illustrated in Fig. 6-20(c) to (f). In Fig. 6-20(e), two slots are made in the upper and lower parts of Leg m as an alternative to shaping around the minor apertures. In Fig. 6-20(f), the axes of the major and minor apertures are perpendicular, and Legs 1, 2, 3, and 4 are shaped in the third dimension.

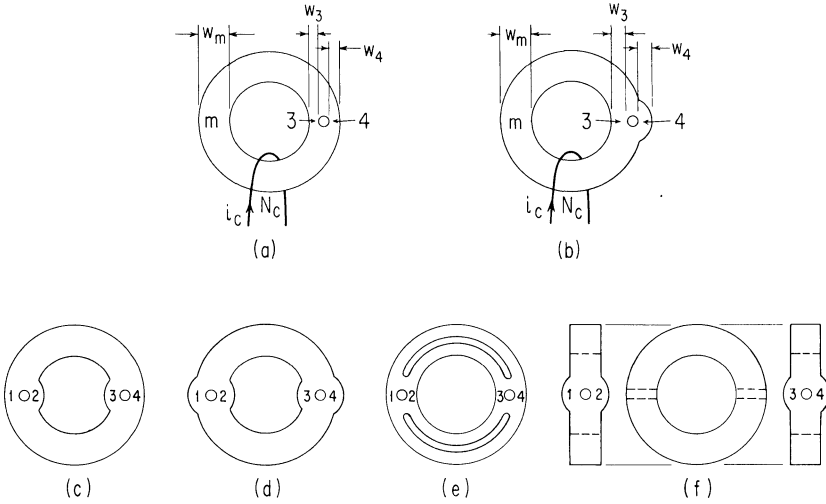


Fig. 6-20. Different methods of core shaping that maintain constant cross-sectional area, as compared to the core in (a).

Design for High Ratio of One/Zero Output. As discussed in Sec. 6-4, the flux state of a multiaperture core may be detected non-destructively by applying an ac drive to a minor aperture. Our objective now is to consider the effect on readout voltage (or flux) as we vary the magnitude of $w_3 + w_4$ as compared with w_m .

First, consider the case of a core with $w_3 + w_4 > w_m$. An mmf $N_C i_C$ large enough to saturate all legs is applied in the clear direction to Leg m (Fig. 6-21(a)). As i_C is removed, a magnetic pole distribution is established, as indicated by the plus and minus signs in Fig. 6-21(a), causing partial demagnetization of Leg 3 along the shortest path length. With ac drive applied as in Fig. 6-8, some flux can now switch inelastically around the minor aperture, in amount proportional to $(w_3 + w_4 - w_m)/2$. The magnitude of switchable inelastic flux for the core in the set state is proportional to $[\min(w_3, w_4)]$, that is, the lesser of the two values w_3 and w_4 . Therefore, the *one/zero* ratio of output flux values is approximately

$$\frac{\Delta\phi_1}{\Delta\phi_0} \approx \frac{[\min(w_3, w_4)] + \delta}{[(w_3 + w_4 - w_m)/2] + \delta} \quad \text{for } w_3 + w_4 \geq w_m \quad (6-51)$$

where δ is a correction term for elastic flux, assumed the same for both the *one* and *zero* cases. Following Eq. (6-51), the highest *one/zero* ratio is obtained for $w_3 + w_4 = w_m$ and $w_3 = w_4$.

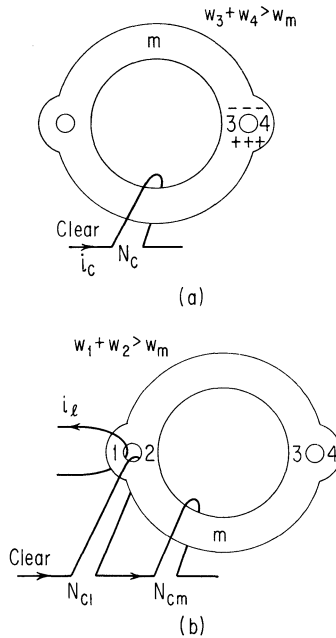


Fig. 6-21. Circuits for testing the effect of differences in cross-sectional areas of the major leg versus the sum of the minor leg areas on (a) *one/zero* readout ratio, and (b) input-aperture clipping.

If $w_3 + w_4 < w_m$, then after the clearing pulse, the polarity of the poles is reversed from that shown in Fig. 6-21(a), and the remaining static field causes Legs 3 and 4 to be magnetically stressed in the clear direction. The elastic permeability is therefore lower, and the δ terms of Eq. (6-51) are therefore even smaller than in the case of $w_3 + w_4 = w_m$, though the signal output for the set state is very nearly the same as for $w_3 + w_4 = w_m$. Thus, we can actually obtain an enhanced *one/zero* ratio with $w_3 = w_4$ and $w_3 + w_4$ slightly less than w_m . (It is not practical, however, to design for equally enhanced *one/zero* ratios from each of two or more apertures, because of dimensional variations. The highest ratio will actually be obtained from the aperture that happens to end up with the smallest effective cross-sectional area in its adjacent legs.)

Minor-Aperture Flux Clipping. Consider again the case $w_1 + w_2 > w_m$ and the drive arrangement of Fig. 6-21(b). After a large clearing mmf has been applied, Legs m and 1 will be left in

a hard clear state and Leg 2 will be partially demagnetized. In this case, some inelastic flux will switch in Leg 2 in response to a relatively low level of input information current i_p . In other words, flux clipping may be achieved for Leg-1 input if Leg 2 is unsaturated at the beginning of the input phase. This condition is assured in Fig. 6-21(b) by the linking of a Clear winding around Leg 1 to ensure that this leg is saturated by the Clear mmf. This provision is not actually necessary for typical MAD-R circuits, since the back-loop current generally reverses in direction after removal of the Clear pulse, with sufficient magnitude to assure full clearing of the leg that is linked by the input coupling loop.

6-10 Summary

This chapter is concerned exclusively with the MAD-R scheme, which to date has received the greatest study with respect to design and application. In Secs. 6-1 to 6-3, three different derivations of the MAD-R scheme are presented, each one starting from a scheme that was developed earlier in the book. The approach is to try to eliminate the prominent weakness of the previous scheme, and in so doing, we end up in each case with a MAD-R circuit. Each derivation adds emphasis to different aspects of the MAD-R circuit and each therefore helps to convey some feeling for why this scheme, though relatively simple in structure, exhibits such good performance. (In Secs. 8-3 and 9-1, variations on the MAD-R scheme are presented which hold promise of even further improved performance, but at the expense of increased physical complexity.)

The remainder of this chapter is concerned with techniques that have been developed for practical design of the various portions of MAD-R circuits, primarily the coupling loops and the advance and prime circuits, as well as design of the cores themselves. Coupling-loop design involves the choice of transmitter turns and receiver turns, as well as the choice of wire size and length, which in turn govern the values of coupling-loop resistance and inductance. Starting in Sec. 6-6, we develop basic design equations for the coupling-loop and advance circuits, assuming the availability of certain key design parameters. Then we describe relatively simple experimental techniques for deriving quantitative expressions for these design parameters. Analysis of the priming circuit

shows the basic trade-off that is possible between speed of operation and drive-current tolerances. In particular, it is shown how these circuits are relatively easily designed for operation over a wide temperature range, e.g., from -50 to $+75^{\circ}\text{C}$. Finally, it is noted how certain aspects of the design of the multileg cores themselves affect performance.

The design techniques presented here are relatively crude by comparison with those that might be developed, based on the computer models for cores described in Chap. 12. However, these techniques are actually quite simple to apply, and they have proven to be very effective in the development of practical MAD-R circuits.

FORMAL DERIVATION OF TRANSFER SCHEMES

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In the previous chapters, many of the concepts and principles important to the subject of core-wire transfer circuits were introduced, and a number of different types of schemes were derived. In Chaps. 8 and 9, we will discuss still other kinds of core-wire schemes, some of which may become quite practical, depending on application requirements and future material developments. All of these schemes, the earlier ones as well as those to be discussed later, were discovered in rather random fashion, independently, and it is therefore important to develop tools whereby the interrelations of these various schemes can be more clearly seen. The network representation of Chap. 5 is helpful in that it provides an easy way to follow sequencing between flux states. The method of this chapter is another step in this direction; it provides some formal steps for dissecting and classifying schemes, and leads to an interesting overall way to view them. The technique is not essential for understanding the remainder of the book, however, and

the reader may therefore bypass this chapter without loss of continuity. The main reason for presenting this material now is that it offers a more consolidated overall view of the relatively simple schemes developed thus far, before we go on to the more complex schemes of Chaps. 8 and 9.

The primary approach is: (1) choose a certain network configuration to study; (2) list all possible flux patterns for this network; (3) form a set-state chart, by investigating which flux patterns can be converted into which other patterns by a $\Delta\phi$ -transfer operation; and (4) form sequences of connected states that represent closed cycles. Each such sequence represents a potential scheme to study further, and all schemes can thus be systematically searched. Though only a few simple types of configurations have thus far been investigated in this manner, the process has resulted in a systematic "rediscovery" of some of the schemes already discussed, as well as some new ones.

7-1 Van De Riet Representation

In Sec. 5-3, it was noted that by manipulating node types, a given scheme could be realized in various circuit configurations. No matter how different the physical appearance, however, we nevertheless considered the variations as realizations of the same basic scheme. Differences between schemes were described only on the basis of (1) the basic network form, and (2) the particular sequence of flux states. For these criteria the node type is not important. For consistency in discussion of schemes, then, we might profitably think in terms of network diagrams in which all nodes are deliberately of the same type; following Van De Riet (1963) we will use all synthetic nodes, corresponding to an all-toroid form of realization.

A given number of toroids can be interconnected in a large number of ways. Our job is to find those methods of interconnection which lead to useful transfer schemes. We assume the same method of data representation used in the previous chapters: a binary *one* is represented by storage or transfer of a certain unit of $\Delta\phi$, and a binary *zero* is represented by nominally zero $\Delta\phi$ transfer. We temporarily add another constraint, namely that all bits of a register are processed identically at every instant.

Configurations (a) to (d). By the configuration of a toroid-wire circuit, we mean the specific way in which the toroids and coupling

loops are linked together. Two toroid-wire circuits have the same configuration if they can be made to coincide geometrically by stretching, twisting or bending the loops and elements. The configuration of a circuit is important in classifying a scheme but we will see that it is not complete in itself. In most cases, different sequences of flux-state patterns can be shifted along the same configuration, each of these then amounting to a different scheme of transfer.

The number of coupling loops linking a given toroid is an important aspect of the circuit configuration and of the structure of the equivalent network. A core linked by only a single coupling loop will be referred to here as a *loop core*. A core that couples a pair of coupling loops, by virtue of being linked by both, will be referred to as a *coupling core*. The method discussed here has not been developed in sufficient generality to handle circuits that contain other than such singly and doubly linked cores.

It is convenient to distinguish between simple and complex configurations. In a *simple configuration*, two adjacent loops are coupled through only a single core so that there are just two coupling cores linking each loop (though any number of loop cores). Thus, a simple configuration can always be transformed to a ladder network (see Sec. 5-2). In a *complex configuration*, there may be more than two coupling cores in some loops. For example, in the toroid-wire flux doubler of Fig. 5-23, there are four coupling cores and one loop core per coupling loop. (In the orthogonal scheme of Fig. 8-13, we will find eight coupling cores and no loop cores per coupling loop.) We consider here only simple configurations, although there is no reason why the technique cannot be extended to complex configurations.

A simple configuration can be represented by a chain of coupling loops, each pair of adjacent loops being interconnected by a single coupling core. Some examples of simple configurations, with their corresponding unbalanced network representations, are sketched in Fig. 7-1. (No winding polarities are shown in the figure because we need not be concerned with such details at the moment.) Recall from Chap. 5 that each coupling loop is represented by only a single node in an unbalanced network, there being one ground node for the entire network. Coupling cores are represented by series branches between two nodes, and loop cores are represented by shunt branches to ground.

Iterative or periodic configurations have been indicated for all the examples shown. The shortest section that repeats is called the *period*. In Examples (a), (b), and (d), the period brackets only

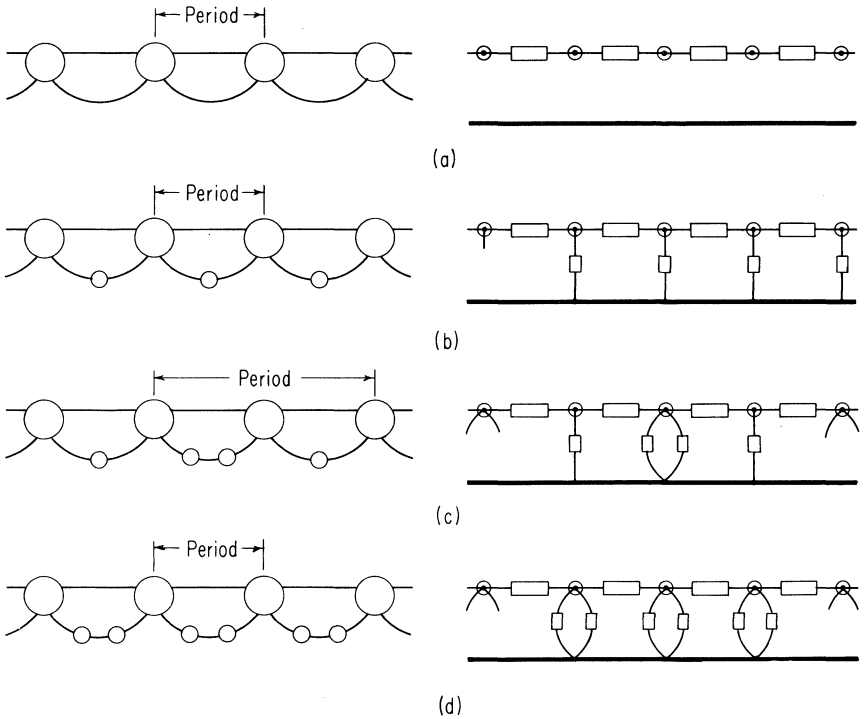


Fig. 7-1. Some simple configurations with their corresponding network representations.

a single coupling loop. In Example (c), the period encompasses two coupling loops. It is clear that aside from polarities, simple configurations can differ only in the number of loop cores in the coupling loops. Thus, all possible simple configurations can be drawn by systematically increasing the number of loop cores in each loop. We will treat schemes having the configurations shown in the last three parts of Fig. 7-1, that is, schemes with configurations (b), (c), or (d). (There can be no schemes having the configuration of Fig. 7-1(a), since there can be no flux switching except in all cores simultaneously.)

Transfer between Set-State Patterns. With idealized zero-impedance coupling loops, there are only certain patterns of saturation states that can exist in a coupling loop, because there can never be a net change in flux linkage in the loop. We will always assume one of these patterns to be the clear state, arbitrarily

(but not restrictively) defined as the state in which all cores are saturated clockwise. Any set-state pattern then requires two or more cores to be set, or saturated, counterclockwise. If any one core in the circuit switches, then some other core in the same loop must switch simultaneously. Assuming for now that all cores have the same flux capacity and that if a core switches at all, it switches completely, then only an even number of cores can switch simultaneously in every coupling loop.

Let us consider the set-state patterns involving only one pair of cores per loop, as in Fig. 7-2(a), (c), and (e), where the set cores are shown shaded. From these patterns it can be inferred that any pattern limited to a single pair of set cores per loop will always be made up of two loop cores that are set, and some arbitrary number of set coupling cores between these two loop cores. The networks corresponding to the circuits of Fig. 7-2(a), (c), and (e) are shown in Fig. 7-2(b), (d), and (f).

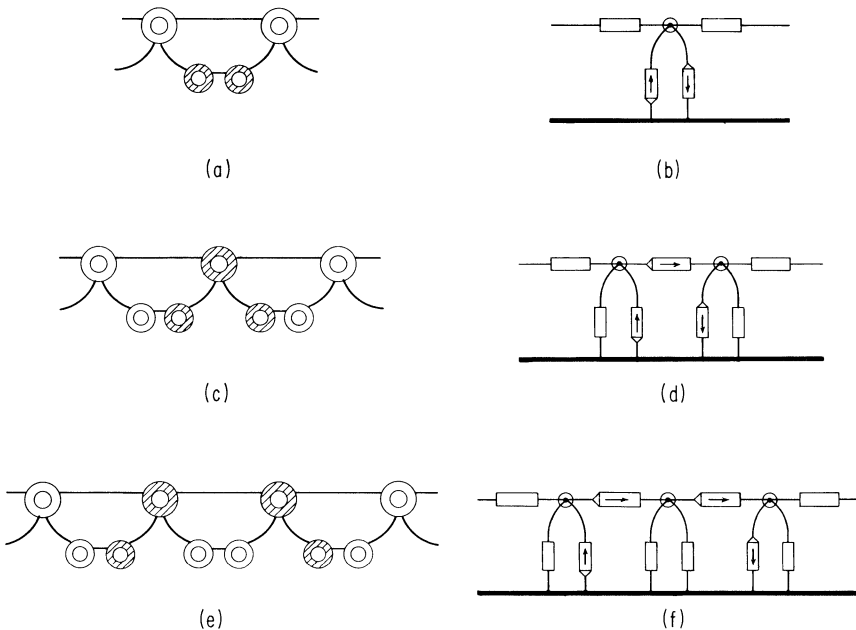


Fig. 7-2. Set-state patterns involving only one pair of cores per loop.

Though no winding polarities are shown in Fig. 7-2, allowable polarity combinations can be readily determined. If two cores that are linked by the same loop are switched simultaneously, they must

have winding polarities that lead to emf cancellation in the loop. Thus if two such cores are in their clear states (or both in their set states) prior to switching, then they must have opposite winding polarity; and conversely, with their initial states opposite, the winding polarities must be the same.

Let us now consider the transition from one data state, or flux-state pattern, to another. For purposes of illustration we use the Engelbart scheme of Fig. 5-20(d). The circuit for a three-bit section of register is indicated in Fig. 7-3, where the bit length encompasses two periods of the structure. A *one* is represented by each triple-core set-state pattern shown shaded (in the first and second bit positions). The same group of toroids would contain a *zero* if all toroids in the group were initially in their clear states. During the shifting operation, different groups of toroids will hold the set-state pattern. For example, the pattern for 110 is shown in the figure and it is assumed that there is a *zero* to the left. The drive sequence $O \rightarrow E$, Clear O , $E \rightarrow O$, Clear E , advances the pattern exactly two periods, or one bit length, to the right, as indicated below the figure. After one complete clock cycle, the triplet of cores initially holding the set-state pattern for the j th bit again holds the same pattern, but now representing the $(j + 1)$ st bit.

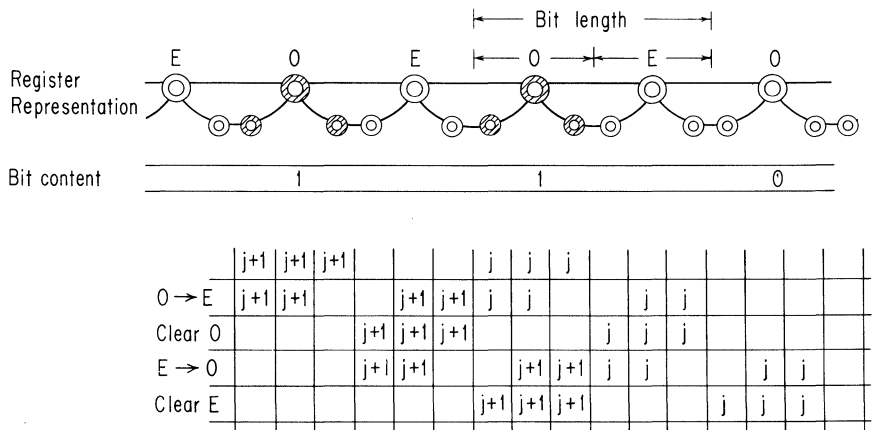


Fig. 7-3. Cycle of set-state patterns for the Engelbart scheme of Fig. 5-20(d).

pattern, but rather by a sequence of such patterns. Our main goal now is to search for all of the possible sequences of set-state patterns that can lead to proper binary transfer. (We might note that a flux transfer, or transmission, can be thought of as the setting of one core as the result of clearing another core linking the same coupling loop. If necessary, bias drives are applied to aid the switching of the receiver and inhibit the spurious switching of other cores. It will be assumed here that proper clearing and bias currents can be provided, and only the sequence of the transfer will be considered, although it is possible to devise flux-transfer sequences that satisfy all flux-state transition requirements, but yet cannot be driven in such a way as to be operable.)

7-2 Set-State Chart

Schemes with Configuration (b). The configuration of Fig. 7-1(b) will be used to show a technique for generating all possible schemes in a given category. One bit-length of a register having this configuration is shown in Fig. 7-4. The bit-length is chosen as three

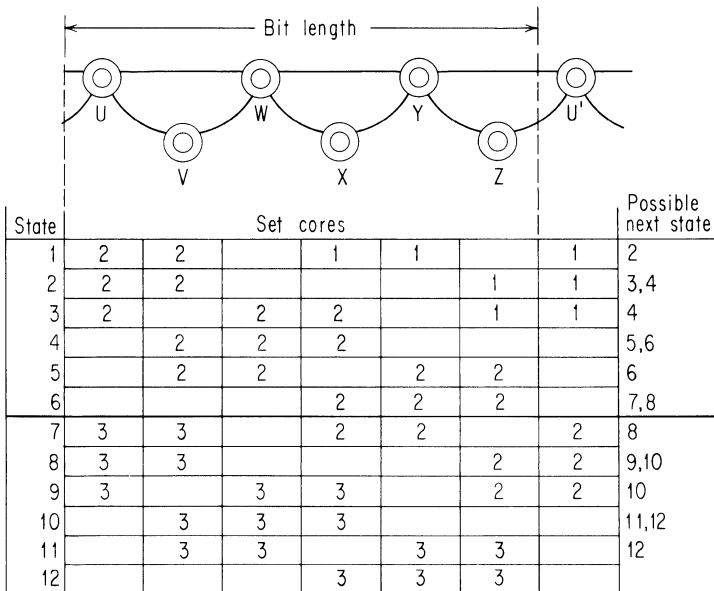


Fig. 7-4. List of set-state patterns for the configuration of Fig. 7-1(b) and a bit-length of three periods.

periods long because, as we will see, there are no schemes with bit-lengths of only one or two periods for this configuration. Assume the bit-length of Fig. 7-4 holds part or all of a set-state group which represents a *one*. Assume also that there are *ones* in both adjacent bits, and let the three bits be represented by set-state patterns labeled 1, 2, and 3.

In general, there is a relatively large number of possible set-state patterns, though we will now describe a simple procedure for listing all of the patterns for a given configuration. Consider the second bit-length of some arbitrary simple configuration, and draw the configuration with a coupling core as the leftmost core. Build up the pattern, as in Fig. 7-4, by setting the two leftmost cores and record it by placing a 2 in each of the two leftmost columns. Now set other cores, as necessary, to meet the requirement of identical bit processing and an even number of set cores in any given loop. Where there is more than one possibility, order them so that the states with the leftmost set cores come first. Following these rules, we obtain the first six rows of the chart in Fig. 7-4. (The bottom six rows are identical to the top six rows except that the numbering is advanced by one. Though redundant, it is useful later to have these rows labeled independently.)

When we draw only a single bit-length, some of the cores in a set-state pattern will of course not be shown because they are in adjacent bit lengths. However, their location is known because there will be set cores in the bit-length in question, corresponding to the ones not shown. In other words, the position of all cores in any set-state pattern is known though only one bit-length is shown. Thus we can readily see that in Row 1 the basic set-state pattern contains four set toroids per bit, but that in Rows 2 and 4 there are only three set toroids per bit in the set-state pattern.

Permitted Transitions. From the above, we see that under the temporary restriction of processing all bits identically, there are six and only six possible set-state patterns in a bit-length of the configuration of Fig. 7-4. Any transfer scheme using this configuration must therefore use set-state patterns included in the above list, and any shifting process will simply represent a series of changes from one set-state pattern to another.

In terms of the patterns listed in Fig. 7-4, a shift cycle is accomplished when all the numbers in the final set-state pattern correspond in position to the numbers in the initial pattern, but advanced by one. For example, a complete shift cycle should

convert the pattern of Row 1 to the pattern of Row 7. To determine what set-state patterns might be involved in a complete shift cycle, it is necessary to determine for each pattern which other patterns it can be changed to in one step. These changes are just the transfers described earlier, where clearing of one loop core causes the setting of some other loop core on the right, either directly in the same loop, or indirectly through a chain of coupling cores. For example, the set-state pattern of Row 1 can be changed or transferred in one step to that of Row 2 by clearing Cores X and Y and setting Core Z. The set state in effect is taken out of Loop Core X and put into Loop Core Z, reversing Coupling Core Y as it passes.

Finding which set-state pattern can be changed in one step into which other ones can be done by inspection, provided we keep in mind some simple rules. Basically, we check to see if one set-state pattern can be changed into another one by the clearing of one loop core and the setting of another, while reversing the state of all intermediate coupling cores, according to these rules:

1. Only one loop core can be cleared in a bit length and only one loop core set during one clock time.
2. No core being cleared can be set during the same clock time.
3. Between the pair of loop cores being set and cleared, there can be no coupling cores which hold part of a set-state pattern representing a different bit.

Following these rules, we find the allowed transitions listed to the right of each set-state pattern in Fig. 7-4.

Shift Cycles. It now becomes clear that finding all possible schemes for a particular configuration is just a matter of finding the possible paths between all pairs of set-state patterns representing endpoints of a complete shift cycle. To find these paths, it is convenient to write down the row numbers for all of the set-state patterns and to draw a line between each pair of numbers for which a transfer is possible in one step. In this way we obtain the transfer diagram of Fig. 7-5.

The problem of finding all possible cycles is now simple. Consider, for example, the set-state patterns 2 and 8, which are different by exactly one shift cycle. From Pattern 2 we can go to Pattern 4; from 4 to 6; and from 6 to 8. This scheme requires

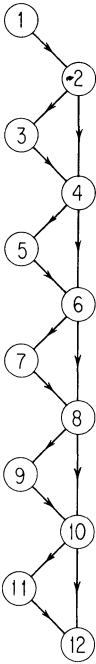


Fig. 7-5. Diagram of all possible set-state transitions for the configuration of Fig. 7-4.

three steps to accomplish the shift, each of these steps corresponding to one of three clock pulses. This particular scheme is shown in network form in Fig. 7-6, along with the flux switching path for the State-4 to State-6 transition. In this transition Branches V, W, and X are initially set, and the idea is to transfer from V to Z, via Branches W and Y, but without disturbing X. For this transfer to be accomplished, the shunt branches must have a relatively high threshold compared to the coupling branches, so that proper biasing can be applied.

We would like now to show that there are no other possible schemes with the configuration of Fig. 7-4 for three or less stages per bit. At first glance, we might think that we could develop a four-clock state sequence of the form 2, 4, 5, 6, 8, or even a six-clock sequence involving all of the states. To see that these sequences are in fact not possible, we must note an additional requirement of consistency for the entire sequence of states, in addition to the rules for a single transition between two states.

Consider States 4, 5, and 6. The transition to State 4 must occur with Cores W and X switching together from their initial clear states. This implies that the two cores must have opposite winding polarities. The transition from State 5 to State 6 also requires Cores W and X to switch together, but this time starting from opposite flux states. This requires that they have the same winding polarity in the loop. The two requirements are clearly inconsistent and therefore make it impossible to have a scheme in which these three states appear. Similarly, none of the other states in the left-hand column of Fig. 7-5 can be included. Thus we see how the requirement of overall

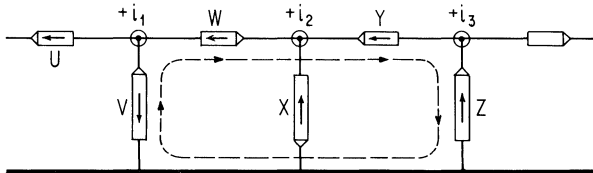


Fig. 7-6. Three-clock scheme corresponding to set-state transition sequence 2-4-6-8.

consistency means that some transitions cannot appear in a given cycle with certain other transitions.

From the above, we see that with a three-period bit-length for Configuration (b), the three-clock scheme of Fig. 7-4 is the only possible one. If we had assumed a bit-length of only two periods, the set-state chart would have shown only two possible states, with no allowed transition, and in the case of a single-period bit length, there are no possible set states at all. Hence, we need at least three periods per bit with this configuration.

7-3 Schemes with Configuration (c)

We could proceed to develop a new set-state chart and search for permitted sequences based on Configuration (c) of Fig. 7-1(c), but we can short-cut this entire effort based on the following observation. Configuration (c) is derived directly from Configuration (b) if we can eliminate one of the coupling cores, specifically, Core Y in the conversion from Fig. 7-7(a) to (b). We can be sure that with this configuration and bit-length, there are no additional

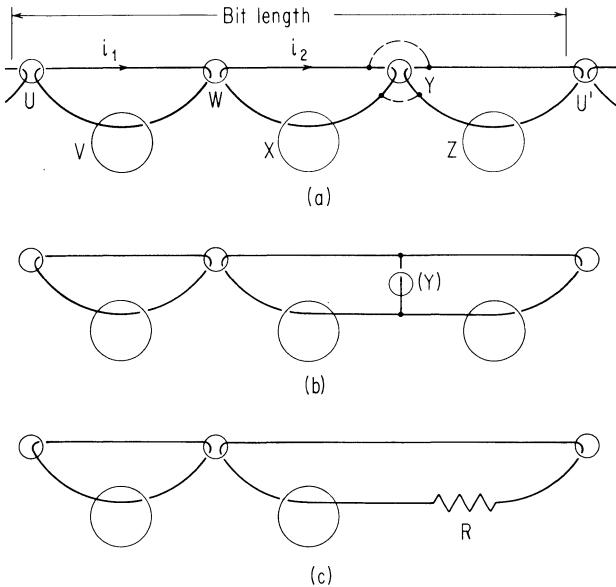


Fig. 7-7. Converting from Configuration (b) of Fig. 7-1 to Configuration (c) by eliminating Core Y; and then to a corresponding resistance scheme by replacing Core Z by a resistor.

schemes beyond those already shown for Configuration (b), since the set-state chart for this abridged configuration would if anything be more confined than the original.

Let us see now why Core Y can in fact be eliminated. First, Core Y is not required for turns ratio since there are other coupling cores in the chain available for this function. Second, by tracing the state sequence $2 \rightarrow 4 \rightarrow 6$ in Fig. 7-4 we see that Core Y is set and cleared on adjacent clock pulses, and therefore serves no essential memory function. The primary role of Core Y is in isolating against back transfer (during transfer out of Core Z), but it is not absolutely necessary. Thus the same three-clock scheme derived for Configuration (b) applies also to Configuration (c), though more care is required in the drive circuits. (One might think that we could eliminate Core W as well, leaving only a single coupling loop per bit, but there would then no longer be sufficient isolation between bits.)

The physical process of eliminating Core Y can be thought of as follows. Since Core Y is not required for turns ratio, we can assume equal input and output turns. In this case, the voltages generated in the two windings are always identical, and the two windings may therefore be connected together, as indicated by the dashed lines in Fig. 7-7(a). The circuit then has the form of Fig. 7-7(b), and unless Core Y is used for holding against back transfer, as described above, it can simply be eliminated.

A corresponding resistance version can be arranged by replacing Core Z by a resistance, as in Fig. 7-7(c). This circuit is just the all-toroid version of the Engelbart circuit of Fig. 4-7(c). Thus we see that the latter arrangement is minimal in the sense of the total number of branches required per bit, namely, four core branches and one resistance branch. No known scheme in the categories considered thus far has fewer cores and resistors per bit (though in Sec. 9-2 we will find a scheme that requires only $1\frac{1}{2}$ magnetic elements and $1\frac{1}{2}$ resistors per bit, based on the coherent-rotation property of thin films).

7-4 Schemes with Configuration (d)

The configuration shown in Fig. 7-1(d) is one in which a number of different schemes have been discovered. The set-state chart and transfer diagram for this configuration are shown in Figs. 7-8 and 7-9, respectively. From the rather complicated nature of the

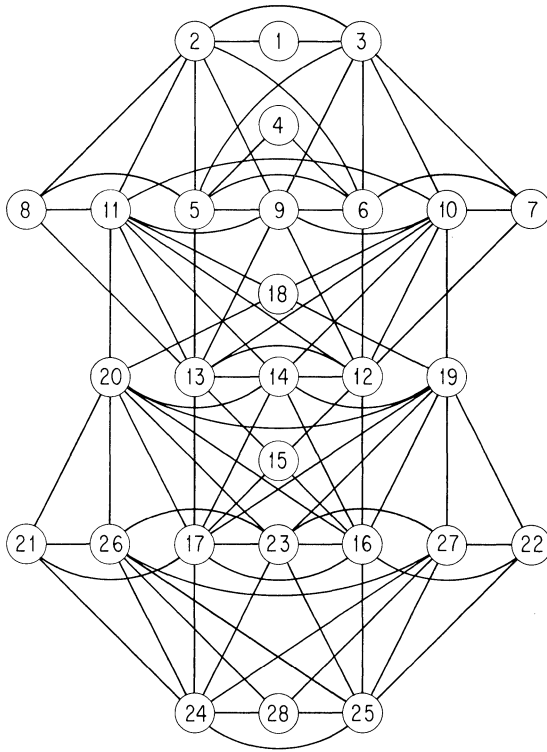


Fig. 7-9. Transfer diagram for Configuration (d).

from each other. These trivial differences are of two types, related to (1) starting point difference, and (2) differences due to loop-core interchanges:

1. A scheme is a repeating sequence of set-state patterns, and there is no real starting or ending pattern as such. Thus any given sequence will show up as a scheme as many different times as there are set-state patterns in the sequence, each scheme starting with a different set-state pattern but having in effect the same sequence.

2. Reversing the roles of two loop cores on the same loop produces only trivially different schemes. The two sets of schemes that result from this interchange manifest themselves in a mirror-image symmetry, such that for every scheme path; there is another that is exactly symmetrical with respect to a vertical line through the center of the transfer diagram.

We have already seen two four-phase schemes having this configuration, namely, the Engelbart and Russell schemes of Secs. 5-4 and 4-3, respectively. Referring to the earlier derivations of these schemes, it is readily verified that the set-state sequences are

- 3 → 7 → 12 → 15 → 17 (3) for Engelbart, and
- 3 → 9 → 12 → 14 → 17 (3) for Russell,

which are sketched on the abridged diagram of Fig. 7-10.

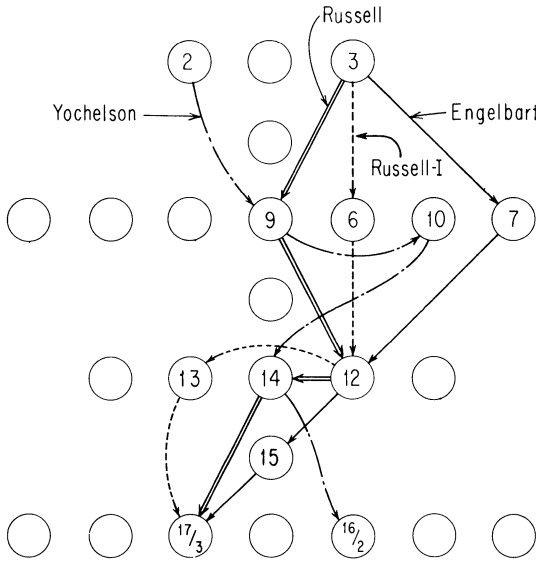
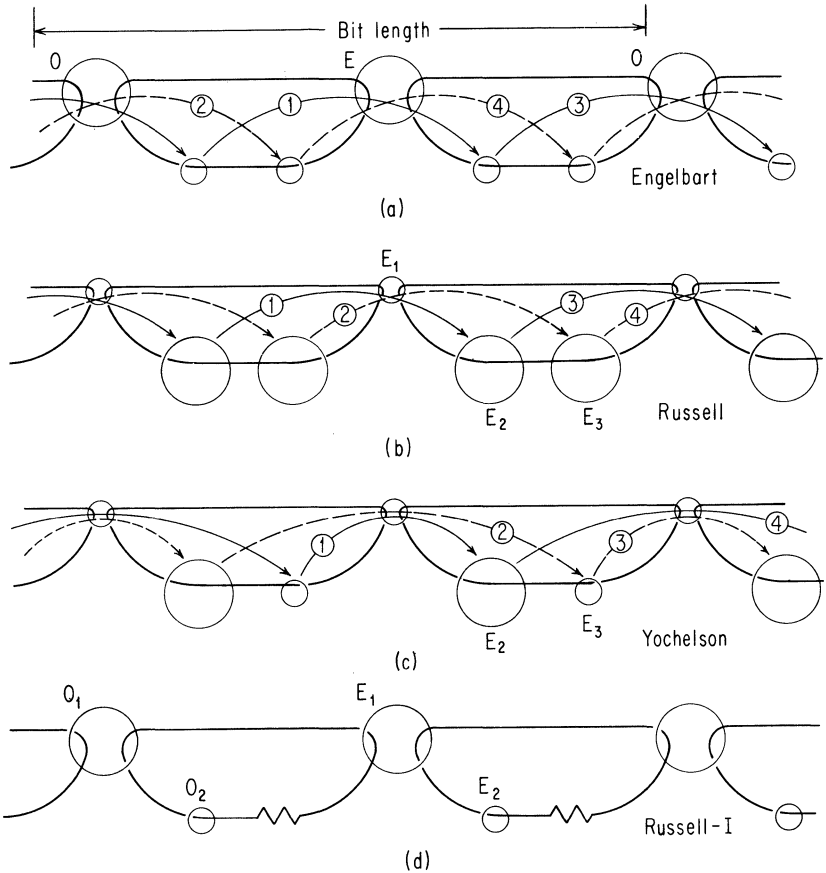


Fig. 7-10. Abridged transfer diagram showing the four-phase schemes.

The circuits for these two schemes are shown together for comparison in Fig. 7-11(a) and (b), with the four clock phases indicated by the notation 1, 2, 3, and 4. Recall that the Russell scheme has better isolation than the Engelbart scheme, because the coupling core is set and cleared on adjacent clock phases and therefore can be unconditionally held to give good isolation. (For example, in Fig. 7-11(b) we set E_2 through the coupler E_1 , and then immediately set E_3 while clearing the coupler.) But recall also that this resulted in the need for two large cores in the coupling loop, which tends to increase flux losses because of the larger loop currents that are therefore required.



Set state #							
③	2	2				①	1
⑥	2		②			①	1
⑫			②	2	2		
⑬			②	2		②	
⑰ ₃	3	3				②	2

Fig. 7-11. Four-phase schemes based on Configuration (d).

By still another change in sequencing we obtain the Yochelson (1960) scheme in which we find that we can make E_3 a small core, as shown in Fig. 7-11(c). The set-state sequence for this scheme is $2 \rightarrow 9 \rightarrow 10 \rightarrow 14 \rightarrow 16(2)$. In the Russell scheme we transmit

from Cores E_2 and E_3 in the same sequence that they are set, first from E_2 and then from E_3 . However, in the Yochelson scheme we transmit from E_3 before E_2 , so that E_3 is set and cleared on adjacent clock phases (i.e., it serves no storing role during any other clock phase) and can be held unconditionally during transfer from E_2 . It is for this reason that E_3 can be a small core, with the advantage of smaller drive currents and therefore smaller flux losses.

Finally, in Fig. 7-11(d), we diagram the Russell Type-I scheme of Fig. 6-4(b). Though this is a resistance scheme, we can determine the appropriate set-state sequence by imagining the loop resistance to be replaced by a core. The sequence of flux states thus obtained is shown below the circuit. Note that this scheme is quite different from the other three, because of the ‘within-the-loop’ transfer, that is, $\Delta\phi$ transfer from O_2 to the loop resistance, or to its replacement core, at the time we clear O_2 . The circled ‘2’ in the chart is a reminder that in the resistance version of the scheme, the transmitted $\Delta\phi$ is actually dissipated.

Though the set-state charts derived thus far are on the basis of identical data-state representation in adjacent bit positions, Van De Riet (1963) found one four-clock scheme, Fig. 7-12, that uses nonidentical representation. The set state sequence for this scheme is $2 \rightarrow 11 \rightarrow 20 \rightarrow 26 \rightarrow 30$ (2).

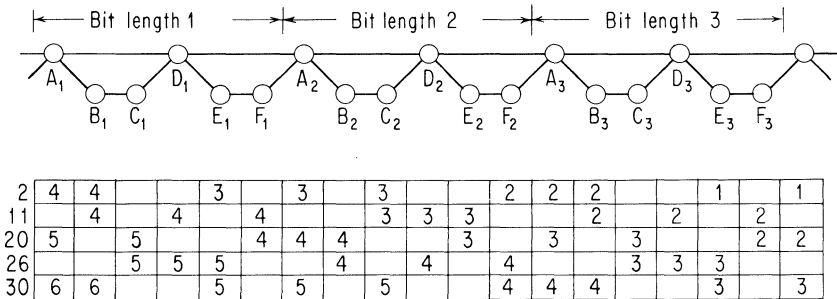


Fig. 7-12. Van De Riet double-speed four-phase scheme.

This sequence was found from an expanded transfer diagram, discussed by Van De Riet, of the type shown in Fig. 7-9 but where the states for several bits of transfer are followed. State 30 of the sequence comes from this extended diagram. An interesting point regarding this scheme is that each data bit moves two bit positions in a single four-phase cycle. From the flux states shown below the figure, we see that each coupling core processes a new data bit

every two clock phases. But each loop core responds only to every other data bit. Core B_1 responds to the even bits, and Core C_1 to the odd bits. In the neighboring loop, Core E_1 responds to the odd bits and Core F_1 to the even bits.

Van De Riet also shows that there are just two different three-phase schemes that are possible with Configuration (d). One of these has the sequence $2 \rightarrow 6 \rightarrow 12 \rightarrow 16$ (2), and the other one has the only slightly different sequence, $2 \rightarrow 9 \rightarrow 12 \rightarrow 16$ (2). The first of these has a $2 \rightarrow 6$ within-the-loop transition, as in the Russell-I scheme. The other sequence has a $2 \rightarrow 9$ transfer, which implies that the data at one time is stored solely in the two loop cores in a single loop, with no coupling cores involved. This is true also of the Russell and Yochelson schemes, though not for the Engelbart scheme.

For Configuration (d), we have treated the only two possible three-phase schemes and five of the four-phase schemes. These five were selected from the ten or so significant ones for a cross-section representation of the more distinctly different types of sequencing of states. Each of the remaining schemes is quite similar to one or the other of the ones considered.

7-5 Summary

A method is illustrated by which all possible transfer schemes can be derived for any given core-wire configuration. Though the technique may be cumbersome for complex configurations, it is relatively easy to apply for simple configurations, and we were able by this method to formally derive and identify a number of the schemes already discussed previously, as well as several new schemes. Derivation within the framework of a formal method such as this provides additional insight into the relationship between these different schemes. We were able to show examples of: (1) different configurations, (2) schemes with different numbers of clock phases within a given configuration, and (3) even different schemes for the same configuration and the same number of clock phases. However, exhaustive derivation of all possible transfer schemes in this way would be extremely tedious and is an area in which automated computer search could offer great aid.

FLUX SOURCES, ORTHOGONALITY, AND DYNAMIC BIASING

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Three concepts not discussed earlier are considered in this chapter: flux sources, orthogonal switching, and dynamic bias. An array of new schemes evolves with each of these concepts.

In the schemes developed thus far, a high or low level of flux is transmitted according to whether a similar level of flux was received previously. In Sec. 8-1 we consider the inverse situation, where a high level of received flux leads to a low level subsequently transmitted, and vice versa. This mode of transfer is referred to as *negation transfer*, in distinction to the first type which may be termed *simple transfer*. Except in a few cases, every simple-transfer scheme can be converted to a negation-transfer scheme, and the use of flux sources is a primary way to achieve this conversion. In Sec. 8-2, the notion of *modes* of switching, as opposed to individual paths of switching, is developed. A

number of new schemes evolve from consideration of orthogonal modes in particular. In Sec. 8-3, dynamic-bias techniques for effectively eliminating core threshold are introduced. These lead to schemes of increased physical complexity, but improved performance. (We will see in Chap. 9 how these concepts can be effectively combined with the bipolar mode of data representation to achieve still other transfer schemes of potentially practical importance.)

8-1 Negation-Transfer Schemes

By the term *negation*, we mean complementation of the data state, that is, replacement of each *one* by a *zero*, and vice versa. Since negation is one of the basic logical operations, techniques discussed here are relevant to general logic synthesis, as discussed in Chap. 10. Here, however, we are interested in negation transfer only from the standpoint of generating an additional class of transfer schemes. We will show two methods that can be used to convert most simple-transfer schemes to negation-transfer schemes, after we point out some general properties of the latter.

Flux-Transfer Properties for Negation. Consider the two-stage-per-bit transfer circuit of Fig. 8-1(a) in which all transfers are assumed to be negative. The basic response of each negation stage is shown in Fig. 8-1(b) and can be expressed as

$$\Delta\phi_T(j) = 2\phi_r - \Delta\phi_R(j) \quad (8-1)$$

where $\Delta\phi_R(j)$ is the received $\Delta\phi$ and $\Delta\phi_T(j)$ is the flux available for subsequent transmission from the j th stage. Suppose data is stored in the E stages. After two transfers the data is again held in the E stages, in identical form but one bit-length removed, since two

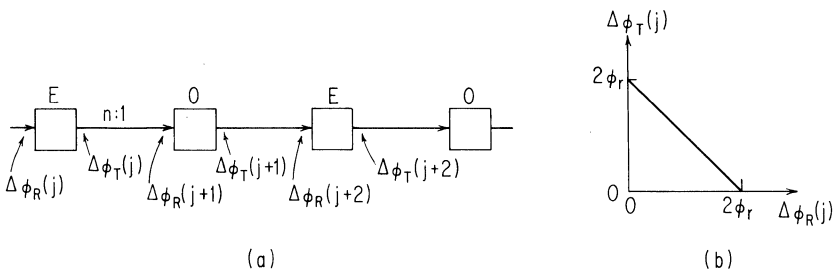


Fig. 8-1. Negation transfer: the transfer chain of (a) is composed of stages having the basic $\Delta\phi_T - \Delta\phi_R$ characteristic shown in (b).

negation transfers are logically equivalent to a simple transfer. However, there are some special properties of this double-negation mode of achieving transfer. In particular, flux clipping (or any other low-level loss mechanism) is not required, and the symmetry of the range maps is significantly altered.

Suppose that we introduce a gain mechanism by letting $N_T/N_R = n > 1$. Assuming a lossless loop, then provided the receiver is not saturated, that is, $\Delta\phi_R(j+1) < 2\phi_r$, we have

$$\Delta\phi_R(j+1) = n\Delta\phi_T(j) \quad (8-2)$$

Under these conditions, substituting Eq. (8-1) into Eq. (8-2) yields

$$\Delta\phi_R(j+1) = n[2\phi_r - \Delta\phi_R(j)] \quad (8-3)$$

which is plotted in Fig. 8-2(a). Note that for $\Delta\phi_R(j) \leq$ some value $\Delta\phi_a$, then $\Delta\phi_R(j+1) = 2\phi_r$ because of the saturation properties of the receiver. By substituting $\Delta\phi_R(j+1) = 2\phi_r$ into Eq. (8-3), the magnitude of $\Delta\phi_a$ is found to be $2\phi_r(n-1)/n$.

The overall transfer curve for two stages has the bistable form of Fig. 8-2(b), characterized by the equation

$$\Delta\phi_R(j+2) = n^2\Delta\phi_R(j) - n(n-1)2\phi_r \quad (8-4)$$

which is derived by extending Eq. (8-3) to the next stage. For $\Delta\phi_R(j) \leq \Delta\phi_a$, $\Delta\phi_R(j+1) = 2\phi_r$, and hence $\Delta\phi_R(j+2) = 0$. Similarly, for $\Delta\phi_R(j) \geq \Delta\phi_b$, $\Delta\phi_R(j+1) \leq \Delta\phi_a$, and therefore $\Delta\phi_R(j+2) = 2\phi_r$. Thus, with negation transfer we see that core saturation leads to bistable operation with just a linear gain mechanism, without the need for a subsidiary nonlinear loss mechanism.

In general, realistic negation transfer curves depart considerably from the straight-line characteristics of Fig. 8-2(a) and (b), being more like those of Fig. 8-2(c) and (d). The stable unity gain points at levels $\Delta\phi_c$ and $\Delta\phi_d$ are found by intersection of the single-stage transfer curve with its own reflection across the 45° line, as in Fig. 8-2(c).

Let us now consider the change in symmetry in the range maps with negation transfer. For the four-clock MAD-N scheme with simple transfer, we saw that there was essentially no upper limit on the clear currents. Plotting the allowed ranges of the two advance currents, we obtain a map that has a certain symmetry about the 45° line, as indicated in Fig. 8-3(a). An increase in $I_{E \rightarrow O}$ leads to increased gain on the $E \rightarrow O$ phase. This can be compensated

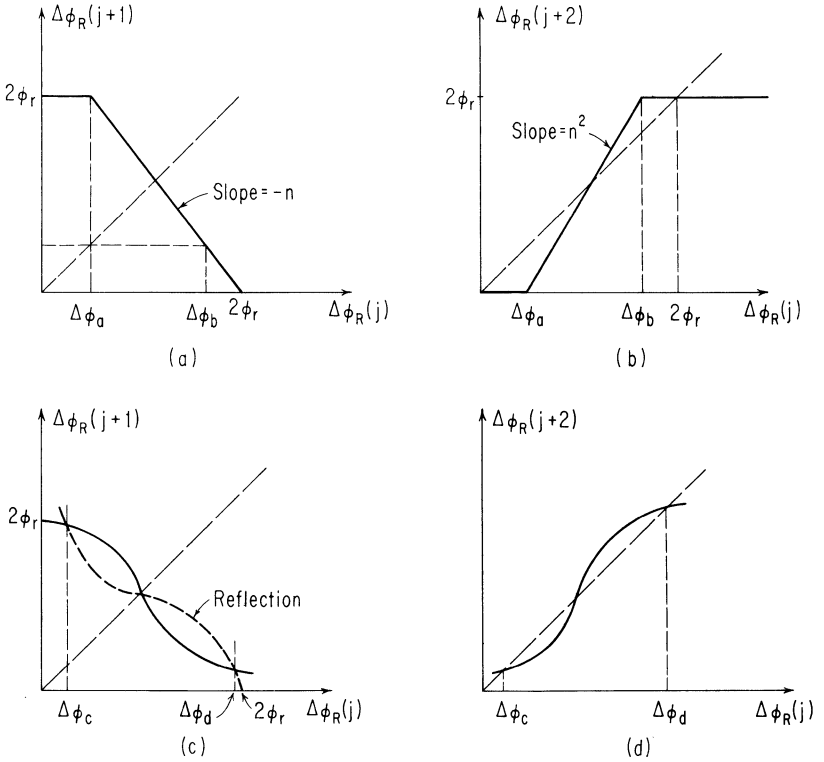


Fig. 8-2. Bistable flux-gain characteristic with negation transfer: (a,b) flux saturation in the basic transfer characteristic leads to bistable response in two transfers; (c,d) more realistic forms of response.

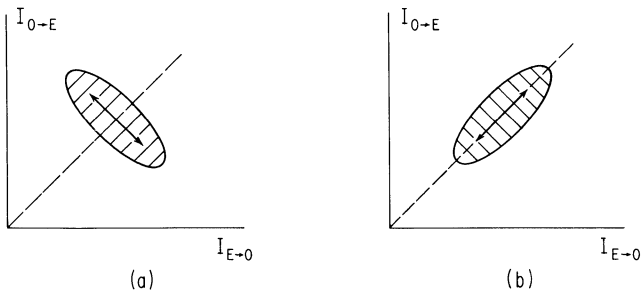


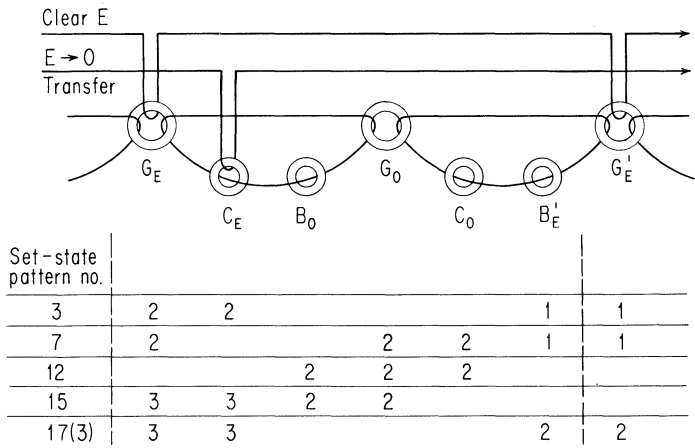
Fig. 8-3. Difference in range-map symmetry for (a) simple transfer, and (b) negation transfer.

by a corresponding decrease in $I_{O \rightarrow E}$, so that the overall transfer function for two stages preserves two stable levels. In other words, an increase in one current is compensated by a reduction in the other current, resulting in elongation perpendicular to the 45° line. The opposite effect occurs for negation transfer. Suppose that $I_{E \rightarrow O}$ increases. This results in an increase in the low level of flux transfer and a subsequent reduction in the high level of flux for the following transfer. To compensate, we must *increase* the following drive $I_{O \rightarrow E}$. Hence for negation transfer we obtain the orthogonal elongation of the range map shown in Fig. 8-3(b). This new symmetry could result in practical advantage, because with most driver arrangements the various clock pulse amplitudes tend to vary in the same direction in response to supply-voltage variations. Also, changes in core thresholds with ambient temperature generally call for a similar scaling in both driver currents, so that for a given set of clock drivers we can get a larger range of temperature operation for negation circuits without the need for compensation.

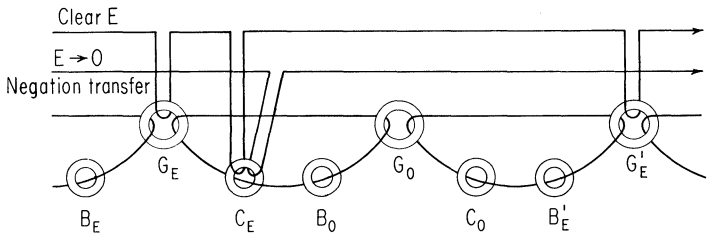
Driving the Transmitter to the Set State. Most schemes for simple transfer can be converted to negation transfer simply by driving the transmitter cores toward their *set* rather than *clear* states and reversing the polarity of coupling to the receiver cores. Then, if a transmitter core had previously been fully set by an incoming *one*, only a *zero* level of flux would be transferred; but if a *zero*, i.e., no flux, had been previously received, then the transmitter core would be set by the drive, causing the receiver core to set, i.e., to receive a *one*.

For example, Fig. 8-4(a) shows the Engelbart scheme with the appropriate sequence of set states from Fig. 7-8 tabulated below. In Fig. 8-4(b) is shown the negation version. Note that with a *one* initially in the *E*-stage, a *zero* is now transmitted to the *O*-stage during the $E \rightarrow O$ and clear-*E* phases. But if the *E*-stage initially stores a *zero*, then the setting of C_E (by the driver) causes G_O and C_O to be set, and the subsequent clearing of C_E causes Core B_O to be set, thus completing the same set-state pattern in the receiving group of toroids that would have existed after simple transfer of a *one*.

For typical four-phase schemes, the negation process can be repeated for each half bit-length of a transfer chain, thus resulting in double negation in each bit length. Except for the double-speed register of Fig. 7-12, all of the four-phase schemes described in previous chapters, when realized in toroid-wire form, can be



(a)



Start	$\Delta\phi_1$	$\Delta\phi_1$	$\Delta\phi_1$			
E \rightarrow 0	$\Delta\phi_1$	$\Delta\phi_1$	$\Delta\phi_1$		$\Delta\phi_0$	$\Delta\phi_0$
Clear E				$\Delta\phi_0$	$\Delta\phi_0$	$\Delta\phi_0$
0 \rightarrow E				$\Delta\phi_0$	$\Delta\phi_0$	$\Delta\phi_1$
Clear 0						$\Delta\phi_1$
						$\Delta\phi_1$

Note: Start with one in E; transfer zero to 0; end with one in E'.

(b)

Fig. 8-4. Comparison of flux-state sequences in corresponding simple- and negation-transfer schemes: (a) Englebart scheme of Fig. 5-20(d); and (b) after conversion to negation transfer.

converted to negation-transfer schemes by this technique without requiring additional cores. But for realizations employing multileg cores, this conversion generally cannot be done without alteration of the core shape, because of the static flux-closure requirements. To see why this is so, consider the multileg MAD-N scheme in

network form (Fig. 8-5), but with the $E \rightarrow O$ drive source shown in a direction to set Branch C_E for negation transfer on the $E \rightarrow O$ phase. According to this method it is also necessary to reverse the elements to the right of the dashed line; however, it is impossible to reverse the reference state of D_E without also altering the reference state of G_E or C_E , since these three branches connect at a physical node. Hence, to achieve negation with this scheme we must derive an alternate form of multileg core, which we now consider.

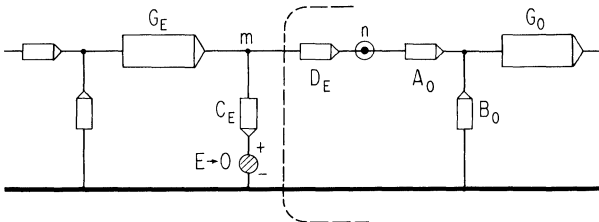


Fig. 8-5. Conversion of the MAD-N scheme of Fig. 5-19 to negation requires reversal of drive and reversal of element orientation to the right of dashed line.

For negation transfer, the reference states of the legs adjacent to the input and output apertures must be as shown in Fig. 8-6(a). To satisfy the flux closure requirements, we insert a cross leg F , as suggested by the dashed lines, which is held against actual switching. (An actual holding mmf would not be required if the cross leg F had a sufficiently high threshold.) In this way, any flux switched through the input leg A_E is forced to switch through Leg C_E .

The corresponding network for this new magnetic circuit is shown in Fig. 8-6(b). The main leg G_E is in effect divided into two parts, labeled G_1 and G_2 . With this arrangement, the net flux through G_2 , in the cleared state, is zero. Since an unsaturated region can lead to soft-threshold problems, Leg G_2 should be made as short as possible, i.e., the crosspiece should be moved close to the output aperture.

In Fig. 8-6(c) is shown an alternative arrangement that overcomes the soft-threshold problem by providing a separate Branch G_3 for flux switching, while utilizing single-width Legs G_1 and G_2 for satisfying flux-closure requirements. A direct physical realization of this element is shown in Fig. 8-6(d), where it is assumed that Legs G_1 and G_2 are held in their clear states at all times.

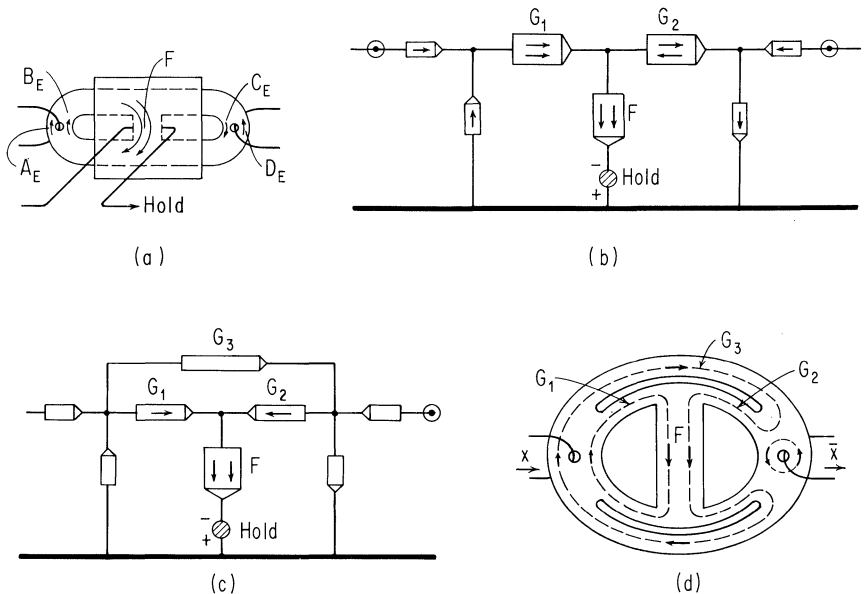


Fig. 8-6. Alteration of the basic multileg core shape to permit the required reversals of Fig. 8-5 for negation transfer.

In terms of the device of Fig. 8-6(d), it is correct to think of the logical operation of negation as taking place within the multileg core itself. Note that this same core can be used for simple transfer by reversing the clear state of Leg G_2 and still holding Legs G_1 and G_2 clear, resulting in zero net flux in Leg F .

Negation by Use of a ϕ or $\Delta\phi$ Source. In the method just considered, a transmitter core, driven in the set direction, switches only if it has previously received a *zero*. An alternate method is to drive a transmitter core to its clear state, as for simple transfer, but to incorporate in the coupling loop a suitable voltage source $v(t)$ with polarity to oppose the transmitted signal, as indicated in Fig. 8-7(a) for the configuration of Fig. 8-4. As in the previous method, the polarities of the receiver cores (but not of the $E \rightarrow O$ drive) are reversed. Thus, at $E \rightarrow O$ time, if the transmitter has received a *one*, its flux-linkage signal cancels the integrated value of $v(t)$; if it had received a *zero*, the new source sets the receiver cores G_0 and C_0 to the *one* state, and negation transfer is thus accomplished. For completing the cycle, the source is required to provide a voltage of the opposite polarity at the next clock phase

(Clear E), either to balance the emf due to the clearing of G_E or to cause setting of B_O , depending upon whether G_O had received a *zero* or a *one*, respectively.

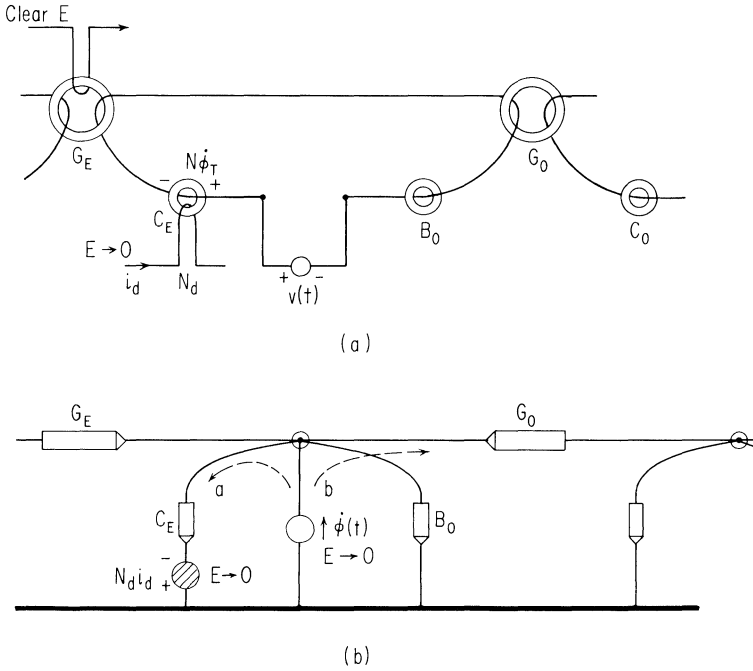


Fig. 8-7. Use of a $\dot{\phi}$ or $\Delta\phi$ source for negation transfer.

The network representation for the circuit of Fig. 8-7(a) is shown in Fig. 8-7(b), where the voltage source is represented by a $\dot{\phi}$ source that injects flux at a specified rate into the node representing the coupling loop. By use of preferential biasing during $E \rightarrow O$ transfer, such that the effective threshold of Branch G_O is less than that of Branch G_E but more than that of Branch C_E , the mmf drive in series with Branch C_E may be eliminated, and the $\dot{\phi}$ source will cause switching in the paths *a* or *b* depending upon whether C_E is set or cleared, i.e., contains a *one* or *zero*, respectively.

Let us return again to the network of Fig. 8-5, where it was found that the first method of converting to negation transfer could not be applied without changing the form of the multileg cores. Note that to replace the mmf generator in series with C_E by a $\dot{\phi}$

generator in parallel with C_E , that is, connected to Node m , would require a synthetic node. However, by sliding the $\dot{\phi}$ generator to the other side of Branch D_E , that is, to Node n , and by reversing all branches to the right of Node n , we can achieve exactly what is desired, as shown in Fig. 8-8(a). (This network is seen to be exactly the same as that of Fig. 8-7 except for insertion of Branches D_E and A_O .) The circuit realization of the network of Fig. 8-8(a) is shown in Fig. 8-8(b). With this method we can thus achieve negation transfer with the same multileg elements as previously used for simple transfer, but we must have means for providing a suitable voltage source or $\dot{\phi}$ source. In the case of a voltage source, it must be energized for just the length of time needed to inject the proper amount of flux linkage (measured in terms of volt-seconds). To eliminate this additional requirement, the voltage source can be replaced by a $\Delta\phi$ source that injects just the desired amount of flux linkage. An unconditionally driven toroid can serve as such a source, in which case the network takes the form of Fig. 8-8(c), with the corresponding circuit of Fig. 8-8(d).

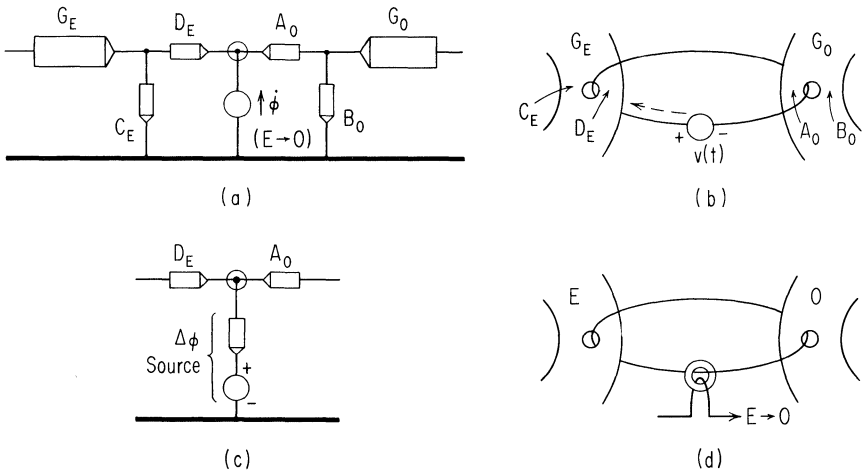


Fig. 8-8. Applying a $\dot{\phi}$ or $\Delta\phi$ source for negation transfer with minor-aperture input and output.

Conversion of the MAD-R scheme of Fig. 8-9(a) to negation, by the two methods discussed, is summarized in Fig. 8-9(b) and (c). With both methods applied in conjunction, as indicated in Fig. 8-9(d), the effect is double negation in two phases (Prime O followed by $O \rightarrow E$), resulting in simple transfer as the net effect in transferring from an O to an E stage, or from an E to an O stage.

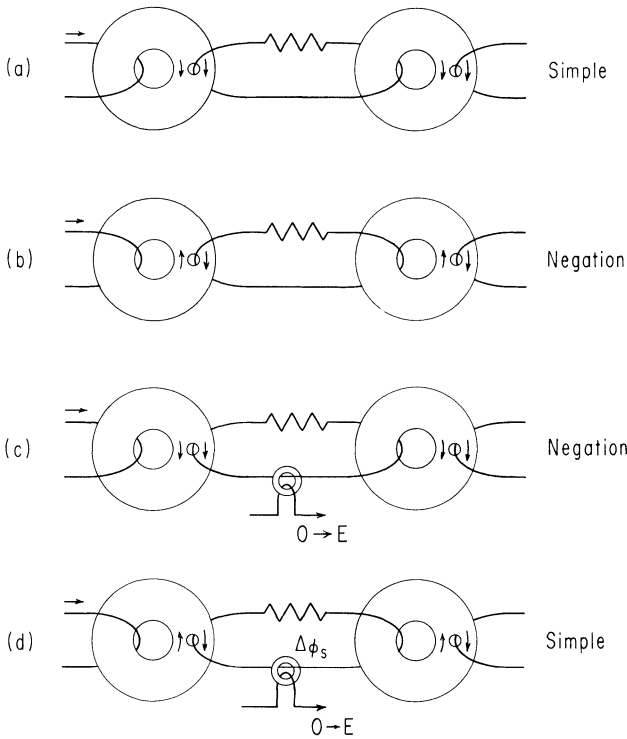


Fig. 8-9. Summary of transfer methods: (a) simple transfer; (b) negation transfer by driving to the set state; (c) negation transfer by use of a flux source; (d) simple transfer by simultaneous application of both negation transfer techniques.

In Secs. 8-3 and 8-4 we discuss other ways that $\Delta\phi$ sources can be employed in achieving simple transfer. In Chap. 10, we show how $\Delta\phi$ sources can be used not only for NEGATION synthesis, but for synthesizing many other logic functions as well.

8-2 Engelbart Orthogonal-Mode Technique

It can be instructive and helpful to study the switching characteristics of certain modes of a magnetic system, where a mode involves the interaction of two or more cores, in addition to the switching dynamics of individual toroids or core legs. To illustrate the method of modes as described by Engelbart (1963), consider the two-toroid circuit of Fig. 8-10(a) for which we define the two modes as the flux linkages $\lambda_a = \phi_1 + \phi_2$ and $\lambda_b = \phi_1 - \phi_2$

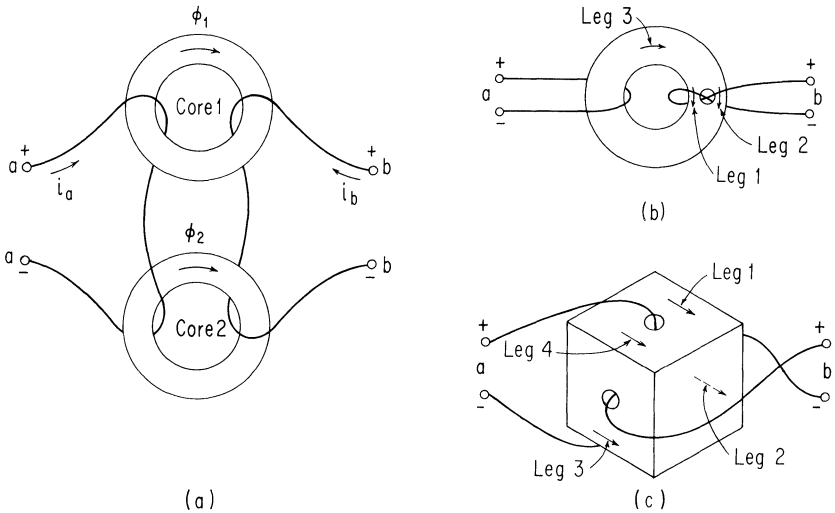


Fig. 8-10. Orthogonal modes in: (a) a pair of toroids, (b) a multileg core, and (c) a Biax element.

(for simplicity we assume every winding to have a single turn). Assuming zero-impedance coupling loops, $\Delta\lambda_a$ is the time-integrated voltage across terminals $a-a$, and $\Delta\lambda_b$ is the time-integrated voltage across terminals $b-b$. For a voltage V applied across terminals $a-a$ for an interval T , then $\Delta\lambda_a$ is simply equal to VT no matter how ϕ_1 and ϕ_2 change individually. If ϕ_1 and ϕ_2 change identically, then $\Delta\lambda_b = 0$, and the modes are said to be orthogonal; otherwise $\Delta\lambda_b \neq 0$. In other words, the modes represent the terminal characteristics. Given λ_a and λ_b , we can immediately solve for ϕ_1 and ϕ_2 , and vice versa.

The situation may be summarized in the plot of Fig. 8-11 in which mode axes λ_a and λ_b are superimposed on the ϕ_1, ϕ_2 axes. Suppose we start at some initial point A and trace the trajectory ABC . A positive voltage applied to terminals $a-a$ of the Mode- a winding generates a positive current i_a that causes the necessary flux switching. Assuming a constant- ρ model, so that both cores switch at the same rate, then the induced voltages cancel in the Mode- b winding, though they add in the Mode- a winding. As long as the switching is symmetrical, there is no change of state in Mode b as Mode a increases its flux along the path AB . At Point B , however, Core 1 saturates ($\phi_1 = \phi_r$), and Mode a obtains all of its additional flux from Core 2. With only one core switching, equal

(but opposite) voltages appear at the two mode-winding terminals as flux switches along the path BC.

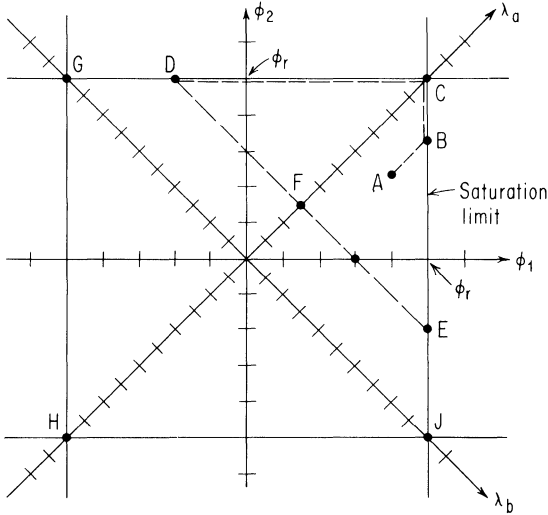


Fig. 8-11. Relation between core flux values ϕ_1 and ϕ_2 and mode flux values $\lambda_a = \phi_1 + \phi_2$ and $\lambda_b = \phi_1 - \phi_2$.

At Point C, both of the cores 1 and 2 are saturated in their positive directions; Mode a is saturated in its positive direction ($\lambda_a = 2\phi_r$) and Mode b is at the midpoint of its range, that is, $\lambda_b = 0$. Switching either core to the opposite saturation limit would send Mode b to one of its limits, and Mode a to its midpoint.

Now we turn our attention to Fig. 8-10(b) and the multileg realization of the two-mode system. We have labeled three legs in this figure, but the flux displacement in the three legs is not independent, since $\phi_3 = \phi_1 + \phi_2$. If we consider Legs 1 and 2 as independent, and express the modes as $\lambda_a = \phi_1 + \phi_2$ and $\lambda_b = \phi_1 - \phi_2$, we find that Fig. 8-11 is directly applicable, where Mode a represents the flux encircling the major aperture and Mode b represents flux encircling the minor aperture. Note that two turns link the minor aperture as opposed to one through the major aperture and that flux switches in Mode b with considerably lower current than for Mode a. The familiar characteristics of cores with minor apertures are easily derived from Fig. 8-11 if it is kept in mind that any switching of λ_a takes considerably more mmf than for λ_b . For example, suppose that Mode b is excited at an mmf level intermediate between the switching thresholds for the two modes.

If the system state is at Point C , that is, the core is in its clear state, no displacement in Mode b can occur, because a similar displacement would be required in Mode a , which the mmf is too small to permit. But if some larger mmf in either mode causes a displacement in Mode a , say to Point F (that is, major-aperture switching) then Mode b can be independently switched back and forth between the saturation limits at D and E .

In the Biax core (Wanlass, 1959) of Fig. 8-10(c), there are four directly linkable legs, assuming that the two orthogonal apertures intersect. However, flux-closure constraints demand that the displacements of all four legs sum to zero, which reduces the number of independent variables to three. Further, if the core and its switching characteristics are symmetrical, the fact that the mmf from Modes a and b act in equal but opposite manner upon Leg 1 and Leg 3, and in equal but opposite manner upon Leg 2 and Leg 4, adds one more independent equation (either $\phi_1 + \phi_3 = 0$ or $\phi_2 + \phi_4 = 0$). Therefore, when driven by the windings shown, the Biax flux state is completely characterized by $\phi_1 = -\phi_3$ and $\phi_2 = -\phi_4$, and we find again that $\lambda_a = \phi_1 + \phi_2$ and $\lambda_b = \phi_1 + \phi_4 = \phi_1 - \phi_2$. Figure 8-11 is then seen to characterize the Biax core with symmetrical characteristics as qualitatively identical to the toroidal-core system of Fig. 8-10(a).

Nonideal Orthogonality: The Threshold Burden. Current in a given mode winding causes an mmf in the system. This mmf can be considered on the flux plane of Fig. 8-11 as a force vector trying to move the flux-state point parallel to the mode axis. Current in the other mode winding causes a similar vector parallel to the other mode axis. In a truly orthogonal system, not only would the mode axes be geometrically orthogonal, but the movement of the flux-state point in response to any resultant mmf vector would be exactly parallel to that vector (assuming that we have not reached a saturation-limit boundary). All of the nominally orthogonal magnetic systems depart from this ideal for two reasons, both of which stem from nonlinear switching characteristics of the individual legs. The first reason is associated with the threshold mmf for flux switching, and the second is due to the actual nonlinearity of core switching resistance. To understand the first effect, consider the system of Fig. 8-10(a). The mmf F_1 acting on Core 1 is $i_a + i_b$, and the mmf F_2 is equal to $i_a - i_b$. A necessary condition for any flux switching in Core 1 or Core 2 is that the absolute value of F_1 or F_2 , respectively, be greater than threshold F_0 . Thus, a necessary condition for any switching to occur in either one of the cores is

that

$$|i_a| + |i_b| > F_0 \quad (8-5)$$

If only one core is switching, then both modes are switching simultaneously with the same absolute magnitudes of λ . To have one mode switching more than the other one, it is necessary that both cores be switching simultaneously, and for this we have the additional necessary condition

$$\left| |i_a| - |i_b| \right| > F_0 \quad (8-6)$$

Based on these conditions on mmf, it is readily seen that whenever the two modes have different switching rates, the one with the larger absolute value of λ must carry the entire mmf burden of bringing the two cores up to threshold plus the switching increment in excess of threshold. The low- λ mode need essentially provide only the mmf required to "steer" or redistribute the relative amount of ϕ in the two cores. On the flux-plane of Fig. 8-11 this mmf burden skews the total λ vector away from the total mmf vector, toward a horizontal or vertical axis. This effect can produce a rather marked dependence of the current required in one mode (to yield a given λ) upon the concurrent switching rate of the other mode. For example, a strong dependence will be found in both of the symmetrical systems of Fig. 8-10(a) and (c), though for the asymmetrical multileg core system of Fig. 8-10(b), it is only the burden of the threshold mmf around the small aperture that is passed back and forth to whichever mode has the higher λ , and the effect is not so noticeable.

Nonideal Orthogonality: Variable Switching Resistance. The second effect stems from the variation of switching resistance with change in flux state. Based on the more realistic parabolic $\phi(\phi)$ model (derived in Sec. 12-5), we find that a core whose flux state is nearer its zero value yields a greater ϕ for a given mmf. In general, therefore, if a flux-state point is subjected to a switching mmf from one of the modes, the switching trajectory will project a λ component onto the undriven-mode axis. (The only exception is a flux-state point lying on one of the mode axes and being driven in that same mode. We will see in the next section that it is just this condition that is important in dynamic bias.) Thus, even if the threshold burden were carried by an outside mmf source, the λ vector resulting from a given mmf vector (resultant of the two separate mode mmf) is not generally parallel to the mmf

vector, and thus the two modes do not have truly independent switching characteristics.

Nonorthogonal Modes; MAD-R Example. The above deviations from truly orthogonal modes can often be tolerated when the coupling between modes can be countered by mmf that are smaller than the threshold mmf of some critical, associated flux path. Going further, the same threshold effects allow the use in some circuits of modes that are not even nominally orthogonal. An example is the arrangement of Fig. 8-12(a), in which an output winding links only a single output leg. Here $\lambda_a = \phi_1 + \phi_2$ and $\lambda_b = \phi_2$, and the mode axes, rather than being orthogonal, are skewed, as in Fig. 8-12(b), where the trajectory *GHIG* for the MAD-R scheme (Chap. 6) is traced. During the input phase, we switch Mode-*a* flux. Without other constraints, this would result in a change in Mode-*b* flux as well, since flux tends to switch on both sides of the output aperture. But current in the very low-impedance output circuit prevents any significant Mode-*b* switching, and the operating point of Fig. 8-12(b) moves orthogonally to Mode *b*, from *G* to *H*. Priming moves the operating point orthogonally to Mode *a*, from *H* to *I*. Clearing finally switches flux in both modes simultaneously.

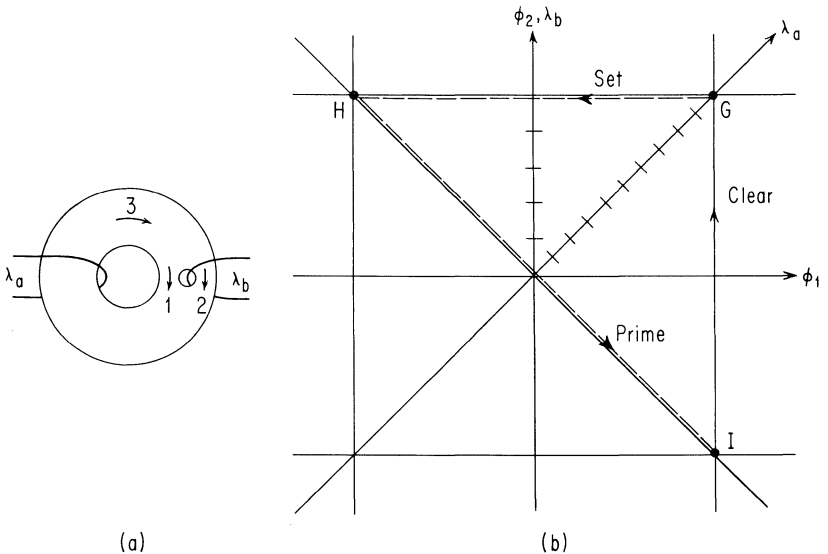


Fig. 8-12. Mode plot for the MAD-R scheme.

Engelbart Orthogonal Scheme. It is not possible to build a non-resistance transfer scheme with the simple two-mode (orthogonal) arrangement of Fig. 8-13(a) as the basic stage to be iterated, for the following reason. To receive a certain magnitude of linkage $\Delta\lambda_{in}$ without forward coupling, both cores would be set at identical rates. To transfer out of the pair, without backward coupling, both cores would be driven at equal and opposite rates, but then it would be impossible to clear the pair without intolerable coupling, both forward and backward.

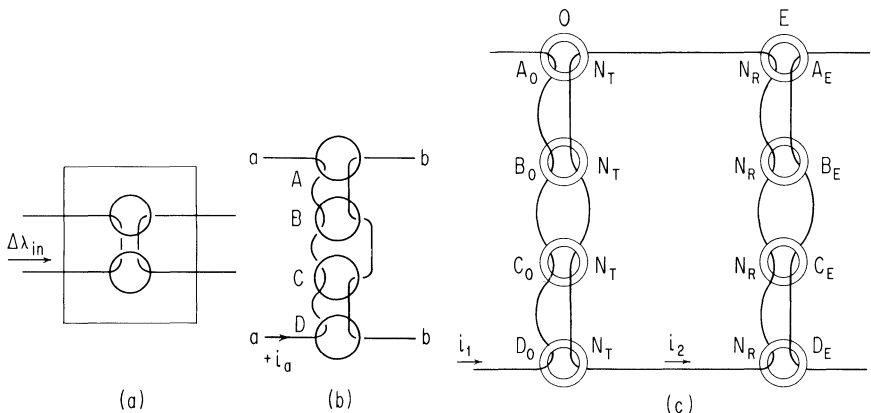


Fig. 8-13. Engelbart orthogonal-mode scheme.

One way to satisfy the decoupling requirements is to arrange two two-mode circuits, as in Fig. 8-13(b). Assume each core in this figure is cleared to a clockwise flux state. An input current $+i_a$ sets Cores A and B at the same rate, and there is zero forward transfer. A subsequent current $-i_a$ switches Cores C and D, also at the same rate, again with no forward transfer. Forward transfer is also a two-step process—Cores A and C being cleared first, and then Cores B and D—with no back transfer in either case.

Iterating the arrangement of Fig. 8-13(b), Engelbart (1963) developed the nonresistance transfer scheme of Fig. 8-13(c), which has the particularly interesting feature of containing only doubly-linked (coupling) cores. The basic operation can be summarized as follows. A binary *zero* is represented by nominally zero flux switching, typical of unipolar schemes. For the case of a binary *one*, let us assume that all four toroids of the O stage have been set. An $O \rightarrow E$ pulse clears A_0 and C_0 , which results in a positive i_2 that sets cores A_E and B_E . Orthogonality ensures no back trans-

fer from the O stage or forward transfer from the E stage. The Clear- O pulse now clears Cores B_0 and D_0 , resulting in a negative i_2 that sets C_E and D_E again with orthogonal isolation. Thus, the O cores are cleared and the E cores set, and the cycle is completed with an $E \rightarrow O$ pulse followed by a Clear- E pulse.

The network representation of this scheme takes the form of the lattice of Fig. 5-11, redrawn in Fig. 8-14, and on which the switching paths noted above are easily traced. Starting with all cores of the O stage having been set, as illustrated by the internal arrows, the $O \rightarrow E$ and Clear O operations have the symmetrical switching paths shown in Fig. 8-14(b). The paths for subsequent $E \rightarrow O$ and Clear- E switching are similar, but displaced one stage along the register.

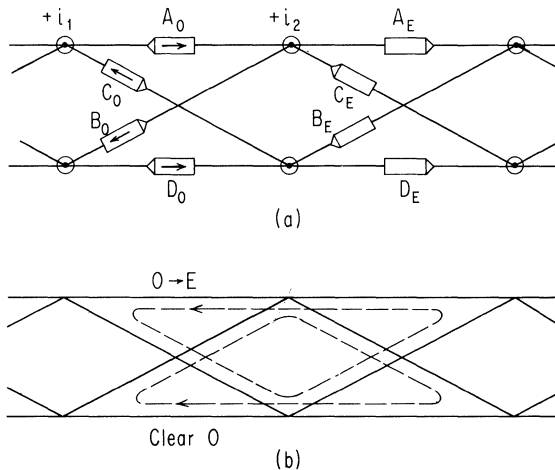


Fig. 8-14. Network representation of the orthogonal-mode scheme.

We thus have a scheme configuration that is different from any that we have previously discussed, namely, a configuration that involves only coupling cores. Pursuing the orthogonal coupling technique further, we will later find still a different configuration in the bipolar, orthogonal-mode, thin-film scheme of Sec. 9-2.

8-3 Dynamic Bias

Besides the requirement of driving a transmitter core in order to achieve flux transfer, we have seen that it is generally necessary in the case of nonresistance schemes, and sometimes desirable in

the case of resistance schemes, to bias receiver or other cores towards the *set* state. For example, in the scheme of Fig. 7-6, redrawn in Fig. 8-15, suppose we start with a binary *one*, i.e., a set-state pattern, stored in Cores V, W, and X. On the next phase, V and W are driven clear, inducing loop currents i_1 and i_2 . Positive bias is applied to Core X, to prevent it from being unset by i_1 , and to Core Z to lower its effective threshold relative to i_2 . If these two cores are biased exactly to threshold, and if the drive is limited so that i_1 comes just short of unsetting Core X, then this condition results in the largest possible value of i_2 , which supplies the excess mmf for switching the receiver core Z.

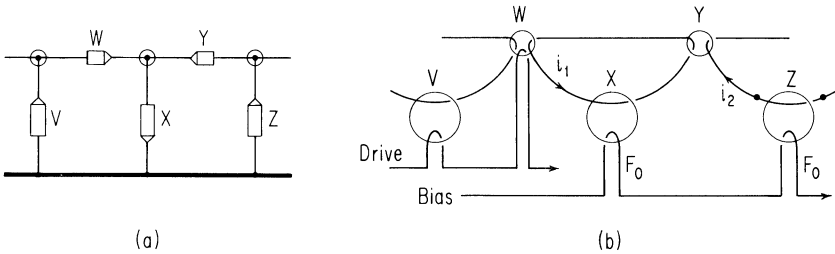


Fig. 8-15. Applying bias to the transfer scheme of Fig. 7-6.

Now consider the nature of the circuit tolerance for reducing the drive below this maximum value. If the bias line is pulsed in series with the drive line, then not only do loop currents decrease with drive, but they must now provide part of the threshold of Core Z, resulting in a still greater decrease of excess mmf acting on Core Z. For typical wire-resistance values, relative loop losses increase rapidly as loop currents, and therefore core switching rates, decrease. Under these conditions, the lower end of the current range is reached quickly as drive is decreased.

To increase the operating range, what is sought is a bias technique that can effectively maintain full-threshold bias over a range of bias mmf. The clue to this achievement is provided by the orthogonal-mode analysis of Sec. 8-2, where it was found that when one mode of an orthogonal pair is switching more rapidly than the other, the entire threshold burden is supplied by the current driving the former mode, and the current for the slower-switching mode acts entirely as excess mmf. Thus let us consider replacing the receiver core Z in Fig. 8-15(b) by the pair of orthogonally linked cores of Fig. 8-16(a). Corresponding to the terminology used in

Sec. 8-2, we define Mode *a* relative to the bias windings and Mode *b* relative to the coupling-loop windings. To guarantee that Mode *a* carries the entire threshold burden, the bias current must be set somewhat greater than threshold. Thus for the case of $i_2 = 0$ (nominally so for zero transfer), the cores *Z* and *Z'* switch equally, and there is no coupling into the loop, i.e., no Mode-*b* switching. During one transfer, $i_2 > 0$ and therefore $\dot{\phi}_Z > \dot{\phi}_{Z'}$ (ideally, $\dot{\phi}_{Z'} = 0$).

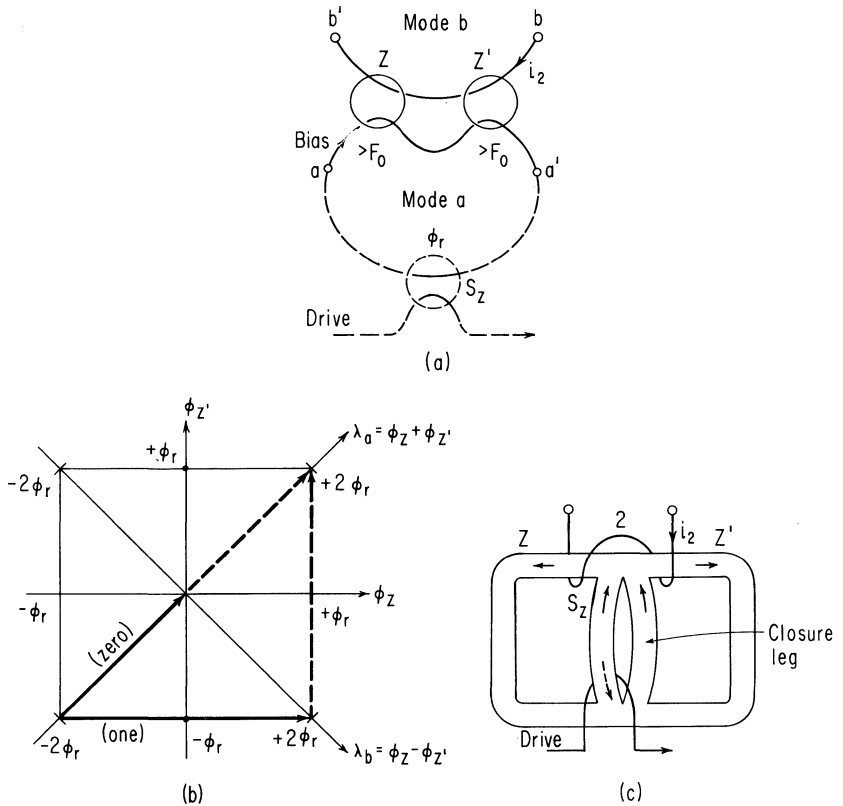


Fig. 8-16. A pair of orthogonally connected cores for purposes of applying dynamic bias in (a); its mode-plot representation in (b); and a single equivalent multileg core in (c).

The amount of flux-linkage signal stored in the *Z*-pair is the difference $\Delta\lambda_Z = \Delta\phi_Z - \Delta\phi_{Z'}$, and it is this amount of flux-linkage that is available for later transmission. Because the bias current causes switching in both receiver cores, regardless of binary state, it is commonly termed *dynamic bias*.

Note that if the bias current continues to switch flux after the loop current has terminated, we have the danger that both cores may be forced to positive saturation, thus forcing the difference component, i.e., the signal, to zero. To better see what may happen, consider the mode plot of Fig. 8-16(b). The *signal mode* $\Delta\lambda_b$ for a *one* is the distance perpendicular to the λ_a axis in the direction of positive λ_b . It is seen that this can have a maximum value of $2\phi_r$ in the case where the change in the *common mode* $\Delta\lambda_a$ is also just equal to $2\phi_r$. The solid arrows, terminating on the λ_b axis, indicate the desired changes for *zero* and *one* transfer (in the latter case only Core Z would switch). But if the bias current is not terminated, then switching will continue along the dashed lines, forcing the states for *zero* and *one* to come closer together, yielding a smaller $\Delta\lambda_b$, as the maximum point on the positive λ_a axis is approached.

Limiting with a $\Delta\phi$ Source. The answer to the above problem is that the bias current should be derived from a flux source of capacity exactly equal to $2\phi_r$. This could be applied from a voltage source V energized for a period $\tau = 2\phi_r/V$, though, as suggested in Fig. 8-8, a more practical way is simply to use another core, having the same flux capacity as each Z core. Such an arrangement is indicated by the dashed circuitry of Fig. 8-16(a), where the drive on the source core S_Z can vary over quite a range and still cause proper dynamic biasing of the Z cores. Incorporation of flux limitation makes dynamic bias a valuable technique. Thus, we see another use of a $\Delta\phi$ source in addition to those described in Sec. 8-1. This technique of flux-limited dynamic bias was first applied to a unipolar scheme by Heckler and Baer (1964).

By network transformation, the triplet of cores Z, Z', and S_Z can be converted to the single multileg core of Fig. 8-16(c), a basic core shape devised by Newhall (1963) for use in bipolar circuits (Sec. 9-1). The *clear* state is shown by the solid arrows. (Note that it has been necessary to add an extra leg for proper flux closure.) For receiving a *zero*, the flux reversed in the source leg S_Z (dashed arrow) switches equally (ideally) through the two outside legs; for *one* reception, flux switches predominantly through the left-hand leg.

If each loop core in Fig. 8-15 is replaced by a triplet of cores, the circuit of Fig. 8-17 is obtained. To transfer from Cores V and W to Cores Y and Z, we clear Source Core S_V and set Source Core

S_Z , but do not apply dynamic bias to the X cores, since we do not wish switching to occur in either one. However, there is even less need now for biasing the X cores, since the operating loop currents tend to be lower with dynamic bias on the Z cores, and in fact some unsetting can even be tolerated, provided the coupling loop turns ratio is >1 . Nevertheless, it is still possible to supply ordinary bias to the X cores, as indicated by the dashed line, as a possible means of improving the circuit performance still further. We can also improve the transfer by unconditionally clearing Coupling Core W as well as Loop Cores V and V' , as suggested in the figure. (This assures good return to the clear state.) In the circuit, as shown, the current i_1 must still overcome the threshold of Core Y , but the coupling cores may be made small compared to the loop cores. (In Sec. 9-1, we will take the additional step of also replacing each coupling core by a dynamically biased pair of cores, and we will then find that a radically different type of behavior is obtained.)

To summarize to this point, a general way for incorporating dynamic bias is, first, to start with the scheme in toroidal-core form. Second, each toroid selected for dynamic biasing (generally including all the larger ones) is replaced by a pair of orthogonal-mode cores connected to a third core acting as a flux source, as in Fig. 8-17. If such a core is a coupling rather than a loop core, then the pair of cores is linked by both input and output windings in the same mode as well as a winding from the source core in the orthogonal mode. Third, network methods are then used to transform the circuit from the all-toroidal form to whatever other form may be desired.

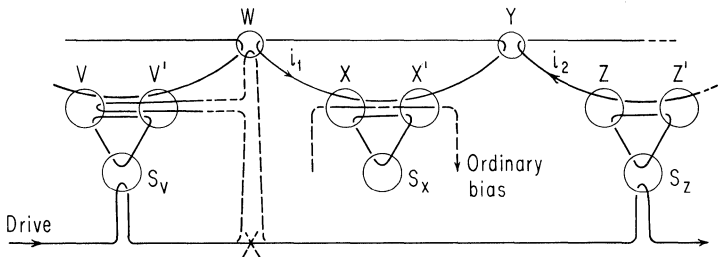


Fig. 8-17. Using the orthogonally connected core pairs of Fig. 8-16 to replace all of the loop cores in Fig. 8-15, for purposes of applying dynamic bias.

The manner of achieving dynamic bias has been described in terms of a particular scheme but, like the conversions to negation

transfer in Sec. 8-1, it is generally applicable to all of the schemes earlier described, including the resistance types.

Dynamically Biased MAD-R. For the MAD-R scheme (Chap. 6), which already exhibits very good range, the benefit to be expected from dynamic bias is higher speed. A straightforward way to incorporate dynamic bias in MAD-R is to start with the toroid-wire equivalent of Fig. 6-5(a), sketched again in Fig. 8-18(a). To overcome the threshold of the large cores with dynamic bias, we replace each of these by triplets as shown in Fig. 8-18(b). The remaining part of the problem is to convert this circuit to a practical form using multileg cores. The magnetic-network transformation methods of Chap. 5 are very useful in making this conversion.

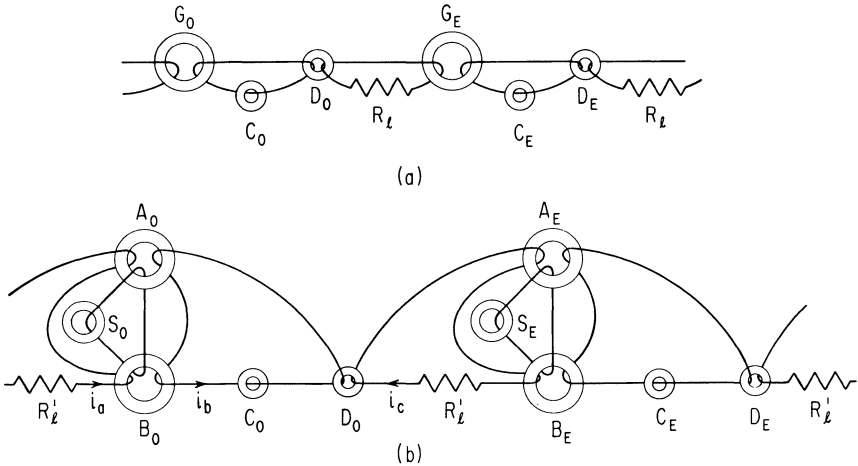


Fig. 8-18. Applying dynamic bias to the main elements of the MAD-R circuit.

Inclusion of the flux-source cores (\$S_0\$ and \$S_E\$) in the transformation results in undue complication; hence we leave them out of consideration for the moment, but they will have to be restored in the final circuit after the conversion is otherwise completed. We also assume single-turn coupling loops, so that we will have to restore turns ratio >1 after the conversion also. With these items in mind, we now proceed to construct a network representation for the circuit of Fig. 8-18(b).

Each of the coupling loops of Fig. 8-18(b) is represented by a node pair in Fig. 8-19(a), with the loop current appearing as the associated mmf potential difference. Each toroid is represented

by a single branch or pair of equal branches attached to the nodes in such a way that the mmf acting on each branch or branch pair are equal to the mmf imposed on the toroids by loop currents. For example, the total mmf in series with the D pair of branches is $i_c - i_b$, as required. Some of these nodes must be converted to physical nodes (representing core junctions) in order to obtain a realization using multileg cores. Let us replace the synthetic nodes to which the C branches are attached by physical nodes. The nodes to which resistance is attached must of course remain synthetic. All the branches between the a and c node pairs can now represent legs of one multileg core; the branches with E subscripts represent the next multileg core; etc.

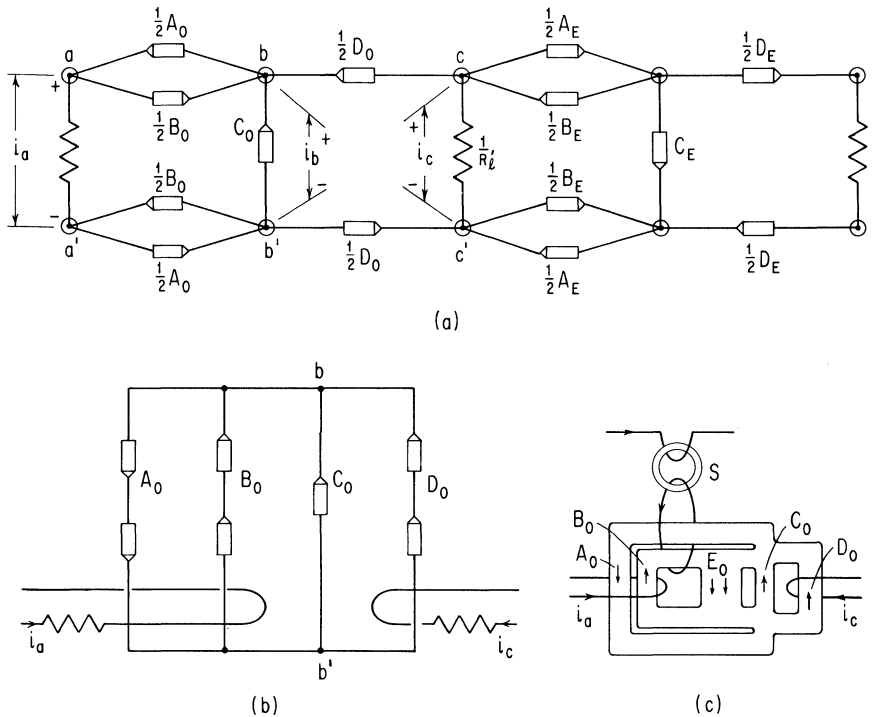


Fig. 8-19. Converting to a multileg version of the dynamically biased toroid circuit of Fig. 8-18(b).

The reverse transformation, from network to circuit form, amounts to rejoining the a and a' ends of the A_0 and B_0 branch pairs and the c and c' ends of the D_0 branch pairs, followed by restoration of appropriate coupling loops (Fig. 8-19(b)), except that

if all legs are interpreted as having the same width, the net clear-state flux does not sum to zero at each node, as required. A straightforward physical realization is shown in Fig. 8-19(c), in which an extra, double-width leg (E_0) has been added to provide the necessary flux closure.

Aside from the A and B legs being different in length, the core of Fig. 8-19(c) is a difficult one to make because of the long slot. A simpler version is the core of Fig. 8-20(a), with the B leg flipped to the other side. Further, by splitting the E leg in two halves, to be stretched out along the A and B legs, we obtain the even simpler core of Fig. 8-20(b), to which a toroidal flux source is shown connected. This design at first looks poor since the entire right-hand leg remains in a soft-state after clearing. However, with dynamic bias present, good advance current range can be retained and the main effect of the soft state is a moderate reduction of the upper limit on priming current (applied to Legs C and D in figure-eight fashion, though not shown here).

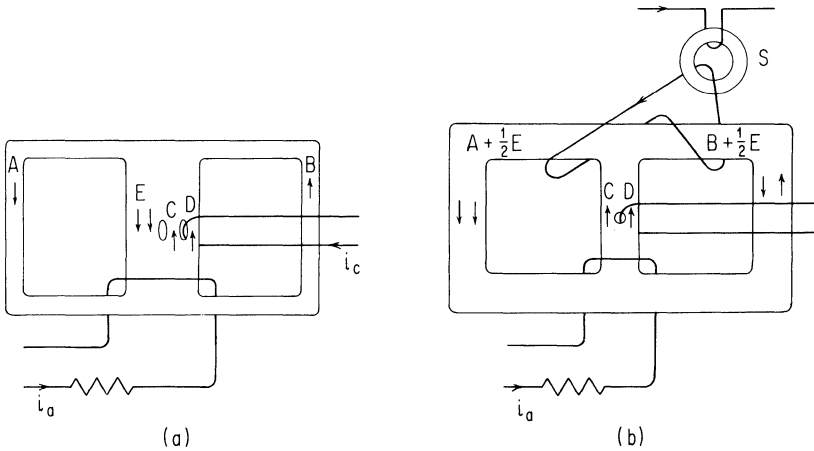


Fig. 8-20. Alternate forms of multileg cores for the dynamically biased version of MAD-R.

Laboratory results with experimental cores of the type shown in Fig. 8-20(b) have shown that unity gain can be obtained with a coupling-loop resistance several times higher than in the basic MAD-R scheme, with a corresponding ratio of improvement in priming speed of about 3 to 1 (unpublished notes of W. K. English of Stanford Research Institute). This result illustrates the higher-speed potential of dynamically biased resistance-type circuits.

8-4 Summary

In this chapter, we first discuss techniques for achieving negative transfer, by which we mean transfer of a high level of flux if a low level had previously been received, and vice versa. One technique involves the specific use of flux-source cores in the coupling circuitry. Though negation transfer is important for general logic synthesis, the main interest here is the derivation of basically different flux-transfer methods. We then develop the notion of orthogonal modes of flux transfer, where we consider the state of flux in several cores at once rather than in each core individually. This is a useful and important concept not only for generating new transfer schemes, but also as a basic tool, as in the development of the dynamic-bias technique.

Previously, bias was employed as a means of bringing certain selected cores to their static switching threshold, with the bias itself causing no switching. We have here shown how an improvement in performance can be obtained by replacement of certain selected cores by orthogonally connected pairs of cores. These cores are driven from a flux-source core and switch unconditionally, but equally, when excited only by the drive current. The information-bearing coupling-loop currents then need be only large enough to "steer" or "tip" the switching, i.e., to cause a differential in switching rates of the two cores in a pair. The term *dynamic bias* is used to describe this type of technique.

In Chap. 9, we will extend the use of dynamic bias to achieve a completely symmetric circuit form in which the magnitude of flux transfer is uniform, but of one polarity or the other depending on the data state, referred to as a bipolar mode of transfer.

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With the unipolar representation used thus far a binary *one* is represented by a high level of flux transfer and a binary *zero* by nominally zero flux transfer. In an alternate representation, the binary states are symmetrically represented and binary transfer involves equal magnitudes of flux, of one polarity or the other. On the basis of this *bipolar* principle, many important new schemes can be evolved. A number of such schemes are developed in Sec. 9-1, some of which may have significant practical importance. We will see that the technique of dynamic bias developed in Chap. 8 is rather naturally adapted to use in bipolar circuits; in a sense, bipolar techniques are a natural step after dynamic bias.

In Sec. 9-2, several magnetic thin-film transfer schemes are considered. Of special interest is a distinctly different gain mechanism obtained from coherent rotation of magnetization in thin films, which makes thin-film components ideally adapted to bipolar operation. Because of the generally higher speed of thin-film components, the thin-film circuits typically operate at higher rates than the ferrite circuits; megacycle bit rates are not unusual, as we will see, for example, in the elegantly simple multimegacycle scheme of Dick and Farmer.

It becomes clear that unipolar and bipolar techniques do not exhaust the data representation possibilities when, in Sec. 9-3, we consider still another form referred to as non-return-to-reference (NRR). In an NRR scheme, not all cores are unconditionally driven to their reference state once each cycle, but rather, switching occurs only to signal a change in the bit pattern; i.e., no switching occurs during transmission of a string of *zeros* or a string of *ones*. One such scheme is described; although it is not of any particular practical interest, it has a basic elegance and is distinguished as the only two-phase core-wire circuit presently known to have been built and operated. It, too, is naturally adapted to the use of bipolar transfer.

9-1 Bipolar Schemes

Complete Dynamic Biasing: Newhall Scheme. By the procedure given in Sec. 8-3 for applying dynamic bias to a toroidal-core circuit, not all the toroids were replaced by dynamically biased pairs. But suppose we do attempt to use full dynamic biasing so that loop currents do not have to overcome even the minor thresholds of the small coupling cores. For example, let us also replace Cores W and Y in the circuit of Fig. 8-17 by such biased pairs, as shown in Fig. 9-1.

For transfer from the V cores to the Z cores, the V and W cores are unconditionally cleared and the S_Y and S_Z sources are activated, but not the S_X source. With exactly zero net flux transmitted from the clearing of the W pair, loop current i_1 is zero and there is only common-mode switching (in the sense defined in Sec. 8-3) in the Y pair, with no linkage to the forward or back coupling loops. However, if $\Delta\phi_w > \Delta\phi_w'$, the resulting flux linkage injected into the loop induces a $+i_1$ loop current, which causes transmission of signal-mode flux through the Y cores to the Z cores.

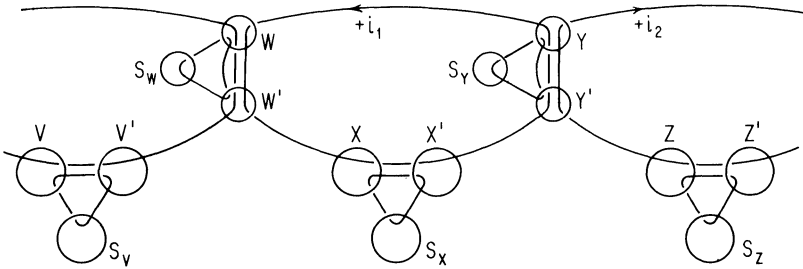


Fig. 9-1. Newhall bipolar scheme derived by dynamic biasing of all of the coupling cores and loop cores in Fig. 8-17.

With the threshold burdens and primary switching mmf provided by the sources, and with no flux-clipping introduced into the loop, the transfer ratio tends to be as high for low levels of signal as for higher levels. Hence, with a gain mechanism present, even a small signal will build up to a level limited only by core saturation, as indicated by Point *a* in Fig. 9-2(a). The really interesting point, however, is that with all cores other than sources occurring in symmetrical pairs, a negative value of flux linkage, resulting from $\Delta\phi_w < \Delta\phi_{w'}$, can be transmitted as readily as a positive value. Negative loop currents $-i_1$ and $-i_2$ will then flow, and this negative signal mode will cause Core *Z'* to be set by a larger amount than Core *Z*. The transfer curve for negative $\Delta\phi$ is therefore just the reflection of the positive curve through the origin, with a stable point *b* at the same magnitude of $\Delta\phi$ as the stable point *a*. By letting the positive level of $\Delta\phi$ at Point *a* represent a *one*, and the negative $\Delta\phi$ at Point *b* represent a *zero*, we have in effect a bipolar scheme.

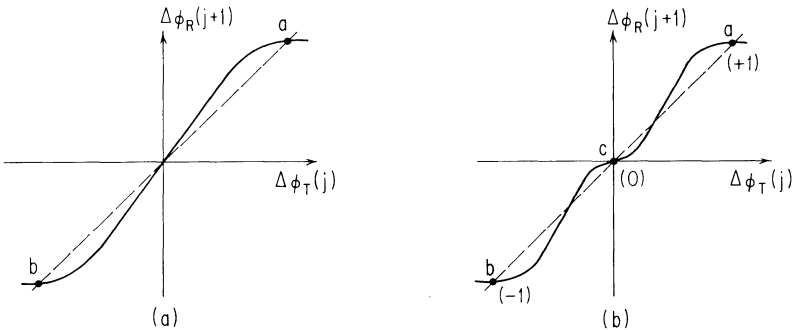


Fig. 9-2. Bipolar gain curve: (a) with no low-level loss mechanism, and (b) with a low-level loss mechanism leading to a third stable state.

In terms of the orthogonal-mode plot of Fig. 8-16(b), *zero* transfer is now represented by an arrow (not shown) veering off toward the negative end of the λ_b axis, symmetrical with the arrow shown going toward the positive end. Because of the full dynamic biasing, the symmetrical nature of the transfer curve, and the elimination of the need for clipping or some other low-level loss mechanism, even greater drive tolerances can be obtained for this circuit than for the dynamically biased unipolar circuit of Fig. 8-17.

For the present scheme, no biasing at all of the X cores is used during transfer to the Z cores. Actually, for a coupling-loop turns ratio of 2/1, it has been found experimentally that a considerable amount of signal-flux loss in the X cores can be tolerated, thus resulting in an even greater range of operation than originally anticipated.

The circuit of Fig. 9-1 is one form of the bipolar scheme described by Newhall (1963). Newhall also shows how this scheme may be realized in terms of cores of the general type shown in Fig. 8-16(c)—either taken individually, or themselves built into more compound structures to reduce the amount of wiring.

Modification for Ternary Operation. Suppose that all of the $\Delta\phi$ sources for the coupling cores (S_W, S_Y , etc.) are removed, or are simply not activated. Then the circuit can still operate in bipolar fashion, but of each coupling pair, only the upper core (W, Y , etc.) will switch for *one* transfer and only the lower core (W', Y' , etc.) will switch for *zero* transfer. But more important, either polarity of loop current i_1 will have to overcome the threshold of a coupling core, resulting in some bipolar flux-clipping due to the inductance of the loop. Consequently, the transfer ratio can again be less than unity for values of signal near zero, resulting in a third stable point, at the origin, as indicated in Fig. 9-2(b). This stable common-mode range of operation is undesired for the normal case of a bipolar binary register, though it has potential use for storing and shifting ternary information, each digit having possible values $-1, 0, +1$. This ternary mode of operation is readily achieved in bipolar circuits without the use of any dynamic bias at all. With dynamic bias applied to the loop cores only, and with small, bilateral clipping (which could be increased by inserting a pair of small, oppositely cleared toroids in the loop), current tolerances for all three states should be comparable to those for dynamically biased unipolar circuits.

Derivation from a Pair of Complementary Registers. It has been assumed that the shape of the current pulse on each drive

line is independent of the information state. However, for a unipolar scheme, where flux is switched only for transfer of a *one*, the load imposed on the driver circuit is very dependent on the total information state. For driving a long register that holds arbitrary information, it is thus desirable to have a relatively high source impedance in order to minimize drive-pulse variations. Such drivers can be expensive and inefficient since they require a large voltage source compared to the maximum switching voltage of the register.

One way to reduce this driver problem is to add a second register that carries the complement of the information in the first register and is driven by the same driver, as indicated schematically in Fig. 9-3. For an N -bit register, the total number of *ones* in both registers is always equal to N ; thus the load due to core switching is independent of information and equal to the maximum load from one register alone. Because of this constant load, the requirements on driver voltage and internal impedance are greatly reduced. In fact, the driver now can be basically a controlled voltage source, or flux source, that injects the proper magnitude of flux linkage into the drive line.

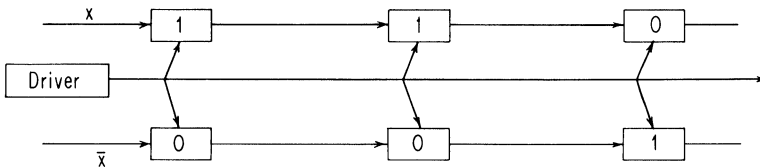


Fig. 9-3. Schematic representation of a coupled pair of registers that contain complementary information, in order to make the driver load independent of the data state.

A pair of complementary registers based on the circuit of Fig. 8-15 is shown in Fig. 9-4. This balanced circuit can really be viewed as a form of bipolar circuit in the sense that at any position of the register a unit of flux is transmitted in one coupling loop, say the upper loop, for a *one* and an equal magnitude of flux is transmitted in the other loop for a *zero*. What we would like to do now is show how to convert the circuit of Fig. 9-4 to the bipolar circuit of Fig. 9-1 and in the process show why the circuit of Fig. 9-1 is superior even to the balanced circuit of Fig. 9-4.

Dynamic bias can be applied to the pair of complementary registers, without adding any additional cores other than $\Delta\phi$ sources, since corresponding loop cores can be connected in pairs to a $\Delta\phi$ source, as indicated in Fig. 9-5. Drive is shown

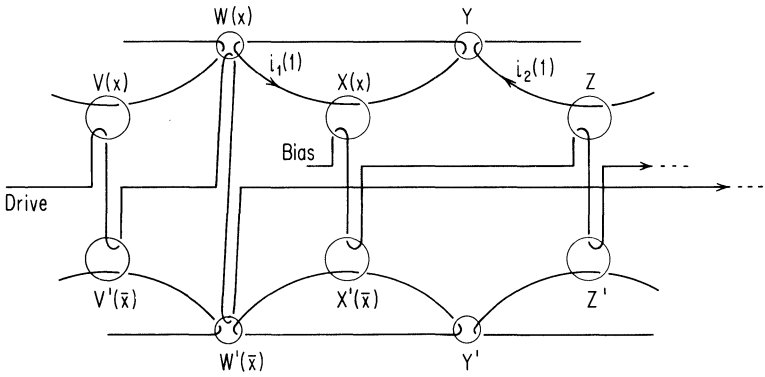


Fig. 9-4. Coupling a pair of unipolar registers of the form of Fig. 8-15 into a complementary pair in the manner of Fig. 9-3.

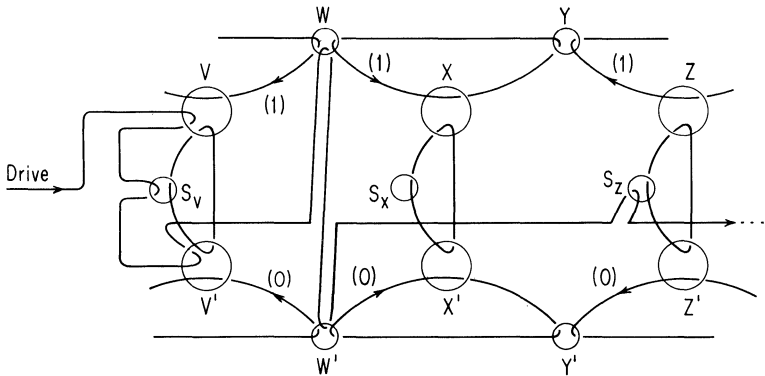


Fig. 9-5. Dynamically biasing the loop cores of Fig. 9-4 with the addition of one flux source for each pair of loop cores.

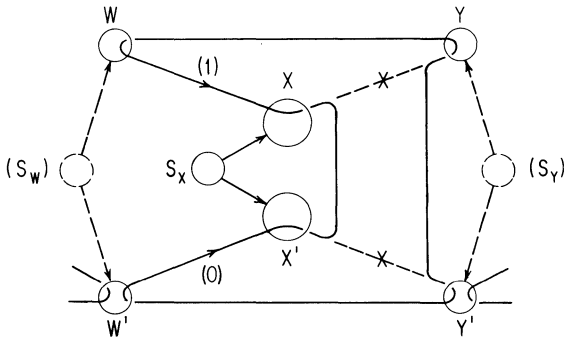


Fig. 9-6. Converting the circuit of Fig. 9-5 to a fully biased bipolar register of the same form as in Fig. 9-1.

applied for the case of $V \rightarrow Z$ transfer, where Cores V and V' are being cleared, and Cores Z and Z' are the receiver cores for the two registers. Suppose now that we alter this circuit further by breaking each pair of corresponding coupling loops and reconnecting them into a single loop in the manner shown for one pair of loops in Fig. 9-6. Now the current causing *one* transfer along the upper side flows in a direction to actually oppose any flux switching along the lower side, and vice versa for *zero* transfer. As a result, there is increased differential flux switching in receiver cores, and hence effectively higher gain in the circuit of Fig. 9-6 as compared to Fig. 9-5.

But note that the coupling-loop connection in the circuit of Fig. 9-6 is exactly the same as in the circuit of Fig. 9-1, except with the cores arranged in a different order. By merely adding S_W and S_Y sources (shown with dashed lines) for dynamic biasing of the coupling cores, we have exactly the bipolar circuit of Fig. 9-1. By having derived it this way, however, we see that the bipolar circuit of Fig. 9-1 is superior to the balanced circuit of Fig. 9-4, or even to the partially coupled circuit of Fig. 9-5.

Unipolar-to-Bipolar Conversion. To convert unipolar resistance and nonresistance schemes to bipolar schemes, in general, one need merely start with the unipolar circuit in toroidal-core form and then replace each toroid by a pair of dynamically biased toroids or by a core of the type shown in Fig. 8-16(c), as was done in the conversion from the circuit of Fig. 8-15 to that of Fig. 9-1. Then, if desired, network methods can be used to transform the circuit to a form using a smaller number of more complex multileg cores.

Bipolar MAD-R with Dynamic Bias. A straightforward approach to a bipolar MAD-R scheme is shown in Fig. 9-7. This circuit does not utilize dynamic bias and, though operable, is considerably poorer even than the basic unipolar MAD-R circuit. By placing

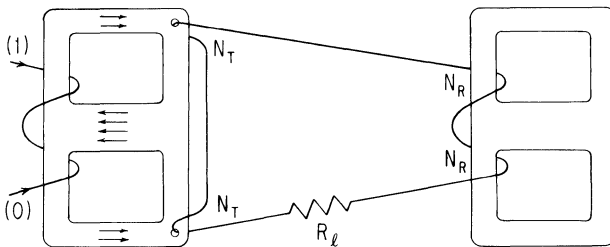


Fig. 9-7. Bipolar MAD-R without dynamic bias.

two minor apertures in the center leg of each element, as shown in Fig. 9-8(a), W. K. English (unpublished notes) has shown how dynamic bias can be incorporated into this circuit. The leg between the two minor apertures serves as a one-unit flux source that sets one-half unit of flux in each half of the core when no input signal is present. Each of the other central legs must have 1-1/2 units of capacity for proper flux closure, as indicated by the pairs of long and short arrows.

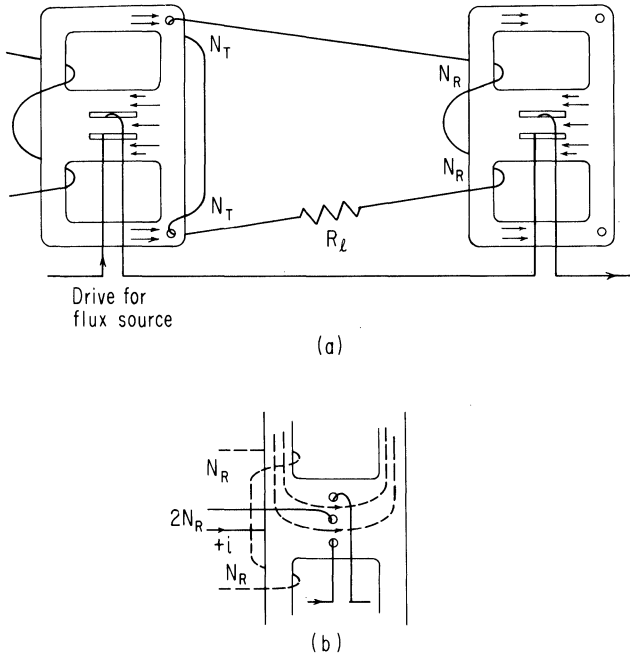


Fig. 9-8. Incorporating dynamic bias into the bipolar MAD-R circuit of Fig. 9-7: (a) by the use of two minor apertures in the central leg; and (b) by the use of three minor apertures in the central leg, in which case the two input windings may be replaced by a single input winding of twice the turns through the central minor aperture, as shown.

The wiring is more complex for this circuit than for the dynamically-biased unipolar MAD-R circuits of Sec. 8-3, though the flux source is now built into the multiaperture core, making an auxiliary toroid unnecessary. Laboratory results with experimental cores of this type have shown that unity gain can be obtained with a coupling loop resistance four to five times higher than in the basic MAD-R scheme, with a corresponding ratio of

improvement in priming speed. (As noted in Sec. 8-3, with the dynamically biased unipolar version, the maximum increase is about three to one.)

To illustrate the variety of form possible with bipolar circuits, we take note of one particularly interesting variation. By dividing the flux source leg by still another aperture, as in Fig. 9-8(b), then the two receiver input windings of Fig. 9-8(a) may be merged to a single winding through the added central aperture of Fig. 9-8(b). As a result, the two transmitter windings and the single receiver winding may now have the same number of turns (in particular, single turn windings) without loss in flux gain. This is in effect a flux-doubling configuration resulting from the fact that during transfer, the input winding (of twice the turns) is linked by only half of the signal flux, i.e., the difference flux, that is set around the output apertures. For example, in the limiting case of complete steering by the input current, the entire capacity of the flux source switches to one side of the core, as indicated by the dashed lines in Fig. 9-8(b), but only half of this flux actually links the input winding.

9-2 Thin-Film Schemes

In the description of transfer schemes in previous chapters, the basic elements have generally been assumed to be fabricated from ferrite material, although any type of magnetic element with reasonable threshold, saturation, and switching properties could actually be used. In particular, considerable attention has been given to the use of magnetic thin films in the realization of core-wire circuits. The primary motivation is the potential of batch fabrication, miniaturization, and low power consumption. Furthermore, higher speed and other increased functional capability might be expected because of the coherent rotation properties of thin films.

Interconnected Thin-Film Patches; Coherent Rotation. In Fig. 9-9 we show a pair of planar thin films interconnected by a strip-line coupling loop (ignore the dashed lines for the moment). Film patches are typically of the order of a micron or less in thickness and therefore have a much lower flux capacity than typical ferrite toroids. The requirement of relatively low flux losses during transfer therefore implies that the absolute magnitude of losses be much lower than with ferrite cores, and hence (assuming comparable loop current and switching speed) that the value of loop R

and L must be very small. (It is for this reason that a wide strip-line configuration is shown for the coupling loop.)

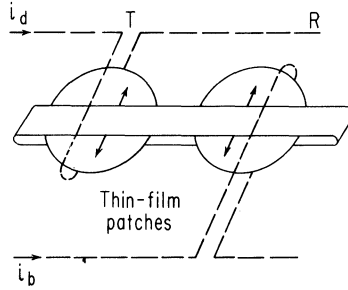


Fig. 9-9. A pair of planar thin films connected by a strip-line coupling loop.

Considering practical limitations on strip lines (such as a minimum spacing due to the requirement of a reliable insulation layer), it was shown by Engelbart (1959) that transfer would be extremely difficult to achieve with strip-line coupling loops unless some functional difference were realized in the direct replacement of ferrite toroids with thin films. Such differences are in fact realized because flux switching by coherent rotation, rather than by domain-wall motion, can readily be achieved with thin films, resulting not only in increased speed and reduced loop losses, but also in a new flux-gain mechanism.

The basic property of coherent rotation is illustrated in Fig. 9-10. Each oriented film has preferred (i.e., "easy") directions of magnetization, as indicated in Fig. 9-10(a) by the arrows on the film. In Fig. 9-10(b) a current i_d drives the magnetization into the "hard" direction, i.e., at right angles to the

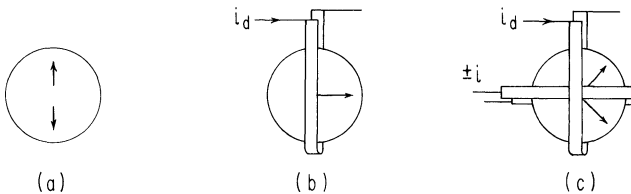


Fig. 9-10. Coherent rotation of magnetization: (a) easy directions of magnetization; (b) driving to the hard state of magnetization; and (c) steering the direction of coherent fallback of magnetization (for $i_d = 0$) with a tipping current $\pm i$

preferred directions. This is an unstable condition of magnetization, and if i_d were now removed the magnetization would fall back either coherently to one or the other states of easy magnetization, i.e., as a single domain—see Sec. 11-3, or more likely the magnetization would break up into some complex domain pattern. If, prior to removal of i_d , however, an orthogonal steering (or “tipping”) current $\pm i$ is applied, then the fallback can be guided to one or the other easy directions of magnetization. To ensure coherent fallback, the steering current must be sufficient to tip the magnetization vector beyond some small (critical) angle from the hard direction. Once started, the magnetization falls back coherently without further guidance (i.e., with $i = 0$) to the easy direction toward which it was steered.

Let us now consider the basic mode of operation as devised by Engelbart, in order to make use of coherent rotation. First, a bias current i_b is applied to the receiver of Fig. 9-9, as shown, to initially force the magnetization of the receiver into the hard direction. Then, a drive current i_d switches the transmitter film to the hard direction, thereby inducing a loop current of one polarity or the other, depending on the initial easy-direction of magnetization of the transmitter. Assuming that the loop current tips the magnetization vector of the receiver sufficiently (in the sense of Fig. 9-10(c)), then the receiver magnetization falls (coherently) in the steered direction. Hence the initial direction of magnetization of the transmitter is transferred to the receiver under control of a relatively small steering current in the coupling loop. In this tipping mode, the loop-loss quantity of importance is just that which occurs up to the point in time where the receiver magnetization passes the critical angle. The magnitude of received $\Delta\phi$ to just reach the critical angle is proportional to the sine of the critical angle, and is therefore small compared to the total $\Delta\phi$ transmitted. Hence, loop losses can be allowed to absorb a major part of the transmitted $\Delta\phi$, up to this point in time, after which the remainder of the switching process is automatic. Because of relatively high losses in the coupling loop, however, the transmitter finishes switching, and loop current decreases to zero, before the receiver itself can finish switching. Completion of receiver switching induces a reverse current in the coupling loop, but this merely has the effect of slowing down the final state of receiver switching.

A study by Green (1959) includes theoretical calculations and some experiments with films of about 0.1 micron in thickness. Based on applying this technique to the scheme of Fig. 5-20(d), it was concluded that a logic system is possible but probably not

practical. It is interesting, therefore, that Dick and Doughty (1963) were able to achieve quite good performance with a change to a cylindrical film geometry and a more favorable transfer scheme for this type of operation, as described in the following section.

Dick and Doughty Bipolar Orthogonal Scheme. It was shown in connection with Fig. 8-13(a) that a workable scheme could not be synthesized with a simple two-mode configuration as the basic stage. Figure 8-13(b) illustrated an expansion to a 4-mode configuration that was used as the basic stage in Fig. 8-13(c). We would like now to show an alternate 4-mode derivation that leads to still a different configuration.

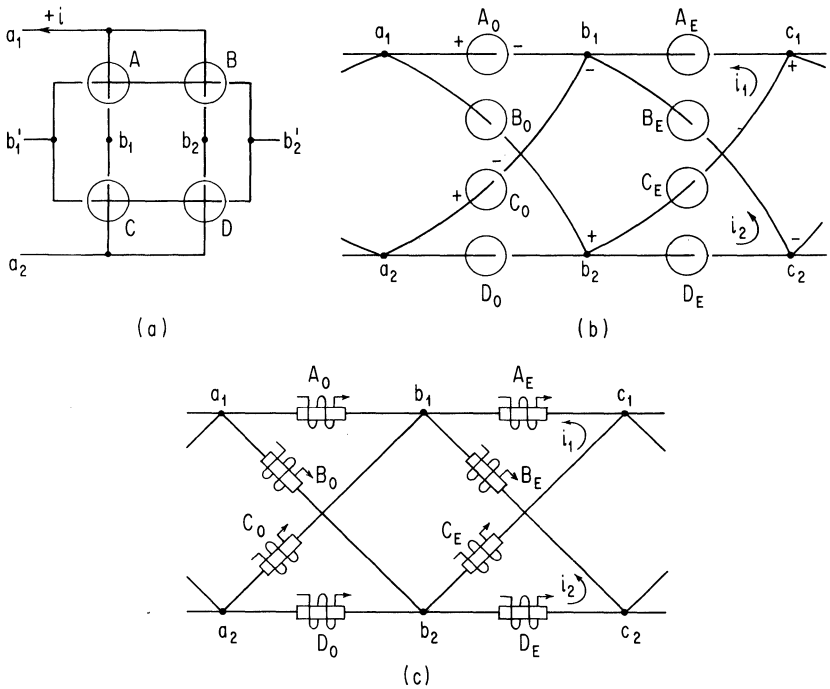


Fig. 9-11. Dick and Doughty orthogonal-mode, bipolar, thin-film register.

In the arrangement of Fig. 9-11(a), Cores A and B are set in response to a positive input current i (just as in Fig. 8-13(b)) and Cores C and D are subsequently set in response to a negative input current. During either phase, there is zero voltage developed across the output terminals $b'_1 b'_2$. A series of such stages could be

arranged into a register using N_R turns on all windings connecting to terminals $a_1 a_2$, and N_T turns on all windings linking terminals $b'_1 b'_2$. But let us ignore the problem of $\Delta\phi$ gain for the moment and set $N_T = N_R$. In this case, the voltage across terminals $b_1 b_2$ is exactly the same as that across terminals $b'_1 b'_2$. Using the former as output terminals, and dispensing with the latter, we have a conventional bridge circuit that can be rearranged in the form of a lattice. A register consisting of a chain of these lattice circuits is shown in Fig. 9-11(b).

Disregarding the fact that we do not yet have a gain mechanism, let us consider paths of switching for unipolar *one* transfer. (For a *zero* state, there would be no flux switching at all.) Assume all O cores are set. The $O \rightarrow E$ pulse clears A_O and C_O so that a voltage is developed across terminals $b_1 b_2$, of the polarity shown, and the induced currents i_1 and i_2 then set A_E and B_E , respectively. Note that this results in zero voltage across terminals $a_1 a_2$ and $c_1 c_2$; that is, there is no spurious forward or back transfer. During the Clear- O phase, Cores B_O and D_O are cleared, with the result that Cores C_E and D_E are set. Thus, in two phases, all of the O cores are cleared and the E cores are set. The cycle is completed with $E \rightarrow O$ and Clear- E pulses. (Note the similarity of this lattice electric circuit and the lattice magnetic network of Fig. 8-14.)

Dick and Doughty (1963) use the configuration of Fig. 9-11(b) to construct a bipolar, thin-film register, where the coherent rotation of the films supplies the necessary flux-gain mechanism. Cylindrical films about 1.0 micron thick are electrodeposited on each branch wire (in place of a separate toroid), as shown in Fig. 9-11(c), with the easy directions of magnetization being circumferential. A *zero* is represented by all films in a given column being magnetized, say clockwise, looking down the register, and a *one* by counterclockwise magnetization. Films in alternate lattice sections, which are not storing data, are magnetized in a hard direction by solenoidal drive fields. During $O \rightarrow E$ transfer, A_O and C_O are driven to their hard direction, by applying solenoidal drive fields, and the drive fields are relaxed on A_E and B_E . The potential across terminals $b_1 b_2$, and hence the induced currents i_1 and i_2 , are positive or negative depending on whether a *zero* or *one* is being transferred, and the coherent fallback of magnetization in A_E and B_E is steered accordingly.

During the following Clear- O phase, films B_O and D_O are driven to their hard direction, and the solenoidal fields are relaxed on C_E and D_E . Now Currents i_1 and i_2 are of opposite polarity than during the first phase and properly steer films C_E and D_E during their

fallback. Thus, in two phases, the E films are magnetized to the same easy direction as the O films previously were. The cycle is completed with $E \rightarrow O$ and Clear- E pulses. This, then, is a bipolar thin-film scheme relying on coherent rotation for overcoming losses and for achieving $\Delta\phi$ gain.

Dick and Farmer Bipolar Resistance Scheme. A recent development by Dick and Farmer (1966) is a resistance scheme that requires a surprisingly small number of elements per bit, and which has operated at quite high bit rates. Only three elements (1-1/2 magnetic elements and 1-1/2 resistive elements) per bit are required as compared to five per bit for the minimal scheme of Sec. 7-3. Operation is reported at bit rates of a few Mc/s which is 2-3 orders of magnitude higher than those typical of resistance schemes using ferrite cores (1 to 50 kc/s).

The scheme is illustrated in Fig. 9-12(a), where the cylinders represent cylindrical film elements electroplated on a central conductive wire, and the coupling loop resistance is provided by

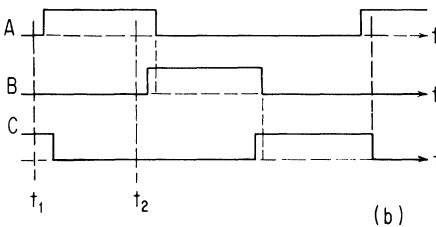
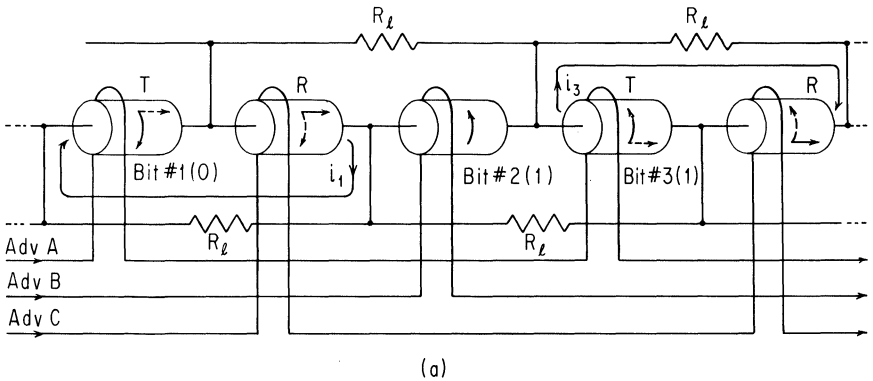


Fig. 9-12. Dick and Farmer thin-film bipolar resistance scheme.

the resistance of a parallel wire outside the film. The preferred, or easy, directions of magnetization are circumferential; let downward magnetization represent a *zero* and upward magnetization a *one*. Bits of information are stored in two out of three elements, leaving one out of three ready for reception. The labels *T* and *R* (for transmitter and receiver) correspond to transfer of the first and third bits that takes place during the Advance-*A* phase of drive. One or another of the three advance pulses is energized at all times, with overlapping as indicated in Fig. 9-12(b). The solid arrows in Fig. 9-12(a) represent the states of magnetization at the time t_1 , just prior to application of the *A* pulse. At this instant, Current *C* is still energized and holding the receivers *R* in their hard direction of magnetization.

Application of the *A* pulse turns the magnetization of each transmitter into the hard direction and the resulting loop currents turn the magnetization of each receiver toward the direction formerly stored in the corresponding transmitter. Release of the previous advance pulse *C*, near the peak of the transfer current, allows the receiver magnetization to fall back toward the appropriate preferred direction, resulting in the dashed directions being reached by the time t_2 , just prior to application of the *B* advance pulse. This coherent fallback causes reversal of direction of the transfer currents, as described earlier in connection with Fig. 9-9, which are allowed to decay prior to the start of the next advance pulse.

There will also be currents induced in all the other loops, e.g., in those coupling the element storing Bit #2, but of insufficient level to turn the magnetization of the second bit significantly away from the preferred direction. Thus every third core acts as a buffer that obviates the problem of back transfer. Large receiver loading exists, but the effect is overcome by the high gain mechanism inherent in coherent rotation. In the earlier three-phase schemes (see, for example, Figs. 3-11 and 3-12) buffering was achieved by unconditionally holding each third core in a saturation state to prevent back transfer. It is interesting that in the present case this isolation is obtained not by explicit holding but by the strongly preferred directions of easy magnetization. Thus, effective isolation is obtained even though the buffering element itself holds useful data. This is a good example of an effectively large threshold that is readily overcome, when required, by the use of dynamic bias.

Continuous Thin Film with Reverse Domains. The possibility of transfer techniques using continuous strips of thin films is

attractive because explicit coupling loops would not be required. One such scheme based on the use of a continuous strip of film is illustrated in Fig. 9-13. The strip of film, although uniform, has been divided into segments with imaginary dotted lines. Three segments are required per bit (as indicated by the labeling A, B, C) and we assume that information is initially stored in the B segments. The film is oriented longitudinally, with the *zero* state represented by magnetization M pointing uniformly to the right, as in B' , the same as the clear state in the adjacent A and C segments. A *one* is represented by M pointing to the left, as in B , that is, by a reverse domain relative to the adjacent segments. Any reverse domain must of course involve flux closure through the air. The high magnetic-pole densities (see Sec. 11-3) associated with opposing M vectors result in complex domain-wall configurations (suggested by the jagged lines at the boundaries of B) that form in such a way as to spread out the pole densities until field strengths at the edges of adjacent strips are just at threshold or less.

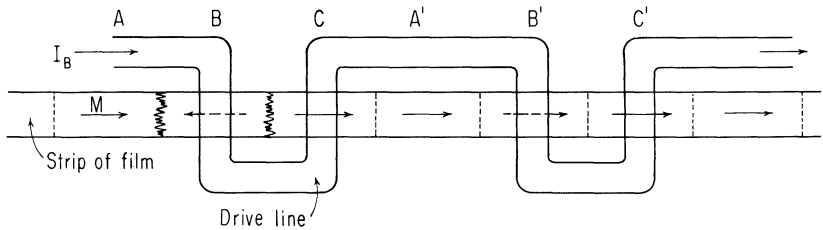


Fig. 9-13. Continuous-film register in which data states are represented by local polarity of magnetization.

In order to shift information from the B to the C segments, a drive current I_B is energized, which applies clear-direction mmf to all B segments and set-direction mmf to all C segments. Whenever a *one* state is held in a B segment, the left edge of the neighboring C segment is biased toward threshold by the poles existing at the boundary. As a result, only a low drive current is required to reverse the segment C by means of wall movement from the right side of B to the right side of C . Similarly, the domain wall at the left side of B (the left boundary of the reverse domain) moves to the left side of C . Thus the reverse domain travels one segment to the right. A significantly higher current level is required, however, to nucleate a new reverse domain where a *zero* is being transferred, as at C' , and hence C' remains in its original state, with M pointing to the right, and thus correctly represents the

zero bit formerly stored in B' . Two other drive lines symmetrical with the one shown are needed to shift from the C to the A segments, and then to the B segments one bit-length ahead, to complete the cycle.

Because of the physical symmetry, at least three clock phases are needed for directivity. However, more than three clock phases may be used for additional isolation between information segments containing reverse domains. Bobeck and Fischer (1959) realized this type of scheme with a magnetic wire, as opposed to a strip of film, in connection with a five-phase cycle. Broadbent (1960) described a convenient wiring arrangement involving only two drive lines for a four-phase clock cycle (based on opposite polarities being applied alternately to each of the drive lines). Recent work has been done on this scheme at Bell Telephone Laboratories, for example, by D. H. Smith (1965). Spain, Jauvitz, and Fuller (1965) describe a similar scheme based on the easy direction being transverse to the direction of propagation.

Smith Continuous-Film Scheme; Sense of Wall Rotation. In any domain wall there are two senses in which the spin vectors can rotate, in turning from the direction in one domain to the direction in the other domain (see Chap. 11). For Bloch walls, the spin vectors turn to point out the plane of the film, as shown in Fig. 9-14(a) and (b), representing "right-hand" and "left-hand" walls, respectively. In ultrathin films, Néel walls occur, for which rotation is within the plane of the film, as shown in Fig. 9-14(c) and (d), again for the right-hand and left-hand walls, respectively.

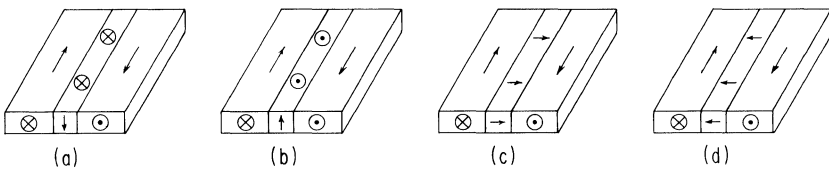


Fig. 9-14. 180° domain walls: (a,b) Bloch walls in which the spins are perpendicular to the plane of the film; and (c,d) Néel walls in which the spins are in the plane of the wall.

A transfer scheme described by Smith (1961), based on data representation by polarity of spin rotation, is illustrated in Fig. 9-15. As indicated by the arrows on the films, the preferred, or easy, directions here are transverse to the film. A bit of information is represented by the sense of the spin rotation within

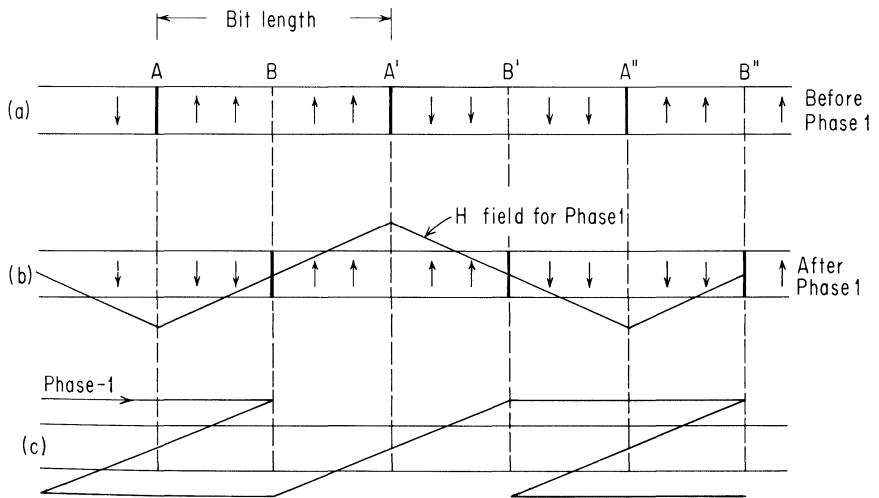


Fig. 9-15. Smith thin-film scheme, in which data states are represented by direction of rotation of spin in the 180° walls between adjacent transverse domains.

a wall at each A position of Fig. 9-15(a). The domain magnetization vectors between the walls alternate as shown, independent of information state. The Phase-1 clock pulse is applied so as to produce a field that varies with distance as indicated in Fig. 9-15(b). These fields cause a shift of the walls to the B positions. The Phase-2 clock pulse applies a similar field pattern, but shifted half a segment to the right, so that walls are again shifted to the A positions, but one bit position advanced from the original. After these two phases, all domain directions are exactly opposite to the original ones. Third and fourth clock pulses are then applied to the same drive lines, but with polarities opposite to those of the first and second phases, respectively. Thus a four-phase clock cycle is needed, but the information (stored in the walls) is transferred two bit positions each cycle (cf. Van De Riet scheme of Fig. 7-12).

The alternating field pattern of Fig. 9-15(b) is physically awkward because it requires currents of alternating polarity flowing along the film. The solution given by Smith for this problem is to apply currents across the film at a slant, as indicated with the Phase-1 drive line in Fig. 9-15(c). The fields from the slanting segments cancel to a resultant field of zero at points along the film in line with ends of segments such as B, but reach maximum values at points such as A. Thus the net vertical component of the field due to the crossing currents has approximately the variation indicated in Fig. 9-15(b).

9-3 Non-Return-to-Reference Schemes

In every scheme discussed thus far, each magnetic element involved in information transfer is cleared to a reference state at least once each clock cycle, and hence these schemes have a "return to reference" nature. For unipolar schemes, the reference state is nominally equivalent to the *zero* state. For bipolar schemes it is an intermediate state. The term "non-return to reference" (NRR) is related to the term "non-return to zero" (NRZ) as used in digital magnetic recording. For NRR schemes, at least one core in each stage remains constantly in the *one* state during the shifting of a set of adjacent *ones*. Such a core is switched to the *zero* state only for a change from *one* to *zero* in the information sequence, and it remains in a *zero* state until there is a change to *one* in the sequence.

A Method of Converting Schemes to NRR Operation. To illustrate a method for potentially converting a large class of schemes to NRR operation, let us return to the Van De Riet representation (Chap. 7) and consider as an example the Engelbart scheme of Fig. 7-3 for which the set-state pattern for two adjacent *ones*, flanked by *zeros*, is represented. The same information pattern in NRR operation is shown in Fig. 9-16. A string of *ones* of any length would be similarly represented, with a pair of set loop cores representing the boundaries of the string and with all intervening coupling cores in the *one* state. For transfer of such a *one*-state pattern, all loop cores are driven to their reference states in the same sequence as before, but no more than bias

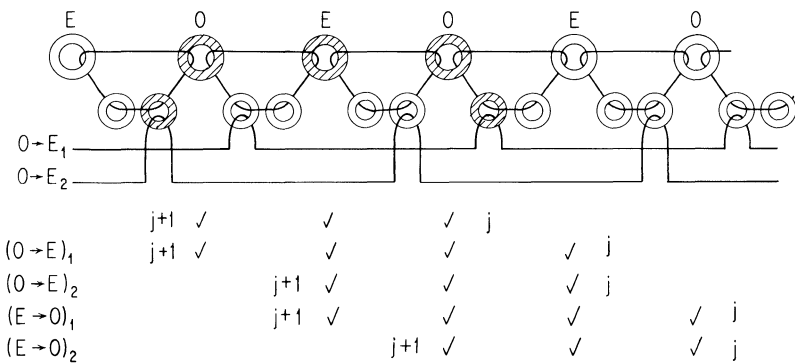


Fig. 9-16. Illustrating the use of the Engelbart scheme of Fig. 7-3 with a non-return-to-reference data representation.

levels of drive mmf, i.e., not exceeding core threshold, are ever applied to coupling cores. What was formerly the reference state of a coupling core is now simply the *zero* state, and we view the clock sequence as consisting of four advance pulses rather than two advance and two clear pulses. (Data is still shifted one bit position per clock cycle.)

The effect of NRR operation on core switching during transfer can be seen by comparing the chart in Fig. 9-16 with that in Fig. 7-3. The designations j and $j + 1$ indicate that the boundaries of the *one*-state pattern correspond to bit numbers j and $j + 1$ in this case. After any phase of operation, each intervening core that is in the set state is indicated by a check mark.

One advantage of NRR operation is the reduction of total core-switching energy, since cores are switched only at the boundaries of a string of *ones*. Transfer of the alternating pattern, $\dots 10101010 \dots$, requires more cores to be switched each cycle than any other pattern, but only half as many cores as for a pattern of all *ones* in the case of return-to-reference operation. In other words, for a given bit rate, conversion to NRR operation, in the manner described, reduces the peak core-switching power by 50 percent and also reduces the average power required for random information. This would tend to lessen the problem of driver design and also, for high-speed operation, the problem of core heating. A serious disadvantage, however, is that the coupling cores, being switched by information currents only, are never driven hard into saturation and hence exhibit soft-state switching properties at all times. This factor alone very seriously reduces the range of operation. In fact, the only successfully operated NRR scheme thus far reported is a very interesting two-phase NRR resistance scheme, which is bipolar in nature. This scheme will now be described.

Mina and Walters Bipolar NRR Scheme. In the version of the Mina and Walters (1964) circuit shown in Fig. 9-17, only one multi-leg core is needed for each bit-length of the register. The right side of the core (Legs $D, E, F, G,$ and H) has a definite reference state (as shown by the solid arrows) to which it is unconditionally driven by each advance pulse. (Actually, Legs $F, G,$ and H never switch, but simply provide for proper flux closure.) The left side of the core (Legs $A, B,$ and C), which is driven only by coupling loop current, is in the *one* or *zero* state for clockwise or counter-clockwise direction of flux, respectively. For illustration, we assume that the bits initially stored in Cores n and $n + 1$ are a *zero*

and a *one*, respectively, as indicated by the dotted arrows in Fig. 9-17.

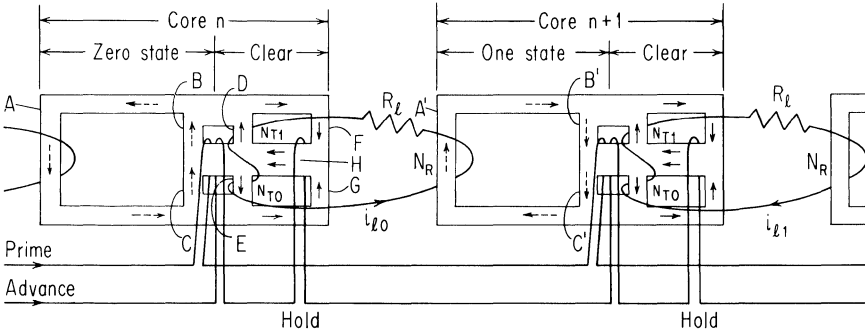


Fig. 9-17. Mina and Walters bipolar non-return-to-reference scheme.

The first phase of operation, i.e., priming, is accomplished with a current within a range of magnitude large enough to cause switching around one of the two small central apertures but not around the large left-hand aperture. With the priming line linking the pair of small apertures symmetrically, switching can occur only around the lower aperture in case of a *zero* and only around the upper one in case of a *one*. During this phase, there is slow dissipation of $\Delta\phi$ in the loop resistance R_l , as usual, via induced loop currents which are of opposite polarity for the two different information states.

After priming, application of the advance drive (including holding on Leg H) switches Leg D or E into its original (reference) direction. There is a resulting flux change linking either N_{T1} or N_{T0} , with polarity to induce currents i_{l1} or i_{l0} , respectively, depending on information state. If the information state at the receiving end of a loop is opposite to that at the transmitting end (as in the case here for Core $n + 1$ versus Core n), then the loop current causes reversal in Leg A and in Legs C and D (if $i_l = i_{l0}$) or in Legs B and E (if $i_l = i_{l1}$). Assuming N_{T1} and N_{T0} are each $> N_R$ to provide flux gain, then the information state in the receiving core is thus changed. If the adjacent information states are the same, however, then i_l cannot switch Leg A inelastically, and the transmitted flux is all dissipated in loop resistance, just as during the priming phase. The advance mmf can be larger than the priming mmf without disturbing existing information states, since if the loop current does not switch the receiver, it simply

drives the receiver further into its present flux direction. Thus less time is required for the transfer phase than for priming.

Several aspects of this interesting scheme deserve comment. First, the two phases required are one less than the minimum of three found in Chap. 7 for the class of schemes considered there. Second, dc priming may be used (in which case priming begins immediately as each advance phase is completed), so that only a single pulse is actually required for the two-phase operation. Third, the scheme is bipolar in the sense that loop currents are bipolar and the circuit is symmetrical with respect to *one* and *zero* storage and transfer. But it is different from the bipolar schemes of Sec. 9-1 in that storage is in terms of two polarities of flux in the same path, rather than in terms of flux in two symmetrical but different paths.

In spite of considerable bit-to-bit interaction with two-phase, single-clock-pulse operation, substantial tolerances on drive currents are reported by Mina and Walters for a coupling-loop turns ratio of 3:1.

9-4 Summary

In Chap. 8 we saw that with dynamic bias the driver circuit assumes the entire "threshold burden" and that signal currents need only steer the division of the unconditionally switching flux in favor of one path or another. Here we show that by dynamically biasing all cores in the circuit we achieve a complete symmetry of operation in which positive and negative loop currents have equal but opposite flux-steering effects. This leads directly to a bipolar representation in which transferred binary states are represented by flux linkages of one polarity or the other, rather than by presence of flux linkage, or not, as in the case of unipolar representation. The advantage of bipolar transfer schemes is a significant increase in performance over unipolar schemes, but at the cost of substantial increase in circuit complexity.

We also discuss schemes based on the use of magnetic film films. It is first shown why schemes using isolated thin-film patches must depend on the use of coherent rotation as a gain mechanism, a mode of operation in which the film is driven to a hard direction of magnetization and the signal current simply controls the direction of coherent magnetization fallback to either of the two easy directions of magnetization. This naturally leads to a symmetrical bipolar representation. It is also possible to

synthesize continuous-film transfer schemes, however, in which magnetization states are shifted along a continuous film without the use of coupling loops. In one scheme, information is represented in the polarity of magnetization. In a second scheme, information is contained in the sense (clockwise or counterclockwise) of spin rotation in the walls separating oppositely magnetized domains along a continuous film strip. In spite of the simple elegance of thin film schemes, a general practical difficulty is that of sensing information states, because of the very low signal levels involved.

Finally, we consider a non-return-to-reference representation in which flux switching occurs only to signal a change in state in a binary string, similar to the non-return-to-zero technique of magnetic recording. Thus, during transfer of a string of *ones* embedded in a string of *zeros*, switching to the *one* state signals the *zero-to-one* transition, and there is no further core switching until the left end of the string is reached, at which time there is a switch to the *zero* state. The Mina and Walters non-return-to-reference scheme, though primarily of academic interest, is particularly interesting in that it is the only two-phase core-wire scheme known to have been operated successfully, and with dc priming only one clock pulse is actually required.

In this chapter we have introduced a number of very elegant techniques that are discussed in the literature. But in spite of their great elegance and intellectual appeal they have as yet found no practical application. The bipolar schemes suffer primarily from relatively great circuit complexity, and as we will see in Chap. 10, the large gain in performance achieved in simple transfer circuits can be rather quickly dissipated in more complex logic circuits. The thin-film schemes, as we already noted above, suffer from very low signal levels and from a general difficulty in extending them to general logic. The non-return-to-reference scheme offers only the potential for a single-clock system and at the cost of circuit complexity and relatively poor performance.

In fact, of all the schemes discussed to date, only the MAD-R scheme has withstood the technological and economic tests of practical application, and, where applied, these circuits have performed superbly, especially with respect to achieving the very high levels of reliability of which such circuits are inherently capable.

With this chapter we end the treatment of basic flux-transfer techniques. Our hope was that the step by step development would permit the reader not only to become acquainted with all of the basic techniques and schemes presently known, but also to see the

relationship between all of the various schemes—in particular, to see how to transform from one scheme to another and thereby judge the advantages and disadvantages of each scheme by the nature of the transformations involved. We now enlarge the scope of the treatment, and consider how independent units of flux, which represent different binary logic variables, can be combined to achieve a general logic synthesis.

SYNTHESIS OF GENERAL LOGIC CIRCUITS

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10-1 Introduction

Thus far the main emphasis has been to describe the nature of core-wire circuits, in particular the properties of flux transfer along chains of magnetic elements that have neither logical fan-in nor fan-out. We wish to consider in this chapter methods for extending the basic circuit techniques to the synthesis of digital logic circuits.

There are many possibilities for the formation of logical functions in core-wire circuits because of the inherent electrical isolation between windings, with the result that: (1) transmitter

windings can be arranged in different series-parallel combinations; (2) the polarity of any transmitter signal can be reversed merely by reversing the sense of the corresponding winding; and (3) the same signal current can be made to link a number of different receiver cores, to provide branching, or fan-out. Because of this flexibility, there generally exists a number of different ways to synthesize any given logical function, even a very simple function. The circuits that result from these different synthesis methods often exhibit significant differences in performance, as well as in the number of devices required and the number of windings used.

A disadvantage of core-wire circuits generally is that they have low gain, compared, say, with ordinary transistor circuits. The result is that performance is more dependent on exact circuit conditions—the degree of loading, and so on—and the degree of fan-out in one step is always of relatively low degree. There is need, therefore, to know the best ways to exploit the inherent flexibility in order to achieve efficient design.

In Sec. 10-2 we review the general organization of a synchronous digital logic system, and in Sec. 10-3 we turn the discussion to the synthesis of synchronous core-wire systems in particular. The general synthesis of logic functions is considered in Sec. 10-4, and an actual design example is given in Sec. 10-5. The design method for the MAD-R scheme (Chap. 6) is extended to logic circuits in Sec. 10-6.

10-2 Synchronous Logic System

A convenient representation of a synchronous logic system is indicated in Fig. 10-1(a). It recognizes that two types of components are required, namely, storage units (e.g., transistor flip-flops) and logic units. At any instant, the *state* of the system is determined by the state of the storage elements. At each clock pulse, the storage elements are altered to a new state. The new state (or “next” state, as it is generally called) of any particular storage element is determined by a logical combination of the present state of some set of storage elements (and possibly some set of external inputs, e.g., switches). Thus, the relation between the set of next states and the set of present states is determined by the specific arrangement of the combinational-logic network.

In the one-clock system of Fig. 10-1(a), a minimum delay must be present somewhere in each loop between the input and output of

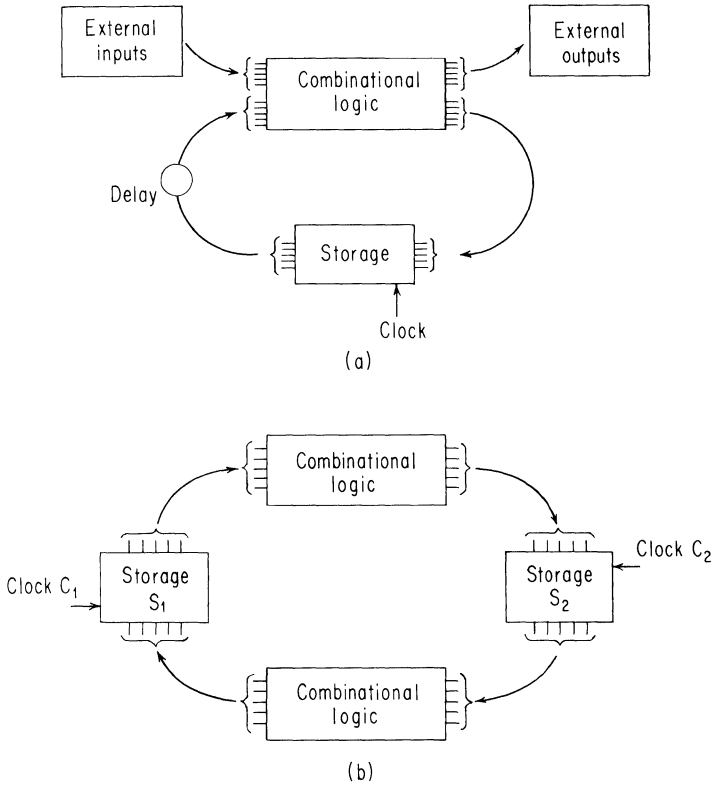


Fig. 10-1. Representation of a synchronous logic system: (a) single-clock system, and (b) two-clock system.

each storage element. Without such delay, some storage elements might tend to change state more than once during the *same* clock pulse. The need for delay is eliminated in a two-clock system, where there are two separate groups of storage and logic elements, as in Fig. 10-1(b). At Clock Pulse C_1 , storage elements S_1 are altered to their next state, under control of the state of storage elements S_2 . No circuit delay is required since the information state of the elements S_2 cannot be changed except during Clock Pulse C_2 , which follows C_1 after a minimum time delay to ensure that the elements S_1 have reached their new steady state. During Clock Pulse C_2 , the storage elements S_2 are altered to their next state, under control of the state of storage elements S_1 . Logical functions can be synthesized on each step. It is of course possible to arrange for even more than two groups of storage and logic sets,

with a corresponding increase in the number of clock-pulse sources.

10-3 Magnetic Synchronous Logic System

With all cores of a core-wire circuit being of the square-loop type, we might at first think that all cores are therefore storage elements. Though this is true from the point of view of flux storage, it is not true for the handling of logic states. Some cores, for example, might be driven only by the clocks and never store any of the system variables at all. We must be careful therefore to distinguish between core types in terms of the way they are used. We should also note that, whereas in a conventional transistor system, for example, the dc voltages are the primary power sources (the clock signals providing a timing function—opening and closing the low-powered gates in the proper sequence), in a core-wire system the clocks are the source of all switching energy as well as of timing.

In this section we first show how direct replacement of each transistor flip-flop by a one-bit shift register would permit direct synthesis of magnetic logic systems in the image of familiar transistor logic synthesis. We will readily see, however, that such a direct mapping would lead to impractical systems. With this mapping as an introduction, we then show a variation that is well suited to magnetic logic systems.

Simulating a Transistor Flip-Flop. To achieve a bistable gain characteristic, transistors are arranged in pairs, in familiar flip-flop configuration. One can view a flip-flop as a pair of negation transfer circuits, in the sense of Fig. 8-2, where an increase in signal level from one element, or stage, results in a subsequent decrease from the other stage, which causes a still further increase in signal from the first stage, regeneratively, i.e., with gain greater than unity, until a stable (saturation) state is achieved. There is an important difference in operation, however, from a practical point of view. The transistor operates from dc voltages and exhibits what we might call dc gain. Square-loop magnetic cores, on the other hand, are basically flux-storage devices, which can exhibit only ac (or dynamic) gain, and regenerative action must be specifically clocked. Thus, with a bistable gain characteristic, if the signal level is initially on one side or the other of the intermediate unity-gain point, then the signal will monotonically build

to one or the other stable states, but only so long as the clock pulses are operating. If the clock pulses are stopped, then the regeneration stops, but it picks up again from the same point whenever the clock pulses are turned on again. (This leads to one of the practical advantages of magnetic logic circuits in applications where energy is at a premium. With the clocks stopped, the present state of the system is maintained indefinitely with no energy dissipation whatever.)

With this analogy in mind, we can consider a possible structure for a synchronous magnetic logic system. We might note first, though, that we here introduced a negation-transfer register only because the negation transfer is analogous to the polarity-inverting transistor stage. However, a simple-transfer register could serve just as well, such being more analogous to a coupled pair of the earlier point-contact transistors, which exhibited voltage gain even in the non-inverting emitter-follower configuration.

Timing Clocks and Pumping Clocks. Based on the use of "magnetic flip-flops" (one-bit registers) the direct synthesis of a magnetic logic system in the fashion of Fig. 10-1(b) is straightforward (assuming the ability to do magnetic combinational logic). In terms of Fig. 10-2, the basic operation would be as follows: Clock Pulse C_1 causes a shift from the right-hand to the left-hand storage elements, followed by a set of clocks $\{C_{S1}\}$ energized to build up, or regenerate, the flux levels in the left-hand storage registers. Then Clock Pulse C_2 causes transfer to the right-hand elements, and a second set of clocks $\{C_{S2}\}$ restores the levels there. Constructed in this way, the logic system would be completely analogous to the transistor flip-flop system of Fig. 10-1(b).

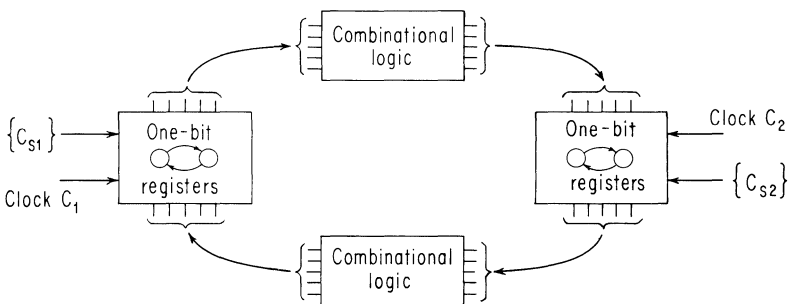


Fig. 10-2. Replacing the transistor flip-flops with one-bit shift registers and pumping clocks $\{C_{S1}\}$ and $\{C_{S2}\}$.

However, this method would be impractical because of the large number of clock drivers that would be required.

We should distinguish between the two different types of clock pulses required in Fig. 10-2. The clock pulses $\{C_{S1}\}$ and $\{C_{S2}\}$ really have no logical function in the sense of timing or gating, but simply serve the role of energizing the ac-gain mechanism in the magnetic storage registers. We refer to these clocks therefore as "pumping clocks," in contrast to the "timing clocks" C_1 and C_2 that effect the actual transfer, via logic circuits, from one storage bank to the next.

It is the need for separate sets of pumping clocks that makes this technique impractical. Let us consider how we may reduce the number of clock pulses that are required.

Combined Clocking System for Timing and Pumping. It is clear that we require the equivalent of what we have called pumping clocks, for in one way or another we must achieve signal gain. But perhaps the same pumping clocks can be used as timing clocks as well. That this is clearly possible can be deduced from our previous study of core-wire shift registers. A shift register is a simple logic circuit, but a logic circuit nevertheless, in which the "next" state of an element is the present state of its neighboring element. Any of the transfer schemes with symmetrical O and E clock phasing, corresponding to two sets of elements that we have generally designated as Odd and Even sets, satisfy the purpose of the argument. We can arrange these two sets of storage elements as in Fig. 10-3. The $E \rightarrow O$ clock pulse is in effect the timing clock

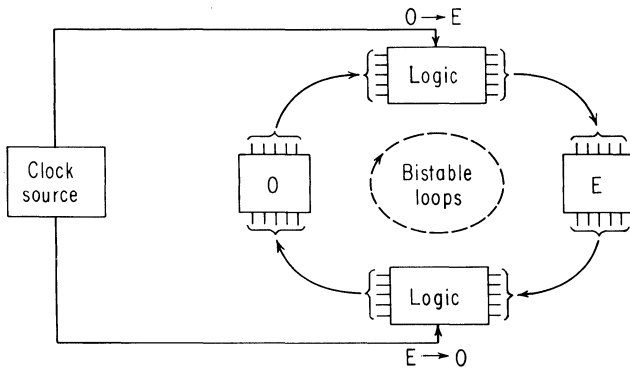


Fig. 10-3. Arranging for a single set of clocks to serve for both flux gain and timing.

Six of these functions, namely $f_0, f_3, f_5, f_{10}, f_{12}, f_{15}$, are trivial in the sense of not being functions of both variables, e.g., $f_{10} = x$. The remaining ten functions can be considered in three groups: those that are *one* for only a single input state, those that are *one* for two input states, and those that are *one* for three input states. These three groups are referred to as AND functions, exclusive-OR functions, and (inclusive) OR functions, respectively, and are written as shown in Table 10-2. The special symbol \oplus is used to specify the exclusive-OR function f_6 , which is *one* only if one or the other, but not both, of the input variables is *one*.

Table 10.2

AND functions	Exclusive-OR functions	OR functions
$f_1 = \bar{x}\bar{y}$	$f_6 = x \oplus y$	$f_7 = \bar{x} + \bar{y}$
$f_2 = x\bar{y}$	$f_9 = \overline{x \oplus y}$	$f_{11} = x + \bar{y}$
$f_4 = \bar{x}y$		$f_{13} = \bar{x} + y$
$f_8 = xy$		$f_{14} = x + y$

Note that functions f_6 and f_9 , which are the complements of each other, can also be written in the form $x\bar{y} + \bar{x}y$ and $\bar{x}\bar{y} + xy$, respectively, i.e., as the OR function of two AND functions. Thus, we see that any function of two variables can be synthesized with the three logical operations NEGATION, OR, and AND. However, by the well-known De Morgan's theorem (which states that the complement of any function can be obtained by: (1) replacing each variable by its complement, and (2) interchanging the symbols for OR and AND), we find that only two of the three logical operations are actually required. For example, we can synthesize the AND function itself in terms of OR and NEGATION, namely $xy = \overline{\bar{x} + \bar{y}}$, so that any function of two variables can be written solely in terms of NEGATION and OR. A similar derivation shows that any function of two variables can also be written solely in terms of NEGATION and AND.

It can be shown that De Morgan's theorem can be applied to functions of any number of variables, and therefore that any function can be synthesized solely with an array of NEGATION and OR circuits, or alternately with an array of NEGATION and AND circuits. This is a well-known result of switching theory.

A final result of importance is that OR or AND circuits with just two inputs are sufficient for general logic synthesis. This is shown from the associative property of the OR and AND functions.

For example, the OR function $(x_1 + x_2 + x_3 + \cdots + x_n)$ can be written in the nested form $(\cdots((x_1 + x_2) + x_3) + x_4) + \cdots + x_n)$, where the OR functions are formed two at a time. The same result applies for the AND function. The availability of circuits that can handle more than two input variables simultaneously, or realize directly such functions as the exclusive-OR function, leads to considerable reduction of system complexity and of the total number of elements required. Nevertheless, we see that this extra capability is not an essential requirement for synthesis of even the most complex functions.

We wish now to introduce various ways of generating the basic logic functions.

OR Function. Formation of an OR function of two or more variables implies that the receiver element is set to the *one* state if any one or more of the transmitters are in the *one* state. A common technique for achieving this function with semiconductor elements is to merge the various input signals through a diode network. Applying this principle to core circuits, we obtain the core-diode circuit of Fig. 10-4(a). In this case, if more than one transmitter holds a *one*, then the mmf drive on the receiver during transfer is accordingly higher.

It is also possible to merge the outputs in series instead of in parallel, as in Fig. 10-4(b), in which case no mixing diodes are needed. Now, multiple *one* transmission results in flux summation, as compared with mmf summation in Fig. 10-4(a).

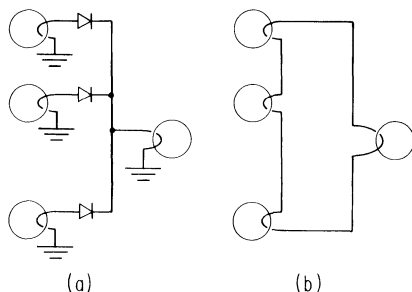


Fig. 10-4. Synthesis of the logical OR function; (a) parallel input (mmf summation), and (b) series input ($\Delta\phi$ summation).

In analyzing any particular OR configuration, the primary concern is that the receiver be properly set if any number of trans-

mitters are in the *one* state. With either of the above arrangements the general performance deteriorates as the number of transmitters increases, primarily because of the increased level of $\Delta\phi$ transfer for the *zero* state. If we let δ represent the nominal magnitude of $\Delta\phi$ for zero transfer, then with n transmitters in series, the all-*zero*-state flux is $n\delta$ and an amount of flux $(n - 1)\delta$ must be clipped in order to restore the same *zero* level as for a simple transfer. If n is very large, then for a single transmitter in the *one* state, the received flux is the difference between the two relatively large numbers, and the operation is sensitive to small differences from core to core.

For two input variables, the series OR connection for the MAD-R scheme takes the form indicated in Fig. 10-5(a). For $x = 0$ and $y = 1$, priming results in flux switching along the dashed line of the network representation in Fig. 10-5(b). After priming, flux states in D_x and D_y are in opposite directions with respect to their common node and, hence, the driving of D_y would tend to switch flux in D_x . However, the advance-drive generator in the D_x circuit prevents such switching, and the full flux linkage from y is therefore directed to the receiver. In other words, with only a single transmitter in the *one* state, there is nominally no effect from the presence of the second transmitter.

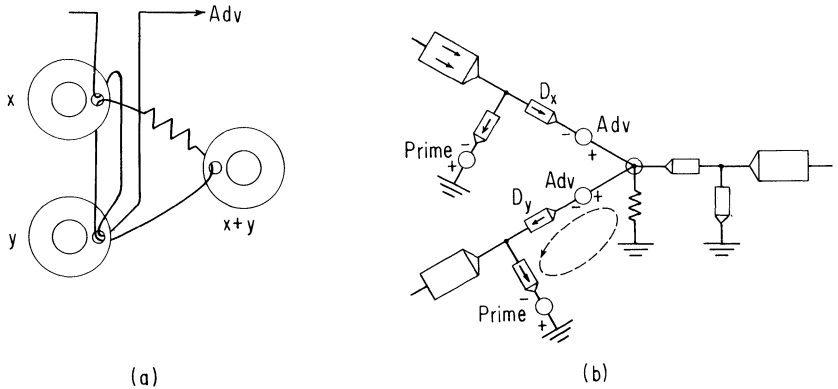


Fig. 10-5. Series OR connection for MAD-R logic.

In the circuit of Fig. 10-5(a), the transmitters are coupled by a single coupling loop and primed flux from both transmitters dissipates in a common loop resistance. In terms of the network representation, we see that flux from both transmitters is summed in

only one of the input legs of the receiver. By network manipulation we can derive a more symmetrical input arrangement, as in Fig. 10-6(a), where both input branches of the receiver are symmetrically linked. In the corresponding circuit (Fig. 10-6(b)), the transmitter coupling loops are isolated, each linking a receiver input leg separately. Because of the separate resistance in each of the two loops, full priming in the double-*one* case here will take no more time than the priming of a single *one*, whereas full priming in the double-*one* case of Fig. 10-5(a) would nominally be twice as long as for a single *one*.

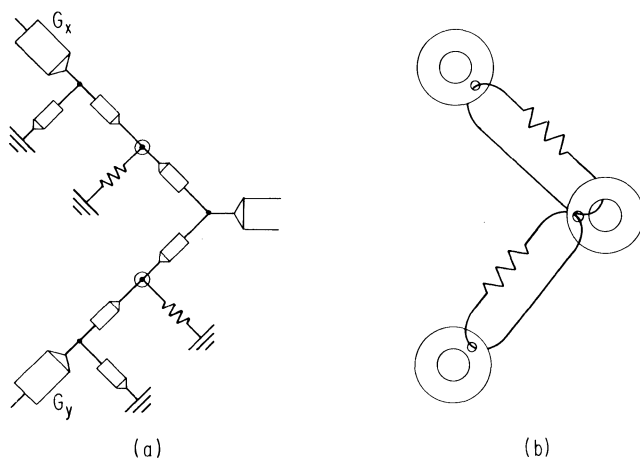


Fig. 10-6. Series OR connection for MAD-R logic with independent inputs merging in the receiver element.

In a direct core-wire equivalent of the parallel connection scheme of Fig. 10-4(a) we substitute a core for each diode element, as shown in Fig. 10-7(a). It is possibly easier to understand the operation in this case if the circuit from each transmitter is visualized as being linked to the receiver separately with the same number of receiver turns, as in Fig. 10-7(b). Now we see that if the receiver is switched from one of the inputs, flux is injected into the other input loop and is absorbed by the input "diode core" with very small current flow. In the double-*one* case, there is nominally double mmf drive on the receiver. The input cores can be incorporated into the receivers as in Fig. 10-7(c), where each winding now couples through a separate input aperture.

By combining the OR schemes of Figs. 10-5 and 10-7, we can compound the input mixing, as in Fig. 10-8(a), where we illustrate

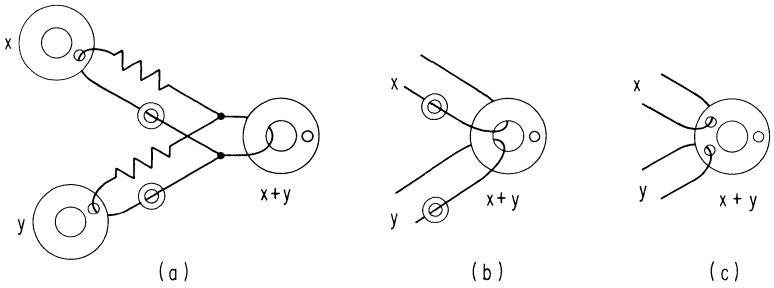


Fig. 10-7. Parallel OR connection for MAD-R logic.

the synthesis of a four-input function $(w + x) + (y + z)$. The other two-input OR functions, $\bar{x} + y$, $x + \bar{y}$, $\bar{x} + \bar{y}$, are also easily synthesized. For example, $\bar{x} + y$ can be derived with parallel input in the form of Fig. 10-8(b) where the flux-source negation technique of Sec. 8-1 is indicated.

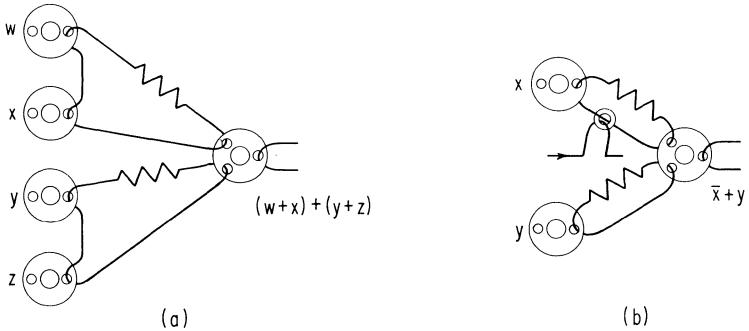


Fig. 10-8. OR functions: (a) combined series-parallel input of four variables, and (b) application of negation transfer to one input.

AND Function. For the AND function, the receiver is to be set only if all of the transmitters are in a state to transmit flux. Either of the elementary OR circuits can be converted to an AND circuit merely by establishing a suitable mmf or $\Delta\phi$ threshold, as shown for two-input circuits in Figs. 10-9(a) and 10-10(a), respectively. In the first circuit we apply a negative bias $-i_T$ to the receiver (where i_T is the nominal transmitter output current in the case of a one) so that the receiver is set only if mmf coincidence occurs in both transmitter loops. In Fig. 10-10(a) we insert into the loop a negative flux source of nominal capacity $N_S \Delta\phi_S = -N_T \Delta\phi_T$ (where

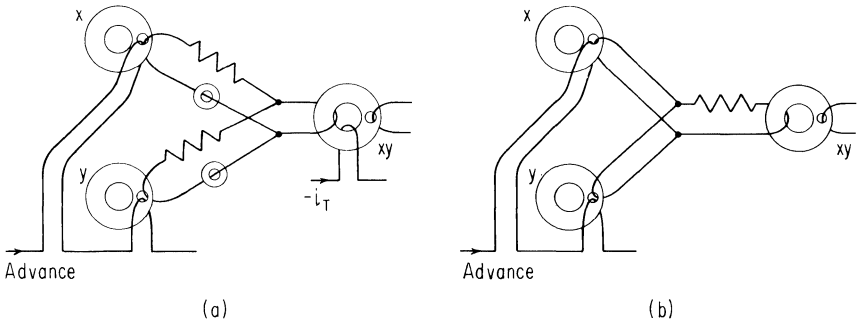


Fig. 10-9. Synthesis of the logical AND function: (a) parallel input with mmf bias; (b) elimination of "diode cores" and of the need for mmf bias.

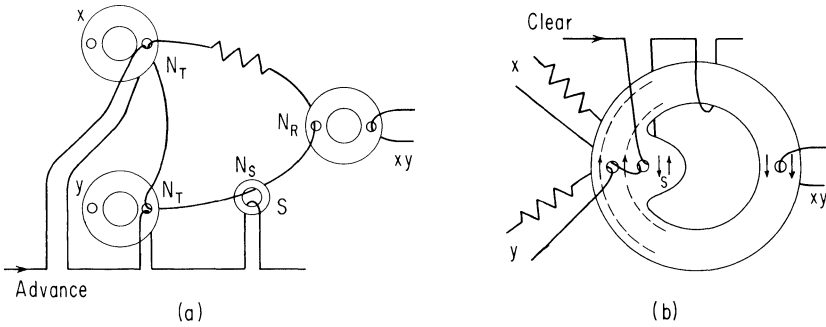


Fig. 10-10. Series AND connection: (a) with a separate flux source, and (b) with the flux source incorporated into the receiver.

$\Delta\phi_T$ is the nominal *one* signal level) so that the receiver is again prevented from switching except for coincidence of flux transfer from both transmitters.

The term "coincidence" is intended to refer to information and not necessarily to time, although for the circuit of Fig. 10-9(a) the mmf signals must also be coincident in time. This difference in current-threshold and flux-threshold operation comes about because of the capability for flux storage but not for current storage. For example, if the source S has a low threshold and is left undriven at the time of transfer, then the transmitters can be driven sequentially. The first transmission would switch the $\Delta\phi$ source (or rather, in this case, the $\Delta\phi$ sink), with small current, and the second transmission would result in a loop current large enough to switch the receiver.

The parallel input arrangement of Fig. 10-9(a) can actually be realized without the use of an mmf threshold, simply by eliminating the input diode elements, as in Fig. 10-9(b). Now if both transmitters are primed to the *one* state, then during transfer both output currents sum to set the receiver. But if only a single transmitter is in the *one* state, the other acts as an effective shunt (short circuit) and there can be no transfer. In fact, for zero-resistance transmitter windings it would not even be possible to prime either transmitter unless both primed together, since a *zero*-state element would also be a short circuit during priming. This method of achieving an effective threshold is preferable to applying a negative bias directly to a receiver, because in the latter case loop currents, and hence losses in loop impedance, are much larger.

We can transform the series circuit of Fig. 10-10(a) to the separate input arrangement of Fig. 10-10(b), for two inputs, in the same manner as we did in Fig. 10-6 for the OR circuit. The flux sink, which takes the form of Leg S, switches and become saturated by the first unit of input flux. Flux switches around the main aperture, therefore, only if both input legs are switched. (The opposing arrows in Leg S merely indicate a demagnetized state initially.) Although this is a practical circuit arrangement, the circuit in Fig. 10-10(a) is the one found most useful to date mainly because of its reliance on a simpler multiaperture core shape.

Exclusive-OR Function. The two-input exclusive-OR function is similar to the inclusive OR function except that for an input of two *ones*, the output is again *zero*. A way to accomplish this is to arrange for the $\Delta\phi$ signals representing two input *ones* to cancel each other, but yet result in transfer if either input variable alone is a *one*. Another way is to employ $\Delta\phi$ summation as for OR, but to make provision that the two input *ones* cause saturation or blocking at the output of the receiver stage, just as for an input of two *zeros*.

We can achieve $\Delta\phi$ opposition in a coupling loop by arranging the two transmitter windings with opposite polarity, as shown in Fig. 10-11. But now the induced loop mmf are of opposite polarity for the two cases of a single *one*, implying the need for some type of rectification in order that either polarity input can set the receiver R through the same input winding. A straightforward method is to insert a bridge rectifier into the circuit, as shown in the figure. The dashed line shows the path of current flow for the case $x = 1, y = 0$.

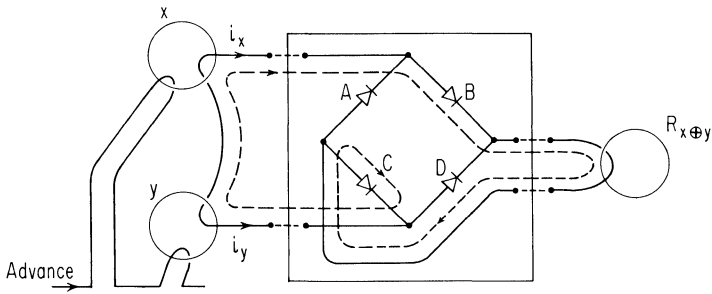


Fig. 10-11. Synthesizing the exclusive-OR function with a diode bridge input.

Replacing each diode with a core, and providing isolating windings on Cores A, C, and R, we obtain the circuit of Fig. 10-12(a), with the corresponding network of Fig. 10-12(b). The latter is shown rearranged in Fig. 10-12(c), where Cores A and D are given the same label, $L_1/2$, since they switch identically, as is true also for Cores B and C, which are labeled $L_2/2$. From this form it is clear that an alternate circuit realization to Fig. 10-12(a) is that shown in Fig. 10-13(a). (Recall the derivation illustrated by

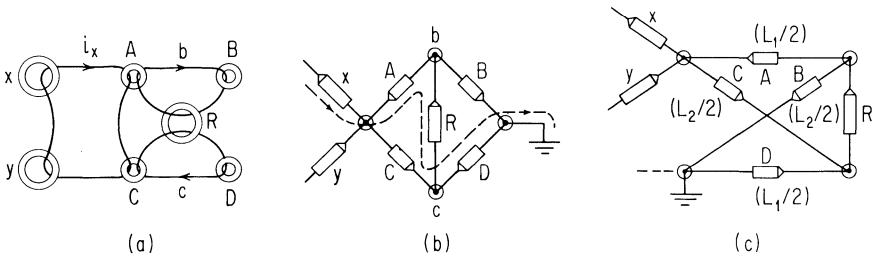


Fig. 10-12. Core-wire synthesis of the bridge of Fig. 10-11.

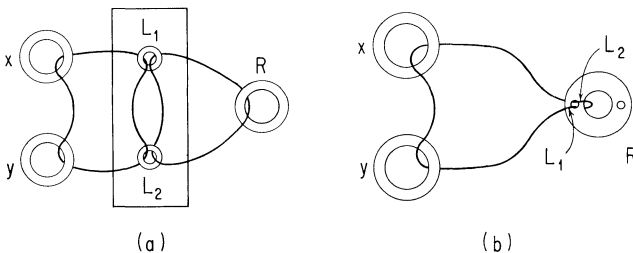


Fig. 10-13. Exclusive-OR: (a) alternate circuit realization of lattice network of Fig. 10-12(c), and (b) incorporating cores L_1 and L_2 into the receiver element.

Fig. 5-14.) In terms of the equivalent orthogonal-mode arrangements of Fig. 8-10, we see that the cores L_1 and L_2 can be integrated into a single multileg receiver core with a figure-eight input winding, as in Fig. 10-13(b). (In this form, it is readily evident that either polarity of input will set the receiver.)

Thus far we have considered a bridge network at the input of the receiver, though the bridge could also be used on the output of the receiver, as shown in Fig. 10-14(a), corresponding to a figure-eight winding linking the output (Fig. 10-14(b)). However, whereas in Fig. 10-12(c) the x and y inputs are opposed to one another, in Fig. 10-14(a) the x and y inputs connect symmetrically and their flux contributions sum up in setting the two output legs L_1 and L_2 . Thus, with a single input *one*, a full unit of flux is available for priming and subsequent transfer, as indicated by the primed state shown in Fig. 10-14(a). But with two units of input flux, priming is again blocked, just as with no inputs, and clearing both output legs results in no net signal at the output of the bridge (recall that in Fig. 10-12(c), the double-*one* case results in no flux transfer *into* the bridge).

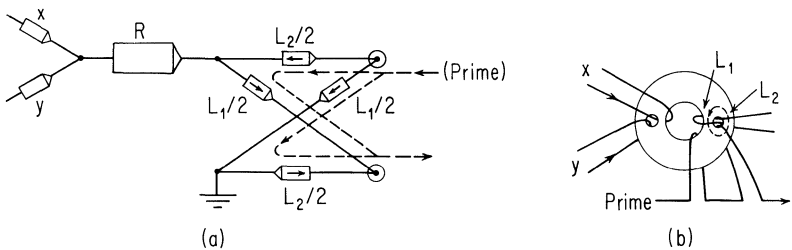


Fig. 10-14. Synthesis of exclusive-OR with a bridge network at the output. In (b), internal arrows show primed state for input of a single *one*.

Fan-Out. Fan-out ratio refers to the number of receivers that can be set from a single transmitter. A fan-out ratio of 2:1 is sufficient for general system design, though higher ratios lead to more efficient design (without necessitating repeated branching in order to achieve effectively higher fan-out ratios).

In Fig. 10-15(a) and (b) are shown series fan-out and parallel fan-out circuits, respectively. In the series circuit, loop current induced by driving the transmitter tends to set the two receivers equally. To obtain the same flux-transfer gain for each receiver that would be obtained with only a single receiver in the circuit, the transmitter turns must at least be doubled. For a given level

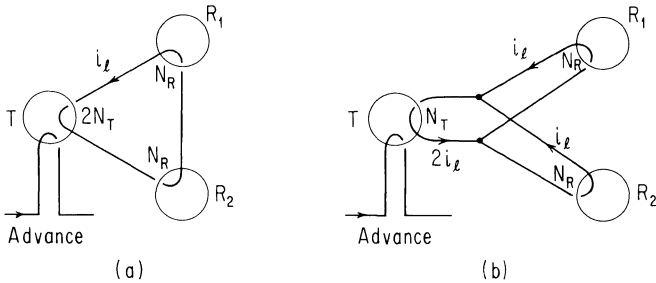


Fig. 10-15. Series and parallel fan-out.

of loop current, this implies at least a doubling of transmitter load mmf (or in general for n receivers an n -fold increase in loading). In the parallel circuit, the transmitter turns may remain nominally unchanged, though again there is a doubling of load mmf for the same input current to each receiver. Thus, it can be concluded that for either type of circuit, the maximum "gain-excess product" (Sec. 4-5) is only half as great as for the case of single transfer; or in general, $1/n$ times that for single transfer. This reduction results in lower current tolerances, and for this reason fan-out ratios of more than two or three in a single step are seldom used in practical core-wire circuits.

It is possible to maintain the basic current tolerances with fan-out > 1 , though at the cost of increased time for transfer, or for priming, depending on the scheme. Each mmf-limited phase may, for example, be divided into a number of sub-phases equal to the fan-out ratio required. Thus, in Fig. 10-16 the advance pulse $(O \rightarrow E)_1$ reverses flux locally around the upper output aperture and transfers to Receiver R_1 , but without significant effect on the flux condition at the other output aperture or in the remainder of the core. Transfer to R_2 is accomplished subsequently with the advance $(O \rightarrow E)_2$ pulse. Each transfer therefore has properties similar to simple transfer. The cost is an n -fold multiplication of advance drivers and time for completing the transfer. (This type of subclock fan-out is employed in the system described in Sec. 10-5.)

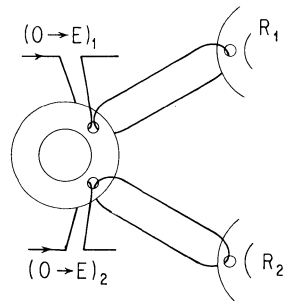


Fig. 10-16. Increasing fan-out by means of subclocks.

Bipolar Logic Synthesis. In Chap. 9, we noted that bipolar transfer is usually

used with the aid of dynamic bias, and that with dynamic bias, flux is easily steered with relatively small mmf through one or the other of two equal paths. Extending this approach, as discussed by Newhall (1963), we can divide each of these branches again and use still another input signal to steer flux through these new legs. Thus, with two input currents i_1 and i_2 (associated with input variables x_1 and x_2 , respectively), flux can be steered to any one of the four equal legs of Fig. 10-17. For $+i_1$ (implying $x_1 = 1$), $\Delta\phi$ is steered through the right-hand branch, and for $-i_1$ (or $x_1 = 0$), $\Delta\phi$ is steered through the left-hand branch. In each of these branches, input current i_2 in turn determines whether $\Delta\phi$ shall switch through the left- or right-hand sub-branches. We readily see, then, that flux switches through the extreme left branch only if $x_1 = x_2 = 0$, or $\bar{x}_1\bar{x}_2 = 1$. This branch is therefore labeled $\bar{x}_1\bar{x}_2$. Similarly, the other branches are labeled \bar{x}_1x_2 , $x_1\bar{x}_2$, and x_1x_2 , respectively. To form an output function, we simply link with one polarity those legs corresponding to *ones* in the truth table, and the remaining legs with the opposite polarity. This will result in a plus or a minus output, i.e., a bipolar output, for every possible input state. For example, formation of $S = x_1\bar{x}_2 + \bar{x}_1x_2 = x_1 \oplus x_2$ and $C = x_1x_2$, that is, the sum and carry functions for a two-input adder, are shown in Fig. 10-17.

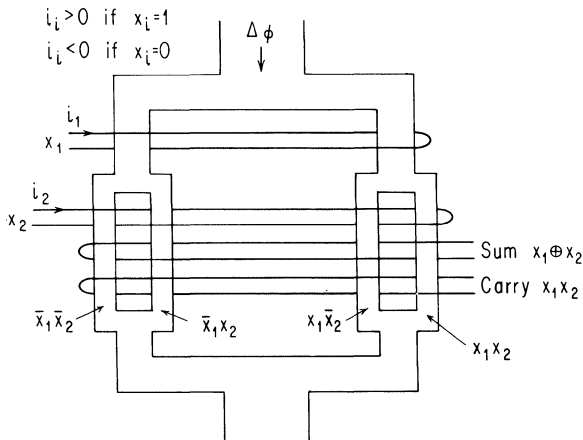


Fig. 10-17. Logic synthesis based on flux steering

While this arrangement is logically correct, we must note an important unbalance effect when a winding links a different number of legs in one direction than the other; namely, for $i_1 = i_2 = 0$,

the output flux linkage will no longer be zero even though $\Delta\phi$ divides equally between the four legs. In other words, the flux-gain curve does not pass through the origin, as in the curve of Fig. 9-2, and this can seriously reduce the otherwise wide range of operation that is possible. The unbalance can be lessened in two ways. In the case of the carry winding, for example, the right-hand leg could be linked with three turns, so that the net $\Delta\phi$ linking the output winding would be zero even with equal flux division. A second technique is to provide a flux-source core of capacity $\Delta\phi/2$ in series with the carry winding. With either method, however, the output currents themselves tend to unbalance the steering currents, because the output currents add in different combinations on the various legs and therefore result in different net values of mmf on these legs.

With this synthesis technique there are potentially 2^n legs required, where n is the number of input variables involved, though in many cases it would not be necessary to have all legs available separately. For the AND function of Fig. 10-17, for example, the three left legs are similarly linked and need not be separately provided, if not otherwise needed for the formation of other output functions.

The threshold methods for logic synthesis discussed above for unipolar synthesis can also be applied to bipolar synthesis. Although we have discussed threshold logic for only two input variables, a more general theory for any number of input variables exists. In the general threshold synthesis of logic, a set of input variables are weighted and summed, the result being a *one* if the sum passes some threshold, and *zero* otherwise.

Applying this method to the bipolar scheme of Fig. 9-1, we realize the AND function for three variables as in Fig. 10-18, where there is a coupling core for each input variable, a core for bias, and a loop core Z in which the output function is formed. The flux linkage from each input core is ± 1 unit. The schematic core form implies a core of the type discussed

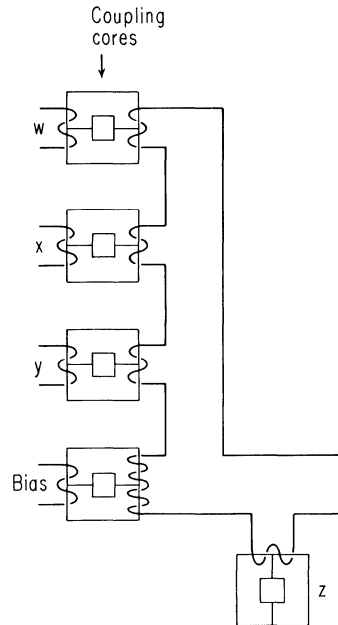


Fig. 10-18. Majority-logic synthesis of bipolar logic circuits.

earlier in connection with Fig. 8-16(c). In this case, the bias core is doubly linked in order to provide -2 units of flux linkage. (It is assumed that the bias signal has the same form and amplitude as the variables, but of fixed polarity.) The net magnitude of flux linkage transferred to Core Z depends on the input state, and can vary from -5 units for $w = x = y = 0$ to $+1$ for $w = x = y = 1$. To accommodate this variable magnitude of flux linkage, either the flux capacity of the Z element must be made appropriately larger, or else for some input combinations the Z core saturates before the coupling cores are fully switched, and switching in the coupling cores then becomes heavily loaded. Where these same cores are not used for other output functions simultaneously, this may be permissible; however, where several output circuits are excited simultaneously, early termination of switching in one circuit can significantly affect the proper operation of the others. In any case, note that here too, as in Fig. 10-17, the output current differentially affects the switching of the various coupling cores, and it may be difficult to maintain the high tolerances that are achieved in simple register circuits.

The potential for bipolar circuits is not yet clear. It will depend eventually on the practical trade-off between increased complexity and the net improved performance actually achievable.

10-5 Design Example: Decimal Arithmetic Unit

We will describe briefly a system design that illustrates clearly a number of the circuit and logic principles discussed earlier. This system was purely experimental and, in fact, was the first core-wire system of any size ever built. The function of the unit was to provide decimal addition, subtraction, and multiplication under control of a manual keyboard. The circuit design and logic design (based on an extension of the nonresistance MAD-N scheme) are discussed in detail by Crane and Van De Riet (1961) and Crane (1961), respectively. The main purpose here is to note some of the main points of the design.

The entire system was built with a single type of circuit module that formed the OR function $x + y$ of two inputs and could transmit $x + y$, or $\overline{x + y}$, independently to each of three receivers. To assure sufficient flux gain for the relatively long coupling loops in the machine, the multileg flux-doubling circuit of Fig. 5-25 was adopted. Thus, each circuit module consisted of two identical multileg cores. The cores that were used had four minor apertures,

which were assigned one for input and three for output. Fan-out was achieved by the use of subclocks, in the manner of Fig. 10-16, and only a single receiver was driven from each corresponding pair of transmitter apertures. The basic clock system thus had the form $(\square \rightarrow \circ)_1, (\square \rightarrow \circ)_2, (\square \rightarrow \circ)_3$, Clear $\square, (\circ \rightarrow \square)_1, (\circ \rightarrow \square)_2, (\circ \rightarrow \square)_3$, Clear \circ, \dots , where symbols \square and \circ are substituted for the more familiar E and O symbols (for Even and Odd). The (\square, \circ) notation leads to simpler logic diagrams since we can readily show which phase a particular module belongs to, simply by drawing the module directly in the \square or \circ shape.

To minimize the effects of variable coupling-loop impedance, due to the wide range in physical coupling-loop length, the approach taken was to achieve minimum possible impedance through the use of strip transmission lines, and to synthesize the required low-level flux loss, required for bistability, by the use of flux-clipper cores, as in Fig. 3-6.

The basic circuit arrangement can be seen in Fig. 10-19. The cores are mounted in pairs, in the manner shown in Fig. 10-19(a), where each pair represents one circuit module, that is, one flux-doubling circuit. All of the $\square \rightarrow \circ$ coupling loops are wired on one side of the board and all $\circ \rightarrow \square$ coupling loops are wired on the opposite side of the board. The actual wiring takes the form shown in Fig. 10-19(b). Single-turn transmitter windings and single-turn receiver windings are used exclusively, the coupling loop itself being in the form of a strip transmission line (made of copper shim stock with plastic tape insulation). Each coupling loop incorporates a single-toroid flux clipper. Negation transfer is achieved by the use of a flux source, as discussed in Sec. 8-1, so that those loops wired for negation transfer also incorporate a flux source, which consists of a stack of five toroids, each the same as the clipper core.

The multileg cores are shown schematically in Fig. 10-19(c), with all three output apertures drawn close together, and offset, for convenience of drawing. Each transfer from a given circuit module is at a different subclock phase, and all clipper cores and flux-source cores are arranged spatially into three separate columns according to whether they belong to the $(\square \rightarrow \circ)_1, (\square \rightarrow \circ)_2$, or $(\square \rightarrow \circ)_3$ subclock phase. This facilitates straight-through wiring of large groups of modules at once. Assuming that the upper and lower left-hand modules hold variables x and y , respectively, then according to the wiring sketched in Fig. 10-19(c), we see that $x + y$ is formed in the upper right-hand module, and $x + \bar{y}$ is formed in the lower right-hand module. Variable x is transferred to the

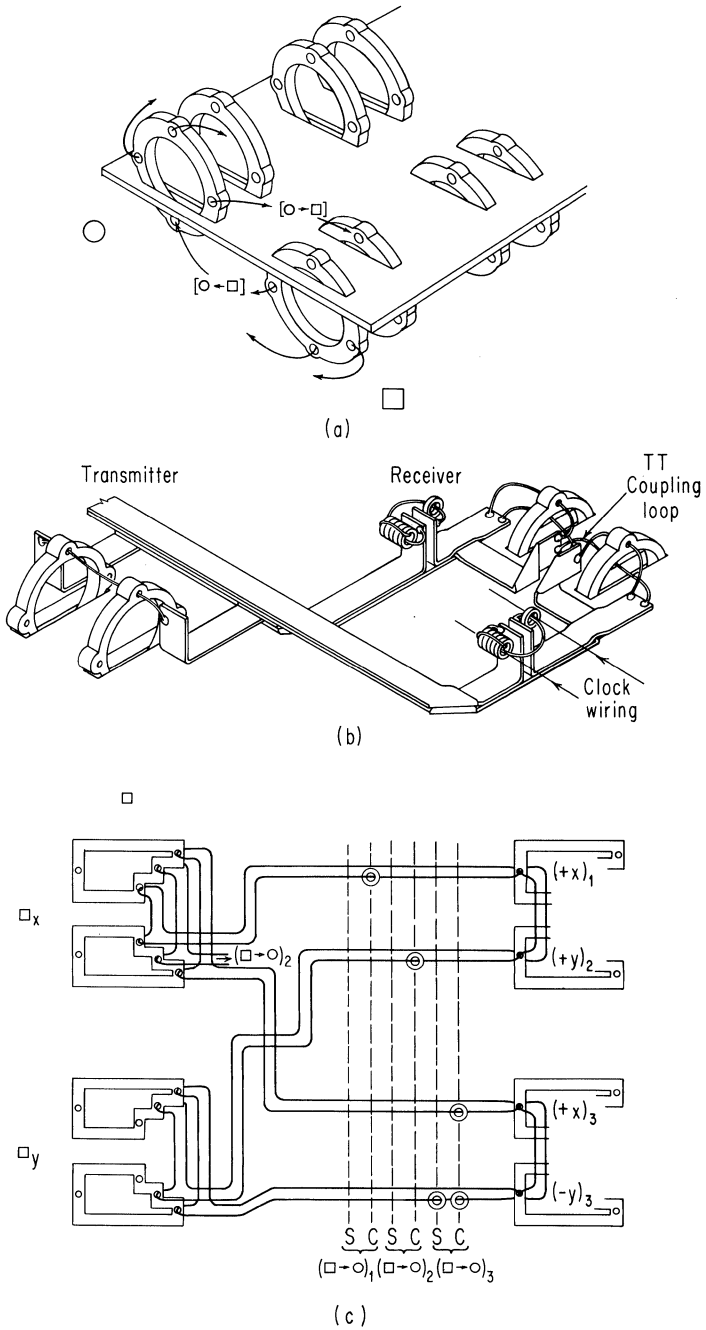


Fig. 10-19. Circuit design of decimal arithmetic unit: (a) three-dimensional view of element layout, (b) coupling-loop construction, and (c) transfer-circuit detail.

upper and lower modules on the first and third subphases, respectively, and y is transferred on the second and third subphases, respectively. (The actual clock-drive wiring is not shown on the figure.) Following the ($\square \rightarrow \circ$) transfer, the OR function is formed in each of the right-hand modules by transmitting between the two receiver cores of each module, as discussed in connection with the TT operation of Fig. 5-25. Thus, if either core of the module had been set, then both become set, and we thereby synthesize the OR function.

The overall logic schematic is shown in Fig. 10-20. The abbreviations IER, ICAND, and PROD stand for multiplier, multiplicand, and product, respectively. The ICAND is stored in a bank of ten-bit shift registers, where the position of a single *one* in each register represents the decimal digit. The PROD registers hold decimal numbers in a biquinary representation. Each line on the diagram represents a single coupling loop. Double lines between a pair of modules represents double transfer, i.e., at two different phases, which of course is logically redundant, but nevertheless increases the net flux gain. A dot on the line near the transmitter indicates NEGATION transfer. A pair of \circ and \square symbols within a larger rectangle indicates a one-bit negation register (negation coupling not shown), which forms a logical flip-flop in the sense discussed in Sec. 10-3. The flip-flop holds its state until explicitly changed by one of its inputs.

The basic operation is as follows: Each keyboard operation starts the clocks (see START signal in lower right of diagram), which run until a STOP signal is obtained (right center of diagram). When any keyboard button is pressed, current flows through certain set and reset windings which sets up the machine for the particular operation (in the manner of presetting flip-flops in a transistor machine). The set-up current also sets the toroid at the lower right. Release of the keyboard button resets this core and sends a signal to start the clock generators. This assures that all cores are properly reset before the generator starts and eliminates any problems from switch bounce.

For multiplication, each digit of the IER is entered separately, and the partial products from this IER are added to the PROD registers, in proper registration, before the next IER digit is entered. If the IER digit were a 5, for example, then the ICAND registers would cycle, i.e., shift, completely five times, adding their contents into the PROD registers once each cycle. On the last, i.e., the fifth cycle, the ICAND registers are connected end-to-end, and the ICAND shifts one decimal place, ready for the next IER entry. After each IER entry, the clocks remain energized for

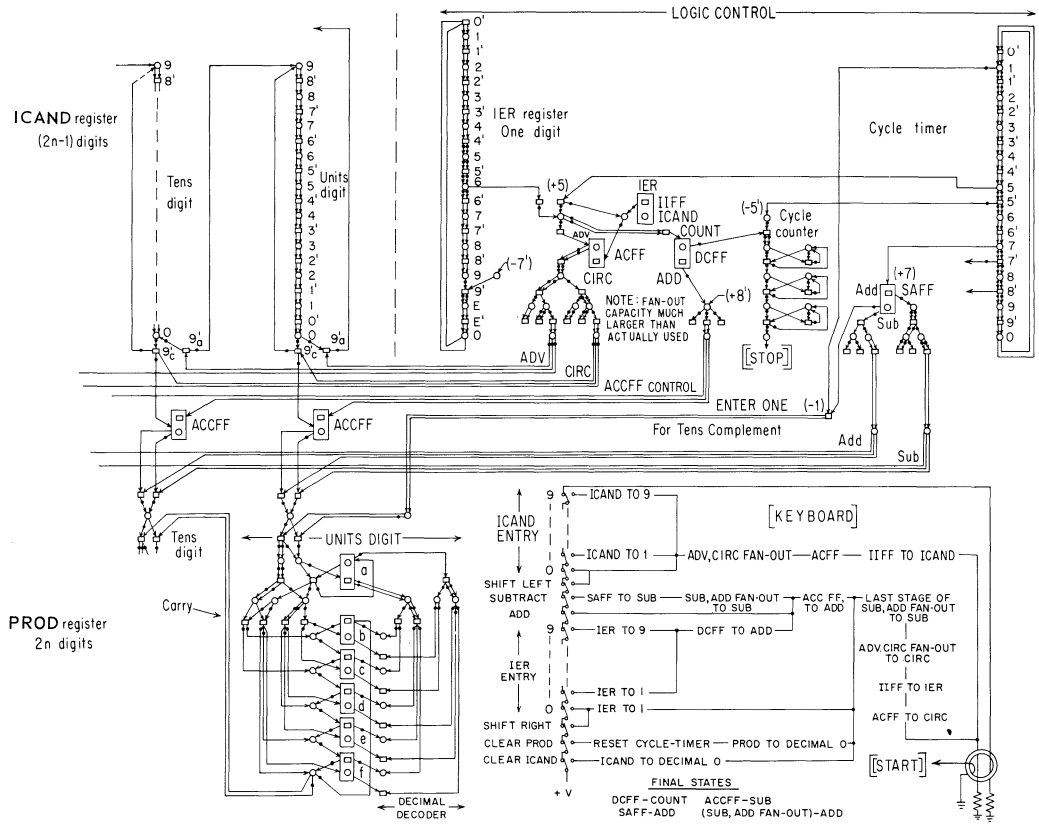


Fig. 10-20. Logic schematic of decimal arithmetic unit.

eight more "dummy" cycles to allow for the maximum possible carry propagation delay in the PROD registers for $n = 10$, that is, a 10 by 10 digit multiplication. Timing of these extra eight cycles is accomplished by the "cycle counter," which consists of a chain of three binary scalars that count to $2^3 = 8$. (Synthesis of a binary scaler is discussed in connection with Fig. 10-22(a).)

Because of the relatively small fan-in and fan-out, logic functions are built up relatively slowly, as discussed earlier. Thus, some of the flip-flops in the "logic control" section are controlled by tap-offs from the cycle-timer, and these tap-offs must be chosen so that the flip-flop state is changed at just the right time. For example, some of these flip-flops control the gating between the ICAND and PROD registers. To exercise gate control of $(2n - 1)$ ICAND registers require several stages of fan-out, as shown by the fan-out networks at the bottom of the logic section. To have these control signals available at the proper moment, the flip-flop gating must in turn occur at the proper earlier moment. Although this seems to lead to a complex design problem, there are some simple tricks that greatly facilitate the design. For example, note in Fig. 10-20 that only \square elements or \circ elements appear across any given horizontal row. This synchronizes all (vertical) movements of ones in the various registers and timers so that, in fact, tap-off points for control are automatically determined.

Although not shown in the diagram, all ICAND and PROD registers incorporate a nondestructive readout in the manner discussed in Fig. 6-8. Thus, the decimal numbers held in the ICAND registers are displayed visually in a one-out-of-ten code. For a similar display for the PROD registers, each biquinary PROD register has a built-in decimal decoder, as shown in the figure. Thus, the results of each operation are immediately visible on incandescent lamps.

Though this system operated quite well, and demonstrated that large-scale systems were at least feasible, it is clearly not a practical approach because of the large number of clock drivers required, the need for two cores per stage, and the need for strip transmission-line wiring to maintain low losses. In the next section we will see that with the MAD-R approach (which was not well developed at the time this first experimental system was built), we require only two clock drivers, have far greater tolerance in coupling-loop construction, require only one core per stage, and can achieve very wide operating tolerances over a large temperature range.

10-6 Extension of the MAD-R Scheme to General Logic Synthesis

We now wish to consider more explicitly the logic capabilities of MAD-R circuits, and to provide some notes on extension of the circuit-design method of Secs. 6-5 to 6-8.

A Configuration for Synthesizing All Two-Input Logic Functions. We have already seen how to realize the ten nontrivial functions of two variables. The circuits for at least two of these, for example, $\bar{x} + y$ in Fig. 10-8(b) and xy in Fig. 10-10, make use of flux sources in the coupling loops. We will now show how the type of AND circuit in Fig. 10-10, when generalized to the circuit of Fig. 10-21, can be designed—by choice of windings, polarities, and size of the flux source—to yield any one of the two-input logic functions (Nitzan and English (1967)).

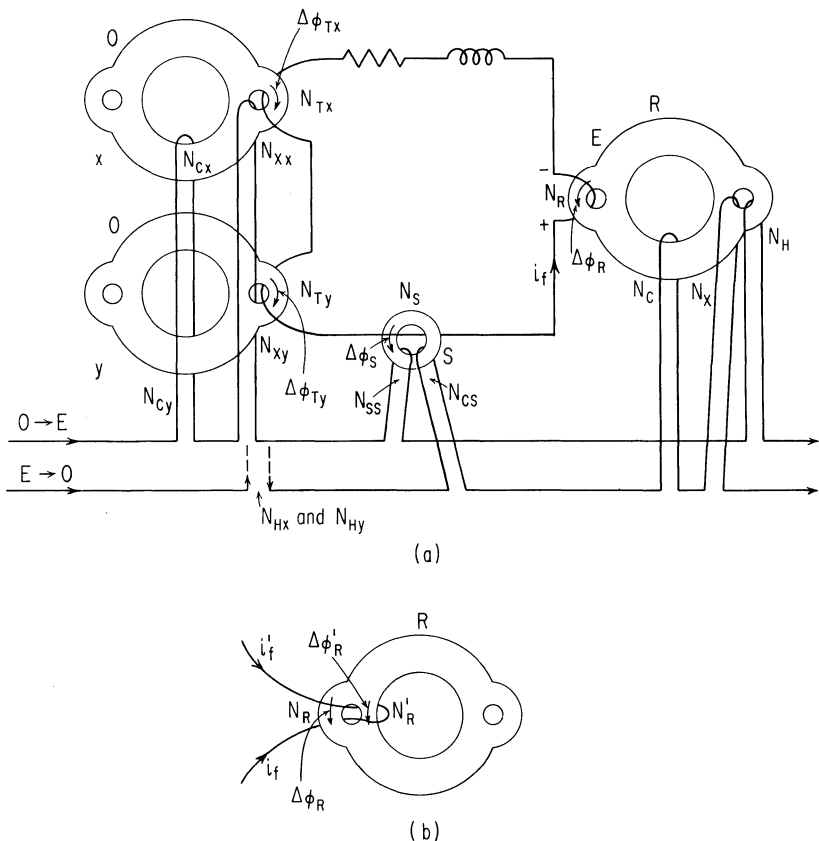


Fig. 10-21. MAD-R configuration for realization of any two-input logic function.

The general form of coupling loop shown in Fig. 10-21(a) is used for realizing all two-input logic functions except the exclusive-OR functions $x \oplus y$ and $\overline{x \oplus y}$, which, in line with Fig. 10-13(b), are realized with the same basic circuit modified for a figure-eight input winding, as shown in Fig. 10-21(b). The transmitter windings N_{Tx} and N_{Ty} are in each case 2, 0, or -2 turns, as shown in Table 10-3. The input winding N_R is just a single turn (or a single-turn figure-eight winding). The ratio of source flux linkage to transmitter flux level has the nominal values shown in the table. The assumptions resulting in these nominal values, along with the procedure for designing more exact values of $N_S \Delta \phi_S$ and specifying coupling-loop impedance, are covered in the next subsection.

Table 10.3

$f(x,y)$	x	\bar{x}	xy	$\bar{x}y$	$\bar{x}\bar{y}$	$x+y$	$\bar{x}+\bar{y}$	$\bar{x}+\bar{y}$	$x \oplus y$	$\overline{x \oplus y}$
N_{Tx}	2	-2	2	-2	-2	2	-2	-2	2	2
N_{Ty}	0	0	2	2	-2	2	2	-2	-2	2
$N_S \Delta \phi_S / \Delta \phi_T$	0	2.5	-2	0.5	3	-0.5	2	4.5	0	-2.5

Designing Coupling Loops and Flux Sources. We will now show a simple extension of the design method of Sec. 6-6 to the more general circuit of Fig. 10-21, in order to explain Table 10-3 and to indicate how to obtain quantitative designs of coupling-loop parameters R_ℓ , L_ℓ , and $N_S \Delta \phi_S$. The basic approach is to assume that good operation is achieved by the design methods of Chap. 6, for the case of a single transmitter, and proceed to see what additional design criteria must be met in order to obtain similarly good operation for each case of the general two-input logic circuit of Fig. 10-21. We will see that it is possible to specify a value of flux source for each logic function such that the worst case of *zero* transfer matches the *zero* transfer for the single transmitter case, and, under the same conditions, the *one* signal then also matches the single-transmitter case. This is true at least for every function except the exclusive-OR and its inverse. (In these two cases, the available *one* signal is somewhat lower, implying the need for a lower loop impedance (lower R_ℓ and L_ℓ) and hence longer priming time than for any other logic circuits.) Application to general logic circuits of design parameters obtained from simple register measurements—sometimes termed *similarity* design—usually results in an excellent first cut for design of a logic circuit.

The basic coupling-loop equation of Eq. (6-9) is expanded to the following form for the two-input circuit of Fig. 10-21:

$$N_{Tx} \dot{\phi}_{Tx} + N_{Ty} \dot{\phi}_{Ty} + N_S \dot{\phi}_S - N_R \dot{\phi}_R = R_\ell i_f + L_\ell \frac{di_f}{dt} \quad (10-1)$$

One or more of the values of N_{Tx} , N_{Ty} , or N_S may be negative, corresponding to winding polarities opposite to those shown in Fig. 10-21(a). With no loss of generality, N_R may be assumed positive, except in the two cases of a figure-eight input winding, where the receiver input winding may be assumed to have two values, N_R and N'_R , of opposite polarity.

Integrating each term of Eq. (10-1) to time t_2 , in the sense of Fig. 6-11, and substituting from Sec. 6-6 the expressions $F_{0S} = N_R i_f(t_2)$ and $\Pi_R = N_R q_f(t_2)$, for the stop-switching mmf and receiver charge-turns, respectively, we obtain

$$\Delta\phi_\ell = N_{Tx} \Delta\phi_{Tx} + N_{Ty} \Delta\phi_{Ty} + N_S \Delta\phi_S - N_R \Delta\phi_R = \frac{R_\ell \Pi_R + L_\ell F_{0S}}{N_R} \quad (10-2)$$

where $\Delta\phi_\ell$ represents the net flux linkage that must be absorbed by dissipation in R_ℓ and storage in L_ℓ (at time t_2). For the case of only a single transmitter, and no flux source, we have $\Delta\phi_{\ell 1} = N_T \Delta\phi_T - \Delta\phi_R$ for transfer of a *one* and $\Delta\phi_{\ell 0} = N_T \Delta\phi_{T0} - \Delta\phi_{R0}$ for transfer of a *zero*, where $\Delta\phi_T$ and $\Delta\phi_R$, and $\Delta\phi_{T0}$ and $\Delta\phi_{R0}$ represent, respectively, the *one* and *zero* flux levels produced by the transmitter and absorbed by the receiver. We assume here that $\Delta\phi_T = \Delta\phi_R$. ($\Delta\phi_T$ is not necessarily the same as $\Delta\phi_R$ primarily because of flux clipping in the receiver. However, the difference is generally small for high-level *one* transfer, so that setting $\Delta\phi_T = \Delta\phi_R$ is actually a good assumption.)

We now state a simple, but important, *zero* flux-level condition. It has been found experimentally that good shift-register performance is achieved in almost all cases if the transmitter *zero* output is limited to no more than

$$\Delta\phi_{T0} = 0.25 \Delta\phi_T \quad (10-3)$$

and if enough flux-clipping occurs in the receiver to allow *zero* receiver flux

$$\Delta\phi_{R0} = 0.1 \Delta\phi_R \quad (10-4)$$

For the worst-case condition encompassed by Eqs. (10-3) and (10-4), and following the assumption that $\Delta\phi_R = \Delta\phi_T$, then

$$\Delta\phi_{\ell 0}^{\max} = 2\Delta\phi_{T0}^{\max} - \Delta\phi_{R0}^{\min} \approx 0.4\Delta\phi_T \quad (10-5)$$

which serves as an empirical rule-of-thumb for the maximum coupling-loop loss of flux linkage that one should assume for design purposes. (If the limiting condition (10-3) is violated, i.e., if $\Delta\phi_{T0} > 0.25\Delta\phi_T$, then it may still be possible to keep $\Delta\phi_\ell$ within the limit specified by Eq. (10-5) if $\Delta\phi_{R0}$ is, or can be made to be, suitably greater than $0.1\Delta\phi_R$, for example, by incorporating greater flux clipping into the receiver. If not, then it may be necessary to use a negative flux source (Core S in Fig. 10-21) for additional clipping, although this is usually not necessary.)

We now show how to derive values for the flux source for each of the two-input logic functions, assuming the worst-case zero condition of Eq. (10-5), namely, $\Delta\phi_{\ell 0} = 0.4\Delta\phi_T$. Let us first consider the AND function xy . Selecting $N_{Tx} = N_{Ty} = 2$, $N_R = 1$, and assuming that $\Delta\phi_R = \Delta\phi_T$, then for the worst case of zero transfer, i.e., when one of the transmitters, say x , contains a one, we find from Eq. (10-2) that

$$0.4\Delta\phi_T = 2\Delta\phi_T + 2(0.25)\Delta\phi_T + N_S\Delta\phi_S - 0.1\Delta\phi_T$$

or

$$N_S\Delta\phi_S = -2.0\Delta\phi_T \quad (10-6)$$

which verifies the nominal value in Table 10-3. Assuming this source value, we find from Eq. (10-2) that the loop dissipation $\Delta\phi_{\ell 1}$ for the case of one transfer, that is, $x = y = 1$, is

$$\Delta\phi_{\ell 1} = 2(\Delta\phi_T + \Delta\phi_T) - 2\Delta\phi_T - \Delta\phi_R$$

or

$$\Delta\phi_{\ell 1} = 2\Delta\phi_T - \Delta\phi_R \quad (10-7)$$

which is also the same as for the single-transmitter case. Hence, satisfaction of the design equation (10-2) results in specification of essentially the same coupling loop as provided by Eq. (6-16) for a single transmitter. An important difference in the present case, however, is that the loop must thread more cores, and hence there is less freedom in choosing wire size. The tendency, of course, is for a longer loop, with increased loop inductance L_ℓ , so that to maintain a comparable $\Delta\phi$ -loss level the loop resistance R_ℓ must correspondingly be reduced, resulting in the need for a larger diameter of wire. A result of reduced loop resistance is a longer priming time even when only a single transmitter contains a one.

Let us now consider the OR function $x + y$. Repeating the similarity-design procedure, we obtain for a double-*zero* transfer the following

$$0.4\Delta\phi_T = 0.5\Delta\phi_T + 0.5\Delta\phi_T + N_S\Delta\phi_S - 0.1\Delta\phi_T$$

or

$$N_S\Delta\phi_S = -0.5\Delta\phi_T \quad (10-8)$$

which again verifies the nominal value in Table 10-3. Substituting into Eq. (10-2) for single-*one* transfer, i.e., the weakest *one*-transfer case, we again obtain the result shown by Eq. (10-7).

What we have done in essence, to achieve a similarity design for OR and AND, is to choose a value of flux source to exactly cancel the second-transmitter flux for the state that contributes the strongest *zero* transmission. Thus, for the AND function, we desire *zero* transfer even if the second transmitter is in the *one* state and we simply set $N_S\Delta\phi_S = -2\Delta\phi_T$. This guarantees the same net flux availability for *one* transfer when the first transmitter is also in the one state. For the OR function, we cancel only the *zero*-level flux from the second transmitter, which again guarantees full *one* transfer levels if the first transmitter (or by symmetry, if either transmitter) is in the *one* state.

This method does not work for exclusive-OR, however, because the need for symmetrical bipolar-loop-current transfer requires that $\Delta\phi_S = 0$. Setting $N_{Tx} = 2$ and $N_{Ty} = -2$, we see that there is no difficulty with *zero* transfer since for both $x = y = 0$ and $x = y = 1$ the transmitter flux linkages exactly cancel. However, for *one* transfer, we have from Eq. (10-2) that $\Delta\phi_{\ell 1}$ is only as large as $2\Delta\phi_T - 2(.25)\Delta\phi_T - \Delta\phi_R = 1.5\Delta\phi_T - \Delta\phi_R$. Thus we see, as pre-viewed above, that there is less flux available for loop losses than is given by Eq. (10-7) for the previous two cases. The practical effect is that a lower impedance loop must be used for this function (the same is true for its inverse $\overline{x \oplus y}$) resulting again in more difficult wiring and longer priming time.

Taking values of N_{Tx} and N_{Ty} from Table 10-3, and using the above process for all of the functions, we obtain all of the flux-source values shown in the table. These were derived on the basis of minimal explicit clipping, and under the assumed limiting conditions of equality in Eqs. (10-4) and (10-5). With a larger amount of clipping, i.e., more *zero* suppression, but at the price of lower-impedance loops, all the values in Table 10-3 except the final two entries for exclusive-OR may be algebraically decreased by as much as 0.5 units (the limit corresponding to full clipping of *zero* flux from the transmitters), and this also includes the case of

simple transfer even though a toroidal clipper was not considered in Sec. 6-6.

Advance Circuit. It is important to consider the effect that a flux source in the loop has on the number of turns of all advance windings. Note that in addition to the turns N_X , N_H , and N_C , we now also have N_{SS} for setting the source core (during $O \rightarrow E$ transfer in this case) and N_{CS} for clearing it (during $E \rightarrow O$ transfer). The charge-balance principle expressed by Eq. (6-22), namely $N_X q_A = N_T q_f$ is still applicable. However, the selection of N_H is a little more involved than for a simple transfer since the amount of holding required now depends on the clearing of source cores and on the polarity of transmitter output windings. For example, in the case of the AND function xy , Eq. (6-24) is replaced by

$$N_R \Delta\phi_{T1} + |N_S \Delta\phi_S| = R_l q_b(t_2) + L_l i_b(t_2) \quad (10-9)$$

and since $|N_S \Delta\phi_S| \approx 2\Delta\phi_T$ for the AND function, then roughly speaking, q_b , and hence N_H also, will be about tripled in comparison to simple transfer. (Such high-drive windings must be placed carefully in order to avoid air fields any larger than necessary.) The values of N_C , N_{SS} , and N_{CS} must similarly be carefully chosen in the light of loop mmf levels to be expected; in particular, the value of N_C is dependent on the logic function performed in the *input* loop.

Multiple Coupling Loops. Thus far we have considered the formation of only a single logic function. When we consider the requirements for fan-out and multiple function formation, the situation becomes more complex. Let us consider the example of a binary scaler, which in effect is a flip-flop with a single input arranged such that the flip-flop changes state with each input pulse. A schematic form of such a scaler is shown in Fig. 10-22(a). The basic flip-flop consists of the upper two elements x and $x \oplus y$ coupled in a loop, where y represents the control input. For $y = 0$, $x \oplus y = x$ and the upper pair of elements will simply circulate the state of x (either *zero* or *one*). But for $y = 1$, $x \oplus y = \bar{x}$ and the state of the flip-flop is unconditionally reversed. (These functions were synthesized from OR and NEGATION functions for the design-example of Sec. 10-5.)

A binary counter consists of a cascade of such stages where the input signal, i.e., the y signal, to each stage derives from a "carry" signal from the previous stage, for example, see the CYCLE COUNTER of Fig. 10-20. If the y signal is considered a carry input, then a carry output (in the arithmetic sense) occurs only if

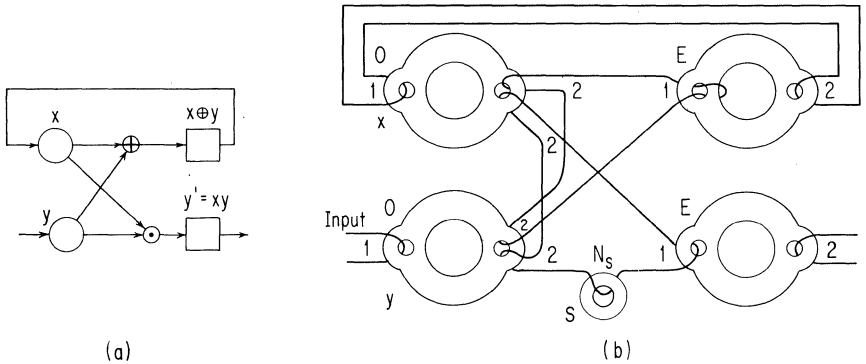


Fig. 10-22. Binary scaler: (a) schematic representation, and (b) MAD-R realization with compound coupling loops.

$x = 1$ when $y = 1$. The carry output y' is then simply the AND function xy .

A MAD-R synthesis of the scaler, using the circuits of Table 10-3, is shown in Fig. 10-22(b), where the same pair of transmitters simultaneously drives two coupling loops wired for the two different functions, exclusive-OR and AND.

An important point to consider in the case of multiple coupling loops is that the priming of one transmitter can cause loop currents that affect the simultaneous priming of the other transmitter. Fortunately, for the particular combination in Fig. 10-22(b), the two loop currents cancel in the other transmitter when only one transmitter is being primed. But many other combinations do not match so well, and if such combinations must be used, then it is especially important to exploit the techniques of Sec. 6-8 to obtain whatever prime-current tolerances are needed. (Recall that there exists a large range over which operating speed can be sacrificed for operating tolerances.)

Using the design method outlined above, a large set of compatible logic circuits can be designed, as evidenced by the set of range maps shown in Fig. 10-23(a) for a particular design example. (By compatible it is meant that the range maps overlap, as shown in the figure.) The symbol $3x$ for one of the curves implies a triple fan-out of x ; xy and $x\bar{y}$ means a double fan-out of x , where x is combined in one circuit with y and in the other circuit with \bar{y} . (These curves were obtained with advance and prime currents of nominally a damped half-sinusoid shape with respective rise and fall times of approximately $2.0 \mu\text{sec}$ and $5.0 \mu\text{sec}$ for Advance, and $125 \mu\text{sec}$ and $200 \mu\text{sec}$ for Prime.)

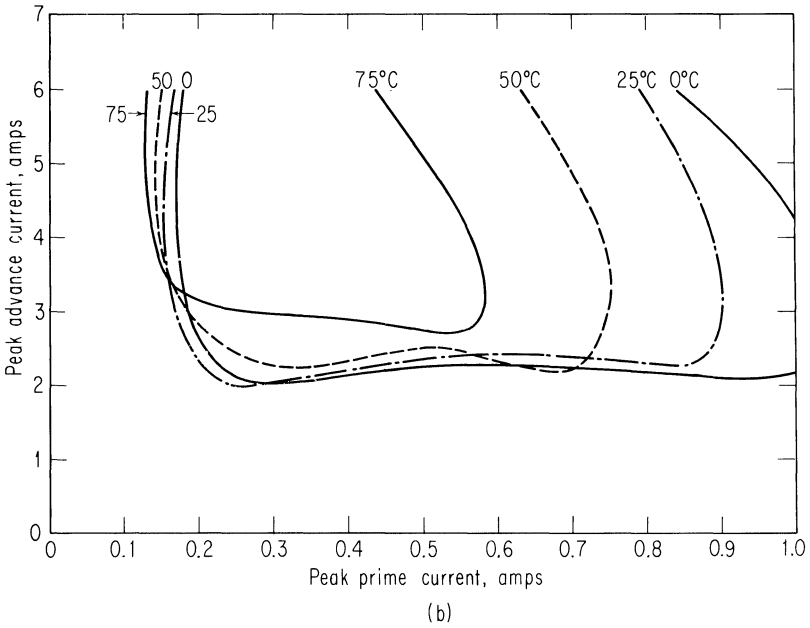
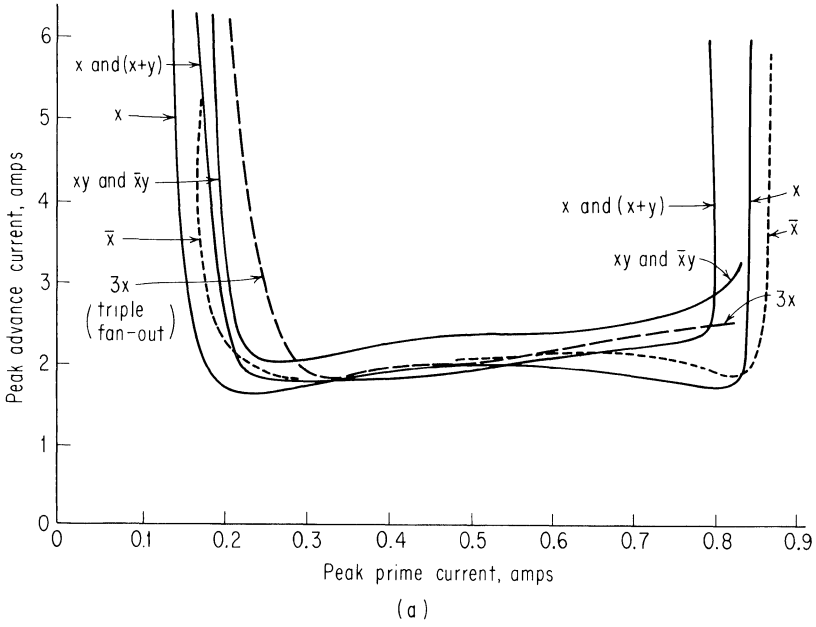


Fig. 10-23. Range maps for various logic functions in (a), and for an entire system of a couple of hundred cores in (b).

Starting from the values obtained by the design method, in essentially every case only minor adjustment of parameters was required to achieve the closely matched set of range maps.

The particular set of functions shown in Fig. 10-23(a) has been used in actual system designs. Condon (1963) has described one experimental system, which was designed for control inside an atomic reactor and which involved the use of about two hundred cores. The overall range map for this particular system is shown in Fig. 10-23(b) for a number of different operating temperatures.

As seen above and in Chap. 6, the design procedure becomes relatively complex in detail. However, it is quite straightforward in practice; furthermore, it need be done only once to obtain a compatible set of designs for any given core type.

10-7 Summary

In Secs. 10-2 and 10-3, we review the general structure of a synchronous digital system and show how, in principle, magnetic-core systems could be synthesized in the same manner as transistor flip-flop systems, by substitution of one-bit shift registers on a one-for-one basis for the flip-flops. With this approach, however, we not only require the usual logic clocks but also sets of clocks to pump up the one-bit registers to standardized signal levels after each transfer (as occurs automatically in a transistor flip-flop). This results in an impractical synthesis technique because of the large number of clock sources required. A more practical arrangement is to have all transfers incorporate signal gain, in which case a single set of clocks plays both the logic-stepping role and flux-pumping role, and a general logic system then needs no more clock pulses than a simple register.

In Sec. 10-4 we review some general aspects of combinational logic and show techniques for synthesizing the basic logic functions with both unipolar and bipolar schemes. We then discuss an actual design example that illustrates a large number of basic circuit and logic principles. This is a decimal arithmetic unit based on an extended version of the nonresistance MAD-N scheme.

Finally, we consider a basic MAD-R circuit configuration that yields all functions of two variables. We show how the circuit-design approach of Chap. 6 can be extended to the design of this circuit for all of the different logic combinations, and we show performance data typical of some actual system designs. These results verify the very wide operating tolerances that can be achieved with such core-wire circuits.

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Part II

MAGNETISM AND FLUX-SWITCHING MODELS

ELEMENTARY PHYSICS OF MAGNETISM

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This chapter summarizes the basic physical properties of magnetic materials that are applicable in digital magnetic circuits. In Sec. 11-1, the sources of magnetization are discussed; Sec. 11-2 deals with the various types of magnetism; in Sec. 11-3, domain theory is reviewed; and in Sec. 11-4, the mechanisms involved in the change of magnetization are introduced.

11-1 Magnetization

Magnetic Flux Density. (Ramo and Whinnery (1956); Panofsky and Phillips (1956).)* Consider two loops, Loop 1 and Loop 2, conducting currents i_1 and i_2 in vacuum, as shown in Fig. 11-1. The force df due to Loop 1 acting on an element of length dl_2 in Loop 2 at Point P is

$$df = i_2 dl_2 \times \mathbf{B} \quad (11-1)$$

where \mathbf{B} is the *magnetic flux density* at Point P . Using mks units,

$$\mathbf{B} = \mu_0 \mathbf{H} \quad (11-2)$$

where $\mu_0 = 4\pi \cdot 10^{-7}$ henry/meter, and, following Ampere's law,

$$\mathbf{H} = \frac{i_1}{4\pi} \oint \frac{dl_1 \times \mathbf{a}_r}{r^2} \quad (11-3)$$

is the *magnetic field* at Point P due to Current i_1 in Loop 1 (\mathbf{a}_r being a unit vector along the line of length r connecting dl_1 and Point P).

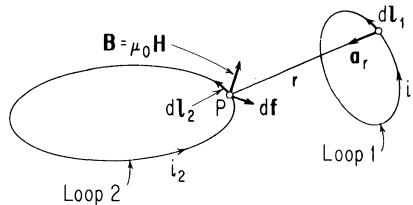


Fig. 11-1. Interaction between true currents.

The magnetic field \mathbf{H} (and hence $\mathbf{B} = \mu_0 \mathbf{H}$) is generated by a *true current* i_1 . If Point P is inside a material, an additional contribution to \mathbf{B} may arise from *atomic currents* consisting of orbiting and spinning electrons. Such a contribution is represented by the *magnetization vector*

$$\mathbf{M} = \frac{1}{\Delta v} \sum_j \mathbf{m}_j \quad (11-4)$$

*References at the head of each subsection in Chap. 11 are given as selective examples where more detailed information on the subjects under discussion may be found.

where Δv is a small volume element surrounding Point P , and m_j is the *magnetic moment* of the j th atom in Δv . The mks units of \mathbf{M} are the same as those of \mathbf{H} , and the total flux density at Point P is

$$\mathbf{B} = \mu_0 (\mathbf{H} + \mathbf{M}) \quad (11-5)$$

Angular Momentum and Magnetic Moment. (Peaslee (1956); Chikazumi (1964).) In Fig. 11-2, a single electron of charge $-e$ and mass m_e orbits with an angular velocity ω along a circle of radius r . Associated with this orbital motion is an *angular momentum*

$$\mathbf{L} = m_e r^2 \boldsymbol{\omega} \quad (11-6)$$

and a *loop magnetic moment*

$$\mathbf{m} = \frac{-er^2}{2} \boldsymbol{\omega} \quad (11-7)$$

The ratio

$$\gamma = -\frac{\mu_0 \mathbf{m}}{\mathbf{L}} = \mu_0 \frac{e}{2m_e} \quad (11-8)$$

is called the *gyromagnetic constant*. For an electron spin (to be discussed later), γ is twice this value. By adding a “ g factor,” Eq. (11-8) is modified to the general form

$$\gamma = -\frac{\mu_0 \mathbf{m}}{\mathbf{L}} = g\mu_0 \frac{e}{2m_e} = 1.105 \cdot 10^5 \text{ g (meter/ampere-second)} \quad (11-8a)$$

where $g = 1$ for orbiting electron and $g = 2$ for electron spin.

If a magnetic field \mathbf{H} is applied along, say, the z axis (making an angle θ with $\boldsymbol{\omega}$), a torque

$$\mathbf{T} = \mu_0 \mathbf{m} \times \mathbf{H} = \frac{d\mathbf{L}}{dt} \quad (11-9)$$

is developed. Since \mathbf{m} is collinear with \mathbf{L} , then following Eq. (11-9) $d\mathbf{L}/dt$ is perpendicular to both \mathbf{L} and \mathbf{H} , and, thus, both \mathbf{L} and \mathbf{m} precess in the same direction around \mathbf{H} , i.e., clockwise looking along

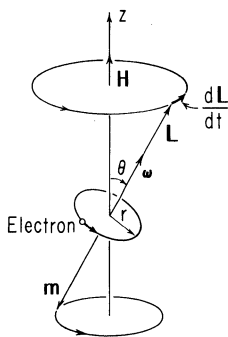


Fig. 11-2. Precession of orbital magnetic moment and angular momentum of an electron around an applied magnetic field.

H , as shown in Fig. 11-2. The frequency of precession, called the *Larmor frequency*, can be shown to be

$$\nu_L = \frac{1}{2\pi} \gamma H = 17.6 \cdot 10^3 gH \quad (11-10)$$

For an orbiting electron ($g = 1$), ν_L is 17.6 kc per (ampere-turn/meter) or 1.4 Mc per oersted (1 oersted = $10^3/(4\pi)$ ampere-turns/meter). For an electron spin, since $g = 2$, ν_L is twice this value.

Quantized Orbital and Spin L and m of an Electron. (Born; Richtmyer *et al.* (1955); Peaslee (1956).) According to classical mechanics, the magnitude and direction of L (and hence also of m) may vary continuously. On the other hand, in quantum mechanics, the magnitude of L is quantized; for an electron of a hydrogenlike atom, it is

$$L_l = \frac{h}{2\pi} \sqrt{l(l+1)} \quad (11-11)$$

where h is Planck's constant ($h = 6.625 \cdot 10^{-34}$ joule-second) and l is the azimuthal quantum number, which varies from 0 to $n - 1$ (n being the principal quantum number). The orientation of L_l (and the corresponding magnetic moment m_l) is determined by quantizing one of its three spatial components, in this case the component along the applied magnetic field H , arbitrarily assumed to be along the z axis, so that

$$L_{l,z} = \frac{h}{2\pi} m \quad (11-12)$$

where m is the magnetic quantum number, which varies in $2l + 1$ unit steps from $-l$ to $+l$. For example, for $l = 2$, $L_l = \sqrt{6} h/(2\pi)$, and five cones of precession of L around H are possible, as shown in Fig. 11-3(a). For electrons of nonhydrogenlike atoms, the quantization of L_l is much more complex than described above.

In addition to L_l (and m_l), the electron possesses an angular momentum (and a magnetic moment) associated with the electron *spin*. In the presence of H , the spin angular momentum L_s is

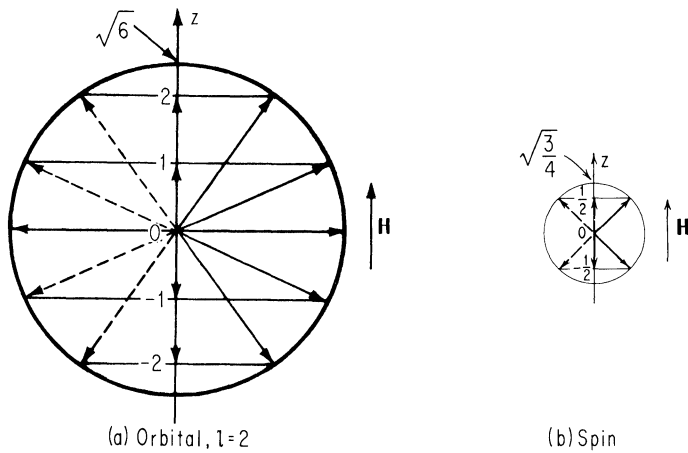


Fig. 11-3. Quantized orbital and spin angular momentum vectors in units of $h/(2\pi)$. Each vector precesses clockwise around the z axis.

quantized according to Eqs. (11-11) and (11-12), except that l is replaced by a single-valued spin quantum number $s = 1/2$. Thus, L_s has a magnitude $L_s = \sqrt{3/4} h/(2\pi)$ and two possible z components, $L_{s,z} = \sigma h/(2\pi)$, where $\sigma = \pm 1/2$, as shown in Fig. 11-3(b). As pointed out in connection with the gyromagnetic ratio—see Eq. (11-8a)— $g \equiv g_l = 1$ for orbital motion, whereas $g \equiv g_s = 2$ for a spin.

Combining Eqs. (11-8a), (11-11), and (11-12), the magnitude of the orbital magnetic moment m_l is

$$m_l = g_l \sqrt{l(l+1)} \mu_B \tag{11-13}$$

and its z component is

$$m_{l,z} = g_l m \mu_B \tag{11-14}$$

where

$$\mu_B = \frac{eh}{4\pi m_e} = 0.927 \cdot 10^{-23} \text{ ampere-turn-(meter)}^2 \tag{11-15}$$

is known as the *Bohr magneton*. Replacing g_l by $g_s = 2$ and m by $\sigma = \pm 1/2$ in Eq. (11-14), the components of spin magnetic moment along the applied H , that is, along the z axis, may have the value $+\mu_B$ or $-\mu_B$.

Atomic Shells. (Born; Richtmyer *et al.* (1955); Peaslee (1956).) Following Pauli's exclusion principle, different electrons are characterized by different quantum numbers n, l, m , and σ . The nucleus of the atom is surrounded by electrons that are classified into *shells* of different quantum numbers n ($n = 1, 2, 3, 4, \dots$). Each shell of quantum number n is divided into n subshells; each subshell is characterized by a quantum number l ($l = 0, 1, \dots, n - 1$) and is designated by the letter s, p, d, f, \dots corresponding to $l = 0, 1, 2, 3, \dots$. Electrons occupying the same subshell, which are called equivalent electrons, have the same n and l quantum numbers, and thus must differ from each other by their m and σ quantum numbers. There are, therefore, $2(2l + 1)$ electrons in a full subshell, and $\sum_{l=0}^{l=n-1} 2(2l + 1) = 2n^2$ electrons in a full shell.

Quantized Orbital and Spin L and m of an Atom. (Born; Peaslee (1956); Kittel (1957); Chikazumi (1964); Morrish (1965).) In a light atom with strong s - s coupling and l - l coupling, the spin and orbital angular momenta (and magnetic moments) of the electrons add vectorially (each precessing around the resulting vector sum) according to *Russell-Saunders* (or L - S) coupling (see Fig. 11-4): The spins add vectorially to form a resultant L_S (and m_S) of quantum number S , and the orbital momenta add vectorially to form a resultant L_Q (and m_Q) of quantum number Q ; these resultants then add vectorially into overall resultants L_J (and m), where J is an integer or a half-integer. (Addition of two L vectors may be viewed as a precession of these vectors about their sum, in this case L_J .) Note that since $g_s = 2g_l$, then from Eq. (11-8a), $m_S/m_Q = 2L_S/L_Q$, and L_J and m are not collinear. However, with m_S antiparallel to L_S and with m_Q antiparallel to L_Q , the sum m is then regarded as precessing around L_J . Consequently, the time average of the component of m

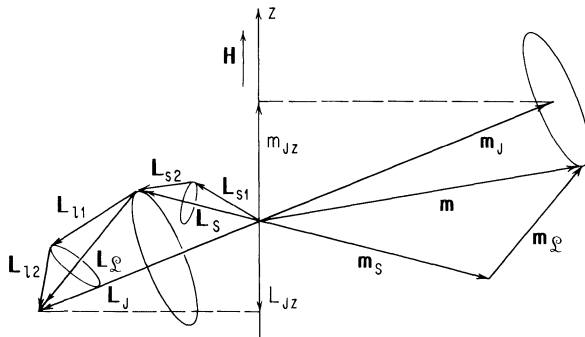


Fig. 11-4. Russell-Saunders (or L - S) coupling of moments in a light atom.

normal to L_J disappears, and the net time average of \mathbf{m} is its component m_J along L_J . The magnitude of m_J is

$$m_J = g\sqrt{J(J+1)}\mu_B \quad (11-16)$$

where, as can be shown from Fig. 11-4, the atomic g factor, called *Lande splitting factor*, is

$$g = \frac{3}{2} + \frac{S(S+1) - \mathcal{L}(\mathcal{L}+1)}{2J(J+1)} \quad (11-17)$$

In a magnetic field, the z components of L_J and m_J , L_{Jz} and m_{Jz} , are quantized; thus, $m_{Jz} = g\mathcal{M}\mu_B$, where $\mathcal{M} = -J, -J+1, \dots, J$ (totally, $2J+1$ possible values).

The values of S , \mathcal{L} , and J of an atom in its ground state are determined by *Hund's rule*: With decreasing m values, the maximum number of spins in a subshell are aligned parallel without violating Pauli's exclusion principle, thus establishing the values of σ and m of every electron in the subshell. Correspondingly, $S = \Sigma\sigma$, $\mathcal{L} = \Sigma m$, and $J = |\mathcal{L} - S|$ if the subshell is less than half full, but if the subshell is more than half full, then $J = \mathcal{L} + S$.

If all the subshells of an atom are filled, then $S = \mathcal{L} = J = 0$, and $m_J = 0$ (i.e., no spontaneous magnetization). We are, therefore, concerned only with atoms with at least one unfilled subshell.

The value of J given by Hund's rule is also valid in a crystal, provided that the electrons in the unfilled subshell(s) of an atom are shielded from the electrostatic field produced by the surrounding atoms. This is the case of a rare-earth ion whose unfilled $4f$ subshell lies deep inside the atom. On the other hand, the unfilled $3d$ subshell of an ion of the iron group (Elements No. 22 through 29) is not shielded, and as a result of the nonuniform electrostatic field generated by the surrounding ions in the crystal, L_{Jz} averages to zero, $\mathcal{L} \approx 0$, and the orbital moment is *quenched*, i.e., it is about zero. For most magnetic materials that contain elements of the iron group, the magnetic moment is thus essentially due to the spins only. (These results are further modified by concepts from band theory, which are not considered here.)

11-2 Types of Magnetism

The magnetic properties of materials are classified into several types: dia-, para-, ferro-, antiferro-, and ferrimagnetism. *Diamagnetism* results from Lenz's law: an applied H induces M

that opposes the applied H . Diamagnetism is induced in every material, but its effect on the net M of nondiamagnetic materials (to be discussed next) is negligible.

Magnetism Due to Permanent Atomic Moments. (Kittel (1957); Smit and Wijn (1959); Chikazumi (1964); Morrish (1965).) The types of magnetism other than diamagnetism result from permanent atomic magnetic moments. In the absence of an applied magnetic field, the net magnetization is affected by two opposing factors: (1) thermal agitation, which tends to reduce M by distributing the atomic magnetic moments randomly in all directions, and (2) a coupling between the atomic moments, which tends to align the moments parallel or antiparallel. If the coupling is weak, then the thermal agitation predominates, and the material is *paramagnetic* (e.g., iron-group ionic salts and the rare earths). If the coupling is strong, then two cases are distinguished: (a) The moments are aligned parallel by a direct exchange interaction between electron spins of neighboring atoms whose orbital wave functions overlap; in this case the material is *ferromagnetic* (e.g., iron, cobalt, nickel, and some of their alloys). (b) The moments are aligned antiparallel by an indirect exchange (superexchange) interaction between the spins of two cations via a neighboring nonmagnetic anion, such as oxygen; in this case the material is respectively *antiferromagnetic* or *ferrimagnetic* depending on whether the antiparallel magnetic moments exactly compensate or not. Many oxides, such as MnO , are antiferromagnetic, whereas ferrites, such as $MnFe_2O_4$, are ferrimagnetic.

The various types of magnetism are shown schematically in Fig. 11-5. Ferromagnetic and ferrimagnetic materials possess a spontaneous moment, i.e., a net nonzero magnetic moment even without the application of an external magnetic field. The volume density of this spontaneous magnetic moment is called *saturation magnetization*, and is denoted by M_s . The value of M_s for ferrites is usually smaller than the M_s value for ferromagnetic metals, primarily because it results from the difference between aligned spins. On the other hand, for diamagnetic, paramagnetic, and antiferromagnetic materials, $M_s = 0$, and in order to obtain a nonzero magnetization, an external H field must be applied. These are related according to

$$M = \chi H \quad (11-18)$$

where χ is the *susceptibility*. The diamagnetic χ is negative and its

magnitude is of the order of 10^{-6} . The paramagnetic χ is positive and its magnitude varies from about 10^{-6} to about 10^{-3} .

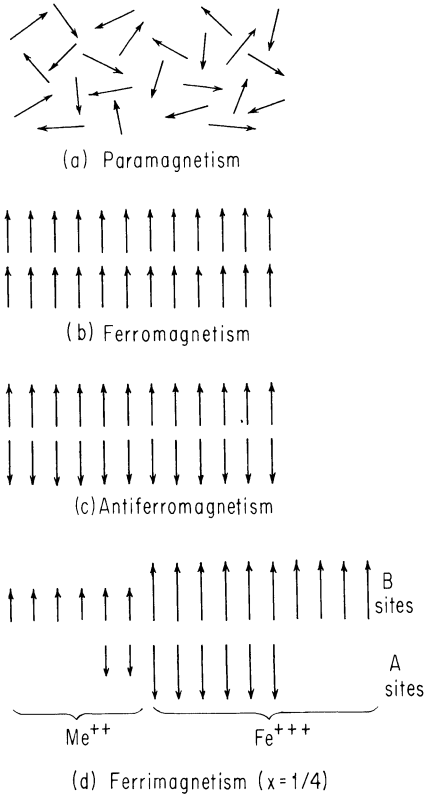


Fig. 11-5. Schematic spin-order arrangements in different types of magnetism.

Effects of Temperature. (Kittel (1957); Smit and Wijn (1959).) Due to thermal agitation, both M_s and χ are affected by temperature T . Schematic plots of M_s and $1/\chi$ vs. T are shown in Fig. 11-6. For ferromagnetic and most ferrimagnetic materials, M_s decreases with T , reaching zero at the *Curie temperature* T_c , at which point the thermal energy is equal to the exchange energy. For $T > T_c$, the thermal agitation predominates and the material becomes paramagnetic.

Ferrites are discussed next because of their application in digital magnetic circuits.

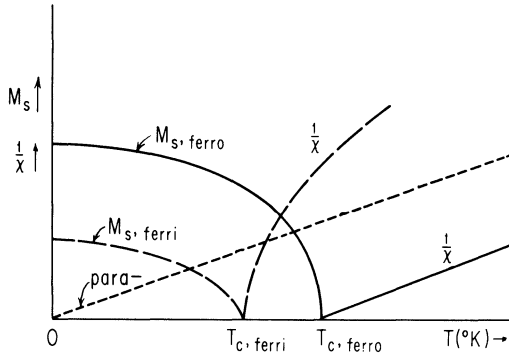
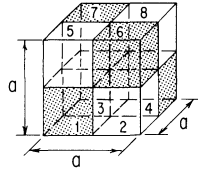
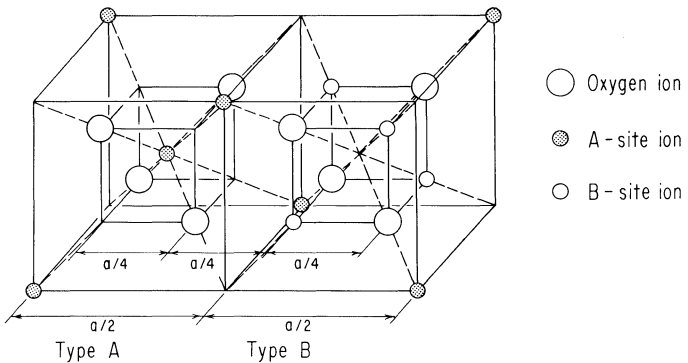


Fig. 11-6. M_s and $1/\chi$ vs. temperature.

Ferrites. (Gorter (1954); Smit and Wijn (1959); Chikazumi (1964); Morrish (1965); Yafet and Kittel (1952).) The unit cell of a simple ferrite consists of eight $Me^{++}Fe_2^{+++}O_4$ molecules in a *spinel* structure. Here, Me^{++} stands for a divalent cation, such as Mn^{++} , Fe^{++} , Co^{++} , Ni^{++} , Cu^{++} , Mg^{++} , Zn^{++} , Cd^{++} , or the mixture $Li_{0.5}^+Fe_{0.5}^{+++}$. The octants of a spinel unit cell are shown in Fig. 11-7.



(a) Division of a unit cell into 8 octants.
 Octants 1, 4, 6, and 7 - Type A
 Octants 2, 3, 5, and 8 - Type B

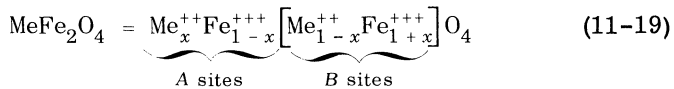


(b) Two neighboring octants

Fig. 11-7. Octants of a Spinel Unit Cell. (Oxygen ions are larger in proportion than is shown.)

The length of a unit-cell edge is denoted by a (typically, $a \approx 8.3 \text{ \AA}$). The interstices occupied by the cations are classified into A sites and B sites: An A site is surrounded by four oxygen ions forming a *tetrahedron*; a B site is surrounded by six oxygen ions forming an *octahedron*. (To visualize the latter, examine the nearest oxygen ions in the corresponding octant and in three neighboring octants.) There are eight A sites and sixteen B sites per unit cell.

The site occupation per molecule is expressed as



where $0 \leq x \leq 1$. If $x = 1$, the spinel is "normal" (the A sites are occupied by $\text{Me}^{\text{++}}$ ions); if $x = 0$, the spinel is "inverse" (the A sites are occupied by $\text{Fe}^{\text{+++}}$ ions).

There are three types of negative superexchange (indirect exchange) interaction among the cation spins, which tend to align them antiparallel: A - A between the spins of the A -type cations; B - B between the spins of the B -type cations; and A - B between the spins of the A -type and the B -type cations. The oxygen ion plays an important role in each of these indirect exchange interactions; as a result, the interaction is strong if (a) the Me-O distances between an oxygen ion and the neighboring cations are short and (b) the angle Me-O-Me is large (maximum 180°). On the basis of these criteria, it can be shown that the A - B interaction is the strongest, the B - B interaction is intermediate, and the A - A interaction is the weakest. It is impossible for neighboring spins of one type to be antiparallel both to each other and to a neighboring spin of the other type. Therefore, since the (negative) A - B interaction is the strongest, the A -type spins are aligned antiparallel to the B -type spins. As a result, spins of the A -type cations are forced to be aligned parallel to each other, thus forming the A sublattice of moment m_A . If the B - B interaction is not strong enough, then the spins of the B -type cations are also forced to be aligned parallel to each other, thus forming the B sublattice. However, if the A - B and B - B interactions are comparable in magnitude, then the parallel alignment of the B sublattice is perturbed, and the B sublattice is split into two sublattices B' and B'' whose moments are canted (though equal in magnitude). In any case, the net moment m_B is antiparallel to m_A and, since $m_B \neq m_A$, there is a nonzero net spontaneous magnetic moment whose magnitude is $|m_B - m_A|$.

Effects of Applied H. (Kittel (1957); Smit and Wijn (1959); Chikazumi (1964); Morrish (1965).) The relation $M = \chi H$ (Eq. (11-18)) for dia-, para-, and antiferromagnetism is characteristic of a linear magnetic material. In contrast, a ferromagnetic or ferrimagnetic material is nonlinear, and is characterized by an $M(H)$ hysteresis loop, as shown in Fig. 11-8(b). This loop results from the existence of small regions, called *domains*, which are discussed in the following section. Each domain is saturated along a certain preferred direction, which is different from its neighbor's. (The value of M_s of each domain decreases with increasing temperature, as shown in Fig. 11-6.) Changing of M by a low applied H is usually achieved by domain-boundary displacements. However, application of a high H is required to saturate the entire specimen by rotating all the domain-magnetization vectors into alignment with H . As the applied H is then dropped to zero, these vectors rotate back into alignment with their nearest preferred directions, which are randomly distributed within an angle whose magnitude depends on the material. The resulting M is the maximum *remanent magnetization*, M_r .

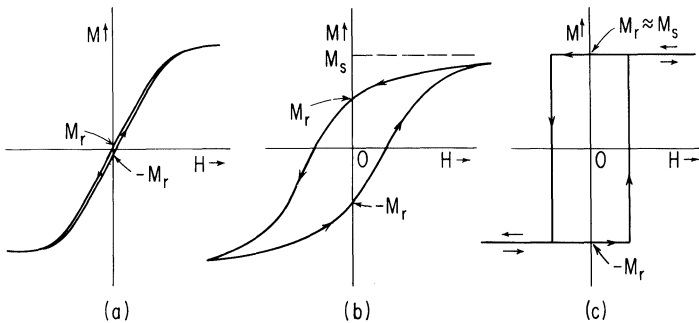


Fig. 11-8. $M(H)$ Loops of ferromagnetic and ferrimagnetic materials.

Extending the $M(H)$ loop in Fig. 11-8(b), two extreme cases are distinguished. In Fig. 11-8(a), $M_r \approx 0$ and, in a limited region of H , the material is essentially a high- χ linear material. In Fig. 11-8(c), $M_r \approx M_s$, and the $M(H)$ loop is "square."

11-3 Domain Theory

Introduction. (Kittel and Galt (1956).) A weak magnetic field, e.g., a fraction of an oersted, can change the magnetization of

certain ferromagnetic and ferrimagnetic materials to any value between the positive and negative remanent states M_r and $-M_r$ (see Fig. 11-8). This change is not caused by overcoming the exchange interaction between neighboring spins; the magnetic field required to overcome spin alignment is extremely high (about 10^7 oersteds for iron; a dc field of such magnitude has yet to be produced in the laboratory). This change in magnetization is explained by domain theory.

Magnetic Domains. (Kittel and Galt (1956); Chikazumi (1964); Morrish (1965); Carey and Isaac (1966).) As mentioned above, an unsaturated ferromagnetic or ferrimagnetic specimen is divided into small regions, called magnetic domains. Each domain is held essentially in saturation by exchange forces.

The boundary between two neighboring domains is called a *domain wall*. The magnetization M of the specimen is the vector sum of the magnetization vectors of the individual domains. An example of a demagnetized state ($M = 0$) of a single crystal is shown in Fig. 11-9(a). Upon application of an external field H (at a constant temperature), M may change in two ways: (1) by *wall displacement* that increases the volume of those domains whose magnetization vectors point closest to H and decreases the volume of those domains whose magnetization vectors point farthest from H , Fig. 11-9(b), and (2) by *rotation of magnetization* toward alignment with H , Fig. 11-9(c). For the same amount of change in the component of M along the applied H , rotation of magnetization usually requires a higher H than wall motion.

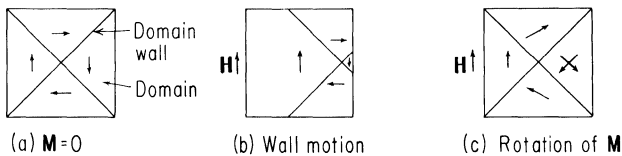


Fig. 11-9. Magnetic domains and changes of M by wall motion and rotation of magnetization.

Domain structure follows a rule which is simple in principle: domains are formed in such a way that the total energy involved in the resulting structure is minimum. This energy has four components—exchange, magnetostatic, anisotropy, and magnetoelastic—which are described briefly below.

Exchange Energy. (Kittel and Galt (1956); Chikazumi (1964); Morrish (1965).) Exchange energy stems from the electrostatic interaction between adjacent orbiting electrons, which tends to align their spins parallel or antiparallel. Exchange energy per unit volume is

$$e_{\text{ex}} = -2J_e S^2 \sum_{i>j} \cos \varphi_{ij} \quad (11-20)$$

where J_e is the exchange integral, S is the spin angular momentum (in units of $h/(2\pi)$), and φ_{ij} is the angle between two neighboring spins. If φ_{ij} is small, then Eq. (11-20) reduces to

$$e_{\text{ex}} = J_e S^2 \sum_{i>j} \varphi_{ij}^2 + \text{constant} \quad (11-21)$$

For ferromagnetism, $J_e > 0$ and e_{ex} is minimal if $\varphi_{ij} = 0$ (spins are parallel); for antiferromagnetism and ferrimagnetism, $J_e < 0$ and e_{ex} is minimal if $\varphi_{ij} = \pi$ (spins are antiparallel). Misalignment of neighboring spins is energetically unfavorable because it involves an increase in e_{ex} .

Magnetostatic Energy. (Kittel and Galt (1956); Chikazumi (1964); Morrish (1965).) Magnetostatic energy stems from the interaction between a magnetic moment m and the magnetic field H which tends to align m and H parallel. Per unit volume, if M and H are independent, the magnetostatic energy is

$$e_{\text{mag}} = -\mu_0 \mathbf{H} \cdot \mathbf{M} \quad (11-22)$$

If M varies in space (as at the poles of a permanent magnet), then, satisfying Maxwell's equation $\nabla \cdot \mathbf{B} = 0$, a *demagnetizing* field H_{dm} is generated in opposition to M in order to maintain B continuous. Since $\mathbf{B} = \mu_0 (\mathbf{M} + \mathbf{H})$ and $\nabla \cdot \mathbf{B} = 0$, then $\nabla \cdot \mathbf{H} = -\nabla \cdot \mathbf{M} \equiv \rho_m$, where ρ_m is defined as volume density of *magnetic poles*. According to this model, these poles may be assumed to be the source of the demagnetizing field. Since H_{dm} is generated by M itself, the corresponding e_{mag} is *self energy* and a factor of 1/2 must be included, that is,

$$e_{\text{mag, self}} = -\frac{1}{2} \mu_0 \mathbf{H}_{dm} \cdot \mathbf{M} \quad (11-23)$$

Note that since H_{dm} and M tend to be directed oppositely, that is, $H_{dm} \cdot M < 0$, $e_{mag, self}$ is always positive. In other words, creation of magnetic poles is energetically unfavorable because it involves an increase in energy.

Anisotropy Energy. (Kittel and Galt (1956); Chikazumi (1964); Morrish (1965).) Anisotropy energy results from the preference of the magnetic moment of each atom to be aligned along certain directions of the crystal lattice, which are called directions of *easy* magnetization. For a cubic crystal, such as the body-centered cubic crystal shown in Fig. 11-10, the expression for the anisotropy energy per unit volume, based on the crystal symmetry, is

$$e_{an} = K_1 (\alpha_1^2 \alpha_2^2 + \alpha_2^2 \alpha_3^2 + \alpha_3^2 \alpha_1^2) + K_2 \alpha_1^2 \alpha_2^2 \alpha_3^2 + \dots \quad (11-24)$$

where α_1, α_2 , and α_3 are the direction cosines of M , and K_1 and K_2 are the anisotropy constants. The sum $\alpha_1^2 \alpha_2^2 + \alpha_2^2 \alpha_3^2 + \alpha_3^2 \alpha_1^2$ varies between a minimum value of zero (when M is aligned with a cubic edge) and a maximum value of $1/3$ (when M is aligned with a cube diagonal). Since a deviation of M from an easy axis results in an increase in e_{an} , then $K_1 > 0$ if the cubic edge is an easy direction, but if the cube diagonal is an easy direction, then $K_1 < 0$. Thus, for example, $K_1 > 0$ for iron, but for nickel and ferrites, $K_1 < 0$ (for cobalt ferrites, however, $K_1 > 0$).

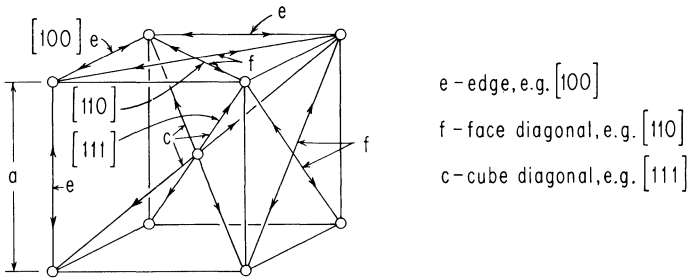


Fig. 11-10. Body-centered cubic crystal.

In the case of a uniaxial crystalline anisotropy (e.g., in cobalt, whose crystal is hexagonal, and in permalloy thin films), due to the symmetry,

$$e_{an} = K_1 \sin^2 \theta + K_2 \sin^4 \theta + \dots \quad (11-25)$$

where θ is the angle between M and the easy direction.

Magnetoelastic Energy. (Kittel and Galt (1956); Chikazumi (1964); Morrish (1965).) Magnetoelastic (or magnetostriction) energy is the change in the crystal anisotropy energy caused by interaction between the magnetization and a mechanical stress. If a uniaxial mechanical tension T_m is applied, the volume density of this energy is given by the expression

$$e_{me} = \frac{3}{2} \lambda T_m \sin^2 \theta \quad (11-26)$$

where λ is the coefficient of isotropic magnetostriction and θ is the angle between T_m and the saturation-magnetization vector. Conversely, if application of \mathbf{H} field causes \mathbf{M} of a specimen to change by rotation of magnetization, then the specimen will deform spontaneously along \mathbf{M} , becoming longer if $\lambda > 0$ and shorter if $\lambda < 0$. (However, a change in \mathbf{M} due to 180° -wall displacement will cause no such deformation.) For iron, $\lambda > 0$; for nickel, $\lambda < 0$; for Permalloy (81 percent nickel and 19 percent iron), $\lambda \simeq 0$.

Types of Anisotropy and Anisotropy Field. (Smit and Wijn (1959); Chikazumi (1964).) The term anisotropy is used to designate the preference of the magnetization vector of a domain to be aligned along certain directions in order to minimize a given type of energy. We have already encountered the *crystalline* anisotropy. Another type of anisotropy is *strain* anisotropy, which is associated with the magnetoelastic energy.

A third type of anisotropy is the *shape* anisotropy. It amounts to the preference of \mathbf{M} to align along the direction of minimum demagnetizing field H_{dm} in order to minimize the self magnetostatic energy (Eq. (11-23)). The value of H_{dm} depends on the shape of the specimen. For example, a prolate (needle-like) ellipsoid is characterized by a uniaxial shape anisotropy along the long axis where the demagnetizing field is minimal. Note that even powers of the $\sin \theta$ function describe uniaxial anisotropy of any kind: crystalline (Eq. (11-25)), strain (Eq. (11-26)), and shape anisotropy.

Anisotropy energy e_{an} is required to turn the domain-magnetization vector \mathbf{M} (of magnitude M_s) away from its preferred direction by some angle θ . The stiffness that tends to turn \mathbf{M} back toward the preferred direction may be viewed as giving rise to an *anisotropy field* \mathbf{H}_k directed along the preferred direction and acting on \mathbf{M} . Thus e_{an} is equivalent to $-\mu_0 \mathbf{H}_k \cdot \mathbf{M}$ (Eq. (11-22)), or $e_{an} = -\mu_0 H_k M_s \cos \theta$; hence, for a small θ , that is, $\cos \theta \approx 1$, we obtain

$$H_k = \frac{1}{\mu_0 M_s} \left(\frac{\partial^2 e_{an}}{\partial \theta^2} \right) \tag{11-27}$$

It can be shown from Eqs. (11-24) and (11-25) that for both cube-edge anisotropy and uniaxial anisotropy, $e_{an} \approx K_1 \theta^2$ if θ is small, and hence

$$H_k = \frac{2K_1}{\mu_0 M_s} \tag{11-27a}$$

For a preferred direction along a cube diagonal (such as for nickel or ferrites), it can be shown that $e_{an} \approx (K_1/3) - (2K_1/3)\theta^2$ if θ is small, and hence

$$H_k = -\frac{4K_1}{3\mu_0 M_s} \tag{11-27b}$$

Domain Walls. (Kittel and Galt (1956); Chikazumi (1964); Morrish (1965); Carey and Isaac (1966).) A domain wall is the transition layer in which the spin direction changes gradually between two neighboring domains. In bulk materials and films that are not too thin (for example, 80-20 Ni-Fe film of thickness larger than about 1000 Å), the spins rotate in the plane of the wall in such a way that no volume poles are created in the wall. This type of wall is called a *Bloch wall*. A 180° Bloch wall is shown in Fig. 11-11. The width of a 180° wall is of the order of 200 atomic layers, i.e., lattice spacings.

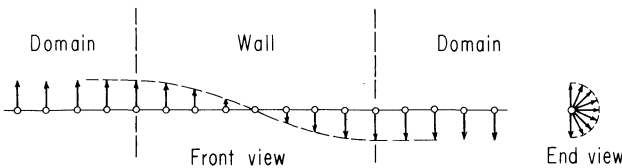


Fig. 11-11. A 180° Bloch wall.

The energy E_w involved in formation of a domain wall is proportional to the wall area A_w , that is, $E_w = \sigma_w A_w$, where σ_w is the energy per unit area of wall. The components of Bloch-wall energy are: (1) exchange energy, because neighboring spins across the

wall are tilted relative to each other; (2) anisotropy energy, because the spins in the wall volume are not directed along the easy axes; and (3) magnetostatic energy, due to magnetic poles at the surface of the specimen. The last component is generally negligible in bulk materials, but not in thin films. In fact, in very thin films, e.g., of less than $\sim 300 \text{ \AA}$ thickness for 80%–20% Ni-Fe film, the surface poles force the spins to rotate essentially in the plane of the film, thus creating positive and negative poles within the film. This type of wall is called a *Néel wall*.

Domain Formation. (Kittel and Galt (1956); Chikazumi (1964); Morrish (1965); Carey and Isaac (1966).) Domain formation, which is based on the principle of minimization of the total energy E of a specimen of volume V , is illustrated in Fig. 11-12 by *hypothetically* adding the various energy components one at a time. Assuming that $J_e > 0$, all spins must be parallel in (a) in order to minimize e_{ex} (Eq. (11-20)). In (b), e_{mag} due to the demagnetizing field (Eq. (11-23)) is added, and the spins line head-to-toe in order to reduce the magnetic poles. In (c), cube-edge crystalline anisotropy is added, thus forcing the magnetic moments to line along the easy directions. This results in the formation of four domains that are separated by one 180° wall and four 90° walls. The top and bottom domains are called *domains of closure*. In (d), a uniaxial strain anisotropy is induced by a mechanical stress, and more domains are formed in order to decrease the volume of the domains of closure where M is not aligned along a preferred direction. The mechanical stress may be applied externally or may be developed internally due to the tendency of each closure domain to deform along the direction of its magnetization. The same domain formation

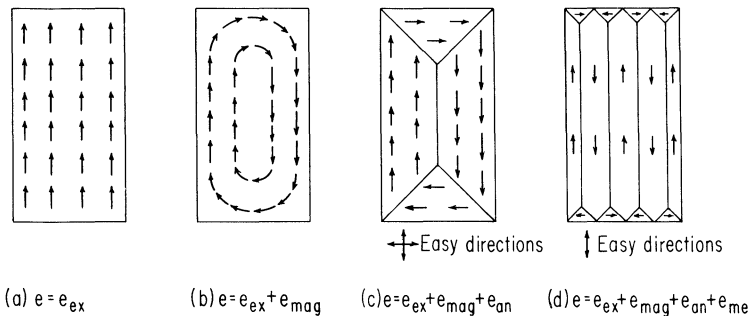


Fig. 11-12. Domain formation to minimize the total energy.

in (d) may also result in the absence of a mechanical stress if the material is characterized by a uniaxial crystalline anisotropy, e.g., cobalt. It would seem that the subdivision into domains in (d) should continue indefinitely in order to decrease the total volume V of the closure domains to zero. However, this subdivision increases the total area A_w of the 180° domain walls. A balance is reached when the total energy $E = Ve + A_w\sigma_w$ is minimum, where e is the total volume energy density of the closure domain.

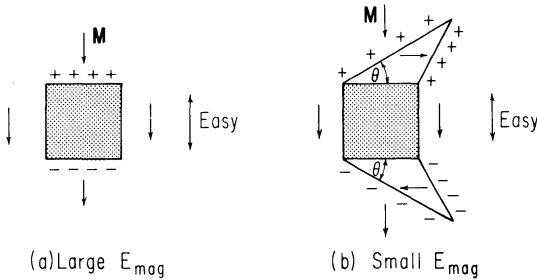


Fig. 11-13. Nonmagnetic inclusion in a domain.

Imagine now a cubic imperfection, as shown in Fig. 11-13. Néel calculated the magnetostatic energy in (a) and found it to be much larger than the total energy associated with the domains of closure in (b). He thus predicted the formation of spiky domains of closure, such as those shown in (b), around nonmagnetic inclusions. Such “Néel spikes” were observed experimentally later. In the upper domain of closure in Fig. 11-13(b), the angle between each wall and the incoming M is larger than the angle between the wall and the outgoing M ; as a result, positive poles are generated. The converse is true for the lower domain of closure. The resulting angle θ is such that the total energy is minimum.

Observation of Domain Patterns. (Kittel and Galt (1956); Chikazumi (1964); Carey and Isaac (1966).) The most direct proof for the existence of magnetic domains is the experimental observation of such domains. There are several techniques for such an observation. The most common one is the *magnetic powder* technique, known also as the Bitter technique. A drop of colloidal suspension of Fe_3O_4 powder of small particle size (about 100 to 1000 Å) is placed on a carefully polished surface and flattened by a microscope cover glass. The particles move randomly (Brownian motion) in the suspension until they are trapped by the inhomogeneous

magnetic field near the wall. The particle size is smaller than the wavelength of visible light. However, a magnetic dipole-dipole interaction between these particles forms visible particle chains along H above the domain wall. Because of strains and nonpreferred directions at the surface of a specimen, the observed domain patterns are usually more complex than they actually are inside the specimen. Simple domain patterns are observed only after special specimen preparation.

11-4 Mechanisms of Magnetization Switching

Changing the Magnetization. (Stoner and Rhodes (1949); Chikazumi (1964).) So far, we have discussed the static states of magnetization and domain patterns. We now turn to the mechanisms by which the magnetization is changed. Such a process is commonly referred to as *magnetization switching*.

Consider a specimen of volume V which contains n domains. Its net magnetization vector with reference to a specified direction is

$$\mathbf{M} = \frac{1}{V} \sum_{j=1}^n v_j \mathbf{M}_j \quad (11-28)$$

where v_j and \mathbf{M}_j are the volume and the magnetization vector of the j th domain. The magnitude of \mathbf{M} is

$$M = \frac{1}{V} \sum_{j=1}^n v_j M_j \cos \varphi_j \quad (11-28a)$$

where φ_j is the angle between \mathbf{M}_j and \mathbf{M} . Differentiating Eq. (11-28a) with respect to time, we obtain

$$\frac{dM}{dt} \equiv \dot{M} = \frac{1}{V} \sum_{j=1}^n \left(v_j \cos \varphi_j \frac{dM_j}{dt} + M_j \cos \varphi_j \frac{dv_j}{dt} - v_j M_j \sin \varphi_j \frac{d\varphi_j}{dt} \right) \quad (11-29)$$

The three terms in Eq. (11-29) correspond to the three mechanisms that may be responsible for a change in M :

1. A change in the magnitude of M_j of a domain (due to temperature effect on M_s , for example)

2. A change in domain volume (i.e., by domain-wall motion)
3. Rotation of magnetization of a domain

Assuming that the environmental conditions (temperature, etc.) are fixed, $\dot{\mathbf{M}}$ may be generated by either domain-wall motion or rotation of magnetization, or both. However, since wall motion involves rotation of spins within the wall, a domain-wall motion may be viewed as a sequential rotation of magnetization. Rotation of \mathbf{M} is, therefore, common to both mechanisms, and will be treated first.

Rotation of Magnetization. (Chikazumi (1964); Morrish (1965).) Combining Eqs. (11-8) and (11-9) and dividing by the volume, we obtain

$$\dot{\mathbf{M}} = -\gamma\mathbf{M} \times \mathbf{H} \quad (11-30)$$

where \mathbf{H} is the total field. Since this relation describes an endless precession of \mathbf{M} around \mathbf{H} , that is, with a constant θ in Fig. 11-2, a rotation of \mathbf{M} into alignment with \mathbf{H} would be impossible unless another term that causes θ to change with time is added to $-\gamma\mathbf{M} \times \mathbf{H}$. Such a term stems from the dissipation of energy due to viscous damping associated with the change in \mathbf{M} . Two phenomenological forms have been proposed for this term: $-(\lambda/M_s^2)(\mathbf{M} \times \dot{\mathbf{M}} \times \mathbf{H})$ by Landau-Lifshitz, and $(\alpha/M_s)(\mathbf{M} \times \dot{\mathbf{M}})$ by Gilbert, where $M_s = (\mathbf{M} \cdot \mathbf{M})^{1/2}$ is the saturation magnetization, and where λ and α are viscous-damping constants. It can be shown that the two dissipative terms are equivalent if

$$\lambda = \alpha\gamma M_s \quad (11-31)$$

and $\alpha^2 \ll 1$. The resulting differential equations are the Landau-Lifshitz equation

$$\dot{\mathbf{M}} = -\gamma\mathbf{M} \times \mathbf{H} - \frac{\lambda}{M_s^2} (\mathbf{M} \times \dot{\mathbf{M}} \times \mathbf{H}) \quad (11-32)$$

and the Gilbert equation

$$\dot{\mathbf{M}} = -\gamma\mathbf{M} \times \mathbf{H} + \frac{\alpha}{M_s} (\mathbf{M} \times \dot{\mathbf{M}}) \quad (11-33)$$

By using spherical coordinates M_s , θ , and φ , it can be shown that either equation becomes a set of two differential equations

$$\dot{\theta} = -\frac{1}{\tau} \sin \theta \quad (11-34)$$

and

$$\dot{\phi} = \Omega \quad (11-35)$$

where

$$\tau = \begin{cases} \frac{M_s}{\lambda H} & \text{(Landau-Lifshitz)} \\ \frac{1 + \alpha^2}{\alpha \gamma H} & \text{(Gilbert)} \end{cases} \quad (11-36)$$

and

$$\Omega = \begin{cases} \gamma H & \text{(Landau-Lifshitz)} \\ \frac{\gamma H}{1 + \alpha^2} & \text{(Gilbert)} \end{cases} \quad (11-37)$$

If \mathbf{H} is constant in time, then the solution of Eqs. (11-34) and (11-35) yields

$$\tan \frac{\theta}{2} = \left(\tan \frac{\theta_0}{2} \right) e^{-t/\tau} \quad (11-38)$$

and

$$\varphi = \varphi_0 + \Omega t \quad (11-39)$$

where θ_0 and φ_0 are the initial values of θ and φ , respectively.

Initially, \mathbf{M} is aligned along the internal field $\mathbf{H}_i = \mathbf{H}_k + \mathbf{H}_{dm}$, where \mathbf{H}_k is the total anisotropy field and \mathbf{H}_{dm} is the demagnetizing field. Upon application of an external field \mathbf{H}_{ap} , \mathbf{M} spirals into alignment with the total field $\mathbf{H} = \mathbf{H}_i + \mathbf{H}_{ap}$, as shown in Fig. 11-14. The internal field \mathbf{H}_i may vary during the transient time, in which case Eqs. (11-38) and (11-39) are invalid and the solution of $\mathbf{M}(t)$ is very complex.

A distinction is made between elastic and inelastic rotation of magnetization. The rotation is elastic if θ_0 is smaller than the angle between \mathbf{H} and any preferred direction other than the original one

because, upon removal of H_{ap} , H_i returns M back to its original orientation. (In ferrites, whose easy axes are along the cube diagonals, the maximum value that θ_0 may have while satisfying this condition is 54.73° .) On the other hand, if M falls into a new preferred direction, then the rotation of magnetization is inelastic, as is the case in Fig. 11-14.

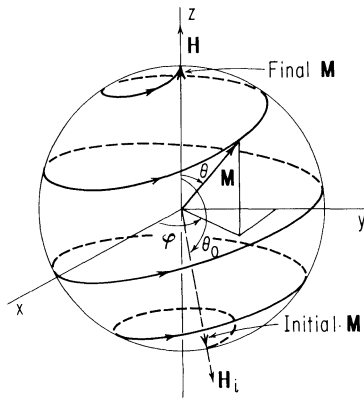


Fig. 11-14. Spiraling during rotation of magnetization.

The Landau-Lifshitz and Gilbert equations are equivalent if $\alpha^2 \ll 1$ (cf. Eqs. (11-36) and (11-37)). In the limit, as $\alpha \rightarrow 0$ (that is, no damping), both equations predict that $\tau \rightarrow \infty$ (that is, infinite switching time) because of endless precession of M . On the other hand, for $\alpha \rightarrow \infty$ (that is, infinite damping), $\tau \rightarrow 0$ according to the Landau-Lifshitz equation, whereas $\tau \rightarrow \infty$ according to the Gilbert equation. Since M cannot actually move if $\alpha \rightarrow \infty$, the Landau-Lifshitz equation is invalid for this condition. From the Gilbert expression for τ in Eq. (11-36), τ is found to be minimum for $\alpha = 1$; hence, $\tau_{\min} = 2/(\gamma H)$.

Domain-Wall Displacements. (Stoner and Rhodes (1949); Tebble (1955); Chikazumi (1964); Knowles (1960).) Consider a 180° Bloch wall of area A_w in a ferromagnetic or ferrimagnetic crystallite. Assume that the wall lies in the x - y plane and separates two domains whose saturation-magnetization vectors are along the $+x$ and $-x$ directions. Suppose that, under the influence of applied field H_{ap} , the wall moves slowly along the z direction toward a nonmagnetic inclusion. Assuming that the wall remains rigidly planar, its interaction with the inclusion is illustrated in Fig. 11-15. In (a),

there is no interaction as yet. In (b), the wall touches the spiky domains of closure, and there is a sudden change to the (c) configuration because in (c) the walls bisect the angles between the magnetization vectors and, as a result, the magnetic poles in (b) are eliminated and the energy is reduced. The energy is further reduced by decreasing the wall area and volume of the closure domains, (d), until the state of minimum energy in (e) is reached. As the wall departs from (e), the energy increases as domains of closure stretch out, (f), with essentially no poles. However, as the length of the closure domain increases from (g) to (h), it is energetically more favorable for the closure domains to narrow down in order to reduce their volume and their wall area, despite the development of poles. As the closure domains become narrow spikes, (h), the wall breaks free and the spiky domains snap back to an optimal shape, (i).

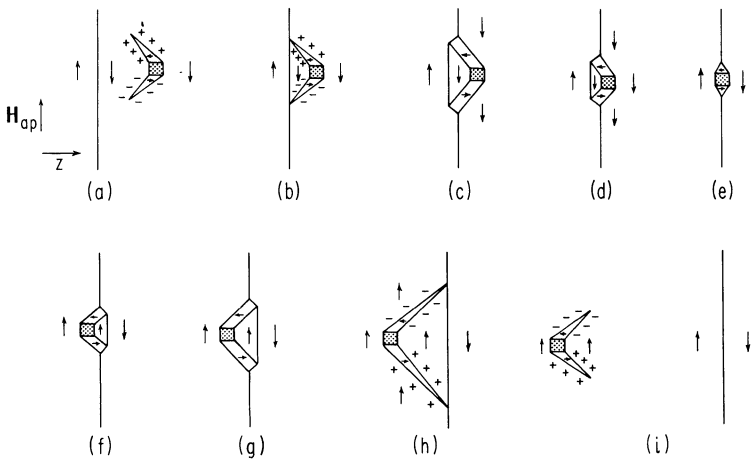


Fig. 11-15. Interaction between a 180° wall and a nonmagnetic inclusion.

The example in Fig. 11-15 illustrates how the total energy E may vary with the wall position z as a result of inhomogeneities in the material. In the absence of an applied field H_{ap} , the wall settles where E is minimum, i.e., where $dE/dz = 0$ and $d^2E/dz^2 > 0$. With H_{ap} applied along the $\pm x$ axis, a force $2\mu_0 M_s H_{ap} A_w$ moves the wall along the $\pm z$ axis in a direction to expand the domain whose magnetization vector points along H_{ap} . This motion is opposed by a restoring (or stiffness) force dE/dz .

It is convenient to examine the net effect on the wall motion by comparing the applied H with $c(dE/dz)$ as a function of z , where $c = 1/(2\mu_0 M_s A_w)$. Schematic plots of $c(dE/dz)$ vs. z are shown in Fig. 11-16 for two typical walls (in the same crystallite) whose positions at Points R and R' , respectively, correspond to the remanent state $M = -M_r$ of the crystallite. By definition, as H_{ap} is applied, a wall is displaced *elastically* if, upon removal of H_{ap} , the restoring field $c(dE/dz)$ returns the wall to its original position; but if a new position is reached, the wall displacement is *inelastic*.

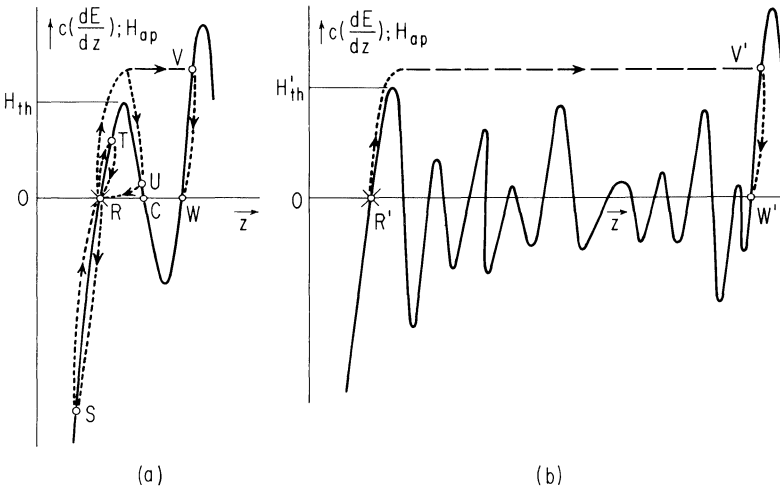


Fig. 11-16. Schematic plots of energy gradient vs. wall position and elastic (dotted line) and inelastic (dashed line) displacements of two domain walls. (a) Elastic and minor inelastic wall displacements. (b) Elastic and major inelastic wall displacements.

Suppose that the wall of Fig. 11-16(a) is initially situated at Point R . The threshold field imposed by the first energy hill is marked by H_{th} . Three types of elastic wall displacement are distinguished:

1. Displacement due to a negative H_{ap} pulse; for example, Displacement $R-S$
2. Displacement due to a positive H_{ap} pulse, provided that $H_{ap} < H_{th}$; for example, Displacement $R-T$
3. Displacement due to a positive H_{ap} pulse whose amplitude exceeds H_{th} , provided that the pulse duration is short enough to prevent z from reaching the position of maximum energy z_C at Point C ; for example, Displacement $R-U$

If $H_{ap} > H_{th}$ and the pulse duration is not as short as in Case 3 above, the wall overcomes its energy barrier, and its displacement is inelastic. (This is the source of the *Barkhausen noise*.) It is useful to distinguish between minor and major wall displacements. A *minor* inelastic wall displacement is relatively short or local; hence, the wall area is essentially constant during the switching time. On the other hand, a wall experiencing a *major* inelastic displacement travels a relatively long distance and thus may collide with other walls; its area will vary during the switching time (usually increasing in the beginning and decreasing in the end). A minor inelastic wall displacement results from the obstruction of the wall motion by an energy hill whose $c(dE/dz)_{max} > H_{ap}$ in the vicinity of the initial wall position. For example, Displacement $R-V$ in Fig. 11-16(a) is composed of a potentially elastic displacement followed by a minor inelastic displacement. (In order to avoid ambiguity, we might assume that the displacement is elastic if $z < z_C$ and inelastic if $z \geq z_C$. However, because of the effect of the wall mass, the boundary value of z is actually somewhat smaller than z_C .) Upon termination of the H_{ap} pulse, the wall pulls back (elastically) to Point W , and the net Δz is the difference between the z values at Points W and R . In contrast, a major inelastic wall displacement is long because no obstructing energy hill is encountered by the wall in the vicinity of its original position. For example, the larger of the positive H_{ap} pulses of Fig. 11-16(a) may force another wall in the same specimen to experience a major inelastic displacement, such as Displacement $R'-V'$ in Fig. 11-16(b).

A stable wall position can be achieved only in the range where $d^2E/dz^2 > 0$. Thus, the energy gradient in Fig. 11-16(b) is metastable, i.e., it includes a number of z regions where this condition is satisfied. For $H_{ap} = 0$, the wall may settle at the quiescent point, where $dE/dz = 0$, in any of these regions.

To be exact, a distinction should be made between elasticity and reversibility of a magnetic process, i.e., of wall motion or rotation of magnetization. Reversibility is a thermodynamic property: a magnetic process is reversible if it is performed *quasi-statically* (i.e., infinitely slowly) with *no energy dissipation*; otherwise, it is irreversible. The area enclosed between the transition path and the plot of $c(dE/dz)$ is proportional to the dissipated energy. Thus, all the elastic and inelastic wall displacements shown in Fig. 11-16 (for which the rise time of the H_{ap} pulse is short compared to the switching time) are irreversible. Only if H_{ap} were changed quasi-statically would displacements $R-S$ and $R'-T$ be reversible, because only then would they follow the curve $c(dE/dz)$

(which thermodynamically represents the equation of states of equilibrium at a constant temperature), and would thus involve no energy dissipation. But if H_{ap} is increased very slightly beyond H_{th} , the wall breaks free and moves irreversibly to a position between Points V and W , where $c(dE/dz) = H_{th}$. (Note that reversible tracking of H_{ap} along $c(dE/dz)$ in the region where $d^2E/dz^2 < 0$ is unrealizable because wall positioning in this region is unstable.)

If the magnetization M of a crystallite changes by the motion of a single wall, then ΔM is proportional to Δz . In Fig. 11-17, the *major static $M(H)$ curve* of such a crystallite is obtained by essentially reversible and irreversible wall displacements as H_{ap} is changed quasi-statically in the negative and then in the positive directions. The two extreme stable positions of the wall, designated by $R^{(-)}$ and $R^{(+)}$, correspond to the remanent values of magnetization $-M_r$ and $+M_r$, respectively. For M between $-M_r$ and M_r , H_{th} may be smaller than H_{th} near $M = -M_r$. An example is shown in Fig. 11-17, where a *minor static $M(H)$ loop* is traversed. Furthermore, if the peaks of $c(dE/dz)$ near $R^{(-)}$ are higher than the following ones in an appreciably wide z region, then the major $M(H)$ curve is said to be *re-entrant*.

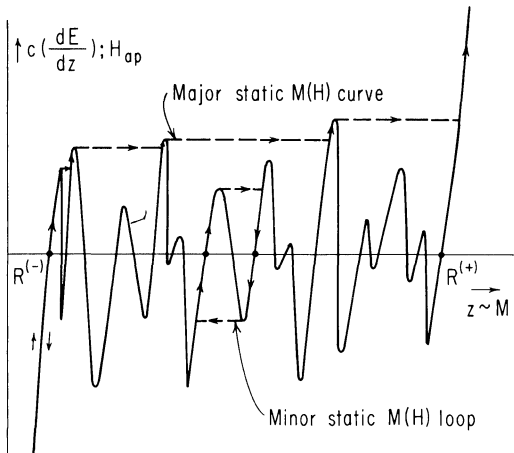


Fig. 11-17. Schematic construction of static $M(H)$ major curve and minor loop due to reversible and irreversible displacements of a single domain wall.

So far we have examined the displacements of a 180° domain wall in a single crystallite. Consider now a polycrystalline “square-loop” specimen, e.g., a ferrite core used in memory or

logic circuits. The specimen contains many 180° walls having $c(dE/dz)$ vs. z plots of different shapes whose features (including the direction of z) vary randomly. Upon application of a step- H field H_{ap} , a number n of domain walls will be displaced inelastically. We assume that these displacements are classified into two groups: np minor displacements (as in Fig. 11-16(a)) and $n(1-p)$ major displacements (as in Fig. 11-16(b)), where p is the portion of the inelastic displacements that are minor ($0 \leq p \leq 1$). The distribution of H_{th} (for both types of displacement) may be described by a probability-density function $f(H_{th})$ with a mean value in the neighborhood of the threshold H_d^{min} of the major static $M(H)$ curve, as shown in Fig. 11-18. On the basis of this description, n increases with H_{ap} because n is proportional to $\int_0^{H_{ap}} f(H_{th}) dH_{th}$. Assuming that major inelastic wall displacements can occur only if $H_{ap} \gtrsim H_d^{min}$,

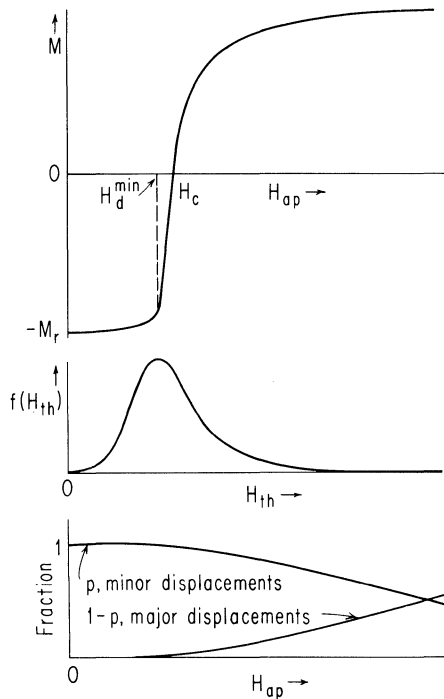


Fig. 11-18. Relations among a static $M(H)$ curve for positive H , a probability-density function of H_{th} , and the portions of minor and major wall displacements in a polycrystalline square-loop specimen.

then p is essentially unity in the region $0 < H_{ap} \lesssim H_d^{\min}$, but as H_{ap} increases beyond H_d^{\min} , p decreases gradually, as shown schematically in Fig. 11-18. The length of an irreversible wall displacement is also a random variable with a similar probability-density function. Due to these random distribution functions, the static $M(H)$ curve of the specimen may appear to be smooth, as shown in Fig. 11-18, but actually consists of a large number of relatively small Barkhausen jumps. In addition to elastic wall displacements and elastic rotation of magnetization, this curve results from minor inelastic wall displacements in the region $0 < H_{ap} \lesssim H_d^{\min}$ and from major and minor inelastic wall displacements in the region $H_d^{\min} \lesssim H_{ap}$. The contribution of the major inelastic wall displacements to the total ΔM for $H_{ap} > H_d^{\min}$ is predominant. The applied magnetic field H_c at which $M = 0$ corresponds to $\Delta M = M_r$, and is called the *coercive force*.

Elastic and inelastic changes in M due to a trapezoidal applied H pulse of amplitude H_{ap} and duration T are superimposed on a static $M(H)$ loop of a polycrystalline square-loop core in Fig. 11-19. Let us examine these changes in the light of the wall displacement in Fig. 11-16: Transition A-B is elastic regardless of the magnitudes of H_{ap} and T . Transition C-D is elastic regardless of T , provided that H_{ap} is smaller than H_{th} of any of the walls corresponding to Point C. Transition A-E is elastic (cf. Newhouse (1957)) even though H_{ap} is much larger than H_{th} at Point A, provided T is so short that H_{ap} is removed before any wall reaches the peak of its first

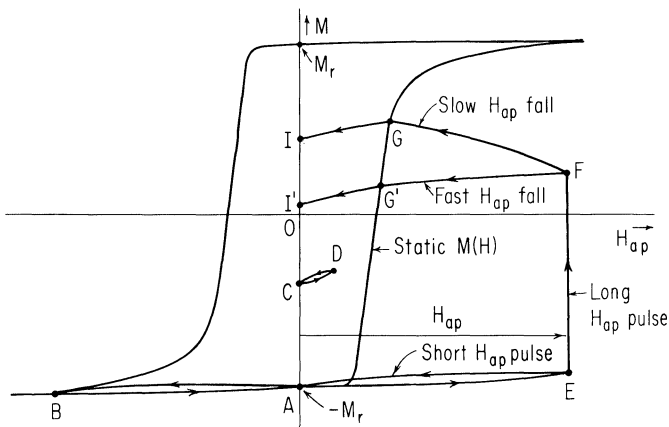


Fig. 11-19. Elastic and inelastic changes in magnetization of a polycrystalline square-loop core.

energy hill. On the other hand, Transition $E-F$ is inelastic because, for most of the walls, $H_{ap} > H_{th}$ and T is long enough. Transition $F-G$ for a long fall time of H_{ap} is inelastic, but for Transition $F-G'$, elastic fallback predominates over any inelastic changes that may occur during the short fall time of H_{ap} . (Referring to Fig. 11-16(b), domains move more slowly where $c(dE/dz) > 0$ than where $c(dE/dz) < 0$, so that, statistically, more domains are expected to fall back (elastically) than to fall forward (inelastically) when H_{ap} is suddenly removed.) Finally, Transitions $G-I$ and $G'-I'$ are both elastic.

11-5 Summary

Magnetic flux density $B = \mu_0(H + M)$ results from two components: magnetic field H due to true currents, and magnetization M due to orbital and spin moments of electrons in a small volume Δv . Different electrons have different quantum numbers n, l, m , and σ whose values may be $n = 1, 2, 3, \dots$; $l = 0, 1, \dots, n - 1$; $m = -l, -l + 1, \dots, l$; and $\sigma = \pm 1/2$. With the z components (along H) of the orbital and spin angular momenta of an electron quantized, the corresponding quantized magnetic moments may have the values $m_{l,z} = m\mu_B$ and $m_{s,z} = \pm\mu_B$, respectively, where μ_B is the Bohr magneton. For an atom in its ground state, the electron spin and orbital moments add vectorially to resultants of quantum numbers $S = \sum\sigma$ and $\mathcal{L} = \sum m$, which then add vectorially to a resultant of quantum number $J = |\mathcal{L} - S|$ (or $\mathcal{L} + S$) for a subshell less (or more) than half full. The quantized component of the total m along H is $m_{Jz} = g\mathcal{M}\mu_B$, where $\mathcal{M} = -J, -J + 1, \dots, J$ and $g = (3/2) + [S(S + 1) - \mathcal{L}(\mathcal{L} + 1)]/[2J(J + 1)]$. In most magnetic materials that contain iron-group elements, as a result of the electrostatic crystal field, the orbital moment may be "quenched," that is, $\mathcal{L} \approx 0$, and m is essentially the net spin moment only.

The net magnetization M of materials having nonzero atomic magnetic moments is affected by thermal disorder (which tends to cause paramagnetism) and direct or indirect exchange interactions, which tend to align neighboring spins parallel (causing ferromagnetism) or antiparallel (causing antiferromagnetism if spin moments exactly cancel or ferrimagnetism otherwise). Below the Curie temperature T_c , a ferromagnetic or ferrimagnetic material possesses a nonzero saturation magnetization M_s , but above T_c it becomes paramagnetic and $M_s = 0$. The cations in a simple ferrite, whose unit cell consists of eight $Me^{++}Fe_2^{+++}O_4$ molecules in a spinel structure, are divided into A and B types

(each comprising one or two sublattices) of oppositely aligned spins due to a predominant negative A - B superexchange interaction, but since $m_B \neq m_A$, the net $M_s = |m_B - m_A|$ is nonzero. The $M(H)$ characteristics of magnetic materials vary between two extremes, a linear $M(H)$, $\mathbf{M} = \chi\mathbf{H}$, for which $M_r \approx 0$, and a square-loop $M(H)$, for which $M_r \approx M_s$, where M_r is the maximum remanent M .

A partially demagnetized ferromagnetic (or ferrimagnetic) specimen is divided into magnetic domains, each saturated along a certain direction by exchange (or superexchange) interaction. A domain structure corresponds to the minimum sum of four energies that are involved in creating the domains and the walls between them: exchange, magnetostatic, anisotropy, and magneto-elastic energies.

An applied magnetic field may change the magnetization of a specimen, elastically or inelastically, by rotation of magnetization or domain-wall motion or both. Rotation of magnetization with low viscous damping may be described by the phenomenological Landau-Lifshitz or Gilbert equation, although for high viscous damping, the latter should be used. A schematic plot of energy gradient versus wall position may be used to illustrate the difference between elastic and inelastic (and between reversible and irreversible) wall displacements. A distinction is made between minor and major inelastic wall displacements, which involve constant and varying wall areas, respectively. A random variation of such wall displacements in a polycrystalline specimen results in relatively smooth major and minor static $M(H)$ loops.

MAGNETIC FLUX-SWITCHING MODELS

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This chapter deals with models (mathematical expressions) that describe the static and dynamic switching properties of square-loop ferrite cores. These models may be extended to tape-wound

metallic cores if the effects of eddy currents are included. In Sec. 12-1, relations are established for magnetomotive force (mmf) and magnetic flux in single-leg and multileg cores. Experiments for studying the switching properties of a core are presented in Sec. 12-2. Models for static properties are proposed in Sec. 12-3. Elastic flux-switching models are developed in Sec. 12-4; it is shown that two separate components of elastic switching may be identified and modeled. Models for inelastic flux-switching, which usually accounts for most of the flux switching, are developed in Sec. 12-5; we similarly identify and model two different components of inelastic switching. These models are applied in Sec. 12-6 to computation on a digital computer of flux switching in magnetic circuits, and the results are compared with experimental data.

12-1 MMF and Flux in Magnetic Cores

The basic properties of magnetic materials are described in Chap. 11 in terms of the magnetization M and the magnetic field H . The magnitudes of M and H , which are point quantities, cannot be measured directly in magnetic circuits. Instead, their values may be deduced under simple geometrical conditions from measurements of certain *bulk properties* of a magnetic core.

Magnetic Field and Magnetomotive Force. Consider a closed-path magnetic core of uniform material and uniform cross section, as shown in Fig. 12-1. Currents i_1 , i_2 , and i_3 , which are applied to

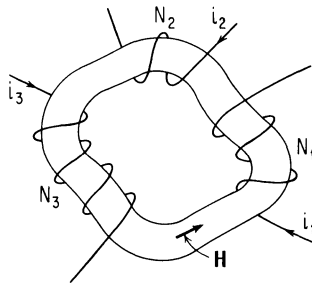


Fig. 12-1. Application of magnetomotive force to a closed-path magnetic core.

three windings of N_1 , N_2 , and N_3 turns, respectively, generate a magnetic field \mathbf{H} along the core. By definition, the mmf (magneto-motive force) along a path l is

$$F = \int_l \mathbf{H} \cdot d\mathbf{l} \quad (12-1)$$

Following Ampere's circuital law, the line integral of $\mathbf{H} \cdot d\mathbf{l}$ over a closed path is equal to the ampere-turns of the current linkage enclosed, that is

$$\oint \mathbf{H} \cdot d\mathbf{l} = \sum_k N_k i_k \quad (12-2)$$

For reference, we assume that $N_k i_k$ is positive if i_k inside the closed path comes out of the paper (generating \mathbf{H} in the counter-clockwise direction by the right-hand rule) and vice versa. Thus, the mmf acting on the core of Fig. 12-1, for example, is

$$F = N_1 i_1 - N_2 i_2 + N_3 i_3 \quad (12-3)$$

If the component of \mathbf{H} along the path of integration is constant, then Eq. (12-2) reduces to

$$H = \frac{1}{l} \sum_k N_k i_k \quad (12-4)$$

where l also designates the length of Path l . A constant circumferential H along the core of Fig. 12-1 may be realized by using a large number of turns uniformly distributed along the core. With a toroidal core, a constant circumferential H may also be achieved with a single-turn central conductor. (The current returns via a remote wire or via a concentric tube outside the core.) In most practical magnetic circuits, neither of these winding conditions is met; nevertheless, Eq. (12-4) is still applicable because the variations in the circumferential H along the core are negligible. Hammond (1955) explained this phenomenon by considering a coil of N turns that carries a step current I , as shown in Fig. 12-2(a). The magnetic field H_A at Point A (the middle of the coil) is much larger than the magnetic field H_B at Point B (far from the coil). Suppose that the same coil is now wrapped around a switchable ferromagnetic (or ferrimagnetic) core, as shown in Fig. 12-2(b). At the instant that a step I is applied, we have $H_A \gg H_B$ as in Fig. 12-2(a), and, assuming that H_A and H_B are in a direction to

switch M inelastically, then M at Point A changes much more than M at Point B . This results in a large build-up of magnetic poles ($\nabla \cdot \mathbf{M}$) throughout the core and especially on the core surface, as shown in Fig. 12-2(b). These poles generate a magnetic field that subtracts from the H due to NI at Point A and adds to the H due to NI at Point B . As a result, the initial difference between the magnitudes of M at Points A and B is reduced, and the pole density is decreased until $H_A \approx H_B$ (H_A is finally only slightly larger than H_B). In other words, the presence of magnetic poles in a switchable core tends to equalize H along the core, and therefore Eq. (12-4) is applicable to inelastic switching of practical (not too thin) cores even if the winding is not applied symmetrically.

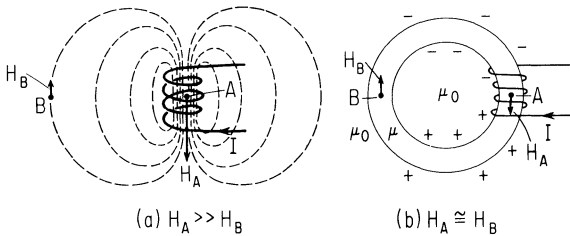


Fig. 12-2. Effect of magnetic poles on equalization of H (Hammond, 1955).

Magnetic Flux. The magnetic flux through a surface of area A is, by definition,

$$\phi = \int_A \mathbf{B} \cdot d\mathbf{A} \tag{12-5}$$

where $\mathbf{B} = \mu_0(\mathbf{M} + \mathbf{H})$ (Eq. (11-5)). If the normal component of the flux density, B_n , is constant over A , then Eq. (12-5) reduces to

$$\phi = B_n A \tag{12-6}$$

Multileg Magnetic Core. Equations (12-1) through (12-6) are applicable to multileg cores as well as to single-leg cores. As expressed by Eq. (5-4), and also following Eqs. (12-1) and (12-2), for every closed magnetic path composed of ℓ legs and linked by m windings, we have

$$\sum_{j=1}^{\ell} F_j = \sum_{k=1}^m N_k i_k \tag{12-7}$$

where F_j is the mmf along the j th leg. Neglecting air flux, following Eq. (12-5) and Maxwell's equation $\oint_A \mathbf{B} \cdot d\mathbf{A} = 0$, then in every core junction of n legs

$$\sum_{j=1}^n \phi_j = 0 \quad (12-8)$$

where ϕ_j is the flux of the j th leg, and hence also

$$\sum_{j=1}^n \dot{\phi}_j = 0 \quad (12-9)$$

Consider, for example, the saturable core and its mmf drives in Fig. 12-3. The core consists of three legs, 1, 2, and 3, and two junctions, A and B . Assume that the positive direction of F in each leg is the same as that shown for ϕ , that is, counterclockwise around the large aperture. Applying Eqs. (12-7) and (12-9) to this case, we obtain

$$F_1 + F_2 = N_{a1} i_a - N_{a2} i_a - N_{b1} i_b \quad (12-10)$$

$$F_3 - F_2 = N_{a2} i_a - N_{a3} i_a + N_{b3} i_b + N_{c3} i_c \quad (12-11)$$

and

$$\dot{\phi}_1 - \dot{\phi}_2 - \dot{\phi}_3 = 0 \quad (12-12)$$

Note that there are two independent loop (path) equations and one independent node (junction) equation. These three equations include six unknowns, i.e., the ϕ and F of each of the three legs. The other

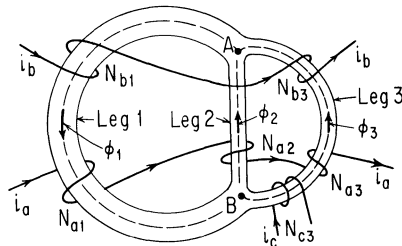


Fig. 12-3. Current drives and flux closure in a three-leg core.

three equations that are necessary to solve for these six unknowns are based on the functional relationship

$$\dot{\phi}_j = \dot{\phi}(\dot{F}_j, F_j, \phi_j, t) \quad (12-13)$$

for each leg ($j = 1, 2, 3$). Derivation of the functional form of this relationship, which describes the magnetic flux-switching properties of a leg, is the main topic of this chapter.

In general, if a core has n_ℓ legs and n_j junctions, there are $(n_\ell - n_j + 1)$ independent loop equations and $(n_j - 1)$ independent node equations (Guilleman (1953)), i.e., a total of n_ℓ independent network equations. (For a single-leg core, such as a toroid, $n_\ell = n_j = 1$ since the leg closes on itself.) These n_ℓ equations are supplemented by additional n_ℓ flux-switching equations, each of the form of Eq. (12-13), providing a total of $2n_\ell$ equations for the solution of the $2n_\ell$ unknowns, i.e., the ϕ and F of each of the n_ℓ legs.

The magnetic properties of each leg in a multileg core are similar to the properties of a single-leg core of the same material and of the same cross section and length. However, the measurement of these properties in a multileg core is difficult because the F and ϕ of each leg depend on the F and ϕ of all the other legs (as is illustrated in the example above). Consequently, whenever possible, these properties are measured on a single-leg core with the simplest geometry, namely, a toroid.

12-2 Flux-Switching Experiments

Flux-switching models to be developed here are based on the results of fundamental flux-switching experiments performed on a thin toroidal ferrite core. Two arrangements of the core and the drive and sense windings are shown in Fig. 12-4. The arrangement in Fig. 12-4(a) may be used if the rise time of the *test* mmf (which sets the core or drives it further into saturation) is not too short (e.g., about 20 nanoseconds or longer). However, for shorter rise times, an arrangement such as in Fig. 12-4(b) should be used in order to minimize the ringing and distortion due to the capacitance of the sense and drive windings.

In Fig. 12-4(a), the core is driven by two mmf drives: (1) A *clear* mmf F_{CL} , generated by a current pulse of amplitude I_{CL} through a distributed winding of N_{CL} turns, which switches the core

to negative saturation, and (2) a *test* mmf F , generated by a current pulse of amplitude I through a single-turn, central-conductor winding, which switches the core to any level between saturation flux levels $-\phi_s$ and $+\phi_s$. The resulting $\dot{\phi}(t)$ is sensed by a *sense* winding of N_v turns, and the voltage $N_v \dot{\phi}(t)$ is applied to an oscilloscope, or to an integrator if we wish to measure the change in flux, $\Delta\phi$.

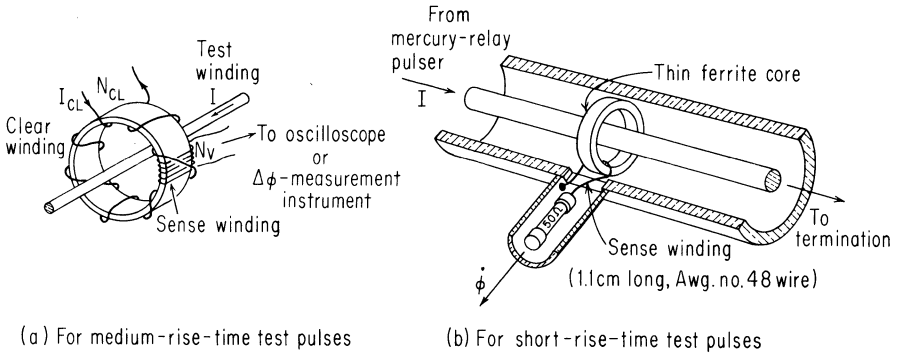


Fig. 12-4. A thin core and windings in flux-switching experiments (Nitzan *et al.*, 1966).

The arrangement of Fig. 12-4(b) is similar to that of Fig. 12-4(a) except for the following: First, both the *clear* and *test* mmf are generated by applying currents of opposite polarities to a single-turn, central-conductor winding. Second, $\dot{\phi}$ is sensed by a single-turn winding made of as short and fine a wire as practical in order to minimize its capacitance. Third, the short-rise-time *clear* and *test* current pulses are generated by discharging a coaxial transmission line into a matched termination via a mercury-relay switch. We shall refer to this arrangement later in this chapter when dealing with fast-rising drive pulses.

Typical waveforms of trapezoidal *clear* and *test* pulses used in Fig. 12-4(a) are shown in Fig. 12-5(a). The *clear* pulse has a duration T_{CL} , and the *test* pulse has a 10-percent to 90-percent rise time T_r and a duration T . The resulting $\dot{\phi}(t)$ waveforms are shown in Fig. 12-5(b). The corresponding variations of ϕ versus F and $\dot{\phi}$ versus ϕ are shown in Fig. 12-5(c) and (d), respectively.

In order to assure a reproducible remanent state of $\phi = -\phi_r$, the amplitude $N_{CL}I_{CL}$ and the duration T_{CL} must be large enough to switch the core far into negative saturation. In some cases it is desirable to switch the core first into positive saturation, before switching it into negative saturation, in order to wipe out possible 360° Bloch walls (see Hewitt and Overn (1963)).

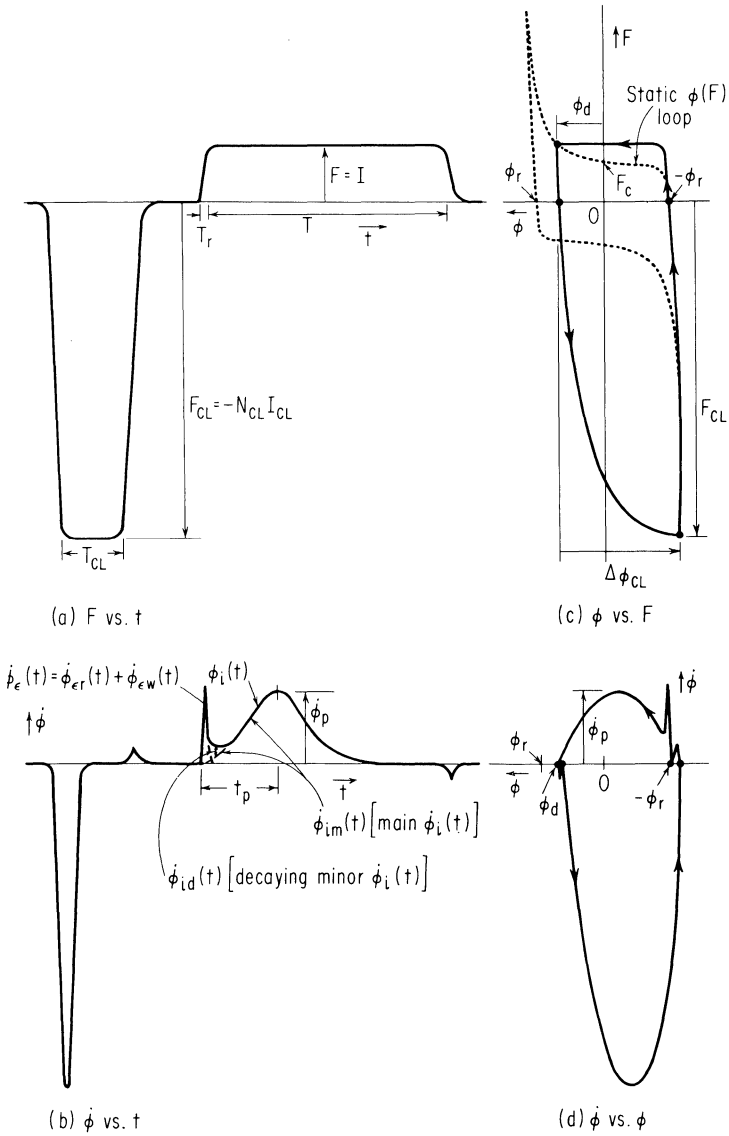


Fig. 12-5. Waveforms of $F(t)$ and $\dot{\phi}(t)$ and variations of $\phi(F)$ and $\dot{\phi}(\phi)$ during a full cycle in a flux-switching experiment.

The resulting $\dot{\phi}(t)$ waveform (Fig. 12-5(b)) is composed of an elastic $\dot{\phi}(t)$ spike, denoted by $\dot{\phi}_\epsilon(t)$, and a bell-shaped inelastic $\dot{\phi}(t)$, denoted by $\dot{\phi}_i(t)$. We shall show later that $\dot{\phi}_\epsilon(t)$ has two components, $\dot{\phi}_{\epsilon r}(t)$ due to elastic rotation of magnetization and $\dot{\phi}_{\epsilon w}(t)$ due to

elastic domain-wall motion, and, if F is too low to cause inelastic rotation of magnetization, that $\dot{\phi}_i(t)$ also has two components, a decaying component $\dot{\phi}_{id}(t)$ due to minor domain-wall displacements, and a bell-shaped main component $\dot{\phi}_{im}(t)$ due to major domain-wall displacements. The smaller the values of T_r and F , the more distinguishable are the components $\dot{\phi}_\epsilon(t)$ and $\dot{\phi}_{id}(t)$. Masking of these components by $\dot{\phi}_{im}(t)$ during the clearing time in Fig. 12-5(b) is caused by the relatively long rise time and high amplitude of the *clear* mmf pulse.

With a long *test* pulse (ideally, $T \rightarrow \infty$), flux switching is completed during the pulse, that is, ϕ reaches a static value, ϕ_d . (See Fig. 12-5(c) and compare with Figs. 11-17 and 11-18.) The measurement of the flux change $\Delta\phi$ needed to determine ϕ_d is performed by applying the sensed voltage $N_v \dot{\phi}(t)$ (Fig. 12-4(a)) to an R - C integrator. Due to integrator decay, however, the measured $\Delta\phi$ has an error which is smaller the smaller the switching time. For this reason, the set flux $\Delta\phi = \phi_r + \phi_d$ is determined by measuring the flux change $\Delta\phi_{CL}$ during the clearing time and subtracting the elastic component, that is, $\Delta\phi_{CL}$ corresponding to $F = 0$ (see Fig. 12-5(c)). By repeating the measurement of ϕ_d for various positive and negative values of F , one obtains the major static $\phi(F)$ curve. If F is large enough to saturate the core, then $\phi_d(+F) = -\phi_d(-F)$. On the basis of this antisymmetry, the reference $\phi = 0$ is established by letting $F = N_{CL} I_{CL} = -F_{CL}$ and dividing the corresponding $|\Delta\phi_{CL}|$ by two, that is, ϕ_d at $F = N_{CL} I_{CL}$ is equal to $|\Delta\phi_{CL}|/2$. Once the reference $\phi = 0$ is established, the remanent flux ϕ_r is determined by equating $-\phi_r$ to ϕ_d corresponding to $F = 0$. The static $\phi(F)$ curve intersects the F axis ($\phi_d = 0$) at the *coercive* mmf F_c . If we now add a second curve antisymmetric to the static $\phi(F)$ curve, we obtain the overall static $\phi(F)$ loop, which is shown dotted in Fig. 12-5(c).

Flux-switching properties from a remanent state $\phi = -\phi_r$, such as is shown in Fig. 12-5, are classified into three categories:

1. static $\phi(F)$ curve
2. elastic $\dot{\phi}(t)$: $\dot{\phi}_\epsilon(t) = \dot{\phi}_{er}(t) + \dot{\phi}_{ew}(t)$
3. inelastic $\dot{\phi}(t)$: $\dot{\phi}_i(t) = \dot{\phi}_{id}(t) + \dot{\phi}_{im}(t)$

Flux-switching models describing each of these properties are presented in the following three sections.

12-3 Static $\phi(F)$ Models

Hyperbolic Model for Static $M(H)$. Consider a toroidal core of dimensions r_i (inside radius), r_o (outside radius), and h (height). If the core is thin (that is, r_o/r_i is close to unity) and driven centrally, as in Fig. 12-4, then M and H may be assumed to be uniform across the core. In this case, the static $M(H)$ curve may be obtained directly from the static $\phi(F)$ curve in Fig. 12-5(c) by using the relations

$$\phi = (M + H)\mu_0 h(r_o - r_i) \approx M\mu_0 h(r_o - r_i) \tag{12-14}$$

and

$$F = H\pi(r_o + r_i) \tag{12-15}$$

It is found empirically that the static $M(H)$ curve of a ferrite core may be described quite closely by two hyperbolas, one for the saturation region and the other for the nonsaturation region, which intersect at $H = H_d^{\min}$, as shown in Fig. 12-6. Denoting the static M value for a given H value by M_d , we find that

$$M_d = \begin{cases} -M_r - (M_s - M_r) \frac{H}{H - H_a} & \text{for } H \leq H_d^{\min} \tag{12-16a} \\ -M_r + (M_s + M_r) \frac{H - H_q}{H - H_n} & \text{for } H \geq H_d^{\min} \tag{12-16b} \end{cases}$$

where M_s is the saturation magnetization and H_a, H_n , and H_q are empirical material parameters. Note that the asymptotes of the hyperbola describing $M_d(H)$ for $H \leq H_d^{\min}$ are $M = -M_s$ and $H = H_a$ and that the asymptotes of the hyperbola describing $M_d(H)$ for $H \geq H_d^{\min}$ are $M = M_s$ and $H = H_n$.

For either a thin or a thick core, $M_r/M_s = \phi_r/\phi_s$, where $\phi_s = M_s\mu_0 h(r_o - r_i)$ is the saturation flux. Equating Eqs. (12-16a) and (12-16b) in order to find their intersection point, and replacing M_r/M_s by ϕ_r/ϕ_s , the following expression is found for the static threshold field

$$H_d^{\min} = \frac{1}{4} \left[H' - \sqrt{H'^2 - 8 \left(1 + \frac{\phi_r}{\phi_s} \right) H_a H_q} \right] \tag{12-17}$$

where

$$H' = H_a + H_q + H_n + \frac{\phi_r}{\phi_s} (H_a + H_q - H_n) \tag{12-18}$$

By equating Eq. (12-16b) first to zero and then to M_r , and again replacing M_r/M_s by ϕ_r/ϕ_s , we obtain expressions for the coercive force H_c and the field H_r at which $M_d = M_r$ (see Fig. 12-6)

$$H_c = H_q + \frac{\phi_r}{\phi_s} (H_q - H_n) \tag{12-19}$$

and

$$H_r = \frac{H_q + (H_q - 2H_n)(\phi_r/\phi_s)}{1 - (\phi_r/\phi_s)} \tag{12-20}$$

The *squareness* of the static $M(H)$ curve for $H \geq H_d^{\min}$ may be described by the ratio H_q/H_n , where $H_q/H_n \geq 1$. The closer H_q/H_n is to unity, the sharper is the upper knee of the static $M(H)$ curve. In the limit, as $H_q/H_n \rightarrow 1$, the static $M(H)$ region expressed by Eq. (12-16b) becomes ideally square.

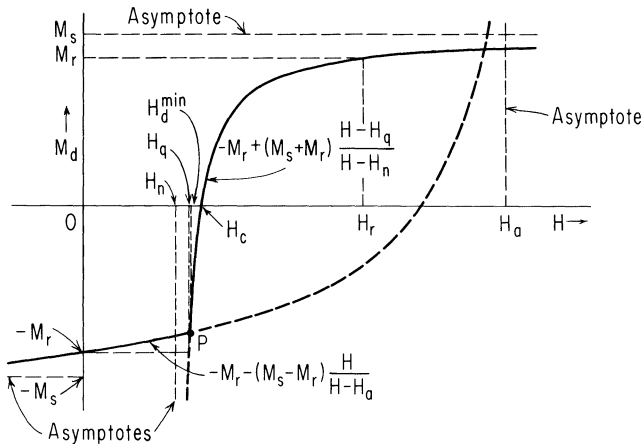


Fig. 12-6. Hyperbolic model for the static $M(H)$ curve of a ferrite core.

A Model for the Static $\phi(F)$ Curve. The hyperbolic functions in Eqs. (12-16a) and (12-16b) describe the static $M(H)$ curve of the core material and also, in conjunction with Eqs. (12-14) and (12-15), the static $\phi(F)$ curve of a thin toroid. This hyperbolic model will now be used to calculate the static $\phi(F)$ curve of a constant-width leg of more general shape.

Fig. 12-7 shows the top view of a leg of constant width w , constant height h , angle α , length of the short edge l_i , and length of the long edge l_o . (For a toroid, $\alpha = 2\pi$, $l_i = 2\pi r_i$, and $l_o = 2\pi r_o$.)

A curve of length l is drawn at a distance x from the short edge. Let R be the radius of curvature of the short edge (R varies along the leg). A segment of angle $d\theta$ is drawn perpendicular to the leg edges. The difference between the segment elements dl and dl_i is $d(l - l_i) = (R + x)d\theta - Rd\theta = xd\theta$, which, upon integration along the leg, yields $(l - l_i) = x\alpha$. Hence,

$$l = l_i + \alpha x \tag{12-21}$$

where, since $l = l_o$ for $x = w$,

$$\alpha = \frac{l_o - l_i}{w} \tag{12-22}$$

The angle α may vary between two extremes: $\alpha = 0$ (for a leg whose ends are parallel and, therefore, $l_i = l_o$) and $\alpha = 2\pi$ (for a single-leg core, such as in Fig. 12-1, or a toroid).

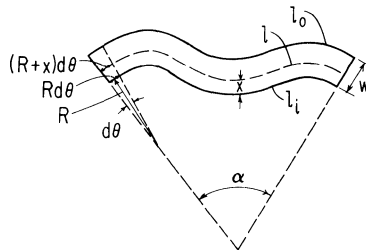


Fig. 12-7. A constant-width leg.

Assuming that $H = F/l$, that is, H is constant along a path of constant x in Fig. 12-7, application of Eq. (12-21) gives

$$H = \frac{F}{l_i + \alpha x} \tag{12-23}$$

Substitution of Eq. (12-23) into the hyperbolic model for static $M(H)$ (Eqs. (12-16a) and (12-16b)) results in $M_d(F, x)$ functions. Integrating $\mu_0 M_d(F, x) h dx$ from $x = 0$ to $x = w$, we obtain the following expressions for the static $\phi(F)$ curve in three regions of F :

$$\phi_d(F) = \begin{cases} V_1 F \ln \left(\frac{F - H_a l_o}{F - H_a l_i} \right) - \phi_r & \text{for } F \leq F_d^{\min} & (12-24a) \\ V_2 \left[\frac{F}{H_d^{\min}} - l_i + F \left(\frac{1}{H_n} - \frac{1}{H_q} \right) \ln \left(\frac{1 - (H_n/H_d^{\min})}{1 - (H_n l_i/F)} \right) \right] - \phi_r & \text{for } F_d^{\min} \leq F \leq H_d^{\min} l_o & (12-24b) \\ V_2 \left[l_o - l_i + F \left(\frac{1}{H_n} - \frac{1}{H_q} \right) \ln \left(\frac{F - H_n l_o}{F - H_n l_i} \right) \right] - \phi_r & \text{for } H_d^{\min} l_o \leq F & (12-24c) \end{cases}$$

where

$$V_1 = \frac{\phi_s - \phi_r}{(l_o - l_i) H_a} \quad (12-25)$$

$$V_2 = \frac{(\phi_s + \phi_r) H_q}{(l_o - l_i) H_n} \quad (12-26)$$

and

$$F_d^{\min} = H_d^{\min} l_i \quad (12-27)$$

Note that the material at the inner wall of the core reaches switching threshold as F reaches $H_d^{\min} l_i$, and that the material at the outer wall reaches threshold as F reaches $H_d^{\min} l_o$. For $F_d^{\min} \leq F \leq H_d^{\min} l_o$, the term representing flux change in the outer section of the leg, where $H < H_d^{\min}$, is negligible compared with the total flux change. For this reason, this term is not included in Eq. (12-24b).

The contribution of "air flux" ϕ_{air} is also not included in Eqs. (12-24) because in practical applications it is usually negligible (unless $|F| \gg F_c$). However, to determine the magnitude of ϕ_{air} in the core itself, we apply Eq. (12-23), and integrate $h\mu_0 H dx = h\mu_0 F dx / (l_i + \alpha x)$ from $x = 0$ to $x = w$. We thus obtain

$$\phi_{\text{air}} = F \frac{A\mu_0}{l_o - l_i} \ln \left(\frac{l_o}{l_i} \right) \quad (12-28)$$

where $A = hw$ is the cross-sectional area of the leg. The total air flux linking a loose winding around the core is larger than ϕ_{air} given by Eq. (12-28).

Determination of Parameters. Seven parameters are needed to compute $\phi_d(F): l_i$ and l_o (dimensions), ϕ_r and ϕ_s (flux capacities), and $H_a, H_n,$ and H_q (material field parameters). Because of possible tapering in a ferrite core, l_i and l_o should be measured on both faces of the core and averaged. The value of ϕ_r is readily available from the measured static $\phi(F)$ curve (Fig. 12-5(c)). The remaining parameters may be computed by curve fitting of Eqs. (12-24) with the measured static $\phi(F)$ curve. (For some ferrite cores, $\phi_s \approx 1.1\phi_r$ in a region of practical interest, e.g., for $|F| \lesssim 10F_c$, and, therefore, ϕ_s need not be computed.) Curve fitting of experimental data with a given model is generally achieved by the method of least-mean-square error, i.e., by minimizing the sum $\sum_j E_j^2$, where E_j is the difference between the computed and the measured variable. In this case, $E_j = \phi_{d,comp} - \phi_{d,exp}$ at the F value of the j th experimental point. This type of computation is most economically performed on a digital computer.

Experimental Verification. The model for static $\phi(F)$ in Eqs. (12-24) is found to be quite useful for a variety of ferrite cores. An example of a very close agreement with experimental data is shown in Fig. 12-8. In this example, a three-leg core was utilized

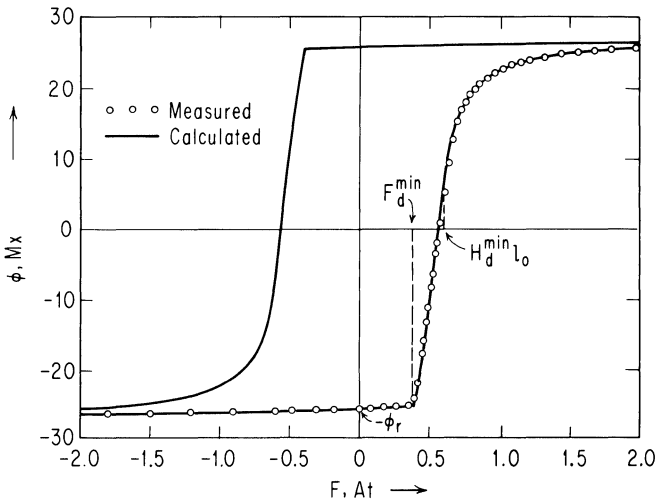


Fig. 12-8. Measured and computed static $\phi(F)$ curve at room temperature. Material (Telemeter Magnetics T-5 ferrite) parameters: $\phi_r = 25.67$ Mx; $\phi_s = 27.6$ Mx; $H_a = 230$ At/m; $H_n = 32.0$ At/m; $H_q = 36.0$ At/m. Dimensions: $l_i = 10.56$ mm; $l_o = 16.47$ mm; $h = 1.31$ mm. (Nitzan, 1964.)

in forming a "core" consisting effectively of two legs of identical cross section. Flux switching in the third leg was prevented by linking it with a short-circuited turn. The values of l_i and l_o given in the figure caption are the sums of l_i and l_o of the two switchable legs.

Discontinuous Static $\phi(F)$ Curves. If the static $M(H)$ curve is re-entrant, then, as the applied H reaches the H threshold, M_d jumps to some value M_{dd} between $-M_r$ and $+M_r$. As explained in connection with Fig. 11-17, this phenomenon occurs if the peaks of the energy gradient versus wall position corresponding to $M = -M_r$ are higher than the following peaks in the region $-M_r < M \leq M_{dd}$. In this case, Eqs. (12-16) are still directly applicable, except that H_d^{\min} is replaced by a threshold field larger than H_d^{\min} calculated from Eqs. (12-17) and (12-18).

Similarly, if the measured static $\phi(F)$ curve exhibits a jump to some value ϕ_{dd} between $-\phi_r$ and ϕ_r , then Eqs. (12-24) in conjunction with Eqs. (12-17) and (12-18) are still directly applicable, except that $F_d^{\min} > H_d^{\min} l_i$. (Note that if $F_d^{\min} > H_d^{\min} l_o$, then Eq. (12-24b) is bypassed.) An example is shown in Fig. 12-9 for three nominally identical commercial ferrite cores.

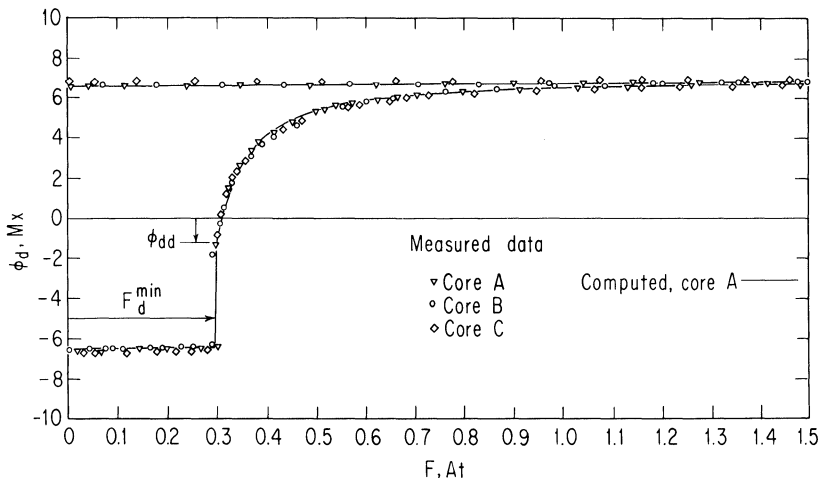


Fig. 12-9. Measured and computed discontinuous static $\phi(F)$ curves at $T = 25^\circ\text{C}$. Core type: Lockheed 100SC1 (100 mils OD; 70 mils ID); $\phi_r = 6.52$ Mx; $\phi_s = 7.17$ Mx; $H_a = 307$ At/m; $H_n = 36.0$ At/m; $H_q = 40.8$ At/m; $l_i = 5.59$ mm; $l_o = 7.98$ mm; $h = 0.762$ mm (Nitzan *et al.*, 1966).

12-4 Elastic $\dot{\phi}(t)$ Models

Introduction. It was shown in Sec. 11-4 that application of an external H pulse, H_{ap} , may cause the magnetization M to switch by either rotation of magnetization or by domain-wall motion or both. In each case, the switching may be inelastic or elastic, depending on whether or not there is a net change in magnetization when H_{ap} is removed. Typical experimental data of elastic and inelastic $\dot{\phi}(t)$ waveforms and the corresponding variation of $\dot{\phi}(\phi)$ and $\phi(F)$ were shown in Fig. 12-5. The elastic $\dot{\phi}(t)$ has two components, that is

$$\dot{\phi}_\epsilon(t) = \dot{\phi}_{\epsilon r}(t) + \dot{\phi}_{\epsilon w}(t) \quad (12-29)$$

where $\dot{\phi}_{\epsilon r}(t)$ is generated by elastic rotation of magnetization and $\dot{\phi}_{\epsilon w}(t)$ is generated by elastic domain-wall motion. For relatively slow-rising F pulses, we will find that $\dot{\phi}_\epsilon(t)$ may be modeled by the simple relation $\dot{\phi}_\epsilon = \epsilon \dot{F}$, where ϵ is a coefficient. However, the response is more complex for fast-rising F pulses. The purpose of the following two sections is to develop the equations of motion for each of the $\dot{\phi}_\epsilon$ components, first assuming fast-rising F pulses and then simplifying the results for the cases of medium-rising and slow-rising F pulses.

A Model for $\dot{\phi}_\epsilon(t)$ Due to Rotation of Magnetization. Consider a single crystallite and assume that its magnetization M is saturated along an internal field $H_i \approx H_k + H_{dm}$, where H_k is the anisotropy field (Eq. (11-27)), and H_{dm} is the demagnetizing field. An applied field H_{ap} causes M to spiral within a small solid angle θ_0 into alignment with the total field $H = H_i + H_{ap}$, as shown in Fig. 12-10. Let the plane formed by H_i and H_{ap} define the $y-z$ plane, and let the resultant total field $H = H_i + H_{ap}$ be along the z axis. The angle between H and M_0 (the initial M) is θ_0 , and the angle between H and H_{ap} is ψ .

Assuming that H is constant in time, then on the basis of the Landau-Lifshitz equation, Eq. (11-32), or the Gilbert equation, Eq. (11-33), the variations of $\theta(t)$ and $\varphi(t)$ during the transient time are expressed by Eqs. (11-38) and (11-39), respectively. The component of $\dot{M}(t)$ along H_{ap} is sensed during this transient time. Defining the direction of H_{ap} as the y' axis, we wish to calculate $M_a(t)$, the component of $M(t)$ along the y' axis.

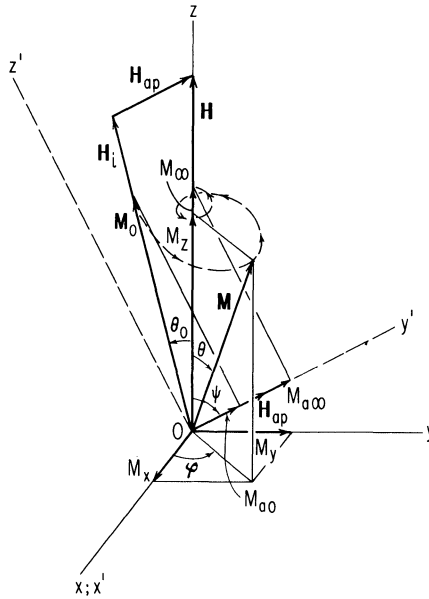


Fig. 12-10. Damped precession of a magnetization vector toward alignment with the total field H.

The components of M in the (x, y, z) coordinate system are

$$\left. \begin{aligned} M_x &= M_s \sin \theta \cos \varphi \\ M_y &= M_s \sin \theta \sin \varphi \\ M_z &= M_s \cos \theta \end{aligned} \right\} \quad (12-30)$$

where M_s is the magnitude of M . Since the (x', y', z') coordinate system is obtained by rotating the (x, y, z) coordinate system around the x axis by the angle $(\pi/2 - \psi)$, we obtain

$$M_a = M_s (\sin \theta \sin \varphi \sin \psi + \cos \theta \cos \psi) \quad (12-31)$$

Substitution of Eqs. (11-38) and (11-39) into Eq. (12-31) yields

$$M_a(t) = M_s \frac{\left[1 - e^{-2(t/\tau)} \tan^2(\theta_0/2) \right] \cos \psi - 2 e^{-(t/\tau)} \tan(\theta_0/2) \cos(\Omega t) \sin \psi}{1 + e^{-2(t/\tau)} \tan^2(\theta_0/2)} \quad (12-32)$$

where τ and Ω are expressed in Eqs. (11-36) and (11-37), respectively. Since, usually, the value of θ_0 under elastic-switching

conditions is small, then $\tan^2(\theta_0/2) \ll 1$ and Eq. (12-32) reduces to

$$M_a(t) = M_s \cos \psi - 2M_s \sin \psi \tan\left(\frac{\theta_0}{2}\right) e^{-(t/\tau)} \cos(\Omega t) \quad (12-33)$$

Differentiating Eq. (12-33) with respect to time, we obtain

$$\dot{M}_a(t) = 2M_s \sin \psi \tan\left(\frac{\theta_0}{2}\right) \sqrt{\frac{1}{\tau^2} + \Omega^2} e^{-(t/\tau)} \sin\left[\Omega t + \tan^{-1}\left(\frac{1}{\Omega \tau}\right)\right] \quad (12-34)$$

We now wish to show that Eqs. (12-33) and (12-34) have the same forms as the solutions to the second-order differential equation

$$M_a + \delta_r \dot{M}_a + \eta_r \ddot{M}_a = \chi_r H_{ap} + M_{a0} \quad (12-35)$$

where χ_r is the rotational susceptibility and M_{a0} is the initial value of M_a . Assuming that initially $\dot{M}_a = 0$, the Laplace transform of Eq. (12-35) for a step $H_{av}(t)$ is

$$M_a(s) = M_{a0} \frac{s^2 + s(\delta_r/\eta_r) + (\chi_r H_{ap} + M_{a0})/(M_{a0} \eta_r)}{s \left\{ s + [\delta_r/(2\eta_r)] \right\}^2 + (1/\eta_r) - [\delta_r/(2\eta_r)]^2} \quad (12-36)$$

For the underdamped condition (that is, $\delta_r < 2\sqrt{\eta_r}$), which is quite likely to be the case (cf. Smith (1958); Wolf (1961); Nitzan and Hesterman (1967)), the inverse function of Eq. (12-36) yields

$$M_a(t) = M_{a0} + \chi_r H_{ap} - \frac{\chi_r H_{ap}}{\sqrt{1 - [\delta_r^2/(4\eta_r)]}} e^{-[\delta_r/(2\eta_r)]t} \cos\left[\sqrt{\frac{1}{\eta_r} - \left(\frac{\delta_r}{2\eta_r}\right)^2} t - \sin^{-1} \zeta_r\right] \quad (12-37)$$

where

$$\zeta_r = \frac{\delta_r}{2\sqrt{\eta_r}} \quad (12-38)$$

Differentiating Eq. (12-37) with respect to time, we obtain

$$\dot{M}_a(t) = \frac{\chi_r H_{ap}}{\eta_r \sqrt{(1/\eta_r) - [\delta_r/(2\eta_r)]^2}} e^{-[\delta_r/(2\eta_r)]t} \sin\left[\sqrt{\frac{1}{\eta_r} - \left(\frac{\delta_r}{2\eta_r}\right)^2} t\right] \quad (12-39)$$

Equations (12-33) and (12-37) are of the same form, except for the phase angle $\sin^{-1} \zeta_r$ in the latter, which results from assuming the initial condition $M_{a0} = 0$ in deriving Eq. (12-36), whereas according to Eq. (12-34), $M_{a0} = 2M_s \sin \psi \tan(\theta_0/2)/\tau$. In any case, if $\delta_r^2 \ll 2\eta_r$ (low damping), then $\zeta_r \ll 1$, and $\sin^{-1} \zeta_r \approx 0$. Under this condition, the expressions for $M_a(t)$ in Eqs. (12-33) and (12-37) are equivalent. By equating the terms representing the decay time constant and the frequency of oscillation, we obtain the relations

$$\tau = \frac{2\eta_r}{\delta_r} \quad (12-40)$$

and

$$\Omega = \sqrt{\frac{1}{\eta_r} - \left(\frac{\delta_r}{2\eta_r}\right)^2} \quad (12-41)$$

Using Eqs. (12-40) and (12-41), the low damping condition $\delta_r^2 \ll 2\eta_r$ is equivalent to the condition $(\Omega\tau)^2 \gg 1$, which amounts to $[\lambda/(\gamma M_s)]^2 \ll 1$ according to the Landau-Lifshitz equation, and $\alpha^2 \ll 1$ according to the Gilbert equation (see Eqs. (11-36) and (11-37)).

Equating the expressions for τ , Eqs. (11-36) and (12-40), and for Ω , Eqs. (11-37) and (12-41), we obtain the following relations:

$$\eta_r = \begin{cases} \frac{1}{H^2 [\gamma^2 + (\lambda/M_s)^2]} & \text{(Landau-Lifshitz)} \\ \frac{1 + \alpha^2}{H^2 \gamma^2} & \text{(Gilbert)} \end{cases} \quad (12-42)$$

and

$$\delta_r = \begin{cases} \frac{2(\lambda/M_s)}{H [\gamma^2 + (\lambda/M_s)^2]} & \text{(Landau-Lifshitz)} \\ \frac{2\alpha}{H\gamma} & \text{(Gilbert)} \end{cases} \quad (12-43)$$

Equating the initial and final values of M_a in Eqs. (12-32) and (12-37), we obtain the relations

$$M_{a0} = M_s \cos(\theta_0 + \psi) \quad (12-44)$$

and

$$M_s \cos \psi = M_{a0} + \chi_r H_{ap} \quad (12-45)$$

Substituting Eq. (12-44) and the trigonometric relation $H_{ap} = H_i \sin \theta_0 / \sin \psi$ into Eq. (12-45), we obtain

$$\chi_r = \frac{M_s}{2H_i} \left[\tan \psi + \tan \left(\frac{\theta_0}{2} \right) \right] \sin 2\psi \quad (12-46)$$

and with $\psi \gg \theta_0/2$, Eq. (12-46) reduces to

$$\chi_r \approx \frac{M_s}{H_i} \sin^2 \psi \quad (12-47)$$

We have seen that a second-order differential equation, Eq. (12-35), may be used to describe the component of elastic rotation of magnetization of a single crystallite (or a domain) along the applied magnetic field that causes this rotation. Applied to every j th crystallite (of volume v_j) in a polycrystalline specimen, Eq. (12-35) then describes the overall M_a of the specimen, provided that χ_r represents an average value, that is

$$\chi_r = \frac{1}{\sum_j v_j} \sum_j \chi_{rj} v_j \approx \frac{M_s}{\sum_j v_j} \sum_j \frac{v_j \sin^2 \psi_j}{H_{ij}} \quad (12-48)$$

For simplicity, suppose that the leg is thin enough to assume uniform M and applied H across it. Substituting $H_{ap} = F/l$ and $M = \phi/(\mu_0 A)$ into Eq. (12-35), we finally obtain a model for the component of $\dot{\phi}$ due to elastic rotation of magnetization. Thus,

$$\phi_{\epsilon r} + \delta_r \dot{\phi}_{\epsilon r} + \eta_r \ddot{\phi}_{\epsilon r} = \epsilon_r F \quad (12-49)$$

where

$$\phi_{\epsilon r} = \mu_0 A (M_a - M_{a0}) \quad (12-50)$$

is the elastic rotational change in the component of flux along the applied field, and

$$\epsilon_r = \chi_r \mu_0 \frac{A}{l} \quad (12-51)$$

The term $\eta_r \ddot{\phi}_{\epsilon r}$ in Eq. (12-49) is negligible if $T_r \gg 2\eta_r/\delta_r$ (for example, $T_r \gtrsim 10\eta_r/\delta_r$), where T_r is the rise time of the F pulse. Under this condition, Eq. (12-49) reduces to

$$\phi_{\epsilon r} + \delta_r \dot{\phi}_{\epsilon r} \approx \epsilon_r F \quad (12-52)$$

If, in addition, $T_r \gg \delta_r$, then Eq. (12-49) reduces further to

$$\phi_{\epsilon r} \approx \epsilon_r F \quad (12-53)$$

A Model for $\dot{\phi}_\epsilon(t)$ Due to Domain-Wall Motion. Consider a 180° Bloch wall lying in the x - y plane and suppose that the wall undergoes a small elastic displacement in the z direction as a result of an applied field H_{ap} . A schematic variation of the gradient of the total energy E with wall-position z is illustrated in Fig. 11-16. Per unit wall area, the applied force $2\mu_0 M_s H_{ap}$ is opposed by three forces (cf. Kittel and Galt (1956)): by $dE/dz \approx kz$, where k is the *stiffness* coefficient of a restoring force; by $\beta\dot{z}$, where β is the *viscous-damping* coefficient; and by $m_w \ddot{z}$, where m_w is the *effective mass* of the wall. The equation of motion of a small wall displacement from equilibrium is, then,

$$kz + \beta\dot{z} + m_w \ddot{z} = 2\mu_0 M_s H_{ap} \quad (12-54)$$

Assuming that Eq. (12-54) describes the motion of a typical wall whose properties represent the average properties of all the walls moving elastically, we may replace z by $bM_{\epsilon w}$, where b is a proportionality constant and $M_{\epsilon w}$ is the change in M due to the elastic wall motion. Denoting the wall-motion susceptibility by χ_w , Eq. (12-54) then becomes

$$M_{\epsilon w} + \delta_w \dot{M}_{\epsilon w} + \eta_w \ddot{M}_{\epsilon w} = \chi_w H_{ap} \quad (12-55)$$

where

$$\delta_w = \frac{\beta}{k} \quad (12-56)$$

$$\eta_w = \frac{m_w}{k} \quad (12-57)$$

and

$$\chi_w = \frac{2\mu_0 M_s}{kb} \quad (12-58)$$

Multiplying Eq. (12-55) by $\mu_0 A$ and replacing H_{ap} by F/l , we obtain a model for $\dot{\phi}$ due to elastic wall motion, which, like the $\dot{\phi}_{\epsilon r}$ model, is also a second-order differential equation:

$$\phi_{\epsilon w} + \delta_w \dot{\phi}_{\epsilon w} + \eta_w \ddot{\phi}_{\epsilon w} = \epsilon_w F \quad (12-59)$$

where

$$\epsilon_w = \frac{X_w \mu_0 A}{l} \quad (12-60)$$

The term $\eta_w \ddot{\phi}_{\epsilon w}$ in Eq. (12-59) is negligible if $T_r \gg 2\eta_w/\delta_w$ (for example, $T_r \gtrsim 10\eta_w/\delta_w$). Under this condition, Eq. (12-59) reduces to

$$\phi_{\epsilon w} + \delta_w \dot{\phi}_{\epsilon w} \approx \epsilon_w F \quad (12-61)$$

Furthermore, if also $T_r \gg \delta_w$, then Eq. (12-59) reduces further to

$$\phi_{\epsilon w} \approx \epsilon_w F \quad (12-62)$$

Total $\dot{\phi}_\epsilon(t)$. The total elastic $\dot{\phi}(t)$ is expressed in Eq. (12-29) as the sum of the rotational component $\dot{\phi}_{\epsilon r}(t)$ (Eq. (12-49)) and the wall-motion component $\dot{\phi}_{\epsilon w}(t)$ (Eq. (12-59)). Theoretical waveforms of $\dot{\phi}_{\epsilon r}(t)$ and $\dot{\phi}_{\epsilon w}(t)$, in response to an applied mmf pulse of amplitude F_D and a short rise time T_r , are drawn in Fig. 12-11. On the basis of experimental observation to be described later, it is assumed that $\dot{\phi}_{\epsilon r}(t)$ is underdamped, whereas $\dot{\phi}_{\epsilon w}(t)$ is close to critically damped (slightly underdamped or slightly overdamped). Thus, following Eqs. (12-49) and (12-52), the $\dot{\phi}_{\epsilon r}(t)$ component is oscillatory if T_r is not large compared with $2\eta_r/\delta_r$.

It was found experimentally that the parameters δ , η , and ϵ corresponding to either $\dot{\phi}_{\epsilon w}$ or $\dot{\phi}_{\epsilon r}$ may depend on T_r . If $T_r \gg \max(\eta_w/\delta_w; \eta_r/\delta_r)$ and $\delta_w \approx \delta_r \equiv \delta$, then Eqs. (12-52) and (12-61) may be combined to describe the overall $\dot{\phi}_\epsilon$ by

$$\phi_\epsilon + \delta \dot{\phi}_\epsilon \approx \epsilon F \quad (12-63)$$

where

$$\epsilon = \epsilon_r + \epsilon_w \quad (12-64)$$

Furthermore, if also $T_r \gg \delta$, then Eq. (12-63) may be simplified to

$$\phi_\epsilon \approx \epsilon F \quad (12-65)$$

In other words, if $F(t)$ is relatively slow-rising, then the elastic $\dot{\phi}$ is simply

$$\dot{\phi}_\epsilon = \epsilon \dot{F} \quad (12-66)$$

as noted in the introduction to this section.

For example, in a pulse experiment to be described later, it was found that $\delta_r = 0.28$ nsec, $\eta_r = 0.08$ nsec², $\delta_w = 4$ nsec, and $\eta_w = 2$ nsec² for a magnesium-manganese-zinc ferrite core. For this core, then, if $T_r \gtrsim 3$ nsec, then Eq. (12-49) may be approximated by Eq. (12-52), and if $T_r \gtrsim 5$ nsec, then Eq. (12-59) may be approximated by Eq. (12-61). It was further found that δ_r and δ_w increase with T_r ; for example, for $T_r = 65$ nsec, $\delta_r \approx \delta_w \approx 6$ nsec; hence, if $T_r \gtrsim 60$ nsec, then $\dot{\phi}_\epsilon \approx \epsilon \dot{F}$ (Eq. (12-66)). Determination of ϵ is discussed below.

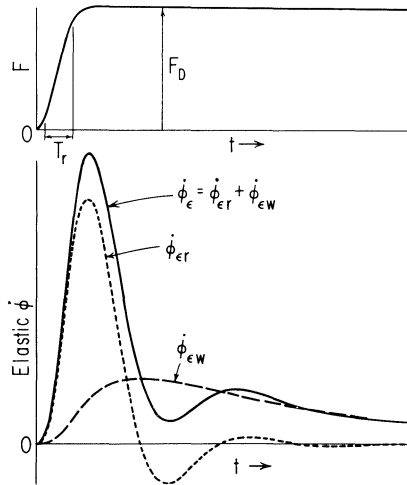


Fig. 12-11. Postulated waveforms of $\dot{\phi}_\epsilon(t)$ and its components $\dot{\phi}_{\epsilon r}(t)$ and $\dot{\phi}_{\epsilon w}(t)$, in response to applied $F(t)$ of amplitude F_D and short rise time T_r (less than a nanosecond).

Let the top and bottom portions of the major static $\phi(F)$ loop, where $|\phi| > \phi_r$, be referred to as "saturation regions," in abbreviation of "regions of approach to saturation." Any flux switching occurring in a saturation region is elastic, and if the rise of $F(t)$ is slow enough to justify the use of Eq. (12-65), the ϕ_ϵ versus F traces the static $\phi(F)$ curve in this region. Recalling that initially $\phi_\epsilon = 0$, then ϕ_ϵ versus F amounts to the *change* in ϕ_d versus F (Eq.

(12-24(a)). If the change in F (around a bias value) is not excessive, then the switching is confined to a limited $\phi_d^{(F)}$ region that may be approximated by a straight-line segment, i.e., with ϵ assumed to be constant and equal to $d\phi_d/dF$. Extending Eq. (12-24a) to the positive saturation region by using the antisymmetry property $\phi_d^{(F)} = -\phi_d^{(-F)}$, adding the air-flux term (Eq. (12-28)), and differentiating with respect to F , we obtain the following relation for $\epsilon^{(F)}$, which is valid for either positive or negative saturation

$$\epsilon = \frac{\phi_s - \phi_r}{(l_o - l_i)H_a} \left[|F| \left(\frac{1}{|F| + H_a l_o} - \frac{1}{|F| + H_a l_i} \right) + \ln \left(\frac{|F| + H_a l_o}{|F| + H_a l_i} \right) \right] + \frac{\mu_0 A}{l_o - l_i} \ln \left(\frac{l_o}{l_i} \right) \quad (12-67)$$

If the switching takes place around $F = 0$, then $\epsilon \equiv \epsilon(0)$ and Eq. (12-67) reduces to

$$\epsilon(0) = \left(\frac{\phi_s - \phi_r}{H_a} + \mu_0 A \right) \frac{1}{l_o - l_i} \ln \left(\frac{l_o}{l_i} \right) \approx \frac{\phi_s - \phi_r}{H_a (l_o - l_i)} \ln \left(\frac{l_o}{l_i} \right) \quad (12-68)$$

On the basis of Eqs. (12-67) and (12-68), symmetrical plots of ϵ versus F in negative and positive saturation regions are sketched in Fig. 12-12.

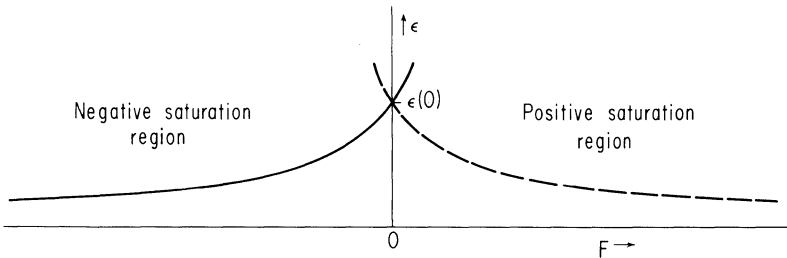


Fig. 12-12. ϵ vs. F in saturation regions.

Switching from a Partially Set State. Equations (12-67) and (12-68) are valid along the saturation regions, where $|\phi| > \phi_r$ and

where $|F|$ may be quite large. Now, if the initial flux ϕ_0 is between $-\phi_r$ and ϕ_r , then the core is in a *partially set*, or "soft," state. Assuming that the duration of $F(t)$ is not too short, no pure elastic switching can occur from this state unless $|F|$ is below the corresponding static F threshold. We shall, therefore, confine our discussion to elastic switching due to small changes in $|F|$ around the zero value, i.e., examine only $\epsilon(0)$. Following the relation $\epsilon = \epsilon_r + \epsilon_w$ (Eq. (12-64)), $\epsilon(0)$ has two components, $\epsilon_r(0)$ due to rotation of magnetization and $\epsilon_w(0)$ due to domain-wall motion. Assuming that the magnetization vectors that have been involved in changing ϕ from $-\phi_r$ to ϕ_0 have switched by 180° , the value of $\epsilon_r(0)$ may be considered independent of ϕ_0 because the small angle of rotation (due to the applied torque) is essentially the same for parallel and antiparallel magnetization vectors. In contrast, $\epsilon_w(0)$ depends very highly on the total domain-wall area ΣA_w . Since ΣA_w varies with ϕ_0 and since the same ϕ_0 value may correspond to different values of ΣA_w , the function $\epsilon_w(0)$ versus ϕ_0 is not unique. It is said to be *history dependent* in the sense that the value of $\epsilon_w(0)$ depends on how the flux state ϕ_0 was obtained. For a given value of ϕ_0 , the faster the previous switching, the larger the number of domains that have expanded inelastically and the larger is ΣA_w ; hence, the larger is $\epsilon_w(0)$. Therefore, $\epsilon(0)$ depends on both the initial ϕ and the flux-switching history in the manner illustrated schematically in Fig. 12-13. Such a behavior has been observed experimentally by McKay (1959).

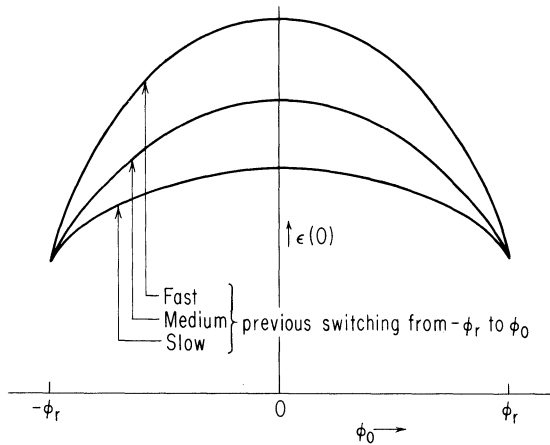


Fig. 12-13. Effects of ϕ_0 and previous switching on elastic-switching coefficient $\epsilon(0)$.

Fast-Switching Experiments. In order to examine the validity of the models for $\dot{\phi}_{er}(t)$ and $\dot{\phi}_{ew}(t)$, Eqs. (12-49) and (12-59), elastic-switching experiments using fast rising $F(t)$ pulses were performed on a thin toroidal polycrystalline ferrite core. In Table 12-1 are given the composition, the dimensions, the static $\phi(F)$ parameters, the elastic switching parameters, and the inelastic switching parameters (to be defined in Sec. 12-5) of this core. Results of elastic and inelastic flux-switching experiments performed on this core will be referred to several times in the remainder of this chapter.

Table 12-1 Parameters at $T = 30^\circ\text{C}$ of a Thin Toroidal Polycrystalline Ferrite Core Used in Several Flux-Switching Experiments

Nominal composition:	$[\text{Mg}_{0.32}\text{Zn}_{0.10}\text{Mn}_{0.58}]^{++}[\text{Mn}_{0.52}\text{Fe}_{1.48}]^{+++}\text{O}_4$
Dimensions:	$r_i = 3.53 \text{ mm}; r_o = 3.75 \text{ mm}; r_o/r_i = 1.06;$ $h = 0.69 \text{ mm}; w = 0.22 \text{ mm}; A = 0.149 \text{ mm}^2.$
Static $\phi(F)$ parameters:	$\phi_r = 3.45 \text{ Mx}; \phi_s = 3.73 \text{ Mx}; H_a = 950 \text{ At/m};$ $H_q = 35.0 \text{ At/m}; H_n = 30.0 \text{ At/m}; F_c = 0.90 \text{ At}.$
$\dot{\phi}_e$ parameters:	$\delta_r = 0.28 \text{ ns}; \eta_r = 0.08 \text{ (ns)}^2;$ $\epsilon_r \approx 0.14(1 - 0.005 F_D) \cdot 10^{-9} \text{ Ht}^{-2};$ $\delta_w = 4.0 \text{ ns}; \eta_w = 2.0 \text{ (ns)}^2;$ $\epsilon_w \approx 0.266(1 - 0.008 F_D) \cdot 10^{-9} \text{ Ht}^{-2}.$
$\dot{\phi}_{id}$ parameters:	$F_{id}^{\text{max}} = 0.55 \text{ At}; \nu_{id} = 1.33; \lambda_{id} = 0.013 \Omega t^{-2.33} \text{ A}^{-0.33};$ $C_{id} = 0.1 \text{ At-}\mu\text{s}.$
$\dot{\phi}_{im}$ parameters:	$F_d^{\text{min}} = 0.78 \text{ At}; \nu' = 2.5; \lambda' = 0.124 \Omega t^{-3.5} \text{ A}^{-1.5};$ $F_0'' = 0.92 \text{ At}; \nu = 1.33; \lambda = 0.069 \Omega t^{-2.33} \text{ A}^{-0.33};$ $F_0 = 1.45 \text{ At}; \rho_p = 0.113 \Omega t^{-2};$ $F_B' = 1.08 \text{ At}; F_B = 3.12 \text{ At}.$

Note:

Mx—maxwell	μs —microsecond
t—turn	H—henry
A—ampere	Ω —ohm
ns—nanosecond	

The core was mounted in a section of a 50- Ω coaxial transmission line, as shown in Fig. 12-4(b). Rectangular current pulses were generated by a mercury-relay pulser. The pulse amplitude I was varied in five steps from 0.9 to 40 amperes, while the 10%-90% rise time T_r remained constant at 0.4 nanosecond. The current pulses switched the core elastically from $\phi = \phi_r$ further into the

positive saturation region and back (sometimes referred to as "shuttle" switching). The resulting $\dot{\phi}_\epsilon(t)$ was sensed by a single-turn winding of a short fine wire (1.1 cm of AWG No. 48), chosen to minimize the winding capacitance. The waveforms of the drive current and the positive portion of $\dot{\phi}_\epsilon(t)$ were photographed on a sampling oscilloscope with a 0.4 nanosecond response time. Included in the $\dot{\phi}_\epsilon(t)$ waveform was a component due to air flux

$$\dot{\phi}_{\text{air}}(t) = \frac{\mu_0 A_{sw} \dot{F}}{l} \quad (12-69)$$

where A_{sw} is the projection of the sense-winding area normal to the applied circumferential field $H = F/l$. The value of $\mu_0 A_{sw}/l$ was determined experimentally from the peak values of the $\dot{\phi}_{\text{air}}(t)$ and $\dot{F}(t)$ waveforms observed with the core removed.

The $\dot{\phi}_\epsilon$ parameters in Table 12-1 were determined by fitting the computed sum $\dot{\phi}_{\epsilon_r}(t) + \dot{\phi}_{\epsilon_w}(t) + \dot{\phi}_{\text{air}}(t)$ with the observed $\dot{\phi}_\epsilon(t)$ for all five values of drive. As may be seen in the table, values of ϵ_r and ϵ_w were found to decrease as the amplitude F_D of the drive mmf increased. (The nonlinear relation of ϵ versus F in Fig. 12-12 is approximated here by a straight line.)

Two examples of experimental and computed $F(t)$ and $\dot{\phi}_\epsilon(t)$ waveforms are compared in Fig. 12-14 for the extreme F_D values of 0.9 and 40.0 ampere-turns. The oscilloscope response time was accounted for by assuming the computed $F(t)$ to rise earlier than

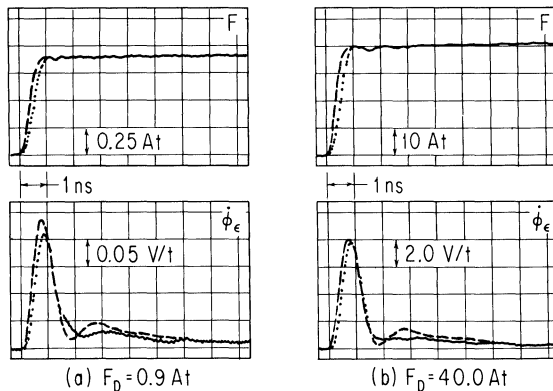


Fig. 12-14. Experimental (dotted and solid line) and computed (dashed line) $F(t)$ and $\dot{\phi}_\epsilon(t)$ waveforms of a thin ferrite core (Table 12-1) using $F(t)$ with $T_r = 0.4 \text{ ns}$ and different values of amplitude F_D (Nitzan and Hesterman, 1967).

the experimental $F(t)$ according to the relation

$$T_{r,obs} \approx \sqrt{T_r^2 + T_{r,osc}^2} \tag{12-70}$$

where $T_{r,obs}$ is the observed T_r , and $T_{r,osc}$ is the response time of the oscilloscope. From Fig. 12-14, it is found that $T_{r,obs} \approx 0.56$ nanosecond for both values of F_D ; the same value of $T_{r,obs}$ was found for all intermediate values of F_D . Since $T_{r,osc} = 0.4$ nanosecond, then $T_r \approx 0.4$ nanosecond for all values of F_D . As expected, the experimental $\dot{\phi}_\epsilon(t)$ waveforms lag behind the computed waveforms due to the oscilloscope response time. For the same reason, the peaks of the computed $\dot{\phi}_\epsilon(t)$ waveforms are found to be higher than the observed $\dot{\phi}_\epsilon$ peaks (they agree with $\dot{\phi}_\epsilon$ peaks observed on a much faster sampling oscilloscope, i.e., with $T_{r,osc} = 0.09$ nanosecond).

In another experiment, when a permanent-magnet field of about $96 \cdot 10^3$ amperes/meter was superimposed transversely to the applied circumferential field, the decaying $\dot{\phi}_\epsilon(t)$ tail disappeared and the initial $\dot{\phi}_\epsilon(t)$ spike became narrower, as shown in Fig. 12-15. The demagnetizing field was roughly $56 \cdot 10^3$ amperes/meter; hence, the net field was about $40 \cdot 10^3$ amperes/meter. A magnetic field of such magnitude is high enough to annihilate most of the domain walls and to increase the net bias field appreciably. The disappearance of the decaying $\dot{\phi}_\epsilon(t)$ tail confirms the hypothesis made in Fig. 12-11 that the wall-motion component $\dot{\phi}_{ew}(t)$ is characterized by appreciably slower switching than the rotational component $\dot{\phi}_{er}(t)$. The narrowing of the $\dot{\phi}_\epsilon(t)$ spike (which may be identified with $\dot{\phi}_{er}(t)$) agrees with Eqs. (11-37) and (12-34) in which Ω (the angular velocity of oscillation) becomes higher as H is increased. A further increase in the transverse field caused $\dot{\phi}_{er}(t)$ to become still narrower and lower in amplitude. The latter effect is explained by the decrease in θ_0 (Eq. (12-34)), which is caused by the increase in the total quiescent field while leaving H_{ap} unchanged.

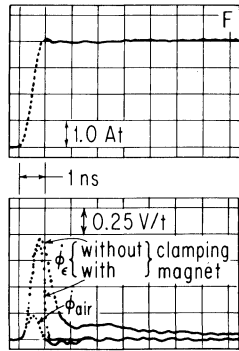


Fig. 12-15. Superposition of experimental waveforms of $\dot{\phi}_\epsilon(t)$ of a thin ferrite core (Table 12-1) without a magnet, $\dot{\phi}_\epsilon(t)$ with a magnet, and $\dot{\phi}_{air}(t)$, in response to a step $F(t)$ of $T_r = 0.4$ ns and amplitude $F_D = 4.0$ At (Nitzan and Hesterman, 1967).

The results of Figs. 12-14 and 12-15 verify that $\dot{\phi}_\epsilon(t) = \dot{\phi}_{er}(t) + \dot{\phi}_{ew}(t)$ (Eq. (12-29)), and that the initial $\dot{\phi}_\epsilon(t)$ spike is

primarily $\dot{\phi}_{\epsilon r}(t)$ and the decaying $\dot{\phi}_{\epsilon}(t)$ tail is primarily $\dot{\phi}_{\epsilon w}(t)$. This conclusion agrees also with the fact that switching by rotation of magnetization (where spins rotate in unison) is inherently faster than switching by domain-wall motion (where spins rotate sequentially). Further support for this conclusion can be derived from the following: The $\dot{\phi}_{\epsilon r}$ component is underdamped since, following Eq. (12-38), $\zeta_r = \frac{1}{2}\delta_r\eta_r^{-\frac{1}{2}} = 0.495 < 1$, and from Eq. (12-41), $\Omega/(2\pi) = \left(\eta_r^{-1} - \frac{1}{4}\delta_r^2\eta_r^{-2}\right)^{\frac{1}{2}}/(2\pi) = 487 \text{ Mc/s}$. For switching elastically further toward saturation, the $\dot{\phi}_{\epsilon w}$ component is overdamped since $\omega = \frac{1}{2}\delta_w\eta_w^{-\frac{1}{2}} = 1.414$. These results are consistent with *magnetic spectra* (plots of the real and the imaginary components of the complex permeability $\mu = \mu' - j\mu''$ versus frequency) of polycrystalline ferrites, which exhibit resonance in the microwave region but may or may not exhibit resonance in the radio-frequency region (see Rado et al. (1950); Smit and Wijn (1959); Rado et al. (1956); Harrison et al. (1958)). The resonance in the microwave region is due to rotation of magnetization. The sources of resonance in the radio-frequency region are not completely understood, and may depend on the material composition. Rado (1950; 1956) showed that the radio-frequency dispersion (the plot of $(\mu' - 1)$ versus frequency) and the static initial permeability of magnesium ferrites are due to domain-wall displacements. A similar conclusion was drawn by Harrison et al. (1958) for manganese ferrites.

On the basis of these switching experiments, we may determine approximate values for the viscous damping α and the anisotropy constant K_1 . Following Eqs. (12-42) and (12-43)

$$\alpha = \frac{\delta_r}{\sqrt{4\eta_r - \delta_r^2}} \quad (12-71)$$

and

$$H = \frac{2}{\gamma\sqrt{4\eta_r - \delta_r^2}} \quad (12-72)$$

Substituting $\delta_r = 0.28$ nanosecond and $\eta_r = 0.08$ nanosecond², we find that $\alpha = 0.57$ and, since $H_i \gg H_{ap}$ and $\gamma = 2.21 \cdot 10^5$ meters/ampere-second, that $H_i \approx 18.5 \cdot 10^3$ amperes/meter. From Eq. (11-27b),

the anisotropy constant K_1 of materials whose easy axes are body diagonals, such as ferrites, is given by

$$K_1 = -\frac{3}{4}\mu_0 M_s H_k \quad (12-73)$$

For this magnesium-manganese-zinc ferrite core, $\mu_0 M_s = 0.262$ weber/meter², and if $H_{dm} \ll H_k$, then $H_k \approx H_i$ and so $K_1 \approx -3.6 \cdot 10^3$ joules/meter³. This value lies between values of K_1 for magnesium and manganese polycrystalline ferrites obtained by Rado et al. (1956) and Harrison et al. (1958), respectively.

12-5 Inelastic $\dot{\phi}(t)$ Models

Introduction. In most applications of square-loop magnetic cores, it is the inelastic flux switching that plays the most important role. Unfortunately, the physical mechanisms involved in inelastic flux switching are much more complex than those in elastic flux switching. It is thus of no surprise that so many different models for inelastic switching of magnetization have been proposed in the past. Most of these models may be described generally by the differential equation

$$\dot{M} = f(M)[H_{ap}(t) - H_0] \quad (12-74)$$

where H_0 is the *dynamic threshold field* (to be discussed later), $H_{ap}(t)$ is the magnitude of the applied field, M is the magnetization component along H_{ap} , and $f(M)$ is some function of the instantaneous value of M . Let us first review some of these models.

One may distinguish between physical models, which are derived from physical reasoning, and semiempirical models, for which $f(M)$ and H_0 are determined experimentally. A physical model is often derived primarily in order to verify a theory of flux-switching mechanism, whereas a semiempirical model is obtained for application in magnetic circuit analysis when the physical models are either too complex or inadequate.

Among the physical models, we may distinguish between models that are based on domain-wall motion (Menyuk and Goodenough (1955); Conger and Essig (1957); Haynes (1958); Lindsey (1959); Knowles (1960); Hilberg (1964)) and models that are based on rotation of magnetization (Coleman (1957); Gyorgy (1963)). There is little doubt that flux switching occurs mainly by domain-wall motion

at low fields and mainly by coherent rotation of magnetization at high fields (see Gyorgy (1963)). It was proposed by Gyorgy (1958) that at intermediate fields, flux switching occurs by incoherent rotation in such a way that, except near the core surface, the demagnetizing fields effectively cancel due to formation of closely spaced surface poles of alternate polarity.

For the switching models based on domain-wall motion, various probability-distribution functions of occurrence of nucleation centers have been assumed. Different domain configurations during switching were postulated, such as expanding and colliding ellipsoidal (Haynes (1958)) or cylindrical (Lindsey (1959)) domains, and domains with constant wall area (Knowles (1960)). Although these physical models shed light on the mechanism of flux switching, their parameters have to be measured rather than calculated from more basic properties. This results from the difficulty in describing the details of the magnetic properties of materials, which are highly sensitive to inhomogeneities, such as impurities, strains, voids, and lattice imperfections.

The semiempirical models may be classified according to the form of $f(M)$, H_0 , and the effect of core thickness. Let us examine each of these features separately.

According to several semiempirical models, such as the ones proposed by Chen and Papoulis (1958), Betts and Bishop (1961), Gilli and Meo (1963), and Ching and Stram (1963), $f(M)$ or its equivalent is determined point by point from experimental data. Neeteson (1964) and Tancrell and McMahon (1960) assumed that $f(M)$ is semicircular, i.e., proportional to $[1 - (M/M_s)^2]^{1/2}$; hence, Eq. (12-74) results in a half-sinusoidal $\dot{M}(t)$ for a step $H_{ap}(t)$. A parabolic $f(M)$ that is proportional to $[1 - (M/M_s)^2]$ was assumed in the semiempirical model applied by Cushman and Park (1960). This $f(M)$ function was modified by Holtwijk (1964) to the form $\{1 - [(M + \Delta M)/(M_s + \Delta M)]^2\}$ where $\Delta M \approx 0.05 M_s$. If $f(M)$ in Eq. (12-74) is parabolic, then a step $H_{ap}(t)$ results in \dot{M} which is a sech^2 function of time. Hesterman (1961) made a comparison between experimental $\dot{\phi}(t)$ of a common soft-ferrite material and $\dot{\phi}(t)$ computed from the various models that can be expressed analytically (including the physical models), and concluded that the best agreement (although not by far) is generally obtained if $f(M)$ is parabolic, and that the agreement for the semicircular $f(M)$ is relatively poor. (However, a few soft ferrite materials do not exhibit a parabolic $f(M)$ behavior. See, for example, Nitzan and Hesterman (1964).) It is interesting that $f(M)$ is also parabolic in the physical models derived by Coleman (1957) and Gyorgy (1958) on the basis

of rotation of magnetization. The good agreement between experimental $\dot{M}(t)$ and the calculated $\dot{M}(t)$ based on a parabolic $f(M)$ offers some support for the rotational models. However, a similar good agreement is obtained in the region of low H_{ap} , where the switching process occurs by domain-wall motion.

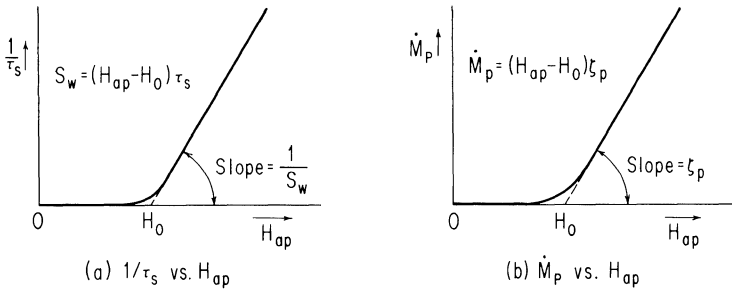


Fig. 12-16. Inverse switching time and peak inelastic \dot{M} vs. applied H field.

Typical plots of two types of measured data from step- H_{ap} switching experiments are shown in Fig. 12-16: $1/\tau_s$ versus H_{ap} , where τ_s is the time of switching essentially from $-M_r$ to M_r , and \dot{M}_p versus H_{ap} , where \dot{M}_p is the peak value of the inelastic $\dot{M}(t)$. (To be exact, τ_s is commonly defined as the time between the points at which $\dot{M} = 0.1 \dot{M}_p$.) Both the $1/\tau_s$ versus H_{ap} and \dot{M}_p versus H_{ap} plots are usually characterized by linear portions whose slopes are $1/S_w$ and ζ_p , respectively, where S_w is called the *switching coefficient*. Most models assume a constant dynamic H threshold, regardless of H_{ap} , whose value H_0 may be determined in Fig. 12-16 by extrapolating to the H_{ap} axis the linear portion of either $1/\tau_s$ versus H_{ap} or \dot{M}_p versus H_{ap} . The extrapolated values of H_0 obtained from the two sets of data are not necessarily the same, although they are likely to be close to each other. By assuming a constant H_0 , the nonlinear region of either $1/\tau_s$ versus H_{ap} or \dot{M}_p versus H_{ap} is ignored. The error introduced by this assumption may be quite significant because many magnetic circuits operate in this nonlinear region, which, for some materials, may extend to H_{ap} values three to ten times the coercive force. (Conger and Essig (1957) proposed that the threshold field for domain-wall motion in thin films is distributed randomly over the range between the coercive force and the anisotropy field. As a result, the number of walls, in addition to the wall velocity, increases with H_{ap} , thus causing the nonlinearity of $1/\tau_s$ versus H_{ap} .)

So far we have discussed flux switching in terms of M and H_{ap} rather than ϕ and F . This is justified in the case of a thin toroid for which $F = H_{\text{ap}} l$ and $\phi = \mu_0 MA$. For a thick core, $M(t)$ varies with the radius r , and $\phi(t)$ should be determined by integration of $\mu_0 M(r, t) h dr$ from $r = r_i$ to $r = r_o$. For the models referred to so far, such an integration cannot be done analytically in a closed form, but can be approximated by Taylor series or performed numerically. The latter method was used by Tancrell and McMahon (1960), Hesterman (1961), and Ching and Stram (1963).

On the basis of experimental observation to be described next, we shall propose semiempirical models for the components of inelastic flux switching.

Observed Flux Switching. Typical results from a flux-switching experiment using a thin toroidal core (Fig. 12-4) were shown in Fig. 12-5. Waveforms of the setting F pulse and the resulting $\dot{\phi}(t)$, as well as the variation of ϕ versus F during the switching time, are redrawn in Fig. 12-17. The amplitude F is shown larger than the coercive mmf F_c , but not large enough to fully switch ϕ to positive saturation.

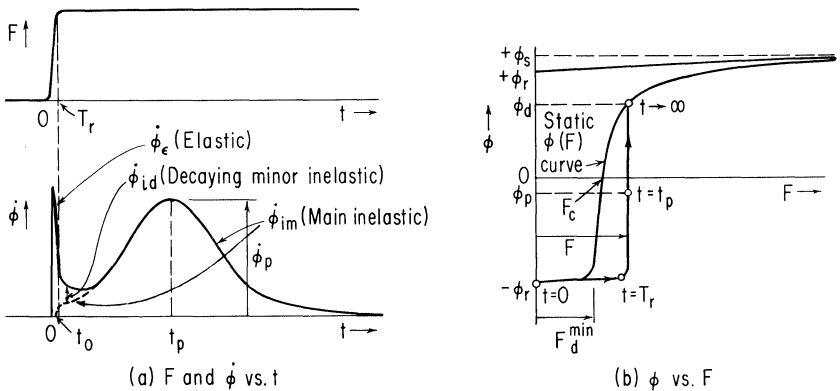


Fig. 12-17. Step- F flux switching.

The rotational and wall-motion components of $\dot{\phi}_\epsilon(t)$ were analyzed in detail in Sec. 12-4. We shall now show that $\dot{\phi}_i(t)$, the inelastic $\dot{\phi}(t)$, may also be analyzed in terms of two components: a decaying inelastic $\dot{\phi}(t)$ component, $\dot{\phi}_{id}(t)$, due to minor wall displacements, and a bell-shaped main inelastic $\dot{\phi}(t)$ component, $\dot{\phi}_{im}(t)$, due to major wall displacements, which starts at $t = t_0$ and reaches its peak value

$\dot{\phi}_p$ at $t = t_p$. The main component is so termed because the corresponding flux change $\Delta\phi_{im} = \int_0^\infty \dot{\phi}_{im} dt$ is much larger than $\Delta\phi_{id} = \int_0^\infty \dot{\phi}_{id} dt$ due to $\dot{\phi}_{id}(t)$ —except for F values near F_d^{\min} .

Suppose now that the above flux-switching experiment is repeated with one modification: the step- F setting pulse is interrupted in the beginning of switching. This results in two F pulses of the same amplitude. A waveform of $F(t)$ with amplitude of $1.3 F_c$ and a typical waveform of the resulting $\dot{\phi}(t)$ for the thin ferrite core of Table 12-1 are shown in Fig. 12-18. Fast-switching elastic $\dot{\phi}(t)$ spikes are shown during the rise and fall of the first F pulse and during the rise of the second F pulse. But most important, note that during the first F pulse and in the beginning of the second F pulse, the overall inelastic component $\dot{\phi}_i(t)$ is decaying despite the rise of the main inelastic component $\dot{\phi}_{im}(t)$ (Fig. 12-17(a)). The difference between $\dot{\phi}_i(t)$ and $\dot{\phi}_{im}(t)$ is the decaying inelastic component $\dot{\phi}_{id}(t)$. This component may be attributed to inelastic domain-wall motions. It is inelastic because there is a net flux change due to the first F pulse, which cannot be accounted for by the small contribution of the $\dot{\phi}_{im}$ component only. It is due to domain-wall motions for the following two reasons: First, the relaxation time of $\dot{\phi}_{id}(t)$ is much longer than typical relaxation time for rotation of magnetization, which in this case is on the order of 5 nanoseconds (cf. Fig. 12-14). Second, $\dot{\phi}_i(t)$ that follows the positive $\dot{\phi}_\epsilon(t)$ spike of the second F pulse continues to decay smoothly from the same value at the end of the first F pulse; this is characteristic only of domain-wall motion.

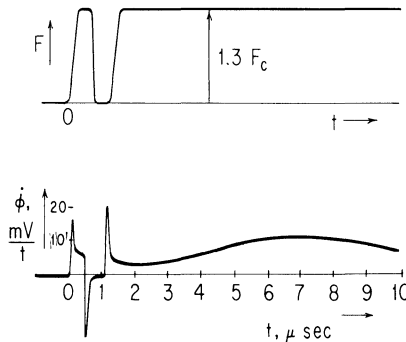


Fig. 12-18. Waveforms of interrupted $F(t)$ and $\dot{\phi}(t)$ of a thin toroidal ferrite core (Table 12-1)

Components of Inelastic $\dot{\phi}(t)$. The large difference in shape between the waveforms of $\dot{\phi}_{id}(t)$ and $\dot{\phi}_{im}(t)$ implies that different

mechanisms are involved in generating these inelastic $\dot{\phi}(t)$ components. The nature of these mechanisms is postulated as follows.

For simplicity, suppose that the core is thin enough to assume uniform M and H_{ap} across it; hence, $F = lH_{ap}$ and $\dot{\phi} = \mu_0 A\dot{M}$. Referring to Fig. 11-18, we have seen that the n inelastic wall displacements due to a step $H_{ap}(t)$ are divided into np minor displacements of essentially constant areas and $n(1-p)$ major displacements of varying areas, where $p \leq 1$. We now postulate that the minor wall displacements generate the $\dot{\phi}_{id}(t)$ component, whereas the $\dot{\phi}_{im}(t)$ component is generated by the major wall displacements. The waveform of each of these inelastic $\dot{\phi}(t)$ components depends on the average velocity, the expected number, the average area, and the travel time of the corresponding walls. The first two factors affect $\dot{\phi}_{id}(t)$ and $\dot{\phi}_{im}(t)$ in a similar fashion, whereas the third and fourth factors affect each $\dot{\phi}$ component differently. On the basis of these features, we shall next propose a model for each of these components.

A Model for Decaying Minor $\dot{\phi}_i(t)$. As a first approximation, assume that the average velocity of walls moving inelastically is proportional to the excess of the applied H over an average threshold \bar{H}_{th} . Denoting \bar{H}_{th} corresponding to minor wall displacements by H_{id} , then $\dot{\phi}_{id}$ is proportional to $(H_{ap} - H_{id})$. The magnitude of $\dot{\phi}_{id}$ also increases with the number np of the walls experiencing minor displacements. We have seen that n increases with H_{ap} and that p is essentially unity in the region $0 < H_{ap} \lesssim H_d^{min}$, but that p decreases gradually as H_{ap} increases beyond H_d^{min} . Consequently, the product np increases with H_{ap} until it reaches a peak, and then decreases. For the $\dot{\phi}_{id}(t)$ model proposed here, we shall assume that H_{ap} is below the value at which np reaches its peak, i.e., that np increases with H_{ap} . It has been found experimentally that, to a good approximation, the magnitude of $\dot{\phi}_{id}$ is proportional to $(H_{ap} - H_{id})^{\nu_{id}}$, where $\nu_{id} > 1$ (for example, $\nu_{id} \approx 1.5$). Since $\dot{\phi}_{id}$ is proportional to $(H_{ap} - H_{id})$ on the basis of wall velocity alone, the increase of np with H_{ap} may account for the extra factor $(H_{ap} - H_{id})^{\nu_{id} - 1}$.

Under the assumption that $\dot{\phi}_{id}(t)$ is generated by minor wall displacements, the corresponding average wall area is unlikely to change significantly during the switching time; hence, $\dot{\phi}_{id}(t)$ should be essentially rectangular if these displacements were identical. However, since the length of the minor wall displacement is a random variable and since the wall velocities are not necessarily the same, the termination times of these displacements

will vary randomly among the walls. When a step H_{ap} is applied, all np walls begin moving and generate $\dot{\phi}_{id}$; as one wall after another terminates its motion, $\dot{\phi}_{id}(t)$ decays in an exponential-like manner. The time constant τ_{id} associated with the $\dot{\phi}_{id}(t)$ decay is assumed to be inversely proportional to the average wall velocity; hence, $\tau_{id} = S_{id}/(H_{ap} - H_{id})$, where S_{id} is a parameter. Thus, $\dot{\phi}_{id}(t)$ generated by a step H_{ap} is proportional to

$$(H_{ap} - H_{id})^{\nu_{id}} \exp \left[-\frac{t(H_{ap} - H_{id})}{S_{id}} \right]$$

Suppose now that $H_{ap}(t)$ increases from zero to above H_{id} . Letting T_{id} be the time when H_{ap} reaches H_{id} ($\dot{\phi}_{id} = 0$ during $0 \leq t \leq T_{id}$) and replacing H_{ap} by F/l , then during $t \geq T_{id}$

$$\dot{\phi}_{id}(t) = \lambda_{id}(F - F_{id})^{\nu_{id}} \exp \left[-\frac{(t - T_{id})(F - F_{id})}{C_{id}} \right] \tag{12-75}$$

where λ_{id} is a constant of proportionality, $F_{id} = H_{id}l$, and $C_{id} = S_{id}l$.

To a good approximation, Eq. (12-75) is applicable regardless of the rise time T_r and the shape of $F(t)$. Examples of constant- F drives with relatively short and long rise times are sketched in Fig. 12-19. As F increases with time, the term $(F - F_{id})^{\nu_{id}}$ tends to increase $\dot{\phi}_{id}$, while the exponential terms tends to decrease $\dot{\phi}_{id}$; as a result, $\dot{\phi}_{id}(t)$ increases during $T_{id} \leq t \leq T_r$ from zero to a peak

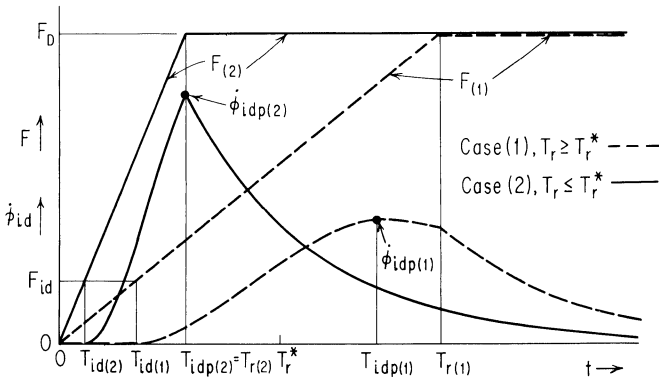


Fig. 12-19. Sketched waveforms of $\dot{\phi}_{id}(t)$ for two $F(t)$ drives of the same amplitude F_D and different rise time T_r .

value $\dot{\phi}_{idp}$ at $t = T_{idp}$, and then decreases. If the slope of $F(t)$ is low enough, then $T_{idp} < T_r$; otherwise, $T_{idp} = T_r$. The shorter the rise time, the higher $\dot{\phi}_{idp}$; in the limit, as $T_r \rightarrow 0$, $\dot{\phi}_{idp} \rightarrow \lambda_{id}(F - F_{id})^{\nu_{id}}$, whereas as $T_r \rightarrow \infty$, $\dot{\phi}_{idp} \rightarrow 0$.

In each of the examples in Fig. 12-19, $F(t)$ rises linearly from zero to a constant value F_D . The T_r value that just coincides with the peaking time (when $\dot{\phi}_{id}(t) = 0$) can be shown to be

$$T_r^* = \frac{C_{id}^{\nu_{id}} F_D}{2(F_D - F_{id})^2} \quad (12-76)$$

Two cases are considered: if $T_r \geq T_r^*$ (Case (1)), then $T_{idp} \leq T_r$ and

$$\dot{\phi}_{idp(1)} = \lambda_{id} \left[\frac{C_{id}^{\nu_{id}} F_D}{2eT_r} \right]^{\nu_{id}/2} \quad (12-77)$$

(where $e = 2.718 \dots$), but if $T_r \leq T_r^*$ (Case (2)), then $T_{idp} = T_r$ and $\dot{\phi}_{idp(2)}$ is obtained by substituting $t = T_r$ and $F = F_D$ into Eq. (12-75).

Although the values of F_{id} and C_{id} have been assumed to be constant, there are actually functional dependences of F_{id} on F and C_{id} on T_r . Recalling that $H_{id} = \bar{H}_{th}$, we see from the probability-density function $f(H_{th})$ in Fig. 11-18 that as the magnitude H_{ap} of a step $H_{ap}(t)$ increases from zero, H_{id} also increases from zero to an asymptotic value, denoted by H_{id}^{\max} , which is in the neighborhood of H_d^{\min} . Letting $F_{id}^{\max} = H_{id}^{\max} l$, a function that satisfies this condition as well as the condition $H_{id} \leq H_{ap}$ is, for example,

$$F_{id} = F_{id}^{\max} \tanh\left(\frac{F}{F_{id}^{\max}}\right) \quad (12-78)$$

Let us next examine the effect of T_r on C_{id} . If a constant- F drive is left for a long enough time (theoretically, infinite time), then the flux change $\Delta\phi_{id(\infty)} = \int_0^\infty \dot{\phi}_{id} dt$ increases with F_D but is independent of T_r . In order to obtain the dependence of $\Delta\phi_{id(\infty)}$ on F_D , we substitute Eq. (12-78) into Eq. (12-75) and let $T_{id} = T_r = 0$, that is, assume that $F(t) = F_D$ is a step function. We then find that

$$\Delta\phi_{id(\infty)} = C_{id} \lambda_{id} \left[F_D - F_{id}^{\max} \tanh\left(\frac{F_D}{F_{id}^{\max}}\right) \right]^{\nu_{id}-1} \quad (12-79)$$

Now, if T_r is considerably smaller than τ_{id} , then $\Delta\phi_{id(\infty)} \approx \dot{\phi}_{idp}\tau_{id}$, and since $\tau_{id} = C_{id}/(F_D - F_{id}')$, we obtain

$$C_{id} \approx \Delta\phi_{id(\infty)} \frac{F_D - F_{id}'}{\dot{\phi}_{idp}} \tag{12-80}$$

Hence, for a given F_D value, $\dot{\phi}_{idp}C_{id} \approx \text{constant}$, and since $\dot{\phi}_{idp}$ increases as T_r decreases, C_{id} must decrease as T_r decreases. According to Eq. (12-80), C_{id} depends also on F_D . However, the increase of $\dot{\phi}_{idp}$ with F_D is such that $\dot{\phi}_{idp}/(F_D - F_{id}')$ may be approximated by a constant for large F_D values. This is evident from the illustrative plots in Fig. 12-20 of computed $\dot{\phi}_{idp}$ versus F_D for different T_r values, using the thin ferrite core of Table 12-1.

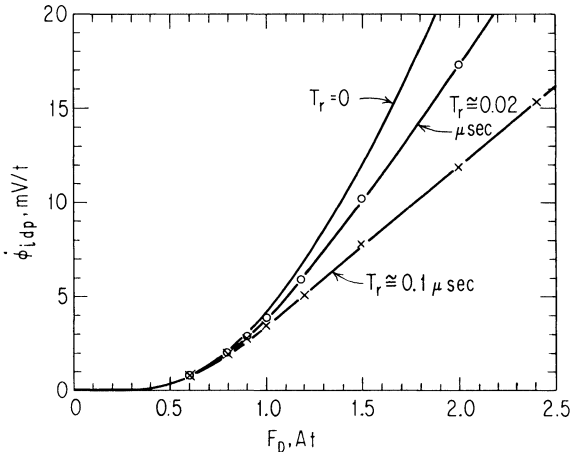


Fig. 12-20. Computed $\dot{\phi}_{idp}$ vs. F_D with T_r as a parameter for a thin ferrite core (Table 12-1). (Nitzan, 1966.)

(The $\dot{\phi}_{id}(t)$ component is significant in connection with the signal-to-noise ratio of a coincident-current memory. Consider two essentially identical cores, one in an undisturbed *one* state ($\phi \approx \phi_r$) and the other in an undisturbed *zero* state ($\phi \approx -\phi_r$). The difference between the $\dot{\phi}$ outputs of the two undisturbed cores, generated by a *partial-read* pulse of amplitude near F_d^{min} , is the so-called maximum *delta noise*. Since the difference in $\dot{\phi}_\epsilon(t)$ between the two cores is considerably smaller than $\dot{\phi}_{id}(t)$ of the core driven away from saturation, this delta noise is essentially $\dot{\phi}_{id}(t)$. Application of a *post-write disturb* pulse before the *partial-read* pulse

decreases the delta noise appreciably by causing minor inelastic wall displacements to new stable positions, e.g., from Point R to Point W in Fig. 11-16(a). The longer the duration of this pulse, the larger the number of completed minor inelastic wall displacements, and thus the smaller the following delta noise. Furthermore, previous *partial-read* and *partial-write* pulses also affect the delta noise by causing minor inelastic wall displacements in opposite directions. Since $\dot{\phi}_{id}(t)$ is due primarily to domain-wall motion, one could possibly describe delta noise by incorporating the switching history into Eq. (12-75).)

A Model for Main $\dot{\phi}_i(t)$. Referring to Fig. 11-18, the average threshold \bar{H}_{th} corresponding to major inelastic wall displacements increases from a value of H_d^{min} to an asymptotic value as H_{ap} increases above H_d^{min} . The corresponding number of walls, $n(1-p)$, increases with H_{ap} because n increases and p decreases as H_{ap} increases. Thus, as in the case of $\dot{\phi}_{id}(t)$, the major component $\dot{\phi}_{im}(t)$ is proportional to $(H_{ap} - \bar{H}_{th})^\nu$, where $\nu \geq 1$. However, unlike $\dot{\phi}_{id}(t)$, $\dot{\phi}_{im}(t)$ is affected appreciably by a change in the average domain-wall area versus time. According to Menyuk and Goodenough (1955), the domain-wall area increases in the early portion of switching, reaches a peak in the middle of switching (while domains collide with each other), and decreases with time toward the end of switching. The probability-density function of the domain switching time is more complex than in the case of $\dot{\phi}_{id}(t)$ because it depends on domain collisions. Haynes (1958) extended Goodenough's work by calculating a model for $\dot{\phi}_i(t)$ based on the assumption that nucleation centers (from where major wall displacements begin) are distributed randomly according to Poisson's distribution function. Independently, Lindsey (1959) calculated a model similar to that of Haynes, except that he assumed the domains to be cylindrical. Models of this type were treated in a general way by Hilberg (1964). Each of these models for $\dot{\phi}_i(t)$ yields a reasonably satisfactory agreement with experimental data. However, a parabolic $\dot{\phi}_{im}(\phi)$ model is preferred here simply because it offers better agreement with experimental data for many square-loop materials. According to this model, $\dot{\phi}_{im}$ is proportional to a parabolic function of ϕ , and reaches a peak in the middle of switching. Qualitatively, therefore, the parabolic model has the physical features hypothesized by Menyuk and Goodenough (1955).

Consider again the flux-switching experiment using a thin toroidal core (Figs. 12-4 and 12-5). Typical $\dot{\phi}(\phi)$ oscillograms for step- F switching of the thin ferrite core of Table 12-1 are

shown in Fig. 12-21 for amplitude values of 1.2 and 1.8 ampere turns. After approximately 15 percent of the total amount of switching is completed, $\dot{\phi}_\epsilon \approx 0$ and $\dot{\phi}_{id} \ll \dot{\phi}_{im}$; thus, $\dot{\phi}(\phi) \approx \dot{\phi}_{im}(\phi)$. In each case, the $\dot{\phi}_{im}(\phi)$ curve is extrapolated by a dashed line to the ϕ axis. The resulting overall $\dot{\phi}_{im}(\phi)$ curve is found to be very close to a parabola that intersects the ϕ axis at $-\phi_r$ and at $\phi_d(F)$, where $\phi_d(F)$ (the static $\phi(F)$ curve; see Fig. 12-17(b)) may be calculated using the model in Eqs. (12-24). Similar parabolic $\dot{\phi}_{im}(\phi)$ oscillograms are typically observed for all values of F , except for very low F values, for example, $F \lesssim F_c$. Consequently, if F is larger, say, than F_c , then $\dot{\phi}_{im}$ may be described by the differential equation

$$\dot{\phi}_{im} = \dot{\phi}_p(F) \left\{ 1 - \left[\frac{2\phi + \phi_r - \phi_d(F)}{\phi_r + \phi_d(F)} \right]^2 \right\} \tag{12-81}$$

where $\dot{\phi}_p(F)$ is the peak value of $\dot{\phi}_{im}$ (see Fig. 12-17(a)) for a given value of F .

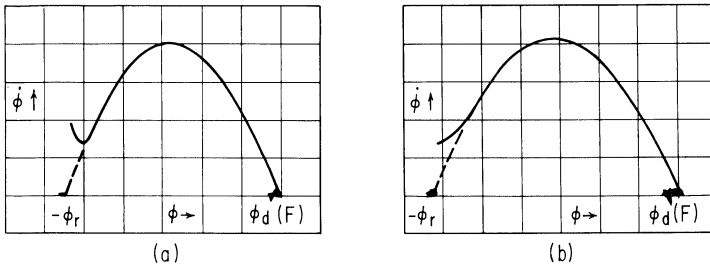


Fig. 12-21. $\dot{\phi}(\phi)$ oscillograms for step- F switching of a thin ferrite core (Table 12-1). ϕ scale = 1.04 Mx/major div. (a) $F = 1.2$ At; $\dot{\phi}$ scale = 3.3 mV/t/major div. (b) $F = 1.8$ At; $\dot{\phi}$ scale = 13.8 mV/t/major div. (Nitzan, 1966.)

Experimental $\dot{\phi}_p(F)$ data may be curve-fitted by several different functions, such as the ones shown in Fig. 12-22, where the curve is broken into four regions, i.e.,

$$\dot{\phi}_p(F) = \begin{cases} 0 & \text{for } 0 \leq F \leq F_d^{\min} & (12-82a) \\ \lambda'(F - F_d^{\min})^{\nu'} & \text{for } F_d^{\min} \leq F \leq F'_B & (12-82b) \\ \lambda(F - F_0'')^{\nu} & \text{for } F'_B \leq F \leq F_B & (12-82c) \\ \rho_p(F - F_0) & \text{for } F_B \leq F & (12-82d) \end{cases}$$

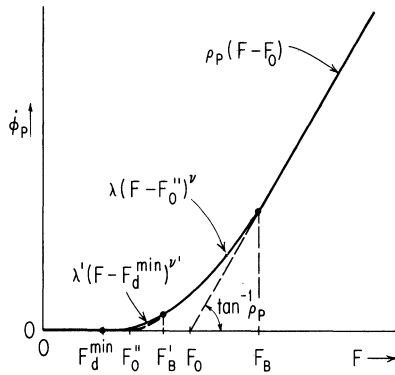


Fig. 12-22. Functions for $\dot{\phi}_p(F)$ curve fitting.

where F_d^{\min} is the static F threshold, F_0'' and F_0 are extrapolated values of dynamic threshold, F_B' and F_B are the F values at the boundaries between the $\dot{\phi}_p(F)$ regions, λ' and λ are proportionality constants and ν' and ν are exponents for the nonlinear $\dot{\phi}_p(F)$ regions, and ρ_p is the slope of the linear region of $\dot{\phi}_p(F)$. For continuity, the expressions for $\dot{\phi}_p(F)$ and $d\dot{\phi}_p(F)/dF$ of neighboring regions must be equal at the borders $F = F_B'$ and $F = F_B$. Continuity at $F = F_B'$ imposes the relations

$$\nu' = \nu \frac{F_B' - F_d^{\min}}{F_B' - F_0''} \quad (12-83)$$

and

$$\lambda' = \lambda \frac{(\nu/\nu')^\nu}{(F_B' - F_d^{\min})^{\nu'-\nu}} \quad (12-84)$$

and continuity at $F = F_B$ imposes the relations

$$\nu = \frac{F_B - F_0''}{F_B - F_0} \quad (12-85)$$

and

$$\lambda = \rho_p \frac{1}{\nu(F_B - F_0'')^{\nu-1}} \quad (12-86)$$

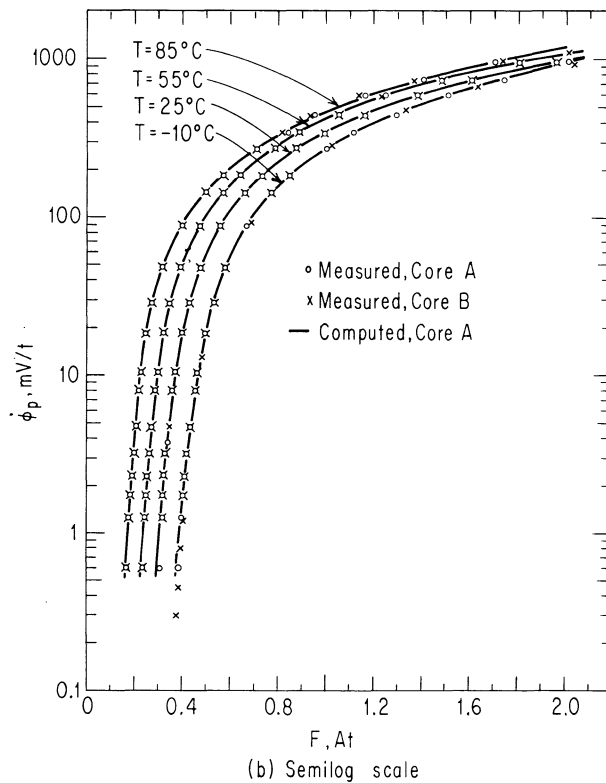
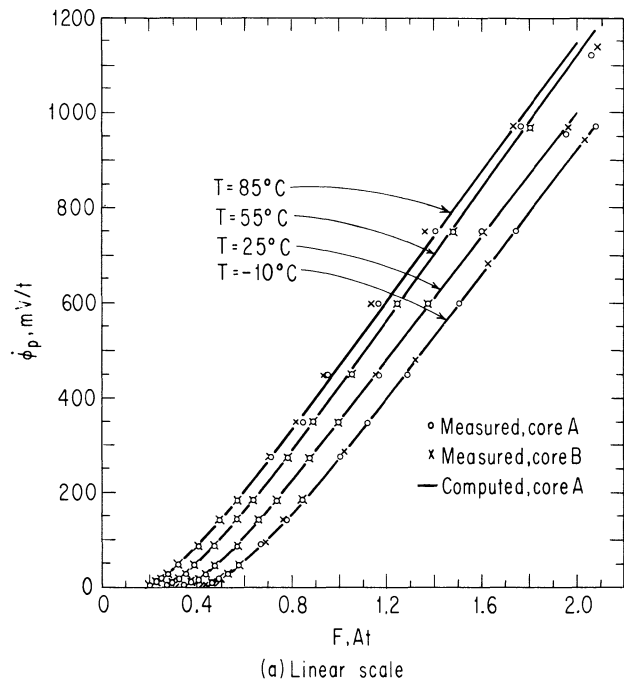


Fig. 12-23. Measured and computed $\phi_p(F)$ curves vs. temperature. Core type of both core A and core B: Lockheed 100 SC1. (Nitzan *et al.*, 1966.)

These relations impose four constraints on the nine parameters in Eqs. (12-82). Hence, the values of only five parameters are needed to completely specify $\dot{\phi}_p$ versus F .

A computer program was developed for determination of the $\dot{\phi}_p(F)$ parameters by least-mean-square curve fitting of Eqs. (12-82) to measured $\dot{\phi}_p(F)$ data. The resulting curve fitting is illustrated in Fig. 12-23(a) for a commercial ferrite core at different temperatures. Since the resolution with a linear scale is poor at low F values, the results are redrawn in Fig. 12-23(b), using a semilog scale.

The semiempirical model $\dot{\phi}_{im}(F, \phi)$ (Eqs. (12-81) and (12-82)) is summarized graphically in Fig. 12-24. Switching characteristics for three F values ($F_1, F_2,$ and F_3) are traced in the figure. For a given F value, the ϕ_d value is determined from Eqs. (12-24), and the $\dot{\phi}_p$ value is determined from Eqs. (12-82). Knowing the value of ϕ_r , we can then plot the parabolic function $\dot{\phi}_{im}$ versus ϕ of Eq. (12-81).

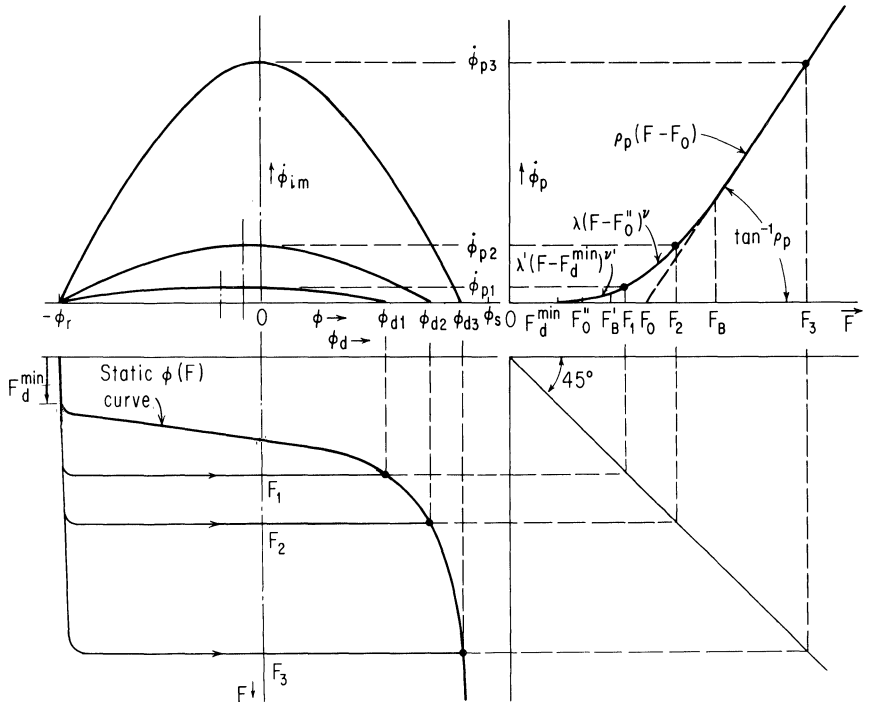


Fig. 12-24. Graphical relations among $\phi_d(F)$, $\dot{\phi}_p(F)$ and $\dot{\phi}_{im}(F, \phi)$.

The excess mmf in the region $F_d^{\min} \leq F \leq F'_B$ is so low that the variations in threshold during the switching time become significant. The assumption in Eq. (12-82b) that the mmf threshold in this region is constant may thus result in an appreciable error. It is more exact to replace F_d^{\min} by the F value on the static $\phi(F)$ curve corresponding to ϕ . If this modification is applied, then $\dot{\phi}_{im}(\phi)$ is no longer parabolic and $\dot{\phi}(t)$ peaks at a value of ϕ_p (see Fig. 12-17) lower than the midpoint between $-\phi_r$ and ϕ_d , which agrees with observed behavior of certain ferrite cores.

Fortunately, the model for $\dot{\phi}_{im}(t)$ (Eqs. (12-81) and (12-82)), is reasonably applicable even if the core is not thin (e.g., a toroid with $r_o/r_i = 1.6$) and also for monotonic $F(t)$ functions other than a step function, though with some modification of the parameter values. The way to apply the model is to divide the switching time into small time intervals, at each of which $\phi_d(F)$ and $\phi_p(F)$ are computed from Eqs. (12-24) and (12-82); these values are then used to compute $\dot{\phi}_{im}$ from Eq. (12-81). For a variable $F(t)$ function, the values of the switching parameters λ , F''_0 , and other parameters of the same nature in Eqs. (12-82) are somewhat different from those for a step $F(t)$. They are generally lower if $F(t)$ is monotonically increasing, and they are generally higher if $F(t)$ is monotonically decreasing. For example, as we shall see later in connection with Fig. 12-29, a good agreement with experimental data was obtained for a ramp function $F(t) = kt$ over a wide range of k (for example, 100:1) using fixed values of λ and F''_0 that are lower than step- F parameters by about 25 to 30 percent.

Since the model for $\dot{\phi}_{im}(t)$ is not restricted to step- $F(t)$ functions only, it may be used in computation of flux switching in square-loop core circuits in general. Such an application is discussed in Sec. 12-6.

Dependence of Main $\dot{\phi}_1(t)$ on Other $\dot{\phi}(t)$ Components. On the basis of the models for $\dot{\phi}_{er}(t)$, $\dot{\phi}_{ew}(t)$, and $\dot{\phi}_{id}(t)$ (Eqs. (12-49), (12-59), and (12-75)), these $\dot{\phi}(t)$ components are independent of each other. In contrast, the solution for $\dot{\phi}_{im}(t)$ is dependent on the other $\dot{\phi}(t)$ components because the required value of the flux ϕ in Eq. (12-81) is

$$\phi = -\phi_r + \int_0^t \dot{\phi}(t) dt \tag{12-87}$$

where

$$\dot{\phi}(t) = \dot{\phi}_{er}(t) + \dot{\phi}_{ew}(t) + \dot{\phi}_{id}(t) + \dot{\phi}_{im}(t) \tag{12-88}$$

In the absence of these other components, the solution of Eq. (12-81) as it stands is absurd because, with nothing to change $\dot{\phi}(t)$ from its initial zero value, the core (or leg) would never start switching. Even if $\dot{\phi}_\epsilon(t)$ were included, the resulting switching time could be unrealistically long because, without $\dot{\phi}_{id}$, the values of $\dot{\phi}_{im}$ in the beginning of switching would be too low.

The relative magnitude of each of the $\dot{\phi}(t)$ components in the beginning of switching is illustrated in Fig. 12-25 for the thin ferrite core of Table 12-1, which was driven by an mmf pulse of amplitude $F_D = 2.22 F_c$. The area under each waveform is the contribution of the corresponding $\dot{\phi}(t)$ component to the increase of the total ϕ . It is evident from this example that the presence of the $\dot{\phi}_{id}(t)$ component is very important for the correct solution of $\dot{\phi}_{im}(t)$, and hence of $\dot{\phi}_i(t)$. The computed total $\dot{\phi}(t)$ was found to be very close to the experimental $\dot{\phi}(t)$ waveform (Nitzan (1966)).

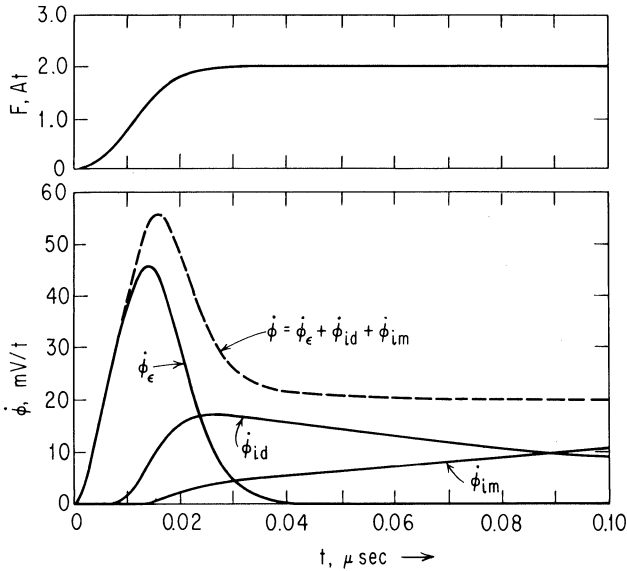


Fig. 12-25. Computed $\dot{\phi}_\epsilon$, $\dot{\phi}_{id}$, $\dot{\phi}_{im}$, and $\dot{\phi}$ vs. t during the beginning of switching of a thin ferrite core (Table 12-1). (Nitzan, 1966.)

Approximate Models for $\dot{\phi}_i(t)$. For switching from $\phi = -\phi_r$ with F larger, say, than $2F_c$, an approximate solution for $[\dot{\phi}_{id}(t) + \dot{\phi}_{im}(t)]$ may be calculated from Eq. (12-81) if ϕ_r is replaced by ϕ_s . By making such a simple modification, the total inelastic $\dot{\phi}(t)$ may be calculated from the approximation

$$\dot{\phi}_i = \dot{\phi}_{id} + \dot{\phi}_{im} \approx \dot{\phi}_p(F) \left\{ 1 - \left[\frac{2\phi + \phi_s - \phi_d(F)}{\phi_s + \phi_d(F)} \right]^2 \right\} \quad (12-89)$$

where $\dot{\phi}_p(F)$ is the same as expressed in Eqs. (12-82). With this model, the initial value of $\dot{\phi}_i$ is not zero, and the switching proceeds even in the absence of the $\dot{\phi}_\epsilon(t)$ components. Neglecting $\dot{\phi}_\epsilon(t)$, the $\dot{\phi}_i(t)$ waveform calculated from Eq. (12-89) closely resembles the waveform $\dot{\phi}_i(t) = \dot{\phi}_{id}(t) + \dot{\phi}_{im}(t)$ calculated from Eqs. (12-75) and (12-81), as illustrated in Fig. 12-26 for a step $F(t)$.

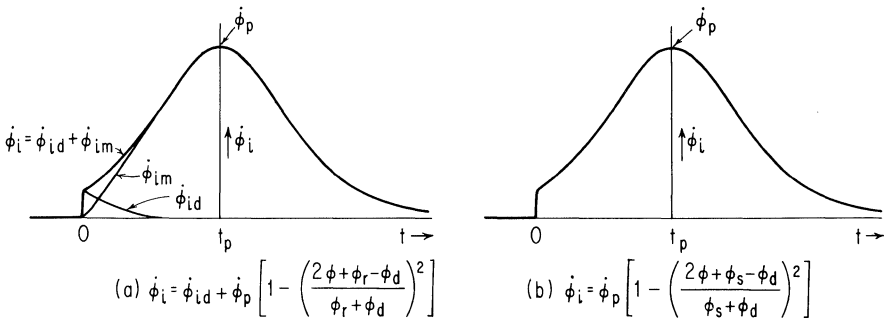


Fig. 12-26. Resemblance between $\dot{\phi}_i(t)$ waveforms derived from different models for inelastic $\dot{\phi}(t)$.

The limitation of the model in Eq. (12-89) should be emphasized. For low F values (for example, $F \lesssim F'_B$), the contribution of $\dot{\phi}_{id}(t)$ is not accounted for adequately by replacing ϕ_r by ϕ_s . In fact, for $F \leq F_d^{\min}$, Eq. (12-89) predicts $\dot{\phi}_i = 0$, since $\dot{\phi}_p = 0$ from Eq. (12-82a), whereas in reality, $\dot{\phi}_i = \dot{\phi}_{id} > 0$.

In many applications, F is sufficiently high to make Eq. (12-89), in conjunction with $\dot{\phi}_p(F)$ of Eq. (12-82), actually very useful. As with Eq. (12-81), Eq. (12-89) may be applied to compute $\dot{\phi}_i(t)$ for an arbitrary monotonic $F(t)$ function by computing the values of $\phi_d(F)$ and $\dot{\phi}_p(F)$ at each time interval. If $F(t)$ is a step function and the contribution of $\phi_\epsilon(t)$ to $\phi(t)$ is ignored, then the solution of Eq. (12-89), obtained by separation of variables, is

$$\phi(t) = \frac{\phi_s + \phi_d(F)}{2} \tanh \left\{ \frac{2\dot{\phi}_p(F)}{\phi_s + \phi_d(F)} t - \tanh^{-1} \left[\frac{2\phi_r + \phi_d(F) - \phi_s}{\phi_s + \phi_d(F)} \right] \right\} - \frac{\phi_s - \phi_d(F)}{2} \quad (12-90)$$

Differentiating Eq. (12-90) with respect to time, we obtain

$$\dot{\phi}_i(t) = \dot{\phi}_p(F) \operatorname{sech}^2 \left\{ \frac{2\dot{\phi}_p(F)}{\phi_s + \phi_d(F)} t - \tanh^{-1} \left[\frac{2\phi_r + \phi_d(F) - \phi_s}{\phi_s + \phi_d(F)} \right] \right\} \quad (12-91)$$

Differentiating again and setting $\ddot{\phi}_i(t)$ equal to zero, we obtain an expression for the time at which $\dot{\phi}_i$ reaches its peak value (see Fig. 12-17), that is

$$t_p = \frac{\phi_s + \phi_d(F)}{2\dot{\phi}_p(F)} \tanh^{-1} \left[\frac{2\phi_r + \phi_d(F) - \phi_s}{\phi_s + \phi_d(F)} \right] \quad (12-92)$$

A further simplification in the model of $\dot{\phi}_i$ may be achieved if F is high enough to replace $\phi_d(F)$ by ϕ_s , for example, if $F > F_3$ in Fig. 12-24. Under this condition, Eq. (12-89) reduces to

$$\dot{\phi}_i \approx \dot{\phi}_p(F) \left[1 - \left(\frac{\phi}{\phi_s} \right)^2 \right] \quad (12-93)$$

We shall show later that under certain simplifying assumptions, Eq. (12-93) may be applied to manual computation of inelastic flux switching. In general, however, utilization of the flux-switching models presented in this chapter requires the use of a digital computer. In the following section we discuss the methods of computation involved in employing these models in computer analyses and compare some computed results with experimental data.

12-6 Computation of Flux Switching in Magnetic-Core Circuits

We now wish to apply the switching models to computation of flux switching in magnetic-core circuits. Both the complexity and the repetitious application of the switching models dictate numerical computation by digital computer. Simple numerical methods that are suitable for this purpose will be illustrated by applying these methods to computation of flux switching of an unloaded core and a core loaded by different combinations of R , L , C , and a diode. We shall also derive from the main inelastic parabolic $\dot{\phi}(\phi)$ model

an approximate relation which is amenable to manual computation of flux switching.

Unloaded Core. Consider an unloaded core whose flux is switched from $-\phi_r$ toward positive saturation by an applied mmf $F(t)$. The objective is to compute $\dot{\phi}(t)$ and $\phi(t)$ and compare the results with experimental data.

Let us temporarily make two simplifying assumptions:

1. F is high enough to justify the use of Eq. (12-89) in computation of $\dot{\phi}_i(F, \phi)$.
2. The elastic $\dot{\phi}(t)$ component is negligible.

On the basis of these assumptions, $\dot{\phi} \approx \dot{\phi}_i$ and, since F is a function of time, $\dot{\phi}$ is described by a first-order nonlinear differential equation of the form

$$\dot{\phi} = \dot{\phi}(t, \phi) \quad (12-94)$$

where t is an independent variable and ϕ is a dependent variable. We divide time t into small Δt intervals and solve Eq. (12-94) numerically. There are several known methods of numerical solutions of differential equations (see, for example, Milne (1950); Scarborough (1950)). For this problem, the following simple predictor-corrector method is adequate.

For generality, let us replace ϕ by y and look for the solution of the first-order differential equation $\dot{y} = \dot{y}(t, y)$. Designating each variable by a subscript representing the time-interval index, consider the n th interval ($t = t_n$) and suppose that the values of y_{n-2} , \dot{y}_{n-2} , y_{n-1} , and \dot{y}_{n-1} have already been determined. We now wish to compute y_n and \dot{y}_n . As a first step, an approximate value of \dot{y}_n is predicted using the relation

$$y_n = y_{n-2} + 2\Delta t \dot{y}_{n-1} \quad (12-95)$$

We now compute $\dot{y}_n = \dot{y}(t_n, y_n)$ and correct y_n using the relation

$$y_n = y_{n-1} + \Delta t \frac{\dot{y}_n + \dot{y}_{n-1}}{2} \quad (12-96)$$

which is closer to the correct y_n value than the relation in Eq. (12-95). The last two steps (in which \dot{y}_n and y_n are computed) are

repeated until convergence is achieved, i.e., the change in \dot{y}_n (or y_n) is negligible. This predictor-corrector process is repeated for succeeding Δt 's until the end of switching, which we define as the time τ_s when $\phi(t)$ approaches ϕ_d to within a small interval (for example, $0.001 \phi_r$) and hence, $\dot{\phi} \approx 0$.

The smaller the value of Δt , the more accurate the results; however, the cost of computation may be higher. One way to determine Δt is to repeat a typical portion of the computation, using decreasing values of Δt , until the changes in the results are negligible. For some cases it is found that Δt should be below two percent of τ_s . If Δt is chosen well below this empirical value, for example, $\Delta t = \tau_s/200$, then only a rough estimate of τ_s is needed in order to determine Δt . An alternative and more efficient way is to adjust Δt automatically in accordance with the number of iterations at the previous Δt .

Assuming that τ_s is the switching time corresponding to $\Delta\phi = 2\phi_r \approx 1.8\phi_s$, an adequate estimate for τ_s may be obtained by substituting Eq. (12-93) into the relation $\int_{-\phi_r}^{\phi_r} d\phi = \int_0^{\tau_s} \dot{\phi}_i dt$, from which we find that

$$\int_0^{\tau_s} \dot{\phi}_p(F) dt \approx \int_{-\phi_r}^{\phi_r} \frac{d\phi}{1 - (\phi/\phi_s)^2} \approx 3.25 \phi_r \quad (12-97)$$

where $\dot{\phi}_p(F)$ is given in Eqs. (12-82). For a step $F(t)$, $\dot{\phi}_p(F)$ is not a function of time, and hence Eq. (12-97) yields

$$\tau_{s, \text{step}} \approx \frac{3.25 \phi_r}{\dot{\phi}_p(F)} \quad (12-98)$$

For a ramp function $F = kt$, evaluation of the integral in Eq. (12-97) is more complex because switching may occur while F increases from F_d^{min} through the three regions of $\dot{\phi}_p(F)$, Eqs. (12-82). However, since τ_s need not be determined accurately, we shall consider only the middle $\dot{\phi}_p(F)$ region. We thus assume that switching starts at $t_0 = F_0''/k$, and by substituting $\dot{\phi}_p(F) = \lambda(kt - F_0'')^\nu = \lambda k^\nu(t - t_0)^\nu$ into Eq. (12-97), the approximate switching time is found to be

$$\tau_{s, \text{ramp}} \approx \left[\frac{3.25(\nu + 1)\phi_r}{\lambda k^\nu} \right]^{\frac{1}{\nu+1}} \quad (12-99)$$

Note that switching terminates at $t = t_0 + \tau_{s, \text{ramp}}$.

Now that we have outlined the steps of computation of inelastic flux switching, let us remove Assumption (2) and include the elastic $\dot{\phi}(t)$ component as well. First consider the case in which the rise of $F(t)$ justifies the use of Eq. (12-63), that is

$$\dot{\phi}_\epsilon = \frac{\epsilon F - \phi_\epsilon}{\delta} \quad (12-100)$$

Since F and ϵ may vary in time, this first-order differential equation will be solved numerically. Here, again, we may use the simple predictor-corrector method represented by Eqs. (12-95) and (12-96).

If the rise time of $F(t)$ is very short (of the order of 1 nano-second), then $\dot{\phi}_\epsilon(t)$ should be computed from Eqs. (12-49) and (12-59), each of which is of the form

$$\phi_\epsilon + \delta \dot{\phi}_\epsilon + \eta \ddot{\phi}_\epsilon = \epsilon F \quad (12-101)$$

In general, any differential equation of the n th order may be reduced to a set of n first-order differential equations by introducing $(n - 1)$ dummy variables (see Milne (1950)). For the second-order differential equation under discussion, we introduce the dummy variable v_ϵ such that

$$\dot{\phi}_\epsilon = v_\epsilon \quad (12-102)$$

and Eq. (12-101) becomes

$$\dot{v}_\epsilon = \frac{\epsilon F - \delta v_\epsilon - \phi_\epsilon}{\eta} \quad (12-103)$$

Equations (12-102) and (12-103) are a set of two first-order differential equations that may be solved for v_ϵ and ϕ_ϵ at each n th Δt interval by using Eqs. (12-95) and (12-96). First, $v_{\epsilon n}$ is predicted using Eq. (12-95) and then, since $\dot{\phi}_{\epsilon n} = v_{\epsilon n}$, the value of $\phi_{\epsilon n}$ is predicted using Eq. (12-96). At each iteration cycle, $\dot{v}_{\epsilon n}$ and $v_{\epsilon n}$ are computed from Eqs. (12-103) and (12-96) and $\dot{\phi}_{\epsilon n}$ and $\phi_{\epsilon n}$ are computed from Eqs. (12-102) and (12-96). These iterations are repeated until convergence is achieved, and t is stepped up by Δt .

We finally remove Assumption (1), and compute $\dot{\phi}_{id}(t)$ from Eqs. (12-75) and (12-78) and $\dot{\phi}_{im}(t)$ from Eqs. (12-81) and (12-82).

Computation of $\dot{\phi}(t)$ and $\phi(t)$, on the basis of the selected switching models and the predictor-corrector method, is readily

performed on a digital computer. Since the same switching model may be applied in different computer programs, or several times within a given program, the steps of computation involved in this model are usually written as a separate "subroutine" or a "procedure" that is "called" within the main program.

Experimental verification of the model for each of the $\dot{\phi}(t)$ components requires that the other components be relatively small. Experimental and computed results are compared in Fig. 12-27 for positive switching from $\phi = -\phi_r$ of the thin ferrite core of Table 12-1, using step- F drives and time durations chosen such that $\dot{\phi}_\epsilon(t)$ followed by $\dot{\phi}_{id}(t)$ are the predominant components. A similar comparison is made in Fig. 12-28 using step- F drives and time durations such that $\dot{\phi}_{im}(t)$ is predominant. Note the wide range of F , from 0.8 to 20.0 ampere-turns, in which the switching models yield a satisfactory agreement with experimental data.

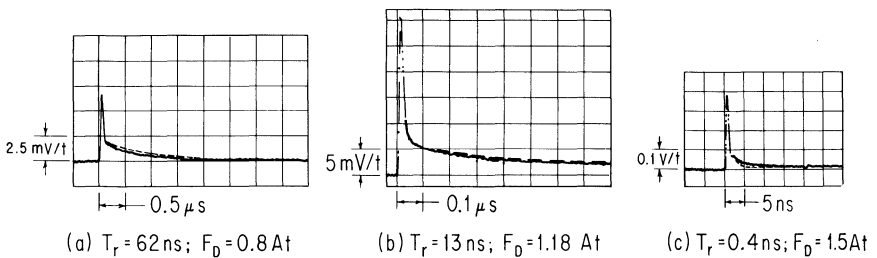


Fig. 12-27. Experimental (dotted or solid line) and computed (dashed line) $\dot{\phi}(t)$ waveforms of a thin ferrite core (Table 12-1) in the beginning of switching using different step- $F(t)$ drives of 10-90% rise-time T_r , and amplitude F_D which emphasize $\dot{\phi}_\epsilon(t)$ and $\dot{\phi}_{id}(t)$.

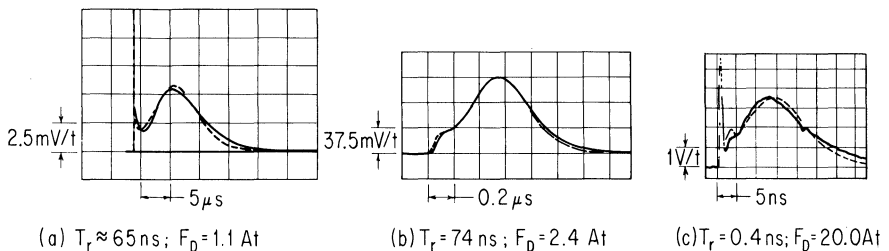
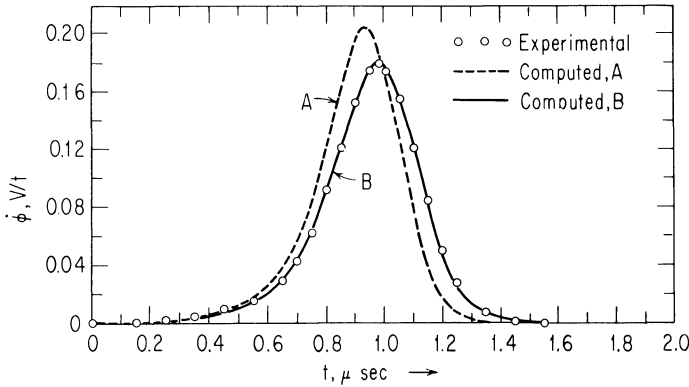
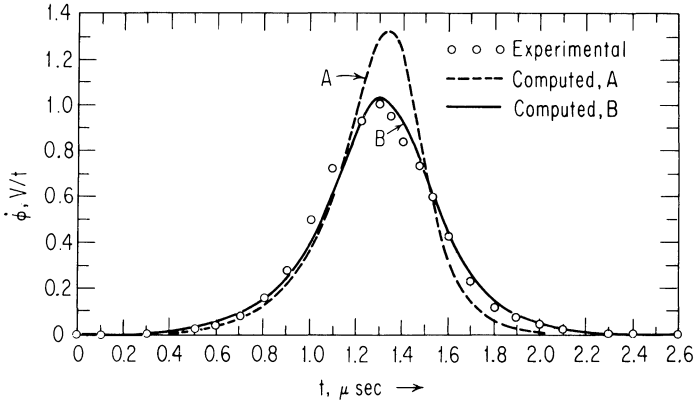


Fig. 12-28. Experimental (dotted or solid line) and computed (dashed line) $\dot{\phi}(t)$ waveforms of a thin ferrite core (Table 12-1) switched fully by different step- $F(t)$ drives of 10-90% rise-time T_r and amplitude F_D .

Experimental $\dot{\phi}(t)$ and computed $\dot{\phi}_i(t)$ waveforms of switching caused by ramp $F(t)$, $F = kt$, are compared in Fig. 12-29 for thin



(a) Thin core ($OD/ID = 1.06$): $k = 3.58 \text{ At}/\mu\text{sec}$; $T = 29 \pm 0.5^\circ\text{C}$. Core parameters are given in Table 12-1.



(b) Thick core ($OD/ID = 1.61$): $k = 0.8575 \text{ At}/\mu\text{sec}$; $T = 30 \pm 0.5^\circ\text{C}$. Core parameters: $r_i = 1.143 \text{ mm}$; $r_o = 1.84 \text{ mm}$; $A = 1.244 \text{ mm}^2$; $\phi_r = 31.0 \text{ Mx}$; $\phi_s = 33.48 \text{ Mx}$; $H_a = 250.0 \text{ At/m}$; $H_q = 26.0 \text{ At/m}$; $H_n = 22.5 \text{ At/m}$; $F_c = 0.28 \text{ At}$; $F_0'' = 0.27 \text{ At}$; $\nu = 1.43$; $\lambda = 1.64 \Omega t^{-2.43} A^{-0.43}$; $F_0 = 0.55 \text{ At}$; $\rho_p = 2.27 \Omega/t^2$; $F_B = 1.2 \text{ At}$.

Fig. 12-29. Experimental and computed $\dot{\phi}(t)$ waveforms of ramp- F switching ($F = kt$) of ferrite cores. Waveform A - Computed, using step- F values of λ and ρ_p . Waveform B - Computed, using λ and ρ_p values which are a fraction (75% in (a); 70% in (b)) of step- F values and shifted to the left (by $0.04 \mu\text{sec}$ in (a); by $0.15 \mu\text{sec}$ in (b)). (Nitzan, 1965.)

and thick ferrite cores. For either case, the computed peak value of $\dot{\phi}$ is higher than the experimental value if step- F switching parameters are used (Waveforms A). However, very good agreement is obtained for both cores (Waveforms B) if λ and ρ_p are lowered by 25 to 30 percent and time shifts of about $0.1 \tau_s$ are introduced. These time shifts are significantly reduced by lowering the values of F_0'' and F_0 as well.

Loaded Core. The switching behavior of a core with resistive, inductive, and capacitive loads is analyzed in Chap. 1, using a very crude switching model. We now wish to apply the more sophisticated switching models of this chapter to such cases.

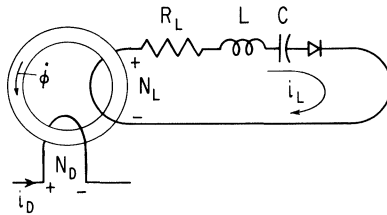


Fig. 12-30. Flux switching in a loaded core.

In Fig. 12-30, a core is coupled by N_L turns to resistance R_L , inductance L , capacitance C , and a p - n junction diode, all in series. The core is switched by drive-mmf $N_D i_D(t)$ from $\phi = -\phi_r$ toward positive saturation. We wish to compute the various time variables during the switching time, and compare $\dot{\phi}(t)$ and the load current $i_L(t)$ with experimental waveforms.

The net mmf acting on the core is

$$F = N_D i_D - N_L i_L \quad (12-104)$$

The resulting $\dot{\phi}$ is a function of F and ϕ , but since F is a function of i_D and i_L , and since i_D is a given function of time, $\dot{\phi}$ is a function of t , i_L , and ϕ , formally expressed as

$$\dot{\phi} = \dot{\phi}(t, i_L, \phi) \quad (12-105)$$

The loop equation is

$$N_L \dot{\phi} = R_L i_L + L \left(\frac{di_L}{dt} \right) + \frac{1}{C} \int_0^t i_L dt' + V_{pn} \quad (12-106)$$

where V_{pn} is the voltage across the diode.

Ignoring the diffusion and junction capacitances of the diode (cf. Gray *et al.* (1964); Searle *et al.* (1964)), we use the model

$$V_{pn} = \theta_{md} \ln \left[1 + \left(\frac{i_L}{I_{sd}} \right) \right] + i_L R_d \quad (12-107)$$

where R_d is the forward resistance of the diode, I_{sd} is its saturation

current, and

$$\theta_{md} = \frac{kT}{q} m_d = 0.86 \cdot 10^{-4} T m_d \quad (12-108)$$

in which k is the Boltzmann constant ($k = 1.381 \cdot 10^{-23}$ joule/°K), q is the charge of an electron ($q = 1.602 \cdot 10^{-19}$ coulomb), T is the absolute temperature in °K, and m_d is a factor which varies between 1 and 2, depending on the junction type.

Substituting Eq. (12-107) into Eq. (12-106) and letting $R = R_L + R_d$, we obtain

$$\frac{di_L}{dt} = \frac{1}{L} \left[N_L \dot{\phi} - \frac{1}{C} q - Ri_L - \theta_{md} \ln \left(1 + \frac{i_L}{I_{sd}} \right) \right] \quad (12-109)$$

where

$$\dot{q} = i_L \quad (12-110)$$

Equations (12-105), (12-109), and (12-110) are a system of three simultaneous first-order differential equations in which t is an independent variable and ϕ , i_L , and q are the dependent variables. The solution of these time variables may be obtained numerically by using Eq. (12-95) and (12-96) or any other predictor-corrector method.

If $L = 0$, then di_L/dt cannot be expressed explicitly as in Eq. (12-109). Instead, the loop equation becomes implicit, i.e., transcendental, in i_L

$$f(i_L) = \frac{1}{C} q + Ri_L + \theta_{md} \ln \left(1 + \frac{i_L}{I_{sd}} \right) - N_L \dot{\phi} = 0 \quad (12-111)$$

Regardless of whether a diode is present or not, the loop equation is transcendental in i_L because $\dot{\phi}$ (Eq. (12-105)) is a function of i_L . Thus, at each iteration, while using the predictor-corrector equations for evaluating ϕ and q , Eq. (12-111) is solved transcendently for the root of i_L . If we use the Newton-Raphson iterative method (see Henrici (1963)), then i_L at the j th iteration is corrected

using the relation

$$i_{L,j} = i_{L,j-1} - \frac{f(i_{L,j-1})}{f'(i_{L,j-1})} \quad (12-112)$$

where $f'(i_L) = df(i_L)/di_L$. Differentiating Eq. (12-111) with respect to i_L , we obtain

$$f'(i_L) \approx \frac{1}{C} \frac{i_L}{di_L/dt} + R + \frac{\theta_{md}}{i_L + I_{sd}} + N_L^2 \frac{\partial \dot{\phi}}{\partial F} \quad (12-113)$$

where $\partial \dot{\phi}/\partial F$ is obtained by differentiating the $\dot{\phi}(F, \phi)$ model (Eqs. (12-66), (12-89), (12-82), and (12-24)) with respect to F . The Newton-Raphson method (Eq. (12-112)) is powerful because it is characterized by quadratic convergence, i.e., the relative error at the j th iteration is the square of the one at the $(j-1)$ th iteration. However, there is the danger that a low $|f'(i_{L,j-1})|$ may result in a divergence from the correct solution. Also, the correction at the j th iteration following Eq. (12-112) will not necessarily yield the fastest convergence. If the convergence turns out to be oscillatory and too slow, then taking half of the change in i_L prescribed by Eq. (12-112) will often yield the proper convergence within very few iterations. In general, convergence is guaranteed in a region where certain conditions are satisfied (see Henrici (1963)).

A computer program for computing the time variables may be written directly on the basis of these numerical methods. For example, using the $\dot{\phi}_i(t)$ model in Eq. (12-89) with step- F parameters and neglecting $\dot{\phi}_e(t)$, computed waveforms of $\dot{\phi}(t)$ and $i_L(t)$ with different step- F drives and different loads are compared with experimental oscillograms in Fig. 12-31 for the same thick core used in Fig. 12-29(b). In judging the agreement between the computed and the experimental waveforms in Fig. 12-31, one should keep in mind that step- F switching parameters were used in the computation, although the net $F(t)$ of the loaded core was not constant because of variations in load current. The variation of computed ϕ versus F during switching is shown in Fig. 12-32 for each of the load cases. The time interval between any two adjacent marked points is constant for each curve. The resulting S -shaped $\phi(F)$ curve is characteristic of a loaded core and may be observed even if the drive current $i_D(t)$ is a ramp. Typical effects of inductive and capacitive loads on $\dot{\phi}$ during the switching time may be observed in Figs. 12-31 and 12-32: $\dot{\phi}$ peaks early with an inductive load, and late with a capacitive load, as expected.

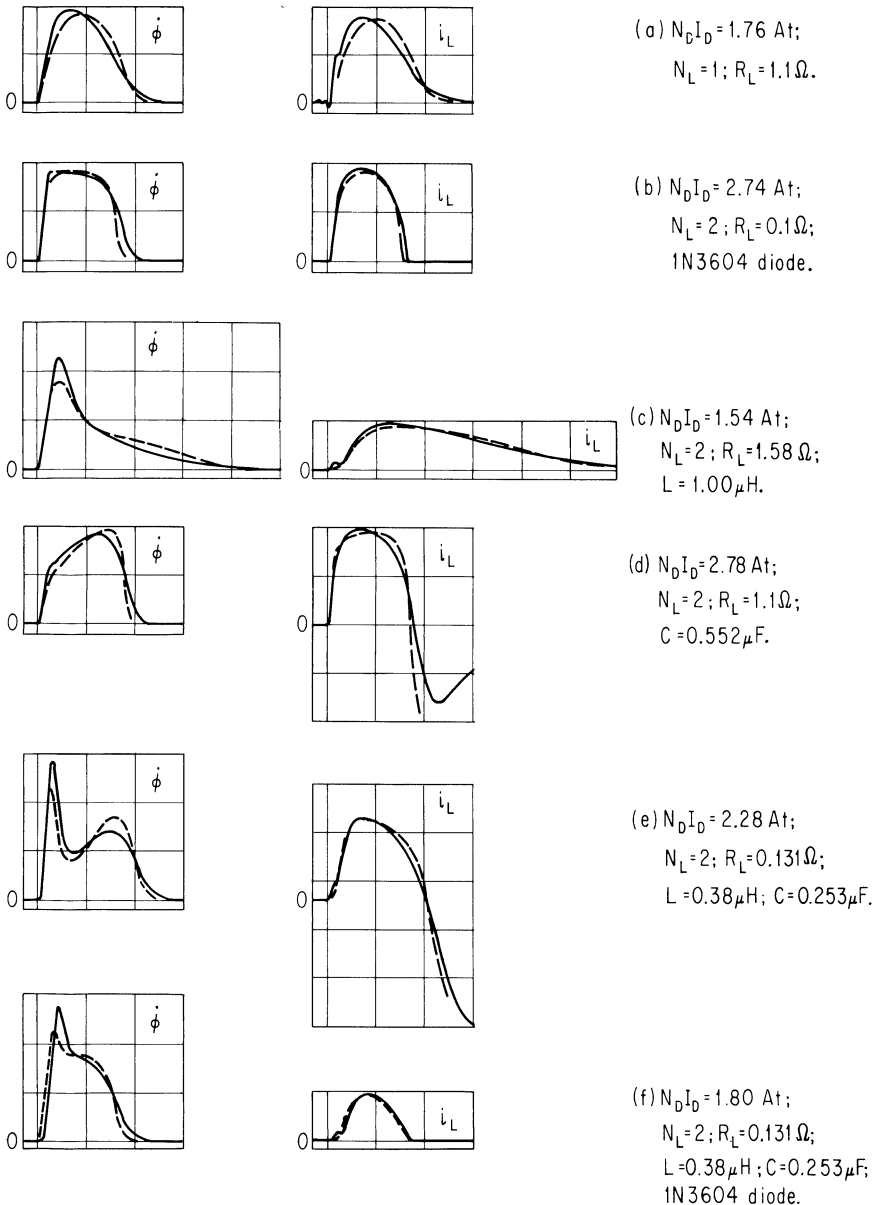
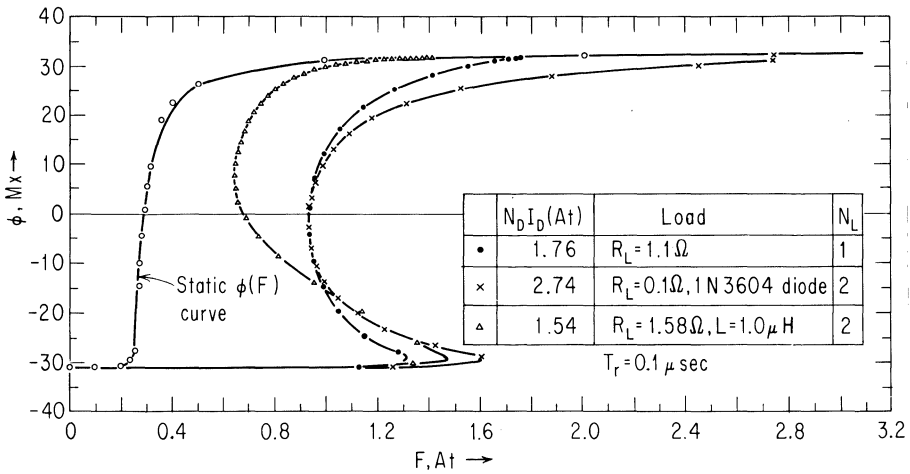
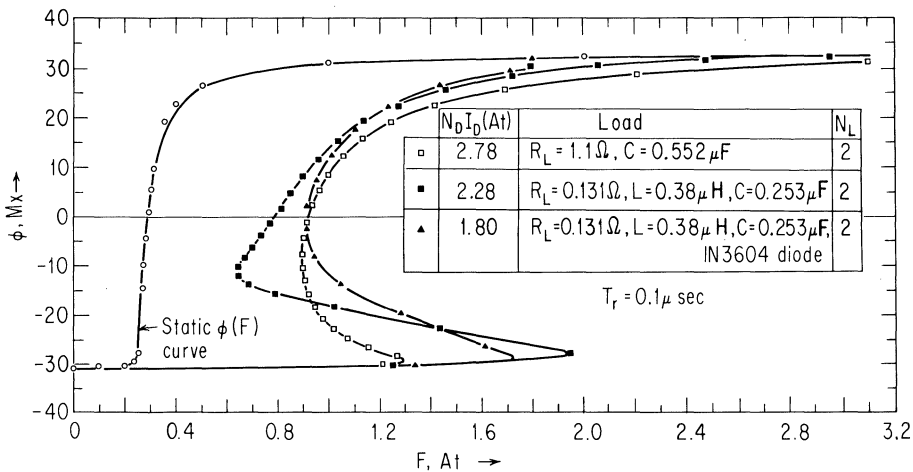


Fig. 12-31. Experimental (solid line) and computed (dashed line) $\dot{\phi}(t)$ and $i_L(t)$ waveforms of a thick ferrite core (OD/ID = 1.61) switching with different loads and amplitudes $N_D I_D$ of step- F drive. Time scale = $0.5 \mu\text{s}/\text{div}$; $\dot{\phi}$ scale = $0.5 \text{ V}/\text{t}/\text{div}$; i_L scale = $0.5 \text{ A}/\text{div}$. (Nitzan, 1965.)



(a) R, R-diode, and RL loads



(b) RC, RLC, and RLC-diode loads

Fig. 12-32. Variations of ϕ vs. F during the switching time, corresponding to the load cases in Fig. 12-31 (Nitzan, 1965).

Voltage Drive. Although flux switching has so far been based on evaluation of $\dot{\phi}$ for given values of \dot{F} , F , and ϕ , in many applications a core is driven by a voltage source rather than a current source, and there is a need then to compute the corresponding net magnetizing current. However, the same switching models used so far are applicable for computation of F for given \dot{F} , $\dot{\phi}$, and ϕ . This is so because the functional relationship among the four

variables \dot{F} , F , $\dot{\phi}$, and ϕ is the same regardless of which variable is solved for. However, since F is implicit in the switching model (see Eq. (12-89)), computations of F for given \dot{F} , $\dot{\phi}$, and ϕ must be performed transcendently.

Average "Switching Resistance." The switching models presented so far are too complex to be applied manually. Quite often, however, a manual calculation of a rough approximation of flux change $\Delta\phi$ is very helpful. This need may arise when either a computer is not available, or if the circuit analysis is to be performed algebraically, or if only a rough estimate of the switching performance is needed. On the basis of the simplified parabolic model for $\dot{\phi}_i(\phi)$ (Eq. (12-93)) we shall now derive a relation that enables us to perform such a manual calculation. This relation is adequate for computing the net flux change $\Delta\phi$ but not the $\dot{\phi}(t)$ waveform. Since the net ϕ_ϵ is usually negligible compared with the net $\Delta\phi_i$, we shall neglect ϕ_ϵ and identify $\dot{\phi}_i$ alone with $\dot{\phi}$.

Consider a core (or core leg) that is switched from an initial flux $\phi_0 = -\phi_r$ to some final flux ϕ_f by a net mmf $F(t)$ of arbitrary waveform, and suppose that during most of the switching time, $F \gtrsim F_B$ (Eq. (12-82d)). The flux switching may become flux-limited by saturation, in which case it is complete and $\phi_f \approx \phi_s$, or it may be time-limited, in which case it is partial and $\phi_0 < \phi_f < \phi_s$. Let τ_s denote the switching time in either case. Since $F \gtrsim F_B$, then $\dot{\phi}_p(F) = \rho_p(F - F_0)$, and Eq. (12-93) becomes

$$\dot{\phi} = \rho(F - F_0) \tag{12-114}$$

where

$$\rho = \rho_p \left[1 - \left(\frac{\phi}{\phi_s} \right)^2 \right] \tag{12-115}$$

Since the units of $\dot{\phi}$ and F are volt/turn and ampere-turn, respectively, ρ is regarded as "switching resistance per turn squared." Defining

$$\frac{1}{\bar{\rho}} \equiv \left(\frac{1}{\rho} \right)_{\text{av}} = \frac{1}{\phi_f - \phi_0} \int_{\phi_0}^{\phi_f} \left(\frac{1}{\rho} \right) d\phi \tag{12-116}$$

then $\bar{\rho}$ is the average value of ρ during the switching time. Substitution of Eq. (12-115) into Eq. (12-116) gives

$$\bar{\rho} = \frac{\phi_f - \phi_0}{\int_{\phi_0}^{\phi_f} \frac{d\phi}{\rho_p [1 - (\phi/\phi_s)^2]}} \quad (12-117)$$

which provides a means for computing $\bar{\rho}$ over the flux change $\Delta\phi = \phi_f - \phi_0$. Assuming in Eq. (12-117) that $\phi_0 = -\phi_r$, then $\bar{\rho}$ versus ϕ_f is found to be

$$\bar{\rho} = \rho_p \frac{(\phi_f/\phi_s) + (\phi_r/\phi_s)}{\tanh^{-1}(\phi_f/\phi_s) + \tanh^{-1}(\phi_r/\phi_s)} \quad (12-118)$$

To see how to use $\bar{\rho}$, note that from Eq. (12-114) we obtain

$$\int_{\phi_0}^{\phi_f} \frac{1}{\rho} d\phi = \int_0^{\tau_s} (F - F_0) dt \quad (12-119)$$

and from Eqs. (12-116) and (12-119) we obtain

$$\Delta\phi = \phi_r + \phi_f = \bar{\rho} \int_0^{\tau_s} F_{\text{ex}} dt = \bar{\rho} \bar{F}_{\text{ex}} \tau_s \quad (12-120)$$

where $F_{\text{ex}} = F - F_0$ is the excess mmf and \bar{F}_{ex} is the average value of F_{ex} over the switching time. (Note that Eq. (12-120) is identical with the crude flux-switching model, Eq. (1-8), used in Part I.) Thus, in order to calculate the flux change due to a given mmf drive, we calculate $\bar{\rho}$ from Eq. (12-118) and multiply $\bar{\rho}$ by the "excess charge-turns" $\bar{F}_{\text{ex}} \tau_s$. However, since $\bar{\rho}$ itself is a function of ϕ_f , the solution for ϕ_f is transcendental, and may require a few iterations.

On the basis of Eq. (12-118), plots of $\bar{\rho}/\rho_p$ versus ϕ_f/ϕ_s are shown in Fig. 12-33 for three assumed ϕ_r/ϕ_s values: 0.84 (dashed line), 0.90 (solid line), and 0.96 (dashed line). Each plot is shown in the region where Eq. (12-118) is valid, i.e., where $-\phi_r \leq \phi_f \leq \phi_s$. Knowing the values of ϕ_r/ϕ_s , ρ_p , and $\bar{F}_{\text{ex}} \tau_s$, then ϕ_f may be determined graphically instead of by the transcendental solution mentioned above. An example is shown in Fig. 12-33 for $\phi_r/\phi_s = 0.9$ (which is a reasonable value for many common square-loop ferrites) and $\bar{F}_{\text{ex}} \tau_s = 2\phi_r/\rho_p$. The resulting value of ϕ_f/ϕ_s corresponds to the intersection point (open circle) of the curve $\bar{\rho}/\rho_p$ versus ϕ_f/ϕ_s (Eq. (12-118)) and the straight line $\bar{\rho}/\rho_p = [\phi_r + \phi_s(\phi_f/\phi_s)]/(\rho_p \bar{F}_{\text{ex}} \tau_s)$ (Eq. (12-120)).

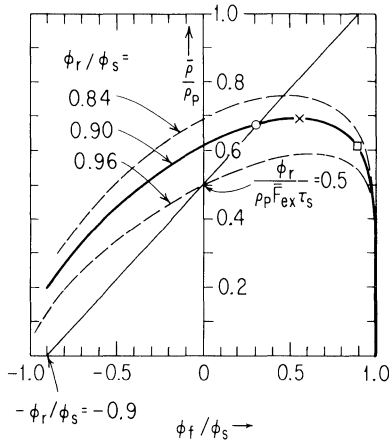


Fig. 12-33. $\bar{\rho}/\rho_p$ vs. ϕ_f/ϕ_s for $\phi_r/\phi_s = 0.84, 0.90, \text{ and } 0.96$, and graphical determination of ϕ_f for the case of $\phi_r/\phi_s = 0.9$ and $\bar{F}_{ex} \tau_s = 2\phi_r/\rho_p$.

Note in Fig. 12-33 that for $\phi_r/\phi_s = 0.9$, $\bar{\rho}/\rho_p$ reaches a maximum value of 0.695 (marked by x) at $\phi_f \approx 0.55\phi_s$. If “efficiency” of flux switching is measured by the flux change due to a given quantity of charge-turns, then this point corresponds to the most efficient flux switching. As ϕ_r/ϕ_s increases from 0.84 to 0.96, the maximum value of $\bar{\rho}/\rho_p$ decreases from 0.75 to 0.59 while the corresponding ϕ_f/ϕ_s value increases from 0.50 to 0.64.

For $\phi_r/\phi_s = 0.9$ and essentially full switching ($\phi_f = \phi_r$), we find that $\bar{\rho} = 0.611\rho_p$ (see the point marked by a square in Fig. 12-33). This result allows us to determine the average full-switching resistance from the slope ρ_p of the linear portion of the measured $\dot{\phi}_p(F)$ plot (Fig. 12-22). The value of $\bar{\rho}$ corresponding to $\phi_f = \phi_r$ may also be related to the switching coefficient

$$S_w = (H_{ap} - H_0)\tau_s = \frac{F - F_0}{l} \tau_s \tag{12-121}$$

where τ_s is the full-switching time under constant- F drive (see Fig. 12-16(a)), and l is the average switching-path length. Substituting Eq. (12-121) and $\Delta\phi = 2\phi_r$ into Eq. (12-120), we obtain the relation

$$\bar{\rho} \approx 0.61\rho_p \approx \frac{2\phi_r}{S_w l} \tag{12-122}$$

The notion of average switching resistance is very useful in qualitative understanding of flux switching in complex magnetic-core circuits. Thus, with this section we reach full circle since the notion of average switching resistance was introduced in Chap. 1, and all of Part I relied on this simplifying notion. The reader was thus spared the necessity of treating complex core models while being introduced to circuit principles and techniques.

12-7 Summary

Flux ϕ and mmf F of each leg in a multileg core depend on the ϕ and F of other legs according to two rules: (1) along a closed path of ℓ legs enclosing m windings, $\sum_{j=1}^{\ell} F_j = \sum_{k=1}^m N_k i_k$, and (2) in any junction of n legs, $\sum_{j=1}^n \phi_j = 0$ (hence, also $\sum_{j=1}^n \dot{\phi}_j = 0$). Flux-switching models (the functional relationships among $\dot{\phi}$, ϕ , \dot{F} , F , and t) for a leg are based on experimental results of flux switching in ferrite cores using constant- F drives. The models encompass the static $\phi(F)$ curve and the elastic and inelastic components of $\dot{\phi}(t)$.

The saturation and nonsaturation regions of a static $M(H)$ curve for ferrites are described by two hyperbolic functions. Integration of these functions over the leg cross section yields expressions for a three-region static $\phi(F)$ curve, $\phi_d(F)$. This model can be modified to handle discontinuous static $\phi(F)$ curves resulting from "re-entrant" $M_d(H)$ curves.

The elastic component of $\dot{\phi}(t)$, namely $\dot{\phi}_\epsilon(t)$, has two sub-components: a high-amplitude spike $\dot{\phi}_{\epsilon r}(t)$ due to rotation of magnetization, and a low $\dot{\phi}_{\epsilon w}(t)$ tail due to domain-wall motion. Each component is described by a second-order differential equation of the form $\phi_\epsilon + \delta\dot{\phi}_\epsilon + \eta\ddot{\phi}_\epsilon = \epsilon F$ (initially, $\phi_\epsilon = 0$ and $\dot{\phi}_\epsilon = 0$). For $\dot{\phi}_{\epsilon w}(t)$, this equation results directly from the stiffness, viscous damping, and mass of an average domain wall. The solution of $\dot{\phi}_{\epsilon r}(t)$ for a step $F(t)$ is consistent with the Landau-Lifshitz and Gilbert equations. For either $\dot{\phi}_\epsilon$ component, $\phi_\epsilon + \delta\dot{\phi}_\epsilon \approx \epsilon F$ if $T_r \gg \eta/\delta$ (for example, $T_r > 5$ nsec), where T_r is the rise time of $F(t)$, and if also $T_r \gg \delta$ (for example, $T_r > 65$ nsec), then $\dot{\phi}_\epsilon \approx \epsilon \dot{F}$. The overall ϵ peaks near $\phi = 0$ and increases with the speed of previous switching, but for $|\phi| > \phi_r$ along the saturation regions, $\epsilon = d\phi_d(F)/dF$.

Two components of inelastic $\dot{\phi}(t)$ are distinguished: a decaying minor component $\dot{\phi}_{id}(t)$ due to minor inelastic wall displacements of essentially constant wall areas, and the bell-shaped main component $\dot{\phi}_{im}(t)$ due to major inelastic wall displacements (involving domain collisions) whose wall areas vary in time. Assuming that

initially $\phi = -\phi_r$, the semiempirical models proposed for these components are

$$\dot{\phi}_{id}(t) = \lambda_{id}(F - F_{id})^{\nu_{id}} \exp\left[-\frac{(t - T_{id})(F - F_{id})}{C_{id}}\right]$$

where λ_{id} , F_{id} , ν_{id} , and C_{id} are switching parameters, and the non-linear differential equation

$$\dot{\phi}_{im} = \dot{\phi}_p(F) \left[1 - \left(\frac{2\phi + \phi_r - \phi_d}{\phi_r + \phi_d} \right)^2 \right]$$

where $\dot{\phi}_p(F)$ is the peak of $\dot{\phi}_{im}(t)$ for a given step $F(t)$, and where ϕ_d is the static ϕ versus F . Expressions are proposed for a four-region $\dot{\phi}_p(F)$ curve fitting. For $F \gtrsim 2F_c$, where F_c is the coercive mmf, approximate $\dot{\phi}_i$ may be obtained from the $\dot{\phi}_{im}$ model above by replacing ϕ_r by ϕ_s . Using this composite $\dot{\phi}_i$ model for a step $F(t)$, the solution $\dot{\phi}_i(t)$ is a sech² function of time. The $\dot{\phi}_i$ models are also applicable for arbitrary monotonic $F(t)$ functions encountered in square-loop-core circuits, e.g., a ferrite core driven by step or ramp $F(t)$ and loaded by different combinations of R, L, C , and a diode. Such application requires the use of a digital computer, and involves numerical methods of integration and transcendental solutions of dependent variables for each increment of switching time τ_s . Experimental verification is given for a wide range of amplitude and different net $F(t)$ waveforms. If an applied step $F(t)$ is sufficiently high to drive the core into saturation, then $\phi_d \approx \phi_s$ and the $\dot{\phi}_i$ model is further simplified to $\dot{\phi}_i \approx \rho(F - F_0)$, where $\rho = \rho_p [1 - (\phi/\phi_s)^2]$ and F_0 is the threshold for high F . A calculated time-averaged ρ for switching from $-\phi_r$ to ϕ_f is

$$\bar{\rho} = \rho_p \frac{u_f + u_r}{\tanh^{-1}u_f + \tanh^{-1}u_r}$$

where $u_f = \phi_f/\phi_s$ and $u_r = \phi_r/\phi_s$. For full switching, $u_f \approx u_r \approx 0.9$, and $\bar{\rho} \approx 0.61 \rho_p \approx 2\phi_r/(S_w l)$, where l is the average switching path and $S_w = (H_{ap} - H_0)\tau_s$ is the switching coefficient. Manual calculation of flux switching is based on the relation $\Delta\phi = \bar{\rho}\bar{F}_{ex}\tau_s$, where $F_{ex} = F - F_0$ is the net excess mmf. The $\bar{\rho}$ model is the crude switching model used throughout Part I.

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