

SPC-LPV11
Printer Interface
Manual

CORRECTIONS

PAGE	DATE
7	1-JUL-88

SPC-LPV11
Printer Interface
Manual

SIGMA INFORMATION SYSTEMS - ANAHEIM, CALIFORNIA

MA400135 REV B - FEBRUARY 1986

Contents

Section 1 - General Information	1
1.1 INTRODUCTION	1
1.2 GENERAL DESCRIPTION	2
1.3 SPECIFICATIONS	2
Section 2 - Installation	3
2.1 UNPACKING AND INSPECTION	3
2.2 FACTORY-SET JUMPERS	3
2.3 INTERFACE TYPE JUMPER SELECTION	5
2.4 DEVICE ADDRESS SELECTION	7
2.5 VECTOR INTERRUPT	7
2.6 DEMAND POLARITY	8
2.7 AUTO-CARRIAGE RETURN	8
2.8 OUTPUT INTERFACE	8
2.9 MODULE INSTALLATION	9
Section 3 - Programming Considerations	10
3.1 ADDRESS SELECTION	11
3.2 CONTROL/STATUS REGISTER	12
3.3 BUFFER REGISTER	13
Appendix - Q Bus Pin Assignments	15

Figures/Tables

FIGURE 2-1	Factory-set Jumpers	4
Figure 2-2	Address Selection	7
Figure 2-3	Vector Interrupt Selection	7
Figure 2-4	Output Connector J1	8
TABLE 2-1	Factory-set Jumpers	3
Table 2-2	Interface Type Jumper Selection	5
Table 2-3	J1 Pin Assignments	9

Section 1 - General Information

1.1 INTRODUCTION

This manual provides the necessary information to install and operate the SPC-LPV11 printer interface circuit board manufactured by Sigma Information Systems, Anaheim, California.

The information in this manual is arranged into the following sections:

Section 1 - GENERAL INFORMATION. This section contains a brief general description of the SPC-LPV11 and the specifications for the interface module

Section 2 - INSTALLATION. This section explains the procedures for equipment installation.

Section 3 - PROGRAMMING CONSIDERATIONS. This section provides the register information for programming the SPC-LPV11.

APPENDIX - The appendix contains a list of the Q bus signals.

1.2 GENERAL DESCRIPTION

The SPC-LPV11 is a parallel interface between the LSI-11 bus and standard line printers such as those manufactured by DEC, Dataproducts, Printronix, and Centronics. The interface receives parallel data from the LSI-11 bus, conditions it, and transmits it to the peripheral printer.

The single dual-wide board interface is completely compatible with DEC operating systems and diagnostics designed for the LPV11. Interface selection is jumper selectable for standard printers. Non-standard printers may be used by reconfiguring the jumpers. Device address and vector interrupt are switch selectable.

1.3 SPECIFICATIONS

Dimensions:	Standard dual-wide module: 8.9 inches (22.8 centimeters) high 5.2 inches (13.2 centimeters) wide
Interface:	Parallel - Dataproducts or DEC LA180A/Centronics compatible
Device Address:	777514. Switch selectable alternates
Interrupt Vector:	200. Switch selectable alternates from 000 to 776
Interrupt Level:	4
Bus Loads:	1 AC, 1 DC
Power Requirements:	+5VDC @ 1 amp (typical)
Temperature	
Operating:	0°C to 50°C
Storage:	-40°C to 85°C
Relative Humidity:	10% to 90% non-condensing

*DEC and Q bus are registered trademarks of Digital Equipment Corporation.

Section 2 - Installation

2.1 UNPACKING AND INSPECTION

The SPC-LPV11 is shipped in a special packing carton designed to keep the module from vibrating and to give it maximum protection during shipment. The packing carton should be retained in case the unit requires reshipment.

Unpack the SPC-LPV11 and visually inspect for physical damage. If any damage has occurred, contact the factory immediately.

2.2 FACTORY-SET JUMPERS

The SPC-LPV11 controller is shipped configured with DEC standard operating parameters as defined in Table 2-1. The location of the switches and jumpers that determine these parameters are shown in Figure 2-1.

PARAMETER	FACTORY SELECTION	2 nd	3 rd
Device Address	777514	764004	764014
Vector Address	200	170	174
Auto-Carriage Return	Enabled		
Demand Polarity	Negative		

TABLE 2-1: FACTORY-SET JUMPERS

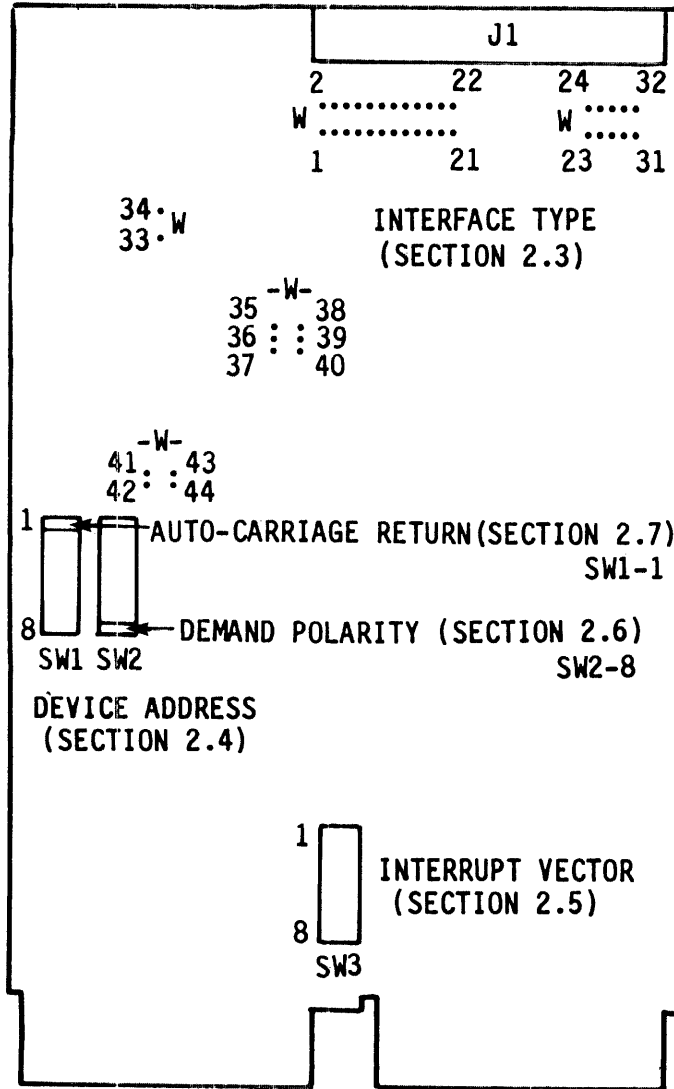


FIGURE 2-1: SPC-LPV11 FACTORY-SET JUMPERS

Before installing modules, verify that these configurations are properly installed. The following sections describe the procedures to verify and/or reconfigure these operating parameters.

2.3 INTERFACE TYPE JUMPER SELECTION

The SPC-LPV11 is shipped with jumpers configured for Dataproducts compatibility. DEC LA180PA/Centronics 101 compatibility is selected by removing the jumper from W3-W4 and installing it at W1-W2.

The jumpers can be reconfigured for non-standard applications. Table 2-1 lists the functions of jumpers W1 through W44. A description of each function follows Table 2-2.

NOTE

W3-W4 and W33-W34 are removable jumpers. All other connections are etched. The etch must be cut to reconfigure the interface type.

JUMPER	STATUS	FUNCTION	JUMPER	STATUS	FUNCTION
W1-W2	Out	Strobe	W23-W24	Out	Line Terminator
W3-W4	In*	Strobe	W25-W26	Out	REM FF
W5-W6	In	Data 5	W27-W28	Out	REM EOT
W7-W8	In	Data 6	W29-W30	In	Data 8
W9-W10	Out	Prime	W31-W32	Out	BUF CLR
W11-W12	In	Data 2	W33-W34	In*	D00 Option
W13-W14	In	Data 1	W35-W36	In	D05 Option
W15-W16	In	Data 4	W37-W40	Out	Lower Case
W17-W18	In	Data 7	W38-W39-W40	In	Parity/VFU
W19-W20	In	Data 3	W41-W42	Out	Upper Case
W21-W22	Out	Mode	W41-W43-W44	In	Upper/Lower Case

*Removable

TABLE 2-2: INTERFACE TYPE JUMPER SELECTION

STROBE	If W1-W2 is installed (DEC LA180PA/Centronics 101 compatible), an active low STROBE will be sent to the printer. If W3-W4 is installed (Dataproducts compatible), an active high STROBE will be sent.
DATA	Data 1 through Data 8 jumpers connect the conditioned data lines to the output pins for DATA 01-08.
PRIME	If W9-W10 is installed, an active high pulse is sent to the printer on INIT.
MODE	Used only with electrostatic printers. If W21-W22 is installed, the PLOT mode can be used by setting CSR bit 00.
LINE TERMINATOR	Used only with electrostatic printers. If W23-W24 is installed, the corresponding bits in the CSR are enabled for printer control when in PLOT mode.
REF FF	Used only with electrostatic printers. If W25-W26 is installed, the corresponding bits in the CSR are enabled for printer control when in PLOT mode.
REM EOT	Used only with electrostatic printers. If W27-W28 is installed, the corresponding bits in the CSR are enabled for printer control when in PLOT mode.
D00 OPTION	If W33-W34 is installed, the MODE control bit 00 of the CSR is disabled.
D05 OPTION	If W35-W36 is installed, information from BDAL 05 is transferred to output Data 6. If not, W40-W37 is installed for conversion of upper case code to lower case.
LOWER CASE	If W37-W40 is installed, upper case letters are converted to lower case letters. Used only if D05 OPTION jumper is removed.
PARITY/VFU	If W38-W39 is installed, the information on BDAL 07 is transferred to output Data 8. This bit is usually used for variable form control but may be user-defined.
UPPER CASE	If W41-R42 is installed, lower case ASCII letters are converted to upper case letters.
UPPER/LOWER CASE	If W43-W44 is installed, both upper and lower case ASCII codes are transmitted to the printer.

2.4 DEVICE ADDRESS SELECTION

Address selection is determined by switches SW1 and SW2. Figure 2-2 shows address bits and associated switch positions. An example is given for 777514, the typical first installation. Refer to DEC's "Microcomputer Interface Handbook" for recommended address and vector assignments.

ADDRESS																	
BITS--->	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
	-----!			-----!				-----!				-----!					
SWITCH->				SW1	SW1	SW1	SW1	SW1	SW2	SW2	SW2	SW2	SW2	SW2			
POSITION	*	*	*	6	5	4	3	2	6	5	4	3	2	1	†	†	!
	-----!			-----!				-----!				-----!					
*ALWAYS 1																	
†ALWAYS 0																	
OFF = 1				OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF			
BINARY->	1	1	1	1	1	1	1	1	0	1	0	0	1	1	0	0	
ADDRESS	-- -----			-----				-----				-----					
HEX----->	7	7		7				5				1			4		

FIGURE 2-2: ADDRESS SELECTION

2.5 VECTOR INTERRUPT

Vector interrupt selection is determined by switch SW3. Figure 2-3 shows vector interrupt bits and associated switch positions. An example of the default vector 200 is described also.

SW3 POSITION	1	8	7	6	4	2	3	5	
VECTOR									
BITS----->	08	07	06	05	04	03	02	01	00
	-----!			-----!				-----!	
SW3 POSITION->	1	8	7	6	4	2	3	5	*
	-----!			-----!				-----!	
OFF = 1		ON	OFF	ON	ON	ON	ON	ON	ON
BINARY----->	0	1	0	0	0	0	0	0	0
VECTOR	!-----!			!-----!				!-----!	
HEX----->	2			0				0	

NOTE: SW3 POSITIONS ARE OUT OF ORDER.

*ALWAYS 0

FIGURE 2-3: VECTOR INTERRUPT SELECTION

2.6 DEMAND POLARITY

Demand polarity is controlled by switch SW2-8. When this switch is ON, the interface accepts a negative demand signal. When this switch is OFF, the unit accepts a positive demand signal. Factory configuration for this switch is OFF for Dataproducts interfaces and ON for LA180PA/Centronics interfaces.

2.7 AUTO-CARRIAGE RETURN

Auto-carriage return function is enabled when switch SW1-1 is ON, which causes the interface to automatically output a carriage return character whenever a line feed or form feed is sent to the printer. Factory setting for this switch is ON>

2.8 OUTPUT INTERFACE

The parallel output connector (J1) is shown in Figure 2-4 and pin assignments are defined in Table 2-3.

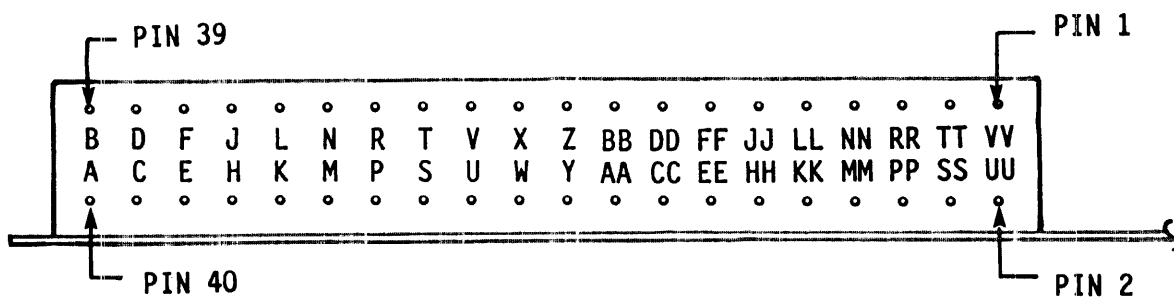


FIGURE 2-4: OUTPUT CONNECTOR J1

	PIN	SIGNAL		PIN	SIGNAL
40	A	GROUND	20	Y	GROUND
39	B	BUF CLR	19	Z	MODE
38	C	GROUND	18	AA	GROUND
37	D	DATA 8	17	BB	DATA 3
36	E	GROUND	16	CC	GROUND
35	F	REM EOT	15	DD	DATA 7
34	H	GROUND	14	EE	GROUND
33	J	REM FF	13	FF	DATA 4
32	K	GROUND	12	HH	GROUND
31	L	LINE TERM	11	JJ	DATA 1
30	M	GROUND	10	KK	GROUND
29	N	SELECT	9	LL	DATA 2
28	P	GROUND	8	MM	GROUND
27	R	FAULT	7	NN	PRIME
26	S	GROUND	6	PP	GROUND
25	T	HDWR	5	RR	DATA 6
24	U	GROUND	4	SS	GROUND
23	V	PAPER	3	TT	DATA 5
22	W	GROUND	2	UU	GROUND
21	X	DEMAND	1	VV	STROBE

TABLE 2-3: J1 PIN ASSIGNMENTS

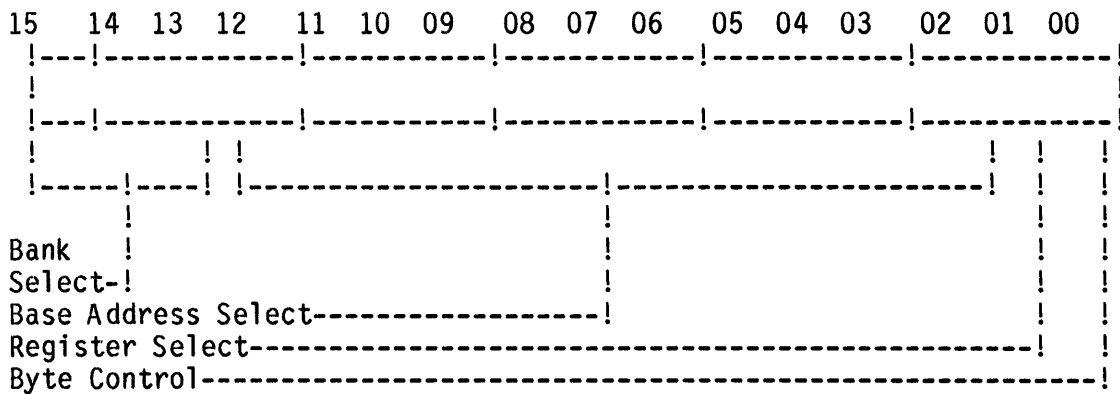
2.9 MODULE INSTALLATION

After switch positions are determined, plug the SPC-LPV11 into any standard Q bus backplane slot. Since the SPC-LPV11 is an interrupting device, the user must be certain that continuity of the BIAK1 and BIAKO lines from the CPU to the SPC-LPV11 exists. There must be no open slots in the priority level.

Section 3 - Programming Considerations

3.1 ADDRESS SELECTION

The address format for the SPC-LPV11 is shown below.



The Bank Select bits are not used in the SPC-LPV11. The bank is selected by the BBS7L (bank 7) select line signal.

The Base Address is selected by switches SW1 and SW2. See Figure 2-2 for bit-switch correspondence.

If the Register Select bit is LOW, the CSR is addressed. If it is HIGH, the BUF is addressed.

3.2 CONTROL/STATUS REGISTER

The format for the Control/Status register is shown below.

```

15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
!---!-----!-----!-----!-----!-----!-----!
!ERR ////////////// ////////////// // RDY INT // BUF REM  REM LINE MC!
!   ////////////// ////////////// //      ENB // CLR EOT  FF  TERM  !
!---!-----!-----!-----!-----!-----!-----!

```

BIT	CODE	DESCRIPTION
-----	------	-------------

15	ERR	ERROR. Read only. Set when an error condition exists. cleared only by manual correction of the error condition. Exact error condition is determined by the particular line to which the SPC-LPV11 is interfaced. Possible errors include:
----	-----	---

No printer connected to interface
Printer power OFF
No paper
Printer OFF LINE
Printer drum gate open
Over temperature alarm
Hardware alarm

When set, initiates an interrupt if INT ENB (bit 6) is set.

14-08	Unused	Read as zeros.
-------	--------	----------------

7	RDY	READY. Read only. Set when the printer is ready to accept a new character. Also set by INIT if the printer is ON LINE and no errors are present.
---	-----	--

6	INT ENB	INTERRUPT ENABLE. read/Write. When set, allows an interrupt sequence to begin when READY (bit 7) or ERROR (bit 15) is set. Cleared by INIT.
---	---------	---

5	Unused	Read as zero.
---	--------	---------------

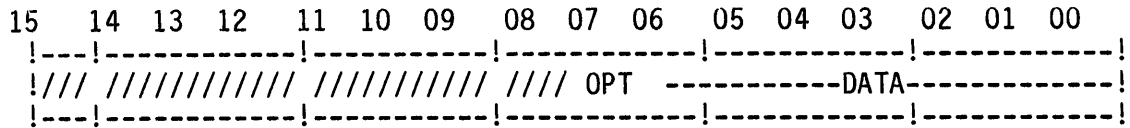
4	BUF CLR	BUFFER CLEAR. Write only. Used only with some electrostatic printers. When set, clears the buffer indicated by the MODE CONTROL (bit 0). Cleared by INIT.
---	---------	---

3	REM EOT	REMOTE END OF TRANSMISSION. Write only. Used only with some electrostatic printers. Set to perform an EOT function when in the PLOT mode (ASCII code disabled). Cleared by INIT.
---	---------	--

- 2 REM FF REMOTE FORM FEED. Write only. Used only with some electrostatic printers. Set to perform a form feed when in the PLOT mode
- 1 LINE TERM LINE TERMINATOR. Write only. Used only with some electrostatic printers. Set to print the graphics line prior to receipt of a complete scan line. Cleared by INIT.
- 0 MC MODE CONTROL. Write only. Used to select the mode of operation in printer/plotters. Set for plotter operation. Cleared for printer operation. Cleared by INIT.

3.3 BUFFER REGISTER

The format for the buffer register is shown below.



BIT CODE DESCRIPTION

15-08 Unused

7 OPT OPTION. Write only. The operation of this bit is user-definable. It is usually used as a vertical form (VFU) control. Other options include:

- Parity Bit (software generated)
- Plotting Option

Cleared by INIT.

06-00 DATA DATA BITS 06-00. Write only. Provide character information to the line printer. Cleared by INIT.

PIN	SIGNAL	LSI-11/2	LSI-11/23	PIN	SIGNAL	LSI-11/2	LSI-11/23
AA1	BIRQ5L			AA2	+5V		
AB1	BIRQ6L			AB2	-12V		
AC1	BDAL16L			AC2	GND		
AD1	BDAL17L			AD2	+12V		
AE1	*SS1	STOP L	SINGLE STEP	AE2	BDOUTL		
AF1	*SRUNL	SRUNL	SRUNL	AF2	BRPLYL		
AH1	*SRUNL	SRUNL	SRUNL	AH2	BDINL		
AJ1	GND			AJ2	BSYNCL		
AK1	*MSPAREA	MTOEL	NOT USED	AK2	BWTBTL		
AL1	*MSPAREB	GND	NOT USED	AL2	BIRQ4L		
AM1	GND			AM2	*BIAK1L	NOT USED	MMUSTRH
AN1	BDMRL			AN2	*BIAK0L		
AP1	BHALTL			AP2	BBS7L		
AR1	BREFL	NOT USED	NOT USED	AR2	*BDMG1L	NOT USED	UBMAAPL
AS1	+12VB			AS2	*BDMG0L		
AT1	GND			AT2	BINITL		
AU1	PSPARE1			AU2	BDAL0L		
AV1	+5VB			AV2	BDAL1L		
BA1	BDCOKH			BA2	+5V		
BB1	BPOKH			BB2	-12V		
BC1	*SSPARE4	SCLK3H	MMUDAL18H	BC2	GND		
BD1	*SSPARE5	SWMIB18H	MMUDAL19H	BD2	+12V		
BE1	*SSPARE6	SWMIB19H	MMUDAL20H	BE2	BDAL2L		
BF1	*SSPARE6	SWMIB20H	MMUDAL21H	BF2	BDAL3L		
BH1	*SSPARE8	SWMIB21H	CLKDISL	BH2	BDAL4L		
BJ1	GND			BJ2	BDAL5L		
BK1	*MSPAREB	NOT USED	NOT USED	BK2	BDAL6L		
BL1	*MSPAREB	NOT USED	NOT USED	BL2	BDAL7L		
BM1	BND			BM2	BDAL8L		
BN1	BSACKL			BN2	BDAL9L		
BP1	BIRQ7L			BP2	BDAL10L		
BR1	BEVNTL			BR2	BDAL11L		
BS1	PSPARE4	PSPARE4	+12VB	BS2	BDAL12L		
BT1	GND			BT2	BDAL13L		
BU1	PSPARE2			BU2	BDAL14L		
BV1	+5V			BV2	BDAL15L		

*NOT BUSSED

PARTS LIST	Sigma Information Systems Inc.	DRAWN		PARTS LIST NO.			400135-100	4
		CHECK						
ASSY TITLE: SPC-10Y11 Q BUS PARALLEL LINE PRINTER INTERFACE		DESIGN ENG		D NO.	D NO.	SH 1 OF 4		REV
		PROJ ENG						
		DOC CONT						
		OTHER						

LTR	AUTHORITY	EFFECTIVITY	DESCRIPTION	BY	DATE	APPROVED

REV STATUS BY SHEET	REV LTR										
	SHEET	1	2	3	4	5	6	7	8	9	10

PARTS LIST	Sigma Information Systems Inc.		CODE IDENT. NO.	PARTS LIST NO.	SHEET	REV LTR.
				400135-100	2 OF 4	A

FIND NO.	REV LTR	NOTE	QTY	UM	SIGMA PART NO	VENDOR PART NO	DESCRIPTION	REFERENCE DESIGNATOR	SPEC/SOURCE	CODE IDENT
1			1	EA	400134		PWB, SPC-LPV II		SIGMA	
2			1	EA		SP-18 WHITE	HANDLE, SIGMA LOGO, 1.8"		S. PHILLIPS	
3			2	EA		4 X 641	RIVET, POP, AL 1/8" SHORT		DAYTON	
4						RH6240D2R	CONNECTOR, 40 PIN HEADER		SAE	
5			1	EA		\$N 7400	IC, QUAD 2 INPUT NAND	U18	T. I.	
6			1	EA		\$N 7402	IC, QUAD 2 INPUT NOR	U5	↑ T. I.	
7			1	EA		\$N 7404	IC, HEX INVERTER	U19		
8			3	EA		\$N 7408	IC, QUAD 2 INPUT AND	U4, 12, 21		
9			1	EA		\$N 7410	IC, TRIPLE 3 INPUT NAND	U27		
10			1	EA		\$N 7425	IC, DUAL 4 INPUT NOR	U17		
11			1	EA		\$N 7430	IC, 8 INPUT NAND	U13		
12			1	EA		\$N 7437	IC, QUAD 2 INPUT NAND DR.	U8		
13			1	EA		\$N 7438	IC, QUAD 2 INPUT NAND OC.	U35		
14			1	EA		\$N 7440	IC, DUAL 4 INPUT NAND DR.	U15		
15			4	EA		\$N 7474	IC, DUAL D EDGE TRIG F/F	U1, 22, 25, 29		
16			1	EA		\$N 7486	IC, QUAD EX OR	U14		
17			4	EA		\$N 74123	IC, DUAL RET MONO MULTIV.	U2, 3, 11, 28		
18			1	EA		\$N 74174	IC, HEX D EDGE TRIG F/F w/cle	U16		
19			1	EA		\$N 74LS24	IC, OCTAL DRIVER 3S	U26		
20			1	EA		\$N 74LS241	IC, OCTAL DRIVER 3S	U7		T. I.

PARTS LIST	Sigma Information Systems Inc.			CODE IDENT. NO.	PARTS LIST NO.	SHEET	REV LTR.
						3 OF 4	A

FIND NO.	REV LTR	NOTE	QTY	UM	SIGMA PART NO	VENDOR PART NO	DESCRIPTION	REFERENCE DESIGNATOR	SPEC/SOURCE	CODE IDENT
21			1	EA		SN74273	IC, OCTAL D F/F W/CLR	U6	T. I.	
22			2	EA		DM8136	IC, ADDRESS COMPARATOR	U23, 24	NATIONAL	
23			4	EA		D58640	IC, UNIBUS RECEIVER	U9, 20, 33, 34	NATIONAL	
24			3	EA		D58641	IC, UNIBUS TRANSMITTER	U30, 31, 32	NATIONAL	
25			3	EA		2-435668-8	SMD, DIP 8 POS	SW1, 2, 3	AMP	
26			4	EA		750-81-R1K	RES MOD, 1K Ω , 2% SIP	RU1, 3, 4, 5	CTS	
27			2	EA		RN55D1780F	RES, MF 178 Ω 1%, 1/8W	R25, 27	MIL-R-11	
28			1	EA		RC076F181J	RES, 180 Ω , 1/4W, 5%	R17	↑	
29			2	EA		RN55D3830F	RES, 383 Ω , 1/8W, 1%	R24, 26		
30			15	EA		RC076F102J	RES, 1k Ω , 1/4W, 5%	R2, 5, 7-12, 14-16	↓	
31			3	EA		RC076F103J	RES, 10k Ω , 1/4W, 5%	R1, 3, 23		
32			4	EA		RC076F308J	RES, 30k Ω , 1/4W, 5%	R4, 6, 13, 22	MIL-R-11	
33			6	EA		1N914	DIODE, H.S., S.S.	CR1-6	MOTOROLA	
34			4	EA		CD15ED470J03	CAP, MICA, 47PF, 5%, 500V	C2, 6, 21, 22	CORNELL-DUBLIER	
35			2	EA		CD15FD101J03	CAP, MICA, 100PF, 5%, 500V	C1, 4	CORNELL-DUBLIER	
36			1	EA		CD15FD471J03	CAP, MICA, 470PF, 5%, 500V	C20	CORNELL-DUBLIER	
37			20	EA		CGB103ZDZ	CAP, CER GLASS .01 μ f, 50V ^{+20%} _{-20%}	C3, 5, 7-10, 13, 19, 23-29	UNITRODE	
38			3	EA		150D475X 0010A2	CAP, TANT 4.7 μ f, 10V, 20%	C36-38	SPRAGUE	
39										
40										

PARTS LIST	Σ Sigma Information Systems Inc.	CODE IDENT. NO.	PARTS LIST NO. 400135-100	SHEET 4 OF 4	REV LTR. A
-------------------	---	------------------------	-------------------------------------	------------------------	----------------------

FIND NO.	REV LTR	NOTE	QTY	UM	SIGMA PART NO	VENDOR PART NO	DESCRIPTION	REFERENCE DESIGNATOR	SPEC/SOURCE	CODE IDENT
41			2	EA		ECE B1JV 220F	CAP, ALUM, 22uf, 35V, AXIAL	C11, 12	PANASONIC	
42			AR			5951-1	WIRE, 30AWG SOLID, KYNAR		ALPHA	
43			1	EA		WTS-36S-1-T	POST, W/W, TIN PLATE	CUT TO SIZE	ROBINSON/ ALPHA	
44										
45										

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

JUMPER TABLE

	-100	-101	-102
W1-W2	OUT	IN	IN
W3-W4	IN	OUT	OUT
W5-W6	IN	IN	IN
W7-W8	IN	IN	IN
W9-W10	OUT	OUT	OUT
W11-W12	IN	IN	IN
W13-W14	IN	IN	IN
W15-W16	IN	IN	IN
W17-W18	IN	IN	IN
W19-W20	IN	IN	IN
W21-W22	OUT	OUT	OUT
W23-W24	OUT	OUT	OUT
W25-W26	OUT	OUT	OUT
W27-W28	OUT	OUT	OUT
W29-W30	IN	IN	IN
W31-W32	OUT	OUT	OUT
W33-W34	IN	IN	IN
W35-W36	IN	IN	IN
W37-W40	OUT	OUT	OUT
W39-W38	IN	IN	IN
W41-W42	OUT	OUT	OUT
W43-W44	IN	IN	IN

SIDE 2		SIDE 1	
+5V	A		
	B		
0V	C		
	D		
BDOUTL	E		
BRPLY	F		
BDINL	H		
B5YNL	J	0V	
BWTBT	K		
BIRG	L		
BIKINL	M	0V	
BIKOUTL	N		
BB5TL	P		
	R		
	S		
BINITL	T	0V	
BDAL00L	U		
BDAL01L	V		
+5V	A		
	B		
0V	C		
	D		
BDAL02L	E		
BDAL03L	F		
BDAL04L	H		
BDAL05L	J	0V	
BDAL06L	K		
BDAL07L	L		
BDAL08L	M	0V	
BDAL09L	N		
BDAL10L	P		
BDAL11L	R		
BDAL12L	S		
	T	0V	
	U		
BDAL15L	V	+5V	

J1

GND	A	B	BUF CLR
	C	D	DATA 8
	E	F	REM EOT
	H	J	REM FF
	K	L	LINE TERM
	M	N	SELECT
	P	R	FAULT
	S	T	HPWR
	U	V	PAPER
	W	X	DEMAND
	Y	Z	MODE
	AA	BB	DATA 3
	CC	DD	DATA 7
	EE	FF	DATA 4
	HH	JJ	DATA 1
	KK	LL	DATA 2
	MM	NN	PRIME
	PP	RR	DATA 6
	SS	TT	DATA 5
GND	UU	VV	STROBE

LAST REFERENCE DESIGNATION USED

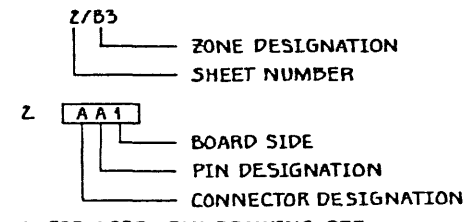
INTEGRATED CIRCUIT	U35
RESISTOR	R27
CAPACITOR	C38
SWITCH	SW3
RESISTOR MODULE	RU5
DIODE	CR6

REFERENCE DESIGNATION NOT USED

CAPACITOR	C30-35
-----------	--------

REF DESIG.	GATES USED PER TOTAL	PART NUMBER
U11	1/2	74123
U15	1/2	7440
U18	2/4	7400
U20	3/4	
U29	1/2	74LS74
U35	3/4	

- CAPACITOR VALUES ARE IN MICROFARADS.
- RESISTOR VALUES ARE IN OHMS ±5%, 1/4W.
- DESIGNATIONS SHOWN IN PARENTHESIS INDICATES WHERE A SIGNAL ORIGINATES OR TERMINATES.



1. FOR ASSEMBLY DRAWING SEE
 NOTES: UNLESS OTHERWISE SPECIFIED

SDC-LPV11

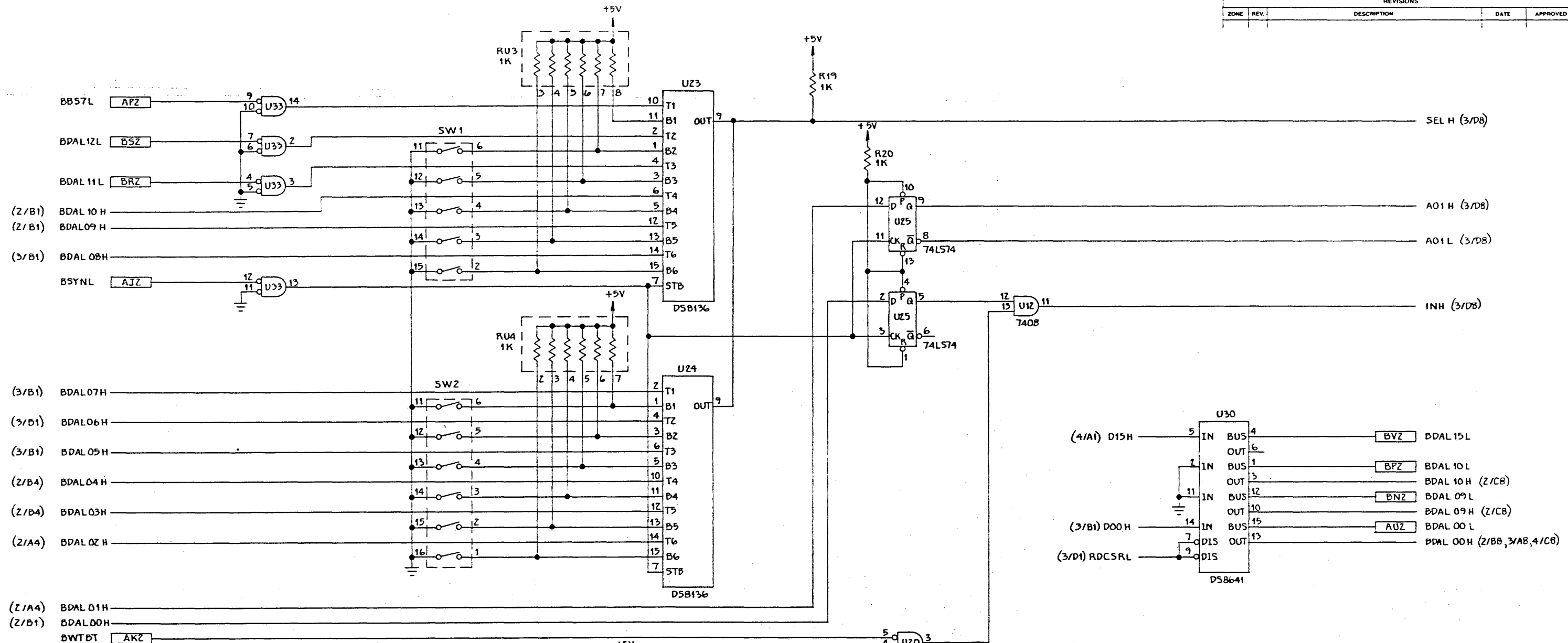
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES 1/64 .XX ± 0.020 ± 0°30' .XXX ± 0.010		THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO SIGMA INFORMATION SYSTEMS, INC. AND MAY NOT BE REPRODUCED OR USED FOR OTHER THAN MAINTENANCE PURPOSES WITHOUT PRIOR WRITTEN PERMISSION FROM AN OFFICER OF THE ABOVE FIRM.			
MATERIAL	FINISH	DRAWN	CHECKED	TITLE SCHEMATIC DIAGRAM Q-BUS PARALLEL LINE PRINTER INTERFACE	
NEXT ASSY.	USED ON	ENGINEER	APPROVED	SIZE D	CODE IDENT. NO. SD400135
APPLICATION	DO NOT SCALE DRAWING	APPROVED	APPROVED	SCALE	WORK ORDER NO. SHEET 1 of 4

DWG. NO. SD 400135

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

D

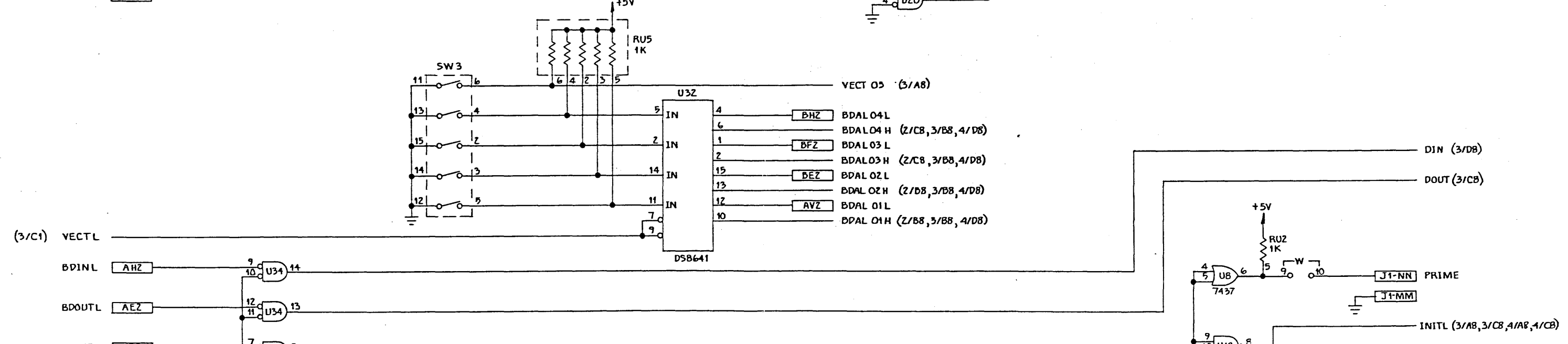
D



C

C

B



A

A

SIZE D	CODE IDENT. NO.	DRAWING NO. SD400135	REV. NC
SCALE	WORK ORDER NO.	SHEET 2 OF 4	

DRAWING NO. SD 400135

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

D

D

C

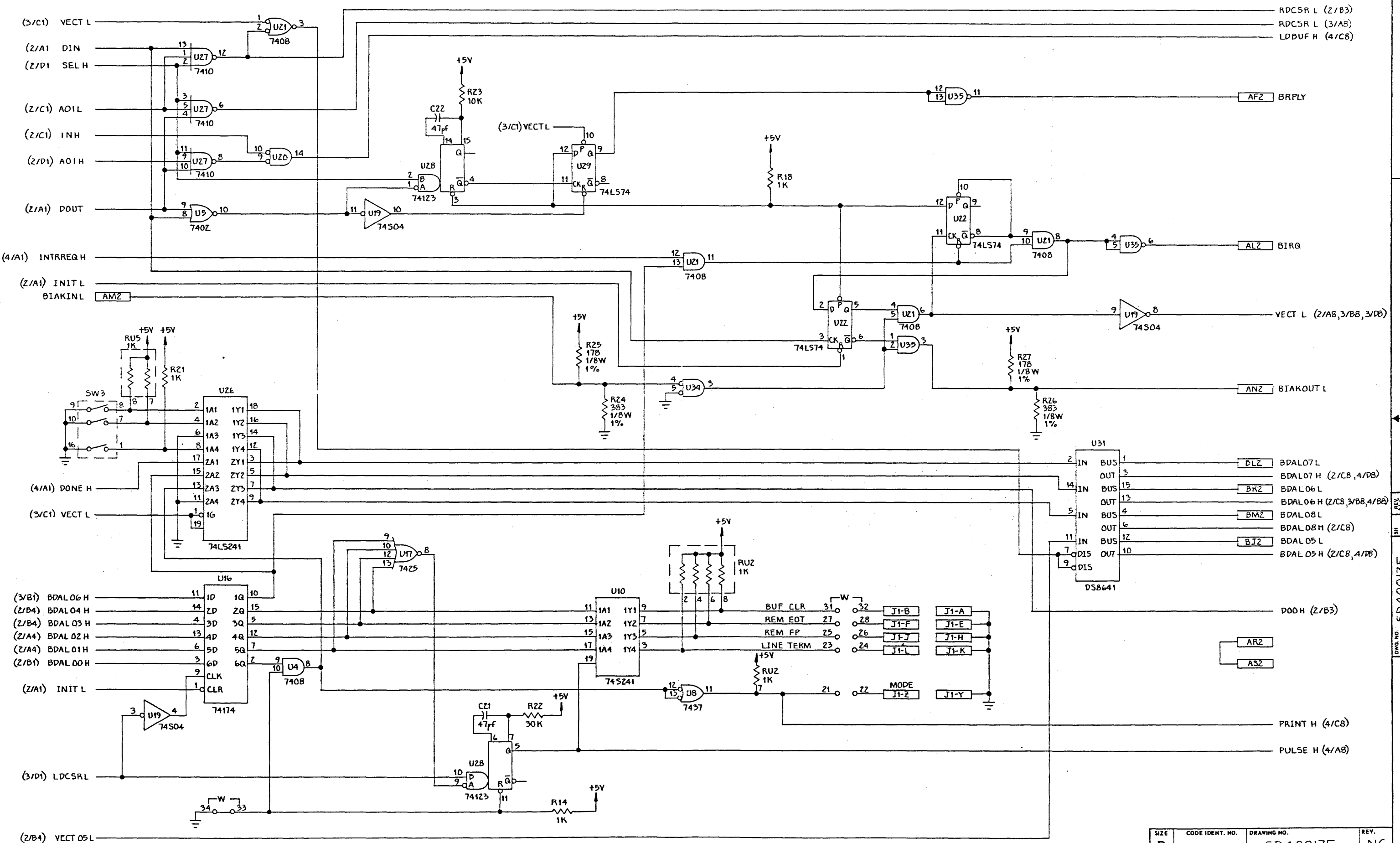
C

B

B

A

A

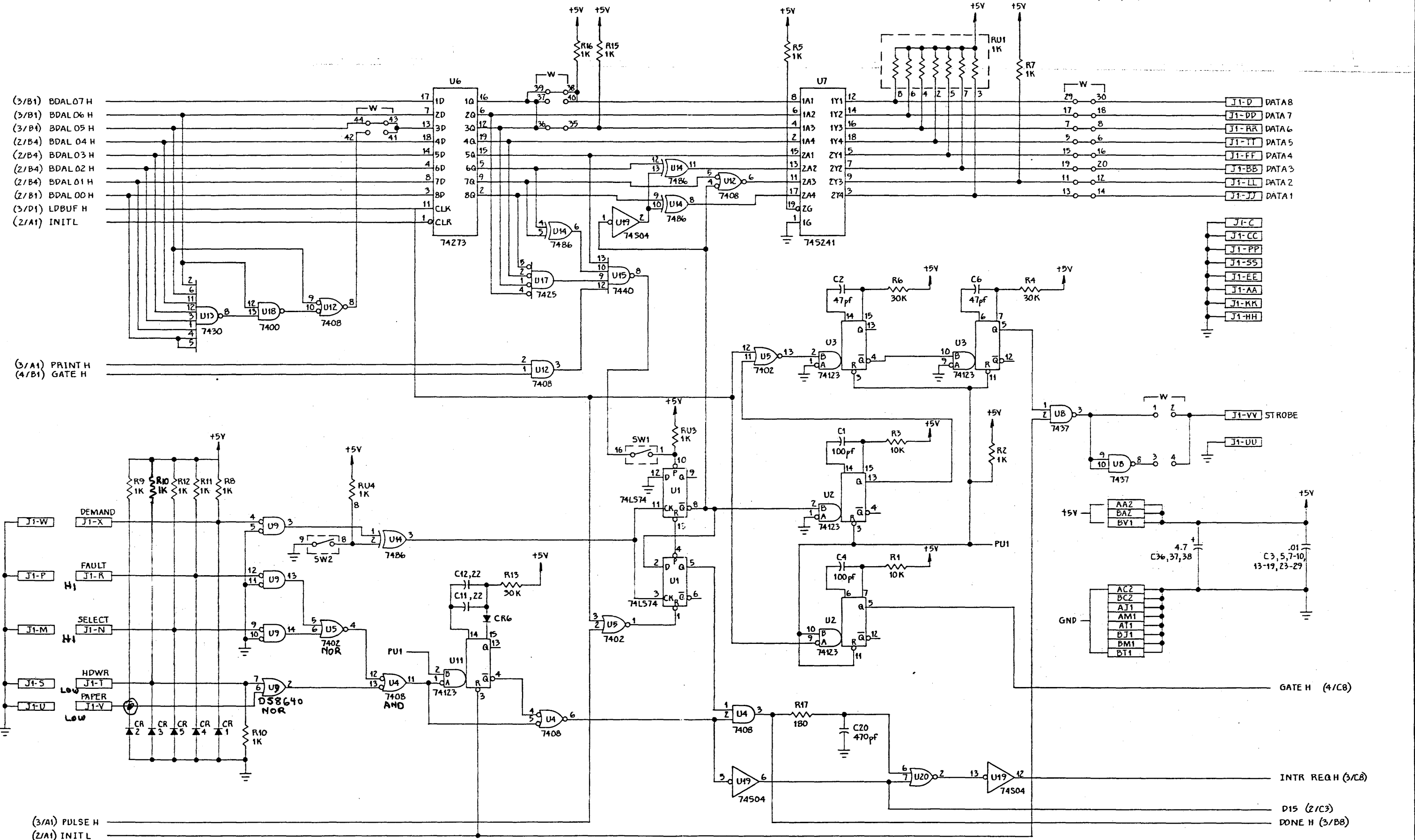


U31	IN	OUT	Label
2	IN	1	DLZ BDAL07L
3	OUT	3	BDAL07H (2/CB, 4/DB)
14	IN	15	BKZ BDAL06L
13	OUT	13	BDAL06H (2/CB, 3/BB, 4/DB)
4	IN	4	BMZ BDAL08L
6	OUT	6	BDAL08H (2/CB)
12	IN	12	BJZ BDAL05L
10	OUT	10	BDAL05H (2/CB, 4/DB)

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400135	NC
SCALE	WORK ORDER NO.	SHEET 3	OF 4

DWG. NO. SD400135

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED



D

D

C

C

B

B

A

A

DRAWING NO. SD400135

SIZE D	CODE IDENT. NO.	DRAWING NO. SD400135	REV. NC
SCALE	WORK ORDER NO.	SHEET 4	OF 4