Price: $6.25

MODELS 92200/93200 SERIES TIME-MULTIPLEXED COMMUNICATION CHANNELS (TMCC) Technical Manual

SDS 900685C September 1965

SCIENTIFIC DATA SYSTEMS/1649 Seventeenth Street/Santa Monica, California/UP 1-0960

Printed in U.S.A.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

LIST OF TABLES (Continued)

SECTION I
GENERAL DESCRIPTION

1.1 GENERAL

1.2 This publication provides information relating to the Time-Multiplexed Communication Channel option manufactured by Scientific Data Systems, 1649 Seventeenth Street, Santa Monica, California.

1.3 In this publication, the Time-Multiplexed Communication Channel option is referred to as "TMCC". The models covered, with their description and the figure references, are listed in table 1-1.

Table 1-1. TMCC Models

Model	Description	Channel Used	Figure
92200	6-bit characters with interlace	W(A), C	1-1
92210	6-bit characters with interlace	Y(B), D	1-1
92201	12-bit characters with interlace	C	1-1
92211	12-bit characters with interlace	D	1-1
92202	24-bit characters with interlace	C	1-1
92212	24-bit characters with interlace	D	1-1
93200	6-bit characters without interlace, single channel	W(A), C	1-2
91210	Interlace option for Model 93200		
93201	12-bit character extension option for Model 93200		
93202	24-bit character extension option for Model 93200		
93221	6-bit characters without interlace, two channels	W + Y (A + B)	1-2
91210	Interlace option for either channel of Model 93221		
93201	12-bit character extension option for Model 93221		
93202	24-bit character extension option for Model 93221		

1.4 The information in this publication relates to the TMCC as utilized with the 925/930/9300 computers. Other publications containing information relating to the TMCC and input/output operation are listed in table 1-2.

Table 1-2. Applicable Publications

Title of Publication	Publication No.
SDS 925/930/9300 TMCC Input/Output Unit Logic Layouts, Current and History	900557
SDS 925 Computer Reference Manual	900099
Model 925 Computer, Technical Manual	900633
SDS 930 Computer Reference Manual	900064
Model 930 Computer, Technical Manual	900066
SDS 9300 Computer Reference Manual	900050
Model 9300 Computer, Technical Manual	900570

1.5 PURPOSE OF OPTION

1.6 The TMCC is a time-multiplexed input/output channel utilized for communication between peripheral devices and the 925/930/9300 computers. Its operation is designated "time-multiplexed" because it gains access to the computer memory through the same path utilized by the computer and must, therefore, momentarily interrupt computation to store or obtain a word of information. Up to four TMCCs may be connected to one computer and all may be active simultaneously but since their operation is time-multiplexed, only one channel at a time communicates with the computer memory.

1.7 DESCRIPTION AND LEADING PARTICULARS

1.8 A computer may have from one to four TMCCs connected to it. These are designated by letter symbols in the order of their installation. When only one

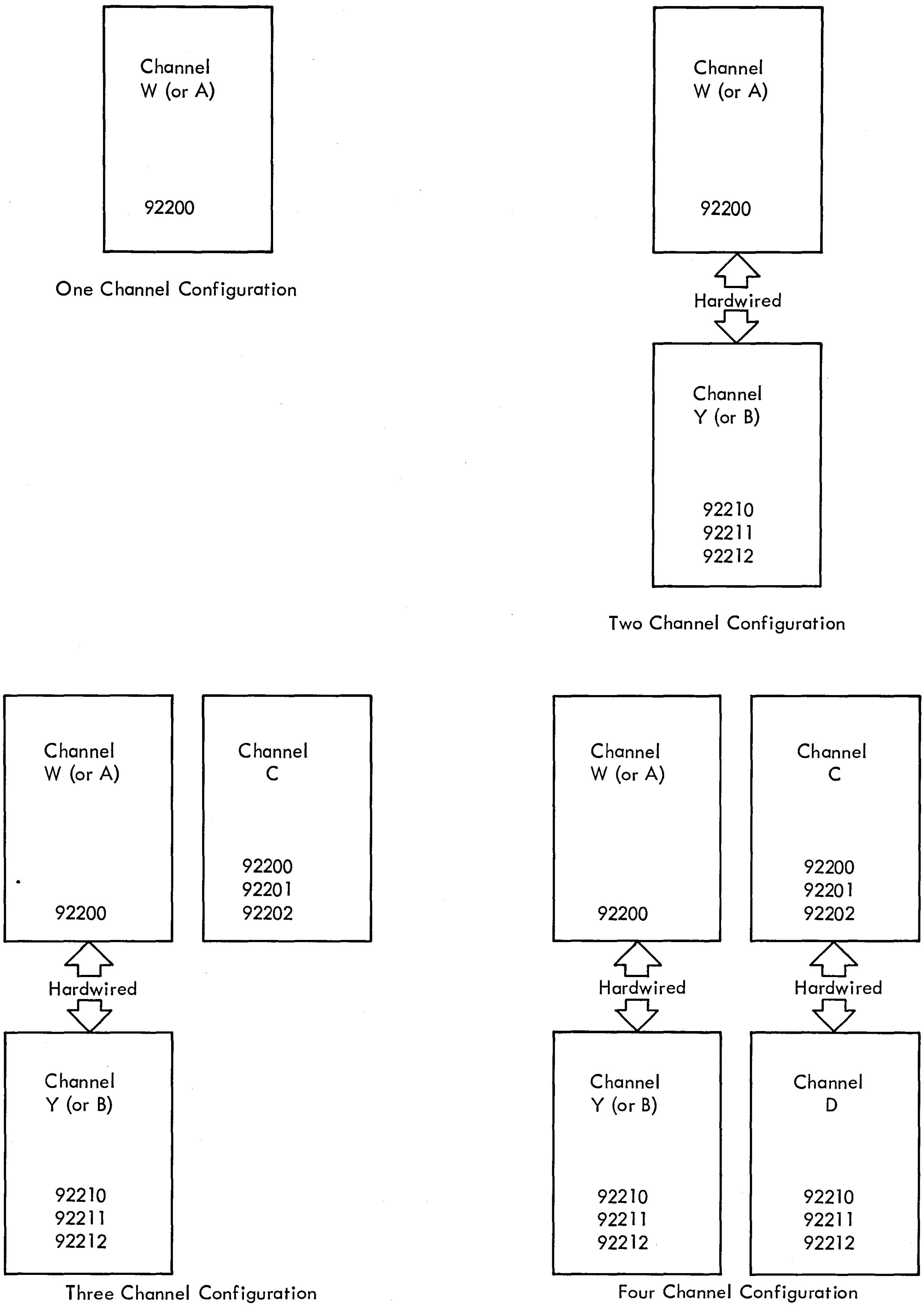
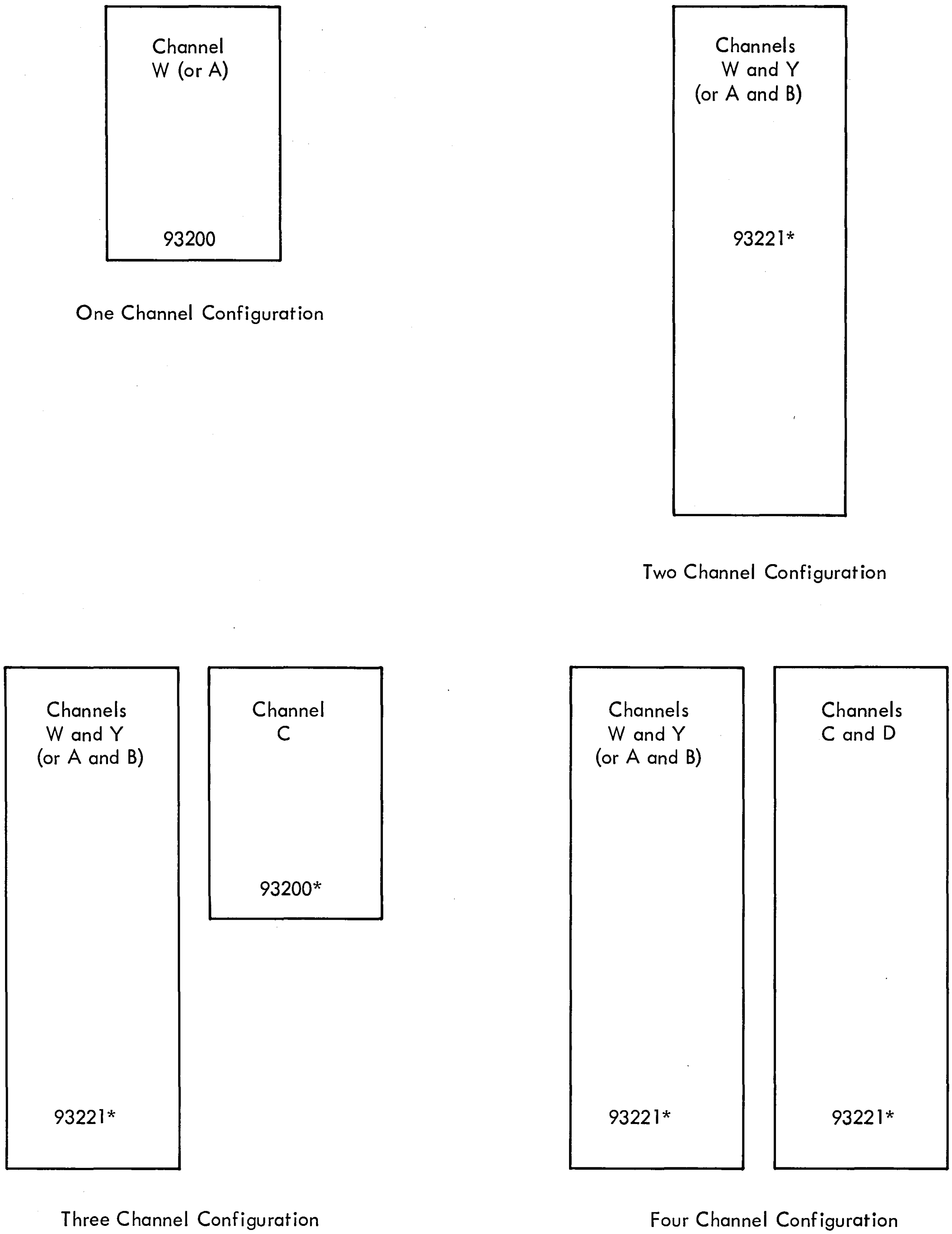


Figure 1-1. TMCC Configuration, Models 922XX



*Note: The Interlace feature, Model 91210, is required on channels B, C and D, and is optional on W, A and Y. All channels may have 93201 or 93202 options.

Figure 1-2. TMCC Configuration, Models 932XX channel is used it is specified as the W channel on the 925 and 930 computers or as the A channel on the 9300 computer. As additional channels are added they are designated, in order, Y (or B on the 9300 computer), C, and D. Because single-word input/output instructions (Memory Into W, Memory Into Y, Memory Into A, W Into Memory, Y Into Memory, and A Into Memory) are not available for all channels, the interlace feature is mandatory on channels B, C, and D.

1.9 Primary differences between the models occur in the hardware layouts, connections between channels, and the options available.

1-10 PHYSICAL DESCRIPTION

1.11 The TMCC consists of plug-in modules contained in chassis consisting of four or six rows of modules. Each row contains 32 connectors thereby allowing the insertion of up to 32 modules in each row. Physical location of each module is given in Section 4 of this manual.

1.12 TMCC Models 922XX

1.13 In TMCC Models 922XX, the character length is fixed for a particular model and the interlace feature is included. One channel must be six bits to allow entering a program into the computer.

1.14 One Channel Configuration

1.15 A one channel configuration TMCC (Model 92200) consists of a single chassis containing four rows of modules (C through F). The quantity and type of modules are listed in table 1-3.

Table 1-3. Models 922XX Module Complement

Item	Description	Model	Quantity					
			92200 6-Bit "W" "A" or "C"	92201 12-Bit	92202 24-Bit	92210 6-Bit "Y" "B" or "D"	92211 12-Bit "Y" "B" or "D"	92212 24-Bit "Y" "B" or "D"
1	Triple Flip-Flop	FB52	19	21	25	18	20	24
2	NAND Flip-Flop	FB54	14	14	14	13	13	13
3	Cable Driver No. 2	AB55	2	2	2	1		
4	NAND No. 2	IB56	5	5	5	5	5	5
5	Band NAND	IB57	4	4	4	4	4	4
6	NAND Module	IB52	2	2	2			
7	Shift Register	DB50	3	3	3	3	3	3
8	Receiver Inverter Buffer	AB53	2	2	2			
9	Termination Module	ZB52	2	2	2			
10	Interface +8 to +4	NB50	1	2	2	1	1	1
11	Cable Driver	AK53	9	10	11	3	1	2
12	Cable Driver	NB52	3	3	3			
13	Termination Module +4	ZB50	7	7	7	7	7	7
14	Termination Module	ZB55	1			1		
15	Receiver, Inverter	AB52	2	2	2			
16	NAND No. 4	IB59	5	5	5	4	4	4
17	Schmitt Trigger	AK54	1	1	1			
18	Termination Module	ZB56		1			2	
19	Termination Module	ZB57			1			2

1.16 Two Channel Configuration

1.17 A two channel configuration TMCC consists of two chassis, one containing four rows of modules (C through F) and the other containing two rows of modules (A and B). These two chassis are physically bolted together and hardwired to allow mounting as a single unit. The two channel configuration consists of a Model 92200 for channel W (or A) and either a six bit option (92210), a twelve bit option (92211) or a twenty-four bit option (92212) for channel Y (B). The options selected determine the quantity and type of modules. Table 1-3 lists the modules required for each model.

1.18 Three Channel Configuration

1.19 The three channel configuration consists of three chassis, two containing four rows of modules and the third containing two rows of modules. Channel W (or A), consists of a Model 92200; channel Y (or B) consists of a six bit option (92210), a twelve bit option (92211), or a twenty-four bit option (92212); channel C consists of a six bit option (92200), a twelve bit option (92201), or a twenty-four bit option (92202). The quantity and types of modules for each option are listed in table 1-3.

1.20 Four Channel Configuration

1.21 The four channel configuration consists of four chassis, two containing four and two containing two rows of modules. The four channel configuration consists of a Model 92200 for channel W (A); a six bit option (92210), a twelve bit option (92211) or a twenty-four bit option (92212) for channel Y(B); a six bit option (92200), a twelve bit option (92201), or twenty-four bit option (92202) for channel C; and a six bit option (92210), twelve bit option (92211), or a twenty-four bit option (92212) for channel D. The quantity and types of modules are listed in table 1-3.

1.22 TMCC Models 932XX

1.23 In TMCC Models 932XX, the interlace registers are optional equipment. Interlace options may be installed in any of the four TMCCs that a 925/930/9300 computer may have. However, channels C and D (and B on the 9300 computer) must have interlace installed since there are no computer instructions allowing use of these channels without it.

1.24 One Channel Configuration

1.25 A one channel configuration TMCC (Model 93200) consists of a single chassis containing four rows of modules. The quantity and types of modules are listed in table 1-4.

1.26 Two Channel Configuration

1.27 The two channel configuration consists of a single chassis containing six rows of modules. For channels W and Y, a Model 93221 TMCC may be used. The Model 93221 may be extended to twelve bit or twenty-four bit characters by addition of modules as listed in table 1-4. The Model 93221 must have the Model 91210 Interlace installed in either or both channels. The modules comprising the Model 91210 Interlace are indicated in table 1-4.

1.28 Three Channel Configuration

1.29 A three channel configuration TMCC consists of a single chassis containing six rows of modules and another chassis of four rows of modules. Channels W and Y (or A and B) are as given in paragraph 1.27. Channel C consists of a Model 93200 TMCC (with character extension options) and must include a Model 91210 Interlace.

1.30 Four Channel Configuration

1.31 A four channel configuration TMCC consists of two chassis, each containing six rows of modules. Two Model 93221 TMCCs may be used with character extension options if desired. Model 91210 Interlace options must be installed on at least channels C, and D (and B on the 9300).

1.32 SEMICONDUCTOR COMPLEMENT

1.33 The semiconductor complement may be derived from the Material Lists and Module Data Sheets contained in Section 6. The module complement for each model of TMCC is contained in tables 1-3 and 1-4.

1.34 INTERLACE FEATURE

1.35 The purpose of the interlace feature is to provide the TMCC with a means of transferring blocks of words without requiring a separate instruction for each word. To do this, two counters are added to the TMCC. One counter is loaded with a count of the number of words in the block, and the other counter is loaded with the address of the memory position of the first word in the block. Then, as each input or output word is transferred to or from memory, the Word Counter and the Address Counter are incremented. The Word Counter holds the one's complement of the count; thus the count is decreased as the counter counts up. In addition to the two counters, the interlace logic also includes Channel Command Interrupt Enables, and all the necessary control logic.

Table 1-4. Models 923XX Module Complement

Item	Description	Model	Quantity 93200 6-Bit "W"	93221 6-Bit "W" & "Y"	93201 12-Bit "W" or "Y"	93202 24-Bit "W" or "Y"	91210 Interlace "W" or "Y"
1	Triple Flip-Flop	FB52	6	11	2	6	13
2	NAND Flip-Flop	FB54	13	25	-	-	1
3	Cable Driver No. 2*	AB55	3	4	-	-	-
4	NAND No. 2	IB56	4	8	-	-	1
5	Band NAND	IB57	3	7	-	-	1
6	NAND Module	IB52	2	2	-	-	-
7	Shift Register	DB50-2	3	6	-	-	-
8	Receiver Inverter Buffer	AB53	2	2	-	-	-
9	Termination Module	ZB52	2	2	-	-	-
10	Interface +8 to +4	NB50	1	2	1	1	-
11	Cable Driver	AK53	9	13	1	2	-
12	Driver Cable Interface	NB52	1	1	-	-	2
13	Termination Module +4	ZB50	6	10	0	0	1
14	Priority Interrupt**	SK61	2	2	-	-	-
15	Receiver Inverter	AB52	2	2	-	-	-
16	NAND No. 4	IB59	3	5	-	-	3
17	Schmitt Trigger	AK54	1	1	-	-	-

*SK61s are located in computer basic interrupt: 925/930 Reference Drawing 107352
9300 Reference Drawing 107626

**One AB55 is located in 5E (930 only) if I/O is used as a "C" or "C-D" channel.

SECTION II
PROGRAMMING

2.1 PURPOSE

2.2 The 925/930/9300 computers include as standard equipment one Time-Multiplexed Communication Channel (TMCC), without interlacing capability, as well as provision for three additional channels. The interlace unit is available as an option. The W and Y channels are available with or without interlace; the C and D channels are available only with interlace. The W channel on the 925 and 930 computers is equivalent to the A channel on the 9300 computer and the Y channel on the 925 and 930 computers ie equivalent to the B channel on the 9300 computer. (The B channel on the 9300 must also have the interlace feature). These channels are capable of automatically controlling the flow of data to and from memory at rates up to one word every 3.5 microseconds. These channels run independently of the central processor and only communicate with it to transfer data to or from memory.

2.3 GENERAL OPERATION

2.4 Utilizing channels W and Y (or A), characters, and words can be transmitted between memory and peripheral devices under the direct control of single instructions. Each of these channels has associated with it two instructions to facilitate direct control operations. For channel W, W INTO MEMORY (WIM) (channel A, A INTO MEMORY (AIM)), causes a word from a peripheral transmission to be taken from the channel W (A) buffer register and placed directly in the specified memory location without disturbing any internal registers. MEMORY INTO W (MIW), (MEMORY INTO A (MIA)), causes a word to be taken from a specified memory location and placed in the channel W (A) buffer register to be read out to the currently operating peripheral device connected to the channel. WIM (AIM) and MIW (MIA) are preceded by instructions from the EOM group that set up the input/output operation. YIM and MIY instructions function in an analogous manner for channel Y. The general test instruction, SKIP IF SIGNAL NOT SET (SKS) provides the facility for testing error indications and/or for testing various peripheral device indicators.

2.5 Additionally, using any channel including channels W and Y (A and B) with interlace, data can be transmitted to and from core storage under channel control. Operation of a channel is initiated by the execution of a sequence of instructions in the central processor. Once started, the channel operates independently of the central processor, automatically transferring each word at the correct time.

2.6 Three instructions control the process of transmitting and receiving data between channel peripheral equipment and the central processor. These instructions are:

EOM	ENERGIZE OUTPUT M
POT	PARALLEL OUTPUT
SKS	SKIP IF SIGNAL NOT SET

2.7 EOM instructions activate one of channels W (A), Y (B), C, or D, to select the peripheral device to be used, and to set up the initial conditions of the data transmission, including the peripheral operation to be performed. An EOM instruction also specifies terminal conditions for an operation.

2.8 PARALLEL OUTPUT (POT) instruction sends out to the channel the number of words in the transmission and the address at which the output begins.

2.9 SKIP IF SIGNAL NOT SET (SKS) instruction can test the Error indicators, End-of-Transmission indicators, and other input/output control indicators, such as printer end-of-form or card hopper empty.

2.10 The general order of use of these instructions for interlaced operation is:

Instruction	Function
EOM	to address the channel, connect the peripheral device, specify various input/output conditions, and alert the optional channel interlace (see Communication Channel Input/Output, paragraph 2.30).
EOM	to specify the terminal conditions and interrupts desired during the transmission
POT	to transmit to the channel a word containing the transmission starting address and block length

Bits 0 through 9 of this latter word contain the ten lower order bits of the word count; bits 10 through 23 contain the 14 bits of the starting address. The second EOM contains the high-order bits of the word count and starting address when needed.

2.11 DIRECT PARALLEL INPUT/OUTPUT

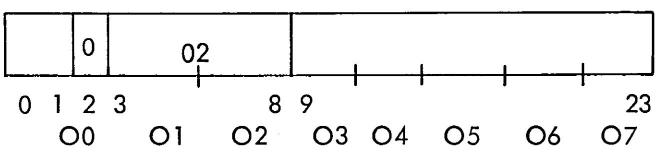
2.12 The direct parallel input/output (POT/PIN) facility allows any word in core memory to be presented, in parallel, at any special system connector or applicable standard peripheral connector; or, conversely, allows signals sent to a connector to be stored in any core memory location. EOM and SKS instructions control parallel input/output operations in the same way as in channel operations. POT/PIN instructions also generate or check for correct parity with each word transmitted.

2.13 SINGLE-BIT INPUT/OUTPUT

2.14 EOM and SKS instructions also perform single-bit input/output and testing for special or standard devices. The execution of an EOM transmits a single signal of approximately 1.4 microseconds duration to an external connector and also provides the connector with a 15-bit address for the destination of this signal. SKS tests whether a similar signal is present on an external connector and skips accordingly.

2.15 PRIMARY INPUT/OUTPUT INSTRUCTIONS

2.16 ENERGIZE OUTPUT M (EOM)



2.17 The major instruction for preparing channel W (or Y, C, D) and an attached peripheral device to perform a data transmission or other peripheral activity is the multi-purpose instruction, ENERGIZE OUTPUT M (EOM). This instruction operates in four distinct modes with many functional configurations. These modes are Buffer Control, Input/Output Control, Internal Control, and System Control. In the third and fourth modes, EOM controls and initiates non-communication channel operations such as special systems transmissions. Each of the frequently used EOM instruction configurations has a mnemonic tag used with standard SDS assemblers. The different modes of operation are program-selectable by the setting of two bits (10, 11 of octal position 3) within the EOM instruction format:

Octal Value	Bit Position 10	Bit Position 11	Area
0	0	0	Buffer Control
1	0	1	Input/Output Control
2	1	0	Internal Control
3	1	1	System Control

2.18 A Buffer Control mode EOM operates essentially as a set-up or preparation facility for data transmissions or other peripheral activities using the channel. The channel to be used, the peripheral unit on that channel, the operation to be performed, and the type of character format to be used are all detailed within this EOM. It also details the use of BCD or binary data transmission, the allowance or not of a leader (as in paper tape), and the direction of operation (as in forward direction for magnetic tape). Execution of such an EOM "connects" the specified peripheral unit to the channel. An EOM in this mode can also alert the interlace, which is the optional, automatic buffer control for input/output.

2.19 An EOM in the Input/Output mode directs peripheral devices to perform non-transmitting operations such as rewind magnetic tape and upspace the printer. This EOM selects certain channel operations such as interrupt response and input/output terminal function desired. It alerts peripheral devices that a PARALLEL INPUT (PIN) or PARALLEL OUTPUT (POT) instruction follows. It also can give an extension of the word count to 15-bits for the number of words to be transmitted and an extension of the address specification to 15-bits. Without disturbing the associated channel, this EOM can also set up the interlace unit. It is with the input/output mode EOM that the user selects his I/O operation as compatible or extended I/O modes.

2.20 This coding sequence initiates such an interlaced channel operation (compatible mode):

Instruction	Function
EOM (Input/Output Control Mode)	Alert the interlace
POT	transmit starting address and block length to interlace
EOM (Buffer Control Mode)	address channel, connect peripheral device, specify various input/output conditions, start transmission

2.21 Initiating an interlaced input/output operation via this sequence of instructions facilitiates checkout by allowing the programmer to single-step through this portion of the program. The first two instructions, EOM (Ioc) and POT, set up the interlace with data address and block length. Therefore, single-stepping through the sequence allows the interlaced channel to complete the input/output operation. When a single EOM (Buffer Control mode) sets up the channel and interlace with a POT instruction following, the programmer cannot step through the sequence since the input/output operation proceeds before the next stepped instruction (POT) places the address and block length in the interlace.

2.22 An EOM in the Internal Control mode enables and disables the interrupt system. EOM in this mode also can prepare the system for the selective arming and disarming of the system interrupt levels. This mode does not directly concern the input/output programmer.

2.23 An EOM in the System Control mode is specifically coded for a given installation and system. Address capability is 15-bits or 32,768 combinations for these special system designations.

NOTE

If an interrupt occurs during the execution of an EOM in any mode, no acknowledgement occurs until the completion of the execution of the instruction following the EOM.

2.24 SKIP IF SIGNAL NOT SET (SKS)

0	0	40(20)			
0	1 2	3 8	9	10 11	12 23

O0 O1 O2 O3 O4 O5 O6 O7

2.25 The principal instruction for testing the states and responses of data channels and their attached peripheral devices, as well as testing internal and external indicators, is the multi-purpose instruction, SKIP IF SIGNAL NOT SET (SKS). SKS is a "skip class" instruction yielding a decision and transfer capability to all channels, devices, indicators, and systems that require it. It operates in four distinct modes: Special Internal Test, Channel and Device Test, Internal Test, and Special System Test. In the second mode, SKS tests channel-oriented, input/output functions. Each of the frequently used SKS instruction configurations has a mnemonic tag, used with SDS assemblers.

2.26 These different modes of operation are program-selectable by the setting of two bits (10, 11 of octal position 3) within the SKS instruction format:

Octal Value	Bit Position 10	Bit Position 11	Area
0	0	0	Special Internal Test
1	0	1	Channel and Device Test
2	1	0	Internal Test
3	1	1	Special System Test

2.27 In the Channel and Device Test mode, SKS tests a channel for channel Ready (not active), interlace Word Count Equal to Zero, and Error. This mode also tests peripheral devices directly. These include testing indicators in a magnetic tape unit such as Beginning-of-Tape, End-of-Tape, File-Protect Ring present, and End-of-File. For example, an SKS instruction might address an indicator within the printer to determine whether the paper is at the End-of-Form.

2.28 In the Internal Test mode, SKS tests whether the interrupt system is enabled or disabled, whether a breakpoint switch is set, and whether Overflow is set.

2.29 In the Special Internal and Special System Test modes, SKS tests signals of special configuration as the specific system requires.

2.30 COMMUNICATION CHANNEL INPUT/OUTPUT

2.31 GENERAL INFORMATION

2.32 SDS Communication Channels provide fully buffered, input/output control and transmission, multiplexed or simultaneous with computation. Up to four data channels can connect to the central processor, all operating independently of each other.

2.33 Each channel can control as many as 30 input/output devices and automatically handles character, word assembly and disassembly, input/output parity detection and generation, data transmission to and from memory, and End-of-Transmission detection.

2.34 All channels are bi-directional and can communicate with 6-bit character devices or word devices of up to 24-bits. In the case of character-oriented devices, the program specifies the number of characters to be contained in each word during the transmission.

2.35 A channel buffer assembles and disassembles data words as they are transmitted between core memory and the peripheral equipment. The buffer maintains control of operations such as characters per word transmitted and direction of peripheral operation (as in magnetic tape forward/reverse).

2.36 A Buffer Control mode EOM sets up the channel buffer for operation. The execution of this EOM sets the operation controls, places the unit address in the buffer, and initiates data assembly/disassembly. The presence of the unit address activates the buffer, causing it to look for data coming from the peripheral device or from memory, as determined by the unit address.

2.37 When in use, a channel interlace controls the transfer of the data words going through the associated channel buffer. This interlace supplies the memory address of data coming from or going to memory and maintains the word count determining the number of words transferred. The terminal interrupts, End-of-Record and Zero Word Count, come from the interlace and are under its control. The interlace controls input/output termination functions during interlaced operation.

2.38 Two EOM instructions and a POT instruction alert and set up a channel interlace. The first EOM alerts the interlace, that is activates the interlace and instructs it to expect a word count and starting address to be sent to it by the POT instruction. The second EOM is an Input/Output mode EOM that specifies the interrupt and the terminal function to be used. This EOM also can specify a 15th address bit and five more high-order word count bits expanding the word count from 10-bits to 15. This sequence is written: EOM (Alert), EOM (I/O), and POT. When the channel buffer is being set up at the same time, the buffer control EOM can alert the interlace. When the buffer is already set up, during a continuing I/O operation, the programmer may use the I/O EOM, ALERT CHANNEL (00250000), to alert the interlace.

2.39 When the programmer does not desire to program the Extended Mode with the input/output terminal functions, interrupts, and additional count or address, only the EOM (Alert) and the POT are necessary to set up the channel interlace (Compatible mode).

2.40 In the Extended Mode, the four channels are programmed in the same way.

2.41 The Time-Multiplexed Channels use the memory logic of the central processor to facilitate input and output of data words. The transfer of each word between a time-multiplexed channel buffer and memory requires two memory cycles. During this time, computation stops in the central processor. Priority for the use of the word input/output logic is in the order: Channel D, C, Y (B), W (A). Any Time-Multiplexed Channel operating with interlace has priority over the central processor for memory access.

2.42 COMMUNICATION CHANNEL DESCRIPTION

2.43 Up to 30 peripheral devices may be connected to one channel. Each of these devices has a unique, two-digit, octal address by which it is selected for an input/output operation. To select the peripheral device, the program loads the proper unit address into the 6-bit Unit Address Register (UAR) in the channel buffer. This address selects both the device and, if appropriate, the function to be performed. Placing a non-zero unit address in the Unit Address Register "connects" the peripheral unit addressed to the channel and it becomes "active". When the UAR contains a zero address, or any time that a terminal or initial condition clears the contents of UAR, the channel is "inactive." The zero in UAR also means that it is not connected to a peripheral unit.

2.44 When the channel and the peripheral unit to be used have been connected, the channel must have information pertaining to the location in memory of the data to be transmitted or received and pertaining to the number of data words in the transfer.

2.45 TIME-MULTIPLEXED CHANNEL REGISTERS

2.46 In the Time-Multiplexed Channels W (A) through D, there are two registers important to the programmer, the Word Assembly Register (WAR) and the Single-Character Register (SCR). The WAR, a 24-bit, word-sized buffer, contains the word of data actively being received or transmitted during an input or output operation. During input, 6-bit characters (plus parity) enter the Single-Character Register where the channel buffer assembles them, one at a time, into the WAR. Then the completed word is placed in memory. Depending on the number of characters per word specified, the word assembled and placed in memory during input has the form:

Word in Memory

One character per word mode

Unpredictable	1st
0 – 17	18 – 23

Two characters per word mode

Unpredictable	1st	2nd
0 – 11	12 – 17	18 – 23

Three characters per word mode

Unpred	1st	2nd	3rd
0 – 5	6 – 11	12 – 17	18 – 23

Four characters per word mode

1st	2nd	3rd	4th
0 – 5	6 – 11	12 – 17	18 – 23

2.47 The unfilled character positions contain unpredictable data. When assembled during a one-word operation, a WIM (AIM) instruction places the word into memory. Under interlace control, the interlaced channel automatically places the word in memory when assembled.

2.48 When the end of an information record is detected by a buffer, the buffer automatically disengages from the device and is then "ready" for another operation. The buffer logic is reset, except that the state of the error indicator is maintained and the last word of the input is still in the word register. If the number of characters in the input record was not a multiple of the number of characters assembled into each computer word, then zeros are automatically forced into the least significant positions of the last word. This last word can then be stored in memory by a BUFFER INTO M WHEN READY WIM (AIM) or YIM instruction after the buffer has disengaged. If the number of characters in the input record was a multiple of the number of characters assembled into each computer word, then the word remaining in the W buffer is either the last group of characters from the input device, if they were not previously transferred to memory by a BUFFER INTO M WHEN READY WIM (AIM) or YIM, or zeros if the last group of characters had been transferred to memory. In either case, it is safe to issue one such instruction after the buffer has disengaged without "hanging up" the computer.

2.49 During output, words come from memory into the WAR where the channel buffer disassembles them into the SCR one 6-bit character at a time. Depending on the characters per word mode specified, the 6-bit characters within the word are output as follows:

Function	Mode
Output one character from bits 0 through 5	One character per word
Output two characters from bits 0 through 5, 6 through 11	Two characters per word
Output three characters from bits 0 through 5, 6 through 11, 12 through 17	Three characters per word
Output four characters from bits 0 through 5, 6 through 11, 12 through 17, 18 through 23	Four characters per word

2.50 As required, the characters are transferred into the One Character Register and output with generated parity. After each character transfer, the word in the WAR is shifted left six bits to be ready for the next transfer. Only those characters needed from each word are used; when required, a new word is brought to the WAR for the next character. For special applications a Time-Multiplexed Channel may be equipped with a 12- or 24-bit One Character Register. The external device which has a character size greater than 6-bits specifies to the channel what its size is, 12- or 24-bits. Standard 6-bit devices are unaffected by the installation of a wider SCR.

2.51 Interlace Registers

2.52 A channel interlace contains two working registers, the Word Count Register (WCR) and the Memory Address Register (MAR). In the set-up sequence -- EOM, EOM, POT -- for an interlaced input/output operation, the POT instruction transmits to the interlace a data word made up of the word count (that is, length) and the starting address of the data block. The 15-bit Word Count Register (WCR) contains the data word count during a data transfer. The number of data words is decremented by one and the new count replaces the old one in the WCR for each word transmitted.

2.53 The count is assembled into the WCR from two places: the least significant 10-bits is from the "POTed" word and the most significant 5-bits is from the "HI COUNT" field of the second EOM. The form of the "POTed" word is:

Word Count	Start Address
0 – 9	10 – 23

2.54 When the word count is equal to zero, the transmission is complete. During output, this causes a termination; during input, the interlace allows any further data to fill the channel buffer and generates the End-of-Word interrupt, if enabled.

2.55 The Memory Address Register (MAR) contains the starting destination or source address in memory of the transmitted data. The memory locations to or from which data words are to be transmitted enter the MAR at the same time the word count does. During transmission of data, the interlace increments the contents of the MAR after each word as it decrements the contents of the WCR. These two registers provide the interlace control of block transmissions. The high-order 15th address bit comes from the second EOM, also.

2.56 COMMUNICATION CHANNEL PROGRAMMING

2.57 The ENERGIZE OUTPUT M (EOM) used in the Buffer Control mode addresses and connects the specified Channel W (A), Y (B), C, or D, and selects the desired unit address. The detailed instruction format is:

0	B1	0	02	I/N	0	0	F/R	L/N	D/B	C/W	B2	Unit
0	1	2	3 – 8	9	10	11	12	13	14	15 – 16	17	18 – 23

Octal digits: O0 (bits 0–2), O1 (bits 3–5), O2 (bits 6–8), O3 (bits 9–11), O4 (bits 12–14), O5 (bits 15–17), O6 (bits 18–20), O7 (bits 21–23)

Bit Designation	Octal Position	Octal Value	Function
B1	O0	2	Bit positions 1 and 17 specify the channel to be activated.
B2	O5	1	Channel W (A) is numbered 00, channel Y (B) is 01, channel C is 10, and channel D is 11.
02	O1-2	02	Bit positions 3 through 8 contain 02, the instruction code for EOM.
I/N	O3	4	A 1-bit in position 9 alerts the buffer interlace.
00	O3	0	Bit positions 10 and 11 contain the EOM mode indicator for the Buffer Control mode.
F/R	O4	4	Bit position 12 specifies the direction in which the peripheral device will operate. A "0" specifies the forward direction. A "1" specifies the reverse direction.
L/N	O4	2	Bit position 13 specifies whether the device should be started with a leader as in paper tape. A "0" specifies a start with leader. A "1" specifies a start without leader.
D/B	O4	1	Bit position 14 specifies the mode of character format. A "0" specifies BCD format. A "1" specifies Binary format.
C/W	O5		Bit positions 15 and 16 specify the number of characters to be assembled into, or disassembled from, each transmitted word. One character per word is specified by 00, two by 01, three by 10 and four by 11.
UNIT	O6-7		Bit positions 18 through 23 specify the unit and the function to be performed with that unit.

2.58 STANDARD EOM CHANNEL INSTRUCTIONS

2.59 Several EOM function configurations have standard uses. These have standard, assembler-type mnemonics and are separate instructions.

2.60 ALERT CHANNEL (ALC)

X	02	50X00
0 2	3 8	9 23

2.61 ALC alerts the channel interlace. This instruction does not disturb the channel buffer in any way. ALC has no effect on W or Y Buffers without interlace. The channel Alerts are:

Mnemonic	Alert Channel	Instruction
ALC 0	W (A)	0 02 50000
ALC1	Y (B)	0 02 50100
ALC 2	C	2 02 50000
ALC 3	D	2 02 50100

2.62 DISCONNECT CHANNEL (DSC)

X	02	00X00
0 2	3 8	9 23

2.63 DSC disconnects the channel. It unconditionally sets the Unit Address Register to 00 regardless of whether the channel is currently addressing a device. This instruction disconnects any device which may be connected to the channel. It also unconditionally makes the channel Ready (Inactive) and clears the Error indicator.

Mnemonic	Disconnect Channel	Instruction
DSC 0	W (A)	0 02 00000
DSC 1	Y (B)	0 02 00100
DSC 2	C	2 02 00000
DSC 3	D	2 02 00100

2.64 ALERT TO STORE ADDRESS FROM CHANNEL (ASC)

X	02	12X00
0 2	3 8	9 23

2.65 ASC alerts an interlaced channel so the PIN instruction that follows can store the contents of the Memory Address Register. This instruction does not affect the operation of the channel.

2.66 ASC is always used in conjunction with PIN to determine the current status of a peripheral operation being performed by the selected channel. The two instructions are written together:

ASC n

PIN m, x

2.67 When the program executes these two instructions, the contents of the effective memory location designated by the PIN instruction are:

Bit Positions	Contents
0 through 8	Zero
9 through 23	Contents of channel's Memory Address Register

Mnemonic	Channel	Instruction
ASC 0	W (A)	0 02 12000
ASC 1	Y (B)	0 02 12100
ASC 2	C	2 02 12000
ASC 3	D	2 02 12100

2.68 TERMINATE OUTPUT OF CHANNEL (TOP)

X	02	14X00
0 2	3 8	9 23

2.69 When the last word of a block enters the channel, TOP terminates channel output. After the execution of this instruction, the following occurs. When the channel buffer delivers the last character to the peripheral device, the buffer disconnects.

2.70 TOP always terminates a non-interlaced channel output operation. It may be used with all communication channels if the particular function selected is terminal function 11 but no further data output is required.

Mnemonic	Terminate Output on Channel	Instruction
TOP 0	W (A)	0 02 14000
TOP 1	Y (B)	0 02 14100
TOP 2	C	2 02 14000
TOP 3	D	2 02 14100

2.71 COMPATIBLE/EXTENDED INPUT/OUTPUT MODES

2.72 The termination of an I/O operation and the interrupts that may be associated with that termination fall into two classes: Compatible and Extended. The choice of one of these two "modes" of input/output operation determines how the system behaves when the termination of an I/O operation occurs.

2.73 Interrupts occurring at the same level (e.g., location 30, 31, etc.) can have difference names (e.g., Count Equal Zero and End-of-Word). These names reflect the different I/O mode in operation when the interrupt occurs. The differences include the timing of interrupt occurrence relative to the I/O operation and type of interrupt requested.

2.74 The Compatible mode of operation for channels W (A), Y (B), C, D is directly compatible with the SDS 900 Computer series modes of I/O operation. The types of interrupts that can be requested are the End-of-Word and End-of-Transmission interrupts.

2.75 The Extended mode for all channels expands the I/O capabilities to include the "terminal functions" discussed below. The types of interrupts that can be requested are the Count Equal Zero and End-of-Record interrupts.

2.76 The I/O mode is selected in the Input/Output EOM via bit 12, the Interrupt Arm bit. A 0-bit makes the system operate in the Compatible mode; a 1-bit sets the system in the Extended mode.

2.77 In particular, the Interrupt Arm (IA) bit determines whether any of the Extended functions operate; that is, a "0" in IA means that the other Extended mode controls, bits 13, 14, 15 and 16, have no effect.

2.78 INPUT/OUTPUT CLASS EOM

2.79 The Input/Output EOM selects the I/O operation mode. When the Extended mode is selected, this EOM also selects (arms) which interrupts are to be operational and selects the desired terminal function. This EOM applies to channels W (A), Y (B), C, and D.

0	B1	0	02/06	0	0	1	IA	ER	ZC	F	C	B2	A	HI Count
0	1	2	3 8	9	10	11	12	13	14	15	16	17	18	19 23

O0 O1 O2 O3 O4 O5 O6 O7

Bit Designation	Octal Position	Octal Value	Function
0			Bit positions 0 and 2 are not used with this EOM.
B1 B2	O0 O5	2 1	Bit positions 1 and 17 specify the channel.
02/06	O1-O2	02	Bit positions 3 through 8 contain 02/06, the instruction code for EOM.
01	O3	1	Bit positions 10 and 11 contain the EOM indicator for the Input/Output control mode.
IA	O4	4	Bit position 12 selects the mode of I/O operation. A "0" specifies the Compatible mode. The operation of bits 13, 14, 15, and 16 are disallowed. Channels W (A), Y (B), C and D operate in this mode which is completely SDS 900 series compatible. If interrupts are required, the user enables the Interrupt System, thus enabling and arming the End-of-Word and End-of-Transmission interrupts. A "1" specifies the Extended mode. All channels can operate in this mode. This allows the use of bits 13, 14, 15, and 16. If interrupts are required, the user arms the associated ones by placing 1-bit in bits 13 and/or 14. The "terminal function" to be used is selected via bits 15 and 16.
ER		2	Bit position 13 controls the arming of the End-of-Record interrupt. A 1-bit arms the interrupt. A 0-bit disarms the interrupt.
ZC		1	Bit position 14 controls the arming of the Zero Word Count interrupt. A 1-bit arms the interrupt. A 0-bit disarms the interrupt.
FC	O5		Bit positions 15 and 16 specify the terminal condition function to be performed with the transmission.
A			Bit position 18 is the high-order address bit.
HI Count			Bit positions 19 through 23 contain the most significant four bits of the 15-bit word count. These positions specify a word count greater than 1023.

NOTE

A 1-bit in 13 and/or 14 does the following:

1. Arms that interrupt during this complete I/O operation; disconnecting this channel disarms the interrupt.

2. Once armed by bits 13 and/or 14, the interrupt can be enabled or disabled by the Enable/Disable feature of the Interrupt System. If a channel generates an extended mode I/O interrupt while the system is disabled, the designated interrupt level goes to the Waiting state. When the program again enables the interrupt system, the interrupt goes to the Active state when its priority allows.

2.80 TERMINAL FUNCTIONS; EXTENDED MODE

2.81 A 2-bit function code in the Input/Output EOM controls the termination of input/output operation in the extended mode. These functions are described below with the letter C representing the specified word count of the transmission.

2.82 INPUT/OUTPUT OF A RECORD AND DISCONNECT (IORD)

2.83 Input

2.84 Read C words. If C equals zero before the End-of-Record is detected, the rest of the record is ignored. At the End-of-R cord, the peripheral device is disconnected and the channel becomes inactive.

2.85 Output

2.86 Write C words. When C equals zero, output is terminated (i.e., the device is signaled that the last characters have been transmitted). When the peripheral device has generated the end of record and, if necessary, checked the validity of the record, it sends an End-of-Record response to the channel buffer. When received by the buffer, the End-of-Record signal generates an End-of-Record interrupt (if armed) and disconnects the channel.

2.87 The line printer generates the End-of-Record response when it completes the printing of a line. If the printer encounters any print errors or faults, it sends a signal to the channel that sets the channel error indicator; this can occur since the printer has not disconnected from the channel. The IORD is useful when the program is to print several lines and the program is not otherwise to use the channel between lines. When the printer completes each line, it causes an End-of-Record interrupt (assumed to be armed), notifying the program that it can immediately transmit the next paper control instruction and the next line image.

2.88 The unbuffered card punch operates similarly. It generates the End-of-Record response after punching each row. If any faults occur during the punching of the entire card, the card punch sends a signal to the channel that sets the channel error indicator; this occurs after punching the last row (row 9).

NOTE

A program should not use IORD with devices that do not have End-of-Record conditions on input (e.g., typewriter) or generate End-of-Record responses upon output termination, (e.g., devices such as the paper tape punch and typewriter). These devices do terminate output but give the program no indication when they receive the last characters.

2.89 INPUT/OUTPUT UNTIL SIGNAL THEN DISCONNECT (IOSD)

2.90 Input

2.91 Read C words. When C equals zero or when the End-of-Record is encountered, the device is disconnected and the channel becomes inactive. If the channel disconnects because of a zero count, an EOR interrupt (if armed) will be generated in addition to the count equal zero interrupt. If both are armed, C=0 will occur first.

2.92 Output

2.93 Write C words. When C equals zero and when the last character has been transmitted, the channel disconnects the device and becomes inactive. If an End-of-Record signal is received before the count reaches zero, the channel will disconnect immediately.

NOTE

The IOSD is designed for use on devices which are normally operated on the basis of the word count only. Typewriters and paper tape devices are of this type, as are the printer and card punch when the user does not wish to stay connected until the operation is complete.

2.94 INPUT/OUTPUT OF A RECORD AND PROCEED (IORP)

2.95 Input

2.96 Read C words. If the channel counts C down to zero before the peripheral device encounters the End-of-Record (EOR), the channel ignores the rest of the record (to the End-of-Record). When the peripheral device sends the End-of-Record signal to the channel, the channel sets its End-of-Record Indicator; this signal sets the End-of-Record interrupt (if armed). The channel does not disconnect. The channel is now in an "Inter-record" condition.

2.97 When the peripheral device is magnetic tape, the tape continues to move when the tape handler encounters the End-of-Record. The End-of-Record occurs when the tape read-heads encounter tape gap; this also causes a Tape Gap signal to "come high". If the program executes a new read tape or scan tape EOM during the inter-gap time (approximately one millisecond while the Tape Gap signal is high), the tape remains in motion and proceeds to read or scan the next record.

If the program executes no such EOM before the Tape Gap signal drops, the channel disconnects and the tape comes to a stop. No additional interrupt occurs. This is the only condition that causes a channel to disconnect automatically.

2.98 All other input devices remain connected until the program takes further action. The paper tape reader remains in motion; the program should issue a "disconnect channel" instruction if the program is not reading any more tape. To proceed after the End-of-Record occurs, the program first executes a Buffer Control mode EOM to re-initialize the Channel Unit Address Register and then reloads the interlace portion of the channel (the program can alert the Interlace via the Buffer Control EOM). Otherwise, the channel immediately terminates any attempt to use its interlace portion since the channel is aware that it is still active and in the End-of-Record condition. When the program continues from an Inter-record condition, the program should use an extended mode terminal function. An IORP should not be used to read devices which do not have EOR signals (e.g., the typewriter and paper tape punch).

2.99 Output

2.100 Write C words. When the channel interlace counts C down to zero, the Interlace notifies the channel buffer that it has received the last word that is to be output; when the buffer outputs this last word, it sends a signal to the connected peripheral device indicating that the device has the last word now. When the peripheral device "receives, outputs and checks the validity of" this last word, it sends an End-of-Record response to the channel buffer. When received by the buffer, the End-of-Record signal generates an End-of-Record interrupt (if armed) and sets the Inter-record indicator; the channel does not disconnect.

2.101 When the peripheral device is magnetic tape, the tape continues to move after it signals End-of-Record. As in reading tape, the signal causes the Tape Gap signal to come high. If the program executes a new write tape or erase tape EOM during the inter-gap time (approximately one millisecond), the tape remains in motion and proceeds to write or erase a new record. If the program executes no such EOM before the Tape Gap signal drops, the channel disconnects and the tape comes to a stop. No interrupt occurs at this time. This is the only condition which causes a channel to disconnect automatically.

2.102 To proceed after the End-of-Record occurs, the program first executes a Buffer Control mode EOM to re-initialize the Channel Unit Address Register and then reloads the interlace portion of the channel (the program can alert the Interlace via the Buffer Control EOM). Otherwise, the channel immediately terminates any attempt to use its interlace portion, since the channel is aware that it is still active and in the End-of-Record condition. When the program continues from an Inter-record condition, the program should use an extended mode terminal function.

2.103 A program should not use IORP with devices that do not generate End-of-Record responses upon output termination; such devices are paper tape and typewriter. These devices do terminate output but give the program no indication when they receive the last characters.

2.104 The IORP should also not be used with the printer and card punch since these devices expect the channel to disconnect after they send EOR.

2.105 INPUT/OUTPUT UNTIL SIGNAL THEN PROCEED (IOSP)

2.106 Input

2.107 Read C words. If the channel counts C down to zero before the peripheral device encounters the End-to-Record, the channel generates a Count Equals Zero interrupt (if armed). The program should reload the interlace portion of the channel to continue reading the record. As far as the peripheral device knows, nothing happens at this time. Failure to reload the Interlace before the peripheral device sends enough characters to overfill the channel buffer causes a rate error; this sets the channel error indicator.

2.108 When the peripheral device encounters the End-of-Record, IOSP operates identically like the IORP command.

2.109 Output

2.110 Write C words. When the channel counts C down to zero, the channel generates a Count Equals Zero interrupt (if armed); the channel does not terminate output. The program should reload the interlace portion of the channel to continue writing in the same record. Failure to reload the Interlace before the buffer transmits all of the characters in its registers and before the peripheral device requests the next character from the buffer results in a rate error; this sets the channel error indicator.

2.111 If the program executes a TERMINATE OUTPUT (TOP) instruction after the channel has counted C down to zero, the channel terminates the output and operates identically like the IORP from this point on.

2.112 CHANNEL AND DEVICE SKS

2.113 The Channel and Device Test mode SKIP IF SIGNAL NOT SET (SKS) tests the indicators in a channel as well as devices attached to it. To test the channel, use unit address 00. The instruction format is:

2.114 CHANNEL TESTS

0	C 2	0	40(20)	C 1	0	1	R	C	E	I	0	C 3	00
0	1	2	3 … 8	9	10	11	12	13	14	15	16	17	18 … 23

Octal digits: O0 O1 O2 O3 O4 O5 O6 O7

Bit Designation	Octal Position	Octal Value	Function
40(20)	O1-O2	40(20)	Bit positions 3 through 8 contain 40(20), the SKS instruction code.
01	O3	1	Bit positions 10 and 11 contain the mode selection.
C1 C2 C3	O3 O0 O5	4 2 1	Bits C1, C2, C3 used as an octal address, specify the channel to be tested. Channel W (A) is 0, channel Y (B) is 1, and so on.
R			Test for ready. A 1-bit selects the test. Skip if Ready or Inactive.
C	O4	2	Test if indicator for Word Count Equal to Zero is set. A 1-bit selects the test. Skip if word count zero.
E		1	Test for error indicator reset. A 1-bit selects the test. Skip if no error.
I	O5	4	Test for Inter-record condition.
00			Bit positions 18 through 23 are zero to specify a channel test. Each of these tests causes a skip when the test condition is true.

2.115 STANDARD SKS INSTRUCTIONS

2.116 Several SKS function configurations have standard uses. These have standard, assembler-type mnemonics and are always used as shown.

2.117 CHANNEL ACTIVE TEST (CAT)

SKIP IF CHANNEL NOT ACTIVE

X	40(20)	14X000
0 … 2	3 … 8	9 … 23

2.118 If the channel is ready to accept a new input/output instruction, the computer skips the next instruction in sequence and executes the following instruction. If the channel is active, or in the process of disconnecting a peripheral unit, the computer executes the next instruction in sequence.

Mnemonic	Channel Active Test	Instruction
CAT 0	W (A)	0 40(20) 14000
CAT 1	Y (B)	0 40(20) 14100
CAT 2	C	2 40(20) 14000
CAT 3	D	2 40(20) 14100

2.119 The following SDS 900 series compatible instructions make the identical test as the above instructions on channels W and Y;

BRTW	0 40 21000	W BUFFER READY TEST
BRTY	0 40 22000	Y BUFFER READY TEST

2.120 The indicator that CAT tests is reset only by the next EOM that connects and alerts the same channel.

2.121 CHANNEL ERROR TEST (CET)

SKIP IF NO ERROR ON CHANNEL

X	40(20)	11X000
0 … 2	3 … 8	9 … 23

2.122 CET tests the error indicator in the channel for being in the set condition. If the error indicator has not been set, the computer skips the next instruction in sequence and executes the following instruction. If the error indicator has been set, the computer executes the next instruction in sequence.

Mnemonic	Channel Error Test	Instruction
CET 0	W (A)	0 40(20) 11000
CET 1	Y (B)	0 40(20) 11100
CET 2	C	2 40(20) 11000
CET 3	D	2 40(20) 11100

2.123 The following SDS 900 series compatible instructions make the identical test of channels W and Y:

BETY	0 40 20020	Y BUFFER ERROR TEST
BETW	0 40 20010	W BUFFER ERROR TEST

2.124 The indicator that CET tests is reset only by the next EOM that connects and alerts the same channel.

2.125 CHANNEL ZERO COUNT TEST (CZT)

SKIP IF CHANNEL WORD COUNT IS ZERO

X	40(20)	12X00
0 2	3 8	9 23

2.126 CZT tests whether the contents of the Word Count Register in the channel have been reduced to zero. If the contents of WCR are zero, the computer skips the next instruction in sequence and executes the following instruction. If the contents of the WCR are non-zero, the computer executes the next instruction in sequence.

Mnemonic	Channel Zero Count Test	Instruction
CZT 0	W (A)	0 40(20) 12000
CZT 1	Y (B)	0 40(20) 12100
CZT 2	C	2 40(20) 12000
CZT 3	D	2 40(20) 12100

2.127 The indicator that CZT tests is reset only by a POT instruction to set up the word count and data address in the same channel.

2.128 CHANNEL INTER-RECORD TEST (CIT)

SKIP IF INTER-RECORD INDICATOR IS SET

X	40(20)	10X00
0 2	3 8	9 23

2.129 CIT tests the Inter-record indicator in the selected channel. If the Inter-record indicator is set, the computer skips the next instruction in sequence and executes the following instruction. If the indicator is reset, the computer executes the next instruction in sequence.

Mnemonic	Channel Active Test	Instruction
CIT 0	W (A)	0 40(20) 10400
CIT 1	Y (B)	0 40(20) 10500
CIT 2	C	2 40(20) 10400
CIT 3	D	2 40(20) 10500

2.130 The Inter-record indicator is set only during extended mode operation when using a Proceed Function; the indicator is set for an inter-record or zero count condition. The indicator is reset by the next alert and connect EOM.

2.131 DEVICE TESTS

2.132 The SKIP IF SIGNAL NOT SET (SKS) below, used in the Channel and Device Test mode, tests the condition of the peripheral devices in the system directly. The peripheral device sections contain the individual instruction descriptions.

0	C 2	0	40(20)	C 1	0	1	Unit Tests	C 3	Unit Address
0	1	2	3 8	9	10	11	12 16	17	18 23

O0 O1 O2 O3 O4 O5 O6 O7

Bit Designation	Octal Position	Octal Value	Function
C1	O3	4	Bit positions 9, 1, and 17 are used as an octal digit to specify the channel.
C2	O0	2	Channel W (A) is 0, channel Y (B) is 1, and so on.
C3	O5	1	
40(20)	O1-O2	40(20)	Bit positions 3 through 8 contain the SKS instruction code.
01	O3	1	Bit positions 10 and 11 contain the mode selection.
Unit Tests	O4-O5		Bit positions 12 through 16 select the particular test and are system dependent.
Unit Address	O6-O7		Bit positions 18 through 23 specify the unit address.

2.133 SINGLE-WORD DATA TRANSFER VIA CHANNELS W (A) AND Y

2.134 INSTRUCTIONS

2.135 Channels W (A) and Y can be programmed as single-word input/output buffers. Data transfer is performed under direct program control or with the aid of the interrupt system. Interlace is not used with these instructions.

2.136 The following two instructions perform data transfer using channel W.

2.137 MEMORY INTO CHANNEL W WHEN EMPTY (MIW)

R	X	0	12	I	M
0	1	2	3 — 8	9	10 — 23

2.138 MIW transfers the contents of the effective memory location into the channel W word buffer. If necessary, the central processor "hangs up" until the buffer is empty and ready to accept the data word.

2.139 The W buffer must be connected to the desired peripheral device by a previous "connect" EOM instruction that selects the buffer, the unit address, and all appropriate control functions.

2.140 CHANNEL W INTO MEMORY WHEN FULL (WIM)

R	X	0	32	I	M
0	1	2	3 — 8	9	10 — 23

2.141 WIM transfers contents of the channel W word buffer into effective memory location. If necessary, the central processor "hangs up" until the buffer is full and ready to deliver the data word.

2.142 MEMORY INTO CHANNEL Y WHEN EMPTY (MIY)

R	X	0	10	I	M
0	1	2	3 — 8	9	10 — 23

2.143 MIY transfers the contents of the effective memory location into the channel Y word buffer. If necessary, the central processor "hangs up" until the buffer is empty and ready to accept the data word.

2.144 CHANNEL Y INTO MEMORY WHEN FULL (YIM)

R	X	0	30	I	M
0	1	2	3 — 8	9	10 — 23

2.145 YIM transfers the contents of the channel Y word buffer into the effective memory location. If necessary, the central processor hangs up" until the buffer is full and ready to deliver the data word.

2.146 MEMORY INTO CHANNEL A WHEN EMPTY (MIA)

I	X	30	M
0	1 2	3 — 8	9 — 23

2.147 The contents of the effective memory location are transferred into the channel A word buffer. The central processor "hangs up" until the buffer is empty and ready to accept the data word.

2.148 CHANNEL A INTO MEMORY WHEN FULL (AIM)

I	X	32	M
0	1 2	3 — 8	9 — 23

2.149 The contents of the channel A word buffer are transferred into the effective memory location. The central processor "hangs up" until the buffer is full and ready to deliver the data word.

2.150 SINGLE-WORD OPERATIONS

2.151 The single-word buffer operations are used in two ways. Data words transfer between the channel and memory under direct program control. The "connect" EOM and the input or output channel instruction are in sequence and the computer "hangs up" until the buffer is ready to perform the transfer. This delay is usually due to buffer tie-up while the buffer is actively transmitting or receiving the previously requested data word.

2.152 Use of the priority interrupt system eliminates the tie-up of the central processor. The interrupt system allows the program to connect the device to be used in the transfer, to enable the interrupt, and then to continue processing in the main program. When the buffer is ready to receive from, or transfer to, memory, the End-of-Word interrupt to the corresponding interrupt location notifies the program that the buffer is Ready. A service routine entered via a BRANCH AND MARK PLACE (BRM) instruction in the appropriate interrupt location processes the interrupt. This routine contains the instruction (MIW or WIM, for example) that can execute immediately without computer tie-up.

2.153 During single-word operations, a parity error or incorrect timing error sets the buffer error indication in the channel. The incorrect timing error occurs when characters enter the buffer during input before the removal of the previous word; during output, buffer error indication occurs if characters are needed for output before the buffer receives the next word. The transmission does not terminate upon detection of any of these errors.

2.154 The interrupt system can detect an End-of-Record termination. During output, use of TERMINATE OUTPUT (TOP) after the final MIW (MIY) causes an interrupt to the appropriate End-of-Transmission location when that final data word has been processed by the buffer. This interrupt takes the place of the End-of-Word interrupt; the End-of-Transmission condition inhibits the End-of-Word interrupt. During input, the End-of-Transmission interrupt is sent to the End-of-Transmission location when the End-of-Record is detected. During input from devices which do not generate an End-of-Record, an EOM disconnects (DSC) the channel to terminate the transmission. This termination generates no End-of-Transmission interrupt.

SECTION III
THEORY OF OPERATION

3.1 GENERAL

3.2 The TMCC communicates with an external system or device by means of a shift register utilizing 6, 12, or 24-bit characters plus a parity bit. The maximum character size depends on the optional registers that may be installed. In TMCC Models 922XX, the character length is fixed at 6, 12, or 24 bits and can not be varied from one size to another. However, TMCC Models 932XX having the larger character length options may be switched from one size to another under control of the external system. The length is selected through activation of one of the character size control lines. External devices may activate these lines as necessary but if none are activated the TMCC assumes 6-bit characters. The rate of information transfer is determined by a clock signal from the external device. For both input and output, the TMCC slaves itself to the clock frequency of the device up to the TMM maximum data rate of two machine cycles per character.

3.3 The TMCC communicates with the computer by means of a 24-bit shift register which transfers words, an octal group at a time, between the TMCC and the computer C Register. The TMCC thus has two registers for data storage. These provide the means to assemble input characters into words or disassemble words into output characters. The number of characters per word is under program control but is limited to a maximum of four 6-bit characters, two 12-bit characters, or one 24-bit character.

3.4 Information may be input or output by executing an instruction for each word (channels W (A), or Y, only). The instruction may be given in advance of the time it is needed, in which case the computer remains idle until the channel is ready. Or the computer interrupt system may be employed so that the channel can call for an instruction when it is ready to use it. This allows the computer to continue with other computations when not actually engaged in the input/output (I/O) process.

3.5 An optional interlace feature may be installed in the TMCC to facilitate I/O operations with fewer instructions. The interlace logic allows a program to designate to the TMCC how many words are to be transferred and the memory location of the first word. Then, without further instructions, the TMCC can assemble or disassemble the number of words specified and time-share with the computer each time it is ready to transfer a word to or from memory. The I/O process may thus be interlaced with computation or with similar I/O operations on other channels.

3.6 Figure 3-1 is a block diagram of the TMCC. As indicated on the figure, the principal parts of the TMCC are the Character Buffer, Word Assembly Register, Unit Address Register, Word Counter, and Address Counter.

3.7 CHARACTER BUFFER

3.8 Depending on the option, the Character Buffer is a single character storage register of 6, 12, or 24 bits. It is implemented with S-R type flip-flops connected in a series-parallel manner so shifting takes place in octal groups (i.e. three bits in parallel). Transfer of data between the Character Buffer and an external system is entirely parallel for the whole character whether it be input or output.

3.9 WORD ASSEMBLY REGISTER

3.10 This register is also connected in series-parallel to allow shifting in octal groups. It is composed of three parallel registers of eleven flip-flops each. The register includes twenty-four flip-flops to store a complete word plus additional flip-flops on the ends of each series string to allow for timing considerations. The Word Assembly Register is implemented with flip-flops connected in such a manner that continuous recirculation occurs.

3.11 UNIT ADDRESS REGISTER

3.12 The 6-bit address code to select a specific peripheral device is set-up in the Unit Address Register. The register is composed of five flip-flops whose outputs are sent to the peripheral unit for decoding. A sixth flip-flop, associated with the Unit Address Register, is also set-up at the same time to signal the external device whether an input or an output is to take place.

3.13 WORD COUNTER

3.14 The Word Counter is part of the optional interlace equipment. It is a fifteen stage flip-flop counter used to store the number of words to be transferred during an interlaced I/O operation. With each word transfer, the counter is decremented by "one". (Actually, the complement of the count is incremented.)

3.15 ADDRESS COUNTER

3.16 This counter is also part of the optional interlace feature. Its purpose is to store the address of the d memory location currently being accessed. Each time a word is taken from or sent to memory, the Address

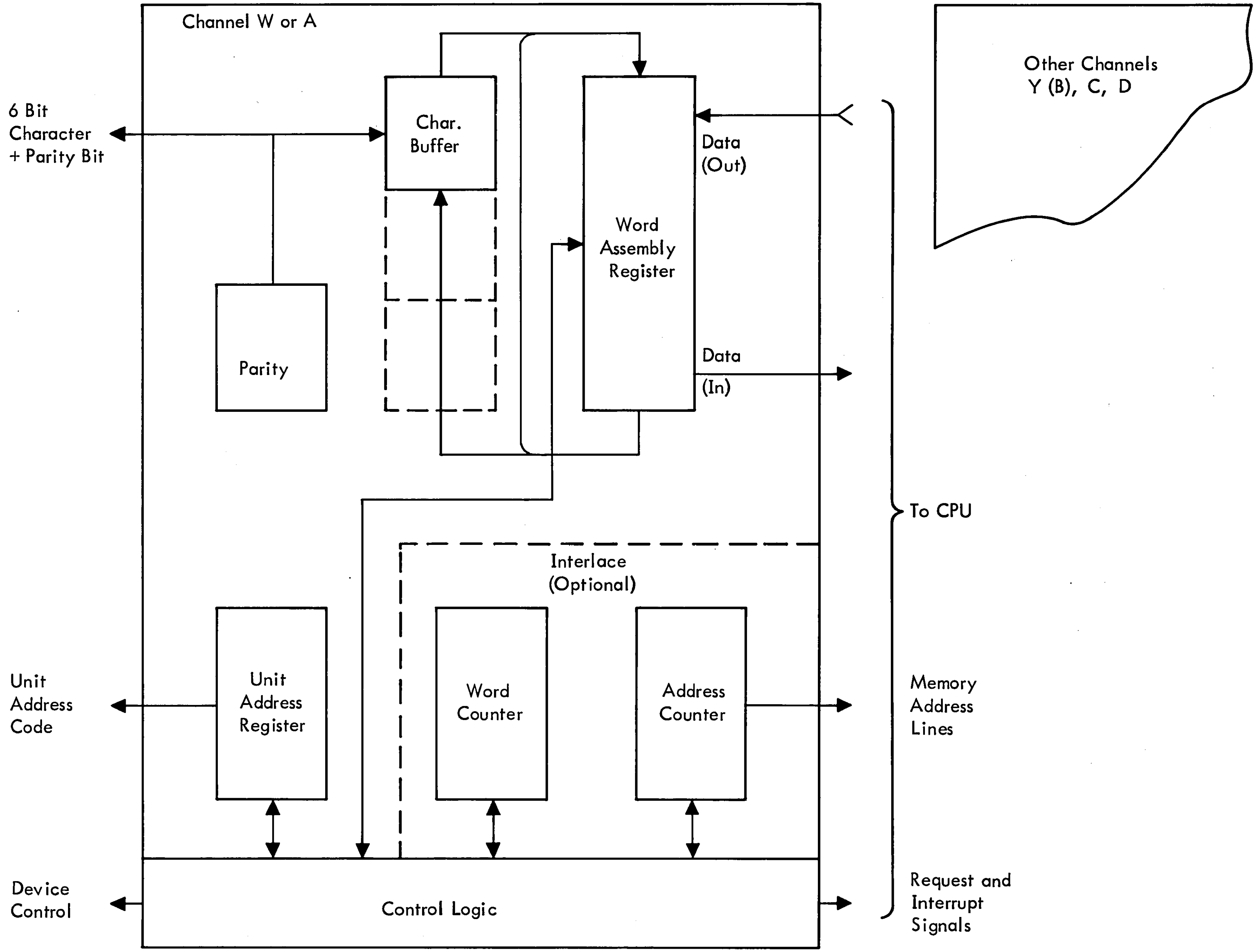


Figure 3-1. Time Multiplexed Communication Channel With Interlace, Block Diagram

Counter is incremented by "one" to prepare for locating the next word.

3.17 INPUT PROCESS

3.18 A brief outline of a non-interlaced input process follows. The TMCC is initialized by an EOM instruction to set-up the address code of the peripheral device, to designate input or output, and specify the number of characters per word. When the address is decoded by a peripheral device, the device is activated and begins sending clock signals and data to the channel.

3.19 Input clocks are synchronized with TMCC timing by clock counter flip-flops which detect the peripheral device clock, transfer the input data to the Character Buffer and cause the Word Assembly Register to circulate through the Character Buffer. Ordinarily the Word Assembly Register recirculates on itself but as each new input character is ready it circulates through the Character Buffer for one machine cycle to pick up the new character. A machine cycle is defined as eleven computer clock pulse periods.

3.20 As each character is clocked in, the character counter (W7 W8) is decremented until the count reaches zero, signaling that a complete word has been formed. Depending on the particular channel (TMCC W (A) or Y) a WIM, AIM, or YIM instruction may be used to transfer the word from the TMCC to memory. When the instruction is executed, a word is shifted in octal groups from the Word Assembly Register to the computer C Register and then stored in the memory location specified by the effective address of the WIM, AIM, or YIM instruction.

3.21 To prepare for the next word, the Character Counter is reset to its original count which was designated by the initializing EOM instruction. Storage of the original count is accomplished by utilizing excess positions of the Word Assembly Register.

3.22 The input process may be terminated by another EOM instruction or by detection of an externally applied halt condition.

3.23 OUTPUT PROCESS

3.24 A non-interlaced output process is started in the same way that an input operation is initialized. A MIW (MIY or MIA) instruction can then be used to transfer words from memory to the Word Assembly Register via the computer C Register.

3.25 Each time the external device sends a clock signal to the TMCC, it is detected by the Clock Counter. At a certain point in the counter sequence, the device extracts information from the Character Buffer. At the end of the counter sequence, the Word Assembly Register recirculates through the buffer for one machine cycle. At the conclusion of the cycle, a new character is available in the Character Buffer awaiting the next clock. The Clock Counter also decrements the Character Counter. When it is decremented to zero, the last character of a word is in the buffer. By this time another MIW (MIY or MIA) instruction should be executed; or the instruction may be called for through the interrupt system. As with input, the Character Counter is reloaded between words from the Word Assembly Register.

3.26 The output operation is concluded by a Terminate Output EOM instruction.

3.27 Parity

3.28 During input, a parity flip-flop accepts the input parity bit and checks the character for odd parity. The same flip-flop is also used to generate the parity bit for output characters.

3.29 TMCC AND INTERLACE CONFIGURATION

3.30 The theory of operation contained in this manual is applicable to all models of the Time-Multiplexed Communication Channels for the 925/930/9300 Computers. The operation is for the most part identical for all models. Those differences that do exist, however, are covered in the explanation where appropriate.

3.31 DETAILED DESCRIPTION

3.32 Many portions of the TMCC logic are common to both input and output operations. Other portions of the logic are specifically related to input only, output only, or interlace only. The following logic description begins with the common logic functions.

3.33 Subsequent to the logic descriptions are the Glossary of Logic Term and the Logic Equations.

3.34 PULSE COUNTER

3.35 The pulse counter consists of flip-flops Qr1, Qr2, Qr3, and Qr4. These flip-flops perform the same function for the TMCC that the pulse counter, Q1 through Q6, does for the central processor (CPU). The counter is included in the TMCC in addition to the counter in the CPU in order to avoid excessive delays and loading that would occur if all timing signals were obtained directly from the CPU. The Pulse Counter defines the pulse times, T8, T7, T6, T5, T4, T3, T2, T1 T0, Tr, and Tp needed for timing of all processes within the unit. Refer to table 3-1 for the Pulse Counter Truth Table.

Table 3-1. Pulse Counter Truth Table

	Qr1	Qr2	Qr3	Qr4
Tp	0	0	0	0
T8	1	0	0	0
T7	1	0	0	1
T6	1	1	1	1
T5	0	1	1	1
T4	0	0	1	1
T3	0	0	1	0
T2	1	0	1	0
T1	1	1	1	0
T0	0	1	1	0
Tr	0	0	0	0
Tp	0	0	0	0

3.36 It is logically impossible to set Qr2, Qr3, and Qr4 unless Qr1 has been previously set. Therefore, without the additional set signal provided by Tpc, the counter would soon reach the reset state of time Tr + Tp and then stop counting. However, Tpc, the Tp signal from the CPU, is used to advance the TMCC pulse counter from Tp to T8. Thus, both counters advance to T8 at the same time and both remain in synchronism. An examination of the logic also indicates that the two pulse counters will synchronize regardless of the turn-on state.

$$sQr1 = Tpc + \overline{Qr2}\ Qr3\ \overline{Qr4}$$
$$rQr1 = Qr2$$

$$sQr2 = Qr1\ \overline{Qr2}\ Qr4\ (Qr4 + T0) + Qr1\ Qr3$$
$$rQr2 = \overline{Qr1}$$

$$sQr3 = Qr1\ Qr4$$
$$rQr3 = Qr3\ \overline{Qr4}\ (Qr4 + T0)$$

$$sQr4 = Qr1\ \overline{Qr3}$$
$$rQr4 = \overline{Qr1}\ \overline{Qr2}$$

Only those pulse times or combinations of pulse times that are need for timing in the TMCC are decoded. For example:

$$T0 = \overline{Qr1}\ Qr2\ \overline{Qr4}$$

$$T6 - T0 = Qr3$$

3.37 In examining the pulse counter and the T0 decoding logic, it appears that the term (Qr4 + T0), as used on the inputs of Qr2 and Qr3, contains redundant logic. This is a result of logic mechanization and the redundant terms are not significant to the counter operation.

3.38 A TMCC pulse counter is associated with each W and C channel. The Y and D channels share the same pulse counters as the W and C channels, respectively. Other logic is shared in a similar manner by two channels and will be noted as each case arises.

3.39 INPUT/OUTPUT PROCESSING

3.40 When an EOM instruction of the form, EOM-0XXXX or EOM4XXXX, is executed to start an input or output process, a Buffer Control Signal, Buc, produces a clear signal, Wc, and a set signal, Ws. These two signals, Wc and Ws, permit initialization for the input/output operation. The Unit Address and the Character Count are set up from the C-Register. The registers are first cleared by Wc and then set by Ws. Refer to figure 3-2.

$$Buc = Eom\ \overline{C10}\ \overline{C11}\ \overline{C1}\ *$$

$$Wc = Buc\ \overline{C17}\ (T6 + T5) + St + \ldots$$

$$Ws = Buc\ \overline{C17}\ (T3 - T0)$$

*C1 is used in place of $\overline{C1}$ for Channels C and D. Similarly, C17 and $\overline{C17}$ distinguish between the W and Y channels, or between the C and D channels.

(T6 + T5) and (T3 - T0) are decoded timing signals from the pulse counter. Frequent use is made of such pulse times throughout the manual without further explanation. The term $\overline{C17}$ distinguishes enabling of the W channel rather than the Y channel. The combination of terms which make up the input of Buc indicate that the computer is in phase (Ø) 5 of the execution of an EOM Buffer Control instruction. The term, St, is produced by the start switch which may also be used to reset the TMCC. The register logic involved in the clear and set sequencing is:

$$sW14 = Ws\ C23$$
$$rW14 = Wc$$
$$\vdots$$
$$sW11 = Ws\ C20$$
$$rW11 = Wc$$

$$sW10 = Ws\ C19 + \ldots$$
$$rW10 = Wc$$

Unit Address Register: 5-bits provide 31 addressing codes and a disconnect code.

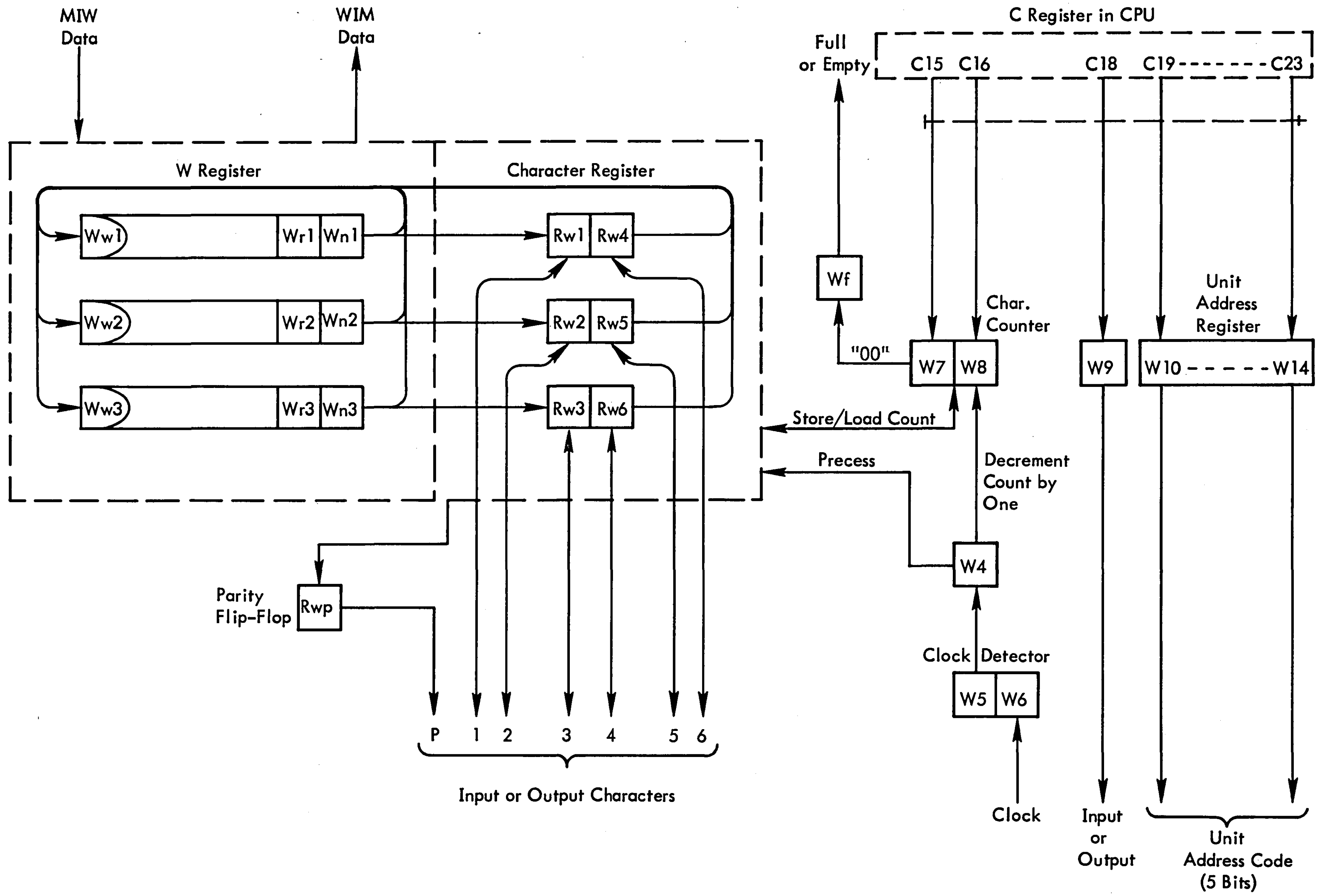


Figure 3-2. TMCC Information Flow Diagram, Input/Output (6 bit)

sW9 = Ws C18 W9 = 1 for output

rW9 = Wc W9 = 0 for input

sW8 = Ws C16 + . . .

rW8 = Wc + . . .

sW7 = Ws C15 + . . .

rW7 = Wc + . . .

Character Counter

W7	W8	Characters/Word
1	1	4
1	0	3
0	1	2
0	0	1

3.41 At the end of the Buc type instruction and during the last pulse time (T0) that Ws is on, the flip-flop, W4, is set on for three pulse times.

sW4 = Ws T0 + . . .

rW4 = W4 T8 + . . .

During this time, W4 allows the contents of the character counter to be copied into the W-Register. The bit in W7 goes into Ww1 and the bit in W8 goes into Ww2.

$$Ww1 = W4\ W7\ \overline{(T7 - T0)} + \ldots$$

$$Ww2 = W4\ W8\ \overline{(T7 - T0)} + \ldots$$

During this period, $\overline{W4}$ or timing singals inhibit the other inputs to the W-Register.

3.42 This process provides a means for the TMCC to remember the initial character count while using flip-flops W7 and W8 to perform the actual count-down of the characters as each word is assembled on input or disassembled on output. As a word is processed, the original count is reloaded into the counter to get ready for the next word.

$$sW8 = Wxx\ Wn2\ \overline{(T7 - T0)}\ \overline{W4}$$

$$sW7 = Wxx\ Wn1\ \overline{(T7 - T0)}\ \overline{W4}$$

The term Wxx is true during the transmission of a word being processed. Thus, in addition to its normal word handling functions, the W-Register provides storage of the character count for W7 and W8.

3.43 W-Register

3.44 The W-Register is a one word recirculating flip-flop register with additional flip-flops at the read and write ends. The Write input signals to the first flip-flops of the register are designated Ww-, the intermediate Read flip-flops are designated Wr- and these drive the last flip-flops which are designated Wn-. The n represents now.

3.45 During normal recirculation, the outputs of the n flip-flops are fed to the w inputs, which, in turn, feed the remaining serial shift circuits. There are a total of eleven stages in a recirculating loop, one for each pulse time of a machine cycle. Three recirculating loops are required to hold a 24-bit word. The first recirculating loop holds only the most significant bits of each of the eight octal digits in a word. The second recirculating loop holds the middle bits of the eight octals. The third recirculating loop holds the least significant bits of each of the eight octals. If the octal word 07030407 (000 111 000 011 000 100 000 111) were being held in the register, its bits at pulse time Tp would appear as follows:

→ C 0 1 0 0 0 1 0 1 C C →

C = Character Count

→ C 0 1 0 1 0 0 0 1 C C →

X = Irrelevant

→ X 0 1 0 1 0 0 0 1 X X →

At the next pulse time, T8, all bits would be moved one bit position to the right and for succeeding pulse times as the register recirculates. At the least significant pulse time, T7, the bits of the least significant octal digit are in their respective now flip-flops, Wn1, Wn2, and Wn3. At succeeding pulse times the now flip-flops present the corresponding octal digits. The additional positions beyond the eight octals of the register act as fill-in bits to satisfy logic timing requirements (so that a word is back in its original position after one machine cycle of 11 clock pulses) and are also used to store the character count. Normal recirculation is allowed by the following logic:

$$Ww1 = \overline{W4}\ Wn1\ \overline{Wxx} + \ldots$$

$$Ww2 = \overline{W4}\ Wn2\ \overline{Wxx} + \ldots$$

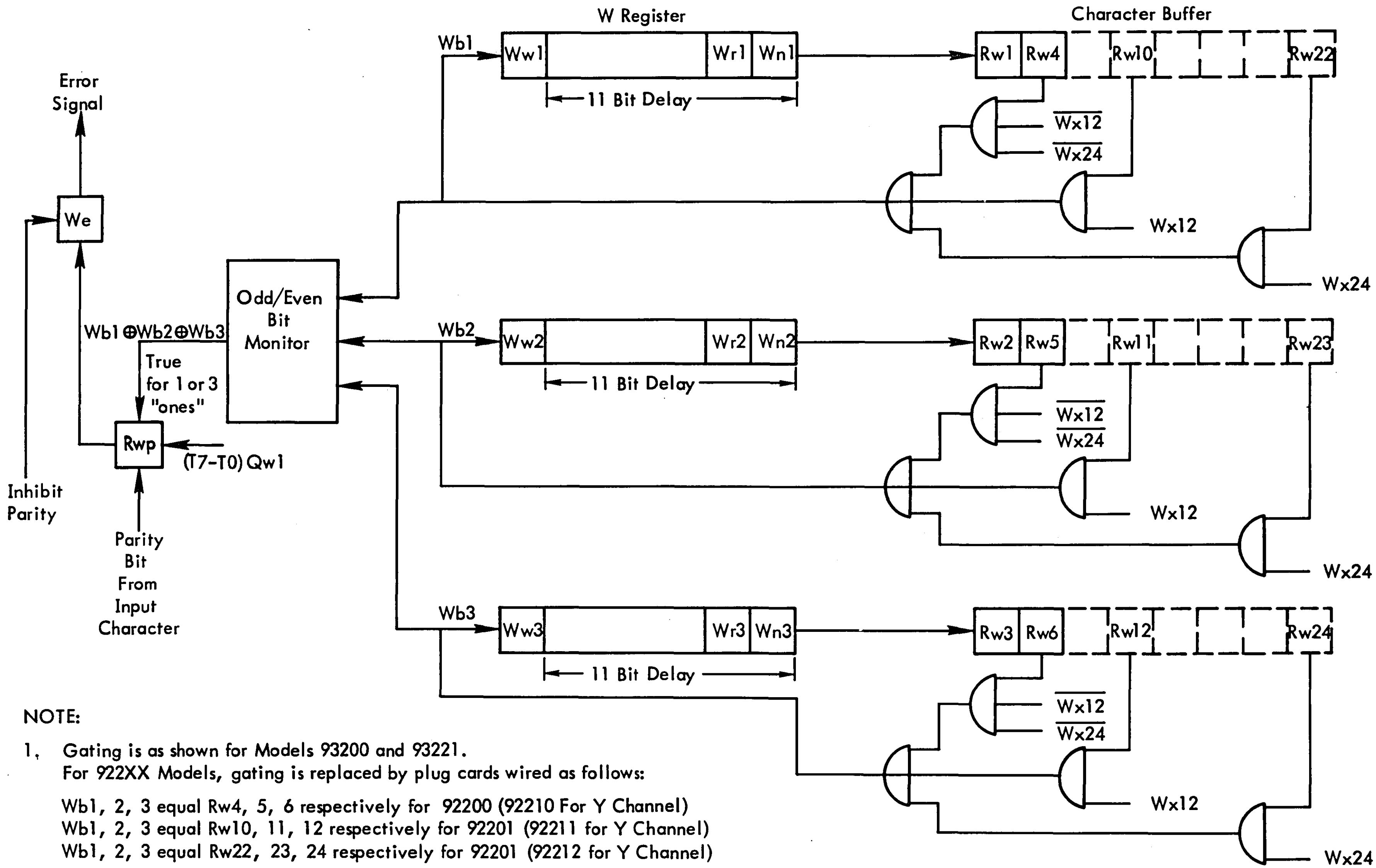
$$Ww3 = \overline{W4}\ Wn3\ \overline{Wxx} + \ldots$$

$\overline{W4}\ \overline{Wxx}$ indicates the W-Register is not participating in some other operation.

3.46 The Character Register is composed of six, twelve, or twenty-four R-S type flip-flops. When shifting an input character from the Character Register into the W-Register or an output character from the W-Register to the Character Register, W4 is set for the period (T7 - T0) of one machine cycle. This enables the gating of one character precession in the W-Register by causing the data in the W-Register to recirculate through the Character Register. Refer to figure 3-3.

$$Ww1 = W4\ Wb1\ (T7 - T0) + \ldots$$

$$Ww2 = W4\ Wb2\ (T7 - T0) + \ldots$$



NOTE:

1. Gating is as shown for Models 93200 and 93221.
   For 922XX Models, gating is replaced by plug cards wired as follows:

   Wb1, 2, 3 equal Rw4, 5, 6 respectively for 92200 (92210 For Y Channel)
   Wb1, 2, 3 equal Rw10, 11, 12 respectively for 92201 (92211 for Y Channel)
   Wb1, 2, 3 equal Rw22, 23, 24 respectively for 92201 (92212 for Y Channel)

2. Wx12 and Wx24 are signals derived from the peripheral device to select the I/O character size. If the device does not designate a character size then $\overline{Wx12}$ and $\overline{Wx24}$ are true and Wx12 and Wx24 are false.

Figure 3-3. Precession Loop and Input Parity Checking Logic

$$Ww3 = W4\ Wb3 + \ldots$$

$$sRw1 = W4\ \overline{Wxx}\ (T7 - T0)\ Wn1 + \ldots$$
$$rRw1 = W4\ \overline{Wxx}\ \overline{Wn1} + \ldots$$

$$sRw2 = W4\ \overline{Wxx}\ (T7 - T0)\ Wn2 + \ldots$$
$$rRw2 = W4\ \overline{Wxx}\ \overline{Wn2} + \ldots$$

$$sRw3 = W4\ \overline{Wxx}\ (T7 - T0)\ Wn3 + \ldots$$
$$rRw3 = W4\ \overline{Wxx}\ \overline{Wn3} + \ldots$$

Wxx is a signal denoting that an MIW, WIM or Time Share operation is occurring.

$$Wxx = Rx\ Pwy + \ldots *$$
$$Pwy = 05\ **$$

*Rx is always false for the C-channel. Another term, not shown allows Wxx to function in that channel only on an interlaced basis.

**In Model 92200. See 05, Pw5 in the Glossary of terms.

3.47 The Time Share Operation is discussed beginning with paragraph 3.102. Since there are no WIM/MIW type instructions for TMCC-B, C, or D, Rx is always false for these channels.

3.48 The timing signals (T7 - T0) on the inputs of Ww1 and Ww2 are necessary to prevent interference with the storage of the character count which was previously described. The character count does not precess but recirculates. This recirculation is allowed by:

$$Ww1 = \overline{W4}\ Wn1\ (\overline{T7 - T0}) + \ldots$$
$$Ww2 = \overline{W4}\ Wn2\ (\overline{T7 - T0}) + \ldots$$

3.49 During the input or output precession, the shift logic for the character register is as shown below. Depending on the 12- or 24-bit character option, all bits may not be installed.

$$sRw4 = W4\ \overline{Rw4}\ Rw1 + \ldots$$
$$rRw4 = W4\ Rw4\ \overline{Rw1} + \ldots$$

$$sRw5 = W4\ \overline{Rw5}\ Rw2 + \ldots$$
$$rRw5 = W4\ Rw5\ \overline{Rw2} + \ldots$$
$$\vdots$$
$$sRw23 = W4\ \overline{Rw23}\ Rw20 + \ldots$$
$$rRw23 = W4\ Rw23\ \overline{Rw20} + \ldots$$

$$sRw24 = W4\ \overline{Rw24}\ Rw21 + \ldots$$
$$rRw24 = W4\ Rw24\ \overline{Rw21} + \ldots$$

The shift inputs for Rw1, Rw2, and Rw3 are given in paragraph 3.46. The precession of characters is controlled by W4. When a WIM or MIW instruction is executed, Wf is set. Wf remains set until the count in W7 and W8 is 00.

$$sWf = Rx\ T0\ Twy$$
$$rWf = \overline{W7}\ \overline{W8}\ W4\ (T6 + T5)$$

Rx Pwy = Wxx which indicates a WIM or MIW instruction is occurring. Wf is later used to indicate to the computer when the W-Register is full on input or empty on output.

3.50 Two other flip-flops, W5 and W6, detect external device clocks (which may occur either before or after Wf is set). The clock Ecw is first detected by W6 as follows:

$$sW6 = \overline{W5}\ Ecw\ T8\ \overline{\overline{W10}\,\overline{W11}\,\overline{W12}\,\overline{W13}\,\overline{W14}}$$
$$rW6 = W4\ T0 + Wc$$

At the next T0 pulse after the device clock goes false, W5 sets allowing W6 to reset again. Setting of W5 inhibits further clock detection until the current clock is processed.

$$sW5 = \overline{W5}\ W6\ \overline{Ecw}\ T0 + \ldots$$
$$rW5 = W4\ T0 + \ldots$$

Setting of W4 is interlocked with W5 and Wf to allow one precession of the W Register to take place after each external clock signal.

$$sW4 = W5\ Wf\ T8\ \overline{Wg} + \ldots$$
$$rW4 = W4\ T0 + \ldots$$

The term, $\overline{Wg}$, explained in detail in paragraphs 3-66 and 3-150) is assumed to be true at this time.

3.51 The equation for Wf contains $\overline{W7}\ \overline{W8}$, indicating that precession is complete when the character count reaches 00. The count down is enabled by W4 and is accomplished by:

$$sW8 = W7\ \overline{W8}\ W4\ T0 + \ldots$$
$$rW8 = W8\ W4\ T0 + \ldots$$
$$rW7 = W7\ \overline{W8}\ W4\ T0 + \ldots$$

3.52 The foregoing discussion was limited to processes common to input and output operations. The interrupt function, which allows the TMCC to signal the computer when it is ready to transfer a word to or from memory, was omitted. In subsequent paragraphs, features peculiar to input or output operation are discussed separately. Details concerning interrupt operation are included.

3.53 INPUT PROCESS (W9 true)

3.54 The characteristics of a typical input clock signal and its relationship to the input data and Clock Counter flip-flops are illustrated in figure 3-4. Examination of figure 3-4 indicates that if the data is to be sampled by $W6\ \overline{W5}$ it has to be on by the time the clock, Ecw, returns to zero volts. Also, in order not to be read by the previous or next clock, the data may not come on until at least one machine cycle after the previous clock and must go off before the next clock appears.

3.55 Two detailed examples of the clock signal, Ecw, are illustrated in figure 3-5. To be assured of a timing pulse occurring during the on period (to set W6) and the off period (to set W5) of Ecw, each of these periods must be at least one machine cycle in length. This prescribes an input clock cycle of no less than two machine cycles. The clock rate must be somewhat slower than this for proper operation of W6, W5, and W4. Figure 3-5a illustrates two input clocks with timing such that the second clock is missed. Any clock rate slower than that illustrated in figure 3-5a would be satisfactory, however, a safety margin must be provided to compensate for noise and variations in waveshape and frequency.

3.56 The input frequency may be increased as illustrated in figure 3-5b if the clocks are interlocked within the peripheral device with W5 and W6 from the TMCC such that

$$\text{Ecw} = \overline{\text{(Device Clock)}\ \overline{W5}\ \overline{W6}}$$

In this case, only two machine cycles per input clock are needed. Some of the peripheral device couplers include this interlocking feature.

3.57 When a Buc type EOM instruction is executed to activate the TMCC for an input operation, the halt detector, Wh, is reset and the computer interlock flip-flop, Wf, is set by the clearing signal, Wc.

$$Wc = Buc\ \overline{C17}\ (T6 + T5) + - - -$$

$$sWf = Wc\ \overline{Wh} + \ldots$$

$$rWh = Wc\ (T6 + T5) + \ldots$$

This prepares the Character Register to precess the first input character into the W- Register enabling W4 which gates Ww1, Ww2 and Ww3.

3.58 The Character Register and parity flip-flop are cleared originally and again between each input character by $\overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$. After processing the Buc type EOM instruction, the Character Register is ready to receive an input character and clock even though a WIM instruction is not immediately given. The input bits, Zw1 through Zw24 and the parity bit Zwp, are gated into the Character Register and the Parity Flip-Flop by $\overline{W9}\ W6\ \overline{W5}$. $\overline{W9}$ signifies an input operation and $W6\ \overline{W5}$ indicate an input clock has been detected from the peripheral device.

$$sRw1 = \overline{W9}\ W6\ \overline{W5}\ Zw1$$

$$rRw1 = \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$$

$$\vdots \qquad \vdots$$

$$sRw24 = \overline{W9}\ W6\ \overline{W5}\ Zw24$$

$$rRw24 = \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$$

$$sRwp = \overline{W9}\ W6\ \overline{W5}\ Zwp$$

$$rRwp = \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$$

3.59 Precession then takes place as described earlier and another input character can be read into the Character Register. This read-precess cycle is repeated for each input character until the Character Counter is decremented to 00 causing Wf to reset. Resetting of Wf inhibits further precessions and indicates to the computer that the W-Register is full and ready to transfer a word into memory. The program should now provide a WIM instruction to enable the transfer. One more character may still be stored in the Character Register before receiving the WIM instruction. Further input characters are blocked because W4 is inhibited while Wf is reset. This prevents W5 from resetting, which in turn disables clock detection by W6. When a WIM instruction does occur late, The Error Detection Flip-Flop, We, is set. This condition can be tested by an SKS instruction. The error detection flip-flop is reset by Wc which occurs with an EOM-Buc instruction.

$$sWe = W0\ \overline{W6}\ W5\ Ecw\ T8 + \ldots$$

$$rWe = Wc\ \overline{Wh}$$

This equation signifies that a WIM instruction is late if the clock signal, Ecw, is received before the previous character has been precessed out of the Character Register. The W0, Halt Interlock, and Wh, Halt Detector, signals appearing here are discussed in detail in paragraphs 3.65 and 3.66. When the interlock feature of figure 3-5 is employed, the condition $\overline{W6}\ W5$ Ecw cannot occur to set We. Under such circumstances, the peripheral device (or coupler) must be capable of detecting its own rate errors and reporting them via the Error Signal line, Wes .

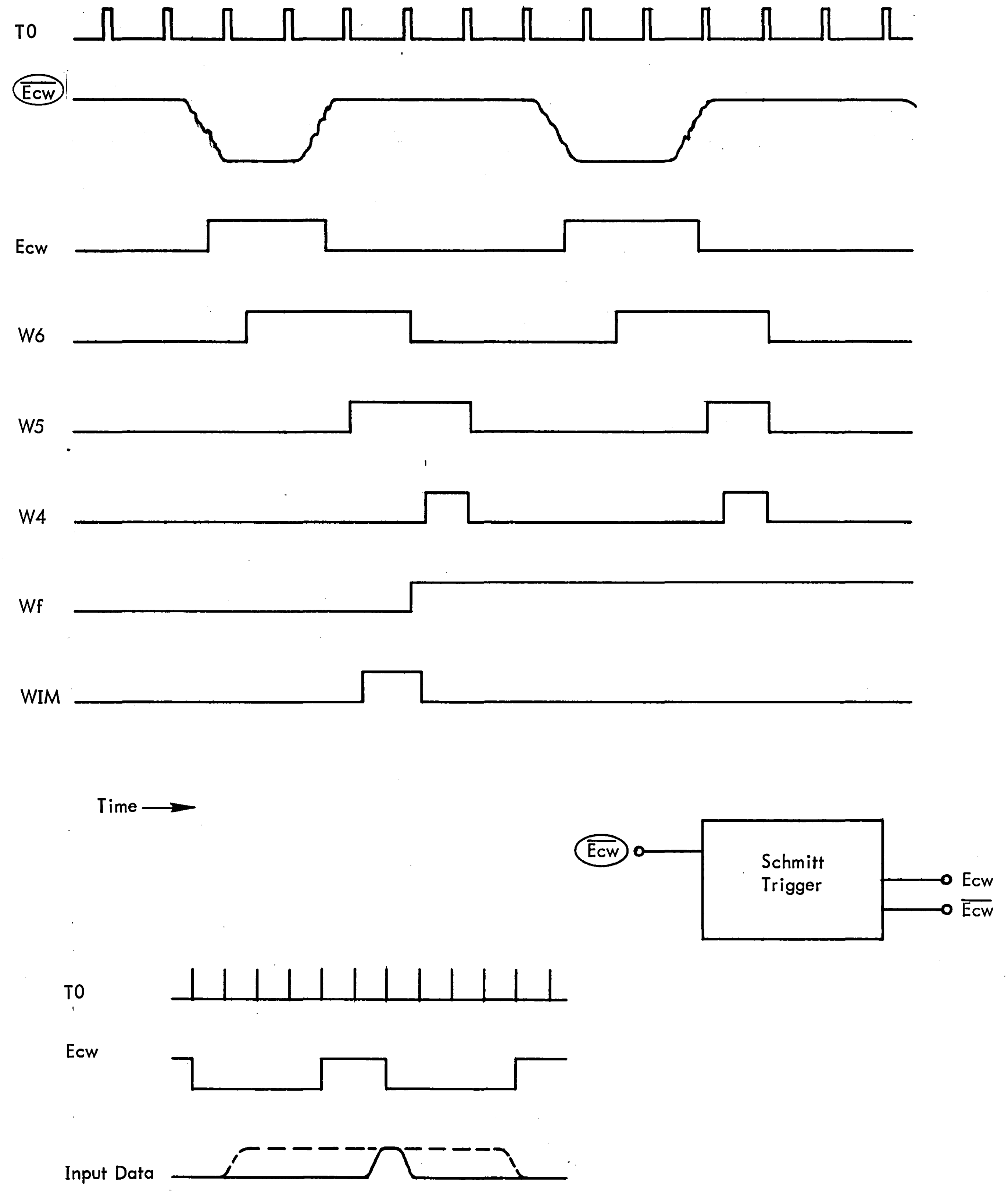
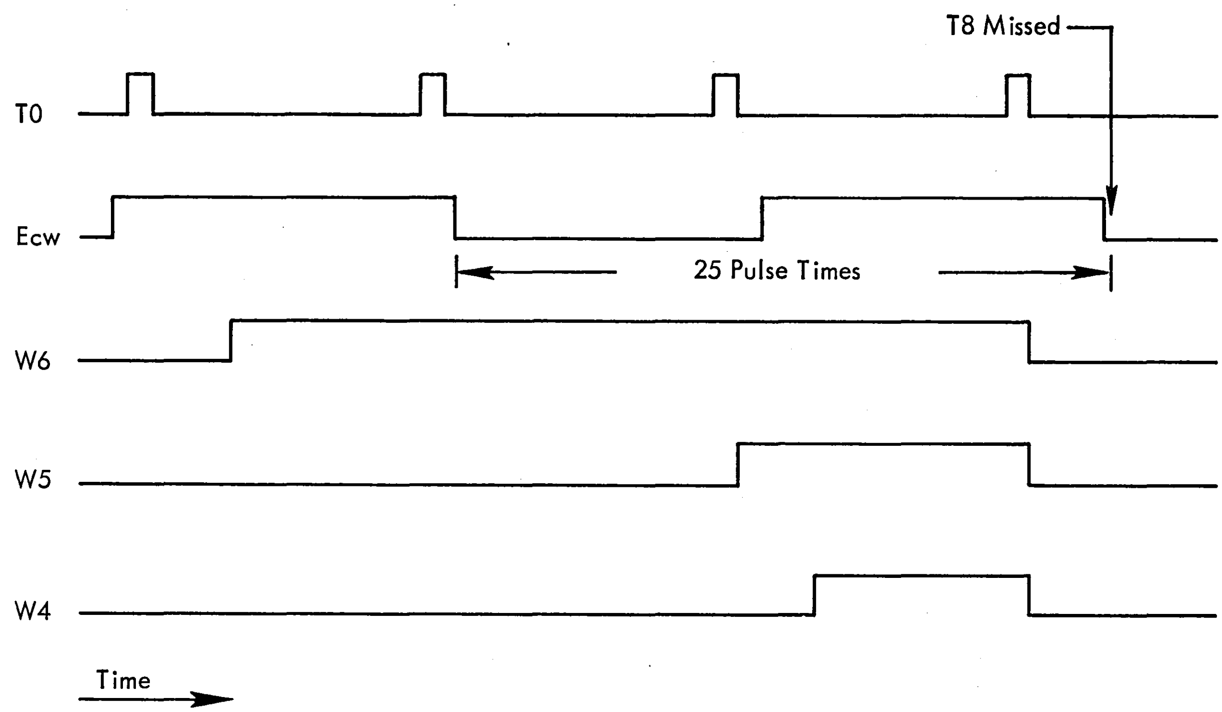
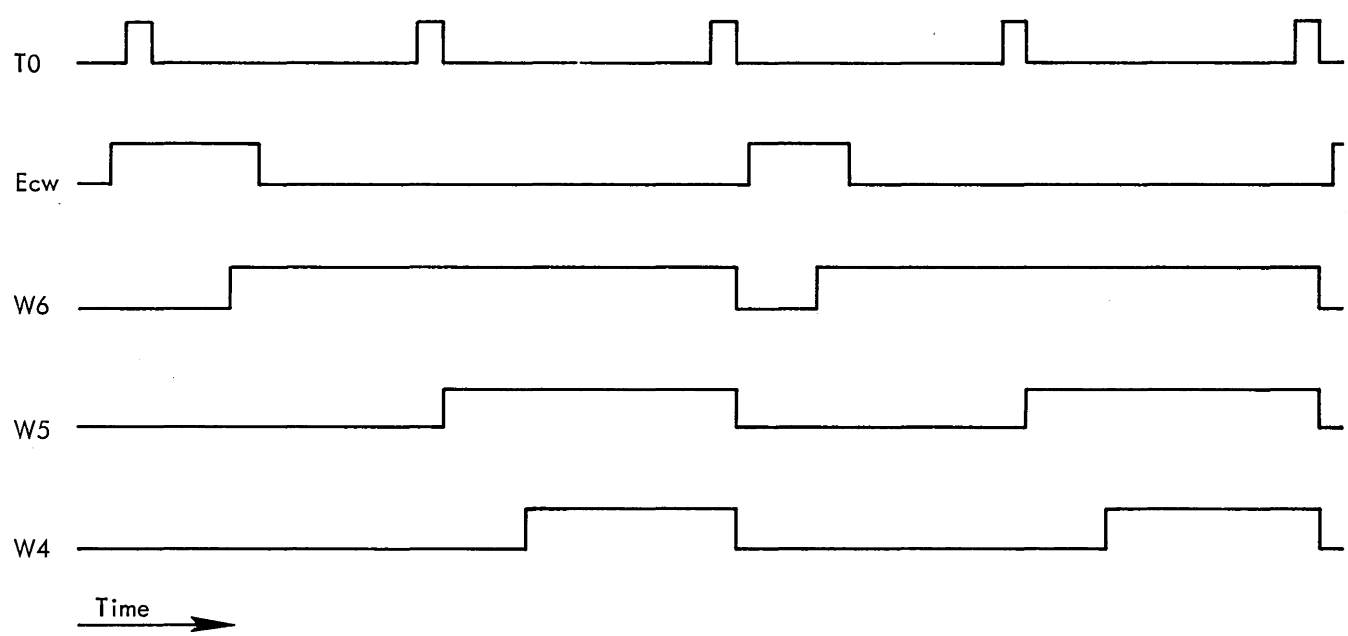


Figure 3-4. Input Clock Timing Charts (Typical)



a. Input Clocks too Fast



b. Input Clocks Interlocked With $\overline{W5}\ \overline{W6}$

Figure 3-5. Input Clock Timing Charts

$$sWe = Wes + . . .$$

3.60 The Input Timing Chart, figure 3-6, indicates the flow of the basic input process. The first WIM instruction is shown occurring late to illustrate how the Character Register accepts one more character after the W-Register is full.

3.61 The error detector flip-flop may also be set if the input character has even parity.

$$sWe = \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}\ Rwp\ \overline{Wg}\ Npw\ \overline{Iwg} + . . .$$

In this equation, $\overline{W9}$ indicates an input process, $\overline{W6}$ $\overline{W5}$ $\overline{W4}$ indicates that the received character has already been precessed into the W-Register when We is set. The term Npw is a signal received from the peripheral device to disable parity checking when a parity bit is not supplied. Wg and Iwg are End-of-Record and Extended Mode signals. These are discussed in paragraph 3-131 dealing with Interlace. Rwp is the Parity Flip-Flop which is toggled while the character is precessing out of the Character Register. During input, the operation of Rwp takes place as follows: Initially and again between each character precession, Rwp is reset by $\overline{W9}$ $\overline{W6}$ $\overline{W5}$ $\overline{W4}$. If the parity bit of the input character is a one, Rwp is set by $\overline{W9}$ W6 $\overline{W5}$.

$$sRwp = \overline{W9}\ W6\ \overline{W5}\ Zwp + . . .$$

$$rRwp = \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4} + Wc + . . .$$

Since W6 is set at pulse time T8 in the above equations Rwp may be set (if Zwp = 1) at the next pulse time, T7. At the next T0, W5 is set and the state of Rwp is reversed at T8, three pulse times later.

$$sRwp = Wf\ W5\ T8\ \overline{Rwp} + . . .$$

$$rRwp = Wf\ W5\ T8\ \overline{W9}\ Rwp + . . .$$

As a result of this reversal, Rwp is set if the input parity bit was a zero and reset if the bit was a one. The parity of the 6-, 12- or 24-data bits of the input character is now examined. This takes place while the character is being precessed into the W-Register. While precession occurs, the three bits of each octal group appearing as the output of the Character Register are tested by (Wb1 $\oplus$ Wb2 $\oplus$ Wb3). This parity logic term is true whenever there is an odd number of one's in a three bit group. It is used to reverse the state of Rwp for each such octal group containing an odd number of ones.

$$sRwp = \overline{W9}\ W4\ \overline{Rwp}\ (Wb1 \oplus Wb2 \oplus Wb3)$$
$$(T7 - T0)\ Qw1 + . . .$$

$$rRwp = \overline{W9}\ W4\ Rwp\ (Wb1 \oplus Wb2 \oplus Wb3)$$
$$(T7 - T0)\ Qw1 + . . .$$

The proper state of Rwp is thereby achieved, establishing whether the incoming character had a parity error. For example, if the following twelve bit character were received,

1 101 101 111 001

(parity bit)

its parity bit would cause Rwp to start off by setting then being reversed to the reset state. Of the four octal groups, two of them have an odd number of ones. This would cause Rwp to change state twice as precession took place thus returning to the reset condition. With Rwp reset, no parity error would be reported by We.

3.62 The number of octal groups that must be checked for each character precession and which outputs of the Character Register to be monitored for 6-, 12-, and 24-bit characters must also be determined. The number of octal groups to check is solved by (T7 - T0) Qw1, which is true for 2, 4, or 8 pulse times in accordance with the character length. Table 3-2 lists the values of signal Qw1. The character length may be determined by hardwired logic or by gating of Wx12 and Wx24 signals (depending on the model). Which outputs to monitor is solved by using the same gating signals, Wx12 and Wx24, or by hardwiring to select the proper outputs. Whether gating or hardwiring is employed depends on the equipment model number. The variations in models are detailed in table 3-2.

3.63 The characters have now been read into the Character Register, precessed into the W-Register, and parity has been checked. The contents of the W-Register must now be transferred to the C-Register in the Central Processor Unit (CPU). Each time a WIM (AIM) instruction is executed, the contents of the W (A) and C-Registers are interchanged. At this time (Ø4 of the WIM instruction execution) precession is blocked by W4 and recirculation is blocked by Wxx. The condition $\overline{Wf}\ \overline{W9}$ is used to signal the computer that the exchange can take place.

$$Wxx = Rx\ Pwy + . . . \qquad (Pwy = 05 \text{ in Model } 92200)$$

Rx indicates that a WIM or MIW instruction is being processed. It is always false for the C and D channels, since no WIM or MIW type instructions exist for those channels.

$$Ww1 = \overline{W4}\ C21r\ (T7 - T0)\ Wxx$$

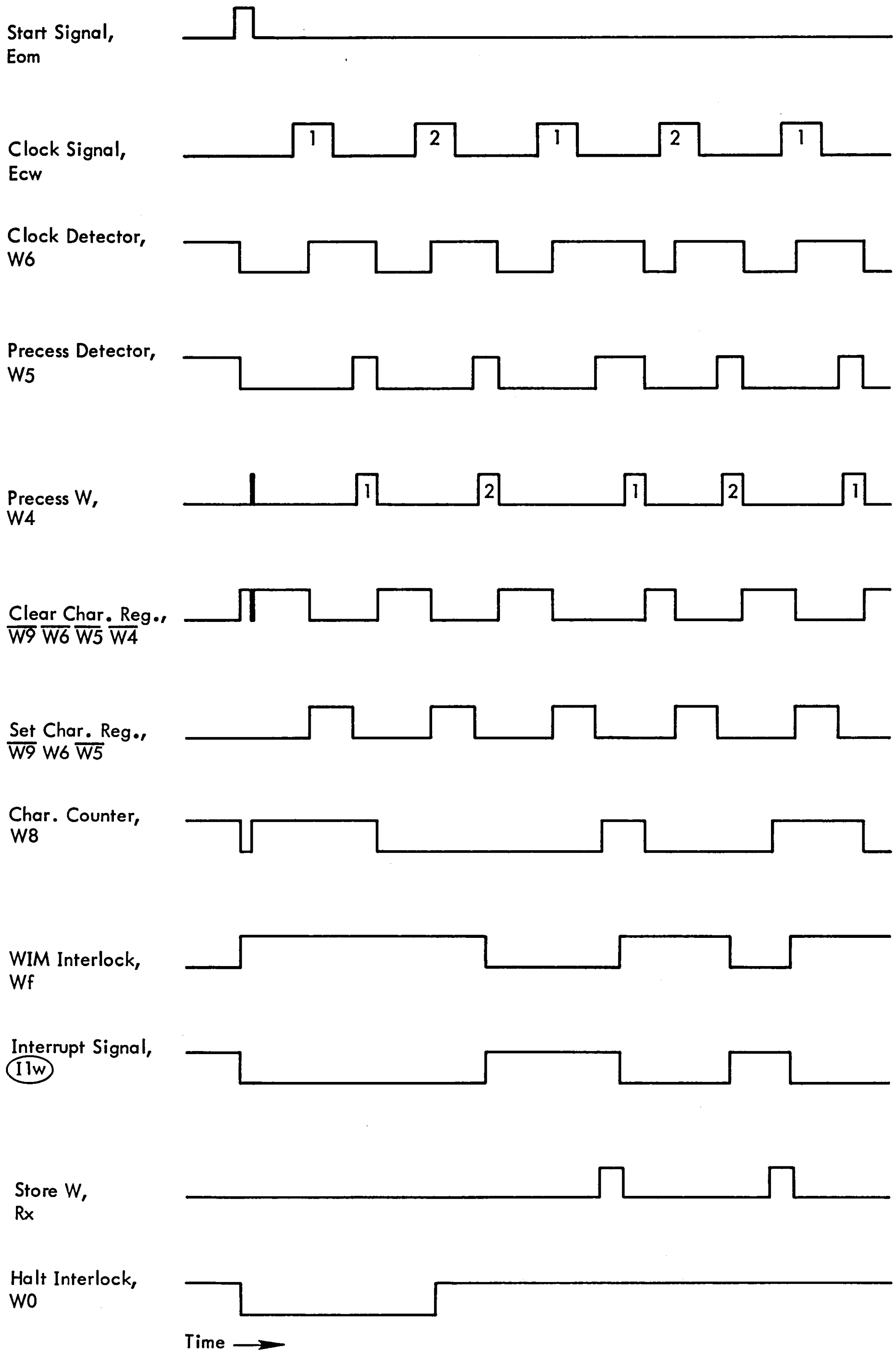


Figure 3-6. Input Timing Chart (Two Characters Per Word)

Table 3-2. Value of Parity Timing Signal Qw1

TMCC Model No.	Value of Qw1	Time When (T7 - T0) Qw1 is true
92200	Qw1 = Qr1 Qr4*	T7, T6
92201	Qw1 = Qr4*	T7, T6, T5, T4
92202	Qw1 = 1 (Qw1 is deleted)*	T7 through T0
93200/93221	$Qw1 = \overline{\overline{Wx12}\ \overline{Qr4} + \overline{Wx12}\ \overline{Wx24}\ \overline{Qr1}\ \overline{Qr4}}$	T7, T6 if Wx12 and Wx24 are off. T7 through T4 if Wx12 is on. T7 through T0 if Wx24 is on.

*Qw1 is replaced by the signal shown.

$$Ww2 = \overline{W4}\ C22r\ (T7 - T0)\ Wxx$$

$$Ww3 = \overline{W4}\ C23r\ (T7 - T0)\ Wxx$$

The terms C21r, C22r, and C23r are logically equivalent to the outputs of the C-Register, C21, C22, and C23, respectively, but are implemented through special drivers for this transfer function in order to minimize the delay. The three parallel portions of the C-Register behave in a manner similar to one another, therefore only one is listed below (all three are illustrated in figure 3-7).

$$sC0 = Cr3\ (Rx\ Rn1 + \ldots)$$

$$rC0 = Cr3\ \overline{(Rx\ Rn1 + \ldots)}$$

$$sRn1 = Rwy1\ \overline{Tsr} + \ldots$$

$$rRn1 = \overline{Rwy1}\ \overline{Tsr} + \ldots$$

3.64 The data transfer takes place during one machine cycle of the WIM instruction (Rx) and when completed, the computer Interlock Flip-Flop, Wf, is set to prepare the TMCC to accept the next input word.

$$sWf = Rx\ T0\ Twy + \ldots$$

Terminating an input operation can take place in one of several ways. The more sophisticated methods are discussed in paragraph 3.131 dealing with the interlace. The simplest procedure is to program an EOM instruction to disconnect the peripheral unit after a sufficient number of WIM instructions have been processed. Other methods will now be discussed and illustrated as they apply to specific devices. Use will be made of the interlock and interrupt signals while considering these devices. These features are applicable to other I/O units as well.

3.65 A photoreader input process (refer to figure 3-8) can be terminated by detecting tape gap following a block of input data. The tape gap consists of one or more tape frames where only the sprocket hole is punched. However, the photoreader must be able to initially read through a tape gap or leader without terminating at every tape frame. This is accomplished by the Halt Interlock Flip-Flop, W0, which detects the start of a block of data and is used by the peripheral device coupler to inhibit sprocket clocks until the first (or second) character is sent to the TMCC. Clocks for these first characters are derived from the characters themselves. The equation for W0 is given below, but to fully understand its action, the equation for a typical photoreader clock signal is also shown.

$$sW0 = \overline{W9}\ W6\ \overline{W8}\ Ecw + \ldots$$

$$rW0 = Wc + \ldots$$

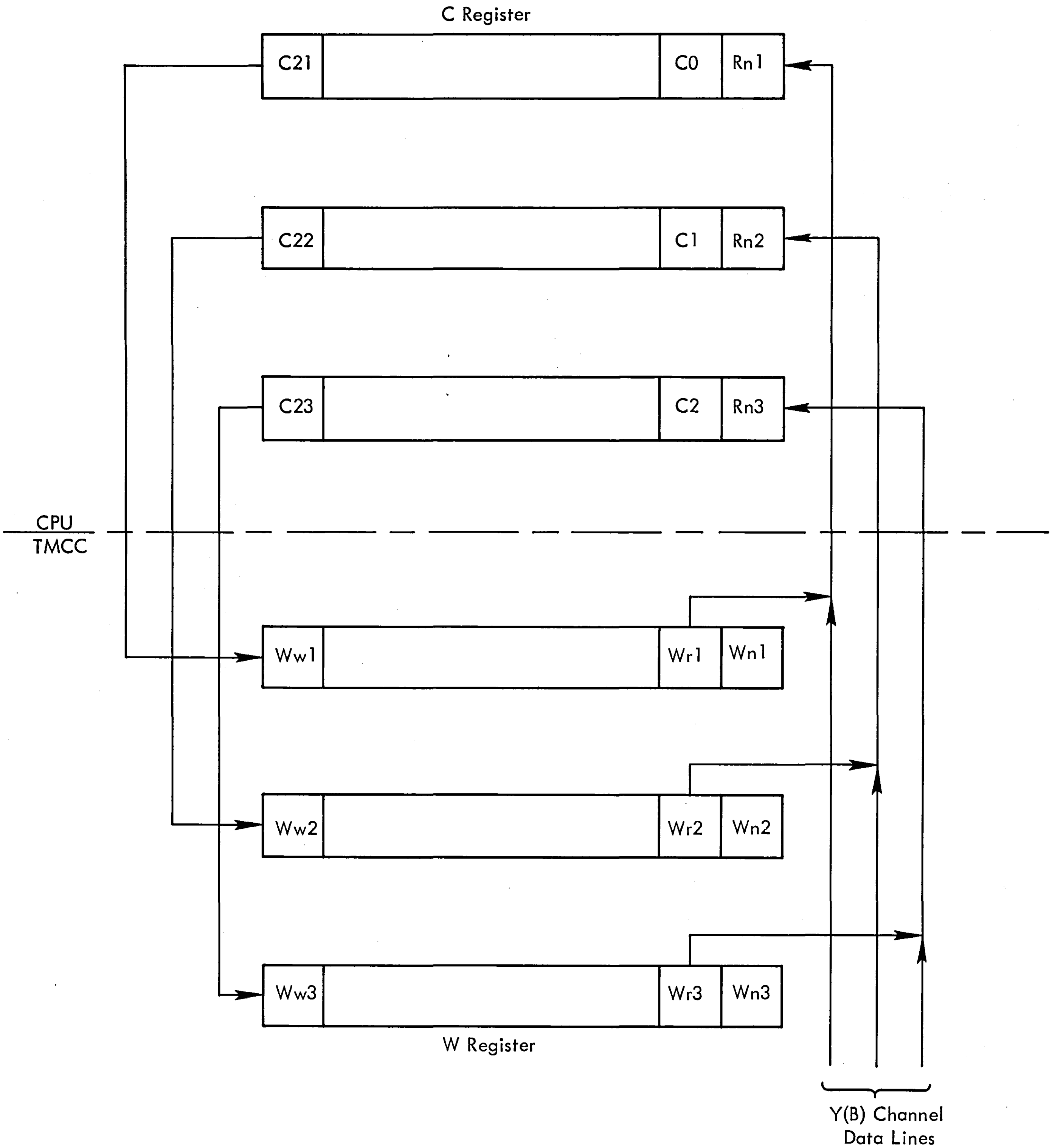


Figure 3-7. Data Transfer from W Register to C Register

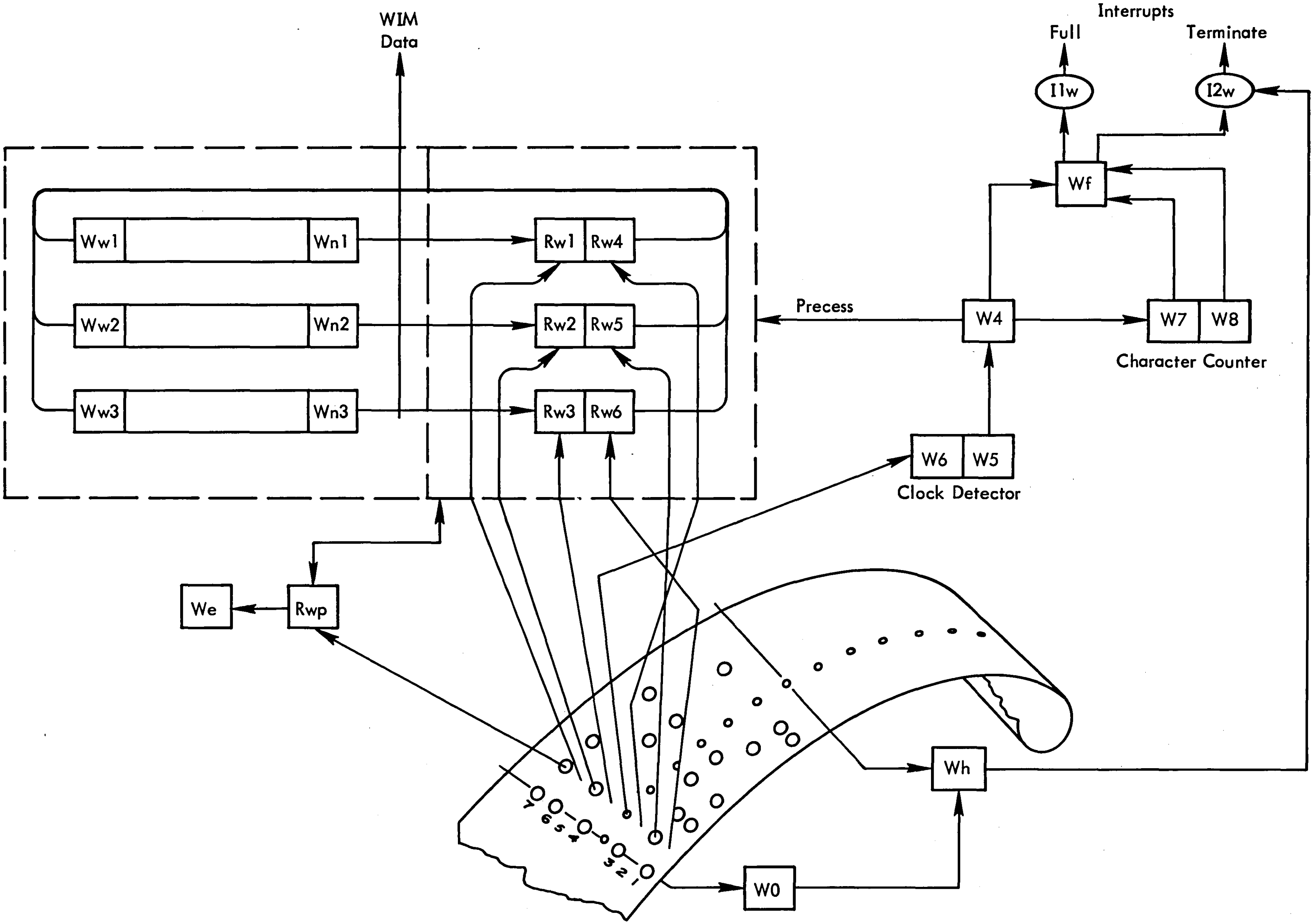


Figure 3-8. Information Flow Diagram - Phototape

$$Ecw = (Zw1 + Zw2 + Zw3 + Zw4 + Zw5 + Zw6 + Zwp + W0)\ Sp\ Re$$

In the latter equation, Zw1 through Zw6 are the character reader signals, Zwp is the parity bit signal, Sp is the sprocket hole signal, and Re is a photoreader enable level. The result of this combination is that while W0 is reset, the clocks are derived from the character bits. After setting W0, the term in parentheses is always true so Ecw varies with Sp only. When the first character is read following leader, a clock is produced which sets W6. W6 allows W0 to be set. The term W8 on the input of W0 prevents setting of W0 until the second character appears (in the four character per word mode). Waiting until the second character is desirable when reading from magnetic tape so a single noise character within a gap does not set W0. It is also important during a reverse scan of magnetic tape to avoid setting W0 on the longitudinal parity character.

3.66 After W0 has been set to enable the clocks to read in data, the End-of-Record Detector, Wg, is used to detect the first all-zeros, or gap, character (all zeros including the parity bit). Wg then enables the Halt Detector Flip-Flop, Wh.

$$sWg = \overline{W9}\ \overline{W10}\ \overline{W11}\ W12\ \overline{W13}\ (\overline{Rw1}\ \overline{Rw2}\ \overline{Rw3}\ \overline{Rw4}\ \overline{Rw5}\ \overline{Rw6}\ \overline{Rwp})\ W5\ (\overline{T7 - T0})\ (\overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}})$$

$$rWg = Wc$$

$$sWh = Wg\ \overline{Iwg}\ T8$$

The combination, $\overline{W9}\ \overline{W10}\ \overline{W11}\ W12\ \overline{W13}$, at the input of Wg decodes the fact that paper tape reader number 1 or number 2 is being used for input. The terms $(\overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}})$ are redundant and are due to the logic mechanization.

3.67 After Wg sets, parity errors no longer set the Error Detector Flip-Flop, We.

$$sWe = \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}\ Rwp\ \overline{Wg}\ Npw\ \overline{Iwg} + \ldots$$

Disabling We avoids parity testing for the next few machine cycles. During this time a complete word is precessed into the W-Register if the input did not supply sufficient characters to finish the last word. In the case where Wh sets but the W-Register is not yet full, W4 is set for successive cycles until the character counter reads 00. This process is termed "flushing". When W7 W8 read 00, Wf is reset and a Wc signal is generated to disconnect the TMCC.

$$sW4 = Wh\ Wf\ T8 + \ldots$$

$$rW4 = W4\ T0 + \ldots$$

$$sWf = Wc\ \overline{Wh} + \ldots$$

$$rWf = \overline{W7}\ \overline{W8}\ W4\ (T6 + T5) + \ldots$$

$$Wc = Wh\ \overline{Wf}\ (T3 - T0) + \ldots$$

The clear signal, Wc, disconnects the tape reader and clears the character counter, End-of-Record Detector, and Halt Interlock.

$$rW0 = Wc$$

$$rWg = Wc$$

The Halt Detector is then reset at the next T8 pulse time.

$$rWh = Wh\ \overline{Wf}\ T8$$

3.68 By allowing the character counter to count down to 00 before resetting, the final input word is filled-in with zero characters. The Phototape Termination Timing Charts illustrate the flow of this termination precess. Figure 3-9 illustrates the case where the last input word does not contain a full complement of characters. Figure 3-10 illustrates the timing for the case where the last word does have all characters filled before an all zeros character is detected.

3.69 If the interrupt system is enabled during the termination process, the $\overline{Wf}$ Wh condition generates an interrupt signal to call for a final WIM instruction from the computer.

$$I2w = (En + \textcircled{En})\ \overline{Iwg}\ Wh\ \overline{Wf}$$

The signals En and $\textcircled{En}$ are programmable and manual enable signals for the interrupt system. The final WIM instruction, as provided by a halt subroutine, stores the last word even though it may not have originally contained a sufficient number of characters. The final WIM instruction may be executed before or after the channel is disconnected. However, additional WIM instructions after that cause the computer to lock-up because it would be waiting for another input word.

3.70 When operating with devices other than punched paper tape, the input process is very similar to that just described, although the method used to derive the clock signals may vary somewhat from one device to another. Also, the gap (End-of-Record) signal, when required, is normally supplied by the external device rather than developed within the TMCC as is done for paper tape.

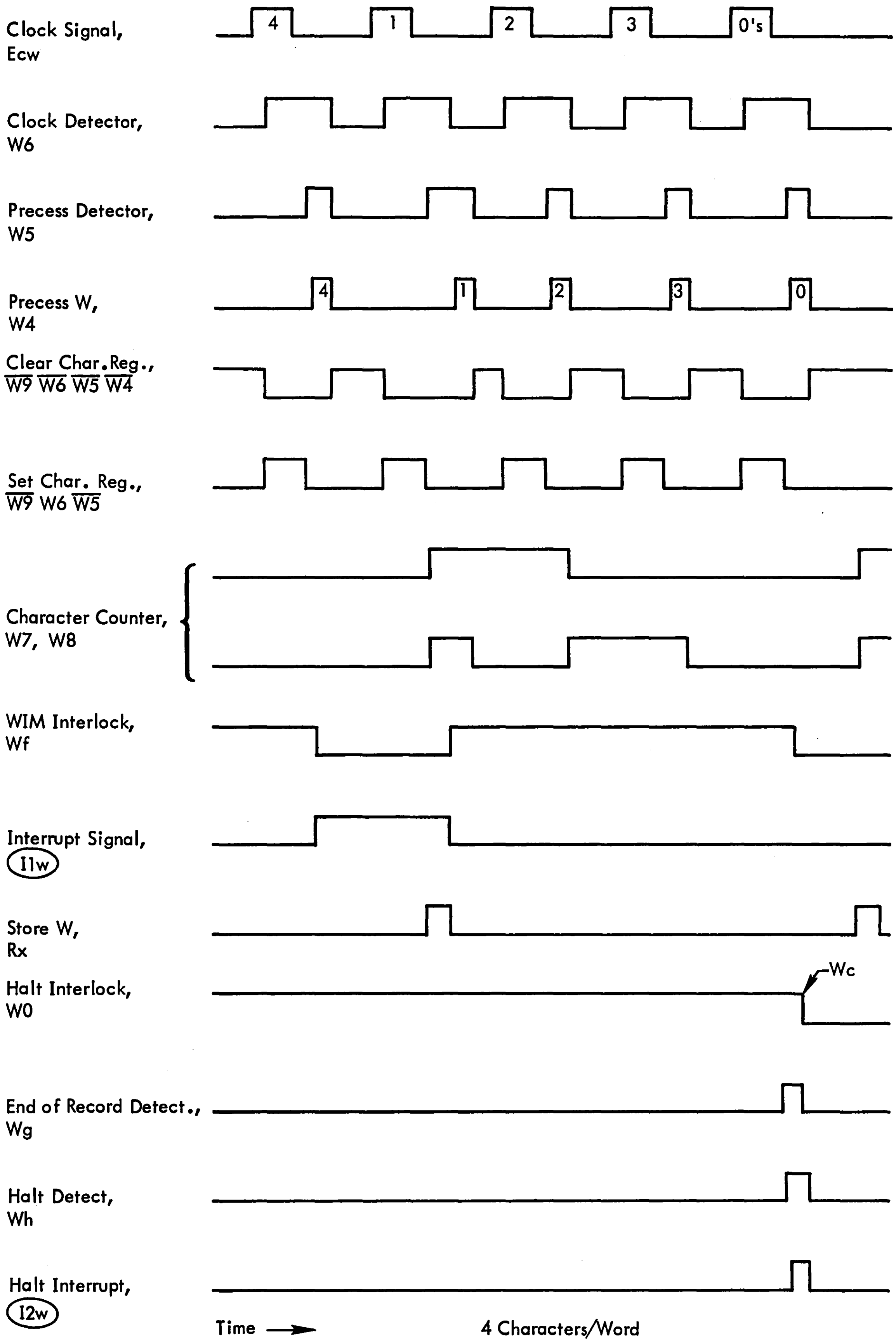


Figure 3-9. Termination Timing A. Phototape Input

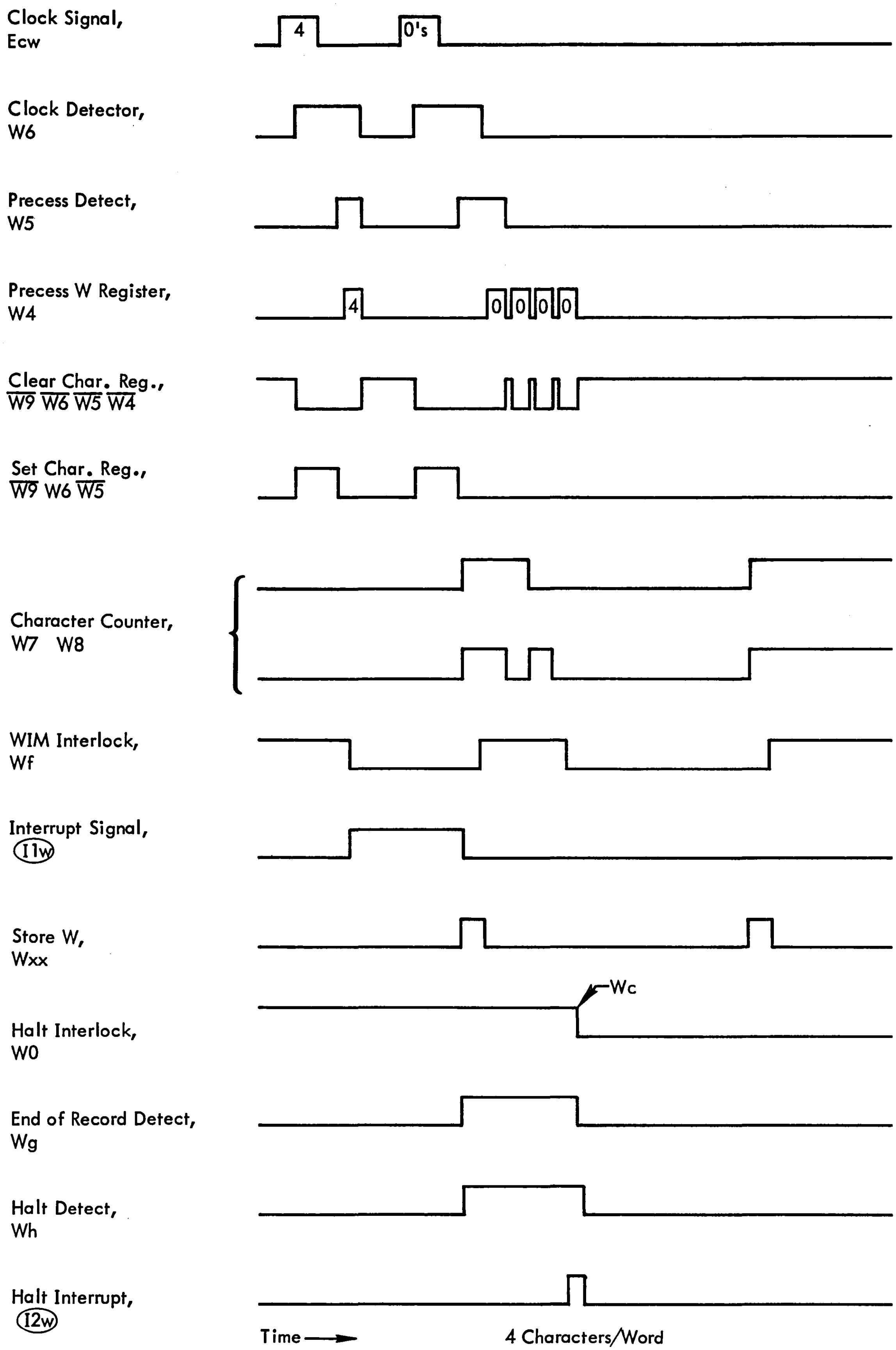


Figure 3-10. Termination Timing B - Phototape Input

3.71 An information flow diagram for magnetic tape input is illustrated in figure 3-11. The input timing for magnetic tape using the two character per word mode is illustrated in figure 3-12. When terminating, the magnetic tape unit generates a halt signal with a time delay triggered by the tape gap and W0. The halt detector is then triggered by the delayed signal.

$$sWg = Whs\ \overline{(T7 - T0)}\ \overline{W10\ W11\ W12\ W13\ W14}$$

$$rWg = Wc$$

$$sWh = Wg\ \overline{Iwg}\ T8$$

Whs is a halt signal from the peripheral device. In this case, it is the delayed signal from the magnetic tape unit. The delay allows time for the tape reader to check the longitudinal parity character following the block of data. Refer to figure 3-11. When a longitudinal parity error occurs, the tape reader sends an error signal (Wes) and the Error Detector is set. The (Wes) signal may also result from a rate error.

$$sWe = Wes + \ldots$$

Other devices may also supply error inputs via the (Wes) line. Unless inhibited by Npw, character parity is checked by Rwp when precession takes place.

3.72 Input termination timing for magnetic tape is illustrated in figure 3-13. The figure illustrates the case in which the input furnishes only three characters for the last four character word and the remaining character is filled with zeros. Also illustrated in figure 3-13 are the Halt Interrupt, calling for one more WIM instruction, and the final WIM instruction, itself.

3.73 Another type of input operation in which the TMCC participates is the scanning of magnetic tape. The process is similar to the usual magnetic tape reading process except that the character counter is prevented from reaching 00 again after W0 is set. The counter flip-flop, W8, is held in the "one" or set state by:

$$sW8 = \overline{W7}\ \overline{W9}\ W10\ W11\ \overline{Wh} + \ldots$$

In this equation, $\overline{W9}$ W10 W11 indicates a scan process has been programmed. A forward scan can be initiated by an EOM 0363X instruction. It may also be programmed by modifying a read process. While magnetic tape is being read, if an EOM14000 instruction is given, the flip-flop, W10, is set to convert directly from reading to scanning of the same tape.

$$sW10 = (Ioc\ C12\ \overline{C17}\ \overline{C19}\ \overline{C20}\ \overline{C21}\ \overline{C22}\ \overline{C23})$$

$$\overline{W9}\ \overline{W10} + \ldots$$

With W8 of the character counter held in a set state, the Buffer Full Signal, $\overline{W9}\ \overline{Wf}$, and the normal interrupt signals are prevented by keeping Wf from being reset.

$$rWf = \overline{W7}\ \overline{W8}\ W4\ (T6 + T5) + \ldots$$

$$I1w = \overline{Wf}\ W0\ \overline{Wh}\ (En + \textcircled{En})\ \overline{Iw}\ \overline{Ew}\ \overline{Iwg} + \ldots$$

$$I2w = (En + \textcircled{En})\ \overline{Iwg}\ Wh\ \overline{Wf} + \ldots$$

This allows each input character to be precessed into the W-Register without requiring WIM instructions to set Wf. However, when the end of a data block is reached, Wf is reset by a gap signal from the tape reader.

$$rWf = \overline{W9}\ W10\ W11\ W0\ Mtgw\ \overline{W7}\ (T6 + T5)\ Wh$$

And an interrupt is generated.

$$I1w = \overline{Wf}\ W0\ \overline{Wh}\ (\ldots)$$

This interrupt calls on the computer to enter a subroutine to execute a WIM instruction. The WIM instruction stores the last four characters read from the tape and which were precessed into the W-Register. The WIM instruction sets W7 and Wf in preparation for scanning another record.

$$sW7 = Wxx\ Wn1\ \overline{(T7 - T0)}\ W4 + \ldots$$

$$sWf = Tx\ T0\ Pwy + \ldots \qquad (Pwy = 05 \text{ for } 92200)$$

3.74 Based on a block counting program or an examination of the last four characters, the computer may reset W0 with another EOM0363X instruction, to cause the scan process to continue without a pause through the gap and into the next record. If W0 is not reset, the scan process is terminated by a (Whs) signal from the tape unit in a manner similar to that previously described for normal input termination. When the scan process does terminate, a halt interrupt signal is generated.

$$I2w = (En + \textcircled{En})\ \overline{Iwg}\ Wh\ \overline{Wf}$$

3.75 During the scan process the character parity is checked by the Rwp flip-flop and the longitudinal parity is checked by the tape unit (only if W0 is reset after the longitudinal parity character). Any error during the scan process sets the Error Detector flip-flop, We.

3.76 A reverse scan of magnetic tape is started by an EOM 0563X instruction. The process is similar to a forward scan, except that the WIM instruction at the end of a data block scan stores the first four characters of the block in reverse order. The longitudinal parity is not properly checked, with the result that We may be erroneously set.

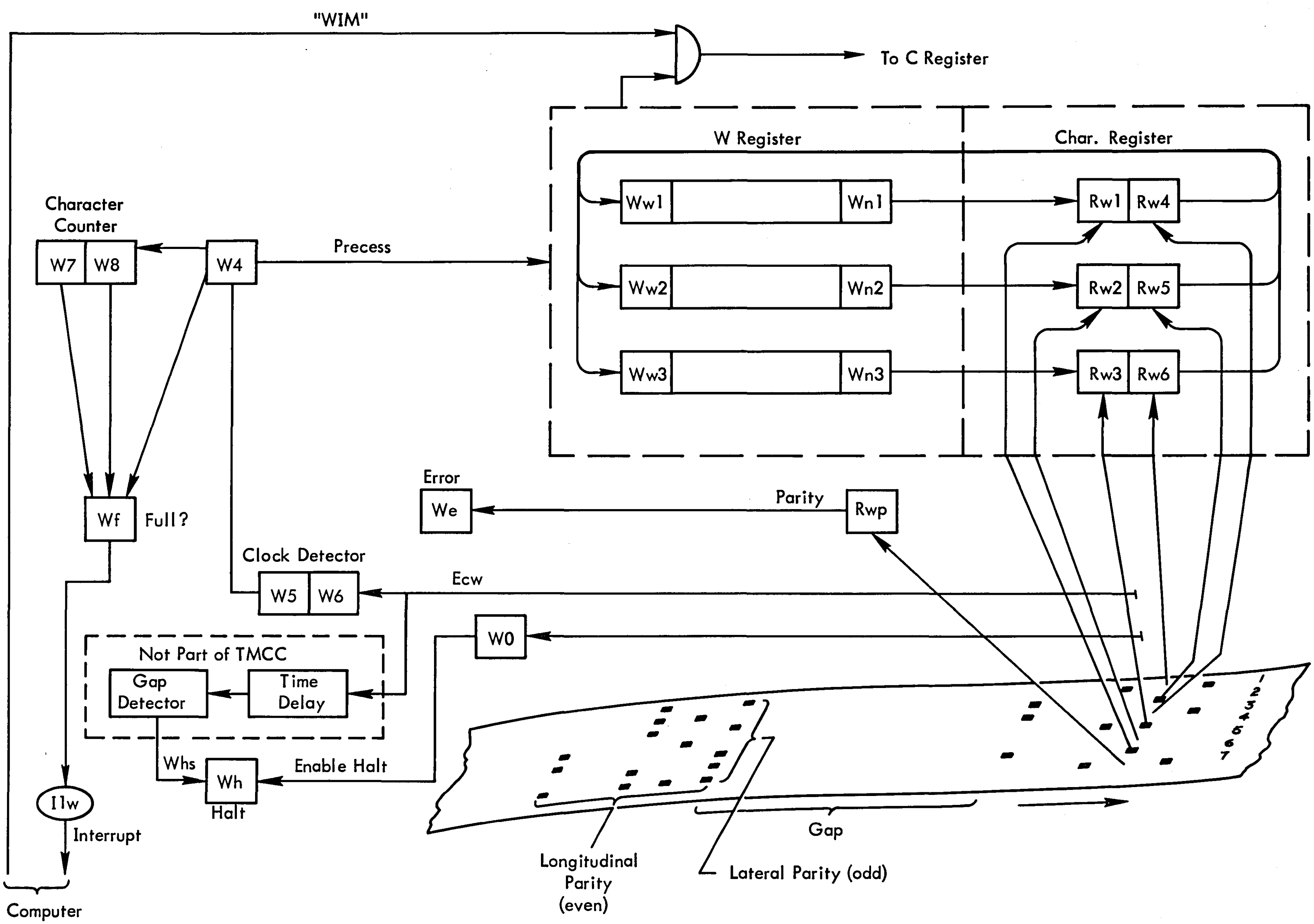


Figure 3-11. Information Flow Diagram - Magnetic Tape

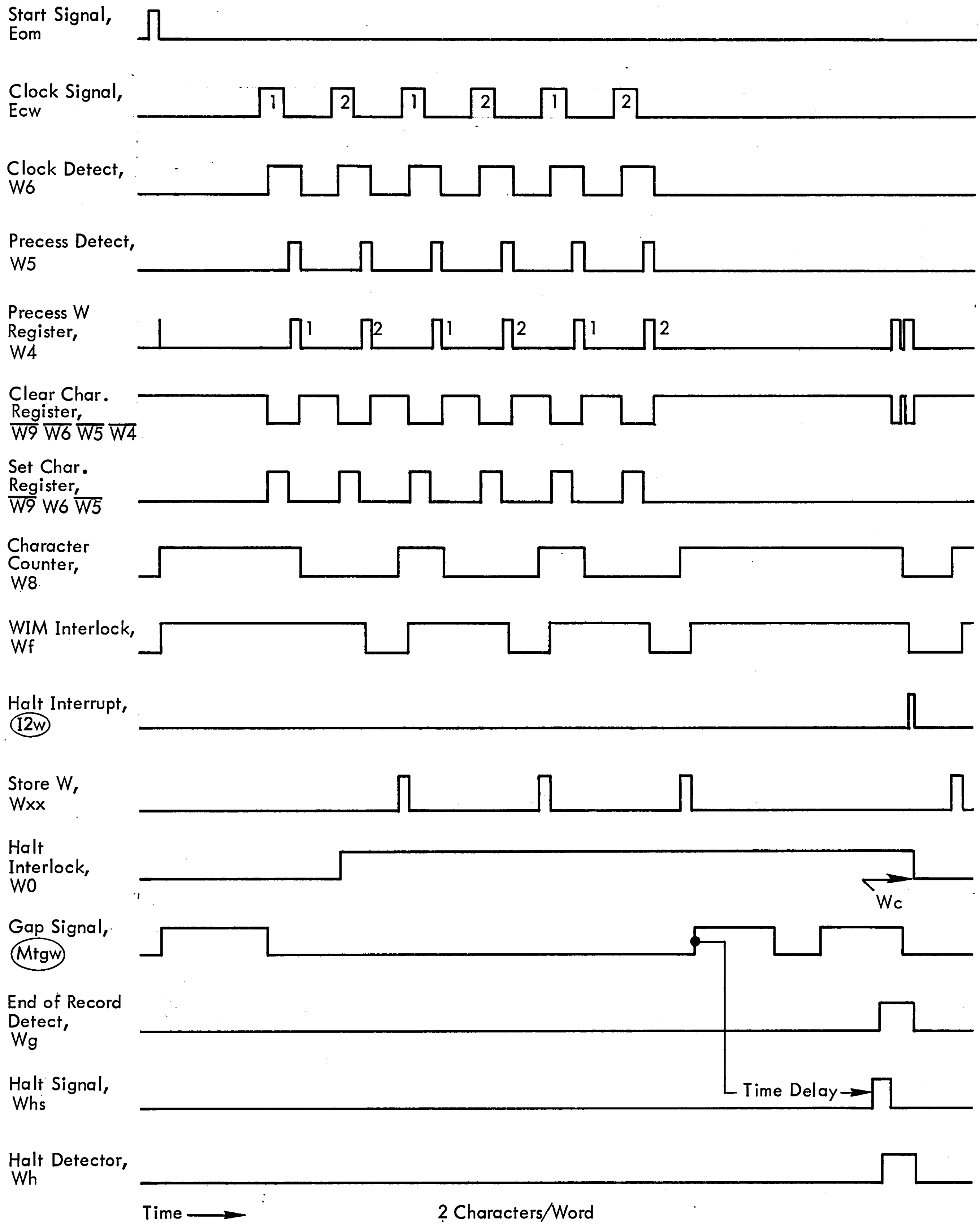


Figure 3-12. Input Timing - Magnetic Tape

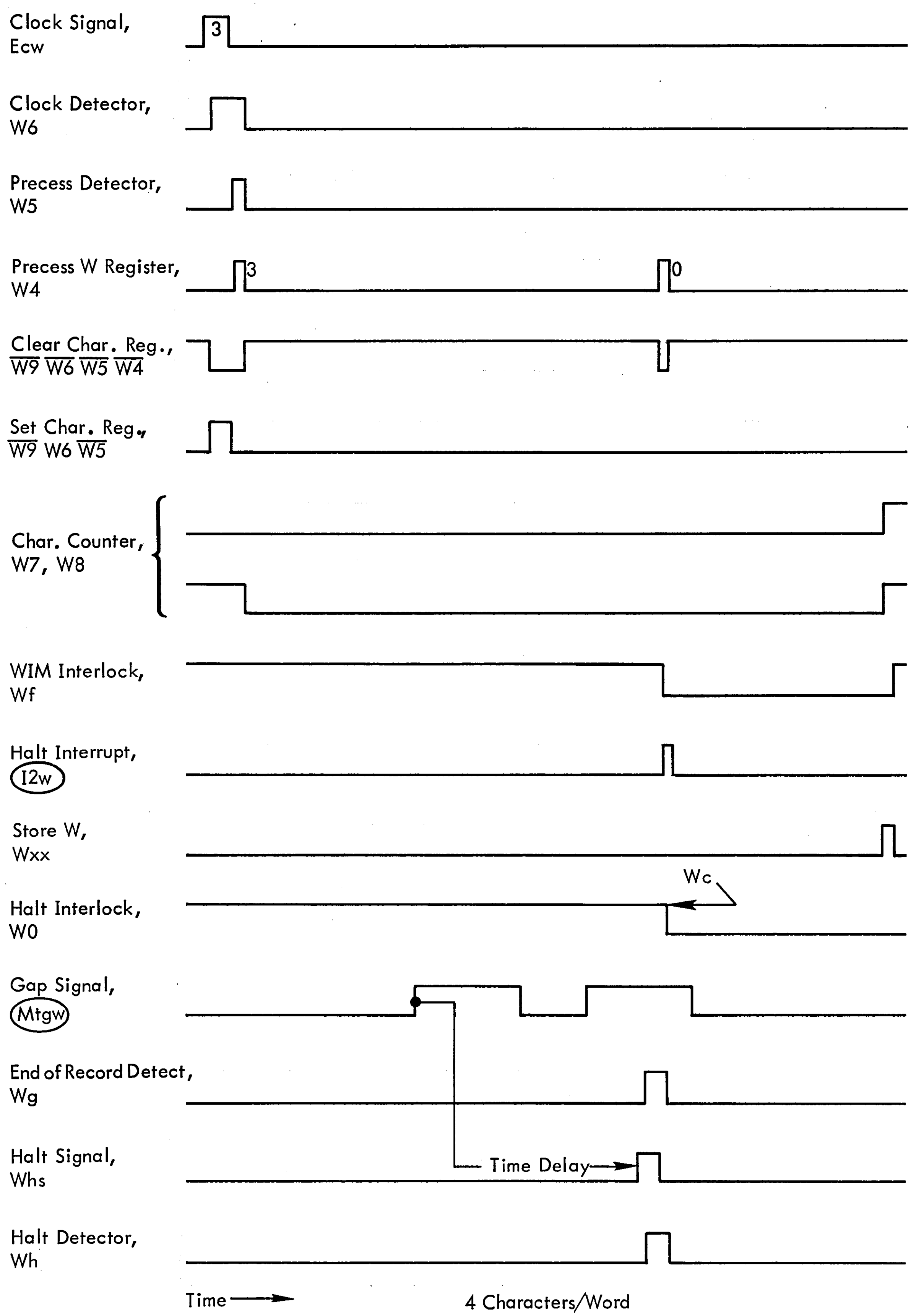


Figure 3-13. Input Termination Timing - Magnetic Tape

3.77 In the Magnetic Tape Forward Scan Timing Chart (refer to figure 3-14) and Reverse Scan Timing Chart (refer to figure 3-15), when the first interrupt informs the computer that the gap has been reached, a WIM instruction stores the last four characters read. Another EOM instruction then resets W0 to continue the scan process through the next block

$$rW0 = (Ioc\ C12\ \overline{C17}\ \overline{C19}\ \overline{C20}\ \overline{C21}\ \overline{C23})\ W9\ T0 + \ldots$$

Dotted lines indicate the reaction if the process were terminated. In case of termination, W0 allows the Tape Reader Halt Signal, Whs, to come through.

$$sWg = Whs\ \overline{T7 - T0}\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}} + \ldots$$

$$sWh = Wg\ \overline{Iwg}\ T8 + \ldots$$

Whs sets Wg, which in turn sets Wh. After Wh is set, the Character Counter Flip-Flop, W8, is no longer held on and a count-down begins.

$$sW8 = \overline{W7}\ \overline{W9}\ W10\ W11\ \overline{Wh} + \ldots$$

$$rW8 = W8\ W4\ T0 + Wc$$

This process is very similar to that described for terminating a normal read operation and Wf is reset as soon as the count-down reaches a point where W7 and W8 are both reset.

$$rWf = \overline{W7}\ \overline{W8}\ W4\ (T6 + T5)$$

A clear signal, Wc, then resets the TMCC after the four precessions.

$$Wc = Wh\ \overline{Wf}\ (T3 - T0) + \ldots$$

3.78 OUTPUT PROCESS (W9 true)

3.79 When an EOM0XXXX or EOM4XXXX instruction is executed to start an output process, an interlock signal, $\overline{Wf}$ (W0 + . . .) is immediately sent to the computer. And, if enabled, an interrupt calls for the computer to load the W-Register with the first output word. If the interrupt is disabled, the program should supply the MIW loading instruction before it is needed (i.e. before a clock signal is received from the peripheral unit).

$$rWf = Ws\ C18 + \ldots \quad \text{(denotes W register is empty)}$$

$$sW0 = Ws\ C18\ W9 + \ldots$$

$$(Ilw) = \overline{Wf}\ W0\ \overline{Wh}\ (En + (En))\ \overline{Iw}\ \overline{Ew}\ \overline{Iwg} + \ldots$$

3.80 Each MIW instruction, or time-share operation if interlace is being used (Wxx), exchanges the W-Register and the C-Register. Refer to figure 3-16.

$$Ww1 = \overline{W4}\ C21r\ (T7 - T0)\ Wxx + \ldots$$

$$Ww2 = \overline{W4}\ C22r\ (T7 - T0)\ Wxx + \ldots$$

$$Ww3 = \overline{W4}\ C23r\ Wxx + \ldots$$

$$sC0 = Cr3\ [(Tsr + Rx)\ Rn1 + \ldots]$$

$$rC0 = Cr3\ [\overline{(Tsr + Rx)\ Rn1 + \ldots}]$$

similarly for C1 and C2

$$sRn1 = Rwy1\ \overline{Tsr} + Rr1\ Tsr$$

$$rRn1 = \overline{Rwy1}\ \overline{Tsr} + \overline{Rr1}\ Tsr$$

similarly for Rn2 and Rn3

$$Wxx = Rx\ Pwy + \ldots$$

(Pwy = 05 for 92200, Rx is always false for TMCC-C)

3.81 As with the input process, $\overline{Wxx}$ blocks recirculation and with W4 false precession is blocked at this time also. When precession does take place, as enabled by W4, an output character is shifted from the W-Register to the Character Register and Rwp is used to generate an odd parity bit. During the output operation the parity flip-flop operates in a manner similar to its action during input.

3.82 Rwp is initially set by Wf W5 T8. Then, when precession occurs, each octal group coming from the W-Register is examined for an odd or even number of ones. This checking is done by (Wn1 ⊕ Wn2 ⊕ Wn3) which is true whenever there are one or three ones in Wn1, Wn2, and Wn3. Each time this term is true during the checking period, Rwp is switched to its opposite state.

$$sRwp = W9\ W4\ \overline{Rwp}\ \overline{Wxx}\ (Wn1 \oplus Wn2 \oplus Wn3)\ Qw2\ (T7 - T0) + Wf\ W5\ T8\ \overline{Rwp} + \ldots$$

$$rRwp = W9\ W4\ Rwp\ \overline{Wxx}\ (Wn1 \oplus Wn2 \oplus Wn3)\ Qw2\ (T7 - T0) + \ldots$$

Qw2 is a term similar to the Qw1 used during the input process. Qw2 with (T7 - T0) establishes the pulse times during which the parity checking is done. It may either be hardwired or function with the gating signals Wx12 and Wx24 depending on the equipment model number. Refer to table 3-3.

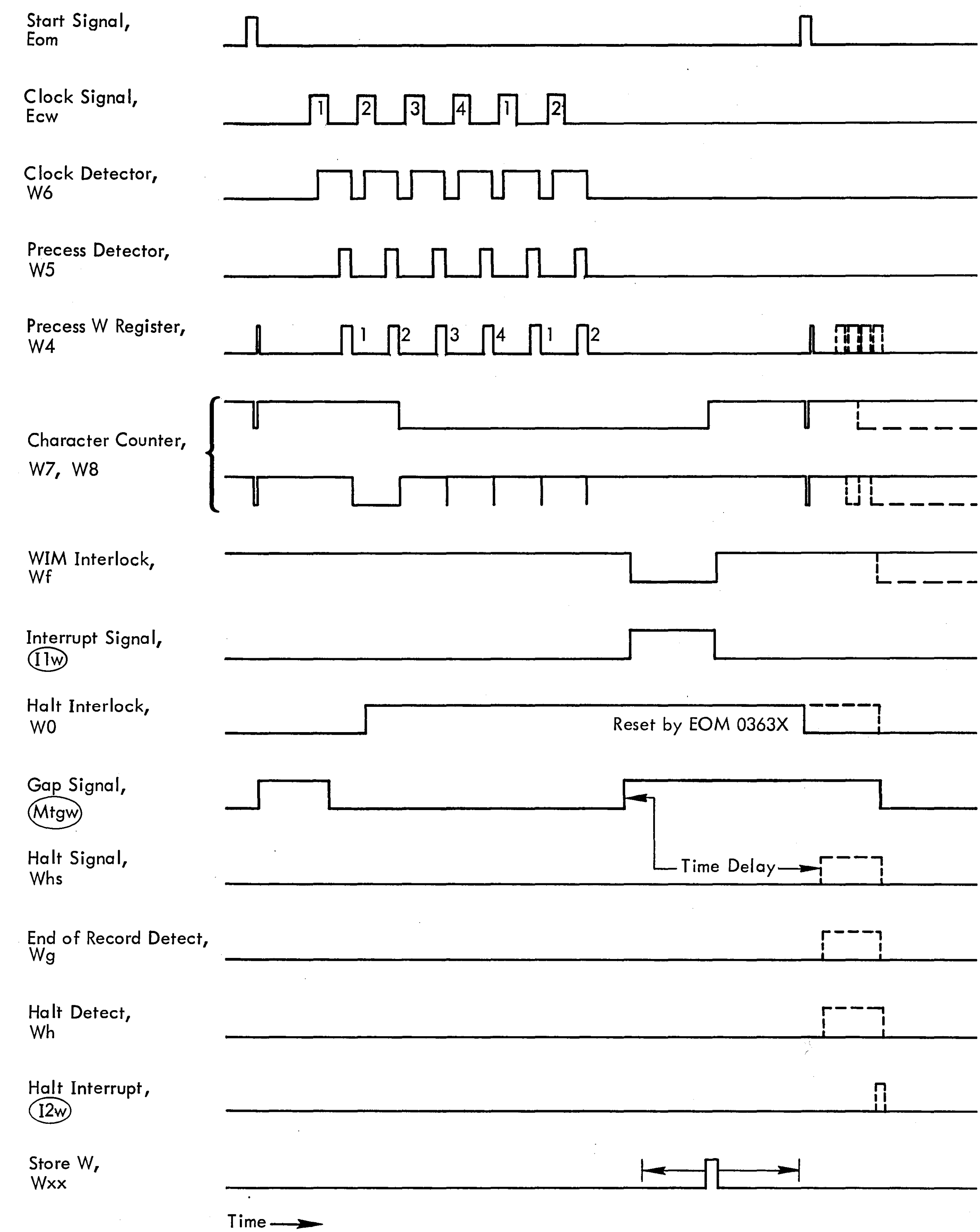


Figure 3-14. Forward Scan Timing Chart - Magnetic Tape

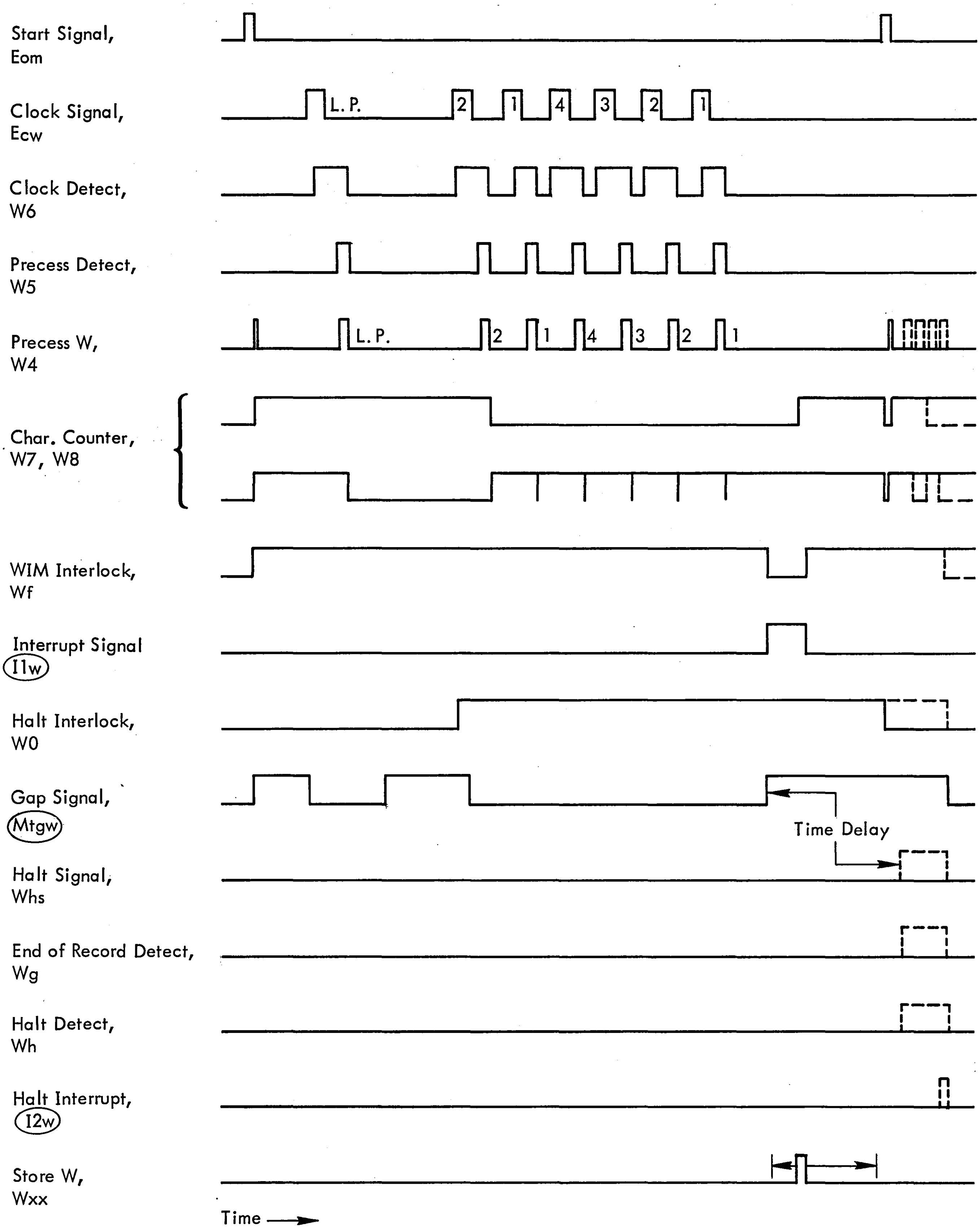


Figure 3-15. Reverse Scan Timing Chart - Magnetic Tape

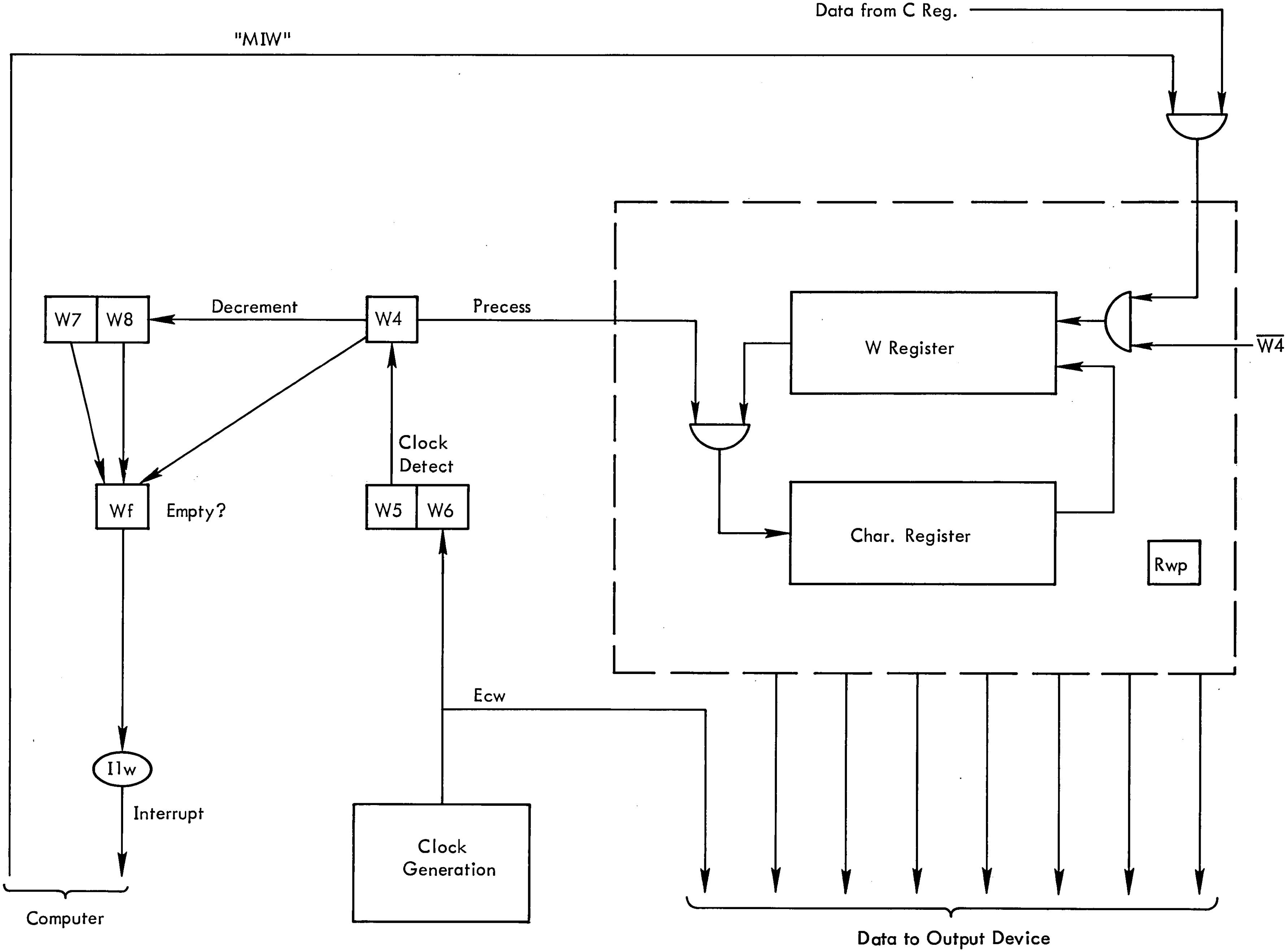


Figure 3-16. Output Information Flow Diagram

Table 3-3. Value of Qw2 Parity Timing Signal

TMCC Model No	Value of Qw2	Pulse Times When (T7 - T0) Qw2 is True
92200	$Qw2 = Qr2\ \overline{Qr4}$ *	T0, T1
92201	$Qw2 = \overline{Qr4}$ *	T3 through T0
92202	$Qw2 = 1$ (Qw2 is deleted)	T7 through T0
93200/93221	$Qw2 = \overline{Wx12\ Qr4 + \overline{Wx12}\ \overline{Wx24}\ \overline{Qr2}\ \overline{Qr4}}$	T0 and T1, if Wx12 and Wx24 are both off. T3 through T0, if Wx12 is on T7 through T0, if Wx24 is on

*Qw2 is replaced by the signal shown above for Models 92200/201/202.

3.83 As an example of output parity generation, consider the twelve-bit character 111 010 101 001. Rwp would start in the set condition and would then switch states three times, once for each of the octals containing an odd number of ones. Thus, Rwp would conclude its switching operation in the reset state to produce a zero parity bit for an odd parity output character.

3.84 The basic flow of the output process is illustrated in figure 3-17. The execution of the second MIW instruction is shown occurring late to depict how the Character Register is cleared when a new output character is not available. If another output character is still not available when the next clock signal, Ecw appears, the error detector (We) is set as is done during an input process.

$$sWe = W0\ \overline{W6}\ W5\ Ecw\ T8 + \ldots$$

$$rWe = Wc\ \overline{Wh}$$

3.85 In the output processes (as in the input processes), the Character Register is initially cleared by $\overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$. The first output character to be read is, therefore, all zeros. This is appropriate for a leader or gap in paper tape punching. However, for some forms of output, such as typing or leaderless punching, and magnetic tape writing (the tape unit automatically generates leader), the first output character should be in the Character Register before the first clock signal. For this type of output, an EOM2XXXX instruction with a "one" bit in C13 is used. This code bit is used to set W5 which then causes the first loading of the W-Register to be followed directly by precession of the first output character into the Character Register. In this case the sequence of operations again starts by resetting Wf and setting W0 with the resulting interrupt Ilw. However, now W5 is also set by the Ws signal. Then, as usual, when the MIW instruction is executed and Rx goes true, Wf is set. With W5 on, W4 can be set at pulse time T8 just after the data transfer takes place. Figure 3-18, Output Timing Chart 2, illustrates the flow of this process.

$$sWf = Rx\ T0\ Pwy + \ldots \quad (Pwy = 05 \text{ for } 92200)$$

$$rWf = Ws\ C18 + \ldots$$

$$sW5 = Ws\ C13\ C18\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}} + \ldots$$

$$rW5 = W4\ T0 + Wc$$

$$sW4 = Wr\ Wf\ T8\ \overline{Wg} + \ldots$$

$$rW4 = W4\ T0 + \ldots$$

3.86 To terminate an output process, the MIW instruction which loads the last output word into the W-Register is followed by an EOM14000 instruction to reset W0. An EOM14100 instruction is used to terminate the Y channel.

$$rW0 = (Ioc\ C12\ \overline{C17}\ \overline{C19}\ \overline{C20}\ \overline{C21}\ \overline{C22}\ \overline{C23})\ W9\ T0 + \ldots$$

$$Ioc = Ioc1\ \overline{C1}\ \overline{Er}\ Qr3$$

$$Ioc1 = Eom\ \overline{C10}\ C11$$

$\overline{Er}$ is a signal inhibiting Eom and Ioc when the Interlace Prepare flip-flop (to be discussed later) has been set. The C1 bit, which appears on Ioc, indicates a W or Y channel instruction. C1 is used with the C and D channels.

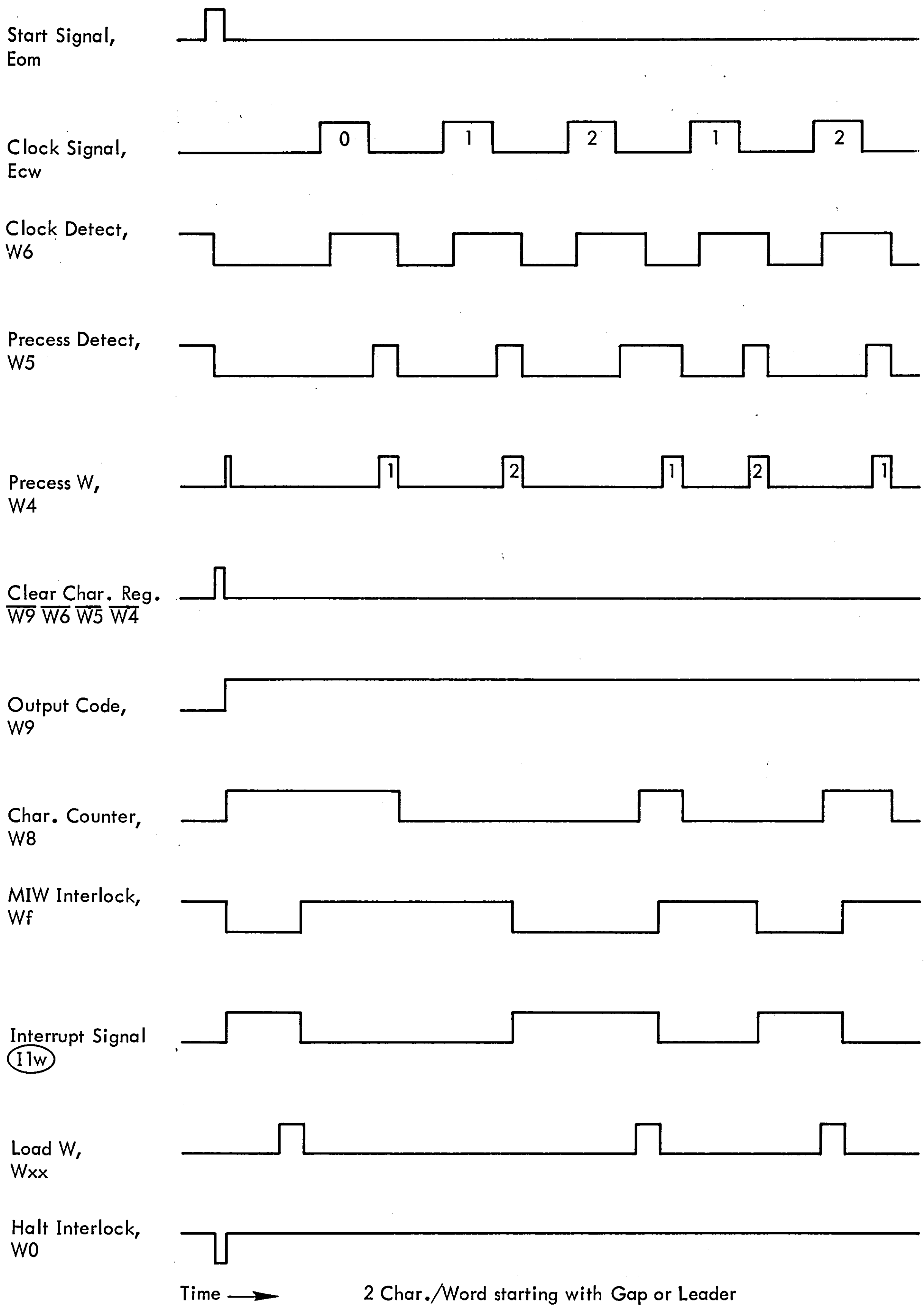


Figure 3-17. Output Timing Chart 1

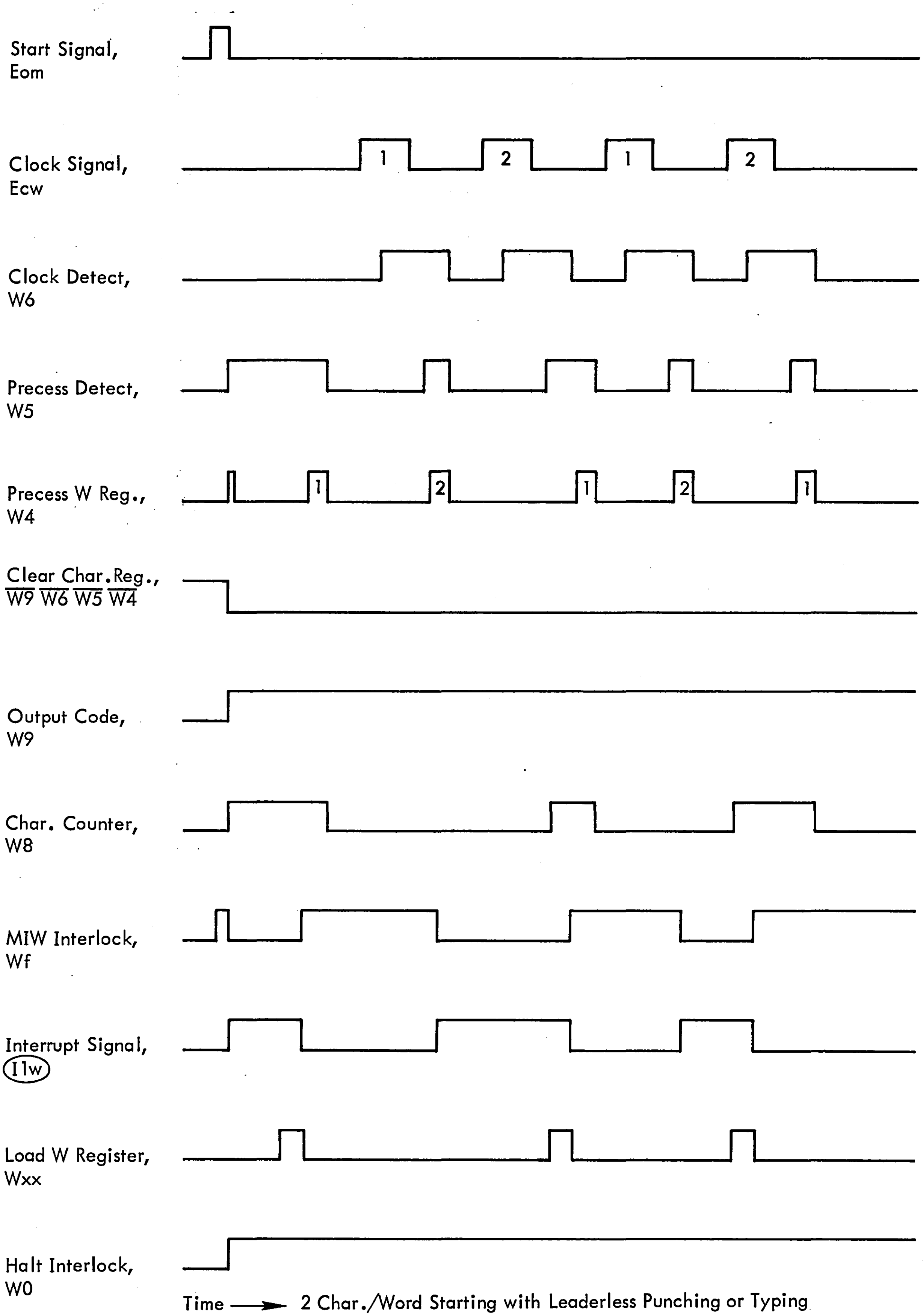


Figure 3-18. Output Timing Chart 2

3.87 Resetting of W0 results in the following: Further normal interrupt signals are blocked.

$$\mathrm{Iw1} = \overline{\mathrm{Wf}}\ \mathrm{W0}\ \overline{\mathrm{Wh}}\ (\ .\ .\ .\ )$$

Further late-load error signals are blocked.

$$\mathrm{sWe} = \mathrm{W0}\ \overline{\mathrm{W6}}\ \mathrm{W5}\ \mathrm{Ecw}\ \mathrm{T8} + .\ .\ .$$

The WIM/MIW Interlock Signal Wf W0 is blocked. As a result of inhibiting the interlock and interrupt signals, no further MIW instructions are processed and, therefore, Wf is not set again after the last character is precessed into the Character Register.

$$\mathrm{sWf} = \mathrm{Rx}\ \mathrm{T0}\ \mathrm{Pwy} + .\ .\ . \qquad (\mathrm{Pwy} = 05 \text{ for } 92200)$$

$$\mathrm{rWf} = \overline{\mathrm{W7}}\ \overline{\mathrm{W8}}\ \mathrm{W4}\ (\mathrm{T6} + \mathrm{T5}) + .\ .\ .$$

With Wf reset, W4 is prevented from setting after the last output character is precessed. This results in the state, $\overline{\mathrm{W0}}\ \overline{\mathrm{W4}}\ \mathrm{W5}\ \overline{\mathrm{W6}}$, following the precession.

$$\mathrm{sW4} = \mathrm{W5}\ \mathrm{Wf}\ \mathrm{T8}\ \overline{\mathrm{Wg}} + .\ .\ .$$

$$\mathrm{rW4} = \mathrm{W4}\ \mathrm{T0} + \mathrm{W4}\ \mathrm{T8}$$

$$\mathrm{sW6} = \overline{\mathrm{W5}}\ \mathrm{Ecw}\ \mathrm{T8}\ \overline{\overline{\mathrm{W10}}\ \overline{\mathrm{W11}}\ \overline{\mathrm{W12}}\ \overline{\mathrm{W13}}\ \overline{\mathrm{W14}}} + .\ .\ .$$

$$\mathrm{rW6} = \mathrm{W5}\ \mathrm{W0} + \mathrm{Wc}$$

$$\mathrm{sW5} = \overline{\mathrm{W5}}\ \mathrm{W6}\ \overline{\mathrm{Ecw}}\ \mathrm{T0} + .\ .\ .$$

$$\mathrm{sW5} = \mathrm{W4}\ \mathrm{T0} + \mathrm{Wc}$$

The state, $\overline{\mathrm{W0}}\ \mathrm{W5}\ \overline{\mathrm{W6}}$, is used to set the halt detector unless magnetic tape is being used ($\overline{\mathrm{W11}}$ indicates not magnetic tape).

$$\mathrm{sWh} = \mathrm{W9}\ \overline{\mathrm{W11}}\ \overline{\mathrm{W0}}\ \mathrm{W5}\ \overline{\mathrm{W6}}\ (\overline{\mathrm{Iwg}} + .\ .\ .\ )\ \mathrm{T8} + .\ .\ .$$

When the output is to a magnetic tape unit, the state $\overline{\mathrm{W0}}\ \mathrm{W5}\ \overline{\mathrm{W6}}$ is sent to that unit and after a suitable delay (while the tape unit generates a longitudinal parity character) a Whs halt signal is received back to set Wh.

$$\mathrm{sWh} = \mathrm{Whs}\ \mathrm{W11}\ \mathrm{T8} + .\ .\ .$$

Regardless of the method of setting Wh to terminate an output process, the Halt Interrupt Signal, I2w, is generated in the cycle in which Wh is set.

$$\mathrm{I2w} = (\mathrm{En} + \mathrm{En})\ \overline{\mathrm{Iwg}}\ \mathrm{Wh}\ \overline{\mathrm{Wf}} + .\ .\ .$$

Ana a clear signal is generated.

$$\mathrm{Wc} = \mathrm{Wh}\ \overline{\mathrm{Wf}}\ (\mathrm{T3} - \mathrm{T0}) + .\ .\ .$$

Then Wh is reset, as well as the rest of the TMCC.

$$\mathrm{rWh} = \mathrm{Wh}\ \overline{\mathrm{Wf}}\ \mathrm{T8} + \mathrm{Wc}\ (\mathrm{T6} + \mathrm{T5})$$

The Output Termination Timing Charts indicate the flow of these output termination processes for devices other than magnetic tape (refer to figure 3-19) and for magnetic tape (refer to figure 3-20).

3.88 Two additional timing charts are included to illustrate the output sequences for specific devices. The flow of the complete output process for a paper tape punch operation is illustrated in figure 3-21. The EOM0XX4X start instruction causes tape leader to be punched while the device inhibits clock signals. An all zeros character is also punched for the first output clock signal. After the last output character is processed, a halt interrupt signal is generated.

3.89 The flow of an output process using magnetic tape is illustrated in figure 3-22. A time delay triggered by the EOM02X5X start instruction causes a tape gap to be recorded first while inhibiting output clock signals. $\overline{\mathrm{W0}}\ \mathrm{W5}\ \overline{\mathrm{W6}}$ signals the tape unit to count three clocks and record the longitudinal parity character, and triggers a second time delay to cause a gap to be recorded after the data block. When the gap is completed, the tape unit generates a Whs signal to halt the output process. Each character parity and the longitudinal parity of the characters reproduced at the read head are checked by the tape unit and an error signal, Wes, is generated to set We for any detected errors. Several other error conditions are also checked, such as slew, amplitude, and rate error.

$$\mathrm{sWe} = \mathrm{Wes} + .\ .\ .$$

3.90 A special case of a magnetic tape output operation is the erase function. The tape erase is started by an EOM01X7X instruction. The erase procedure is performed in the same way as any other output to magnetic tape but the W10 bit is used by the tape unit to cause writing of all zero data regardless of what may be appearing at the character register outputs.

3.91 SYS GATE

3.92 The system control EOM instruction has little effect on the TMCC. It is included here only because the Sys signal is gated through the TMCC channel.

3.93 When an EOM instruction, containing "ones" in bits 10 and 11, is executed, an Sys signal is generated as an output from the TMCC on the Sys line.

$$\mathrm{Sys} = \mathrm{Eom}\ \mathrm{C10}\ \mathrm{C11}\ \overline{\mathrm{C9}}$$

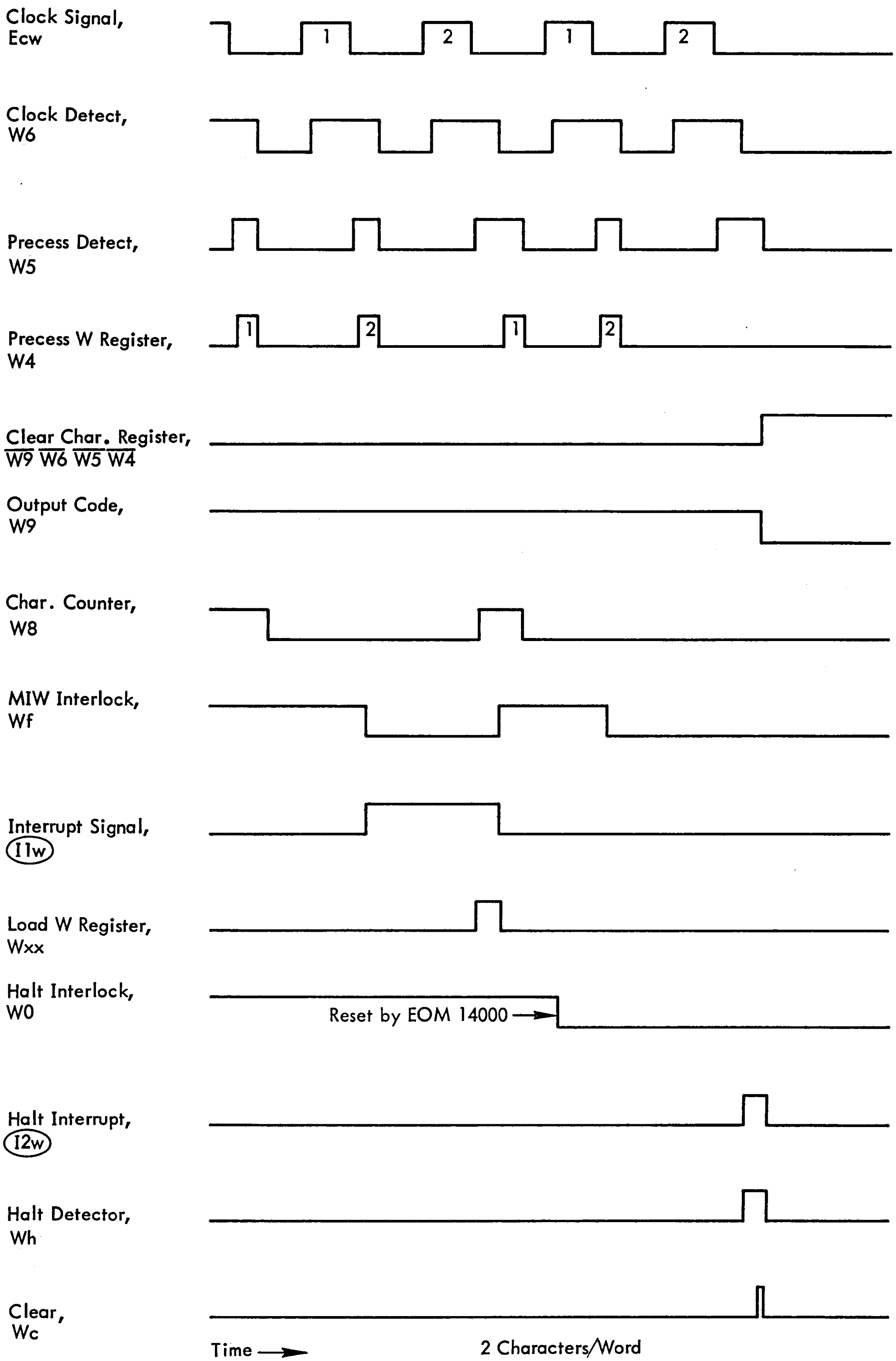


Figure 3-19. Output Termination Timing (Except Magnetic Tape)

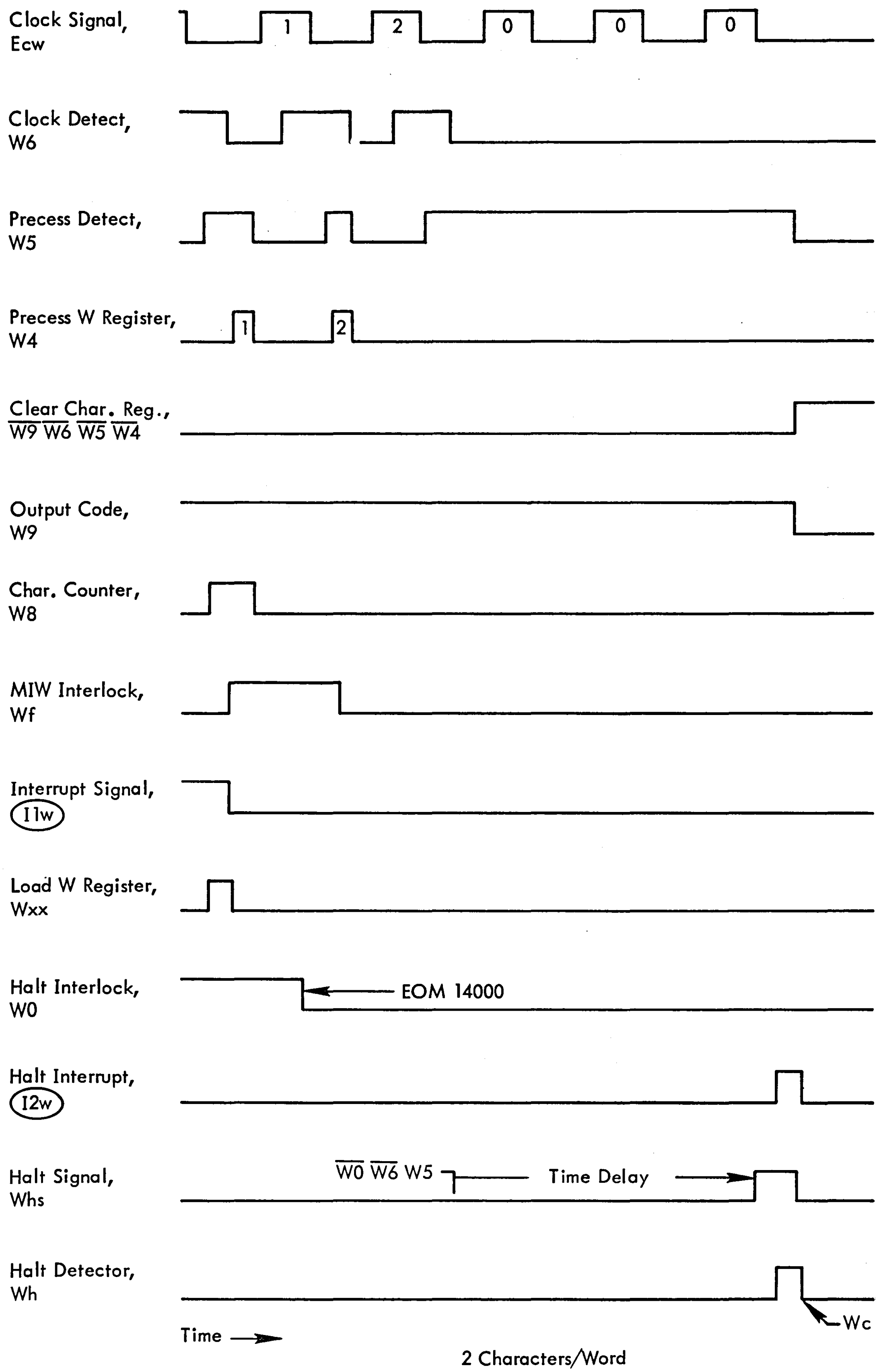


Figure 3-20. Output Termination Timing - Magnetic Tape

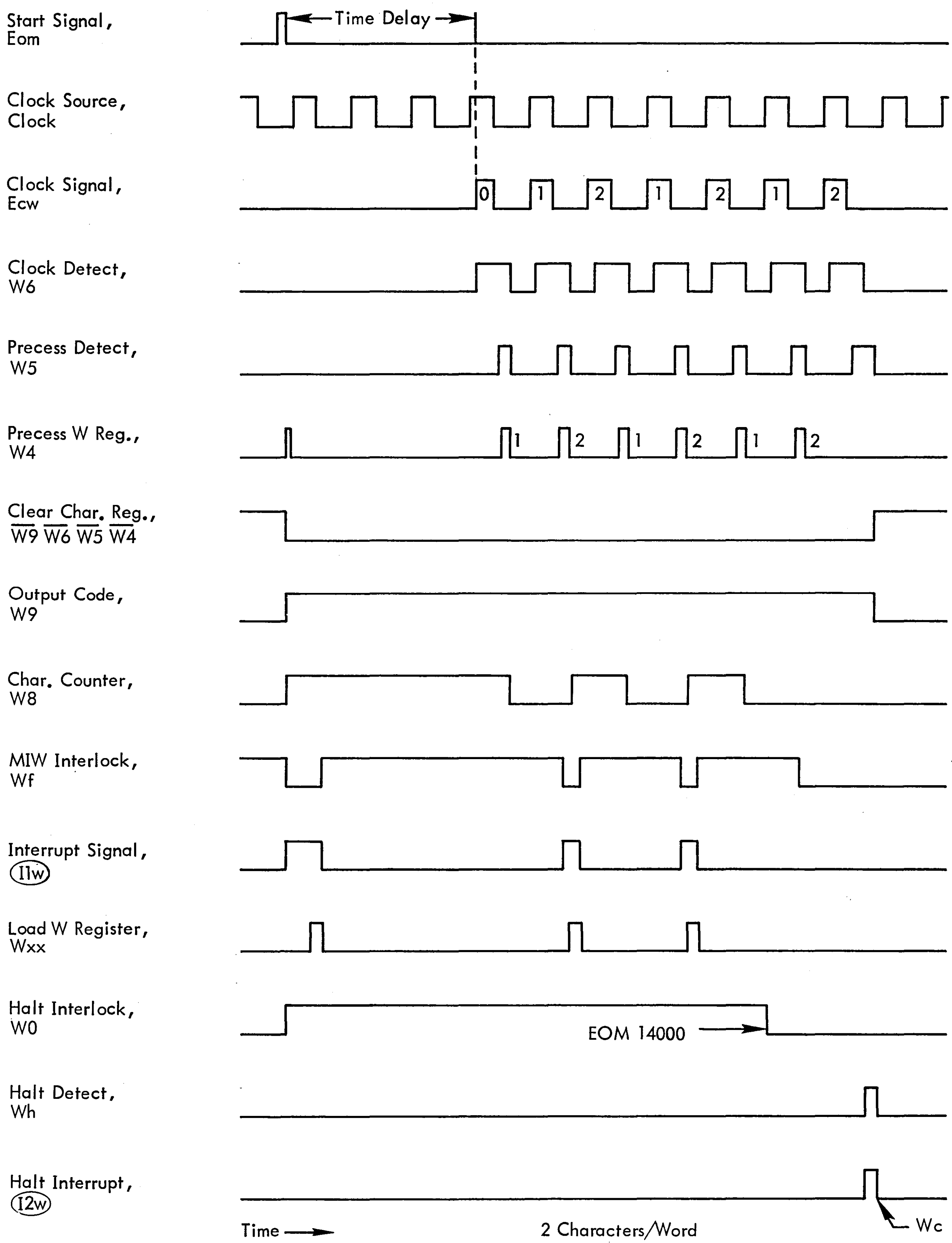


Figure 3-21. Output Timing Chart - Punch

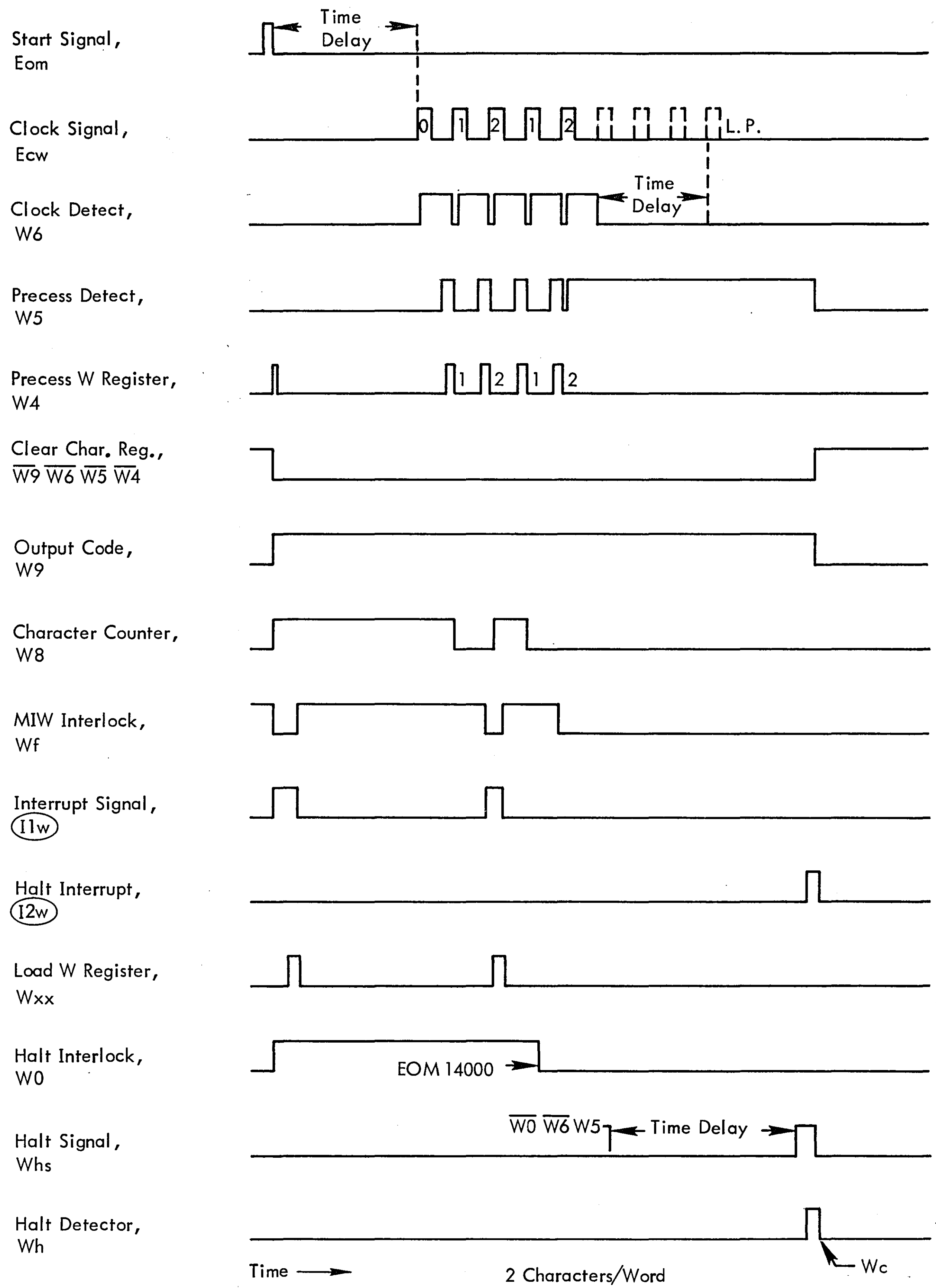


Figure 3-22. Output Timing Chart - Magnetic Tape

$$(Sys) = \overline{\overline{Sys\ (T5 - T1)\ \overline{Tsr}\ Pwy}}$$

(delete Pwy for 92200 and 92210)

The (Sys) signal may be used in conjunction with the C-Register output lines (C0) through (C24) to select and control special system devices. One (Sys) line is provided on each TMCC W (A) channel or each W(A) + Y(B) channel pair. One more (Sys) line is provided on the C or C + D channels (for a maximum of two lines).

3.94 SKIP GATE

3.95 The Skip Gate, Skr, and its associated line driver, $/\overline{Skrz}/$, provide interrogation response signals for use with SKS instructions.

The equation for the line driver is:

$$/\overline{Skrz}/ = \overline{Skr}\ \overline{(C10\ C11\ Ssc)}\ \overline{(\overline{C1}\ \overline{C9}\ \overline{C10}\ C11\ Sio)}\ \ldots *$$

*$\overline{C1}$ becomes C1 for TMCC-C and TMCC-D

This signal is inverted in the CPU and sampled during execution of an SKS instruction to determine if a response has been received. At times other than when being tested, the signal is changing levels and has no meaning. The inverse of $/\overline{Skrz}/$ is:

$$Skrz = Skr + C10\ C11\ Sec + \overline{C1}\ \overline{C9}\ \overline{C10}\ C11\ Sio + \ldots$$

3.96 The dashed lines indicate that other response signals may be connected to satisfy special system requirements. Sio is a response from the addressed peripheral I/O unit. The addressing is performed using SKS instruction bits 18 through 23 and the same address codes as assigned for EOM instructions. The output lines (C0) through (C24) provide the necessary addressing and control connections to the peripheral units. As seen above, Sio is used in conjunction with $\overline{C1}\ \overline{C9}\ \overline{C10}$ C11. Bits 1 and 9 (along with bit 17 decoded by the peripheral device) select one channel out of four TMCC and four DACC channels. Bits 10 and 11 determine the type of the SKS instruction.

3.97 Ssc is an interrogation response from external system equipment. This type of interrogation is selected by an SKS instruction with "ones" in bits 10 and 11. The control and address bits may be assigned as required. Again the (C0) - (C24) lines provide the necessary connections.

3.98 The remaining term in Skrz is Skr, the output of the Skip-Gate in the TMCC. The use of Skr is similar to that of Sio just described except the SKS instruction address bits (19-23) are "zeros". This causes the instruction to address the I/O channel itself rather than peripheral devices.

$$\begin{aligned} Skr = {} & \overline{C1}\ \overline{C17}\,\overline{C9}\,\overline{C10}\,C11\,\overline{C19}\,\overline{C20}\,\overline{C21}\,\overline{C22}\,\overline{C23}\,C15\,Wsc \\ & + \overline{C1}\,\overline{C17}\,\overline{C9}\,\overline{C10}\,C11\,\overline{C19}\,\overline{C20}\,\overline{C21}\,\overline{C22}\,\overline{C23}\,C12 \\ & \quad \overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14} \\ & + \overline{C1}\,\overline{C17}\,\overline{C9}\,\overline{C10}\,C11\,\overline{C19}\,\overline{C20}\,\overline{C21}\,\overline{C22}\,\overline{C23}\,C13\,Iwf \\ & + \overline{C1}\,\overline{C17}\,\overline{C9}\,\overline{C10}\,C11\,\overline{C19}\,\overline{C20}\,\overline{C21}\,\overline{C22}\,\overline{C23}\,C14\,\overline{We} \end{aligned}$$

3.99 In these equations, bits 1, 9, and 17 select one of eight channels (TMCCs and DACCs). Bits 10 and 11 determine the type of SKS instruction. "Zeros" in bits 19 through 23 address the channel rather than a peripheral unit. Bits 12, 13, 14, and 15 select the particular test function. A "one" in bit 15 tests the Signal-Complete flip-flop. Similarly, a "one" in bits 12, 13, or 14 tests the Unit Address Register, the Interlace Address Register, or the Error Flip-Flop, respectively.

3.100 Two additional TMCC channel tests, similar to two of those just described, are provided by the Skr gate. These also test the Unit Address Register and the Error Flip-Flop but with a different type of SKS instruction. This is done to provide program compatibility with the SDS 910/920 Computers.

$$\begin{aligned} Skr = {} & C10\ \overline{C11}\ C14\ \overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}\ \overline{C1} \\ & + C10\ \overline{C11}\ C20\ \overline{We}\ \overline{C1} + \ldots \end{aligned}$$

3.101 The equations shown in this discussion are specifically applicable to the W(A) channel TMCC. To select the other channels C1 must replace $\overline{C1}$ for channels C and D. To distinguish between W and Y or between C and D, C17 is switched (except in the last two equations where C14 and C20 are used for W and are changed to C13 and C19 for the Y channel).

3.102 INTERLACE, COMPATIBLE MODE (Time Share)

3.103 The Interlace register is enabled by a "one" in bit position 9 of either BUC or IOC type of EOM instruction. These produce Buc or Ioc signals which are derived from EOM0XXXX and EOM1XXXX instructions, respectively. Therefore, the interlace register can be enabled by the same instruction that sets up the other TMCC registers, (i.e., by Buc), or it can be enabled without disturbing the rest of the TMCC, (i.e., by Ioc). Either of the EOM instructions clears the entire interlace register then sets the Enable Flip-Flop, Ew.

Interlace Clear: $Iwc = Eom\ C9\ \overline{C10}\,\overline{C1}\,\overline{C17}\ (T3 - T0)$

$\overline{C1}$ Becomes C1 for TMCC-C

Interlace Prepare: $sEw = Iwc\ \overline{Ew}\ (T3 - T0)$

$$rEw = Wc\ T0 + \ldots$$

3.104 For a Buc instruction, Ew is first reset by Wc at pulse time T0 then reset during the next pulse time. The above equation for Iwc is specifically related to the W(A) channel. To select any of the other three TMCC channels, different combinations of C1 and C17 are used.

Channel	C1	C17
W(A)	0	0
Y(B)	0	1
C	1	0
D	1	1

With Ew set, the computer can preset the interlace register with the starting memory address and the word count for an I/O process. Refer to figure 3-23. The loading of these counts is accomplished by a POT instruction. The POT instruction, which produces a Pot1 signal, is ordinarily used to parallel transfer data from the C-Register to an external device. Pot1, then, produces the loading signal,

$$Iwp = Pot1\ (T6 + T5)\ Ew$$

then resets Ew,

$$rEw = Pot1\ (T3 - T0)\ Ew + \ldots$$

3.105 The Word Counter, Wc0 through Wc14, is initially cleared by Iwc which sets all stages of the counter. The one's complement of the count is then produced by resetting the counter flip-flops for corresponding "ones" in the C-Register during Iwp. Actually, this applies to only the ten least significant bits of the counter. If a word count greater than 1023 is needed, the five most significant bits of the counter must be preset by a second EOM instruction. This instruction must be executed after the Interlace is enabled and before the POT instruction is executed. An Ioc instruction, without bit 9, is given for this purpose and it generates an Iwe load signal.

$$Iwe = Ioc1\ (T6 + T5)\ Ew$$

Iwe then resets the most significant bits of the Word Counter to complete the storage of the one's complement count.

$$sWc14 = Iwc + \ldots$$

$$rWc14 = Iwp\ C9 + \ldots$$

$$\vdots$$

$$sWc5 = Iwc + \ldots$$

$$rWc5 = Iwp\ C0 + \ldots$$

$$sWc4 = Iwc + \ldots$$

$$rWc4 = Iwe\ C23 + \ldots$$

$$\vdots$$

$$sWc0 = Iwc + \ldots$$

$$rWc0 = Iwe\ C19 + \ldots$$

3.106 Using the one's complement, the Word Counter can count up rather than down and produce a termination signal when it contains "ones" in all of its stages. The counting is performed by triggering each stage of the counter on the falling edge of a previous stage. For example:

$$sWc13 = \overline{Ew}\ \overline{Wc13}\ \underline{Wc14\ \overline{Ew}}$$

$$rWc13 = \overline{Ew}\ Wc13\ \underline{Wc14\ \overline{Ew}}$$

where the underlined term represents the clock or triggering level. This method of counting conserves gating but produces a propagation delay through the counter. This delay is minimized to a satisfactory level with some increase in the number of gates by arranging the fifteen counter stages into five octal groups. The first stage of each group is connected to only the last stage of the previous group. An example of one octal group is:

$$sWc10 = \overline{Ec}\ \overline{Wc10}\ \underline{Wc11\ \overline{Ew}}$$

$$rWc10 = \overline{Ec}\ Wc10\ \underline{Wc11\ \overline{Ew}}$$

$$sWc9 = \overline{Ew}\ \overline{Wc9}\ Wc10\ \underline{Wc11\ \overline{Ew}}$$

$$rWc9 = \overline{Ew}\ Wc9\ Wc10\ \underline{Wc11\ \overline{Ew}}$$

$$sWc8 = \overline{Ew}\ \overline{Wc8}\ Wc9\ Wc10\ \underline{Wc11\ \overline{Ew}}$$

$$rWc8 = \overline{Ew}\ Wc8\ Wc9\ Wc10\ \underline{Wc11\ \overline{Ew}}$$

Here it is seen that for this octal group, a common clock term $\underline{Wc11\ \overline{Ew}}$ is used for all three stages.

3.107 This reduces the propagation delay for each group to the delay that would be expected for a single flip-flop. The delay for the entire fifteen stage counter is therefore equivalent to that of five flip-flop stages. The double appearance of $\overline{Ew}$ is due to the clocking arrangement and the flip-flop module layout. During the loading operations, Ew is set to allow the clock pulses to appear as the Gc4 clock for use by the flip-flop. After Ew is reset and the counting is to take place, Gc4 is held off while $\underline{\overline{Ew}.Wc14}$ performs the triggering. Refer to figure 3-24.

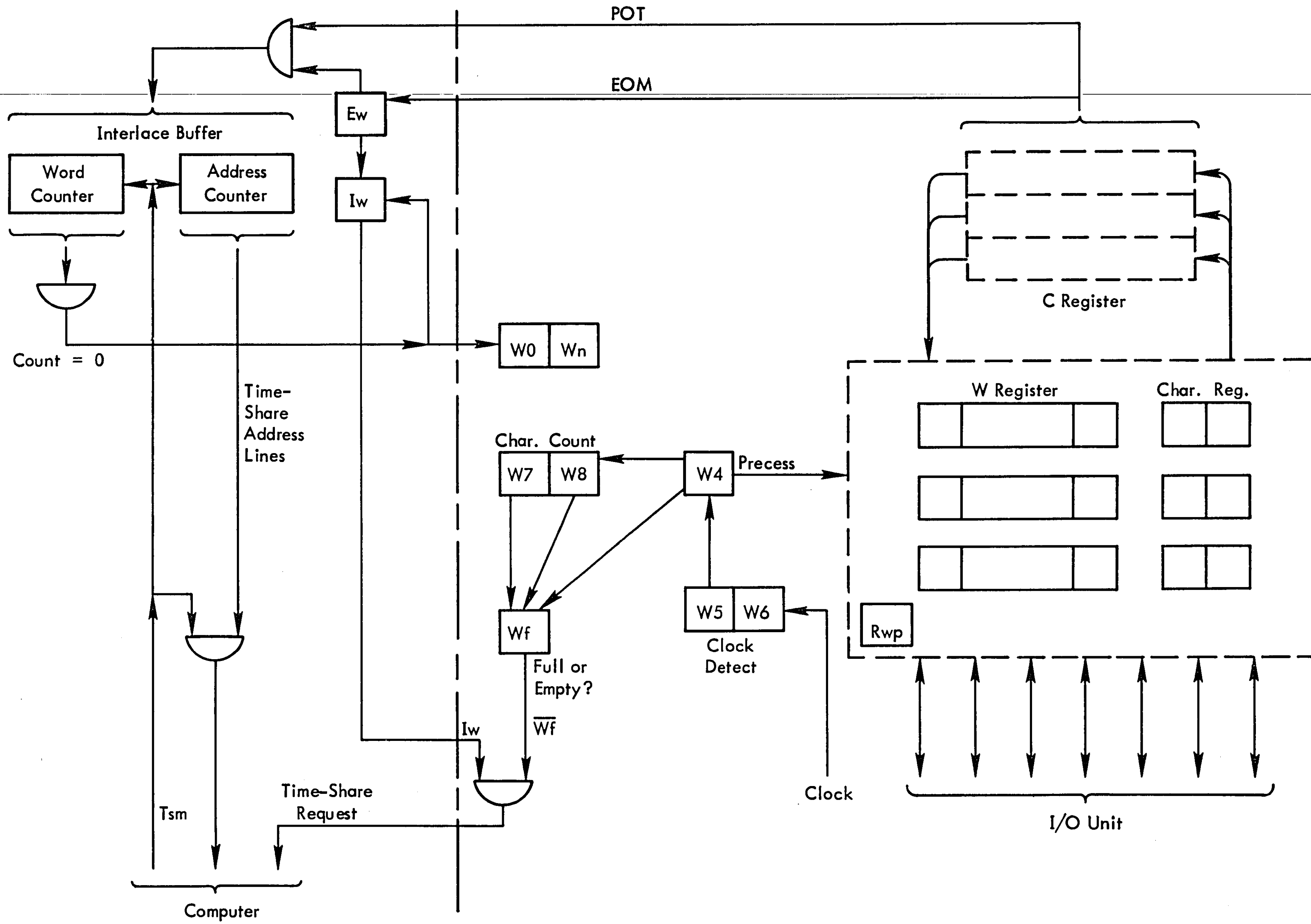


Figure 3-23. Information Flow - Interlace Operation

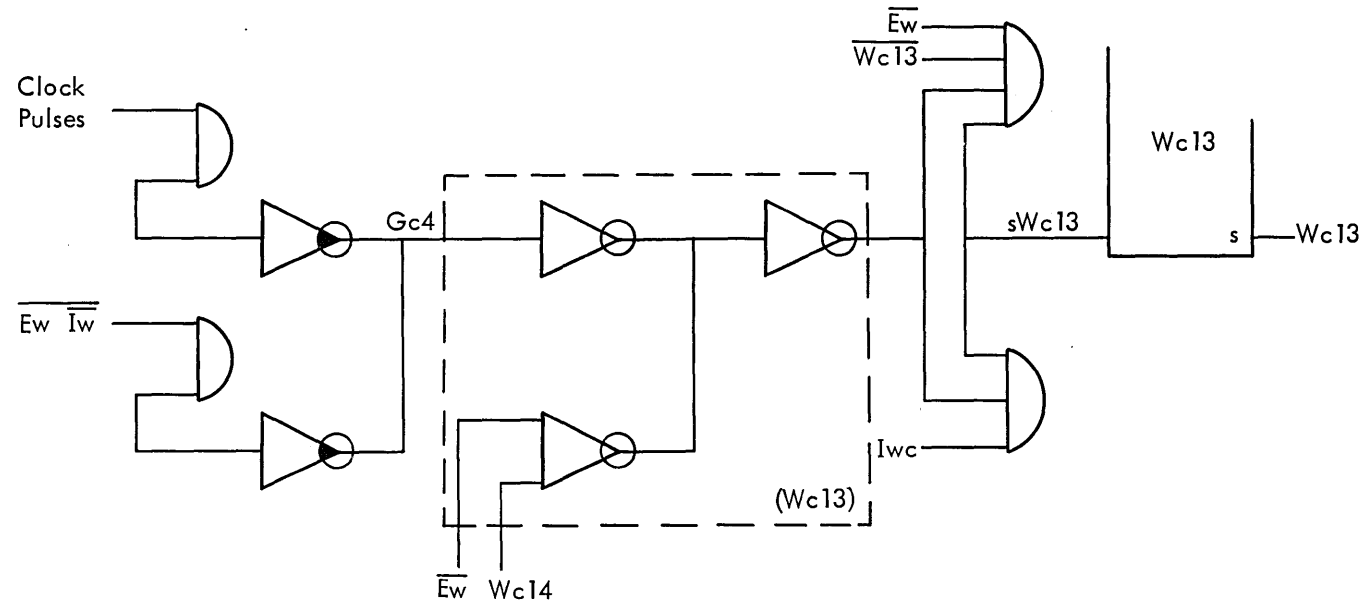


Figure 3-24. Interlace Word Counter - Typical Clock Input

3.108 The Address Counter is set up in much the same way as the Word Counter. Again the counter counts up, but in this case the one's complement is not used. With the Address Counter, the actual address of the first memory location to be used is placed in the register. As with the Word Counter, Iwc clears the counter then Iwp or Iwe sets up each stage with data from the C-Register. For some stages of the counter, the flip-flops are reset by Iwc then set with the data. For other stages, the flip-flops are set by Iwc then reset with the complement of the data. Either way, the same thing is accomplished. It was a matter of convenience in wiring for one method or the other to have been used.

3.109 The counting of the Address Counter is handled in the same way as the Word Counter. The least significant stages of both counters are triggered by $\underline{Iwa\ \overline{Ew}}$.

$$Iwa = Rxw\ Tsm$$

Rwx is the Time Share Select Flip-Flop and is covered in detail in paragraph 3.113. Tsm is a signal from the CPU indicating that counter information for each word has been received by the CPU.

3.110 In the instruction sequence, EOM, EOM, POT, used to set up and start the interlace operation, the second EOM may be omitted if the most significant bits of the Word and Address Counters are "zeros". Refer to figure 3-25 for the relationship between the instruction bits stored in the C-Register and their respective positions in the counters.

3.111 The POT instruction which resets the Interlace Prepare Flip-Flop, Ew, also sets the Interlace Active Flip-Flop, Iw.

$$sIw = Pot\ 1\ (T3 - T0)\ Ew\ \overline{Iw}$$

Ew furnishes the ready signal required for the POT instruction. Both the Ew and Iw flip-flops inhibit W-channel interrupts.

$$I1w = \overline{Wf}\ W0\ \overline{Wh}\ (En + \textcircled{En})$$
$$\overline{Iw}\ \overline{Ew}\ \overline{Iwg}$$

3.112 Refer to figure 3-26 for the timing for the interlace loading process. The Interlace Active Flip-Flop, Iw, allows the buffer to issue a time share request (Trqw) to the CPU whenever the channel needs access to memory.

$$Trqw = \overline{Wf}\ W0\ \overline{Wh}\ Iw\ \overline{Iwf}$$

Trqw is combined with similar signals from the other channels to produce a common request term for all TMCC's.

$$Trqx = Trq(c) + Trq(d)$$
$$Trq = Trqx + Trqw + Trqy$$

	2nd EOM					POT									
Word Counter	Wc0	Wc1	Wc2	Wc3	Wc4	Wc5	Wc6	Wc7	Wc8	Wc9	Wc10	Wc11	Wc12	Wc13	Wc14
C Register	C19	C20	C21	C22	C23	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9

Address Counter	Wa0	Wa1	Wa2	Wa3	Wa4	Wa5	Wa6	Wa7	Wa8	Wa9	Wa10	Wa11	Wa12	Wa13	Wa14
C Register	C18	C11	C12	C13	C14	C15	C16	C17	C18	C19	C20	C21	C22	C23	C24

Figure 3-25. Relationship of Instruction Bits to Address and Word Counter Bits

3.113 When two or more TMCC's make a time share request at the same time or when one channel makes a request while another is already performing a time share operation, the TMCC priority logic determines which channel is allowed to access memory first. For this purpose, each channel has its own Time Share Select flip-flop. No more than one of these flip-flops may be set at any time. The priority established by the flip-flops for the four TMCC channels is D, C, Y, and W in descending order. However, once a channel has been selected, it is allowed to complete the processing of its word without being disturbed by other channels. Using the Time Share Request signals mentioned previously, the priority logic to select the channel is:

Channel W; $sRwx = \overline{Tsm}\ Trqw\ \overline{Trqy}\ \overline{Trqx}\ (T7 - T0)$

$rRwx = \overline{Tsm}\ T0$

Channel Y; $sRyx = \overline{Tsm}\ Trqy\ \overline{Trqx}\ (T7 - T0)$

$rRyx = \overline{Tsm}\ T0$

3.114 The TMCC's for the C and D channels are identical to those for the W and Y channels and so use the same logic nomenclature as above. But a request signal, Trqx, is not brought into the C and D units from other higher priority TMCC's. Then, for simplicity the C and D channel equations may be written:

Channel C, $sRcx = \overline{Tsm}\ Trq\ (c)\ \overline{Trq\ (d)}\ \overline{(T7 - T0)}$

$rRcx = \overline{Tsm}\ T0$

Channel D, $sRdx = \overline{Tsm}\ Trq\ (d)$

$rRdx = \overline{Tsm}\ T0$

The terms Rcx and Rdx are used here for clarity but do not actually appear in the logic equations for the equipment.

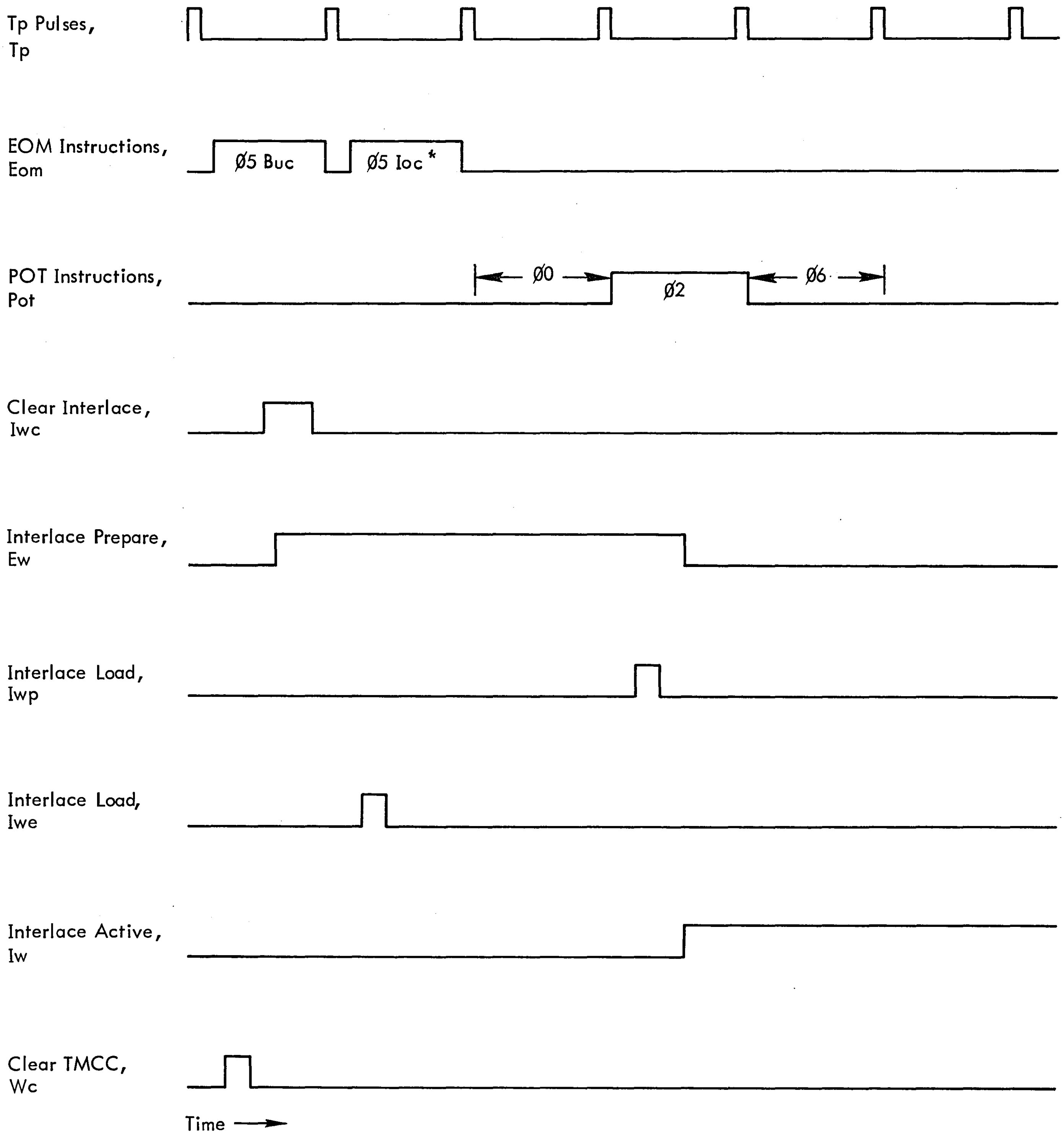
3.115 If a TMCC channel makes a time share request and has the highest priority of those making such a request, and if $\overline{Tsm}$ is true, then the channel can set its Time Share Select flip-flop. $\overline{Tsm}$ indicates that the CPU is not already engaged in a time share operation. Confining the discussion to the W channel, Rwx would set at pulse time Tr - T8.

3.116 The Interlace Prepare flip-flop (Ew) also produces Er which prevents output signals, Eom and Ioc, from reaching external devices while initializing the Interlace.

$$\overline{Er} = \overline{Ew}\ \overline{Ey}\ . . .$$

$$Ioc = Ioc\ 1\ \overline{C1}\ \overline{Er}\ Qr3$$

$$(Eom) = \overline{\overline{Eom\ \overline{Er}}}$$



*Second EOM may be eliminated if not needed to set count in most significant bits of Address and Word Counters or to set up the extended mode.

Figure 3-26. Interlace Register Loading Timing Chart

The CPU then answers the request with a Tsr signal which remains on for two machine cycles. Tsr enables Wxx to permit a data transfer between W and C registers. While Tsr is true, the CPU sets Tsm to increment the Word and Address Counters.

$$Iwa = Rwx\ Tsm = \text{count trigger}$$

$$Wxx = Rwx\ Tsr\ Iw = \text{load buffer from C}$$

3.117 Refer to figure 3-27 for the timing of the signals involved in the data transfer between the W and C Registers. Figure 3-27, indicates that Wxx remains on for two machine cycles. This allows the data exchange to take place twice. The two cycles are used as follows.

a. Input Operation. The first cycle exchanges the input word and any word currently in the C-Register. Then between cycles, the input word is copied from the C-Register into memory (in parallel). During the second exchange cycle, the word temporarily stored in the W-Register is returned to the C-Register where it can continue in whatever function it may have been participating.

b. Output Operation. The first cycle shifts any information which was being operated on in the C-Register to the W-Register for temporary storage. The word requested by the TMCC Interlace Address Counter is then parallel transferred from memory to the C-Register (between cycles). The second exchange cycle then returns the word from the W-Register back to the C-Register and brings the word out of memory from the C to the W-Register.

3.118 The double exchange cycle thus provides the TMCC with a means of:

a. moving a word from the W-Register through the C-Register to memory or vice versa, and

b. preserving the contents of the C-Register while the transfer takes place. This is important if the CPU is engaged in some form of computation when the time share takes place. Figure 3-28 is an illustration of the timing involved for a typical interlaced I/O process.

3.119 Another important aspect of the W and C-Register data exchange during an interlaced output concerns the path taken by the output word in getting to the W-Register. If a clock has read the last word out of the Character Register when the exchange takes place, the next word is precessed simultaneously with its transfer to the W-Register. This occurs as follows. During both of the exchange cycles, Wxx is on because of Rxw and Tsr.

$$Wxx = Rwx\ Tsr\ Iw + \ldots$$

3.120 If at this time a clock has already been detected (to read the last character of the previous word) so that W5 is set, W4 is set at pulse time T8 in the beginning of the second exchange cycle.

$$sW4 = W5\ Wf\ T8\ \overline{Wg}$$

3.121 Thus, during the second cycle, Wxx and W4 are both true. The output word may then be shifted directly from the C-Register to the Character Register and on through to the W-Register. A one cycle precession is thereby automatically accomplished and the character may be read by the next clock without waiting for another precession to take place.

$$sRw1 = W4\ Wxx\ C21r + \ldots$$

$$rRw1 = W4\ Wxx\ \overline{C21r} + \ldots$$

$$sRw2 = W4\ Wxx\ C22r + \ldots$$

$$rRw2 = W4\ Wxx\ \overline{C22r} + \ldots$$

$$sRw3 = W4\ Wxx\ C23r + \ldots$$

$$rRw3 = W4\ Wxx\ \overline{C23r} + \ldots$$

$$\left.\begin{aligned} Ww1 &= W4\ Wb1\ (T7 - T0) + \ldots \\ Ww2 &= W4\ Wb2\ (T7 - T0) + \ldots \\ Ww3 &= W4\ Wb3 + \ldots \end{aligned}\right\} \text{Refer to figure 3-3 for Wb1, Wb2, and Wb3.}$$

3.122 This same path for loading the W-Register through the Character Register is also followed when the interlace is initially set up and the first word is called for, if the EOM instruction calls for starting without leader. In this case W5 is first set by Ws C13 instead of a clock signal from the peripheral unit.

$$sW5 = Ws\ C13\ \overline{C18\ \overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}}$$

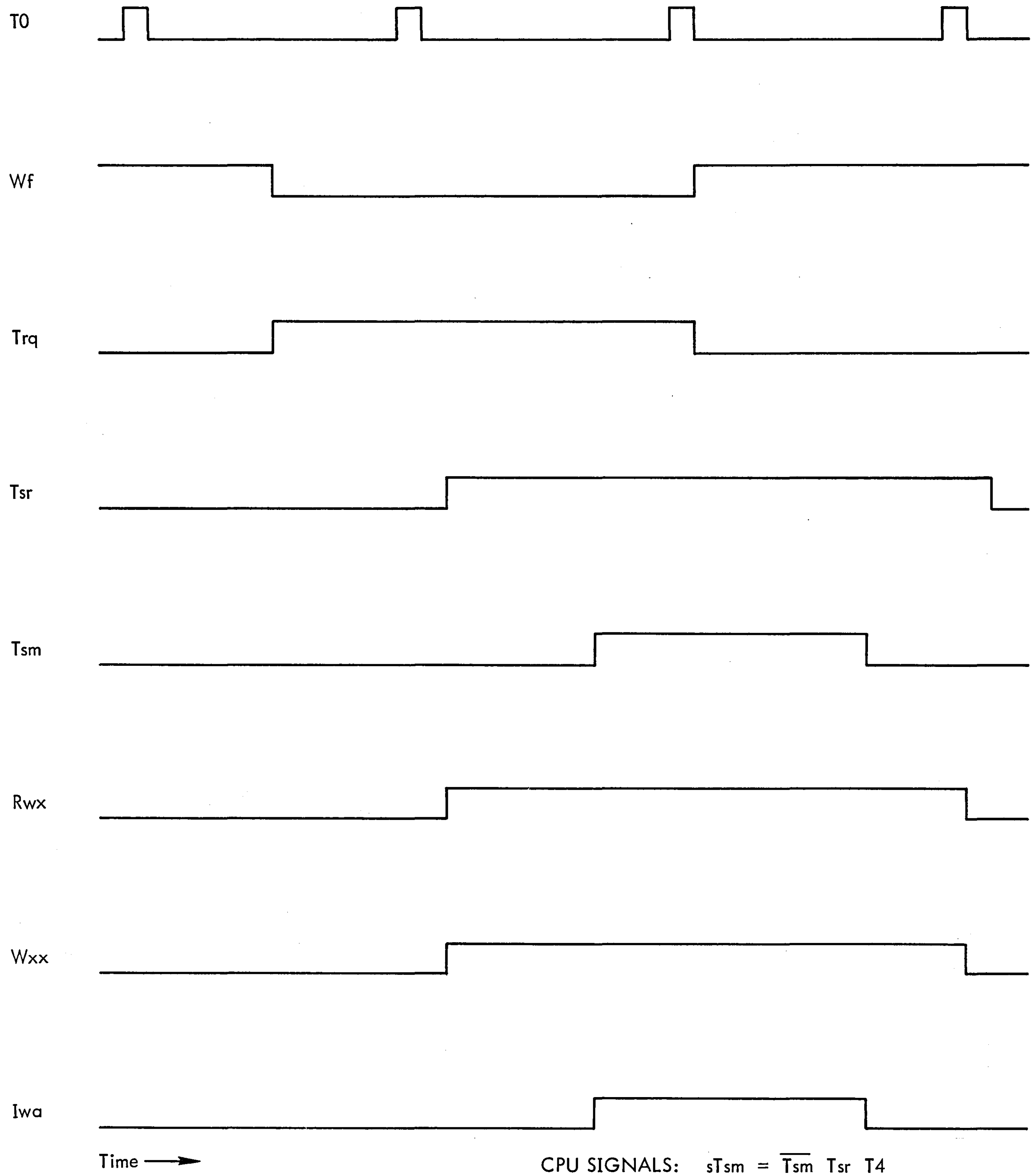
Figure 3-29 illustrates the use of this feature in loading the first word.

3.123 When transferring data directly from the C to the Character Register, the parity bit is generated as previously described except that Cpr is used in place of ($Wn1 \oplus Wn2 \oplus Wn3$). Cpr performs a similar function but originates in the CPU and monitors the parity of the octal groups coming from the C-Register rather than from the W-Register.

$$sRwp = W9\ W4\ \overline{Rwp}\ Wxx\ Cpr\ Qw2\ (T7 - T0) + \ldots$$

$$rRwp = W9\ W4\ Rwp\ Wxx\ Cpr\ Qw2\ (T7 - T0) + \ldots$$

Refer to figure 3-4 for Qw2.



CPU SIGNALS:

$sTsm = \overline{Tsm}\ Tsr\ T4$

$rTsm = Tsm\ \overline{(Ts\ \overline{Tsr})}\ T4$

$sTsr = \left[\overline{Mit}\ (Trq + Tsm)\right]\ Tr$

$rTsr = \left[Mit\ (Trq + Tsm)\right]\ Tr$

Figure 3-27. Interlace Word Transfer Timing Chart

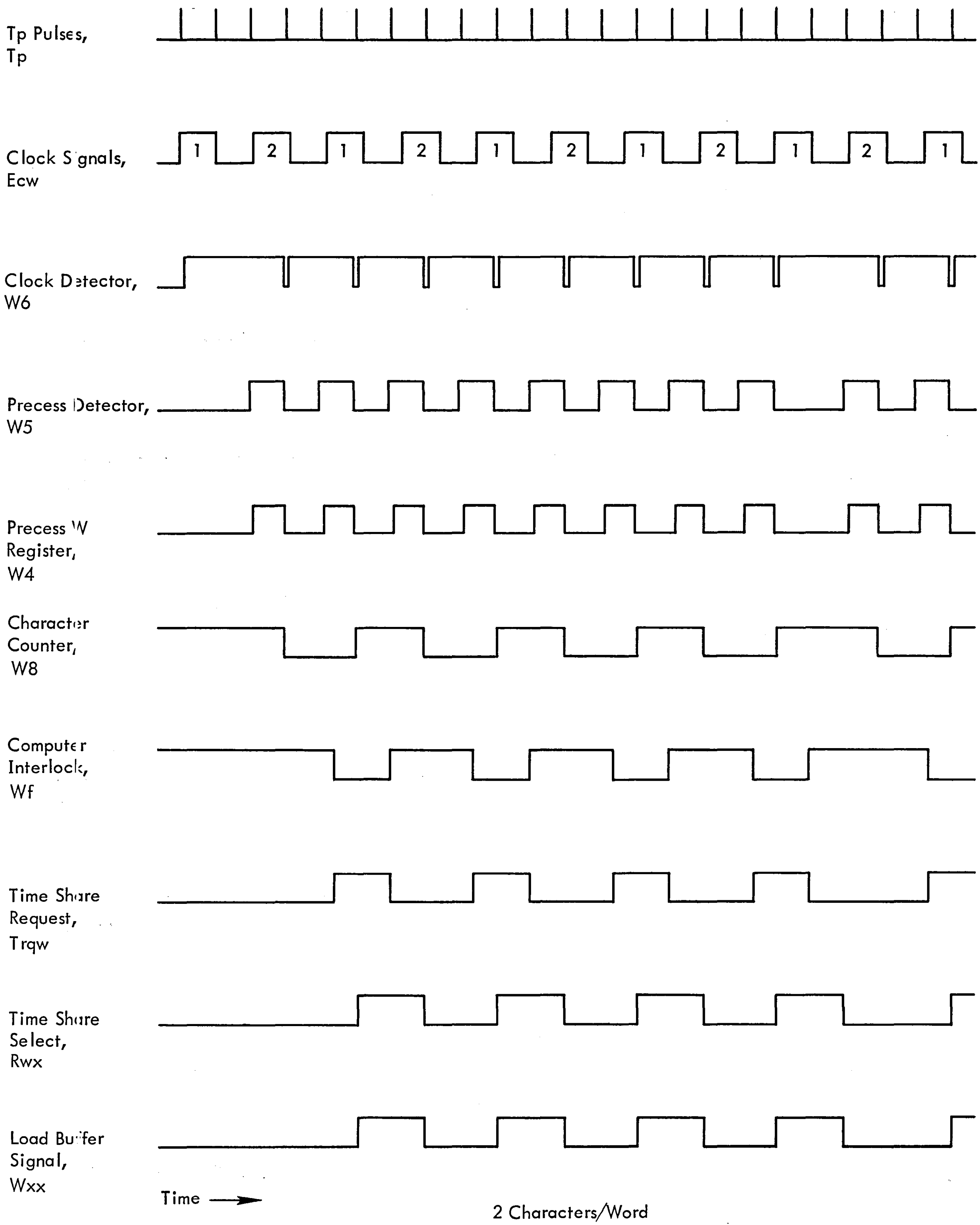


Figure 3-28. Interlace Input/Output Timing Chart

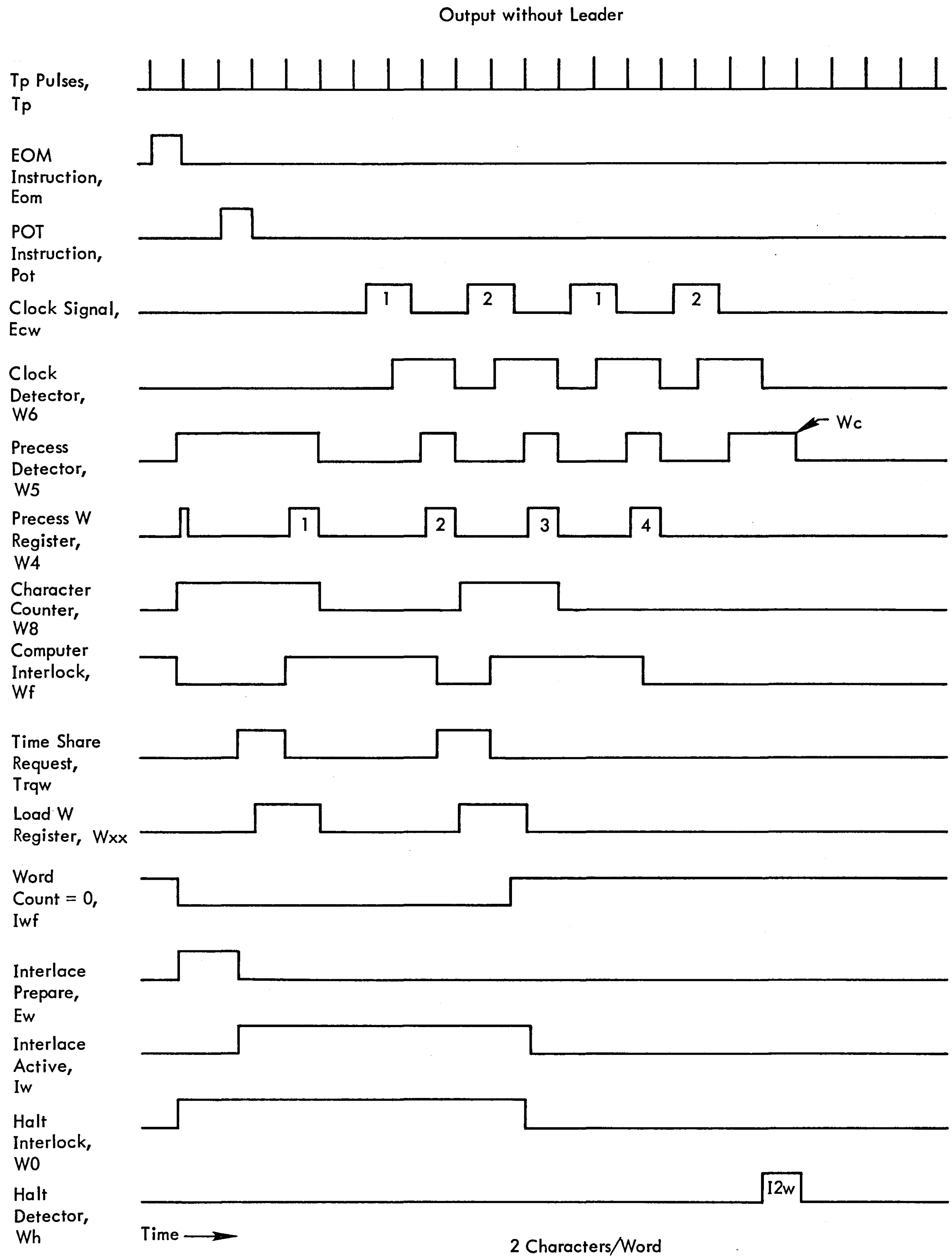


Figure 3-29. Interlace Output Timing Chart

3. 124 As each I/O word is processed, the Word and Address Counters are incremented by Iwa. Iwa also sets Wf again after it has issued the time share request via Trqw.

$$\text{Iwa} = \text{Rwx Tsm}$$

$$\text{sWf} = \text{Iwa } \overline{\text{Mit}} \text{ T0}$$

The term $\overline{\text{Mit}}$, when false, denotes that a direct access I/O channel (DACC) is accessing the memory. Since the DACC may require access during an I/O operation by the TMCC, $\overline{\text{Mit}}$ is used to momentarily stop the TMCC's action. Memory access by the DACC, although producing Tsm, thus cannot set Wf.

3. 125 When the Word Counter reaches the all "ones" condition, the count is decoded by Iwf.

$$\text{Iwf} = \text{Wc0 Wc1 Wc2 Wc3 Wc4 Wc5 Wc6 Wc7 Wc8 Wc9 Wc10 Wc11 Wc12 Wc13 Wc14 } \overline{\text{Ew}}$$

Iwf inhibits further time share request signals and resets the Interlace Active flip-flop.

$$\text{Trqw} = \overline{\text{Wf}} \text{ W0 } \overline{\text{Wh}} \text{ Iw } \overline{\text{Iwf}} = \text{time share request}$$

$$\text{rIw} = \text{Iwf T8} = \text{Interlace Active}$$

3. 126 If the Interlace is controlling an input process, the next word loaded into the W-Register after Iw is reset, generates a Word Ready Interrupt, I1w.

$$\text{I1w} = \overline{\text{Wf}} \text{ W0 } \overline{\text{Wh}} \text{ (En} + \textcircled{\text{En}}) \ \overline{\text{Iw}} \ \overline{\text{Ew}} \ \overline{\text{Iwg}}$$

At this time the program can reload the interlace if reading is to continue. On channel W (or Y) the contents of the buffer can be stored with a WIM (or YIM) instruction.

3. 127 During the input process, if an End-of-Record is encountered before the word count is completed, termination takes place as described earlier for the non-interlaced input. Wg detects the gap and sets Wh.

$$\text{sWh} = \text{Wg } \overline{\text{Iwg}} \text{ T8}$$

An interrupt is generated and the TMCC is cleared in the usual manner.

$$\text{I2w} = (\text{En} + \textcircled{\text{En}}) \ \overline{\text{Iwg}} \text{ Wh } \overline{\text{Wf}} + \ldots$$

3. 128 If the Interlace is controlling an output process, Iwf resets the Halt Interlock flip-flop, W0, and blocks I1w and Trqw.

$$\text{rW0} = \text{W9 Iw Iwf } (\overline{\text{Iwg}} + \ldots) \ (\overline{\text{T7} - \text{T0}})$$

$$\text{I1w} = \overline{\text{Wf}} \text{ W0 } \overline{\text{Wh}} \text{ (En} + \textcircled{\text{En}}) \ \overline{\text{Iw}} \ \overline{\text{Ew}} \ \overline{\text{Iwg}}$$

$$\text{Trqw} = \overline{\text{Wf}} \text{ W0 } \overline{\text{Wh}} \text{ Iw } \overline{\text{Iwf}}$$

Thus, Rwx is not set again and Iwa cannot be turned on.

$$\text{sRwx} = \overline{\text{Tsm}} \text{ Trqw } \overline{\text{Trqy}} \ \overline{\text{Trqx}} \ (\overline{\text{T7} - \text{T0}})$$

$$\text{Iwa} = \text{Rwx Tsm}$$

Then when the last word is precessed out of the W-Register, Wf is not set again.

$$\text{sWf} = \text{Iwa } \overline{\text{Mit}} \text{ T0}$$

This results in a situation similar to that for the non-interlaced output. The condition, $\overline{\text{W0}}\ \overline{\text{W4}}\ \text{W5}\ \overline{\text{W6}}$, exists following the precession of the last character. The state, $\overline{\text{W0}}\ \text{W5}\ \overline{\text{W6}}$, then sets Wh. Or, if magnetic tape is being used, $\overline{\text{W0}}\ \text{W5}\ \overline{\text{W6}}$ is detected by the tape unit and after a delay, Whs is generated to set Wh.

$$\text{sWh} = \text{W9 } \overline{\text{W11}} \ \overline{\text{W0}} \text{ W5 } \overline{\text{W6}} \ (\overline{\text{Iwg}} + \ldots) \text{ T8} + \text{Whs W11 T8} + \ldots$$

Then, halt interrupt and clear signals are generated and the TMCC, including Wh, is reset.

$$\text{I2w} = (\text{En} + \textcircled{\text{En}}) \ \overline{\text{Iwg}} \text{ Wh } \overline{\text{Wf}} + \ldots$$

$$\text{Wc} = \text{Wh } \overline{\text{Wf}} \text{ (T3} - \text{T0)} + \ldots$$

$$\text{rWh} = \text{Wh } \overline{\text{Wf}} \text{ T8} + \ldots$$

3. 129 The termination timing for a typical interlaced input process is illustrated in figure 3-30. In general, termination of a Compatible Mode I/O process is much the same as that for a non-interlaced I/O operation, but figure 3-30 illustrates the relationship of the additional interlace signals involved with those shown in earlier figures.

3. 130 As with other forms of I/O operation, a disconnect EOM (address 00) can also terminate an interlaced operation. This is done by resetting the Interlace Active Flip-Flop and the Extend Operations Flip-Flop through Ws and Wsc. (Refer to the paragraphs on Extended Mode beginning with 3-100 for explanation of Iwg.)

$$\text{rIw} = \text{Ws } \overline{\text{C19}} \ \overline{\text{C20}} \ \overline{\text{C21}} \ \overline{\text{C22}} \ \overline{\text{C23}} \text{ (T3} - \text{T0) Iw} + \ldots$$

$$\text{rIwg} = \text{Wsc T8 } \overline{\text{W10}} \ \overline{\text{W11}} \ \overline{\text{W12}} \ \overline{\text{W13}} \ \overline{\text{W14}} \text{ Iwg} + \ldots$$

$$\text{sWsc} = \text{Ws } \overline{\text{C19}} \ \overline{\text{C20}} \ \overline{\text{C21}} \ \overline{\text{C22}} \ \overline{\text{C23}} + \ldots$$

3.131 INTERLACE, EXTENDED MODE (Time Share)

3. 132 The Word Counter and Address Counter set-up procedures are similar for both the Compatible and Extended

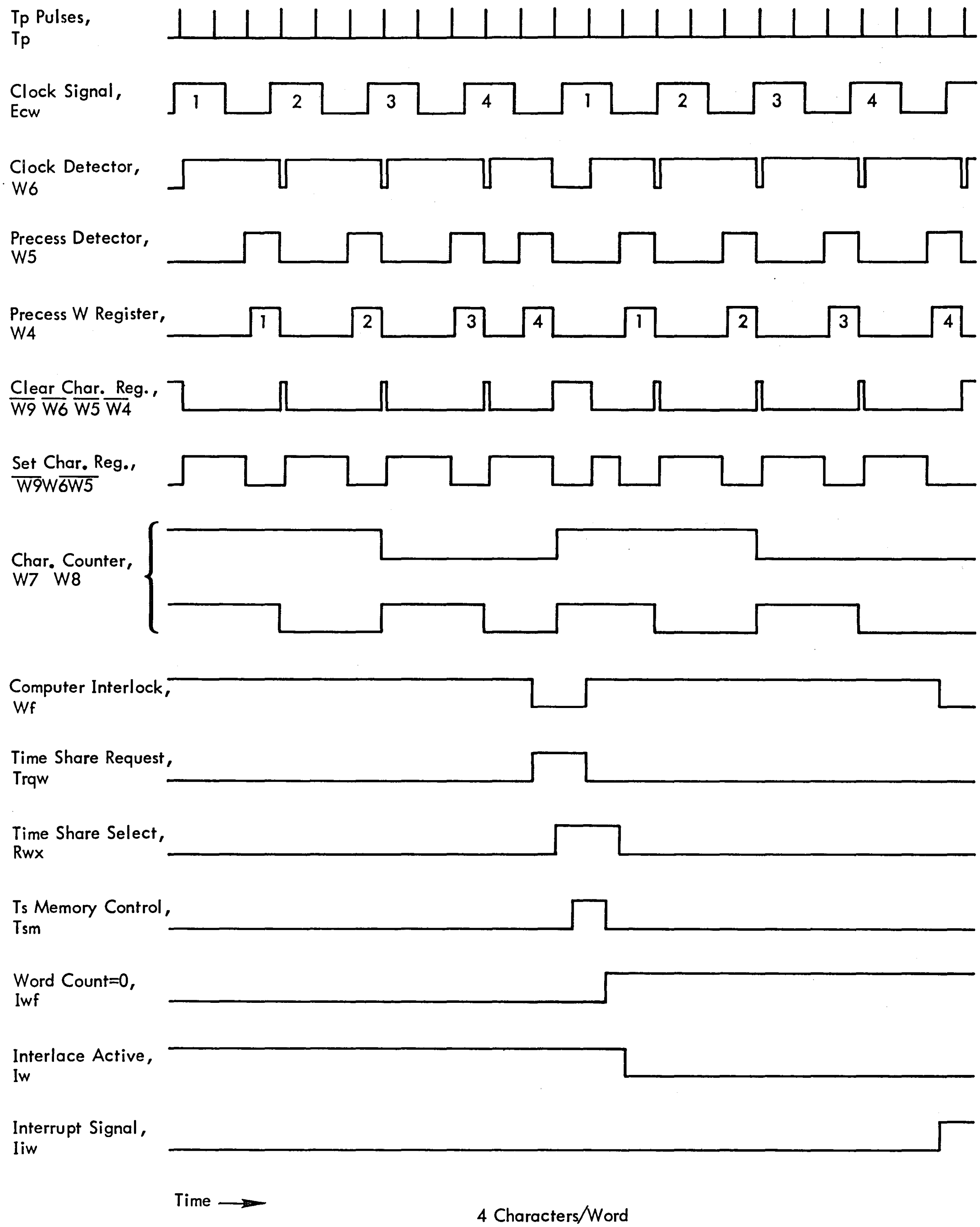


Figure 3-30. Input Termination Timing Chart - Interlace (Compatible Mode)

Modes. That is, the same sequence of instructions is used, (EOM-EOM-POT). However, to select the Extended Mode of operation, it is necessary to place a "one" in bit 12 of the second EOM (Ioc) instruction. When this instruction is processed, the Iwe loading signal sets bit 12 into the Extended Operations Flip-Flop, Iwg.

$$Iwe = Ioc\ 1\ (T6 + T5)\ Ew$$

$$sIwg = Iwe\ C12$$

Prior to this, Iwg was cleared by the first EOM instruction as was the rest of the Interlace logic.

$$Iwc = Eom\ C9\ \overline{C10}\ \overline{C1}\ \overline{C17}\ (T3 - T0) \quad \overline{C1} \text{ becomes C1 for TMCC-C}$$

$$rIwg = Iwc + \ldots$$

3.133 To use the Extended Mode, four additional flip-flops are loaded by the Ioc instruction. Two of these, Iwh and Iwi, comprise the Channel Command Register which selects the type of termination. The remaining two flip-flops, Iwj and Iwk, are employed to arm the I2w and I1w interrupts on a selective basis.

$$sIwj = Iwe\ C13$$

$$rIwj = Iwc + \ldots$$

$$sIwk = Iwe\ C14$$

$$rIwk = Iwc + \ldots$$

$$sIwh = Iwe\ C15$$

$$rIwh = Iwc$$

$$sIwi = Iwe\ C16$$

$$rIwi = Iwc$$

By decoding Iwj and Iwk, the Extended Mode can perform the four different terminal functions listed in table 3-4. Each function can be used to control either an input or an output operation. In the following paragraphs, each of the four functions is discussed in detail. In each case, it is assumed that the interlace registers have already been loaded by the EOM-EOM-POT instructions and that the interlaced I/O operation is proceeding normally.

3.134 IORD - Iwg $\overline{Iwh}$ $\overline{Iwi}$

3.135 <u>Output</u>

3.136 Write C words. When C equals zero, output is terminated (i.e. the device is signaled that the last characters have been transmitted). When the peripheral device has generated the End-of-Record and, if necessary, checked the validity of the record, it sends an End-of-Record response to the channel buffer. When received by the buffer, the End-of-Record signal generates an End-of-Record interrupt (if armed) and disconnects the channel.

3.137 The line printer generates the End-of-Record response when it completes the printing of a line. If the printer encounters any print errors or faults, it sends a signal to the channel that sets the channel error indicator. This can occur since the printer has not disconnected from the channel. The IORD is useful when the program is to print several lines and the program is not otherwise to use the channel between lines. When the printer completes each line, it causes an End-of-Record interrupt (assumed to be armed), notifying the program that it can immediately transmit the next paper control instruction and the next line image.

3.138 The unbuffered card punch operates similarly. It generates the End-of-Record response after punching each row. If any faults occur during the punching of the entire card, the card punch sends a signal to the channel that sets the channel error indicator; this occurs after punching the last row (row 9).

NOTE

A program should not use IORD with devices that do not have End-of-Record conditions on output (e.g., devices such as the paper tape punch and typewriter). These devices to terminate output but give the program no indication when they receive the last characters.

After the last word is accessed from memory, zero word count is established.

3.139 The interlace is counted by the Interlace Count Trigger, Iwa.

$$Iwa = Rwx\ Tsm$$

Zero Word Count, Iwf, occurs and the Interlace Active flip-flop, Iw is reset.

$$Iwf = Wc0\ Wc1\ \ldots\ Wc13\ Wc14\ \overline{Ew}$$

$$rIw = Iwf\ T8$$

The Halt Interlock, W0, is reset.

$$rW0 = W9\ Iw\ Iwf\,(\overline{Iwg} + \overline{Iwh} + \overline{Iwi})\ (\overline{T7 - T0}) + \ldots$$

If the End-of-Transmission Interrupt Enable, Iwk, has been previously armed, an I1w interrupt occurs and Iwk is reset.

$$I1w = Iwg\ \overline{Iw}\ Iwf\ Iwk + \ldots$$

Table 3-4. Interlace Extended - Mode Terminal Functions

Terminal Function	Iwg	Iwh	Iwi	Summary of Operation
IORD Input/Output of record then disconnect.	1	0	0	The I/O operation proceeds until the word count equals zero then terminates. On input, the channel disconnects when the End-of-Record is encountered. On output, the channel signals the device that the last character has been transmitted then disconnects after the device provides an End-of-Record response.
IOSD Input/Output until signal then disconnect.	1	0	1	The channel disconnects when the word count equals zero or at the end of a record.
IORP Input/Output of a record then proceed.	1	1	0	The I/O operation proceeds until the word count equals zero but does not terminate. On input, the channel sets the inter-record indicator when the end of a record is encountered. On output, the channel signals the device that the last character has been transmitted then sets the inter-record indicator after the device provides an End-of-Record response. The channel does not disconnect (except for magnetic tape).
IOSP Input/Output until signal then proceed.	1	1	1	When the word count equals zero, the program should either reload the interlace to continue, or terminate the operation before the next clock is received; otherwise a rate error will occur.

$$rIwk = I1w\ Iwk\ T8 + \ldots$$

When the last character of the last word has been precessed into the Character Register, Wf is reset.

$$rWf = \overline{W7}\ \overline{W8}\ W4\ (T6 + T5) + \ldots$$

Because the Halt Interlock, W0, and Interlace Active, Iw, have been reset, a Time Share Request, Trqw, cannot be made.

$$Trqw = \overline{Wf}\ W0\ \overline{Wh}\ Iw\ \overline{Iwf}$$

Any further clocking, Ecw, of the buffer generates a Halt Interlock Signal condition.

$$sW6 = \overline{W5}\ Ecw\ T8\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}}$$

$$sW5 = \overline{W5}\ W6\ \overline{Ecw}\ T0 + \ldots$$

$$rW6 = W5\ T0 + \ldots$$

Halt Interlock Signal (decoded by the peripheral device)

$$= W5\ \overline{W6}\ \overline{W0}$$

If the Halt Signal, Whs, is received the Halt Detector Wh, is set and a disconnect occurs.

$$sWh = W9\ \overline{Iwh}\ T8\ Whs + \ldots$$

$$Wc = Wh\ \overline{Wf}\ (T3 - T0) + \ldots$$

$$rW9 = Wc$$

$$rW10 = Wc$$

etc.

The Signal Complete flip-flop, Wsc, is set.

$$sWsc = Wh\ \overline{Wf}\ T8 + \ldots$$

If the End-of-Record Interrupt Enable, Iwj, has been previously armed, an I2w interrupt occurs and Iwj is reset.

$$I2w = Wsc\ Iwj\ Iwg + \ldots$$

$$rIwj = I2w\ Iwj\ T8 + \ldots$$

The Extend Operations flip-flop, Iwg, and the Signal Complete flip-flop, Wsc are then reset.

$$rIwg = Wsc\ T8\ \overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}\ Iwg + \ldots$$

$$rWsc = Wsc\ \overline{Iwg}\ T8$$

3. 140 IOSD - Iwg $\overline{Iwh}$ Iwi

3. 141 Output

3. 142 Write C words. When C equals zero and when the last character has been transmitted, the channel disconnects the device and becomes inactive. If an End-of-Record signal is received before the count reaches zero, the channel disconnects immediately.

NOTE

> The IOSD is designed for use on devices which are normally operated on the basis of the word count only. Typewriters and paper tape devices are of this type, as are the printer and card punch when the user does not wish to stay connected until the operation is complete.

3. 143 The interlace is counted by the Interlace Count Trigger, Iwa.

$$Iwa = Rwx\ \ Tsm$$

Zero Word Count, Iwf, occurs and the Interlace Active flip-flop, Iw, is reset.

$$Iwf = Wc0\ Wc1\ \ldots\ Wc13\ Wc14\ \overline{Ew}$$

$$rIw = Iwf\ T8 + \ldots$$

The Halt Interlock, W0, is reset.

$$rW0 = W9\ Iw\ (\overline{Iwg} + \overline{Iwh} + \overline{Iwi})\,(\overline{T7 - T0}) + \ldots$$

If the End-of-Transmission Interrupt Enable, Iwk, has been previously armed, an I1w interrupt occurs and Iwk is reset.

$$I1w = Iwg\ \overline{Iw}\ Iwk\ Iwk + \ldots$$

$$rIwk = I1w\ Iwk\ T8 + \ldots$$

When the last character of the last word has been processed into the Character Register, Wf is reset.

$$rWf = \overline{W7}\ \overline{W8}\ W4\ (T6 + T5) + \ldots$$

Because the Halt Interlock, W0, has been reset, a Time Share Request, Trqw, cannot be made.

$$Trqw = \overline{Wf}\ W0\ \overline{Wh}\ Iw\ \overline{Iwf}$$

Any further clocking, Ecw, of the buffer generates a Halt Interlock Signal condition.

$$sW6 = \overline{W5}\ Ecw\ T8\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}}$$

$$sW5 = \overline{W5}\ W6\ \overline{Ecw}\ T0 + \ldots$$

$$rW6 = W5\ T0 + \ldots$$

Halt Interlock Signal

$$= W5\ \overline{W6}\ \overline{W0}$$

For devices other than magnetic tape, the Halt Detector, Wh, sets upon reaching zero Word Count, Iwf, and after the last character has been clocked from the buffer.

$$sWh = W9\ \overline{W11}\ \overline{W0}\ W5\ \overline{W6}\ (\overline{Iwh}\ Iwi + \ldots)\,T8 + \ldots$$

The Halt Detector, Wh, also sets upon the occurrence of a Halt Signal, Whs, from the magnetic tape unit.

$$sWh = W9\ \overline{Iwh}\ Whs\ T8 + \ldots$$

The setting of the Halt Detector, Wh, initiates a buffer disconnect sequence.

$$Wc = Wh\ \overline{Wf}\ (T3 - T0) + \ldots$$

$$rW9 = Wc$$

$$rW10 = Wc$$

etc.

The Signal Complete flip-flop, Wsc, is set.

$$sWsc = Wh\ \overline{Wf}\ T8$$

If the End-of-Record Interrupt Enable, Iwj, has been previously armed, an I2w interrupt occurs and Iwj is reset.

$$I2w = Wsc\ Iwj\ Iwg + \ldots$$

$$rIwj = I2w\ Iwj\ T8 + \ldots$$

The Extend Operations flip-flop, Iwg, and the Signal Complete flip-flop, Wsc, are then reset.

$$rIwg = Wsc\ T8\ \overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}\ Iwg + \ldots$$

$$rWsc = Wsc\ \overline{Iwg}\ T8$$

3. 144 IORP - Iwg Iwh $\overline{Iwi}$

3. 145 Output

3. 146 Write C words. When the channel interlace counts C down to zero, the interlace notifies the channel buffer that it has received the last word that is to be

output; when the buffer outputs this last word, it sends a signal to the connected peripheral device indicating that the device has the last word. When the peripheral device receives, outputs and checks the validity of this last word, it sends an End-of-Record response to the channel buffer. When received by the buffer, the End-of-Record signal generates an End-of-Record interrupt (if armed) and sets the Inter-Record indicator; the channel does not disconnect.

3.147 When the peripheral device is magnetic tape, the tape continues to move after it signals End-of-Record. As in reading tape, the signal causes the Tape Gap signal to come high. If the program executes a new write tape or erase tape EOM during the inter-gap time (approximately one millisecond), the tape remains in motion and proceeds to write or erase a new record. If the program executes no such EOM before the Tape Gap signal drops, the channel disconnects and tape comes to a stop. No interrupt occurs at this time. This is the only condition which causes a channel to disconnect automatically for an IORP.

3.148 To proceed after the End-of-Record occurs, the program first executes a Buffer Control mode EOM to re-initialize the Channel Unit Address Register and then reloads the interlace portion of the channel (the program can alert the Interlace via the Buffer Control EOM). Otherwise, the channel immediately terminates any attempt to use its interlace portion, since the channel is still active and in the End-of-Record condition. When the program continues from an Inter-Record condition, the program should use an extended mode terminal function.

NOTE

> A program should not use IORP with devices that do not generate End-of-Record responses upon output termination; such devices are paper tape and typewriter. These devices do terminate output but give the program no indication when they receive the last characters. The IORP should also not be used with the printer and card punch since these devices expect the channel to disconnect after they send EOR.

3.149 After the last word is accessed from memory, the Interlace is counted and zero word count is established. The Interlace is counted by the Interlace Count Trigger, Iwa.

$$Iwa = Rwx\ Tsm$$

Zero Word Count, Iwf, occurs and the Interlace Active flip-flop, Iw, is reset.

$$Iwf = Wc0\ Wc1 \ldots Wc13\ Wc14\ \overline{Ew}$$

$$rIw = Iwf\ T8 + \ldots$$

The Halt Interlock, W0, is reset.

$$rW0 = W9\ Iwf\ (\overline{Iwg} + \overline{Iwh} + \overline{Iwi})\ \overline{(T7 - T0)} + \ldots$$

If the End-of-Transmission Interrupt Enable, Iwk, has been previously armed, an I1w interrupt occurs and Iwk is reset.

$$I1w = Iwg\ \overline{Iw}\ Iwf\ Iwk + \ldots$$

$$rIwk = I1w\ Iwk\ T8 + \ldots$$

When the last character of the last word has been precessed into the Character Register, Wf is reset.

$$rWf = \overline{W7}\ \overline{W8}\ W4\ (T6 + T5) + \ldots$$

Because the Halt Interlock, W0, and Interlace Active, Iw, have been reset, a Time Share Request, Trqw, cannot be made.

$$Trqw = \overline{Wf}\ W0\ \overline{Wh}\ Iw\ \overline{Iwf}$$

Any further clocking, Ecw, of the buffer generates a Halt Interlock Signal condition.

$$sW6 = \overline{W5}\ Ecw\ T8\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}}$$

$$sW5 = \overline{W5}\ W6\ \overline{Ecw}\ T0 + \ldots$$

$$rW6 = W5\ T0 + \ldots$$

Halt Interlock Signal

$$= W5\ \overline{W6}\ \overline{W0}$$

3.150 For non-magnetic tape devices, the buffer awaits the receipt of a Halt Signal, Whs, from the device. The End-of-Record Detector, Wg, is set.

$$sWg = Whs\ \overline{(T7 - T0)}\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}} + \ldots$$

The Signal Complete Detector, Wsc, sets and if the End-of-Record Interrupt Enable, Iwj, has been previously armed, an I2w interrupt is generated and Iwj is reset.

$$sWsc = Wg\ Iwg\ Iwh\ T8\ (Iwf + \ldots) + \ldots$$

$$I2w = Wsc\ Iwj\ Iwg + \ldots$$

$$rIwj = I2w\ Iwj\ T8 + \ldots$$

The device does not disconnect because Wh is not permitted to set.

3.151 For magnetic tape, the buffer awaits the receipt of a gap signal, Mtgw. The End-of-Record Detector, Wg, is set.

$$sWg = Mtgw\ T0\ Iwg\ W11\ (\overline{W0}\ W5\ \overline{W6}\ W9 + \ldots) + \ldots$$

The Signal Complete Detector, Wsc, sets and if the End-of-Record Interrupt Enable, Iwj, has been previously armed, an I2w interrupt is generated and Iwj is reset.

$$sWsc = Wg\ Iwg\ Iwh\ T8\ (Iwf + \ldots) + \ldots$$

$$I2w = Wsc\ Iwj\ Iwg$$

$$rIwj = I2w\ Iwj\ T8 + \ldots$$

The magnetic tape system can continue if the interrupt sub-routine executes an EOM to the tape within approximately one millisecond from the occurrence of the interrupt. If no EOM is executed, the tape generates a Halt Signal, Whs, and the Halt Detector, Wh, sets. The magnetic tape is disconnected and the buffer is cleared.

$$sWh = Whs\ W11\ T8 + \ldots$$

$$Wc = Wh\ \overline{Wf}\ (T3 - T0) + \ldots$$

$$rW9 = Wc$$

$$rW10 = Wc$$

etc.

$$rIwg = Wsc\ T8\ \overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}\ Iwg + \ldots$$

$$rWsc = Wsc\ T8\ \overline{Iwg}$$

$$rWh = Wh\ \overline{Wf}\ T8 + \ldots$$

3.152 IOSP - Iwg Iwh Iwi

3.153 <u>Output</u>

3.154 Write C words. When the channel counts C down to zero, the channel generates a Count Equals Zero interrupt (if armed); the channel does not terminate output. The program should reload the interlace portion of the channel to continue writing in the same record. Failure to reload the Interlace before the buffer transmits all of the characters in its registers and before the peripheral device requests the next character from the buffer results in a rate error; this sets the Channel Error Indicator.

3.155 If the program executes a TERMINATE OUTPUT (TOP) instruction after the channel has counted C down to zero, the channel terminates the output and operates identically like the IORP from this point on.

3.156 After the last word is accessed from memory, the interlace is counted and zero word count is established.

The Interlace is counted by the Interlace Count Trigger, Iwa.

$$Iwa = Rwx\ Tsm$$

Zero Word Count, Iwf, occurs and the Interlace Active flip-flop, Iw, is reset.

$$Iwf = Wc0\ Wc1 \ldots Wc13\ Wc14\ \overline{Ew}$$

$$rIw = Iwf\ T8 + \ldots$$

If the End-of-Transmission Interrupt Enable, Iwk, has been previously armed, an I1w interrupt occurs and Iwk is reset.

$$I1w = Iwg\ \overline{Iw}\ Iwf\ Iwk + \ldots$$

$$rIwk = I1w\ Iwk\ T8 + \ldots$$

The program, upon receipt of an I1w interrupt, should reload the Interlace to permit the transmission to continue with a new set of parameters (i.e., word count, address, terminal functions, etc.). The loading of the Interlace with a zero word count could permit conversion of the current IOSP to some other terminal function, for example to an IORD, thereby effecting a disconnect.

3.157 Execution of a TERMINATE OUTPUT (TOP) instruction, e.g., EOM14000, would convert the IOSP to an IORP. The TOP instruction resets the Halt Interlock flip-flop, W0.

$$rW0 = Ioc\ C12\ \overline{C17}\ \overline{C19}\ \overline{C20}\ \overline{C21}\ \overline{C22}\ \overline{C23}\ W9\ T0 + \ldots$$

Any further clocking of the channel by Ecw generates a Halt Interlock Signal condition when the last character has been clocked from the buffer.

$$sW6 = \overline{W5}\ Ecw\ T8\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}}$$

$$sW5 = \overline{W5}\ W6\ \overline{Ecw}\ T0 + \ldots$$

$$rW6 = W5\ T0 + \ldots$$

$$rW5 = W4\ T0 + \ldots$$

Halt Interlock Signal

$$= W5\ \overline{W6}\ \overline{W0}$$

The Halt Interlock Signal is representative of the buffer status had the IOSP been an IORP.

3.158 IORD - Iwg $\overline{Iwh}$ $\overline{Iwi}$

3.159 Input

3.160 Read C words. If C equals zero before the End-of-Record is detected, the rest of the record is ignored. At the End-of-Record, the peripheral device is disconnected and the channel becomes inactive.

3.161 When the W-Register acquires the specified number of characters, a Time Share Request, Trqw, is generated.

$$Trqw = \overline{Wf}\ W0\ \overline{Wh}\ Iw\ \overline{Iwf}$$

When memory is accessed, the interlace registers are counted by the Interlace Count Trigger, Iwa.

$$Iwa = Rwx\ Tsm$$

Zero Word Count, Iwf, may occur and the Interlace Active flip-flop, Iw, is reset.

$$Iwf = Wc0\ Wc1\ \ldots\ Wc13\ Wc14\ \overline{Ew}$$

$$rIw = Iwf\ T8 + \ldots$$

If the Zero Word Count Interrupt Enable, Iwk, has been previously armed, then an I1w interrupt occurs.

$$I1w = Iwg\ \overline{Iw}\ Iwf\ Iwk + \ldots$$

$$rIwk = I1w\ Iwk\ T8 + \ldots$$

Additional characters entering the channel after Zero Word Count has been reached are precessed into the W-Register.

$$sW6 = \overline{W5}\ Ecw\ T8\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}}$$

$$rW6 = W5\ T0 + \ldots$$

$$sW5 = \overline{W5}\ W6\ \overline{Ecw}\ T0 + \ldots$$

$$rW5 = W4\ T0 + \ldots$$

$$sW4 = W5\ Wf\ T8\ \overline{Wg} + $$
$$+ Iwg\ \overline{W9}\ \overline{Iwi}\ W5\ Iwf\ T8 + \ldots$$

$$sW4 = Wr\ T0 + \ldots$$

$$Ww1 = W4\ Wb1\ (T7 - T0) + \ldots$$

$$Ww2 = W4\ Wb2\ (T7 - T0) + \ldots$$

$$Ww3 = W4\ Wb3 + \ldots$$

However, Time Share Request, Trqw, is inhibited.

$$Trqw = \overline{Wf}\ W0\ \overline{Wh}\ Iw\ \overline{Iwf}$$

Parity errors cannot occur after Zero Word Count.

$$sWe = \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}\ Rwp\ \overline{Wg}\ Npw$$
$$(\overline{Iwg} + Iwi + \overline{Iwf}) + \ldots$$

Rate errors cannot set We while W4 is enabled by Iwg W9 Iwi Iw.

$$sWe = W0\ \overline{W6}\ W5\ Ecw\ T8 + \ldots$$

After Zero Word Count is established, detection of a Halt Signal or Photoreader Gap sets the End-of-Record Detector, Wg.

$$sWg = Whs\ \overline{(T7 - T0)}\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}}$$
$$+ \overline{W9}\ \overline{W10}\ \overline{W11}\ W12\ \overline{W13}$$
$$(\overline{Rw1}\ \overline{Rw2}\ \overline{Rw3}\ \overline{Rw4}\ \overline{Rw5}\ \overline{Rw6}\ \overline{Rwp})$$
$$W5\ \overline{(T7 - T0)}\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}} + \ldots$$

The Halt Detector, Wh, sets.

$$sWh = Whs\ W11\ T8 + Wg\ \overline{W9}\ \overline{W11}\ \overline{Iwh}\ Iwg\ T8$$
$$(Iwf + \ldots) + \ldots$$

The buffer is flushed (i.e., allowed to precess without receiving input clocks until the Character Count equals zero) until it is assured that Wf is reset.

$$sW4 = Wh\ Wf\ T8 + \ldots$$

$$rWf = \overline{W7}\ \overline{W8}\ W4\ (T6 + T5) + \ldots$$

The buffer is cleared and the peripheral device disconnected.

$$Wc = Wh\ Wf\ (T3 - T0) + \ldots$$

If the End-of-Record Interrupt Enable, Iwj, has been previously armed, and End-of-Record Interrupt, Iw2, occurs.

$$sWsc = Wh\ \overline{Wf}\ T8 + \ldots$$

$$rWsc = Wsc\ T8\ \overline{Iwg}$$

$$I2w = Wsc\ Iwj\ Iwg + \ldots$$

$$rIwj = I2w\ Iwj\ T0 + \ldots$$

$$rIwg = Wsc\ Iwg\ \overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}\ T8 + \ldots$$

Should an End-of-Record occur before Zero Word Count is established, the End-of-Record Detector is set.

$$\begin{aligned} sWg = {} & Mtgw\ T0\ Iwg\ W11\ (W0\ \overline{W9} + \ldots) \\ & + Whs\ \overline{(T7 - T0)}\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}} \\ & + \overline{W9}\ \overline{W10}\ \overline{W11}\ W12\ \overline{W13} \\ & (\overline{Rw1}\ \overline{Rw2}\ \overline{Rw3}\ \overline{Rw4}\ \overline{Rw5}\ \overline{Rw6}\ \overline{Rwp})\ W5 \\ & \overline{(T7 - T0)}\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}} \end{aligned}$$

Any character remaining in the W-Register are flushed by W4 and a Time Share Request, Trqw, is generated.

$$sW4 = Iwg\ Wg\ Wf\ W0\ \overline{Wev}\ Iw\ T8\ \overline{\overline{W7}\ \overline{W9}\ W10\ W11\ \overline{Wh}} + \ldots$$

where:

$$\begin{aligned} Wev = {} & W8\ Wn2\ W7\ Wn1 + \overline{W8}\ \overline{Wn2}\ W7\ Wn1 \\ & + \overline{W8}\ \overline{Wn2}\ \overline{W7}\ \overline{Wn1} + W8\ Wn2\ \overline{W7}\ \overline{Wn1} \end{aligned}$$

$$rWf = \overline{W7}\ \overline{W8}\ W4\ (T6 + T5) + \ldots$$

$$Trqw = \overline{Wf}\ W0\ \overline{Wh}\ Iw\ \overline{Iwf}$$

and $\overline{\overline{W7}\ \overline{W9}\ W10\ W11\ \overline{Wh}}$ indicates that a scan operation is not taking place.

3.162 As a result of one Time Share operation, Wf is set.

$$sWf = Iwa\ \overline{Mit}\ T0 + \ldots$$

The Character Counter is reloaded with its original count, making Wev true and the flush operation ceases.

3.163 The Halt Detector, Wh, is now permitted to set. For Magnetic Tape operation this occurs upon receipt of a Halt Signal, Whs.

$$\begin{aligned} sWh = {} & Whs\ W11\ T8 + Wg\ \overline{W9}\ \overline{W11}\ \overline{Iwh} \\ & (Iwf + Wev\ Wf)\ T8\ Iwg + \ldots \end{aligned}$$

Before the buffer is cleared, the buffer is again flushed but a Time Share Request, Trqw, is inhibited.

$$sW4 = Wh\ Wf\ T8 + \ldots$$

$$rWf = \overline{W7}\ \overline{W8}\ W4\ (T6 + T5) + \ldots$$

$$Trqw = \overline{Wf}\ W0\ \overline{Wh}\ Iw\ \overline{Iwf}$$

The buffer is then cleared.

$$Wc = Wh\ \overline{Wf}\ (T3 - T0) + \ldots$$

If the End-of-Record Interrupt Enable, Iw_j, has been previously armed, an End-of-Record Interrupt, I2w, occurs.

$$sWsc = Wh\ \overline{Wf}\ T8 + \ldots$$

$$rWsc = Wsc\ T8\ \overline{Iwg}$$

$$I2w = Wsc\ Iw_j\ Iwg$$

$$rIw_j = I2w\ \ Iw_j\ T8 + \ldots$$

$$rIwg = Wsc\ Iwg\ \overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}\ T8 + \ldots$$

3.164 IOSD - Iwg $\overline{Iwh}$ Iwi

3.165 Input

3.166 Read C words. When C equals zero or when the End-of-Record is encountered, the device is disconnected and the channel becomes inactive. If the channel disconnects because of a zero count, an EOR interrupt (if armed) is generated in addition to the count-equal-zero interrupt. If both are armed, the count-equal-zero interrupt occurs first.

When the W-Register acquires the specified number of characters, a Time Share Request, Trqw, is generated.

$$Trqw = \overline{Wf}\ W0\ \overline{Wh}\ Iw\ \overline{Iwf}$$

When memory is accessed, the interlace registers are counted by the Interlace Count Trigger, Iwa.

$$Iwa = Rwx\ \ Tsm$$

Zero Word Count, Iwf, may occur and the Interlace Active flip-flop, Iw, is reset.

$$Iwf = Wc0\ Wc1\ \ldots Wc13\ Wc14\ \overline{Ew}$$

$$rIw = Iwf\ T8 + \ldots$$

If the zero Word Count Interrupt Enable, Iwk, has been previously armed, then an I1w interrupt occurs.

$$I1w = Iwg\ \overline{Iw}\ Iwf\ Iwk + \ldots$$

$$rIwk = I1w\ Iwk\ T0 + \ldots$$

The Halt Detector is set.

$$sWh = \overline{W9}\ \overline{W11}\ Iwg\ \overline{Iwh}\ Iwi\ Iwf\ T8\ W0 + \ldots$$

The buffer is flushed, but no Time Share Request, Trqw, may be initiated.

$$sW4 = Wh\ Wf\ T8 + \ldots$$

$$rW4 = W4\ T0 + \ldots$$

$$rWf = \overline{W7}\,\overline{W8}\,T8 + \ldots$$
$$Trqw = \overline{Wf}\,W0\,\overline{Wh}\,Iw\,\overline{Iwf}$$

The channel is cleared and the peripheral device disconnected.

$$Wc = Wh\,\overline{Wf}\,(T3 - T0) + \ldots$$

If the End-of-Record Interrupt Enable, Iwj, has been previously armed, and End-of-Record Interrupt, I2w, occurs.

$$sWsc = Wh\,\overline{Wf}\,T8 + \ldots$$
$$rWsc = Wsc\,\overline{Iwg}\,T8$$
$$I2w = Wsc\,Iwj\,Iwg + \ldots$$
$$rIwj = I2w\,Iwj\,T8 = \ldots$$
$$rIwg = Wsc\,Iwg\,\overline{W10}\,\overline{W11}\,\overline{W12}\,\overline{W13}\,\overline{W14}\,T8 + \ldots$$

Should an End-of-Record occur before Zero Word Count is established, the End-of-Record Detector is set.

$$\begin{aligned} sWg = {} & Mtgw\,T0\,Iwg\,W11\,(W0\,\overline{W9} + \ldots) \\ & + Whs\,\overline{(T7 - T0)}\,\overline{\overline{W10}\,\overline{W11}\,\overline{W12}\,\overline{W13}\,\overline{W14}} \\ & + \overline{W9}\,\overline{W10}\,\overline{W11}\,W12\,\overline{W13} \\ & \quad (\overline{Rw1}\,\overline{Rw2}\,\overline{Rw3}\,\overline{Rw4}\,\overline{Rw5}\,\overline{Rw6}\,Rwp) \\ & \quad W5\,\overline{(T7 - T0)}\,\overline{\overline{W10}\,\overline{W11}\,\overline{W12}\,\overline{W13}\,\overline{W14}} \end{aligned}$$

Any characters remaining in the W-Register are flushed and a Time Share Request, Trqw, is generated.

$$sW4 = Iwg\,Wg\,Wf\,W0\,\overline{Wev}\,Iw\,\overline{\overline{W7}\,\overline{W9}\,W10\,W11}\,\overline{\overline{Wh}}\,T8 + \ldots$$

where:

$$\begin{aligned} Wev = {} & W8\,Wn2\,W7\,Wn1 + \overline{W8}\,\overline{Wn2}\,W7\,Wn1 \\ & + \overline{W8}\,\overline{Wn2}\,\overline{W7}\,\overline{Wn1} + W8\,Wn2\,\overline{W7}\,\overline{Wn1} \end{aligned}$$

$$rWf = \overline{W7}\,\overline{W8}\,W4\,(T6 + T5) + \ldots$$
$$Trqw = \overline{Wf}\,W0\,\overline{Wh}\,Iw\,\overline{Iwf}$$

As a result of the Time Share operation, Wf, is set.

$$sWf = Iwa\,\overline{Mit}\,T0$$

When the term Wev is true the flush and store operation ceases. The Halt Detector, Wh, is permitted to set

$$sWh = Whs\,W11\,T8 + Wg\,\overline{W9}\,\overline{W11}\,\overline{Iwh}\,(Iwf + Wev\,Wf)\,T8\,Iwg + \ldots$$

Before the buffer is cleared, the buffer is again flushed but a Time Share Request, Trqw, is inhibited.

$$sW4 = Wh\,Wf\,T8 + \ldots$$
$$rWf = \overline{W7}\,\overline{W8}\,W4\,(T6 + T5) + \ldots$$
$$Trqw = \overline{Wf}\,W0\,\overline{Wh}\,Iw\,\overline{Iwf}$$

The buffer is then cleared.

$$Wc = Wh\,\overline{Wf}\,(T3 - T0) + \ldots$$

If the End-of-Record Interrupt Enable, Iwj, has been previously armed, an End-of-Record Interrupt, I2w, occurs.

$$sWsc = Wh\,\overline{Wf}\,T8 + \ldots$$
$$rWsc = Wsc\,\overline{Iwg}\,T8$$
$$I2w = Wsc\,Iwj\,Iwg + \ldots$$
$$rIwk = I2w\,Iwk\,T8 + \ldots$$
$$rIwg = Wsc\,Iwg\,\overline{W10}\,\overline{W11}\,\overline{W12}\,\overline{W13}\,\overline{W14}\,T8 + \ldots$$

3.167 Should an IOSD mode be used on input with magnetic tape devices, no disconnect will occur at Iwf. Should additional characters enter the buffer after Iwf, a rate error may occur.

$$sWe = W0\,\overline{W6}\,W5\,Ecw\,T8 + \ldots$$

Disconnect occurs upon receipt of a Halt Signal, Whs, from the magnetic tape system.

$$sWh = Whs\,W11\,T8 + \ldots$$
$$sW4 = Wh\,Wf\,T8 + \ldots$$
$$rW4 = W4\,T0 + \ldots$$
$$rWf = \overline{W7}\,\overline{W8}\,W4\,(T6 + T5) + \ldots$$
$$Wc = Wh\,\overline{Wf}\,(T3 - T0) + \ldots$$

3.168 IORP - Iwg Iwh $\overline{Iwi}$

3.169 Input

3.170 Read C words. If the channel counts C down to zero before the peripheral device encounters the End-of-Record (EOR), the channel ignores the rest of the record (to the End-of-Record). When the peripheral device sends the End-of-Record signal to the channel, the channel sets its End-of-Record Indicator; this signal sets the End-of-Record interrupt (if armed). The channel does not disconnect. The channel is now in an "Inter-Record" condition.

3.171 When the peripheral device is magnetic tape, the tape continues to move when the tape handler encounters the End-of-Record. The End-of-Record occurs when the tape read-heads encounter tape gap; this also causes a Tape Gap signal to come high. If the program executes a new read tape or scan tape EOM during the inter-gap time (approximately one millisecond while the Tape Gap signal is high), the tape remains in motion and proceeds to read or scan the next record. If the program executes no such EOM before the Tape Gap signal drops, the channel disconnects and the tape comes to a stop. No additional interrupt occurs. This is the only condition that causes a channel to disconnect automatically in an IORP.

3.172 All other input devices remain connected until the program takes further action. The paper tape reader remains in motion; the program should issue a "disconnect channel" instruction if the program is not reading any more tape. To proceed after the End-of-Record occurs, the program first executes a Buffer Control mode EOM to re-initialize the Channel Unit Address Register and then reloads the interlace portion of the channel (the program can alert the Interlace via the Buffer Control EOM). Otherwise, the channel immediately terminates any attempt to use its interlace portion since the channel is aware that it is still active and in the End-of-Record condition. When the program continues from an Inter-Record condition, the program should use an extended mode terminal function. An IORP should not be used to read with devices that do not have EOR signals (e.g., the typewriter).

3.173 When the W-Register acquires the specified number of characters, a Time-Share Request, TRQW, is generated.

$$Trqw = \overline{Wf}\ W0\ \overline{Wh}\ Iw\ \overline{Iwf}$$

When memory is accessed, the interlace registers are counted by Interlace Count Trigger, Iwa.

$$Iwa = Rwx\ Tsm$$

Zero Word Count, Iwf, may occur and the Interlace Active flip-flop, Iw, is reset.

$$Iwf = Wc0\ Wc1\ \ldots\ Wc13\ Wc14\ \overline{Ew}$$

$$rIw = Iwf\ T8 + \ldots$$

If the Zero Word Count Interrupt Enable, Iwk, has been previously armed, then an I1w interrupt occurs.

$$I1w = Iwg\ \overline{Iw}\ Iwf\ Iwk + \ldots$$

$$rIwk = I1w\ Iwk\ T8 + \ldots$$

3.174 Additional characters entering the channel after Zero Word Count has been reached are precessed into the W-Register.

$$sW6 = \overline{W5}\ Ecw\ T8\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}}$$

$$rW6 = W5\ T0 + \ldots$$

$$sW5 = \overline{W5}\ W6\ \overline{Ecw}\ T0 + \ldots$$

$$rW5 = W4\ T0 + \ldots$$

$$sW4 = W5\ Wf\ T8\ \overline{Wg} + Iwg\ \overline{W9}\ \overline{Iwi}\ W5\ Iwf\ T8 + \ldots$$

$$rW4 = W4\ T0 + \ldots$$

$$Ww1 = W4\ Wb1\ (T7 - T0) + \ldots$$

$$Ww2 = W4\ Wb2\ (T7 - T0) + \ldots$$

$$Ww3 = W4\ Wb3 + \ldots$$

However, Time Share Requests, Trqw, are inhibited.

$$Trqw = \overline{Wf}\ W0\ \overline{Wh}\ Iw\ \overline{Iwf}$$

Parity and rate errors cannot occur after Zero Word Count.

$$sWe = \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}\ Rwp\ \overline{Wg}\ Npw\ (\overline{Iwg} + Iwi + \overline{Iwf}) + W0\ W5\ \overline{W6}\ Ecw\ T8 + \ldots$$

Detection of magnetic tape gap, photoreader gap or a halt signal sets the End-of-Record Detector.

$$sWg = Mtgw\ T0\ Iwg\ W11\ (W0\ \overline{W9} + \ldots) + Whs\ \overline{(T7 - T0)}\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}} + \overline{W9}\,\overline{W10}\,\overline{W11}\,W12\,\overline{W13}\,(\overline{Rw1}\ \overline{Rw2}\ \overline{Rw3}\ \overline{Rw4}\ \overline{Rw5}\ \overline{Rw6}\ \overline{Rwp})\ W5\ \overline{(T7 - T0)}\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}}$$

If the End-of-Record Detector is set before Zero Word Count has occurred, then the buffer is flushed and the completed word is stored in memory.

$$sW4 = Iwg\ Wg\ Wf\ W0\ \overline{\overline{Wev}\ Iw\ \overline{W7}\ \overline{W9}\ W10\ W11\ \overline{Wh}}\ T8 + \ldots$$

$$rW4 = W4\ T0 + \ldots$$

where:

$$Wev = W8\ Wn2\ W7\ Wn1 + \overline{W8}\,\overline{Wn2}\,W7\ Wn1 + \overline{W8}\ \overline{Wn2}\ \overline{W7}\ \overline{Wn1} + W8\,Wn2\ \overline{W7}\,\overline{Wn1}$$

Wf is reset and Time Share Request is inhibited.

$$rWf = \overline{W7}\,\overline{W8}\,W4\,(T6 + T5) + \ldots$$

$$Trqw = \overline{Wf}\,W0\,\overline{Wh}\,Iw\,\overline{Iwf}$$

$$sWf = Iwa\,\overline{Mit}\,T0 + \ldots$$

If Wg is set, Wsc is set after the buffer is flushed or immediately if Zero Word Count exists.

$$sWsc = Wg\,Iwg\,Iwh\,(Wev\,Wf + Iwf)\,T8 + \ldots$$

$$rWsc = Wsc\,\overline{Iwg}\,T8$$

If the End-of-Record Interrupt Enable, Iwj, has been previously armed, an I2w interrupt occurs.

$$I2w = Wsc\,Iwj\,Iwg + \ldots$$

$$rIwj = I2w\,Iwg\,T8 + \ldots$$

3.175 In general, the buffer does not disconnect, as the Halt Detector has not been set. For magnetic tape operation, a new EOM may be given within 0.75 millisecond from the occurrence of I2w to permit the magnetic tape system to proceed to a new record. In the case of magnetic tape, failure to give an EOM results in the tape stopping and the buffer disconnecting.

$$sWh = Whs\,W11\,T8 + \ldots$$

The buffer is flushed but not stored as Trqw is inhibited.

$$sW4 = Wh\,Wf\,T8 + \ldots$$

$$rW4 = W4\,T0 + \ldots$$

$$rWf = \overline{W7}\,\overline{W8}\,W4\,(T6 + T5)$$

$$Trqw = \overline{Wf}\,W0\,\overline{Wh}\,Iw\,\overline{Iwf}$$

The buffer is cleared.

$$Wc = Wh\,\overline{Wf}\,(T3 - T0) + \ldots$$

3.176 IOSP - Iwg Iwh Iwi

3.177 Input

3.178 Read C words. If the channel counts C down to zero before the peripheral device encounters the End-of-Record, the channel generates a Count Equals Zero interrupt (if armed). The program should reload the interlace portion of the channel to continue reading the record. As far as the peripheral device knows, nothing happens at this time. Failure to reload the Interlace before the peripheral device sends enough characters to overfill the channel buffer causes a rate error; this sets the channel error indicator.

3.179 When the peripheral device encounters the End-of-Record, IOSP operates identically like the IORP command. An IOSP is identical to an IORP in operation except that when Zero Word Count occurs it is anticipated that the interlace will be reloaded. Failure to reload the interlace in time results in rate errors. Parity error detection is not inhibited after Zero Word Count.

$$sWe = \overline{W9}\,\overline{W6}\,\overline{W5}\,\overline{W4}\,Rwp\,\overline{Wg}\,Npw\,(Iwi + \ldots)$$

$$+ W0\,\overline{W6}\,W5\,Ecw\,T8 + \ldots$$

3.180 PIN ADDRESS COUNTER

3.181 The PIN Address Counter flip-flop allows a PIN instruction to interrogate the Interlace Address Counter. The flip-flop is set by an I/O Unit Control instruction EOM (Ioc) in which the address bits are "zeros" and bit 13 is a "one". Bit 17 of the instruction selects either the W or Y channel TMCC.

$$sWpa = Ioc\,\overline{C17}\,C13\,\overline{C19}\,\overline{C20}\,\overline{C21}\,\overline{C22}\,\overline{C23}\,T0$$

The Ioc signal indicates that an I/O control instruction is being processed and also distinguishes between the W - Y channels and the C - D channels.

$$Ioc = Ioc\,1\,\overline{C1}\,\overline{Er}\,Qr3$$

$\overline{C1}$ becomes C1 for TMCC-C & D

$$Ioc\,1 = Eom\,\overline{C10}\,C11$$

3.182 After Wpa is turned on, the Interlace Memory Address Counter flip-flops are gated to the CPU via the parallel input lines (Cd0) - (Cd23). For this purpose, only fifteen of the lines are required.

$$(Cd9) = (Wa0\,Wpa)\,(Ya0\,Ypa) + \ldots$$

$$\vdots \qquad \vdots$$

$$(Cd23) = (Wa14\,Wpa)\,(Ya14\,Ypa) + \ldots$$

The dotted lines indicate other parallel signals may be connected to the same lines.

3.183 When a PIN instruction is executed, Wpa is re reset and the interrogation is complete.

$$rWpa = Pin\,T0 + St$$

3.184 GLOSSARY OF LOGIC TERMS

Buc	A control signal derived from the EOM instruction used to activate the TMCC and peripheral devices.
C0 - C23	The 24 signals received from the C register in the CPU.
$\overline{C1x}$	A signal from the C1 flip-flop in the C register in the CPU. $\overline{C1x}$ is utilized to distinguish between TMCC W or Y and TMCC C or D. $\overline{C1x}$ becomes C1x for TMCC C or D.
C21r - C23r	Signals from the C register in the CPU used when serial transfers occur from the C register to the W register.
($\overline{Cd0}$) - ($\overline{Cd23}$)	Input data lines that are read by the C register in the CPU during a PIN instruction.
/$\overline{Ci0}$/ - /$\overline{Ci23}$/	The 24 signals derived from the C register in the CPU and transmitted on the interconnecting cable
Cpr	A signal from the CPU indicating the parity of C21r - C23r from the C register as information is serially transmitted to the TMCC.
Ecw	The clocking signal from external devices used in clocking of information into or out of the TMCC.
En + (En)	A signal from the CPU denoting that interrupt system is enabled.
Eom	A signal from the CPU occurring during an EOM instruction.
Er	A signal which inhibits Eom and Ioc to external devices when an Interlace Prepare flip-flop has been set.
Ew	A flip-flop which when set prepares the interlace to be loaded.
I1w	An interrupt signal indicating in the compatible mode that a WIM or MIW instruction should either empty or load the TMCC and in the extended mode indicating that the interlace word count is zero.
I2w	An interrupt signal indicating in the compatible mode that the input or output process has been terminated and the external device has been disconnected and in the extended mode indicating that an End-of-Record condition has been detected.
Ioc	An input/output control signal derived from Eom.
/$\overline{Ir0}$/ - /$\overline{Ir14}$/	Interlace address signals transmitted to the CPU.
Iw	A flip-flop which when set denotes that the interlace system is active.
Iwa	A signal which counts the interlace word and address counters when a memory access is performed.
Iwc	A signal occurring during the interlace loading sequence which clears the interlace registers.
Iwe	A signal occurring during the EOM instruction of an interlace loading sequence which sets the high order bits of the interlace counters and set several flip-flops used in the extended mode.
Iwf	A signal denoting that the Interlace Word Count Register has reached zero word count.
Iwg	A flip-flop which when set denotes extended mode operation.
Iwh, Iwi	Two flip-flops comprising the Channel Command Register used in the extended mode to control terminal functions of the TMCC.
Iwj	The Channel Command Interrupt Enable flip-flop used in the extended mode to permit selective arming of the I2w interrupt signal.
Iwk	The Channel Command Interrupt Enable flip-flop used in the extended mode to permit selective arming of the I1w interrupt signal.
Iwp	A signal occurring during the POT instruction of an interlace loading sequence which sets initial word count and memory address information into the Interlace Word and Address Counters.

/Kcc0/-/Kcc2/	Switch controlled signals from the Control Console used to select a particular TMCC or DACC for Unit Address and Error display on the Control Console.
/$\overline{\text{Kcc1x}}$/	A switch controlled signal used to distinguish between TMCC W or Y and TMCC C or D. /Kcc1/ becomes /$\overline{\text{Kcc1x}}$/ for TMCC C or D.
Kccw	A signal decoded from /Kcc0/-/Kcc2/ such that when true enables displaying the TMCC-W Unit Address and Error status.
Mit	A signal derived from memory indicating the DACC is in process of accessing the memory.
Mtgw	The magnetic tape gap signal generated by the magnetic tape system.
Npw	A signal from external devices used to inhibit parity checking by the TMCC. When Npw is low, parity checking is inhibited.
05, Pwy	A signal from the CPU Operation Code Register, of the SDS 925 and 930. "05" is always true from the 9300.
Pin	A signal from the CPU derived from a PIN instruction.
Pot	A signal from the CPU derived from a POT instruction.
Qr1-Qr4	The four flip-flops in the TMCC comprising the pulse counter.
(Qq1)	Timing signal sent to external devices which is true from T5 through T0.
(Qq2)	Timing signal sent to external devices which is true from T6 through T3.
(Qq3)	Timing signal sent to external devices which is true from T7 through T4.
Qw2	Timing signal which varies when a TMCC character length is expanded.
/$\overline{\text{R9}}$/	A signal transmitted from the TMCC to the CPU defining whether the TMCC memory access operation is a load or store.

/Ra0/-/Ra3/	Signals from the TMCC to the CPU denoting which particular TMCC's are active. These signals are displayed on the SDS 9300 Control Console and not used on the SDS 930.
/$\overline{\text{Rd9}}$/-/$\overline{\text{Rd14}}$/	Signals from the TMCC to the CPU denoting Unit Address Register contents for the particular TMCC selected for displays. These signals are displayed on the Control Console.
/$\overline{\text{Rde}}$/	A signal from the TMCC to the CPU denoting the status of the Error Detector for the particular TMCC selected for display. This signal is displayed on the Control Console.
/Re0/-/Re3/	Signals from the TMCC to the CPU denoting the Error Detector status for each particular TMCC. These signals are displayed on the SDS 9300 Control Console and not used on the SDS 930.
/$\overline{\text{Rr1}}$/-/$\overline{\text{Rr3}}$/	Serial data signals transmitted from the TMCC to the CPU during time share operations.
($\overline{\text{Rt}}$)	A ready signal from the TMCC on external devices used to release PIN or POT instructions from Ø2.
Rti	A signal from the CPU to external devices indicating that a PIN instruction has terminated.
Rw1-Rw24	Twenty four flip-flops comprising the character buffer. Rw1 through Rw6 are basic. Rw7 through Rw12 are optionally added to expand the character buffer to 12 bits. Rw7 through Rw24 are optionally added to expand the character buffer to 24 bits. TMCC Y, C, D are the only buffers which may be expanded.
Rwp	The parity flip-flop in the TMCC. An "odd" parity system is used.
Rwx	A flip-flop in each TMCC which is set if a Time Share Request for the particular TMCC can occur.
/$\overline{\text{Rwy1}}$/-/$\overline{\text{Rwy3}}$/	Serial data signals transmitted from the TMCC to the CPU during WIM instructions.

Rx	A signal from the CPU denoting that a WIM or MIW instruction is occurring.
Sio	A response signal from peripheral devices interrogated by an SKS instructions.
Skss	A signal generated in the CPU during SKS instructions and sent to external equipment to be used as a strobe.
$/\overline{Skz}/$	A signal generated by TMCC's or DACC's which is sent to the CPU for interrogation during SKS instructions.
Ssc	A response signal from external systems equipment interrogated by SKS instructions.
St	A signal from the CPU derived from the manual start button.
Sys	A control signal for systems communication derived from EOM.
T8, T7-T0, T6 + T5, T6-T0, T4-T0, T3-T0, T0	Timing pulses used in the TMCC decoded from the Pulse Counter, Qr1 through Qr4.
Tpc	A timing pulse from the CPU used to synchronize the Pulse Counter, Qr1 through Qr4 in the TMCC with the Pulse Counter, Q1 through Q6, in the CPU.
Trq	A signal transmitted from the TMCC to the CPU indicating that a TMCC requests a Time Share operation.
Trqx	A signal transmitted from TMCC C and D indicating to TMCC W and Y that TMCC C and D are requesting a Time Share operation.
Trqw	A signal generated by TMCC-W indicating that TMCC-W is requesting a Time Share operation.
Tsm	A signal from the CPU indicating that the interlace address counter information has been received by the CPU.
Tsr	A signal from the CPU indicating that a Time Share operation is in process.
W4	A flip-flop in the TMCC which controls the precessing of data between the Character Buffer and the W register.
W5	A flip-flop which detects that a precess should occur.
W6	A flip-flop which detects that an external clock is present.
W7, W8	Two flip-flops comprising the Character Counter.
W9	A flip-flop which is part of the Unit Address Register defining whether a process is input or output.
W10-W14	The Unit Address Register which designates to the TMCC and peripheral devices which device is activated.
Wa0-Wa14	Fifteen flip-flops comprising the Interlace Address Register.
Wb1-Wb3	Inputs to the W register from the Character Register which will vary depending on whether the TMCC is expanded.
Wc	The signal which resets the TMCC and prepares it for a new operation.
Wc0-Wc14	Fifteen flip-flops comprising the Interlace Word Counter.
We	The Error Detector flip-flop.
Wes	An error signal from peripheral devices.
Wev	A signal which when true indicates that the Character Counter is set to the same character count as it was when initially set up by the EOM.
Wf	A flip-flop which when reset denotes on input that the W register is full and on output that the W register is empty.
Wg	A flip-flop used to detect End-of-Record conditions.
Wh	The Halt Detector flip-flop.

Whs	A halt signal from peripheral devices.
Wn1-Wn3	The "now" flip-flops of the W register.
W0	The Halt Interlock flip-flop used on output to enable the Halt Detector after output has been terminated and used on input to denote that the input process has proceeded to process characters.
Wpa	The PIN Address Counter flip-flop which when set allows a PIN instruction to interrogate the Interlace Address Counter.
Wr1-Wr3	The "read" flip-flops of the W register.
Ws	The signal derived from an EOM instruction which initially sets up the TMCC.
Wsc	The Signal Complete flip-flop.
Ww1-Ww3	The signals which permit "writing" into the W register.
Wxx	A signal which denotes that an MIW, WIM or Time Share operation is occurring.
Zw1-Zw24	The twenty four inputs to the Character Register from peripheral devices.
Zwp	The input to the Parity flip-flop from peripheral devices.

3.185 LOGIC EQUATIONS

3.186 Pulse Counter

$sQr1 = Tpc + \overline{Qr2}\ Qr3\ \overline{Qr4}$

$rQr1 = Qr2$

$sQr2 = Qr1\ \overline{Qr2}\ Qr4\ (Qr4 + T0) + Qr1\ Qr3$

$rQr2 = \overline{Qr1}$

$sQr3 = Qr1\ Qr4$

$rQr3 = Qr3\ \overline{Qr4}\ (Qr4 + T0)$

$sQr4 = Qr1\ \overline{Qr3}$

$rQr4 = \overline{Qr1}\ \overline{Qr2}$

	Qr1	Qr2	Qr3	Qr4
Tp	0	0	0	0
T8	1	0	0	0
T7	1	0	0	1
T6	1	1	1	1
T5	0	1	1	1
T4	0	0	1	1
T3	0	0	1	0
T2	1	0	1	0
T1	1	1	1	0
T0	0	1	1	0
Tr	0	0	0	0
Tp	0	0	0	0

$T8 = Qr1\ \overline{Qr3}\ \overline{Qr4}$

$T6 + T5 = Qr2\ Qr4$

$T7 - T4 = Qr4$

$T7 - T0 = Qr3 + Qr4$

$T6 - T0 = Qr3$

$T6 - T3 = (Qr4 + \overline{Qr1}\ \overline{Qr2})\ Qr3$

$T3 - T0 = Qr3\ \overline{Qr4}$

$T0 = \overline{Qr1}\ Qr2\ \overline{Qr4}$

$T5 - T1 = Qr3\ \overline{Qr1\ Qr4}\ \overline{T0}$

$T5 - T0 = Qr3\ \overline{Qr1\ Qr4}$

3.187 Buc, Ioc, Sys, etc.

$Buc = Eom\ \overline{C10}\ \overline{C11}\ \overline{C1}$*

$Ioc1 = Eom\ \overline{C10}\ C11$

$Ioc = Ioc1\ \overline{C1}\ \overline{Er}\ Qr3$*

$Sys = Eom\ C10\ C11\ \overline{C9}$

*$\overline{C1}$ becomes C1 for TMCC-C and TMCC-D

3.188 CPU Signals Received

$C0 = /\overline{Ci0}/$

C1 =

C2 =

C3 =

C4 =

C5 =

C6 =

C7 =

C8 =

C9 =

C10 =

C11 =

C12 =

C13 =

C14 =

C15 =

C16 =

$C17 = /\overline{Ci17}/$

C18	= /$\overline{Ci18}$/
C19	= |
C20	= |
C21	= |
C22	= |
C23	= /$\overline{Ci23}$/
$\overline{Tpc}$	= /$\overline{Tpc}$/
Eom	= /$\overline{Eom}$/
Pot 1	= /$\overline{Pot}$/
Pin	= /$\overline{Pin}$/
$\overline{Rti}$	= /$\overline{Rti}$/
Cpr	= /$\overline{Cpr}$/
C21r	= /$\overline{C21r}$/
C22r	= /$\overline{C22r}$/
C23r	= /$\overline{C23r}$/
Rx	= /$\overline{Rx}$/
$\overline{Tsm}$	= /$\overline{Tsm}$/
Tsr	= /$\overline{Tsr}$/
C1x	= /$\overline{C1x}$/ *For TMCC-C and TMCC-D: C1x = /$\overline{C1x}$/
Pwy	= /$\overline{Pwy}$/ (Pwy = 05 for 92200 and 92210)
$\overline{Mit}$	= /$\overline{Mit}$/
En + (En)	= /$\overline{En + (En)}$ /
St	= /$\overline{St}$/
Skss	= /$\overline{Skss}$/
Kccw	= /$\overline{Kcc0/ + /Kcc1/ + /Kcc2/}$*
$\overline{Kcc2}$	= /Kcc2/
Kccy	= /$\overline{Kcc0/ + /Kcc1/ + /\overline{Kcc2}/}$*

*For TMCC-C and TMCC-D, /Kcc1/ becomes /$\overline{Kcc1}$/

3.189 Input/Output Signals Generated

(C0)	= C0
(C1)	= C1
(C2)	= C2
(C3)	= C3
(C4)	= C4
(C5)	= C5
(C6)	= C6
(C7)	= C7
(C8)	= C8
(C9)	= C9
(C10)	= C10
(C11)	= C11
(C12)	= C12
(C13)	= C13
(C14)	= C14
(C15)	= C15
(C16)	= C16
(C17)	= C17
(C18)	= C18
(C19)	= C19
(C20)	= C20
(C21)	= C21
(C22)	= C22
(C23)	= C23
(C17)	= C17
(C24)	= Cpr (93200 and 92331 only)
(Qq1)	= Qr3 ($\overline{Qr1}$ $\overline{Qr4}$) = T5 - T0
(Qq2)	= (T7 - T3) Qr3 = T6 - T3
(Qq3)	= Qr4 = T7 - T4 Replaces Mtgw on POT connectors at 23F & 24F
(Buc)	= Buc
(Ioc)	= Ioc
(Eom)	= $\overline{Eom\ Er}$
(Sys)	= Sys (T5 - T1) $\overline{Tsr}$ Pwy (delete Pwy for 92200 and 92210)
(St)	= St
(Pin)	= Pin
(Pot 1)	= Pot 1
(Pot 2)	= Pot 1 (T5 - T1) $\overline{Tsr}$ Pwy (delete Pwy for 92200 and 92210)
($\overline{Rti}$)	= $\overline{Rti}$
(Skss)	= Skss

3.190 CPU Signals Generated

/Rd9/	= $\overline{W9\ Kccw}$ $\overline{Y9\ Kccy}$ . . .
/Rd10/	= $\overline{W10\ Kccw}$ $\overline{Y10\ Kccy}$ . . .

$/\overline{Rd11}/ = \overline{W11\ Kccw}\ \overline{Y11\ Kccy}$ . . .

$/\overline{Rd12}/ = \overline{W12\ Kccw}\ \overline{Y12\ Kccy}$ . . .

$/\overline{Rd13}/ = \overline{W13\ Kccw}\ \overline{Y13\ Kccy}$ . . .

$/\overline{Rd14}/ = \overline{W14\ Kccw}\ \overline{Y14\ Kccy}$ . . .

$/\overline{Rde}/ = \overline{We\ Kccw}\ \overline{Ye\ Kccy}$ . . .

$/\overline{Ra0}/ = \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}}$

$/\overline{Ra2}/$ for TMCC-C

$/\overline{Ra1}/ = \overline{\overline{Y10}\ \overline{Y11}\ \overline{Y12}\ \overline{Y13}\ \overline{Y14}}$

$/\overline{Ra3}/$ for TMCC-D

$/\overline{Re0}/$ = We $/\overline{Re2}/$ for TMCC-C

$/\overline{Re1}/$ = Ye $/\overline{Re3}/$ for TMCC-D

$/\overline{\overline{Wf}\,(W0+\overline{W9})}/ = \overline{\overline{Wf}\ (W0+\overline{W9})}$

$/\overline{\overline{Yf}\,(Y0+\overline{Y9})}/ = \overline{\overline{Yf}\ (Y0+\overline{Y9})}$

$/\overline{Trq}/ = \overline{\overline{Trqw\ Trqy\ Trqx}}$

$/I1w/ = \overline{\overline{I1w}}$ $/I1c/$ for TMCC-C

$/I2w/ = \overline{\overline{I2w}}$ $/I2c/$ for TMCC-C

$/I1y/ = \overline{\overline{I1y}}$ $/I1d/$ for TMCC-D

$/I2y/ = \overline{\overline{I2y}}$ $/I2d/$ for TMCC-D

$/\overline{Skrz}/ = \overline{Skr}\ \ \overline{\overline{C10}\ C11\ Ssc}\ \overline{\overline{C1}}\ \overline{\overline{C9}}$

$\overline{\overline{C10}\ C11\ Sio}$ . . .*

*$\overline{C1}$ becomes C1 for TMCC-C and TMCC-D

$/\overline{Rr1}/ = \overline{Wr1\ Rwx}\ \overline{Yr1\ Ryx}$ . . .

$/\overline{Rr2}/ = \overline{Wr2\ Rwx}\ \overline{Yr2\ Ryx}$ . . .

$/\overline{Rr3}/ = \overline{Wr3\ Rwx}\ \overline{Yr3\ Ryx}$ . . .

$/\overline{Rwy1}/ = \overline{Wr1\ Pwy}\ \overline{Yr1\ \overline{Pwy}}$

(Pwy = 05 for 92200 and 92210)

$/\overline{Rwy2}/ = \overline{Wr2\ Pwy}\ \overline{Yr2\ \overline{Pwy}}$

(Pwy = 05 for 92200 and 92210)

$/\overline{Rwy3}/ = \overline{Wr3\ Pwy}\ \overline{Yr3\ \overline{Pwy}}$

(Pwy = 05 for 92200 and 92210)

$(\overline{Cd0}) = (\overline{Cd0})$ . . .

$(\overline{Cd1}) = (\overline{Cd1})$ . . .

$(\overline{Cd2}) = (\overline{Cd2})$ . . .

$(\overline{Cd3}) = (\overline{Cd3})$ . . .

$(\overline{Cd4}) = (\overline{Cd4})$ . . .

$(\overline{Cd5}) = (\overline{Cd5})$ . . .

$(\overline{Cd6}) = (\overline{Cd6})$ . . .

$(\overline{Cd7}) = (\overline{Cd7})$ . . .

$(\overline{Cd8}) = (\overline{Cd8})$ . . .

$(\overline{Cd9}) = (\overline{Cd9})\ \overline{Wa0\ Wpa}\ \overline{Ya0\ Ypa}$ . . .

$(\overline{Cd10}) = (\overline{Cd10})\ \overline{Wa1\ Wpa}\ \overline{Ya1\ Ypa}$ . . .

$(\overline{Cd11}) = (\overline{Cd11})\ \overline{Wa2\ Wpa}\ \overline{Ya2\ Ypa}$ . . .

$(\overline{Cd12}) = (\overline{Cd12})\ \overline{Wa3\ Wpa}\ \overline{Ya3\ Ypa}$ . . .

$(\overline{Cd13}) = (\overline{Cd13})\ \overline{Wa4\ Wpa}\ \overline{Ya4\ Ypa}$ . . .

$(\overline{Cd14}) = (\overline{Cd14})\ \overline{Wa5\ Wpa}\ \overline{Ya5\ Ypa}$ . . .

$(\overline{Cd15}) = (\overline{Cd15})\ \overline{Wa6\ Wpa}\ \overline{Ya6\ Ypa}$ . . .

$(\overline{Cd16}) = (\overline{Cd16})\ \overline{Wa7\ Wpa}\ \overline{Ya7\ Ypa}$ . . .

$(\overline{Cd17}) = (\overline{Cd17})\ \overline{Wa8\ Wpa}\ \overline{Ya8\ Ypa}$ . . .

$(\overline{Cd18}) = (\overline{Cd18})\ \overline{Wa9\ Wpa}\ \overline{Ya9\ Ypa}$ . . .

$(\overline{Cd19}) = (\overline{Cd19})\ \overline{Wa10\ Wpa}\ \overline{Ya10\ Ypa}$ . . .

$(\overline{Cd20}) = (\overline{Cd20})\ \overline{Wa11\ Wpa}\ \overline{Ya11\ Ypa}$ . . .

$(\overline{Cd21}) = (\overline{Cd21})\ \overline{Wa12\ Wpa}\ \overline{Ya12\ Ypa}$ . . .

$(\overline{Cd22}) = (\overline{Cd22})\ \overline{Wa13\ Wpa}\ \overline{Ya13\ Ypa}$ . . .

$(\overline{Cd23}) = (\overline{Cd23})\ \overline{Wa14\ Wpa}\ \overline{Ya14\ Ypa}$ . . .

$(Rt) = (Rt)\ \overline{Wap + Ew}\ \ \overline{Yap + Ey}$ . . .

$(\overline{Cd24}) = (\overline{Cd24})$ (93200 and 93221 only)

$(\overline{Bt}) = (\overline{Bt})$ (93200 and 93221 only)

$/\overline{Ir0}/ = \overline{Wa0\ Rwx}\ \overline{Ya0\ Ryx}$ . . .

$/\overline{Ir1}/ = \overline{Wa1\ Rwx}\ \overline{Ya1\ Ryx}$ . . .

$/\overline{Ir2}/ = \overline{Wa2\ Rwx}\ \overline{Ya2\ Ryx}$ . . .

$/\overline{Ir3}/ = \overline{Wa3\ Rwx}\ \overline{Ya3\ Ryx}$ . . .

$/\overline{Ir4}/ = \overline{Wa4\ Rwx}\ \overline{Ya4\ Ryx}$ . . .

$/\overline{Ir5}/ = \overline{Wa5\ Rwx}\ \overline{Ya5\ Ryx}$ . . .

$/\overline{Ir6}/ = \overline{Wa6\ Rwx}\ \overline{Ya6\ Ryx}$ . . .

$/\overline{Ir7}/ = \overline{Wa7\ Rwx}\ \overline{Ya7\ Ryx}$ . . .

$/\overline{Ir8}/ = \overline{Wa8\ Rwx}\ \overline{Ya8\ Ryx}$ . . .

$/\overline{Ir9}/ = \overline{Wa9\ Rwx}\ \overline{Ya9\ Ryx}$ . . .

$/\overline{Ir10}/ = \overline{Wa10\ Rwx}\ \overline{Ya10\ Ryx}$ . . .

$/\overline{Ir11}/ = \overline{Wa11\ Rwx}\ \overline{Ya11\ Ryx}$ . . .

$/\overline{Ir12}/ = \overline{Wa12\ Rwx}\ \overline{Ya12\ Ryx}$. . .

$/\overline{Ir13}/ = \overline{Wa13\ Rwx}\ \overline{Ya13\ Ryx}$ . . .

$/\overline{Ir14}/ = \overline{Wa14\ Rwx}\ \overline{Ya14\ Ryx}$ . . .

$/\overline{R9}/ = \overline{W9\ Rwx}\ \overline{Y9\ Ryx}$ . . .

3.191 TMCC Signals Received

Er	=	$/\overline{Er}/$
Trqx	=	$/\overline{\overline{Trqx}}/$

3.192 Input/Output Signals Received

Sio	=	$\overline{Sio}$ (circled)
Ssc	=	$\overline{Ssc}$ (circled)

3.193 TMCC Signals Generated

$/\overline{Er}/$	=	$\overline{\overline{Ew}\ \overline{Ey}\ldots}$
$/\overline{Trqx}/$	=	$\overline{\overline{Trq(c)}\ \overline{Trq(d)}}$

3.194 LOGIC EQUATIONS FOR W BUFFER

3.195 Unit Address Register

sW14	=	Ws C23
rW14	=	Wc
sW13	=	Ws C22
rW13	=	Wc
sW12	=	Ws C21
rW12	=	Wc
sW11	=	Ws C20
rW11	=	Wc
sW10	=	$Ws\ C19 + (Ioc\ C12\ \overline{C17}\ \overline{C19}\ \overline{C20}\ \overline{C21}\ \overline{C22}\ \overline{C23})\ \overline{W9}\ \overline{W10}$
rW10	=	Wc

3.196 Input/Output

sW9	=	Ws C18
rW9	=	Wc

3.197 Clear and Set Signals

Wc	=	$Buc\ \overline{C17}\ (T6 + T5) + Wh\ \overline{Wf}\ (T3 - T0) + St$
Ws	=	$Buc\ \overline{C17}\ (T3 - T0)$

3.198 Clock Counter

sW6	=	$\overline{W5}\ Ecw\ T8\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}}$
rW6	=	W5 T0 + Wc
sW5	=	$\overline{W5}\ W6\ \overline{Ecw}\ T0 + Ws\ C13\ C18\ T0\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}}$
rW5	=	W4 T0 + Wc
sW4	=	$W5\ Wf\ T8\ \overline{Wg}$
	+	Ws T0
	+	Wh Wf T8
	+	$Iwg\ \overline{W9}\ \overline{Iwi}\ W5\ Iwf\ T8$
	+	$Iwg\ Wg\ Wf\ W0\ \overline{Wev}\ Iw\ T8\ \overline{\overline{W7}\ \overline{W9}\ W10\ W11\ \overline{Wh}}$
rW4	=	W4 T0 + W4 T8

3.199 Character Counter

sW8	=	Ws C16
	+	$W7\ \overline{W8}\ W4\ T0$
	+	$Wxx\ Wn2\ (\overline{T7 - T0})\ \overline{W4}$
	+	$\overline{W7}\ \overline{W9}\ W10\ W11\ \overline{Wh}$
rW8	=	W8 W4 T0 + Wc
sW7	=	Ws C15
	+	$Wxx\ Wn1\ (\overline{T7 - T0})\ \overline{W4}$
rW7	=	Wc
	+	$W7\ \overline{W8}\ W4\ T0$

3.200 Character Counter Even

Wev	=	$W8\ Wn2\ W7\ Wn1 + \overline{W8}\ \overline{Wn2}\ W7\ Wn1$
	+	$\overline{W8}\ \overline{Wn2}\ \overline{W7}\ \overline{Wn1} + W8\ Wn2\ \overline{W7}\ \overline{Wn1}$

3.201 Halt Interlock

sW0	=	$\overline{W9}\ W6\ \overline{W8}\ Ecw$
	+	Ws C18 W9
rW0	=	Wc
	+	$(Ioc\ C12\ \overline{C17}\ \overline{C19}\ \overline{C20}\ \overline{C21}\ \overline{C22}\ \overline{C23})\ W9\ T0$
	+	$W9\ Iw\ Iwf\ (\overline{Iwg} + \overline{Iwh} + \overline{Iwi})\ \overline{T7 - T0}$

3.202 Computer Interlock

sWf	=	$Wc\ \overline{Wh}$
	+	$Iwa\ \overline{Mit}\ T0$
	+	Rx T0 Pwy *(Pwy = 05 for 92200)

*Rx is always false for TMCC-C

$$
\begin{aligned}
rWf &= \overline{W7}\ \overline{W8}\ W4\ (T6 + T5) \\
&+ Ws\ C18 \\
&+ \overline{W9}\ W10\ W11\ W0\ Mtgw\ \overline{W7}\ (T6 + T5)\ \overline{Wh}
\end{aligned}
$$

3.203 End-of-Record Detector

$$
\begin{aligned}
sWg &= Mtgw\ T0\ Iwg\ W11\ (W0\ \overline{W9} + \overline{W0}\ W5\ \overline{W6}\ W9) \\
&+ Whs\ \overline{T7 - T0}\ \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}} \\
&+ \overline{W9}\ \overline{W10}\ \overline{W11}\ W12\ \overline{W13}\ (\overline{Rw1}\ \overline{Rw2}\ \overline{Rw3} \\
&\quad \overline{Rw4}\ \overline{Rw5}\ \overline{Rw6}\ \overline{Rwp})\ W5\ \overline{T7 - T0} \\
&\quad \overline{\overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}} \\
rWg &= Wc \\
&+ Wg\ \overline{Iwg}\ W11\ T0
\end{aligned}
$$

3.204 Halt Detector

$$
\begin{aligned}
sWh &= Wg\ \overline{Iwg}\ T8 \\
&+ Whs\ W11\ T8 \\
&+ Wg\ \overline{W9}\ \overline{W11}\ \overline{Iwh}\ (Iwf + Wev\ Wf)\ T8\ Iwg \\
&+ W9\ \overline{W11}\ \overline{W0}\ W5\ \overline{W6}\ (\overline{Iwg} + Iwi\ \overline{Iwh})\ T8 \\
&+ \overline{W9}\ \overline{W11}\ Iwg\ \overline{Iwh}\ Iwi\ Iwf\ T8\ W0 \\
&+ W9\ \overline{Iwh}\ T8\ Whs \\
rWh &= Wc\ (T6 + T5) \\
&+ Wh\ \overline{Wf}\ T8
\end{aligned}
$$

3.205 Signal Complete

$$
\begin{aligned}
sWsc &= Wg\ Iwg\ Iwh\ (Wev\ Wf + Iwf)\ T8 \\
&+ Wh\ \overline{Wf}\ T8 + St \\
&+ Ws\ \overline{C19}\ \overline{C20}\ \overline{C21}\ \overline{C22}\ \overline{C23} \\
rWsc &= Wsc\ T8\ \overline{Iwg}
\end{aligned}
$$

3.206 Interrupt Signals

$$
\begin{aligned}
I1w &= \overline{Wf}\ W0\ \overline{Wh}\ (En + \enclose{circle}{En})\ \overline{Iw}\ \overline{Ew}\ \overline{Iwg} \\
&+ Iwg\ \overline{Iw}\ Iwf\ Iwk \\
I2w &= (En + \enclose{circle}{En})\ \overline{Iwg}\ Wh\ \overline{Wf} \\
&+ Wsc\ Iwj\ Iwg
\end{aligned}
$$

3.207 WIM + MIW Interlock =

$$\overline{Wf}\ (W0 + \overline{W9})$$

3.208 Load Buffer from C

$$Wxx = Rx\ Pwy + Rwx\ Tsr\ Iw^{*}$$

(Pwy = 05 and Iw deleted from 92200)

*Rx is always false for TMCC-C

3.209 Time Share Request

$$Trqw = \overline{Wf}\ W0\ \overline{Wh}\ Iw\ \overline{Iwf}$$

3.210 Time Share Select

$$
\begin{aligned}
sRwx &= \overline{Tsm}\ Trqw\ \overline{Trqy}\ \overline{Trqx}\ (\overline{T7 - T0}) \\
rRwx &= \overline{Tsm}\ T0
\end{aligned}
$$

3.211 Time Share Priority

Trqx = Priority signal from TMCC-C and TMCC-D

$$
\begin{aligned}
Trqx &= Trq(c) + Trq(d) \\
Trq &= Trqx + Trqw + Trqy
\end{aligned}
$$

3.212 W Register

$$
\begin{aligned}
Ww1 &= W4\ W7\ (\overline{T7 - T0}) \\
&+ \overline{W4}\ Wn1\ (\overline{T7 - T0}) \\
&+ \overline{W4}\ Wn1\ \overline{Wxx} \\
&+ W4\ Wb1\ (T7 - T0)\ ^{*} \\
&+ \overline{W4}\ C21r\ (T7 - T0)\ Wxx \\
Ww2 &= W4\ W8\ (\overline{T7 - T0}) \\
&+ \overline{W4}\ Wn2\ (\overline{T7 - T0}) \\
&+ \overline{W4}\ Wn2\ \overline{Wxx} \\
&+ W4\ Wb2\ (T7 - T0)^{*} \\
&+ \overline{W4}\ C22r\ (T7 - T0)\ Wxx
\end{aligned}
$$

sWr1, 2, 3 = Ww1, 2, 3 Delayed by 9 pulse times

sWn1, 2, 3 = Wr1, 2, 3 respectively

$$
{}^{*}\left\{
\begin{aligned}
Wb1 &= \overline{Wx12}\ \overline{Wx24}\ Rw4 + Wx12\ Rw10 \\
&+ Wx24\ Rw22 \\
Wb2 &= \overline{Wx12}\ \overline{Wx24}\ Rw5 + Wx12\ Rw11 \\
&+ Wx24\ Rw23
\end{aligned}
\right\} \text{ for 93200 and 93221}
$$

$Ww3 = \overline{W4}\ Wn3\ \overline{Wxx}$
$\quad + W4\ Wb3$ *
$\quad + \overline{W4}\ C23r\ Wxx$

* $Wb3 = \overline{Wx12}\ \overline{Wx24}\ Rw6 + Wx12\ Rw12 + Wx24\ Rw24$ for 93200 and 93221

Wb1, 2, 3 equals Rw4, 5, 6 respectively for 92200
Wb1, 2, 3 equals Rw10, 11, 12 respectively for 92201
Wb1, 2, 3 equals Rw22, 23, 24 respectively for 92202

3.213 Character Buffer*

$sRw1 = W4\ \overline{Wxx}\ (T7 - T0)\ Wn1 + \overline{W9}\ W6\ \overline{W5}\ Zw1 + W4\ Wxx\ C21r$

$rRw1 = W4\ \overline{Wxx}\ \overline{Wn1} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4} + W4\ Wxx\ \overline{C21r}$

$sRw2 = W4\ \overline{Wxx}\ (T7 - T0)\ Wn2 + \overline{W9}\ W6\ \overline{W5}\ Zw2 + W4\ Wxx\ C22r$

$rRw2 = W4\ \overline{Wxx}\ \overline{Wn2} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4} + W4\ Wxx\ \overline{C22r}$

$sRw3 = W4\ \overline{Wxx}\ (T7 - T0)\ Wn3 + \overline{W9}\ W6\ \overline{W5}\ Zw3 + W4\ Wxx\ C23r$

$rRw3 = W4\ \overline{Wxx}\ \overline{Wn3} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4} + W4\ Wxx\ \overline{C23r}$

$sRw4 = W4\ \overline{Rw4}\ Rw1 + \overline{W9}\ W6\ \overline{W5}\ Zw4$
$rRw4 = W4\ Rw4\ \overline{Rw1} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

$sRw5 = W4\ \overline{Rw5}\ Rw2 + \overline{W9}\ W6\ \overline{W5}\ Zw5$
$rRw5 = W4\ Rw5\ \overline{Rw2} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

$sRw6 = W4\ \overline{Rw6}\ Rw3 + \overline{W9}\ W6\ \overline{W5}\ Zw6$
$rRw6 = W4\ Rw6\ \overline{Rw3} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

*For 12-bit extension, add Rw7 through Rw12
For 24-bit extension, add Rw7 through Rw24

Character Size

12 bit character = Wx12 (93200 and 93221 only)
24 bit character = Wx24 (93200 and 93221 only)

3.214 Character Buffer Extended to 12 Bits

$sRw7 = W4\ \overline{Rw7}\ Rw4 + \overline{W9}\ W6\ \overline{W5}\ Zw7$
$rRw7 = W4\ Rw7\ \overline{Rw4} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

$sRw8 = W4\ \overline{Rw8}\ Rw5 + \overline{W9}\ W6\ \overline{W5}\ Zw8$
$rRw8 = W4\ Rw8\ \overline{Rw5} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

$sRw9 = W4\ \overline{Rw9}\ Rw6 + \overline{W9}\ W6\ \overline{W5}\ Zw9$
$rRw9 = W4\ Rw9\ \overline{Rw6} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

$sRw10 = W4\ \overline{Rw10}\ Rw7 + \overline{W9}\ W6\ \overline{W5}\ Zw10$
$rRw10 = W4\ Rw10\ \overline{Rw7} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

$sRw11 = W4\ \overline{Rw11}\ Rw8 + \overline{W9}\ W6\ \overline{W5}\ Zw11$
$rRw11 = W4\ Rw11\ \overline{Rw8} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

$sRw12 = W4\ \overline{Rw12}\ Rw9 + \overline{W9}\ W6\ \overline{W5}\ Zw12$
$rRw12 = W4\ Rw12\ \overline{Rw9} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

3.215 Character Buffer Extended to 24 Bits

$sRw13 = W4\ \overline{Rw13}\ Rw10 + \overline{W9}\ W6\ \overline{W5}\ Zw13$
$rRw13 = W4\ Rw13\ \overline{Rw10} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$
$sRw14 = W4\ \overline{Rw14}\ Rw11 + \overline{W9}\ W6\ \overline{W5}\ Zw14$
$rRw14 = W4\ Rw14\ \overline{Rw11} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$
$sRw15 = W4\ \overline{Rw15}\ Rw12 + \overline{W9}\ W6\ \overline{W5}\ Zw15$
$rRw15 = W4\ Rw15\ \overline{Rw12} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$
$sRw16 = W4\ \overline{Rw16}\ Rw13 + \overline{W9}\ W6\ \overline{W5}\ Zw16$
$rRw16 = W4\ Rw16\ \overline{Rw13} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

$sRw17 = W4\ \overline{Rw17}\ Rw14 + \overline{W9}\ W6\ \overline{W5}\ Zw17$
$rRw17 = W4\ Rw17\ \overline{Rw14} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

$sRw18 = W4\ \overline{Rw18}\ Rw15 + \overline{W9}\ W6\ \overline{W5}\ Zw18$
$rRw18 = W4\ Rw18\ \overline{Rw15} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

$sRw19 = W4\ \overline{Rw19}\ Rw16 + \overline{W9}\ W6\ \overline{W5}\ Zw19$
$rRw19 = W4\ Rw19\ \overline{Rw16} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

$sRw20 = W4\ \overline{Rw20}\ Rw17 + \overline{W9}\ W6\ \overline{W5}\ Zw20$
$rRw20 = W4\ Rw20\ \overline{Rw17} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

$sRw21 = W4\ \overline{Rw21}\ Rw18 + \overline{W9}\ W6\ \overline{W5}\ Zw21$
$rRw21 = W4\ Rw21\ \overline{Rw18} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

$sRw22 = W4\ \overline{Rw22}\ Rw19 + \overline{W9}\ W6\ \overline{W5}\ Zw22$
$rRw22 = W4\ Rw22\ \overline{Rw19} + \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$

sRw23 $= W4\,\overline{Rw23}\,Rw20 + \overline{W9}\,W6\,\overline{W5}\,Zw23$

rRw23 $= W4\,Rw23\,\overline{Rw20} + \overline{W9}\,\overline{W6}\,\overline{W5}\,\overline{W4}$

sRw24 $= W4\,\overline{Rw24}\,Rw21 + \overline{W9}\,W6\,\overline{W5}\,Zw24$

rRw24 $= W4\,Rw24\,\overline{Rw21} + \overline{W9}\,\overline{W6}\,\overline{W5}\,\overline{W4}$

3.216 Parity Flip-Flop

sRwp $= \overline{W9}\,W4\,\overline{Rwp}\,(Wb1 \oplus Wb2 \oplus Wb3)\,(T7 - T0)\;Qw1$ *

$+ W9\,W4\,\overline{Rwp}\,\overline{Wxx}\,(Wn1 \oplus Wn2 \oplus Wn3)\,Qw2\,(T7 - T0)$ *

$+ W9\,W4\,\overline{Rwp}\,Wxx\,Cpr\,Qw2\,(T7 - T0)$ *

$+ \overline{W9}\,W6\,\overline{W5}\,Zwp$

$+ Wf\,W5\,T8\,\overline{Rwp}$

rRwp $= \overline{W9}\,W4\,Rwp\,(Wb1 \oplus Wb2 \oplus Wb3)\,(T7 - T0)\,Qw1$ *

$+ W9\,W4\,Rwp\,\overline{Wxx}\,(Wn1 \oplus Wn2 \oplus Wn3)\,Qw2\,(T7 - T0)$ *

$+ W9\,W4\,Rwp\,Wxx\,Cpr\,Qw2\,(T7 - T0)$ *

$+ \overline{W9}\,\overline{W6}\,\overline{W5}\,\overline{W4}$

$+ Wf\,W5\,T8\,\overline{W9}\,Rwp$

$+ Wc$

* Qw1 $= \overline{Wx12\,\overline{Qr4} + \overline{Wx12}\,\overline{Wx24}\,\overline{Qr1}\,\overline{Qr4}}$ (for 93200 and 93221)

Qw2 $= \overline{Wx12\,Qr4 + \overline{Wx12}\,\overline{Wx24}\,\overline{Qr2}\,\overline{Qr4}}$ (for 93200 and 93221)

Qw1 = Qr1 Qr4 for 92200

Qw1 = Qr4 for 92201

Qw1 is deleted for 92202

Qw2 = Qr2 $\overline{Qr4}$ for 92200

Qw2 = $\overline{Qr4}$ for 92201

Qw2 is deleted for 92202

3.217 Error Detector

sWe $= \overline{W9}\,\overline{W6}\,\overline{W5}\,\overline{W4}\,Rwp\,\overline{Wg}\,Npw\,(\overline{Iwg} + Iwi + \overline{Iwf})$

$+ W0\,\overline{W6}\,W5\,Ecw\,T8$

$+ Wes$

rWe $= Wc\,\overline{Wh}$

3.218 Interlace Prepare

sEw $= Iwc\,\overline{Ew}\,(T3 - T0)$

rEw $= Wc\,T0$

$+ Pot\,1\,(T3 - T0)\,Ew$

3.219 Interlace Clear

Iwc $= Eom\,C9\,\overline{C10}\;\;\overline{C1}\,\overline{C17}\,(T3 - T0)$ *

* $\overline{C1}$ becomes C1 for TMCC-C

3.220 Interlace Load

Iwp $= Pot\,1\,(T6 - T5)\,Ew$

Iwe $= Ioc\,1\,(T6 + T5)\,Ew$

3.221 Interlace Active

sIw $= Pot\,1\,(T3 - T0)\,Ew\,\overline{Iw}$

rIw $= Iwf\,T8\,(\overline{T7 - T0})$

$+ (Wc + Iwc + Ws\,\overline{C19}\,\overline{C20}\,\overline{C21}\,\overline{C22}\,\overline{C23})\,(T3 - T0)\,Iw$

3.222 Zero Count

Iwf $= Wc0\,Wc1\,Wc2\,Wc3\,Wc4\,Wc5\,Wc6\,Wc7\,Wc8\,Wc9\,Wc10\,Wc11\,Wc12\,Wc13\,Wc14\,Ew$

3.223 Interlace Count Trigger

Iwa $= Rwx\;Tsm$

3.224 Interlace Counter Clock Enables

Computer Clock Enable: $Ew\,\overline{Iw}$

Counter Clock Enable: $\overline{Ew}$

3.225 Extend Operations

sIwg $= Iwe\,C12$

rIwg $= Iwc + Wsc\,T8\,\overline{W10}\,\overline{W11}\,\overline{W12}\,\overline{W13}\,\overline{W14}\,Iwg$

3.226 Channel Command Interrupt Enables

$sIwj = Iwe\ C13$ (Eor)

$rIwj = Iwc + I2w\ T8\ Iwj$

$sIwk = Iwe\ C14$ (Iwf)

$rIwk = Iwc + I1w\ T8\ Iwk$

3.227 Channel Command Register

$sIwh = Iwe\ C15$

$rIwh = Iwc$

$sIwi = Iwe\ C16$

$rIwi = Iwc$

3.228 Word Counter

$sWc14 = Iwc + \overline{Ew}\ \overline{Wc14}\ \underline{Iwa\ \overline{Ew}}$

$rWc14 = Iwp\ C9 + \overline{Ew}\ Wc14\ \underline{Iwa\ \overline{Ew}}$

$sWc13 = Iwc + \overline{Ew}\ \overline{Wc13}\ \underline{Wc14\ \overline{Ew}}$

$rWc13 = Iwp\ C8 + \overline{Ew}\ Wc13\ \underline{Wc14\ \overline{Ew}}$

$sWc12 = Iwc + \overline{Ew}\ \overline{Wc12}\ Wc13\ \underline{Wc14\ \overline{Ew}}$

$rWc12 = Iwp\ C7 + \overline{Ew}\ \overline{Wc12}\ Wc13\ \underline{Wc14\ \overline{Ew}}$

$sWc11 = Iwc + \overline{Ew}\ \overline{Wc11}\ Wc12\ Wc13\ \underline{Wc14\ \overline{Ew}}$

$rWc11 = Iwp\ C6 + \overline{Ew}\ Wc11\ Wc12\ Wc13\ \underline{Wc14\ \overline{Ew}}$

$sWc10 = Iwc + \overline{Ew}\ \overline{Wc10}\ \underline{Wc11\ \overline{Ew}}$

$rWc10 = Iwp\ C5 + \overline{Ew}\ Wc10\ \underline{Wc11\ \overline{Ew}}$

$sWc9 = Iwc + \overline{Ew}\ \overline{Wc9}\ Wc10\ \underline{Wc11\ \overline{Ew}}$

$rWc9 = Iwp\ C4 + \overline{Ew}\ Wc9\ Wc10\ \underline{Wc11\ \overline{Ew}}$

$sWc8 = Iwc + \overline{Ew}\ \overline{Wc8}\ Wc9\ Wc10\ \underline{Wc11\ \overline{Ew}}$

$rWc8 = Iwp\ C3 + \overline{Ew}\ Wc8\ Wc9\ Wc10\ \underline{Wc11\ \overline{Ew}}$

$sWc7 = Iwc + \overline{Ew}\ \overline{Wc7}\ \underline{Wc8\ \overline{Ew}}$

$rWc7 = Iwp\ C2 + \overline{Ew}\ Wc7\ \underline{Wc8\ \overline{Ew}}$

$sWc6 = Iwc + \overline{Ew}\ \overline{Wc6}\ Wc7\ \underline{Wc8\ \overline{Ew}}$

$rWc6 = Iwp\ C1 + \overline{Ew}\ Wc6\ Wc7\ \underline{Wc8\ \overline{Ew}}$

$sWc5 = Iwc + \overline{Ew}\ \overline{Wc5}\ Wc6\ Wc7\ \underline{Wc8\ \overline{Ew}}$

$rWc5 = Iwp\ C0 + \overline{Ew}\ Wc5\ Wc6\ Wc7\ \underline{Wc8\ \overline{Ew}}$

$sWc4 = Iwc + \overline{Ew}\ \overline{Wc4}\ Wc5\ \overline{Ew}$

$rWc4 = Iwe\ C23 + \overline{Ew}\ Wc4\ \underline{Wc5\ \overline{Ew}}$

$sWc3 = Iwc + \overline{Ew}\ \overline{Wc3}\ Wc4\ \underline{Wc5\ \overline{Ew}}$

$rWc3 = Iwe\ C22 + \overline{Ew}\ Wc3\ Wc4\ \underline{Wc5\ \overline{Ew}}$

$sWc2 = Iwc + \overline{Ew}\ \overline{Wc2}\ Wc3\ Wc4\ \underline{Wc5\ \overline{Ew}}$

$rWc2 = Iwe\ C21 + \overline{Ew}\ Wc2\ Wc3\ Wc4\ \underline{Wc5\ \overline{Ew}}$

$sWc1 = Iwc + \overline{Ew}\ \overline{Wc1}\ \underline{Wc2\ \overline{Ew}}$

$rWc1 = Iwe\ C20 + \overline{Ew}\ Wc1\ \underline{Wc2\ \overline{Ew}}$

$sWc0 = Iwc + \overline{Ew}\ \overline{Wc0}\ Wc1\ \underline{Wc2\ \overline{Ew}}$

$rWc0 = Iwe\ C19$

3.229 Address Counter

$sWa14 = Iwc + \overline{Ew}\ \overline{Wa14}\ \underline{Iwa\ \overline{Ew}}$

$rWa14 = Iwp\ \overline{C23} + \overline{Ew}\ Wa14\ \underline{Iwa\ \overline{Ew}}$

$sWa13 = Iwc + \overline{Ew}\ \overline{Wa13}\ Wa14\ \underline{Iwa\ \overline{Ew}}$

$rWa13 = Iwp\ \overline{C22} + \overline{Ew}\ Wa13\ Wa14\ \underline{Iwa\ \overline{Ew}}$

$sWa12 = Iwc + \overline{Ew}\ \overline{Wa12}\ \underline{Wa13\ \overline{Ew}}$

$rWa12 = Iwp\ \overline{C21} + \overline{Ew}\ Wa12\ \underline{Wa13\ \overline{Ew}}$

$sWa11 = Iwc + \overline{Ew}\ \overline{Wa11}\ Wa12\ \underline{Wa13\ \overline{Ew}}$

$rWa11 = Iwp\ \overline{C20} + \overline{Ew}\ Wa11\ Wa12\ \underline{Wa13\ \overline{Ew}}$

$sWa10 = Iwc + \overline{Ew}\ \overline{Wa10}\ Wa11\ Wa12\ \underline{Wa13\ \overline{Ew}}$

$rWa10 = Iwp\ \overline{C19} + \overline{Ew}\ Wa10\ Wa11\ Wa12\ \underline{Wa13\ \overline{Ew}}$

$sWa9 = Iwp\ C18 + \overline{Ew}\ \overline{Wa9}\ \underline{Wa10\ \overline{Ew}}$

$rWa9 = Iwc + \overline{Ew}\ Wa9\ \underline{Wa10\ \overline{Ew}}$

$sWa8 = Iwp\ C17 + \overline{Ew}\ \overline{Wa8}\ Wa9\ \underline{Wa10\ \overline{Ew}}$

$rWa8 = Iwc + \overline{Ew}\ Wa8\ Wa9\ \underline{Wa10\ \overline{Ew}}$

$sWa7 = Iwp\ C16 + \overline{Ew}\ \overline{Wa7}\ Wa8\ Wa9\ \underline{Wa10\ \overline{Ew}}$

$rWa7 = Iwc + \overline{Ew}\ Wa7\ Wa8\ Wa9\ \underline{Wa10\ \overline{Ew}}$

$sWa6 = Iwp\ C15 + \overline{Ew}\ \overline{Wa6}\ \underline{Wa7\ \overline{Ew}}$

$rWa6 = Iwc + \overline{Ew}\ Wa6\ \underline{Wa7\ \overline{Ew}}$

$sWa5 = Iwp\ C14 + \overline{Ew}\ \overline{Wa5}\ Wa6\ \underline{Wa7\ \overline{Ew}}$

$rWa5 = Iwc + \overline{Ew}\ Wa5\ Wa6\ \underline{Wa7\ \overline{Ew}}$

$sWa4 = Iwp\ C13 + \overline{Ew}\ \overline{Wa4}\ Wa5\ Wa6\ \underline{Wa7\ \overline{Ew}}$

$rWa4 = Iwc + \overline{Ew}\ Wa4\ Wa5\ Wa6\ \underline{Wa7\ \overline{Ew}}$

$sWa3 = Iwp\ C12 + \overline{Ew}\ \overline{Wa3}\ \underline{Wa4\ \overline{Ew}}$

$rWa3 = Iwc + \overline{Ew}\ Wa3\ \underline{Wa4\ \overline{Ew}}$

$sWa2 = Iwp\ C11 + \overline{Ew}\ \overline{Wa2}\ Wa3\ \underline{Wa4\ \overline{Ew}}$

$rWa2 = Iwc + \overline{Ew}\ Wa2\ Wa3\ \underline{Wa4\ \overline{Ew}}$

$sWa1 = Iwp\ C10 + \overline{Ew}\ \overline{Wa1}\ Wa2\ Wa3\ \underline{Wa4\ \overline{Ew}}$

$rWa1 = Iwc + \overline{Ew}\ Wa1\ Wa2\ Wa3\ \underline{Wa4\ \overline{Ew}}$

$sWa0 = Iwe\ C18 + \overline{Ew}\ \overline{Wa0}\ \underline{Wa1\ \overline{Ew}}$

$rWa0 = Iwc$

3.230 PIN Address Counter

$sWpa = Ioc\ \overline{C17}\ C13\ \overline{C19}\ \overline{C20}\ \overline{C21}\ \overline{C22}\ \overline{C23}\ T0$

$rWpa = Pin\ T0 + St$

3.231 Skip Gate:

$$
\begin{aligned}
Skr = {} & \overline{C1}\ \overline{C17}\ \overline{C9}\ \overline{C10}\ C11\ \overline{C19}\ \overline{C20}\ \overline{C21}\ \overline{C22} \\
& \overline{C23}\ C15\ Wsc^* \\
+ {} & \overline{C1}\ \overline{C17}\ \overline{C9}\ \overline{C10}\ C11\ \overline{C19}\ \overline{C20}\ \overline{C21}\ \overline{C22} \\
& \overline{C23}\ C12\ \overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}^* \\
+ {} & \overline{C1}\ \overline{C17}\ \overline{C9}\ \overline{C10}\ C11\ \overline{C19}\ \overline{C20}\ \overline{C21}\ \overline{C22} \\
& \overline{C23}\ C13\ Iwf^* \\
+ {} & \overline{C1}\ \overline{C17}\ \overline{C9}\ \overline{C10}\ C11\ \overline{C19}\ \overline{C20}\ \overline{C21}\ \overline{C22} \\
& \overline{C23}\ C14\ \overline{We}^* \\
+ {} & C10\ \overline{C11}\ C14\ \overline{W10}\ \overline{W11}\ \overline{W12}\ \overline{W13}\ \overline{W14}\ \overline{C1}^* \\
+ {} & C10\ \overline{C11}\ C20\ We\ \overline{C1}^* \\
+ {} & ---
\end{aligned}
$$

*$\overline{C1}$ becomes C1 for TMCC-C

3.232 Input/Output Signals Received

Zwp = (Zwp)
Zw1 = (Zw1)
Zw2 = (Zw2)
Zw3 = (Zw3)
Zw4 = (Zw4)
Zw5 = (Zw5)
Zw6 = (Zw6)
Zw7 = (Zw7)
Zw8 = (Zw8)
Zw9 = (Zw9)
Zw10 = (Zw10)
Zw11 = (Zw11)
Zw12 = (Zw12)
Zw13 = (Zw13)
Zw14 = (Zw14)
Zw15 = (Zw15)
Zw16 = (Zw16)
Zw17 = (Zw17)
Zw18 = (Zw18)
Zw19 = (Zw19)
Zw20 = (Zw20)
Zw21 = (Zw21)
Zw22 = (Zw22)
Zw23 = (Zw23)
Whs = (Whs)
Wes = (Wes)
Mtgw = (Mtgw)
Npw = (Npw)
Ecw = (Ecw)
Wx12 = (Wx12) (93200 and 93221 only)
Wx24 = (Wx24) (93200 and 93221 only)

3.233 Input/Output Signals Generated

(Rwp) = Rwp
(Rw1) = Rw1
(Rw2) = Rw2
(Rw3) = Rw3
(Rw4) = Rw4
(Rw5) = Rw5
(Rw6) = Rw6
(Rw7) = Rw7
(Rw8) = Rw8
(Rw9) = Rw9
(Rw10) = Rw10
(Rw11) = Rw11

(Rw12) = Rw12

(Rw13) = Rw13

(Rw14) = Rw14

(Rw15) = Rw15

(Rw16) = Rw16

(Rw17) = Rw17

(Rw18) = Rw18

(Rw19) = Rw19

(Rw20) = Rw20

(Rw21) = Rw21

(Rw22) = Rw22

(Rw23) = Rw23

(Rw24) = Rw24

(W9) = W9

(W10) = W10

(W11) = W11

(W12) = W12

(W13) = W13

(W0) = W0

(W5) = W5

(W6) = W6

(Iw) = Iw

3.234 LOGIC EQUATIONS FOR Y BUFFER

3.235 Unit Address Register

$sY14 = Ys\ C23$

$rY14 = Yc$

$sY13 = Ys\ C22$

$rY13 = Yc$

$sY12 = Ys\ C21$

$rY12 = Yc$

$sY11 = Ys\ C20$

$rY11 = Yc$

$sY10 = Ys\ C19 + (Ioc\ C12\ C17\ \overline{C19}\ \overline{C20}\ \overline{C21}\ \overline{C22}\ \overline{C23})\ \overline{Y9}\ \overline{Y10}$

$rY10 = Yc$

3.236 Input/Output

$sY9 = Ys\ C18$

$rY9 = Yc$

3.237 Clear and Set Signals

$Yc = Buc\ C17\ (T6 + T5) + Yh\ \overline{Yf}\ (T3 - T0) + St$

$Ys = Buc\ C17\ (T3 - T0)$

3.238 Clock Counter

$sY6 = \overline{Y5}\ Ecy\ T8\ \overline{\overline{Y10}\ \overline{Y11}\ \overline{Y12}\ \overline{Y13}\ \overline{Y14}}$

$rY6 = Y5\ T0 + Yc$

$sY5 = \overline{Y5}\ Y6\ \overline{Ecy}\ T0 + Ys\ C13\ C18\ T0\ \overline{\overline{Y10}\ \overline{Y11}\ \overline{Y12}\ \overline{Y13}\ \overline{Y14}}$

$rY5 = Y4\ T0 + Yc$

$sY4 = Y5\ Yf\ T8\ \overline{Yg}$
$+ Ys\ T0$
$+ Yh\ Yf\ T8$
$+ Iyg\ \overline{Y9}\ \overline{Iyi}\ Y5\ Iyf\ T8$
$+ Iyg\ Yg\ Yf\ Y0\ \overline{Yev}\ Iy\ T8\ \overline{\overline{Y7}\ \overline{Y9}\ Y10\ Y11\ \overline{Yh}}$

$rY4 = Y4\ T0 + Y4\ T8$

3.239 Character Counter

$sY8 = Ys\ C16$
$+ Y7\ \overline{Y8}\ Y4\ T0$
$+ Yxx\ Yn2\ (\overline{T7 - T0})\ \overline{Y4}$
$+ \overline{Y7}\ \overline{Y9}\ Y10\ Y11\ \overline{Yh}$

$rY8 = Yc$
$+ Y8\ Y4\ T0$

$sY7 = Ys\ C15$
$+ Yxx\ Yn1\ (\overline{T7 - T0})\ Y4$

$rY7 = Yc$
$+ Y7\ \overline{Y8}\ Y4\ T0$

3.240 Character Counter Even

$Yev = Y8\ Yn2\ Y7\ Yn1 + \overline{Y8}\ \overline{Yn2}\ Y7\ Yn1$
$+ \overline{Y8}\ \overline{Yn2}\ \overline{Y7}\ \overline{Yn1} + Y8\ Yn2\ \overline{Y7}\ \overline{Yn1}$

3.241 Halt Interlock

sY0 $= \overline{Y9}\ Y6\ \overline{Y8}\ Ecy$

$+\ Ys\ C18\ Y9$

rY0 $= Yc$

$+\ (Ioc\ C12\ C17\ \overline{C19}\ \overline{C20}\ \overline{C21}\ \overline{C22}\ \overline{C23})$

$Y9\ T0$

$+\ Y9\ Iy\ Iyf\ (\overline{Iyg} + \overline{Iyh} + \overline{Iyi})\ \overline{T7 - T0}$

3.242 Computer Interlock

sYf $= Yc\ \overline{Yh}$

$+\ Iya\ \overline{Mit}\ T0$

$+\ Rx\ T0\ \overline{Pwy}$ * ($\overline{Pwy} = \overline{05}$ for 92210)

rYf $= \overline{Y7}\ \overline{Y8}\ Y4\ (T6 + T5)$

$+\ Ys\ C18$

$+\ \overline{Y9}\ Y10\ Y11\ Y0\ Mtgy\ \overline{Y7}\ (T6 + T5)\ \overline{Yh}$

*Rx is always false for TMCC-D

3.243 End-of-Record Detector

sYg $= Mtgy\ T0\ Iyg\ Y11\ (Y0\ \overline{Y9} + \overline{Y0}\ Y5\ \overline{Y6}\ Y9)$

$+\ Yhs\ \overline{T7 - T0}\ \overline{\overline{Y10}\ \overline{Y11}\ \overline{Y12}\ \overline{Y13}\ \overline{Y14}}$

$+\ \overline{Y9}\ \overline{Y10}\ \overline{Y11}\ Y12\ \overline{Y13}\ (\overline{Ry1}\ \overline{Ry2}\ \overline{Ry3}\ \overline{Ry4}$

$\overline{Ry5}\ \overline{Ry6}\ \overline{Ryp})\ Y5\ \overline{T7 - T0}\ \overline{\overline{Y10}\ \overline{Y11}\ \overline{Y12}\ \overline{Y13}\ \overline{Y14}}$

rYg $= Yc$

$+\ Yg\ \overline{Iyg}\ Y11\ T0$

3.244 Halt Detector

sYh $= Yg\ \overline{Iyg}\ T8$

$+\ Yhs\ Y11\ T8$

$+\ Yg\ \overline{Y9}\ \overline{Y11}\ \overline{Iyh}\ (Iyf + Yev\ Yf)\ T8\ Iyg$

$+\ Y9\ \overline{Y11}\ \overline{Y0}\ Y5\ \overline{Y6}\ (\overline{Iyg} + Iyi\ \overline{Iyh})\ T8$

$+\ \overline{Y9}\ \overline{Y11}\ Iyg\ \overline{Iyh}\ Iyi\ Iyf\ T8\ Y0$

$+\ Y9\ \overline{Iyh}\ Yhs\ T8$

rYh $= Yc\ (T6 + T5)$

$+\ Yh\ \overline{Yf}\ T8$

3.245 Signal Complete

sYsc $= Yg\ Iyg\ Iyh\ \ (Yev\ Yf + Iyf)\ T8$

$+\ Yh\ \overline{Yf}\ T8 + St$

$+\ Ys\ \overline{C19}\ \overline{C20}\ \overline{C21}\ \overline{C22}\ \overline{C23}$

rYsc $= Ysc\ T0\ \overline{Iyg}$

3.246 Interrupt Signals

I1y $= \overline{Yf}\ Y0\ \overline{Yh}\ (En + (En))\ \overline{Iy}\ \overline{Ey}\ \overline{Iyg}$ (second En circled)

$+\ Iyg\ \overline{Iy}\ Iyf\ Iyk$

I2y $= (En + (En))\ \overline{Iyg}\ Yh\ \overline{Yf}$ (second En circled)

$+\ Ysc\ Iyj\ Iyg$

3.247 YIM + MIY Interlock =

$\overline{Yf}\ (Y0 + \overline{Y9})$

3.248 Load Buffer from C

Yxx $= Rx\ \overline{Pwy} + Ryx\ Tsr\ Iy$ * ($\overline{Pwy} = \overline{05}$ and Iy deleted for 92210)

*Rx is always false for TMCC-D

3.249 Time Share Request

Trqy $= \overline{Yf}\ Y0\ Yh\ Iy\ \overline{Iyf}$

3.250 Time Share Select

sRyx $= \overline{Tsm}\ Trqy\ \overline{Trqx}\ (\overline{T7 - T0})$

rRyx $= \overline{Tsm}\ T0$

3.251 Time Share Priority

Trqx = Priority Signal from TMCC-C and TMCC-D

Trqx $= Trq(c) + Trq(d)$

Trq $= Trqx + Trqw + Trqy$

3.252 Y Register

Yw1 $= Y4\ Y7\ (\overline{T7 - T0})$

$+\ \overline{Y4}\ Yn1\ (\overline{T7 - T0})$

$+\ \overline{Y4}\ Yn1\ \overline{Yxx}$

$+ Y4\ Yb1\ (T7 - T0)$ *

$+ \overline{Y4}\ C21r\ (T7 - T0)\ Yxx$

$Yw2 = Y4\ Y8\ \overline{(T7 - T0)}$

$+ \overline{Y4}\ Yn2\ \overline{(T7 - T0)}$

$+ \overline{Y4}\ Yn2\ \overline{Yxx}$

$+ Y4\ Yb2\ (T7 - T0)$ *

$+ \overline{Y4}\ C23r\ (T7 - T0)\ Yxx$

$Yw3 = \overline{Y4}\ Yn3\ \overline{Yxx}$

$+ Y4\ Yb3$ *

$+ \overline{Y4}\ C23r\ Yxx$

sYr1, 2, 3 = Yw1, 2, 3 delayed by 9 pulse times

sYn1, 2, 3 = Yr1, 2, 3 respectively

* $Yb1 = \overline{Yx12}\ \overline{Yx24}\ Ry4 + Yx12\ Ry10 + Yx24\ Ry22$

$Yb2 = \overline{Yx12}\ \overline{Yx24}\ Ry5 + Yx12\ Ry11 + Yx24\ Ry23$

$Yb3 = \overline{Yx12}\ \overline{Yx24}\ Ry6 + Yx12\ Ry12 + Yx24\ Ry24$

(for 93221)

Yb1, 2, 3 equals Ry4, 5, 6 respectively for 92210

Yb1, 2, 3 equals Ry10, 11, 12 respectively for 92211

Yb1, 2, 3 equals Ry22, 23, 24 respectively for 92212

3.253 Character Buffer Extended to 12 Bits

$sRy7 = Y4\ \overline{Ry7}\ Ry4 + \overline{Y9}\ Y6\ \overline{Y5}\ Zy7$

$rRy7 = Y4\ Ry7\ \overline{Ry4} + \overline{Y9}\ \overline{Y6}\ \overline{Y5}\ \overline{Y4}$

$sRy8 = Y4\ \overline{Ry8}\ Ry5 + \overline{Y9}\ Y6\ \overline{Y5}\ Zy8$

$rRy8 = Y4\ Ry8\ \overline{Ry5} + \overline{Y9}\ \overline{Y6}\ \overline{Y5}\ \overline{Y4}$

$sRy9 = Y4\ \overline{Ry9}\ Ry6 + \overline{Y9}\ Y6\ \overline{Y5}\ Zy9$

$rRy9 = Y4\ Ry9\ \overline{Ry6} + \overline{Y9}\ \overline{Y6}\ \overline{Y5}\ \overline{Y4}$

$sRy10 = Y4\ \overline{Ry10}\ Ry7 + \overline{Y9}\ Y6\ \overline{Y5}\ Zy10$

$rRy10 = Y4\ Ry10\ \overline{Ry7} + \overline{Y9}\ \overline{Y6}\ \overline{Y5}\ \overline{Y4}$

$sRy11 = Y4\ \overline{Ry11}\ Ry8 + \overline{Y9}\ Y6\ \overline{Y5}\ Zy11$

$rRy11 = Y4\ Ry11\ \overline{Ry8} + \overline{Y9}\ \overline{Y6}\ \overline{Y5}\ \overline{Y4}$

$sRy12 = Y4\ \overline{Ry12}\ Ry9 + \overline{Y9}\ Y6\ \overline{Y5}\ Zy12$

$rRy12 = Y4\ Ry12\ \overline{Ry9} + \overline{Y9}\ \overline{Y6}\ \overline{Y5}\ \overline{Y4}$

3.254 Character Buffer *

$sRy1 = Y4\ \overline{Yxx}\ (T7 - T0)\ Yn1 + \overline{Y9}\ Y6\ \overline{Y5}\ Zy1 + Y4\ Yxx\ C21r$

$rRy1 = Y4\ \overline{Yxx}\ \overline{Yn1} + \overline{Y9}\ \overline{Y6}\ \overline{Y5}\ \overline{Y4} + Y4\ Yxx\ \overline{C21r}$

$sRy2 = Y4\ \overline{Yxx}\ (T7 - T0)\ Yn2 + \overline{Y9}\ Y6\ \overline{Y5}\ Zy2 + Y4\ Yxx\ C22r$

$rRy2 = Y4\ \overline{Yxx}\ \overline{Yn2} + \overline{Y9}\ \overline{Y6}\ \overline{Y5}\ \overline{Y4} + Y4\ Yxx\ \overline{C22r}$

$sRy3 = Y4\ \overline{Yxx}\ (T7 - T0)\ Yn3 + \overline{Y9}\ Y6\ \overline{Y5}\ Zy3 + Y4\ Yxx\ C23r$

$rRy3 = Y4\ \overline{Yxx}\ \overline{Yn3} + \overline{Y9}\ \overline{Y6}\ \overline{Y5}\ \overline{Y4} + Y4\ Yxx\ \overline{C23r}$

$sRy4 = Y4\ \overline{Ry4}\ Ry1 + \overline{Y9}\ Y6\ \overline{Y5}\ Zy4$

$rRy4 = Y4\ Ry4\ \overline{Ry1} + \overline{Y9}\ \overline{Y6}\ \overline{Y5}\ \overline{Y4}$

$sRy5 = Y4\ \overline{Ry5}\ Ry2 + \overline{Y9}\ Y6\ \overline{Y5}\ Zy5$

$rRy5 = Y4\ Ry5\ \overline{Ry2} + \overline{Y9}\ \overline{Y6}\ \overline{Y5}\ \overline{Y4}$

$sRy6 = Y4\ \overline{Ry6}\ Ry3 + \overline{Y9}\ Y6\ \overline{Y5}\ Zy6$

$rRy6 = Y4\ Ry6\ \overline{Ry3} + \overline{Y9}\ \overline{Y6}\ \overline{Y5}\ \overline{Y4}$

* For 12-bit extension, add Ry7 through Ry12
For 24-bit extension, add Ry7 through Ry24

Character Size

12 bit character = Yx12 (93221 only)

24 bit character = Yx24 (93221 only)

3.255 Character Buffer Extended to 24 bits

$sRy13 = Y4\ \overline{Ry13}\ Ry10 + \overline{Y9}\ Y6\ \overline{Y5}\ Zy13$

$rRy13 = Y4\ Ry13\ \overline{Ry10} + \overline{Y9}\ \overline{Y6}\ \overline{Y5}\ \overline{Y4}$

$sRy14 = Y4\ \overline{Ry14}\ Ry11 + \overline{Y9}\ Y6\ \overline{Y5}\ Zy14$

$rRy14 = Y4\ Ry14\ \overline{Ry11} + \overline{Y9}\ \overline{Y6}\ \overline{Y5}\ \overline{Y4}$

$sRy15 = Y4\,\overline{Ry15}\,Ry12 + \overline{Y9}\,Y6\,\overline{Y5}\,Zy15$

$rRy15 = Y4\,Ry15\,\overline{Ry12} + \overline{Y9}\,\overline{Y6}\,\overline{Y5}\,\overline{Y4}$

$sRy16 = Y4\,\overline{Ry16}\,Ry13 + \overline{Y9}\,Y6\,\overline{Y5}\,Zy16$

$rRy16 = Y4\,Ry16\,\overline{Ry13} + \overline{Y9}\,\overline{Y6}\,\overline{Y5}\,\overline{Y4}$

$sRy17 = Y4\,\overline{Ry17}\,Ry14 + \overline{Y9}\,Y6\,\overline{Y5}\,Zy17$

$rRy17 = Y4\,Ry17\,\overline{Ry14} + \overline{Y9}\,\overline{Y6}\,\overline{Y5}\,\overline{Y4}$

$sRy18 = Y4\,\overline{Ry18}\,Ry15 + \overline{Y9}\,Y6\,\overline{Y5}\,Zy18$

$rRy18 = Y4\,Ry18\,\overline{Ry15} + \overline{Y9}\,\overline{Y6}\,\overline{Y5}\,\overline{Y4}$

$sRy19 = Y4\,\overline{Ry19}\,Ry16 + \overline{Y9}\,Y6\,\overline{Y5}\,Zy19$

$rRy19 = Y4\,Ry19\,\overline{Ry16} + \overline{Y9}\,\overline{Y6}\,\overline{Y5}\,\overline{Y4}$

$sRy20 = Y4\,\overline{Ry20}\,Ry17 + \overline{Y9}\,Y6\,\overline{Y5}\,Zy20$

$rRy20 = Y4\,Ry20\,\overline{Ry17} + \overline{Y9}\,\overline{Y6}\,\overline{Y5}\,\overline{Y4}$

$sRy21 = Y4\,\overline{Ry21}\,Ry18 + \overline{Y9}\,Y6\,\overline{Y5}\,Zy21$

$rRy21 = Y4\,Ry21\,\overline{Ry18} + \overline{Y9}\,\overline{Y6}\,\overline{Y5}\,\overline{Y4}$

$sRy22 = Y4\,\overline{Ry22}\,Ry19 + \overline{Y9}\,Y6\,\overline{Y5}\,Zy22$

$rRy22 = Y4\,Ry22\,\overline{Ry19} + \overline{Y9}\,\overline{Y6}\,\overline{Y5}\,\overline{Y4}$

$sRy23 = Y4\,\overline{Ry23}\,Ry20 + \overline{Y9}\,Y6\,\overline{Y5}\,Zy23$

$rRy23 = Y4\,Ry23\,\overline{Ry20} + \overline{Y9}\,\overline{Y6}\,\overline{Y5}\,\overline{Y4}$

$sRy24 = Y4\,\overline{Ry24}\,Ry21 + \overline{Y9}\,Y6\,\overline{Y5}\,Zy24$

$rRy24 = Y4\,Ry24\,\overline{Ry21} + \overline{Y9}\,\overline{Y6}\,\overline{Y5}\,\overline{Y4}$

3.256 Parity Flip-Flop

$sRyp = \overline{Y9}\,Y4\,\overline{Ryp}\,(Yb1 \oplus Yb2 \oplus Yb3)\,(T7-T0)\,Qy1^*$

$+ Y9\,Y4\,\overline{Ryp}\,\overline{Yxx}\,(Yn1 \oplus Yn2 \oplus Yn3)\,Qy2\,(T7-T0)^*$

$+ Y9\,Y4\,\overline{Ryp}\,Yxx\,Cpr\,Qy2\,(T7-T0)^*$

$+ \overline{Y9}\,Y6\,\overline{Y5}\,Zyp$

$+ Yf\,Y5\,T8\,\overline{Ryp}$

$rRyp = \overline{Y9}\,Y4\,Ryp\,(Yb1 \oplus Yb2 \oplus Yb3)\,(T7-T0)\,Qy1^*$

$+ Y9\,Y4\,Ryp\,\overline{Yxx}\,(Yn1 \oplus Yn2 \oplus Yn3)\,Qy2\,(T7-T0)^*$

$+ Y9\,Y4\,Ryp\,Yxx\,Cpr\,Qy2\,(T7-T0)^*$

$+ \overline{Y9}\,\overline{Y6}\,\overline{Y5}\,\overline{Y4}$

$+ Yf\,Y5\,T8\,\overline{Y9}\,Ryp$

$+ Yc$

$^*Qy1 = \overline{Yx12\,\overline{Qr4} + \overline{Yx12}\,\overline{Yx24}\,\overline{Qr1}\,\overline{Qr4}}$ for 93221

$Qy2 = Yx12\,Qr4 + \overline{Yx12}\,\overline{Yx24}\,\overline{\overline{Qr2}\,\overline{Qr4}}$ for 93221

$Qy1 = Qr1\,Qr4$ for 92210

$Qy1 = Qr4$ for 92211

Qr1 is deleted for 92212

$Qy2 = Qr2\,\overline{Qr4}$ for 92210

$Qy2 = \overline{Qr4}$ for 92211

Qy2 is deleted for 92212

3.257 Error Detector

$sYe = \overline{Y9}\,\overline{Y6}\,\overline{Y5}\,\overline{Y4}\,Ryp\,\overline{Yg}\,Npy\,(\overline{Iyg} + Iyi + \overline{Iyf})$

$+ Y0\,\overline{Y6}\,Y5\,Ecy\,T8$

$+ Yes$

$rYe = Yc\,\overline{Yh}$

3.258 Interlace Prepare

$sEy = Iyc\,\overline{Ey}\,(T3-T0)$

$rEy = Yc\,T0$

$+ Pot\,1\,(T3-T0)\,Ey$

3.259 Interlace Clear

$Iyc = Eom\,C9\,\overline{C10}\,\overline{C1}\,C17\,(T3-T0)^*$

$^*\overline{C1}$ becomes C1 for TMCC-D

3.260 Interlace Load

$Iyp = Pot\,1\,(T6+T5)\,Ey$

$Iye = Ioc\,1\,Ey\,(T6+T5)$

3.261 Interlace Active

$sIy = Pot\,1\,(T3-T0)\,Ey\,\overline{Iy}$

$rIy = Iyf\,T8$

$+ (Yc + Iyc + Ys\,\overline{C19}\,\overline{C20}\,\overline{C21}\,\overline{C22}\,\overline{C23})\,(T3-T0)\,Iy$

3.262 Zero Count

Iyf = Yc0 Yc1 Yc2 Yc3 Yc4 Yc5 Yc6 Yc7 Yc8 Yc9 Yc10 Yc11 Yc12 Yc13 Yc14 $\overline{Ey}$

3.263 Interlace Count Trigger

Iya = Ryx Tsm

3.264 Interlace Counter Clock Enables

Computer Clock Enable: Ey $\overline{Iy}$

Counter Clock Enable: $\overline{Ey}$

3.265 Extend Operations

sIyg = Iye C12

rIyg = Iyc + Ysc T8 $\overline{Y10}\ \overline{Y11}\ \overline{Y12}\ \overline{Y13}\ \overline{Y14}$ Iyg

3.266 Channel Command Interrupt Enables

sIyj = Iye C13

rIyj = Iyc + I2y T8 Iyj

sIyk = Iye C14

rIyk = Iyc + I1y T8 Iyk

3.267 Channel Command Register

sIyh = Iye C15

rIyh = Iyc

sIyi = Iye C16

rIyi = Iyc

3.268 Word Counter

sYc14 = Iyc + $\overline{Ey}\ \overline{Yc14}\ \underline{Iya\ \overline{Ey}}$

rYc14 = Iyp C9 + $\overline{Ey}$ Yc14 $\underline{Iya\ \overline{Ey}}$

sYc13 = Iyc + $\overline{Ey}\ \overline{Yc13}$ Yc14 $\overline{Ey}$

rYc13 = Iyp C8 + $\overline{Ey}$ Yc13 $\underline{Yc14\ \overline{Ey}}$

sYc12 = Iyc + $\overline{Ey}\ \overline{Yc12}$ Yc13 Yc14 $\overline{Ey}$

rYc12 = Iyp C7 + $\overline{Ey}$ Yc12 Yc13 $\underline{Yc14\ \overline{Ey}}$

sYc11 = Iyc + $\overline{Ey}\ \overline{Yc11}$ Yc12 Yc13 Yc14 $\overline{Ey}$

rYc11 = Iyp C6 + $\overline{Ey}$ Yc11 Yc12 Yc13 $\underline{Yc14\ \overline{Ey}}$

sYc10 = Iyc + $\overline{Ey}\ \overline{Yc10}\ \underline{Yc11\ \overline{Ey}}$

rYc10 = Iyp C5 + $\overline{Ey}$ Yc10 $\underline{Yc11\ \overline{Ey}}$

sYc9 = Iyc + $\overline{Ey}\ \overline{Yc9}$ Yc10 $\underline{Yc11\ \overline{Ey}}$

rYc9 = Iyp C4 + $\overline{Ey}$ Yc9 Yc10 $\underline{Yc11\ \overline{Ey}}$

sYc8 = Iyc + $\overline{Ey}\ \overline{Yc8}$ Yc9 Yc10 $\underline{Yc11\ \overline{Ey}}$

rYc8 = Iyp C3 + $\overline{Ey}$ Yc8 Yc9 Yc10 $\underline{Yc11\ \overline{Ey}}$

sYc7 = Iyc + $\overline{Ey}\ \overline{Yc7}\ \underline{Yc8\ \overline{Ey}}$

rYc7 = Iyp C2 + $\overline{Ey}$ Yc7 $\underline{Yc8\ \overline{Ey}}$

sYc6 = Iyc + $\overline{Ey}\ \overline{Yc6}$ Yc7 $\underline{Yc8\ \overline{Ey}}$

rYc6 = Iyp C1 + $\overline{Ey}$ Yc6 Yc7 $\underline{Yc8\ \overline{Ey}}$

sYc5 = Iyc + $\overline{Ey}\ \overline{Yc5}$ Yc6 Yc7 $\underline{Yc8\ \overline{Ey}}$

rYc5 = Iyp C0 + $\overline{Ey}$ Yc5 Yc6 Yc7 $\underline{Yc8\ \overline{Ey}}$

sYc4 = Iyc + $\overline{Ey}\ \overline{Yc4}\ \underline{Yc5\ \overline{Ey}}$

rYc4 = Iye C23 + $\overline{Ey}$ Yc4 $\underline{Yc5\ \overline{Ey}}$

sYc3 = Iyc + $\overline{Ey}\ \overline{Yc3}$ Yc4 $\underline{Yc5\ \overline{Ey}}$

rYc3 = Iye C22 + $\overline{Ey}$ Yc3 Yc4 $\underline{Yc5\ \overline{Ey}}$

sYc2 = Iyc + $\overline{Ey}\ \overline{Yc2}$ Yc3 Yc4 $\underline{Yc5\ \overline{Ey}}$

rYc2 = Iye C21 + $\overline{Ey}$ Yc2 Yc3 Yc4 $\underline{Yc5\ \overline{Ey}}$

sYc1 = Iyc + $\overline{Ey}\ \overline{Yc1}\ \underline{Yc2\ \overline{Ey}}$

rYc1 = Iye C20 + $\overline{Ey}$ Yc1 $\underline{Yc2\ \overline{Ey}}$

sYc0 = Iyc + $\overline{Ey}\ \overline{Yc0}$ Yc1 $\underline{Yc2\ \overline{Ey}}$

rYc0 = Iye C19

3.269 Address Counter

sYa14 = Iyc + $\overline{Ey}\ \overline{Ya14}\ \underline{Iya\ \overline{Ey}}$

rYa14 = Iyp $\overline{C23}$ + $\overline{Ey}$ Ya14 $\underline{Iya\ \overline{Ey}}$

sYa13 = Iyc + $\overline{Ey}\ \overline{Ya13}$ Ya14 $\underline{Iya\ \overline{Ey}}$

rYa13 = Iyp $\overline{C22}$ + $\overline{Ey}$ Ya13 Ya14 $\underline{Iya\ \overline{Ey}}$

sYa12 = Iyc + $\overline{Ey}\ \overline{Ya12}\ \underline{Ya13\ \overline{Ey}}$

rYa12 = Iyp $\overline{C21}$ + $\overline{Ey}$ Ya12 $\underline{Ya13\ \overline{Ey}}$

sYa11 = Iyc + $\overline{Ey}\ \overline{Ya11}$ Ya12 $\underline{Ya13\ \overline{Ey}}$

rYa11 = Iyp $\overline{C20}$ + $\overline{Ey}$ Ya11 Ya12 $\underline{Ya13\ \overline{Ey}}$

sYa10 = Iyc + $\overline{Ey}\ \overline{Ya10}$ Ya11 Ya12 $\underline{Ya13\ \overline{Ey}}$

rYa10 = Iyp $\overline{C19}$ + $\overline{Ey}$ Ya10 Ya11 Ya12 $\underline{Ya13\ \overline{Ey}}$

$\mathrm{sYa9} = \mathrm{Iyp\ C18} + \overline{\mathrm{Ey}}\ \overline{\mathrm{Ya9}}\ \underline{\mathrm{Ya10}\ \overline{\mathrm{Ey}}}$

$\mathrm{rYa9} = \mathrm{Iyc} + \overline{\mathrm{Ey}}\ \mathrm{Ya9}\ \underline{\mathrm{Ya10}\ \overline{\mathrm{Ey}}}$

$\mathrm{sYa8} = \mathrm{Iyp\ C17} + \overline{\mathrm{Ey}}\ \overline{\mathrm{Ya8}}\ \mathrm{Ya9}\ \underline{\mathrm{Ya10}\ \overline{\mathrm{Ey}}}$

$\mathrm{rYa8} = \mathrm{Iyc} + \overline{\mathrm{Ey}}\ \mathrm{Ya8\ Ya9}\ \underline{\mathrm{Ya10}\ \overline{\mathrm{Ey}}}$

$\mathrm{sYa7} = \mathrm{Iyp\ C16} + \overline{\mathrm{Ey}}\ \overline{\mathrm{Ya7}}\ \mathrm{Ya8\ Ya9}\ \underline{\mathrm{Ya10}\ \overline{\mathrm{Ey}}}$

$\mathrm{rYa7} = \mathrm{Iyc} + \overline{\mathrm{Ey}}\ \mathrm{Ya7\ Ya8\ Ya9}\ \underline{\mathrm{Ya10}\ \overline{\mathrm{Ey}}}$

$\mathrm{sYa6} = \mathrm{Iyp\ C15} + \overline{\mathrm{Ey}}\ \overline{\mathrm{Ya6}}\ \underline{\mathrm{Ya7}\ \overline{\mathrm{Ey}}}$

$\mathrm{rYa6} = \mathrm{Iyc} + \overline{\mathrm{Ey}}\ \mathrm{Ya6}\ \underline{\mathrm{Ya7}\ \overline{\mathrm{Ey}}}$

$\mathrm{sYa5} = \mathrm{Iyp\ C14} + \overline{\mathrm{Ey}}\ \overline{\mathrm{Ya5}}\ \mathrm{Ya6}\ \underline{\mathrm{Ya7}\ \overline{\mathrm{Ey}}}$

$\mathrm{rYa5} = \mathrm{Iyc} + \overline{\mathrm{Ey}}\ \mathrm{Ya5\ Ya6}\ \underline{\mathrm{Ya7}\ \overline{\mathrm{Ey}}}$

$\mathrm{sYa4} = \mathrm{Iyp\ C13} + \overline{\mathrm{Ey}}\ \overline{\mathrm{Ya4}}\ \mathrm{Ya5\ Ya6}\ \underline{\mathrm{Ya7}\ \overline{\mathrm{Ey}}}$

$\mathrm{rYa4} = \mathrm{Iyc} + \overline{\mathrm{Ey}}\ \mathrm{Ya4\ Ya5\ Ya6}\ \underline{\mathrm{Ya7}\ \overline{\mathrm{Ey}}}$

$\mathrm{sYa3} = \mathrm{Iyp\ C12} + \overline{\mathrm{Ey}}\ \overline{\mathrm{Ya3}}\ \underline{\mathrm{Ya4}\ \overline{\mathrm{Ey}}}$

$\mathrm{rYa3} = \mathrm{Iyc} + \overline{\mathrm{Ey}}\ \mathrm{Ya3}\ \underline{\mathrm{Ya4}\ \overline{\mathrm{Ey}}}$

$\mathrm{sYa2} = \mathrm{Iyp\ C11} + \overline{\mathrm{Ey}}\ \overline{\mathrm{Ya2}}\ \mathrm{Ya3}\ \underline{\mathrm{Ya4}\ \overline{\mathrm{Ey}}}$

$\mathrm{rYa2} = \mathrm{Iyc} + \overline{\mathrm{Ey}}\ \mathrm{Ya2\ Ya3}\ \underline{\mathrm{Ya4}\ \overline{\mathrm{Ey}}}$

$\mathrm{sYa1} = \mathrm{Iyp\ C10} + \overline{\mathrm{Ey}}\ \overline{\mathrm{Ya1}}\ \mathrm{Ya2\ Ya3}\ \underline{\mathrm{Ya4}\ \overline{\mathrm{Ey}}}$

$\mathrm{rYa1} = \mathrm{Iyc} + \overline{\mathrm{Ey}}\ \mathrm{Ya1\ Ya2\ Ya3}\ \underline{\mathrm{Ya4}\ \overline{\mathrm{Ey}}}$

$\mathrm{sYa0} = \mathrm{Iye\ C18} + \overline{\mathrm{Ey}}\ \overline{\mathrm{Ya0}}\ \underline{\mathrm{Ya1}\ \overline{\mathrm{Ey}}}$

$\mathrm{rYa0} = \mathrm{Iyc}$

3.270 Pin Address Counter

$\mathrm{sYpa} = \mathrm{Ioc\ C17\ C13}\ \overline{\mathrm{C19}}\ \overline{\mathrm{C20}}\ \overline{\mathrm{C21}}\ \overline{\mathrm{C22}}\ \overline{\mathrm{C23}}\ \mathrm{T0}$

$\mathrm{rYpa} = \mathrm{Pin\ T0} + \mathrm{St}$

3.271 Skip Gate

$\mathrm{Skr} = \overline{\mathrm{C1}}\ \mathrm{C17}\ \overline{\mathrm{C9}}\ \overline{\mathrm{C10}}\ \mathrm{C11}\ \overline{\mathrm{C19}}\ \overline{\mathrm{C20}}\ \overline{\mathrm{C21}}\ \overline{\mathrm{C22}}\ \overline{\mathrm{C23}}\ \mathrm{C15\ Ysc}^*$

$+ \overline{\mathrm{C1}}\ \mathrm{C17}\ \overline{\mathrm{C9}}\ \overline{\mathrm{C10}}\ \mathrm{C11}\ \overline{\mathrm{C19}}\ \overline{\mathrm{C20}}\ \overline{\mathrm{C21}}\ \overline{\mathrm{C22}}\ \overline{\mathrm{C23}}\ \mathrm{C12}\ \overline{\mathrm{Y10}}\ \overline{\mathrm{Y11}}\ \overline{\mathrm{Y12}}\ \overline{\mathrm{Y13}}\ \overline{\mathrm{Y14}}^*$

$+ \overline{\mathrm{C1}}\ \mathrm{C17}\ \overline{\mathrm{C9}}\ \overline{\mathrm{C10}}\ \mathrm{C11}\ \overline{\mathrm{C19}}\ \overline{\mathrm{C20}}\ \overline{\mathrm{C21}}\ \overline{\mathrm{C22}}\ \overline{\mathrm{C23}}\ \mathrm{C13\ Iyf}^*$

$+ \overline{\mathrm{C1}}\ \mathrm{C17}\ \overline{\mathrm{C9}}\ \overline{\mathrm{C10}}\ \mathrm{C11}\ \overline{\mathrm{C19}}\ \overline{\mathrm{C20}}\ \overline{\mathrm{C21}}\ \overline{\mathrm{C22}}\ \overline{\mathrm{C23}}\ \mathrm{C14}\ \overline{\mathrm{Ye}}^*$

$+ \mathrm{C10}\ \overline{\mathrm{C11}}\ \mathrm{C13}\ \overline{\mathrm{Y10}}\ \overline{\mathrm{Y11}}\ \overline{\mathrm{Y12}}\ \overline{\mathrm{Y13}}\ \overline{\mathrm{Y14}}\ \overline{\mathrm{C1}}^*$

$+ \mathrm{C10}\ \overline{\mathrm{C11}}\ \mathrm{C19}\ \overline{\mathrm{Ye}}\ \overline{\mathrm{C1}}^*$

$+ - - -$

*$\overline{\mathrm{C1}}$ becomes C1 for TMCC-D

3.272 Input/Output Signals Received

$\mathrm{Zyp} = \overline{\mathrm{Zyp}}$

$\mathrm{Zy1} = \overline{\mathrm{Zy1}}$

$\mathrm{Zy2} = \overline{\mathrm{Zy2}}$

$\mathrm{Zy3} = \overline{\mathrm{Zy3}}$

$\mathrm{Zy4} = \overline{\mathrm{Zy4}}$

$\mathrm{Zy5} = \overline{\mathrm{Zy5}}$

$\mathrm{Zy6} = \overline{\mathrm{Zy6}}$

$\mathrm{Zy7} = \overline{\mathrm{Zy7}}$

$\mathrm{Zy8} = \overline{\mathrm{Zy8}}$

$\mathrm{Zy9} = \overline{\mathrm{Zy9}}$

$\mathrm{Zy10} = \overline{\mathrm{Zy10}}$

$\mathrm{Zy11} = \overline{\mathrm{Zy11}}$

$\mathrm{Zy12} = \overline{\mathrm{Zy12}}$

$\mathrm{Zy13} = \overline{\mathrm{Zy13}}$

$\mathrm{Zy14} = \overline{\mathrm{Zy14}}$

$\mathrm{Zy15} = \overline{\mathrm{Zy15}}$

$\mathrm{Zy16} = \overline{\mathrm{Zy16}}$

$\mathrm{Zy17} = \overline{\mathrm{Zy17}}$

$\mathrm{Zy18} = \overline{\mathrm{Zy18}}$

$\mathrm{Zy19} = \overline{\mathrm{Zy19}}$

$\mathrm{Zy20} = \overline{\mathrm{Zy20}}$

$\mathrm{Zy21} = \overline{\mathrm{Zy21}}$

$\mathrm{Zy22} = \overline{\mathrm{Zy22}}$

$\mathrm{Zy23} = \overline{\mathrm{Zy23}}$

Yhs	= ($\overline{\text{Yhs}}$)	
Yes	= ($\overline{\text{Yes}}$)	
$\overline{\text{Mtgy}}$	= ($\overline{\overline{\text{Mtgy}}}$)	
$\overline{\text{Npy}}$	= ($\overline{\overline{\text{Npy}}}$)	
Ecy	= ($\overline{\text{Ecy}}$)	
Yx12	= ($\overline{\text{Yx12}}$)	(93221 only)
Yx24	= ($\overline{\text{Yx24}}$)	(93221 only)

3.273 <u>Input/Output Signals Generated</u>

(Ryp)	= Ryp
(Ry1)	= Ry1
(Ry2)	= Ry2
(Ry3)	= Ry3
(Ry4)	= Ry4
(Ry5)	= Ry5
(Ry6)	= Ry6
(Ry7)	= Ry7
(Ry8)	= Ry8
(Ry9)	= Ry9
(Ry10)	= Ry10
(Ry11)	= Ry11
(Ry12)	= Ry12
(Ry13)	= Ry13
(Ry14)	= Ry14
(Ry15)	= Ry15
(Ry16)	= Ry16
(Ry17)	= Ry17
(Ry18)	= Ry18
(Ry19)	= Ry19
(Ry20)	= Ry20
(Ry21)	= Ry21
(Ry22)	= Ry22
(Ry23)	= Ry23
(Ry24)	= Ry24
(Y9)	= Y9
(Y10)	= Y10
(Y11)	= Y11
(Y12)	= Y12
(Y13)	= Y13
(Y14)	= Y14
(Y0)	= Y0
(Y5)	= Y5
(Y6)	= Y6
(Iy)	= Iy

SECTION IV
INSTALLATION AND MAINTENANCE

4.1 GENERAL

4.2 This section contains information relating to the installation and maintenance of Model 932XX series TMCCs. As the Model 922XX series TMCCs are no longer being installed, only the Model 932XX series is covered in this section.

4.3 INSTALLATION

4.4 The basic 925/930/9300 computers are shipped with the TMCC physically installed. After installation of the computer, the intercabling of the TMCCs must be performed.

4.5 INTERCABLING

4.6 Figure 4-1 illustrates typical intercabling of the Model 93200 TMCC for the 925/930/9300 computers. Figure 4-2 illustrates the intercabling of the Model 93221 TMCC. Power distribution for the various chassis is illustrated in figure 4-3.

4.7 Intercabling of the input/output devices to the W (or A) channel may be found in the applicable input/output device technical manual.

4.8 After intercabling the TMCCs and the input/output devices, a program should be run to ensure proper operation of the W (or A) channel. Any diagnostic program utilizing the input/output device may be run.

4.9 925/930 COMPUTER W CHANNEL TEST PROGRAM

4.10 Table 4-1 lists a sample program which may be run to check out the W channel for proper operation. This test program causes the message ASSEMBLY DONE ENTER NEW PROGRAM to be typed out under program control. The computer stores the internal codes for these characters in memory beginning in location 2000. The routine inserts the carriage return code, 52, and the space code, 12, where needed and requests End-of-Record interrupt. It is written as a closed subroutine using interrupts, channel W and Typewriter Number One. The internal code for the output message is as follows:

A S S E 21 62 62 25	M B L Y 44 22 43 71	Sp D O N 12 24 46 45	E C/R E N 25 52 25 45	2000
T E R Sp 62 25 51 12	N E W Sp 45 25 66 12	P R O G 47 51 46 27	R A M Sp 51 21 44 12	2004

4.11 9300 COMPUTER A CHANNEL TEST PROGRAM

4.12 Table 4-2 lists a sample program which may be run to check out the A channel for proper operation. This test program causes the message ASSEMBLY DONE ENTER NEW PROGRAM to be typed out under program control. The computer internal codes for these characters are stored beginning in location 02000. The carriage return code, 052, and the space code, 012, are inserted where needed. The End-of-Record interrupt is requested. The routine is written as a closed subroutine which uses interrupts, channel A, and Typewriter Number One. The internal code for the output message is the same as given in paragraph 4.10.

4.13 MODULE LOCATION

4.14 Figure 4-4 illustrates the location of all modules for the various models of TMCCs.

4.15 MAINTENANCE

4.16 The following information is presented as an aid in maintaining the Models 932XX TMCCs. Presented herein are descriptions and timing diagrams of the signals available on the various input/output connectors and the diagnostic test programs for maintenance of the TMCC.

4.17 PERIODIC INSPECTION

4.18 No periodic inspection is required for the TMCC other than that required for the computer as a whole. No attempt should be made to periodically check for loose wires, poor solder connections, or bent pins because of the packaging density of the wiring and components and the possibility of causing malfunctions. Wiring layout and length is critical in some areas and should not be touched except for correcting a malfunction.

4.19 CORRECTIVE MAINTENANCE

4.20 If it should become necessary to replace a component on a module, the physical location of the component, quantity, type, and part number are indicated on the module drawings contained in Section 6.

4.21 INPUT/OUTPUT SIGNALS AND TIMING RELATIONSHIPS

4.22 The signals described are available on the input/output connectors as illustrated in figure 4-5. The signals are theoretical and do not take into consideration circuit and transmission delays which tend to add 200 to 400 nanoseconds of delay.

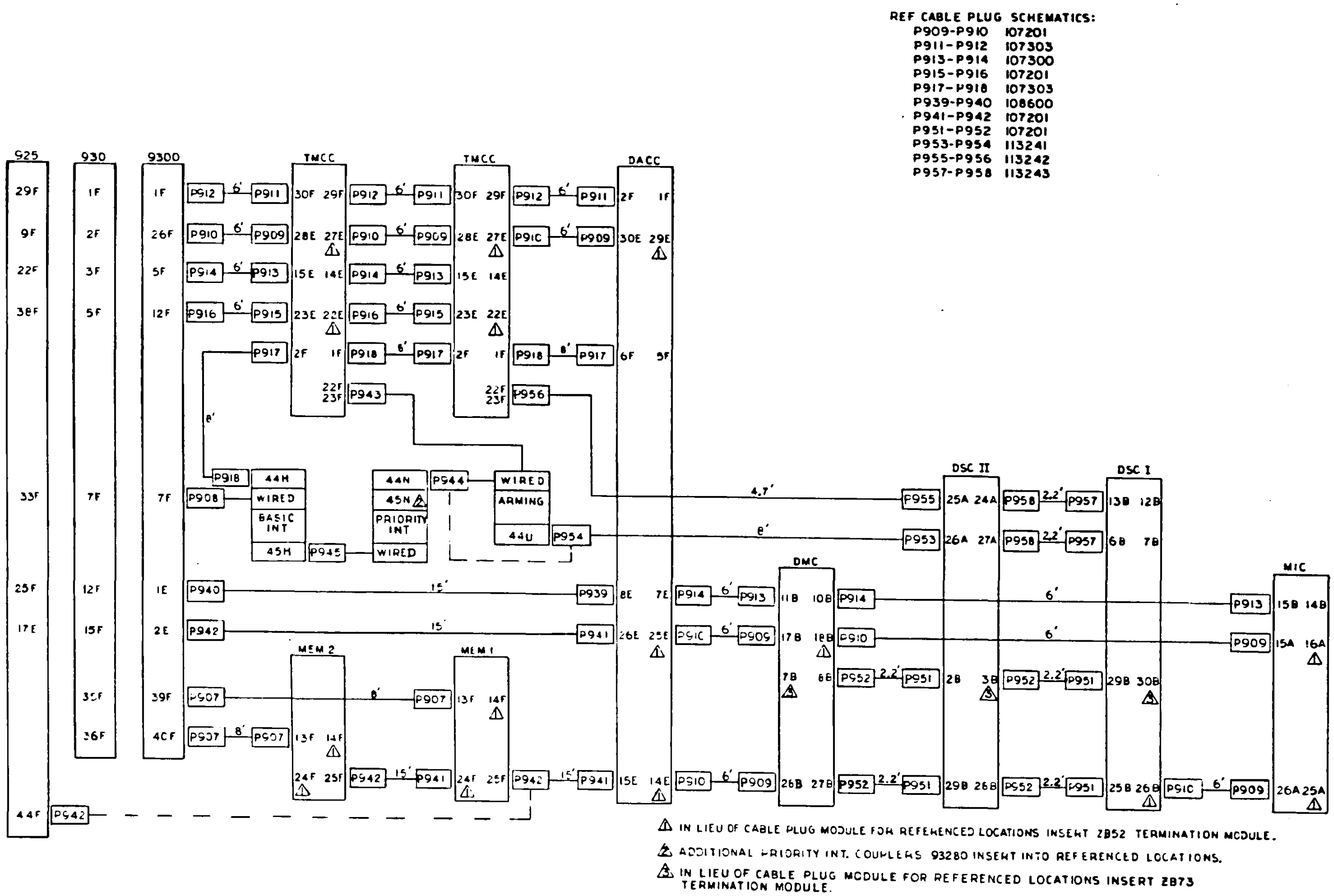


Figure 4-1. Model 93200 TMCC, Intercabling Diagram

REF CABLE PLUG SCHEMATICS:

P909-P910	107201
P911-P912	107303
P913-P914	107300
P915-P916	107201
P917-P918	107303
P939-P940	108600
P941-P942	107201
P951-P952	107201
P953-P954	113241
P955-P956	113242
P957-P958	113243

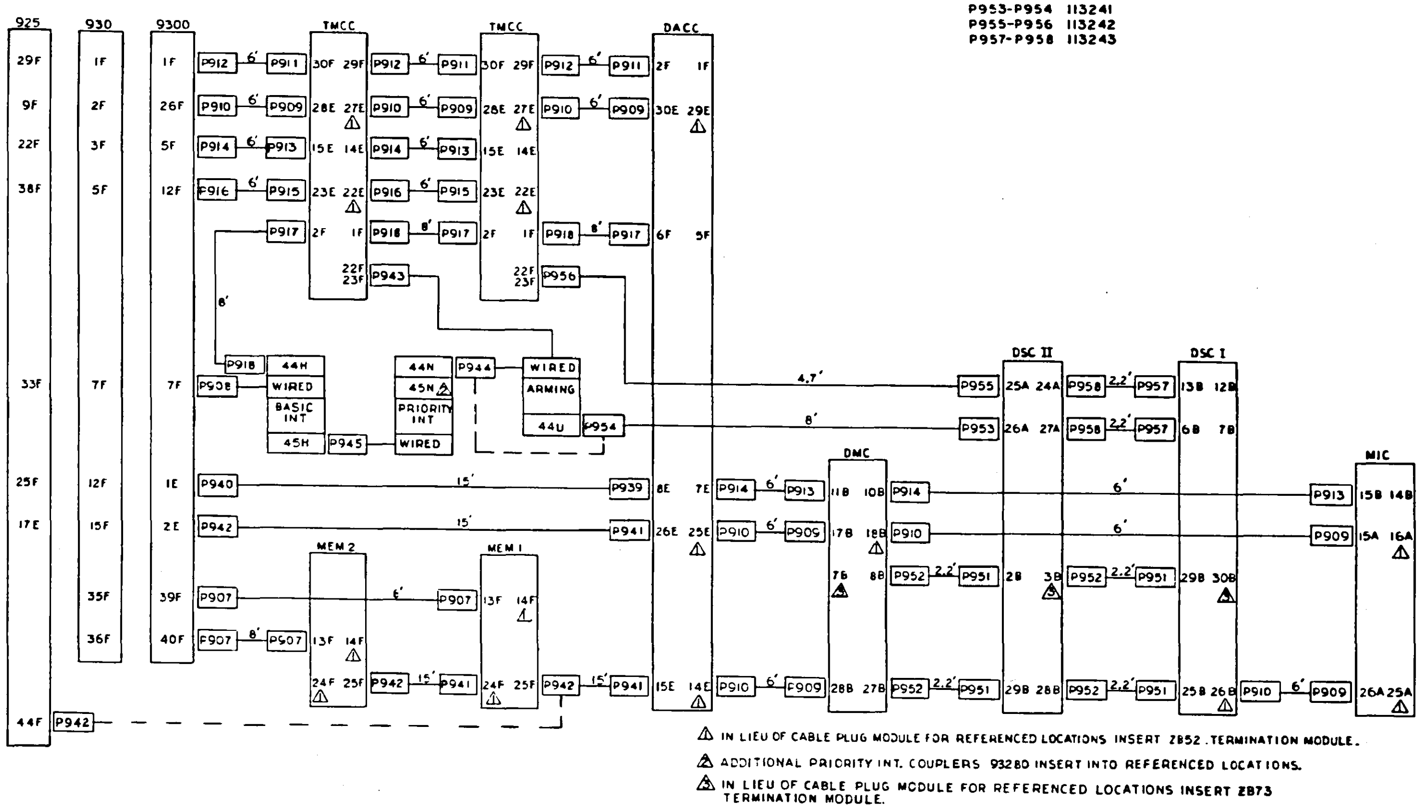
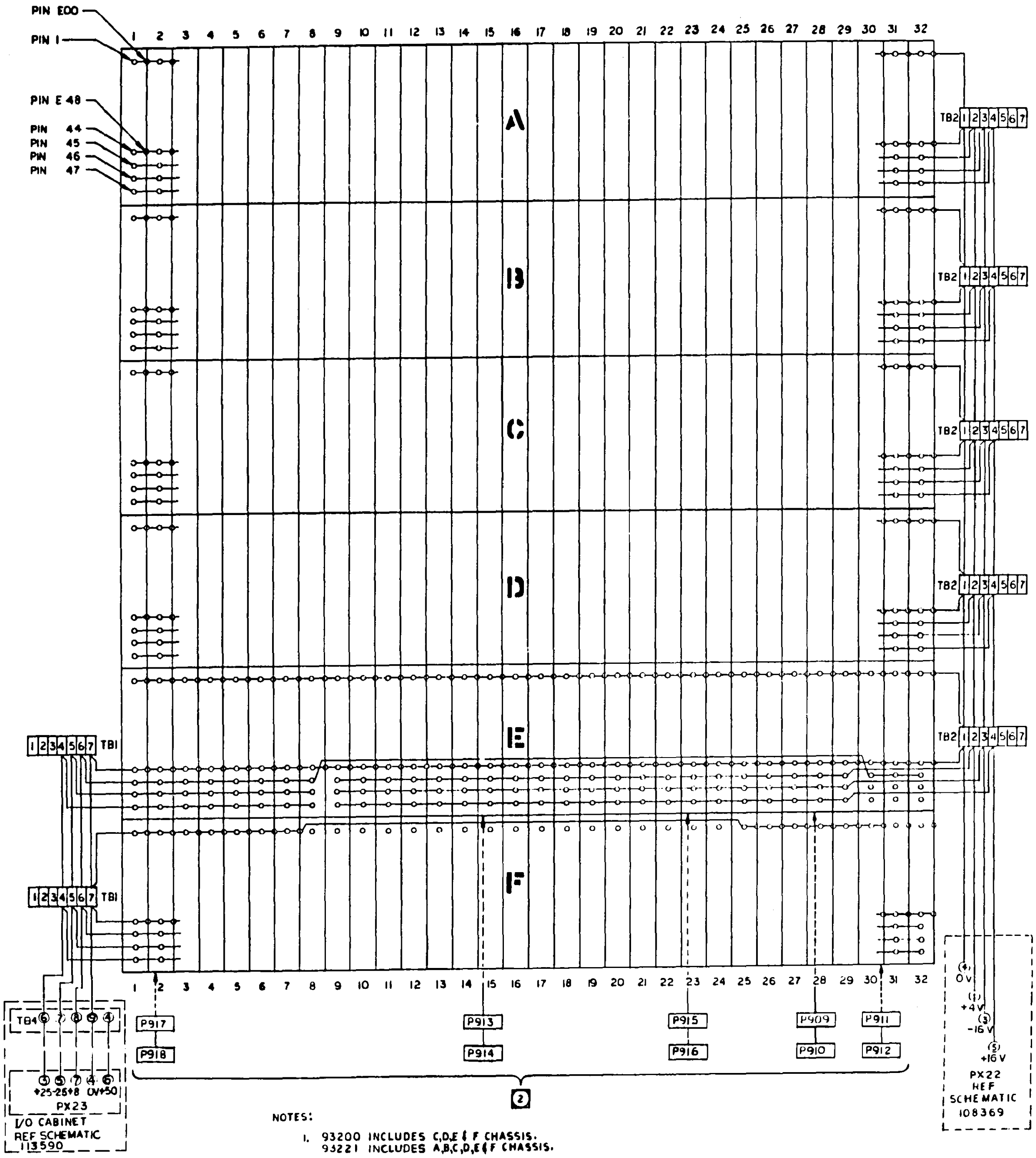


Figure 4-2. Model 93221 TMCC, Intercabling Diagram



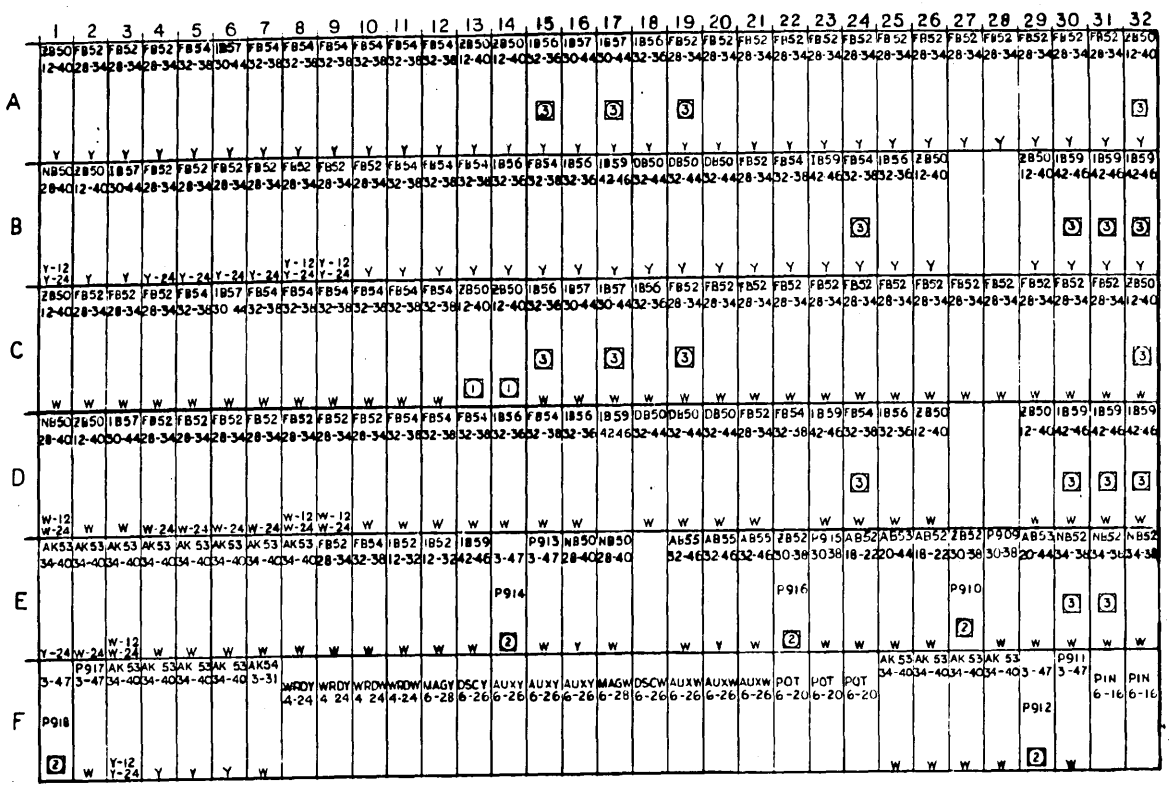
NOTES:

1. 93200 INCLUDES C,D,E & F CHASSIS.
   93221 INCLUDES A,B,C,D,E & F CHASSIS.

2. FOR INSTALLATION OF CABLE PLUGS IN ASSOCIATED COMPUTER SEE PAGES 9 & 10.

3. REF CABLE PLUG SCHEMATICS:
   107201 (P909-P910)(P915-P916)
   107300 (P913-P914)
   107303 (P911-P912)(P917-P918)

Figure 4-3. Power Distribution Diagram



NOTE:

1 - W = Modules Required For 6 Bit W Buffer
2 - W12 = Modules Added To Convert 6 Bit W Buffer To 12 Bit W Buffer.
3 - W24 = Modules Added To Convert 6 Bit W Buffer To 24 Bit W Buffer.
4 - Y = Modules Required For 6 Bit Y Buffer Requires All W Modules
5 - Y12 = Modules Added To Convert 6 Bit Y Buffer To 12 Bit Y Buffer.
6 - Y24 = Modules Added To Convert 6 Bit Y Buffer To 24 Bit Y Buffer.

1 These Modules Deleted When Y-TMCC Buffer Used With W-TMCC Buffer

2 Add P910, P912, P914, P916, P918 when C and D Buffers are Added.

3 These Modules Used Only With The Interlace Option.

4 Use ZB 52, Where Indicated, When C and D Buffers are Not added.

Figure 4-4. Module Location Diagram

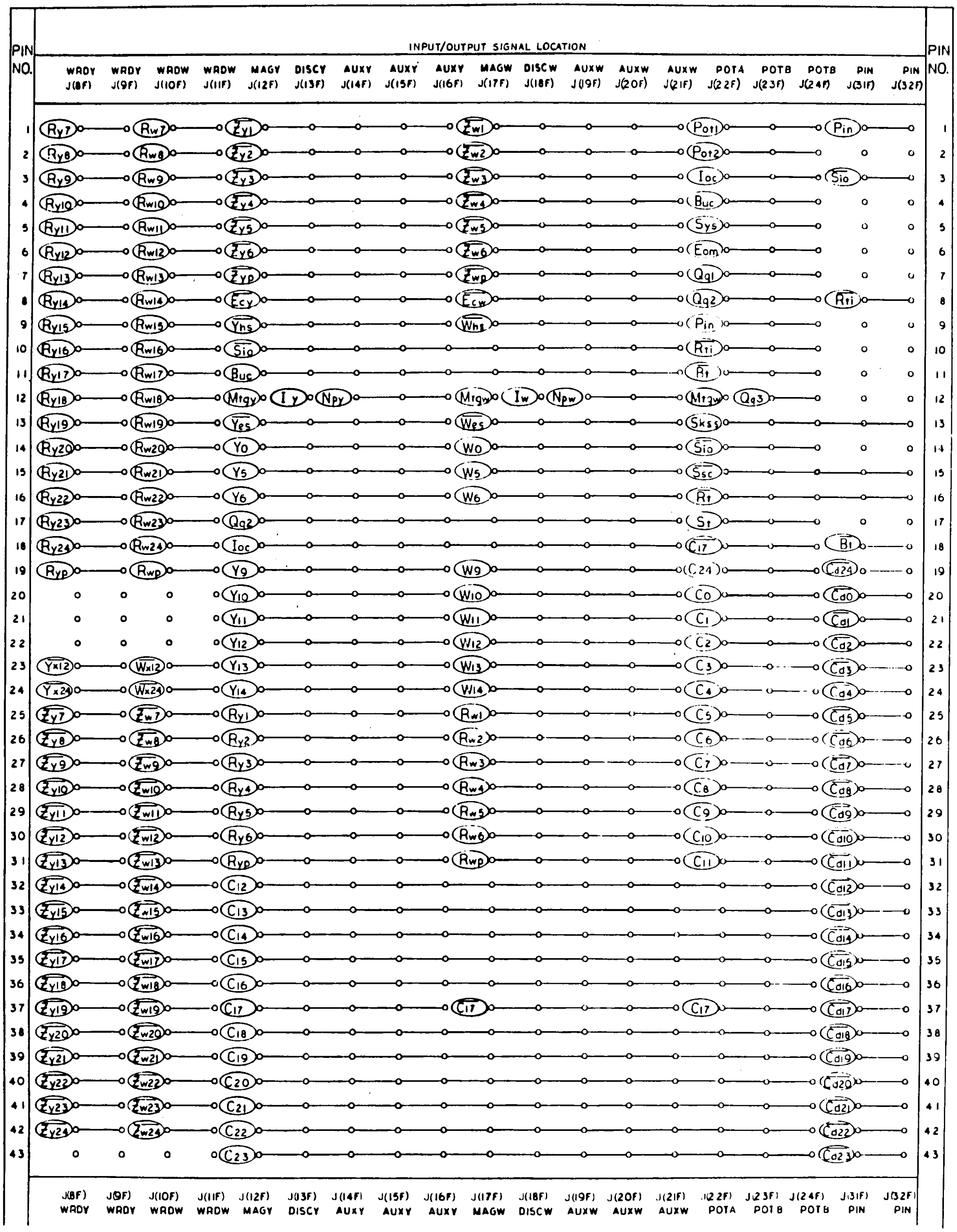


Figure 4-5. Input/Output Signal Location Diagram

Table 4-1. 925/930 Computers, W Channel Sample Test Program

Location	Instruction	Address	Comments
1000	PZE		This instruction is an assembler instruction, used as a convenient way to reserve the entry location for subroutine use.
	CLR		Clears the A and B Registers.
	STA	SWICH	Clears the location called SWICH. SWICH later indicates to the main program that output is complete.
	TYP	*0, 1, 4	Connects Typewriter Number One to channel W for output, specifies four characters per word mode, and alerts channel W interlace. The instruction is an EOM with octal configuration, 0 02 40641.
	EXU	WRITE	Causes the Input/Output EOM in location WRITE to be executed.
	POT	WRITE + 1	Sends the word count and starting address in WRITE + 1 to the channel.
	BRR	1000	Branches back to the main program.
WRITE	EOM 00403720	16200	Specifies output function code 00 and the End-of-Record interrupt. The word in WRITE + 1 specifies that eight words will output from memory beginning in location 2000. According to output function 00, when the word count equals zero during the transmission, the output terminates, and when the last character is out, the device disconnects and the interrupt occurs.
33	BRM	OKAY	Branches and marks to location OKAY elsewhere in memory.
OKAY	PZE		Saves the entry location
	MIN	SWICH	Increments location SWICH as an indicator for the main program.
	BRU	*OKAY	Branches to the main program and clears the active interrupt.

Table 4-2. 9300 Computer, A Channel Sample Test Program

Location	Instruction	Address	Comments
01000	PZE		This instruction is an assembler instruction used as a convenient way to reserve the entry location for subroutine use.
	STZ	SWICH	Clears the location called SWICH. SWICH is later used to indicate to the main program that output is complete.
	TYP	*0, 1, 4	Connects Typewriter Number One to channel A for output, specifies four characters per word mode, and alerts channel A interlace. The instruction is an EOM with octal configuration, 0 02 42641.
	EXU	WRITE	Causes the Input/Output Control EOM in location WRITE to be executed.
	POT	WRITE + 1	Sends the word count and starting address in WRITE + 1 to the channel.
	BRR	01000	Branches back to the main program.
WRITE	EOM 00403720	016200	Specifies output function code 01 (IOSD) and the End-of-Record interrupt. The word in WRITE + 1 specifies that eight words will be output from memory beginning in location 03720. According to output function 01 (IOSD) when the word count equals zero during the transmission, the device is disconnected when the last character is out and the interrupt then occurs.
011	BRM	OKAY	Branches and marks to location OKAY elsewhere in memory.
OKAY	PZE		Saves the entry location.
	MPO	SWICH	Increments location SWICH as an indicator for the main program.
	BRC	*OKAY	Branches to the main program and clears the active interrupt, level 011.

4.23 The logic terms for signals generated in the main frame referred to in these paragraphs represent the 930 computer logic equations. Although the 925 and 9300 computer implementation may differ somewhat from the 930 computer, the functions achieved are similar.

4.24 Qq1, Qq2, and Qq3 (See figure 4-6)

4.25 Qq1, Qq2, and Qq3 are clocking signals provided to external devices. They are functionally similar to the Q1 and Q2 signals provided to external equipment on the 910 and 920 computers. Signals Qq1, Qq2, and Qq3 are derived from the Pulse Counter, Qr1 through Qr4, in the TMCC.

$$Qq1 = Ts - T0$$

$$T5 - T0 = Qr3\ \overline{Qr1}\ \overline{Qr4}$$

$$Qq2 = T6 - T3$$

$$T6 - T3 = Qr3\ Qr4 + Qr3\ \overline{Qr2}\ \overline{Qr1}$$

$$Qq3 = T7 - T4$$

$$T7 - T4 = Qr4$$

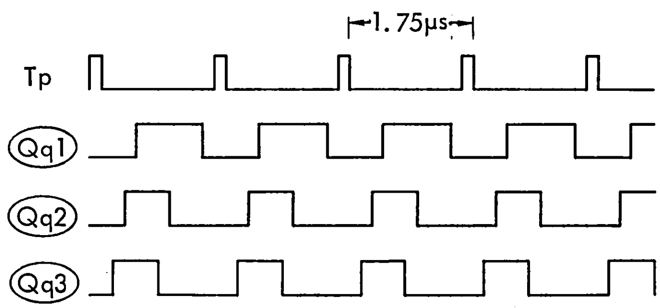


Figure 4-6. 930/9300 Timing Diagram, Qq1, Qq2, Qq3

4.26 Eom, Buc, Ioc, Sys (See figure 4-7)

4.27 Eom is the execution signal for the EOM instruction.

$$Eom = Eom\ \overline{Er}$$

The term $\overline{Er}$ inhibits Eom during the interlace loading sequence. Eom is derived from the CPU and transmitted to the TMCC. Eom is true from T7 through Tr.

$$Eom = Q5\ \overline{01}\ \overline{04}\ 05\ \overline{Ts}\ (Q2 + Q5) + \ldots$$

$$Q2 + Q5 = T7 - Tr$$

During FILL operations, a pseudo Eom is generated.

$$Eom = Ix\ \overline{Go}\ \overline{Ht}\ Kg\ (A2 + Q5) + \ldots$$

The term $\overline{Ts}$ inhibits Eom during all time share operations.

4.28 Buc is a control signal derived from the EOM instruction and is used to activate the TMCC and peripheral devices. Buc is true from T7 through Tr.

$$Buc = Eom\ \overline{C10}\ \overline{C11}\ \overline{C1}$$

For TMCC channels C and D,

$$Buc = Eom\ \overline{C10}\ \overline{C11}\ C1$$

Peripheral devices must use $\overline{C17}$ and C17 to distinguish between channels W and Y and similarly, between channels C and D.

4.29 Ioc is an input/output control signal derived from the EOM instruction. Ioc is true from T6 through T0.

$$Ioc = Eom\ \overline{C10}\ C11\ \overline{C1}\ \overline{Er}\ Qr3$$

$$Qr3 = T6 - T0$$

For channels C and D,

$$Ioc = Eom\ \overline{C10}\ C11\ C1\ \overline{Er}\ Qr3$$

The term $\overline{Er}$ is used to inhibit Ioc during the interlace loading sequence. Peripheral devices must use $\overline{C17}$ and C17 to distinguish between channels W and Y, or similarly, between channels C and D.

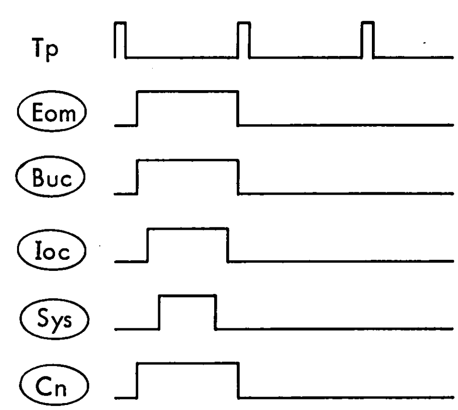


Figure 4-7. 930/9300 Timing Diagram, Eom, Buc, Ioc, Sys

4.30 (Sys) is a control signal for systems communication derived from an EOM instruction. (Sys) is true from T5 through T1.

$$(\text{Sys}) = \text{Eom C10 C11 } \overline{\text{C9}}\ \overline{\text{Tsr}}\ (\text{T5 - T1})$$

Systems devices must use $\overline{\text{C17}}$ and C17 to distinguish between channels W and Y, or similarly, between channels C and D. The term $\overline{\text{Tsr}}$ inhibits Sys during time-share operations with the TMCC.

4.31 (Pin), ($\overline{\text{Rt}}$), ($\overline{\text{Cdn}}$), ($\overline{\text{Rti}}$)

(See figures 4-8, 4-9, and 4-10)

4.32 The PIN instruction permits direct parallel entry of up to 24-bits of data to memory via the C register. A "Ready for Input" signal, (Pin), is provided by the TMCC to external equipment.

$$(\text{Pin}) = \text{Pin}$$

$$\text{Pin} = \overline{\text{F1}}\ \text{F2}\ \overline{\text{F3}}\ \text{02 06}\ \overline{\text{Ts}}\ \text{Q1}$$

$$\text{Q1} = \text{T7 - T0}$$

While the Pin signal is true, the C register is first reset and then the external data, ($\overline{\text{Cdn}}$), is strobed.

$$\text{rCn} = \text{Cxi Q2}$$

$$\text{Cxi} = \overline{\text{F1}}\ \text{F2}\ \overline{\text{F3}}\ \text{02 06}\ \overline{\text{Ts}}\ \text{Q1}$$

$$\text{Q2} = \text{T7 - T3}$$

$$\text{sCn} = \text{Cxi Cdn}$$

$$\text{Cdn} = (\overline{\text{Cdn}})$$

The process of resetting the C register and then strobing the data repeats until the external device provides a "Ready" indication by making ($\overline{\text{Rt}}$) false. The data lines, ($\overline{\text{Cdn}}$), must be in a stable condition prior to the time ($\overline{\text{Rt}}$) goes false and should remain stable for the duration of the (Pin) signal. Until ($\overline{\text{Rt}}$) goes false, the PIN instruction was locked in phase Ø2, but is now permitted to proceed to phase Ø4. A "PIN Complete" signal, ($\overline{\text{Rti}}$), is generated and sent to the external device.

$$\text{sRf} = \text{06 F2 } \overline{\text{F3}}\ \text{Q2 Rt} + \ldots$$

$$\text{Rt} = (\overline{\text{Rt}})$$

$$\text{sF1} = \overline{\text{F1}}\ \overline{\text{F3}}\ \overline{\text{01}}\ \text{03}\ \overline{\text{04}}\ \overline{\text{Ia}}\ \text{Rf Tp} + \ldots$$

$$\text{rF2} = \overline{\text{F1}}\ \overline{\text{F3}}\ \overline{\text{01}}\ \text{03}\ \overline{\text{04}}\ \overline{\text{Ia}}\ \text{Rf Tp} + \ldots$$

$$\text{Rti} = \overline{\text{Ø4}\ \overline{\text{01}}\ \overline{\text{04}}\ \text{06}\ \overline{\text{Ts}}\ (\text{Q2 + Q5})}$$

$$(\text{Q2 + Q5}) = \text{T7 - Tr}$$

$$(\overline{\text{Rti}}) = \overline{\text{Rti}}$$

If ($\overline{\text{Rt}}$) is always held false during the PIN instruction, the PIN instruction remains in phase Ø2 for only one cycle.

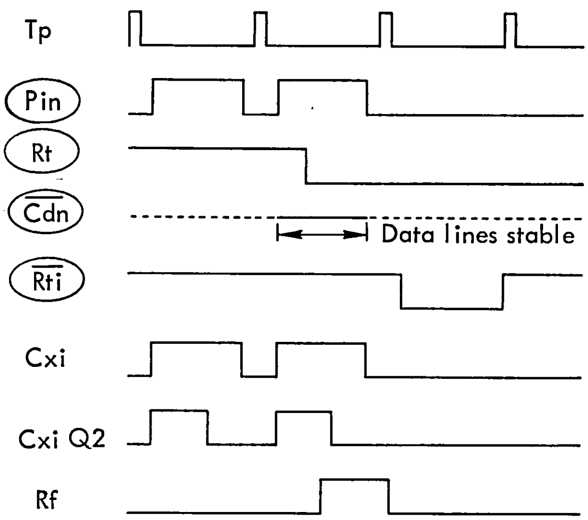


Figure 4-8. 930/9300 Timing Diagram, (Pin), ($\overline{\text{Rt}}$), ($\overline{\text{Cdn}}$), ($\overline{\text{Rti}}$)

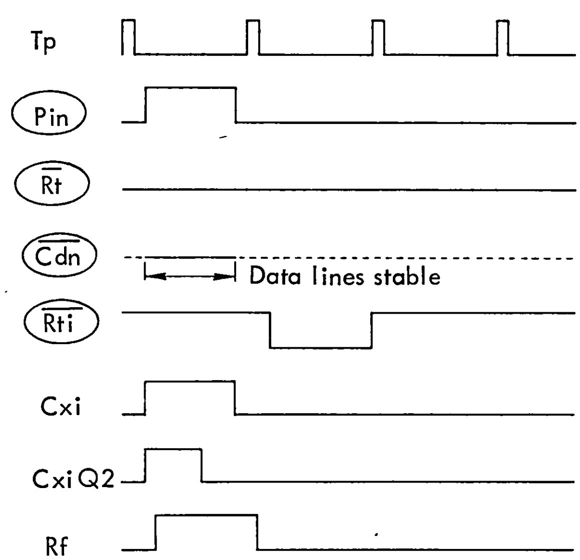


Figure 4-9. 930/9300 Timing Diagram, (Pin), ($\overline{\text{Rt}}$), ($\overline{\text{Cdn}}$), ($\overline{\text{Rti}}$), ($\overline{\text{Rt}}$) Initially False

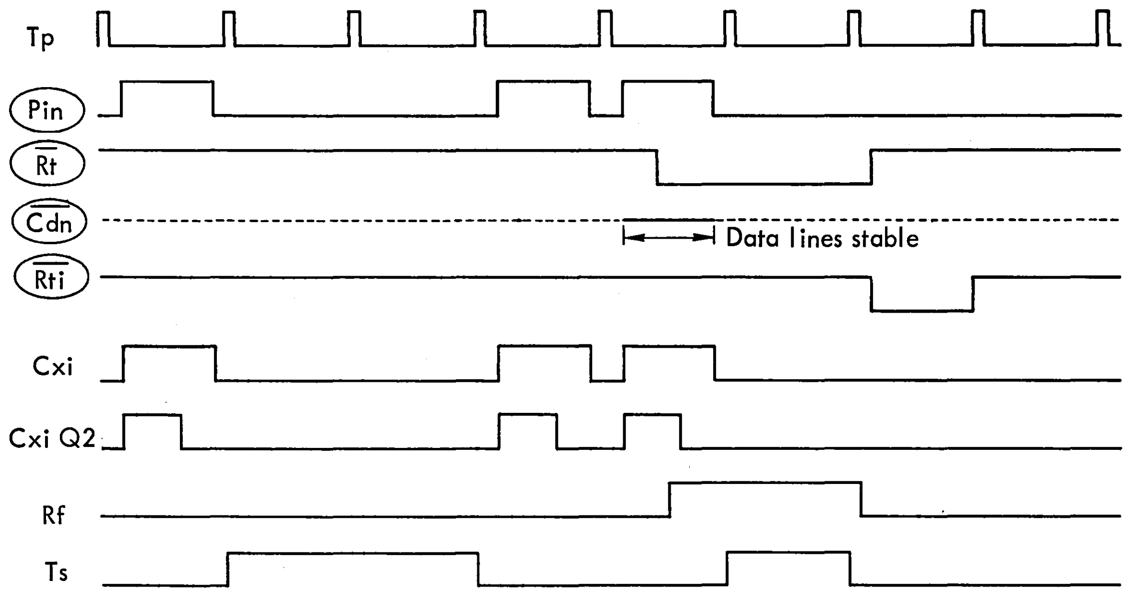


Figure 4-10. 930/9300 Timing Diagram, Pin, $\overline{Rt}$, $\overline{Cdn}$, $\overline{Rti}$, Effects of Time-Share

4.33 Should a time-share operation occur during phase Ø2 of the PIN instruction, the Pin signal is inhibited. At the completion of the time-share operation, depending on the condition of $\overline{Rt}$, at least one more cycle of the Pin signal occurs. Should a time-share operation occur during phase Ø4, the "Pin Complete" signal is inhibited until the time-share operation(s) is/are completed.

4.34 Pot 1, Pot 2, Rt, Cn

(See figures 4-11, 4-12, and 4-13)

4.35 The POT instruction permits direct parallel output of up to 24-bits of data to external devices from memory via the C register. The Pot 1 signal denotes to external devices that the computer is in the process of executing a POT instruction.

Pot 1 = Pot 1

Pot 1 = $\overline{F1}$ F2 $\overline{F3}$ $\overline{02}$ 06

The Pot 2 signal denotes to external devices that the contents of the C register may be strobed.

Pot 2 = Pot 1 (T5 - T1) $\overline{Tsr}$

The Pot 1 signal stays true and the Pot 2 signal repeats as long as the computer is locked in phase Ø2.

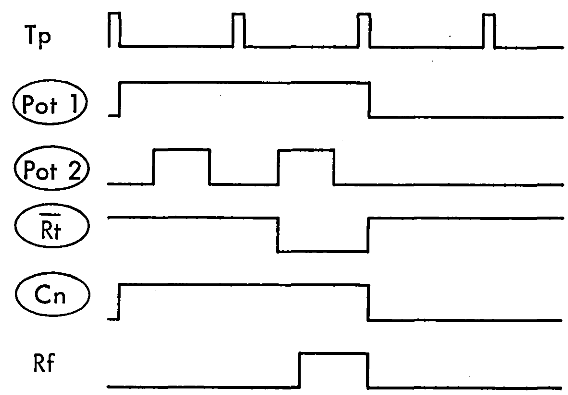


Figure 4-11. 930/9300 Timing Diagram, Pot 1, Pot 2, Rt, Cn

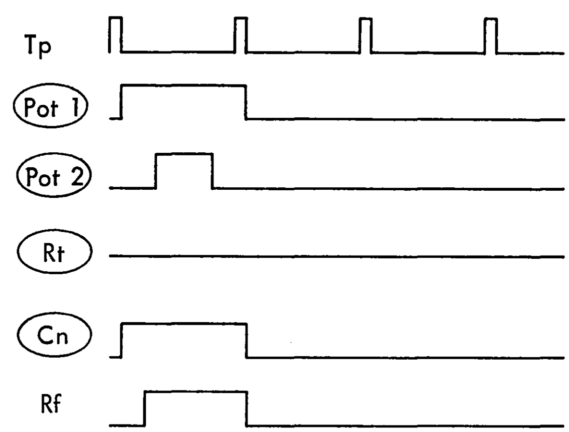


Figure 4-12. 930/9300 Timing Diagram, Pot 1, Pot 2, $\overline{Rt}$, Cn, Rt Initially False

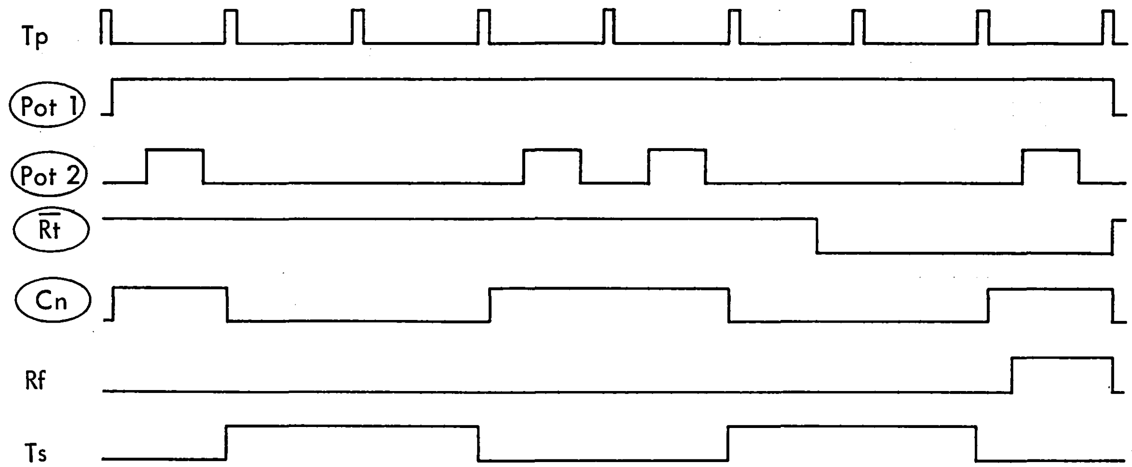


Figure 4-13. 930/9300 Timing Diagram, (Pot 1), (Pot 2), ($\overline{Rt}$), (Cn) Effects of Time-Share

When the Ready signal, ($\overline{Rt}$), from the external device goes false (low), the POT instruction proceeds to phase Ø6. (Pot 1) and (Pot 2) are then inhibited.

$$sRf = 06\ F2\ \overline{F3}\ Q2\ Rt$$

$$Rt = (Rt)$$

$$sF1 = \overline{F1}\ \overline{F3}\ \overline{01}\ 03\ \overline{04}\ \overline{Ia}\ Tp\ Rf$$

If ($\overline{Rt}$) is always held false during the POT instruction, the POT instruction remains in phase Ø2 for only one cycle.

4.36 Should a time-share operation occur during the phase Ø2, the (Pot 1) signal remains true but (Pot 2) is inhibited. At the completion of the time-share operation, depending on the condition of (Rt), at least one more cycle of (Pot 1) and (Pot 2) occurs. It is necessary that ($\overline{Rt}$) be held at ground until the computer acknowledges receipt of the Ready signal by making (Pot 1) go false.

4.37 (Skss), ($\overline{Ssc}$) (See figure 4-14)

4.38 On instructions for external system devices, an Sks strobe pulse, (Skss), is provided from the TMCC.

$$(Skss) = Skss$$

$$Skss = Ø5\ 01\ \overline{04}\ \overline{Ts}\ (\overline{A00}\ (Q3 + Q5) + \overline{C9})$$

$$Q3 + Q5 = T6 - Tr$$

The SKS instruction remains in phase Ø5 for two cycles to permit the C register outputs, (Cn), to attain a stable configuration at the external system device. The signal (Skss) is generated during the second cycle if C9 is true. (Skss) is true for approximately two cycles if $\overline{C9}$ is true. The response from external system devices, ($\overline{Ssc}$), (false for a skip condition) is received by the TMCC and is sent to the computer as Skrz. If a skip is to occur, the Sk flip-flop is set at Tr time during the second cycle of phase Ø5.

$$sSk = Ø5\ 01\ \overline{04}\ \overline{A00}\ Tr\ Sks + \ldots$$

$$Sks = Skrz + \ldots$$

If a time-share operation occurs during the SKS instruction, phase Ø5 is repeated for two cycles, thereby permitting the C register outputs, (Cn), to attain a stable configuration prior to the generation of the (Skss) probe pulse.

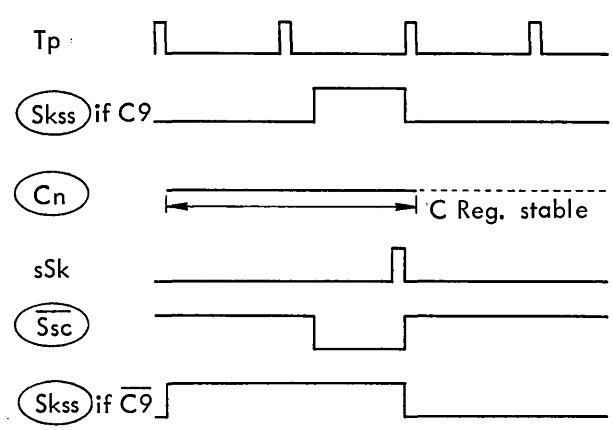


Figure 4-14. 930/9300 Timing Diagram, (Skss), (Cn), ($\overline{Ssc}$)

4.39 If $\overline{C9}$ is true, the (Skss) signal may occur for only one cycle if a time-share operation occurs during the SKS instruction. At the completion of the time-share, however, a two cycle (Skss) signal occurs. If C9 is true and time-share operation occurs, the (Skss) signal occurs only once, during the last of the two phase Ø5 cycles.

4.40 TEST PROGRAMS

4.41 Proper operation of the TMCC can be checked by performance of the applicable test program. Operation in the compatible mode of the TMCC can be checked by performing the test program for the input/output device connected to the TMCC. The sample test programs given in tables 4-1 and 4-2 may be performed. Test programs for the extended modes are given in the following paragraphs.

4.42 EXTENDED MODE I/O TEST PROGRAM FOR 925/930 COMPUTERS

4.43 This program tests as many of the extended I/O operations as possible with paper tape. Any 925/930 computer with a typewriter attached to the W channel and a paper-tape punch and reader on any interlaced communication channel may be utilized. The W channel need not be interlaced for the typewriter.

4.44 The program occupies 838_{10} locations from 0177 to 1714 octal. It is supplied on paper tape with a self-loading bootstrap. To load, insert tape in tape reader and perform fill procedure.

4.45 Fill

4.46 The fill procedure is as follows:

a. Set up selected input device with the input program. Initial portion of the program contains the "bootstrap" program.

b. Set RUN-IDLE-STEP switch to the IDLE position.

c. Press START switch.

d. Press PAPER TAPE FILL switch. This causes a WIM 2 (03200002) instruction to be inserted into the instruction register and loads the Index Register with 77777771. The FILL switch also prepares the channel to operate in the forward, binary, four characters per word mode.

4.47 Operation

4.48 To select the reader and punch units to be used enter:

"CU" P to select punch

"CU" R to select reader

The letter C is the channel number and may be any digit 0-7, and the letter U is the unit, either one or two. The reader and punch need not be on the same channel.

4.49 The test is started by entering the letter "S". Control of the test operation is then a function of the Breakpoint Switches. Table 4-3 summarizes the switch functions.

Table 4-3. 925/930 Computers Breakpoint Switch Functions

Breakpoint Switch	Reset	Set
1	Run in the normal mode as determined by the other switches	Stop and return to keyboard control at the end of the current pass (punch or read)
2	Continue to run test selected by switch 3	Cycle test runs from punch to read to punch and so on
3*	Selects punch mode	Selects read mode
4	Stop and type diagnostic messages whenever an error occurs	Do not stop and type on errors but continue to run.

*Used when switch 2 is reset or when starting test

4.50 When running cyclic tests from puch to read, the tape from the punch should be inserted into the reader.

4.51 Punching

4.52 The program punches four blocks of 64 characters each in one pass. The characters form a counting sequence from 00 to 77_8. The first block is started with leader and output with an IOSP. All punching is done in the one character per word mode. When the word count reaches zero, an IOSD is loaded to punch a second block of 64 characters. No leader is punched between the first and second blocks. This results in one physical block 128 characters long. Starting with leader, two additional blocks of 64 characters are then punched with an IOSD.

4.53 At the conclusion of each output operation, the channel address register is stored and compared with the expected value. If they do not agree, the program types the expected and actual values.

4.54 The program tests the channel during the output operation to see if the channel should erroneously disconnect before the word count reaches zero.

4.55 Reading

4.56 Each of the four blocks is read with a different set of commands and counts so as to test as many operations as possible. After reading a block, a general subroutine checks for input parity errors, channel end address for agreement with the expected address, and the data read character by character. Error messages with block numbers are typed in the event of any one of these tests failing. If a test fails, reference should then be made to the test program flow diagram and troubleshooting information in Section 5 of this manual. The handling of each block is as follows:

a. Block 1. The first block is one-half of a 128 character physical block. Reading one character per word, an IOSD with a count of 64 is used to read this block. The program checks to see if the count reaches zero and the channel becomes inactive at the same time.

b. Block 2. This is the second half of the first physical block and is read with an IOSP with a count of 65. The read should terminate because of the end of record. The program checks to see that the word count does not reach zero and the channel remains active after the CIT (inter-record test) instruction skips. The tape is finally stopped with a disconnect before the data is checked.

c. Block 3. Block 3 is a 64-character physical block. It is read with two channel commands. The first is an IOSP with a count of 32. If the count goes to zero before the channel disconnects, an IORP with a count of 33 is loaded. This should cause the inter-record indicator to be turned on at the end of the record. The count should not reach zero and the channel should remain active. The tape is again stopped with a disconnect before the data is checked.

d. Block 4. This is the third physical block of 64-characters and is read with an IORD with a count of 56. The program waits for the channel to be inactive then checks to see if the channel ignored the last eight characters. If the tape was erroneously stopped after the 56th character it will show up as a failure on the first block of the next read pass.

4.57 Test Program

4.58 Table 4-4 gives the test program for the 925/930 computers I/O extended mode.

4.59 EXTENDED MODE I/O TEST PROGRAM FOR 9300 COMPUTER

4.60 This program tests as many of the extended I/O operations as possible with paper tape. Any 9300 computer with a typewriter attached to the W channel and a paper-tape punch and reader on any interlaced communication channel may be utilized. The W channel need not be interlaced for the typewriter.

4.61 The program occupies 838_{10} locations from 0177 to 1714_8. It is supplied on paper tape with a self-loading bootstrap. To load, insert tape in tape reader and perform fill procedure.

4.62 Fill

4.63 The fill procedure is as follows:

a. Press POWER switch on. When power is on, the switch is lighted.

b. Press IDLE switch.

c. With computer in IDLE, press RESET switch. This clears the D register and the program counter.

d. Press RUN switch. The computer now executes the instruction in the D register (which is a HALT instruction). The program counter advances to 00001.

e. Press PAPER TAPE LOAD switch. This switch causes an AIM 2 (0 32 00002) instruction to be inserted into the D register and clears the HALT instruction. Index 1 is loaded with 001 77771. The LOAD switch also prepares the channel to operate in the forward, binary, four character per word mode.

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 1 of 20)

```
00001642   TYPE    EQU      930                    MACHINE DEFINITION: 930/925
           *
           *
           *    EXTENDED MODE I/O TEST PROGRAM. (925/930/9300 ALL CHANNELS)
           *
           *    A.W. ENGLAND, SDS
           *
           *
           *        THIS PROGRAM USES THE PAPER TAPE READER AND PUNCH TO CHECK THE
           *    OPERATION OF THE I/O CHANNELS IN THE EXTENDED INTERLACE MODE OF
           *    OPERATION.  THE READER AND PUNCH MAY BE CONNECTED TO ANY INTERLACED
           *    TMCC OR DACC.  THEY NEED NOT BE ATTACHED TO THE SAME CHANNEL.  THE
           *    PROGRAM ADDRESSES THE KEYBOARD FOR INFORMATION ABOUT UNIT AND CHANNEL
           *    SELECTION.
           *
           *        TO SELECT PUNCH TYPE:  'CU'P
           *
           *        TO SELECT READER TYPE: 'CU'R
           *
           *        WHERE 'C' REPRESENTS CHANNEL NO. AND MAY HAVE THE VALUES 0-7;
           *    AND 'U' REPRESENTS UNIT NO. AND MAY HAVE THE VALUE 1-2.  THE LETTER
           *    P OR R CAUSE THE SELECTION TO BE MADE WITH THE TWO PREVIOUS DIGITS.
           *    SPACES SHOULD NOT BE TYPED BETWEEN DIGITS OR CONTROL CHARACTER.
           *
           *        TO START THE TEST TYPE:  S
                    PAGE
           *
           *
           *        BREAKPOINTS OR SENSE SWITCHES CONTROL THE RUNNING OF THE PROGRAM:
           *
           *       SWITCH          RESET                          SET
           *       ------          -----                          -----
           *
           *        BP 1    RUN IN THE NORMAL MODE    STOP AT THE END OF THE CURRENT
           *        SW 1    AS DETERMINED BY THE      PASS AND RETURN TO KEY BOARD
           *                OTHER SWITCHES.           CONTROL
           *
           *
           *        BP 2    CONTINUE TO RUN THE       CYCLE TEST RUNS FROM READ TO
           *        SW 2    TEST MODE SELECTED BY     PUNCH TO READ, ETC.
           *                SWITCH 3.
           *
           *
           *        BP 3    SELECTS PUNCH MODE        SELECTS READ MODE.
           *        SW 3    (USED WHEN SWITCH 2 IS RESET OR WHEN STARTING THE TEST)
           *
           *
           *        BP 4    STOP AND TYPE DIAGNOSTIC  DO NOT STOP OR TYPE ON ERRORS.
```

```
*       SW 4    MESSAGES WHENEVER AN      CONTINUE RUNNING REGARDLESS.
*               ERROR OCCURS.
*
*
* NOTE: TO RUN CONTINOUS FROM READ TO PUNCH THE OUTPUT OF THE PUNCH
*       SHOULD BE FED INTO THE READER.  A LOOP SHOULD BE USED TO RUN
*       CONTINOUS ON THE READER.
        PAGE
*
*  THE FOLLOWING SECTION OF CODE DEFINES EITHER A 925/930 INSTRUCTION
*  SET OR A 9300 INSTRUCTION SET. THIS IS DONE ON THE BASIS OF THE
*  MACHINE TYPE STATEMENT AT THE BEGINNING OF THE DECK.
*
*
*
*
        PROC
DF9300  NAME
$INST   FORM    3,6,15
P       PROC    1                         DEFINE INDEX OP'S TO IMPLY X1.
$LDX    NAME    017
$STX    NAME    077
$BRX    NAME    057
        INST    (P(*1)*/2)++1,P(0),P(1)
        END
P       PROC    1
$XAB    NAME    037733                    DEFINE COMPATIBLE REGISTER OP'S
$ABC    NAME    037731
$BAC    NAME    037713
$CLR    NAME    037711
        INST    0,040,P(0)
        END
P       PROC    1
$RSH    NAME    000                       DEFINE COMPATIBLE SHIFTS
$RCY    NAME    002
$LSH    NAME    004
$LCY    NAME    006
$NOD    NAME    044
$SHFT   FORM    3,6,6,9
        SHFT    P(2),060,P(0),P(1)**0777
        END
P       PROC    1                         DEFINE MISC. COMPATIBLE OP'S.
$MIN    NAME    071
$MIB    NAME    030
$BIM    NAME    032
        INST    (P(*1)*/2)++P(2),P(0),P(1)
        END
*
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 3 of 20)

```
$X       EQU      1                     DEFINE INDEX TAG'X' FOR X1
*                                       EOD CONSTANT
         AORG     0177
$EODC    DATA     04000000              EOD CONSTANT
*
$SWTFRM      FORM  3,6,3,12
Q        PROC     1
$BPT     NAME     040000
$OVT     NAME     014040
$ROV     NAME     04000
$SOV     NAME     00040
         SWTFRM   0,022,Q(0)*/(-12)**7,Q(0)**07777++(Q(1)>0)*/(6-Q(1))
         END
         END
*
         PROC
DF930    NAME
*
* IF NOT A 9300 THEN DO THE FOLLOWING OPERATIONS
*
P        PROC     1                     DEFINE I/O INSTRUCTIONS
$MIB     NAME     012
$BIM     NAME     032
INST     FORM     3,6,1,14
         INST     P(2),P(0),P(*1),P(1)
         END
*
$X       EQU      2                     DEFINE INDEX TAG 'X' FOR 2 ON 930
*
*
         AORG     0177
$EODC    DATA     0400000               EOD CONSTANT
*
*
N        PROC     1                     SET OVERFLOW
$SOV     NAME
         BRR      $,4
         END
*
M        PROC     1                     BRANCH AND CLEAR INTERRUPT
$BRC     NAME
         DO       M(*1),1,2
         BRU      M(1)
         BRU      *$+1
         PZE      M(1)
         END
P        PROC     1
$DSC     NAME     0
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 4 of 20)

```
                         $ALC    NAME    050000
                         $ASC    NAME    012000
                         $TØP    NAME    014000
                         I       FØRM    3,6,15
                                 I       P(1)**2,(P(1)**4)*/3++2,P(0)++(P(1)**1)*/6
                                 END
                         P       PRØC    1
                         $CAT    NAME    014000
                         $CET    NAME    011000
                         $CIT    NAME    010400
                         $CZT    NAME    012000
                         I       FØRM    3,6,15
                                 I       P(1)**2,040,P(0)++(P(1)**4)*/12++(P(1)**1)*/6
                                 END
                                 END
                                 DØ      TYPE=9300
                                 DF9300
                                 DØ      TYPE<9300
00177   00400000                 DF930
                                 PAGE
                         *
                         *   THE START ØF THE PRØGRAM
                         *
00200                            AØRG    0200
00200   0 76 0 00233     BEGIN   LDA     BRUGØ         INITIALIZE RECØVERY LØCATIØNS
00201   0 35 0 00001             STA     1
00202   0 35 0 00032             STA     032
00203   0 01 0 00204     BRUGØ   BRU     KYBD
00204   0 23 0 01241     KYBD    EXU     RDIS
00205   0 23 0 01231             EXU     PDIS
00206   0 46 30003       GØ2     CLR
00207   0 35 0 01444             STA     T1
00210   0 02 0 02031             RKB     0,1,1
00211   0 32 0 01445     GØ1     BIM     T1+1          READ CHARACTER
00212   0 76 0 01445             LDA     T1+1
00213   0 75 0 01636             LDB     =077
00214   0 70 0 01637             SKM     ='  P'       CHECK FØR CØNTRØL CHAR.
00215   0 01 0 00217             BRU     $+2
00216   0 01 0 00233             BRU     PO
00217   0 70 0 01640             SKM     ='  R'
00220   0 01 0 00222             BRU     $+2
00221   0 01 0 00256             BRU     RO
00222   0 70 0 01641             SKM     ='  S'
00223   0 01 0 00225             BRU     $+2
00224   0 43 0 00317             BRM     SO
00225   0 72 0 01642             SKA     =070         CHECK FØR DIGIT
00226   0 01 0 00206             BRU     GØ2           IF NØT CØNTRØL ØR DIGIT CLEAR
00227   0 75 0 01444             LDB     T1
```

```
00230  0 36 0 01446    193          STB      T1+2                     SAVE CHANNEL NUMBER IN T1+2
00231  0 35 0 01444    194          STA      T1                       SAVE UNIT NUMBER IN T1
00232  0 01 0 00211    195          BRU      G01
                       196          PAGE
                       197 *
                       198 *    PUNCH CHANNEL SET UP ROUTINE
                       199 *
00233  0 43 0 00323    200 PO       BRM      MAKECH                   GET CHANNEL NO. BUILT. SAVED IN T1+2
00234  0 71 0 01643    201          LDX      =-4**0177777             UPDATE EOM/EOD'S
00235  2 76 0 01234    202          LDA      PALC+1,X
00236  0 14 0 01644    203          ETR      =050277677
00237  0 16 0 01446    204          MRG      T1+2                     INSERT CHANNEL DESIGNATION
00240  0 35 1 00235    205          STA      *$-3
00241  0 41 0 00235    206          BRX      $-4
00242  0 71 0 01645    207          LDX      =-3**0177777             UPDATE SKS'S
00243  2 76 0 01227    208          LDA      PCET+1,X
00244  0 14 0 01646    209          ETR      =057737677
00245  0 16 0 01447    210          MRG      T1+3
00246  0 35 1 00243    211          STA      *$-3
00247  0 41 0 00243    212          BRX      $-4
00250  0 71 0 01643    213          LDX      =-4**0177777             UPDATE CHANNEL COMMANDS
00251  2 76 0 01212    214          LDA      PIOSD+2,X
00252  0 14 0 01647    215          ETR      =050277777
00253  0 16 0 01450    216          MRG      T1+4
00254  0 35 1 00251    217          STA      *$-3
00255  0 41 0 00256    218          BRX      $+1
00256  0 41 0 00251    219          BRX      $-5
00257  0 76 0 01230    220          LDA      PTL                      UPDATE UNIT NO.
00260  0 14 0 01650    221          ETR      =-2
00261  0 16 0 01444    222          MRG      T1
00262  0 35 0 01230    223          STA      PTL
00263  0 16 0 01651    224          MRG      =02000                   MAKE NO L. DER EOM
00264  0 35 0 01227    225          STA      PPT
00265  0 01 0 00234    226          BRU      KYBD
                       227 *
                       228 *    READER CHANNEL SET UP ROUTINE
                       229 *
                       230 *
00266  0 43 0 00323    231 RO       BRM      MAKECH                   GET CHANNEL NO BUILT
00267  0 71 0 01643    232          LDX      =-4**0177777             UPDATE EOM/EOD'S
00270  2 76 0 01244    233          LDA      RALC+1,X
00271  0 14 0 01644    234          ETR      =050277677
00272  0 16 0 01446    235          MRG      T1+2
00273  0 35 1 00270    236          STA      *$-3
00274  0 41 0 00270    237          BRX      $-4
00275  0 71 0 01643    238          LDX      =-4**0177777             BUILD SKS'S
00276  2 76 0 01240    239          LDA      RCIT+1,X
00277  0 14 0 01646    240          ETR      =057737677
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 6 of 20)

```
00300   0 16 0 01447           MRG    T1+3
00301   0 35 1 00276           STA    *$-3
00302   0 41 0 00276           BRX    $-4
00303   0 71 0 01652           LDX    =-10**0177777      BUILD CHANNEL COMMAND EOM/EOD'S
00304   2 76 0 01224           LDA    RIORD+2,X
00305   0 14 0 01653           ETR    =070277777
00306   0 16 0 01450           MRG    T1+4
00307   0 35 1 00304           STA    *$-3
00310   0 41 0 00311           BRX    $+1
00311   0 41 0 00304           BRX    $-5
00312   0 76 0 01240           LDA    RPT                  BUILD RPT WITH UNIT NO.
00313   0 14 0 01650           ETR    =-2
00314   0 16 0 01444           MRG    T1
00315   0 35 0 01240           STA    RPT
00316   0 01 0 00204           BRU    KYBD
                         *
                         *
                         *  START TEST RUNNING
                         *
00317   0 02 00000       SO    DSC    0                    DISCONNECT
00320   0 40 20100             BPT    3                    START READ OR PUNCH?
00321   0 01 0 00640           BRU    IN                   READ
00322   0 01 0 00356           BRU    OUT                  PUNCH
                               PAGE
                         *
                         *  BUILD CHANNEL NO. SUBROUTINE
                         *
00323   0 00 0 00000     MAKECH PZE
00324   0 46 30003             CLR
00325   0 76 0 01446           LDA    T1+2                 GET CH. NO.
00326   0 72 0 01654           SKA    =4                  EOD REQUIRED
00327   0 75 0 00177           LDB    EODC                 YES
00330   0 36 0 01450           STB    T1+4                 NO, SAVE EOD BIT.
00331   0 14 0 01655           ETR    =3
00332   0 35 0 01446           STA    T1+2
00333   0 71 0 01446           LDX    T1+2
00334   0 76 0 01450           LDA    T1+4
00335   2 16 0 00352           MRG    MAKETB,X             BUILD EOM/EOD SELECTION
00336   0 35 0 01446           STA    T1+2                 SAVE EOM
00337   0 46 10012             BAC                         BUILD SKS SELECTION
00340   0 72 0 00177           SKA    EODC
00341   0 75 0 01656           LDB    =040000
00342   0 46 00014             XAB
00343   2 16 0 00352           MRG    MAKETB,X
00344   0 35 0 01447           STA    T1+3                 SAVE SKS
00345   0 76 0 01444           LDA    T1                   BUILD UNIT NO. BIT
00346   0 14 0 01657           ETR    =1
00347   0 17 0 01657           EOR    =1
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 7 of 20)

```
00350  0 35 0 01444    289        STA    T1               SAVE UNIT NO. BIT
00351  0 51 0 00323    290        BRR    MAKECH           EXIT
                       291 *
00352  00000000        292 MAKETB DATA   0,0100,020000000,020000100
00353  00000100
00354  20000000
00355  20000100
                       293        PAGE
                       294 *
                       295 *  PAPER TAPE PUNCH OUTPUT SECTION.
                       296 *
00356  0 71 0 01650    297 OUT    LDX    =-64**0177777    SET UP OUTPUT IMAGE WITH 64 WORDS
00357  0 46 30003      298        CLR
00360  2 35 0 01344    299        STA    IMAGE+64,X
00361  0 55 0 01651    300        ADD    =01000000
00362  0 41 0 00360    301        BRX    $-2
00363  0 23 0 01230    302 OUT4   EXU    PTL              START PUNCH WITH LEADER
00364  0 23 0 01233    303        EXU    PALC             ALERT CHANNEL
00365  0 23 0 01236    304        LCH    PIOSP            LOAD IOSP IMAGE,64
00366  0 13 0 01237
00367  0 71 0 01643    305        LDX    =-4**0177777     SET UP FOR SUBROUTINE TO TYPE:
00370  0 75 0 01652    306        LDB    =ERMSG1           IOSP, OUTPUT
00371  0 76 0 00431    307        LDA    PCATC
00372  0 43 0 00610    308        BRM    WCZ              WAIT FOR CHANNEL COUNT = ZERO
00373  0 23 0 01226    309        EXU    PCET             ERROR ON OUTPUT
00374  0 40 20040      310        BPT    4                YES, CHECK BP4 FOR NO STOP
00375  0 01 0 00416    311        BRU    OUT4A            NO, NO STOP ON ERROR
00376  0 23 0 01231    312 OUT2   EXU    PDIS             ERROR, DISCONNECT CHANNEL
00377  0 02 0 02641    313        TYP    0,1,4            TYPE GENERAL ERROR MESSAGE
00400  0 12 0 01653    314        MIB    =052121225       I  E
00401  0 12 0 01654    315        MIB    =051514651       RROR
00402  0 12 0 01655    316        MIB    =012246451        OUR
00403  0 12 0 01656    317        MIB    =031452712       ING
00404  0 46 00014      318        XAB                     TYPE SPECIFIC ERROR MESSAGE
00405  0 16 0 01635    319        MRG    MIBX
00406  0 35 0 00407    320        STA    $+1
00407  0 12 0 00000    321        MIB    00               TO BE REPLACED AT RUN TIME
00410  0 61 0 00407    322        MIN    $-1
00411  0 41 0 00407    323        BRX    $-2
00412  0 02 14000      324 GOTOP  TOP    0
00413  0 40 14000      325        CAT    0
00414  0 01 0 00413    326        BRU    $-1
00415  0 01 0 00204    327        BRU    KYBD
                       328 *
00416  0 43 0 00476    329 OUT4A  BRM    OUTPIN           GO PIN AND CHECK CHANNEL ADDRESS
00417  0 23 0 01224    330        EXU    PCAT             IF CHANNEL INACTIVE READDRESS PUNCH
00420  0 01 0 00422    331        BRU    $+2
00421  0 23 0 01227    332        EXU    PPT
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 8 of 20)

```
00422  0 23 0 01233          EXU   PALC
00423  0 23 0 01210          LCH   PIØSD            LØAD CH. IØSD IMAGE,64
00424  0 13 0 01211
00425  0 71 0 01643    ØUT1  LDX   =-4**0177777    SET UP ERRØR MESSAGE:
00426  0 75 0 01657          LDB   =ERMSG2          IØSD, ØUTPUT
00427  0 76 0 00431          LDA   PCATC
00430  0 43 0 00610          BRM   WCZ              WAIT FØR CØUNT EQUAL ZERØ
00431  0 23 0 01224    PCATC EXU   PCAT             CHAN. ACTIVE?
00432  0 01 0 00431          BRU   $-1              YES
00433  0 23 0 01226          EXU   PCET             NØ, ERRØR?
00434  0 40 20040            BPT   4                YES, IS STØP ALLØWED?
00435  0 01 0 00437          BRU   $+2              NØ ERRØR ØR NØ STØP
00436  0 01 0 00376          BRU   ØUT2             ERRØR STØP ALLØWED
00437  0 43 0 00476          BRM   ØUTPIN           GØ PIN AND CHECK CHANNEL ADDRESS
00440  0 46 30003            CLR
00441  0 35 0 01452          STA   PRF              R(PUNCH REPEAT)
00442  0 23 0 01230    ØUT1A EXU   PTL
00443  0 23 0 01233          EXU   PALC
00444  0 23 0 01210          LCH   PIØSD            LØAD IØSD  IMAGE,64
00445  0 13 0 01211
00446  0 71 0 01643          LDX   =-4**0177777    SET UP ERRØR MESSAGE:
00447  0 75 0 01657          LDB   =ERMSG2
00450  0 76 0 00431          LDA   PCATC
00451  0 43 0 00610          BRM   WCZ
00452  0 23 0 01224          EXU   PCAT             CHAN. ACTIVE?
00453  0 01 0 00452          BRU   $-1              YES
00454  0 23 0 01226          EXU   PCET             NØ, CHAN. ERRØR
00455  0 40 20040            BPT   4                YES, IS ERRØR STØP ALLØWED
00456  0 01 0 00450          BRU   $+2              NØ,NØ
00457  0 01 0 00376          BRU   ØUT2             YES
00460  0 43 0 00476          BRM   ØUTPIN           GØ PIN AND CHECK CHANNEL ADDRESS
00461  0 53 0 01452          SKN   PRF              PUNCH REPEAT
00462  0 01 0 00454          BRU   $+2              RESET
00463  0 01 0 00457          BRU   ØUT3             SET
00464  0 76 0 01670          LDA   =-1             S(PUNCH REPEAT)
00465  0 35 0 01452          STA   PRF
00466  0 01 0 00442          BRU   ØUT1A
                       *
                       *
00467  0 40 20400      ØUT3  BPT   1                GØ ØR STØP
00470  0 01 0 00234          BRU   KYBD             STØP
00471  0 40 20200            BPT   2                GØ, CYCLE?
00472  0 01 0 00640          BRU   IN               YES
00473  0 40 20100            BPT   3                ØNE ØNLY
00474  0 01 0 00640          BRU   IN
00475  0 01 0 00356          BRU   ØUT
                       *
                       *  SUBRØUTINE TØ CHECK CHANNEL ADDRESS
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 9 of 20)

```
                        *
00476  0 00 0 00000     OUTPIN PZE    0
00477  0 23 0 01232            EXU    PASC                ALERT TO STORE PUNCH CHANNEL
00500  0 33 0 01444            PIN    T1                  STORE ADDRESS
00501  0 76 0 01444            LDA    T1
00502  0 17 0 01671            EOR    =IMAGE+64           COMPARE WITH EXPECTED
00503  0 72 0 01670            SKA    =-1
00504  0 40 20040              BPT    4                   NOT EQUAL
00505  0 51 0 00476            BRR    OUTPIN              EQUAL OR ERROR STOP NOT PERMITTED
00506  0 37 0 01445            STX    T1+1                SAVE LENGTH OF ERROR MESSAGE
00507  0 46 00014              XAB                        SET UP ERROR OUTPUTTER
00510  0 16 0 01635            MRG    MIBX
00511  0 35 0 00530            STA    OTPIN1
00512  0 76 0 01671            LDA    =IMAGE+64           GENERATE EXPECTED PIN WORD IN BCD
00513  0 43 0 00537            BRM    MKOCT
00514  0 35 0 00577            STA    OTPNM1              SAVE EXPECTED
00515  0 36 0 00600            STB    OTPNM1+1
00516  0 76 0 01444            LDA    T1                  GENERATE ACTUAL PIN WORD IN BCD
00517  0 43 0 00537            BRM    MKOCT
00520  0 35 0 00605            STA    OTPNM2
00521  0 36 0 00606            STB    OTPNM2+1
00522  0 23 0 01231            EXU    PDIS                DISCONNECT PUNCH CHANNEL
00523  0 71 0 01672            LDX    =-15**0177777
00524  0 02 0 02641            TYP    0,1,4
00525  2 12 0 00574            MIB    OTPNM+15,X          OUTPUT MESSAGE
00526  0 41 0 00525            BRX    $-1
00527  0 71 0 01445            LDX    T1+1                OUTPUT SPECIAL MESSAGE
00530  0 12 0 00000     OTPIN1 MIB    00
00531  0 61 0 00530            MIN    $-1
00532  0 41 0 00530            BRX    $-2
00533  0 71 0 01673     OTPIN2 LDX    =-12**0177777       OUTPUT RECEIVED AND EXPECTED MESSAGE
00534  2 12 0 00610            MIB    OTPNM2+3,X
00535  0 41 0 00534            BRX    $-1
00536  0 01 0 00412            BRU    GOTOP
                        *
                        *
                        *  SUBROUTINE TO MAKE ONE WORD INTO 8 BCD OCTAL DIGITS
                        *
00537  0 00 0 00000     MKOCT  PZE    0
00540  0 71 0 01674            LDX    =-8**0177777
00541  0 46 20005              ABC                        0 TO WORD TO B
00542  0 6700 003              LSH    3                   SHIFT OUT OCTAL DIGIT
00543  2 35 0 01456            STA    T1+10,X             SAVE BCD CHARACTER
00544  0 76 0 01675            LDA    =0                  CLEAR A
00545  0 41 0 00542            BRX    $-3
00546  0 46 30003              CLR
00547  0 71 0 01674            LDX    =-8**0177777        REASSEMBLY BCD CHARACTERS INTO A + B.
00550  0 6720 006              LCY    6
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 10 of 20)

```
00551  2 16 0 01456        MRG    T1+10,X
00552  0 41 0 00550        BRX    $-2
00553  0 46 00014          XAB
00554  0 51 0 00537        BRR    MK8CT                EXIT
                       *
                       *
                       *  ERROR MESSAGES FOR CHANNEL ADDRESS TEST SUBROUTINE
                       *
00555  52254524        0TPNM  BCD    52,1END ADDRESS FROM CHANNEL DID NOT AGREE WITH EXPECTE
00556  12212424
00557  51256262
00560  12265146
00561  44122330
00562  21454525
00563  43122431
00564  24124546
00565  63122127
00566  51252512
00567  66316330
00570  12256747
00571  25236325
00572  24122126               BCD    8,D AFTER
00573  63255112
00574  25674725               BCD    12,EXPECTED
00575  23632524
00576  12121212
00577  00000000        0TPNM1 DATA   0,0
00600  00000000
00601  73121252               BCD    16,,  1RECEIVED
00602  51252325
00603  31652524
00604  12121212
00605  00000000        0TPNM2 DATA   0,0
00606  00000000
00607  33125252               BCD    4,. 11
                              PAGE
                       *
                       *  WAIT FOR COUNT EQUAL ZERO SUBROUTINE.
                       *
00610  0 00 0 00000    WCZ    PZE                         ENTRY
00611  0 35 0 00617           STA    $+6                  SAVE R/PCAT
00612  0 55 0 01657           ADD    =1                   MAKE A CZT
00613  0 35 0 00614           STA    $+1                  SAVE R/PCZT
00614  0 40 12000             CZT    00                   C = 0?
00615  0 01 0 00617           BRU    $+2                  NO
00616  0 51 0 00610           BRR    WCZ                  YES
00617  0 40 14000             CAT    00                   CHANNEL ACTIVE?
00620  0 01 0 00614           BRU    $-4                  YES
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 11 of 20)

```
00621  0 40 20040             BPT    4                   NO, INHIBIT ERRORS
00622  0 51 0 00610           BRR    WCZ                 YES
00623  0 37 0 01444           STX    T1                  NO, PRINT ERROR MESSAGE
00624  0 46 00014             XAB
00625  0 16 0 01635           MRG    MIBX
00626  0 35 0 00634           STA    $+6
00627  0 71 0 01676           LDX    =-13**0177777
00630  0 02 0 02641           TYP    0,1,4
00631  2 12 0 01530           MIB    DISMSG+13,X
00632  0 41 0 00631           BRX    $-1
00633  0 71 0 01444           LDX    T1
00634  0 12 0 00030           MIB    00
00635  0 61 0 00634           MIN    $-1
00636  0 41 0 00634           BRX    $-2
00637  0 01 0 00412           BRU    GOTOP
                              PAGE
                       *
                       *  INPUT SECTION
                       *
00640  0 43 0 01177    IN     BRM    STARTP              START READER
00641  0 02 20001             ROV
00642  0 23 0 01243           EXU    RALC                ALERT
00643  0 23 0 01212           LCH    RIOSD               LOAD IOSD  BUFFER,64
00644  0 13 0 01213
00645  0 23 0 01235    INOB   EXU    RCZT                C=0
00646  0 01 0 00657           BRU    INO                 NO
00647  0 23 0 01234    RCATC  EXU    RCAT                YES, CHAN. ACTIVE
00650  0 40 20040             BPT    4                   YES, ERROR STOP PERMITTED
00651  0 01 0 00670           BRU    INOA                NO, NO CONT.
00652  0 71 0 01676           LDX    =-13**0177777       YES
00653  0 02 0 02641           TYP    0,1,4
00654  2 12 0 01525           MIB    ERMSG4+13,X
00655  0 41 0 00654           BRX    $-1
00656  0 01 0 00412           BRU    GOTOP
                       *
00657  0 23 0 01234    INO    EXU    RCAT                CHAN. ACTIVE STILL?
00660  0 01 0 00645           BRU    INOB                YES
00661  0 23 0 01235           EXU    RCZT                NO, C=0
00662  0 01 0 00654           BRU    $+2                 NO
00663  0 01 0 00670           BRU    INOA                YES
00664  0 71 0 01645           LDX    =-3**0177777        SET UP ERROR MESSAGE
00665  0 75 0 01677           LDB    =ERMSG5
00666  0 76 0 00647           LDA    RCATC
00667  0 43 0 00610           BRM    WCZ                 GO DO DISCONNECT ERROR TEST
00670  0 76 0 01700    INOA   LDA    =033120152          BLOCK NO. 1
00671  0 75 0 01701           LDB    =BUFFER+64          END ADDRESS EXPECTED
00672  0 43 0 01055           BRM    CHECK               GO CHECK DATA
00673  0 43 0 01177    IN1    BRM    STARTP              START READER IF DATA CHECKED O.K.
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 12 of 20)

```
00674  0 02 20001           RθV
00675  0 23 0 01243         EXU    RALC
00676  0 23 0 01214         LCH    RIθSP               LθAD IθSP BUFFER,65
00677  0 13 0 01215
00700  0 76 0 01670         LDA    =-1
00701  0 35 0 01451         STA    SPF                 S(IθSP INPUT)
00702  0 23 0 01237    IN4  EXU    RCIT                INTERRECθRD CθNDITIθN
00703  0 01 0 00705         BRU    $+2                 Nθ
00704  0 01 0 00732         BRU    IN2                 YES
00705  0 23 0 01234         EXU    RCAT                CHAN. ACTIVE
00706  0 01 0 00716         BRU    IN1A                YES
00707  0 40 20040           BPT    4                   Nθ, ERRθR STθP PERMITTED
00710  0 01 0 00732         BRU    IN2                 Nθ
00711  0 71 0 01672         LDX    =-15**0177777       YES
00712  0 02 0 02641         TYP    0,1,4
00713  2 12 0 01547         MIB    ERMSG6+15,X
00714  0 41 0 00713         BRX    $-1
00715  0 01 0 00412         BRU    GθTθP
                       *
00716  0 23 0 01235    IN1A EXU    RCZT                C=0
00717  0 01 0 00702         BRU    IN4                 Nθ
00720  0 23 0 01237         EXU    RCIT                YES, CHAN. INTER-RECθRD
00721  0 01 0 00732         BRU    IN2                 Nθ
00722  0 40 20040           BPT    4                   YES, ERRθR STθP PERMITTED
00723  0 01 0 00732         BRU    IN2                 Nθ
00724  0 23 0 01241         EXU    RDIS                YES, STθP TAPE
00725  0 71 0 01702         LDX    =-17**0177777
00726  0 02 0 02641         TYP    0,1,4
00727  2 12 0 01570         MIB    ERMSG7+17,X
00730  0 41 0 00727         BRX    $-1
00731  0 01 0 00412         BRU    GθTθP
                       *
00732  0 23 0 01236    IN2  EXU    RCET                IF CHANNEL ERRθR
00733  4 51 0 00733         SθV                        SET θVERFLθW
00734  0 23 0 01241         EXU    RDIS                STθP TAPE
00735  0 53 0 01451         SKN    SPF                 IθSP INPUT FLAG
00736  0 01 0 00756         BRU    IN3                 RESET
00737  0 76 0 01703         LDA    =033120252          SET, GET BLθCK Nθ. 2
00740  0 75 0 01444         LDB    BUFFER+64           END ADDRESS EXPECTED
00741  0 43 0 01055         BRM    CHECK               CHECK DATA INPUT
                       *                               IF CθRRECT CθNTINUE.
00742  0 43 0 01177         BRM    STARTP              START TAPE
00743  0 02 20001           RθV
00744  0 23 0 01243         EXU    RALC                ALERT
00745  0 23 0 01216         LCH    RIθSP1              LθAD IθSP BUFFER,32
00746  0 13 0 01217
00747  0 71 0 01645         LDX    =-3**0177777        SET UP ERRθR MESSAGE
00750  0 75 0 01704         LDB    =ERMSG8
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 13 of 20)

```
00751  0 76 0 00647              LDA    RCATC
00752  0 43 0 00610              BRM    WCZ                GO WAIT FOR C=0
00753  0 23 0 01236              EXU    RCET               IF CHANNEL ERROR
00754  4 51 0 00754              SOV                       SET OVERFLOW
00755  0 23 0 01234              EXU    RCAT               IS READER STILL RUNNING
00756  0 01 0 00750              BRU    IN5                YES
00757  0 23 0 01240              EXU    RPT                NO, RESTART TAPE READER
00760  0 23 0 01243        IN5   EXU    RALC
00761  0 23 0 01220              LCH    RIORP              LOAD IORD BUFFER+32,33
00762  0 13 0 01221
00763  0 46 30003                CLR
00764  0 35 0 01451              STA    SPF                R(IOSP INPUT)
00765  0 01 0 00702              BRU    IN4
                           *
00766  0 76 0 01705        IN3   LDA    =033120352         BLOCK NO. 3
00767  0 75 0 01701              LDB    =BUFFER+64         END ADDRESS EXPECTED
00770  0 43 0 01055              BRM    CHECK              GO CHECK DATA
00771  0 43 0 01177              BRM    STARTP             START TAPE
00772  0 23 0 01243              EXU    RALC
00773  0 23 0 01222              LCH    RIORD              LOAD IORD BUFFER,56
00774  0 13 0 01223
00775  0 23 0 01234              EXU    RCAT               CHAN. ACTIVE
00776  0 01 0 00775              BRU    $-1                YES, WAIT FOR STOP
00777  0 71 0 01674              LDX    =-8**0177777       CHAN. INACTIVE
01000  0 76 0 01636              LDA    =077
01001  2 72 0 01444              SKA    BUFFER+64,X        CHECK FOR 0'S IN LAST 8 CHARACTERS
01002  0 01 0 01024              BRU    IN3A
01003  0 41 0 01001              BRX    $-2
01004  0 71 0 01674        IN3B  LDX    =-8**0177777       O.K. INSERT CORRECT 8 CHARACTERS
01005  0 76 0 01642              LDA    =070
01006  2 35 0 01444              STA    BUFFER+64,X
01007  0 55 0 01657              ADD    =1
01010  0 41 0 01006              BRX    $-2
01011  0 76 0 01706              LDA    =033120452         BLOCK NO. 4
01012  0 75 0 01707              LDB    =BUFFER+56         END ADDRESS EXPECTED
01013  0 02 20001                ROV
01014  0 43 0 01055              BRM    CHECK              GO CHECK DATA
01015  0 40 20400                BPT    1                  TEST STOP?
01016  0 01 0 00204              BRU    KYBD               YES
01017  0 40 20200                BPT    2                  TEST CYCLE?
01020  0 01 0 00356              BRU    OUT                YES
01021  0 40 20100                BPT    3                  TEST ONE ONLY.
01022  0 01 0 00640              BRU    IN                 READ
01023  0 01 0 00356              BRU    OUT                PUNCH
                           *
01024  0 40 20040          IN3A  BPT    4                  ERROR STOP PERMITTED
01025  0 01 0 01004              BRU    IN3B               NO
01026  0 71 0 01674              LDX    =-8**0177777       FORMAT LAST EIGHT CHARACTERS FOR TYPE
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 14 of 20)

```
01027  0 46 30003                      CLR
01030  2 76 0 01444           IN3D     LDA     BUFFER+64,X
01031  0 6700 003                      LSH     3
01032  2 16 0 01444                    MRG     BUFFER+64,X
01033  0 14 0 01710                    ETR     =0707
01034  0 16 0 01711                    MRG     =052120000
01035  0 6700 006                      LSH     6
01036  2 35 0 01055                    STA     MSGIMG+8,X
01037  0 41 0 01030                    BRX     IN3D
01040  0 71 0 01712                    LDX     =-19**0177777        OUTPUT ERROR MESSAGE
01041  0 02 0 02641                    TYP     0,1,4
01042  2 12 0 01616                    MIB     ERMSG9+19,X
01043  0 41 0 01042                    BRX     $-1
01044  0 02 14000                      TOP     0
01045  0 40 14000                      CAT     0
01046  0 01 0 01045                    BRU     $-1
01047  0 02 0 02041                    TYP     0,1,1                OUTPUT 8 CHARACTERS
01050  0 71 0 01674                    LDX     =-8**0177777
01051  2 12 0 01055                    MIB     MSGIMG+8,X
01052  0 41 0 01051                    BRX     $-1
01053  0 12 0 01533                    MIB     ERMSG1+3             CR
01054  0 01 0 00412                    BRU     GOTOP
                              *
                              *
01055                         MSGIMG   RES     8
                                       PAGE
                              *
                              *  CHECK INPUT DATA SUBROUTINE.
                              *
01065  0 00 0 00030           CHECK    PZE
01066  0 35 0 01626                    STA     ERMSG0+6             SAVE BLOCK NO.
01067  0 23 0 01236                    EXU     RCET                 CHECK FOR ERROR
01070  0 01 0 01141                    BRU     PARERR               GO TO PARITY ERROR ROUTINE
01071  0 40 20001                      OVT                          CHECK FOR PREVIOUSLY NOTED ERROR
01072  0 01 0 01141                    BRU     PARERR               GO TO PARITY ERROR ROUTINE
01073  0 23 0 01242                    EXU     RASC                 STORE CHANNEL ADDRESS
01074  0 33 0 01444                    PIN     T1
01075  0 36 0 01445                    STB     T1+1                 SAVE EXPECTED
01076  0 76 0 01444                    LDA     T1
01077  0 17 0 01445                    EOR     T1+1                 COMPARE ACTUAL WITH EXPECTED
01100  0 72 0 01670                    SKA     =-1                  AGREE
01101  0 01 0 01154                    BRU     PINERR               NO
01102  0 71 0 01650           CHECK2   LDX     =-64**0177777        YES
01103  0 76 0 01675                    LDA     =0C
01104  0 75 0 01636                    LDB     =077
01105  2 70 0 01444                    SKM     BUFFER+64,X          CHECK INPUT BUFFER
01106  0 01 0 01112                    BRU     CHECK1               ERROR
01107  0 55 0 01657                    ADD     =1
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 15 of 20)

```
01110  0 41 0 01105                 BRX     $-3
01111  0 51 0 01055                 BRR     CHECK              EXIT IF ALL CORRECT
                             *
01112  0 40 20040           CHECK1  BPT     4                  ERROR STOP PERMITTED?
01113  0 51 0 01055                 BRR     CHECK              NO. EXIT
01114  0 35 0 01444                 STA     T1                 YES
01115  0 6700 003                   LSH     3                  FORMAT EXPECTED
01116  0 16 0 01444                 MRG     T1
01117  0 14 0 01710                 ETR     =0707
01120  0 6700 006                   LSH     6
01121  0 16 0 01713                 MRG     =012000052
01122  0 35 0 01631                 STA     ERMSG0+9           STORE EXPECTED
01123  2 76 0 01444                 LDA     BUFFER+64,X        FORMAT RECEIVED
01124  0 6600 003                   RSH     3
01125  2 76 0 01444                 LDA     BUFFER+64,X
01126  0 6700 003                   LSH     3
01127  0 14 0 01710                 ETR     =0707
01130  0 6700 006                   LSH     6
01131  0 16 0 01713                 MRG     =012000052
01132  0 35 0 01634                 STA     ERMSG0+12          STORE RECEIVED
01133  0 71 0 01676                 LDX     =-13**0177777
01134  0 23 0 01241                 EXU     RDIS               DISCONNECT READER CHANNEL
01135  0 02 0 02641                 TYP     0,1,4
01136  2 12 0 01635                 MIB     ERMSG0+13,X
01137  0 41 0 01136                 BRX     $-1
01140  0 01 0 00412                 BRU     GOTOP
                             *
                             *  PARITY ERROR SUBROUTINE
                             *
01141  0 40 20040           PARERR  BPT     4                  ERROR STOP PERMITTED?
01142  0 51 0 01055                 BRR     CHECK              NO
01143  0 23 0 01241                 EXU     RDIS               YES, DISCONNECT READER CHANNEL
01144  0 02 0 02641                 TYP     0,1,4
01145  0 71 0 01714                 LDX     =-9**0177777
01146  2 12 0 01627                 MIB     ERMSGP+9,X         OUTPUT PARITY ERROR MESSAGE
01147  0 41 0 01146                 BRX     $-1
01150  0 02 14000                   TOP     0
01151  0 40 14000                   CAT     0
01152  0 01 0 01151                 BRU     $-1
01153  0 01 0 01102                 BRU     CHECK2             RETURN TO CHECK NUMBERS
                             *
                             *   PIN ADDRESS ERROR SUBROUTINE
                             *
01154  0 40 20040           PINERR  BPT     4                  ERROR STOP PERMITTED
01155  0 01 0 01102                 BRU     CHECK2             NO
01156  0 76 0 01444                 LDA     T1                 YES
01157  0 43 0 00537                 BRM     MKOCT              EXPAND ACTUAL TO BCD
01160  0 35 0 00605                 STA     OTPNM2             SAVE
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 16 of 20)

```
01161  0 36 0 00606           STB    OTPNM2+1
01162  0 76 0 01445           LDA    T1+1              EXPAND EXPECTED TO BCD
01163  0 43 0 00537           BRM    MKOCT
01164  0 35 0 00577           STA    OTPNM1            SAVE
01165  0 36 0 00600           STB    OTPNM1+1
01166  0 23 0 01241           EXU    RDIS              DISCONNECT READER
01167  0 02 0 02641           TYP    0,1,4
01170  0 71 0 01672           LDX    =-15**0177777
01171  2 12 0 00574           MIB    OTPNM+15,X        OUTPUT GENERAL MESSAGE
01172  0 41 0 01171           BRX    $-1
01173  0 12 0 01624           MIB    ERMSGO+4          OUTPUT BLOCK NO.
01174  0 12 0 01625           MIB    ERMSGO+5
01175  0 12 0 01626           MIB    ERMSGO+6
01176  0 01 0 00533           BRU    OTPIN2            GO OUTPUT RECEIVED AND EXPECTED
                       *
                       *  START TAPE READER SUBROUTINE
                       *
01177  0 00 0 00000    STARTP PZE
01200  0 71 0 01650           LDX    =-64**0177777
01201  0 46 30003             CLR
01202  2 35 0 01444           STA    BUFFER+64,X       CLEAR BUFFER
01203  0 41 0 01202           BRX    $-1
01204  0 23 0 01240           EXU    RPT               START TAPE
01205  0 51 0 01177           BRR    STARTP            EXIT
                              PAGE
                       *
                       *  I/O CHANNEL COMMANDS
                       *
01206  002 146 0 00    PIOSP  IOSP   IMAGE,64
01207  0100 01244
01210  002 142 0 00    PIOSD  IOSD   IMAGE,64
01211  0100 01244
                       *
01212  002 142 0 00    RIOSD  IOSD   BUFFER,64
01213  0100 01344
01214  002 146 0 00    RIOSP  IOSP   BUFFER,65
01215  0101 01344
01216  002 146 0 00    RIOSP1 IOSP   BUFFER,32
01217  0040 01344
01220  002 144 0 00    RIORP  IORP   BUFFER+32,33
01221  0041 01404
01222  002 140 0 00    RIORD  IORD   BUFFER,56
01223  0070 01344
                       *
                       *
                       *  I/O CHANNEL INSTRUCTIONS.
                       *
01224  0 40 14000      PCAT   CAT    0
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 17 of 20)

```
01225  0 40 12000        PCZT    CZT     0
01226  0 40 11000        PCET    CET     0
                         *
01227  0 02 0 02044      PPT     PPT     0,1,1
01230  0 02 0 00044      PTL     PTL     0,1,1
01231  0 02 00000        PDIS    DSC     0
01232  0 02 12000        PASC    ASC     0
01233  0 02 50000        PALC    ALC     0
                         *
                         *
01234  0 40 14000        RCAT    CAT     0
01235  0 40 12000        RCZT    CZT     0
01236  0 40 11000        RCET    CET     0
01237  0 40 10400        RCIT    CIT     0
                         *
01240  0 02 0 02034      RPT     RPT     0,1,1
01241  0 02 00000        RDIS    DSC     0
01242  0 02 12000        RASC    ASC     0
01243  0 02 50000        RALC    ALC     0
                         *
                         *
                         *   OUTPUT IMAGE AREA, INPUT BUFFER AREA
                         *
01244                    IMAGE   RES     64
01344                    BUFFER  RES     64
                         *
                         *
                         *   TEMPORARY STORAGE AND FLAGS
                         *
01444                    T1      RES     13
01461                    SPF     RES     1                   IOSP INPUT FLAG
01462                    PRF     RES     1                   PUNCH REPEAT FLAG
                                 PAGE
                         *
                         *   ERROR AND STATUS MESSAGES.
                         *
01463  52233021          DISMSG  BCD     52,!CHANNEL ERROROUSLY DISCONNECTED BEFORE C=0, DURING
01464  45452543
01465  12255151
01466  46514664
01467  62437012
01470  24316223
01471  46454525
01472  23632524
01473  12222526
01474  46512512
01475  23130073
01476  12246451
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 18 of 20)

```
01477   31452712
01500   31466247        768 ERMSG1 BCD      16,IOSP, OUTPUT. ↓↓
01501   73124664
01502   63476463
01503   33125252
01504   31466224        769 ERMSG2 BCD      16,IOSD, OUTPUT. ↓↓
01505   73124664
01506   63476463
01507   33125252
01510   52233021        770 ERMSG4 BCD      52,↓CHANNEL DID NOT DISCONNECT WHEN C=0 ON IOSD INPUT↓
01511   45452543
01512   12243124
01513   12454663
01514   12243162
01515   23464545
01516   25236312
01517   66302545
01520   12231300
01521   12464512
01522   31466224
01523   12314547
01524   64635212
01525   31466224        771 ERMSG5 BCD      12,IOSD, INPUT↓
01526   73123145
01527   47646352
01530   52233021        772 ERMSG6 BCD      52,↓CHANNEL DISCONNECTED DURING IOSP INPUT, CIT NEVER
01531   45452543
01532   12243162
01533   23464545
01534   25236325
01535   24122464
01536   51314527
01537   12314662
01540   47123145
01541   47646373
01542   12233163
01543   12452565
01544   25511212
01545   63516425        773        BCD      8,TRUE. ↓
01546   33125212
01547   52246451        774 ERMSG7 BCD      48,↓DURING IOSP INPUT C=0 INDICATING EOR PAST BUT C
01550   31452712
01551   31466247
01552   12314547
01553   64631223
01554   13001231
01555   45243123
01556   21633145
```

Table 4-4. 925/930 Computers, Extended Mode I/O Test Program (Sheet 19 of 20)


```
01557  27122546
01560  51124721
01561  62631222
01562  64631223
01563  31631266      775          BCD      20.IT WAS NEVER TRUE. !
01564  21621245
01565  25652551
01566  12635164
01567  25331252
01570  31466247      776 ERMSG8   BCD      12.!0SP. INPUT!
01571  73123145
01572  47646352
01573  52314651      777 ERMSG9   BCD      52.!!0RD 0N INPUT DID N0T IGN0RE THE LAST 8 CHARACTERS.
01574  24124645
01575  12314547
01576  64631224
01577  31241245
01600  46631231
01601  27454651
01602  25126330
01603  25124321
01604  62631210
01605  12233021
01606  51212363
01607  25516273
01610  12226463      778          BCD      24. BUT READ THE F0LL0WING!
01611  12512521
01612  24126330
01613  25122646
01614  43434666
01615  31452752
01616  52524721      779 ERMSGP   BCD      8.!!PARITY
01617  51316370
01620  52314547      780 ERMSG0   BCD      40.!INPUT ERR0R IN BL0CK N0. N!EXPECTED DD!
01621  64631225
01622  51514651
01623  12314512
01624  22434623
01625  42124546
01626  33124552
01627  25674725
01630  23632524
01631  12242452
01632  51252325      781          BCD      12.RECEIVED DD!
01633  31652524
01634  12242452
                     782 *
01635  0 12 0 00030  783 MIBX     MIB      0                   0UTPUT INSTRUCTI0N
```

```
                        784 *
                        785 *
         00000200       786          END      BEGIN
01636    00000077
01637    00606047
01640    00606051
01641    00606062
01642    00000070
01643    00177774
01644    50277677
01645    00177775
01646    57737677
01647    50277777
01650    77777776
01651    00002000
01652    00177766
01653    70277777
01654    00000004
01655    00000003
01656    00040000
01657    00000001
01660    00177700
01661    01000000
01662    00001500
01663    52121225
01664    51514651
01665    12246451
01666    31452712
01667    00001504
01670    77777777
01671    00001344
01672    00177761
01673    00177764
01674    00177770
01675    00000000
01676    00177763
01677    00001525
01700    33120152
01701    00001444
01702    00177757
01703    33120252
01704    00001570
01705    33120352
01706    33120452
01707    00001434
01710    00000707
01711    52120000
01712    00177755
01713    12000052
01714    00177767
```

4.64 Operation

4.65 To select the reader and punch units to be used enter:

"CU" P to select punch,

"CU" R to select reader.

The letter C is the channel number and may be any digit 0-7 and the letter U is the unit, either one or two. The reader and punch need not be on the same channel.

4.66 The test is started by entering the letter "S". Control of the test operation is then a function of the Breakpoint Switches. Table 4-5 summarizes the switch functions.

4.67 When running cyclic tests from punch to read, the tape from the punch should be inserted into the reader.

4.68 Punching

4.69 The program punches four blocks of 64 characters each in one pass. The characters form a counting sequence from 00 to 77_8. The first block is started with leader and output with an IOSP. All punching is done in the one character per word mode. When the word count reaches zero, an IOSD is loaded to punch a second block of 64 characters. No leader is punched between the first and second blocks. This results in one physical block 128 characters long. Starting with leader, two additional blocks of 64 characters are then punched with an IOSD.

4.70 At the conclusion of each output operation, the channel address register is stored and compared with the expected value. If they do not agree, the program types the expected and actual values.

4.71 The program tests the channel during the output operation to see if the channel should erroneously disconnect before the word count reaches zero.

4.72 Reading

4.73 Each of the four blocks is read with a different set of commands and counts so as to test as many operations as possible. After reading a block, a general subroutine checks for input parity errors, for channel end address agreement with the expected address, and the data read character by character. Error messages with block numbers are typed in the event of any one of these tests failing. In the event of a test failing, reference should then be made to the test program flow diagram and troubleshooting information contained in Section 5 of this manual. The handling of each block is as follows:

a. Block 1. The first block is one-half of a 128 character physical block. Reading one character per word, an IOSD with a count of 64 is used to read this block. The program checks to see if the count reaches zero and the channel becomes inactive at the same time.

b. Block 2. This is the second half of the first physical block and is read with an IOSP with a count of 65. The read should terminate because of the end of record. The program checks to see that the word count does not reach zero and the channel remains active after the CIT (inter-record test) instruction skips. The tape is

Table 4-5. 9300 Computer Breakpoint Switch Functions

Breakpoint Switch	Reset	Set
1	Run in the normal mode as determined by the other switches	Stop and return to keyboard control at the end of the current pass (punch or read)
2	Continue to run test selected by switch 3	Cycle test runs from punch to read to punch and so on
3*	Selects punch mode	Selects to punch and so on
4	Stop and type diagnostic messages whenever an error occurs	Do not stop and type on errors but continue to run

*Used when switch 2 is reset or when starting test finally stopped with a disconnect before the data is checked.

c. Block 3. Block 3 is a 64 character physical block. It is read with two channel commands. The first is an IOSP with a count of 32. If the count goes to zero before the channel disconnects, an IORP with a count of 33 is loaded. This should cause the inter-record indicator to be turned on at the end of the record. The count should not reach zero and the channel should remain active. The tape is again stopped with a disconnect before the data is checked.

d. Block 4. This is the third physical block of 64 characters and is read with an IORD with a count of 56. The program waits for the channel to be inactive then checks to see if the channel ignored the last eight characters. If the tape was erroneously stopped after the 56th character, it will show up as a failure on the first block of the next read pass.

4.74 Test Program

4.75 Table 4-6 gives the test program for the 9300 computer I/O extended mode.

Table 4-6. 9300 Computer, Extended Mode I/O Test Program (Sheet 1 of 20)

```
00022124     TYPE    EQU     9300                   MACHINE DEFINITION: 9300
             *
             *
             *   EXTENDED MODE I/O TEST PROGRAM. (925/930/9300 ALL CHANNELS)
             *
             *   A.W. ENGLAND, SDS
             *
             *
             *       THIS PROGRAM USES THE PAPER TAPE READER AND PUNCH TO CHECK THE
             *   OPERATION OF THE I/O CHANNELS IN THE EXTENDED INTERLACE MODE OF
             *   OPERATION.  THE READER AND PUNCH MAY BE CONNECTED TO ANY INTERLACED
             *   TMCC OR DACC.  THEY NEED NOT BE ATTACHED TO THE SAME CHANNEL.  THE
             *   PROGRAM ADDRESSES THE KEYBOARD FOR INFORMATION ABOUT UNIT AND CHANNEL
             *   SELECTION.
             *
             *       TO SELECT PUNCH TYPE:  'CU'P
             *
             *       TO SELECT READER TYPE: 'CU'R
             *
             *       WHERE 'C' REPRESENTS CHANNEL NO. AND MAY HAVE THE VALUES 0-7;
             *   AND 'U' REPRESENTS UNIT NO. AND MAY HAVE THE VALUE 1-2.  THE LETTER
             *   P OR R CAUSE THE SELECTION TO BE MADE WITH THE TWO PREVIOUS DIGITS.
             *   SPACES SHOULD NOT BE TYPED BETWEEN DIGITS OR CONTROL CHARACTER.
             *
             *       TO START THE TEST TYPE:  S
                     PAGE
             *
             *
             *       BREAKPOINTS OR SENSE SWITCHES CONTROL THE RUNNING OF THE PROGRAM:
             *
             *      SWITCH          RESET                           SET
             *      ------          -----                          -----
             *
             *       BP 1    RUN IN THE NORMAL MODE   STOP AT THE END OF THE CURRENT
             *       SW 1    AS DETERMINED BY THE     PASS AND RETURN TO KEY BOARD
             *               OTHER SWITCHES.          CONTROL
             *
             *
             *       BP 2    CONTINUE TO RUN THE      CYCLE TEST RUNS FROM READ TO
             *       SW 2    TEST MODE SELECTED BY    PUNCH TO READ, ETC.
             *               SWITCH 3.
             *
             *
             *       BP 3    SELECTS PUNCH MODE       SELECTS READ MODE.
             *       SW 3    (USED WHEN SWITCH 2 IS RESET OR WHEN STARTING THE TEST)
             *
             *
             *       BP 4    STOP AND TYPE DIAGNOSTIC DO NOT STOP OR TYPE ON ERRORS.
```

Table 4-6. 9300 Computer, Extended Mode I/O Test Program (Sheet 2 of 20)

```
*        SW 4    MESSAGES WHENEVER AN     CONTINUE RUNNING REGARDLESS.
*                ERROR OCCURS.
*
*
* NOTE: TO RUN CONTINOUS FROM READ TO PUNCH THE OUTPUT OF THE PUNCH
*        SHOULD BE FED INTO THE READER.  A LOOP SHOULD BE USED TO RUN
*        CONTINOUS ON THE READER.
         PAGE
*
*  THE FOLLOWING SECTION OF CODE DEFINES EITHER A 925/930 INSTRUCTION
*  SET OR A 9300 INSTRUCTION SET. THIS IS DONE ON THE BASIS OF THE
*  MACHINE TYPE STATEMENT AT THE BEGINNING OF THE DECK.
*
*
*
*
         PROC
DF9300   NAME
$INST    FORM    3,6,15
P        PROC    1                         DEFINE INDEX OP'S TO IMPLY X1.
$LDX     NAME    017
$STX     NAME    077
$BRX     NAME    057
         INST    (P(*1)*/2)++1,P(0),P(1)
         END
P        PROC    1
$XAB     NAME    037733                    DEFINE COMPATIBLE REGISTER OP'S
$ABC     NAME    037731
$BAC     NAME    037713
$CLR     NAME    037711
         INST    0,040,P(0)
         END
P        PROC    1
$RSH     NAME    000                       DEFINE COMPATIBLE SHIFTS
$RCY     NAME    002
$LSH     NAME    004
$LCY     NAME    006
$NOD     NAME    044
$SHFT    FORM    3,6,6,9
         SHFT    P(2),060,P(0),P(1)**0777
         END
P        PROC    1                         DEFINE MISC. COMPATIBLE OP'S.
$MIN     NAME    071
$MIB     NAME    030
$RIM     NAME    032
         INST    (P(*1)*/2)++P(2),P(0),P(1)
         END
*
```

Table 4-6. 9300 Computer, Extended Mode I/O Test Program (Sheet 3 of 20)

```
$X       EQU      1                          DEFINE INDEX TAG*X* FOR X1
*                                            EOD CONSTANT
         AORG     0177
$EODC    DATA     04000000                   EOD CONSTANT
*
$SWTFRM      FORM   3,6,3,12
Q        PROC     1
$BPT     NAME     040000
$OVT     NAME     014040
$ROV     NAME     04000
$SOV     NAME     00040
         SWTFRM   0,022,Q(0)*/(-12)**7,Q(0)**07777++(Q(1)>0)*/(6-Q(1))
         END
         END
*
         PROC
DF930    NAME
*
* IF NOT A 9300 THEN DO THE FOLLOWING OPERATIONS
*
P        PROC     1                          DEFINE I/O INSTRUCTIONS
$MIB     NAME     012
$BIM     NAME     032
INST     FORM     3,6,1,14
         INST     P(2),P(0),P(*1),P(1)
         END
*
$X       EQU      2                          DEFINE INDEX TAG *X* FOR 2 ON 930
*
*
         AORG     0177
$EODC    DATA     0400000                    EOD CONSTANT
*
*
N        PROC     1                          SET OVERFLOW
$SOV     NAME
         BRR      $,4
         END
*
M        PROC     1                          BRANCH AND CLEAR INTERRUPT
$BRC     NAME
         DO       M(*1),1,2
         BRU      M(1)
         BRU      *$+1
         PZE      M(1)
         END
P        PROC     1
$DSC     NAME     0
```

Table 4-6. 9300 Computer, Extended Mode I/O Test Program (Sheet 4 of 20)

```
                          $ALC    NAME    050000
                          $ASC    NAME    012000
                          $STOP   NAME    014000
                          I       FORM    3,6,15
                                  I       P(1)**2,(P(1)**4)*/3++2,P(0)++(P(1)**1)*/6
                                  END
                          P       PROC    1
                          $CAT    NAME    014000
                          $CET    NAME    011000
                          $CIT    NAME    010400
                          $CZT    NAME    012000
                          I       FORM    3,6,15
                                  I       P(1)**2,040,P(0)++(P(1)**4)*/12++(P(1)**1)*/6
                                  END
                                  END
                                  DO      TYPE=9300
00177  04000000                   DF9300
                                  DO      TYPE<9300
                                  DF930
                                  PAGE
                          *
                          *  THE START OF THE PROGRAM
                          *
00200                             AORG    0200
00200  0 0 16 00203       BEGIN   LDA     BRUGO           INITIALIZE RECOVERY LOCATIONS
00201  0 0 76 00001               STA     1
00202  0 0 76 00032               STA     032
00203  0 0 01 00204       BRUGO   BRU     KYBD
00204  0 0 21 01241       KYBD    EXU     RDIS
00205  0 0 21 01231               EXU     PDIS
00206  0 40 37711         GO2     CLR
00207  0 0 76 01444               STA     T1
00210  0 02 0 02001               RKB     0,1,1
00211  0 32 01445         GO1     BIM     T1+1            READ CHARACTER
00212  0 0 16 01445               LDA     T1+1
00213  0 0 14 01636               LDB     =077
00214  0 0 55 01637               SKM     =' P'          CHECK FOR CONTROL CHAR.
00215  0 0 01 00217               BRU     $+2
00216  0 0 01 00233               BRU     PO
00217  0 0 55 01640               SKM     =' R'
00220  0 0 01 00222               BRU     $+2
00221  0 0 01 00256               BRU     RO
00222  0 0 55 01641               SKM     =' S'
00223  0 0 01 00225               BRU     $+2
00224  0 0 03 00317               BRM     SO
00225  0 0 54 01642               SKA     =070            CHECK FOR DIGIT
00226  0 0 01 00206               BRU     GO2              IF NOT CONTROL OR DIGIT CLEAR
00227  0 0 14 01444               LDB     T1
```

Table 4-6. 9300 Computer, Extended Mode I/O Test Program (Sheet 5 of 20)

```
00230  0 0 74 01446         STB     T1+2                 SAVE CHANNEL NUMBER IN T1+2
00231  0 0 76 01444         STA     T1                   SAVE UNIT NUMBER IN T1
00232  0 0 01 00211         BRU     GO1
                            PAGE
                     *
                     *   PUNCH CHANNEL SET UP ROUTINE
                     *
00233  0 0 03 00323  PO     BRM     MAKECH               GET CHANNEL NO. BUILT. SAVED IN T1+2
00234  1 17 01643           LDX     =-4**0177777         UPDAIE EOM/EOD'S
00235  0 1 16 01234         LDA     PALC+1,X
00236  0 0 11 01644         ETR     =050277677
00237  0 0 13 01446         MRG     T1+2                 INSERT CHANNEL DESIGNATION
00240  1 0 76 00235         STA     *$-3
00241  1 57 00235           BRX     $-4
00242  1 17 01645           LDX     =-3**0177777        UPDATE SKS'S
00243  0 1 16 01227         LDA     PCFT+1,X
00244  0 0 11 01646         ETR     =057737677
00245  0 0 13 01447         MRG     T1+3
00246  1 0 76 00243         STA     *$-3
00247  1 57 00243           BRX     $-4
00250  1 17 01643           LDX     =-4**0177777         UPDAIE CHANNEL COMMANDS
00251  0 1 16 01212         LDA     PIOSD+2,X
00252  0 0 11 01647         ETR     =050277777
00253  0 0 13 01450         MRG     T1+4
00254  1 0 76 00251         STA     *$-3
00255  1 57 00256           BRX     $+1
00256  1 57 00251           BRX     $-5
00257  0 0 16 01230         LDA     PTL                  UPDAIE UNIT NO.
00260  0 0 11 01650         ETR     =-2
00261  0 0 13 01444         MRG     T1
00262  0 0 76 01230         STA     PTL
00263  0 0 13 01651         MRG     =02000              MAKE NO LEADER EOM
00264  0 0 76 01227         STA     PPT
00265  0 0 01 00204         BRU     KYBD
                     *
                     *   READER CHANNEL SET UP ROUTINE
                     *
                     *
00266  0 0 03 00323  RC     BRM     MAKECH               GET CHANNEL NO BUILT
00267  1 17 01643           LDX     =-4**0177777         UPDAIE EOM/EOD'S
00270  0 1 16 01244         LDA     RALC+1,X
00271  0 0 11 01644         ETR     =050277677
00272  0 0 13 01446         MRG     T1+2
00273  1 0 76 00270         STA     *$-3
00274  1 57 00270           BRX     $-4
00275  1 17 01643           LDX     =-4**0177777        BUILD SKS'S
00276  0 1 16 01240         LDA     RCIT+1,X
00277  0 0 11 01646         ETR     =057737677
```

Table 4-6. 9300 Computer, Extended Mode I/O Test Program (Sheet 6 of 20)

```
00300  0 0 13 01447           MRG   T1+3
00301  1 0 76 00276           STA   *$-3
00302  1 57 00276             BRX   $-4
00303  1 17 01652             LDX   =-10**0177777       BUILD CHANNEL COMMAND E0M/E0D'S
00304  0 1 16 01224           LDA   RI0RD+2,X
00305  0 0 11 01653           ETR   =070277777
00306  0 0 13 01450           MRG   T1+4
00307  1 0 76 00304           STA   *$-3
00310  1 57 00311             BRX   $+1
00311  1 57 00304             BRX   $-5
00312  0 0 16 01240           LDA   RPT                  BUILD RPT WITH UNIT N0.
00313  0 0 11 01650           ETR   =-2
00314  0 0 13 01444           MRG   T1
00315  0 0 76 01240           STA   RPT
00316  0 0 01 00204           BRU   KYBD
                        *
                        *
                        *     START TEST RUNNING
                        *
00317  0 02 00000       S0    DSC   0                    DISC0NNECT
00320  0 22 4 00010           BPT   3                    START READ 0R PUNCH?
00321  0 0 01 00640           BRU   IN                   READ
00322  0 0 01 00356           BRU   0UT                  PUNCH
                              PAGE
                        *
                        *     BUILD CHANNEL N0. SUBR0UTINE
                        *
00323  0 0 00 00000     MAKECH PZE
00324  0 40 37711             CLR
00325  0 0 16 01446           LDA   T1+2                 GET CH. N0.
00326  0 0 54 01654           SKA   =4                  E0D REQUIRED
00327  0 0 14 00177           LDB   E0DC                 YES
00330  0 0 74 01450           STB   T1+4                 N0, SAVE E0D BIT.
00331  0 0 11 01655           ETR   =3
00332  0 0 76 01446           STA   T1+2
00333  1 17 01446             LDX   T1+2
00334  0 0 16 01450           LDA   T1+4
00335  0 1 13 00352           MRG   MAKETB,X             BUILD E0M/E0D SELECTI0N
00336  0 0 76 01446           STA   T1+2                 SAVE E0M
00337  0 40 37713             BAC                        BUILD SKS SELECTI0N
00340  0 0 54 00177           SKA   E0DC
00341  0 0 14 01656           LDB   =040000
00342  0 40 37733             XAB
00343  0 1 13 00352           MRG   MAKETB,X
00344  0 0 76 01447           STA   T1+3                 SAVE SKS
00345  0 0 16 01444           LDA   T1                   BUILD UNIT N0. BIT
00346  0 0 11 01657           ETR   =1
00347  0 0 12 01657           E0R   =1
```

Table 4-6. 9300 Computer, Extended Mode I/O Test Program (Sheet 7 of 20)

```
00350  0 0 76 01444              STA    T1                    SAVE UNIT NO. BIT
00351  0 0 41 00323              BRR    MAKECH                EXIT
                           *
00352  00000000           MAKETB DATA   0,0100,020000000,020000100
00353  00000100
00354  20000000
00355  20000100
                                 PAGE
                           *
                           *  PAPER TAPE PUNCH OUTPUT SECTION.
                           *
00356  1 17 01660         OUT    LDX    =-64**0177777        SET UP OUTPUT IMAGE WITH 64 WORDS
00357  0 40 37711               CLR
00360  0 1 76 01344              STA    IMAGE+64,X
00361  0 0 05 01651              ADD    =01000000
00362  1 57 00360                BRX    $-2
00363  0 0 21 01230        OUT4   EXU    PTL                   START PUNCH WITH LEADER
00364  0 0 21 01233              EXU    PALC                  ALERT CHANNEL
00365  0 0 21 01236              LCH    PIOSP                 LOAD IOSP IMAGE,64
00366  0 0 31 01207
00367  1 17 01643                LDX    =-4**0177777         SET UP FOR SUBROUTINE TO TYPE:
00370  0 0 14 01652              LDB    =ERMSG1               IOSP, OUTPUT
00371  0 0 16 00431              LDA    PCATC
00372  0 0 03 00610              BRM    WCZ                   WAIT FOR CHANNEL COUNT = ZERO
00373  0 0 21 01226              EXU    PCET                  ERROR ON OUTPUT
00374  0 22 4 0004               BPT    4                     YES, CHECK BP4 FOR NO STOP
00375  0 0 01 00416              BRU    OUT4A                 NO, NO STOP ON ERROR
00376  0 0 21 01231        OUT2   EXU    PDIS                  ERROR, DISCONNECT CHANNEL
00377  0 02 0 02641              TYP    0,1,4                 TYPE GENERAL ERROR MESSAGE
00400  0 30 01663                MIB    =052121225            I  E
00401  0 30 01664                MIB    =051514651            RROR
00402  0 30 01665                MIB    =012246451             DUR
00403  0 30 01666                MIB    =031452712            ING
00404  0 40 37733                XAB                          TYPE SPECIFIC ERROR MESSAGE
00405  0 0 13 01635              MRG    MIBX
00406  0 0 76 00407              STA    $+1
00407  0 30 00000                MIB    00                    TO BE REPLACED AT RUN TIME
00410  0 71 00407                MIN    $-1
00411  1 57 00407                BRX    $-2
00412  0 02 14000         GOTOP  TOP    0
00413  0 20 14000                CAT    0
00414  0 0 01 00413              BRU    $-1
00415  0 0 01 00204              BRU    KYBD
                           *
00416  0 0 03 00476        OUT4A  BRM    OUTPIN                GO PIN AND CHECK CHANNEL ADDRESS
00417  0 0 21 01224              EXU    PCAT                  IF CHANNEL INACTIVE READDRESS PUNCH
00420  0 0 01 00422              BRU    $+2
00421  0 0 21 01227              EXU    PPT
```

Table 4-6. 9300 Computer, Extended Mode I/O Test Program (Sheet 8 of 20)

```
00422  0 0 21 01233      333        EXU     PALC
00423  0 0 21 01210      334        LCH     PIOSD                 LOAD CH. IOSD IMAGE,64
00424  0 0 31 01211
00425  1 17 01643        335 OUT1   LDX     =-4**0177777         SET UP ERROR MESSAGE:
00426  0 0 14 01657      336        LDB     =ERMSG2               IOSD, OUTPUT
00427  0 0 16 00431      337        LDA     PCATC
00430  0 0 03 00610      338        BRM     WCZ                   WAIT FOR COUNT EQUAL ZERO
00431  0 0 21 01224      339 PCATC  EXU     PCAT                  CHAN. ACTIVE?
00432  0 0 01 00431      340        BRU     $-1                   YES
00433  0 0 21 01226      341        EXU     PCET                  NO, ERROR?
00434  0 22 4 0004       342        BPT     4                     YES, IS STOP ALLOWED?
00435  0 0 01 00437      343        BRU     $+2                   NO ERROR OR NO STOP
00436  0 0 01 00376      344        BRU     OUT2                  ERROR STOP ALLOWED
00437  0 0 03 00476      345        BRM     OUTPIN                GO PIN AND CHECK CHANNEL ADDRESS
00440  0 40 37711        346        CLR
00441  0 0 76 01452      347        STA     PRF                   R(PUNCH REPEAT)
00442  0 0 21 01230      348 OUT1A  EXU     PTL
00443  0 0 21 01233      349        EXU     PALC
00444  0 0 21 01210      350        LCH     PIOSD                 LOAD IOSD  IMAGE,64
00445  0 0 31 01211
00446  1 17 01643        351        LDX     =-4**0177777         SET UP ERROR MESSAGE:
00447  0 0 14 01657      352        LDB     =ERMSG2
00450  0 0 16 00431      353        LDA     PCATC
00451  0 0 03 00610      354        BRM     WC7
00452  0 0 21 01224      355        EXU     PCAT                  CHAN. ACTIVE?
00453  0 0 01 00452      356        BRU     $-1                   YES
00454  0 0 21 01226      357        EXU     PCET                  NO, CHAN. ERROR
00455  0 22 4 0004       358        BPT     4                     YES, IS ERROR STOP ALLOWED
00456  0 0 01 00450      359        BRU     $+2                   NO,NO
00457  0 0 01 00376      360        BRU     OUT2                  YES
00460  0 0 03 00476      361        BRM     OUTPIN                GO PIN AND CHECK CHANNEL ADDRESS
00461  0 0 53 01452      362        SKN     PRF                   PUNCH REPEAT
00462  0 0 01 00454      363        BRU     $+2                   RESET
00463  0 0 01 00457      364        BRU     OUT3                  SET
00464  0 0 16 01670      365        LDA     =-1                  S(PUNCH REPEAT)
00465  0 0 76 01452      366        STA     PRF
00466  0 0 01 00442      367        BRU     OUT1A
                         368 *
                         369 *
00467  0 22 4 0040       370 OUT3   BPT     1                     GO OR STOR
00470  0 0 01 00204      371        BRU     KYBD                  STOP
00471  0 22 4 0020       372        BPT     2                     GO, CYCLE?
00472  0 0 01 00640      373        BRU     IN                    YES
00473  0 22 4 0010       374        BPT     3                     ONE ONLY
00474  0 0 01 00640      375        BRU     IN
00475  0 0 01 00356      376        BRU     OUT
                         377 *
                         378 *  SUBROUTINE TO CHECK CHANNEL ADDRESS
```

Table 4-6. 9300 Computer, Extended Mode I/O Test Program (Sheet 9 of 20)

```
                             *
00476  0 0 00 00000          OUTPIN PZE     0
00477  0 0 21 01232                 EXU     PASC                ALERT TO STORE PUNCH CHANNEL
00500  0 0 33 01444                 PIN     T1                  STORE ADDRESS
00501  0 0 16 01444                 LDA     T1
00502  0 0 12 01671                 EOR     =IMAGE+64           COMPARE WITH EXPECTED
00503  0 0 54 01670                 SKA     =-1
00504  0 22 4 0004                  BPT     4                   NOT EQUAL
00505  0 0 41 00476                 BRR     OUTPIN              EQUAL OR ERROR STOP NOT PERMITTED
00506  1 77 01445                   STX     T1+1                SAVE LENGTH OF ERROR MESSAGE
00507  0 40 37733                   XAB                         SET UP ERROR OUTPUTTER
00510  0 0 13 01635                 MRG     MIBX
00511  0 0 76 00530                 STA     OTPIN1
00512  0 0 16 01671                 LDA     =IMAGE+64           GENERATE EXPECTED PIN WORD IN BCD
00513  0 0 03 00537                 BRM     MKOCT
00514  0 0 76 00577                 STA     OTPNM1              SAVE EXPECTED
00515  0 0 74 00600                 STB     OTPNM1+1
00516  0 0 16 01444                 LDA     T1                  GENERATE ACTUAL PIN WORD IN BCD
00517  0 0 03 00537                 BRM     MKOCT
00520  0 0 76 00605                 STA     OTPNM2
00521  0 0 74 00606                 STB     OTPNM2+1
00522  0 0 21 01231                 EXU     PDIS                DISCONNECT PUNCH CHANNEL
00523  1 17 01672                   LDX     =-15**0177777
00524  0 02 0 02641                 TYP     0,1,4
00525  1 30 00574                   MIB     OTPNM+15,X          OUTPUT MESSAGE
00526  1 57 00525                   BRX     $-1
00527  1 17 01445                   LDX     T1+1                OUTPUT SPECIAL MESSAGE
00530  0 30 00000            OTPIN1 MIB     00
00531  0 71 00530                   MIN     $-1
00532  1 57 00530                   BRX     $-2
00533  1 17 01673            OTPIN2 LDX     =-12**0177777       OUTPUT RECEIVED AND EXPECTED MESSAGE
00534  1 30 00610                   MIB     OTPNM2+3,X
00535  1 57 00534                   BRX     $-1
00536  0 0 01 00412                 BRU     GOTOP
                             *
                             *
                             *  SUBROUTINE TO MAKE ONE WORD INTO 8 BCD OCTAL DIGITS
                             *
00537  0 0 00 00000          MKOCT  PZE     0
00540  1 17 01674                   LDX     =-8**0177777
00541  0 40 37731                   ABC                         0 TO WORD TO B
00542  0 60 04 003                  LSH     3                   SHIFT OUT OCTAL DIGIT
00543  0 1 76 01456                 STA     T1+10,X             SAVE BCD CHARACTER
00544  0 0 16 01675                 LDA     =0                  CLEAR A
00545  1 57 00542                   BRX     $-3
00546  0 40 37711                   CLR
00547  1 17 01674                   LDX     =-8**0177777        REASSEMBLY BCD CHARACTERS INTO A + B.
00550  0 60 06 005                  LCY     6
```

```
00551   0 1 13 01456             MRG      T1+10,X
00552   1 57 00550               BRX      $-2
00553   0 40 37733               XAB
00554   0 0 41 00537             BRR      MK8CT               EXIT
                          *
                          *
                          *  ERROR MESSAGES FOR CHANNEL ADDRESS TEST SUBROUTINE
                          *
00555   52254524          OTPNM  BCD      52,1END ADDRESS FROM CHANNEL DID NOT AGREE WITH EXPECTE
00556   12212424
00557   51256262
00560   12265146
00561   44122330
00562   21454525
00563   43122431
00564   24124546
00565   63122127
00566   51252512
00567   66316330
00570   12256747
00571   25236325
00572   24122126                 BCD      8,D AFTER
00573   63255112
00574   25674725                 BCD      12,EXPECTED
00575   23632524
00576   12121212
00577   00000000          OTPNM1 DATA     0,0
00600   00000000
00601   73121252                 BCD      16,,  1RECEIVED
00602   51252325
00603   31652524
00604   12121212
00605   00000000          OTPNM2 DATA     0,0
00606   00000000
00607   33125252                 BCD      4,. 11
                                 PAGE
                          *
                          *  WAIT FOR COUNT EQUAL ZERO SUBROUTINE.
                          *
00610   0 0 00 00000      WCZ    PZE                          ENTRY
00611   0 0 76 00617             STA      $+6                 SAVE R/PCAT
00612   0 0 05 01657             ADD      =1                  MAKE A CZT
00613   0 0 76 00614             STA      $+1                 SAVE R/PCZT
00614   0 20 12000               CZT      00                  C = 02?
00615   0 0 01 00617             BRU      $+2                 NO
00616   0 0 41 00610             BRR      WCZ                 YES
00617   0 20 14000               CAT      00                  CHANNEL ACTIVE?
00620   0 0 01 00614             BRU      $-4                 YES
```

Table 4-6. 9300 Computer, Extended Mode I/O Test Program (Sheet 11 of 20)

```
00621  0 22 4 0004                  BPT     4                        NO, INHIBIT ERRORS
00622  0 0 41 00610                 BRR     WCZ                      YES
00623  1 77 01444                   STX     T1                       NO, PRINT ERROR MESSAGE
00624  0 40 37733                   XAB
00625  0 0 13 01635                 MRG     MIBX
00626  0 0 76 00634                 STA     $+6
00627  1 17 01676                   LDX     =-13**0177777
00630  0 02 0 02641                 TYP     0,1,4
00631  1 30 01500                   MIB     DISMSG+13,X
00632  1 57 00631                   BRX     $-1
00633  1 17 01444                   LDX     T1
00634  0 30 00000                   MIB     00
00635  0 71 00634                   MIN     $-1
00636  1 57 00634                   BRX     $-2
00637  0 0 01 00412                 BRU     GOTOP
                                    PAGE
                              *
                              *  INPUT SECTION
                              *
00640  0 0 03 01177           IN    BRM     STARTP                   START READER
00641  0 22 0 4000                  ROV
00642  0 0 21 01243                 EXU     RALC                     ALERT
00643  0 0 21 01212                 LCH     RIOSD                    LOAD IOSD  BUFFER,64
00644  0 0 31 01213
00645  0 0 21 01235           INOB  EXU     RCZT                     C=0
00646  0 0 01 00657                 BRU     INO                      NO
00647  0 0 21 01234           RCATC EXU     RCAT                     YES, CHAN. ACTIVE
00650  0 22 4 0004                  BPT     4                        YES, ERROR STOP PERMITTED
00651  0 0 01 00670                 BRU     INOA                     NO, NO CONT.
00652  1 17 01676                   LDX     =-13**0177777            YES
00653  0 02 0 02641                 TYP     0,1,4
00654  1 30 01525                   MIB     ERMSG4+13,X
00655  1 57 00654                   BRX     $-1
00656  0 0 01 00412                 BRU     GOTOP
                              *
00657  0 0 21 01234           INO   EXU     RCAT                     CHAN. ACTIVE STILL?
00660  0 0 01 00645                 BRU     INOB                     YES
00661  0 0 21 01235                 EXU     RCZT                     NO, C=0
00662  0 0 01 00664                 BRU     $+2                      NO
00663  0 0 01 00670                 BRU     INOA                     YES
00664  1 17 01645                   LDX     =-3**0177777            SET UP ERROR MESSAGE
00665  0 0 14 01677                 LDB     =ERMSG5
00666  0 0 16 00647                 LDA     RCATC
00667  0 0 03 00610                 BRM     WCZ                      GO DO DISCONNECT ERROR TEST
00670  0 0 16 01700           INOA  LDA     =033120152               BLOCK NO. 1
00671  0 0 14 01701                 LDB     =BUFFER+64               END ADDRESS EXPECTED
00672  0 0 03 01055                 BRM     CHECK                    GO CHECK DATA
00673  0 0 03 01177           IN1   BRM     STARTP                   START READER IF DATA CHECKED O.K.
```

```
00674  0 22 0 4003          R0V
00675  0 0 21 01243          EXU    RALC
00676  0 0 21 01214          LCH    RI0SP              L0AD I0SP BUFFER,65
00677  0 0 31 01215
00700  0 0 16 01670          LDA    =-1
00701  0 0 76 01451          STA    SPF                S(I0SP INPUT)
00702  0 0 21 01237     IN4  EXU    RCIT               INTERREC0RD C0NDITI0N
00703  0 0 01 00705          BRU    $+2                N0
00704  0 0 01 00732          BRU    IN2                YES
00705  0 0 21 01234          EXU    RCAT               CHAN. ACTIVE
00706  0 0 01 00716          BRU    IN1A               YES
00707  0 22 4 0004           BPT    4                  N0, ERR0R ST0P PERMITTED
00710  0 0 01 00732          BRU    IN2                N0
00711  1 17 01672            LDX    =-15**0177777      YES
00712  0 02 0 02641          TYP    0,1,4
00713  1 30 01547            MIB    ERMSG6+15,X
00714  1 57 00713            BRX    $-1
00715  0 0 01 00412          BRU    G0T0P
                        *
00716  0 0 21 01235     IN1A EXU    RCZT               C=0
00717  0 0 01 00702          BRU    IN4                N0
00720  0 0 21 01237          EXU    RCIT               YES, CHAN. INTER-REC0RD
00721  0 0 01 00732          BRU    IN2                N0
00722  0 22 4 0004           BPT    4                  YES, ERR0R ST0P PERMITTED
00723  0 0 01 00732          BRU    IN2                N0
00724  0 0 21 01241          EXU    RDIS               YES, ST0P TAPE
00725  1 17 01702            LDX    =-17**0177777
00726  0 02 0 02641          TYP    0,1,4
00727  1 30 01570            MIB    ERMSG7+17,X
00730  1 57 00727            BRX    $-1
00731  0 0 01 00412          BRU    G0T0P
                        *
00732  0 0 21 01236     IN2  EXU    RCET               IF CHANNEL ERR0R
00733  0 22 0 0040           S0V                       SET 0VERFL0W
00734  0 0 21 01241          EXU    RDIS               ST0P TAPE
00735  0 0 53 01451          SKN    SPF                I0SP INPUT FLAG
00736  0 0 01 00756          BRU    IN3                RESET
00737  0 0 16 01703          LDA    =033120252         SET, GET BL0CK N0. 2
00740  0 0 14 01444          LDB    BUFFER+64          END ADDRESS EXPECTED
00741  0 0 03 01055          BRM    CHECK              CHECK DATA INPUT
                        *                              IF C0RRECT C0NTINUE.
00742  0 0 03 01177          BRM    STARTP             START TAPE
00743  0 22 0 4003           R0V
00744  0 0 21 01243          EXU    RALC               ALERT
00745  0 0 21 01216          LCH    RI0SP1             L0AD I0SP BUFFER,32
00746  0 0 31 01217
00747  1 17 01645            LDX    =-3**0177777       SET UP ERR0R MESSAGE
00750  0 0 14 01704          LDB    =ERMSG8
```

```
00751  0 0 16 00647      548        LDA     RCATC
00752  0 0 03 00610      549        BRM     WCZ                 GO WAIT FOR C=0
00753  0 0 21 01236      550        EXU     RCET                IF CHANNEL ERROR
00754  0 22 0 0040       551        SOV                         SET OVERFLOW
00755  0 0 21 01234      552        EXU     RCAT                IS READER STILL RUNNING
00756  0 0 01 00760      553        BRU     IN5                 YES
00757  0 0 21 01240      554        EXU     RPT                 NO, RESTART TAPE READER
00760  0 0 21 01243      555 IN5    EXU     RALC
00761  0 0 21 01220      556        LCH     RIORP               LOAD IORD BUFFER+32,33
00762  0 0 31 01221
00763  0 40 37711        557        CLR
00764  0 0 76 01451      558        STA     SPF                 R(IOSP INPUT)
00765  0 0 01 00702      559        BRU     IN4
                         560 *
00766  0 0 16 01705      561 IN3    LDA     =033120352          BLOCK NO. 3
00767  0 0 14 01701      562        LDB     =BUFFER+64          END ADDRESS EXPECTED
00770  0 0 03 01055      563        BRM     CHECK               GO CHECK DATA
00771  0 0 03 01177      564        BRM     STARTP              START TAPE
00772  0 0 21 01243      565        EXU     RALC
00773  0 0 21 01222      566        LCH     RIORD               LOAD IORD BUFFER,56
00774  0 0 31 01223
00775  0 0 21 01234      567        EXU     RCAT                CHAN. ACTIVE
00776  0 0 01 00775      568        BRU     $-1                 YES, WAIT FOR STOP
00777  1 17 01674        569        LDX     =-8**0177777       CHAN. INACTIVE
01000  0 0 16 01636      570        LDA     =077
01001  0 1 54 01444      571        SKA     BUFFER+64,X         CHECK FOR O'S IN LAST 8 CHARACTERS
01002  0 0 01 01024      572        BRU     IN3A
01003  1 57 01001        573        BRX     $-2
01004  1 17 01674        574 IN3B   LDX     =-8**0177777       O.K. INSERT CORRECT 8 CHARACTERS
01005  0 0 16 01642      575        LDA     =070
01006  0 1 76 01444      576        STA     BUFFER+64,X
01007  0 0 05 01657      577        ADD     =1
01010  1 57 01006        578        BRX     $-2
01011  0 0 16 01706      579        LDA     =033120452          BLOCK NO. 4
01012  0 0 14 01707      580        LDB     =BUFFER+56          END ADDRESS EXPECTED
01013  0 22 0 4000       581        ROV
01014  0 0 03 01055      582        BRM     CHECK               GO CHECK DATA
01015  0 22 4 0040       583        BPT     1                   TEST STOP?
01016  0 0 01 00204      584        BRU     KYBD                YES
01017  0 22 4 0020       585        BPT     2                   TEST CYCLE?
01020  0 0 01 00356      586        BRU     OUT                 YES
01021  0 22 4 0010       587        BPT     3                   TEST ONE ONLY.
01022  0 0 01 00640      588        BRU     IN                  READ
01023  0 0 01 00356      589        BRU     OUT                 PUNCH
                         590 *
01024  0 22 4 0004       591 IN3A   BPT     4                   ERROR STOP PERMITTED
01025  0 0 01 01004      592        BRU     IN3B                NO
01026  1 17 01674        593        LDX     =-8**0177777       FORMAT LAST EIGHT CHARACTERS FOR TYPE
```

Table 4-6. 9300 Computer, Extended Mode I/O Test Program (Sheet 14 of 20)

```
01027  0 40 37711           CLR
01030  0 1 16 01444  IN3D   LDA    BUFFER+64,X
01031  0 60 04 003          LSH    3
01032  0 1 13 01444         MRG    BUFFER+64,X
01033  0 0 11 01710         ETR    =0707
01034  0 0 13 01711         MRG    =052120000
01035  0 60 04 005          LSH    6
01036  0 1 76 01055         STA    MSGIMG+8,X
01037  1 57 01030           BRX    IN3D
01040  1 17 01712           LDX    =-19**0177777       OUTPUT ERROR MESSAGE
01041  0 02 0 02641         TYP    0,1,4
01042  1 30 01616           MIB    ERMSG9+19,X
01043  1 57 01042           BRX    $-1
01044  0 02 14000           TOP    0
01045  0 20 14000           CAT    0
01046  0 0 01 01045         BRU    $-1
01047  0 02 0 02041         TYP    0,1,1               OUTPUT 8 CHARACTERS
01050  1 17 01674           LDX    =-8**0177777
01051  1 30 01065           MIB    MSGIMG+8,X
01052  1 57 01051           BRX    $-1
01053  0 30 01503           MIB    ERMSG1+3            CR
01054  0 0 01 00412         BRU    GOTOP
                     *
                     *
01055                MSGIMG RES    8
                            PAGE
                     *
                     *  CHECK INPUT DATA SUBROUTINE.
                     *
01065  0 0 00 00000  CHECK  PZE
01066  0 0 76 01626         STA    ERMSG0+6            SAVE BLOCK NO.
01067  0 0 21 01236         EXU    RCET                CHECK FOR ERROR
01070  0 0 01 01141         BRU    PARERR              GO TO PARITY ERROR ROUTINE
01071  0 22 1 40400         OVT                        CHECK FOR PREVIOUSLY NOTED ERROR
01072  0 0 01 01141         BRU    PARERR              GO TO PARITY ERROR ROUTINE
01073  0 0 21 01242         EXU    RASC                STORE CHANNEL ADDRESS
01074  0 0 33 01444         PIN    T1
01075  0 0 74 01445         STB    T1+1                SAVE EXPECTED
01076  0 0 16 01444         LDA    T1
01077  0 0 12 01445         EOR    T1+1                COMPARE ACTUAL WITH EXPECTED
01100  0 0 54 01670         SKA    =-1                 AGREE
01101  0 0 01 01154         BRU    PINERR              NO
01102  1 17 01660    CHECK2 LDX    =-64**0177777       YES
01103  0 0 16 01675         LDA    =00
01104  0 0 14 01636         LDB    =077
01105  0 1 55 01444         SKM    BUFFER+64,X         CHECK INPUT BUFFER
01106  0 0 01 01112         BRU    CHECK1              ERROR
01107  0 0 05 01657         ADD    =1
01110  1 57 01105           BRX    $-3
```

Table 4-6. 9300 Computer, Extended Mode I/O Test Program (Sheet 15 of 20)

```
01111  0 0 41 01055           BRR     CHECK               EXIT IF ALL CORRECT
                          *
01112  0 22 4 0004     CHECK1 BPT     4                   ERROR STOP PERMITTED?
01113  0 0 41 01055           BRR     CHECK               NO, EXIT
01114  0 0 76 01444           STA     T1                  YES
01115  0 60 04 003            LSH     3                   FORMAT EXPECTED
01116  0 0 13 01444           MRG     T1
01117  0 0 11 01710           ETR     =0707
01120  0 60 04 005            LSH     6
01121  0 0 13 01713           MRG     =012000052
01122  0 0 76 01631           STA     ERMSG0+9            STORE EXPECTED
01123  0 1 16 01444           LDA     BUFFER+64,X         FORMAT RECEIVED
01124  0 60 00 003            RSH     3
01125  0 1 16 01444           LDA     BUFFER+64,X
01126  0 60 04 003            LSH     3
01127  0 0 11 01710           ETR     =0707
01130  0 60 04 005            LSH     6
01131  0 0 13 01713           MRG     =012000052
01132  0 0 76 01634           STA     ERMSG0+12           STORE RECEIVED
01133  1 17 01676             LDX     =-13**0177777
01134  0 0 21 01241           EXU     RDIS                DISCONNECT READER CHANNEL
01135  0 02 0 02641           TYP     0,1,4
01136  1 30 01635             MIB     ERMSG0+13,X
01137  1 57 01136             BRX     $-1
01140  0 0 01 00412           BRU     GOTOP
                          *
                          *  PARITY ERROR SUBROUTINE
                          *
01141  0 22 4 0004     PARERR BPT     4                   ERROR STOP PERMITTED?
01142  0 0 41 01055           BRR     CHECK               NO
01143  0 0 21 01241           EXU     RDIS                YES, DISCONNECT READER CHANNEL
01144  0 02 0 02641           TYP     0,1,4
01145  1 17 01714             LDX     =-9**0177777
01146  1 30 01627             MIB     ERMSGP+9,X          OUTPUT PARITY ERROR MESSAGE
01147  1 57 01146             BRX     $-1
01150  0 02 14000             TOP     0
01151  0 20 14000             CAT     0
01152  0 0 01 01151           BRU     $-1
01153  0 0 01 01102           BRU     CHECK2              RETURN TO CHECK NUMBERS
                          *
                          *   PIN ADDRESS ERROR SUBROUTINE
                          *
01154  0 22 4 0004     PINERR BPT     4                   ERROR STOP PERMITTED
01155  0 0 01 01102           BRU     CHECK2              NO
01156  0 0 16 01444           LDA     T1                  YES
01157  0 0 03 00537           BRM     MKOCT               EXPAND ACTUAL TO BCD
01160  0 0 76 00605           STA     OTPNM2              SAVE
01161  0 0 74 00606           STB     OTPNM2+1
```

Table 4-6. 9300 Computer, Extended Mode I/O Test Program (Sheet 16 of 20)

```
  01162  0 0 16 01445          LDA    T1+1             EXPAND EXPECTED TO BCD
  01163  0 0 03 00537          BRM    MKOCT
  01164  0 0 76 00577          STA    OTPNM1           SAVE
  01165  0 0 74 00600          STB    OTPNM1+1
  01166  0 0 21 01241          EXU    RDIS             DISCONNECT READER
  01167  0 02 0 02641          TYP    0,1,4
  01170  1 17 01672            LDX    =-15**0177777
  01171  1 30 00574            MIB    OTPNM+15,X       OUTPUT GENERAL MESSAGE
  01172  1 57 01171            BRX    $-1
  01173  0 30 01624            MIB    ERMSG0+4         OUTPUT BLOCK NO.
  01174  0 30 01625            MIB    ERMSG0+5
  01175  0 30 01626            MIB    ERMSG0+6
  01176  0 0 01 00533          BRU    OTPIN2           GO OUTPUT RECEIVED AND EXPECTED
                         *
                         *  START TAPE READER SUBROUTINE
                         *
  01177  0 0 00 00000    STARTP PZE
  01200  1 17 01660            LDX    =-64**0177777
  01201  0 40 37711            CLR
  01202  0 1 76 01444          STA    BUFFER+64,X      CLEAR BUFFER
  01203  1 57 01202            BRX    $-1
  01204  0 0 21 01240          EXU    RPT              START TAPE
  01205  0 0 41 01177          BRR    STARTP           EXIT
                               PAGE
                         *
                         *  I/O CHANNEL COMMANDS
                         *
R 01206  002 146 0 00    PIOSP IOSP   IMAGE,64
  01207  0100 01244
R 01210  002 142 0 00    PIOSD IOSD   IMAGE,64
  01211  0100 01244
                         *
R 01212  002 142 0 00    RIOSD IOSD   BUFFER,64
  01213  0100 01344
R 01214  002 146 0 00    RIOSP IOSP   BUFFER,65
  01215  0101 01344
R 01216  002 146 0 00    RIOSP1 IOSP  BUFFER,32
  01217  0040 01344
R 01220  002 144 0 00    RIORP IORP   BUFFER+32,33
  01221  0041 01404
R 01222  002 140 0 00    RIORD IORD   BUFFER,56
  01223  0070 01344
                         *
                         *
                         *  I/O CHANNEL INSTRUCTIONS.
                         *
  01224  0 20 14000      PCAT  CAT    0
  01225  0 20 12000      PCZT  CZT    0
```

Table 4-6. 9300 Computer, Extended Mode I/O Test Program (Sheet 17 of 20)

```
01226   0 20 11000       PCET    CET      0
                         *
01227   0 02 0 02044     PPT     PPT      0,1,1
01230   0 02 0 00044     PTL     PTL      0,1,1
01231   0 02 00000       PDIS    DSC      0
01232   0 02 12000       PASC    ASC      0
01233   0 02 50000       PALC    ALC      0
                         *
                         *
01234   0 20 14000       RCAT    CAT      0
01235   0 20 12000       RCZT    CZT      0
01236   0 20 11000       RCET    CET      0
01237   0 20 10400       RCIT    CIT      0
                         *
01240   0 02 0 02004     RPT     RPT      0,1,1
01241   0 02 00000       RDIS    DSC      0
01242   0 02 12000       RASC    ASC      0
01243   0 02 50000       RALC    ALC      0
                         *
                         *
                         *  OUTPUT IMAGE AREA, INPUT BUFFER AREA
                         *
01244                    IMAGE   RES      64
01344                    BUFFER  RES      64
                         *
                         *
                         *  TEMPORARY STORAGE AND FLAGS
                         *
01444                    T1      RES      13
01461                    SPF     RES      1                IOSP INPUT FLAG
01462                    PRF     RES      1                PUNCH REPEAT FLAG
                                 PAGE
                         *
                         *  ERROR AND STATUS MESSAGES.
                         *
01463   52233021         DISMSG  BCD      52,ICHANNEL ERROROUSLY DISCONNECTED BEFORE C=0, DURING
01464   45452543
01465   12255151
01466   46514664
01467   62437012
01470   24316223
01471   46454525
01472   23632524
01473   12222526
01474   46512512
01475   23130073
01476   12246451
01477   31452712
```

```
01500  31466247      768 ERMSG1 BCD     16,IOSP, OUTPUT. ll
01501  73124664
01502  63476463
01503  33125252
01504  31466224      769 ERMSG2 BCD     16,IOSD, OUTPUT. ll
01505  73124664
01506  63476463
01507  33125252
01510  52233021      770 ERMSG4 BCD     52,lCHANNEL DID NOT DISCONNECT WHEN C=0 ON IOSD INPUTl
01511  45452543
01512  12243124
01513  12454663
01514  12243162
01515  23464545
01516  25236312
01517  66302545
01520  12231300
01521  12464512
01522  31466224
01523  12314547
01524  64635212
01525  31466224      771 ERMSG5 BCD     12,IOSD, INPUTl
01526  73123145
01527  47646352
01530  52233021      772 ERMSG6 BCD     52,lCHANNEL DISCONNECTED DURING IOSP INPUT, CIT NEVER
01531  45452543
01532  12243162
01533  23464545
01534  25236325
01535  24122464
01536  51314527
01537  12314662
01540  47123145
01541  47646373
01542  12233163
01543  12452565
01544  25511212
01545  63516425      773        BCD     8,TRUE. l
01546  33125212
01547  52246451      774 ERMSG7 BCD     48,lDURING IOSP INPUT C=0 INDICATING EOR PAST BUT C
01550  31452712
01551  31466247
01552  12314547
01553  64631223
01554  13001231
01555  45243123
01556  21633145
01557  27122546
01560  51124721
```

```
01561   62631222
01562   64631223
01563   31631266        775           BCD      20,IT WAS NEVER TRUE. I
01564   21621245
01565   25652551
01566   12635164
01567   25331252
01570   31466247        776 ERMSG8  BCD      12,I0SP, INPUTI
01571   73123145
01572   47646352
01573   52314651        777 ERMSG9  BCD      52,II3RD ON INPUT DID NOT IGNORE THE LAST 8 CHARACTERS,
01574   24124645
01575   12314547
01576   64631224
01577   31241245
01600   46631231
01601   27454651
01602   25126330
01603   25124321
01604   62631210
01605   12233021
01606   51212363
01607   25516273
01610   12226463        778           BCD      24, BUT READ THE FOLLOWINGI
01611   12512521
01612   24126330
01613   25122646
01614   43434666
01615   31452752
01616   52524721        779 ERMSGP  BCD      8,IIPARITY
01617   51316370
01620   52314547        780 ERMSGO  BCD      40,IINPUT ERROR IN BLOCK NO. NIEXPECTED DDI
01621   64631225
01622   51514651
01623   12314512
01624   22434623
01625   42124546
01626   33124552
01627   25674725
01630   23632524
01631   12242452
01632   51252325        781           BCD      12,RECEIVED DDI
01633   31652524
01634   12242452
                        782 *
01635   0 30 00000      783 MIBX    MIB      0                       OUTPUT INSTRUCTION
                        784 *
                        785 *
```

Table 4-6. 9300 Computer, Extended Mode I/O Test Program (Sheet 20 of 20)

```
      00000200        786        END      BEGIN
01636 00000077
01637 00606047
01640 00606051
01641 00606062
01642 00000070
01643 00177774
01644 50277677
01645 00177775
01646 57737677
01647 50277777
01650 77777776
01651 00002000
01652 00177766
01653 70277777
01654 00000004
01655 00000003
01656 00040000
01657 00000001
01660 00177700
01661 01000000
01662 00001500
01663 52121225
01664 51514651
01665 12246451
01666 31452712
01667 00001504
01670 77777777
01671 00001344
01672 00177761
01673 00177764
01674 00177770
01675 00000000
01676 00177763
01677 00001525
01700 33120152
01701 00001444
01702 00177757
01703 33120252
01704 00001570
01705 33120352
01706 33120452
01707 00001434
01710 00000707
01711 52120000
01712 00177755
01713 12000052
01714 00177767
```

SECTION V
TROUBLESHOOTING

5.1 GENERAL

5.2 This section contains information useful when troubleshooting the Model 932XX series TMCCs.

5.3 Troubleshooting information contained herein is based on the test programs given in Section 4 of this manual. When an error is indicated during performance of the tests given in Section 4, reference should first be made to the Programming Flow Charts illustrated in figure 5-1 and then to the applicable referenced data.

5.4 TEST PROGRAM FLOW CHART

5.5 Figure 5-1 illustrates the programming flow data for the extended mode test programs given in Section 4. An example of the usage of the flow charts is given in the following paragraphs.

5.6 FLOW CHART EXAMPLE

5.7 In presenting the example of usage of the flow charts, the following points will be assumed:

a. Paper tape reader connected to one of the interlaced channels.

b. Breakpoint 1 switch reset.

c. Breakpoint 2 switch reset.

d. Breakpoint 3 switch set.

e. Breakpoint 4 switch reset.

f. An error exists in block 4.

5.8 At the initialization of the test, the channel number has been inserted on the typewriter, the unit number being used, and the character "R" for the paper tape reader. The program begins at the top of sheet 1 of figure 5-1. The program initializes restart location, disconnects all channels, addresses the keyboard and reads the character typed. As the character typed is an "R", the flow proceeds to the right from CHAR: R to = R and is picked up again on sheet 2. The program then builds channel and unit mask words, and builds: RPT, RCAT, RCET, RCZT, RCIT, RALC, and RDIS (Read Paper Tape, Channel Active Test, Channel Error Test, Channel Zero Count Test, Channel Inter-Record Test, Alert Channel, and Disconnect Channel, respectively). The EOM/EOD commands are then constructed and the keyboard addressed to determine if the letter "S" has been inserted to start the test. The program returns to sheet 1, KYBD, where the keyboard is addressed, the character "S" is read and Breakpoint Switch 3 is interrogated. As Breakpoint Switch 3 is set (paragraph 5.7d) the line S is followed to IN.

5.9 The program proceeds to sheet 8 (circle labeled IN), the tape is started, IOSD 64 is loaded (block 1), a check is made to determine if the count reaches zero and the channel is inactive. As the count has reached zero and the channel is not active, the program then proceeds to check the data as given on sheet 12. The subroutine is then performed to check End Address, Parity, and Input Data. The block number is then saved, no error exists, the channel address is stored and checked against the expected and the input data is compared. As the input data does compare, the program exits from the subroutine and is picked back up again on sheet 8 and proceeds to IN 1.

5.10 IN 1 continues on sheet 9, the tape is started again and IOSP 65 is loaded (block 2). The program checks that the word count does not reach zero and the inter-record test occurs (CIT). It then proceeds from CIT? to IN 2.

5.11 The program then checks to determine if an error exists (sheet 10) and stops the tape before the data is checked. While the tape is stopped, the data check subroutine is performed (sheet 12). After comparison of the data, block no. 2 is entered and the program exists from the subroutine and proceeds (sheet 10) to start the tape (sheet 13) and then loads IOSP 32 (block 3).

5.12 Subsequent to loading IOSP, the subroutine Wait For Count Zero (sheet 6) is again performed. When the count equals zero, the program exits from the subroutine and returns to the main program (sheet 10). As no error existed and the channel is not active, the tape is started again (sheet 13) and IORP 33 is loaded, SPF is reset, and the inter-record indicator (CIT, sheet 9) is turned on at the end of the record. The count should not reach zero and the channel should remain active. As no error exists (sheet 10), the tape is stopped and SPF is interrogated. SPF has been reset and the program then continues to IN 3 (sheet 11). The data is then checked (sheet 12) and as it does compare, the program exits from the subroutine, block no. 3 is entered, and the tape is started again (sheet 11). The program then loads IORD 56 (block 4), waits for the channel to be inactive and checks to determine if the channel ignored the last eight characters. As the last eight words were not ignored (paragraph 5.7f), an error exists and the program

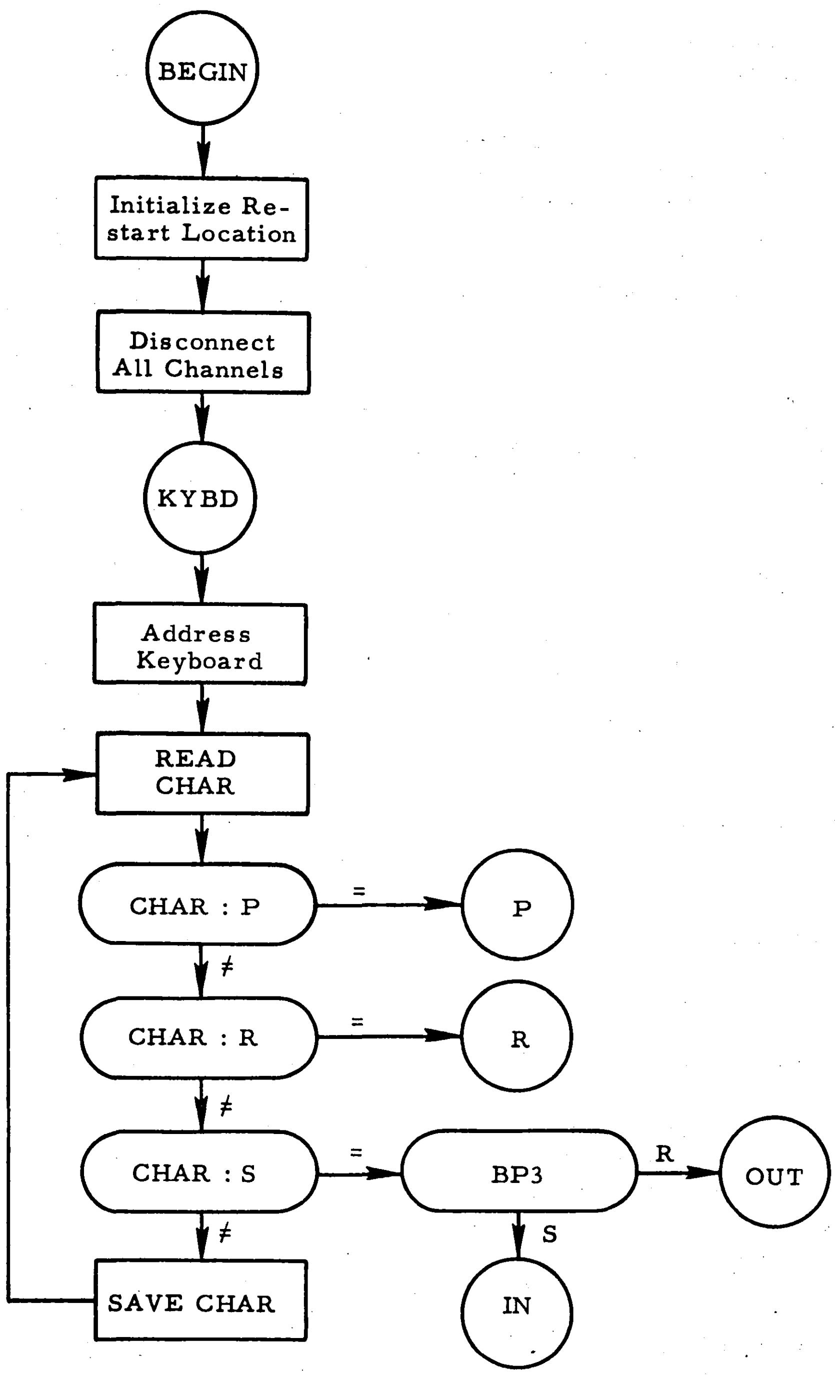


Figure 5-1. Test Program Flow Chart (Sheet 1 of 13)

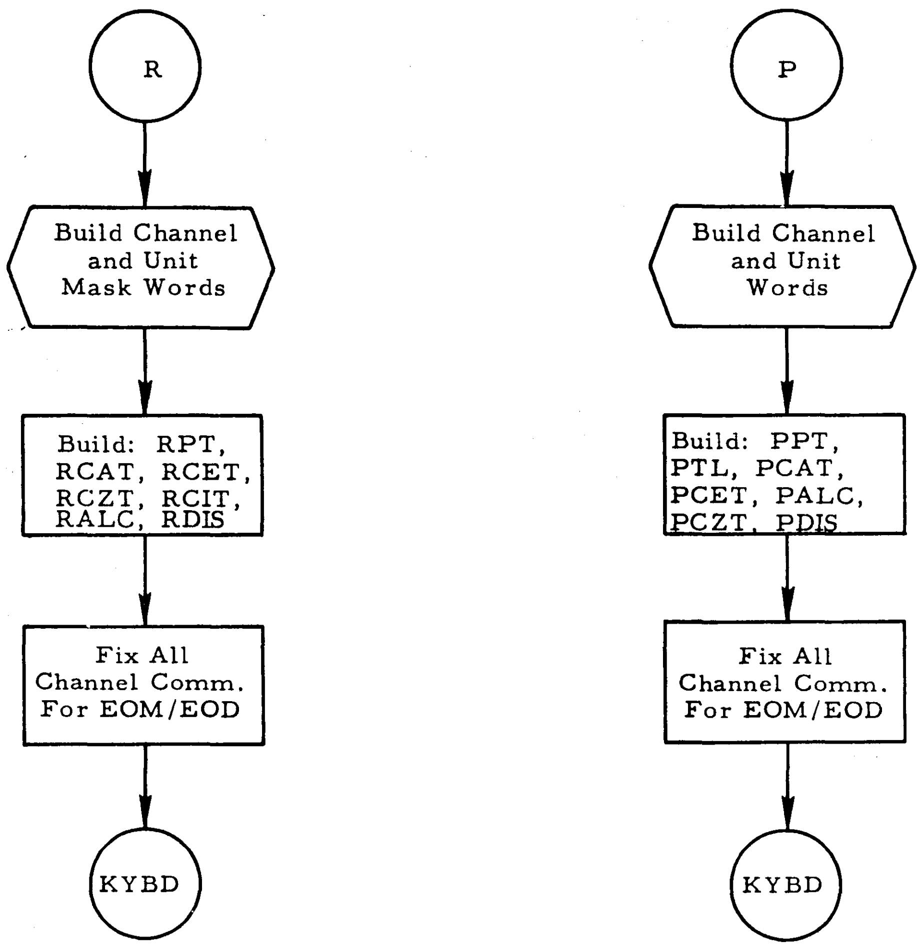


Figure 5-1. Test Program Flow Chart (Sheet 2 of 13)

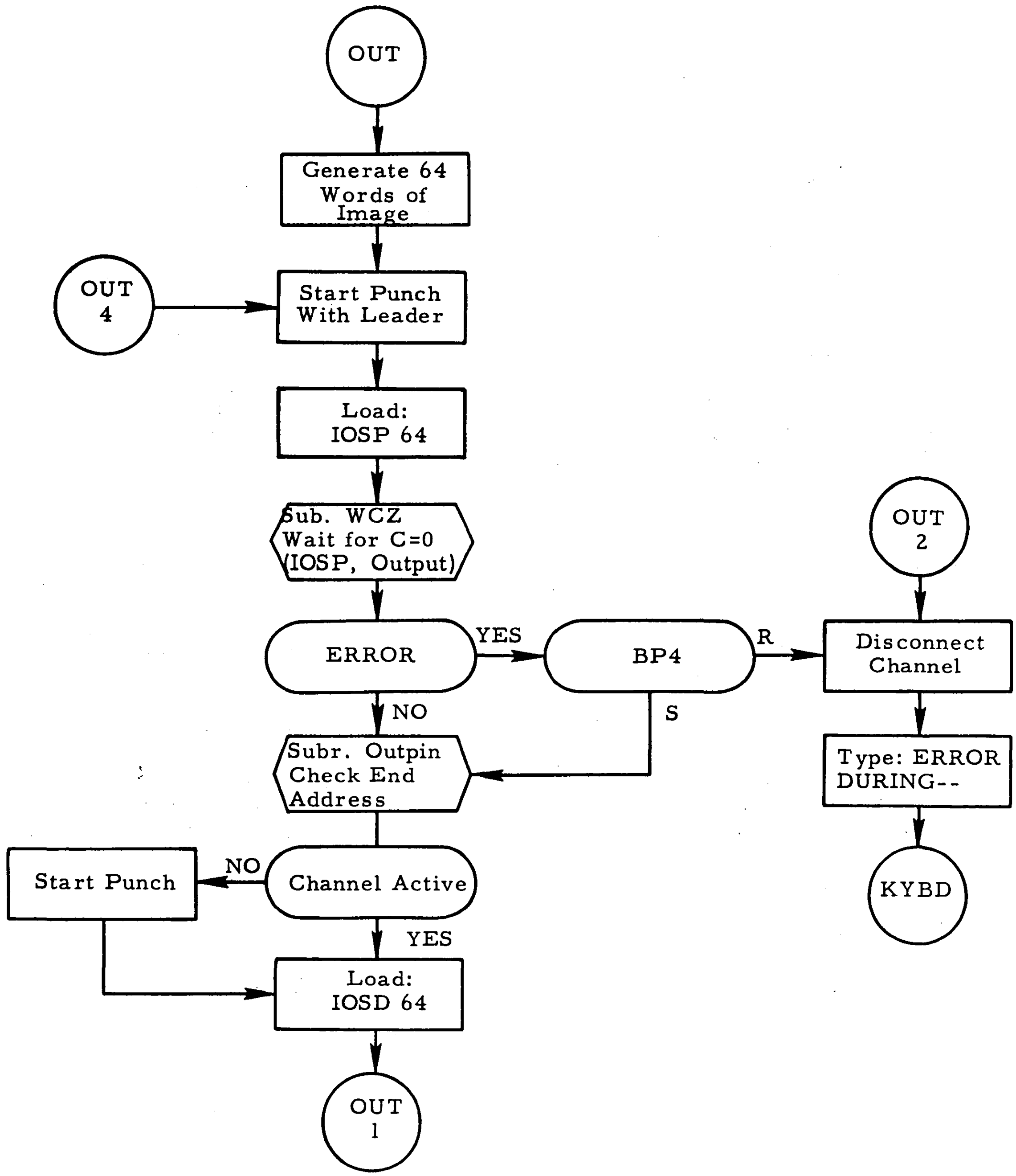


Figure 5-1. Test Program Flow Chart (Sheet 3 of 13)

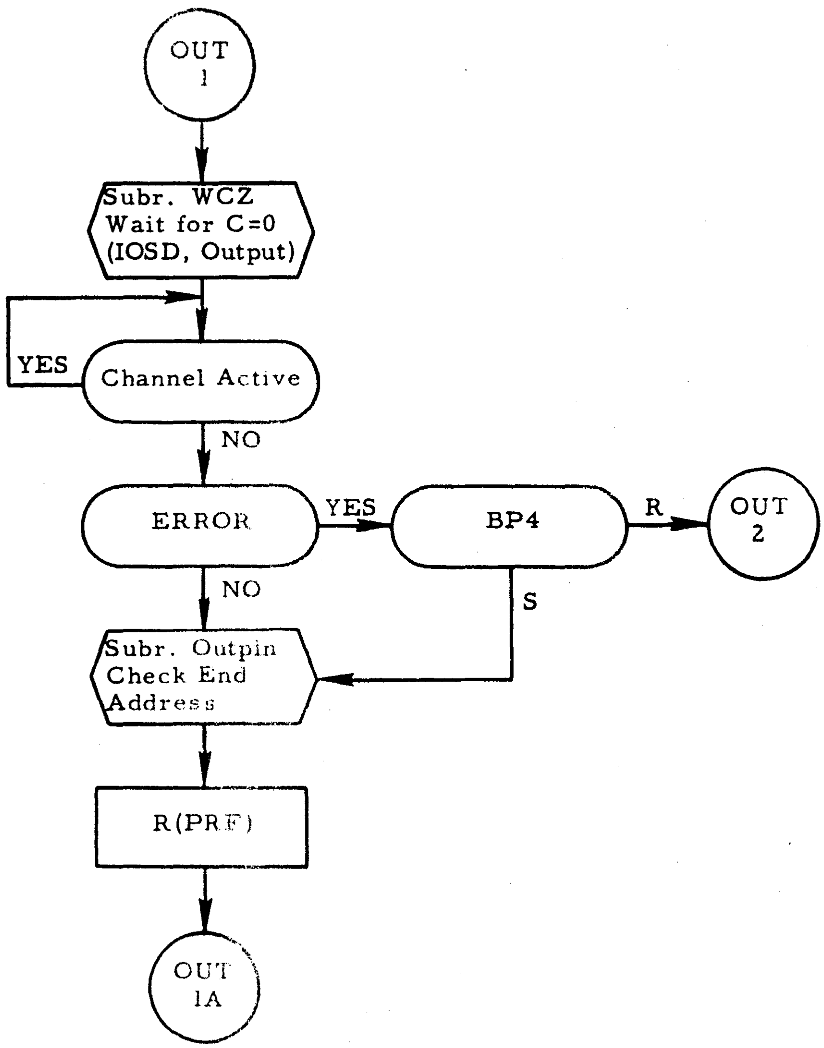


Figure 5-1. Test Program Flow Chart (Sheet 4 of 13)

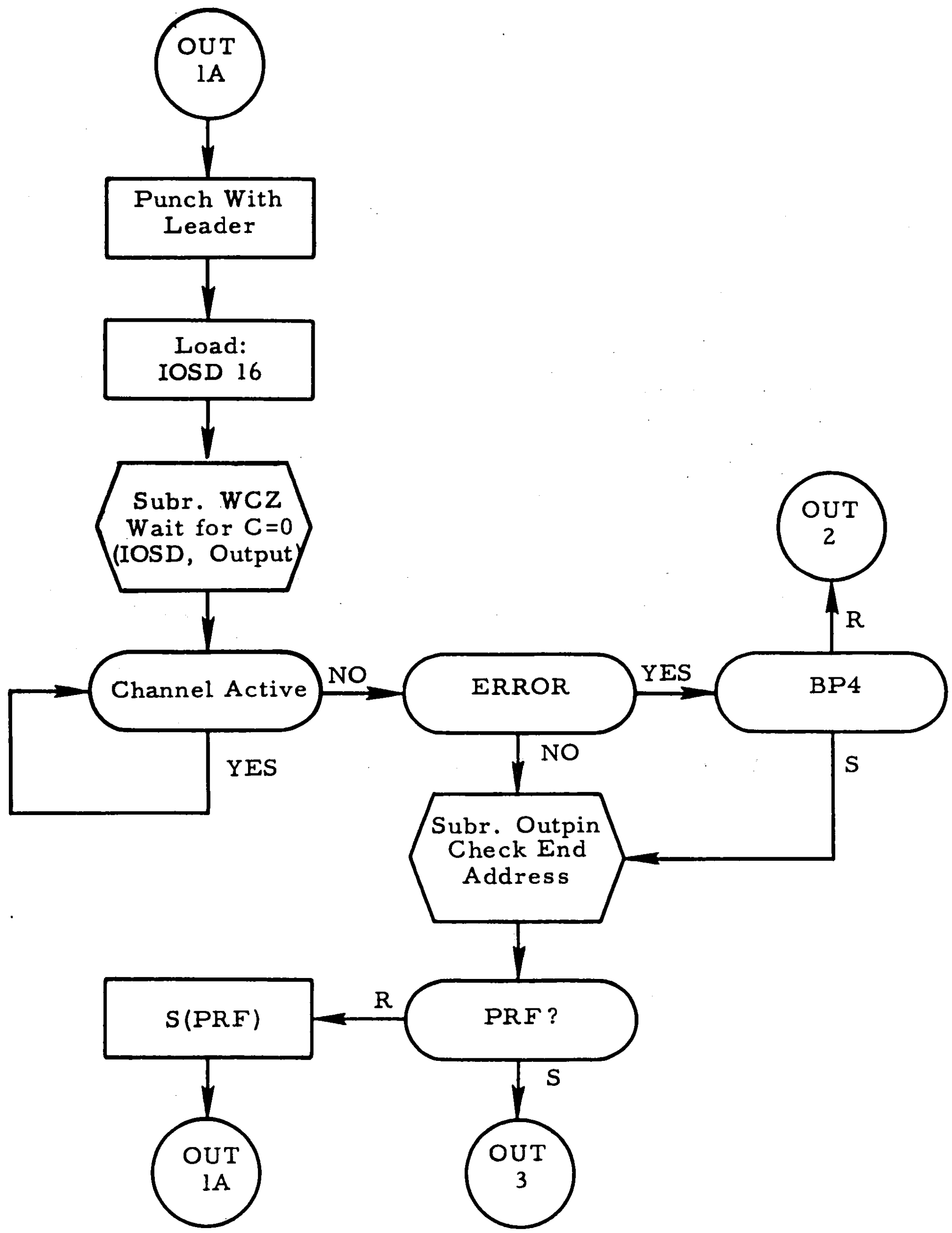


Figure 5-1. Test Program Flow Chart (Sheet 5 of 13)

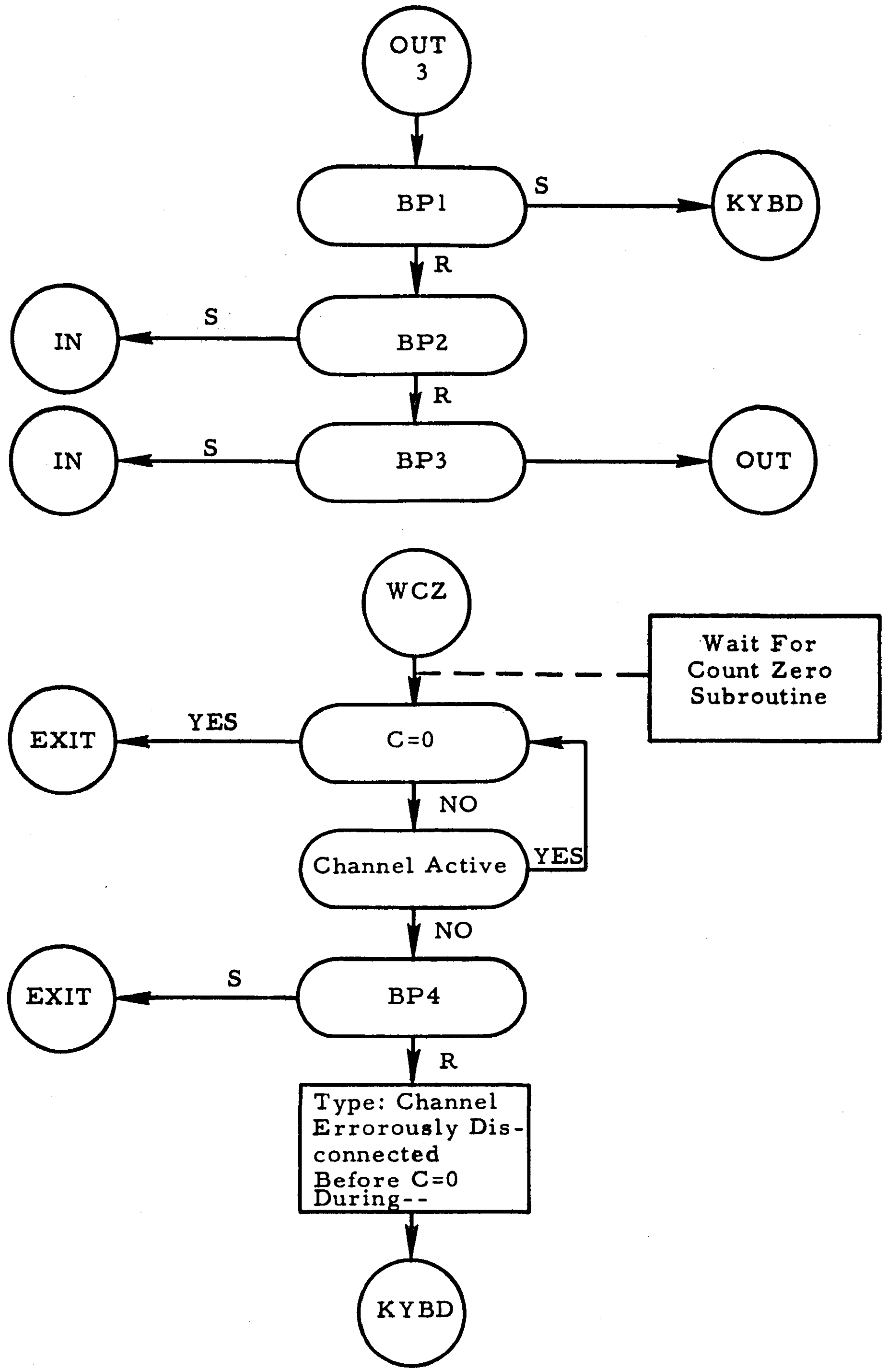


Figure 5-1. Test Program Flow Chart (Sheet 6 of 13)

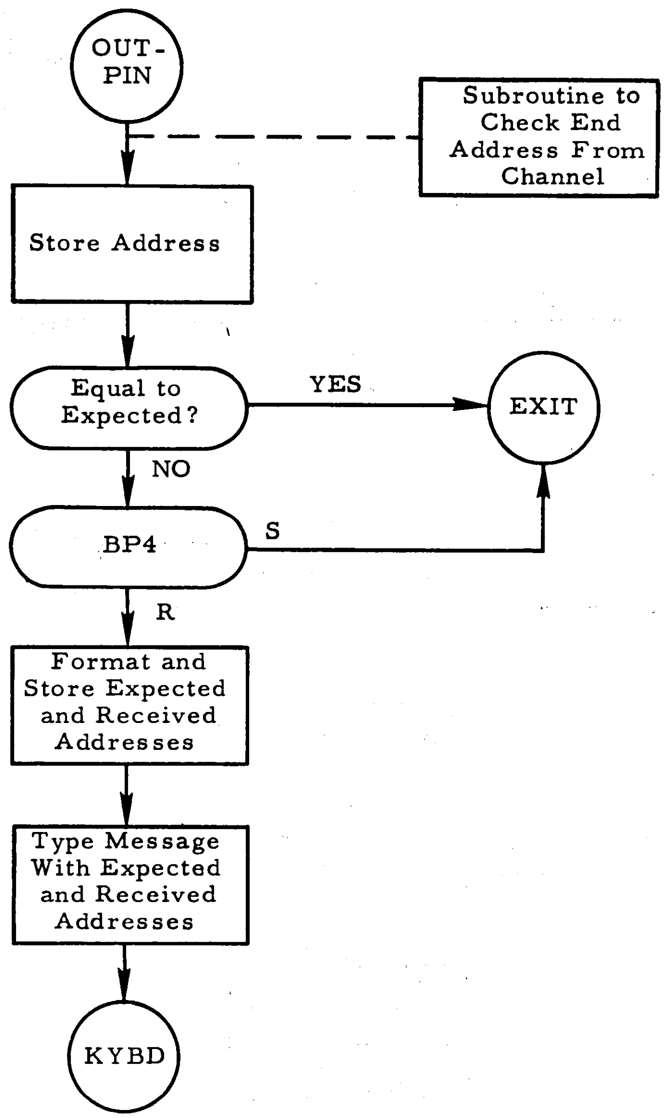


Figure 5-1. Test Program Flow Chart (Sheet 7 of 13)

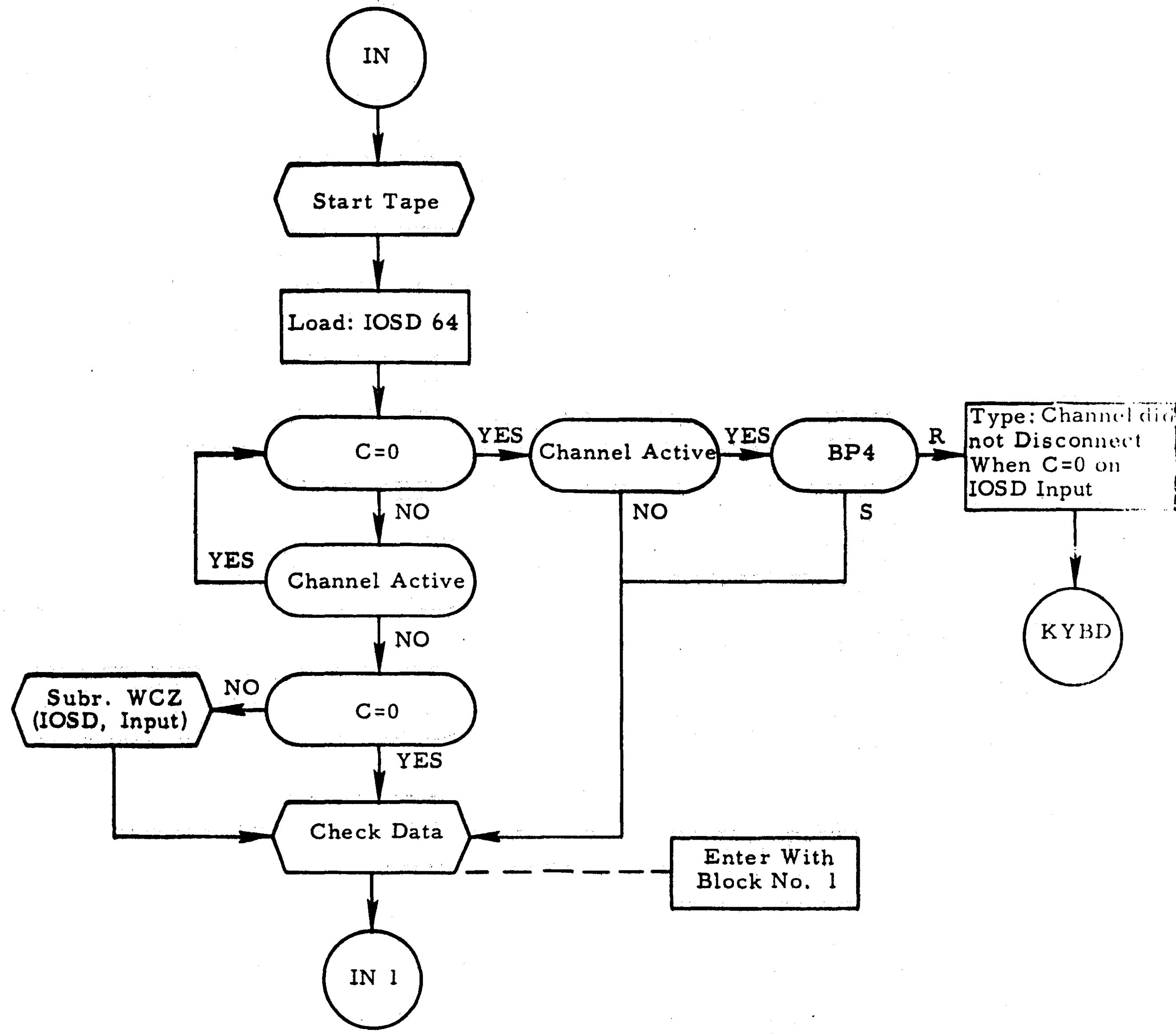


Figure 5-1. Test Program Flow Chart (Sheet 8 of 13)

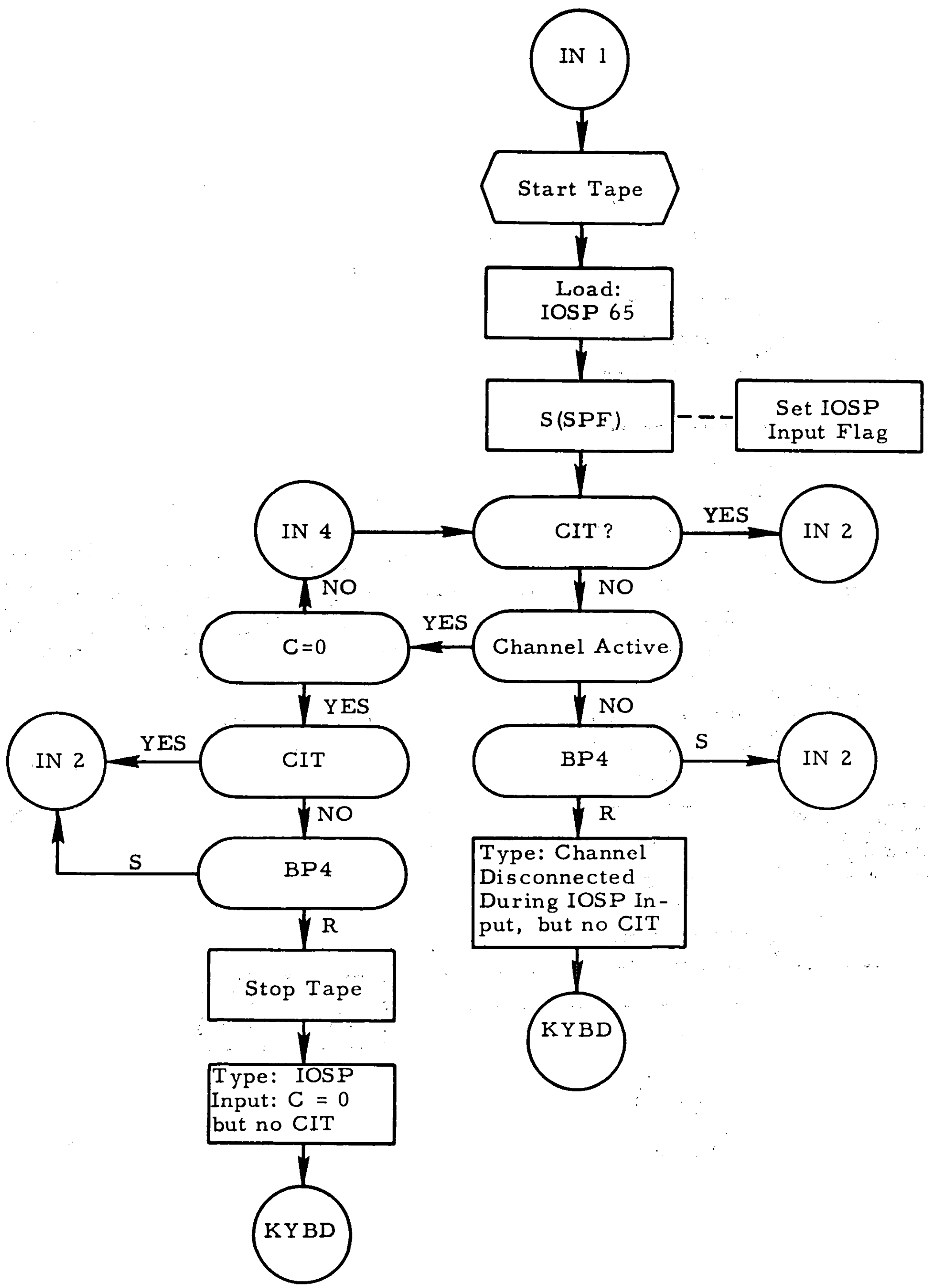


Figure 5-1. Test Program Flow Chart (Sheet 9 of 13)

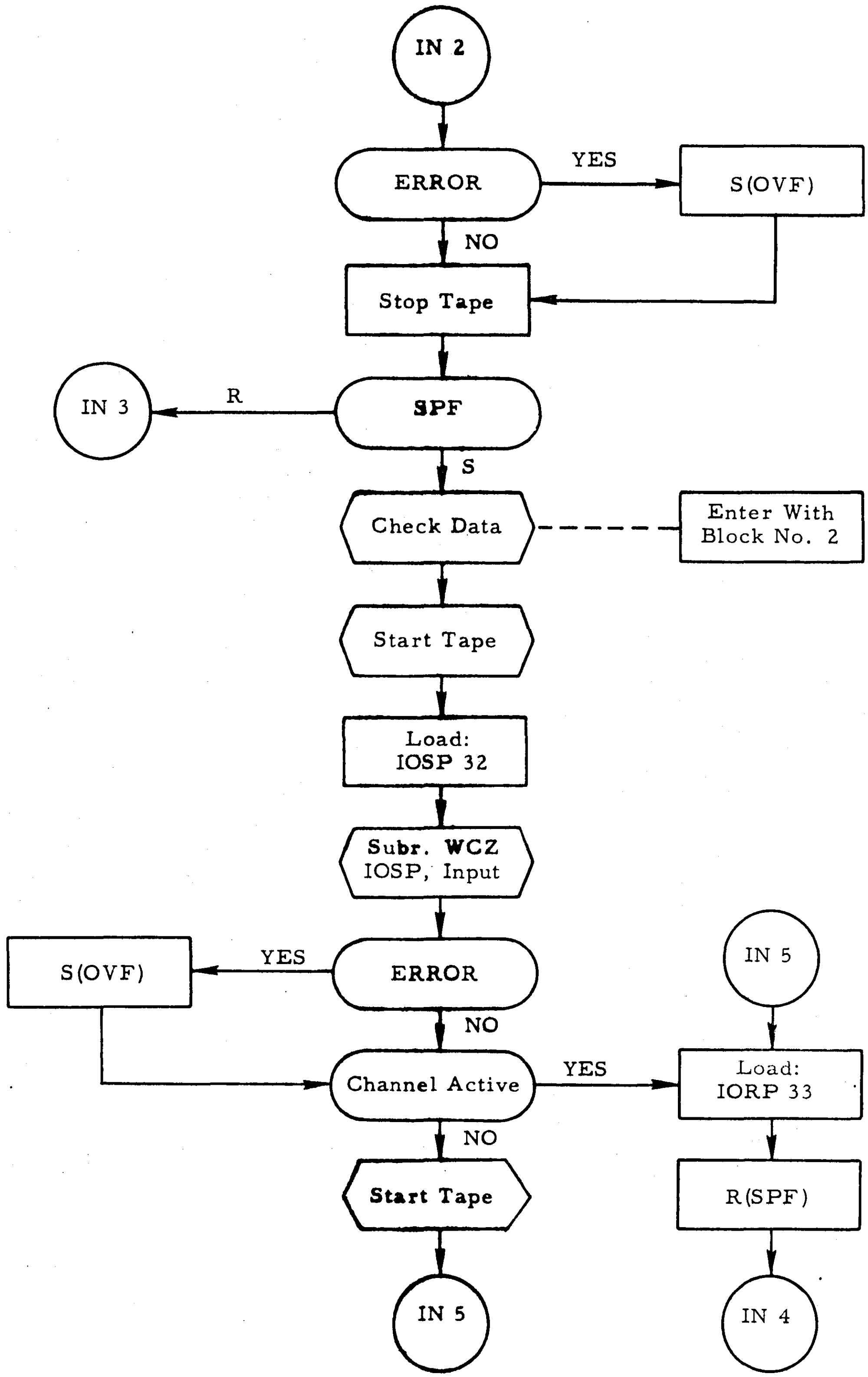


Figure 5-1. Test Program Flow Chart (Sheet 10 of 13)

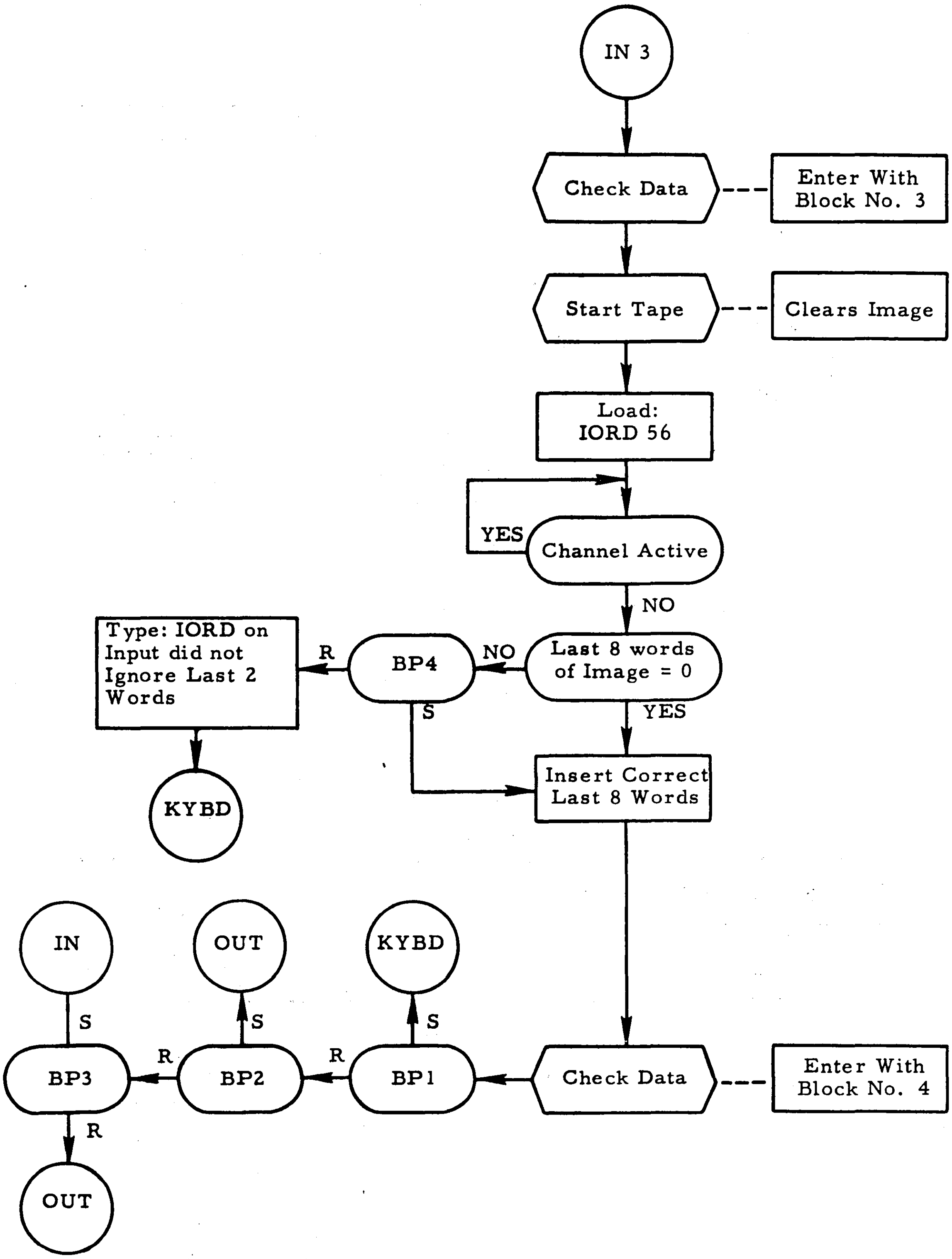


Figure 5-1. Test Program Flow Chart (Sheet 11 of 13)

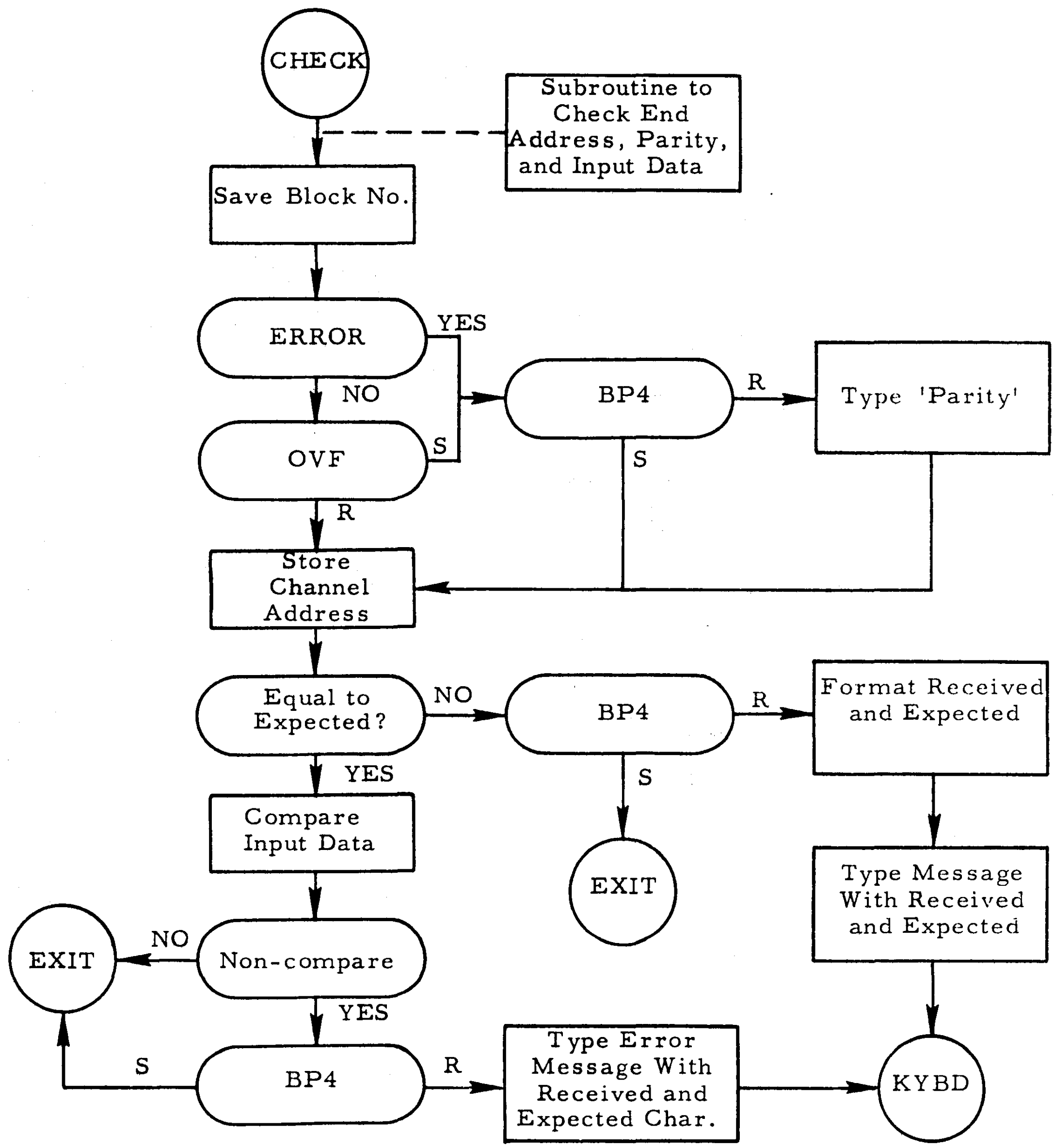


Figure 5-1. Test Program Flow Chart (Sheet 12 of 13)

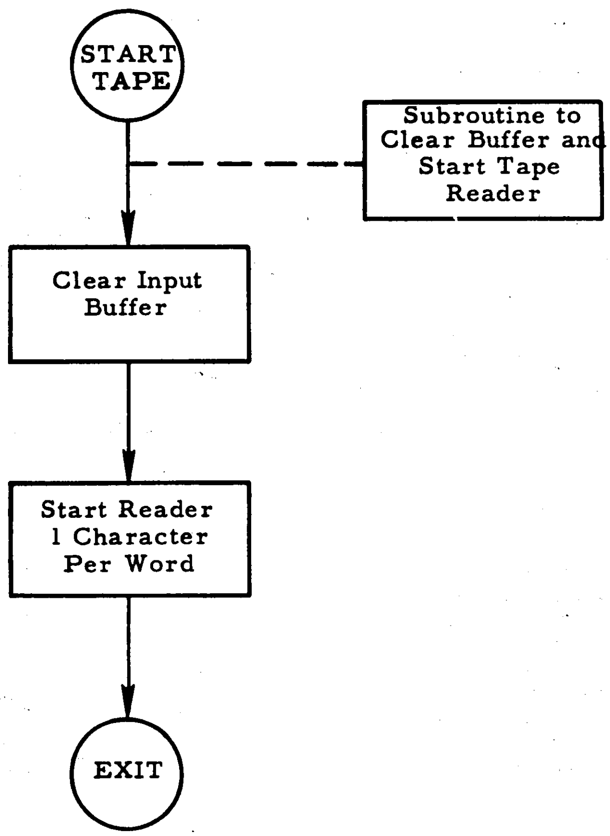


Figure 5-1. Test Program Flow Chart (Sheet 13 of 13)

interrogates Breakpoint Switch 4. Breakpoint Switch 4 is reset (paragraph 5. 7e), therefore, the program types out: IORD on Input did not ignore last two words. Reference should then be made to table 5-8 for information concerning IORD on Input.

5. 13 TROUBLESHOOTING INFORMATION

5. 14 The error printout during the test program is determined by the type of device used with the program. If the device is an output device, the following type of error codes may be printed out:

a. Typewriter -- Error during IOSD output

b. Paper Tape -- Error during IORD/IOSD output

c. Cards -- Error during IOSD/IORD output

d. Printer -- Error during IOSD/IORD output

e. Magnetic Tape -- Error during IORD/IORP output.

5. 15 If the device is an input device, the following types types of error codes may be printed out:

a. Typewriter -- Error during IOSD input

b. Paper Tape -- Error during IORD/IOSD/IORP input

c. Cards -- Error during IORD/IOSD input

d. Magnetic Tape -- Error during IORD/IORP input.

5. 16 TROUBLESHOOTING

5. 17 If a failure occurs during performance of the test program and an error message is printed out, determination must be made whether the malfunction is in the central processor unit (CPU), in the input/output device, or in the TMCC. Normally, this can be determined by performing a portion of the applicable test routine for the input/output device and checking for proper operation.

5. 18 If the determination is made that the malfunction is in the TMCC, reference should then be made to the applicable table (tables 5-1 thru 5-10) for that function. The table describes the function and references the paragraphs in the Theory of Operation section (Section 3) where a detailed description of that function is described.

5. 19 The logic equations pertaining to the particular function can be determined from the description in the theory of operations. A comparison of the logic equations and terms will indicate the particular terms peculiar to the function which has failed. Reference to the logic layout drawings (listed in Section 1) will indicate the module in which the term is used, the physical location of the module, and the terminal connections where the term can then be found.

5.20 Normal troubleshooting procedures can be performed to pinpoint the malfunction to a particular component or terminal.

5.21 Physical location of components and schematics of each module can be found in Section 6.

Table 5-1. IOSP Output Function, W (A) Channel

Iwg	Iwh	Iwi	Output Function	Sec. 3, Par. Ref.
1	1	1	1. I1w at Iwf if Iwk When the channel counts C down to zero (Iwf), the channel generates a zero word count interrupt (I1w), if armed (Iwk), indicating the program should reload the interlace portion of the channel to continue writing in the same record. Failure to reload the interlace before the buffer transmits all of the characters in its registers and before the peripheral device requests the next character from the buffer sets the channel error indicator.	3. 152 thru 3. 157

Table 5-2. IORP Output Function, W (A) Channel

Iwg	Iwh	Iwi	Output Function	Sec. 3, Par. Ref.
1	1	0	1. I1w at Iwf if Iwk 2. At Iwf, reset W0 3. I2w at Mtgw or Whs W11 if Iwj 4. At Whs W11, disconnect When the channel interlace counts C down to zero (Iwf), the channel generates a zero word count interrupt (I1w), if armed (Iwk), notifying the channel buffer that it has received the last word that is to be output. At zero word count (Iwf), the Halt Interlock flip-flop, W0, is reset to inhibit additional time-share requests. When the device receives the last word from the buffer, it sends an End-of-Record response (Whs W11) back to the buffer. If armed, (Iwj), the buffer generates an End-of-Record Interrupt (I2w) and sets the inter-record indicator. If the device is magnetic tape, an End-of-Record response (tape gap signal, Mtgw,) signal is sent to the buffer but the tape continues to move. If the program does not execute an EOM to write a new tape before the tape gap signal drops, the channel disconnects (Whs W11) and the tape stops.	3.144 thru 3.151

Table 5-3. IOSD Output Function, W (A) Channel

Iwg	Iwh	Iwi	Output Function	Sec. 3, Par. Ref.
1	0	1	1. I1w at Iwf if Iwk 2. At Iwf, reset W0 3. Disconnect at Iwf W11 or Whs 4. I2w at disconnect, if Iwj When the channel interlace counts C down to zero (Iwf), the channel generates a zero word count interrupt (I1w), if armed (Iwk), indicating the last character has been transmitted. At zero word count (Iwf), the Halt Interlock flip-flop (W0) is reset inhibiting additional time-share requests. For devices other than magnetic tape (W11), the Halt Detector flip-flop (Wh) is set on reaching zero word count (Iwf) when the last character has been clocked from the buffer. The Halt Detector also sets on occurrence of a Halt Signal (Whs). Setting of the Halt Detector initiates a buffer disconnect sequence. The Signal Complete flip-flop (Wcs) is set and if the End-of-Record Interrupt Enable (Iwj) has been previously armed, an End-of-Record Interrupt (I2w) is generated.	3.140 thru 3.143

Table 5-4. IORD Output Function, W (A) Channel

Iwg	Iwh	Iwi	Output Function	Sec. 3, Par. Ref.
1	0	0	1. I1w at Iwf if Iwk 2. At Iwf, reset W0 3. Disconnect at Whs 4. I2w at disconnect, if Iwj When the channel counts C down to zero (Iwf), the channel generates a zero word count interrupt (I1w), if armed (Iwk), indicating that the last characters have been transmitted. At zero word count (Iwf), the Halt Interlock flip-flop (W0) is reset inhibiting additional time-share requests. If Halt Signal (Whs) is received, the Halt Detector (Wh) is set and a disconnect occurs. The Signal Complete flip-flop (Wsc) is set and, if armed (Iwj), an End-of-Record Interrupt (I2w) is generated.	3. 134 thru 3. 139

Table 5-5. IOSP Input Function, W (A) Channel

Iwg	Iwh	Iwi	Input Function	Sec. 3, Par. Ref.
1	1	1	1. I1w at Iwf if Iwk 2. At Mtgw or Whs W11, flush and store last character(s) if Iwf 3. I2w at Mtgw or Whs W11 if Iwj 4. Disconnect at Whs W11 When the channel counts C down to zero (Iwf), the channel generates a zero word count interrupt (I1w), if armed (Iwk), indicating the program should reload the interlace portion of the channel to continue reading the record. If the End-of-Record (Mtg or Whs W11) occurs before zero word count (Iwf), the buffer is flushed and the completed word is stored in memory. If the End-of-Record Interrupt Enable (Iwj) has been armed, an End-of-Record interrupt (I2w) is generated when a tape gap (Mtgw) or halt signal (Whs) is detected from the device. For magnetic tape operation (W11), a new EOM may be given within one millisecond from the occurrence of I2w to permit the tape system to proceed to a new record. Failure to give an EOM results in the tape stopping and the buffer disconnecting.	3. 176 thru 3. 179

Table 5-6. IORP Input Function, W (A) Channel

Iwg	Iwh	Iwi	Input Function	Sec. 3, Par. Ref.
1	1	0	1. I1w at Iwf if Iwk 2. Inhibit rate errors if Iwf 3. At Mtgw or Whs W11, flush and store last character(s) if Iwf 4. I2w at Mtgw or Whs W11 if Iwj 5. Disconnect at Whs W11 When the channel counts C down to zero (Iwf), the channel generates a zero word count interrupt (I1w), if armed (Iwk), indicating the program should reload the interlace portion of the channel to continue reading the record. Additional characters entering the channel after zero word count are precessed into the W register. Parity and rate errors cannot occur after zero word count because of Iwf. Detection of magnetic tape gap (Mtgw) or a halt signal (Whs) sets the End-of-Record detector. If the End-of-Record detector is set before zero word count has occurred (Iwf), the buffer is flushed and the completed word is stored in memory. If the End-of-Record Interrupt Enable (Iwj) has been armed, an End-of-Record interrupt (I2w) occurs. Failure to reload the interlace within one millisecond of I2w results in the tape stopping and the buffer disconnecting.	3.168 thru 3.175

Table 5-7. IOSD Input Function, W (A) Channel

Iwg	Iwh	Iwi	Input Function	Sec. 3, Par. Ref.
1	0	1	1. I1w at Iwf if Iwk 2. At Whs, flush and store last character(s) if Iwf 3. Disconnect at Iwf W11 or Whs 4. I2w at disconnect if Iwj When the channel counts C down to zero (Iwf), the channel generates a zero word count interrupt (I1w), if armed (Iwk). Should an End-of-Record (Whs) occur before zero word count (Iwf) is established, any characters remaining in the W register are flushed and stored. The Halt Detector is now permitted to set by Iwf W11 or Whs W11 and the channel is disconnected. If the End-of-Record Interrupt Enable (Iwj) has been armed, an End-of-Record interrupt (I2w) occurs.	3.164 thru 3.167

Table 5-8. IORD Input Function, W (A) Channel

Iwg	Iwh	Iwi	Input Function	Sec. 3, Par. Ref.
1	0	0	1. I1w at Iwf if Iwk 2. Inhibit rate errors if Iwf 3. At Mtgw or Whs W11, flush and store last character(s) if Iwf 4. Disconnect at Whs 5. I2w at disconnect if Iwj When the channel counts C down to zero (Iwf), the channel generates a zero word count interrupt (I1w), if armed (Iwk). Parity and rate errors (We) are inhibited by Iwf after zero word count is established. Should an End-of-Record (Mtgw or Whs W11) occur before zero word count is established (Iwf), the End-of-Record detector is set and any characters remaining in the W register are flushed and stored. The Halt Detector (Wh) is permitted to set by Whs, the buffer is cleared and the channel disconnected. If the End-of-Record Interrupt Enable (Iwj) has been armed, an End-of-Record interrupt (2w) occurs.	3.158 thru 3.163

Table 5-9. Output Functions, Y Channel

Iyg	Iyh	Iyi	Output Function	Sec. 3, Par. Ref.
1	1	1	IOSP 1. I1y at Iyf if Iyk	3.152 thru 3.157
1	1	0	IORP 1. I1y at Iyf if Iyk 2. At Iyf, reset Y0 3. I2y at Mtgy or Yhs Y11 if Iyj 4. At Yhs Y11, disconnect	3.144 thru 3.151
1	0	1	IOSD 1. I1y at Iyf if Iyk 2. At Iyf, reset Y0 3. Disconnect at Iyf Y11 or Yhs 4. I2y at disconnect, if Iyj	3.140 thru 3.143
1	0	0	IORD 1. I1y at Iyf if Iyk 2. At Iyf, reset Y0 3. Disconnect at Yhs 4. I2y at disconnect, if Iyj	3.134 thru 3.139
			The output functions for the Y channel are identical to those of the W channel given in tables 5-1, 5-2, 5-3, and 5-4. The only difference is the substitution of the letter "y" for "w" in the logic terms.	

Table 5-10. Input Functions, Y Channel

Iyg	Iyh	Iyi	Input Functions	Sec. 3, Par. Ref.
1	1	1	IOSP 1. I1y at Iyf if Iyk 2. At Mtgy or Yhs Y11, flush and store last character(s) if Iyf 3. I2y at Mtgy or Yhs Y11 if Iyj 4. Disconnect at Yhs Y11	3.176 thru 3.179
1	1	0	IORP 1. I1y at Iyf if Iyk 2. Inhibit rate errors if Iyf 3. At Mtgy or Yhs Y11, flush and store last character(s) if Iyf 4. I2y at Mtgy or Yhs Y11 if Iyj 5. Disconnect at Yhs Y11	3.168 thru 3.175
1	0	1	IOSD 1. I1y at Iyf if Iyk 2. At Yhs, flush and store last character(s) if Iyf 3. Disconnect at Iyf Y11 or Yhs 4. I2y at disconnect if Iyj	3.164 thru 3.167
1	0	0	IORD 1. I1y at Iyf if Iyk 2. Inhibit rate errors if Iyf 3. At Mtgy or Yhs Y11, flush and store last character(s) if Iyf 4. Disconnect at Yhs 5. I2y at disconnect if Iyj	3.158 thru 3.163
			The input functions for the Y channel are identical to those of the W channel given in tables 5-5, 5-6, 5-7, and 5-8. The only difference is the substitution of the letter "y" for "w" in the logic terms.	

SECTION VI
DRAWINGS

6.1 GENERAL

6.2 This section contains drawings useful when troubleshooting and maintaining the TMCC.

6.3 SCOPE OF SECTION

6.4 Included in this section are assembly drawings, schematic diagrams, and material lists for each module.

6.5 The type and quantity of each module are listed in Section 1, table 1-4. Physical location of each module is illustrated in Section 4, figure 4-4.

6.6 Also included in this section is the Semiconductor Cross Reference which provides a cross-reference between Scientific Data Systems semiconductor numbers, commercial Electronic Industries Association (EIA) numbers, specification numbers, and replacements for obsolete semiconductors.

103655 A

SCHEMATIC, RECEIVER INVERTER

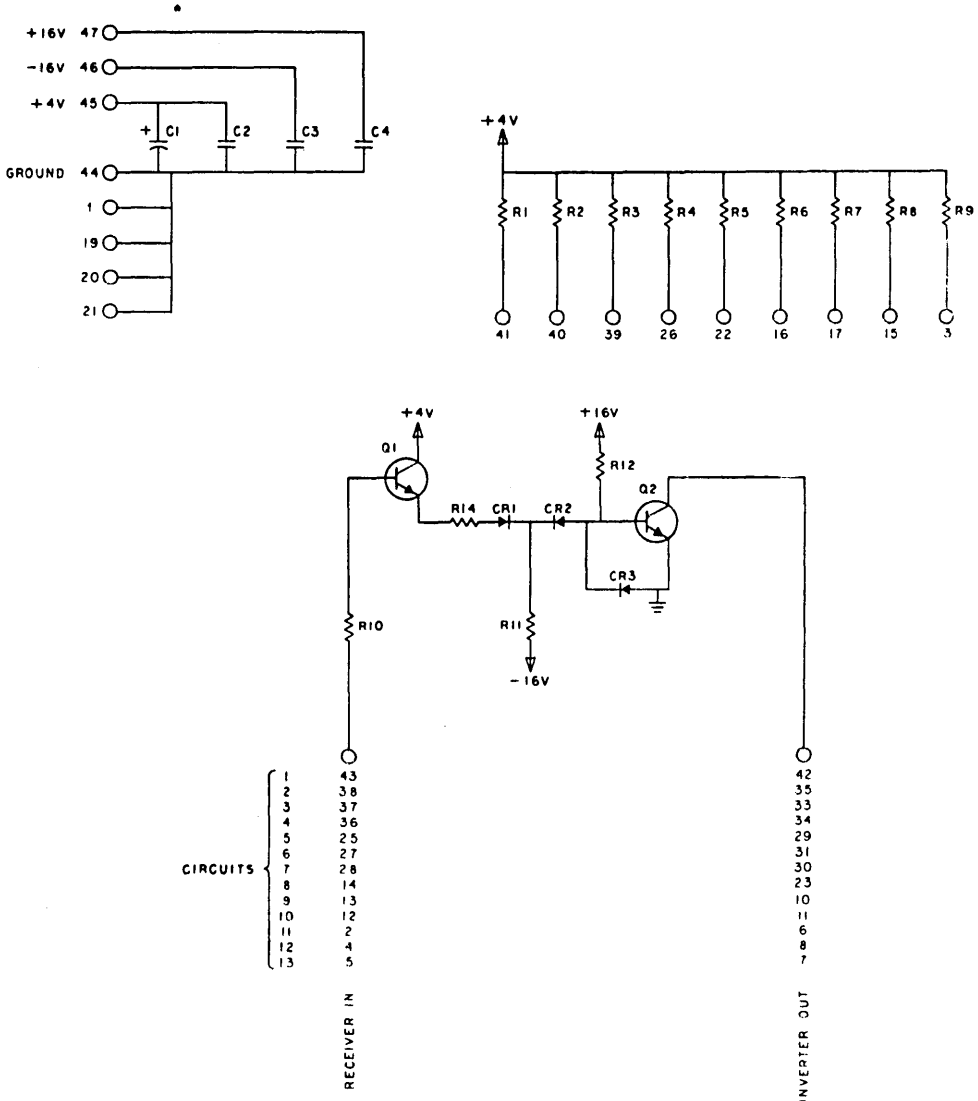
103655

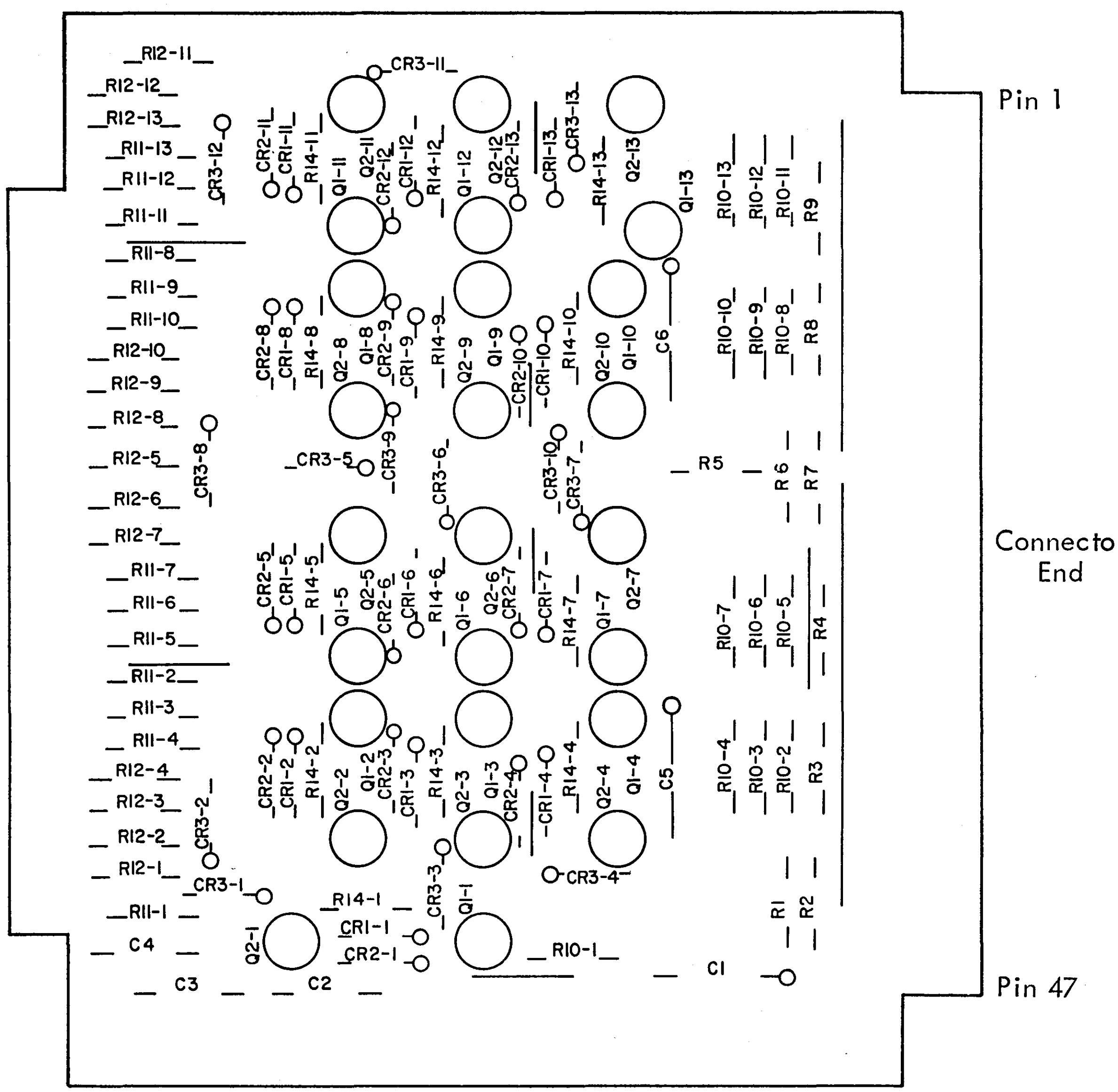
SIZE D

REV A

REVISIONS: A — RELEASED TO MFG

POLARIZING PINS: 18 & 22





Receiver Inverter AB52
103657C

REV	DWG. NO.
A	103657

ML

MATERIAL LIST
DWG. TITLE

SDS SCIENTIFIC DATA SYSTEMS

ML

DWG. NO.	REV
103657	A

ASSY. P. W. RECEIVER INVERTER MOD # AB52 DATE 1/2/4 SHEET 2 OF 2

ITEM	DWG. TITLE	DWG. NO.	NO. REQ.	REMARKS OR CKT. DESIG.
1	Board, Printed Wiring	103656	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn Upper	100097	23	
6	Contact, Conn Lower	100098	24	
7	Transistor (SDS 216)	103242	26	Q1, 2
8	Diode (SDS 103)	100091	39	CR1, 2, 3
9				
10	Capacitor, Mylar	100308-103	3	C2, 3, 4
11	Capacitor, Tantalum	100312-156	1	C1
12	Resistor, $\frac{1}{2}$ watt	100111-680	13	R14
13	Resistor, $\frac{1}{2}$ watt	100111-151	9	R1 thru R9
14	Resistor, $\frac{1}{2}$ watt	100111-221	13	R10
15	Resistor, $\frac{1}{2}$ watt	100111-122	13	R11
16	Resistor, $\frac{1}{2}$ watt	100111-272	13	R12
17	Wire, Solid Bare	100042-024	12 in	
18	Tubing, Teflon	100274-022	12 in	

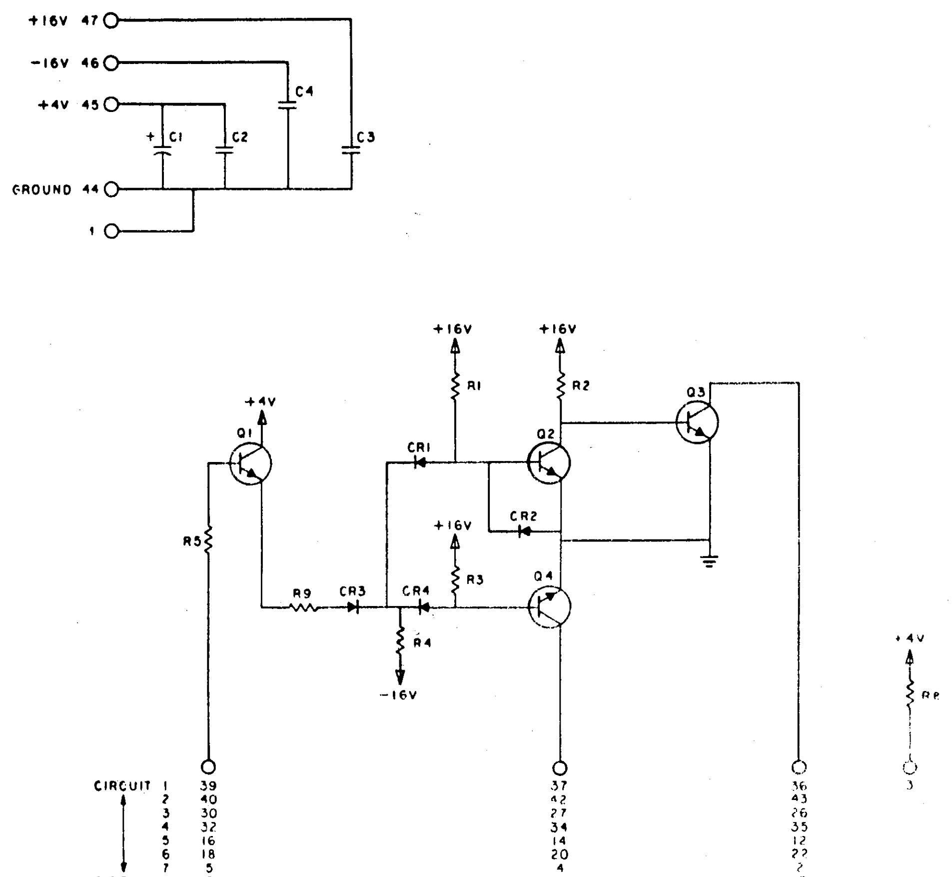
103724 A

SCHEMATIC, RECEIVER INVERTER BUFFER

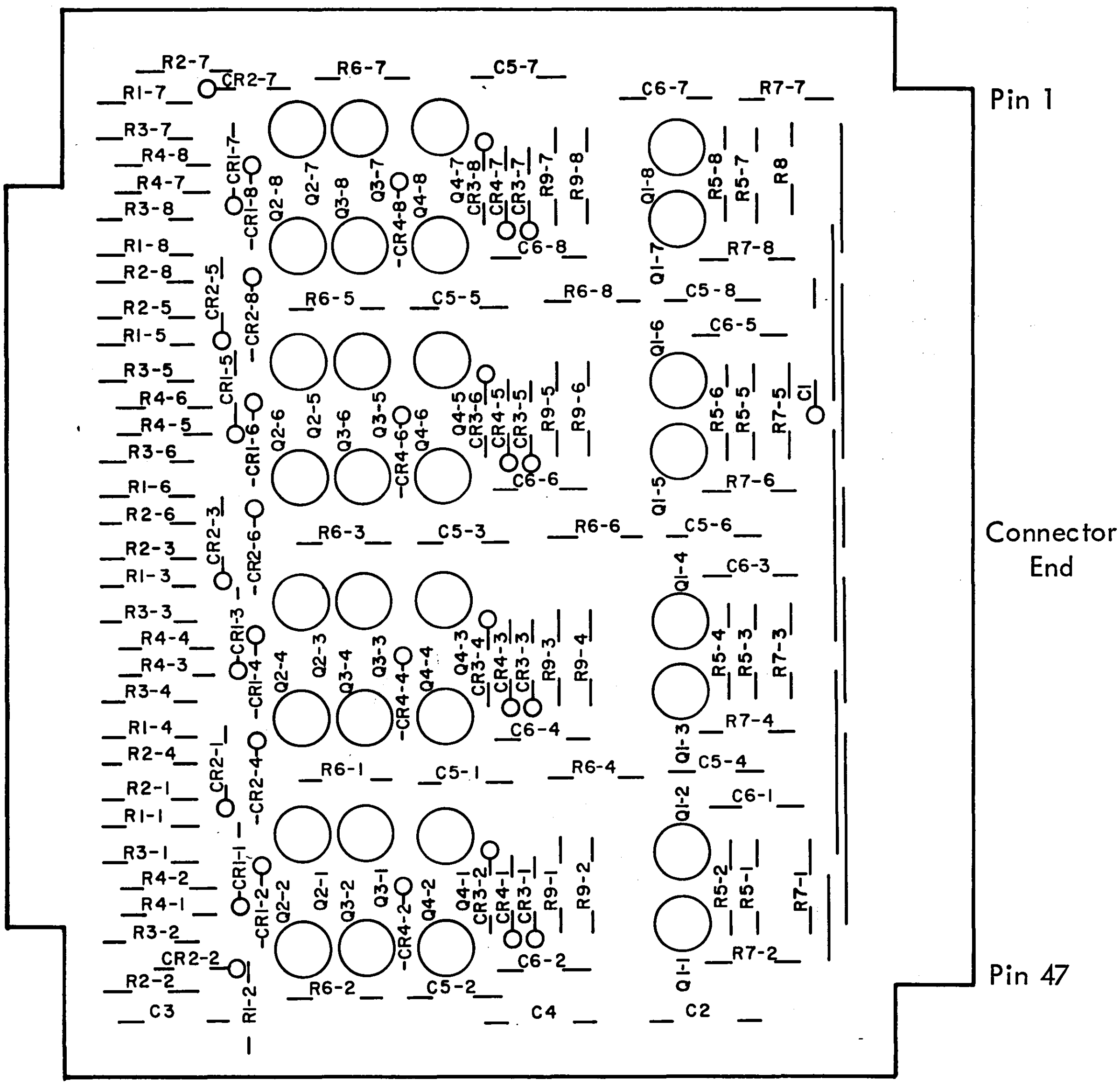
103724 A

A RELEASED TO MFG

POLARIZING PINS: 20 & 44



		Receiver In	Inverter Out	Buffer Out
CIRCUIT	1	39	37	36
	2	40	42	43
	3	30	27	26
	4	32	34	35
	5	16	14	12
	6	18	20	22
	7	5	4	2
CIRCUIT	8	6	8	10



Receiver Inverter Buffer AB53
103726A

REV A | DWG. NO 103726 | ML

MATERIAL LIST

DWG. TITLE

ASSY, P. W.

RECEIVER, INVERTER BUFFER

SDS SCIENTIFIC DATA SYSTEMS

ML | DWG. NO. 103726 | REV A

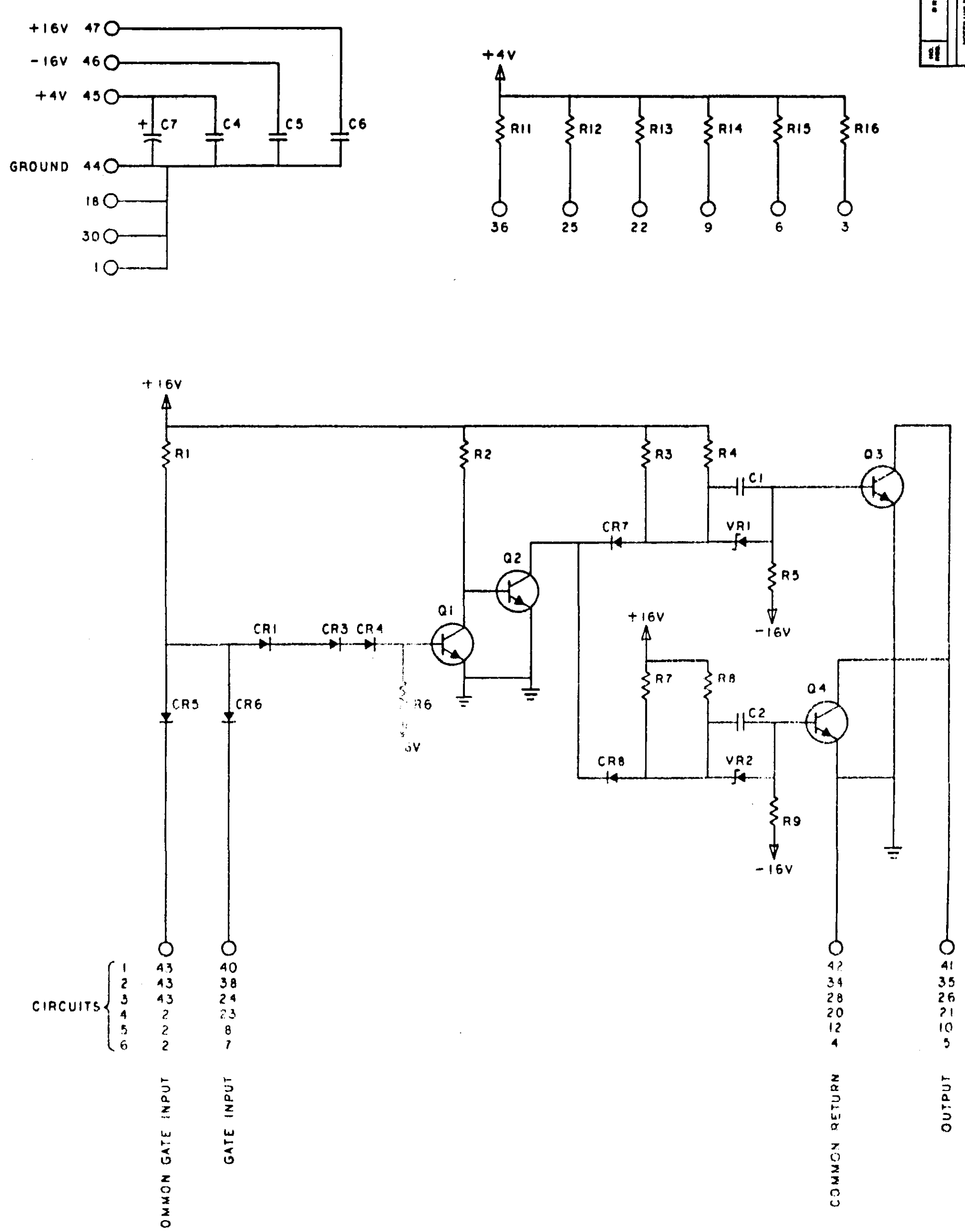
MOD # AB53 DATE 12/14 SHEET 2 OF 2

ITEM	DWG. TITLE	DWG. NO.	NO. REQ	REMARKS ON CKT, DESIG.
1	Board, Printed Wiring	103725	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn Upper	100097	23	
6	Contact, Conn Lower	100098	24	
7	Transistor, (SDS 216)	103242	32	Q1 thru Q4
8	Diode (SDS 103)	100091	32	CR1 thru CR4
9				
10	Capacitor, Mylar	100308-103	3	C2, 3, 4
11	Capacitor, Tantalum	100312-156	1	C1
12	Resistor, ½ watt	100111-680	8	R9
13	Resistor, ½ watt	100111-151	1	R8
14	Resistor, ½ watt	100111-221	8	R5
15	Resistor, ½ watt	100111-122	8	R4
16	Resistor, ½ watt	100111-302	8	R2
17	Resistor, ½ watt	100111-562	16	R1, 3
18	Wire, Solid Bare	100042-024	8½ IN.	
19	Tubing, Teflon	100274-022	8½ IN.	

104838 C

REV.	DESCRIPTION
A	RELEASED TO MFG
B	SEE REVISION E.O.
C	SEE REV E.O.

POLARIZING PINS: 32 & 46



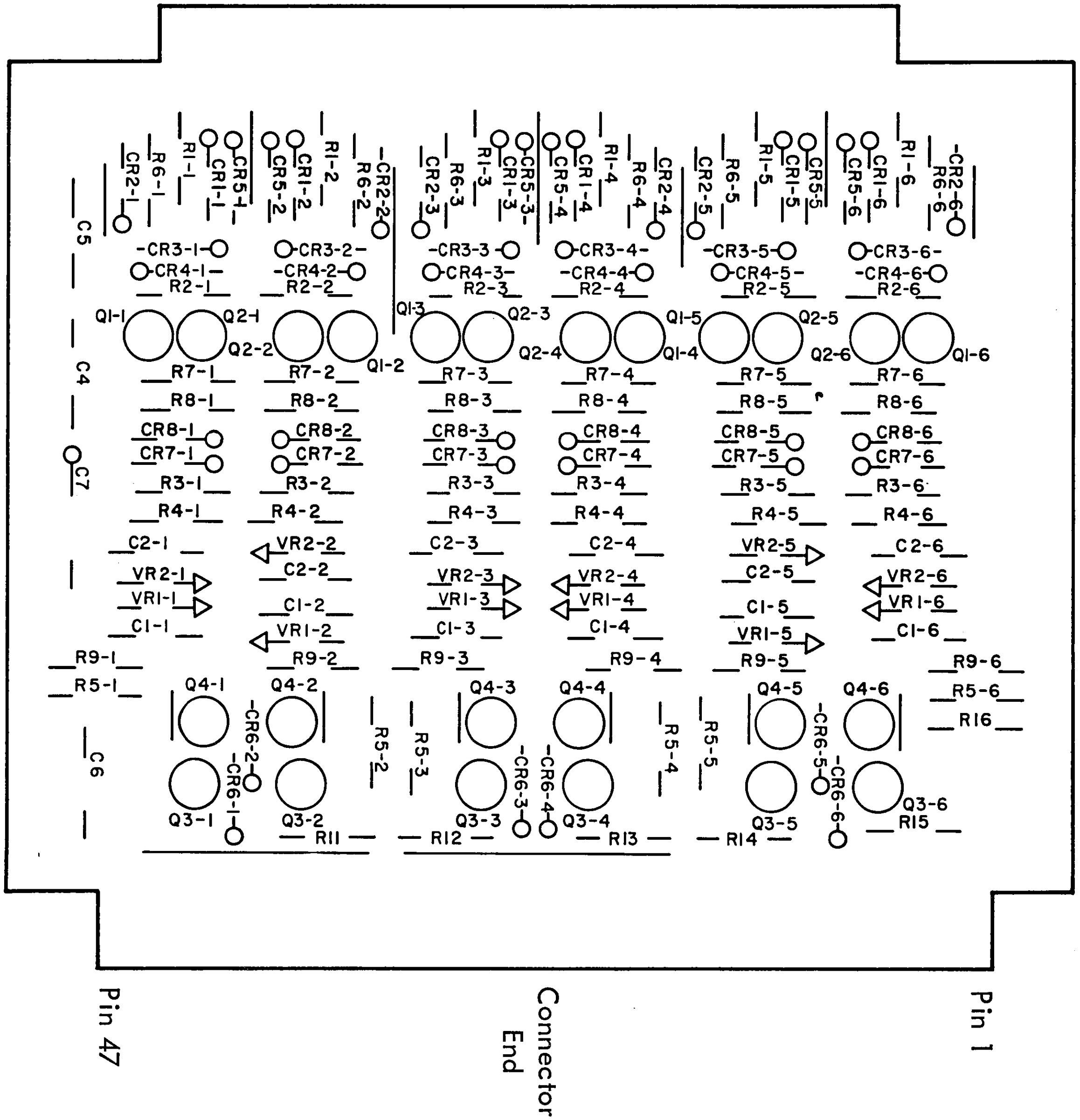
SDS

SCHEMATIC
CABLE DRIVER #2

SIZE D — DWG NO. 104838 — REV C

MODEL NO. AB55

NEXT ASSY 104840



Cable Driver No. 2 AB55
104840E

REV	E
DWG. NO.	104840

ML

MATERIAL LIST
DWG. TITLE

SDS SCIENTIFIC DATA SYSTEMS

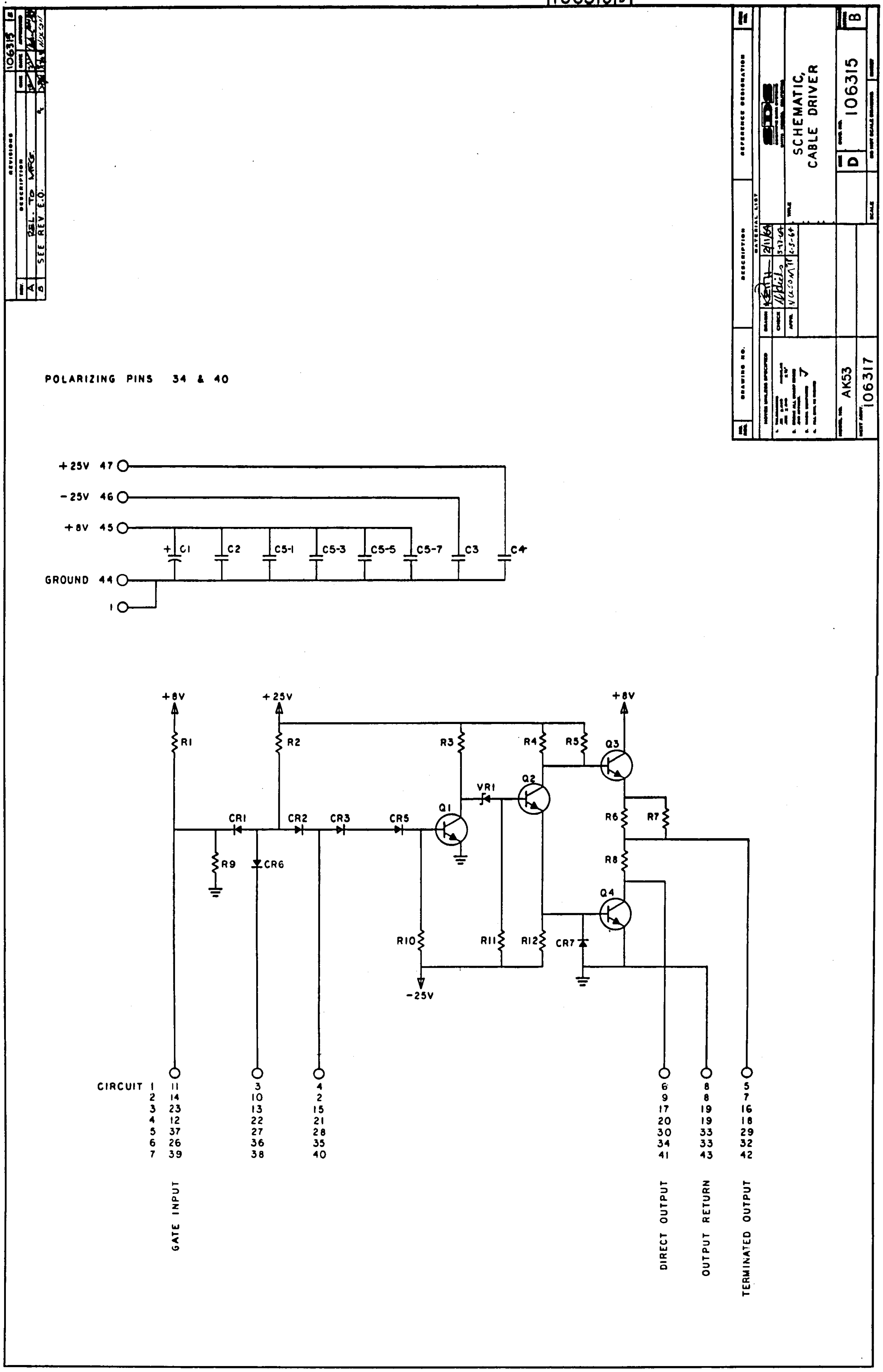
ML | DWG. NO. 104840 | REV E

ASSY. P. W. CABLE DRIVER #8 — MOD # AB55 — DATE 1/2 — SHEET 2 OF 2

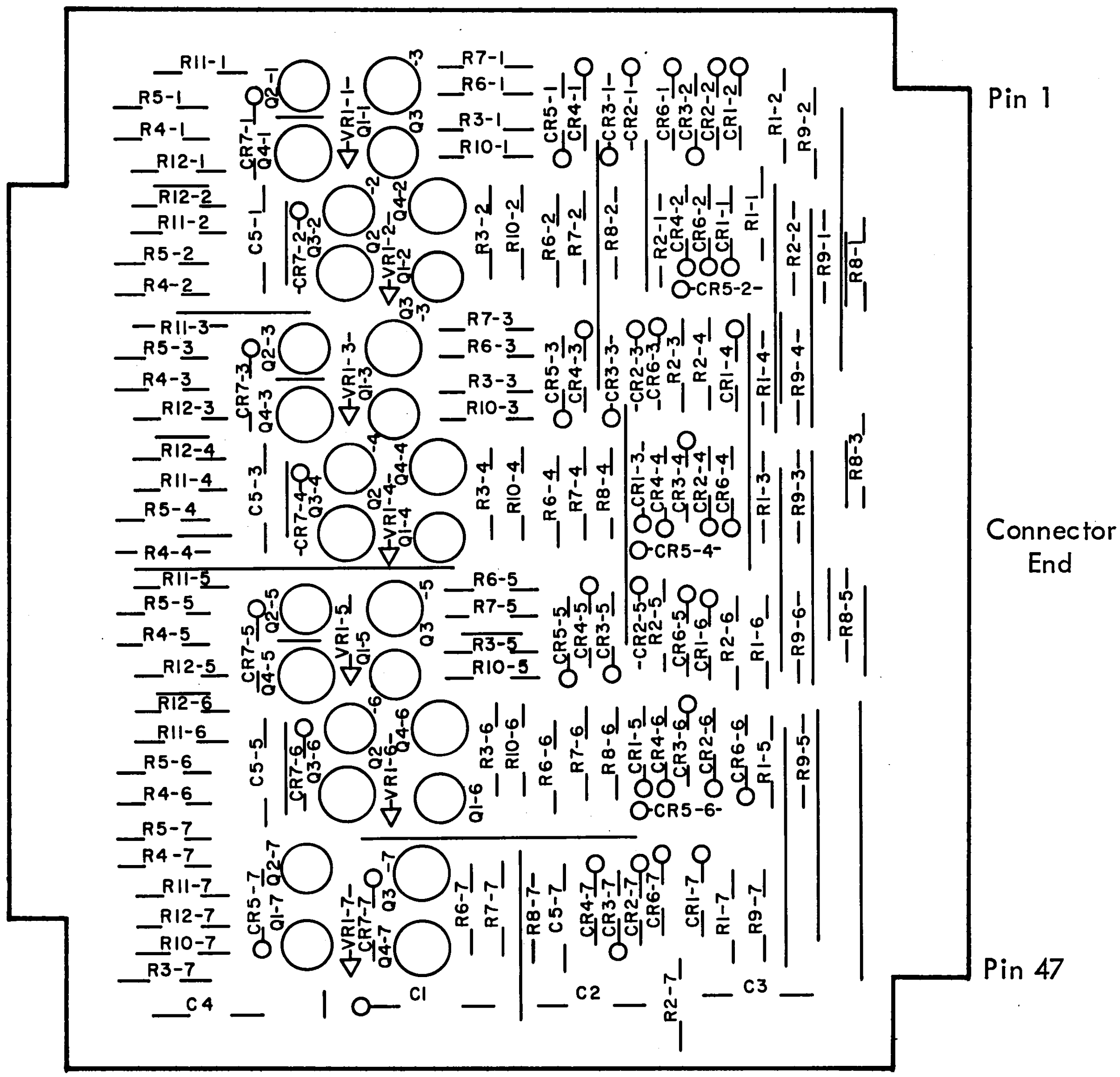
ITEM	DWG. TITLE	DWG. NO.	NO. REQ.	REMARKS OR CKT. DESIG.
1	Board, Printed Wiring	104839	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn Upper	100097	23	
6	Contact, Conn Lower	100098	24	
7	Transistor, SDS 216	103242	12	Q1, 2
8	Transistor, SDS 217	104389	12	Q3, 4
9	Diode SDS 103	100091	42	CR1, CR3 thru CR8
10	Diode SDS 101	100025	12	VR1, 2
11	Capacitor, Silver Mica	100107-221	12	C1, 2
12	Capacitor, Mylar	100308-103	3	C4, 5, 6
13	Capacitor, Tantalum	100312-156	1	C7
14	~~Resistor, $\frac{1}{2}$ watt~~	~~100111-470~~	~~6~~	~~R10~~
15	Resistor, $\frac{1}{2}$ watt	100111-151	6	R11, 12, 13, 14, 15, 16
16	Resistor, $\frac{1}{2}$ watt	100111-122	24	R3, 4, 7, 8
17	Resistor, $\frac{1}{4}$ watt	100111-302	6	R2
18	Resistor, $\frac{1}{2}$ watt	100111-332	6	R1
19	Resistor, $\frac{1}{2}$ watt	100111-822	12	R5, 9
20	Resistor, $\frac{1}{2}$ watt	100111-153	6	R6
21	Wire, Solid Bare	100042-024	15 in.	
22	Tubing, Teflon	100274-022	15 in.	

SDS-E-106

106315 B



106315 B
REVISIONS
A REL. TO MFG.
B SEE REV E.O.
SCHEMATIC,
CABLE DRIVER
D
106315
B
AK53
106317
POLARIZING PINS 34 & 40
+25V 47
-25V 46
+8V 45
GROUND 44
1
C1
C2
C5-1
C5-3
C5-5
C5-7
C3
C4
+8V
+25V
+8V
R1
R2
R3
R4
R5
Q3
Q2
VR1
Q1
CR1
CR2
CR3
CR5
R6
R7
R8
R9
CR6
Q4
R10
R11
R12
CR7
-25V
CIRCUIT 1 11 3 4 6 8 5
2 14 10 2 9 8 7
3 23 13 15 17 19 16
4 12 22 21 20 19 18
5 37 27 28 30 33 29
6 26 36 35 34 33 32
7 39 38 40 41 43 42
GATE INPUT
DIRECT OUTPUT
OUTPUT RETURN
TERMINATED OUTPUT



Cable Driver AK53
106317D

MATERIAL LIST
DWG. TITLE

SDS SCIENTIFIC DATA SYSTEMS

ML | DWG. NO. 106317 | REV D

ASSY, P. W. CABLE DRIVER — MOD # AK53 — DATE 2-10 — SHEET 2 OF 2

ITEM	DWG. TITLE	DWG. NO.	NO. REQ	REMARKS OR CKT. DESIG.
1	Board, Printed Wiring	106316	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn Upper	100097	23	
6	Contact, Conn Lower	100098	24	
7	Transistor, SDS 216	103242	7	Q1
8	Transistor, SDS 201	100092	7	Q2
9	Transistor, SDS 209	100697	14	Q3, 4
10	Diode, SDS 103	100091	42	CR1, 2, 3, 5, 6, 7
11	Diode, SDS 101	100025	7	VR1
12	Resistor, ½ watt	100111-330	7	R8
13		100111-331	14	R9, R1
14		100111-392	14	R4, 5
15		100111-562	7	R2
16		100111-822	7	R3
17				
18	~~Resistor, ½ watt~~	~~100111-392~~	~~7~~	~~R6~~
19	Capacitor, Mylar	100308-103	7	C2, 3, 4, 5, 1, 5-3, 5-5, 5-7
20	Capacitor, Tantalum	100312-156	1	C1
21	Wire, Solid Bare	100042-024	32 in	
22	Tubing, Teflon	100274-022	32 in	
23	Resistor, ½ watt	100111-223	14	R10, 12
24	Resistor, ½ watt	100111-393	7	R11
25	Resistor, ½ watt	100111-680	14	R6, 7

REV D | DWG. NO. 106317 | ML

A RELEASED TO MFG

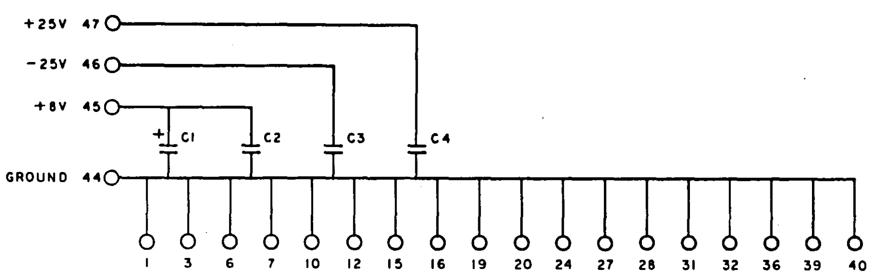
SCHEMATIC, SCHMITT TRIGGER

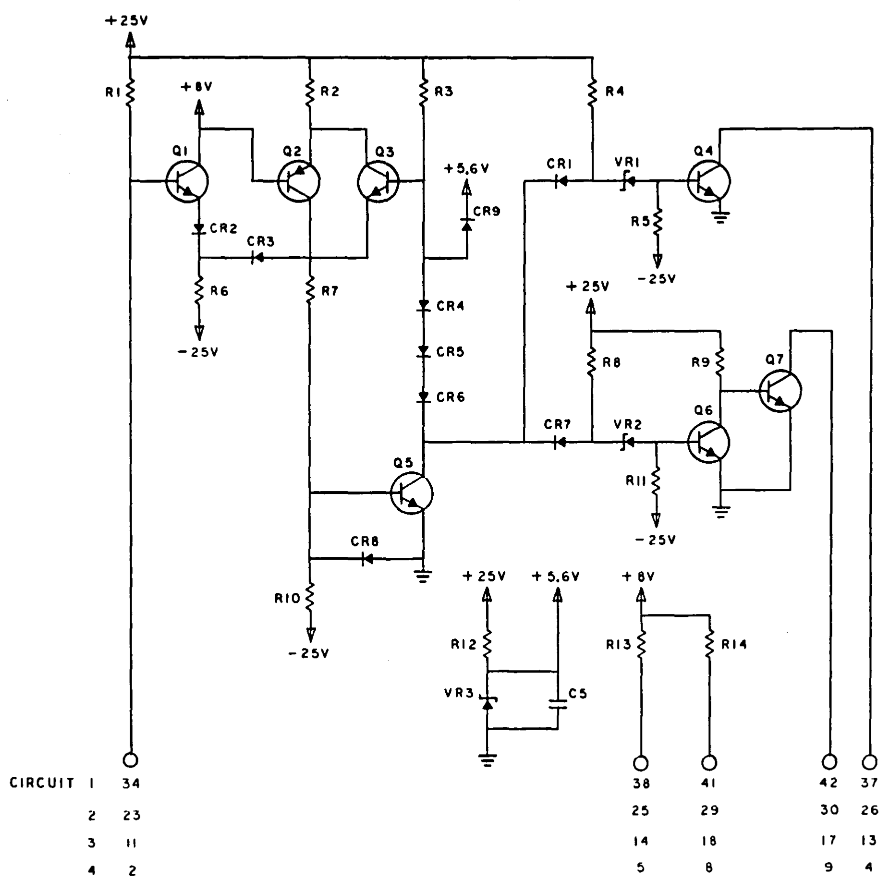
SDS

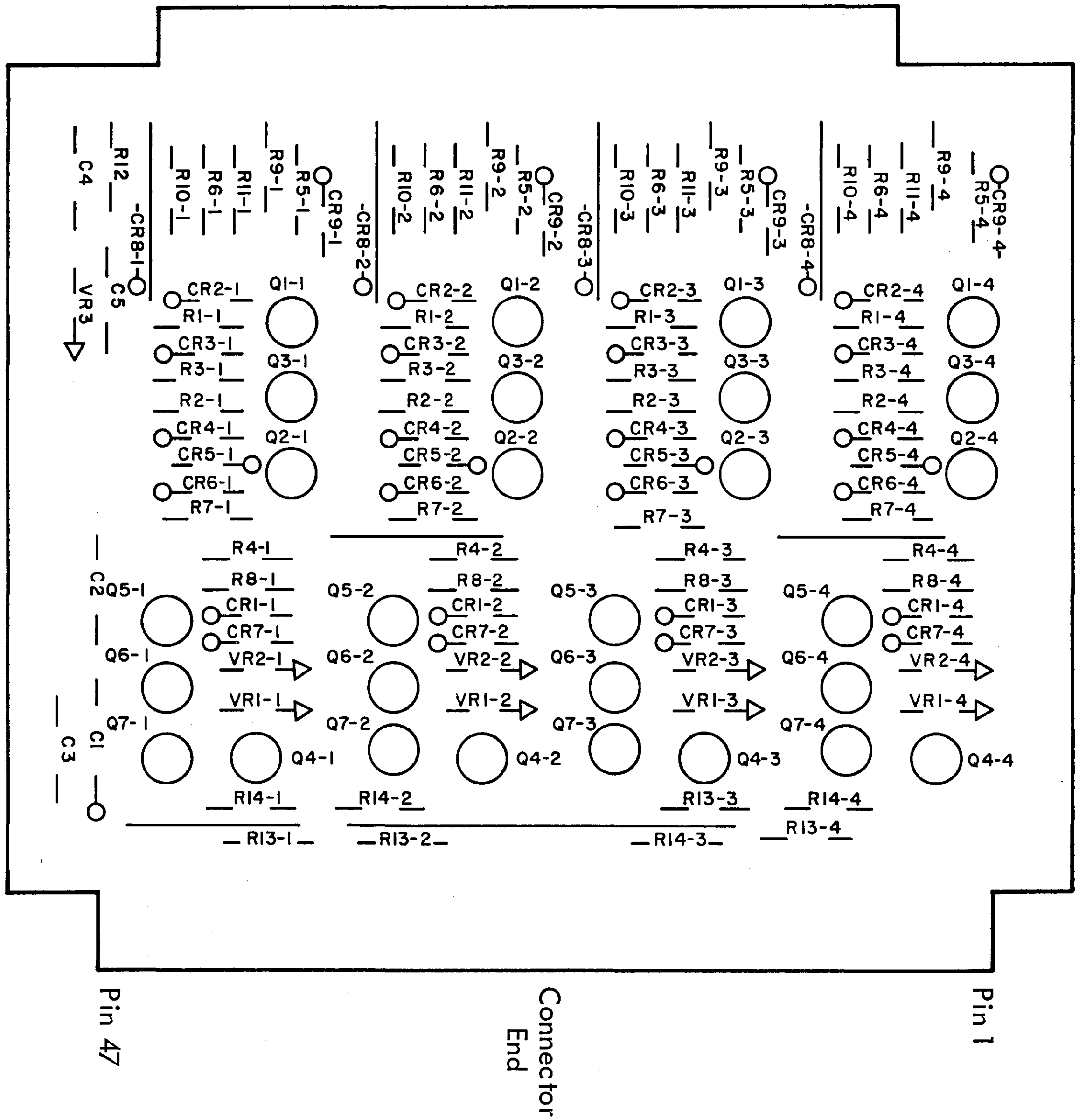
D 107232 A

AK54 107234

POLARIZING PINS: 3 & 31







Schmitt Trigger AK54
107234A

REV. A | DRAWING NO. 107234 | ML

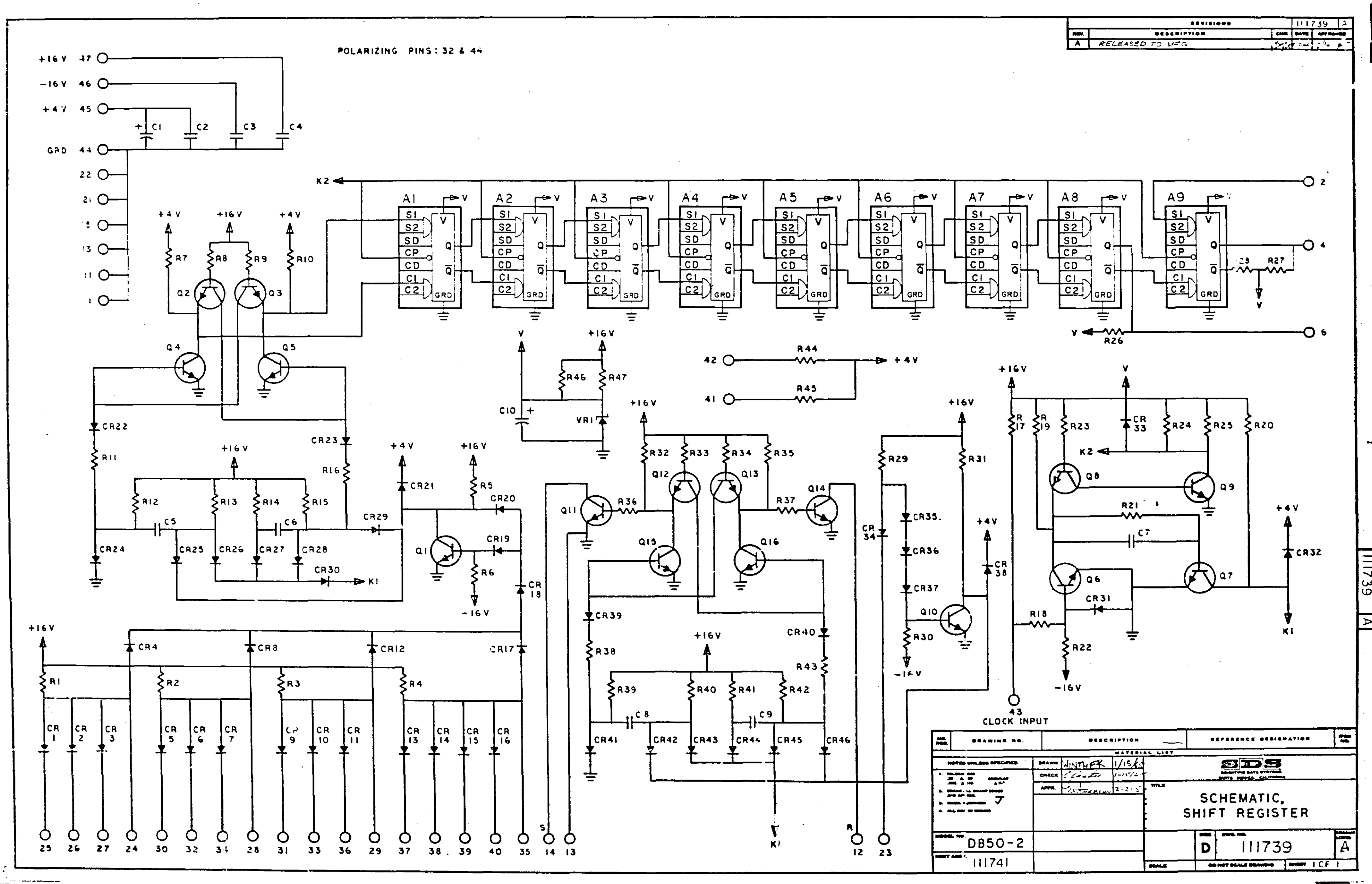
SDS
SCIENTIFIC DATA SYSTEMS

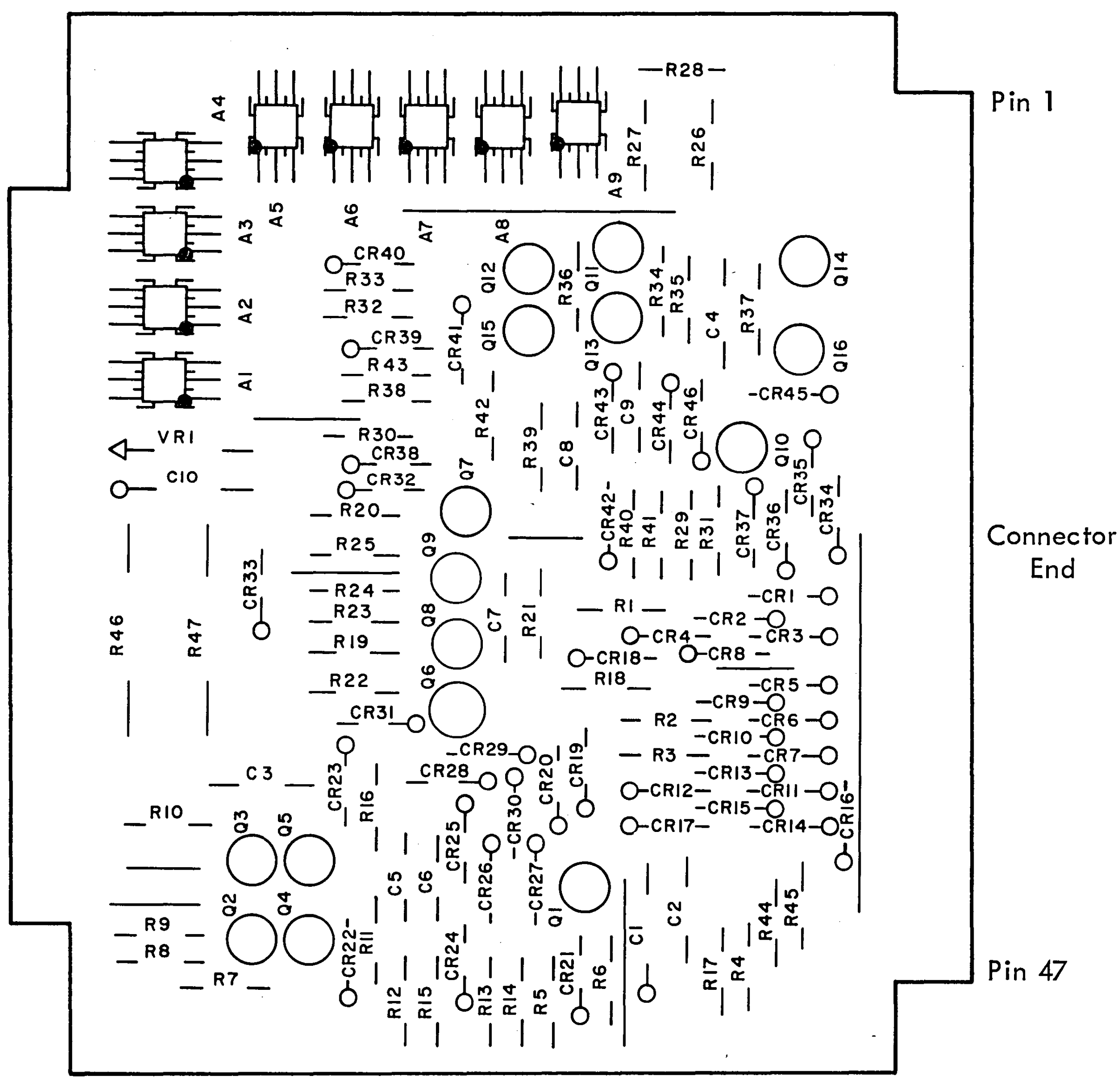
MATERIAL LIST

ML | DRAWING NO. 107234 | REV. A

DRAWING TITLE: Assy, P. W. SCHMITT TRIGGER   MODEL NO. AK54   DATE 6/12   SHEET 2 OF 2

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
1	Board, Printed Wiring	107233	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn. Upper	100097	23	
6	Contact, Conn. Lower	100098	24	
7	Transistor (SDS 216)	103242	24	Q1, 3, 4, 5, 6, 7
8	Transistor (SDS 219)	106378	4	Q2
9	Diode (SDS 101)	100025	8	VR1, 2
10	Diode (SDS 103)	100091	36	CR1 thru CR9
11	Diode (SDS 106)	100323	1	VR3
12	Resistor, 1/2 Watt	100111-392	28	R1, 2, 3, 4, 6, 8, 9
13	Resistor, 1/2 Watt	100111-153	12	R5, 10, 11
14				
15	Resistor, 1/2 Watt	100111-821	8	R13, 14
16	Resistor, 1/2 Watt	100111-102	4	R7
17	Resistor, 1/2 Watt	100111-222	1	R12
18	Capacitor, Tantalum	100312-156	1	C1
19	Capacitor, Mylar	100308-103	4	C2, 3, 4, 5
20	Wire, Solid Bare	100042-024	9 in	
21	Tubing, Teflon	100274-022	9 in	


POLARIZING PINS: 32 & 44
REVISIONS
111739 A
A RELEASED TO MFG.
CLOCK INPUT
SDS
SCHEMATIC,
SHIFT REGISTER
DB50-2
111741
D
111739
A
SHEET 1 OF 1
DO NOT SCALE DRAWING
DRAWN WINTHER 1/15/63



Shift Register DB50-2
111741B

SCIENTIFIC DATA SYSTEMS

MATERIAL LIST

ML | DRAWING NO. 111741 | REV. B

DRAWING TITLE Assy, PW Shift Register MODEL NO. DB50-2 DATE 1/8/65 SHEET 2 OF 3

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
1	Board, Printed Wiring	111740	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn. Upper	100097	23	
6	Contact, Conn. Lower	100098	24	
7	Transistor, SDS 216	103242	10	Q1, 4, 5, 6, 9, 10, 11, 14, 15, 16
8	Transistor, SDS 220	106781	5	Q2, 3, 12, 13, 8
9	Diode, SDS 103	100091	46	CR1 thru CR46
10	Integrated Ckt, SDS 301	108217	9	A1 thru A9
11	Resistor, ¼ Watt	100111-332	5	R1, 2, 3, 4, 29
12	Resistor, ¼ Watt	100111-222	5	R5, 26, 31, 27, 28
13	Resistor, ¼ Watt	100111-153	2	R6, 30
14	Resistor, ¼ Watt	100111-102	8	R7, 10, 13, 14, 24, 25, 40, 41
15	Resistor, ¼ Watt	100111-562	4	R8, 9, 33, 34
16	Resistor, ¼ Watt	100111-101	5	R11, 16, 38, 43, 21
17	Resistor, ¼ Watt	100111-822	4	R12, 15, 39, 42
18	Resistor, ¼ Watt	100111-122	2	R20, 19
19	Resistor, ¼ Watt	100111-182	1	R17
20	Resistor, ¼ Watt	100111-681	1	R18
21	Resistor, ¼ Watt	100111-103	1	R22
22				
23	Resistor, ¼ Watt	100111-302	3	R32, 35, 23
24	Resistor, ¼ Watt	100111-470	2	R36, 37
25	Resistor, ¼ Watt	100111-151	2	R44, 45
26	Capacitor, Tantalum	100312-156	2	C1, 10
27	Capacitor, Mylar	100308-103	3	C2, 3, 4
28	Capacitor, Mica	100107-820	4	C5, 6, 8, 9
29	Capacitor, Mica	100107-221	1	C7
30				
31				
32				

SDS-E-106B

REV. B | DRAWING NO. 111741 | ML

SDS
SCIENTIFIC DATA SYSTEMS

MATERIAL LIST

ML | DRAWING NO. 111741 | REV. B

DRAWING TITLE Assy. PW Shift Register MODEL NO. DB50-2 DATE 1/8/65 SHEET 3 OF 3

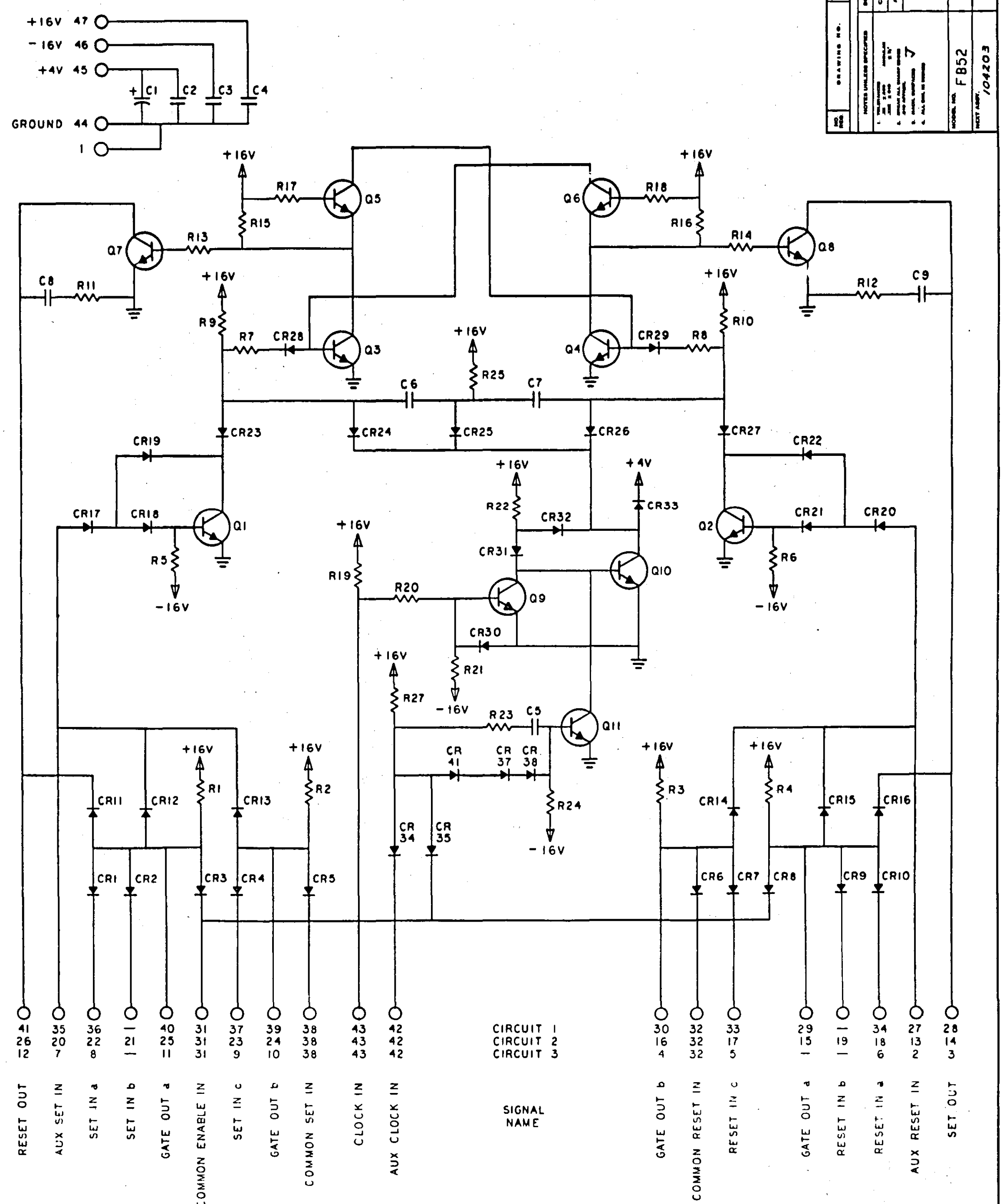
ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
33	Transistor, SDS 217	104389	1	Q7
34	Tubing, Teflon	100274-022	8 in.	
35	Wire, Solid Bare	100042-024	8 in.	
36	Resistor	100681-161	2	R46, 47
37	Diode, (SDS 114)	101711	1	VR1
38	Schematic	111739	x	Ref
39	Drawing List	111742	x	Ref
40	Test spec	111743	x	Ref

SDS-E-105B

104201 B

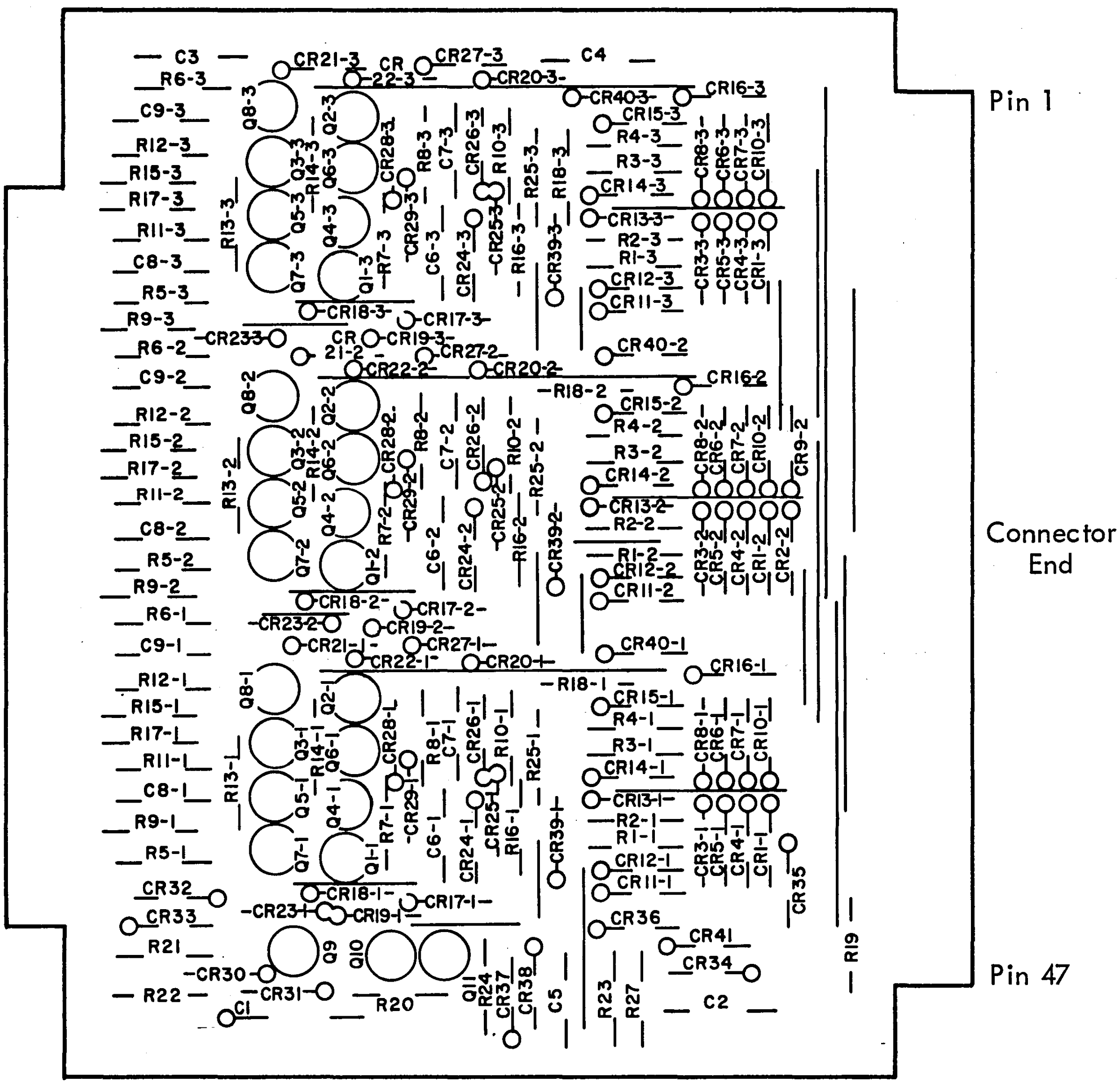
A	RELEASED TO MFG
B	SEE REV E.O.

POLARIZING PINS: 28 & 34



SCHEMATIC, TRIPLE FLIP FLOP

MODEL NO.	FB52
NEXT ASSY.	104203
SIZE	D
DWG. NO.	104201
REV	B
CHECK	V. MASTIS



Triple Flip-Flop FB52
104203D

MATERIAL LIST
DWG. TITLE
ASSEMBLY, P. W.
TRIPLE FLIP FLOP

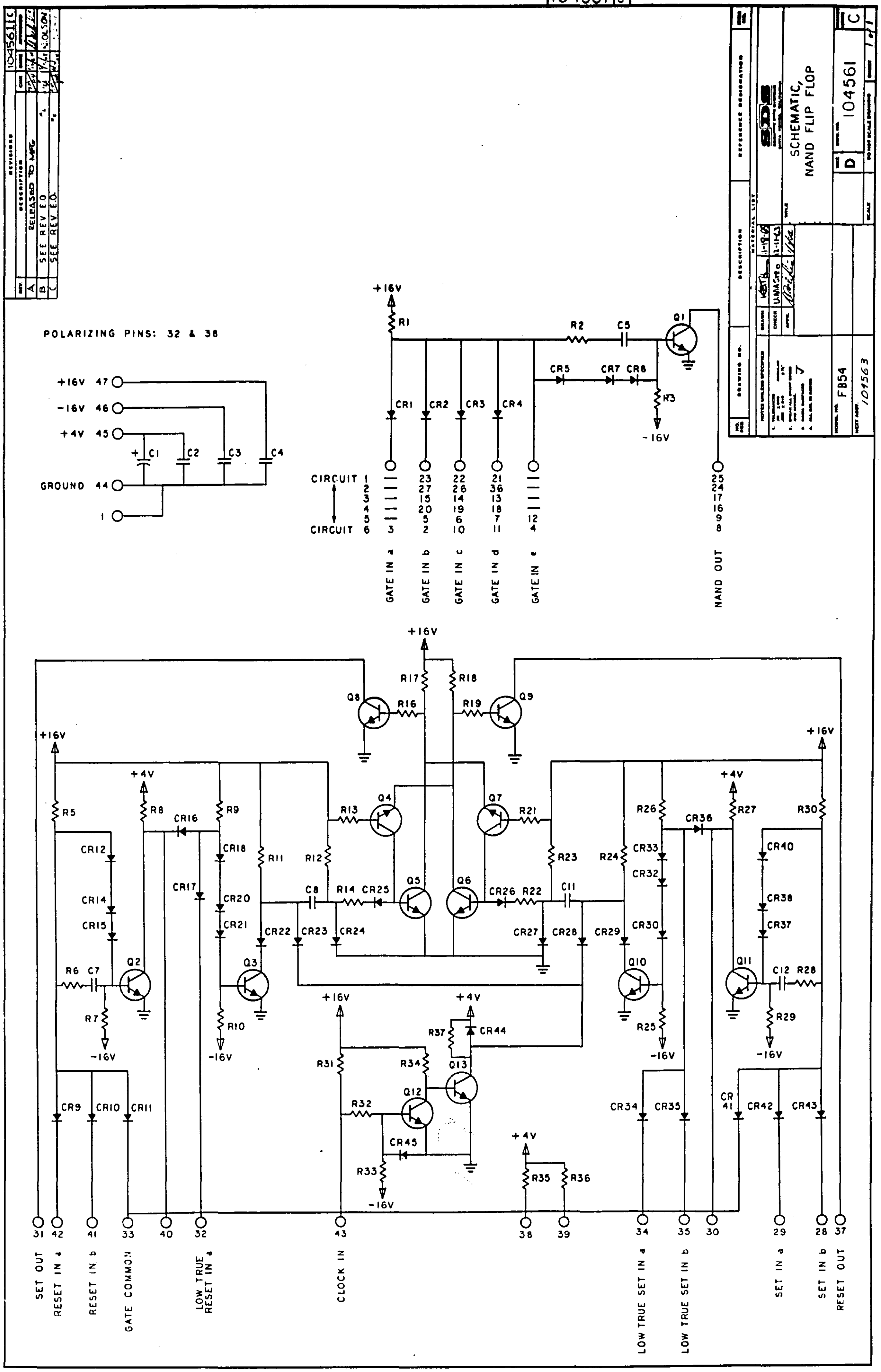
SDS SCIENTIFIC DATA SYSTEMS

ML | DWG. NO. 104203 | REV D

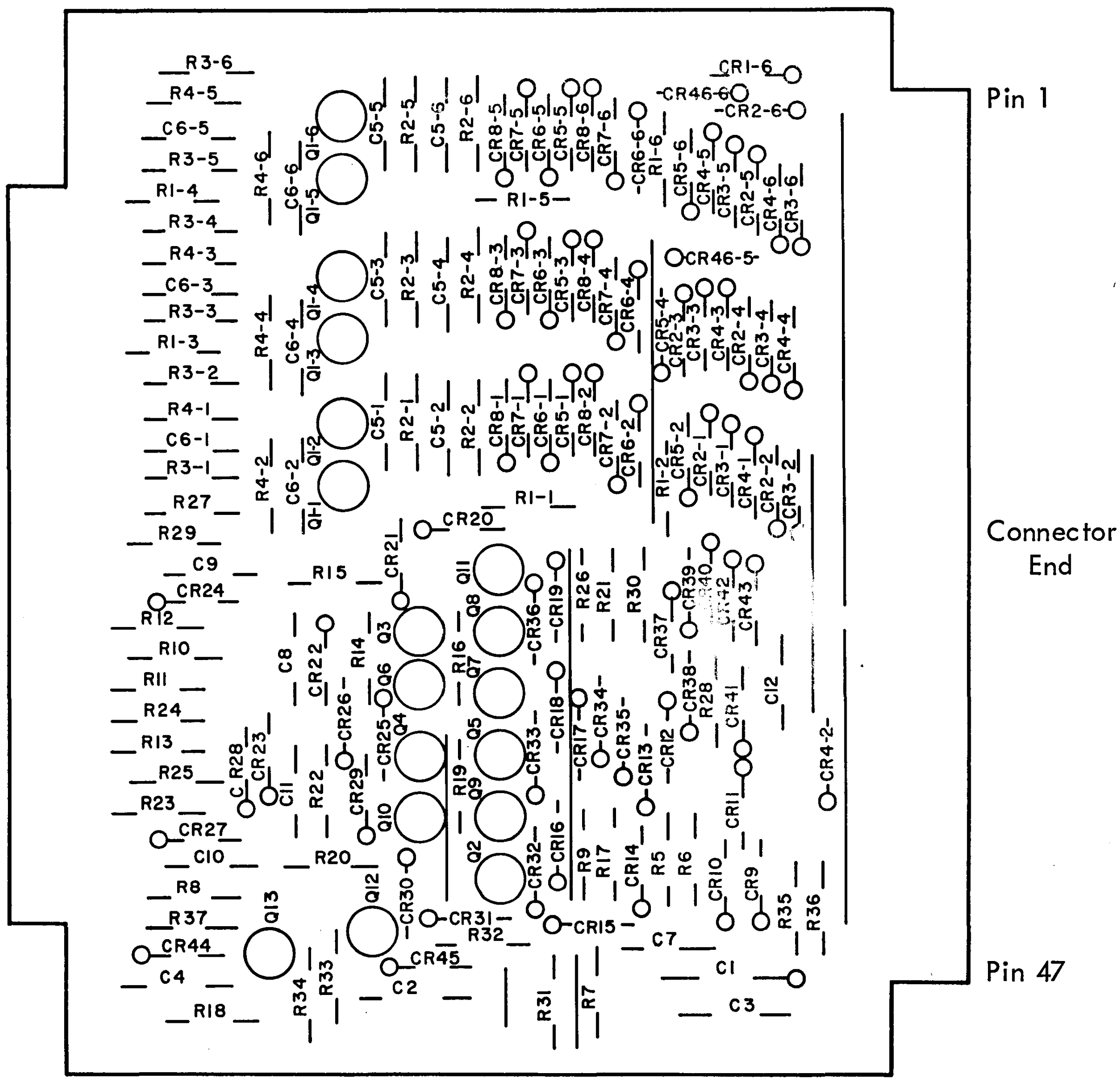
MOD # FB52 DATE 12/4/3 SHEET 2 OF 2

ITEM	DWG. TITLE	DWG. NO.	NO. REQ	REMARKS OR CKT. DESIG.
1	Board, Printed Wiring	104202	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn. Upper	100097	23	
6	Contact, Conn. Lower	100098	24	
7	Transistor, SDS 216	103242	21	Q1 thru Q4, Q7 thru Q11
8	Transistor, SDS 220	106781	6	Q5, 6
9	Diode, SDS 103	100091	92	CR1 thru CR35, 37, 38, 41
10	~~Capacitor, Mica~~	~~100107-220~~	~~7~~	~~C8, 9, 5~~
11	Resistor, ½ watt	100111-103	1	R21
12	Capacitor, Mica	100107-820	6	C6, 7
13	Capacitor, Mylar	100308-103	3	C2, 3, 4
14	Capacitor, Tantalum	100312-156	1	C1
15	Resistor, ½ watt	100111-102	3	R25
16	Resistor, ½ watt	100111-562	6	R17, 18
17	Resistor, ½ watt	100111-302	6	R15, 16
18	Resistor, ½ watt	100111-470	7	R13, 14, 23
19	~~Resistor, ½ watt~~	~~100111-151~~	~~6~~	~~R11, 12~~
20	Resistor, ½ watt	100111-101	6	R7, 8
21	Resistor, ½ watt	100111-822	6	R9, 10
22	Resistor, ½ watt	100111-153	6	R5, 6,
23	Resistor, ½ watt	100111-332	13	R1, 2, 3, 4, 27
24	Resistor, ½ watt	100111-122	1	R22
25	Resistor, ½ watt	100111-681	1	R20
26	Resistor, ½ watt	100111-182	1	R19
27	Resistor, ½ watt	100111-563	1	R24
28	Wire, Solid Bare	100042-024	35 in.	
29	Tubing Teflon	100274-022	35 in.	
30	Capacitor, Mica	100107-470	1	C5

104561 C



REV | DESCRIPTION
A | RELEASED TO MFG
B | SEE REV E.O.
C | SEE REV E.O.
POLARIZING PINS: 32 & 38
+16V 47
-16V 46
+4V 45
GROUND 44
1
C1 C2 C3 C4
+16V
R1
R2 C5 Q1
CR5 CR7 CR8
R3
-16V
CR1 CR2 CR3 CR4
CIRCUIT 1 | 23 | 22 | 21 | 25
2 | 27 | 26 | 36 | 24
3 | 15 | 14 | 13 | 17
4 | 20 | 19 | 18 | 16
5 | 5 | 6 | 7 | 9
CIRCUIT 6 | 3 | 2 | 10 | 11 | 12 | 4 | 8
GATE IN a
GATE IN b
GATE IN c
GATE IN d
GATE IN e
NAND OUT
+16V
R17 R18
Q8 R16 R19 Q9
+16V
+4V
R5 R8 CR16 R9
CR12 CR18
CR14 CR17 CR20
CR15 CR21
R11 R12 R13 Q4
C8 R14 CR25 Q5 Q6 CR26 R22 C11
CR22 CR23 CR24 CR27 CR28 CR29
Q7 R21 R23 R24 R26 CR36 R27 R30
CR33 CR32 CR30 CR40 CR38 CR37
R6 C7 Q2 Q3 Q10 Q11 C12 R28
R7 R10 R25 R29
-16V
+16V +4V
R37 CR44
R31 R34 Q13
R32 Q12
CR45
R33
-16V
+4V
R35 R36
CR9 CR10 CR11
CR34 CR35 CR41 CR42 CR43
31 42 41 33 40 32 43 38 39 34 35 30 29 28 37
SET OUT
RESET IN a
RESET IN b
GATE COMMON
LOW TRUE RESET IN a
CLOCK IN
LOW TRUE SET IN a
LOW TRUE SET IN b
SET IN a
SET IN b
RESET OUT
SDS
SCHEMATIC, NAND FLIP FLOP
D
104561
C
FB54
104563



NAND Flip-Flop FB54
104563E

REV E | DWG. NO. 104563 | ML

MATERIAL LIST
DWG. TITLE
ASSEMBLY, P. W.
NAND, FLIP FLOP

SDS SCIENTIFIC DATA SYSTEMS

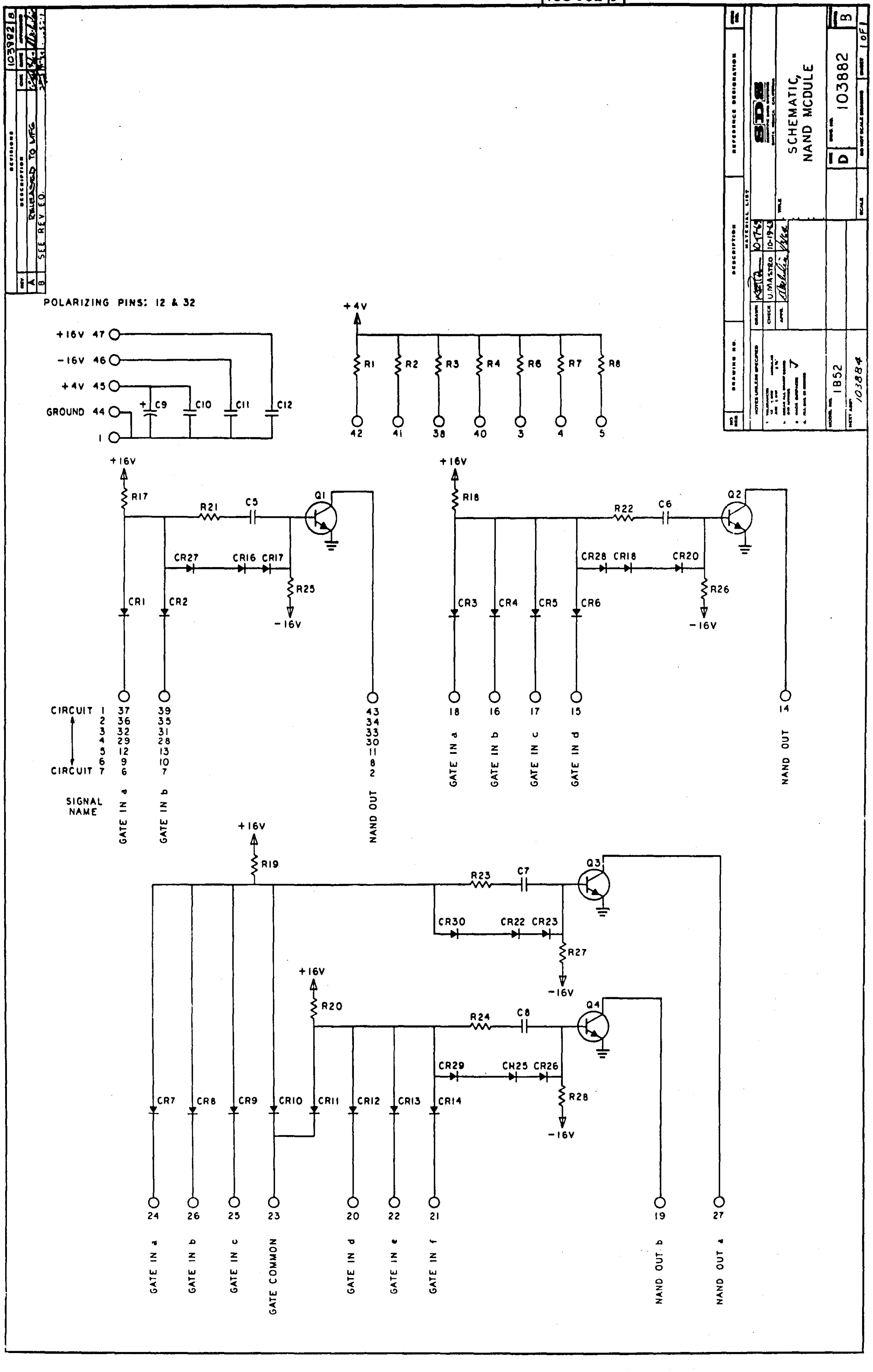
ML | DWG. NO. 104563 | REV E

MOD # FB54 DATE 12/4 SHEET 2 OF 2

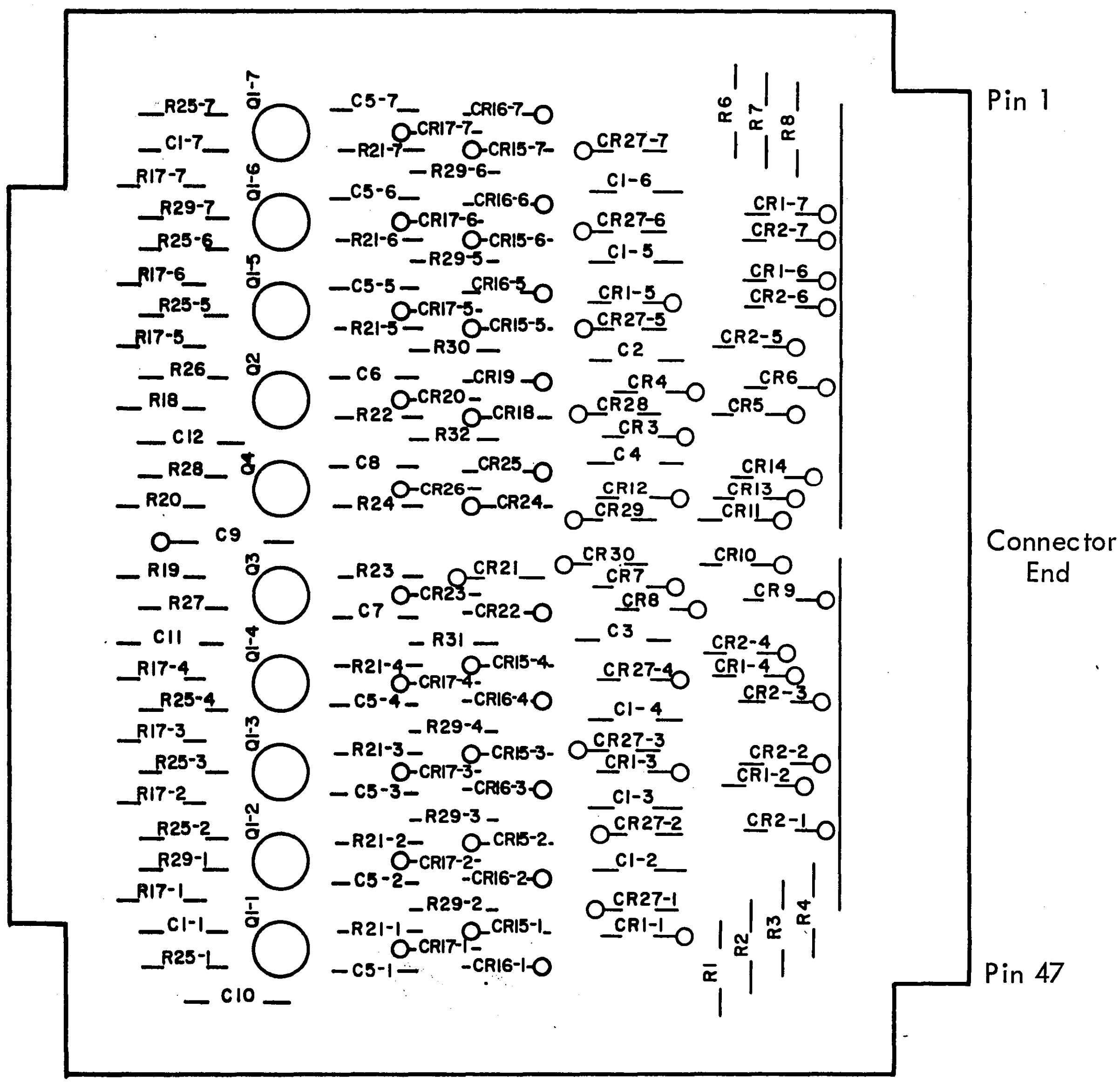
ITEM	DWG. TITLE	DWG. NO.	NO. REQ	REMARKS OR CKT. DESIG.
1	Board, Printed Wiring	104562	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn Upper	100097	23	
6	Contact, Conn Lower	100098	24	
7	Transistor, SDS 216	103242	16	Q1 thru Q3, 5, 6, Q8 thru 13
8	~~Diode, SDS 103~~	~~100091~~	~~72~~	~~CR1 thru CR46~~
9	Capacitor, Silver Mica	100107-470	8	C5, 7, 12,
10	Capacitor, Silver Mica	100107-820	2	C8, 11
11	Capacitor, Mylar	100308-103	3	C2, 3, 4
12	Capacitor, Tantalum	100312-156	1	C1
13	Resistor, ½ watt	100111-470	10	R2, 6, 16, 19, 28
14	Resistor, ½ watt	100111-101	2	R14, 22
15	Resistor, ½ watt	100111-151	4	R8, , 27, 35, 36
16	Resistor, ½ watt	100111-822	2	R12, 23
17	Resistor, ½ watt	100111-681	1	R32
18	Resistor, ½ watt	100111-102	2	R11, 24
19	Resistor, ½ watt	100111-222	1	R34
20	Resistor, ½ watt	100111-302	2	R17, 18
21	Resistor, ½ watt	100111-332	10	R1, 5, 9, 26, 30,
22	Resistor, ½ watt	100111-562	2	R13, R21
23	Resistor, ½ watt	100111-103	1	R33
24	Resistor, ½ watt	100111-223	2	R10, 25
25	Resistor, ½ watt	100111-563	8	R3, 7, 29
26	Wire, Solid Bare	100042-024	18 in.	
27	Tubing, Teflon	100274-022	18 in	
28	Resistor, ½ watt	100111-121	1	R37
29	Resistor, ½ watt	100111-182	1	R31
30	Transistor, SDS 220	106781	2	Q4, Q7
31	Diode, SDS 103	100091	72	CR1 thru CR5, 7 thru 12, 14
				CR15, 16, 17, 18, 20 thru 30
				CR32 thru 38, 40 thru 46

SDS-E-106

|103882|B|



SCHEMATIC, NAND MODULE
103882
D
B
1 OF 1
1B52
103884
REVISIONS
A RELEASED TO MFG
B SEE REV E.O.
POLARIZING PINS: 12 & 32
+16V 47
-16V 46
+4V 45
GROUND 44
1
C9 C10 C11 C12
+4V
R1 R2 R3 R4 R6 R7 R8
42 41 38 40 3 4 5
+16V
R17 R21 C5 Q1
CR27 CR16 CR17
R25
-16V
CR1 CR2
CIRCUIT 1 37 39 43
2 36 35 34
3 32 31 33
4 29 28 30
5 12 13 11
6 9 10 8
CIRCUIT 7 6 7 2
SIGNAL NAME
GATE IN a
GATE IN b
NAND OUT
+16V
R18 R22 C6 Q2
CR28 CR18 CR20
R26
-16V
CR3 CR4 CR5 CR6
18 16 17 15 14
GATE IN a
GATE IN b
GATE IN c
GATE IN d
NAND OUT
+16V
R19 R23 C7 Q3
CR30 CR22 CR23
R27
-16V
+16V
R20 R24 C8 Q4
CR29 CR25 CR26
R28
-16V
CR7 CR8 CR9 CR10 CR11 CR12 CR13 CR14
24 26 25 23 20 22 21 19 27
GATE IN a
GATE IN b
GATE IN c
GATE COMMON
GATE IN d
GATE IN e
GATE IN f
NAND OUT b
NAND OUT a



NAND Module IB52
103884D

REV D | DWG. NO. 103884 | ML

MATERIAL LIST

SDS SCIENTIFIC DATA SYSTEMS

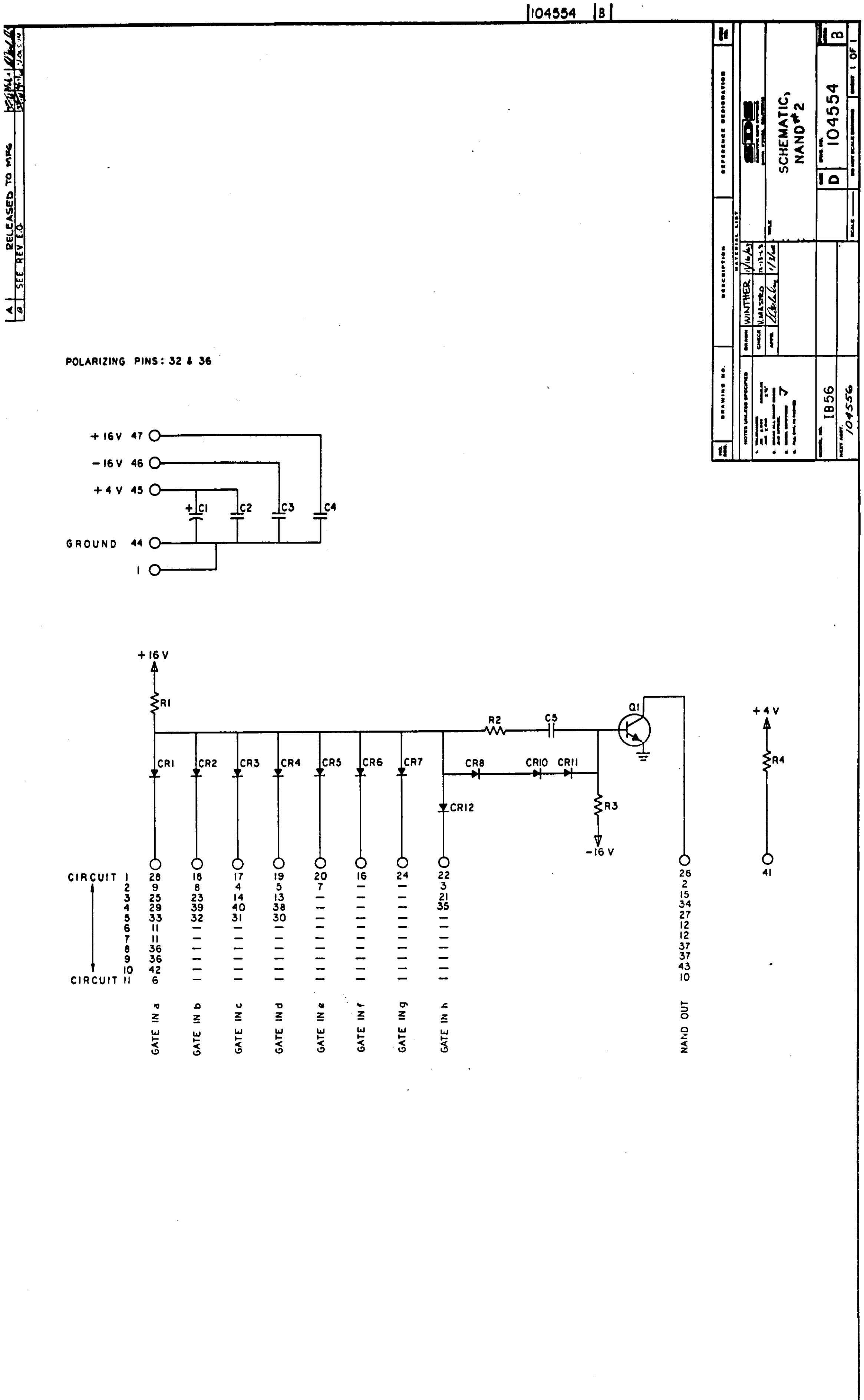
ML | DWG. NO. 103884 | REV D

DWG. TITLE
ASSY, PRINTED WIRING
NAND MODULE

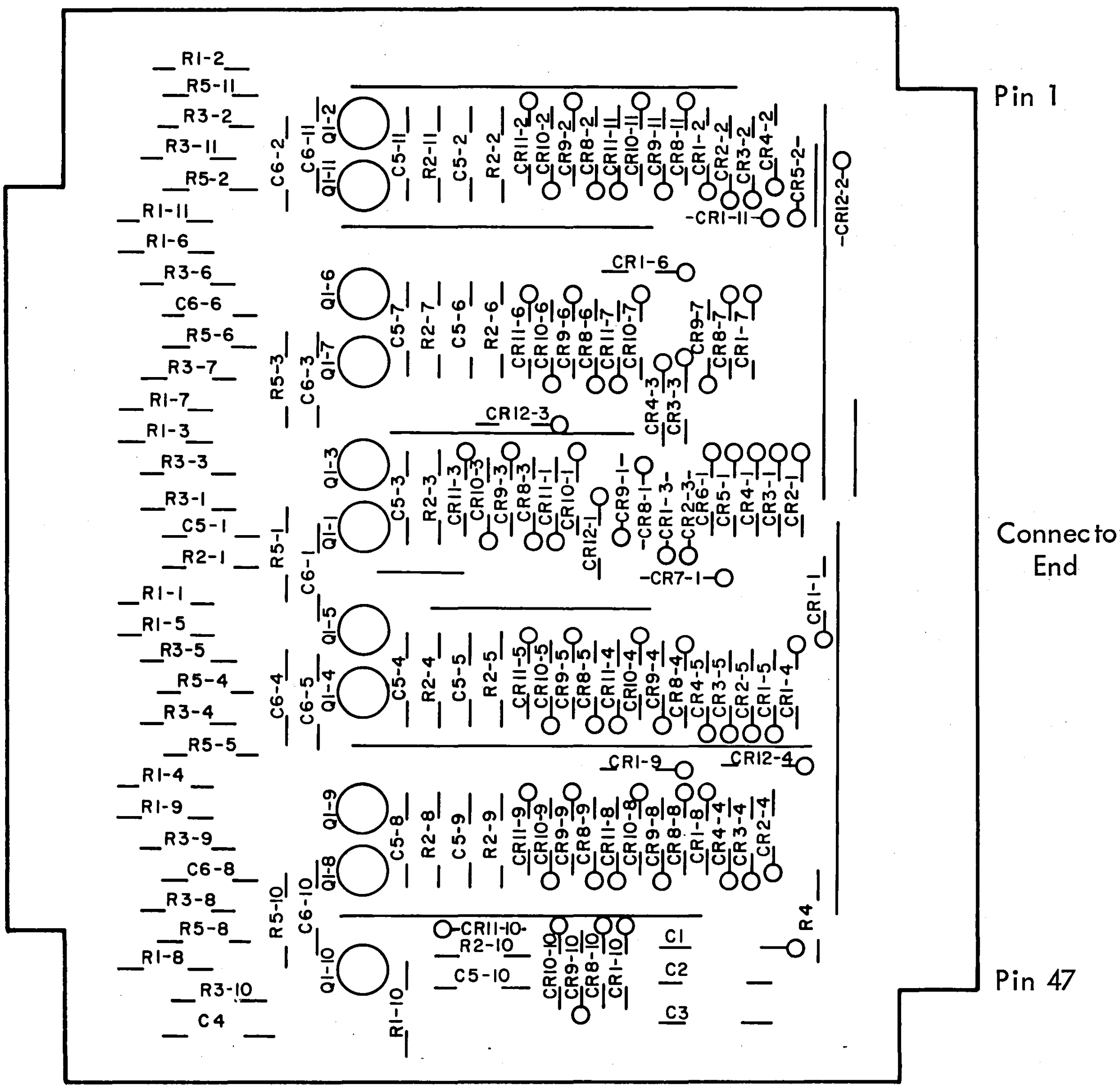
MOD # IB52 DATE ____ SHEET 2 OF 2

ITEM	DWG. TITLE	DWG. NO.	NO. REQ	REMARKS OR CKT. DESIG.
1	Board, Printed Wiring	103883	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn. Upper	100097	23	
6	Contact, Conn. Lower	100098	24	
7	Transistor (SDS 216)	103242	10	Q1, 2, 3, 4
~~8~~	~~Diode (SDS 103)~~	~~100091~~	~~66~~	~~CR1 thru CR30~~
9	Capacitor, Silver Mica	100107-470	10	C5, 6, 7, 8
10				
11	Capacitor, Mylar	100308-103	3	C10, 11, 12
12	Capacitor, Tantalum	100312-156	1	C9
13	Resistor, ½ watt	100111-332	10	R17, 18, 19, 20
14	Resistor, ½ watt	100111-470	10	R21, 22, 23, 24
15	Resistor, ½ watt	100111-563	10	R25, 26, 27, 28
16	Resistor, ½ watt	100111-151	7	R1 thru 4, 6, 7, 8
17	Wire, Solid Bare	100042-024	10 in.	
18	Tubing, Teflon	100274-022	10 in.	
19	Diode (SDS 103)	100091	56	CR1 thru CR14, 16, 17, 18, 20, 22, 23, 25 thru 30

104554 B



A RELEASED TO MFG
B SEE REV E.O.
POLARIZING PINS: 32 & 36
+16V 47
-16V 46
+4V 45
GROUND 44
1
C1
C2
C3
C4
+16V
R1
R2
C5
Q1
R3
-16V
+4V
R4
41
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR10
CR11
CR12
CIRCUIT 1
CIRCUIT 11
GATE IN a
GATE IN b
GATE IN c
GATE IN d
GATE IN e
GATE IN f
GATE IN g
GATE IN h
NAND OUT
WINTHER
V. MASTRO
SCHEMATIC, NAND #2
D
104554
B
SHEET 1 OF 1
1B56
104556



NAND No. 2 IB56
104556E

REV	E
DWG. NO.	104556

ML

MATERIAL LIST

DWG. TITLE ASSEMBLY, P. W. NAND # 2

SDS SCIENTIFIC DATA SYSTEMS

ML

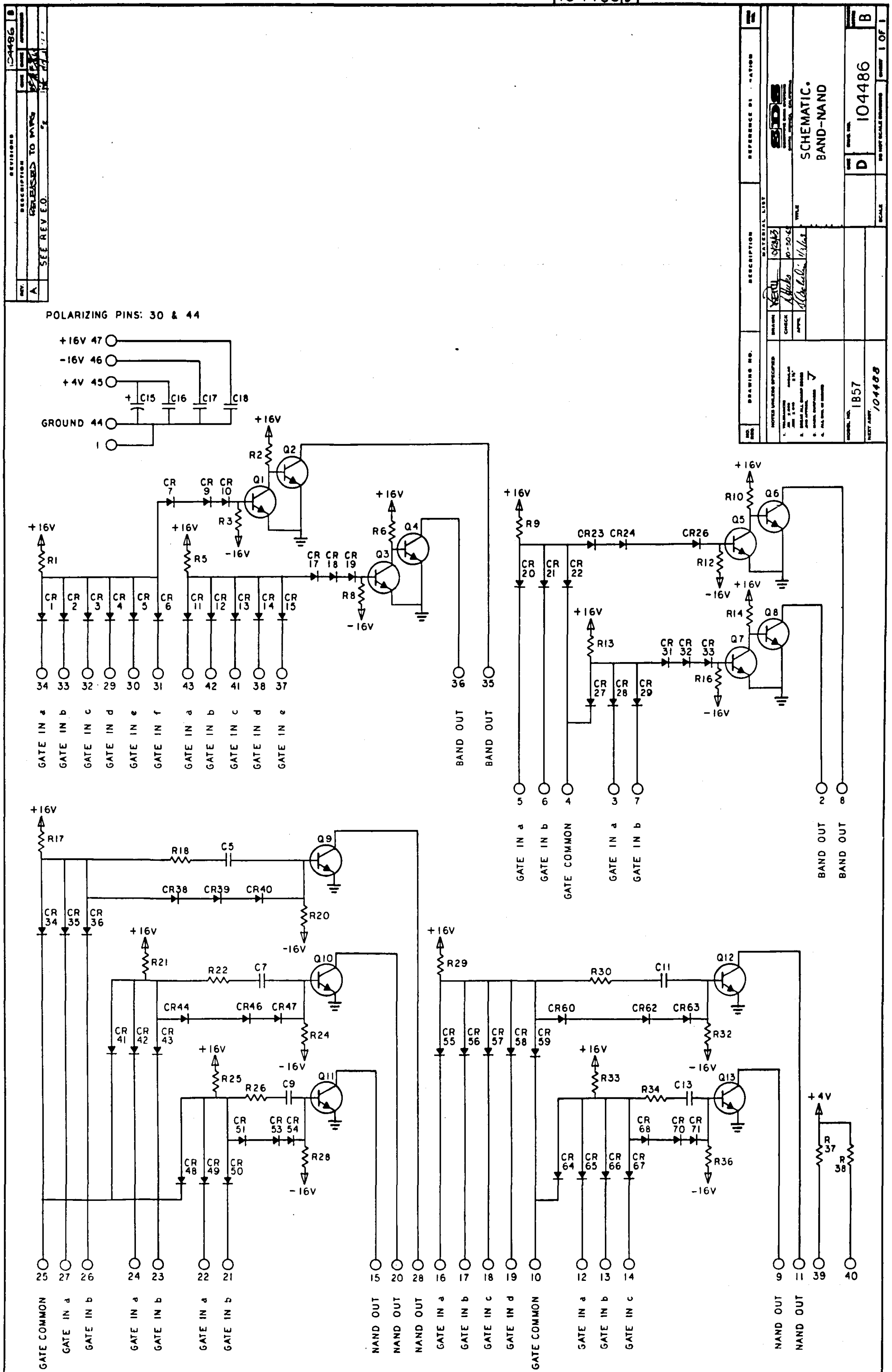
DWG. NO.	REV
104556	E

MOD # IB 56 DATE 12/4 SHEET 2 OF 2

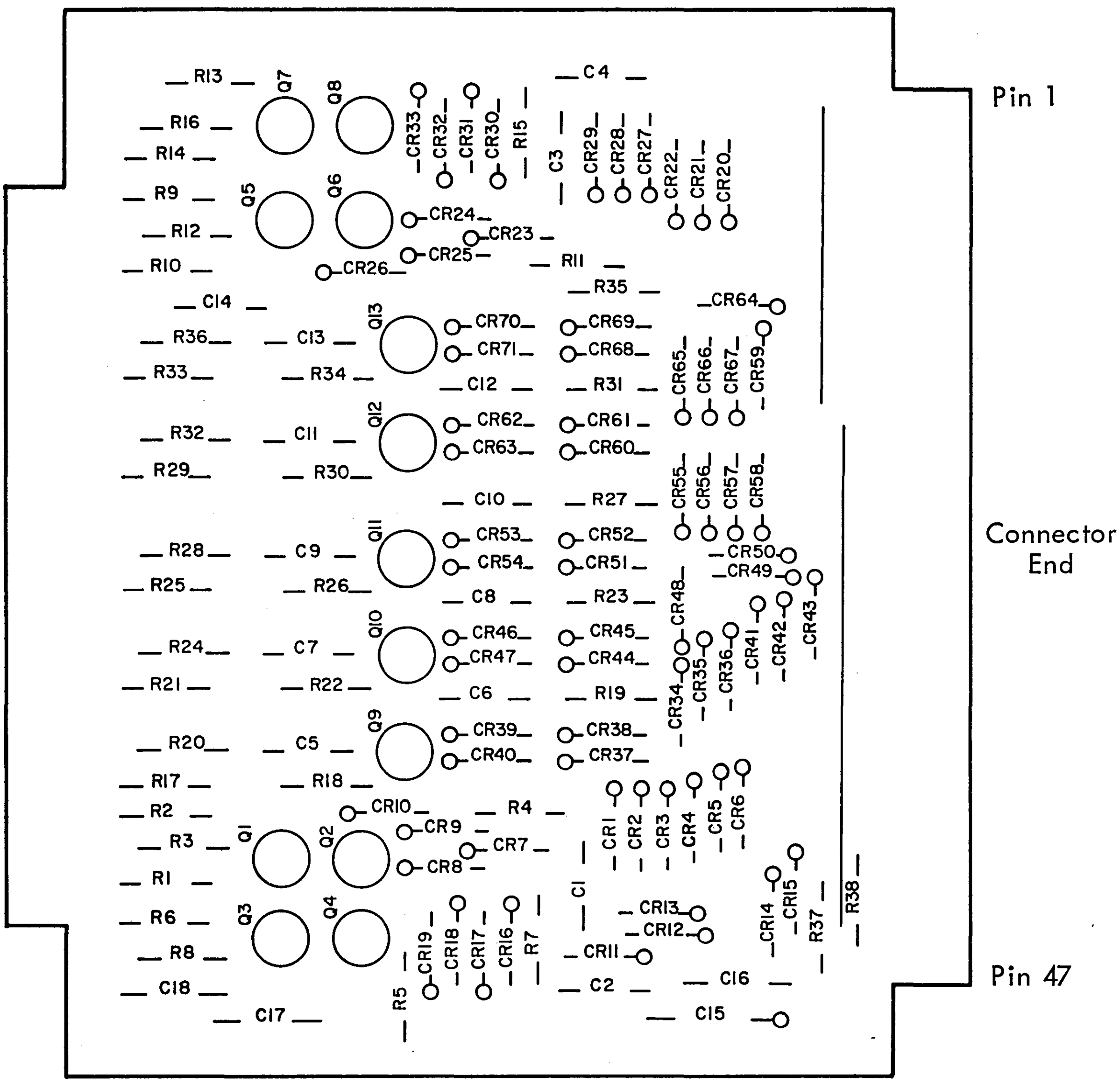
ITEM	DWG. TITLE	DWG. NO.	NO. REQ	REMARKS OR CKT. DESIG.
1	Board, Printed Wiring	104555	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn Upper	100097	23	
6	Contact, Conn Lower	100098	24	
7	Transistor SDS 216	103242	11	Q1
8	Diode, SDS 103	100091	67	CR1 thru CR8, CR10, 11, 12
9	Capacitor, Silver Mica	100107-470	11	C5
10	Capacitor, Mylar	100308-103	3	C2, 3, 4
11	Capacitor, Tantalum	100312-156	1	C1
12	Resistor, ½ watt	100111-151	1	R4
13	Resistor, ½ watt	100111-470	11	R2
14	Resistor, ½ watt	100111-332	11	R1
15	Resistor, ½ watt	100111-563	11	R3
16	Wire, Solid Bare	100042-024	24 in.	
17	Tubing, Teflon	100274-022	24 in.	

SDS-E-106

104486 B



SCHEMATIC, BAND-NAND
104486
D
B
1 OF 1
1B57
104488
REVISIONS
A RELEASED TO MFG
SEE REV E.O.
POLARIZING PINS: 30 & 44
+16V 47
-16V 46
+4V 45
GROUND 44
1
C15 C16 C17 C18
GATE IN a
GATE IN b
GATE IN c
GATE IN d
GATE IN e
GATE IN f
BAND OUT
GATE COMMON
NAND OUT



BAND NAND IB57
104488D

REV	D
DWG. NO.	104488
	ML

MATERIAL LIST SDS SCIENTIFIC DATA SYSTEMS **ML**

DWG. TITLE
ASSY, PRINTED WIRING
BAND - NAND

DWG. NO.	REV
104488	D

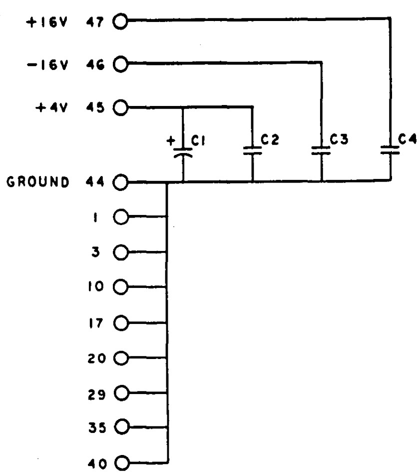
MOD 0 IB57 DATE 12/4 SHEET 2 OF 2

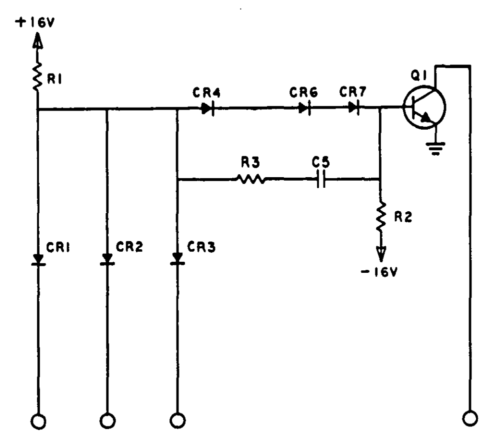
ITEM	DWG. TITLE	DWG. NO.	NO. REQ	REMARKS OR CKT. DESIG.
1	Board, Printed Wiring	104487	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn Upper	100097	23	
6	Contact, Conn Lower	100098	24	
7	Transistor, SDS 216	103242	13	Q1 thru Q13
8				
9	~~Diode, SDS 103~~	~~100091~~	~~71~~	~~CR1 thru CR71~~
10				
11	Capacitor, Mica	100107-470	5	C5, 7, 9, 11, 13
12	Capacitor, Mylar	100308-103	3	C16, 17, 18
13	Capacitor, Tantalum	100312-156	1	C15
14	Resistor, 1/8 watt	100111-151	2	R37, 38
15	Resistor, 1/2 watt	100111-470	5	R18, 22, 26, 30, 34
16	Resistor, 1/2 watt	100111-332	9	R1, 5, 9, 13, 17, 21, 25, 29, 33
17	Resistor, 1/2 watt	100111-153	4	R3, 8, 12, 16,
18	Wire, Solid Bare	100042-024	10 in	
19	Tubing, Teflon	100274-022	10 in	
20	Resistor, 1/2 watt	100111-563	5	R20, 24, 28, 32, 36
21	Resistor, 1/2 watt	100111-302	4	R2, 6, 10, 14
22	Diode, SDS 103	100091	62	CR1 thru 7, 9 thru 15
				CR17 thru 24, 26 thru 29
				CR31 thru 36, 38 thru 44
				CR46 thru 51, 53 thru 60
				CR 62 thru 68, 70, 71

104894 B

REV.	DESCRIPTION
A	RELEASED TO MFG.
B	SEE REV. E.O.

POLARIZING PINS: 42 & 46





CIRCUIT				
1	5	7	8	2
2	6	7	8	4
3	13	14	15	9
4	12	7	8	11
5	24	—	25	16
6	27	14	15	18
7	23	14	15	19
8	22	—	25	21
9	26	—	25	28
10	31	—	32	30
11	33	—	32	34
12	37	—	32	36
13	38	—	43	39
14	42	—	43	41

SDS

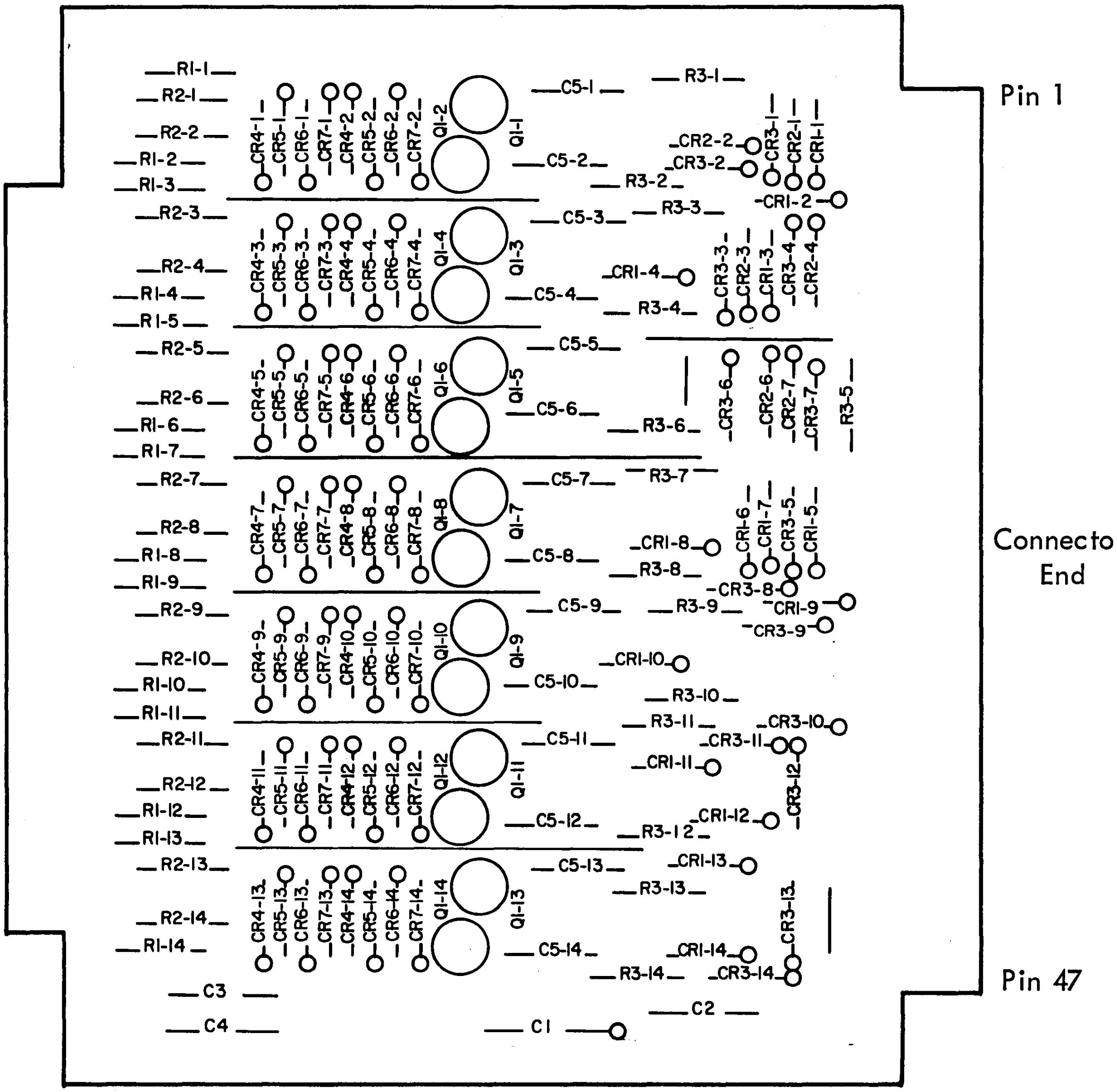
SCHEMATIC, NAND #4

DRAWN Keith 4/30/64
CHECK 6/4/64

SIZE D 104894 B

1B59

NEXT ASSY. 104896



NAND No. 4 IB59
104896D

REV	D
DWG. NO.	104896
	ML

MATERIAL LIST
DWG. TITLE

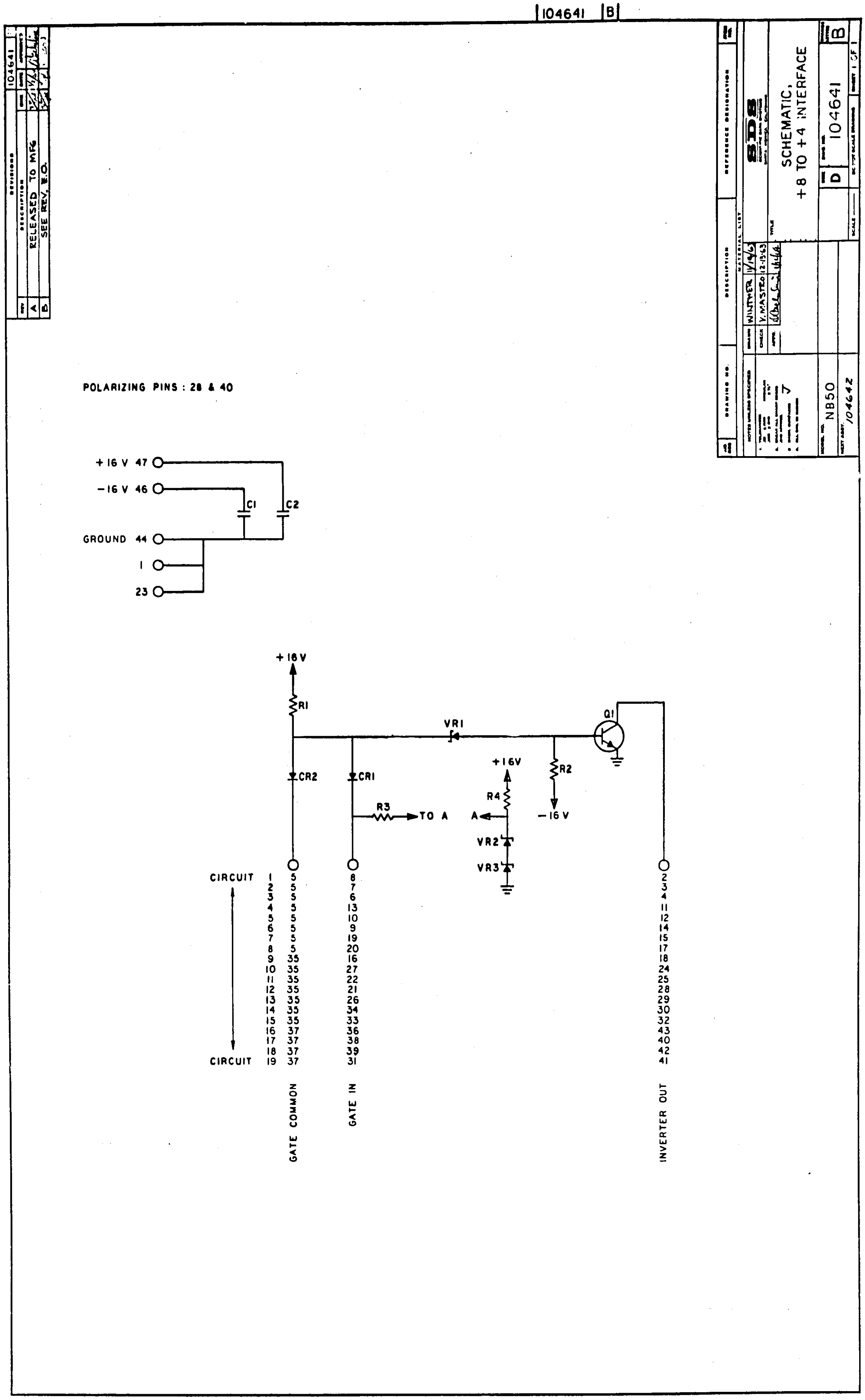
SDS SCIENTIFIC DATA SYSTEMS

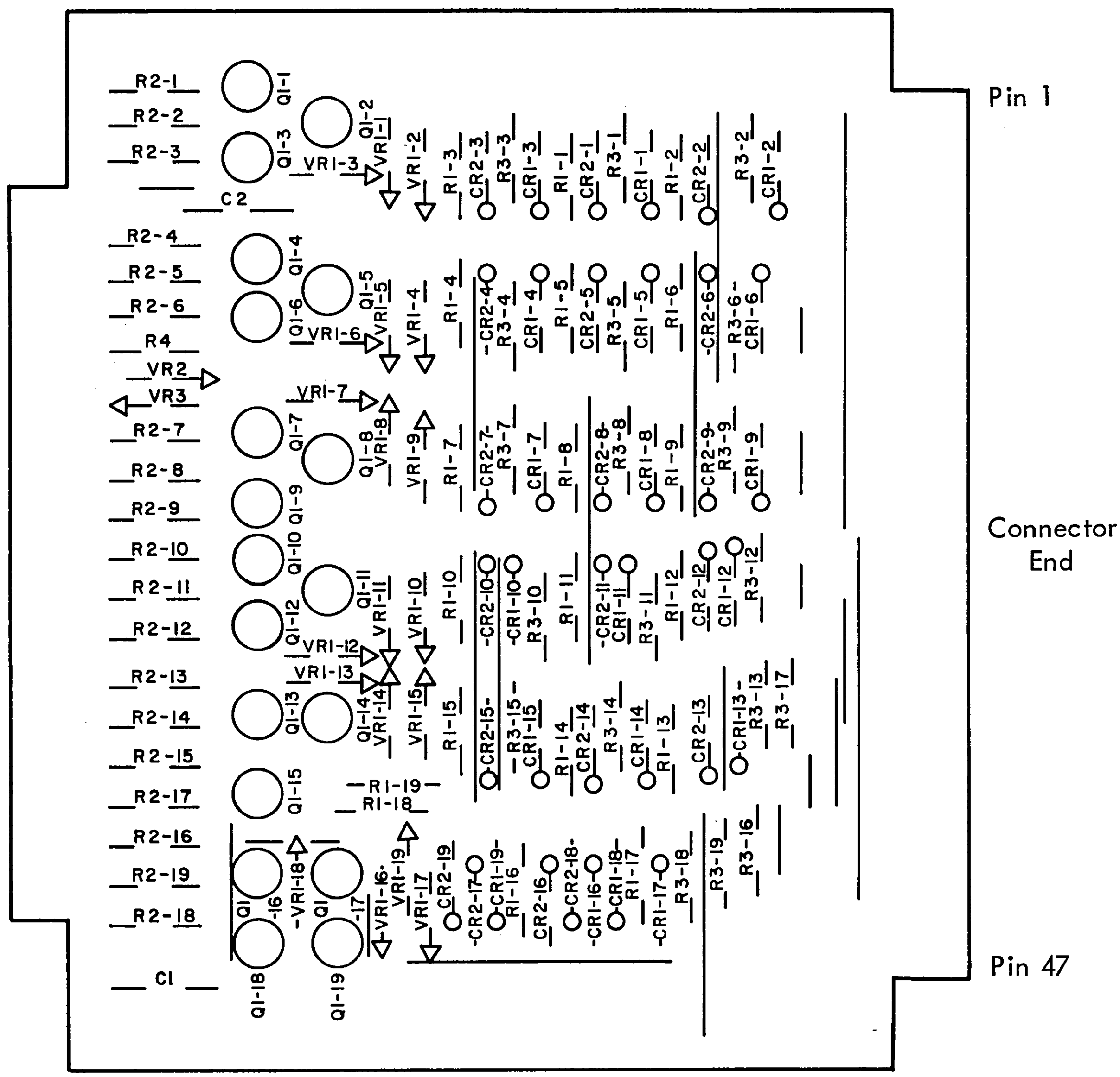
ML	DWG. NO.	REV
	104896	D

ASSY, P. W. NAND #4 MOD # IB59 DATE 2-10 SHEET 2 OF

ITEM	DWG. TITLE	DWG. NO.	NO. REQ	REMARKS OR CKT. DESIG.
1	Board, Printed Wiring	104895	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn Upper	100097	23	
6	Contact, Conn Lower	100098	24	
7	Transistor, SDS 216	103242	14	Q1
8	Diode, SDS 103	100091	76	CR1 thru CR4, 6, 7
9	Capacitor, Silver Mica	100107-470	14	C5
10	Capacitor, Mylar	100308-103	3	C2, 3, 4
11	Capacitor, Tantalum	100312-156	1	C1
12	Resistor, ½ watt	100111-332	14	R1
13	Resistor, ½ watt	100111-563	14	R2
14	Resistor, ½ watt	100111-470	14	R3
15	Wire, Solid Bare	100042-024	24 in	
16	Tubing, Teflon	100274-022	24 in	

104641 B


REVISIONS
A RELEASED TO MFG
B SEE REV. E.O.
104641
SDS
SCHEMATIC,
+8 TO +4 INTERFACE
D 104641 B
WINTNER
V. MASTRO
NB50
104642
POLARIZING PINS : 28 & 40
+16 V 47
−16 V 46
GROUND 44
1
23
C1
C2
+16 V
R1
VR1
Q1
CR2
CR1
+16V
R2
R4
R3
TO A
A
−16 V
VR2
VR3
CIRCUIT
CIRCUIT
1 5 8 2
2 5 7 3
3 5 6 4
4 5 13 11
5 5 10 12
6 5 9 14
7 5 19 15
8 5 20 17
9 35 16 18
10 35 27 24
11 35 22 25
12 35 21 28
13 35 26 29
14 35 34 30
15 35 33 32
16 37 36 43
17 37 38 40
18 37 39 42
19 37 31 41
GATE COMMON
GATE IN
INVERTER OUT



+8 To +4 Interface NB50
104642C

REV	DWG. NO.	
C	104642	ML

MATERIAL LIST

DWG. TITLE ASSY, +8 To +4 INTERFACE

SDS SCIENTIFIC DATA SYSTEMS

ML	DWG. NO.	REV
	104642	C

MOD # NB50 DATE ____ SHEET 2 OF 2

ITEM	DWG. TITLE	DWG. NO.	NO. REQ	REMARKS OR CKT. DESIG.
1	Board, Printed Wiring	104762	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn Upper	100097	23	
6	Contact, Conn Lower	100098	24	
7	Transistor, SDS 216	103242	19	Q1
8	Diode, SDS 103	100091	38	CR1, CR2
9	Diode, SDS 115	107063	21	VR1, VR2, VR3
10	Capacitor, Mylar	100308-103	2	C1, 2
11	Resistor, $\frac{1}{2}$ watt	100111-332	19	R1
12	Resistor, $\frac{1}{2}$ watt	100111-393	19	R2
13	Wire, Solid Bare	100042-024	18 in.	
14	Tubing, Teflon	100274-022	18 in.	
15	Resistor, $\frac{1}{2}$ watt	100111-153	19	R3
16	Resistor, $\frac{1}{2}$ watt	100111-471	1	R4

104864 C

A	RELEASED TO MFG	
B	SEE REV E.O.	
C	SEE REV EO	

SDS

SCHEMATIC, DRIVER-CABLE INTERFACE

SIZE D · DWG NO. 104864 · REV C

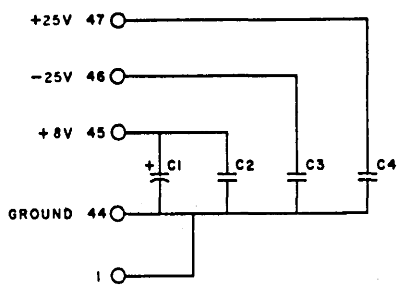
MODEL NO. NB52 & NB58

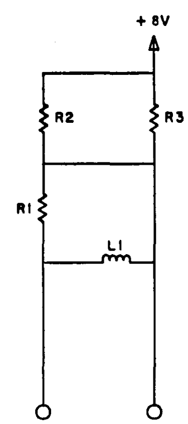
NEXT ASSY. 104866

POLARIZING PINS 34 & 38

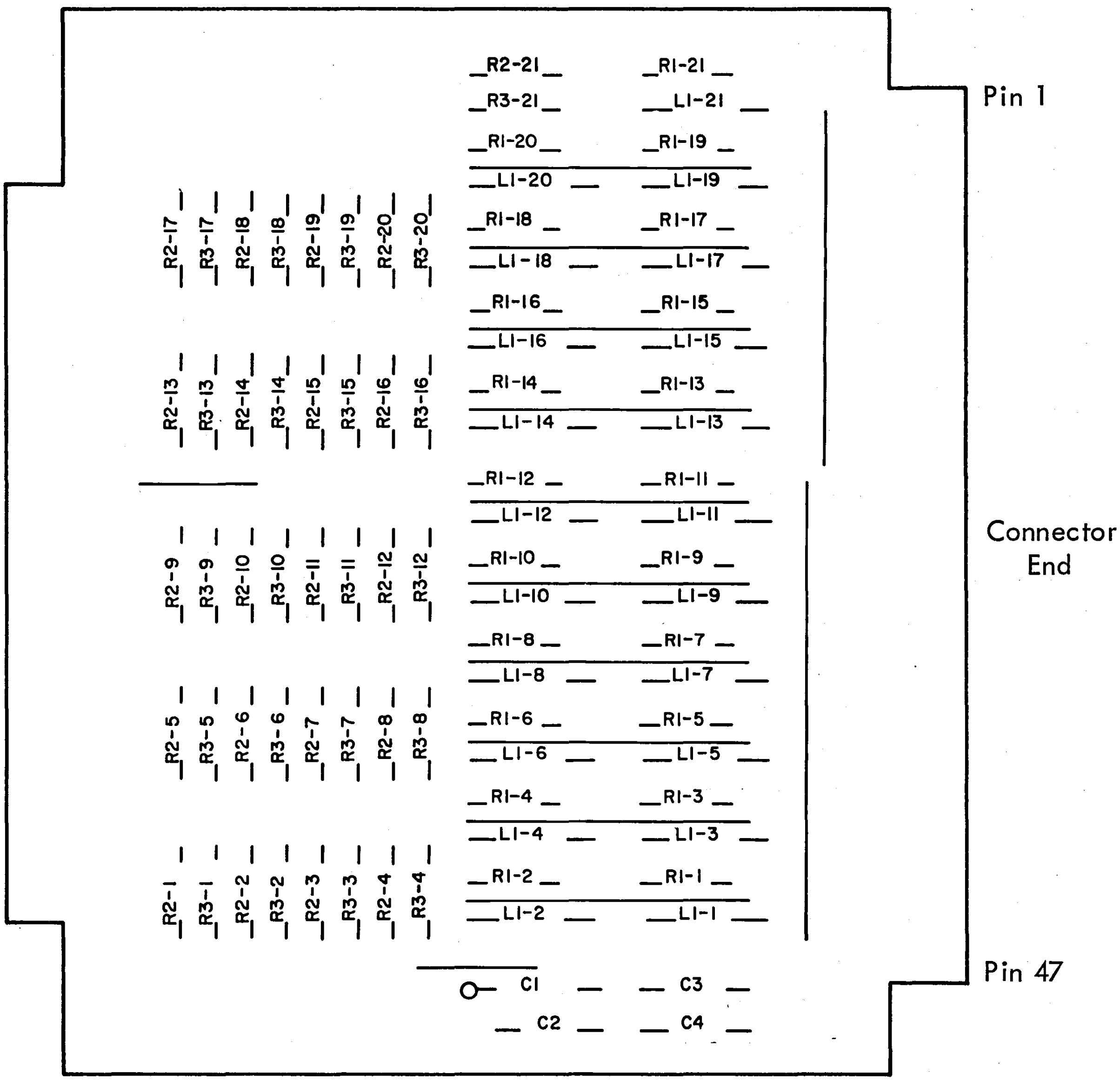
NOTES

1. R3 IS OMITTED ON NB58.





CIRCUIT		
1	42	43
2	40	41
3	38	39
4	36	37
5	34	35
6	32	33
7	30	31
8	28	29
9	26	27
10	24	25
11	22	23
12	20	21
13	18	19
14	16	17
15	14	15
16	12	13
17	10	11
18	8	9
19	6	7
20	4	5
21	2	3



Drive Cable Interface NB52
104866B

REV B | MATERIAL LIST DWG. TITLE | SDS SCIENTIFIC DATA SYSTEMS | ML | DWG. NO. 104866 | REV B

ASSY, P.W. DRIVER CABLE INTERFACE Mod # NB52 DATE 1/2/4 SHEET 2 OF 2

DWG. NO. 104866 ML

ITEM	DWG. TITLE	DWG. NO.	NO. REQ	REMARKS OR CKT. DESIG.
1	Board, Printed Wiring	104865	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn Upper	100097	23	
6	Contact, Conn Lower	100098	24	
7	Capacitor, Mylar	100308-103	3	C2, 3, 4
8	Capacitor, Tantalum	100312-156	1	C1
9	Resistor, $\frac{1}{2}$ watt	100111-151	21	R1
10	Inductor, Molded	100342-223	21	L1
11	Wire, Solid Bare	100042-024	5 in.	
12	Tubing, Teflon	100274-022	5 in	
13	Resistor, $\frac{1}{2}$ watt	100111-102	42	R2, 3

REVISIONS

REV.	DESCRIPTION	DATE	APPROVED
A	RELEASED TO MFG		

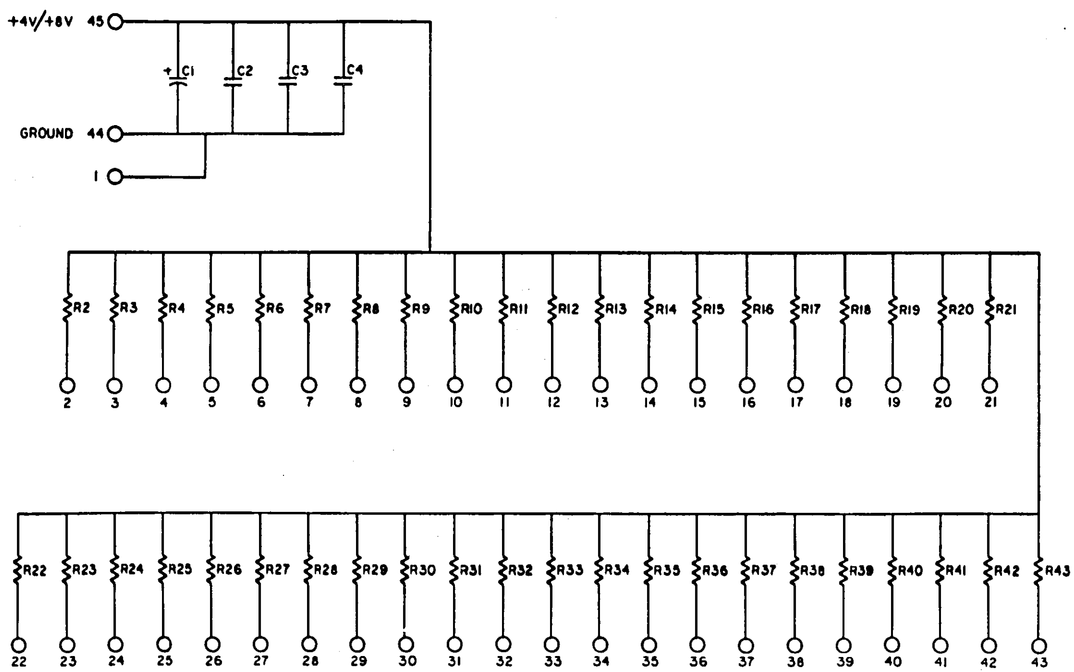
SCHEMATIC, TERMINATION MODULE

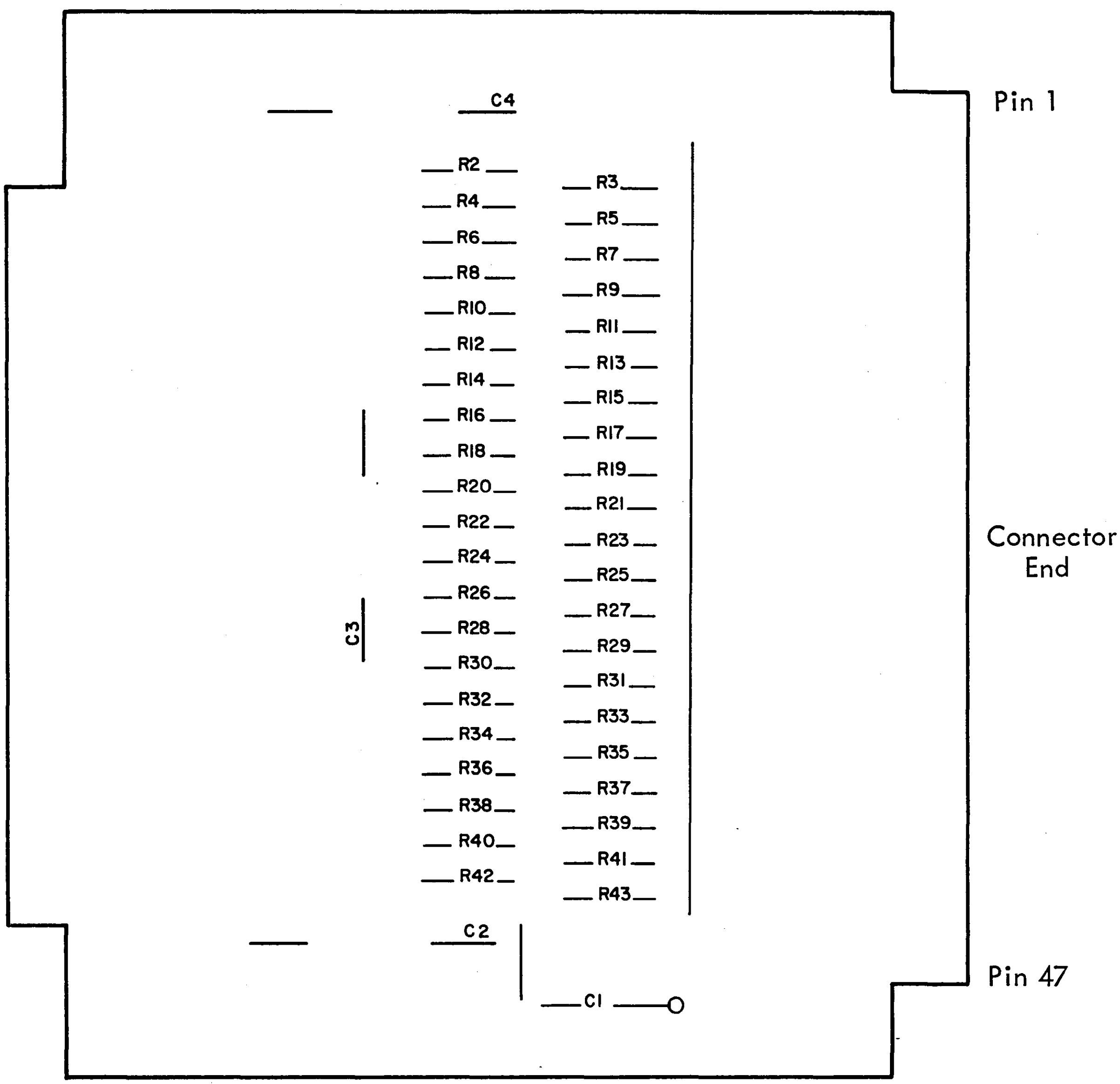
DRAWING NO. 104014 — SIZE D — REV A

MODEL NO. ZB50/ZB51

NEXT ASSY: 104016 104411

POLARIZING PINS: 12 & 40





Termination Module +4 ZB50
104016A

MATERIAL LIST

DWG. TITLE
ASSEMBLY,
P. W. TERMINATION MODULE +4

SDS SCIENTIFIC DATA SYSTEMS

ML DWG. NO. 104016 REV A

MOD Ø ZB50 DATE 11/18/63 SHEET 2 OF 2

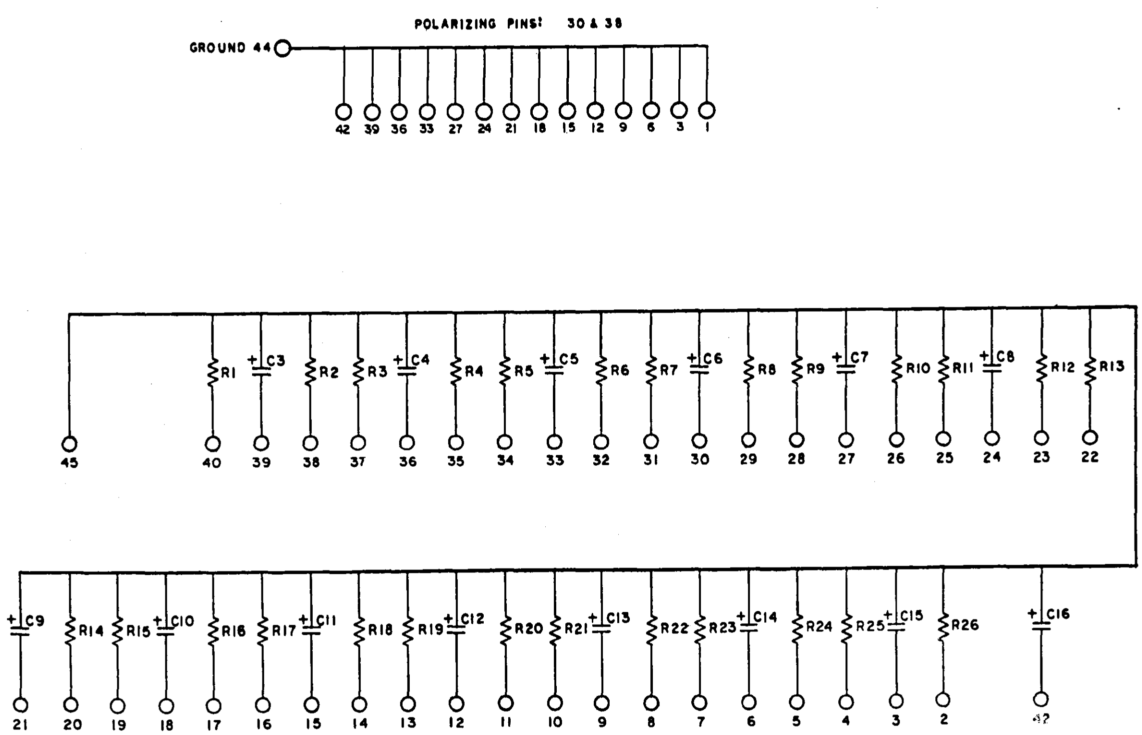
ITEM	DWG. TITLE	DWG. NO.	NO. REQ	REMARKS OR CKT. DESIG.
1	Board, Printed Wiring	104015	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn. Upper	100097	23	
6	Contact, Conn. Lower	100098	24	
7	Capacitor, Mylar	100308-334	3	C2, 3, 4
8	Capacitor, Tantalum	100312-156	1	C1
9	Resistor, ¼ watt	100111-151	42	R2 thru R43
10	Wire, Solid Bare	100042-025	5 in.	
11	Tubing, Teflon	100274-022	5 in.	

REV A DWG. NO. 104016 ML

SDS-E-106

104329 C

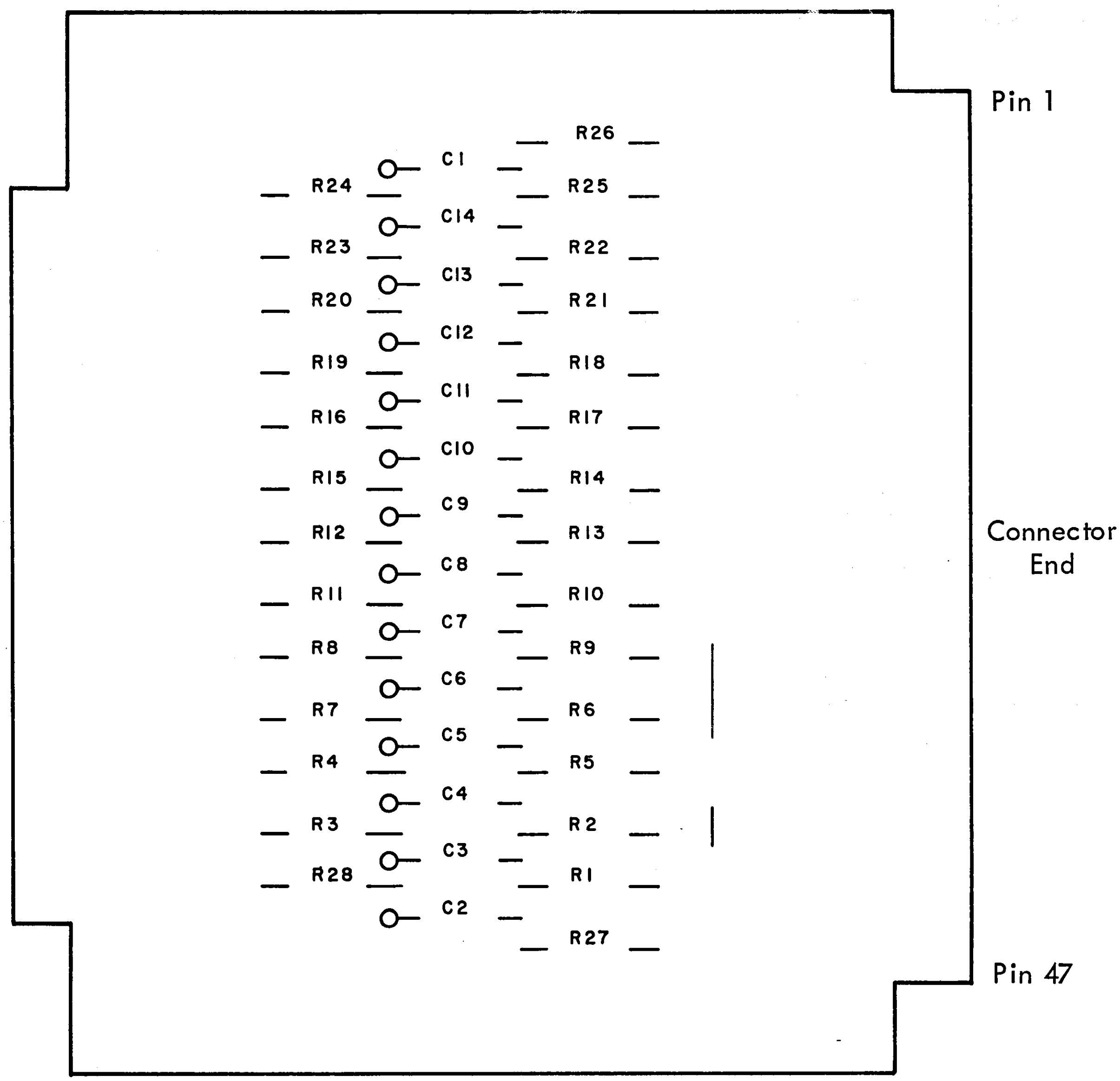
REV.	DESCRIPTION	DATE	APPROVED
A	PRERELEASED		
B	ADDED R27, R28, C16 & REMOVED JUMPER FROM PIN 43 TO PIN 45 RELEASED TO MFG.		
C	SEE REV E.O.		



DRAWN WWW 10/19/65
CHECK V. KASTRO
MODEL NO. ZB52
NEXT ASSY. 104331

SDS
SCHEMATIC, CABLE TERMINATION MODULE

SIZE D | DWG. NO. 104329 | C
SHEET 1 OF 1



Cable Termination Module ZB52
104331E

REV E

DWG. NO. 104331

ML

MATERIAL LIST

DWG. TITLE
ASSEMBLY, P. W. CABLE
TERMINATION MODULE

SDS SCIENTIFIC DATA SYSTEMS

ML

DWG. NO. 104331

REV E

MOD # ZB52 DATE 12/3 SHEET 2 OF 2

ITEM	DWG. TITLE	DWG. NO.	NO. REQ	REMARKS OR CKT. DESIG.
1	Board, Printed Wiring	104330	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn. Upper	100097	23	
6	Contact, Conn. Lower	100098	24	
~~7~~	~~Capacitor, Mylar~~	~~100308-103~~	~~14~~	~~C3 thru C16~~
8	Capacitor, Tantalum	100312-156	14	C1 thru C14
9	Resistor, Metal Film	100680-330	26	R1 thru R26
10	Wire, Solid Bare	100042-024	1 in	
11	Tubing, Teflon	100274-022	1 in	
~~12~~	~~Plate, Heatsink~~	~~106573~~	~~1~~	
13	Heatsink (Extruded)	106579	1	
14	Screw, Flat Hd. Phillips 100°	100012-307	2	
15	Washer, Flat	100018-300	2	
16	Washer, Lock Int Tooth	100024-300	2	
17	Nut, Hex Machine	100008-300	2	

304

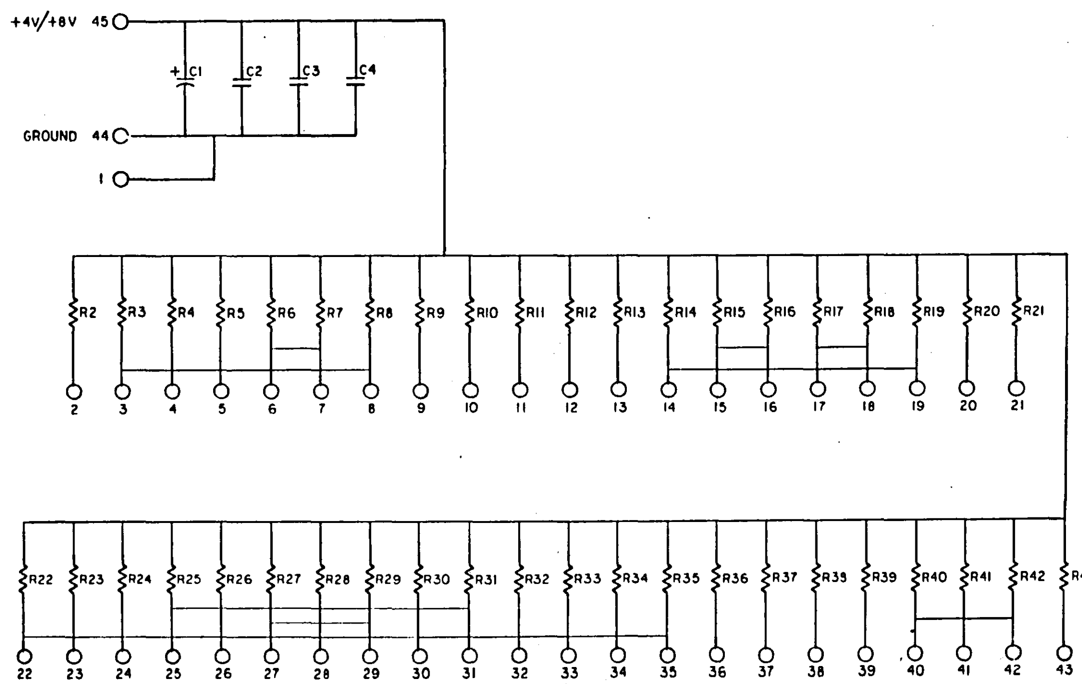
104993 A

REV.	DESCRIPTION
A	RELEASED TO MFG

NOTES:

1. R3, R5 THRU R9, R11, R14 THRU R33, R35, R40, R41 & R42 ARE OMITTED.

POLARIZING PINS: 12 & 40



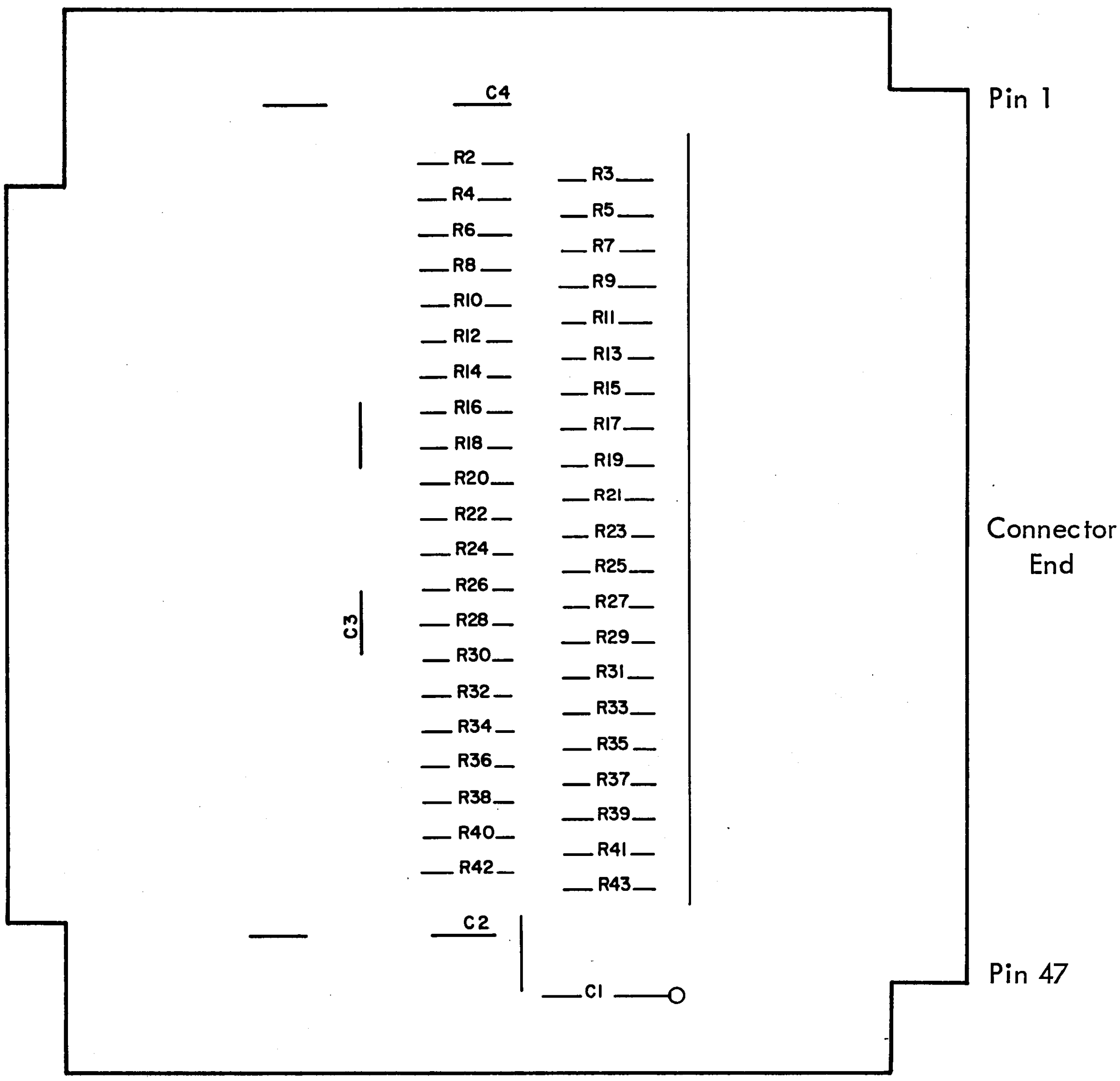
SCHEMATIC,
TERMINATION MODULE

D 104993 A

SHEET 1 OF 1

DRAWN WWW 10/9/73

NEXT ASSY. ZB55 104994



Termination Module ZB55
104994B

MATERIAL LIST

DWG. TITLE

ASSY, P. W.
TERMINATION MODULE

SDS SCIENTIFIC DATA SYSTEMS

ML

DWG. NO. 104994 REV 2

MOD # ZB55 DATE 3/24 SHEET 2 OF 2

ITEM	DWG. TITLE	DWG. NO.	NO. REQ.	REMARKS OR CKT. DESIG.
1	Board, Printed Wiring	104015	1	
2	Handle, Circuit Board	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn Upper	100097	23	
6	Contact, Conn Lower	100098	24	
7	Capacitor, Mylar	100308-334	3	C2, 3, 4
8	Capacitor, Tantalum	100312-156	1	C1
9	Resistor, ¼ watt	100111-151	11	R2, 4, 10, 12, 13, 34, 36, 37, 38, 39, 43
10	Wire, Solid Bare	100042-024	13 in	
11	Tubing, Teflon	100274-022	13 in	

DWG. NO. 104994

ML

SDS-E-106

113043 A

REVISIONS

REV	DESCRIPTION
A	RELEASED

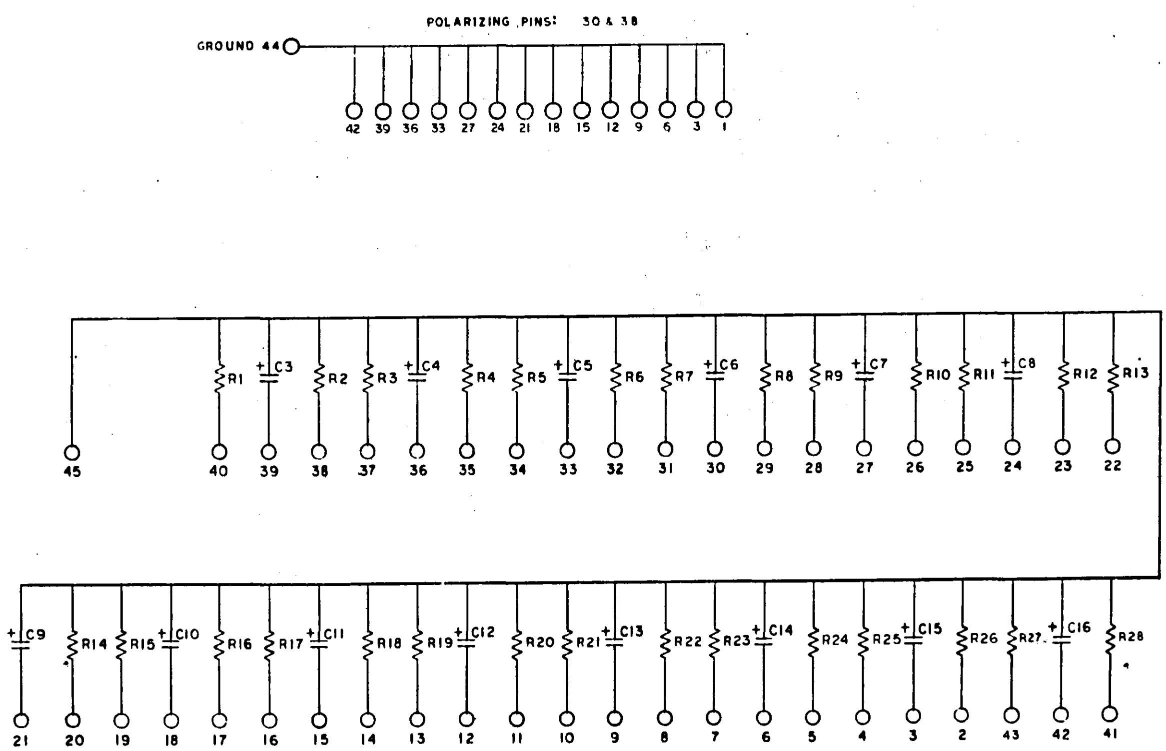
SCHEMATIC, CABLE TERMINATION MODULE

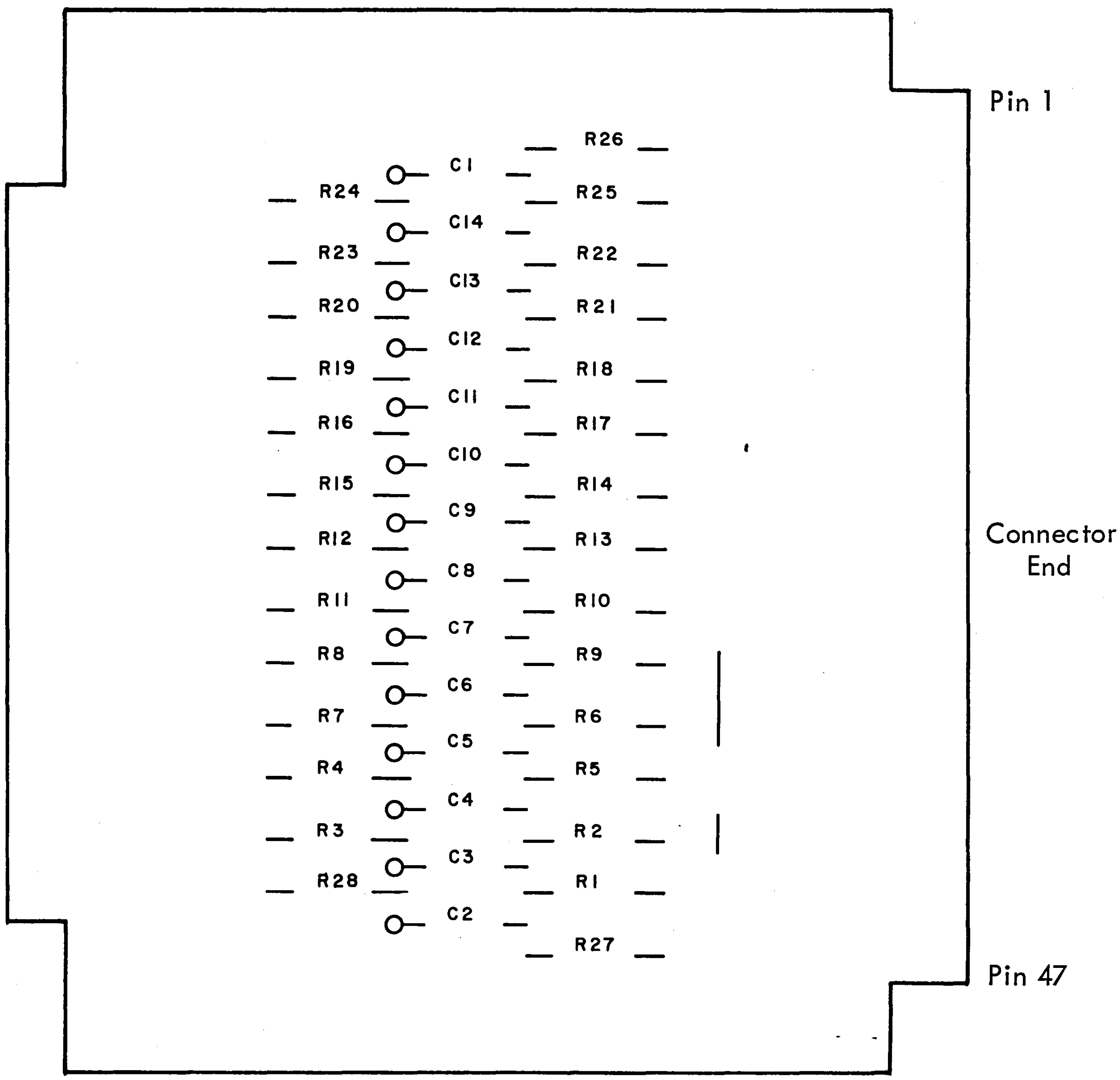
SIZE	D
DWG NO	113043
REV	A
MODEL NO.	2873
NEXT ASSY	111991
	DO NOT SCALE DWG
	SHEET 1 OF 1

DRAWN

CHECK

APPR





Cable Termination Module ZB73
111991A

SDS SCIENTIFIC DATA SYSTEMS

MATERIAL LIST

ML

DRAWING NO. 111991 REV. A

DRAWING TITLE Assy, P.W. Cable Termination Module MODEL NO. ZB73 DATE 2/1/65 SHEET 2 OF 2

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
1	Board, Printed Wiring	104330	1	
2	Handle, Circuit Card	100016	1	
3	Eyelet, Tubular	103896-016	2	
4	Strip, Marker	100197	1	
5	Contact, Conn. Upper	100097	23	
6	Contact, Conn. Lower	100098	24	
7	Capacitor, Tantaium	100312-156	14	C1 thru C14
8	Resistor, Metal Film	100680-330	28	R1 thru R28
9	Wire, Solid Bare	100042-024	1in	
10	Tubing, Teflon	100274-022	1in	
11	Heatsink(Extruded)	106579	1	
12	Screw, Flat Hd. Phillips 100°	100012-307	2	
13	Washer, Flat	100018-300	2	
14	Washer, Lock Int. Tooth	100024-300	2	
15	Nut, Hex Machine	100008-300	2	
16	Schematic	113043	x	ref
17	Dwg List	113044	x	ref
18	Test Spec	113045	x	ref

REV. A DRAWING NO. 111991 ML

SDS-E-106B