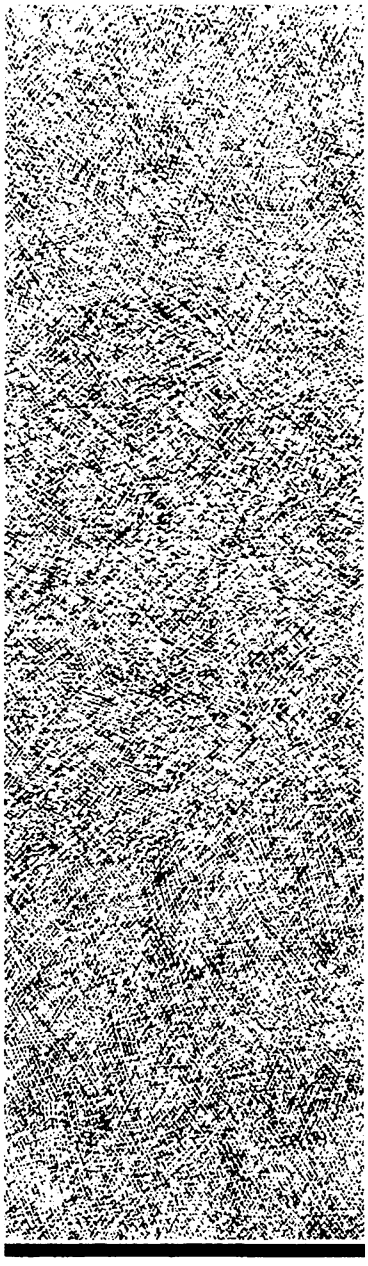
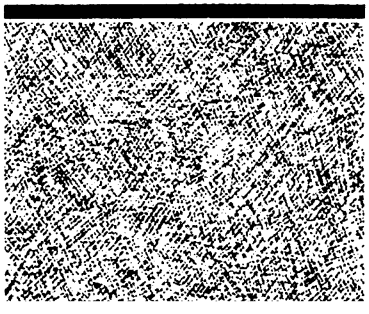


MOTOROLA



MVME025/D1

MVME025
VMEbus System Controller Module User's Manual

MVME025/D1

NOVEMBER 1984

MVME025

VMEbus SYSTEM CONTROLLER MODULE

USER'S MANUAL

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First Edition

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Field Service Division for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

PREFACE

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

Signal names in parentheses denote internal module (onboard) signals.

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the Motorola MVME025 System Controller module. The manual includes a general description, specifications, hardware preparation and installation instructions, and a functional description. A typical module is shown in Figure 1-1.

1.2 FEATURES

The features of the MVME025 include:

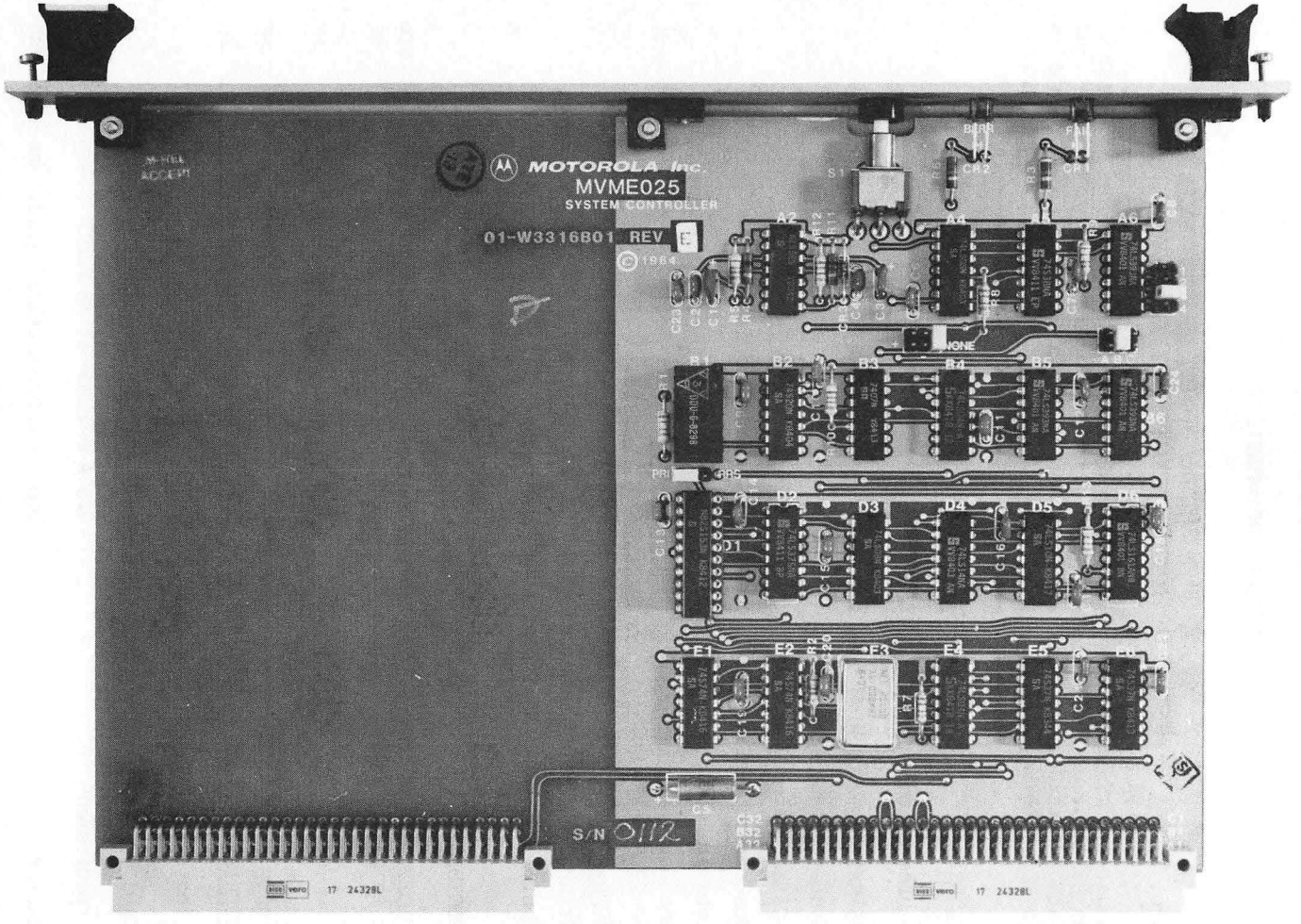
- 16-MHz symmetrical system clock
- System reset generation
- AC-fail detect
- Bus timeout selectable from 4 to 8192 microseconds
- Longword error detect
- Bus arbiter (selectable for fixed-priority or round-robin mode of operation)
- Supports all four levels of bus request and allocation
- Printed-circuit jumper from IACK* to IACKOUT*
- Monitored SYSFAIL* line with LED indicator

1.3 SPECIFICATIONS

The MVME025 is a VMEbus-compatible module. The specifications (which are subject to change without notice) are given in Table 1-1.

TABLE 1-1. MVME025 Specifications

CHARACTERISTIC	SPECIFICATIONS
Operating temperature	0° to 55° C (32° to 131° F)
Operating humidity	8 to 80% (non-condensing)
Power requirement	0.5 A maximum at +5 Vdc
Form factor	Double-width Eurocard (233.4 mm x 160 mm)



8-84-2883

FIGURE 1-1. MVME025 System Controller Module

1.4 GENERAL DESCRIPTION

The MVME025 is a single-module system controller that provides general system utilities necessary for VMEbus-compatible modules to operate in a VMEbus card cage.

1.5 REFERENCE MANUALS

The following manual is applicable to the MVME025.

HB212/D	VMEbus Specification Manual

CHAPTER 2

HARDWARE PREPARATION AND INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides unpacking, hardware preparation, and installation instructions for the MVME025.

2.2 UNPACKING INSTRUCTIONS

NOTE

If shipping carton is damaged upon receipt, request carrier's agent be present during unpacking and inspection of module(s).

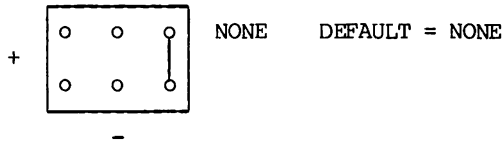
Unpack the MVME025 from its shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping of the module.

CAUTION

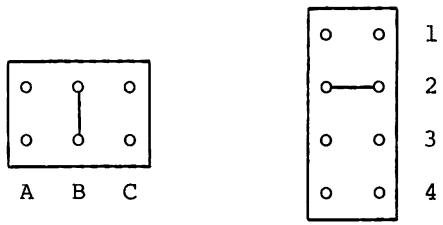
AVOID TOUCHING AREAS OF INTEGRATED CIRCUITRY; STATIC DISCHARGE CAN DAMAGE CIRCUITS.

2.3 HARDWARE PREPARATION

The MVME025 contains three jumper-selectable configuration options -- AC-FAIL, bus timeout, and bus arbitration mode. These are described in the following three paragraphs. The as-shipped factory jumper header configurations are illustrated in Figure 2-1. Figure 2-2 shows jumper header locations.



A. AC-FAIL POLARITY



DEFAULT = B2

B. BUS TIMEOUT

C. BUS ARBITRATION MODE

FIGURE 2-1. Initial Factory Jumper Placements

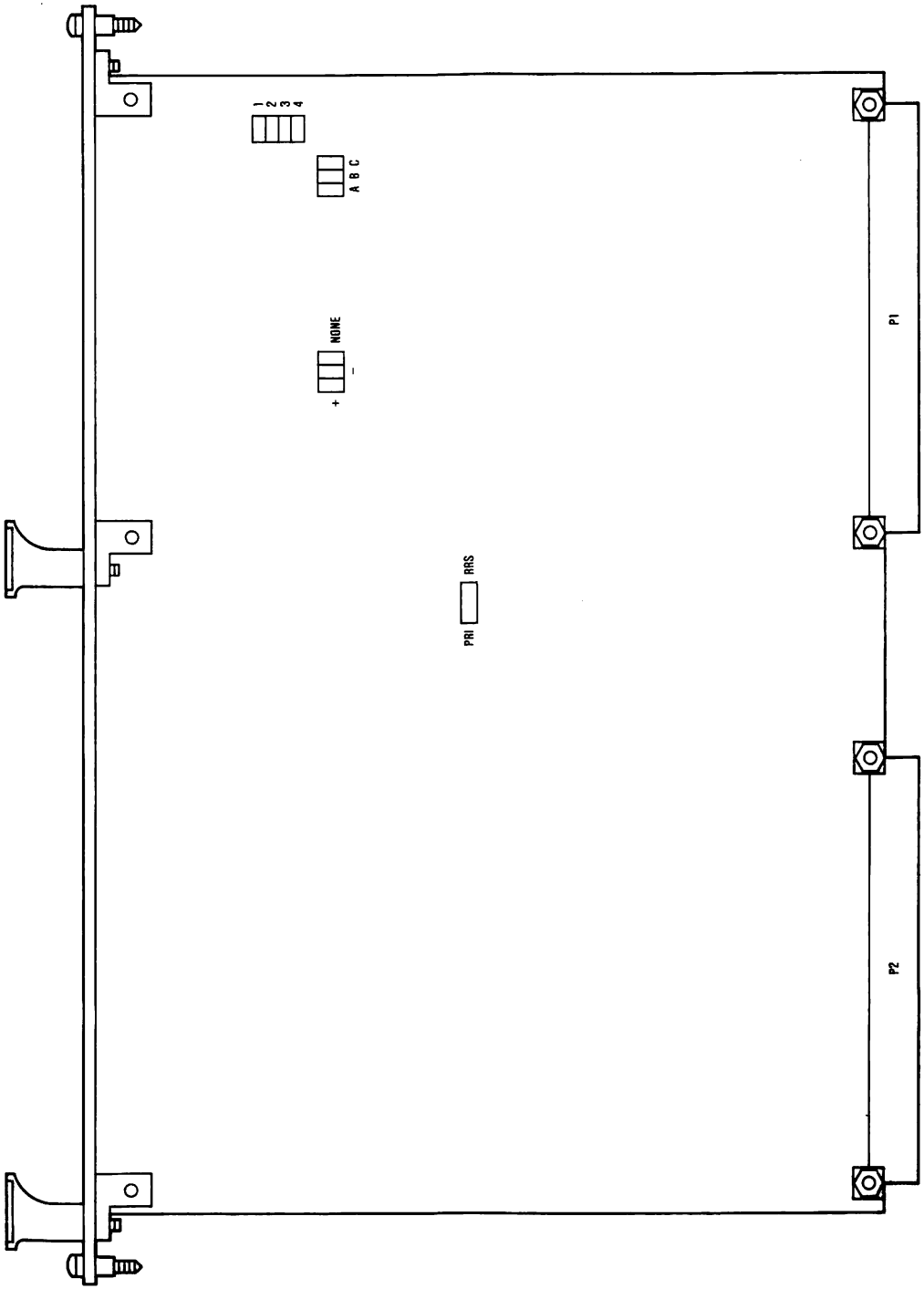


FIGURE 2-2. MVME025 Jumper Header Locations

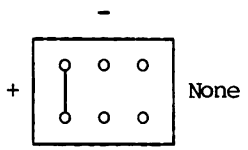
2.3.1 AC-FAIL Polarity

The external AC-FAIL input is provided on connector P2 and is typically driven by the system power supply. The input can be jumpered to one of three modes: positive-true, negative-true, or disabled.

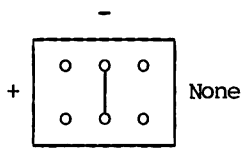
2

The following illustrations show how to install jumpers to select one of three AC-FAIL options -- + (positive-true), - (negative-true), or disabled.

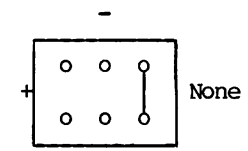
a. Positive-true mode



b. Negative-true mode



c. Disabled mode



2.3.2 Bus Timeout

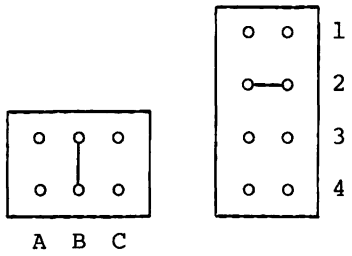
The MVME0250 contains a bus watchdog timer which will terminate a data transfer cycle if a response (DTACK* or BERR*) is not received from a slave within a specified amount of time. To accommodate various system requirements, the timer duration is jumper-selectable for periods of 4 to 8192 microseconds, in steps of powers of 2 (4, 8, 16, etc.).

The timer duration is selected by two jumpers -- one in the jumper block labeled "1 2 3 4" and the other in the jumper block block labeled "A B C".

Use the table below to determine jumpering requirements for the timer duration selected.

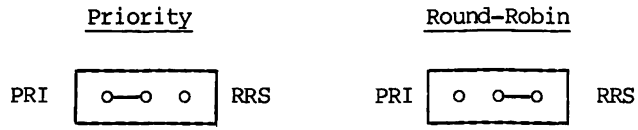
	A	B	C
1	4	64	1024
2	8	128	2048
3	16	256	4096
4	32	512	8192

For example, for 128 microseconds, select B2:



2.3.3 Bus Arbitration Mode

The bus arbitration subsystem is designed to prevent simultaneous access of the VMEbus by two or more masters; it schedules requests from multiple masters for optimum bus usage. The MVME025 contains a jumper block for selecting one of two bus arbitration modes -- PRI (priority) or RRS (round-robin). Select one of the following jumper options.



2.4 INSTALLATION INSTRUCTIONS

Install the MVME025 in slot number 1 of the VMEbus backplane. Only one controller module should be installed per VMEbus card cage (in VMEbus systems using VMEbus-compatible modules).

CHAPTER 3

FUNCTIONAL DESCRIPTION

3.1 INTRODUCTION

This chapter provides a functional description of the system controller and the various modes of operation. For further detail, refer to the schematic diagrams in Chapter 4 and to the VMEbus Specification Manual.

3.2 FUNCTIONAL DESCRIPTION

The MVME025 system controller module consists of four functional blocks.

- Clock generation.
- AC-FAIL and system reset control.
- Bus timeout and error control.
- Bus arbitration.

Each functional block is described in the following four paragraphs.

3.2.1 Clock Generation

The clock signal is provided per the VMEbus specification. SYSCLK is a 16-MHz symmetrical clock signal used for general system timing.

3.2.2 AC-FAIL and System Reset Control

The external AC-FAIL input is provided on connector P2 and is typically driven by the system power supply. The two external inputs on connector P2 are TTL-compatible. The input can be jumper-configured for either a positive-true or a negative-true signal, or it can be disabled for systems not requiring this feature.

When the external AC-FAIL input goes true, the MVME025 will respond by driving the bus ACFAIL* line low. After a 2-millisecond delay, the MVME025 will then drive the SYSRESET* line low.

An active-low system reset (SYSRESET*) signal approximately 500 milliseconds in duration is generated by any of the following conditions.

- Power up.
- Closing of a manually operated switch located on the front edge of the module.
- Detection of the external-reset signal going low (located on connector P2).
- Activation of the external AC-FAIL signal.

3.2.3 Bus Timeout and Error Control

The MVME025 timer, longword error, and indicators are described in the following paragraphs.

3.2.3.1 Timer. The MVME025 contains a bus watchdog timer which will terminate a data transfer cycle if a response (DTACK* or BERR*) is not received from a slave within a specified amount of time. To accommodate various system requirements, the timer duration is jumper-selectable for periods of 4 to 8192 microseconds in steps of powers of 2 (4, 8, 16).

The timer is started when either AS*, DS1*, or DS0* goes low and is normally stopped when DTACK* or BERR* goes low. Should a timeout occur, BERR* is driven low and remains low until AS*, DS1*, and DS0* are high, regardless of the state of DTACK*.

3.2.3.2 Longword Error. In systems using the 32-bit data transfer capabilities of the VMEbus, BERR* will be driven low in the event a master attempts a longword (LWORD* = LOW) transfer on an odd boundary (A01 = HIGH). BERR* will remain low until AS*, DS1*, and DS0* are high, regardless of the state of DTACK*.

3.2.3.3 Indicators. For convenience, two LED indicators are provided on the front edge of the MVME025 module. The first LED lights whenever BERR* is low. The second LED indicator monitors the SYSFAIL* line and lights to indicate that a failure has occurred in the system.

3.2.4 Bus Arbitration

The bus arbitration subsystem is designed to prevent simultaneous access of the VMEbus by two or more bus masters; it also schedules requests from multiple masters for optimum bus usage. Onboard jumpers implement one of two bus arbitration modes -- PRI (priority) or RRS (round-robin). In either case, the arbiter supports all four levels of bus request and allocation, with a typical turnaround time of 100 nsec.

3.2.4.1 Priority Mode (PRI). In PRI mode, the arbiter grants the bus to the highest pending level of request, where BR3* is highest and BR0* is lowest. When a master has been granted to the bus, the master indicates that it has control of the bus by driving BBSY* low. To prevent a master from locking the bus, the arbiter will drive the BCLR* signal low upon receipt of a request on a level higher than that of the current bus master. The present master should then relinquish the bus in a reasonable period of time.

While this method is sufficient in most cases, consider a master that uses BR3* as its request level. Since no other master can generate a higher request, the BCLR* signal will never be driven low while this master has control of the bus. In this case, the master must exercise one of the following options:

- Relinquish the bus after a fixed number of transfers and wait some reasonable period before initiating another request.
- Monitor the four bus-request lines and relinquish the bus within a reasonable period after detecting any other request.
- Allocate high-priority tasks which are short in duration and infrequent in occurrence.
- Assign itself to a lower priority level.

3.2.4.2 Round-Robin Mode (RRS). In RRS mode, the arbiter shifts its priority sequence based on the level of the current bus master. When the bus is busy, the priority is equal to the level currently in use. Upon release of the bus, the priority is stepped one position lower (e.g., from BR2* to BR1*) and if a request is pending, the arbiter issues a grant at that level. If no request is pending at that level, the arbiter will "jump" to the next lower requesting level.

In the RRS mode, the BCLR* signal is not used. Each master must therefore either perform fixed-length transfers or take other action to prevent a lockup condition.

CHAPTER 4

SUPPORT INFORMATION

4.1 INTRODUCTION

This chapter contains connector pin signal descriptions, schematic diagrams, and a parts list for the MVME025 module.

4.2 CONNECTOR PIN SIGNALS

Table 4-1 lists the VMEbus signals on connector P1 giving the signal mnemonic, connector and pin number, and signal characteristic. The signals on connector P2 are listed in Table 4-2.

4.3 PARTS LISTS

Table 4-3 lists the components of the MVME025. Figure 4-1 is the parts location diagram. The parts list reflects the latest issue of hardware at the time of printing.

4.4 SCHEMATIC DIAGRAMS

Figure 4-2 (2 sheets) contains a detailed schematic diagram for the MVME025. This schematic diagram represents the latest design. Occasionally, minor component changes are made at the factory. Therefore, when replacing a component, always use the same value as the defective component even though the schematic diagram may indicate a different value on type.

TABLE 4-1. Connector P1 Signals

SIGNAL MNEMONIC	CONNECTOR AND PIN NUMBER	SIGNAL NAME AND DESCRIPTION
ACFAIL*	1B: 3	AC FAILURE - Open-collector driven signal which indicates that the AC input to the power supply is no longer being provided or that the required input voltage levels are not being met.
IACKIN*	1A: 21	INTERRUPT ACKNOWLEDGE IN - Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKIN* signal indicates to the VME module that an acknowledge cycle is in progress.
IACKOUT*	1A: 22	INTERRUPT ACKNOWLEDGE OUT - Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKOUT* signal indicates to the next module that an acknowledge cycle is in progress.

TABLE 4-1. Connector P1 Signals (cont'd)

SIGNAL MNEMONIC	CONNECTOR AND PIN NUMBER	SIGNAL NAME AND DESCRIPTION
AS*	1A: 18	ADDRESS STROBE - Three-state driven signal that indicates a valid address is on the address bus.
A01	1A: 30	ADDRESS LINE (bit 1) - Three-state driven address lines that specify a memory address.
BBSY*	1B: 1	BUS BUSY - Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BCLR*	1B: 2	BUS CLEAR - Totem-pole driven signal generated by the bus arbitrator to request release by the current DTB master in the event that a higher level is requesting the bus.
BERR*	1C: 11	BUS ERROR - Open-collector driven signal generated by a slave. This signal indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BGOUT*-BG3OUT*	1B: 5,7 9,11	BUS GRANT (0-3) OUT - Totem-pole driven signals Generated by Requesters. Bus grant in and out signals form a daisy-chained bus grant. The bus grant out signal indicates to the next module that it may become the next bus master.
BR0*-BR3*	1B: 12-15	BUS REQUEST (0-3) - Open-collector driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.
DS0*	1A: 13	DATA STROBE 0 - Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D00-D07).
DS1*	1A: 12	DATA STROBE 1 - Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D08-D15).
DTACK*	1A: 16	DATA TRANSFER ACKNOWLEDGE - Open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.

TABLE 4-1. Connector P1 Signals (cont'd)

SIGNAL MNEMONIC	CONNECTOR AND PIN NUMBER	SIGNAL NAME AND DESCRIPTION
GND	1A: 9,11, 15,17,19 1B: 20,23 1C: 9	GROUND
IACK*	1A: 20	INTERRUPT ACKNOWLEDGE - Open-collector or Three-state driven signal from any MASTER processing an interrupt request. Routed via backplane to Slot 1, where it is looped back to become Slot 1 IACKIN* to start the interrupt acknowledge daisy-chain. use.
LWORD*	1C: 13	LONGWORD - Three-state driven signal to indicate
SYSCLK	1A: 10	SYSTEM CLOCK - A constant 16-MHz clock signal that is independent of processor speed or timing. This signal is used for general system timing that the current transfer is a 32-bit transfer.
SYSFAIL*	1C: 10	SYSTEM FAIL - Open-collector driven signal that indicates that a failure has occurred in the system. This signal may be generated by any module on the VMEbus.
SYSRESET*	1C: 12	SYSTEM RESET - Open-collector driven signal which, when low, will cause the system to be reset.
+5V STDBY	1B: 31	+5 Vdc STANDBY - This line supplies +5 Vdc to devices requiring battery backup.
+5V	1A: 32 1B: 32 1C: 32	+5 Vdc Power - Used by system logic circuits.

TABLE 4-2. Connector P2 Signals

SIGNAL MNEMONIC	CONNECTOR AND PIN NUMBER	SIGNAL NAME AND DESCRIPTION
--	P2-A1	EXTERNAL AC-FAIL - TTL input from external power monitor unit indicating loss of AC power.
--	P2-A2	EXTERNAL RESET* - TTL input from user-supplied external source.

TABLE 4-3. MVME025 Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
--	84-W8316B01	PWB for MVME025
A2	51NW9615C60	I.C., MC3456P
A4,D3	51NW9615C22	I.C., SN74LS08N
A5	51NW9615F85	I.C., SN74S38N
A6,B5,B6	51NW9615F38	I.C., SN74LS393N
B1	01NW9804C15	Delay module, tripple, 60NS
B2	51NW9615D92	I.C., SN74S20N
B3	51NW9615B59	I.C., MC7407P
B4,E4	51NW9615C21	I.C., SN74LS04N
C1	21NW9702A09	Capacitor, ceramic, 10,000 pF at 100 Vdc
C2,C4,C6-C24	21NW9702A09	Capacitor, ceramic, 0.1 uF at 50 Vdc
C3	21NW9604A11	Capacitor, ceramic, 0.47 uF at 50 Vdc
C5	23NW9618A61	Capacitor, 10 uF at 25 Vdc
CR1,CR2	48NW9612A19	LED, red
CR3	48NW9616A03	Diode, 1N4148/1N914
D1	51AW4644B15	Programmed I.C.
D2	51NW9615G12	I.C., SN74LS375N
D4	51NW9615E93	I.C., SN74LS14N
D5	51NW9615E88	I.C., SN74LS10N
D6	51NW9615C28	I.C., SN74LS161N
E1,E2	51NW9615C95	I.C., SN74S74N
E3	48AW1016B01	Crystal oscillator, 16 MHz (0.05)
E5,E6	51NW9615J12	I.C., SN74S37N
P1,P2	28NW9802E51	Connector, 96-pin

TABLE 4-3. MVME025 Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
R1,R2,R5,R7,R8, R9,R10,R12,R13	06SW-124A57	Resistor, film, 2.2K ohms, 1/4 w, 5%
R3	06SW-124A41	Resistor, film, 470 ohms, 1/4 w, 5%
R4	06SW-124B46	Resistor, film, 10 megohms, 1/4 w, 5%
R6	06SW-124A35	Resistor, film, 270 ohms, 1/4 w, 5%
R11	06SW-124B22	Resistor, film, 1.0 megohm, 1/4 w, 5%
S1	40NW9801B24	Pushbutton switch, SPDT, momentary
--	38NW9404B97	Cap, snap-on, black (for S1)
--	09NW9811A78	Socket, I.C., DIL, 20-pin (for D1)
--	28NW9802C43	Header, double row, 8-pin
--	28NW9802B21	Header, double row, 6-pin
--	28NW9802D04	Header. single row, 3-pin
--	29NW9805B17	Jumper, shorting, insulated

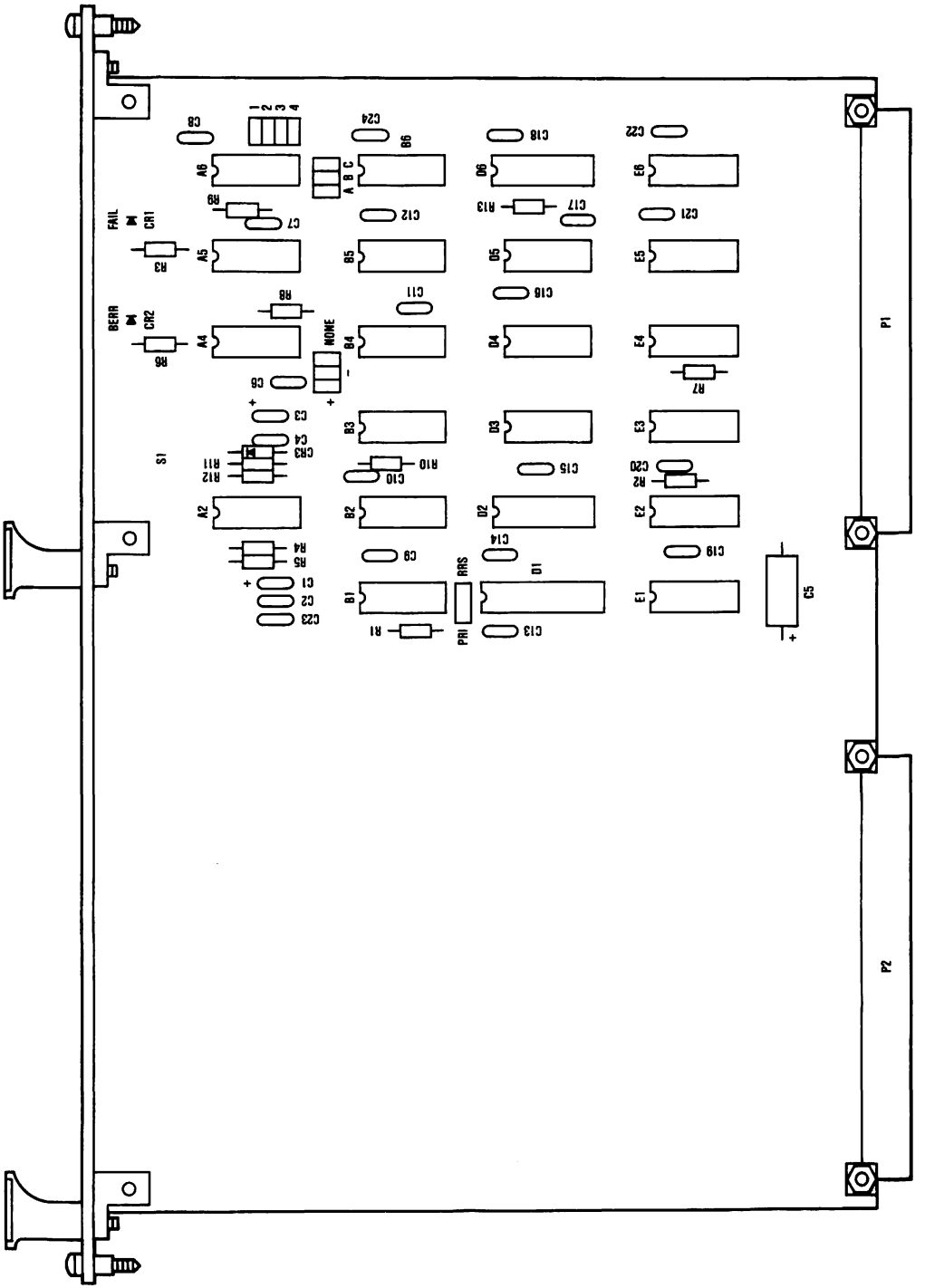


FIGURE 4-1. MVME025 Parts Location Diagram

NOTES:

1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL 01-W3316B01
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ± 5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
	C	PER ECN 300085	2-7-83	
	D	REVISED AND REIDENTIFIED 84273284 FOR CONTROL AND PRODUCTION ASSEMBLY BY MICROSYSTEMS. DWS 3-7-84 JFV	3-22-84	
	E	PCCN221: ES, PING N.C. WAS B21 SERCLK. C/P SAH 11/7/84 GMP.	11-08-84	

DWG NO. 63DW3316B

REV STATUS OF SHEETS: E | E; 1 | 2

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DIMENSIONS IN INCHES	
METRIC DIMENSIONS (MILLIMETERS)	
REMOVE ALL BURRS AND SHARP EDGES.	DRAWN BY D. SCHONIGER DATE 3-7-84
SURFACE TEXTURE IN MICROINCHES	CHECKED BY J. VILLESCAS DATE 3-16-84
TOLERANCE: 2 PLACE DEC. ± 3 PLACE DEC. ± HOLES ± ANGLES ±	PROJECT LEADER P. WASILEWSKI DATE 3/16/84
	DESIGN MANAGER N. WAGNER DATE 3/20/84
	MFG ENGINEER G. CHAILLIE DATE 3/20/84
	DESIGN ENGINEER P. WASILEWSKI DATE 3/14/84

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FIGURE 4-2. MVME025 Schematic Diagram (Sheet 1 of 2)

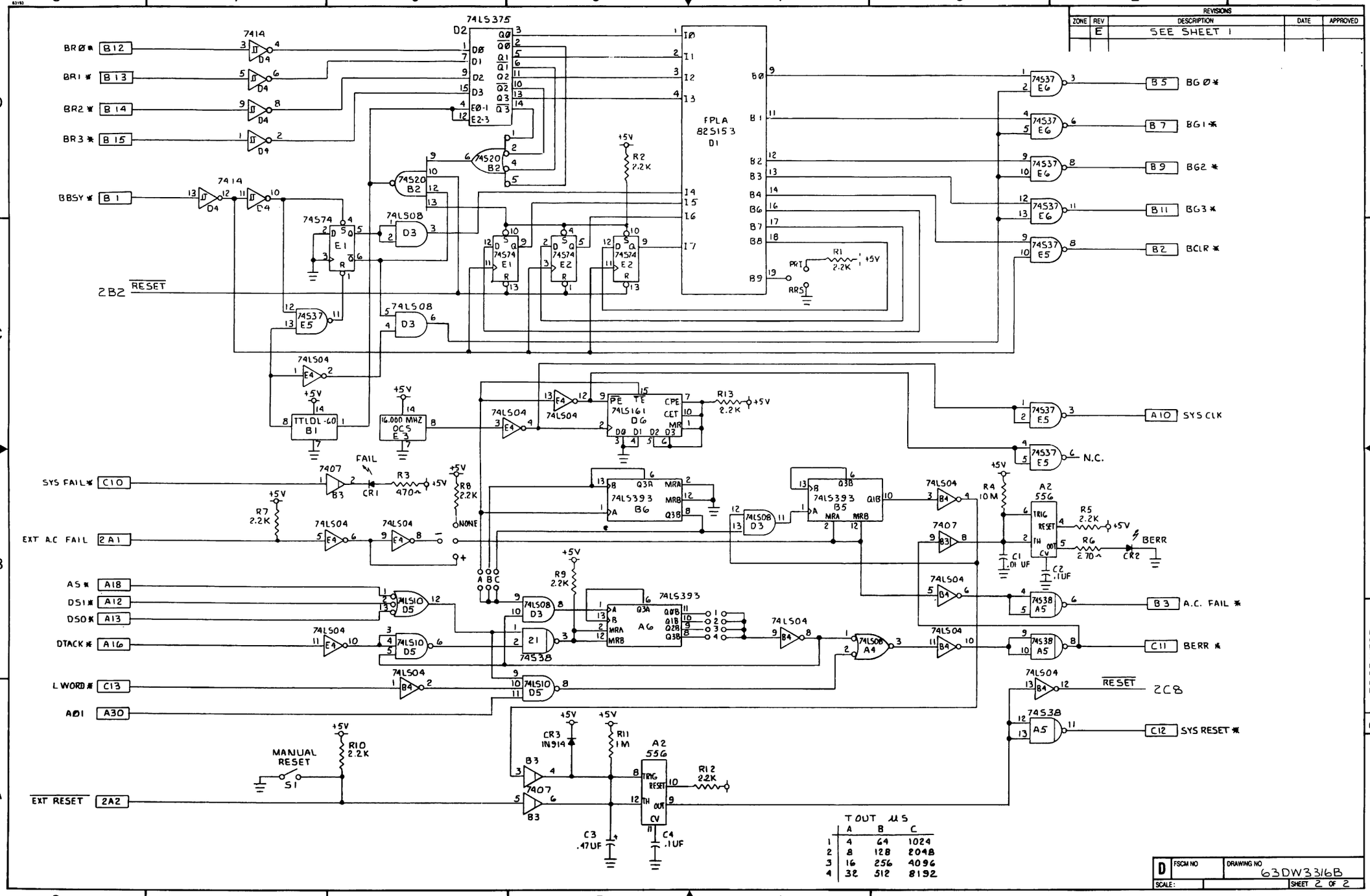

FIGURE 4-2. MVME025 Schematic Diagram (Sheet 2 of 2)

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