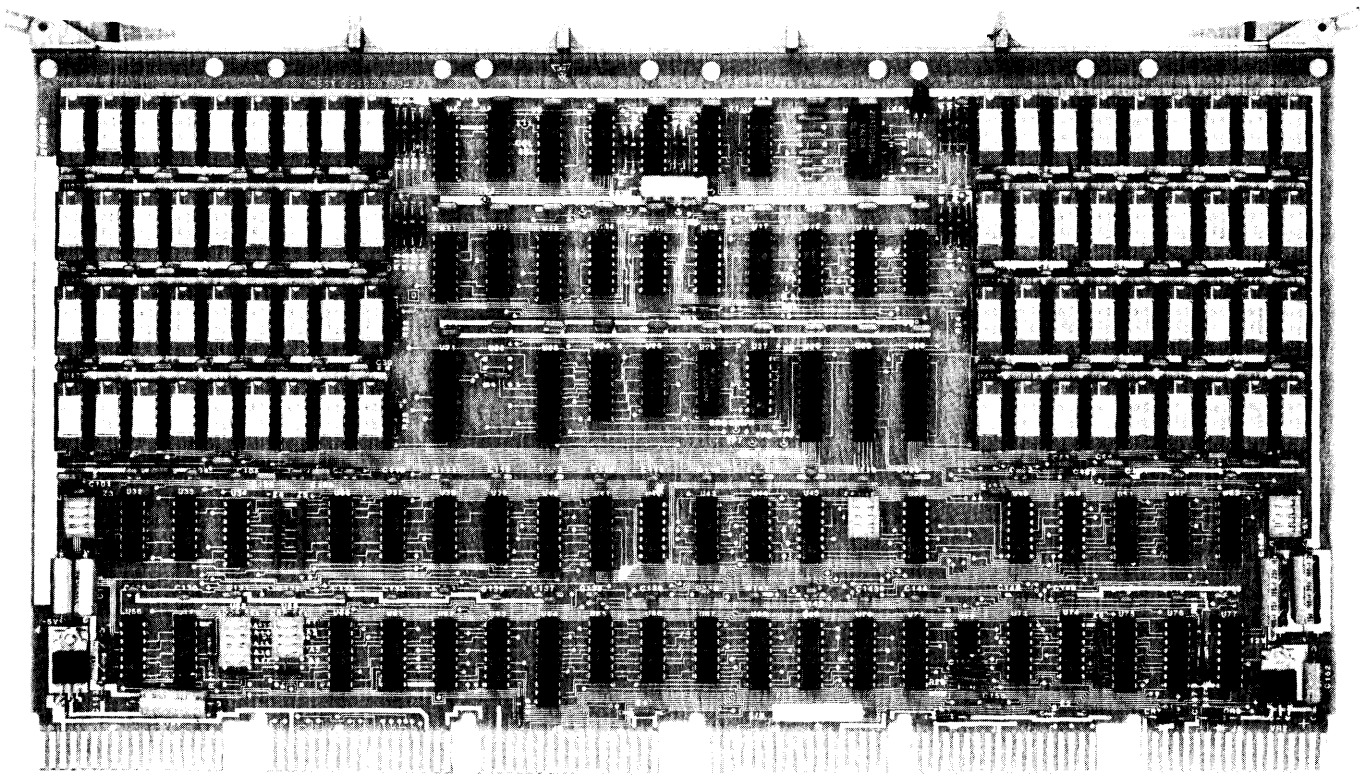
MMS1117

128K x 18
PDP-11 ADD-IN SEMICONDUCTOR MEMORY
MANUAL



MOTOROLA
Memory Systems
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MMS1117

USER MANUAL

PRODUCT: MMS1117 Family
Artwork Revisions A and B

DOCUMENT: Edition A
Revision 2

1 September 78

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CHAPTER I. SPECIFICATIONS

1.0 INTRODUCTION

This manual describes the specifications, installation and operation of the MMS1117 memory system.

The MMS1117 is a family of single-card memory systems, designed for, and fully compatible with, PDP-11* Unibus* mini-computers.

It is capable of storing up to 128 kilobytes of data on a single hex-height module. Parity storage as well as controller functions are optionally available on the same module.

The power and signal pin-outs are compatible with any hex-SPC slot and thus obviate the need for a specific memory back panel.

1.1 OPTION DESIGNATIONS

The several available options are designated with a 4 character suffix to the basic name as shown in the following table:

TABLE 1: MMS1117 OPTION DESIGNATOR SUFFIX

Typical Read Access Time	Parity Options:	Total Storage Capacity (in kilobytes) 32KB	64KB	96KB	128KB
290 nsec	parity + controller	-32-PC	-34-PC	-36-PC	-38-PC
	parity data only	-32-P	-34-P	-36-P	-38-P
	no parity	-32	-34	-36	-38
360 nsec	parity + controller	-42-PC	-44-PC	-46-PC	-48-PC
	parity data only	-42-P	-44-P	-46-P	-48-P
	no parity	-42	-44	-46	-48
390 nsec	parity + controller	-52-PC	-54-PC	-56-PC	-58-PC
	parity data only	-52-P	-54-P	-56-P	-58-P
	no parity	-52	-54	-56	-58

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SPECIFICATIONS (cont'd)

1.2 PINOUT

All electrical signal connections to the system are made to the UNIBUS* pins available at the Small Peripheral Controller (SPC) connectors (i.e., connector row C, D, E and F).

TABLE 2: MMS1117 CONNECTOR PINOUT

SIGNAL	PIN	SIGNAL	PIN
A 00 L	EH2	D 06 L	CV2
A 01 L	EH1	D 07 L	CM2
A 02 L	EF1	D 08 L	CL2
A 03 L	EV2	D 09 L	CK2
A 04 L	EU2	D 10 L	CJ2
A 05 L	EV1	D 11 L	CH1
A 06 L	EU1	D 12 L	CH2
A 07 L	EP2	D 13 L	CF2
A 08 L	EN2	D 14 L	CE2
A 09 L	ER1	D 15 L	CD2
A 10 L	EP1		
A 11 L	EL1	DCLO L	CN1
A 12 L	EC1	INIT L	DL1
A 13 L	EK2	MSYN L	EE1
A 14 L	EK1	NPG IN	CA1
A 15 L	ED2	NPG OUT	CB1
A 16 L	EE2	PA L	CC1
A 17 L	ED1	PB L	CS1
		*PAR DET	BE2
BG 4 IN	DS2		
BG 4 OUT	DT2	*P0 L	AP1
BG 5 IN	DP2	*P1 L	AN1
BG 5 OUT	DR2	SSYN L	EJ1
BG 6 IN	DM2	*SSYN INT. L	BE1
BG 6 OUT	DN2		
BG 7 IN	DK2	+5 VDC	DA2, EA2
BG 7 OUT	DL2		FA2
		+5 BB	BD1
C0 L	EJ2	-15 VDC	FB2
C1 L	EF2		
		+20 VDC	AR1, AV1
D 00 L	CS2		CE1, CU1
D 01 L	CR2		
D 02 L	CU2	GND	AC2, AT1
D 03 L	CT2		BC2, BT1
D 04 L	CN2		CC2
D 05 L	CP2		DC2, DT1
			EC2, FT1

*These signals are used only when the MMS1117-XX-PC and MMS1117-XXP models are used in conjunction with an external parity control module. This configuration is available in certain "Modified Unibus" backpanels.

SPECIFICATIONS (cont'd)

1.3 PHYSICAL

The MMS1117 is implemented on one standard "Hex-height" printed circuit card, compatible with all PDP-11* backpanel connectors and card cages; it requires only one single (1/2") width connector slot.

1.4 ENVIRONMENTAL REQUIREMENTS

Storage Temperature Range:	0 to 70 degrees C.
Operating Temperature Range:	0 to 70 degrees C.
Relative Humidity:	0 to 90 percent without condensation

1.5 COMPATIBILITY

The MMS1117 interfaces electrically with the PDP-11* UNIBUS* as well as the newer modified Unibus* and is logically as well as electrically compatible with the AC and DC parameters specified by it.

1.6 STORAGE CAPACITY

Fully populated capacity is 128 kilobytes; optional 96, 64 or 32 kilobytes.

1.7 BUS LOADING

The MMS117 presents one standard bus load to the UNIBUS*. This parameter is independent of the memory size or parity options selected.

1.8 ADDRESSING

The MMS1117 interfaces to all 18 bus address lines. The memory's starting address can be selected via switches located in position U58, to fall on any 4K word boundary between 0 and 112K. In addition, 1 or 2 kilowords of the I/O page (at address 124K to 126K) can selectively be made available for random access storage. See Table 3 for specific selections.

TABLE 3: MMS1117 STARTING ADDRESS SELECTION

STARTING ADDRESS	BANK NO.	SWITCH POSITION (X = closed, 0 = open) U58/5	U58/4	U58/3	U58/2	U58/1
0K	0	0	0	0	0	0
4K	1	0	0	0	0	X
8K	2	0	0	0	X	0
12K	3	0	0	0	X	X
16K	4	0	0	X	0	0
20K	5	0	0	X	0	X
24K	6	0	0	X	X	0
28K	7	0	0	X	X	X
32K	8	0	X	0	0	0
36K	9	0	X	0	0	X
40K	10	0	X	0	X	0
44K	11	0	X	0	X	X
48K	12	0	X	X	0	0
52K	13	0	X	X	0	X
56K	14	0	X	X	X	0
60K	15	0	X	X	X	X
64K	16	X	0	0	0	0
68K	17	X	0	0	0	X
72K	18	X	0	0	X	0
76K	19	X	0	0	X	X
80K	20	X	0	X	0	0
84K	21	X	0	X	0	X
88K	22	X	0	X	X	0
92K	23	X	0	X	X	X
96K	24	X	X	0	0	0
100K	25	X	X	0	0	X
104K	26	X	X	0	X	0
108K	27	X	X	0	X	X
112K	28	X	X	X	0	0

1.9 PARTIAL USE OF I/O PAGE AS R/W MEMORY

The jumpers or switches in location U22/1 and U22/2 enable the address space from 124-125K and 125-216K as R/W memory:

TABLE 3A: I/O PAGE SELECTION

ADDRESS ENABLED:	(X = switch closed) U22/1	U22/2
none	0	0
124-125K	0	X
124-216K	X	X

Note: To make use of this feature, the address space to which the MMS1117 is configured must overlap the I/O page. For example. A MMS1117 with 32K words of memory must start at address 96K.

SPECIFICATIONS (cont'd)

1.10 Parity

The MMS1117-XX-PC incorporates all the features of the parity control module, thus eliminating the need for an external parity controller. This functional unit is totally self-contained and does not degrade the access or cycle times. Furthermore, it is completely compatible with DEC's equivalent parity controller. The parity control and status register (CSR) address can be switch selected to any of the standard preassigned bus addresses (i.e., 772100 through 772136). No additional bus loading is imposed upon the system by the parity controller.

The Parity Register base address is hardwired for 772100. The position of the switches in locations U59/1, U59/2, U59/3 and U59/4 determine the offset from this base address. See Table 4.

TABLE 4: PARITY REGISTER ADDRESS SELECTION

PARITY REGISTER ADDRESS	SWITCH POSITION (X = closed) U59/4	U59/3	U59/2	U59/1
772100	X	X	X	X
772102	X	X	X	0
772104	X	X	0	X
772106	X	X	0	0
772110	X	0	X	X
772112	X	0	X	0
772114	X	0	0	X
772116	X	0	0	0
772120	0	X	X	X
772122	0	X	X	0
772124	0	X	0	X
772126	0	X	0	0
772130	0	0	X	X
772132	0	0	X	0
772134	0	0	0	X
772136	0	0	0	0

AS Read 3-14-80

The parity register implements the following bits:

Bit <Ø> : Read/write, cleared by Bus INIT. Parity enable, when set to a 1 (via program), enables the parity controller to gate parity errors onto the Bus PB line. When set to a Ø, parity errors are logged but not flagged to the Bus PB line.

Bit <1> : Not used.

Bit <2> : Read/write, cleared by Bus INIT. Write wrong parity. When set to a 1 (via program), the parity generator logic generates and writes wrong parity on all subsequent write cycles to the MMS1117. This feature is intended for diagnostic purposes only.

Bit <3> : Not used.

Bits <11:Ø5> : Read/write. Parity error logger. These data bits store the seven most significant bits of the Bus address of the location where the last parity error occurred, i.e., Bus address lines A <17:12>.

Bits <14:12> : Not used.

Bit <15>: Read/write, cleared by Bus INIT. Parity error flag. This bit will be set by the parity controller whenever a parity error has occurred. It will remain set until explicitly cleared via program or a Bus INIT. It may also come up set upon initial power up. The L.E.D. on the edge of the MMS1117 is connected to this register and will be lit whenever this register is set to a logic 1.

Note that parity errors will be detected, and their address latched regardless of the state of the enable register (bit <Ø>).

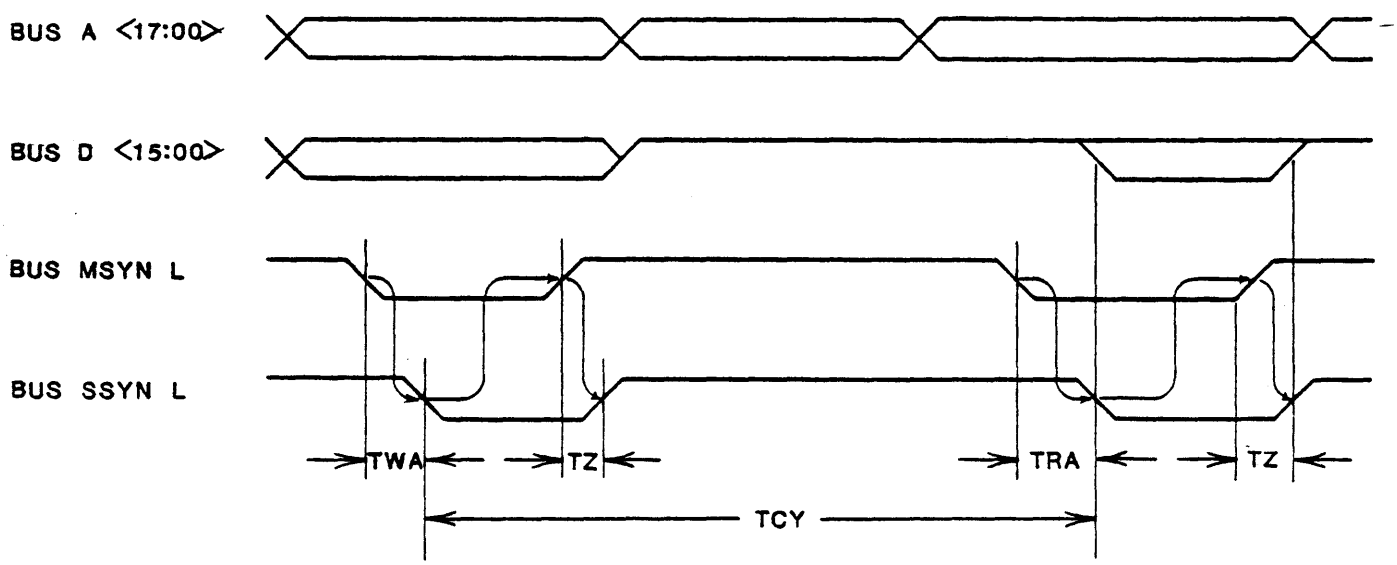
1.11 TIMING

The MMS1117 is fully compatible with the PDP-11 Unibus protocol and timing. DATO, DATOB and DATI are treated as single cycles, while the DATIP/DATO(B) combination is handled as an independent DATI cycle followed by a separate DATO(B) cycle. This sequence is completely transparent to the bus master.

See Table 5 and Figure 1 for specific timing information.

TABLE 5: MMS1117 TIMING

MMS1117 OPTION DESIGNATOR SUFFIX	TIMING (typ./W.C.) - nanoseconds			
	WRITE twa	READ tra	CYCLE tcy	RELEASE tz
-3x	105/125	290/315	375/390	50/75
-4x	115/135	360/390	480/500	50/75
-5x	115/135	390/420	560/585	50/75



Notes: Set up and hold times are as defined by the PDP-11 Unibus Specification. Cycle time is defined here as the maximum continuous access rate sustainable by the MMS1117.

FIG. 1 TIMING DIAGRAM

1.12 REFRESH LATENCY

The storage cells in the MMS1117 are implemented with dynamic MOS devices. The charge stored in the cells is automatically refreshed every 2 milliseconds. The latency induced to bus cycles concurrent with refresh cycles is no greater than the cycle time of the particular memory. A single refresh cycle is initiated approximately once every 16 microseconds.

1.13 POWER REQUIREMENTS

Table 6 shows the power requirements for the 3 required voltages.

TABLE 6: MMS1117 POWER REQUIREMENTS

NOMINAL VOLTAGE	VOLTAGE TOLERANCE MIN	VOLTAGE TOLERANCE MAX	CURRENT REQUIREMENTS STANDBY TYP/WC (AMPERES)	CURRENT REQUIREMENTS ACTIVE(1) TYP/WC (AMPERES)	INPUT PINS
+5 VDC	4.75	5.25	1.0/1.2	1.0/1.2	DA2,EA2,FA2(2)
+5 BB(4)	4.75	5.25	1.0/1.2	1.0/1.2	BD1 (5)
+15 VDC(4)	15	20	.150/.200	.350/.700	AV1,AR1,CE1,CU (3)
-15 VDC(4)	-7	-20	.015/.030	.015/.030	FB2

NOTES:

(1) active denotes that the MMS1117 is accessed at the maximum continuous rate. Standby mode assumes only internal refresh cycles.

(2) these 3 power input pins for +5 VDC are all connected together within the MMS1117

(3) the +15 VDC is automatically selected from among the listed pins that has the highest potential (through a set of isolation diodes)

(4) These voltages must be present during a power failure, in order to maintain data in the memory.

(5) The MMS1117 comes preconfigured such that the +5 BB power is obtained from the +5 VDC power. Pin BD1 is active only when the corresponding jumper wire is explicitly installed. See the section on battery backup configuration for details.

CHAPTER II: THEORY OF OPERATION

2.1 Address Decoding. See logic diagram, sheet 1.

The MMS1117 can be configured to start on any 4K boundary within the total available address space of Ø to 128K. The range of addresses that the MMS1117 will respond to is determined at the low end by the switch selected starting address, and at the high end by the starting address plus the total board capacity.

Figure 1 outlines the logic that performs this address decoding.

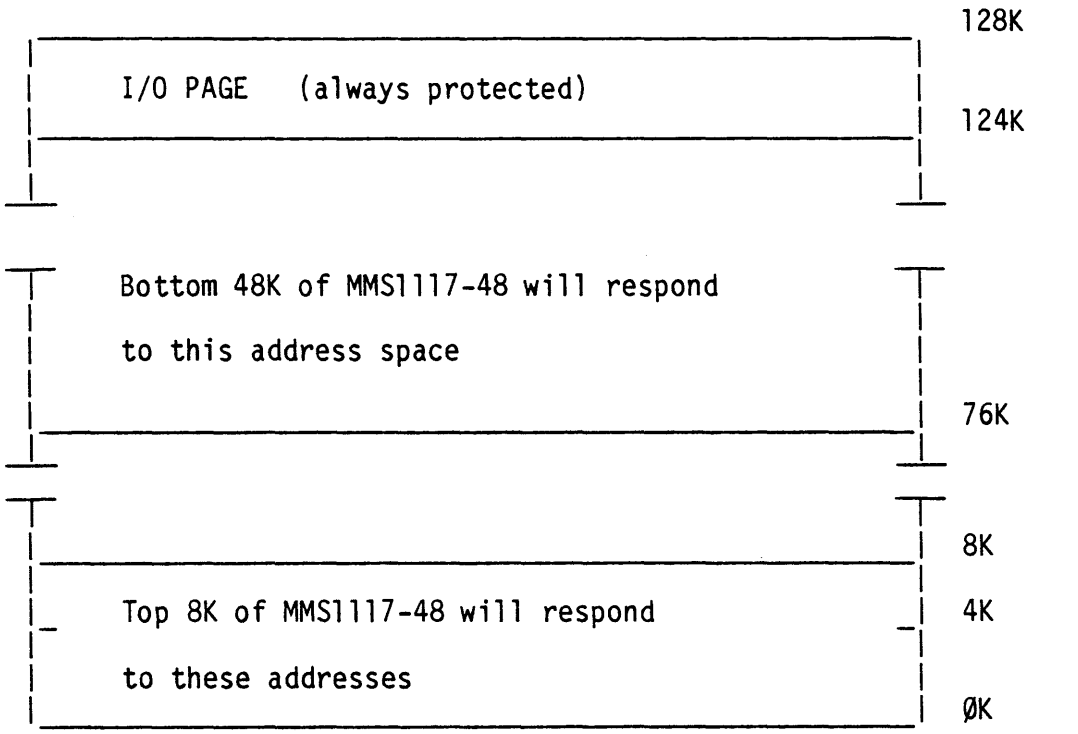
The five most significant Bus address lines are required to decode one of the possible 32 starting banks (i.e.: 0K, 4K, 8K....120K, 124K). This decoding is performed with a 5-bit adder network consisting of U33 and U34. One set of inputs to this adder comes from the Bus receivers for lines A<17:12>, while the other set originates at the 5 position switch located at position U58. The combined output of this network consists of the carry bit appearing at pin 8 of U33. The memory selection is inhibited whenever this carry bit is high. Conversely, the carry bit must be low to enable memory selection.

The address selection switch at position U58 is encoded such that its binary representation corresponds to the number of the starting bank: All switches open corresponds to a starting bank of 0, all switches closed corresponds to a starting bank of 37 octal (equal to 124K).

The Bus addresses within the range of 124K and 128K, i.e.: bank 37 octal, are generally reserved by the system for bootstrap ROMs and I/O controllers. Thus, no memory is allowed to respond to addresses within this region. The MMS1117 accomplishes this function via gate U36: whenever the 5 most significant Bus address lines are asserted (only true if I/O page is selected), U36 will inhibit access to the MMS1117.

Note that the ending address is not selectable. Furthermore, since the memory range is determined by the sum of the selected starting address and the storage capacity, it is possible to configure the MMS1117 such that the ending address will exceed the available 128K address space. Since the addition is performed modulo 128K, the locations left over above 128K will be decoded starting at the bottom, i.e. ØK. For example: if a MMS1117-48 (64 KW total capacity) is selected to start at an address of 76K, the following configuration would result:

2.1 Address Decoding (continued)



A portion of the reserved I/O page can be made available for use as read/write memory by the MMS1117 via switches U22/1 and U22/2. The decoder at U24 detects whether the current Bus address is within the range of 124K-125K (producing an output at switch position U22/2) or 125K-126K (producing an output at switch position U22/1). To make these address spaces available for use as read/write memory, the appropriate switch should be closed.

2.2 Address Paths. See logic diagram, sheet 2.

The buffered Bus addresses are latched into registers at locations U21 and U23. The 128 refresh addresses are generated by counters in locations U2 and U12. A set of 4 to 1 multiplexers gates the proper address lines to the memory chip address bus via drivers in locations U4, U6, U14 and U16. The address lines are source terminated with 18 ohm resistors to eliminate oscillations due to the capacitive loading of the memory chip's address bus.

2.3 Timing.

2.3.1 External Timing. See diagram in Section 1.11.

All external timing is derived from and dependent on the Bus protocol and timing. A detailed description of the Unibus timing and protocol may be found in the PDP-11 Peripherals Handbook. All timing specified for the MMS1117 is measured at the edge connector on the Bus side of the transceiver gates. Access time is the delay between assertion of MSYN by the master on the Bus and the assertion of SSYN by the MMS1117. According to the Unibus protocol requirements, the MMS1117 maintains SSYN asserted until MSYN is negated by the master. The MMS1117 will negate SSYN within 75 nanoseconds (w/c) of receiving ~MYSN.

The maximum sustainable rate at which back-to-back DATI (Read) cycles can be supported by the MMS1117 are not limited by the MMS1117 cycle time because the Bus protocol and timing overhead always exceeds the Read access to cycle time parameter for all models of the MMS1117.

Only during continuous back-to-back DATO/B (write) cycles is the thruput with the MMS1117 limited by the cycle time parameter. Note that the automatic refresh cycles within the MMS1117 have the effect of stretching the access times by up to one cycle time quantum. This interference is otherwise totally transparent to the Bus master and occurs approximately once every 16 microseconds.

2.3.2 Internal Timing. See logic diagram, sheet 4.

All internal timing is derived from one 5-tap delay line and is set off by either an internal refresh request or a bus MSYN in conjunction with BOARD ENABLE. The refresh request is generated by a free-running oscillator and posted in register at U44. The signal START L at test point TP10 will be asserted at the beginning of any cycle. As it propagates thru the delay line it generates transitions that are used to gate the Memory Chip Address Multiplexers (thru U17), the Row Address Strobe (thru U7), the Column Address Strobe (thru U18), the Parity Error Strobe (thru U19 and U20) and Bus SSYN (thru U51, U52, U73, U52 and U65).

The register at U20 serves as a synchronization arbiter between internal refresh requests and external bus cycle requests. Dato (write word), DATO/B (write byte) and DATI (read word) cycles are decoded by U73 and U75. The latter will be set during DATO/B (write) cycles and cleared during DATI/P cycles.

2.4 Data Paths. See logic diagram sheet 3.

The write and read data paths are separate within the MMS1117.

Write data is obtained from the common external bus via bus transceivers at U68-U71 and routed to the storage array via latches/buffers located at U28-U30. These data latches allow write acces times to be considerably shorter than read access times.

Read data is routed from the storage array directly to the external bus bia bus driver gates at U68-U71.

2.5 Parity logic. See logic diagram sheet 5.

All parity generation, detection and logging circuitry is self-contained within the MMS1117-xxPC. A separate parity data bit is generated, stored and checked for each 8-bit data byte for all memory access cycles.

During a DATO (write) cycle the parity generators located at U45 and U47 generate odd parity data bits that are stored as data bit 16 (for the even byte) and data bit 17 (for the odd byte). The logic can be forced to write wrong parity (i.e. even) by setting the register at U43 to a logic 1. This register is accessible to the program via the parity control and status register (CSR) address thru the bus. During normal operation and on first power on this register will be set to a logic 0 such that all write operations will generate the proper parity data (odd).

During a DATI (read) cycle, each 8 bit data byte with its associated parity bit is connected to a separate parity detector located at U42 and U49. If even (wrong) parity is detected in either of thee two data bytes, the bus PB L line is asserted via bus drivers at U77 simultaneously with the reading of the data word. At the same time, gates at U26 and 27 will set the parity error flag at U44 and strobe the signals on the bus address lines into the 7 bits of the register at location U64.

The program can independently access the contents of U64 (containing the address of the most recent parity error - resolved up to a 1 KW block) via bus drivers U65 - U67. Additionally, data may be written into this register via data multiplexers at U40 and U41.

All these several data bits make up the Parity Control and Status Register (CSR) and are grouped such that they can be written and read as one word at a single address. This parity CSR address resides within the I/O page at one of 32 possible locations. A 4-position selector switch at U59 determines the particular address. To access the CSR via program, the bus address must fall within the

2.5 Parity logic (continued)

range of 772100 and 772136 (octal) inclusive; this range being decoded by U24, U36-U39. The particular offset within that range (as determined by switches at U59) is decoded by the comparator at U60.

The register at location U43 is the parity enable flag; it must be set to a logic 1 via program before parity errors are reported thru the bus PB L line.

CHAPTER III: INSTALLATION

3.1 MMS1117 xxPC, Using the built-in parity controller.

3.1.1 Isolate an empty Hex-height SPC slot anywhere on the System Unibus*; the required pinout is listed on Table 2.

3.1.2 Ascertain that the selected SPC slot has the proper voltages at the required current according to Table 6. (If in doubt, measure the voltages; exceeding the specified voltages may damage the memory card and void the warranty.)

3.1.3 Set the MMS1117 memory starting address according to Table 3.

3.1.4 If the range of memory addresses selected in the previous step (range: = selected starting addresses plus total memory on board overlaps the I/O page (124K to 128K) and it is desired to utilize part of this I/O page as R/W memory, set the switches called out in Table 3A.

CAUTION: The address space wraps around, i.e., if the range exceeds the available space on the high end of the addresses, any excess will appear beginning at the bottom, at address 0; for example: if 64K of memory is strapped to start at 72K, the top 8K of the memory would be decoded at address 0-8K. The I/O page is always protected.

3.1.5 Set the parity control register address (switches located in position U59). Table 4 lists the switch positions vs. bus addresses. Use the following algorithm to determine the proper address for this register.

A. If the MMS1117 xxPC is the only parity memory in the system, select 772100 as the parity register address on the MMS1117 xxPC with the lowest starting address.

   If a second MMS1117 xxPC is installed in the same system, select its parity control registers at 772102.

B. If the system already has other parity memory installed, determine the parity register address for the MMS1117 xxPC from the data supplied with the other memory, keeping in mind that no two parity registers may have the same address and that the lowest memory address should have the lowest corresponding parity register address.

3.1.6 Set the switches located in position U22, U46 and U54 as follows:

U22/1	See paragraph 3.1.4
U22/2	See paragraph 3.1.4
U22/3	Open
U22/4	Open
U46/1	Closed
U46/2	Open
U46/3	Closed
U46/4	Open
U46/5	Closed
U54/1	Open
U54/2	Open
U54/3	Closed
U54/4	Closed
U54/5	Open

3.1.6 Turn off the system power and insert the MMS1117 into the selected slot.

3.1.7 Turn on the system power and verify via the console or switch register that each of the several memory banks can be written into and read out of. If a bus time out occurs when accessing a bank of memory that is expected to be present, verify the starting address selection switch settings.

3.1.8 Verify that the Parity CSR can be accessed via the switch register/console at the selected address.

3.1.9 When first powered up, the MMS1117 memory contains random data due to the volatility of its storage elements. Thus, many if not all locations will have wrong parity. This implies that enabling the parity controller after power-up and prior to performing a write cycle to every memory location, the MMS1117 will generate parity errors; this is normal for volatile memories.

3.1.10 Load and run several passes of the current memory diagnostics (i.e., DZQMxxx).

3.1.11 If difficulties arise, contact:

Motorola Memory Systems
3501 Ed Bluestein Blvd.
Austin, Texas 78721
(512) 928-6000

3.2 MMS1117 xx P and MMS1117 xx PC Using An External Parity Controller (i.e., DEC's M7850 module).

In this mode, the MMS1117 xx PC will only store the externally generated and detected parity data. Bus line PØ is used to transmit the parity for the low byte between the controller and the MMS1117 and Bus line P1 is used to transmit the parity for the high byte between the controller and the MMS1117. This scheme is compatible with DEC's Modified Unibus back panel and thus requires the usage of these back panels, i.e., DD11P. Note the use of an external parity controller will impose an additional access delay to all Read (DAT1 and DAT1P) cycles. This delay can be up to 100 nanoseconds.

3.2.1 Isolate an empty Hex-height modified SPC slot anywhere on the System Unibus*; the required pinout is listed on Table 2. A parity controller module must be present within the same back panel.

3.2.2 Ascertain that the selected SPC slot has the proper voltages at the required current according to Table 6. (If in doubt, measure the voltages; exceeding the specified voltages may damage the memory card and void the warranty).

3.2.3 Set the MMS1117 memory starting address according to Table 4.

3.2.4 If the range of memory addresses selected in the previous step (range: = selected starting addresses plus total memory on board overlaps the I/O page (124K to 128K) and it is desired to utilize part of this I/O page as R/W memory, install the straps called out in Table 3A.

CAUTION: The address space wraps around, i.e., if the range exceeds the available space on the high end of the addresses, any excess will appear beginning at the bottom, at address 0; for example: if 64K of memory is strapped to start at 72K, the top 8K of the memory would be decoded at address 0-8K. The I/O page is always protected.

3.2.5 Set the parity control register address (switches located in position U59) such that all four switches are open.

NOTE: The MMS1117-xxP may not have a switch in this location.

INSTALLATION (cont'd)

3.2.7 Set the switches located in positions U22, U46 and U54 as follows:

U22/1	See paragraph 3.2.4
U22/2	See paragraph 3.2.4
U22/3	Closed (senses the presence of external parity controller)
U22/4	Closed
U46/1	Open
U46/2	Closed
U46/3	Open
U46/4	Closed
U46/5	Open
U54/1	Closed
U54/2	Closed
U54/3	Open
U54/4	Open
U54/5	Closed

3.2.8 Turn off the system power and insert the MMS1117 into the selected slot.

3.2.9 Turn on the system power and verify via the console or switch register that each of the several memory banks can be written into and read out of. If a bus time out occurs when accessing a bank of memory that is expected to be present, verify the starting address selection switch settings.

3.2.10 When first powered up, the MMS1117 memory contains random data due to the volatility of its storage elements. Thus, many if not all locations will have wrong parity. This implies that enabling the parity controller after power-up and prior to performing a write cycle to every memory location on the MMS1117 will generate parity errors; this is normal for volatile memories.

3.2.11 Load and run several passes of the current memory diagnostics (i.e., DZQMBxx).

3.2.12 If difficulties arise, contact:

Motorola Memory Systems
3501 Ed Bluestein Blvd.
Austin, Texas 78721
(512) 928-6000

INSTALLATION (cont'd)

3.3 MMS1117 xx (no parity).

3.3.1 Isolate an empty Hex-height SPC slot anywhere on the System Unibus*; the required pinout is listed on Table 2.

3.3.2 Ascertain that the selected SPC slot has the proper voltages at the required current according to Table 6. (If in doubt, measure the voltages; exceeding the specified voltages may damage the memory card and void the warranty.)

3.3.3 Set the MMS1117 memory starting address according to Table 4.

3.3.4 If the range of memory addresses selected in the previous step (range: = selected starting addresses plus total memory on board overlaps the I/O page (124K to 128K) and it is desired to utilize part of this I/O page as R/W memory, install the straps called out in Table 4A.

CAUTION: The address space wraps around, i.e., if the range exceeds the available space on the high end of the addresses, any excess will ap.pear beginning at the bottom, at address Ø; for example: if 64K of memory is strapped to start at 72K, the top 8K of the memory would be decoded at address 0-8K. The I/O page is always protected.

3.3.5 If a set of switches is present in location U59, set all four switches to their open position.

3.3.6 Ascertain that the location labeled as C157 (located between U76 and U77) has a wire jumper installed in place of a capacitor.

3.3.7 Set the switches located in positions U22, U46 and U54 as follows: (note that some MMS1117xx models may not have switches U46 and U54 installed)

U22/1	See paragraph 3.3.4
U22/2	See paragraph 3.3.4
U22/3	Open
U22/4	Open
U46/1	Open
U46/2	Open
U46/3	Open
U46/4	Open
U54/1	Open
U54/2	Open
U54/3	Open
U54/4	Open
U54/5	Open

INSTALLATION (cont'd)

3.3.8 Turn off the system power and insert the MMS1117 into the selected slot.

3.3.9 Turn on the system power and verify via the console or switch register that each of the several memory banks can be written into and read out of. If a bus time out occurs when accessing a bank of memory that is expected to be present, verify the starting address selection switch settings.

3.3.10 When first powered up, the MMS1117 memory contains random data due to the volatility of its storage elements. Thus, many, if not all, locations will have wrong parity. This implies that enabling the parity controller after power-up and prior to performing a write cycle to every memory location on the MMS1117 will generate parity errors; this is normal for volatile memories.

3.3.11 Load and run several passes of the current memory diagnostics (i.e., DZQMxxx).

3.3.12 If difficulties arise, contact:

Motorola Memory Systems
3501 Ed Bluestein Bvd.
Austin, TX 78721
(512) 928-6000

3.4 BATTERY BACKUP MODE - ALL MODELS

To operate the MMS1117 in the battery backup mode, the following conditions have to be met:

3.4.1 Uninterrupted +20V nominal (+15V to +20 Vdc) must be provided at any one of the regular +20V input pins.

3.4.2 Uninterrupted -20V nominal (-7V to -20 Vdc) must be provided at connector pin FB2.

3.4.3 Uninterrupted +5 Vdc must be provided at the connector pin designated as +5BB, i.e., pin BD1.

The average power requirements for these voltages are listed in Table 6 under standby power requirements.

In addition, two wire jumpers on the MMS1117 must be reconfigured as follows:

E14 - Remove (separates the two +5V zones on the MMS1117).

E28 - Install (connects the refresh logic circuitry to connector pin BD1). Note that on Rev A artwork this jumper must be installed on Side 2 (solder side) of the MMS1117. It is located under U74 and delineated by two square solder pads.

CHAPTER IV

REPAIR AND WARRANTY

The MMS1117 family of memory cards is inplemented on a multilayer board with high density printed circuit wiring. Any repair work entailing soldering to this printed circuit board requires special tools and skills or permanent damage can be induced. Thus, Motorola Memory Systems does not encourage field repairs to the MMS1117 and explicitly voids all warranties if it is determined that any repair has been performed or attempted by any person or company without the explicit and written authorization to this effect.

Motorola Memory Systems offers a comprehensive range of service plans in support of its complete product line. These service plans are designed to provide separate types of coverage which allow the user to select that plan which best accommodates his particular situation. The available service plans are:

Type M-FWS: Factory Warranty Service
Type M-FRS: Factory Repair Service
Type M-FES: Factory Exchange Service

Factory service is coordinated and performed by Motorola Memory Systems' Customer Return Order Department whose staff of engineers and technicians provide prompt correction or replacement of factory-authorized returned products. Products being returned under any of the three service plans should be delivered to:

Motorola Memory Systems
3501 Ed Bluestein Blvd.
Austin, Texas 78721
Attention: CRO Department

Type M-FWS
FACTORY WARRANTY
SERVICE PLAN

The Factory Warranty Service plan sets forth the services available at Motorola Memory Systems for the repair of products and product subassemblies which fail during the warranty period. Motorola Memory Systems warrants all factory-supplied products in accordance with the Standard Warranty stated at the end of this service plan.

PLAN

Motorola Memory Systems provides complete factory support for its products and product subassemblies which fail during the warranty period.

Motorola factory authorization for a return must be obtained prior to returning any article to the factory. Upon authorization, the factory will issue a Customer Return Order Number which will be utilized for all correspondence regarding such a product being returned for service by Motorola Memory Systems.*

Any article returned to the factory must be properly packed and marked with a return address which includes the name and telephone number of the individual requesting the repair. The nature of the failure must be clearly identified.

If a subassembly is being returned, the serial number of the assembly from which the subassembly was removed must also be provided.

Within ten working days (plus shipping time) after receipt of the article, Motorola Memory Systems will either refund the purchase price, or repair or replace the article with a new or equivalent-to-new-performance article which has been subjected to appropriate tests, requalifying it to original specifications. See the STANDARD WARRANTY which governs all details of this plan.

CHARGES

Warranty repairs, as defined within the STANDARD WARRANTY, will be made at no charge to the customer for parts and labor. Articles returned to the factory should be shipped prepaid. They will be returned prepaid.

Repair, labor, and/or parts replacement made at the customer's request for failures not covered by warranty provisions will be invoiced to the customer at the then-current rates and conditions for Motorola Memory Systems' Factory Repair Service.

PARTS

The parts replaced will be new or equivalent to new in performance. Defective parts replaced become the property of Motorola Memory Systems.

MECHANICAL CONDITION

Factory repair is restricted to correcting article failure. Cosmetic refurbishment will not be performed.

STANDARD WARRANTY

The Seller warrants that the articles sold hereunder will at the time of shipment be free from defects in material and workmanship and will conform to the Seller's specifications, or as appropriate, to the Buyer's specifications which have been accepted in writing by the Seller. Seller's sole obligation hereunder shall be limited to either refunding the purchase price or repairing or replacing the articles for which written description of nonconformance hereunder is received within one year from date of initial shipment; provided a Customer Return Order Number is obtained* for return of nonconforming articles and; provided such articles are returned FOB Seller's plant or authorized repair center within thirty (30) days from expiration of said one year period. This warranty shall not apply to any products which Seller determines have, by Buyer or otherwise, been subjectd to testing for other than specified electrical characteristics or to operating and/or environmental conditions in excess of the maximum values established therefore in the applicable specifications or otherwise have been subjected to mishandling, misuse, neglect, improper testing, repair, alteration or damage, assembly or processing that alters physical or electrical properties. Transportation charges for the return to the Buyer shall be paid by Motorola within the contiguous 48 United States and Canada. If Motorola determines that the products are not defective, Buyer shall pay Motorola all costs of handling and transportation. The warranty outside the contiguous 48 United States and Canada excludes all costs of shipping, customs clearance and related charges.

In no event will Seller be liable for any incidental or consequential damages. THIS WARRANTY EXTENDS TO BUYER ONLY AND NOT TO BUYER'S CUSTOMERS OR USERS OF BUYER'S PRODUCTS AND IS IN LIEU OF ALL OTHER WARRANTIES WHETHER EXPRESS, IMPLIED, OR STATUTORY INCLUDING IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS.

*Authorization and Customer Return Order Number are obtained by calling (512) 928-6000 X 4203, Motorola Memory Systems, Warranty and Repair Service, 3501 Ed Bluestein Blvd., Austin, Texas 78721

Type M-FRS
FACTORY REPAIR
SERVICE PLAN

The Factory Repair Service plan sets forth the services available at Motorola Memory Systems for the repair of products and product subassemblies which are not under warranty.

PLAN

Motorola Memory Systems provides complete factory service for the repair and requalification of its products and product subassemblies.

Motorola factory authorization for a return must be obtained prior to returning any article to the factory. Upon authorization, the factory will issue a Customer Return Order Number which will be utilized for all correspondence regarding the product being serviced by Motorola Memory Systems*

Factory service requires a method for guaranteed payment for all repair and requalification services prior to any actual work performance.

Any article returned to the factory must be properly packed and marked with a return address which includes the name and telephone number of the individual requesting the repair. The nature of the failure must be clearly identified.

If a subassembly is being returned, the serial number of the assembly from which the subassembly was removed must also be provided.

Within ten working days (plus shipping time) after receipt of the article, Motorola Memory Systems will repair or replace the article with a new or equivalent-to-new-performance article which has been subjected to appropriate tests, requalifying it to original specifications.

CHARGES

Articles returned to the factory should be shipped prepaid. They will be returned prepaid. Repair, labor, and parts replaced will be invoiced to the customer at the then-current rates and conditions for Motorola Memory Systems' Factory Repair Service. A minimum factory service charge will be imposed for processing repair orders of small dollar value. Contact Motorola Memory Systems' Warranty and Repair Service for information regarding minimum factory service charges.

PARTS

The parts replaced will be new or equivalent to new in performance. Defective parts replaced become the property of Motorola Memory Systems.

MECHANICAL CONDITION

Factory repair is restricted to correcting article failure. Cosmetic refurbishment will not be performed.

WARRANTY

Motorola Memory Systems warrants only the repair and parts replaced for a period of ninety (90) days from date of return of repaired article to customer; provided factory authorization and a Customer Return Order Number is obtained* for the return of nonconformance of repair or parts replaced and; provided such repaired article is returned FOB Motorola Memory Systems' plant within thirty (30) days from expiration of said ninety (90) day period.

In no event will Seller be liable for any incidental or consequential damages. THIS WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED OR STATUTORY INCLUDING IMPLIED WARRANTIES OR MERCHANTABILITY OR FITNESS.

*Authorization and Customer Return Order Number are obtained by calling (512) 928-6000 X 4203, Motorola Memory Systems, Warranty and Repair Service, 3501 Ed Bluestein Blvd., Austin, Texas 78721

Type M-FES
FACTORY EXCHANGE
SERVICE PLAN

The Factory Exchange Service plan sets forth the exchange services available at Motorola Memory Systems for products and product subassemblies which are not under warranty.

PLAN

Motorola Memory Systems provides an exchange program for products and product subassemblies, not under warranty, which have been identified by the customer as requiring service. The objective of this plan is to provide a more expedient means of returning the customer's system to full operational status.

Motorola factory authorization for a return must be obtained prior to returning any article to the factory. Upon authorization, the factory will issue a Customer Return Order Number which will be utilized for all correspondence regarding such a product being exchanged by Motorola Memory Systems.*

Any article returned to the factory must be properly packed and marked with a return address which includes the name and telephone number of the individual requesting the repair. The nature of the failure must be clearly identified.

If a subassembly is being returned, the serial number of the assembly from which the subassembly was removed must also be provided.

CHARGES

Articles returned to the factory should be shipped prepaid. They will be returned prepaid. Upon receipt of customer's repairable, defective article and a purchase order or certified check covering the cost of the article exchange at the then-current exchange price, Motorola Memory Systems will ship a new or equivalent-to-new-performance exchange article.

Motorola Memory Systems will ship the exchange article prior to receipt of customer's repairable, defective article upon receipt of a purchase order from those customers having approved credit, or to any customer upon receipt of a certified check for the full, then current purchase price of the exchange article. Upon receipt by Motorola Memory Systems of the customer's repairable article, the customer will be credited the difference between the current purchase price and the current exchange price.

A minimum factory service charge will be imposed for processing exchange orders of small dollar value. Contact Motorola Memory Systems Warranty and Repair Service for information regarding minimum factory service charges.

WARRANTY

Motorola Memory Systems warrants any article purchased under the FACTORY EXCHANGE SERVICE PLAN in accordance with the STANDARD WARRANTY as provided in the M-FWS FACTORY WARRANTY SERVICE PLAN section of this document.

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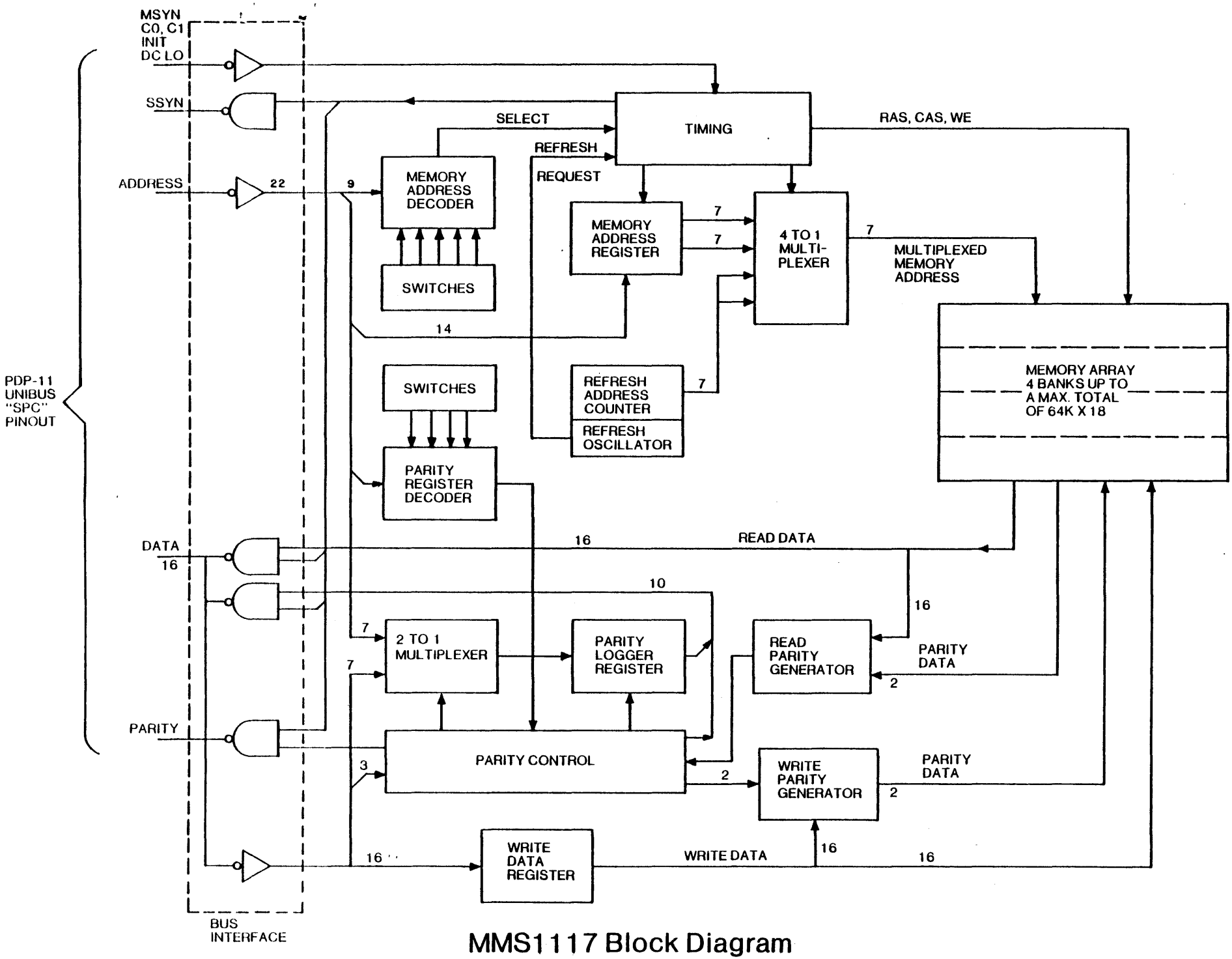
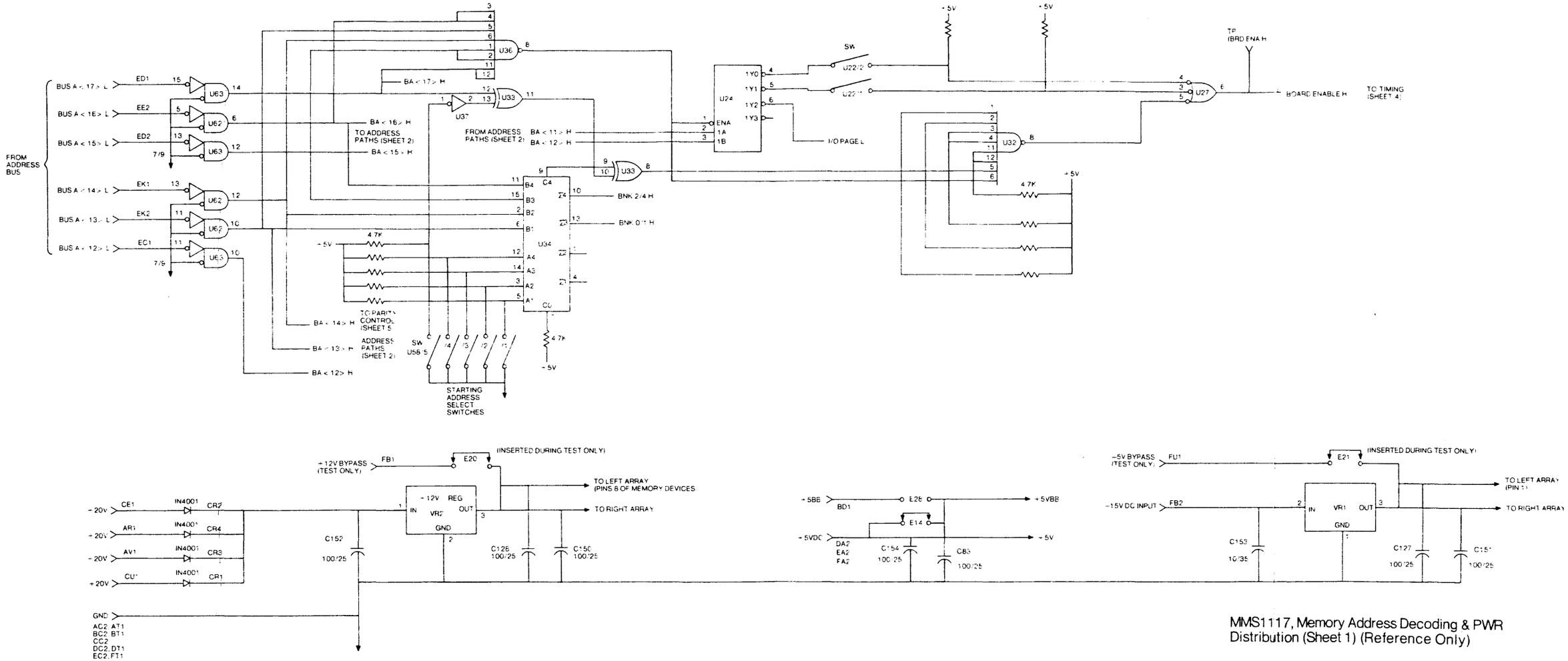
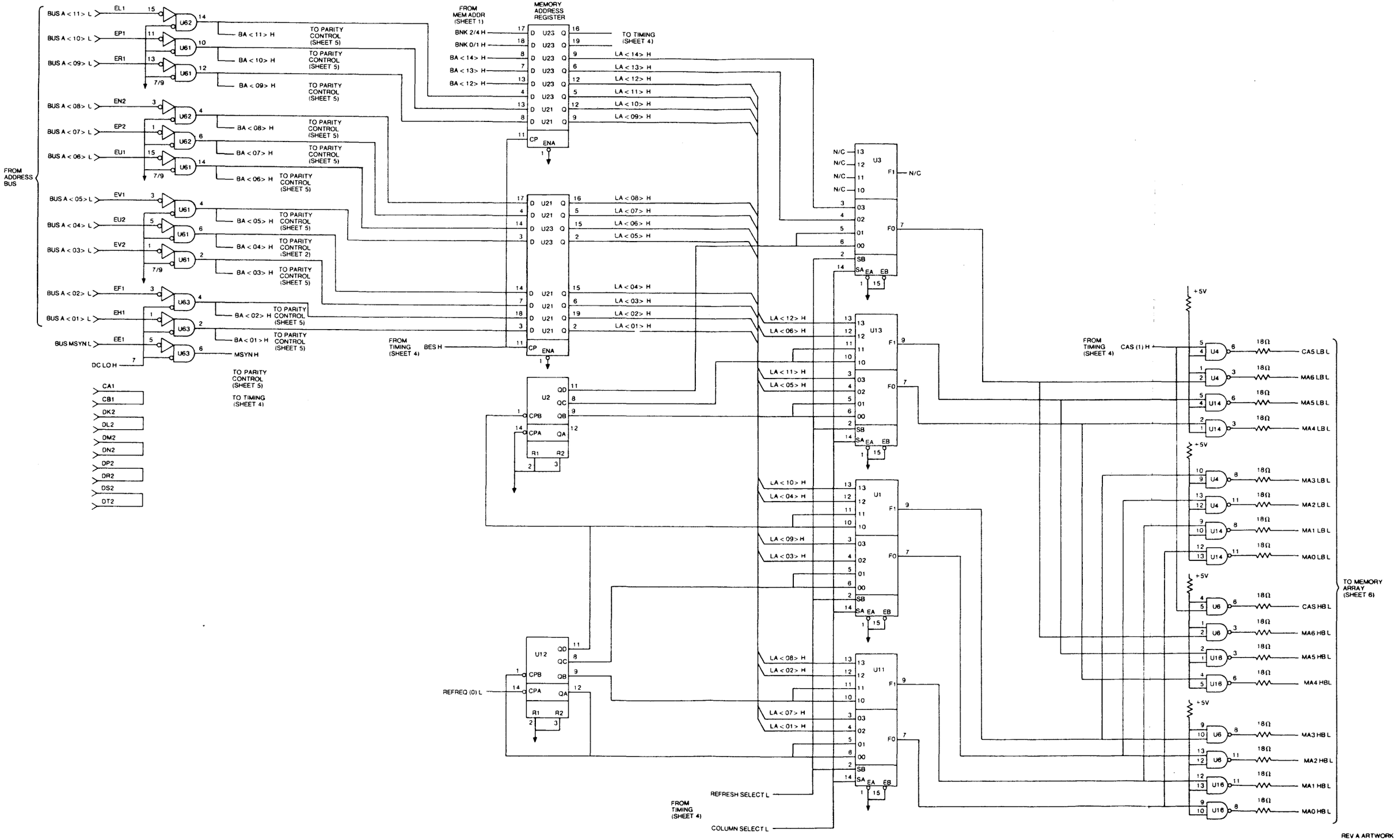
*Authorization and Customer Return Order Number are obtained by calling (512) 928-6000 X 4203, Motorola Memory Systems, Warranty and Repair Service, 3501 Ed Bluestein Blvd., Austin, Texas 78721



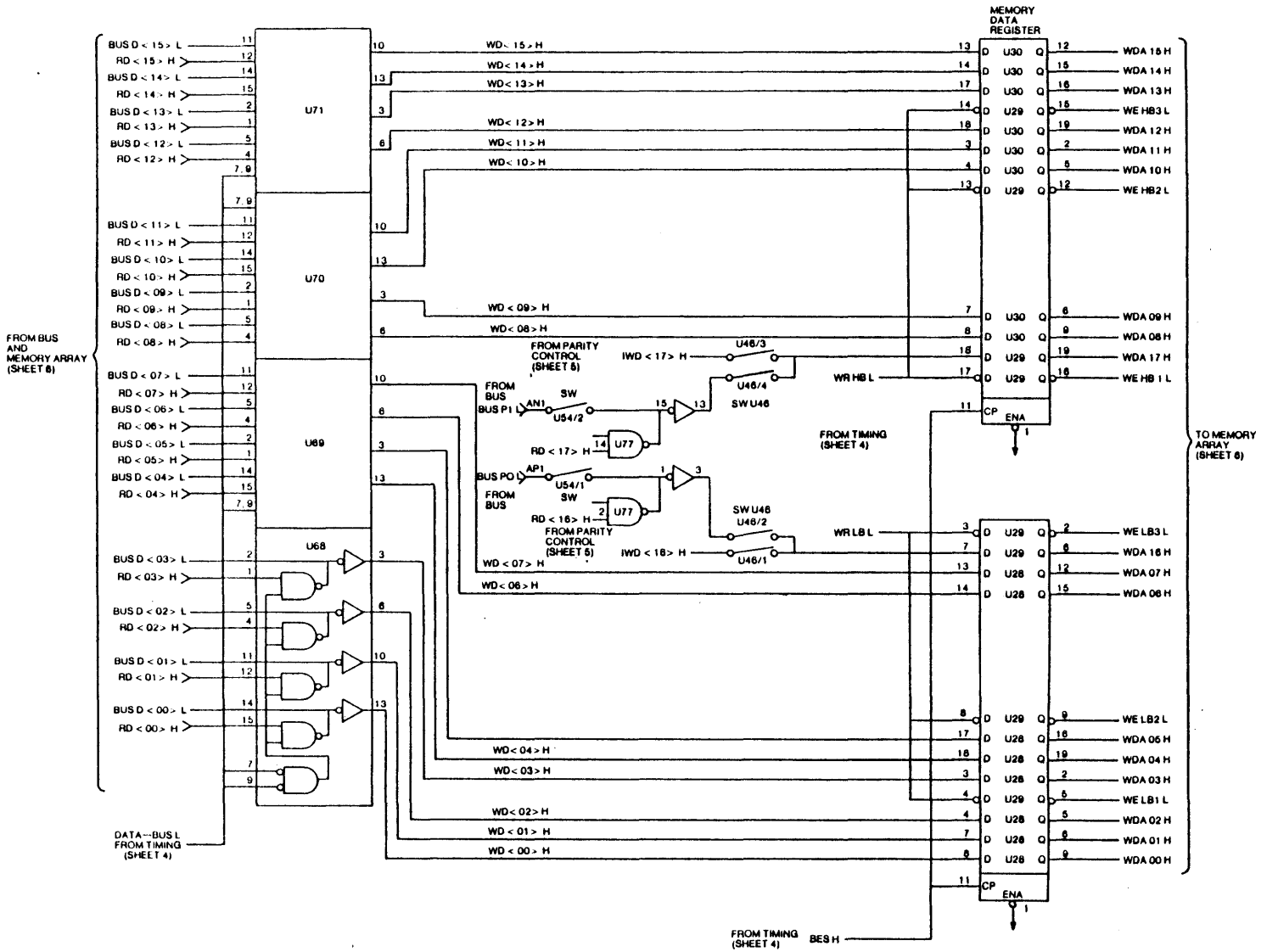
MMS1117 Block Diagram



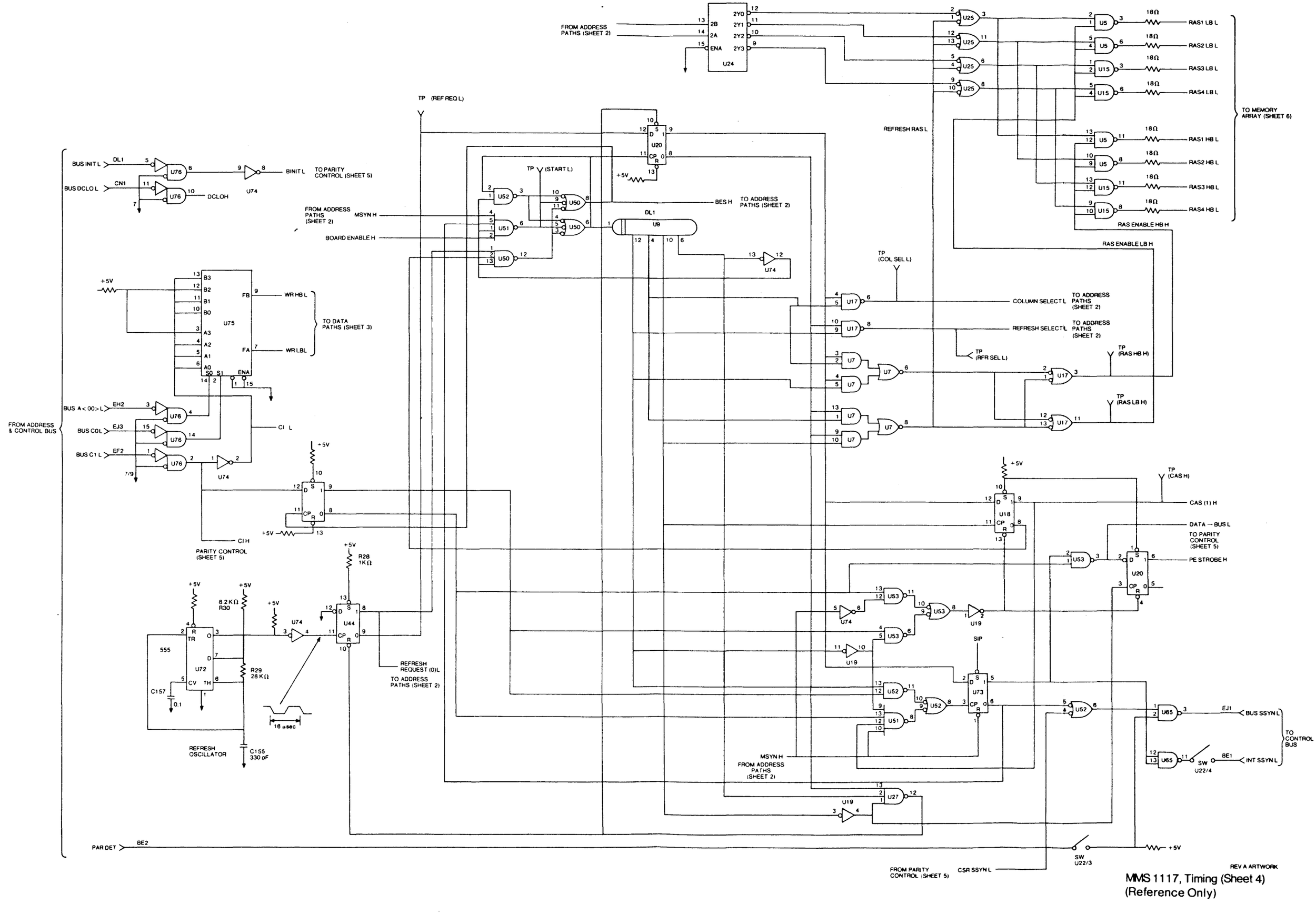
MMS1117, Memory Address Decoding & PWR Distribution (Sheet 1) (Reference Only)



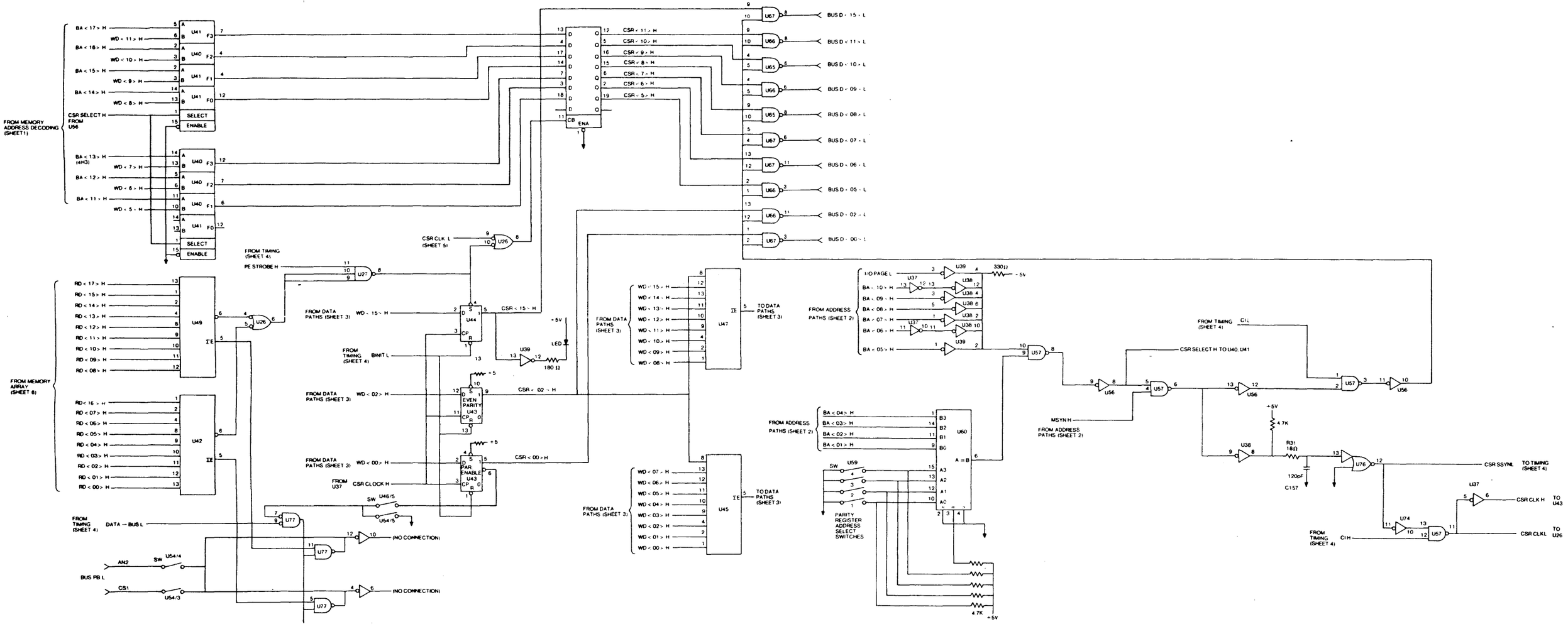
MMS1117, Address Paths (Sheet 2)
(Reference Only)



MMS1117, Data Paths (Sheet 3)
(Reference Only)



MMS 1117, Timing (Sheet 4)
(Reference Only)



MMS1117, Parity Control (Sheet 5)
(Reference Only)

From Data Paths, Sheet 3

WE LB1 L To Pin 3 Of U100, U101, U102, U200, U201, U202, U300, U301, U302, U400, U401, U402

WE LB2 L To Pin 3 Of U103, U104, U105, U203, U204, U205, U303, U304, U305, U403, U404, U405

WE LB 3 L To Pin 3 Of U106, U107, U116, U206, U207, U216, U306, U307, U316, U406, U407, U416

From Address Paths, Sheet 2

MA6 LB L To Pin 13 Of U100 Through U107, U116, U200 Through U207, U216, U300 Through U307, U316, U400 Through U407, U416

MA5 LB L To Pin 10 Of U100 Through U107, U116, U200 Through U207, U216, U300 Through U307, U316, U400 Through U407, U416

MA4 LB L To Pin 11 Of U100 Through U107, U116, U200 Through U207, U216, U300 Through U307, U316 U400 Through U407, U416

MA3 LB L To Pin 12 Of U100 Through U107, U116, U200 Through U207, U216, U300 Through U307, U316, U400 Through U407, U416

MA2 LB L To Pin 6 Of U100 Through U107, U116, U200 Through U207, U216, U300 Through U307, U316, U400 Through U407, U416

MA1 LB L To Pin 7 Of U100 Through U107, U116, U200 Through U207, U216, U300 Through U307, U316, U400 Through U407, U416

MA0 LB L To Pin 5 Of U100 Through U107, U116, U200 Through U207, U216, U300 Through U307, U316, U400 Through U407, U416

From Address Paths, Sheet 2

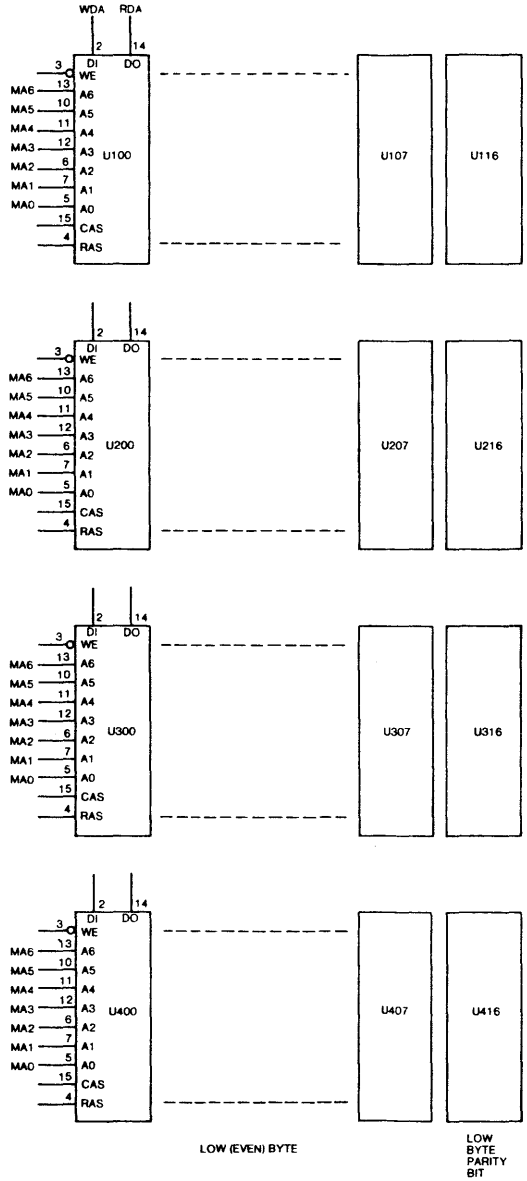
CAS LB L To Pin 15 Of U100 Through U107, U116, U200 Through U207, U216, U300 Through U307, U316, U400 Through U407, U416

From Timing, Sheet 4

RAS 1 LB L To Pin 4 Of U100 Through U107, U116
RAS 2 LB L To Pin 4 Of U200 Through U207, U216
RAS 3 LB L To Pin 4 Of U300 Through U307, U316
RAS 4 LB L To Pin 4 Of U400 Through U407, U416

From Data Paths, Sheet 3

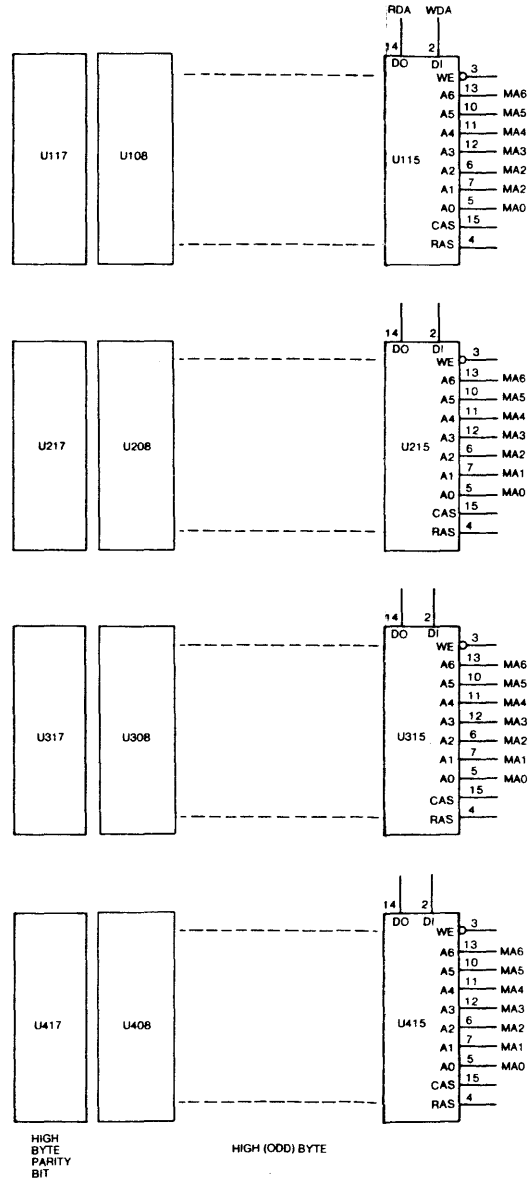
WDA 15 H To Pin 2 Of U115, U215, U315, U415
WDA 14 H To Pin 2 Of U114, U214, U314, U414
WDA 13 H To Pin 2 Of U113, U213, U313, U413
WDA 12 H To Pin 2 Of U112, U212, U312, U412
WDA 11 H To Pin 2 Of U111, U211, U311, U411
WDA 10 H To Pin 2 Of U110, U210, U310, U410
WDA 9 H To Pin 2 Of U109, U209, U309, U409
WDA 8 H To Pin 2 Of U108, U208, U308, U408
WDA 17 H To Pin 2 Of U117, U217, U317, U417
WDA 16 H To Pin 2 Of U116, U216, U316, U416
WDA 7 H To Pin 2 Of U107, U207, U307, U407
WDA 6 H To Pin 2 Of U106, U206, U306, U406
WDA 5 H To Pin 2 Of U105, U205, U305, U405
WDA 4 H To Pin 2 Of U104, U204, U304, U404
WDA 3 H To Pin 2 Of U103, U203, U303, U403
WDA 2 H To Pin 2 Of U102, U202, U302, U402
WDA 1 H To Pin 2 Of U101, U201, U301, U401
WDA 0 H To Pin 2 Of U100, U200, U300, U400



BANK 1
BANK 2
BANK 3
BANK 4

To Data Paths, Sheet 3

RDA 15 H From Pin 14 Of U115, U215, U315, U415
RDA 14 H From Pin 14 Of U114, U214, U314, U414
RDA 13 H From Pin 14 Of U113, U213, U313, U413
RDA 12 H From Pin 14 Of U112, U212, U312, U412
RDA 11 H From Pin 14 Of U111, U211, U311, U411
RDA 10 H From Pin 14 Of U110, U210, U310, U410
WDA 9 H From Pin 14 Of U109, U209, U309, U409
RDA 8 H From Pin 14 Of U108, U208, U308, U408
RDA 17 H From Pin 14 Of U117, U217, U317, U417
RDA 16 H From Pin 14 Of U116, U216, U316, U416
RDA 7 H From Pin 14 Of U107, U207, U307, U407
RDA 6 H From Pin 14 Of U106, U206, U306, U406
RDA 5 H From Pin 14 Of U105, U205, U305, U405
RDA 4 H From Pin 14 Of U104, U204, U304, U404
RDA 3 H From Pin 14 Of U103, U203, U303, U403
RDA 2 H From Pin 14 Of U102, U202, U302, U402
RDA 1 H From Pin 14 Of U101, U201, U301, U401
RDA 0 H From Pin 14 Of U 100, U200, U300, U400



From Data Paths, Sheet 3

WE HB 1 L To Pin 3 Of U117, U108, U109, U217, U208, U209, U317, U308, U309, U417 U408, U409,

WE HB 2 L To Pin 3 Of U110, U111, U112, U210, U211, U212, U310, U311, U312, U410, U411, U412

WE HB 3 L To Pin 3 Of U113, U114, U115, U213, U214, U215, U313, U314, U315, U413, U414, U415

From Address Paths, Sheet 2

MA6 HB L To Pin 13 Of U117, U108 Through U115, U217, U208 Through U215, U317, U308 Through U315, U417, U408 Through U415

MA5 HB L To Pin 10 Of U117, U108 Through U115, U217, U208 Through U215 U317, U308 Through U315 U417 U408 Through U415

MA4 HB L To Pin 11 Of U117, U108 Through U115, U217, U208 Through U215, U317, U308 Through U315, U417, U408 Through U415

MA3 HB L To Pin 12 Of U117, U108 Through U115, U217, U208 Through U215, U317, U308 Through U315, U417, U408 Through U415

MA2 HB L To Pin 6 Of U117, U108 Through U115, U217, U208 Through U215, U317, U308 Through U315, U417, U408 Through U415

MA1 HB L To Pin 7 Of U117, U108 Through U115, U217, U208 Through U215, U317, U308 Through U315, U417, U408 Through U415

MA0 HB L To Pin 5 Of U117, U108 Through U115, U217, U208 Through U215, U317, U308 Through U315, U417, U408 Through U415

From Address Paths, Sheet 2

CAS HB L To Pin 15 Of U117, U108 Through U115 U217, U208 Through U215 U317, U308 Through U315 U417, U408 Through U415

From Timing Sheet 4

RAS 1 HB L To Pin 4 Of U117, U108 Through U115
RAS 2 HB L To Pin 4 Of U217, U208 Through U215
RAS 3 HB L To Pin 4 Of U317, U308 Through U315
RAS 4 HB L To Pin 4 Of U417, U408 Through U415

MMS1117, Memory Array Layout (Sheet 6)
(Reference Only)