TELETEK HARDWARE DOCUMENTATION

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TELETEK INTRODUCTION

The following sections contain information on TELETEK S-100 boards used with the MDZ/OS system. This information is provided as a convenience to MDZ/OS customers because documentation is extra cost from TELETEK. Our sincere thanks to TELETEK for permission to edit and reprint this documentation.

Using the NEC 765AC FDC and Zilog Z80 DMA ICs, SYSTEMASTER provides single- and double-density data storage on both mini- and maxi-floppy disk drives providing capabilities which minimize the overhead burden on the CPU and software. Some of these capabilities are: single- and double-density data transfer under software control; performance of simultaneous seek operations on all drives connected to the system; IBM compatible formatting for ease of information exchange with controllers using similar operating system software; compatibility with both single- and double-sided drives; ANSI standard 50 pin disk drive connector; automatic reading of sequential sectors on a diskette; automatic reading of both tracks of a two-sided diskette; automatic error-checking detected via CRC; under software control, possible selection of sector size to be 128, 256, 512, or 1,024 bytes.

The floppy disk control section of SYSTEMASTER also incorporates a phase-locked oscillator (PLO) which is used to stabilize the separated information and clock for precise data recovery.

A reset-jump circuit on SYSTEMASTER makes the CPU jump to the EPROM software on board whenever the system reset button is activated. This is useful for systems which do not have a front panel. For systems with a front panel, reset-jump will override the functions of the front panel. Also, incorporated as part of the reset-jump circuit, a power-on-clear function is included which generates a reset automatically when power is first applied.

SYSTEMASTER can be used as a cost effective stand-alone microcomputer board or as the basis for a high-performance multi-user multi-processing system.

2.1 Specifications

Central processor: Z80A CPU - 4 MHz operation.

Memory: 64k bytes dynamic RAM, bank selectable. Uses 64k bit x 1 devices, 200nS (or faster), 128 cycle refresh.

Serial: Z80A SIO - 2 RS232C, independent operation. Speeds from 110 to 19200 baud.

Timer: Z80A CTC - 4 channels, 2 used for serial ports, 2 used for real-time clock.

Parallel: Z80A PIO - 1 bidirectional port with 4 handshake lines, 1 port with 8 independent input or output lines.

Floppy disk controller: NEC uPD 765AC, single- or double-density and single- or double-sided operation, mini- or maxi-drives, ANSI standard 50 pin connector, IBM compatible format.

DMA: Z80A DMA controller handles floppy disk transfers

SYSTEMASTER

The SYSTEMASTER is a microcomputer on a single S-100 board. It incorporates all of the features required in a small computing system including a CPU, 64k bytes of RAM, serial and parallel I/O, and a floppy disk controller.

On board is a Z80A CPU which operates at 4 MHz for high-speed, efficient processing of information. The Z80A provides the capability to support many sophisticated applications. The interrupt structure of the Z80A is particularly important for systems which perform multiple tasks concurrently. The SYSTEMASTER utilizes the structured interrupt system of the Z80A in most of its I/O capabilities.

The on-board memory of SYSTEMASTER can provide up to 8k bytes of storage in EPROM/ROM and 64k bytes of RAM. The standard SYSTEMASTER is set up for 2k bytes of EPROM (to be used for on-board initialization routines) and 64k bytes of RAM. Options are available allowing the RAM to be bank switched.

Providing two independent serial ports, the Z80A SIO provides RS232C-compatible serial ports which can be operated under interrupt control. Both serial ports include full handshaking for connection to such external devices as a printer, CRT terminal, or MODEM.

Also on board is a counter-timer chip which provides software-settable clocks for both serial ports and a real time clock. The real time clock is used by the software to provide timekeeping functions. It normally functions under interrupt control requiring a minimum of overhead. This real time clock can be used by software for any time-related functions, such as time dating of files, a stop watch or timing loops for external operations.

The Z80A PIO provides two parallel ports. One of these two ports is bidirectional with 8 data and 4 handshake lines. Normally this port is configured as a printer output, but because it is under software control, it can be reconfigured by the user to be a device input or a truly bidirectional port. The second parallel port has 8 data lines available which can be set independently to be input or output lines.

Disk data transfer rates:

Single density	5-1/4" - 125k bits/sec	8" - 250k bits/sec
Double density	5-1/4" - 250k bits/sec	8" - 500k bits/sec

EPROM/ROM: 2716, 2732, 2764, 2316, 2332, 2364; up to 8k bytes total.

S-100 bus signals:

A0-A15	pHLDA	RFSH*
CDSB*	HOLD*	DODSB*
CLOCK	INT*	sHLTA
DATA IN	ADSB*	sINP
DATA OUT	POC*	sINTA
MWRITE	RDY	sM1
NMI*	RESET*	sMEMR
Ø	pSYNC	sOUT
pSTVAL*	sWO*	XRDY
pDBIN	pWR*	SDSB*
sXTRQ*	SLAVE CLR*	

Note: SYSTEMASTER does not provide 8080-type I/O addressing; only the lower 8 address lines contain the I/O address.

Dimensions: 5.05" x 10.0," excluding edge connector.

Power requirements: +8v @ 2.0 amp, +16v @ 50mA, -16v @ 50mA.

Workmanship conforms to the requirements of MIL-STD-454.

Forced air cooling is required.

2.2 Installation

Upon receipt of SYSTEMASTER, check the shipping package for signs of abuse which may indicate possible damage. Check the board physically to look for any parts which may have been damaged during shipping. If any diskettes were shipped with SYSTEMASTER, check the diskettes for signs of damage which might be any bending or signs of a sharp object placed against the diskettes. Diskettes are quite fragile and any warping of the surface of the diskette may render it inoperative. Notify the shipper of any damage.

SYSTEMASTER is ready for immediate use upon receipt. It requires only that the peripherals which will be used with it be connected to the appropriate female connector which will then plug into the headers along the top of the board. For the particular connections required, see the section entitled "Peripheral Connections."

SYSTEMASTER need only be plugged into a standard S-100 bus for power and it will be functional, able to utilize the peripherals connected to it with the memory on board. The SYSTEMASTER needs to be in a well ventilated area due to the high density of IC's on board. Ideally, the board should be mounted vertically in a stream of air which will be moving across the face of the board. Whatever the mounting position, forced-air cooling is mandatory. Bring peripheral cables neatly away from the board with enough slack to prevent any tension being applied to the cable, as this may cause the cable to separate from its crimp connection causing intermittent problems.

For serial console devices, SIO A is the primary port. With the standard software, SIO A can determine the baud rate of a carriage return and thus set the appropriate speed automatically after a reset. The serial speed must be a standard value between 110 and 19200. Also, SIO A requires the handshake lines of the RS-232-C interface before it will function. See "Serial Ports" for further information.

Some versions of SYSTEMASTER do not have RAM on board. If no RAM is on-board, it must be supplied by the user. Care must be exercised in choosing the right RAM device for use on the board.

2.2.1 Serial Ports

SIO A and SIO-B

						(20)	
2	4	6	8	10	12	14 DTR IN	16
	(2)	(3)	(4)	(5)	(6)	(7)	
1	3 DATA IN	5 DATA OUT	7 RTS IN	9 CTS OUT	11 DSR OUT	13 GND	15

EIA pins shown in parentheses.

These are the connections going into channels A and B of the SIO chip. In this configuration, each channel appears as a data communication device and will connect to a terminal or a printer.

IN and OUT refer to data direction with respect to the SYSTEMASTER. Data from an external device is IN to SYSTEMASTER, and data to an external device is OUT.

CTS (Clear To Send) and DSR (Data Set Ready) are outputs to the external device and are at a positive voltage levels when the SIO channel is ready to function. RTS (Request To Send) and DTR (Data Terminal Ready) are inputs which must be at a positive voltage level for the SIO channel to function if the Auto Enables option is activated through software. This option is normally enabled in the standard SYSTEMASTER software.

Either channel can be crimp-connected to a 25-pin RS-232C connector by aligning Pin 1 of the cable from the SYSTEMASTER connector with Pin 1 of the 25 pin RS-232C connector. In this configuration, the channel connects directly to a terminal or printer.

To connect to a MODEM, the signals must be connected as follows:

SYSTEMASTER Pin #	EIA Pin #	Direction	Function
5	2	OUT	Data to MODEM
3	3	IN	Data to SYSTEMASTER
11	4	OUT	RTS (Request To Send)
14	5	IN	CTS (Clear To Send)
7	6	IN	DSR (Data Set Ready)
13	7	--	Signal Ground
9	20	OUT	DTR (Data Terminal Ready)

IN refers to data sent to SYSTEMASTER, and OUT refers to data sent to the MODEM.

Note: If the terminal or printer does not provide RTS and DTR, Pins 4, 5, and 20 on the terminal side of the RS-232C male connector must be jumpered together. This ensures that the required handshake signals to the SIO port are provided. If the AUTO ENABLES feature of the SIO is not enabled this is not required. In the standard software provided, AUTO ENABLES is enabled.

2.2.1.1 EIA Serial Data Transfer Protocol

Prior to sending or receiving data, the four handshake lines should be active low. However, the SIO will allow control of its receive and transmit functions independently. If the "Auto Enables" function of the SIO channel is enabled (standard), the SIO will not send data until DTR is low. (This function is labelled "CTS" on the SIO chip.) This is handy for buffered printers which need to stop receiving data until the buffer is printed. By pulling DTR high, the printer will stop the flow of data from the SIO. When it is ready to receive more data, it pulls DTR low. Similarly, if "Auto Enables" is enabled, the SIO will not accept information until RTS is low. (This function is labelled "DCD" on the SIO chip.) This is primarily used with a communications link where, if signal conditions deteriorate, the data may be garbled.

In summary, the handshake lines provide a convenient means of controlling the flow of information in a serial channel. If any line goes high, transfer ceases.

2.2.1.2 RS-232C Voltage Levels

A logic high (a binary ONE), or marking condition, is any voltage less than -3 volts to a minimum of -25 volts. A logic low (a binary ZERO), or spacing condition, is any voltage greater than +3 volts to a maximum of +25 volts. Any level between -3 and +3 volts is undefined. This is called the transition region. The maximum transition time between bit cells is four per cent of the basic clock period. The maximum voltage rate of change (slew rate) is 30 volts/uSec. Thus the maximum RS-232C transmission speed, based on voltage swings of -12 to +12 volts, is 50,000 baud.

2.2.1.3 Serial Data Timing

Prior to transmitting data the signal line is held high, or marking. It goes low (spacing) to indicate the start of a character. The bits representing the character are then sent Least Significant Bit first, then a parity bit (if used), and finally 2 stop bits. The stop bits indicate the end of the character and are always logic ONEs. The standard SYSTEMASTER is set up for 8 data bits, no parity, and 2 stop bits.

The value of each character bit is held for the entire length of each bit cell. The length in time of each bit cell is the basic clock period, equal to the reciprocal of the baud rate. Thus for 9600 baud, each bit cell is 104 uSec long (.0001041 Sec=1/9600).

2.2.2 Parallel Ports

PIO A

2	4	6	8	10	12	14	16
RESET*		+5	GND	B STB	B RDY	A STB	A RDY
1	3	5	7	9	11	13	15
D7	D6	D5	D4	D3	D2	D1	D0

PIO B

2	4	6	8	10
GND		D1	D2	D0
1	3	5	7	9
D3	D4	D7	D6	D5

These are the connections into the PIO chip. The PIO chip has two parallel ports, A and B. As configured, PIO A may be used as an input, output, bidirectional or control port with four handshake lines. PIO B is the same except that it does not have bidirectional capabilties or handshake lines.

The signals are:

D0 - D7	8 data lines
A STB	Strobe input pulse from a device. Depending on the mode of operation, it means: 1. Output mode: Positive edge of this strobe is issued by the device to acknowledge the receipt of data made available by PIO A. 2. Input mode: The strobe is issued by the device to load data from the device into PIO A. 3. Bidirectional mode: Same as 1, except output data are present only while A STB is low. 4. Control mode: The strobe is inhibited internally.
A RDY	Ready output to a device. Depending on the mode of operation, it means: 1. Output mode: Indicates that the data bus is stable for transfer to the device. 2. Input mode: When active, it indicates that PIO A is ready to accept data from the device. 3. Bidirectional mode: Same as 1. 4. Control mode: Always in a low state.
RESET*	The active-low reset line on the SYSTEMASTER. This can be used to reset a hard disk connected to PIO A.
B STB	Used when PIO A is in the bidirectional mode; strobes data from the device into PIO A.
B RDY	Used when PIO A is in the bidirectional mode; it goes high to indicate that PIO A is ready for data from the device.

The software supplied by Teletek allows PIO A to be set up as an input port or an output port. PIO B is set up in the control mode with all eight data lines available individually as input or output lines.

2.2.3 Floppy Disk Drive

Ground Pin #	Signal Pin #	Input - I Output - O	Description
1	2	O	Above track 43
3	4	-	Not used
5	6	-	Not used
7	8	O	Above track 43

9	10	I	Dual sided
11	12	-	Not used
13	14	O	Head 1
15	16	-	Not used
17	18	O	Head load
19	20	I	Index
21	22	I	Ready
23	24	-	Not used
25	26	O	Drive select 0
27	28	O	Drive select 1
29	30	O	Drive select 2
31	32	O	Drive select 3
33	34	O	Direction
35	36	O	Step pulse
37	38	O	Write data
39	40	O	Write gate
41	42	I	Track 00
43	44	I	Write protected
45	46	I	Read data, composite
47	48	-	Not used
49	50	O	Motor control

Input/Output are referenced to SYSTEMASTER. Input is a signal from the disk drive to SYSTEMASTER, and output is a signal to the disk drive.

More detailed information regarding floppy disk drive interfacing is available in Section 4. Please refer to that section of the manual when installing disk drives on the SYSTEMASTER.

2.3 Options

This section details the numerous options available on the SYSTEMASETER.

2.3.1 Write Compensation

To help compensate for the shifting of data bits during the read process of the floppy disk drive, the write data are compensated. This is particularly critical for double-density operation. Different drives require different amounts of write compensation. The symptoms of too much or not enough write compensation are as follows: 1. Too much write compensation shows up as read errors (usually CRC) in the outer tracks (0-42); 2. Not enough write compensation shows up as read errors in the inner tracks (43-76).

SYSTEMASTER provides selectable compensation for both 5 1/4" and 8" drives in the following combinations:

Jumper			Compensation	
OP0	OP1	OP2	5 1/4"	8"
0	0	0	None	None
1	0	0	None	125 nSec
0	1	0	None	250 nSec
1	1	0	250 nSec	125 nSec
0	0	1	250 nSec	250 nSec
1	0	1	500 nSec	125 nSec
0	1	1	500 nSec	250 nSec
1	1	1	Illegal, no write data output	

A 0 for OP0-2 indicates the jumper is in place, while a 1 indicates the option pins are open.

Compensation is switched automatically as the on-board drive size control is switched from 5 1/4" to 8" drives.

Compensation depends on the recommendations of the drive manufacturer. Both 5 1/4" and 8" drives usually require 250 nSec compensation.

2.3.2 Track 43 Selectable Compensation

In addition to the above options, SYSTEMASTER provides one more: if the OP3 jumper is in place, the compensation for Tracks 0-42 will be one step less than that in the above table. At Track 43 and higher, write compensation will be equal to the table value. This option is provided because most drives require more compensation on the inner tracks where the recording density is higher. For 5 1/4" drives which do not have more than 42 tracks, select compensation one step greater than that required.

For example, assume an 8" drive which requires 250 nSec compensation, and a 5 1/4" drive with 40 tracks which requires 250 nSec compensation. Option jumper OP3 is in place:

Select OP0=0, OP1=1, OP2=1

At Tracks 0-42, 5 1/4" compensation is 250 nSec, and 8" compensation is 125 nSec. For Tracks 43 and above, the 8" drive will have 250 nSec compensated data.

2.3.3 Extended Head Load

The uPD-765AC floppy disk controller has a maximum head unload time of 240 mSec. In some applications this will cause an undue amount of head loading and unloading. To increase this head unload time and reduce the number of head load actions, a 74LS123 monostable can be wired into the head drive circuit. With the addition of a 6 volt capacitor, the head unload time is extended. This increases the life of the media and the heads where there would normally be a great deal of head load activity. The following table gives the effective head load time for several different capacitor values:

Capacitor (uF)	Head Load Time (sec)
10	0.5
30	1.4
50	2.3
70	3.2
90	4.1
110	5.0
130	5.9
150	6.8
170	7.7
190	8.6
210	9.5
230	10.4
250	11.3

The time values are approximate (since normally resistor values are ± 10% and capacitor values ± 20%) and are arrived with the following equation: HLT = (45 * C)/(1E03), where C is in micro-Farads.

To enable the head load option, jumper Option Pin E-19 to E-20 and install the desired capacitor value at location C-12. If this option is not desired then Pin E-19 should be connected to E-18.

2.3.4 Wait State Generator

The wait-state generator can generate a wait-state during all memory accesses, M1 accesses, or only when the on-board ROM is accessed. The choice of wait-state generation is dictated by the requirements of the system. For the standard SYSTEMASTER, one wait state is generated for every access to the on-board ROM. With a faster ROM (less than 360 nSec access time), the wait state is not needed. The following wait-state options are available:

Option	Jumper
No wait state	E1 open
On-board ROM only	E1 to E4
All memory	E1 to E3
All memory, M1 only	E1 to E2

Note: if the PRDY or XRDY input of the S-100 bus is low, this will be gated into the CPU wait input via U-29 causing the CPU to wait until PRDY or XRDY is released to its inactive high state. CAUTION: An extended wait state will cause a loss of refresh to the dynamic RAMs on the SYSTEMASTER.

2.3.5 CTC Timing

The trigger inputs to CTC channels 0 through 2 connect to a 1.2288 MHz source. Thus all standard baud rates from 150 to 76,800 can be generated by programming the CTC for the counter mode, with a time constant between 1 and 256 (0). The SIO divider is set for 16 or 32 as necessary. For baud rates that are non-standard or below 150, use the CTC in the timer mode with a divide by 16 prescaler, and the SIO divider set for 16 or 32.

To summarize:

Baud rate 300 to 76,800- SIO divider set to 16, CTC in the counter mode, time constant set from 1 to 256.

Baud rate 150- SIO divider set to 32, CTC in the counter mode, time constant set to 256.

Baud rates less than 150:

(CTC in the timer mode, prescaler set to 16)

Baud Rate	SIO divider	Time Constant	Error
45	32	174	0.22%
60	32	130	0.16%
75	16	208	0.16%
110	16	142	0.04%

Channels 2 and 3 of the CTC are ganged together to provide a 1-second interrupt real-time clock. Channel 2 is programmed in the timer mode, pre-scaler set to 256, time constant set to 125. Channel 3 is set to the counter mode, time constant set to 125, and interrupt enabled. For a multi-user operating system which requires a fast clock interrupt, enable the interrupt for Channel 2 also. The interrupt routine for Channel 2 can count down to provide periods which are integral multiples of the 8 millisecond interrupt.

2.3.6 EPROM/RAM Options

The on-board ROM socket can accommodate 24 or 28-pin EPROMs or ROMs occupying 2k, 4k, or 8k bytes of memory space. This ROM can originate at 0000H, E000H, F000H, or F800H depending on the setting of the option jumpers on LA-5:

2.3.7 ROM Memory Space Options

ROM	Origin	End	Space	Jumpers
2316,2716	0000H	07FFH	2k	E14 to E16, E15 to E17
2332,2732	0000H	0FFFH	4k	E14 to E16, G to E17
2364,2764	0000H	1FFFH	8k	G to E16, G to E17
2316,2716	F800H	FFFFH	2k	E14 to E16, E15 to E17
2332,2732	F000H	FFFFH	4k	E14 to E16, E13 to E17
2364,2764	E000H	FFFFH	8k	E13 to E16, E13 to E17

The type of ROM used determines the socket and jumpers used at the socket:

ROM	Size	Socket	Jumpers
2316	2k	24 pin	E5 to E8, E6 to E10, E7 to E12
2332	4k	24	E5 to E11, E6 to E10, E7 to E12
2364	8k	24	E5 to E9, E6 to E12, E7 to E11
2716	2k	24	E5 to E8, E6 to E10, E7 to E12
2732	4k	24	E5 to E11 E6 to E10, E7 to E12
2764	8k	28	E5 to E11, E6 to E10, E7 to E12

The chip select options for the 2316 and 2332 must be specified as follows for the above jumper connections:

2316	Pin 18 active low
	Pin 20 active low
	Pin 21 active high
2332	Pin 18 active low
	Pin 20 active low

Note: when the 24-pin 2364 is used, underlying RAM cannot be written when the ROM is enabled.

Except for the 24-pin 2364, when the ROM is enabled, either during reset-jump or otherwise, the underlying RAM can be written but not read. Memory other than that occupied by the ROM can be accessed normally. Thus on reset the ROM monitor could copy itself into RAM then disable the ROM and continue execution from RAM.

2.3.8 RAM Select

SYSTEMASTER contains 64k bytes of RAM. This RAM is partitioned into a fixed and a selectable block. The selectable block can be disabled allowing CPU access to additional external memory. The fixed block is always resident in the CPU memory space. This combination of fixed and selectable memory accommodates such multi-user operating systems as MP/M from Digital Research, which require a fixed block of RAM for the operating system.

The size of the fixed block of RAM can be varied by option jumpers AJ-1, 2, and 3:

Fixed Block Size	Range	Jumpers	
32k	8000H-FFFFH	AJ-1	Open
		AJ-2	Open
		AJ-3	Open
16k	C000H-FFFFH	AJ-1	Open
		AJ-2	Open
		AJ-3	Connected
8k	E000H-FFFFH	AJ-1	Open
		AJ-2	Connected
		AJ-3	Connected
4k	F000H-FFFFH	AJ-1	Connected
		AJ-2	Connected
		AJ-3	Connected

The selectable block of RAM occupies the memory space from 0000H up to the fixed block of RAM. The selectable block is enabled when /RAMEN is low. (/RAMEN is Bit 7 of the control register.) When disabled, the selectable block of RAM is not affected by memory accesses in its memory space.

Note: The on-board RAM cannot be accessed by off-board temporary bus masters.

2.4 Theory of Operation

SYSTEMASTER is a single-board computer for the S-100 bus. It contains 2k-8k bytes of ROM, 64k bytes of RAM, a flexible-disk controller, two parallel ports, two serial ports, a DMA controller, a CTC, and a CPU. With appropriate software, SYSTEMASTER comprises a complete stand-alone single-user computer. The following discussion details the operation of the various functional areas of SYSTEMASTER.

2.4.1 Central Processor Operations

The heart of SYSTEMASTER is a 4 MHz Z80A. It provides the intelligence to operate the on-board peripherals and to provide the information interchange to the S-100 bus. Connections to the bus are made through tri-state buffers and control logic to provide the correct timing signals and status signals to operate other peripherals within the microcomputer.

2.4.2 CPU Clock Driver

Three sections of U-58 drive the processor clock line. Resistor R-2 pulls this line up to +5 volts, while R-3 controls the low-going overshoot. On an oscilloscope, with a high-impedance probe connected to TP-1 and a short ground line connected to SYSTEMASTER adjacent to TP-1, the low-going clock signal should not overshoot ground potential by more than Ø.3 volts. The measuring oscilloscope must have a bandwidth of one gigahertz. TP-1 is between J-5 and J-2.

2.4.3 Wait State Generator

The wait-state generator functions by holding the CPU wait input low until one clock cycle after MREQ from the CPU is active. U-53A, a J-K flip-flop, has its K input connected to MREQ from the CPU. The inverted state of MREQ connects to the J input. Initially, prior to a memory cycle, MREQ is high. This causes U-53A to clock its Q output low. When MREQ goes active, U-53's Q output is gated with MREQ low via U-28, an OR gate, and the output is gated with the desired state (M1, ROM, or all memory). If the current CPU cycle is the desired state, pin 8 of U-28 will be low, which in U-29, an AND gate, causes the wait input of the CPU to be low. On the next negative edge of the CPU clock, because MREQ is low and the J input of U-53A is now high, the Q output of U-53A will go high. This is gated to the wait input of the CPU allowing it to complete the cycle. U-53A resets itself at the end of the memory cycle when MREQ again goes inactive.

2.4.4 DMA Controller

SYSTEMASTER incorporates a DMA controller to provide efficient, transparent flexible-disk data transfer without requiring CPU intervention. The DMA controller is a single-channel device which can execute only one series of operations at a time. Although it is connected to the 765 flexible-disk controller, when the 765 is idle the DMA controller can perform block moves of data between memory and I/O devices.

Interrupts can be enabled during DMA operations. Prior to a series of DMA data transfers the DMA controller must be set up as necessary for the particular operation desired. No CPU intervention is required during a DMA transfer process. At the completion of the series of data transfers the DMA controller will interrupt the CPU. At this time, the CPU performs any operations necessary to terminate the data transfer.

2.4.5 On-board Control Register

U-13, an octal D-type flip-flop, provides control for several areas of SYSTEMASTER. The output lines of U-13 are:

Bit	Name	Function
7	/RAMEN	When low, enables the selectable block of on-board RAM.
6	/ROMEN	With /JMP, controls the on-board ROM
5	/JMP	With /ROMEN, controls the on-board ROM
4	/MOT	When low, turns on the flexible-disk drive spindle motor
3	/FL8	When low, allows 8" flexible-disk data transfers. When high, 5 1/4" flexible-disk data transfers are enabled.
Ø-2	-	Not presently used

All these bits are reset low when a reset pulse occurs. The control register bits are set simultaneously by a CPU output to Port 1CH. The outputs follow the inputs directly.

2.4.6 ROM-I/O Decoder

LA-5, a logic array, provides the logic necessary to access the on-board ROM, select I/O, and control the RAM data buffer. When the CPU accesses memory, LA-5 decodes the address and option lines to determine if the on-board ROM is being accessed. If the CPU is accessing ROM, the RAM data buffer is held inactive, otherwise it is enabled if LA-1 has determined that on-board memory is to be accessed.

During an I/O operation, if the CPU address is less than 2ØH, the on-board I/O decoder is selected. If /M1 is active at the same time as /IORQ, an interrupt acknowledge cycle is in process and neither ROM, RAM nor I/O is selected.

2.4.7 Power-On Clear

SYSTEMASTER generates a reset pulse when power is applied, to initialize the system automatically. Thus during the start-up operation operator intervention is not required. To develop the power-on reset pulse, circuitry on-board SYSTEMASTER detects the first application of power: Capacitor C-26 is discharged initially. C-26 holds the plus input of U-17 (a dual comparator) low, which causes the output of U-17 to be low. The output of U-17 enables two drivers of U-6, a hex inverting bus driver, which pull RESET* and SLAVE CLR* low on the S-100 bus. In addition, the output of U-17 is buffered by U-18 to drive POC* low. When C-26 charges above the level on the minus input pin of U-17, the output of U-17 goes high. RESET* and SLAVE CLR* are released and pulled high by resistors connected to +5 volts, and POC* goes high. At this time the CPU on board SYSTEMASTER begins execution of the instructions in the on-board ROM. When power is turned off, Diode D-1 discharges C-26 quickly to provide a reset action if power is shortly reapplied. (Such a sequence can occur during a temporary power outage.)

2.4.8 Reset-Jump

After a reset operation SYSTEMASTER begins execution of the instructions in the ROM to initialize the system. Because the ROM may reside at 0000H or a higher memory address, special circuitry enables the ROM independent of its actual location.

The outputs of U-13, an octal D-type flip-flop, the on-board control register, are cleared by a reset pulse. Therefore, outputs /JMP and /ROMEN are low. This combination causes LA-5, a logic array, to enable the ROM for any CPU memory access. If the ROM options are set for a ROM location at E000H, F000H, or F800H, the first instruction in the ROM should be an absolute jump to the ROM location plus three. For example, a SYSTEMASTER set up for a 2716 has the ROM options set for an address of F800H. The first instruction in the ROM is a jump to F803H. This sets the CPU program counter to the actual ROM address space.

After the CPU begins executing the ROM in the correct address space, RAM can be enabled by setting /JMP high if the ROM occupies high address space, or setting /ROMEN high if the ROM occupies memory starting at 0000H. /JMP is Bit 5, and /ROMEN is Bit 6 of U-13, the control register.

To summarize:

ROM is always enabled after a reset.
ROM at 0000H: Set /ROMEN high to enable RAM.
ROM at F000H or higher: CPU jump to ROM + 3, set /JMP high to enable RAM.

2.4.9 Dynamic RAM Control

Logic Array LA-1 controls the access to the on-board dynamic RAM. A RAM cycle is started by /M1 going low, or by /MREQ active low in conjunction with /RD, /WR, or /RFSH. If the RAM-select options match /RAMEN and the option address jumpers, /MSTRT goes low. Both sections of U-19, a dual J-K flip-flop, are clocked active by the action of /MSTRT. U-19A activates the /RAS line of the dynamic RAM ICs. /RAS clocks the lower 8 bits of the memory address into the RAM ICs. U-19B sends a positive pulse into the delay line, U-47. The 20% output of the delay line resets U-19B to terminate the positive pulse, and in addition clocks U-54A. The output of U-54A causes the address multiplexers, U-42 and U-43, to select the upper 8 bits of the memory address.

When the positive pulse in the delay line reaches the 40% tap it clocks U-54B, which generates a /CAS signal to complete the RAM access. After the RAM access time has elapsed, data are stable at the RAM outputs. When the positive pulse in the delay line reaches the 100% tap, U-19A is reset which resets the /RAS signal. This allows the RAM RAS circuit to pre-charge in preparation for the next memory access.

As long as /CAS is low, the RAM outputs are stable. When the CPU terminates the memory request, LA-1 resets U-54 which returns the address multiplexers to the low-order address lines and resets the /CAS signal.

A memory write operation does not begin until /WR from the CPU is active. This ensures that the R/WR line to the RAM ICs is active when the RAM ICs are accessed. This precaution allows the DATA IN and DATA OUT lines of the RAM ICs to be connected together, simplifying the memory circuitry.

A refresh operation begins when /RFSH and /MREQ from the CPU are both active low. A normal memory cycle is started, but the address multiplexer and /CAS circuits are held idle. The CPU outputs a refresh address during this time to refresh one of 128 consecutive locations in the RAM necessary to retain data.

NOTE: An extended RESET* or Wait State condition will cause a loss of refresh in the on board dynamic RAM.

2.4.10 Serial Ports

The Z80A SIO is used to generate two entirely independent serial ports. Both serial ports incorporate all the handshaking lines required by an RS232C data interconnection device. Each channel of the SIO is driven by an independent section of the CTC. This means that baud rates for the two channels can be independently selected. In fact, the baud rates may range anywhere from 45 baud up to 19200 baud. These frequencies are determined during initialization of the CTC. The data lines to and from the SIO channels are buffered by RS232C level translators. These buffers are also inherently protected from short circuits on the external lines.

Both serial ports will interconnect with terminal equipment (printer, CRT terminal, etc.) using standard insulation-displacement connectors. Connection to a MODEM requires a transposition of all six serial lines as required by the MODEM. When connecting to a synchronous MODEM, which provides the receive and transmit clocks, the clock inputs to SIO A must be connected to the MODEM:

SIO A clocks	Jumper
Internal, CTC	E22 to E21, E25 to E24
From MODEM	E22 to E23, E25 to E26

The transmit and receive clocks for SIO A are provided by CTC Channel 0. Those for SIO B are provided by CTC Channel 1.

2.4.11 Parallel Ports

The parallel ports consist primarily of the Z80A PIO. Port A is used as an 8 bit input, output or bidirectional port. The four handshaking lines of the PIO are used with Port A. Normally, Port A is configured as an output for such parallel items as a printer. Under software control, port A can be configured as an input or as a bidirectional port where input data and output data as well as direction are controlled by the four handshaking lines.

Port B of the PIO is used in a bit control mode. This port is normally used to provide individual control lines for interfacing to parallel devices such as hard disk drives.

2.4.12 Floppy Disk Controller Operation

The heart of the flexible-disk controller is the NEC uPD765AC. Capable of single- and double-density, single- and double-sided 5 1/4" and 8" data recording, the 765 provides a flexible, reliable disk controller for SYSTEMASTER. Circuitry on board SYSTEMASTER supports the 765 in stabilizing the read data from the disk drive, compensating data written to the disk drive, and buffering status signals to and from the disk drive. The following discussion details the circuitry surrounding the 765.

The 765 has two drive-select outputs. U-49, a dual decoder, decodes US0 and US1 from the 765 to develop four drive select signals.

To reduce the number of its pins the 765 multiplexes dual signals on four of its control lines. Pin 39 of the 765 selects the seek mode when high and the data read-write mode when low. One section of U-56, an inverting buffer, inverts the signal from Pin 39 to enable the appropriate drivers when the 765 is in its seek mode. When in the seek mode, the 765 positions the disk drive head over the desired track on the diskette. In this mode, the 765 looks at the dual-sided and track 0 signals and outputs drive control signals to the direction and step lines. In the read-write mode, these four function lines become write-protect, write-fault, low-current (track greater than 42), and write-fault reset. As mentioned earlier, the output of the Seek/Read-Write pin selects the necessary signal lines.

2.4.13 765 Interrupt

The 765 generates an interrupt request to the CPU when it detects an error or completes an operation. The 765 interrupt output on Pin 18 is active high, thus it is inverted by U-57 and activates the output of U-7, a tri-state buffer. U-7 pulls down the CPU interrupt request line. When the CPU acknowledges the interrupt, LA-4 will pull down Data Line 0 if no other interrupts are active on SYSTEMASTER. Because the other data lines to the CPU have resistor pull ups to +5 volts, the CPU sees FEH on its data bus and will execute the absolute address stored at FEH in the interrupt table. The data input buffer from the S-100 bus is held inactive by LA-4 during the interrupt acknowledge operation when the 765 interrupt line is active.

2.4.14 Phase-Lock Loop

The read data from the disk drive may vary in frequency due to disk drive rotation speed variations. To maintain reliable read data, a phase-locked loop oscillator follows the frequency of the read data and provides a stabilized read clock for the 765. The read data pulses from the drive are applied first to U-23A, which provides a fixed pulse width for each data pulse to the 765. The read data pulses are also applied to U-23B, which generates a pulse whose width is one-fourth of the read data clock period. The output of U-23B is set by resistors driven by the outputs of LA-3. Depending on drive size and density, the pulse width generated by U-23B will be as follows:

Drive Size	Density	U-23B Pulse Width
5 1/4"	Single	2.0 uSec
5 1/4"	Double	1.0 uSec
8"	Single	1.0 uSec
8"	Double	0.5 uSec

The voltage-controlled oscillator, composed of two sections of U-21 and Transistor Q-3, oscillates at a nominal frequency of 2.0 MHz. Frequency dividers within LA-3 provide outputs that are 2 x the read data frequency and equal to the read data frequency. The output at the read data frequency is sent to the 765. The frequencies depend on drive size and density :

Drive Size	Density	2 x Frequency	1 x Frequency
5 1/4"	Single	250 KHz	125 KHz
5 1/4"	Double	500 KHz	250 KHz
8"	Single	500 KHz	250 KHz
8"	Double	1.0 MHz	500 KHz

In addition, LA-3 provides a write clock whose frequency is determined by drive size and density:

Drive Size	Density	Write Clock Output
5 1/4"	Single	250 KHz
5 1/4"	Double	500 KHz
8"	Single	500 KHz
8"	Double	1.0 MHz

The output of U-23B and the inverted 2 x frequency from LA-3 are applied to U-22, a dual flip-flop connected as a phase detector. The outputs of U-22 will be active depending on the relative occurrence of the applied signals. These outputs are buffered by two sections of U-21 to eliminate amplitude variations. The summing junction of R-21 and R-23, nominally +2.1 volts, is filtered by C-17 and R-24 and applied to the input of an op-amp, U-44. The voltage at the junction of R-21 and R-23 will vary depending on the difference between the frequency of the voltage-controlled oscillator and the read data frequency. U-44 amplifies this error signal and changes the charging current into C-20 which changes the frequency of the voltage-controlled oscillator. Thus the oscillator is made to follow the frequency of the disk drive data.

The action of the phase-lock loop is such that the read data pulses will occur in the center of the high or low portion of the read data clock sent to the 765. This provides the maximum margin for error in disk read operations.

2.4.15 PLL Adjustment

Variable Resistor R-32 is provided to adjust the quiescent output voltage of U-44 which in turn controls the frequency of the oscillator. R-32 is adjusted to provide an oscillator frequency measured at TP-3 of 2.00 + or - 0.02 MHz. If the oscillator will not adjust to 2.00 MHz, either C-20 or U-21 must be changed. After adjustment, the output of U-44 must be 0.4 + or - 0.4 volt as measured at TP-2, adjacent to R-32.

2.4.16 Data Transfer

SYSTEMASTER flexible-disk data transfers are handled via the on-board DMA controller. The sequence of operations should be: set up the DMA controller for the # of bytes to transfer (the sector size) and the starting memory address for the transfer, and finally send the read or write command to the 765. When the DMA controller interrupts the CPU at the end of the data transfer, the interrupt routine must immediately issue a terminal count to the 765 by doing an input from Port 14H.

The DMA controller accesses Port 1ØH to transfer data to or from the 765. This port connects to the DACK (DMA acknowledge) pin of the 765.

2.4.17 Disk Data Encoding

Physically, double density disk drives do not differ significantly from their single density counterparts. Improvements in double density record and playback heads and changes in mechanics often provide less expensive and more durable drives. These changes are minor compared to the differences in reading and writing functions. Figure 1 reviews encoding methods used in single and double density. The standard recording formats are FM (for frequency modulation), MFM (for modified frequency modulation-double density), and MMFM (for modified modified frequency modulation) which is a refinement of MFM. Line 1 of Figure 1 indicates the basic clock frequency which designates the bit cell in which information will be passed. The next line illustrates a sample of information; the line following shows the pulses which generate that information in a single-density FM format. Notice that information actually sent to and received from the drive is a combination of the basic clock frequency and data pulses. Refer to the next line which is MFM.

Here, only the data pulses will be sent to the drive and their orientation within the bit cell determines the value of that particular data pulse (a 1 or a Ø). Every Ø is represented by a data pulse that coincides with the basic clock frequency. Every 1 is represented by a pulse that occurs midway between two clock pulses. Thus, when the data pulse occurs in the middle of a bit cell, it is a 1; when it occurs in the beginning of a bit cell, it is a Ø. Look at the next line which represents MMFM.

This is a slight refinement of MFM; in this instance the data pulses once again represent 1's and Ø's via their placement within the bit cell. However, the rules change slightly. If the preceding data pulse was a Ø and the present datum is a Ø, then the data pulse will occur. If the last data pulse was a 1 and the present datum is a Ø, the present data pulse does not appear. If the last data pulse was a 1 and the present datum is a 1, that data pulse appears. Every time there is a 1, a data pulse will appear in the middle of a bit cell. But whether or not a Ø data pulse occurs depends on the preceding datum. Note that the density of data pulses for MFM is almost exactly one-half the density of data pulses for FM. Thus, for the same density of pulses on the diskette, MFM will record twice as much information as FM. MMFM has slightly less dense data pulses than MFM, but its complexity of encoding and decoding outweighs the slight advantage it might enjoy due to slightly less density.

The basic clock frequency for FM encoding is 25Ø KHz for an 8-inch diskette. When we delete the clock and leave only the data pulses in MFM, that clock rate changes to 5ØØ KHz. The MFM data transfer rate is twice as fast as FM. The density and the speed are both doubled, which means that twice as much information can be stored in the same physical space and manipulated twice as fast.

2.4.18 Interrupts

The SYSTEMASTER CPU is configured in Interrupt Mode 2. In this mode, a requesting peripheral generates an interrupt and when that interrupt is acknowledged, the CPU expects the peripheral device to place an 8 bit address vector on the data lines. The CPU then adds this 8 bit vector with another 8 bit register internal to the CPU to form a 16 bit absolute memory address. This address points to a 2-byte location in memory which contains the absolute address of the desired subroutine to service the interrupt. In the case of the Z8ØA DMA, SIO, PIO and CTC, the necessary interrupt vectors are loaded to internal registers during initialization. For the case of the floppy controller IC, the interrupt vector is simply composed of that vector formed by the pull-up resistors on the data lines, an FE. The Z8Ø peripheral IC's normally begin on an even memory location because Bit Ø is always a Ø during their interrupt response. When a device external to the CPU requests an interrupt, the external device must provide an interrupt vector on the data bus when interrupt acknowledge status line goes active high. The Z8ØA peripheral IC's are series-connected to provide priority interrupts. The last peripheral in the chain, namely the PIO, provides an interrupt enable signal for external devices. When this line is high, interrupts are enabled for external requests. When this line is low, external devices must be prevented from generating a response to an interrupt acknowledge signal. The vector that external devices place on the bus, when combined with the internal high order vector of the CPU, must point to a location in memory which provides the absolute address of the subroutine used for servicing that particular interrupt.

2.4.19 S-100 Bus Interface

The signals generated by SYSTEMASTER are compatible with the proposed IEEE-696 standard. Logic array LA-4 transforms the Z-80 family status signals to those of the S-100 bus. In addition, LA-4 controls the data input bus driver, U-12, to prevent conflicts with on-board I/O and memory devices. If a conflict could occur, SYSTEMASTER ignores the off-board device.

SYSTEMASTER generates the S-100 standard memory write strobe by the logical equation: MWRT= pWR AND /SOUT.

In addition to the standard S-100 signals, SYSTEMASTER brings the Z-80 CPU refresh signal to Pin 66 of the bus for those memory boards which need this signal.

U-5, a dual monostable, generates the pSYNC and pSTVAL* signals. Whenever the CPU activates a status line (M1, MREQ, or IORQ), LA-4 outputs an active-low signal to trigger U-5A. The output of U-5A appears on the bus as pSYNC and also triggers U-5B. U-5B generates a pSTVAL* signal whose active edge occurs after status is valid, and during the pSYNC pulse.

2.4.20 SYSTEMASTER Port Assignments

Port	Device	Function
00H	SIO	A-Data
01	"	A-Control
02	"	B-Data
03	"	B-Control
04	PIO	A-Data
05	"	A-Control
06	"	B-Data
07	"	B-Control
08	CTC	Channel 0, SIO-A baud rate
09	"	Channel 1, SIO-B baud rate
0A	"	Channel 2, Real-time clock
0B	"	Channel 3, Real-time clock-connects to the output of Channel 2.
0C	765	Status register
0D	"	Data
0E-0F	"	Not used
10	DACK	DMA acknowledge to 765
11-13	"	Not used
14	TC	Terminal count to 765
15-17	"	Not used
18	DMA	DMA processor control registers
19-1B	"	Not used
1C	CONT	On-board control register
1D-1F	"	Not used

2.5 In Case of Trouble

If the SYSTEMASTER does not respond the first time it's connected, relax. Due to its complexity, there are many areas that may have inadvertently been overlooked. Take time to read the "Peripheral Connections" section. The following trouble-shooting guide lists the major functional areas of the SYSTEMASTER and some typical problems associated with each. Suggested solutions are offered for each. But remember: it is strongly suggested that the entire manual be read.

Some important considerations:

SIO A, the console serial port, requires handshaking lines before it will function.

After reset, a carriage return must be the first character typed to establish the baud rate into SIO A. If the baud rate is less than 19,200, up to 6 carriage returns may be required.

Floppy drives must be able to seek even if not continually selected during seek operations. This usually means enabling a continuous stepper power option.

Dynamic memories must be set up according to the requirements for interfacing with a Z-80A CPU. Also, no wait states are inserted for system memory accesses with the standard SYSTEMASTER.

SBC-I

3.1 Product Description

The SBC-I is a slave S-100 board designed for a multiprocessing system and provides a CPU, I/O, and 64K-128k of memory for each user. A system processor is also needed in order to supervise system level functions. Because each user has a CPU dedicated to his application, his program will execute almost as fast as if he were the only user of the system. Communication with the main system processor occurs via a 1k-byte FIFO on board, with data transfers across the S-100 bus. Since the SBC-I occupies only four I/O ports on the bus there is great potential for system expansion using this system architecture.

The SBC-I board does not have to be used in an S-100 system. The board is designed to be utilized as a stand alone slave processor that will support one user. The communication to the master processor can be achieved on a RS-232 or RS-422 link. This would allow the installation of the SBC-I in a remote dumb terminal with nothing more than power connections required.

3.2 Features

The following is a list of the features of the SBC-I slave computer.

3.2.1 Memory

The 128k byte RAM incorporating memory management provides the space and flexibility required by the increasingly complex software being used in high performance systems. In addition to RAM, one EPROM on board provides an initialization program to set up the LSI IC's on board. After the routines have completed their function the EPROM can be disabled by software. The RAM is composed of 64k-bit RAM IC's to reduce the physical size of the array.

Bank-select controls the access to the EPROM, and a memory management circuit controls access to the RAM. The EPROM, which occupies 000H to 0FFFH, can be disabled after it initializes the SBC-I. A 2716, a 2732, or a 2764 may be used in the EPROM socket. The RAM is partitioned by setting up a bipolar RAM which provides the ability to enable any 4k segment of RAM and address it at any 4k boundary of the CPU address space. Thus a fixed RAM for the operating system can be established, and several programs may be loaded into the remaining RAM which can subsequently be brought into the CPU address space by appropriate operations on the memory management.

3.2.2 Serial Ports

A Z-80A SIO provides two independent serial ports. Both ports are RS-232C compatible and can operate at software-selectable speeds via two channels of a Z-80A CTC. In addition, provision is made to allow a synchronous MODEM to be connected to SIO A. (A synchronous MODEM supplies both the receive and transmit clocks for the serial ports.) The baud-rate clock is supplied by a 2.4576 MHz packaged oscillator.

3.2.3 Parallel Ports

A Z-80A PIO provides a bidirectional parallel port via its "A" port, and control lines from its "B" port. These lines run to connectors providing an interface to parallel devices. Some of the "B" lines are used for on-board functions.

3.2.4 Reset

Both the user and the main system are able to reset the SBC-I. However, the user reset will reset only his SBC-I, while the main system reset will reset all SBC-I's. A monostable provides a 100uSec reset pulse regardless of the length of time the user enables the reset button. This is to prevent the loss of the dynamic RAM data during reset. In addition, a software reset is implemented which will allow the master CPU in the system to reset the SBC-I in the system. This allows the master CPU to "wake up" an SBC-I that doesn't respond to an inquiry. In this manner a user need never have to reset his module in the event of software bugs; the master CPU will keep it running.

3.2.5 SBC-I is a Slave

The SBC-I cannot function as the main processor of the system. It is dedicated to its user. Only the FIFO on-board communicates with the system, which must have a master processor overseeing the system functions.

3.2.6 Communication with the Master CPU

Communication with the Master CPU in the system occurs via a 1k byte FIFO (First-In, First-Out) memory which provides a means for passing messages and blocks of data between the SBC-I and the Bus Master.

3.2.7 S-100 Compatibility

Only those operations required for the FIFO are IEEE-696 (S-100) compatible, because access by any other means (memory or DMA) is not implemented. Thus, the SBC-I appears only as an I/O port-accessed device to the master CPU. For the I/O operations, the SBC-I is completely IEEE-696 (S-100) compatible.

3.3 Specifications

Central processor:
Z80A, Z80B CPU - 2, 4 or 6 MHz operation.

Memory:
64kbytes RAM, optionally 128kbytes. Uses 200nsec HM4864-3 dynamic RAM at 4 MHz. Memory management circuit allowing 4kbyte segmentation. 128 cycle refresh devices required.

Serial:
Z80A SIO - 2 RS-232C ports, independent operation. Speeds from 110 to 19200 baud.

Parallel:
Z80A PIO - 1 bidirectional port with 4 handshake lines, 4 independent input or output lines. RS-422 adapter available.

EPROM:
2716, 2732, or 2764 device may be used (2716 is standard).

FIFO:
1kbyte 4801 or 2kbyte 2016 may be used (2016 is standard).

S-100 Bus Signals:

A0-A7	sINP	INT*
DO0-DO7	sOUT	+8V
DI0-DI7	sINTA	+16V
RESET*	pWR*	-16V
POC*	pDBIN	GND

Dimensions:
5.125" x 10.00", excluding edge connector

Workmanship conforms to the requirements of MIL-STD-454.

Forced air cooling is required.

3.4 Installation

Upon receipt of SBC-I, check the shipping package for signs of abuse which may indicate possible damage. Check the board physically to look for any parts which may have been damaged during shipping. If any diskettes were shipped with SBC-I, check the diskettes for signs of damage which might be any bending or signs of a sharp object placed against the diskettes. Diskettes are quite fragile and any warping of the surface of the diskette will render it inoperative. Notify Teletek of any discrepancies and call the shipping company if there is shipping damage.

SBC-I is ready for immediate use upon receipt. It requires only that the peripherals which will be used with it be connected to the appropriate connectors along the top of the board. For the particular connections required, see the adjoining section entitled "Peripheral Connections."

SBC-I need only be plugged into a standard S-100 bus for power and it will be functional, able to utilize the peripherals connected to it with the memory on board. The SBC-I needs to be in a well ventilated area due to the high density of IC's on board. Ideally, the board should be mounted vertically in a stream of air which will be moving across the face of the board. Whatever the mounting position, forced-air cooling is essential. Bring peripheral cables neatly away from the board with enough slack to prevent any tension being applied to the cable, as this may cause the cable to separate from its crimp connection causing intermittent problems.

Some versions of SBC-I do not have on-board RAM. If no RAM is on-board, it must be supplied by installing the 200nsec 64k devices in the columns of empty sockets near the right side of the board. Pin 1 on the IC's should point left. The RAM devices must use the 128 cycle refresh mode in order to be compatible with the SBC-I's refresh circuit. Most 64k RAMs currently on the market meet this requirement - one exception is the Texas Instruments TMS 4164 which requires 256 rows to be strobed during refresh.

3.5 Peripheral Connections

3.5.1 Serial Ports

SIO A and SIO-B

						(20)
2	4 RXC*	6	8 TXC*	10 USER RESET	12	14 DTR IN
	(2)	(3)	(4)	(5)	(6)	(6)
1	3 DATA IN	5 DATA OUT	7 RTS IN	9 CTS OUT	11 DSR OUT	13 GND

EIA pins are shown in parentheses

*-These clock signals are on SIOA only

These are the connections going into Channels A and B of the SIO chip. In this configuration, each channel appears as a data communication device, and will connect to a terminal or a printer.

IN and OUT refer to data direction with respect to the SBC-I. Data from an external device is IN to SBC-I, and data to an external device is OUT.

CTS (Clear To Send) and DSR (Data Set Ready) are outputs to the external device and are at a positive voltage levels when the SIO channel is ready to function. RTS (Request To Send) and DTR (Data Terminal Ready) are inputs which must be at a positive voltage level for the SIO channel to function if the Auto Enables option is activated through software.

Either channel can be crimp-connected to a 25-pin RS-232 connector by aligning Pin 1 of the cable from the SBC-I connector with Pin 1 of the 25-pin RS-232 connector. In this configuration the channel connects directly to a terminal or printer. To connect to a MODEM, the signals must be connected as follows:

SBC-I Pin #	EIA pin #	Direction	Function
5	2	OUT	Data to MODEM
3	3	IN	Data to SBC-I
11	4	OUT	RTS (Request To Send)
14	5	IN	CTS (Clear To Send)
7	6	IN	DSR (Data Set Ready)
13	7	--	Signal Ground
9	20	OUT	DTR (Data Terminal Ready)

(IN refers to data sent to SBC-I, and OUT refers to data sent to the MODEM.)

Note: If the terminal or printer does not provide RTS and DTR, Pins 4, 5, and 20 on the terminal side of the RS-232 male connector must be jumpered together. This ensures that the required handshake signals to the SIO port are provided. If the AUTO ENABLES feature of the SIO is not enabled this is not required. In the standard software provided, AUTO ENABLES is enabled.

3.5.1.1 EIA Serial Data Transfer Protocol (Control of Data Flow)

Prior to sending or receiving data, the four handshake lines should be active low. However, the SIO will allow control of its receive and transmit functions independently. If the "Auto Enables" function of the SIO channel is enabled (standard), the SIO will not send data until DTR is low (this function is labelled "CTS" on the SIO chip). This is handy for buffered printers which need to stop receiving data until the buffer is printed. By pulling DTR high, the printer will stop the flow of data from the SIO. When it is ready to receive more data, it pulls DTR low. Similarly, if "Auto Enables" is enabled, the SIO will not accept information until RTS is low (this function is labelled "DCD" on the SIO chip). This is primarily used with a communications link where, if signal conditions deteriorate, the data may be garbled.

3.5.1.2 RS-232-C Voltage Levels

A logic high (a binary ONE), or marking condition, is any voltage less than -3 volts to a minimum of -25 volts. A logic low (a binary ZERO), or spacing condition, is any voltage greater than +3 volts to a maximum of +25 volts. Any level between -3 and +3 volts is undefined. This is called the transition region. The maximum transition time between bit cells is four per cent of the basic clock period. The maximum voltage rate of change (slew rate) is 30 volts/uSec. Thus the maximum RS-232-C transmission speed, based on voltage swings of -12 to +12 volts, is 50,000 baud.

3.5.1.3 Serial Data Timing

Prior to transmitting data, the signal line is held high (marking). It goes low (spacing) to indicate the start of a character. The bits representing the character are then sent Least Significant Bit first, then a parity bit (if used), and finally 2 stop bits. The stop bits indicate the end of the character and are always logic ONEs. The standard SBC-I is set up for 8 data bits, no parity, and 2 stop bits.

The value of each character bit is held for the entire length of each bit cell. The length in time of each bit cell is the basic clock period, equal to the reciprocal of the baud rate. Thus for 9600 baud, each bit cell is 104 uSec long (.0001041 Sec=1/9600).

3.5.2 Parallel Ports

PIO A

2	4	6	8	10	12	14	16
RESET	+12	+5	GND	B STB	B RDY	A STB	A RDY
1	3	5	7	9	11	13	15
D7	D6	D5	D4	D3	D2	D1	D0

PIO B

2	4	6	8	10
	D1		D2	D3
1	3	5	7	9
	D0		-12	GND

These are the connections into the PIO chip. The PIO chip has two parallel ports, A and B. As configured, PIO A may be used as an input, output, bidirectional or control port with four handshake lines. PIO B is the same except that it does not have bidirectional capabilities or handshake lines.

The signals are:

D0 - D7 8 data lines

A STB Strobe input pulse from a device. Depending on the mode of operation, it means:
1. Output mode: Positive edge of this strobe is issued by the device to acknowledge the receipt of data made available by PIO A.
2.Input mode:The strobe is issued by the device to load data from the device into PIO A.
3. Bidirectional mode: Same as 1, except output data are present only while A STB is low.
4. Control mode:The strobe is inhibited internally.

A RDY Ready output to a device. Depending on the mode of operation, it means:
1.Output mode: Indicates that the data bus is stable for transfer to the device.
2.Input mode: When active, it indicates that PIO A is ready to accept data from the device.
3. Bidirectional mode: Same as 1.
4. Control mode: Always in a low state.

RESET The active-low reset line on the SBC-I. This can be used to reset a hard disk connected to PIO A.

B STB Used when PIO A is in the bidirectional mode; strobes data from the device into PIO A.

B RDY Used when PIO A is in the bidirectional mode; it goes high to indicate that PIO A is ready for data from the device.

The software supplied by Teletek allows PIO A to be set up as an input port or an output port printer. PIO B is set up in the control mode as follows:

D7 is interrupt request from S-100 bus (an input). Not available for the user.

D6 is the EPROM enable output. Not available for the user.

D5 is attention request from the S-100 bus (input). Not available for the user.

The remaining bits D0-D4 are not used internally and can be utilized by the user. D0-D3 are supplied on the PIO-B connector.

3.6 Theory of Operation

The SBC-I is a stand-alone computer (CPU with ROM, RAM, serial and parallel I/O) which can communicate with the S-100 Bus Master via a FIFO (First-In, First-Out) memory. Because its operation is independent of the S-100 bus, several SBC-I's can be resident in a system, providing inexpensive multiple-processor, multiple-user capabilities.

3.6.1 Reset

The SBC-I can be reset in three ways: via an active-low line from the user; when RESET* on the S-100 bus is low; whenever Port 03 is read by the master CPU. Any of these reset operations will trigger a monostable which will produce a 100 uSec pulse to reset the on-board logic. Because of this short reset pulse, dynamic memory data will not be lost.

3.6.2 Reset-Jump

After a reset operation, the EPROM/ROM on board will be enabled. This ROM occupies location 0000H to 1FFFH, an 8k-byte block (thus a 2716,2732, or 2764 EPROM may be used). When the ROM is enabled, only the ROM will appear in this memory block: the underlying RAM can be written to, but not read. When the ROM is disabled, all RAM is active.

The initialization program in the ROM must set up the on-board IC's including the memory management bipolar RAM. The program in the ROM can then move itself to another area in RAM and execute that location. It is important to note that the instruction following the disable ROM operation will be fetched from RAM. The ROM is disabled by writing a 0 to Bit 6 of PIO B.

3.6.3 Memory Management

The SBC-I contains 128k bytes of RAM which are organized by a bipolar RAM into 32 independent 4k-byte blocks. Because the Z80A CPU can access only 64k bytes at a time, only 16 RAM blocks can be accessed by the CPU at one time. In addition, each block can be write-protected.

Two bipolar RAMs, each 16 x 4, provide a high-speed lookup table to control access to the dynamic RAM. The four high-order address lines from the CPU (A-12 - A-15) become the address lines for the bipolar RAMs. The selected bipolar RAM data then provide 4 translated address lines, a row-select signal to choose between the two 64k banks of RAM, and a write-protect signal. The write-protect signal will prevent any alteration of the protected RAM block. The protected block will act like ROM. The row-select signal selects the second bank. Blocks from Bank 0 and Bank 1 can be mixed in any manner.

The memory management can be used to keep more than one applications program in RAM at one time. Switching the bank of RAM in and out is much faster than a disk access. Alternatively, or in addition, 64k or more of data can be kept in RAM at one time for fast access.

The bipolar RAM is organized as follows:

Bit	Function
5	Write-protect, active high
4	Select Bank 1, active high
3	Ram A-15
2	Ram A-14
1	Ram A-13
Ø	RAM A-12

The 16 locations of the bipolar RAM are loaded by using the indirect I/O instructions of the Z-80A CPU. The high-order address lines A-12 and A-15 select which bipolar RAM location is accessed. The data on the data bus are then written into the bipolar RAM. The C register is always set to access Port 1CH. The following instructions can be used:

(The data are inverted by the bipolar RAMs. Thus to set a bit high, a zero must be written to the RAM.)

OUT (C), r : the B register is loaded to set A-12 through A-15 as desired. Register r contains the desired data.

OUTI, OUTD : the B register is loaded to set A-12 through A-15 as desired (ØØ, 1Ø, 2Ø, etc), and the appropriate data in RAM or ROM are loaded into the bipolar RAMs. Note: don't alter the control of the RAM block in which the memory management data are stored, or erroneous data will be obtained in the next execution of this instruction. Remember that the decremented value of B is placed on the address bus.

Note: the bipolar RAMs must be initialized by the ROM after reset to access the dynamic RAM. Do not use dynamic RAM prior to this initialization due to the uncertainty of which RAM block will be active or write-protected.

3.6.4 Dynamic RAM Control

The dynamic RAMs are accessed whenever the CPU activates its M1 signal, or MREQ and RD or WR are active. Either case will cause a low on the output of U-19 which will clock U-12A and U-12B high. The output of U-12A is gated through U-35 to activate the RAS line of the selected bank of RAM ICs. The address multiplexers, U-32 and U-33, initially send the low order address lines from the CPU to the dynamic RAMs. When RAS goes active low, the RAMs latch these low order address lines internally.

The output of U-12B starts a positive pulse in U-20, a delay line. When the pulse in U-20 reaches the 20% delay point, Output 1 goes high, which clocks U-28B Q* low, and after being inverted in U-13, resets U-12B. U-28B changes the address multiplexers so that the high-order address lines of the CPU, as modified by the memory management circuit, will be sent to the RAMs.

When the pulse in U-20 reaches the 40% delay point, Output 2 goes high, which clocks U-28A Q* low. U-28A Q* sets the CAS lines of the RAMs low, which causes the RAMs to latch the high order CPU address provided by the address multiplexers.

When the pulse in U-20 reaches the 100% point, Output 5 goes high. This output is inverted by U-13 and resets U12A, to allow the RAM RAS circuits to pre-charge prior ro the next access.

When the RFSH output of the CPU goes low, the CPU places a refresh address on the lower seven address lines. When MREQ subsequently goes active, a memory cycle is started which is identical to a normal RAM access, except that the address multiplexers do not select the upper address lines and CAS remains inactive.

3.7 Options

3.7.1 ROM Options

The SBC-I can support 2716, 2732, and 2764 EPROMs as well as their masked-ROM counterparts. The ROM socket is either 24 or 28 pins and the option jumper below U47 is set according to the device. The following table summarizes the requirements.

ROM	Socket	Jumper
2716	24	E5 to E6
2732	24	E5 to E7
2764	28	E5 to E7

3.7.2 Wait State Options

SBC-I can generate one memory wait-state for the on-board memory cycles. The available options for this wait state are during all ROM accesses, all M1 cycles, or all memory cycles. Usually, only the ROM requires a wait state. For operation at a 6 MHz CPU clock, and with 200nSec RAM, a wait state will be required for all memory cycles. The jumpers for the various wait states are located below U32:

Wait State	Jumper
ROM only	E1 to E4
all M1	E1 to E2
all memory	E1 to E3

3.7.3 CTC

Two channels of a Z-80A CTC provide the clocks for the SIO. Channel 0 provides the clock for SIO-A, and Channel 1 provides the clock for SIO-B. The trigger inputs of Channels 0 and 1 connect to a 1.2288 MHz source. Thus all standard serial transmission rates will be generated by loading the appropriate integral divisor into the CTC channel. The CTC channel must be set to the Counter mode. The divisor loaded into the CTC channel is calculated as follows:

D=1,228,800/(Baud Rate X R) where D = divisor, Baud Rate = desired serial speed (4800, 9600, etc), and R is the lock divider set in the SIO channel (16, 32, 64).

Example: Desired Baud Rate = 19,200; with SIO divider set to 16

D=1,228,800/(19,200 x 16)
D=4

The output of Channel 2 of the CTC connects to the input of Channel 3. This allows a large divisor to be implemented to produce a one-second interrupt in Channel 3. The trigger input of Channel 2 connects to a 9,600 Hz source.

3.7.4 PIO

PIO-A provides parallel communication with an external device. Part of PIO-B provides on-board control functions while the four lines can connect to an external device. Because PIO-B provides the Z-80 Mode II vectored interrupt from the S-100 bus, PIO-A cannot be set to the bidirectional mode. The on-board functions of PIO-B are:

PIO-B bit	Function
7	Interrupt request from S-100 bus, active low. This is an input.
6	ROM enable, active high. This is an output.
5	Attention bit from S-100 bus, active low.
4	Not used.

To avoid confusion, only Bits 5 and 7 of PIO-B should be enabled for interrupts. PIO-B is set up in the control mode.

3.7.5 SIO

Full handshaking is available on both channels of the SIO. In addition, Channel A can connect to a synchronous MODEM that provides the receive and transmit clocks. A user reset line is available at each serial connector. This is an active-low signal that will reset the SBC-I.

If Channel A is to connect to a MODEM, the six RS-232 connections DIN, DOUT, RTS, CTS, DSR, and DTR must be swapped to the appropriate lines from the MODEM. In addition, for connection to a synchronous MODEM that supplies the transmit and receive clocks, the connections to TXCA and RXCA must be cut, and jumpers added to U-44 to supply the MODEM clocks.

Connections required for a MODEM are:

EIA	SBC-I
2	5
3	3
4	11
5	14
6	7
20	9

If a synchronous MODEM is employed that supplies transmit and receive clocks for the SIO, the connections from the CTC to Pins 13 and 14 of the SIO must be cut, and jumpers installed from Pin 13 of the SIO to Pin 11 of U44 and Pin 14 of the SIO to Pin 3 of U-44.

3.7.6 S-100 Bus Addressing

The SBC-I occupies four I/O locations in the S-100 bus I/O space. Address lines A-2 through A-7 of the S-100 bus are decoded to determine the SBC-I address. To set the address, jumpers are placed in the 14-pin address-select pad. This pad is located in the lower right part of the board, just below U11. The pins select A7 through A2 from left to right. If no jumper is in place, the comparator will respond to a logic-high address line. If the jumper is in place, the comparator will respond to a logic-low address line. Example:

Address desired = C0H

Address-select pad

A-7	Open
A-6	Open
A-5	Jumper
A-4	Jumper
A-3	Jumper
A-2	Jumper

3.7.7 FIFO

All information exchanged between the S-100 bus Master and the SBC-I occurs via the on-board 1k-byte FIFO memory. The procedure for passing information is as follows: First, clear the FIFO address counters by 1) performing any read or write to Port 10H by SBC-I, or 2) performing a read operation to Port 02H by the S-100 bus Master. Second, read or write the desired data to the FIFO by performing a block I/O transfer to the FIFO data port. Finally, request an interrupt 1) to the SBC-I by writing any data to Port 00 by the S-100 bus Master, or 2) to the S-100 bus Master by any operation to Port 18H by the SBC-I.

When an interrupt request is serviced, the routine must first clear the interrupt request by 1) performing a read to Port 01 by the S-100 bus Master, if the request is from the SBC-I, or 2) performing any read or write operation to port 14H if the request is from the S-100 bus Master.

3.7.8 1K or 2K FIFO RAM

The on-board FIFO RAM can be 1K or 2K bytes in size. If a Mostek MK4118 or MK4801 RAM (1k byte) is used, Pin 19 must be connected to +5 volts. If a 2k byte RAM is used, Pin 19 must connect to Pin 5 of U-22. Therefore, the option pad E10 connects to E11 for a 1K RAM. For a 2K RAM, E10 connects to E12.

3.7.9 S-100 Interrupts

SBC-I generates a Z-80 mode II interrupt response when the S-100 bus Master acknowledges the SBC-I interrupt request. The vector which SBC-I places on the bus is loaded by the bus Master into the register in SBC-I by writing it to Port 02.

To avoid confusion when more than one SBC-I is requesting an interrupt, a daisy chain is implemented to allow only one SBC-I at a time to respond. This enable daisy chain is at J-2. IEI is the input from he higher-priority SBC-I. IE0 is the output to a lower-priority SBC-I. Thus IE0 of one SBC-I connects to IEI of the next.

SBC-I responds to interrupt-acknowledge from the S-100 bus master without requiring pDBIN active high. If it is desired to respond only when pDBIN is active, connect E8 to E9. This allows the interrupt vector to be placed on the data bus only when pDBIN and sINTA are both active high.

3.7.10 SBC-I Interrupts

On-board the SBC-I, the PIO is the highest-priority interrupting device, the SIO is next, and the CTC is lowest.

3.7.11 Port Assignments SBC-I

Port	Function
00	SIO-A data
01	SIO-A status and control
02	SIO-B data
03	SIO-B status and control
04	PIO-A data
05	PIO-A control
06	PIO-B data
07	PIO-B control
08	CTC Channel 0
09	CTC Channel 1
0A	CTC Channel 2
0B	CTC Channel 3
0C	FIFO data

ØD-ØF	not used
10H	Clear FIFO address counters
11 - 13H	not used
14H	Clear interrupt request from S-100 bus
15 - 17H	not used
18H	Generate interrupt request to S-100 bus
19 - 1BH	not used
1CH	Memory management control
1D - 1FH	not used

3.7.12 Port Assignments S-100 Bus

Write Operation

Port	Function
ØØ	Generate interrupt request to SBC-I, Bit 7 PIOB
Ø1	Write to the FIFO
Ø2	Load interrupt vector register
Ø3	Generate attention request, Bit 5 PIOB

Read Operation

ØØ	Clear interrupt request from SBC-I
Ø1	Read data from the FIFO
Ø2	Clear FIFO address counters
Ø3	Reset SBC-I

Note: SBC-I occupies 4 I/O ports on the S-100 bus. Thus the above addressing for multiple SBC-Is will be multiples of 4: ØØ-Ø3, Ø4-Ø7, Ø8-ØB, 2Ø-23H, etc.

3.8 In Case of Trouble

If the SBC-I does not respond the first time it is connected try the following:

1. It is highly recommended that the entire manual be read carefully, especially the "Peripheral Connections" section.

2. If there is no response at the console, make sure that the handshake lines are functional and the baud rate is correct. Make sure that on-board RAM is working.

3. If the SBC-I was originally shipped without RAM, make sure the memory chips are installed correctly. The RAM devices must use the 128 cycle refresh mode in order to be compatible with the SBC-I's refresh circuit.

DRIVE INTERFACING

4.1 Disk Drive Interfacing

In controlling a disk drive from SYSTEMASTER, proper connections must be made to the disk drive in order for it to be operational. The drive options must be configured as outlined in the appropriate manufacturer's section following this introduction. Particularly important is the fact that the uPD-765 polls all drives in the system continuously to keep track of their status. With some drives this will interfere with their seek function (positioning of the head). Thus, most drives will have a stepper motor enable option, or simultanious seek option, that powers the stepper motor continuously, rather than just when the drive is selected. If the drive won't read initially, check for this option.

Drive interfacing deals with the proper connection of functional signals and the satisfying of electrical and mechanical requirements.

To help ease the shock of transition from the interchanging of various disk drives to other host controllers, a standard known as ANSI was developed which standardized the means of intercommunication between disk drive and host controller by specifying power requirements and voltage levels, edge connector and cable specifications, and specific pin numbers of the connector to particular functional signals.

4.2 ANSI Standards

Functional signals assigned to specific pin numbers of the connector are shown on the next page for a 5.25-inch disk drive and an 8-inch disk drive.

4.2.1 ANSI Standard for 5.25 Inch Drive

Signal Pin No.	Ground Pin No.	Signal
2	1	Not assigned (Head load)
4	3	In use control
6	5	Drive select 3 (Ready)
8	7	Index/sector
10	9	Drive select 0
12	11	Drive select 1
14	13	Drive select 2
16	15	Motor on
18	17	Direction select
20	19	Step
22	21	Composite write data
24	23	Write gate
26	25	Track 0
28	27	Write protected
30	29	Composite read data
32	31	Side one select
34	33	Disk change (Drive select 3)

4.2.2 ANSI Standard for 8-Inch Drive

Signal Pin No.	Ground Pin No.	Signal
2	1	Head current switch
4	3	Not assigned
6	5	Not assigned
8	7	Drive busy
10	9	Two-sided
12	11	Disk change
14	13	Side one select
16	15	In use control
18	17	Head load
20	19	Index
22	21	Drive ready
24	23	Sector
26	25	Drive select 0
28	27	Drive select 1
30	29	Drive select 2
32	31	Drive select 3
34	33	Direction select
36	35	Step
38	37	Composite write data
40	39	Write gate
42	41	Track 0
44	43	Write protected
46	45	Composite read data
48	47	Separated read data
50	49	Separated read clock

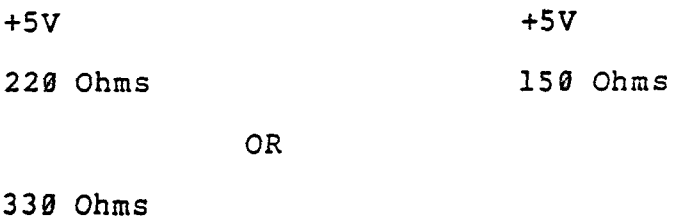
4.2.3 Electrical

1. Multi Drop Bus: Multiple drives may be connected to the same host controller as shown in Figure 1. Only one drive is logically connected to the interface at a time.

2. Voltage Levels (as measured at the driver)

Logical true	Active low	+0V to +0.4V
Logical false	Active high	+2.4V to +5.5V

3. Termination: Signal lines shall be terminated by one of the two resistive networks illustrated below, whether the termination occurs at the drive or the host, but only at the terminal point of a signal.



4. Signal Drivers: The signal drivers should have open collector output stages capable of sinking a minimum of 40mA at logical true (low) level, with maximum voltage of 0.4V as measured at the driver output.

5. Signal Receivers: The signal receivers should not unduly load the multi drop bus and should not require more than 40uA current from the driver at input high (2.4V) nor supply more than 1.6mA to a current sink at input low (0.4V) level.

4.2.4 Interconnecting Cable

Conductor Size
Copper- AWG #30 or larger for solid conductor
AWG #28 or larger for stranded conductor

Non-copper- Sufficient size as to yield a dc resistance not to exceed 110 Ohms per 1000 ft. per conductor.

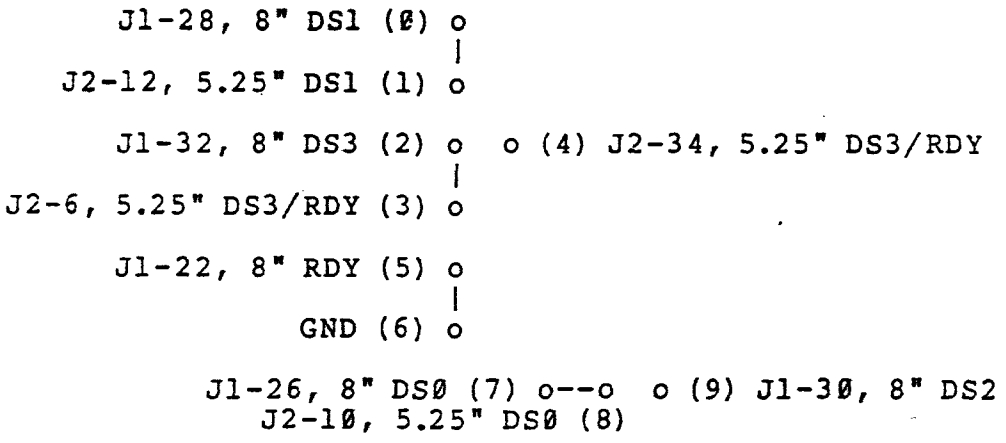
Stray capacitance- Capacitance between one wire in a cable and all others in the cable with all others connected to ground shall not exceed 40pF/ft. and the value shall be reasonably uniform over the length of the cable.

Mutual pair capacitance- Capacitance between one wire of the pair to the other shall not exceed 20pF/ft. and the value should be reasonably uniform over the length of the cable.

4.3 Mini-Floppy Drives

Use of mini-floppy drives requires the use of a special 50 to 34 pin adapter board. The following is a diagram of this board and its options.

Eight inch to five and a quarter inch drive p.c. adaptor board:



J1 is the 50 pin connector and J2 is the 34 pin connector.

4.3.1 Options

1) Pad 0 to 1 - 8" drive select 1 connected to 5.25" drive select 1.

2) Pad 1 to 2 - 8" drive select 2 connected to 5.25" drive select 1.

3) Pad 2 to 3 - 8" drive select 3 connected to 5.25" pin 6. Normally this pin is drive select 3 for 5.25" drives but is the READY signal for Micropolis drives.

4) Pad 2 to 4 - 8" drive select 3 connected to 5.25" pin 34. This pin is drive select 3 for Micropolis drives or READY for Pertec drives.

5) Pad 5 to 3 - 8" READY connected to 5.25" pin 6. This pin is the READY pin for Micropolis drives.

6) Pad 5 to 6 - 8" READY connected to GROUND. Since most 5.25" drives do not provide a READY signal it is neccessary to ground this line.

7) Pad 7 to 8 - 8" drive select 0 connected to 5.25" drive select 0.

8) Pad 9 to 8 - 8" drive select 2 connected to 5.25" drive select 0.

4.4 Micropolis 1015 Disk Drive

Required drive configuration:

1. DS1-4	Select appropiate drive address
2. HDLD	Enable this option

Install the termination network only in the last drive in the daisy chain.

Each drive requires 12 volts at 1.3A and 5 volts at 0.5A.

Required Pre-write Compensation: 250 ns.

Note: Since the Micropolis drive does not follow the ANSI standard several changes are neccessay on the p.c. adaptor board as follows:

1. Cut the trace between pads 2 and 3.
2. Cut the trace between pads 5 and 6.
3. Add a jumper between pads 2 and 4.
4. Add a jumper between pads 3 and 5.

4.5 Shugart SA-400 Disk Drive

Required drive configuration:

1. HL	Jumper
2. DS-1,2,3	Select appropiate drive address
3. MX	Open
4. MH	Open

Install the termination network only in the last drive in the daisy chain.

Each drive requires 12 volts at 1.8A and 5 volts at 0.7A.

Required Pre-write Compensation: none. (If pre-write compensation is wanted use 250 ns.)

4.6 MPI B-51/52 Disk Drive

Required drive configuration:

1. T1	Jumper
2. T2-T4	Select appropiate drive address
3. T5	Open
4. T6	Open
5. T7	Open

Install the termination network only in the last drive in the daisy chain.

Each drive requires 12 volts at 1.5A and 5 volts at 0.7A. Required Pre-write Compensation: none.

4.7 Caldisk 143M Disk Drive

Required drive configuration:

1.	DS A	Closed (DS = Dip Switch)
2.	DS B	Open
3.	DS C	Open
4.	DS D	Open
5.	JPR1	Open
6.	JPR2	Open
7.	JPR3	Open
8.	JPR4	Jumper
9.	JPR5	Open
10.	JPR6	Open
11.	JPR7	Jumper
12.	JPR8-11	Select appropiate drive address
13.	JPR12	Jumper
14.	JPR13	Open
15.	JPR14	Open
16.	JPR15	Open
17.	JPR16	Open

Install the termination network only in the last drive in the daisy chain.

Each drive requires 24 volts at 1.5A and 5 volts at 1.0A.

Required Pre-write Compensation: none.

4.8 Innotronics 410/420 Disk Drive

Required drive configuration*:

1.	EH	Trace intact
2.	AH	Open
3.	TH	Trace intact
4.	NT	Open
5.	TE	Trace intact
6.	NT	Open
7.	LM	Trace intact
8.	TM	Open
9.	WP	Trace intact (2 places)
10.	NP	Open (2 places)
11.	T4	Jumper
12.	T3, T5, T7	Jumpered on last drive in system
13.	S0-3	Select appropriate drive address

To use the Model 420 (Hard Sector) Disk Drive as a Soft Sector Disk Drive, the following link positions must be set:

1.	IB	Jumper
2.	HS	Open
3.	RD	Jumper
4.	SD	Open (2 places)
5.	VV	Jumper to accept -5 volt supply, otherwise open to accept -7 to -12 volts.

Install the termination network only in the last drive in the daisy chain.

Each drive requires +5 volts at 0.8A, -5 volts at .08A, and +24 volts. The current rating for the 24 volts supply depends on whether the drives will seek individually or simultaneously. If CP/M or a similar DOS is used, the total current is 1.4A. This is because Innotronics applies power to the stepper motor only when the drive is seeking. If software is used that can simultaneously seek on all drives in the system, each individual drive will require 1.4A.

Required Pre-write Compensation: 125 ns.
*The model 410 disk drives are shipped fully compatible with the FDC-I.

4.9 PerSci 277 Disk Drive System

The PerSci 277 disk drive system is a system composed of two 8-inch drive units requiring a 50 pin connector to the host system used. Pin assignments to functional signals of the 50 pin connector and the changes required to interface to SYSTEMASTER are shown below.

SM	Signal Pin No.	Ground Pin No.	Signal
2	2	1	Unassigned
4	4	3	Drive select 2 right
6	6	5	Ready 1
Cut	8	7	Index 1
Cut	10	9	Seek complete
12	12	11	Restore
Cut	14	13	Remote eject Ø
18	16	15	Direct headload
Cut	18	17	Drive select 2 left
20	20	19	Index Ø
22	22	21	Ready Ø
50	24	23	Spindle motor enable
26	26	25	Drive select 1 left
28	28	27	Drive select 1 right
Cut	30	29	Write protect 1
Cut	32	31	Remote eject 1
34	34	33	Direction select
36	36	35	Step
38	38	37	Write data
40	40	39	Write gate
42	42	41	Track Ø
44	44	43	Write protect Ø
46	46	45	Read data
48	48	47	Separated data
Cut	50	49	Separated clock

Required drive configuration:

1. Address DIP, U-11: connect pin 4 to 11, and pin 2 to 13.
2. A-B — Raw read data
3. D-BL — Select gate enabled
4. E,F,G — Open
5. J-Z — Enable L=Ø, and R=1
6. K-L — Wire-OR the Write Protect signals
7. M,N,P — Open
8. R,S,T — Open
9. U-V — Wire-OR the Index signals
10. W-X — Enable Index Ø
11. AB-AC — Enable Index Ø
12. AD-AE — Enable Index 1
13. AH-AJ — Enable Index 1
14. AM-AL — For spindle motor control

	or	
	AM-AN	Spindle motor runs continuously
15.	AP-AR	Wire-OR the Ready signals
16.	AS-AT	Remote eject, connects L and R together
17.	AU,AV,AW	Open
18.	BA-BB	Enable Index 1
19.	BD-BE	Seek complete enable
20.	BF,BH,BJ	Open
21.	BK-BM	Enable Index 0

Each drive requires 24 volts at 1.3A, 5 volts at 2.2A, -5 volts at 0.2A and for the spindle power, 7 - 10 volts 2.0A.

Because the PerSci has two physical drives connected to one head positioner, the SYSTEMASTER software must be made to seek and recalibrate only drive 0. Otherwise the uPD-765 will seek on both drives 0 and 1, and position past the correct track. Also, if the motor control option is used, the software must have the motor control option enabled.

If fast seek is required (seek rate less than the standard 10 ms step), the seek complete line must be connected to PIO B on one of its spare lines, and a 150 ohm 1/4 watt resistor connected to +5 volts. Contact the factory for further information relating to software requirements.

Required Pre-write Compensation: 250 ns.

4.1Ø Qume DT-8 Disk Drive

Required drive configuration:

1.	A	Jumper
2.	B	Open
3.	X	Jumper
4.	Z	Jumper
5.	HL	Open
6.	R	Jumper
7.	I	Jumper
8.	RI	Trace intact
9.	RR	Trace intact
1Ø.	C	Jumper
11.	D	Open
12.	DC	Open
13.	2S	Jumper
14.	DS	Open
15.	Y	Open
16.	DL	Open
17.	WP	Trace intact
18.	NP	Open
19.	S2	Trace intact
2Ø.	S1, S3	Open
21.	DS1-4	Select appropriate drive address
22.	B1, 2, 3, 4	Open

Install 2 resistor terminator modules into the last drive in the daisy chain.

Each drive requires 24 volts at Ø.9A and 5 volts at 1.1A.

Required Pre-write Compensation: none.

4.11 Shugart 800/801 Disk Drive

Required drive configuration:

1.	X	Jumper
2.	DC	Open
3.	D	Open
4.	C	Jumper
5.	I	Trace intact
6.	R	Trace intact
7.	S	Trace intact
8.	DS1-4	Select appropriate drive address
9.	T1, 3, 4, 5, 6	Jumper on last drive in system
10.	T2	Jumper
11.	HL	Open
12.	DS	Open
13.	RI	Trace intact
14.	RR	Trace intact
15.	Y	Open
16.	Z	Jumper
17.	800	Jumper
18.	801	Open
19.	A	Jumper
20.	B	Open

Each drive requires 24 volts at 1.7A, +5 volts at 1.0A, and -5 volts at 0.07A. Note: Many power supplies for floppy drives do not have the required current capability for 2 or more Shugart drives.

Required Pre-write compensation: 250 ns.

4.12 Siemens FDD 100-8D Disk Drive

Required drive configuration:

1.	RAD SEL 0-3	Select appropriate drive address
2.	RAD STEP	Jumper pads labelled "2"
3.	"36"	Jumper
4.	A	Open
5.	"34"	Jumper
6.	B	Open
7.	RR	Jumper
8.	"22"	Jumper
9.	RI	Jumper
10.	C	Open
11.	"20"	Jumper
12.	"24"	Jumper
13.	L	Jumper
14.	J	Open
15.	K	Open
16.	"18"	Jumper
17.	M	Open
18.	SS	Jumper
19.	HS	Open
20.	S	Jumper
21.	U	Jumper
22.	R	Open
23.	H	Open (for Activity Indicator)
24.	"16"	Open
25.	E	Jumper
26.	V	Open
27.	"12"	Jumper
28.	G	Open (cut trace)
29.	H	Open (for Phase Option)
30.	F	Jumper

Install the terminator resistor pack in the last drive of the daisy chain.

Each drive requires 24 volts at 1.6A, and +5 volts at 1.0A.

The Siemens drives need to be modified if more than 1 drive will be in the system. On the drive p.c. board, cut the trace going to pin 9 of IC 6C. Add a jumper between pins 9 and 12 of IC 6C. This change accommodates the NEC controller.

Required Pre-write Compensation: 250 ns.

4.13 Remex 2000/4000 Disk Drive

Required drive configuration:

1.	2S	Jumper
2.	DC	Open
3.	C	Jumper
4.	D	Open
5.	DS1-4	Select appropriate drive address
6.	1B, 2B, 3B, 4B	Open
7.	S1, 2, 3	S2
8.	TS-FS	Don't care
9.	4000/4001	4000
10.	DL	Jumper
11.	S	Jumper
12.	R	Jumper
13.	I	Jumper
14.	X	Jumper
15.	B	Open
16.	A	Jumper
17.	HL	Open
18.	Z	Jumper
19.	DS	Open
20.	Y	Open
21.	RI	Traces intact
22.	RR	Traces intact

The last drive in the daisy chain must have the resistor termination pack installed in location 7A.

Each drive requires 24 volts at 0.6A, +5 volts at 1.0A, and -5 volts at 0.05A.

Required Pre-write Compensation: 250 ns.

4.14 MFE 500/700 Disk Drive

Required drive configuration:

1.	SE1,SE2	Open
2.	SE3	Open
3.	L-1	Jumper
4.	L-2	Open
5.	L-3	Open
6.	DL-0	Don't care
7.	DS-1 thru DS-4	Select appropiate drive address
8.	HL3, HL5	Open
9.	HL1, HL2, HL4	Jumper
10.	RR	Jumper
11.	RIS	Jumper
12.	J-4	Jumper
13.	J-6	Jumper
14.	J-7	Jumper
15.	DL0, DL1	Trace intact
16.	DL2, DL3	Open
17.	PRU	Trace intact
18.	PRL	Open
19.	J-5	Jumper
20.	LC2, PS6	Jumper
21.	PS2, LC6	Open
22.	SS1, SS2	Jumper
23.	SS3, SS4	Open
24.	WP1	Jumper
25.	WP2	Open

Only the last drive in the daisy chain should have the termination circuit (Z-15) installed.

Each drive requires 24 volts at 1.4A, +5 volts at 1.2A, and -5 volts at 0.025A.

Required Pre-write Compensation: 250 ns.

4.15 Control Data 9406-2/3 Disk Drive

Required configuration:

1.	RR	Jumper
2.	RI	Jumper
3.	R	Jumper
4.	2S	Jumper
5.	HS	Open
6.	SS	Jumper
7.	DC	Open
8.	WP	Jumper
9.	NP	Open
10.	D	Open
11.	DD	Jumper
12.	DL	Jumper
13.	A	Jumper
14.	B	Open
15.	X	Jumper
16.	C	Jumper
17.	Z	Jumper
18.	Y	Open
19.	S1	Open
20.	S2	Jumper
21.	S3	Open
22.	E	Open
23.	DR	Jumper
24.	TS	Jumper
25.	FS	Open
26.	NS	Jumper
27.	OS	Open
28.	HO	Jumper
29.	IU	Open
30.	I	Jumper
31.	S	Jumper
32.	Switch 1	Select appropriate drive address

Install the termination network RM3 in the last drive only.

Each drive requires +24 volts at 1.4A and +5 volts at 0.8A.

Required Pre-write Compensation: 250 ns.

4.16 NEC FD1160 Disk Drive

Required configuration:

1.	P51, DLD	Jumper (DLS Open)
2.	P52, HLS	Jumper (HLD Open)
3.	P53, N	Jumper (RDR Open)
4.	P54, P55	Select appropriate drive address
5.	P56, E	Jumper (IFU Open)
6.	P57, C	Jumper (PWD Open)
7.	P58, PRI	Jumper (PRS Open)
8.	P59, N	Jumper (DLH Open)
9.	P60, FPL	Jumper (J7 Open)

Install the termination networks RN-1 and RN-2 in the last drive only.

Each drive requires +24 volts at 0.9A, +5 volts at 1.5A and -5 volts at 0.07A.

Required Pre-write Compensation: none.

4.17 Qume DataTrak 5 Disk Drive

Required configuration:

1.	DS0-3	Select appropriate drive address
2.	HS	Jumper
3.	MX	Open
4.	HM	Open
5.	P-M	Jumper
6.	P-S	Open
7.	A	Open
8.	B1	Open
9.	B3	Open
10.	HL	Open

Install the termination network U2B in the last drive only.

Each drive requires +12 volts at . A and +5 volts at . A.

Required Pre-write Compensation: none.

4.18 Pertec FD250 Disk Drive

Required configuration:

1.	Switch 1	Select appropriate drive address
2.	DP	Open
3.	DH	Open
4.	IS	Jumper
5.	DC	Open
6.	HL	Jumper
7.	DL	Open
8.	IB	Open
9.	HB	Jumper

Install the termination network U2 in the last drive only.

Each drive requires +12 volts at 1.6A and +5 volts at 0.8A.

Required Pre-write Compensation: none.

Note: Since the DataTrak 5 does provide a READY signal the following change is neccessary on the p.c. adaptor board:

1. Cut the trace between pads 5 and 6.
2. Add a jumper between pads 4 and 5.

4.19 Pertec FD650/651 Disk Drive

Required configuration:

1.	J101, 1-16	Open
2.	J101, 2-15	Open
3.	J101, 3-14	Open
4.	J101, 4-13	Open
5.	J101, 5-12	Jumper
6.	J101, 6-11	Open
7.	J101, 7-10	Open
8.	J101, 8-9	Jumper
9.	S1	Open
10.	4B, 3B, 2B, 1B	Open
11.	2S	Jumper
12.	IWBSY	Open
13.	IHCS	Open
14.	ID	Open
15.	RI	Jumper
16.	RR	Jumper
17.	SA	Jumper
18.	SS	Open
19.	SH	Open
20.	X	Open
21.	DDS	Open
22.	DD	Jumper
23.	S3	Open
24.	Switch 1	Select appropriate drive address
25.	650	Open
26.	651	Jumper
27.	DL	Open
28.	DSSEP	Jumper
29.	SSD	Open
30.	DSD0	Jumper
31.	HCS	Open
32.	T43	Jumper
33.	WP	Jumper
34.	NP	Open
35.	Ø	Open
36.	WPTD	Open
37.	Z	Jumper
38.	PNL	Open
39.	BDL	Open
40.	S	Jumper
41.	R	Jumper
42.	I	Jumper
43.	D	Open
44.	S2	Jumper
45.	DC	Open

Install the termination networks U1 and U2 in the last drive only.

Required Pre-write Compensation: none.

4.20 Shugart 850/851 Disk Drive

Required configuration:

1.	X	Shunt intact
2.	DC	Open
3.	D	Open
4.	C	Jumper
5.	I	Shunt intact
6.	R	Shunt intact
7.	S	Shunt intact
8.	DS1-4	Select appropriate drive address
9.	HL	Shunt open
10.	DS	Open
11.	RI	Trace intact
12.	RR	Trace intact
13.	Y	Open
14.	Z	Shunt intact
15.	850	Jumper
16.	851	Open
17.	A	Shunt intact
18.	B	Shunt open
19.	1B, 2B, 3B, 4B	Open
20.	2S	Jumper
21.	WP	Trace intact
22.	NP	Open
23.	S1	Open
24.	S2	Jumper
25.	S3	Open
26.	DL	Jumper
27.	M	Jumper
28.	TS	Open
29.	FS	Jumper
30.	IW	Jumper
31.	RS	Jumper
32.	RM	Open
33.	HLL	Open
34.	IT	Jumper
35.	HI	Open
36.	F	Open
37.	AF	Jumper
38.	NF	Open

Install the termination network IC2F in the last drive only.

Each drive requires +24 volts at 1.0A and +5 volts at 1.1A.

Required Pre-write Compensation: 250 ns.

4.21 Tandon TM1ØØ Disk Drive

Required configuration:

1.	MX	Open
2.	HS	Jumper
3.	HM	Open
3.	NDSØ-NDS3	Select appropriate drive address

Install the termination network 2F in the last drive only.

Each drive requires +12 volts at Ø.9A and +5 volts at Ø.6A.

Required Pre-write Compensation: none.

4.22 Tandon TM848-1 and TM848-2 Disk Drives

Required configuration:

1.	DS1-DS4	Select appropriate drive address
2.	1B-4B	Not installed
3.	Z	Jumper
4.	Y	Open
5.	R	Jumper
6.	RR	Jumper
7.	RM	Open
8.	RI	Jumper
9.	I	Jumper
10.	D	Open
11.	DL	Open
12.	DC	Open
13.	2S	Jumper
14.	DS	Open
15.	HL	Open
16.	C	Jumper
17.	A	Jumper
18.	B	Open
19.	X	Jumper
20.	WP	Jumper
21.	NP	Open
22.	S1,S3	Open
23.	S2	Jumper
24.	M1,M3	Jumper
25.	M2,M4	Open
26.	MC1	Jumper
27.	MC2-MC4	Open

Install termination network in the last drive only.