SUPERLETTER

Serving SuperBrain and CompuStar Users Around The World

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Superletter's offices will be closed from Novembers 7th through December 27th due to international travel.

No news yet from Intertec regarding their new product line. Early reports from good sources speak about an 8/16 machine with a detached keyboard that will run as a multi-user system with CP/M 80, CP/86 and MP/M. Still no confirmation the new products will be able to use IBM-compatible software.

Rumors lately about Intertec's financial health have not been encouraging. Yet we also get conflicting information from certain dealers and those close to the company that Intertec is here to stay and any news otherwise is false.

We're hearing grumblings about the video portions of the SuperBrain II's which are going down due to weak solder and contact points on the *underside* portion of thevideo boards. Actually, it's a comparatively simple problem to fix, but if you don't know what to look for, it can be a headache.

The life of Superletter is dependent on a fragile connection between thousands of Intertec users, the factory and us. In order to have a strong end-user network, we need your continued support. Subscriptions and ad dollars help dealers, vendors and us maintain a presence in the marketplace.

As other computer clubs fold or gently disappear, we move forward. As of now, we are one of the longest-lived, if not *the* oldest, professionally published microcomputer newsletter devoted to a single computer system.

Our aim is to always be here for your needs, regardless of what happens in the rapidly changing computer landscape.

Have a Happy Holiday Season!

Albert Abrams
EDITOR

Technical Corner

Floppy Disk Motor Shutoff, Extended Storage Capacity, and Variable Seek Rates for the CMC Targa BIOS.

by
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With the addition of a CMC Targa 10 MB disk drive to my SuperBrain, I was distressed to learn that the CMC PROM did not support the extended floppy disk features which had been provided by Information Engineering's SB/E PROM. Most of my diskettes were formatted at 40 tracks per side, and a 40 TPS operating system was needed in order to dump them onto the hard disk. Inspection of the CMC BIOS revealed provisions for several different disk formats. Unfortunately, CMC did not follow through and implement these formats at the PROM level. Additionally, with the hard disk in operation, the floppy disks sit idle most of the time, and it would be quite advantageous to turn them off between their infrequent operations.

The solution to these problems is to use a different PROM, one which knows about extended floppy disk functions. A "quick fix", which works with the SB/E PROM is provided though use of CMC's BOOTHD utility. BOOTHD is a program which runs in the CP/M transient program area (TPA) and loads the CMC operating system from the hard disk's system tracks. First, boot the SuperBrain with SB/E and optionally use ACTIVATE to establish the desired floopy disk parameters. This will modify two addresses in CPU2's RAM, which control disk motor shutoff, seek rate, and tracks per side. Then run BOOTHD, which will overlay SB/E with the CMC operating system. Because the control bytes are in CPU2's address space, they aren't modified by the CMC BIOS. This procedure may also work with the SOS PROM, but I've never had an opportunity to try it.

A more elegant solution involves modification of the CMC BIOS so that it initializes the floppy disk control bytes in CPU2's RAM during a restart operation. The following patch for CMC BIOS was designed for the SB/E EPROM. It's build around two of the Intertec DOS 3.2 floppy disk subroutines, which swap CPU2's RAM in and out of CPU1's address space. Information Engineering placed the two disk control bytes starting at location 8800H in CPU2's RAM. Location 8800H controls disk motor shut off and seek rate, while location 8801H contains the number of tracks per side. The low order nibble of 8800H controls the seek rate, with values of 0, 1, 2, and 3 selecting respective seek rates of 30ms, 20ms, 12ms, and 6ms. The high order nibble controls disk motor shutoff, with a value of 8 activating disk motor shutoff, and a zero value deactivating it. For example, storing 83H at location 8800H selects disk motor shutoff and 6ms seek rate.

I located the patch in GOCPM, immediately after CALL TRANS, which initializes floppy disk control bytes during a cold start. It's also possible to put the patch at the beginning of WMRET, in which case the control bytes are initialized during a cold start and updated with every warm start. Values to be stored at locations 8800H and 8801H can be added to the end of the Intertec configuration area to allow software modification of floppy disk characteristics. When you add the patch to CMC BIOS, make sure that the HFIRST equate is set to TRUE, which selects the hard disk as disk A. Also set an equate for the desired floppy

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Technical Corner

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disk format (35/40/70/80 tracks per side, single/double sided). Assemble the patched BIOS and incorporate it into CPMH10S.COM (SPMH10D.COM for a double sided system) using DDT. Run CPMH10S and write a copy of the new operating system onto both the hard disk and a floppy diskette. Unfortunately the SB/E PROM doesn't know that the hard disk is there, so you'll have to start the system by placing the floppy that you SYSGENed with CPMH10S, in drive A and pressing both reset buttons. This procedure boots the CMC operating system from the floppy disk, but all subsequent warm starts default to the hard disk. A better solution would be to program a new PROM which contained both the hard disk boot loader and the extended floppy disk driver routines (a hint to reader with an EPROM blaster).

CMC BIOS Patch for Disk Motor Shutoff Variable Seek Rate and 40 Tracks per Side

Dr. James N. Herron
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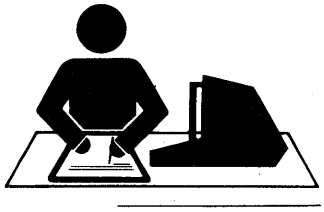
Salt Lake City, UT 84108

```
;
;  Equates
;
DMA1   EQU   0EB99H   ;Select CPU-2 RAM
DMA2   EQU   0EBA8H   ;Select CPU-1 RAM
SETFD  EQU   08800H   ;Bottom of control byte area
;
;  Configuration Area
;
;  Note:add these bytes to the end of the
;       Intertec Configuration Area(location 0EF20H)
;
       DB    83H    ;Disk motor shutoff,6ms seek rate
       DB    28H    ;40 tracks per side
;
;  Code Segment
;
       CALL  DMA1   ;Select CPU-2 RAM
       LHLD  INTFD  ;Load HL with control bytes
       SHLD  SETFD  ;Store them at 8800H
       CALL  DMA2   ;Restore CPU-1 RAM
;
;
```



-New Products-

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Contact: Bill Dotson

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- Locating file positions on a diskette
- Locating specific data within a file
- Moving data within a file (limited to one sector minimum)
- Searching forward or backward for specific information
- Directing data to a printer (CP/M list device)
- Moving data or files from drive to drive or from one location to another within a single drive
- Mapping the remaining free space on diskette
- Displaying the directories of all drives and user groups
- Providing an editing facility in either Hexadecimal or Ascii mode
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A hard-disk version is in the works and their newest update features automated controls. Price: $69.95

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4. "Mail Merger" pulls out specific information from your records in the "Data Base Manager" area and automatically inserts it into another document which you just produced on the "Word Processor". An example of this would be a form letter to club members or clients, or Board members, etc. "Mail Merger" neatly types in the required information such as name and/or address to create what seems like a personal letter.

Available for both the CompuStar and SuperBrain, I and II.

RS-232 Breakout Box
Remark Datacom, Inc.
4 Sycamore Drive
Woodbury, NY 11707
(516) 367-3806
Contact: Ms. Blossom Kramer

The "poorman's" breakout box has been made available by REMARK DATACOM INC. The Model 51 MINI-PATCH BOX provides all users of devices employing RS-232 interfaces with the ability to reconfigure the connections, or signal paths. This is usually necessary when interfacing new devices such as printers and CRT terminals.

The Model 51 is equipped with a male and female, DB-25, 25 pin connector. This allows the placement of the MINI-PATCH BOX in series with any RS-232 cable path. Of the 25 pins, pin 1 (Frame Ground) and pin 7 (Signal Ground) are carried thru from the male to the female connector. The remaining 23 signals from each connector terminate on female jack receptacles. Sup-

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Technical Corner II

FLOPPY DRIVE MOTOR SHUT-OFF
for any
SUPERBRAIN or COMPUSTAR
by
JONATHAN PLATT

I have been accumulating information on the subject of motor shut-off for some time. It is at a point now where I think I can present it to the readers of Superletter with some authority and detail. It has been my tradition to provide not only the how-to but the how-come, the background and sometimes theory as well. No sense in breaking tradition.

Several methods of implementing a motor shut-off feature on the SuperBrain or CompuStar have been employed thus far. IE was the first with their SB/E BIOS and EPROM. They use drive select D to signal whether the motors are on or off. Of course, a hardware modification and their special EPROM is required. SB/E allows only two drives on a system. Both drives run when the motor signal is activated. The motors are turned off after ten seconds of idle use and there is a delay of one second when reactivated to let them come up to speed.

Quite some time later, Intertec released Engineering Change Order (ECO) number E030038. Part to the method covered with this ECO is a bit crude because it asks you to cut a trace on each floppy drive board. In addition to isolating each drive from the motor-off signal, one jumper must be installed on the drive's shunt block socket for all but CDC drives. This jumper's function is to use the drive select signal to also turn on the selected drive's motor. In this manner only the drive being used has its motor running, dramatically increasing every drive's lifetime. It is also much easier on those frequently flaky power supplies. The motor is turned off after three seconds of idle use and there is (or should be) a delay of 0.25 seconds when reactivated to let it come up to speed.

I have supplied my customers with instructions on how to implement motor shut-off in a less destructive manner. I advised them to cut the one conductor which carries the motor-off signal from the main board to the floppy drives under the assumption that a ribbon cable makes for a cheaper cutting board than a floppy drive. Well, this worked with most drives but not Shugarts. The reason was that even though the conductor was cut, the Shugart drives did not keep the signal isolated from the back section of cable (on the other side of the cut.) Thus, more than one drive would be selected at once. Other drives did not have this problem.

One of my customers offered what I think is the best solution which is completely reversible if you decide that motor shut-off is not what you need. This is a streamlined version of my old method and is still functionally identical to the way Intertec implements it. But before I tell you what to do, let me tell you what it does.

TECHNICAL BACKGROUND

The boot EPROM initiates a drive operation by sending a command to the Floppy Drive Controller (FDC). When the FDC receives the command it activates a signal called Head Load (HLD). The HLD signal is the input to what is called a "one-shot". A one-shot basically delays a signal for a certain time set in hardware with a resistor and a capacitor. Intertec set it for 121.5 millseconds delay. After the delay the one-shot outputs the HLD signal back to an FDC input called Head Load Timing (HLT). Only after HLT becomes active will the FDC continue with the disk operation specified in the EPROM'S command.

Under Intertec's drive logic, a drive will only be selected when both the EPROM has the drive selected and HLD is active. So after one of the drives is selected by the EPROM and the FDC receives a command, HLD is activated. This sends a select signal to the selected drive. The select signal activates the drive and with the modifications it also turns the motor on.

Meanwhile, the one-shot is delaying HLD back to the HLT signal, giving the drive motor time to come up to speed before the FDC continues with the disk operation. Drive manufacturers specify a maximum time of 250 milliseconds (one quarter second) before the drive motor will be at its proper speed.

Once a disk operation had been completed, the FDC will count 15 revolutions of the disk and then turn off its HLD signal. Since the drive motors turn at 300 RPM, it works out to three seconds. When the HLD signal goes inactive, the drive is deselected and the motor turns off.

When Intertec designed their one-shot delay, they made it for 121.5 milliseconds. They were only thinking of the time it would take for the read/write head to load against

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Technical Corner II

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the diskette surface. Even this was a little long since 30 milliseconds is the standard for mini-floppies. This was long before they even heard about turning motors off. But even after Intertec finally learned how to accomplish motor shut-off, they still shipped their machines with the 121.5 millisecond delay. I believe they later released an ECO with the proper resistor value change to bring the delay to about 250 milliseconds.

The main effect of not waiting enough time for the drive to come up to speed would be CRC errors. This was not only a symptom of the wrong hardware delay but also some deficient programming in the EPROM. I received Intertec EPROM version 4.2 with my CompuStar 30, the equivalent of a QD SB II, last December. I studied their programming closely. The machine came with motor shut-off already installed but still had the wrong resistor value in the delay circuit.

If there has been no new EPROM released since 4.2, then the bugs are still there as well. First, the internal programmed delay for drive speed is about 138 milliseconds instead of 250. Second, when the same drive is accessed after the three second idle shut-off time, the EPROM does not delay at all. Again, there should be a delay of 250 milliseconds. Luckily, they did think of delaying when going from one drive to another even though the three second time out has not occurred. This must be done since each drive runs independently. Think of how PIP goes back and forth between drives.

Any SuperBrain or CompuStar ever made will support motor shut-off. But if you are using an Intertec boot EPROM then you may have to make one hardware modification. The time allowed for the drive motor to come up to speed is crucial. The hardware delay problem can be remedied by replacing a resistor. The problem with the Intertec EPROM can only be fixed by buying a better EPROM unless they have fixed theirs by now. At the risk of sounding unhumble, the SOS BIOS EPROM handles all timing properly even without the aid of the one-shot. So any hardware change would not be necessary with this EPROM.

If you are using the SB/E BIOS motor-off feature, either stick with what you have or undo the damage your hardware modifications did and use the SOS EPROM. Intertec's EPROM will not respond to disk features of the SB/E BIOS.

MODIFICATIONS

If you are implementing motor shut-off with the Interrtec EPROM, you will need to do the board modification. If you are using the SOS EPROM skip the board modification. It involves removing a resistor from the PC board and replacing it with a new one of higher value. Drive modifications should be followed under all circumstances. If you use any other EPROM, check with the manufacturer before continuing.

If you are not certain about any of the terms used in the following directions then you would be better off by having a technician do the modifications for you.

BOARD MODIFICATION

First take the cover off and locate the floppy drive cable connector on the upper right edge of the main board. To the left of the connector are two columns of chips. Counting from the top edge downward, the resistor is between the second and third chips of those two columns. Just below the resistor there should be a capacitor between the third chips of those two columns. The resistor is color coded with a red, violet, orange and gold band in that order. It is also known as a 27K Ohm resistor.

Remove the resistor and put a 56K Ohm resistor in its place. This involves soldering, so if you do not know what you are doing let a technician do it for you. A 56K Ohm resistor is color coded with a green, blue, orange and gold band in that order. The gold band means that it has a five percent tolerance.

This hardware change will increase the delay before a disk operation to 252 milliseconds. Now the drives will have enough time to come up to speed before trying to attempt any disk access.

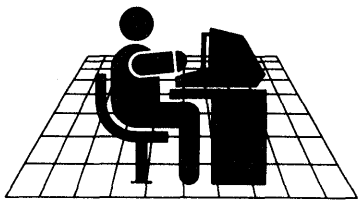
DRIVE MODIFICATIONS

Take the cover off and remove the disk drives. Cut a piece of heavy adhesive tape about one inch long and one eigth inch wide for each drive. I usually use clear stranded packing tape. The tape will cover a conductive connector strip on each drive. On a table, orient the drives as they would normally stand in the computer. Find the eigth gold connector strip up, counting from the bottom strip. Cover this strip on both sides of the connector tab.

If you have CDC drives in your computer, the drive modifications are complete. If you have Tandon, Shugart or other similar drives, continue by locating the shunt block socket on your drives. They usually have the break-away tabs plugged into them. If the sockets are labeled they will have DS0, DS1, DS2, DS3, MX, HM and HS printed on the board beside the socket. Jumper both HS and HM. HS should already have been jumpered anyway. The drive modifications are complete. Put the connectors back onto the drives making sure the tape stays in place. Put the drives back where they belong, replace the cover and test the system.

If the signals are not labeled, the best I can do is give you examples. On the Tandon drives which have a sixteen pin socket, the additional jumper goes from pin eight across to pin nine. On the Shugart drives which have a fourteen pin socket, the additional jumper goes from pin seven across to pin eight.

Have a Super day !



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-Programs-

These programs offer a good way to move files between CP/M machines, even with toatlly different disk systems. The only requirement is that each have a serial port. Transfer can be made with either a direct interface cable or a pair of modems. The programs are very tolerant of timing and contain the facility for retransmitting records containing transmission errors.

Listing 1
Program to transmit a CP/M file

```
;       Program to transmit a CP/M file through a serial port
;       Accesses port directly, bypassing the BDOS
;       Assumes an 8-bit word length and no parity
;
;       Version of 9/2/83
;
;
BOOT    EQU     0000H           ;CP/M reboot address
BDOS    EQU     0005H           ;CP/M BDOS entry point
TFCB    EQU     005CH           ;FCB for file to be transmitted
SIOSTA  EQU     07H             ;SIO status port
SIODAT  EQU     06H             ;SIO data port
IFLAG   EQU     02H             ;Input flag for serial port
OFLAG   EQU     01H             ;Output flag for serial port
BUFREC  EQU     128             ;Buffer size (CP/M records)
;
;
        ORG     100H
;
;       If required, place serial port initialization code here
;
TX:     LDA     TFCB+1
        CPI     ' '             ;Check for filename
        JNZ     OPEN
        LXI     D,FNMER         ;Print error message and reboot
ABORT:  MVI     C,9
        CALL    BDOS
        MVI     E,04H
        CALL    XMTBYT          ;Send EOT character
        JMP     BOOT            ;Return to CP/M
OPEN:   LXI     D,TFCB
        MVI     C,15
        CALL    BDOS            ;Open file
        INR     A
        JNZ     FOUND           ;File present
        LXI     D,FNFER         ;Point at error message
        JMP     ABORT           ;Print and reboot
FOUND:  XRA     A
        STA     TFCB+32         ;Set next record byte to zero
        MOV     C,A             ;Set record count in buffer to zero
READY:  PUSH    B               ;Save record count
        MVI     C,11
        CALL    BDOS            ;Get console status
        POP     B
        ORA     A
        JZ      READY1          ;No key pressed
        PUSH    B
        MVI     C,1
        CALL    BDOS
        POP     B
        CPI     03H
        JNZ     READY1
ENDXMT: LXI     D,EOTMSG        ;Print EOT message and abort
        JMP     ABORT
READY1: IN      SIOSTA          ;Read serial status port
        ANI     IFLAG
        JZ      READY           ;Wait for character to be received
        IN      SIODAT          ;Get received character
        ANI     7FH             ;Mask off bit 7 for ASCII codes
        CPI     04H
        JZ      ENDXMT          ;End transmission
        CPI     01H
        JZ      XMTREC          ;Transmit next record
        CPI     02H
        JNZ     READY           ;Ignore other characters
        LHLD    DATPTR
        LXI     D,-00080H
        DAD     D               ;Point at last record
        SHLD    DATPTR
        INR     C               ;Go back one record
XMTREC: DCR     A
        STA     RPTFLG          ;Save repeat flag
        CZ      COUNT           ;Increase record message if new record
XMTRC1: DCR     C               ;Decrease record count
        JP      XMTRC2          ;More in buffer
        LDA     EOFFLG
        ORA     A
        JZ      READFL          ;More in file
        LXI     D,EOFMSG
        MVI     C,9
        CALL    BDOS            ;Print EOF message
        MVI     E,03H
        CALL    XMTBYT          ;Send EOF byte
        JMP     BOOT
READFL: LXI     H,DATBUF
        SHLD    DATPTR          ;Point at beginning of data buffer
        XCHG
        INR     C               ;Initialize record count to zero
READ:   PUSH    B
        PUSH    D
        MVI     C,26
        CALL    BDOS            ;Set DMA address
        LXI     D,TFCB
        MVI     C,20
        CALL    BDOS            ;Read next record
        POP     D
        POP     B
        ORA     A
        JNZ     NOMORE          ;EOF detected
        LXI     H,00080H
        DAD     D               ;Point at next record in buffer
        XCHG
        INR     C               ;Increase record count
        MVI     A,BUFREC
        CMP     C
        JNZ     READ            ;Stop at end of extent
        JMP     XMTRC1
```

continued

Listing 1, continued

```
NOMORE: MVI     A,1
        STA     EOFFLG          ;Set EOF flag
        JMP     XMTRC1
XMTRC2: LDA     RPTFLG
        INR     A
        MOV     E,A
        CALL    XMTBYT          ;Send response to request for record
        LHLD    DATPTR          ;Point at next record to transmit
        MVI     B,80H           ;Character count for record
        MVI     D,0             ;Checksum for record
XMTRC3: MOV     A,M             ;Get next byte to send
        INX     H               ;Update pointer
        MOV     E,A             ;Save in E
        ADD     D
        MOV     D,A             ;Update checksum
        DCR     B
        JNZ     XMTRC3          ;More in record
        MOV     E,D
        CALL    XMTBYT          ;Send checksum
        PUSH    B
        MVI     C,4
        MVI     E,00H
XMTRC4: CALL    XMTBYT          ;Send 4 NULs to replace any missed bytes
        DCR     C
        JNZ     XMTRC4
        SHLD    DATPTR          ;Save pointer to next record
        LXI     D,RECMSG
        MVI     C,9
        CALL    BDOS            ;Print record message
        LDA     RPTFLG
        ORA     A
        JZ      NEXTLN          ;Skip 'again' if successful first time
        LXI     D,AGAIN
        MVI     C,9
        CALL    BDOS            ;Print 'again' if record repeated
NEXTLN: LXI     D,CRLF
        MVI     C,9
        CALL    BDOS            ;Print CRLF
        POP     B
        JMP     READY           ;Go wait for next prompt to send
COUNT:  LXI     H,RECCNT+4
COUNT1: INR     M
        MVI     A,'9'
        CMP     M               ;Over 9?
        RNC
        MVI     M,'0'
        DCX     H
        MOV     A,M
        CPI     ' '
        JNZ     COUNT1
        MVI     M,'0'
        JMP     COUNT1          ;Put 0 in message
XMTBYT: IN      SIOSTA          ;Transmit character through serial port
        ANI     OFLAG
        JZ      XMTBYT
        MOV     A,E
        OUT     SIODAT
        RET
;
FNMER:  DB      'File name missing',0DH,0AH,'$'
FNFER:  DB      'File not found',0DH,0AH,'$'
EOFMSG: DB      'Transfer complete',0DH,0AH,07H,'$'
EOTMSG: DB      'Transfer terminated',0DH,0AH,07H,'$'
RECMSG: DB      'Record #'
RECCNT: DB      '    0'         ;Record # transmitted
        DB      ' transmitted$'
AGAIN:  DB      ' again$'       ;Repeated record
CRLF:   DB      0DH,0AH,'$'     ;CRLF sequence
DATPTR: DW      DATBUF          ;Pointer to next data byte to send
EOFFLG: DB      0               ;Flag for EOF read
RPTFLG: DB      0               ;Flag for repeated record
DATBUF  EQU     $               ;Data buffer
;
        END
```

Listing 2
Program to receive a CP/M file

```
;       Program to receive a CP/M file through a serial port
;       Accesses port directly, bypassing the BDOS
;       Assumes an 8-bit word length and no parity
;
;       Version of 9/17/83
;
;
BOOT    EQU     0000H           ;CP/M reboot address
BDOS    EQU     0005H           ;CP/M BDOS entry point
TFCB    EQU     005CH           ;FCB for file to be transmitted
SIOSTA  EQU     07H             ;SIO status port
SIODAT  EQU     06H             ;SIO data port
IFLAG   EQU     02H             ;Input flag for serial port
OFLAG   EQU     01H             ;Output flag for serial port
BUFREC  EQU     128             ;Buffer size (CP/M records)
RETRY   EQU     4               ;Number of retries before quitting
;
;
        ORG     100H
;
;       If required, place serial port initialization code here
;
RX:     LDA     TFCB+1
        CPI     ' '             ;Check for filename
        JNZ     OPEN
        LXI     D,FNMER         ;Print error message and reboot
ABORT:  MVI     C,9
        CALL    BDOS
        MVI     E,04H
        CALL    XMTBYT          ;Send EOT character
        JMP     BOOT            ;Return to CP/M
OPEN:   LXI     D,TFCB
        MVI     C,19
        CALL    BDOS            ;Delete old file if present
        LXI     D,TFCB
        MVI     C,22
        CALL    BDOS            ;Make new file
        INR     A
        LXI     D,DFFER         ;Point at error message
        JZ      ABORT           ;Print and reboot
START:  MVI     C,30            ;Send some NULs first
        MVI     E,00H
NULS:   CALL    XMTBYT
        DCR     C
        JNZ     NULS
        IN      SIODAT          ;Clear serial data port
READY:  LDA     RPTCTR
        CPI     RETRY
        MVI     E,01H
```

continued

Listing 2, continued

```
        JZ      READY1          ;First time for this record
        INR     E               ;Change request character to 02H
        ORA     A               ;Test repeat counter
        JNZ     READY1          ;Try again if not zero
ENDXMT: LXI     D,EOTMSG        ;Print EOT message and exit
        JMP     ABORT
READY1: CALL    XMTBYT          ;Send prompting byte
READY2: MVI     C,11
        CALL    BDOS            ;Get console status
        ORA     A
        JZ      READY3          ;No key pressed
        MVI     C,1
        CALL    BDOS
        CPI     03H
        JZ      ENDXMT          ;Terminate if control-C pressed
READY3: IN      SIOSTA          ;Read serial status port
        ANI     1FLAG
        JZ      READY2          ;Wait for character to be received
        IN      SIODAT          ;Get received character
        ANI     7FH             ;Mask off bit 7 for ASCII codes
        CPI     03H
        JZ      CLOSE           ;Flush buffer and close file
        CPI     04H
        JZ      ENDXMT          ;End transmission
        CPI     01H
        JZ      RCVREC          ;Receive next record
        CPI     02H
        JNZ     READY2          ;Ignore other characters
RCVREC: MVI     B,80H           ;Byte count for record
        MVI     D,0             ;Initialize checksum
        LHLD    DATPTR          ;Prepare to store data
RCVRC1: CALL    RCVBYT          ;Get a byte
        MOV     M,A             ;Store in data buffer
        INX     H
        ADD     D
        MOV     D,A             ;Update checksum
        DCR     B
        JNZ     RCVRC1          ;Continue for 128 bytes
        CALL    RCVBYT          ;Get checksum
        CMP     D
        PUSH    PSW             ;Save status
        JNZ     RCVRC2          ;Bad read
        SHLD    DATPTR          ;Save new record pointer
RCVRC2: LXI     D,RECMSG
        MVI     C,9
        CALL    BDOS            ;Print received record message
        LDA     RPTCTR
        CPI     RETRY
        JZ      RCVRC3          ;First try
        LXI     D,AGAIN
        MVI     C,9
        CALL    BDOS            ;Print 'again'
RCVRC3: LXI     D,CRLF
        MVI     C,9
        CALL    BDOS            ;Print CRLF
        LXI     H,RPTCTR
        DCR     M               ;Decrement repeat counter
        POP     PSW
        JNZ     START           ;Successful read
        MVI     A,RETRY
        STA     RPTCTR          ;Reset counter for next record
        LXI     H,RECCNT+4
COUNT:  INR     M
        MVI     A,'9'
        CMP     M               ;Over 9?
        JNC     BUFCHK
        MVI     M,'0'
        DCX     H
        MOV     A,M
```

continued

```
        CPI     ' '
        JNZ     COUNT
        MVI     M,'0'
        JMP     COUNT           ;Put 0 in message
BUFCHK: LHLD    DATPTR
        LXI     D,-(DATBUF+BUFREC*128)
        DAD     D
        CC      FLUSH           ;Flush buffer if full
        JMP     READY           ;Go look for next record
FLUSH:  LXI     D,DATBUF        ;Start at beginning of buffer
FLUSH1: LHLD    DATPTR
        MOV     A,D             ;Compare to see if empty
        CMP     H
        JNZ     FLUSH2          ;More to go
        MOV     A,E
        CMP     L
        JNZ     FLUSH2
        LXI     H,DATBUF
        SHLD    DATPTR          ;Reset data pointer
        RET
FLUSH2: PUSH    D
        MVI     C,26
        CALL    BDOS            ;Set DMA address
        LXI     D,TFCB
        MVI     C,21
        CALL    BDOS            ;Write record
        POP     D
        ORA     A
        JZ      FLUSH3          ;Good write
        LXI     D,DERER         ;Disk error
        JMP     ABORT
FLUSH3: LXI     H,0080H
        DAD     D               ;Point to next record
        XCHG
        JMP     FLUSH1          ;Go write it if present
CLOSE:  CALL    FLUSH           ;Flush buffer of data
        LXI     D,TFCB
        MVI     C,16
        CALL    BDOS            ;Close file
        LXI     D,EOFMSG
        MVI     C,9
        CALL    BDOS            ;Print EOF message
        JMP     BOOT            ;Reboot
RCVBYT: IN      SIOSTA          ;Receive byte from serial port
        ANI     1FLAG
        JZ      RCVBYT
        IN      SIODAT
        RET
XMTBYT: IN      SIOSTA          ;Transmit byte to serial port
        ANI     0FLAG
        JZ      XMTBYT
        MOV     A,E
        OUT     SIODAT
        RET
;
FNMER:  DB      'File name missing',0DH,0AH,'$'
DDFER:  DB      'Disk or directory full',0DH,0AH,'$'
EOFMSG: DB      'Transfer complete',0DH,0AH,07H,'$'
EOTMSG: DB      'Transfer terminated',0DH,0AH,07H,'$'
RECMSG: DB      'Record #'
RECCNT: DB      '    1'         ;Record # received
        DB      ' received$'
AGAIN:  DB      ' again$'       ;Repeated record
CRLF:   DB      0DH,0AH,'$'     ;CRLF sequence
DATPTR: DW      DATBUF          ;Pointer to next storage location in buffer
RPTCTR: DB      RETRY           ;Counter for repeated record
DATBUF  EQU     $               ;Data buffer
;
        END
```

New Products

Continued from Page 2

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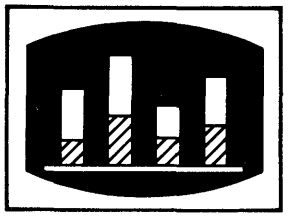

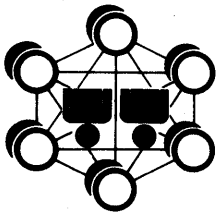

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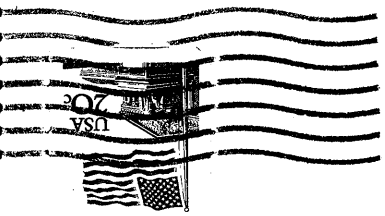

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