

COMMON UNIVERSAL CLOCK MODULE TEST

Consists of:

Program Description
Test Program Paper Tape
Program Listing
R07 Patch Information
R08 Patch Information
R09 Patch Information

B06-133M95R06A15
06-133M17R05
06-133M96R05A13
Sheets i/ii
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R07 PATCH INFORMATION
FOR TEST PROGRAM 06-133

To make "Break" work properly on the Series Sixteen, the program can be patched as follows:

<u>Location</u>	<u>Old Hex</u>	<u>New Hex</u>	
1302	C130	4300	B PATCH
1304	0020	2128	
2128	-	C810	PATCH LHI R1,X'7FFF'
212A	-	7FFF	
212C	-	2711	SIS R1,1
212E	-	2031	BNZS *-2
2130	-	9D01	SSR R0,R1
2132	-	C310	THI R1,X'20'
2134	-	0020	
2136	-	4300	B
2138	-	1306	

Note: This patch to be incorporated in object labeled
06-133 R05.1 on Multimedia Packages.

R08 PATCH INFORMATION
FOR TEST PROGRAM 06-133

To set up the Power Fail Save Area Pointer and the Data Format Fault (Boundary Error) new PSW. Patches are mandatory on Series 3200 and are as follows:

<u>Location</u>	<u>Old</u>	<u>New</u>		
12AE	00A9	00A1		
1412	4030	4300		B PATCH
1414	004E	21E0		
1418	1EE8	2208		
1446	1EE0	2200		
169E	B9AB	B1A3		
16A4	A9AB	A1A3		
16AA	F879	EE71		
16B0	F069	F061		
16B4	003B	0033		
21E0	XXXX	4030	PATCH	STH R3,X'4E'
21E2		004E		
21E4		C830		LHI R3,FORFAULT
21E6		21F0		
21E8		4030		STH R3,X'CE'
21EA		00CE		
21EC		4300		B X'1416'
21EE		1416		
21F0		C820	FORFAULT	LHI R2,C'F7'
21F2		4637		
21F4		4300		B RP+4
21F6	XXXX	15E8		

Note: This patch to be incorporated in object labeled 06-133 R05.2 Multimedia Packages.

R09 PATCH INFORMATION
FOR TEST PROGRAM 06-133

To disarm interrupts after each subtest.

<u>LOCATION</u>	<u>OLD HEX</u>	<u>NEW HEX</u>		
0E28	4810	4300		B PATCH 3
0E2A	0A24	10F4		
10F4	D000	4840	PATCH 3	LH PIC,PREC
10F6	1EE8	188A		
10F8	0830	4850		LH LFC,LINE
10FA	C810	188C		
10FC	0010	DE40		OC PIC,DISARM
10FE	0B13	1EAF		
1100	211C	DE50		OC LFC,DISARM
1102	CD51	1EAF		
1104	0000	4810		LH R1,PSW2
1106	C840	0A24		
1108	0030	4300		B X'0E2C'
110A	9151	0E2C		

Note: This patch to be incorporated in object labeled 06-133 R05.3 on Multimedia Packages.

COMMON UNIVERSAL CLOCK MODULE
TEST PROGRAM DESCRIPTION

COMMON UNIVERSAL CLOCK MODULE TEST

Related Documents

The following documents are related to this test:

Test Program Listing	06-133M96R05A13
Test Program Paper Tape	06-133M17R05
M48-000 Universal Clock Instruction Manual	29-265R07

Consisting of:

Installation Spec.	02-240A20
Maintenance Spec.	02-240A21
Programming Spec.	02-240D08
Schematic	

Test programs to be run prior to loading this test .

For 16-Bit Processors:

Memory Test	06-003
Processor Test	06-106 or
Model 50 Processor Test	06-128 or
5/16 Processor Test Part 1	06-215
5/16 Processor Test Part 2	06-216
8/16 Processor Test Part 1	06-209
8/16 Processor Test Part 2	06-210
8/16E Processor Test Part 1	06-211
8/16E Processor Test Part 2	06-212

For 32-Bit Processors:

Series 32-Processor Test Part 1	06-154
Series 32-Processor Test Part 2	06-155
Series 32-Processor Test Part 3	06-178
Series 32 Memory Test	06-156

Other Test Programs:

Teletype Basic Confidence Test	06-004
Common CRT Test	06-146
Common Current Loop Interface Test	06-184
Common Carousel 300 Test	06-183
Series 32-Processor Test Part 4	06-195
Model 1100 CRT Test Program	06-217

PURPOSE OF TEST

The Common Universal Clock Module Test verifies the operation of the M48-000 Universal Clock Module and assists maintenance personnel in testing and troubleshooting.

Test Sequence

1. Test 0

This test verifies that interrupts do not occur while disabled or disarmed.

2. Test 1

This test verifies that each bit in the interval counter can be properly loaded.

3. Test 2

This test verifies that the Precision Interval Clock (PIC) may generate an interrupt for each programmable resolution.

4. Test 3

This test verifies that the Overflow status bit can be set and reset.

5. Test 4

This test verifies that the Line Frequency Clock (LFC) can generate an interrupt.

6. Test 5

This test verifies that a zero write to the Resolution and Initial Count register (RIC), followed by a 'START' command, stops the clock.

7. Test 6

This test uses the Precision Interval Clock (PIC) to measure the time between Line Frequency Clock (LFC) interrupts.

8. Test 7

This test verifies that the Resolution and Initial Count register (RIC) may be modified during a clock interval (i.e., while the clock is running).

MINIMUM HARDWARE

The following is a list of the minimal hardware required to perform this test.

1. Processor - Model 7/16 Basic or equivalent, or Model 7/32 or equivalent
2. Minimum Memory - 16K Bytes.
3. Console Input Device See Appendix 1. Teletype or CRT on PASLA.
4. List Device See Appendix 1. Teletype, CRT on PASLA, or Line Printer.
5. Paper Tape Reader. Teletype or High Speed Paper Tape Reader.
6. Universal Clock Module (M48-000).

REQUIREMENTS OF MACHINE UNDER TEST

This program assumes that the programs listed in the 'Test Programs' section have been run without the detection of an error.

Device Addresses

The Universal Clock Module should be strapped for device addresses X'6C' and X'6D'. If the addresses are different, enter the DEVADR option. Refer to Appendices 2 and 3.

Hardware Changes

Hardware changes are not required to run this test.

LOADING PROCEDURE

Test Tape Format

Absolute, non-zoned object tape (M17) with front-end boot loader. The test program occupies memory from X'A00' through X'1E6F'.

Normal Loading Procedure

Manually enter the following X'50' Sequence into memory:

	<u>LOCATION</u>	<u>CONTENTS</u>
	X'30'	X'0000'
	X'32'	X'0000'
	X'34'	X'0000'
	X'36'	X'0050'
	X'50'	X'D500'
	X'52'	X'00CF'
	X'54'	X'4300'
	X'56'	X'0080'
For TTY	X'78'	X'0294'
For HSPTR	X'78'	X'0399'
For HSPTR/P	X'78'	X'1399'
For Micro I/O Bus	X'78'	X'C082'

Place the program tape in the Paper Tape Reader.

Execute at address X'30'.

When the Processor halts, observe the CHECKSUM byte displayed on the Console Display Register D1. If it is zero, loading is complete; otherwise, repeat the loading procedure.

Multi-Media Loading Procedure

To load this program from the INTERDATA Multi-Media Diagnostic System, refer to Program Number 06-176M95A15.

Program Execution

Refer to Appendix 1 and set up the addresses for the console input device and the list device.

Address memory location X'A00' in the case of a 32-Bit Processor.
Address memory location X'A04' in the case of a 16-Bit Processor.

Start program execution. The following title is output to the list device:

COMMON UNIVERSAL CLOCK MODULE TEST 06-133R05

OPERATING PROCEDURES

Normal Testing

When the title is printed, enter the appropriate HZ option. See Appendix 3.

Enter the 'RUN' command. All default tests are executed and control returned to the user. See Appendices 4 and 5 for explanation of print-out; see the listing for a description of each test.

Optional Testing

Certain test options may be modified for further testing. See Appendix 3 for available options.

Error Procedures

Recoverable Errors

When a recoverable error is detected, an error message, if possible, is printed, and testing proceeds according to the options selected. See Appendix 5 for error messages printed.

Irrecoverable Errors

If the Machine Malfunction Interrupt is taken, the Processor is halted. When the RUN (EXECUTE) switch is depressed, the following message is displayed:

```
ERROR TTF2  
PSW PPPP LOC LLLL
```

where: TT is the number of the test in which the error was detected.

F2 is the code for the Machine Malfunction.

PPPP is the most significant 16 bits of the PSW status, which is the old PSW, when the error was detected.

LLLL is the least significant 16 bits of the PSW status, which is the old LOC, when the error was detected.

Control is returned to the Command Processor and the program waits for console input.

For Irrecoverable Errors other than Machine Malfunction Interrupt, the following message is immediately printed and control is returned to the Command Processor:

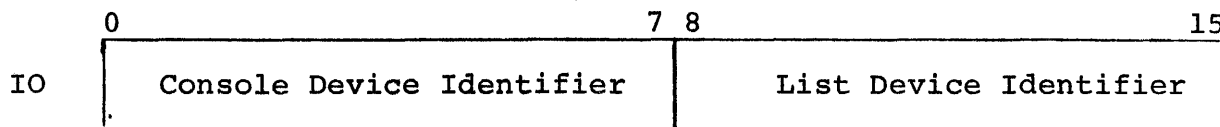
```
ERROR TTFN  
PSW PPPP LOC LLLL
```

Where: N is the code for the Irrecoverable Error detected and other printout is previously described. See Appendix 5.

APPENDIX 1

USER DEVICE DEFINITION

- The halfword labeled 'IO' (see Program Listing) has the default value for teletype, CRT, or Carousel 15/30 (all on Current Loop Interface) as the input/output console device. If the set-up is different, 'IO' must be changed:



Console Device Identifier

Meaning

X'01'	GDT/CRT on PASLA/PALM Interface, strapped for FDX operation at the highest baud rate.
X'02'	TTY/GDT/CRT/Carousel 15/30/35 on TTY/Current Loop Interface.
X'03'	Reserved. Interpreted as X'02'.
X'04'	Carousel 300 on PASLA/PALM Interface, FDX, highest baud rate.
X'05'	Micro I/O Bus Interface.
X'06'-X'FF'	Reserved. Interpreted as X'02'.

List Device Identifier

Meaning

X'01'	As above.
X'02'	As above.
X'03'	Line Printer (Data Printer or Centronics on Line Printer Interface).
X'04'	As above.
X'05'	As above.
X'06-X'FF'	As above.

APPENDIX 1 (Continued)

2. The GDT (Graphic Display Terminal) or CRT, if used on PASLA/PALM Interface, should be strapped for device addresses X'10' and X'11' for Receive and Transmit sides, respectively. If the addresses are different, then the halfword labeled 'PASADR' must be changed accordingly. See the Program Listing.
3. The teletype or current loop interface, if used, should be strapped for device address X'02'. If the address is different, the halfword labeled 'CLIFADR' must be changed. See the Program Listing.
4. The line printer, if used, should be strapped for device address X'62'. If the address is different, the halfword labeled 'LPADR' must be changed. See the Program Listing.
5. The Carousel 300, if used on PASLA/PALM Interface, should be strapped for device address X'10' and X'11' for Receive and Transmit sides, respectively. If the addresses are different, the halfword labeled 'C300ADR' must be changed accordingly. See the Program Listing.
6. The Micro I/O Bus is used should be strapped for device address X'C0'. If the address is different, the halfword labeled MICROBUS must accordingly be changed. See the Program Listing.

APPENDIX 2

OPTION/COMMAND INPUT STRUCTURE

An asterisk (*) is output to the list device to indicate that the program is awaiting an option input. Any option may be typed in from the Console Input Device, followed by a space and the desired hexadecimal value; an exception is the TEST option which accepts arguments separated by commas. A Carriage Return (CR) is issued to terminate every option/command input. An invalid option/command or value causes a (?) followed by a Carriage Return (CR), Line Feed (LF), and an Asterisk (*) to occur.

The left arrow (←) can be typed to delete the previous character; or a string of characters can be deleted by typing a left arrow (←) for each character to be deleted.

APPENDIX 3
OPTIONS TABLE

OPTION	DEFAULT VALUE	DESCRIPTION
TEST	0,1,2,3,4,5,6,7	Selects the test or tests to be executed.
DEVADR	006C	Specifies the physical device address of the Precision Interval Clock. This address must be <u>even</u> . The Line Frequency Clock is assumed to be at the next higher address (e.g., 6D).
INTLEV	0	Specifies Interrupt Priority Level of the Universal Clock Module in the case of Model 8/32. Value can be 0,1,2 or 3.
NOMSG	0	Determines whether or not all messages are printed or only error messages are printed. 0 = All Messages 1 = Error Messages Only
CONTIN	0	Enables the user to run all tests selected continuously, until the Break Key returns the program to the Command Mode. 0 = Normal Execution 1 = Continuous Execution
LOOP	0	Determines the number of times each test is to be executed before the next test is executed. Value ranges from 0 to X'7FFF'.

APPENDIX 3 (Continued)

OPTIONS TABLE

OPTION	DEFAULT VALUE	DESCRIPTION																																	
TIMVAL	D2	<p>Controls the length of software time-outs used in program. If this value is increased, the time-out is increased. The TIMVAL operand should be selected in accordance with the following table:</p> <table border="1" data-bbox="773 831 1511 1178"> <thead> <tr> <th></th> <th data-bbox="1360 831 1419 858">60H</th> <th data-bbox="1471 831 1511 858">50</th> </tr> </thead> <tbody> <tr> <td data-bbox="773 873 919 900">5/16 MOS</td> <td data-bbox="1360 873 1401 900">C4</td> <td data-bbox="1471 873 1511 900">E8</td> </tr> <tr> <td data-bbox="773 905 919 932">6/16 MOS</td> <td data-bbox="1360 905 1419 932">14A</td> <td data-bbox="1471 905 1511 932">190</td> </tr> <tr> <td data-bbox="773 936 1252 963">6/16, 8/16, 8/16E 750 nsec</td> <td data-bbox="1360 936 1419 963">14D</td> <td data-bbox="1471 936 1511 963">195</td> </tr> <tr> <td data-bbox="773 968 1273 995">6/16, 8/16, 8/16E 1000 nsec</td> <td data-bbox="1360 968 1419 995">134</td> <td data-bbox="1471 968 1511 995">180</td> </tr> <tr> <td data-bbox="773 999 956 1026">7/16 Basic</td> <td data-bbox="1360 999 1401 1026">D2</td> <td data-bbox="1471 999 1511 1026">100</td> </tr> <tr> <td data-bbox="773 1031 1122 1058">7/16 HSALU 750 nsec</td> <td data-bbox="1360 1031 1419 1058">14D</td> <td data-bbox="1471 1031 1511 1058">195</td> </tr> <tr> <td data-bbox="773 1062 1143 1089">7/16 HSALU 1000 nsec</td> <td data-bbox="1360 1062 1419 1089">134</td> <td data-bbox="1471 1062 1511 1089">180</td> </tr> <tr> <td data-bbox="773 1094 1013 1121">7/32 750 nsec</td> <td data-bbox="1360 1094 1401 1121">EB</td> <td data-bbox="1471 1094 1511 1121">124</td> </tr> <tr> <td data-bbox="773 1125 1029 1152">7/32 1000 nsec</td> <td data-bbox="1360 1125 1401 1152">D2</td> <td data-bbox="1471 1125 1511 1152">100</td> </tr> <tr> <td data-bbox="773 1157 1050 1184">8/32 3220, 3240</td> <td data-bbox="1360 1157 1419 1184">190</td> <td data-bbox="1471 1157 1511 1184">1E0</td> </tr> </tbody> </table>		60H	50	5/16 MOS	C4	E8	6/16 MOS	14A	190	6/16, 8/16, 8/16E 750 nsec	14D	195	6/16, 8/16, 8/16E 1000 nsec	134	180	7/16 Basic	D2	100	7/16 HSALU 750 nsec	14D	195	7/16 HSALU 1000 nsec	134	180	7/32 750 nsec	EB	124	7/32 1000 nsec	D2	100	8/32 3220, 3240	190	1E0
	60H	50																																	
5/16 MOS	C4	E8																																	
6/16 MOS	14A	190																																	
6/16, 8/16, 8/16E 750 nsec	14D	195																																	
6/16, 8/16, 8/16E 1000 nsec	134	180																																	
7/16 Basic	D2	100																																	
7/16 HSALU 750 nsec	14D	195																																	
7/16 HSALU 1000 nsec	134	180																																	
7/32 750 nsec	EB	124																																	
7/32 1000 nsec	D2	100																																	
8/32 3220, 3240	190	1E0																																	
HZ	60	<p>Specifies frequency of AC line (50 or 60 Hertz)</p>																																	

APPENDIX 4

NORMAL PRINTOUT

COMMON UNIVERSAL CLOCK MODULE TEST 06-133R05

*OPTION

TEST 0,1,2,3,4,5,6,7

LOOP 0000

CONTIN 0000

NOMSG 0000

DEVADR 006C

INTLEV 0000

TIMVAL 00D2

HZ 0060

*RUN

TEST 00

NO ERROR

TEST 01

NO ERROR

TEST 02

NO ERROR

TEST 03

NO ERROR

TEST 04

NO ERROR

TEST 05

NO ERROR

TEST 06

NO ERROR

TEST 07

NO ERROR

END OF TEST

*

APPENDIX 5 - ERROR TABLE

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A5-1

TEST NO.	ERROR CONDITION	EXPLANATION	SUGGESTED ACTION
ANY	ERROR TT01 DEV DDD STA SS	An interrupt occurred while the device was disabled or disarmed.	
ANY	ERROR TT02 INIT COUNT XXXX PRES COUNT YYYY	Precision Clock (PIC) did not decrement after 'START' command issued and software delay executed.	
ANY	ERROR TT03 BITS SET X	The PIC did not interrupt when expected. The Resolution Bits set are displayed as a hexadecimal digit (0,1,2,...E, or F).	
ANY	ERROR TT04 DEV DDD EXP DDD	The PIC Interrupted but the Line Frequency Clock (LFC) address was returned.	
ANY	ERROR TT05 STA SS	The PIC overflow status bit was not set on Interval Time-out following a single write data to the Resolution and Initial Count (RIC) Register.	

NOTE 1. TT = TEST NUMBER, 00-07

APPENDIX 5 - ERROR TABLE (Cont.)

TEST NO.	ERROR CONDITION	EXPLANATION	SUGGESTED ACTION
ANY	ERROR TT06	The LFC did not generate an interrupt (software time-out).	
ANY	ERROR TT07 DEV DDD EXP DDD	The LFC generated an interrupt but the PIC address was returned.	
ANY	ERROR TT08 PRES COUNT XXXX	The PIC did not decrement within the time-out period.	Increase 'TIMVAL' option to determine if PIC is capable of decrementing.
06	ERROR 0609 PRES COUNT XXXX	The PIC should have interrupted before the 51st LFC interrupt but did not.	
06	ERROR 060A PRES COUNT XXXX	After the 52nd LFC interrupt, the PIC Current Interval Count (CIC) was not within 1% of the expected value.	1. Check frequency of 1-MHZ oscillator. 2. Check frequency of AC line.
ANY	ERROR TT0B LOADED XXXX READ YYYY	The Resolution and Initial Count (RIC) Register was loaded, but was not read properly.	

A5-2

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APPENDIX 5 - ERROR TABLE (Cont.)

TEST NO.	ERROR CONDITION	EXPLANATION	SUGGESTED ACTION
ANY	ERROR TTOC PRES COUNT XXXX	The PIC was not stopped by writing two bytes to the RIC with all resolution bits zero, then issuing a command 'START'.	
ANY	ERROR TTOD LOADED XXXX READ YYYY	The RIC Register was not successfully loaded by write instructions during a PIC clock interval.	
ANY	ERROR TTOE STA SS	The PIC Overflow status bit was not reset by a Sense Status instruction.	

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APPENDIX 5 (Continued)

IRRECOVERABLE ERRORS COMMON TO ALL TESTS

ERROR NO.	TYPE OF FAILURE
TTF1	Arithmetic Fault Interrupt
TTF2	Illegal Instruction Interrupt
TT3	Machine Malfunction Interrupt (See Note 2)
TTF4	Unsolicited Immediate Interrupt
TTF5	Memory Access Controller/HW Floating Point Interrupt
TTF6	Interrupt into wrong register set

NOTE 1. TT = Test Number from 00 to 07.

NOTE 2. The PSW resulting from the Machine Malfunction Interrupt is displayed. The last 4 bits of the PSW status define the type of failure, as described below:

X100 Parity Error on Data Fetch

0010 Parity Error on Instruction Fetch

X001 Power Fail

0000 Power Restore

1X0X Parity Error or Power Fail during an Auto Driver Channel Operation (32-bit Processors only).

PROG= CUCMT

ASSEMBLED BY CAL 03-066R05-00 (32-BIT)

1	**0613305	UCM00010
2	CUCMT PROG COMMON UNIVERSAL CLOCK MODULE TEST 06-133R05M96A13	UCM00020
3	SCRAT	UCM00030
4	CROSS	UCM00040
5	WIDTH 120	UCM00050
6	TARGT 16	UCM00060
7	*	UCM00070
8	*COPYRIGHT INTERDATA, INC. APRIL 1977	UCM00080
9	*	UCM00090
10	* COMMON UNIVERSAL CLOCK MODULE TEST 06-133R05	UCM00100
11	*	UCM00110
12	* PROGRAM USES THE COMMON INSTRUCTION SET	UCM00120
13	*	UCM00130
14	* THIS PROGRAM TESTS THE M48-000 UNIVERSAL CLOCK MODULE.	UCM00140
15	* TESTS 0 AND 4 ARE ALSO APPLICABLE TO THE M48-012 AC LINE CLOCK MODULE.	UCM00150
16	* THE PROGRAM CONSISTS OF EIGHT TESTS, NONE OF WHICH REQUIRE	UCM00160
17	* MANUAL INTERVENTION.	UCM00170
18	*	UCM00180
19	* THERE ARE SIX OPTIONS AVAILABLE TO THE USER AND FOURTEEN ERROR	UCM00190
20	* MESSAGES TO ENABLE ISOLATION OF A MALFUNCTION AT THE HARDWARE	UCM00200
21	* LEVEL.	UCM00210
22	*	UCM00220
23	* THE PROGRAM REQUIRES EITHER 7/16 BASIC OR EQUIVALENT PROCESSOR.	UCM00230
24	* OR 7/32 OR EQUIVALENT PROCESSOR, WITH 16K BYTES OF MEMORY. OPTIONS	UCM00240
25	* AND RUN COMMAND ARE TO BE ENTERED VIA A CONSOLE DEVICE. A SINGLE	UCM00250
26	* CLOCK MODULE MAY BE TESTED AT A TIME.	UCM00260
27	*	UCM00270
28	* TEST 0	UCM00280
29	* VERIFIES THAT INTERRUPTS DO NOT OCCUR WHILE DISABLED OR DISARMED.	UCM00290
30	*	UCM00300
31	* TEST 1	UCM00310
32	* VERIFIES THAT EACH BIT IN THE INTERVAL COUNTER CAN BE LOADED	UCM00320
33	* PROPERLY.	UCM00330
34	*	UCM00340
35	* TEST 2	UCM00350
36	* VERIFIES THAT AN INTERRUPT MAY BE GENERATED BY THE PRECISION	UCM00360
37	* INTERVAL CLOCK (PIC) FOR EACH PROGRAMMABLE RESOLUTION.	UCM00370
38	*	UCM00380
39	* TEST 3	UCM00390
40	* VERIFIES THAT THE PIC OVERFLOW STATUS BIT CAN BE SET AND RESET.	UCM00400
41	*	UCM00410
42	* TEST 4	UCM00420
43	* VERIFIES THAT THE LINE FREQUENCY CLOCK (LFC) CAN GENERATE AN	UCM00430
44	* INTERRUPT.	UCM00440
45	*	UCM00450
46	* TEST 5	UCM00460
47	* VERIFIES THAT A ZERO WRITE TO THE PIC RESOLUTION AND INITIAL COUNT	UCM00470
48	* REGISTER (RIC), FOLLOWED BY A 'START' COMMAND, WILL INDEED STOP THE	UCM00480
49	* CLOCK.	UCM00490
50	*	UCM00500
51	* TEST 6	UCM00510
52	* THIS TEST USES THE PRECISION INTERVAL CLOCK (PIC) TO MEASURE THE	UCM00520
53	* TIME BETWEEN LINE FREQUENCY CLOCK (LFC) INTERRUPTS.	UCM00530

54 *
55 * TEST 7
56 * THIS TFST VERIFIES THAT THE PIC RESOLUTION AND INITIAL COUNT REGISTER
57 * (RIC) MAY BE LOADED DURING A CLOCK INTERVAL (I.E., WHILE THE PIC IS
58 * RUNNING).
59 *
60 * ANY COMBINATION OF THE TESTS MAY BE SELECTED AS A STRING AND CAN BE
61 * LOOPED OR RUN CONTINUOUSLY.
62 *

UCM00540
UCM00550
UCM00560
UCM00570
UCM00580
UCM00590
UCM00600
UCM00610
UCM00620

		64	**ETPE			UCM00640
		65	*			UCM00650
		66	*			UCM00660
	0000	0000	67	R0	EQU 0	UCM00670
	0000	0001	68	R1	EQU 1	UCM00680
	0000	0002	69	R2	EQU 2	UCM00690
	0000	0003	70	R3	EQU 3	UCM00700
	0000	0004	71	R4	EQU 4	UCM00710
	0000	0005	72	R5	EQU 5	UCM00720
	0000	0006	73	R6	EQU 6	UCM00730
	0000	0007	74	R7	EQU 7	UCM00740
	0000	0008	75	R8	EQU 8	UCM00750
	0000	0009	76	R9	EQU 9	UCM00760
	0000	000A	77	R10	EQU 10	UCM00770
	0000	000B	78	R11	EQU 11	UCM00780
	0000	000C	79	R12	EQU 12	UCM00790
	0000	000D	80	R13	EQU 13	UCM00800
	0000	000E	81	R14	EQU 14	UCM00810
	0000	000E	82	RET	EQU 14	UCM00820
	0000	000F	83	R15	EQU 15	UCM00830
	0000	000F	84	LINK	EQU 15	UCM00840
		85	*			UCM00850
		86	* BOOTLOADER WITH CHKSUM			UCM00860
		87	*			UCM00870
	0000R		88	ORG	X'80'	UCM00880
	0080	2421	89	LIS	R2,1	UCM00890
	0082	2303	90	BS	BOOT	UCM00900
	0084	1EE0	91	DC	Z(PSWSAVE)	CURRENT PSW SAVE POINTER(32-BIT M/C)
	0086	1EE8	92	DC	Z(RSAVE)	REGISTER SAVE POINTER(32-BIT M/C)
	0088	C810 0A00	93	BOOT	LHI R1,ORIGIN1	R1 = ADR(FIRST BYTE OF TEST PROG)
	008C	C830 1ED1	94		LHI R3,LNZB+1	R3 = ADR(LAST NON-ZERO BYTE)
	0090	4030 0022	95		STH R3,X'22'	REGISTER SAVE POINTERS(16BIT M/C)
	0094	2731	96		SIS R3,1	UCM00950
	0096	C860 0000	97	MN	LHI R6,0	R6 = CHKSUM BYTE = X'MN'
	009A	D340 0078	98		LB R4,X'78'	INPUT DEV ADR
	009E	DE40 0079	99		OC R4,X'79'	UCM00980
	00A2	9D45	100	LEADER	SSR R4,R5	UCM00990
	00A4	2091	101		BTBS 9,1	DU,BSY
	00A6	9845	102		RDR R4,R5	UCM01000
	00A8	0855	103		LDAR R5,R5	UCM01010
	00AA	2234	104		BZS LEADER	UCM01020
	00AC	D251 0000	105	LOAD	STB R5,0(R1)	IGNORE LEADER
	00B0	D351 0000	106		LB R5,0(R1)	STORE 1ST NON-ZERO & SUBSEQUENT BYTE
	00B4	0765	107		XAR R6,R5	RELOAD DATA BYTE TO
	00B6	9481	108		EXBR R8,R1	GENERATE CHKSUM
	00B8	9828	109		WHR R2,R8	UCM01070
	00BA	9D45	110		SSR R4,R5	DISPLAY MEMORY ADDRESS
	00BC	2091	111		BTBS 9,1	UCM01080
	00BE	9845	112		RDR R4,R5	UCM01090
	00C0	C110 00AC	113		BXLE R1,LOAD	DU,BSY
	00C4	9486	114		EXBR R8,R6	UCM01100
	00C6	9828	115		WHR R2,R8	LOAD TILL LAST BYTE
	00C8	2478	116	LOWT	LIS R7,8	FINAL CHKSUM
	00CA	917C	117		SLLS R7,12	UCM01140
	00CC	9557	118		EPSR R5,R7	R7 = X'8000'
						HALT PROCESSOR.
						UCM01150
						UCM01160
						UCM01170
						UCM01180

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BS LDWT

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00CE 2203

UCM01190

EXEC - ETPE R03P2

0000		121	ORG	X'A00'		UCM01210
0A00	4300 0A30	122	ORIGIN1	B START1	START HERE FOR 32-BIT PROCESSOR	UCM01220
	0000 0A04	123	ORIGIN2	EQU *		UCM01230
0A04		124	IFZ	ADC-2		UCM01240
0A04	4300 0A46	125		B START2	START HERE FOR 16-BIT PROCESSOR	UCM01250
0A08	4300 0A5E	126	ORIGIN3	B START3	SPECIAL 32-BIT PROCESSOR START	UCM01260
0A0C	4300 0A62	127	ORIGIN4	B START4		UCM01270
		128		ELSE		UCM01280
		129		B START3	SPECIAL START FOR 32 BIT PROCESSOR	UCM01290
		130		B START3		UCM01300
		131		B START3		UCM01310
		132		ENDC		UCM01320
		133	*			UCM01330
		134	-----			UCM01340
		135	* TEST CONSTANTS			UCM01350
		136	*			UCM01360
0A10	0202	137	IO	DC X'0202'	I/O DEVICE(S) IDENTIFIER	UCM01370
0A12	1011	138	PASLADR	DC X'1011'	PASLA/PALM READ/WRITE ADDRESSES	UCM01380
0A14	0202	139	CLIFADR	DC X'0202'	CURRENT LOOP INTERFACE R/W ADDRESSFS	UCM01390
0A16	6262	140	LPADR	DC X'6262'	LINE PRINTER ADDRFS	UCM01400
0A18	1011	141	C300ADR	DC X'1011'	CAROUSEL 300/PASLA ADDRESSES	UCM01410
0A1A	C0C0	142	MICROBUS	DC X'C0C0'	MICROBUS ADDRESS	UCM01420
0A1C	0000	143		DCX 0	PROVISION FOR SPECIAL DEVICE	UCM01430
		144	*			UCM01440
		145	* IO =	0101 FOR CRT ON PASLA		UCM01450
		146	*	0202 TELETYPE, CAROUSEL 15/30		UCM01460
		147	*	XX03 LINE PRINTER		UCM01470
		148	*	0404 CAROUSEL 300		UCM01480
		149	*	0505 MICROBUS		UCM01490
		150	*			UCM01500
0A1E	0140	151	TIME	DC X'140'	CONSTANT FOR 1 MS DELAY(X'C8'-MOD70)	UCM01510
0A20	0000	152		DCX 0	RESERVED	UCM01520
0A22	70F0	153	PSW	DCX 70F0	PSW USED IN PROGRAM	UCM01530
0A24	30F0	154	PSW2	DCX 30F0	PSW USED IN EXEC	UCM01540
0A26	0000	155		DCX 0	RESERVED	UCM01550
0A28	0000	156		DCX 0	RESERVED	UCM01560
0A2A	0000	157		DCX 0	RESERVED	UCM01570
0A2C	0000	158		DCX 0	RESERVED	UCM01580
0A2E	0000	159		DCX 0	RESERVED	UCM01590
		160	-----			UCM01600
		161	*			UCM01610
0A30	0711	162	START1	XAR R1,R1		UCM01620
0A32	4010 0030	163		STH R1,X'30'	DISABLE INT AT PROCESSOR LEVEL	UCM01630
0A36	4820 0A24	164		LH R2,PSW2		UCM01640
0A3A	4020 0032	165		STH R2,X'32'	SELECT REG SET 15	UCM01650
0A3E		166		IFZ ADC-2		UCM01660
0A3E	2521	167		LCS R2,1		UCM01670
0A40	4020 1684	168		STH R2,MOD32	SET MODEL 32 PROCESSOR FLAG	UCM01680
0A44	2306	169		BS ST		UCM01690
0A46	0711	170	START2	XAR R1,R1		UCM01700
0A48	4010 1684	171		STH R1,MOD32	RESET MOD 32 PROCESSOR FLAG	UCM01710
0A4C	4610 0A24	172		LH R1,PSW2		UCM01720
		173		ENDC		UCM01730

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0A50	C820	0A66	174	ST	LHI	R2,START		UCM01740
0A54	4010	0034	175		STH	R1,X'34'		UCM01750
0A58	4020	0036	176		STH	R2,X'36'	II INT NEW PSW LOC	UCM01760
0A5C	0000		177		DCX	0	TAKE AN ILLEGAL INSTRUCTION INT	UCM01770
			178	*				UCM01780
0A5E	4300	0A30	179	START3	B	START1	INSERT SPECIAL ROUTINE HERE	UCM01790
0A62			180		IFZ	ADC-2		UCM01800
0A62	4300	0A46	181	START4	B	START2	INSERT SPECIAL ROUTINE HERE	UCM01810
			182		ENDC			UCM01820
			183	*				UCM01830
0A66	D310	0A10	184	START	LB	R1,I0	GET I/O IDENTIFIERS	UCM01840
0A6A	D320	0A11	185		LB	R2,I0+1		UCM01850
0A6E	2436		186		LIS	R3,6	IDENTIFIER CAN BE 1,2,3,4,5	UCM01860
0A70	0513		187		CLHR	R1,R3		UCM01870
0A72	2182		188		BLS	I0,OK1	BRANCH IF KB IDENTIFIER OK	UCM01880
0A74	2412		189		LIS	R1,2	OTHERWISE FORCE IT TO BE TTY	UCM01890
0A76	0523		190	IO.OK1	CLHR	R2,R3		UCM01900
0A78	2182		191		BLS	I0,OK2	SAME TEST FOR LIST DEVICE	UCM01910
0A7A	2422		192		LIS	R2,2		UCM01920
0A7C	D210	0A10	193	IO.OK2	STB	R1,I0	REESTABLISH VALUES	UCM01930
0A80	D220	0A11	194		STB	R2,I0+1		UCM01940
0A84	D362	16B4	195		LB	R6,CONRQ2S(R2)		UCM01950
0A88	4060	1698	196		STH	R6,PASFLG2	SET PASLA FLAG (LIST DEVICE)	UCM01960
0A8C	0866		197		LDAR	R6,R6		UCM01970
0A8E	2336		198		BZS	I0,OK3	SKIP IF NOT PASLA	UCM01980
0A90	9121		199		SLHLS	R2,1		UCM01990
0A92	D302	0A11	200		LB	R0,I0+1(R2)		UCM02000
0A96	DE02	16A8	201		OC	R0,CON2ND(R2)	ISSUE 2ND COMMAND (LIST DEVICE)	UCM02010
			202	*				UCM02020
0A9A	41F0	1370	203	IO.OK3	BAL	LINK,SETKB	ESTABLISH KEYBOARD DEVICE	UCM02030
0A9E	9310		204		LBR	R1,R0	(R1) = 1,2,4,5	UCM02040
0AA0	9111		205		SLHLS	R1,1	(R1) = 2,4,6,A	UCM02050
0AA2	4831	0A10	206		LH	R3,I0(R1)		UCM02060
0AA6	4030	169A	207		STH	R3,CONADR	SET UP CONSOLE DEVICE ADDRESS	UCM02070
0AAA	4821	169C	208		LH	R2,CONRD(R1)		UCM02080
0AAE	4020	169C	209		STH	R2,CONRD	SET UP R/W COMMANDS	UCM02090
0AB2	4821	16A8	210		LH	R2,CON2ND(R1)		UCM02100
0AB6	4020	16A8	211		STH	R2,CON2ND	2ND CMD: ENABLE READ CMD	UCM02110
0ABA	9011		212		SRHLS	R1,1		UCM02120
0ABC	D341	16B4	213		LB	R4,CONRQ2S(R1)		UCM02130
0AC0	D240	16B4	214		STB	R4,CONRQ2S	CONSOLE REQUEST TO SEND	UCM02140
0AC4	4040	1696	215		STH	R4,PASFLG	SET PASLA FLAG (CONSOLE)	UCM02150
0AC8	0844		216		LDAR	R4,R4		UCM02160
0ACA	2333		217		BFFS	3,3	SKIP IF NOT PASLA	UCM02170
0ACC	9422		218		EXBR	R2,R2		UCM02180
0ACE	9E32		219		OCR	R3,R2	ISSUE 2ND COMMAND (CONSOLE)	UCM02190
			220	*				UCM02200
0AD0	41F0	13CC	221		BAL	LINK,LCORE	SET UP LOW CORE	UCM02210
0AD4	2400		222		LIS	R0,0		UCM02220
0AD6	4000	16C4	223		STH	R0,WASDU	RESET 'DEVICE UNAVAILABLE' FLAG	UCM02230
0ADA	41F0	1214	224		BAL	LINK,CRLF		UCM02240
0ADE	C850	1806	225		LHI	R5,TITLE		UCM02250
0AE2	41F0	1190	226		BAL	R15,PRINT	PRINT TEST PROGRAM TITLE	UCM02260

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		227	*-----*			UCH02270
		228	* KEYBOARD INPUT ROUTINE			UCH02280
		229	*			UCH02290
		230	OPTIN EQU *			UCH02300
0AE6	0000 0AE6	231	BAL LINK,CRLF	CR,LF TO LIST DEVICE		UCH02310
	0000 0AEA	232	OPTIN1 EQU *			UCH02320
0AEA	4820 0A24	233	LH R2,PSW2			UCH02330
0AEE	9512	234	EPSR R1,R2	NO INT. REG SET 15		UCH02340
0AF0	41F0 1370	235	BAL LINK,SETKB	ESTABLISH CONSOLE		UCH02350
0AF4	0340 1774	236	LB R4,AMSG	OUTPUT AN * TO INDICATE		UCH02360
0AF8	41F0 1222	237	BAL LINK,OUTCHR	COMMAND MODE ESTABLISHED		UCH02370
0AFC	2541	238	LCS R4,1	X'FF'		UCH02380
0AFE	41F0 1222	239	BAL LINK,OUTCHR			UCH02390
0B02	C8C0 12C4	240	LHI R12,QUESTN	SET UP R12 FOR ERR ROUTINE		UCH02400
0B06	C800 2020	241	LHI R0,X'2020'	BLANK OUT COMMAND BUFFER		UCH02410
0B0A	4000 1ED0	242	STH R0,OPTBUF	WHICH WILL CONTAIN OPTION		UCH02420
0B0E	4000 1ED2	243	STH R0,OPTBUF+2	NAME		UCH02430
0B12	4000 1ED4	244	STH R0,OPTBUF+4			UCH02440
0B16	0711	245	XAR R1,R1	CLEAR OPTBUF INDEX		UCH02450
0B18	41F0 1290	246	RDCHR BAL R15,GETCHR	GET A CHAR IN R4		UCH02460
0B1C	C540 0060	247	CLHI R4,X'60'	UPPER CASE ALPHA ?		UCH02470
0B20	2183	248	BLS RDCHAR0	BRANCH IF NO.		UCH02480
0B22	C840 0020	249	SHI R4,X'20'	CONVERT TO LOWER CASE		UCH02490
0B26	C540 0023	250	RDCHAR0 CLHI R4,X'23'	IS IT # ?		UCH02500
0B2A	4330 0AE6	251	BE OPTIN			UCH02510
0B2E	C540 005F	252	CLHI R4,X'5F'	LEFT ARROW, UNDERLINE OR DELETE ?		UCH02520
0B32	2139	253	BNES RDCHR1			UCH02530
0B34	2711	254	SIS R1,1	YES, DECREMENT INDEX		UCH02540
0B36	021C	255	BMR R12	BUFFER UNDERFLOW; PRINT '?'		UCH02550
0B38	C800 0020	256	LHI R0,X'20'			UCH02560
0B3C	0201 1ED0	257	STB R0,OPTBUF(R1)			UCH02570
0B40	4300 0B18	258	B RDCHR			UCH02580
0B44	C540 0000	259	RDCHR1 CLHI R4,X'00'	IS IT CR ?		UCH02590
0B48	233C	260	BES LOOKUP	YES, TRY MATCH		UCH02600
0B4A	C540 0020	261	CLHI R4,X'20'	IS IT A BLANK?		UCH02610
0B4E	2339	262	BES LOOKUP	YES, TRY MATCH		UCH02620
0B50	C510 0006	263	CLHI R1,6	7 CHARACTERS INPUT ?		UCH02630
0B54	038C	264	BNLR R12	IF YES, ERROR		UCH02640
0B56	0241 1ED0	265	STB R4,OPTBUF(R1)	STORE CURRENT BYTE		UCH02650
0B5A	2611	266	AIS R1,1	BUMP BUFFER INDEX		UCH02660
0B5C	4300 0B18	267	B RDCHR	READ NEXT CHARACTER		UCH02670
		268	*-----*			UCH02680
		269	* OPTION MATCH ROUTINE			UCH02690
		270	*			UCH02700
0B60	C810 1776	271	LOOKUP LHI R1,OPT	LOAD ADDRESS OF OPTION TABLE		UCH02710
0B64	0733	272	LOOK1 XAR R3,R3	CLEAR BUFFER INDEX		UCH02720
0B66	0861	273	LDAR R6,R1	SET OPTION WORD INDEX		UCH02730
0B68	4856 0000	274	LOOK2 LH R5,0(R6)			UCH02740
0B6C	021C	275	BMR R12	IF MINUS, THEN NO MATCH = ERROR		UCH02750
0B6E	4553 1ED0	276	CLH R5,OPTBUF(R3)	COMPARE TO OPTBUF HW		UCH02760
0B72	2333	277	BES LOOK3			UCH02770
0B74	261C	278	AIS R1,12			UCH02780
0B76	2209	279	BS LOOK1			UCH02790

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0B78	2632	280	LOOK3	AIS	R3,2	TRY NEXT HW	UCM02800
0B7A	2662	281		AIS	R6,2		UCM02810
0B7C	C530 0006	282		CLHI	R3,6	3 HATCHING HW FOUND ?	UCM02820
0B80	208C	283		BLS	LOOK2		UCM02830
		284	*				UCM02840
0B82	C510 17E2	285		CLHI	R1,RUN	RUN COMMAND ?	UCM02850
0B86	4330 004E	286		BE	RUNIT		UCM02860
0B8A	C510 1706	287		CLHI	R1,OPTION	OPTION CMD ?	UCM02870
0B8E	4230 0C84	288		BNE	LOOK4	NO, LOOK FURTHER	UCM02880
		289					UCM02890
		290	*			* TO PROCESS INPUT COMMAND 'OPTION'	UCM02900
0B92	4420 170E	291		LH	R2,OPTION+8	CHECK FOR SPECIAL ROUTINE	UCM02910
0B96	0232	292		BNZR	R2	LINK TO ROUTINE	UCM02920
0B98	C830 1776	293	OPTRTN	LHI	R3,TEST	RETURN HERE	UCM02930
0B9C	C8E0 0C22	294		LHI	R14,OPTCMD8		UCM02940
0BA0	41F0 1214	295		BAL	LINK,CRLF		UCM02950
0BA4	0722	296	OPTCMD	XAR	R2,R2	RESET COUNTER	UCM02960
0BA6	D342 1776	297	OPTCMD1	LB	R4,OPT(R2)	TO PRINT TEST	UCM02970
0BAA	41F0 1222	298		BAL	LINK,OUTCHR		UCM02980
0BAE	2621	299		AIS	R2,1		UCM02990
0BB0	C520 0006	300		CLHI	R2,6		UCM03000
0BB4	2087	301		BLS	OPTCMD1		UCM03010
0BB6	C840 0020	302		LHI	R4,C' '		UCM03020
0BBA	41F0 1222	303		BAL	LINK,OUTCHR	OUTPUT 1 SPACE	UCM03030
0BBE	0755	304		XAR	R5,R5	TO PRINT SELECTED TEST NUMBERS	UCM03040
0BC0	4050 1682	305		STH	R5,FIRST		UCM03050
0BC4	4823 0006	306		LH	R2,6(R3)	FIRST TEST WORD	UCM03060
0BC8	2440	307	OPTCMD2	LIS	R4,0	START WITH TEST 0	UCM03070
0BCA	4040 1ED8	308		STH	R4,TEMP		UCM03080
0BCE	9121	309	OPTCMD3	SLHLS	R2,1		UCM03090
0BD0	4380 0C02	310		BNC	OPTCMD7		UCM03100
0BD4	4040 1ED8	311	OPTCMD4	STH	R4,TEMP	OPTION VALUE FOUND.	UCM03110
0BD8	4800 1682	312		LH	R0,FIRST	IS IT FIRST ?	UCM03120
0BDC	2335	313		BZS	OPTCMD5		UCM03130
0BDE	C640 002C	314		LHI	R4,C','	NO, OUTPUT COMMA	UCM03140
0BE2	41F0 1222	315		BAL	LINK,OUTCHR		UCM03150
0BE6	40F0 1682	316	OPTCMD5	STH	LINK,FIRST		UCM03160
0BEA	0855	317		LDAR	R5,R5	TEST VALUE FROM SECOND HW	UCM03170
0BEC	2335	318		BZS	OPTCMD6	NO	UCM03180
0BEE	C840 0031	319		LHI	R4,C'1'	YES,OUTPUT '1'	UCM03190
0BF2	41F0 1222	320		BAL	LINK,OUTCHR		UCM03200
0BF6	4840 1ED8	321	OPTCMD6	LH	R4,TEMP	RESTORE R4	UCM03210
0BFA	D344 160C	322		LB	R4,HEXTAB(R4)	CONVERT	UCM03220
0BFE	41F0 1222	323		BAL	LINK,OUTCHR	OUTPUT 0-F	UCM03230
0C02	4840 1ED8	324	OPTCMD7	LH	R4,TEMP	RESTORE	UCM03240
0C06	2641	325		AIS	R4,1	INCREMENT TEST #	UCM03250
0C08	4040 1ED8	326		STH	R4,TEMP		UCM03260
0C0C	C540 0010	327		CLHI	R4,16		UCM03270
0C10	4280 0BCE	328		BL	OPTCMD3		UCM03280
0C14	0855	329	OPTCMD71	LDAR	R5,R5	DONE ?	UCM03290
0C16	023E	330		BNZR	R14		UCM03300
0C18	4823 0Q08	331		LH	R2,8(R3)	SECOND TEST WORD	UCM03310
0C1C	2451	332		LIS	R5,1	R5 = 1 FOR SECOND TEST HW	UCM03320

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0C1E	4300	0BC8	333	B	OPTCMD2		UCM03330	
			334	*-----*			UCM03340	
			335	* TO OUTPUT OTHER OPTION NAMES & VALUES			UCM03350	
			336	*			UCM03360	
0C22	41F0	1214	337	OPTCMD8	BAL	LINK,CRLF	UCM03370	
0C26	2461		338	LIS	R6,1	SET LINE COUNTER	UCM03380	
0C28	C820	1782	339	LHI	R2,OPT+12	R2 POINTS TO THE NAME	UCM03390	
0C2C	2436		340	OPTCMD9	LIS	R3,6	UCM03400	
0C2E	D342	0000	341	OPTCMD10	LB	R4,0(R2)	UCM03410	
0C32	41F0	1222	342	BAL	LINK,OUTCHR	OUTPUT OPTION NAME CHAR	UCM03420	
0C36	2621		343	AIS	R2,1		UCM03430	
0C38	2731		344	SIS	R3,1	6 CHARACTERS OUTPUT ?	UCM03440	
0C3A	2026		345	BPS	OPTCMD10	NO,LOOP	UCM03450	
0C3C	C840	0020	346	LHI	R4,C' '		UCM03460	
0C40	41F0	1222	347	BAL	LINK,OUTCHR	OUTPUT ONE SPACE	UCM03470	
0C44	4852	0000	348	LH	R5,0(R2)	R5 = OPTION VALUE	UCM03480	
0C48	2404		349	LIS	R0,4		UCM03490	
0C4A	41F0	10CA	350	BAL	LINK,RSHEX	WRITE OPTION VALUE IN HEX (4 DIGITS)	UCM03500	
0C4E	D300	0A10	351	LB	R0,10		UCM03510	
0C52	2701		352	SIS	R0,1	CONSOLE = CRT ?	UCM03520	
0C54	213D		353	BNZS	OPTCMD12	BRANCH: NO.	UCM03530	
0C56	2661		354	AIS	R6,1	INCREMENT LINE COUNTER.	UCM03540	
0C58	C560	0014	355	CLHI	R6,20	PAGE FULL ?	UCM03550	
0C5C	2189		356	BLS	OPTCMD12	NO	UCM03560	
0C5E	0766		357	XAR	R6,R6	INITIALIZE LINE COUNT	UCM03570	
0C60	41F0	1290	358	OPTCMD11	BAL	LINK,GETCHR	UCM03580	
0C64	274D		359	SIS	R4,13	CR ?	UCM03590	
0C66	4330	0AEE	360	BZ	OPTIN	TO ACCEPT NEXT COMMAND	UCM03600	
0C6A	2643		361	AIS	R4,3	LF ?	UCM03610	
0C6C	2036		362	BNZS	OPTCMD11	IF YES, PRINT NEXT PAGE	UCM03620	
0C6E	41F0	1214	363	OPTCMD12	BAL	LINK,CRLF	UCM03630	
0C72	41F0	12DE	364	BAL	LINK,TSTBRK	EXIT IF 'BREAK' PRESSED.	UCM03640	
0C76	2626		365	AIS	R2,6		UCM03650	
0C78	C520	17D6	366	CLHI	R2,OPTEND2	ALL PRINTING OPTIONS DONE ?	UCM03660	
0C7C	4280	0C2C	367	BL	OPTCMD9	NO,LOOP FOR NEXT ONE	UCM03670	
0C80	4300	0AEA	368	B	OPTIN1	TO ACCEPT NEXT COMMAND	UCM03680	
			369	*-----*			UCM03690	
0C84	C510	1776	370	LOOK4	CLHI	R1,TEST	'TEST' OPTION ?	UCM03700
0C88	4330	0CFC	371	BE	TESTOP		UCM03710	
			372	* TO PROCESS COMMANDS OTHER THAN 'TEST', 'OPTION'.			UCM03720	
			373	*			UCM03730	
0C8C	274D		374	SIS	R4,13	OPT FOLLOWED BY CR ?	UCM03740	
0C8E	033C		375	BZR	R12	YES, ERROR	UCM03750	
0C90	41E0	106C	376	BAL	R14,OPTVAL	GET OPTION VALUE IN R6	UCM03760	
0C94	274D		377	SIS	R4,13	TERMINATED BY CR ?	UCM03770	
0C96	023C		378	BNZR	R12	IF NO, BRANCH	UCM03780	
0C98	48E1	0008	379	LH	R14,8(R1)	GET OPTION CHECK ROUTINE ADDRESS	UCM03790	
0C9C	2332		380	BZS	LOOK5		UCM03800	
0C9E	01FE		381	BALR	R15,R14	LINK OPTION CHECK ROUTINE	UCM03810	
	0000	0CA0	382	LOOK5	EQU	RETURN HERE	UCM03820	
0CA0	4061	0006	383	STH	R6,6(R1)	STORE OPTION VALUE	UCM03830	
0CA4	4300	0AEE	384	B	OPTIN	TO ACCEPT NEXT COMMAND	UCM03840	
			385	*			UCM03850	

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0CA8	C360	FFFE	386	ZERONE	THI	R6,X'FFFE'	IGNORE LSB	UCM03860
0CAC	033F		387		BZR	R15	OKAY	UCM03870
0CAE	030C		388		BR	R12	ERROR RETURN	UCM03880
			389	*				UCM03890
0CB0	C560	0400	390	ADR	CLHI	R6,X'400'	(R6) = 10 BIT DEVICE ADDRESS	UCM03900
0CB4	028F		391		BLR	R15	RETURN TO LOOKS	UCM03910
0CB6	030C		392		BR	R12		UCM03920
			393	*				UCM03930
0CB8	C560	000F	394	LEVEL	CLHI	R6,15	(R6) = INTERRUPT LEVEL HEX DIGIT	UCM03940
0CBC	028F		395		BLR	R15	RETURN TO LOOKS	UCM03950
0CBE	030C		396		BR	R12		UCM03960
			397	*-----*				UCM03970
			398	* TO CHECK THAT OPTION ENTRY IN R6 IS IN DECIMAL DIGITS.				UCM03980
			399	* TO CONVERT DECIMAL ENTRY IN R6 TO HEX VALUE AND				UCM03990
			400	* STORE IT @ 0(R5).				UCM04000
			401	*				UCM04010
UCC0	D000	1EE8	402	DECHEX	STM	R0,RSAVE		UCM04020
OCC4	2400		403		LIS	R0,0	ACCUMULATOR	UCM04030
OCC6	2410		404		LIS	R1,0	TABLE INDEX	UCM04040
OCC8	2420		405		LIS	R2,0	SHIFT COUNTER	UCM04050
OCCA	0836		406	DECLP1	LDAR	R3,R6	COPY INPUT VALUE	UCM04060
OCCC	CC32	0000	407		SRAL	R3,0(R2)		UCM04070
0CD0	4330	0CF2	408		BZ	DECHEX1	TO RETURN	UCM04080
0CD4	C430	000F	409		NHI	R3,15		UCM04090
0CD8	C530	000A	410		CLHI	R3,10	VALID DECIMAL DIGIT ?	UCM04100
0CDC	038C		411		BNLR	R12	IF NOT, ERROR.	UCM04110
0CDE	4871	16D2	412		LDA	R7,DECTAB(R1)	1,10,....10000	UCM04120
0CE2	2731		413	DECLP2	SIS	R3,1		UCM04130
0CE4	2113		414		BMS	DECLP3		UCM04140
0CE6	0A07		415		AAR	R0,R7	ADD IN CURRENT VALUE	UCM04150
0CE8	2203		416		BS	DECLP2		UCM04160
0CEA	2624		417	DECLP3	AIS	R2,4	INCREMENT SHIFTER	UCM04170
0CEC	2612		418		AIS	R1,ADC	INCREMENT POINTER	UCM04180
0CEE	4300	0CCA	419		B	DECLP1		UCM04190
0CF2	4005	0000	420	DECHEX1	STH	R0,0(R5)	STORE HEX OPTION VALUE	UCM04200
0CF6	D100	1EE8	421		LM	R0,RSAVE		UCM04210
0CFA	030F		422		BR	LINK	RETURN	UCM04220
			423	*-----*				UCM04230
			424	* TEST OPTION PROCESS ROUTINE				UCM04240
			425	*				UCM04250
0CFC	274D		426	TESTOP	SIS	R4,13	'TEST' FOLLOWED BY (CR) ?	UCM04260
0CFE	213B		427		BNZS	TSTOP1		UCM04270
0D00	4800	17F0	428		LH	R0,DEFTTESTS	YES, SET TEST OPTION TO	UCM04280
0D04	4000	177C	429		STH	R0,TEST+6	FIRST TEST WORD	UCM04290
0D08	4800	17F2	430		LH	R0,DEFTTESTS+2	ALL DEFAULT TESTS IN PROGRAM	UCM04300
0D0C	4000	177E	431		STH	R0,TEST+8	SECOND TEST WORD	UCM04310
0D10	4300	0AE6	432		B	OPTIN	TO ACCEPT NEXT COMMAND	UCM04320
			433	*				UCM04330
0D14	4850	17F4	434	TSTOP1	LH	R5,MAXTST		UCM04340
0D18	2470		435		LIS	R7,0	TEST BIT ACCUMULATORS	UCM04350
0D1A	2480		436		LIS	R8,0		UCM04360
0D1C	41E0	106C	437	TSTOP2	BAL	R14,OPTVAL	GET OPTION VALUE IN R6	UCM04370
0D20	0556		438		CLAR	R5,R6		UCM04380

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0D22	028C	439	BLR	R12	ERROR: INVALID TEST NUMBER	UCM04390
0D24	C560 0010	440	CLHI	R6,16	R6 < 16 ?	UCM04400
0D28	2385	441	BNLS	TSTOP3	NO	UCM04410
0D2A	41E0 10A2	442	BAL	R14,UNARY	GET UNARY OPERAND IN R3	UCM04420
0D2E	0673	443	OAR	R7,R3	SET CURRENT BIT	UCM04430
0D30	2306	444	BS	TSTOP4		UCM04440
0D32	CB60 0010	445	TSTOP3	SHI R6,16	R6 = 0-F	UCM04450
0D36	41E0 10A2	446	BAL	R14,UNARY		UCM04460
0D3A	0683	447	OAR	R8,R3	SET CURRENT BIT	UCM04470
0D3C	274D	448	TSTOP4	SIS R4,13	TERMINATED BY CR ?	UCM04480
0D3E	4230 0D1C	449	BNZ	TSTOP2		UCM04490
0D42	4070 177C	450	STH	R7,TEST+6	STORE VALID SELECTED TESTS	UCM04500
0D46	4080 177E	451	STH	R8,TEST+8		UCM04510
0D4A	4300 0AE6	452	B	OPTIN	TO ACCEPT NEXT COMMAND	UCM04520
		453	*-----*			UCM04530
		454	*			UCM04540
	0000 0D4E	455	RUNIT	EQU *		UCM04550
0D4E	41F0 1214	456	BAL	LINK,CRLF		UCM04560
0D52	4800 0A10	457	LH	R0,IO		UCM04570
0D56	4000 1ED6	458	STH	R0,IOSAVE	RESTORE USER'S I/O CHOICE	UCM04580
0D5A	41F0 1214	459	BAL	LINK,CRLF		UCM04590
0D5E	41F0 1E7E	460	BAL	LINK,INIT	LINK USER INITIALIZATION ROUTINE	UCM04600
	0000 0D62	461	INITRET	EQU *	RETURN HERE	UCM04610
0D62	07FF	462	XAR	R15,R15		UCM04620
0D64	40F0 16C6	463	STH	R15,WASDU1		UCM04630
0D68	240F	464	LIS	R0,15	TO FIND HIGHEST SELECTED TEST NO.	UCM04640
0D6A	4810 177E	465	LH	R1,TEST+8	CHECK SECOND TEST HW	UCM04650
0D6E	9011	466	KEEP1	SRLS R1,1		UCM04660
0D70	2188	467	BCS	FOUND1	R0 = F-0	UCM04670
0D72	2701	468	SIS	R0,1		UCM04680
0D74	2213	469	BNMS	KEEP1	TRY NEXT DIGIT	UCM04690
0D76	240F	470	LIS	R0,15	INITIALIZE AGAIN	UCM04700
0D78	4810 177C	471	LH	R1,TEST+6	CHECK FIRST TEST HW	UCM04710
0D7C	9011	472	KEEP2	SRLS R1,1		UCM04720
0D7E	2186	473	BCS	FOUND1+4	R0 = F-0 = TEST #	UCM04730
0D80	2701	474	SIS	R0,1		UCM04740
0D82	2213	475	BNMS	KEEP2	LOOP	UCM04750
0D84	030C	476	BR	R12	TEST NOT SELECTED	UCM04760
0D86	CA00 0010	477	FOUND1	AHI R0,16	ADJUST TEST # FOR SECOND HW	UCM04770
0D8A	4000 16C2	478	STH	R0,SELTST	HIGHEST SELECTED TEST NUMBER	UCM04780
		479	*			UCM04790
		480	* RESET TEST PARAMETERS			UCM04800
		481	*			UCM04810
0D8E	0700	482	XAR	R0,R0		UCM04820
0D90	4000 168E	483	STH	R0,ISITERR	RESET ERROR FLAG	UCM04830
0D94	4000 16C8	484	STH	R0,TOTAL	RESET TOTAL	UCM04840
0D96	4000 16CA	485	STH	R0,TOTERR	RESET TOTERR	UCM04850
0D9C	4000 16C4	486	STH	R0,WASDU	RESET WASDU	UCM04860
0DA0	C810 3030	487	LHI	R1,C'00'		UCM04870
0DA4	4010 16F2	488	STH	R1,MTESTNO	RESET THESE FLAGS TO C'00'	UCM04880
0DA8	4010 16FC	489	STH	R1,ETESTNO		UCM04890
0DAC	4010 16FE	490	STH	R1,ERRNO		UCM04900
0DB0	41F0 13CC	491	BAL	LINK,LCORE	SET UP LOW CORE	UCM04910

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		492	*				UCM04920	
		493	*	START SELECTION FROM TEST 0			UCM04930	
		494	*				UCM04940	
0DB4	0700	495	KEEP3	XAR	R0,R0		UCM04950	
0DB6	4000 16CC	496		STH	R0,BTESTNO	RESET BINARY TEST NUMBER	UCM04960	
0DBA	4000 1600	497		STH	R0,NEXTST	RESET NEXT TEST #	UCM04970	
		498	*				UCM04980	
		499	*	TO FIND THE NEXT SELECTED TEST.			UCM04990	
		500	*				UCM05000	
0DBE	4820 1600	501	KEEP4	LH	R2,NEXTST	GET NEXT TEST #	UCM05010	
0DC2	2408	502	KEEP41	LIS	R0,8		UCM05020	
0DC4	910C	503		SLHLS	R0,12	R0 = X*8000'	UCM05030	
0DC6	CC02 0000	504		SRHL	R0,0(R2)	R0 = NEXT TEST BIT	UCM05040	
0DCA	C520 0010	505		CLHI	R2,X*10'	NEXT TEST < 16	UCM05050	
0DCE	2185	506		BLS	KEEP42		UCM05060	
0DD0	4400 177E	507		NH	R0,TEST+8	LOOK AT TEST HW 2	UCM05070	
0DD4	2137	508		BNZS	KEEPS		UCM05080	
0DD6	2304	509		BS	KEEP43		UCM05090	
0DD8	4400 177C	510	KEEP42	NH	R0,TEST+6	LOOK AT TEST HW 1	UCM05100	
0DDC	2133	511		BNZS	KEEPS		UCM05110	
0DDE	2621	512	KEEP43	AIS	R2,1		UCM05120	
0DE0	220F	513		BS	KEEP41	LOOP FOR NEXT TEST #	UCM05130	
0DE2	4020 16CC	514	KEEPS	STH	R2,BTESTNO	CURRENT TEST #	UCM05140	
0DE6	0812	515		LDAR	R1,R2	R1 = TEST # IN BINARY	UCM05150	
0DE8	2621	516		AIS	R2,1		UCM05160	
0DEA	4020 1600	517		STH	R2,NEXTST		UCM05170	
0DEE	2402	518		LIS	R0,2	SET DIGITS TO PRINT = 2	UCM05180	
0DF0	C820 16F2	519		LHI	R2,MTESTNO	R2 = A(MTESTNO)	UCM05190	
0DF4	41F0 1130	520		BAL	LINK,HEXASC	STORE TEST # IN ASCII @ MTESTNO	UCM05200	
0DF8	4820 16F2	521		LH	R2,MTESTNO		UCM05210	
0DFC	4020 16FC	522		STH	R2,ETESTNO	STORE TEST # IN ASCII @ ETESTNO	UCM05220	
0E00	41F0 120E	523		BAL	LINK,TSTBRK	TEST BREAK	UCM05230	
0E04	C850 16EC	524		LHI	R5,TSTMSG		UCM05240	
0E08	41F0 1190	525		BAL	LINK,PRINT	PRINT 'TEST NN'	UCM05250	
0E0C	0700	526		XAR	R0,R0		UCM05260	
0E0E	4000 16C0	527		STH	R0,NOERR	RESET ERROR FLAG	UCM05270	
0E12	4000 16CE	528		STH	R0,COUNT	RESET COUNT	UCM05280	
0E16	4810 0A24	529	KEEP6	LH	R1,PSW2	DISABLE INTERRUPTS	UCM05290	
0E1A	9501	530		EPSR	R0,R1		UCM05300	
0E1C	4820 16CC	531		LH	R2,BTESTNO	R2 = TEST #	UCM05310	
0E20	9121	532		SLLS	R2,LADC		UCM05320	
0E22	4812 17F6	533		LDA	R1,TESTS(R2)		UCM05330	
0E26	0301	534		BR	R1	GO TO TEST MODULE	UCM05340	
		535	*-----*					UCM05350
		536	*				UCM05360	
		537	*	TEST MODULE END ROUTINE			UCM05370	
		538	*				UCM05380	
		539	TSTEND	EQU	*		UCM05390	
0E28	4810 0A24	540		LH	R1,PSW2		UCM05400	
0E2C	9501	541		EPSR	R0,R1	DISABLE INT @ PROCESSOR LEVEL	UCM05410	
0E2E	4800 16CE	542		LH	R0,COUNT		UCM05420	
0E32	2601	543		AIS	R0,1	INCREMENT COUNT	UCM05430	
0E34	4000 16CE	544		STH	R0,COUNT		UCM05440	

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0E38	4500	1788	545	CLH	R0,LOOP+6	IF COUNT > LOOP,	UCM05450
0E3C	2385		546	BNLS	KEEP7	GO TO NEXT TEST MODULE	UCM05460
0E3E	41F0	12DE	547	BAL	LINK,TSTBRK	IF BREAK GO TO OPTIN	UCM05470
0E42	4300	0E16	548	B	KEEP6	OTHERWISE, REPEAT SAME TEST	UCM05480
0E46	4800	16C0	549	KEEP7	LH R0,NOERR	LOOK @ ERROR FLAG	UCM05490
0E4A	2135		550	BNZS	KEEP71		UCM05500
0E4C	C850	1712	551	LHI	R5,NOERMSG		UCM05510
0E50	41F0	1190	552	BAL	LINK,PRINT	PRINT "NO ERROR"	UCM05520
0E54	4810	16CC	553	KEEP71	LH R1,BTESTNO	GET TEST #	UCM05530
0E58	4510	16C2	554	CLH	R1,SELTST	IS THE LAST SELECTED TEST DONE ?	UCM05540
0E5C	4280	0DBE	555	BL	KEEP4	NO, GO SELECT NEXT TEST	UCM05550
			556	*			UCM05560
			557	*	ALL THE SELECTED TESTS ARE NOW RUN		UCM05570
			558	*			UCM05580
	0000	0E60	559	ABORT	EQU *	COME HERE TO ABORT TEST SEQUENCE.	UCM05590
0E60	4200	0000	560		NOP		UCM05600
0E64	41F0	134A	561	BAL	LINK,TSTDU	RETURN WITH R1 = DU BIT	UCM05610
0E68	4230	0E90	562	BNZ	KEEP9	IF DU, DISPLAY TOTAL	UCM05620
0E6C	4810	16C6	563	LH	R1,WASDU1	WAS IT EVER ?	UCM05630
0E70	4230	0E08	564	BNZ	KEEP10	YES, PRINT TOTAL, TOTERR	UCM05640
0E74	41F0	12DE	565	BAL	LINK,TSTBRK		UCM05650
0E78	4810	1794	566	LH	R1,CONTIN+6	IF CONTIN = 1,	UCM05660
0E7C	4230	0DB4	567	BNZ	KEEP3	GO TO TEST 0	UCM05670
0E80	41F0	1370	568	BAL	LINK,SETKB	KB DEVICE = LIST DEVICE	UCM05680
0E84	C850	1764	569	LHI	R5,EOTMSG		UCM05690
0E88	41F0	1190	570	BAL	LINK,PRINT	'END OF TEST'	UCM05700
0E8C	4300	0AE6	571	B	OPTIN		UCM05710
			572	*	-----		UCM05720
			573	*	ROUTINE INCREMENTS,DISPLAYS & CHECKS 'TOTAL'		UCM05730
			574	*			UCM05740
0E90	4010	16C4	575	KEEP9	STH R1,WASDU	SET 'WASDU' FLAG	UCM05750
0E94	4810	16C8	576	LH	R1,TOTAL	INCREMENT TOTAL	UCM05760
0E98	2611		577		AIS R1,1		UCM05770
0E9A	4010	16C8	578		STH R1,TOTAL		UCM05780
0E9E	2421		579	KEEP91	LIS R2,1		UCM05790
0EA0	DE20	1695	580		OC R2,INCR	DISPLAY: INCREMENTAL MODE	UCM05800
0EA4	4800	16CA	581		LH R0,TOTERR		UCM05810
0EA8	9400		582		EXBR R0,R0		UCM05820
0EAA	9820		583		WHR R2,R0	DISPLAY TOTERR	UCM05830
0EAC	9401		584		EXBR R0,R1	FORMAT FOR DISPLAY	UCM05840
0EAE	9820		585		WHR R2,R0	DISPLAY TOTAL	UCM05850
0EB0	DE20	1694	586		OC R2,NORM	DISPLAY: NORMAL MODE	UCM05860
0EB4	C510	7FFF	587		CLHI R1,X'7FFF'	TOTAL < MAX RETAINABLE ?	UCM05870
0EB8	2389		588		BNLS HALT9		UCM05880
0EBA	4800	16CC	589		LH R0,BTESTNO	R0 = CURRENT TEST #	UCM05890
0EBE	4500	16C2	590		CLH R0,SELTST	IS IT LAST TEST ?	UCM05900
0EC2	4280	0DBE	591		BL KEEP4	NO, GO TO NEXT TEST	UCM05910
0EC6	4300	0DB4	592		B KEEP3	GO TO TEST 0	UCM05920
			593	*			UCM05930
0ECA	C810	080F	594	HALT9	LHI R1,X'80F'		UCM05940
0ECE	9114		595		SLHLS R1,4	(R1) = X'80F0'	UCM05950
0ED0	9521		596		EPSR R2,R1	HALT PROCESSOR	UCM05960
			597	*			UCM05970

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598 * WHEN EXE/RUN IS PRESSED, PRINT TOTAL & TOTERR          UCM05980
599 *                                                           UCM05990
600 BAL LINK,TSTDU SEE IF LIST DEV IS ON UC.106000
601 BNZS HALT9 NO, HALT UCM06010
602 KEEP10 XAR R0,R0 UCM06020
603 STH R0,WASDU RESET FLAG UCM06030
604 BAL LINK,CRLF UCM06040
605 LHI R5,TOTMSG UCM06050
606 STH R5,ISITERR UCM06060
607 BAL LINK,PRINT PRINT 'TOTAL TOTERR' UCM06070
608 LIS R0,4 TO PRINT 4 HEX DIGITS UCM06080
609 LH R5,TOTAL UCM06090
610 BAL LINK,R5HEX PRINT TOTAL IN HEX UCM06100
611 LIS R3,4 UCM06110
612 LHI R4,C' ' SPACE UCM06120
613 KEEP101 BAL LINK,OUTCHR OUTPUT IT UCM06130
614 SIS R3,1 UCM06140
615 BPS KEEP101 4 TIMES UCM06150
616 LIS R0,4 TO PRINT 4 HEX DIGITS UCM06160
617 LH R5,TOTERR UCM06170
618 BAL LINK,R5HEX PRINT TOTERR IN HEX UCM06180
619 B OPTIN GO TO BEGINNING UCM06190
620 * ***** UCM06200
621 * ERROR ROUTINES (OVERRIDE NOMSG OPTION) UCM06210
622 * UCM06220
623 ERR STM R0,ERRSAVE STORE REGISTERS UCM06230
624 BAL R2,ERRCOM RETURN IF LIST DEVICE IS ON UCM06240
625 BAL RET,ERR1 PRINT 'ERROR TTNN' UCM06250
626 ERRCOM2 XAR R0,R0 UCM06260
627 STH R0,ISITERR RESET ERROR FLAG UCM06270
628 LH R2,PSW UCM06280
629 EPSR R0,R2 UCM06290
630 LM R0,ERRSAVE RESTORE REGISTERS UCM06300
631 BR LINK RETURN TO TEST UCM06310
632 ERRD STM R0,ERRSAVE STORE REGISTERS UCM06320
633 BAL R2,ERRCOM RETURN IF LIST DEVICE IS ON UCM06330
634 BAL RET,ERR1 PRINT 'ERROR TTNN' UCM06340
635 BAL RET,ERRD1 PRINT 'DEV DDD' UCM06350
636 B ERRCOM2 UCM06360
637 ERRS STM R0,ERRSAVE STORE REGISTERS UCM06370
638 BAL R2,ERRCOM RETURN IF LIST DEVICE IS ON UCM06380
639 BAL RET,ERR1 PRINT 'ERROR TTNN' UCM06390
640 BAL RET,ERRS1 PRINT 'STA SS' UCM06400
641 B ERRCOM2 UCM06410
642 ERRDS STM R0,ERRSAVE STORE REGISTERS UCM06420
643 BAL R2,ERRCOM RETURN IF LIST DEVICE IS ON UCM06430
644 BAL RET,ERR1 PRINT 'ERROR TTNN' UCM06440
645 BAL RET,ERRDS1 PRINT 'DEV DDD STA SS' UCM06450
646 B ERRCOM2 UCM06460
647 ERRL STM R0,ERRSAVE STORE REGISTERS UCM06470
648 STH R15,OLOC STORE ERROR LOC TO PRINT UCM06480
649 BAL R2,ERRCOM RETURN IF LIST DEVICE IS ON UCM06490
650 BAL RET,ERR1 PRINT 'ERROR TTNN' UCM06500
0ED2 41F0 134A
0ED6 2036
0ED8 0700
0EDA 4000 16C4
0EDE 41F0 1214
0EE2 C850 1702
0EE6 4050 168E
0EEA 41F0 1190
0EEE 2404
0EF0 4850 16C8
0EF4 41F0 10CA
0EF8 2434
0EFA C840 0020
0EFE 41F0 1222
0F02 2731
0F04 2023
0F06 2404
0F08 4850 16CA
0F0C 41F0 10CA
0F10 4300 0AE6
0F14 D000 1FA8
0F18 4120 0F9E
0F1C 41E0 0FD0
0F20 0700
0F22 4000 16BE
0F26 4820 0A22
0F2A 9502
0F2C D100 1FA8
0F30 030F
0F32 D000 1FA8
0F36 4120 0F9E
0F3A 41E0 0FD0
0F3E 41E0 0FDA
0F42 4300 0F20
0F46 D000 1FA8
0F4A 4120 0F9E
0F4E 41E0 0FD0
0F52 41E0 0FF2
0F56 4300 0F20
0F5A D000 1FA8
0F5E 4120 0F9E
0F62 41E0 0FD0
0F66 41E0 100A
0F6A 4300 0F20
0F6E D000 1FA8
0F72 40F0 168E
0F76 4120 0F9E
0F7A 41E0 0FD0

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0F7E	41E0 1030	651	BAL	RET,ERRL1	PRINT 'LOC LLLL'	UCM06510
0F82	4300 0F20	652	B	ERRCOM2		UCM06520
0F86	D000 1FA8	653	ERRALL	STM R0,ERRSAVE	STORE REGISTERS	UCM06530
0F8A	4120 0F9E	654	BAL	R2,ERRCOM	RETURN IF LIST DEVICE IS ON	UCM06540
0F8E	41E0 0FD0	655	BAL	RET,ERR1	PRINT 'ERROR TTNN'	UCM06550
0F92	41E0 100A	656	BAL	RET,ERRDS1	PRINT 'DEV DDD STA SS'	UCM06560
0F96	41E0 1048	657	BAL	RET,ERRPL1	PRINT 'PSW PPPP LOC LLLL'	UCM06570
0F9A	4300 0F20	658	B	ERRCOM2		UCM06580
		659	*			UCM06590
		660	*	COMMON ERROR ROUTINE		UCM06600
		661	*			UCM06610
0F9E	4020 0FB8	662	ERRCOM	STH R2,COMRET		UCM06620
0FA2	4810 0A24	663	LH	R1,PSW2		UCM06630
0FA6	9501	664	EPSR	R0,R1	DISABLE INT. @ PROCESSOR LEVEL	UCM06640
0FA8	41F0 134A	665	BAL	LINK,TSTDU	GET LIST DEVICE DII BIT IN R1	UCM06650
0FAC	2137	666	BNZS	ERRCOM1	BRANCH IF OFF-LINE	UCM06660
0FAE	4020 16BE	667	STH	R2,ISITERR	SET ERROR FLAG	UCM06670
0FB2	4020 16C0	668	STH	R2,NOERR		UCM06680
0FB6	4300 0FB6	669	B	*	GO. PRINT ERROR MESSAGE	UCM06690
	0000 0FB8	670	COMRET	EQU *-2		UCM06700
		671	*			UCM06710
0FBA	4810 16CA	672	ERRCOM1	LH R1,TOTERR	LIST DEVICE IS OFF	UCM06720
0FBE	2611	673	AIS	R1,1		UCM06730
0FC0	4010 16CA	674	STH	R1,TOTERR	INCREMENT TOTERR	UCM06740
0FC4	C510 7FFF	675	CLHI	R1,X'7FFF'	TOTERR < MAX RETAINABLE ?	UCM06750
0FC6	4280 0E9E	676	BL	KEEP91	NO, ABORT CURRENT TEST & GOTO NEXT	UCM06760
0FCC	4300 0ECA	677	B	HALT9	YES, HALT PROCESSOR	UCM06770
		678		-----		UCM06780
		679	*	MESSAGE PRINT ROUTINES	(DO NOT OVERRIDE NOMSG OPTION)	UCM06790
		680	*			UCM06800
		681	*	TO PRINT 'ERROR TTNN'		UCM06810
		682	*			UCM06820
0FD0	C850 16F6	683	ERR1	LHI R5,ERRMSG	PRINT 'ERROR TTNN'	UCM06830
0FD4	41F0 1190	684	BAL	LINK,PRINT	TT = TEST #, NN = ERROR #	UCM06840
		685	*		RETURN	UCM06850
0FD8	030E	686	BR	RET		UCM06860
		687	*			UCM06870
		688	*	TO PRINT 'DEV DDD'		UCM06880
		689	*			UCM06890
0FDA	2403	690	ERRD1	LIS R0,3	SET UP DIGITS = 3	UCM06900
0FDC	4810 1690	691	LH	R1,ERRDEV	R1 = ERROR DEV # IN BINARY	UCM06910
0FE0	C820 1730	692	LHI	R2,ASCIDV2		UCM06920
0FE4	41F0 1130	693	BAL	LINK,HEXASC	CONVERT IT TO ASCII	UCM06930
0FE8	C850 172C	694	LHI	R5,DEVMSG2		UCM06940
0FEC	41F0 1190	695	BAL	LINK,PRINT	PRINT 'DEV DD'	UCM06950
0FF0	030E	696	BR	RET	RETURN	UCM06960
		697	*			UCM06970
		698	*	TO PRINT 'STA SS'		UCM06980
		699	*			UCM06990
0FF2	2432	700	ERRS1	LIS R0,2	SET UP DIGITS = 2	UCM07000
0FF4	D310 1692	701	LB	R1,ERRSTA	R1 = ERROR STATUS	UCM07010
0FF8	C820 1728	702	LHI	R2,ASCISTA		UCM07020
0FFC	41F0 1130	703	BAL	LINK,HEXASC	CONVERT IT TO ASCII	UCM07030

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1000	C850 1724	704	LHI	R5,STAMSG		UCM07040
1004	41F0 1190	705	BAL	LINK,PRINT	PRINT 'STA SS'	UCM07050
1008	030E	706	BR	RET	RETURN	UCM07060
		707	*			UCM07070
		708	*	TO PRINT 'DEV DDD STA SS'		UCM07080
		709	*			UCM07090
100A	2403	710	ERRDS1	LIS R0,3	SET UP DIGITS = 3	UCM07100
100C	4810 1690	711	LH	R1,ERRDEV	R1 = ERROR DEV #	UCM07110
1010	C820 1720	712	LHI	R2,ASCIDEV		UCM07120
1014	41F0 1130	713	BAL	LINK,HEXASC	CONVERT IT TO ASCII	UCM07130
1018	2402	714	LIS	R0,2	SET UP DIGITS = 2	UCM07140
101A	D310 1692	715	LB	R1,ERRSTA	R1 = ERROR STATUS	UCM07150
101E	C820 1728	716	LHI	R2,ASCISTA		UCM07160
1022	41F0 1130	717	BAL	LINK,HEXASC	CONVERT IT TO ASCII	UCM07170
1026	C850 171C	718	LHI	R5,DEVMSG		UCM07180
102A	41F0 1190	719	BAL	LINK,PRINT	PRINT 'DEV DD STA SS'	UCM07190
102E	030E	720	BR	RET	RETURN	UCM07200
		721	*			UCM07210
		722	*	TO PRINT 'LOC LLLL'		UCM07220
		723	*			UCM07230
1030	2404	724	ERRL1	LIS R0,4	SET UP DIGITS = 4	UCM07240
1032	4810 168E	725	LH	R1,OLOC	R1= OLD LOC	UCM07250
1036	C820 1744	726	LHI	R2,ASCILOC		UCM07260
103A	41F0 1130	727	BAL	LINK,HEXASC	CONVERT IT TO ASCII	UCM07270
103E	C850 1740	728	LHI	R5,LOCMSG		UCM07280
1042	41F0 1190	729	BAL	LINK,PRINT	PRINT 'LOC LLLL'	UCM07290
1046	030E	730	BR	RET	RETURN	UCM07300
		731	*			UCM07310
		732	*	TO PRINT 'PSW PPPP LOC LLLL'		UCM07320
		733	*			UCM07330
1048	2404	734	ERRPL1	LIS R0,4	SET UP DIGITS = 4	UCM07340
104A	4810 168A	735	LH	R1,OPSW	R1 = OLD PSW	UCM07350
104E	C820 173A	736	LHI	R2,ASCIPSW		UCM07360
1052	41F0 1130	737	BAL	LINK,HEXASC	CONVERT IT TO ASCII	UCM07370
1056	4810 168E	738	LH	R1,OLOC	R1= OLD LOC	UCM07380
105A	C820 1744	739	LHI	R2,ASCILOC		UCM07390
105E	41F0 1130	740	BAL	LINK,HEXASC	CONVERT IT TO ASCII	UCM07400
1062	C850 1736	741	LHI	R5,PSWMSG		UCM07410
1066	41F0 1190	742	BAL	LINK,PRINT	PRINT 'PSW PPPP LOC LLLL'	UCM07420
106A	030E	743	BR	RET	RETURN	UCM07430
		744	*	*****		UCM07440
		745	*	TO OBTAIN OPTION VALUE IN R6 (16 BITS, TARGT 16)		UCM07450
		746	*			UCM07460
106C	0766	747	OPTVAL	XAR R6,R6	INITIALIZE ACCUMULATOR	UCM07470
106E	41F0 1290	748	BAL	R15,GETCHR	GET A CHAR IN R4	UCM07480
1072	24FF	749	OPTVAL0	LIS R15,15		UCM07490
1074	D44F 16DC	750	OPTVAL1	CLB R4,HEXTAB(R15)	SCAN TABLE	UCM07500
1078	2334	751	BES	OPTVAL2	MATCH	UCM07510
107A	27F1	752	SIS	R15,1		UCM07520
107C	2214	753	BNMS	OPTVAL1		UCM07530
107E	030C	754	BR	R12	ERROR; VALUE NOT IN TABLE.	UCM07540
1080	9164	755	OPTVAL2	SLLS R6,4	SHIFT LEFT 4	UCM07550
1082	066F	756	OAR	R6,R15	OR IN CURRENT DIGIT	UCM07560

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1084	41F0	1290	757	OPTVAL3	BAL	R15,GETCHR	GET NEXT CHAR	UCM07570
1088	C540	005F	758		CLHI	R4,X'5F'	IS IT LEFT ARROW ?	UCM07580
108C	2133		759		BNES	OPTVAL4		UCM07590
108E	9064		760		SRLS	R6,4	THROW AWAY LAST HEX ENTRY	UCM07600
1090	2206		761		BS	OPTVAL3		UCM07610
1092	C540	000D	762	OPTVAL4	CLHI	R4,13	EXIT IF CR	UCM07620
1096	033E		763		BER	R14		UCM07630
1098	C540	002C	764		CLHI	R4,X'2C'	OR COMMA	UCM07640
109C	4230	1072	765		BNE	OPTVAL0	LOOP TO PROCESS	UCM07650
10A0	030E		766		BR	R14	RETURN	UCM07660
			767					UCM07670
			768				* TO CONVERT (R6) FROM BINARY TO UNARY PATTERN, IN R3	UCM07680
			769				*	UCM07690
10A2	2431		770	UNARY	LIS	R3,1	INITIALIZE	UCM07700
10A4	C560	000F	771	UNARY1	CLHI	R6,15	DONE ?	UCM07710
10A8	033E		772		BER	R14	RETURN	UCM07720
10AA	0A33		773		AAR	R3,R3	NO. SHIFT R3.	UCM07730
10AC	2661		774		AIS	R6,1	INCREMENT COUNTER	UCM07740
10AE	2205		775		BS	UNARY1		UCM07750
			776					UCM07760
			777				* TO PROVIDE # OF MILLISECONDS DELAY SPECIFIED BY R0	UCM07770
			778				*	UCM07780
10B0	0000	1EE8	779	TIMER	STM	R0,RSAVE	SAVE REGISTERS	UCM07790
10B4	2410		780		LIS	R1,0		UCM07800
10B6	2421		781		LIS	R2,1		UCM07810
10B8	4830	0A1E	782		LH	R3,TIME	R3 = TIME CONSTANT FOR 1 MS DELAY	UCM07820
10BC	C110	10BC	783		BXLE	R1,*		UCM07830
10C0	2701		784		SIS	R0,1		UCM07840
10C2	2037		785		BNZS	TIMER+4	LOOP TILL SPECIFIED DELAY	UCM07850
10C4	0100	1EE8	786		LM	R0,RSAVE	RESTORE REGISTERS	UCM07860
10C8	030F		787	TIMXT	BR	LINK	RETURN	UCM07870
			788					UCM07880
			789				* RSHX PRINTS CONTENTS OF R5 IN HEX	UCM07890
			790				* PRINTS UPTO 4 DIGITS (8 DIGITS, TARGT 32)	UCM07900
			791				*	UCM07910
10CA	0000	1EE8	792	RSHX	STM	R0,RSAVE	STORE REGISTERS	UCM07920
10CE	0820		793		LDAR	R2,R0	R2 = # OF DIGITS TO BE PRINTED	UCM07930
10D0	2721		794		SIS	R2,1		UCM07940
10D2	4210	10EE	795		BM	R5XB		UCM07950
10D6	9122		796		SLLS	R2,2	R2 = 4(DIGITS-1)	UCM07960
10D8	0845		797	R5X	LDAR	R4,R5		UCM07970
10DA	CC42	0000	798		SRAL	R4,0(R2)		UCM07980
10DE	C440	000F	799		NHI	R4,15	R4 = HEX DIGIT	UCM07990
10E2	D344	16DC	800		LB	R4,HEXTAB(R4)		UCM08000
10E6	41F0	1222	801	R5XA	BAL	R15,OUTCHR		UCM08010
10EA	2724		802		SIS	R2,4		UCM08020
10EC	221A		803		BNAS	R5X	LOOP TILL ALL DIGITS	UCM08030
10EE	D100	1EE8	804	R5XB	LM	R0,RSAVE	RESTORE REGISTERS	UCM08040
10F2	030F		805		BR	LINK	RETURN	UCM08050
			806					UCM08060
			807				* R5BIN PRINTS CONTENTS OF R5 IN BINARY	UCM08070
			808				* PRINTS UPTO 16 DIGITS	UCM08080
			809				*	UCM08090

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10F4	D000	1EE8	810	R5BIN	STM	R0,RSAVE	STORE REGISTERS	UCM08100
10F8	0830		811		LDAR	R3,R0	R3 = # OF DIGITS TO BE PRINTED	UCM08110
10FA	C810	0010	812		LHI	R1,16		UCM08120
10FE	0813		813		SAR	R1,R3		UCM08130
1100	211C		814		BMS	R5B2	EXIT	UCM08140
1102	CD51	0000	815		SLHL	R5,0(R1)	R5 = DATA TO BE PRINTED	UCM08150
1106	C840	0030	816	R5B	LHI	R4,C*0'		UCM08160
110A	9151		817		SLHLS	R5,1		UCM08170
110C	2382		818		BNCS	R5B1		UCM08180
110E	2641		819		AIS	R4,1	IF CARRY, PRINT 1	UCM08190
1110	41F0	1222	820	R5B1	BAL	LINK,OUTCHR		UCM08200
1114	2731		821		SIS	R3,1	R3 = # OF REMAINING DIGITS	UCM08210
1116	2124		822		BPS	R5B3		UCM08220
1118	D100	1EE8	823	R5B2	LM	R0,RSAVE	RESTORE REGISTERS	UCM08230
111C	030F		824		BR	LINK	RETURN	UCM08240
111E	C330	0003	825	R5B3	THI	R3,3	4,8 OR 12 DIGITS LEFT ?	UCM08250
1122	2135		826		BNZS	R5B4	NO	UCM08260
1124	C840	0020	827		LHI	R4,C' '	YES, OUTPUT ONE SPACE	UCM08270
1128	41F0	1222	828		BAL	R15,OUTCHR		UCM08280
112C	4300	1106	829	R5B4	B	R5B	LOOP FOR NEXT DIGIT	UCM08290
			830		*-----*			UCM08300
			831		* TO CONVERT HEXADECIMAL DATA IN R1 TO ASCII CHAR & STORF @ 0(R2)			UCM08310
			832		*			UCM08320
1130	D000	1EE8	833	HEXASC	STM	R0,RSAVE	STORE REGISTERS	UCM08330
1134	0830		834		LDAR	R3,R0	R3 = DIGITS	UCM08340
1136	9132		835		SLLS	R3,2		UCM08350
1138	2734		836		SIS	R3,4	R3 = 4(DIGITS)-4	UCM08360
113A	0841		837	HEXASC1	LDAR	R4,R1	R4 = HEX DATA	UCM08370
113C	CC43	0000	838		SRAL	R4,0(R3)		UCM08380
1140	C440	000F	839		NHI	R4,15	R4 = HEX DIGIT TO BE CONVERTED	UCM08390
1144	D344	16DC	840		LB	R4,HEXTAB(R4)		UCM08400
1148	D242	0000	841		STB	R4,0(R2)	STORE ASCII CHAR	UCM08410
114C	2621		842		AIS	R2,1		UCM08420
114E	2734		843		SIS	R3,4		UCM08430
1150	2218		844		BNMS	HEXASC1	LOOP TILL ALL DIGITS	UCM08440
1152	D100	1EE8	845		LM	R0,RSAVE	RESTORE REGISTERS	UCM08450
1156	030F		846		BR	LINK	RETURN	UCM08460
			847		*-----*			UCM08470
			848		* TO CONVERT BINARY DATA IN R1 INTO DECIMAL DIGITS			UCM08480
			849		* AND STORE THEM IN ASCII @ 0(R2)			UCM08490
			850		*			UCM08500
1158	D000	1EE8	851	DECASC	STM	R0,RSAVE		UCM08510
115C	0830		852		LDAR	R3,R0	COPY DIGIT COUNT	UCM08520
115E	9131		853		SLLS	R3,LADC	&ESTABLISH DECTAB INDEX.	UCM08530
1160	2732		854		SIS	R3,ADC		UCM08540
1162	0744		855	\$DEC1	XAR	R4,R4	CLEAR MODULUS COUNTER	UCM08550
1164	4853	16D2	856		LDA	R5,DECTAB(R3)	LOAD LARGEST REQ. POWER OF 10.	UCM08560
1168	0515		857	\$DEC2	CLAR	R1,R5	EXCEEDS TEST VALUF ?	UCM08570
116A	2188		858		BLS	\$DEC3	BRANCH IF YES.	UCM08580
116C	0B15		859		SAR	R1,R5	DECREMENT TEST VALUE	UCM08590
116E	2641		860		AIS	R4,1	INCREMENT MODULUS COUNTER	UCM08600
1170	C540	000A	861		CLHI	R4,10	VALID DECIMAL DIGIT ?	UCM08610
1174	2086		862		BLS	\$DEC2	BRANCH IF YES; ELSE	UCM08620

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1176	274A	863	SIS	R4,10	FORCE VALID DIGIT.	UCM08630
1178	2208	864	BS	\$DEC2	REPEAT DECREMENT.	UCM08640
117A	D344 16DC	865	\$DEC3	LB R4,HEXTAB(R4)	CONVERT MODULUS COUNT TO ASCII	UCM08650
117E	D242 0000	866	STB	R4,0(R2)	AND STORE AT DESTINATION MSB.	UCM08660
1182	2621	867	AIS	R2,1	INCREMENT DESTINATION POINTER	UCM08670
1184	2732	868	SIS	R3,ADC	DECREMENT DECTAB POINTER	UCM08680
1186	4310 1162	869	BNM	\$DEC1	FALL THROUGH ON DFCTAB UNDERFLOW.	UCM08690
118A	D100 1EE8	870	LM	R0,RSAVE	RESTORE USER'S REGISTERS	UCM08700
118E	030F	871	BR	LINK	RETURN.	UCM08710
		872	*-----*			UCM08720
		873	* TO PRINT THE ASCII MESSAGE			UCM08730
		874	*			UCM08740
1190	D000 1EE8	875	PRINT	STM R0,RSAVE	STORE REGISTERS	UCM08750
1194	41F0 134A	876		BAL LINK,TSTDU		UCM08760
1198	2335	877		BZS P1		UCM08770
119A	4010 16C4	878		STH R1,WASDU	SET FLAG	UCM08780
119E	4300 120A	879		B PRINT5	EXIT	UCM08790
11A2	4820 16C4	880	P1	LH R2,WASDU		UCM08800
11A6	4330 11D4	881		BZ P3		UCM08810
11AA	C810 0140	882		LHI R1,X'140'	DELAY CONSTANT	UCM08820
11AE	C800 1000	883		LHI R0,X'1000'		UCM08830
11B2	2701	884		SIS R0,1		UCM08840
11B4	2031	885		BTBS 3,1		UCM08850
11B6	2711	886		SIS R1,1		UCM08860
11B8	2035	887		BTBS 3,5	LOOP TILL TIMEOUT	UCM08870
11BA	0744	888		XAR R4,R4		UCM08880
11BC	4040 16C4	889		STH R4,WASDU		UCM08890
11C0	2541	890		LCS R4,1	CHARACTER = X'FF'	UCM08900
11C2	4040 16C6	891		STH R4,WASDU1		UCM08910
11C6	2434	892		LIS R3,4		UCM08920
11C8	41F0 1222	893	P2	BAL LINK,OUTCHR		UCM08930
11CC	2731	894		SIS R3,1		UCM08940
11CE	2023	895		BPS P2		UCM08950
11D0	4300 0ED8	896		B KEEP10	PRINT TOTAL, TOTERR	UCM08960
11D4	4800 17A0	897	P3	LH R0,NOMSG+6		UCM08970
11D8	2335	898		BZS PRINT2	NO, PRINT ALL MESSAGES	UCM08980
11DA	4800 16BE	899		LH R0,ISITERR		UCM08990
11DE	4330 120A	900		BZ PRINT5	NOT AN ERROR MSG. EXIT	UCM09000
		901	*			UCM09010
11E2	D345 0000	902	PRINT2	LB R4,0(R5)	GET A MESSAGE BYTE	UCM09020
11E6	41F0 1222	903		BAL LINK,OUTCHR	OUTPUT IT	UCM09030
11EA	2740	904		SIS R4,13	CR ?	UCM09040
11EC	2333	905		BZS PRINT3	MSG OVER	UCM09050
11EE	2651	906		AIS R5,1		UCM09060
11F0	2207	907		BS PRINT2	LOOP FOR NEXT CHAR	UCM09070
11F2	244A	908	PRINT3	LIS R4,10	LF	UCM09080
11F4	D310 1ED7	909		LB R1,IOSAVE+1	GET LIST DEV IDENTIFIER	UCM09090
11F8	2713	910		SIS R1,3	LINE PRINTER ?	UCM09100
11FA	2335	911		BZS PRINT3A	BRANCH IF YES.	UCM09110
11FC	41F0 1222	912		BAL LINK,OUTCHR	LF	UCM09120
1200	2541	913		LCS R4,1	DEL	UCM09130
1202	2302	914		BS PRINT3B		UCM09140
1204	2441	915	PRINT3A	LIS R4,1	YES, OUTPUT X'01'	UCM09150

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1206	41F0	1222	916	PRINT3B	BAL	LINK,OUTCHR	TERMINAL CHARACTER	UCM09160
120A	41F0	12DE	917	PRINT5	BAL	LINK,TSTBRK		UCM09170
120E	0100	1EE6	918		LM	RO,RSAVE	RESTORE REGISTERS	UCM09180
1212	030F		919		BR	LINK	RETURN	UCM09190
			920	*-----*				UCM09200
			921	* SMALL SUPPORT ROUTINES				UCM09210
			922	*				UCM09220
			923	* TO OUTPUT CR,LF TO LIST DEVICE				UCM09230
			924	*				UCM09240
1214	0000	1EE6	925	CRLF	STM	RO,RSAVE	STORE REGISTERS	UCM09250
1218	2440		926		LIS	R4,13		UCM09260
121A	41F0	1222	927		BAL	LINK,OUTCHR	OUTPUT CR	UCM09270
121E	4300	11F2	928		B	PRINT3	LINE FEED, RESTORE, RETURN	UCM09280
			929	*-----*				UCM09290
			930	* TO OUTPUT A CHARACTER TO THE LIST DEVICE				UCM09300
1222	40F0	128C	931	OUTCHR	STH	R15,OUT1+2	SAVE RETURN ADDRESS	UCM09310
1226	D300	1ED7	932		LB	RO,IOSAVE+1		UCM09320
122A	2704		933		SIS	RO,4		UCM09330
122C	4230	1260	934		BNZ	OUTCHR2	BRANCH IF NOT CAROUSEL	UCM09340
1230	4000	128E	935	OTC.	STH	RO,PAUSE		UCM09350
1234	41F0	134A	936	OTC.0	BAL	LINK,TSTDU	ON LINE ?	UCM09360
1238	4230	1286	937		BNZ	OUT0	NO, BRANCH	UCM09370
123C	9D01		938		SSR	RO,R1	GET CAROUSEL STATUS	UCM09380
123E	2386		939		BFFS	8,OTC.1	BRANCH IF CHAR. IS TO BE READ	UCM09390
1240	4810	128E	940		LH	R1,PAUSE	PAUSED NOW ?	UCM09400
1244	2038		941		BNZS	OTC.0	YES, LOOP	UCM09410
1246	4300	1260	942		B	OUTCHR2	NO, GO OUTPUT CHARACTER	UCM09420
	0000	124A	943	OTC.1	EQU	*		UCM09430
124A	9601		944		RDR	RO,R1	GET CAROUSEL CHARACTER	UCM09440
124C	C410	007F	945		NHI	R1,X*7F'		UCM09450
1250	CB10	0012	946		SHI	R1,X*12'	DC2 ?	UCM09460
1254	2336		947		BZS	OUTCHR2	YES, BRANCH	UCM09470
1256	2712		948		SIS	R1,2	DC4 ?	UCM09480
1258	4330	1230	949		BZ	OTC.	YES, GO SET PAUSE FLAG	UCM09490
125C	4300	1234	950		B	OTC.0	NO, GO WAIT FOR DC2	UCM09500
	0000	1260	951	OUTCHR2	EQU	*		UCM09510
1260	4010	128E	952		STH	R1,PAUSE	RESET FLAG	UCM09520
1264	41F0	134A	953		BAL	LINK,TSTDU	OFF-LINE ?	UCM09530
1268	213F		954		BNZS	OUT0	BRANCH IF OFF-LINE	UCM09540
126A	4110	1386	955		BAL	R1,SETUP	SET UP FOR OUTPUT	UCM09550
126E	9D01		956	OTC.4	SSR	RO,R1	WAIT FOR NOT BUSY	UCM09560
1270	2138		957		BTFS	3,OUT0	BRANCH IF OFF-LINE	UCM09570
1272	C510	000C	958		CLHI	R1,12	PASLA OFFLINE ?	UCM09580
1276	2338		959		BES	OUT0	BRANCH: YES.	UCM09590
1278	C310	0008	960		THI	R1,8	BUSY ?	UCM09600
127C	2037		961		BNZS	OTC.4	WAIT FOR NOT BUSY.	UCM09610
127E	9A04		962		WDR	RO,R4	OUTPUT DATA BYTE	UCM09620
1280	9D01		963		SSR	RO,R1		UCM09630
1282	2081		964		BTBS	8,1	WAIT FOR NOT BUSY.	UCM09640
1284	2303		965		BS	OUT1		UCM09650
1286	4010	16C4	966	OUT0	STH	R1,WASDU	SET FLAG	UCM09660
128A	4300	128A	967	OUT1	B	*	RETURN AS SET UP ABOVE	UCM09670
128E	0000		968	PAUSE	DCX	0	SET DURING TRANSMISSION PAUSE	UCM09680

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		969	*-----			UCM09690
		970	* TO GET A CHAR FROM KEYBOARD (IN REG R4)			UCM09700
		971	*			UCM09710
1290	4140 137E	972	GETCHR BAL R4,KBREAD	PUT KB DEVICE IN READ MODE		UCM09720
1294	9D04	973	SSR R0,R4			UCM09730
1296	021F	974	BTBR 1,LINK	IF DU, RETURN		UCM09740
1298	2082	975	BTBS 8,2	IF BUSY, LOOP		UCM09750
129A	D400 0A1A	976	CLB R0,MICROBUS	IS IT MICROBUS ?		UCM09760
129E	2333	977	BES ECHO1	YES, BRANCH		UCM09770
12A0	9B04	978	RDR R0,R4	READ A CHAR IN R4		UCM09780
12A2	2303	979	BS ECHO			UCM09790
12A4	9B04	980	ECHO1 RDR R0,R4			UCM09800
12A6	9A04	981	WDR R0,R4			UCM09810
		982	* TO ECHO RECEIVED CHARACTERS TO CONSOLE DEVICE IN FDX MODE			UCM09820
12A8	D390 169C	983	ECHO LB R9,CONRD			UCM09830
12AC	C590 00A9	984	CLHI R9,X'A9'	CAROUSEL ?		UCM09840
12B0	D137	985	BNES ECHRTN	DO NOT ECHO		UCM09850
12B2	D390 169B	986	LB R9,CONADR+1			UCM09860
12B6	0D90 1693	987	SS R9,SINK			UCM09870
12BA	2082	988	BTBS 8,2			UCM09880
12BC	9A94	989	WDR R9,R4	ECHO RECEIVED BYTE		UCM09890
12BE	C440 007F	990	ECHRTN NHI R4,X'7F'	REMOVE PARITY BIT		UCM09900
12C2	030F	991	BR LINK	RETURN		UCM09910
		992	*-----			UCM09920
		993	* TO OUTPUT '?' TO CONSOLE			UCM09930
		994	*			UCM09940
12C4	41F0 1214	995	QUESTN BAL LINK,CRLF			UCM09950
12C8	40F0 16BE	996	STH LINK,ISITERR	SET FLAG		UCM09960
12CC	C650 1772	997	LHI R5,QMSG			UCM09970
12D0	41F0 1190	998	BAL LINK,PRINT	PRINT '??'		UCM09980
12D4	0700	999	XAR R0,R0			UCM09990
12D6	4000 16BE	1000	STH R0,ISITERR			UCM10000
12DA	4300 0AEA	1001	B OPTINI	TO ACCEPT COMMAND INPUT		UCM10010
		1002	*-----			UCM10020
		1003	* IF BREAK KEY DEPRESSED, GO TO 'OPTIN' OR (BRKVECT); ELSE RETURN.			UCM10030
		1004	*			UCM10040
12DE	D000 1F28	1005	TSTBRK STM R0,RSAVE+64	STORE REGISTERS		UCM10050
12E2	40F0 1348	1006	STH LINK,BRKRTN			UCM10060
12E6	D300 169A	1007	LB R0,CONADR	GET KEYBOARD DEVICE ADR		UCM10070
12EA	9D01	1008	SSR R0,R1			UCM10080
12EC	C310 0020	1009	THI R1,X'20'	'BREAK' KEY PRESSED ?		UCM10090
12F0	4330 133C	1010	BZ TSTBRK3	NO. EXIT		UCM10100
12F4	D320 0A10	1011	LB R2,I0			UCM10110
12F8	C520 0005	1012	CLHI R2,5	IS IT MICROBUS ?		UCM10120
12FC	2139	1013	BNES TSTBRK4	NO. BRANCH		UCM10130
	0000 12FE	1014	TSTBRK5 EQU *			UCM10140
12FE	9B02	1015	RDR R0,R2			UCM10150
1300	9D01	1016	SSR R0,R1			UCM10160
1302	C310 0020	1017	THI R1,X'20'			UCM10170
1306	4230 12FE	1018	BNZ TSTBRK5			UCM10180
130A	4300 1330	1019	B TSTBRK2			UCM10190
	0000 130E	1020	TSTBRK4 EQU *			UCM10200
130E	4820 1696	1021	LH R2,PASFL6	PASLA ?		UCM10210

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1394	DE00 16B4	1075	OC	R0,CONRQ2S		UCM10750
1398	0304	1076	BR	R4	RETURN	UCM10760
		1077	*-----*			UCM10770
		1078	* TO SET UP KEYBOARD DEV TO READ WITH INT ENABLED			UCM10780
		1079	*			UCM10790
139A	D000 1EE8	1080	KBRD	STM	R0,RSAVE	UCM10800
139E	D300 169A	1081		LB	R0,CONADR	UCM10810
13A2	4810 1696	1082		LH	R1,PASFLG	UCM10820
13A6	2333	1083		BZS	KBRD1	UCM10830
13A8	DE00 16B4	1084		OC	R0,CONRQ2S	UCM10840
13AC	DE00 16A9	1085	KBRD1	OC	R0,CONENRD	UCM10850
13B0	D100 1EE8	1086		LM	R0,RSAVE	UCM10860
13B4	030F	1087		BR	LINK	UCM10870
		1088	*-----*			UCM10880
		1089	* LIST DEVICE SET UP ROUTINE			UCM10890
		1090	*			UCM10900
13B6	4010 13CA	1091	SETUP	STH	R1,SET,RTN	UCM10910
13BA	D310 1ED7	1092		LB	R1,IOSAVE+1	UCM10920
13BE	9111	1093		SLHLS	R1,1	UCM10930
13C0	D301 0A11	1094		LB	R0,IO+1(R1)	UCM10940
13C4	DE01 169D	1095		OC	R0,CONWRT(R1)	UCM10950
13C8	4300 13C8	1096		B	*	UCM10960
	0000 13CA	1097	SET,RTN	EQU	*-2	UCM10970
		1098	* *****			UCM10980
		1099	* LOW CORE SET UP ROUTINE			UCM10990
		1100	*			UCM11000
13CC	0711	1101	LCORE	XAR	R1,R1	UCM11010
13CE	2422	1102		LIS	R2,2	UCM11020
13DC	C830 004E	1103		LHI	R3,X'4E'	UCM11030
13D4	0700	1104		XAR	R0,R0	UCM11040
13D6	4001 0000	1105	ZER01	STH	R0,0(R1)	UCM11050
13DA	C110 13D6	1106		BXLE	R1,ZER01	UCM11060
13DE	C810 0080	1107		LHI	R1,X'80'	UCM11070
13E2	C830 00CE	1108		LHI	R3,X'CE'	UCM11080
13E6	4001 0000	1109	ZER02	STH	R0,0(R1)	UCM11090
13EA	C110 13E6	1110		BXLE	R1,ZER02	UCM11100
13EE	C800 151C	1111		LHI	R0,XI32	UCM11110
13F2	C830 08CE	1112		LHI	R3,X'8CE'	UCM11120
13F6	4001 0000	1113	ZER03	STH	R0,0(R1)	UCM11130
13FA	C110 13F6	1114		BXLE	R1,ZER03	UCM11140
13FE	C830 1622	1115		LHI	R3,II	UCM11150
1402	4030 0036	1116		STH	R3,X'36'	UCM11160
1406	C840 163C	1117		LHI	R4,MM	UCM11170
140A	4040 003E	1118		STH	R4,X'3E'	UCM11180
140E	C830 15EE	1119		LHI	R3,AF	UCM11190
1412	4030 004E	1120		STH	R3,X'4E'	UCM11200
		1121	* ARITHMETIC FAULT NEW PSW LOC(32-BIT) FIXED PT DIVIDE FAULT NEW PSW LOC			UCM11210
1416	C840 1EE6	1122		LHI	R4,RSAVE	UCM11220
141A		1123		IFZ	ADC-2	UCM11230
141A	4810 1684	1124		LH	R1,MOD32	UCM11240
141E	4230 1440	1125		BNZ	LCORE32	UCM11250
		1126	* SET UP LOW CORE FOR 16 BIT MACHINE			UCM11260
		1127	* SET UP LOW CORE FOR 16 BIT MACHINE			UCM11270

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		1128	*				UCM11280		
1422	4040	0022		1129	STH	R4,X'22'	REG SAVE POINTER	UCM11290	
1426	C830	15DC		1130	LHI	R3,FP		UCM11300	
142A	4030	002E		1131	STH	R3,X'2E'	FLOATING PT FAULT INT NEW PSW LOC	UCM11310	
142E	4850	0A24		1132	LH	R5,PSW2		UCM11320	
1432	4050	0044		1133	STH	R5,X'44'	HW EXT INT NEW PSW STATUS	UCM11330	
1436	C850	150E		1134	LHI	R5,XI16		UCM11340	
143A	4050	0046		1135	STH	R5,X'46'	EXT INT NEW PSW LOC	UCM11350	
143E	030F			1136	BR	LINK		UCM11360	
				1137	ENDC			UCM11370	
				1138	*			UCM11380	
				1139	* SET UP LOW CORE FOR 32 BIT MACHINE			UCM11390	
				1140	*			UCM11400	
1440	4040	0086		1141	LCORE32	STH	R4,X'86'	REG SAVE POINTER	UCM11410
1444	C840	1EE0		1142	LHI	R4,PSWSAVE	PPF PSW SAVE AREA	UCM11420	
1446	4040	0084		1143	STH	R4,X'84'	. POINTER	UCM11430	
144C	C830	15E4		1144	LHI	R3,RP		UCM11440	
1450	4030	0096		1145	STH	R3,X'96'	RELOC/PROTECT INT NEW PSW LOC	UCM11450	
1454	D310	169A		1146	LB	R1,CONADR	LOAD CONSOLE I/O ADDRESS	UCM11460	
1458	0A11			1147	AAR	R1,R1		UCM11470	
145A	C800	1478		1148	LHI	R0,KBINT0	R0 = A(KEYBOARD INT HANDLER)	UCM11480	
145E	4001	00D0		1149	STH	R0,X'D0'(R1)	STORE @ X'D0'+2(KB DEV ADR)	UCM11490	
1462	0711			1150	XAR	R1,R1	TO SET UP SERVICE POINTER TABLE	UCM11500	
1464	C830	151C		1151	LHI	R3,XI32		UCM11510	
1468	4821	188A		1152	LCORE32A	LH	R2,DEVSADR(R1)	GET DEV ADR FROM TABLE	UCM11520
146C	021F			1153	BMR	LINK	DONE. RETURN	UCM11530	
146E	0A22			1154	AAR	R2,R2		UCM11540	
1470	4032	00D0		1155	STH	R3,X'D0'(R2)	STORE @ X'D0'+2(DEV ADR)	UCM11550	
1474	2612			1156	AIS	R1,2		UCM11560	
1476	2207			1157	BS	LCORE32A		UCM11570	
				1158	*-----*			UCM11580	
				1159	* KEYBOARD INTERRUPT HANDLER			UCM11590	
				1160	*			UCM11600	
1478	C330	0020		1161	KBINT0	THI	R3,X'20'	IS BREAK KEY DEPRFSED ?	UCM11610
147C	4330	14C4		1162	BZ	KBINT1	NO	UCM11620	
1480	D300	0A10		1163	LB	R0,I0		UCM11630	
1484	C500	0005		1164	CLHI	R0,5	IS IT MICROBUS ?	UCM11640	
1488	4230	14A4		1165	BNE	KBINT0B	NO, BRANCH	UCM11650	
148C	DE20	16A6		1166	OC	R2,MREADC	YES, ISSUE READ	UCM11660	
1490	9D23			1167	SSR	R2,R3		UCM11670	
1492	2081			1168	BTBS	8,1		UCM11680	
1494	9B24			1169	KBINT0C	RDR	R2,R4	KNOCK DOWN BREAK	UCM11690
1496	9D23			1170	SSR	R2,R3		UCM11700	
1498	C330	0020		1171	THI	R3,X'20'	BREAK STILL THERE ?	UCM11710	
149C	4230	1494		1172	BNZ	KBINT0C	YES, KNOCK IT DOWN AGAIN	UCM11720	
14A0	4300	14FC		1173	B	RETOPSW	NO, RETURN ON OLD PSW	UCM11730	
	0000	14A4		1174	KBINT0B	EQU	*	UCM11740	
14A4	4850	1696		1175	LH	R5,PASFLG	CONSOLE ON PASLA ?	UCM11750	
14A8	2339			1176	BZS	KBINT0A	BRANCH IF NO.	UCM11760	
14AA	9B24			1177	RDR	R2,R4		UCM11770	
14AC	9D23			1178	SSR	R2,R3		UCM11780	
14AE	2281			1179	BFBS	8,1		UCM11790	
14B0	0844			1180	LDAR	R4,R4		UCM11800	

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14B2	4230	14FC	1181	BNZ	RETOPSW	IGNORE FRERR ONLY	UCM11810
14B6	4300	0AE6	1182	KBINT00	B OPTIN		UCM11820
14BA	9023		1183	KBINT0A	SSR R2,R3		UCM11830
14BC	C330	0020	1184		THI R3,X*20*		UCM11840
14C0	2033		1185		BTBS 3,3	WAIT FOR BREAK RELEASE	UCM11850
14C2	2206		1186		BS KBINT00	GO TO COMMAND MODE	UCM11860
	0000	14C4	1187	KBINT1	EQU *		UCM11870
14C4	C500	0005	1188		CLHI R0,5	IS IT MICROBUS ?	UCM11880
14C8	4230	14DA	1189		BNE KBINT3	NO, BRANCH	UCM11890
14CC	DE20	16A6	1190		OC R2,MREADC	READ COMMAND TO MICROBUS	UCM11900
14D0	9D23		1191		SSR R2,R3		UCM11910
14D2	2081		1192		BTBS 8,1		UCM11920
14D4	9B24		1193		RDR R2,R4	KNOCK DOWN INTERRUPT	UCM11930
14D6	4300	14FC	1194		B RETOPSW	RETURN	UCM11940
	0000	14DA	1195	KBINT3	EQU *		UCM11950
14DA	4020	1690	1196		STH R2,INTDEV		UCM11960
14DE	D230	1692	1197		STB R3,INTSTA		UCM11970
14E2			1198		IFZ ADC-2		UCM11980
14E2	4840	1684	1199		LH R4,MOD32		UCM11990
14E6	2335		1200		BZS KBINT2		UCM12000
			1201		ENDC		UCM12010
14E8	4000	168A	1202		STH R0,OPSW	STORE OLD PSW OF 32-BIT PROCESSOR	UCM12020
14EC	4010	168E	1203		STH R1,OLOC	IN ORDER TO RETURN BACK TO TEST	UCM12030
14F0	9B24		1204	KBINT2	RDR R2,R4		UCM12040
14F2	41F0	12A8	1205		BAL LINK,ECHO	ECHO RECEIVED BYTF	UCM12050
14F6	4890	168A	1206		LH R9,KBINT	IF ZERO,IGNORE; ELSE	UCM12060
14FA	0239		1207		BNZR R9	GO,PROCESS KB INT FURTHER	UCM12070
			1208		* -----		UCM12080
			1209		* TO RETURN ON OLD PSW		UCM12090
			1210		*		UCM12100
	0000	14FC	1211	RETOPSW	EQU *		UCM12110
14FC			1212		IFZ ADC-2		UCM12120
14FC	4890	1684	1213		LH R9,MOD32		UCM12130
1500	2135		1214		BNZS RETOPSW1		UCM12140
1502	D100	1F68	1215		LM R0,INTSAV	RESTORE REGISTERS	UCM12150
1506	C200	0040	1216		LPSW X*40*	RETURN ON OLD PSW AFTER KB INT	UCM12160
			1217		ENDC		UCM12170
150A	C200	1688	1218	RETOPSW1	LPSW OPSW32		UCM12180
			1219		* *****		UCM12190
			1220		* EXTERNAL INTERRUPT HANDLER		UCM12200
150E			1221		IFZ ADC-2		UCM12210
150E	D000	1F68	1222	XI16	STM R0,INTSAV	FOR 16-BIT PROCESSOR	UCM12220
1512	9F23		1223		ACKR R2,R3	ACKNOWLEDGE THE INTERRUPT	UCM12230
1514	D420	169A	1224		CLB R2,CONADR	FROM KEYBOARD DEVICE ?	UCM12240
1518	4330	1478	1225		BE KBINT0		UCM12250
			1226		ENDC		UCM12260
			1227		*		UCM12270
	0000	151C	1228	XI32	EQU *	FOR 32-BIT PROCESSOR	UCM12280
151C	95AA		1229		EPSR R10,R10	CAPTURE CURRENT PSW	UCM12290
151E	40A0	1686	1230		STH R10,INTPSW		UCM12300
1522	4020	1690	1231		STH R2,INTDEV	STORE INTERRUPTING DEVICE ADDRESS	UCM12310
1526	D230	1692	1232		STB R3,INTSTA	STORE INTERRUPTING DEVICE STATUS	UCM12320
152A			1233		IFZ ADC-2		UCM12330

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15B0	41F0 0F86	1287	BAL	LINK,ERRALL	'ERROR XXF4', 'DEV DDD STA SS'	UCM12870
		1288	*		'PSW PPPP LOC LLLL'	UCM12880
15B4	4300 0AEA	1289	B	OPTIN1	TO ENTER COMMAND MODE	UCM12890
		1290	*	-----		UCM12900
		1291	*	DEVICE INTERRUPTED IN WRONG INTERRUPT LEVEL		UCM12910
		1292	*			UCM12920
15B8	C860 4636	1293	LVLERR	LHI R6,C'F6'	ERROR # F6	UCM12930
15BC	4060 16FE	1294		STH R6,ERRNO		UCM12940
15C0	D3AA 16DC	1295		LB R10,HEXTAB(R10)	CONVERT TO ASCII	UCM12950
15C4	D2A0 1760	1296		STB R10,ERRLVL	AND STORE ERROR LFVEL IN MESSAGE	UCM12960
15C8	41F0 0F86	1297	BAL	LINK,ERRALL	'ERROR XXF6', 'DEV DDD STA SS'	UCM12970
		1298	*		'PSW PPPP LOC LLLL'	UCM12980
15CC	C850 174A	1299		LHI R5,INTLVL		UCM12990
15D0	4050 168E	1300		STH R5,ISITERR	SET FLAG TO OVERRIDE NOMSG OPTION	UCM13000
15D4	41F0 1190	1301	BAL	LINK,PRINT	'INTERRUPTED IN LFVEL N'	UCM13010
15D8	4300 0AEA	1302	B	OPTIN1	ENTER COMMAND MODE.	UCM13020
		1303	*	-----		UCM13030
		1304	*	SPURIOUS INTERRUPT HANDLERS		UCM13040
		1305	*			UCM13050
		1306	*			UCM13060
15DC		1307		IFZ ADC-2		UCM13070
		1308	*	FLOATING-PT ARITH FAULT INT TRAP (16 BIT PROCESSOR)		UCM13080
		1309	*			UCM13090
15DC	48E0 0028	1310	FP	LH R14,X'28'	OLD PSW (16-BIT PROCESSOR)	UCM13100
15E0	48F0 002A	1311		LH R15,X'2A'	OLD LOC	UCM13110
		1312		ENDC		UCM13120
		1313	*			UCM13130
		1314	*	RELOCATION/PROTECTION INT TRAP		UCM13140
		1315	*			UCM13150
15E4	C820 4635	1316	RP	LHI R2,C'F5'		UCM13160
15E8	4020 16FE	1317		STH R2,ERRNO	SET ERROR # F5	UCM13170
15EC	230C	1318		BS COMM		UCM13180
		1319	*			UCM13190
		1320	*	ARITHMETIC FAULT INT (32-BIT PROCESSOR) TRAP		UCM13200
15EE		1321		IFZ ADC-2		UCM13210
		1322	*	FIXED-PT DIVIDE FAULT INT (16-BIT PROCESSOR) TRAP		UCM13220
		1323		ENDC		UCM13230
		1324	*			UCM13240
15EE	C820 4631	1325	AF	LHI R2,C'F1'		UCM13250
15F2	4020 16FE	1326		STH R2,ERRNO	SET ERROR # F1	UCM13260
15F6		1327		IFZ ADC-2		UCM13270
15F6	4820 1684	1328		LH R2,M0032		UCM13280
15FA	2135	1329		BNZS COMM		UCM13290
15FC	48E0 0048	1330		LH R14,X'48'	OLD PSW (16-BIT PROCESSOR)	UCM13300
1600	48F0 004A	1331		LH R15,X'4A'	OLD LOC (16-BIT PROCESSOR)	UCM13310
		1332		ENDC		UCM13320
1604	40E0 168A	1333	COMM	STH R14,OPSW		UCM13330
1608	40F0 168E	1334		STH R15,OLOC		UCM13340
160C	4800 0A24	1335	COMM1	LH R0,PS42		UCM13350
1610	9520	1336		EPSR R2,R0	NO INT. , REG SET 15	UCM13360
1612	41F0 0F14	1337		BAL LINK,ERR	PRINT 'ERROR XXFN'	UCM13370
1616	40F0 168E	1338		STH LINK,ISITERR	FORCE PRINT	UCM13380
161A	41E0 1048	1339		BAL RET,ERRPL1	PRINT 'PSW PPPP LOC LLLL'	UCM13390

EXEC - ETPE R05P2

161E	4300	0AEA	1340	B	OPTIN1	ENTER COMMAND MODE	UCM13400
			1341	*			UCM13410
			1342	*	ILLEGAL INSTRUCTION INTERRUPT TRAP		UCM13420
			1343	*			UCM13430
1622	C820	4632	1344	II	LHI R2,C'F2'		UCM13440
1626	4020	16FE	1345		STH R2,ERRNO	SET ERROR # F2	UCM13450
162A			1346		IFZ ADC-2		UCM13460
162A	4820	1684	1347		LH R2,MOD32		UCM13470
162E	2135		1348		BNZS II32		UCM13480
1630	48E0	0030	1349		LH R14,X'30'	OLD PSW	UCM13490
1634	48F0	0032	1350		LH R15,X'32'	OLD LOC	UCM13500
			1351		ENDC		UCM13510
1638	4300	1604	1352	II32	B COMM		UCM13520
			1353	*			UCM13530
			1354	*	MACHINE MALFUNCTION INTERRUPT TRAP		UCM13540
			1355	*			UCM13550
163C	95AA		1356	MM	EPSR R10,R10	CAPTURE MMINT PSW	UCM13560
163E	C820	4633	1357		LHI R2,C'F3'		UCM13570
1642	4020	16FE	1358		STH R2,ERRNO	SET ERROR # F3	UCM13580
1646	48E0	0022	1359		LH R14,X'22'	OLD PSW (32-BIT PROCESSOR)	UCM13590
164A	48F0	0026	1360		LH R15,X'26'	OLD LOC	UCM13600
164E			1361		IFZ ADC-2		UCM13610
164E	4820	1684	1362		LH R2,MOD32		UCM13620
1652	2135		1363		BNZS MM32		UCM13630
1654	48E0	0038	1364		LH R14,X'38'	OLD PSW (16 BIT PROCESSOR)	UCM13640
1658	48F0	003A	1365		LH R15,X'3A'	OLD LOC	UCM13650
			1366		ENDC		UCM13660
165C	C4E0	FFF0	1367	MM32	NHI R14,X'FFF0'		UCM13670
1660	C4A0	000F	1368		NHI R10,X'000F'		UCM13680
1664	06EA		1369		OAR R14,R10		UCM13690
1666	40E0	168A	1370		STH R14,OPSW		UCM13700
166A	40F0	168E	1371		STH R15,OLOC		UCM13710
166E			1372		IFZ ADC-2		UCM13720
166E	C810	7FFF	1373		LHI R1,X'7FFF'		UCM13730
1672	2711		1374	MM16	SIS R1,1		UCM13740
1674	2021		1375		BPS MM16		UCM13750
			1376		ENDC		UCM13760
1676	C800	080F	1377		LHI R0,X'080F'		UCM13770
167A	9104		1378		SLHLS R0,4	R0 = X'80F0'	UCM13780
167C	9520		1379		EPSR R2,R0	HALT PROCESSOR	UCM13790
			1380	*			UCM13800
			1381	*	WHEN EXE/RUN IS DEPRESSED, ERROR MSG IS PRINTED.		UCM13810
			1382	*			UCM13820
167E	4300	160C	1383	B	COMM1		UCM13830
			1384	*	*****		UCM13840
			1385	*	ETPE CONSTANTS & TABLES		UCM13850
			1386	*			UCM13860
1682	0000		1387	FIRST	DCX 0		UCM13870
1684	0000		1388	MOD32	DCX 0	FLAG FOR 32-BIT M/C (NON-ZERO)	UCM13880
1686	0000		1389	INTPSW	DCX 0	(FOR 32-BIT M/C ONLY)	UCM13890
1688			1390		ALIGN 8		UCM13900
			1391	*	-----		UCM13910
1688	0000		1392	OPSW32	DCX 0	OLD PSW STORAGE AREA	UCM13920

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168A	0000	1393	OPSW	DCX	0		UCM13930
168C	0000	1394		DCX	0		UCM13940
168E	0000	1395	QLOC	DCX	0		UCM13950
		1396	*	-----			UCM13960
1690	0000	1397	INTDEV	DCX	0	INTERRUPTING DEV ADR	UCM13970
	0000 1690	1398	ERRDEV	EQU	INTDEV	ERROR DEVICE #	UCM13980
1692	00	1399	INTSTA	DB	0	INTERRUPTING DEV STATUS	UCM13990
	0000 1692	1400	ERRSTA	EQU	INTSTA	ERRONEOUS STATUS	UCM14000
1693	00	1401	SINK	DB	0	BIT BUCKET	UCM14010
1694	80	1402	NORM	DB	X'80'		UCM14020
1695	40	1403	INCR	DB	X'40'		UCM14030
1696		1404		DB	*		UCM14040
1696	0000	1405	PASFLG	DCX	0	SET WHEN CONSOLE ON PASLA/PALM	UCM14050
1698	0000	1406	PASFLG2	DCX	0	SET WHEN LIST DEVICE ON PASLA	UCM14060
		1407	*	-----			UCM14070
		1408	*	ETPE IO COMMANDS			UCM14080
		1409	*				UCM14090
169A	0000	1410	CONADR	DCX	0	CONSOLE DEVICE ADDRESS	UCM14100
		1411	*				UCM14110
169C	0000	1412	CONRD	DCX	0	CONSOLE READ/WRITE COMMANDS	UCM14120
	0000 169D	1413	CONWRT	EQU	CONRD+1		UCM14130
169E	B9AB	1414	CRTRD	DCX	B9AB	FOR CRT	UCM14140
16A0	A4D8	1415	CLIFRD	DCX	A4D8	* CURRENT LOOP INTERFACE	UCM14150
16A2	0080	1416	LPWRT	DCX	0080	* LINE PRINTER	UCM14160
16A4	A9AB	1417	CARRD	DCX	A9AB	* CAROUSEL 300	UCM14170
16A6	8202	1418	MREADC	DCX	8202	* MICROBUS	UCM14180
		1419	*				UCM14190
16A8	0000	1420	CON2ND	DCX	0	2ND COMMAND; ENABLE READ COMMAND	UCM14200
	0000 16A9	1421	CONENRD	EQU	CON2ND+1		UCM14210
16AA	F879	1422	CRT2ND	DCX	F879	FOR CRT	UCM14220
16AC	0064	1423	CLIF2ND	DCX	0064	* CURRENT LOOP INTERFACE	UCM14230
16AE	0000	1424		DCX	0	* DUMMY HW FOR LP	UCM14240
16B0	F069	1425	CAR2ND	DCX	F069	* CAROUSEL 300	UCM14250
16B2	9292	1426		DCX	9292	* FOR MICROBUS	UCM14260
		1427	*				UCM14270
16B4	00	1428	CONRQ2S	DB	0	CONSOLE REQUEST TO SEND CMD	UCM14280
16B5	3B	1429	CRTRQ2S	DB	X'3B'	FOR CRT	UCM14290
16B6	00	1430		DB	0	* DUMMY BYTE FOR CLI	UCM14300
16B7	00	1431		DB	0	* DUMMY BYTE FOR LP	UCM14310
16B8	23	1432	CARRQ2S	DB	X'23'	* CAROUSEL 300	UCM14320
16B9	00	1433		DB	0	* DUMMY BYTE FOR MICROBUS	UCM14330
16BA		1434		DB	*		UCM14340
		1435	*	-----			UCM14350
16BA	14FC	1436	KBINT	DC	Z(RETOPSW)	KEYBOARD INT RETURN ADR	UCM14360
16BC	0000	1437	BRKVECT	DC	Z(0)	BREAK KEY VECTOR	UCM14370
16BE	0000	1438	ISITERR	DCX	0		UCM14380
16C0	0000	1439	NOERR	DCX	0		UCM14390
16C2	0000	1440	SELTST	DCX	0	HIGHEST SELECTED TEST #	UCM14400
16C4	0000	1441	WASDU	DCX	0	1 IF KEYBOARD DEVICE WAS OFF	UCM14410
16C6	0000	1442	WASDU1	DCX	0	NON-ZERO IF TOTAL.TOTERR TO PRINT	UCM14420
16C8	0000	1443	TOTAL	DCX	0	# OF TIMES THE SELECTED TESTS RUN	UCM14430
16CA	0000	1444	TOTERR	DCX	0	TOTAL ERRORS DETECTED WHILE DU	UCM14440
16CC	0000	1445	BTESTNO	DCX	0	CURRENT TEST # IN BINARY	UCM14450

EXEC - ETPE R03P2

16CE	0000			1446	COUNT	UCX	0			UCM14460
16D0	0000			1447	NEXTST	DCX	0	NEXT TEST #		UCM14470
				1448	*					UCM14480
16D2	0001			1449	DECTAB	DC	1,10,100,1000,10000			UCM14490
16D4	000A									
16D6	0064									
16D8	03E8									
16DA	2710									
16DC	3031 3233 3435 3637			1450	HEXTAB	DB	C'0123456789ABCDEF'			UCM14500
16E4	3839 4142 4344 4546									
				1451	*-----*					UCM14510
				1452	* ETPE MESSAGES					UCM14520
				1453	*					UCM14530
16EC	5445 5354 2020 2A2A			1454	TSTMSG	DC	C'TEST **',X'0000'			UCM14540
16F4	0D00									
	0000 16F2			1455	MTESTNO	EQU	*-4			UCM14550
16F6	4552 524F 5220 2A2A			1456	ERRMSG	DC	C'ERROR ****',X'0000'			UCM14560
16FE	2A2A									
1700	0D00									
	0000 16FC			1457	ETESTNO	EQU	*-6	STORED BY ETPE		UCM14570
	0000 16FE			1458	ERRNO	EQU	*-4	STORE ERRNO AS CHAR CONSTANT		UCM14580
1702	544F 5441 4C20 2020			1459	TOTMSG	DC	C'TOTAL TOTERR',X'0000'			UCM14590
170A	544F 5445 5252									
1710	0D00									
1712	4E4F 2045 5252 4F52			1460	NOERMSG	DC	C'NO ERROR',X'0000'			UCM14600
171A	0D00									
171C	4445 5620 2A2A 2A20			1461	DEVMSG	DC	C'DEV *** STA **',X'0000'			UCM14610
1724	5354 4120 2A2A									
172A	0D00									
	0000 1720			1462	ASCIDEV	EQU	*-12			UCM14620
	0000 1724			1463	STAMSG	EQU	*-8			UCM14630
	0000 1726			1464	ASCISTA	EQU	*-4			UCM14640
172C	4445 5620 2A2A 2A20			1465	DEVMSG2	DC	C'DEV ****',X'0000'			UCM14650
1734	0D00									
	0000 1730			1466	ASCIDEV2	EQU	*-6			UCM14660
1736	5053 5720 2A2A 2A2A			1467	PSWMSG	DC	C'PSW **** LOC ****',X'0000'			UCM14670
173E	2020 4C4F 4320 2A2A									
1746	2A2A									
1748	0D00									
	0000 173A			1468	ASCIPSW	EQU	*-16			UCM14680
	0000 1740			1469	LOCMSG	EQU	*-10			UCM14690
	0000 1744			1470	ASCILCC	EQU	*-6			UCM14700
174A	494E 5445 5252 5550			1471	INTLVLM	DC	C'INTERRUPTED IN LEVEL **',X'0000'			UCM14710
1752	5445 4420 494E 204C									
175A	4556 454C 2020 2A20									
1762	0D00									
	0000 1760			1472	ERRLVL	EQU	*-4			UCM14720
1764	454E 4420 4F46 2054			1473	EOTMSG	DC	C'END OF TEST',X'0000'			UCM14730
176C	4553 5420									
1770	0D00									
1772	3F0D			1474	GMSG	DC	X'3F0D'			UCM14740
1774	2A0D			1475	AMSG	DC	X'2A0D'			UCM14750

EXEC - ETPE R03P2

				1477	*-----			UCM14770
				1478	* OPTION/COMMAND TABLE			UCM14780
				1479	*			UCM14790
	0000	1776		1480	OPT	EQU	*	UCM14800
1776	5445	5354	2020	1481	TEST	DC	C'TEST ',X'FF00',X'0000',X'0000'	UCM14810
177C	FF00							
177E	0000							
1780	0000							
1782	4C4F	4F50	2020	1482	LOOP	DC	C'LOOP ',X'0000',X'0000',X'0000'	UCM14820
1788	0000							
178A	0000							
178C	0000							
178E	434F	4E54	494E	1483	CONTIN	DC	C'CONTIN',X'0000',Z(ZERONE),X'0000'	UCM14830
1794	0000							
1796	0CA8							
1798	0000							
179A	4E4F	4D53	4720	1484	NOMSG	DC	C'NOMSG ',X'0000',Z(ZERONE),X'0000'	UCM14840
17A0	0000							
17A2	0CA8							
17A4	0000							
17A6	494E	544C	4556	1485	INTLEV	DC	C'INTLEV',X'0000',Z(LEVEL),X'0000'	UCM14850
17AC	0000							
17AE	0CB8							
17B0	0000							
17B2	5449	4D56	414C	1486	TIMVAL	DC	C'TIMVAL',X'0002',X'0000',X'0000'	UCM14860
17B8	00D2							
17BA	0000							
17BC	0000							
17BE	4445	5641	4452	1487	DEVADR	DC	C'DEVADR',X'6C',ADR,0	UCM14870
17C4	006C							
17C6	0CB0							
17C8	0000							
17CA	485A	2020	2020	1488	HZ	DC	C'HZ ',X'60',0,0	UCM14880
17D0	0060							
17D2	0000							
17D4	0000							
				1489	*			UCM14890
	0000	17D6		1490	OPTEND2	EQU	*	UCM14900
	0000	17D6		1491	OPTEND	EQU	*	UCM14910
17D6	4F50	5449	4F4E	1492	OPTION	DC	C'OPTION',0,0,0	UCM14920
17DC	0000							
17DE	0000							
17E0	0000							
17E2	5255	4E20	2020	1493	RUN	DC	C'RUN ',0,0,0	UCM14930
17E8	0000							
17EA	0000							
17EC	0000							
17EE	FFFF			1494		DCX	FFFF	UCH14940
				1495	*			UCH14950
				1496	* *****			UCH14960
				1497	*			UCH14970
17F0	FF00			1498	DEFTTESTS	DCX	FF00,0000	UCH14980
17F2	0000							

END OF PRINTING OPTIONS

EXEC - ETPE R03P2

17F4	0007		1499	MAXTST	DCX	7		UCM14990		
			1500	*				UCM15000		
17F6	1896		1501	TEST5	DC	TEST0		UCM15010		
17F8	191C		1502		DC	TEST1		UCM15020		
17FA	1982		1503		DC	TEST2		UCM15030		
17FC	1A04		1504		DC	TEST3		UCM15040		
17FE	1A4C		1505		DC	TEST4		UCM15050		
1800	1A8C		1506		DC	TEST5		UCM15060		
1802	1AD8		1507		DC	TEST6		UCM15070		
1804	18E2		1508		DC	TEST7		UCM15080		
			1509	*				UCM15090		
1806	434F	4040	4F4E	2055	1510	TITLE	DC	C'COMMON UNIVERSAL CLOCK MODULE TEST 06-133R05'	UCM15100	
180E	4E49	5645	5253	414C						
1816	2043	4C4F	4348	204D						
181E	4F44	554C	4520	5445						
1826	5354	2030	362D	3133						
182E	3352	3035								
1832	0D0A		1511		DCX	D0A		UCM15110		
			1512	*				UCM15120		
1834	494E	4954	2043	4F55	1513	COUNTMSG	DC	C'INIT COUNT '	UCM15130	
183C	4E54	2020								
1840	2A2A	2A2A	2020		1514	INTASC	DC	C'**** '	UCM15140	
1846	5052	4553	2043	4F55	1515	CNTMSG1	DC	C'PRES COUNT '	UCM15150	
184E	4E54	2020								
1852	2A2A	2A2A	2020		1516	PRESASC	DC	C'**** '	UCM15160	
1858	0D0A				1517		DCX	D0A	UCM15170	
185A	4249	5453	2053	4554	1518	BITMSG	DC	C'BITS SET'	UCM15180	
1862	202A				1519	ASCBIT	DC	C' *'	UCM15190	
1864	0D0A				1520		DCX	D0A	UCM15200	
1866	4558	5020			1521	ASCMSG	DC	C'EXP '	UCM15210	
186A	2A2A	2A20			1522	ASCEXP	DC	C'*** '	UCM15220	
186E	0D0A				1523		DCX	D0A	UCM15230	
1870	4C4F	4144	4544	2020	1524	LOADMSG	DC	C'LOADED '	UCM15240	
1878	2A2A	2A2A	2020		1525	LOADASC	DC	C'**** '	UCM15250	
187E	5245	4144	2020		1526		DC	C'READ '	UCM15260	
1884	2A2A	2A2A			1527	RDASC	DC	C'****'	UCM15270	
1888	0D0A				1528		DCX	D0A	UCM15280	
					1529	*			UCM15290	
					1530	* *****			UCM15300	
	0000	188A			1531	DEVSADR	EQU	*	INTERRUPTING DEVICE TABLE	UCM15310
					1532	*			UCM15320	
188A	0000				1533	PREC	DCX	0	PRECISION INTERVAL CLOCK ADDRESS.	UCM15330
	0000	0004			1534	PIC	EQU	4		UCM15340
188C	0000				1535	LINE	DCX	0	LINE FREQUENCY CLOCK ADDRESS.	UCM15350
	0000	0005			1536	LFC	EQU	5		UCM15360
188E	FFFF				1537		DCX	FFFF		UCM15370
1890					1538	INTLVL	DO	2	EXPECTED INTERRUPT LEVELS FOR ABOVE	UCM15380
1890	00				1539		DB	0		UCM15390
1891	00				1539		DB	0		
					1540	*				UCM15400
	0000	1892			1541	DEVINT	EQU	*	INTERRUPT HANDLER VECTORS	UCM15410
1892	0000				1542	HDLR0	DCX	0	FOR PIC	UCM15420
1894	0000				1543	HDLR1	DCX	0	FOR LFC	UCM15430

COMMON UNIVERSAL CLOCK MODULE TEST 06-133R05M96A13

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EXEC - ETPE R03P2

1544 *

UCM15440

TEST 0

UCM15

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1546 * *****
1547 *
1548 *           T E S T 0
1549 *
1550 * PURPOSE OF TEST:
1551 * TEST 0 VERIFIES THAT THE PRECISION INTERVAL CLOCK (PIC) AND LINE
1552 * FREQUENCY CLOCK (LFC) DO NOT GENERATE INTERRUPTS WHILE DISABLED
1553 * OR DISARMED.
1554 *
1555 * ASSUMPTIONS:
1556 * IT IS ASSUMED THAT THE PROCESSOR, MEMORY, AND TELETYPE TESTS HAVE
1557 * BEEN RUN PRIOR TO SELECTING THIS TEST.
1558 *
1559 * DESIGN SPECIFICATIONS:
1560 * INTERRUPTS FROM BOTH THE PIC AND THE LFC ARE DISARMED. PROCESSOR
1561 * INTERRUPTS ARE ENABLED, A COMMAND 'START' IS ISSUED TO THE PIC,
1562 * TOGETH WITH 'DISARM'. AFTER A SOFTWARE DELAY, THE PIC CURRENT
1563 * DELAYS 12 TO 15 MILLISECONDS TO ENSURE THAT NO INTERRUPT IS
1564 * GENERATED. THE TEST IS THEN REPEATED WITH CLOCK INTERRUPTS DISABLED.
1565 *
1566 * HOW TO RUN THE TEST:
1567 * ENTER APPROPRIATE VALUES FOR THE TIMVAL AND DEVADR OPTIONS. SELECT
1568 * THE TEST, AND ENTER 'RUN'. NO MANUAL INTERVENTION IS REQUIRED.
1569 *
1570 * OPTIONS:
1571 * LOOP, CONTIN, DEVADR, INTLEV, TIMVAL
1572 *
1573 * ERRORS:
1574 * 01,02
1575 *
1576 *
1577 TEST0 EQU *
1578 *
1579 LH PIC,PREC GET DEVICE ADDRESSES.
1580 LH LFC,LINE
1581 *
1582 LHI R0,TOINT INTERRUPT VECTOR
1583 STH R0,HDLR0
1584 STH R0,HDLR1
1585 LIS R0,0
1586 STH R0,EXPDEV INITIALIZE
1587 *
1588 OC PIC,DISARM
1589 OC LFC,DISARM
1590 BAL LINK,DELAY SHOULD NOT INTERRUPT.
1591 WH PIC,RIC1384 1 USEC RES, 900 (0.9 MSEC) INTERVAL
1592 OC PIC,STDSM START, DISARM
1593 BAL LINK,DELAY SHOULD NOT INTERRUPT
1594 RH PIC,CURCOUNT READ DECREMENTED COUNT.
1595 *
1596 LH R1,RIC1384
1597 NHI R1,X'0FFF'
1598 SH R1,CURCOUNT

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UCM15460
UCM15470
UCM15480
UCM15490
UCM15500
UCM15510
UCM15520
UCM15530
UCM15540
UCM15550
UCM15560
UCM15570
UCM15580
UCM15590
UCM15600
UCM15610
UCM15620
UCM15630
UCM15640
UCM15650
UCM15660
UCM15670
UCM15680
UCM15690
UCM15700
UCM15710
UCM15720
UCM15730
UCM15740
UCM15750
UCM15760
UCM15770
UCM15780
UCM15790
UCM15800
UCM15810
UCM15820
UCM15830
UCM15840
UCM15850
UCM15860
UCM15870
UCM15880
UCM15890
UCM15900
UCM15910
UCM15920
UCM15930
UCM15940
UCM15950
UCM15960
UCM15970
UCM15980

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TEST 0

UCM15

18D8	2123	1599	BPS	TST0.1	COUNT DECREMENTED ?	UCM15990
18DA	41F0 1C8A	1600	BAL	R15,TT02	ERROR 02 - COUNT NOT DECREMENTED	UCM16000
		1601	*			UCM16010
18DE	DE50 1EB3	1602	TST0.1	OC	LFC,DISABLE	UCM16020
18E2	DE40 1EB2	1603	OC	PIC,STDSB	START, DISABLE	UCM16030
18E6	41F0 1E5E	1604	BAL	LINK,DELAY	SHOULD NOT INTERRUPT.	UCM16040
		1605	*			UCM16050
18EA	D940 1ECA	1606	RH	PIC,CURCOUNT		UCM16060
18EE	4810 1EB8	1607	LH	R1,RIC1384		UCM16070
18F2	C410 0FFF	1608	NHI	R1,X'0FFF'		UCM16080
18F6	4B10 1ECA	1609	SH	R1,CURCOUNT		UCM16090
18FA	2123	1610	BPS	TST0.2	COUNT DECREMENTED ?	UCM16100
18FC	41F0 1C8A	1611	BAL	R15,TT02	ERROR 02 - COUNT NOT DECREMENTED	UCM16110
	0000 1900	1612	TST0.2	EQU	*	UCM16120
1900	4300 0E28	1613	TOEND	B	TSTEND	UCM16130
		1614	*			UCM16140
		1615	*			UCM16150
	0000 1904	1616	TOINT	EQU	*	UCM16160
1904	4800 1690	1617	LH	R0,INTDEV	ALLOWS ONE INTERRUPT FROM EACH CLOCK	UCM16170
1908	4500 1EC0	1618	CLH	R0,EXPDEV	DID THIS INTERRUPT BEFORE ?	UCM16180
190C	4000 1EC0	1619	STH	R0,EXPDEV	YES.	UCM16190
1910	4330 0E28	1620	BE	TSTEND	ERROR 01 - INTERRUPT WHILE	UCM16200
1914	41F0 1C52	1621	BAL	R15,TT01	. DISABLED OR DISARMED.	UCM16210
		1622	*		CONTINUE TEST.	UCM16220
1918	4300 14FC	1623	B	RETOPSW		UCM16230
		1624	*			UCM16240

TEST 1

		1626	*	*****		UCM16260
		1627	*			UCM16270
		1628	*	TEST 1		UCM16280
		1629	*			UCM16290
		1630	*	PURPOSE OF TEST:		UCM16300
		1631	*	TEST 1 VERIFIES THAT INDIVIDUAL COUNT BITS IN THE PIC RESOLUTION AND		UCM16310
		1632	*	INITIAL COUNT (RIC) REGISTER CAN BE LOADED CORRECTLY.		UCM16320
		1633	*			UCM16330
		1634	*	ASSUMPTIONS:		UCM16340
		1635	*	IT IS ASSUMED THAT THE PROCESSOR, MEMORY, AND TELETYPE TESTS HAVE		UCM16350
		1636	*	BEEN RUN PRIOR TO SELECTING THIS TEST.		UCM16360
		1637	*			UCM16370
		1638	*	DESIGN SPECIFICATIONS:		UCM16380
		1639	*	CLOCK INTERRUPTS ARE DISABLED, A ONE-MILLISECOND RESOLUTION IS		UCM16390
		1640	*	SELECTED, AND THE LEAST SIGNIFICANT INITIAL COUNT BIT IS SET.		UCM16400
		1641	*	A COMMAND 'START' IS ISSUED TO THE PIC, AND THE CURRENT INTERVAL		UCM16410
		1642	*	COUNT (CIC) IS IMMEDIATELY READ TO SEE THAT THE CIC WAS LOADED FROM		UCM16420
		1643	*	THE RIC CORRECTLY. THE TEST IS REPEATED UNTIL EACH COUNT BIT HAS		UCM16430
		1644	*	BEEN TESTED.		UCM16440
		1645	*			UCM16450
		1646	*	HOW TO RUN THE TEST:		UCM16460
		1647	*	ENTER APPROPRIATE VALUES FOR THE TIMVAL AND DEVADR OPTIONS, SELECT		UCM16470
		1648	*	THE TEST, AND ENTER 'RUN'. NO MANUAL INTERVENTION IS REQUIRED.		UCM16480
		1649	*			UCM16490
		1650	*	OPTIONS:		UCM16500
		1651	*	LOOP, CONTIN, DEVADR, INTLEV, TIMVAL		UCM16510
		1652	*			UCM16520
		1653	*	ERRORS:		UCM16530
		1654	*	0B		UCM16540
		1655	*			UCM16550
		1656	*			UCM16560
	0000 191C	1657	TEST1	EQU *		UCM16570
		1658	*			UCM16580
	191C 4840 188A	1659	LH	PIC,PREC	GET DEVICE ADDRESSES	UCM16590
	1920 4850 188C	1660	LH	LFC,LINE		UCM16600
	1924 DE40 1EAF	1661	OC	PIC,DISARM		UCM16610
	1928 DE50 1EAF	1662	OC	LFC,DISARM		UCM16620
		1663	*			UCM16630
	192C 2400	1664	LIS	RO,0		UCM16640
	192E 4000 1ECC	1665	STH	RO,EXPDEV	IN THE EVENT OF UNEXP. INTPT.	UCM16650
	1932 2411	1666	LIS	R1,1		UCM16660
	1934 4010 1ECC	1667	TST1.1	STH	R1,PATSAV	UCM16670
	1938 4810 1ECC	1668	LH	R1,PATSAV		UCM16680
	193C C801 8000	1669	LHI	RO,X'8000'(R1)	1 MSEC RESOLUTION	UCM16690
	1940 9840	1670	WHR	PIC,RO	CURRENT PIC	UCM16700
	1942 DE40 1EB2	1671	OC	PIC,STDSB	START, DISABLE	UCM16710
	1946 D940 1ECA	1672	RH	PIC,CURCOUNT	READ COUNT	UCM16720
	194A 4800 1ECC	1673	LH	RO,PATSAV		UCM16730
	194E C400 0FFF	1674	NHI	RO,X'0FFF'		UCM16740
	1952 4500 1ECA	1675	CLH	RO,CURCOUNT		UCM16750
	1956 2333	1676	BES	TST1.2		UCM16760
	1958 41F0 1DB6	1677	BAL	R15,TT0B	ERROR 0B - COUNT NOT LOADED PROP'LY.	UCM16770
	195C 4810 1ECC	1678	TST1.2	LH	R1,PATSAV	UCM16780

TEST 1

1960	9111	1679	SLLS	R1,1	SELECT NEXT COUNT BIT	UCM16790
1962	C510 1000	1680	CLHI	R1,X'1000'		UCM16800
1966	4280 1934	1681	BL	TST1.1		UCM16810
		1682	*			UCM16820
196A	4810 1ECC	1683	LH	R1,PATSAV	NOW SET ANOTHER BIT.	UCM16830
196E	9011	1684	TST1.3	SRLS	R1,1	UCM16840
1970	2281	1685	BFBS	8,1	CARRY ?	UCM16850
1972	9112	1686	SLLS	R1,2	YES.	UCM16860
1974	2613	1687	AIS	R1,3	RESET BIT & ADD ANOTHER.	UCM16870
1976	C510 1000	1688	CLHI	R1,X'1000'		UCM16880
197A	4280 1934	1689	BL	TST1.1	NOW SHIFT THIS PATTERN.	UCM16890
197E	4300 0E28	1690	T1END	B		UCM16900
		1691	*			UCM16910

TEST 2

		1693	*	*****		UCM16930
		1694	*			UCM16940
		1695	*	TEST 2		UCM16950
		1696	*			UCM16960
		1697	*	PURPOSE OF TEST:		UCM16970
		1698	*	TEST 2 VERIFIES THAT THE PIC IS CAPABLE OF INTERRUPTING FOR EACH		UCM16980
		1699	*	SELECTABLE RESOLUTION.		UCM16990
		1700	*			UCM17000
		1701	*	ASSUMPTIONS:		UCM17010
		1702	*	IT IS ASSUMED THAT THE PROCESSOR, MEMORY, AND TELETYPE TESTS HAVE		UCM17020
		1703	*	BEEN RUN PRIOR TO SELECTING THIS TEST.		UCM17030
		1704	*			UCM17040
		1705	*	DESIGN SPECIFICATIONS:		UCM17050
		1706	*	CLOCK INTERRUPTS ARE DISABLED, A ONE-MICROSECOND RESOLUTION, AND AN		UCM17060
		1707	*	INTERVAL OF TWO ARE SELECTED. PIC INTERRUPTS ARE ENABLED, AND A		UCM17070
		1708	*	COMMAND 'START' IS ISSUED. PROCESSOR INTERRUPTS ARE ENABLED, AND		UCM17080
		1709	*	THE PROGRAM DELAYS 12 TO 15 MILLISECONDS. WHEN THE PIC INTERRUPTS.		UCM17090
		1710	*	THE TEST IS REPEATED, UNTIL ALL RESOLUTION BITS HAVE BEEN TESTED.		UCM17100
		1711	*			UCM17110
		1712	*	HOW TO RUN THE TEST:		UCM17120
		1713	*	ENTER APPROPRIATE VALUES FOR THE TIMVAL AND DEVADR OPTIONS. SELECT		UCM17130
		1714	*	THE TEST, AND ENTER 'RUN'. NO MANUAL INTERVENTION IS REQUIRED.		UCM17140
		1715	*			UCM17150
		1716	*	OPTIONS:		UCM17160
		1717	*	LOOP, CONTIN, DEVADR, INTLEV, TIMVAL		UCM17170
		1718	*			UCM17180
		1719	*	ERRORS:		UCM17190
		1720	*	03,04		UCM17200
		1721	*			UCM17210
		1722	*			UCM17220
		1723	TEST2	EQU *		UCM17230
		1724		LH PIC,PREC		UCM17240
		1725		STH PIC,EXPDEV		UCM17250
		1726		LH LFC,LINE		UCM17260
		1727		OC PIC,DISARM	DISARM INTERRUPTS	UCM17270
		1728		OC LFC,DISABLE		UCM17280
		1729	*			UCM17290
		1730		LHI R0,T2INT	INTERRUPT VECTORS	UCM17300
		1731		STH R0,HDLR0		UCM17310
		1732		STH R0,HDLR1		UCM17320
		1733	*			UCM17330
		1734		LHI R0,X'1000'	LEAST SIGNIFICANT RESOLUTION BIT	UCM17340
		1735		AIS R0,2	INTERVAL = 2	UCM17350
		1736	TST2.1	STH R0,PATSAV	SAVE RIC	UCM17360
		1737		LIS R0,0		UCM17370
		1738		STH R0,FSTINT		UCM17380
		1739		WH PIC,PATSAV	AND WRITE TO CLOCK	UCM17390
		1740		OC PIC,STEN	START CLOCK, ENAB INTPTS	UCM17400
		1741		BAL LINK,DELAY	SHOULD INTERRUPT	UCM17410
		1742		BAL R15,TT03	ERROR 03 - NO INTERRUPT.	UCM17420
		1743	*			UCM17430
		1744	TST2.2	LH R0,PATSAV	TRY WITH NEXT SELECTABLE RESOLUTION	UCM17440
		1745		CLHI R0,X'F002'	MAX. ATTAINED ?	UCM17450
1982	0000 1982					
1986	4840 188A					
198A	4040 1EC0					
198E	4850 188C					
1992	DE40 1EAF					
1996	DE50 1EB3					
199A	C800 19D8					
199E	4000 1894					
19A2	C800 1000					
19A6	2602					
19AA	4000 1ECC					
19AE	2400					
19B2	4000 1EC2					
19B6	0840 1ECC					
19BA	DE40 1EB0					
19BE	41F0 1E5E					
19C2	41F0 1CC6					
19C6	4800 1ECC					
	C500 F002					

TEST 3

```

1766 * *****
1767 *
1768 *           T E S T  3
1769 *
1770 * PURPOSE OF TEST:
1771 * TEST 3 VERIFIES THAT THE PIC OVERFLOW STATUS BIT CAN BE SET AND
1772 * RESET UNDER PROGRAM CONTROL.
1773 *
1774 * ASSUMPTIONS:
1775 * IT IS ASSUMED THAT THE PROCESSOR, MEMORY, AND TELETYPE TESTS HAVE
1776 * BEEN RUN PRIOR TO SELECTING THIS TEST.
1777 *
1778 * DESIGN SPECIFICATIONS:
1779 * CLOCK INTERRUPTS ARE DISABLED, A ONE-MICROSECOND RESOLUTION AND
1780 * AN INTERVAL OF ZERO ARE SELECTED. A COMMAND 'START' IS ISSUED.
1781 * FOLLOWED BY A SINGLE WRITE DATA. THE OVERFLOW STATUS BIT IS TESTED
1782 * BY A SENSE STATUS INSTRUCTION. IT SHOULD BE SET. A SECOND SENSE
1783 * STATUS IS EXECUTED TO TEST THAT THE OVERFLOW STATUS BIT WAS RESET
1784 * BY THE FIRST SENSE STATUS INSTRUCTION.
1785 *
1786 * HOW TO RUN THE TEST:
1787 * ENTER APPROPRIATE VALUES FOR THE TIMVAL AND DEVADR OPTIONS. SELECT
1788 * THE TEST, AND ENTER 'RUN'. NO MANUAL INTERVENTION IS REQUIRED.
1789 *
1790 * OPTIONS:
1791 * LOOP, CONTIN, DEVADR, INTLEV, TIMVAL
1792 * ERRORS:
1793 * 05.0E
1794 *
1795 *
1796 TEST3  EQU  *
1797         LH  PIC,PREC
1798         LH  LFC,LINE
1799 *
1800         OC  PIC,DISABLE
1801         OC  LFC,DISABLE
1802         WD  PIC,RIC1000      1 USEC RES, 0 (USEC) INTERVAL
1803         WD  PIC,RIC1000+1
1804         SSR PIC,R3          TO RESET OVERFLOW IBT
1805         OC  PIC,STDSM      START & DISARM (X'E0')
1806         WD  PIC,RIC1000
1807         SRLS R0,15        DELAY - FORCE OVERFLOW.
1808         WD  PIC,RIC1000+1
1809         SSR PIC,R3
1810         STH R3,TEMPSTA
1811         BTC 8,TST3.1
1812         BAL R15,TT05     ERROR 03 - OVERFLOW STATUS NOT SET.
1813 *
1814 TST3.1  SSR  PIC,R3      WAS OVERFLOW BIT RESET BY SSR?
1815         STH R3,TEMPSTA
1816         BFC 8,T3END
1817         BAL R15,TT0E     ERROR 0E - OVERFLOW NOT RESET BY SSR
1818 T3END   B      TSTEND

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0000	1A04	
1A04	4840	186A
1A08	4850	188C
1A0C	DE40	1EB3
1A10	DE50	1EB3
1A14	DA40	1EB6
1A18	DA40	1EB7
1A1C	9D43	
1A1E	DE40	1EB1
1A22	DA40	1EB6
1A26	900F	
1A28	DA40	1EB7
1A2C	9D43	
1A2E	4030	1ECE
1A32	4280	1A3A
1A36	41F0	1D28
1A3A	9D43	
1A3C	4030	1ECE
1A40	4380	1A48
1A44	41F0	1E16
1A48	4300	0E28

TEST 3

1019 *

UCM18190

TEST 4

	1821	*	*****		UCM18210
	1822	*			UCM18220
	1823	*	TEST 4		UCM18230
	1824	*			UCM18240
	1825	*	PURPOSE OF TEST:		UCM18250
	1826	*	TEST 4 VERIFIES THAT THE LINE FREQUENCY CLOCK (LFC) IS CAPABLE OF		UCM18260
	1827	*	INTERRUPTING.		UCM18270
	1828	*			UCM18280
	1829	*	ASSUMPTIONS:		UCM18290
	1830	*	IT IS ASSUMED THAT THE PROCESSOR, MEMORY, AND TELETYPE TESTS HAVE		UCM18300
	1831	*	BEEN RUN PRIOR TO SELECTING THIS TEST.		UCM18310
	1832	*			UCM18320
	1833	*	DESIGN SPECIFICATIONS:		UCM18330
	1834	*	PIC INTERRUPTS ARE DISABLED AND LFC INTERRUPTS ENABLED. PENDING		UCM18340
	1835	*	INTERRUPTS ARE CLEARED; PROCESSOR INTERRUPTS ARE ENABLED.		UCM18350
	1836	*	THE PROGRAM THEN DELAYS 12 TO 15 MILLISECONDS WAITING FOR AN		UCM18360
	1837	*	INTERRUPT. WHEN THE LFC INTERRUPTS, THE DEVICE ADDRESS IS CHECKED.		UCM18370
	1838	*	IF THE LFC ADDRESS WAS RETURNED, THE TEST TERMINATES. IF THE LFC DOFS		UCM18380
	1839	*	NOT INTERRUPT, OR IF THE WRONG ADDRESS IS RETURNED, AN ERROR MESSAGE		UCM18390
	1840	*	IS PRINTED.		UCM18400
	1841	*			UCM18410
	1842	*	HOW TO RUN THE TEST:		UCM18420
	1843	*	ENTER APPROPRIATE VALUES FOR THE TIMVAL AND DEVADR OPTIONS, SELECT		UCM18430
	1844	*	THE TEST, AND ENTER 'RUN'. NO MANUAL INTERVENTION IS REQUIRED.		UCM18440
	1845	*			UCM18450
	1846	*	OPTIONS:		UCM18460
	1847	*	LOOP, CONTIN, DEVADR, INTLEV, TIMVAL		UCM18470
	1848	*			UCM18480
	1849	*	ERRORS:		UCM18490
	1850	*	06.07		UCM18500
	1851	*			UCM18510
	1852	*			UCM18520
	1853	TEST4	EQU *		UCM18530
1A4C	0000 1A4C		LH PIC.PREC		UCM18540
1A50	4840 188A		LH LFC.LINE		UCM18550
	1855				UCM18560
	1856	*			UCM18570
1A54	4050 1EC0		STH LFC.EXPDEV		UCM18580
1A58	C800 1A78		LHI R0,T4INT	INTERRUPT VECTOR	UCM18590
1A5C	4000 1892		STH R0,HDLR0		UCM18600
1A60	4000 1894		STH R0,HDLR1		UCM18610
	1861	*			UCM18620
1A64	DE40 1EB3		OC PIC.DISABLE		UCM18630
1A68	DE50 1EAE		OC LFC.ENABLE		UCM18640
1A6C	41F0 1E5E		BAL LINK,DELAY	SHOULD INTERRUPT (LFC)	UCM18650
	1865	*			UCM18660
1A70	41F0 1D3C		BAL R15,TT06	ERROR 06- NO INTPT BY LFC	UCM18670
1A74	4300 0E28		T4END B TSTEND		UCM18680
	1868	*			UCM18690
1A78	4800 1690		T4INT LH R0,INTDEV		UCM18700
1A7C	4500 188C		CLH R0.LINE	DID LFC INTERRUPT?	UCM18710
1A80	4330 1A74		BE T4END		UCM18720
1A84	41F0 1D50		BAL R15,TT07	ERROR 07 - LFC INTERRUPT W/PIC ADDR.	UCM18730
1A88	4300 1A74		B T4END		

TEST 4

1874 *

UCM18740

TEST 5

		1876	*	*****		UCM18760
		1877	*			UCM18770
		1878	*	TEST 5		UCM18780
		1879	*			UCM18790
		1880	*	PURPOSE OF TEST:		UCM18800
		1881	*	TEST 5 VERIFIES THAT SELECTION OF ZERO RESOLUTION FOLLOWED BY A		UCM18810
		1882	*	COMMAND 'START' WILL STOP THE PRECISION INTERVAL CLOCK (PIC).		UCM18820
		1883	*			UCM18830
		1884	*	ASSUMPTIONS:		UCM18840
		1885	*	IT IS ASSUMED THAT THE PROCESSOR, MEMORY, AND TELETYPE TESTS HAVE		UCM18850
		1886	*	BEEN RUN PRIOR TO SELECTING THIS TEST.		UCM18860
		1887	*			UCM18870
		1888	*	DESIGN SPECIFICATIONS:		UCM18880
		1889	*	CLOCK INTERRUPTS ARE DISABLED. A ONE-MILLISECOND RESOLUTION AND		UCM18890
		1890	*	AN INTERVAL OF 4096 (MILLISECONDS) IS SELECTED. A COMMAND 'START'		UCM18900
		1891	*	IS THEN ISSUED. WHILE THE PIC IS RUNNING, A ZERO RESOLUTION IS		UCM18910
		1892	*	SELECTED, AND A SECOND COMMAND 'START' IS ISSUED. THE PROGRAM DELAYS		UCM18920
		1893	*	12 TO 15 MILLISECONDS, AND THE PIC CURRENT INTERVAL COUNT (CIC)		UCM18930
		1894	*	IS READ. THE COUNT SHOULD NOT HAVE BEEN DECREMENTED.		UCM18940
		1895	*			UCM18950
		1896	*			UCM18960
		1897	*	HOW TO RUN THE TEST:		UCM18970
		1898	*	ENTER APPROPRIATE VALUES FOR THE TIMVAL AND DEVADR OPTIONS. SELECT		UCM18980
		1899	*	THE TEST, AND ENTER 'RUN'. NO MANUAL INTERVENTION IS REQUIRED.		UCM18990
		1900	*			UCM19000
		1901	*	OPTIONS:		UCM19010
		1902	*	LOOP, CONTIN, DEVADR, INTLEV, TIMVAL		UCM19020
		1903	*			UCM19030
		1904	*	ERRORS:		UCM19040
		1905	*	01,0C		UCM19050
		1906	*			UCM19060
		1907	*			UCM19070
	0000 1A8C	1908	TEST5	EQU *		UCM19080
		1909	*			UCM19090
1A8C	4840 188A	1910	LH	PIC,PREC		UCM19100
1A90	4850 188C	1911	LH	LFC,LINE		UCM19110
		1912	*			UCM19120
1A94	C800 1A00	1913	LHI	RO,T5INT	INTPT VECTOR	UCM19130
1A98	4000 1892	1914	STH	RO,HDLR0		UCM19140
1A9C	4000 1894	1915	STH	RO,HDLR1		UCM19150
		1916	*			UCM19160
1AA0	DE40 1EB3	1917	OC	PIC,DISABLE	DISABLE INTERRUPTS.	UCM19170
1AA4	DE50 1EB3	1918	OC	LFC,DISABLE		UCM19180
1AA8	D840 1EBE	1919	WH	PIC,RIC8FFF	1 MSEC RES., 4095 (MSEC) INTERVAL	UCM19190
1AAC	DE40 1EB1	1920	OC	PIC,STDSM	START CLOCK, DISARM INTPTS.	UCM19200
1AB0	D840 1EB4	1921	WH	PIC,RIC0FFF	0 RES, 4095 INTERVAL.	UCM19210
1AB4	DE40 1EB1	1922	CC	PIC,STDSM	SHOULD STOP PRECISION CLOCK.	UCM19220
1AB8	41F0 1E5E	1923	BAL	LINK,DELAY		UCM19230
1ABC	9940	1924	RHR	PIC,RO	READ PIC CURRENT INTERVAL COUNT	UCM19240
1ABE	4000 1ECA	1925	STH	RO,CURCOUNT		UCM19250
1AC2	C500 0FFF	1926	CLHI	RO,X'0FFF'	DID CLOCK STOP ?	UCM19260
1AC6	2333	1927	BES	T5END	YES.	UCM19270
		1928	*			UCM19280

TEST 5

1AC8 41F0 1DEE
1ACC 4300 0E28

0000 1A00
1A08 41F0 1C52
1A04 4300 1ACC

1929 BAL R15,TT0C
1930 TSEND B TSEND
1931 *
1932 *
1933 T5INT EQU *
1934 BAL R15,TT01
1935 B TSEND
1936 *

ERROR 0C - PIC NOT STOPPED

NO INTERRUPTS EXPECTED
ERROR 01 - INTPT WHILE DISABLED/DSMD

UCM19290
UCM19300
UCM19310
UCM19320
UCM19330
UCM19340
UCM19350
UCM19360

TEST 6

	1938	*	*****		UCM19380
	1939	*			UCM19390
	1940	*	T E S T 6		UCM19400
	1941	*			UCM19410
	1942	*	PURPOSE OF TEST:		UCM19420
	1943	*	TEST 6 USES THE PRECISION INTERVAL CLOCK TO MEASURE THE TIME TAKEN		UCM19430
	1944	*	FOR 50 LINE FREQUENCY CLOCK INTERRUPTS (50 HALF-CYCLES ON THE LINE).		UCM19440
	1945	*			UCM19450
	1946	*	ASSUMPTIONS:		UCM19460
	1947	*	IT IS ASSUMED THAT THE PROCESSOR, MEMORY, AND TELETYPE TESTS HAVE		UCM19470
	1948	*	BEEN RUN PRIOR TO SELECTING THIS TEST.		UCM19480
	1949	*			UCM19490
	1950	*	DESIGN SPECIFICATIONS:		UCM19500
	1951	*	LFC INTERRUPTS ARE ENABLED AND PIC INTERRUPTS DISABLED, A RESOLUTION		UCM19510
	1952	*	OF 100 MICROSECONDS AND AN INTERVAL OF 4096 (409 MILLISECONDS)		UCM19520
	1953	*	ARE SELECTED, PROCESSOR INTERRUPTS ARE ENABLED, AND THE PROGRAM		UCM19530
	1954	*	DELAYS 12 TO 15 MILLISECONDS, WHEN THE LFC INTERRUPTS, PIC INTERRUPTS		UCM19540
	1955	*	ARE ENABLED, AND A COMMAND 'START' IS ISSUED, AN LFC INTERRUPT		UCM19550
	1956	*	COUNTER IS INITIALIZED, AND 50 LFC INTERRUPTS ARE COUNTED, WHEN THE		UCM19560
	1957	*	LAST LFC INTERRUPT IS RECEIVED, THE PIC CURRENT INTERVAL COUNT (CIC)		UCM19570
	1958	*	IS READ, THE VALUE READ IS TESTED, TO VERIFY THAT THE PIC IS NOT		UCM19580
	1959	*	RUNNING TOO FAST OR TOO SLOWLY, AN ACCURACY OF 1% IS ALLOWED.		UCM19590
	1960	*	FOR CRITICAL TESTING, TEST EQUIPMENT SUCH AS AN ACCURATELY CALIBRATED		UCM19600
	1961	*	OSCILLOSCOPE IS REQUIRED.		UCM19610
	1962	*			UCM19620
	1963	*	HOW TO RUN THE TEST:		UCM19630
	1964	*	ENTER APPROPRIATE VALUES FOR THE TINVAL AND DEVADR OPTIONS, SELECT		UCM19640
	1965	*	THE TEST, AND ENTER 'RUN'. NO MANUAL INTERVENTION IS REQUIRED.		UCM19650
	1966	*			UCM19660
	1967	*	OPTIONS:		UCM19670
	1968	*	LOOP, CONTIN, DEVADR, INTLEV, TINVAL, HZ		UCM19680
	1969	*			UCM19690
	1970	*	ERRORS:		UCM19700
	1971	*	01,03,06,09,0A		UCM19710
	1972	*			UCM19720
	1973	*			UCM19730
	0000 1AD8		TEST6 EQU *		UCM19740
					UCM19750
	1AD8 4840 188A		LH PIC,PREC		UCM19760
	1ADC 4850 188C		LH LFC,LINE		UCM19770
	1AE0 C800 1B3A		LHI R0,PRECINT	PIC INTPT HDLR.	UCM19780
	1AE4 4000 1892		STH R0,HDLR0		UCM19790
	1AE8 C800 1B62		LHI R0,LINEINT	LFC INTPT HDLR.	UCM19800
	1AEC 4000 1894		STH R0,HDLR1		UCM19810
					UCM19820
	1AF0 DES0 1EAF		OC LFC,DISARM	'STOP' LFC.	UCM19830
	1AF4 DE40 1EB3		OC PIC,DISABLE		UCM19840
					UCM19850
	1AF8 4800 1EB4		LH R0,RICOFFF		UCM19860
	1AFC 4000 1ECC		STH R0,PATSAV		UCM19870
	1B00 D840 1EB4	TST6.1	WH PIC,RICOFFF	TO STOP CLOCK.	UCM19880
	1B04 9D43		SSR PIC,R3		UCM19890
	1B06 D230 1ECE		STB R3,TEMPSTA		UCM19900

TEST 6

1B0A	DE40 1EB1	1991	OC	PIC,STDSM	START, DISARM (STOP).	UCM19910
1B0E	C430 0008	1992	NHI	R3,X'08'	OVERFLOW ?	UCM19920
1B12	2039	1993	BNZS	TST6.1	YES.	UCM19930
		1994	*CLOCK NOW STOPPED.			UCM19940
1B14	D840 1EBA	1995	WH	PIC,RIC4FFF	RES 100 USEC, 4095 (409 MSEC) INT.	UCM19950
		1996	*			UCM19960
1B18	2400	1997	LIS	R0,0		UCM19970
1B1A	4000 1EC4	1998	STH	R0,FLAG	0 = PIC NOT STARTED	UCM19980
1B1E	4000 1EC6	1999	STH	R0,PICINT	0 = PIC HAS NOT YET INTERRUPTED	UCM19990
1B22	4000 1EC2	2000	STH	R0,FSTINT	0 = 'START' INTPT NOT YET RECEIVED.	UCM20000
1B26	4000 1EC8	2001	STH	R0,INTCNT	LFC INTERRUPT COUNT	UCM20010
1B2A	DE50 1EAE	2002	OC	LFC,ENABLE	'START' LFC	UCM20020
1B2E	41F0 1E5E	2003	TST6.2	BAL LINK,DELAY	WAIT FOR INTERRUPT.	UCM20030
		2004	*			UCM20040
1B32	41F0 1D3C	2005	BAL	R15,TT06	ERROR 06 - LFC INTPT TIMEOUT.	UCM20050
1B36	4300 0E28	2006	T6END	B TSTEND		UCM20060
		2007	*			UCM20070
	0000 1B3A	2008	PRECINT	EQU *	PRECISION CLOCK INTERRUPTED.	UCM20080
		2009	* (ON MODEL 7/32, SOFTWARE OVERHEAD < 75 USEC (ETPE+START/READ DELAY))			UCM20090
1B3A	4840 188A	2010	LH	PIC,PREC		UCM20100
1B3E	4800 1EC4	2011	LH	R0,FLAG	PIC INTERRUPTED. WAS IT RUNNING ?	UCM20110
1B42	2135	2012	BNZS	PREC.1	YES.	UCM20120
1B44	41F0 1C52	2013	BAL	R15,TT01	ERROR 01 - INTPT WHILE DISAB/DSMD.	UCM20130
1B48	4300 1B36	2014	B	T6END		UCM20140
		2015	*			UCM20150
1B4C	4810 1EC2	2016	PREC.1	LH R1,FSTINT	'START' INTPT RECEIVED YET ?	UCM20160
1B50	2135	2017	BNZS	PREC.2	YES.	UCM20170
1B52	4040 1EC2	2018	STH	PIC,FSTINT	NO, THIS IS IT.	UCM20180
1B56	4300 1B2E	2019	B	TST6.2	"THROW IT AWAY"	UCM20190
1B5A	4040 1EC6	2020	PREC.2	STH PIC,PICINT	PIC RUNNING, GOT INTVL INTPT;	UCM20200
1B5E	4300 1B2E	2021	B	TST6.2	SO WAIT FOR NEXT LFC INTPT.	UCM20210
		2022	*			UCM20220
		2023	*			UCM20230
		2024	*			UCM20240
	0000 1B62	2025	LINEINT	EQU *	LFC INTERRUPT RECEIVED.	UCM20250
1B62	4840 188A	2026	LH	PIC,PREC		UCM20260
1B66	0940 1ECA	2027	RH	PIC,CURCOUNT	READ CIC	UCM20270
1B6A	4800 1EC4	2028	LH	R0,FLAG	PIC RUNNING ?	UCM20280
1B6E	2135	2029	BNZS	LINE.1	IF SO, COUNT LFC INTPTS.	UCM20290
1B70	DE40 1EB0	2030	OC	PIC,STEN	START PIC - WILL NOT USE 1ST INTPT.	UCM20300
1B74	4040 1EC4	2031	STH	PIC,FLAG	PIC NOW RUNNING.	UCM20310
		2032	*			UCM20320
1B78	4800 1EC8	2033	LINE.1	LH R0,INTCNT	COUNT LFC INTPTS	UCM20330
1B7C	2601	2034	AIS	R0,1		UCM20340
1B7E	4000 1EC8	2035	STH	R0,INTCNT		UCM20350
1B82	C500 0033	2036	CLHI	R0,51	INTERRUPT QUOTA MET ?	UCM20360
1B86	4200 1B2E	2037	BL	TST6.2	WAIT FOR MORE.	UCM20370
		2038	*			UCM20380
1B8A	4810 1EC2	2039	LH	R1,FSTINT	DID WE GET 'START' INTPT FROM PIC ?	UCM20390
1B8E	2135	2040	BNZS	LINE.2	YES.	UCM20400
1B90	41F0 1CC6	2041	BAL	R15,TT03	ERROR 03 - PIC DID NOT INTERRUPT.	UCM20410
1B94	4300 1B36	2042	B	T6END		UCM20420
		2043	*			UCM20430

TEST 6

1B98	4810	1EC6	2044	LINE.2	LH	R1,PICINT	GOT PIC INTERVAL INTPT. YET ?	UCM20440
1B9C	2135		2045		BNZS	LINE.3	YES.	UCM20450
1B9E	41F0	1D8E	2046		BAL	R15,TT09	ERROR 09 - PIC INTPT LATE.	UCM20460
1BA2	4300	1B36	2047		B	T6END		UCM20470
			2048	*				UCM20480
1BA6	C500	0034	2049	LINE.3	CLHI	R0,52		UCM20490
1BAA	4260	1B2E	2050		BL	TST6.2	WAIT FOR #52	UCM20500
			2051	*				UCM20510
1BAE	4800	1ECC	2052		LH	R0,PATSAV	START COUNT LESS	UCM20520
1BB2	4800	1ECA	2053		SH	R0,CURCOUNT	DECREMENTED COUNT = DECREMENT	UCM20530
1BB6	4810	1700	2054		LH	R1,HZ+6		UCM20540
1BBA	C510	0060	2055		CLHI	R1,X'60'	60 CYCLE LINE ?	UCM20550
1BBE	2338		2056		BES	LINE.4		UCM20560
			2057	*				UCM20570
			2058	*50 CYCLE LINE				UCM20580
1BC0	C500	041F	2059		CLHI	R0,5151&X'0FFF'	50-HZ COUNT + 1%	UCM20590
1BC4	2388		2060		BNLS	LINE.5	COUNT HIGH	UCM20600
1BC6	C500	03B9	2061		CLHI	R0,5049&X'0FFF'	50-HZ COUNT - 1%	UCM20610
1BCA	2188		2062		BLS	LINE.5	COUNT LOW.	UCM20620
1BCC	2309		2063		BS	LINE.6		UCM20630
			2064	*				UCM20640
			2065	* 60 CYCLE LINE				UCM20650
1BCE	C500	00C2	2066	LINE.4	CLHI	R0,4290&X'0FFF'	60-HZ COUNT + 1%	UCM20660
1BD2	2384		2067		BNLS	LINE.5	COUNT HIGH.	UCM20670
1BD4	C500	006E	2068		CLHI	R0,4206&X'0FFF'	60-HZ COUNT - 1%	UCM20680
1BD8	2383		2069		BNLS	LINE.6	COUNT NOT LOW.	UCM20690
			2070	*				UCM20700
1BDA	41F0	1DA2	2071	LINE.5	BAL	R15,TT0A	ERROR 0A - COUNT NOT IN RANGE.	UCM20710
			2072	*				UCM20720
1BDE	4300	1B36	2073	LINE.6	B	T6END		UCM20730
			2074	*				UCM20740

TEST 7

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2076 * *****
2077 *
2078 *           T E S T 7
2079 *
2080 * PURPOSE OF TEST:
2081 * TEST 7 VERIFIES THAT DATA MAY BE WRITTEN TO THE PIC RESOLUTION AND
2082 * INITIAL COUNT (RIC) REGISTER DURING A CLOCK PERIOD (WHILE THE CLOCK
2083 * IS RUNNING).
2084 *
2085 * ASSUMPTIONS:
2086 * IT IS ASSUMED THAT THE PROCESSOR, MEMORY, AND TELETYPE TESTS HAVE
2087 * BEEN RUN PRIOR TO SELECTING THIS TEST.
2088 *
2089 * DESIGN SPECIFICATIONS:
2090 * CLOCK INTERRUPTS ARE DISABLED AND THE PIC IS STOPPED. A ONE-MILLI
2091 * SECOND RESOLUTION AND ONE-MILLISECOND INTERVAL ARE SELECTED. PIC
2092 * INTERRUPTS ARE ENABLED, AND A COMMAND 'START' IS ISSUED. AN INTERVAL
2093 * OF 4096 (MILLISECONDS) IS SELECTED, AND PROCESSOR INTERRUPTS ARE
2094 * ENABLED. THE PROGRAM DELAYS 12 TO 15 MILLISECONDS. WHEN THE PIC
2095 * INTERRUPTS, THE CURRENT INTERVAL COUNT (CIC) IS READ AND THE CURRENT
2096 * COUNT COMPARED TO THE VALUE PREVIOUSLY WRITTEN TO VERIFY THAT THE
2097 * WRITE 'WORKED' DURING THE CLOCK INTERVAL.
2098 *
2099 * HOW TO RUN THE TEST:
2100 * ENTER APPROPRIATE VALUES FOR THE TIMVAL AND DEVA DR OPTIONS, SELECT
2101 * THE TEST, AND ENTER 'RUN'. NO MANUAL INTERVENTION IS REQUIRED.
2102 *
2103 * OPTIONS:
2104 * LOOP, CONTIN, DEVA DR, INTLEV, TIMVAL
2105 *
2106 * ERRORS:
2107 * 01,03,08
2108 *
2109 *
2110 TEST7 EQU *
2111 *
2112 LHI R0,T7INT          INTERRUPT VECTORS
2113 STH R0,HDLR0
2114 STH R0,HDLR1
2115 *
2116 LH PIC,PREC
2117 LH LFC,LINE
2118 *
2119 OC LFC,DISARM
2120 OC PIC,ZERO          SET BYTE POINTER
2121 WH PIC,ZERO
2122 OC PIC,STJSM        STOP PIC.
2123 WH PIC,RIC&001     RES 1 MSEC, INTERVAL 1 (MSEC)
2124 LH R0,RIC&FFF
2125 STH R0,PATSAV
2126 OC PIC,STEN        START PIC
2127 WH PIC,RIC&FFF     RES 1 MSEC, INTERVAL 4095 (MSEC)
2128 BAL LINK,DELAY

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0000	18E2				
18E2	C800	1C26			
18E6	4000	1892			
18EA	4000	1894			
18EE	4840	188A			
18F2	4850	188C			
18F6	DE50	1EAF			
18FA	DE40	1EAC			
18FE	D840	1EAC			
1C02	0E40	1E91			
1C06	D840	1EBC			
1C0A	4800	1EBE			
1C0E	4000	1ECC			
1C12	DE40	1EB0			
1C16	D840	1EBE			
1C1A	41F0	1E5E			

TEST 7

1C1E	41F0	1CC6	2129	*					UCM21290
1C22	4300	0E28	2130		BAL	R15,TT03	ERROR 03 - NO PIC INTERRUPT		UCM21300
			2131	T7END	B	TSTEND			UCM21310
			2132	*					UCM21320
1C26	4840	188A	2133	T7INT	LH	PIC,PREC			UCM21330
1C2A	D940	1ECA	2134		RH	PIC,CURCOUNT	GET COUNT FROM PIC CIC.		UCM21340
1C2E	4800	1690	2135		LH	R0,INTDEV			UCM21350
1C32	4500	188A	2136		CLH	R3,PREC			UCM21360
1C36	2335		2137		BES	T7INT.1			UCM21370
1C38	41F0	1C52	2138		BAL	R15,TT01	ERROR 01 - LFC INTPT WHEN DISARMED.		UCM21380
1C3C	4300	1C22	2139		B	T7END			UCM21390
			2140	*					UCM21400
1C40	C800	0FFF	2141	T7INT.1	LHI	R0,X'0FFF'	COUNT WRITTEN TO PIC.		UCM21410
1C44	4500	1ECA	2142		CLH	R0,CURCOUNT			UCM21420
1C48	2333		2143		BES	T7INT.2			UCM21430
1C4A	41F0	1DB6	2144		BAL	R15,TT08	ERROR 08 - CIC NOT READ PROPERLY		UCM21440
			2145	*					UCM21450
1C4E	4300	1C22	2146	T7INT.2	B	T7END			UCM21460
			2147	*					UCM21470

ERROR HANDLERS

		2149	*	*****		UCM21490
		2150	*			UCM21500
		2151	*	ERROR HANDLERS.		UCM21510
		2152	*			UCM21520
		2153	TT01	EQU *	INTPT WHEN DISABLED/DISARMED	UCM21530
1C52	40F0 1E5C	2154	STH	R15,LINKSAV		UCM21540
1C56	C800 3031	2155	LHI	R0,C'01'		UCM21550
1C5A	4000 16FE	2156	STH	R0,ERRNO		UCM21560
1C5E	41E0 0FD0	2157	BAL	R14,ERR1	'ERROR TT01'	UCM21570
1C62	2403	2158	LIS	R0,3		UCM21580
1C64	4810 1690	2159	LH	R1,INTDEV		UCM21590
1C68	C820 1720	2160	LHI	R2,ASCIDEV		UCM21600
1C6C	41F0 1130	2161	BAL	LINK,HEXASC		UCM21610
1C70	2402	2162	LIS	R0,2		UCM21620
1C72	4810 1692	2163	LH	R1,INTSTA		UCM21630
1C76	C820 1728	2164	LHI	R2,ASCISTA		UCM21640
1C7A	41F0 1130	2165	BAL	LINK,HEXASC		UCM21650
1C7E	C850 171C	2166	LHI	R5,DEVMSG		UCM21660
1C82	41F0 1190	2167	BAL	LINK,PRINT	'DEV DDD STA SS'	UCM21670
1C86	4300 1E40	2168	B	TSTENDX		UCM21680
		2169	*			UCM21690
		2170	TT02	EQU *	PIC DID NOT DECREMENT WHEN STARTED.	UCM21700
1C8A	40F0 1E5C	2171	STH	R15,LINKSAV		UCM21710
1C8E	C800 3032	2172	LHI	R0,C'02'		UCM21720
1C92	4000 16FE	2173	STH	R0,ERRNO		UCM21730
1C96	41E0 0FD0	2174	BAL	R14,ERR1	'ERROR TT02'	UCM21740
1C9A	2404	2175	LIS	R0,4		UCM21750
1C9C	4810 1ECC	2176	LH	R1,PATSAV		UCM21760
1CA0	C410 0FFF	2177	NHI	R1,X'0FFF'		UCM21770
1CA4	C820 1840	2178	LHI	R2,INTASC		UCM21780
1CA8	41F0 1130	2179	BAL	LINK,HEXASC		UCM21790
1CAC	2404	2180	LIS	R0,4		UCM21800
1CAE	4810 1ECA	2181	LH	R1,CURCOUNT		UCM21810
1CB2	C820 1852	2182	LHI	R2,PRESASC		UCM21820
1CB6	41F0 1130	2183	BAL	LINK,HEXASC		UCM21830
1CBA	C850 1834	2184	LHI	R5,COUNTMSG		UCM21840
1CBE	41F0 1190	2185	BAL	LINK,PRINT	'INIT COUNT XXXX PRES COUNT YYYY'	UCM21850
1CC2	4300 1E40	2186	B	TSTENDX		UCM21860
		2187	*			UCM21870
		2188	TT03	EQU *	PIC DID NOT INTERRUPT	UCM21880
1CC6	40F0 1E5C	2189	STH	R15,LINKSAV		UCM21890
1CCA	C800 3033	2190	LHI	R0,C'03'		UCM21900
1CCE	4000 16FE	2191	STH	R0,ERRNO		UCM21910
1CD2	41E0 0FD0	2192	BAL	R14,ERR1	'ERROR TT03'	UCM21920
1CD6	4810 1ECC	2193	LH	R1,PATSAV		UCM21930
1CDA	901C	2194	SRLS	R1,12		UCM21940
1CD0	2401	2195	LIS	R0,1		UCM21950
1CDE	C820 1863	2196	LHI	R2,ASCBIT+1		UCM21960
1CE2	41F0 1130	2197	BAL	LINK,HEXASC		UCM21970
1CE6	C850 185A	2198	LHI	R5,BITMSG		UCM21980
1CEA	41F0 1190	2199	BAL	LINK,PRINT	'BITS SET X'	UCM21990
1CEE	4300 1E40	2200	B	TSTENDX		UCM22000
		2201	*			UCM22010

ERROR HANDLERS

	0000	1CF2	2202	TT04	EQU	*	PIC INTERRUPTED WITH LFC ADDRESS	UCM22020
1CF2	40F0	1E5C	2203		STH	R15,LINKSAV		UCM22030
1CF6	C800	3034	2204		LHI	R0,C'04'		UCM22040
1CFA	4000	16FE	2205		STH	R0,ERRNO		UCM22050
1CFE	41E0	0FD0	2206		BAL	R14,ERR1	'ERROR TT04'	UCM22060
1D02	4800	1690	2207	TT04.1	LH	R0,INTDEV		UCM22070
1D06	4000	1690	2208		STH	R0,ERRDEV		UCM22080
1D0A	41E0	0FDA	2209		BAL	R14,ERRD1	'DEV DDD'	UCM22090
1D0E	4810	1EC0	2210		LH	R1,EXPDEV		UCM22100
1D12	2403		2211		LIS	R0,3		UCM22110
1D14	C820	186A	2212		LHI	R2,ASCEXP		UCM22120
1D18	41FC	1130	2213		BAL	R15,HEXASC		UCM22130
1D1C	C850	1866	2214		LHI	R5,ASCMSG		UCM22140
1D20	41F0	1190	2215		BAL	R15,PRINT	'EXP DDD'	UCM22150
1D24	4300	1E40	2216		B	TSTENDX		UCM22160
			2217	*				UCM22170
	0000	1D28	2218	TT05	EQU	*	PIC OVERFLOW STATUS BIT NOT SET	UCM22180
1D28	40F0	1E5C	2219		STH	R15,LINKSAV		UCM22190
1D2C	C800	3035	2220		LHI	R0,C'05'		UCM22200
1D30	4000	16FE	2221		STH	R0,ERRNO		UCM22210
1D34	41E0	0FD0	2222		BAL	R14,ERR1	'ERROR TT05'	UCM22220
1D38	4300	1E26	2223		B	TT0E.1	'STA SS'	UCM22230
			2224	*				UCM22240
	0000	1D3C	2225	TT06	EQU	*	LFC INTERRUPT TIMEOUT	UCM22250
1D3C	40F0	1E5C	2226		STH	R15,LINKSAV		UCM22260
1D40	C800	3036	2227		LHI	R0,C'06'		UCM22270
1D44	4000	16FE	2228		STH	R0,ERRNO		UCM22280
1D48	41E0	0FD0	2229		BAL	R14,ERR1	'ERROR TT06'	UCM22290
1D4C	4300	1E40	2230		B	TSTENDX		UCM22300
			2231	*				UCM22310
	0000	1D50	2232	TT07	EQU	*	LFC INTERRUPTED WITH PIC ADDRESS	UCM22320
1D50	40F0	1E5C	2233		STH	R15,LINKSAV		UCM22330
1D54	C800	3037	2234		LHI	R0,C'07'		UCM22340
1D58	4000	16FE	2235		STH	R0,ERRNO		UCM22350
1D5C	41E0	0FD0	2236		BAL	R14,ERR1	'ERROR TT07'	UCM22360
1D60	4300	1D02	2237		B	TT04.1	'DEV DDD EXP DDD'	UCM22370
			2238	*				UCM22380
	0000	1D64	2239	TT08	EQU	*	PIC DID NOT DECREMENT (TIMEOUT)	UCM22390
1D64	40F0	1E5C	2240		STH	R15,LINKSAV		UCM22400
1D68	C800	3032	2241		LHI	R0,C'02'		UCM22410
1D6C	4000	16FE	2242		STH	R0,ERRNO		UCM22420
1D70	41E0	0FD0	2243		BAL	R14,ERR1	'ERROR TT08'	UCM22430
1D74	2404		2244	TT08.1	LIS	R0,4		UCM22440
1D76	4810	1ECA	2245		LH	R1,CURCOUNT		UCM22450
1D7A	C820	1852	2246		LHI	R2,PRESASC		UCM22460
1D7E	41F0	1130	2247		BAL	LINK,HEXASC		UCM22470
1D82	C850	1846	2248		LHI	R5,CNTMSG1		UCM22480
1D86	41F0	1190	2249		BAL	LINK,PRINT	'PRES COUNT XXXX'	UCM22490
1D8A	4300	1E40	2250		B	TSTENDX		UCM22500
			2251	*				UCM22510
	0000	1D8E	2252	TT09	EQU	*	NO PIC INTPT BEFORE LFC INTPT #51.	UCM22520
1D8E	40F0	1E5C	2253		STH	R15,LINKSAV		UCM22530
1D92	C800	3039	2254		LHI	R0,C'09'		UCM22540

ERROR HANDLERS

1D96	4000	16FE	2255	STH	R0,ERRNO		UCM22550
1D9A	41E0	0FD0	2256	BAL	R14,ERR1	'ERROR TT09'	UCM22560
1D9E	4300	1D74	2257	B	TT08.1	'PRES COUNT XXXX'	UCM22570
			2258	*			UCM22580
	0000	1DA2	2259	TT0A	EQU *	PIC CIC OUT OF LIMITS AT LFC	UCM22590
1DA2	40F0	1E5C	2260	STH	R15,LINKSAV	. INTERRUPT #52	UCM22600
1DA6	C800	3041	2261	LHI	R0,C'0A'		UCM22610
1DAA	4000	16FE	2262	STH	R0,ERRNO		UCM22620
1DAE	41E0	0FD0	2263	BAL	R14,ERR1	'ERROR TT0A'	UCM22630
1DB2	4300	1D74	2264	B	TT08.1	'PRES COUNT XXXX'	UCM22640
			2265	*			UCM22650
	0000	1DB6	2266	TT0B	EQU *	PIC LOADED BUT NOT READ OK	UCM22660
1DB6	40F0	1E5C	2267	STH	R15,LINKSAV		UCM22670
1DBA	C800	3042	2268	LHI	R0,C'0B'		UCM22680
1DBE	4000	16FE	2269	STH	R0,ERRNO		UCM22690
1DC2	41E0	0FD0	2270	BAL	R14,ERR1	'ERROR TT0B'	UCM22700
1DC6	4610	1ECC	2271	TT0B.1	LH R1,PATSAV		UCM22710
1DCA	2404		2272		LIS R0,4		UCM22720
1DCC	C820	1878	2273	LHI	R2,LOADASC		UCM22730
1DD0	41F0	1130	2274	BAL	LINK,HEXASC		UCM22740
1DD4	4610	1ECA	2275	LH	R1,CURCOUNT		UCM22750
1DD8	2404		2276	LIS	R0,4		UCM22760
1DDA	C820	1884	2277	LHI	R2,RDASC		UCM22770
1DDE	41F0	1130	2278	BAL	LINK,HEXASC		UCM22780
1DE2	C850	1870	2279	LHI	R5,LOADMSG		UCM22790
1DE6	41F0	1190	2280	BAL	LINK,PRINT	'LOADED XXXX READ YYYY'	UCM22800
1DEA	4300	1E40	2281	B	TSTENDX		UCM22810
			2282	*			UCM22820
	0000	1DEE	2283	TT0C	EQU *	PIC NOT STOPPED WITH ZERO WRITE/STRT	UCM22830
1DEE	40F0	1E5C	2284	STH	R15,LINKSAV		UCM22840
1DF2	C800	3043	2285	LHI	R0,C'0C'		UCM22850
1DF6	4000	16FE	2286	STH	R0,ERRNO		UCM22860
1DFA	41E0	0FD0	2287	BAL	R14,ERR1	'ERROR TT0C'	UCM22870
1DFE	4300	1D74	2288	B	TT08.1	'PRES COUNT XXXX'	UCM22880
			2289	*			UCM22890
	0000	1E02	2290	TT0D	EQU *	PIC NOT LOADED OK DURING INTERVAL	UCM22900
1E02	40F0	1E5C	2291	STH	R15,LINKSAV		UCM22910
1E06	C800	3044	2292	LHI	R0,C'0D'		UCM22920
1E0A	4000	16FE	2293	STH	R0,ERRNO		UCM22930
1E0E	41E0	0FD0	2294	BAL	R14,ERR1	'ERROR TT0D'	UCM22940
1E12	4300	1DC6	2295	B	TT0B.1	'LOADED XXXX READ YYYY'	UCM22950
			2296	*			UCM22960
	0000	1E16	2297	TT0E	EQU *	PIC OVERFLOW BIT NOT RESET BY SSR	UCM22970
1E16	40F0	1E5C	2298	STH	R15,LINKSAV		UCM22980
1E1A	C800	3045	2299	LHI	R0,C'0E'		UCM22990
1E1E	4000	16FE	2300	STH	R0,ERRNO		UCM23000
1E22	41E0	0FD0	2301	BAL	R14,ERR1	'ERROR TT0E'	UCM23010
1E26	4610	1ECE	2302	TT0E.1	LH R1,TEMPSTA	DEVICE STATUS	UCM23020
1E2A	C820	1728	2303	LHI	R2,ASCISTA		UCM23030
1E2E	2402		2304	LIS	R0,2		UCM23040
1E30	41F0	1130	2305	BAL	LINK,HEXASC		UCM23050
1E34	C850	1724	2306	LHI	R5,STAMSG		UCM23060
1E38	41F0	1190	2307	BAL	LINK,PRINT	'STA SS'	UCM23070

ERROR HANDLERS

1EA6 4000 1894
1EAA 030F

2359
2360

STH R0.DEVINT+2
BR LINK

UCM23590
UCM23600

TEST CONSTANTS AND STORAGE AREAS

		2362	*			UCH23620
		2363	*	*****		UCH23630
		2364	*			UCH23640
		2365	*	TEST CONSTANTS		UCH23650
		2366	*			UCH23660
1EAC	0000	2367	ZERO	DCX	0000	UCH23670
1EAE	40	2368	ENABLE	DB	X'40'	UCH23680
1EAF	C0	2369	DISARM	DB	X'C0'	UCH23690
1EB0	60	2370	STEN	DB	X'60'	UCH23700
1EB1	E0	2371	STDSM	DB	X'E0'	UCH23710
1EB2	A0	2372	STDSB	DB	X'A0'	UCH23720
1EB3	60	2373	DISABLE	DB	X'80'	UCH23730
		2374	*	*****		UCH23740
		2375	*	RESOLUTION AND INITIAL COUNT VALUES		UCH23750
1EB4	0FFF	2376	RIC0FFF	DCX	0FFF	UCH23760
1EB6	1000	2377	RIC1000	DCX	1000	UCH23770
1EB8	1384	2378	RIC1384	DCX	1384	UCH23780
1EBA	4FFF	2379	RIC4FFF	DCX	4FFF	UCH23790
1EBC	8001	2380	RIC8001	DCX	8001	UCH23800
1EBE	8FFF	2381	RIC8FFF	DCX	8FFF	UCH23810
		2382	*	*****		UCH23820
1EC0	0000	2383	EXPDEV	DCX	0	UCH23830
1EC2	0000	2384	FSTINT	DCX	0	UCH23840
1EC4	0000	2385	FLAG	DCX	0	UCH23850
1EC6	0000	2386	PICINT	DCX	0	UCH23860
1EC8	0000	2387	INTCNT	DCX	0	UCH23870
1ECA	0000	2388	CURCOUNT	DCX	0	UCH23880
1ECC	0000	2389	PATSAV	DCX	0	UCH23890
1ECE	0000	2390	TEMPSTA	DCX	0	UCH23900
		2391	*			UCH23910
	0000 1ED0	2392	LNZB	EQU	*	UCH23920
		2393	*			UCH23930
		2394	**CHKSUM			UCH23940
		2395	*	START OF CHKSUM FILE		UCH23950
		2396	*			UCH23960
		2397	*			UCH23970
		2398	*			UCH23980
1ED0		2399	OPTBUF	DS	6	UCH23990
1ED6		2400	IOSAVE	DS	2	UCH24000
1ED8		2401	TEMP	DS	2	UCH24010
1EE0		2402		ALIGN	8	UCH24020
1EE0	0000 0000	2403	PSWSAVE	DCY	0,0	UCH24030
1EE4	0000 0000					
1EE6		2404	RSAVE	DS	128	UCH24040
1F68		2405	INTSAV	DS	64	UCH24050
1FA8		2406	ERRSAVE	DS	64	UCH24060
1FE8		2407		DS	256	UCH24070
20E8		2408		DS	64	UCH24080
		2409	*			UCH24090
20E8		2410	IF1	IF	1	UCH24100

DISARM
START AND ENABLE
START,DISARM
START, DISABLE
USED IN TOINT
SET WHEN 'START' INTPT RECEIVED.
SET WHEN PIC INTPTS, TEST 6
LFC INTERRUPT COUNTER, TEST 6
VALUE READ FROM PIC CIC
VALUE WRITTEN TO PIC RIC REGISTER
USED AT TIMES FOR DEVICE STATUS

CHKSUM/M17 PUNCHER

2128	2400	2412	\$CHKSUM	LIS	R0,0	PUNCH M17 TAPE WITH CHECKSUM	UCM24120
212A	9510	2413		EPSR	R1,R0	SELECT REG. SET 0	UCM24130
		2414	*				UCM24140
212C	C810 0A00	2415		LDAI	R1,ORIGIN1	START	UCM24150
2130	2421	2416		LIS	R2,1	INCREMENT	UCM24160
2132	C830 1ED0	2417		LDAI	R3,LNZB	FINAL	UCM24170
2136	2440	2418		LIS	R4,0	CHECKSUM BYTE	UCM24180
2138	D351 0000	2419	\$GEN	LB	R5,0(R1)		UCM24190
213C	0745	2420		XAR	R4,R5		UCM24200
213E	C110 2138	2421		\$XLE	R1,\$GEN		UCM24210
2142	D240 0099	2422		STB	R4,MN+3	CHECKSUM BYTE TO ROOT LOADER	UCM24220
		2423	*				UCM24230
2146	C810 0080	2424	\$TAPE	LHI	R1,X'0080'		UCM24240
214A	9E21	2425		OCR	R2,R1	DISPLAY : NORMAL MODE	UCM24250
214C	9444	2426		EXBR	R4,R4		UCM24260
214E	9824	2427		WHR	R2,R4	CHECKSUM BYTE TO D1	UCM24270
2150	9411	2428		EXBR	R1,R1		UCM24280
2152	9501	2429		EPSR	R0,R1	HALT PROCESSOR.	UCM24290
2154	D360 007A	2431	\$PUNCH	LB	R6,X'7A'	GET BOUTDV (PUNCH) ADDRESS.	UCM24310
2158	DE60 007B	2432		OC	R6,X'7B'	START TAPE PUNCH	UCM24320
215C	9D60	2433		SSR	R6,R0		UCM24330
215E	2081	2434		BTBS	8,1		UCM24340
2160	41F0 21A2	2435		BAL	R15,\$STAPL	PUNCH LEADER	UCM24350
2164	9411	2436		EXBR	R1,R1	(R1) = X'0080'	UCM24360
2166	C830 00CF	2437		LHI	R3,X'CF'		UCM24370
216A	DA61 0000	2438	\$PNCH1	WD	R6,0(R1)	PUNCH BOOT LOADER	UCM24380
216E	9D60	2439		SSR	R6,R0		UCM24390
2170	2081	2440		BTBS	8,1		UCM24400
2172	C110 216A	2441		\$XLE	R1,\$PNCH1		UCM24410
2176	41F0 21A8	2442		BAL	R15,\$STAPL1	PUNCH ONE-FOLD GAP.	UCM24420
		2443	*				UCM24430
217A	D340 0099	2444		LB	R4,MN+3	GET CHECKSUM BYTE	UCM24440
217E	C810 0A00	2445		LDAI	R1,ORIGIN1	(NORMALLY X'A00')	UCM24450
2182	C830 1ED0	2446		LDAI	R3,LNZB		UCM24460
2186	D351 0000	2447	\$PNC-2	LB	R5,0(R1)	PUNCH PROGRAM	UCM24470
218A	0745	2448		XAR	R4,R5		UCM24480
218C	9A65	2449		WDR	R6,R5		UCM24490
218E	9401	2450		EXBR	R0,R1		UCM24500
2190	9820	2451		WHR	R2,R0	DATA ADDRESS TO DISPLAY.	UCM24510
2192	9D60	2452		SSR	R6,R0		UCM24520
2194	2081	2453		BTBS	8,1		UCM24530
2196	C110 2186	2454		\$XLE	R1,\$PNC2		UCM24540
219A	41F0 21A2	2455		BAL	R15,\$STAPL	PUNCH TRAILER.	UCM24550
219E	4300 2146	2456		B	\$TAPE	DISPLAY CHECKSUM, HALT PROCESSOR.	UCM24560
21A2	C800 0100	2458	\$STAPL	LHI	R0,256	TO PUNCH BLACK LEADER	UCM24580
21A6	2303	2459		BS	\$STAPLP		UCM24590
21A8	C800 0055	2460	\$STAPL1	LHI	R0,85	TO PUNCH 1-FOLD GAP	UCM24600
21AC	2701	2461	\$STAPLP	SIS	R0,1		UCM24610
21AE	032F	2462		BNPR	R15	RETURN	UCM24620

CHKSUM/M17 PUNCHER

2150	2430	2463	LIS	R3.0
2152	9A63	2464	WDR	R6,R3
2154	9068	2465	SSR	R6,R8
2156	2081	2466	BTSS	8.1
2158	2236	2467	BS	\$TAPLP
		2468 *		
218A		2469	END	

PUNCH BLANK FRAME

CONTINUE.

UCM24630
UCM24640
UCM24650
UCM24660
UCM24670
UCM24680
UCM24690

CHKSUM/M17 PUNCHER

OPTVAL3	0000	1084	757*	761															
OPTVAL4	0000	1092	759	762*															
ORIGIN1	0000	0A00	93	122*	2415	2445													
ORIGIN2	0000	0A04	123*																
ORIGIN3	0000	0A08	126*																
ORIGIN4	0000	0A0C	127*																
OTC.	0000	1230	935*	949															
OTC.0	0000	1234	936*	941	950														
OTC.1	0000	124A	939	943*															
OTC.4	0000	126E	956*	961															
OUT0	0000	1286	937	954	957	959	956*												
OUT1	0000	128A	931	965	967*														
OUTCHK	0000	1222	237	239	298	303	315	320	323	342	347	613	801	820	828				
			893	903	912	916	927	931*											
			934	942	947	951*													
OUTCHR2	0000	1260	877	880*															
P1	0000	11A2	893*	895															
P2	0000	11C8	881	897*															
P3	0000	11D4	215	1021	1072	1082	1175	1405*											
PASFLG	0000	1696	196	1049	1406*														
PASFLG2	0000	1698	138*																
PASLADR	0000	0A12	1667	1668	1673	1678	1683	1736	1739	1744	1987	2052	2125	2176	2193				
PATSAV	0000	1ECC	2271	2389*															
			935	940	952	968*													
PAUSE	0000	128E	1534*	1579	1588	1591	1592	1594	1603	1606	1659	1661	1670	1671	1672				
PIC	0000	0004	1724	1725	1727	1739	1740	1797	1800	1802	1803	1804	1805	1806	1808				
			1809	1814	1854	1862	1910	1917	1919	1920	1921	1922	1924	1976	1984				
			1988	1989	1991	1995	2010	2018	2020	2026	2027	2030	2031	2116	2120				
			2121	2122	2123	2126	2127	2133	2134										
PICINT	0000	1EC6	1999	2020	2044	2386*													
PREC	0000	188A	1533*	1579	1659	1724	1754	1797	1854	1910	1976	2010	2026	2116	2133				
			2136	2348															
PREC.1	0000	1B4C	2012	2016*															
PREC.2	0000	1B5A	2017	2020*															
PRECINT	0000	1B3A	1978	2008*															
PRESASC	0000	1852	1516*	2182	2246														
PRINT	0000	1190	226	525	552	570	607	684	695	705	719	729	742	875*	998				
			1301	2167	2185	2199	2215	2249	2280	2307									
PRINT2	0000	11E2	898	902*	907														
PRINT3	0000	11F2	905	908*	928														
PRINT3A	0000	1204	911	915*															
PRINT3B	0000	1206	914	916*															
PRINT5	0000	120A	879	900	917*														
PSW	0000	0A22	153*	628	2331														
PSW2	0000	0A24	154*	164	172	233	529	540	663	1132	1245	1335							
PSWMSG	0000	1736	741	1467*															
PSWSAVE	0000	1EE0	91	1142	2403*														
PURETOP	0000	0000R																	
QMSG	0000	1772	997	1474*															
QJESTN	0000	12C4	240	995*															
RO	0000	0000	67*	200	201	204	222	223	241	242	243	244	256	257	312				
			349	351	352	402	403	415	420	421	428	429	430	431	457				
			458	464	468	470	474	477	478	482	482	483	484	485	486				

CHKSUM/M17 PUNCHER

		495	495	496	497	502	503	504	507	510	518	526	526	527
		528	530	541	542	543	544	545	549	581	582	582	583	584
		585	589	590	602	602	603	606	616	623	626	626	627	629
		630	632	637	642	647	653	664	690	700	710	714	724	734
		779	784	786	792	793	804	810	811	823	833	834	845	851
		852	870	875	883	884	897	899	918	925	932	933	935	938
		944	956	962	963	973	976	978	980	981	999	999	1000	1005
		1007	1008	1015	1016	1025	1026	1031	1037	1038	1039	1047	1048	1049
		1061	1062	1063	1069	1070	1071	1075	1080	1081	1084	1085	1086	1094
		1095	1104	1104	1105	1109	1111	1113	1148	1149	1163	1164	1188	1202
		1215	1222	1236	1239	1247	1277	1279	1335	1336	1377	1378	1379	1582
		1583	1584	1585	1586	1617	1618	1619	1664	1665	1669	1670	1673	1674
		1675	1730	1731	1732	1734	1735	1736	1737	1738	1744	1745	1747	1756
		1807	1858	1859	1860	1869	1870	1913	1914	1915	1924	1925	1926	1978
		1979	1980	1981	1986	1987	1997	1998	1999	2000	2001	2011	2028	2033
		2034	2035	2036	2049	2052	2053	2059	2061	2066	2068	2112	2113	2114
		2124	2125	2135	2136	2141	2142	2155	2156	2158	2162	2172	2173	2175
		2180	2190	2191	2195	2204	2205	2207	2209	2211	2220	2221	2227	2228
		2234	2235	2241	2242	2244	2254	2255	2261	2262	2268	2269	2272	2276
		2285	2286	2292	2293	2299	2300	2304	2311	2312	2313	2315	2316	2346
		2347	2348	2349	2350	2352	2353	2354	2355	2357	2358	2359	2412	2413
		2429	2433	2439	2450	2451	2452	2458	2460	2461				
R1	0000 0001	56*	93	105	106	108	113	162	162	163	170	170	171	172
		175	184	187	189	193	204	205	206	208	210	212	213	234
		245	245	254	257	263	265	266	271	273	276	285	287	370
		379	383	404	412	418	465	466	471	472	487	488	489	490
		515	529	530	533	534	540	541	553	554	563	566	575	576
		577	578	584	587	594	595	596	663	664	672	673	674	675
		691	701	711	715	725	735	738	780	783	812	813	815	837
		857	859	878	882	886	909	910	938	940	944	945	946	948
		952	955	956	958	960	963	966	1008	1009	1016	1017	1023	1026
		1031	1032	1045	1046	1047	1048	1051	1052	1054	1054	1056	1062	1063
		1064	1082	1091	1092	1093	1094	1095	1101	1101	1105	1106	1107	1109
		1110	1113	1114	1124	1146	1147	1147	1149	1150	1150	1152	1156	1203
		1237	1240	1246	1373	1374	1536	1597	1598	1607	1608	1609	1666	1667
		1668	1669	1678	1679	1680	1683	1684	1686	1687	1688	1753	1754	1758
		2016	2039	2044	2054	2055	2159	2163	2176	2177	2181	2193	2194	2210
		2245	2271	2275	2302	2413	2415	2419	2421	2424	2425	2428	2428	2429
		2436	2436	2438	2441	2445	2447	2450	2454					
R10	0000 00JA	77*	1229	1229	1230	1249	1267	1268	1269	1295	1295	1296	1356	1356
		1368	1369											
R11	0000 000B	78*												
R12	0000 000C	79*	240	255	264	275	375	378	388	392	396	411	439	476
		754												
R13	0000 000D	80*												
R14	0000 000E	81*	294	330	376	379	381	437	442	446	763	766	772	1310
		1330	1333	1349	1359	1364	1367	1369	1370	2157	2174	2192	2206	2209
		2222	2229	2236	2243	2256	2263	2270	2287	2294	2301			
R15	0000 000F	83*	226	246	361	367	391	395	462	462	463	648	748	749
		750	752	756	757	801	828	931	1034	1036	1311	1331	1334	1350
		1360	1365	1371	1600	1611	1621	1677	1742	1760	1762	1812	1817	1866
		1872	1929	1934	2005	2013	2041	2046	2071	2130	2138	2144	2154	2171
		2189	2203	2213	2215	2219	2226	2233	2240	2253	2260	2267	2284	2291

CHKSUM/M17 PUNCHER

TT06.1	0000	1D74	2244*	2257	2264	2288					
TT09	0000	1D8E	2046	2252*							
TT0A	0000	1DA2	2071	2259*							
TT0B	0000	1DB6	1677	2144	2266*						
TT0B.1	0000	1DC6	2271*	2295							
TT0C	0000	1DEE	1929	2283*							
TT0D	0000	1E02	2290*								
TT0E	0000	1E16	1817	2297*							
TT0E.1	0000	1E26	2223	2302*							
TTYGET	0000	1392	1074*								
UNARY	0000	10A2	442	446	770*						
UNARY1	0000	10A4	771*	775							
WASDU	0000	16C4	223	486	575	603	878	880	889	966	1441*
WASDU1	0000	16C6	463	563	891	1442*					
XI1	0000	1558	1252*	1257							
XI16	0000	150E	1134	1222*							
XI16A	0000	1556	1243	1251*							
XI2	0000	1568	1255	1258*							
XI3	0000	158A	1264	1272*							
XI32	0000	151C	1111	1151	1228*						
XI32A	0000	1538	1235	1239*							
XI4	0000	15A0	1274	1276	1279*						
XI5	0000	15A4	1278	1280*							
XIERR	0000	15A8	1253	1259	1285*						
XIEXIT	0000	15A6	1260	1281*							
ZERO	0000	1EAC	2120	2121	2367*						
ZERO1	0000	13D6	1105*	1106							
ZERO2	0000	13E6	1109*	1110							
ZERO3	0000	13F6	1113*	1114							
ZERONE	0000	0CA8	386*	1483	1484						

