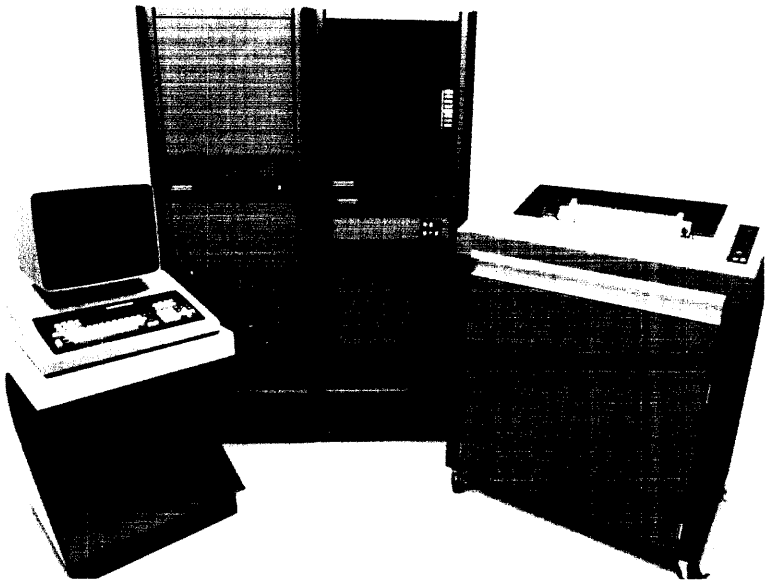


Model 8/16E Processor

PRODUCT DESCRIPTION

The Model 8/16E Processor enhances Interdata's 16-bit processor product line to provide the OEM and the End User with large-machine performance at minicomputer prices.

Interdata processors traditionally have been recognized for their superior architecture and advanced capabilities. The Interdata user enjoys the advantages of flexible hardware designed with state-of-the-art concepts. Field-proven software is completely portable across the breadth of the 16-bit product line. Interdata offers an extensive line of peripherals— discs and magnetic tapes, card readers and line printers, A/D, D/A, and Digital I/O equipment, and communications controllers.

The Model 8/16E combines hardware versatility with software compatibility to offer the user a flexible, expandable, and economical minicomputer system.

FEATURES

- Advanced Architecture
  - 16 General Purpose Registers, of which 15 can be used as Index Registers
  - IBM-like Instruction Set
  - List Processing Instructions
  - Dual I/O Bus Structure
  - 255 Automatic I/O Channels
  - Supervisor Mode
  - Integral Memory Management Hardware permitting addressing up to 262,144 bytes
  - Memory Cycle Time of 750 nanoseconds
  - Memory Access Time of 275 nanoseconds.
- Support for Extended Arithmetic Capabilities
  - Signed and Unsigned Hardware Fixed Point Multiply/Divide
  - * – Single Precision Floating Point Hardware includes 8 Hardware Single Precision Floating Point Registers
  - * – Single/Double Precision Floating Point Hardware includes 16 registers: 8 Hardware Single Precision Floating Point Registers, and 8 Hardware Double Precision Floating Point Registers.
- Built-In Reliability
  - Printed Circuit Back Panel for all Interlaced Connections
  - Thermal-Shock Testing of all Integrated Circuits
  - Vibration Testing to 1.25 G's
  - Temperature Testing – Burn-in at 50°C for 52 hours.
- Field-Proven Software
  - OS/16MT2 – A Real-Time, Multi-Tasking Operating System
  - Utilities – SORT/MERGE,OS EDIT, OS AIDS, OS COPY
  - Languages – FORTRAN IV, FORTRAN IV, BASIC II, MACRO CAL.

* EXTRA COST

SYSTEM ARCHITECTURE

The Model 8/16E's architecture, similar to that of the IBM System 360/370 line, greatly simplifies system design, programming, and debugging. The large task-oriented instruction set allows the programmer to concentrate on system programming instead of programming basic routines for functions like Exclusive OR, multiple shifts, or byte processing.

Sixteen general registers reduce overhead, cut execution time and simplify program development. Temporary results can be stored for instant recall, further reducing overhead.

Supervisor Mode is also a part of the 8/16E system architecture. When Supervisor Mode is enabled, input/output and most status switching instructions become priviledged instructions, and any attempt to execute them causes an illegal instruction interrupt to occur.

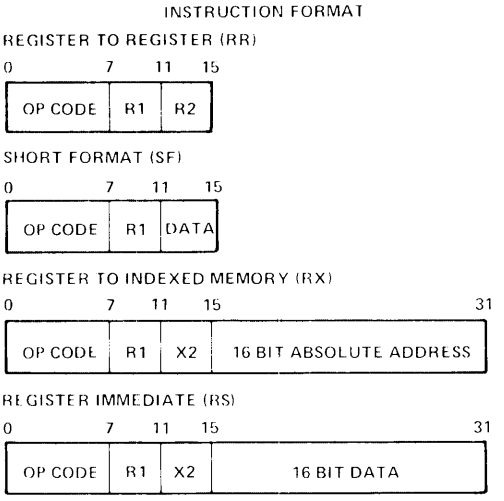
The Model 8/16E's integral memory management hardware permits expansion of physical memory beyond 64K bytes to a maximum of 256K bytes. Program mapping is performed by implementing additional bits in the Program Status Word. Logical program space is viewed as 64KB areas, regardless of physical location. Four new instructions (Load Program Status, Load Program Status Register, Set Map and Set Map Register) control these additional bits. These instructions also minimize the associated overhead incurred by user programs. Mapping for DMA operations to extended addressing areas is handled by the 16-Bit Extended Selector Channel.

The 8/16E Memory Protect Controller (MPC) provides a means of allocating selected blocks of memory to be either write protected, read/write protected, or instruction execution protected. Memory can be partitioned into a maximum of 64 blocks with individual protection for each block. Block sizes of 512 bytes, 1,024 bytes, and 2,048 bytes may be selected. The MPC also provides two loadable maps for data security and integrity: a write or read/write protect map, and an execute protect map.

With the Automatic I/O Channel, the user can service interrupts in two distinct ways. In the standard manner, the user can directly access his interrupt service routine and service the interrupt. In the second mode of operation, the user can access a unique channel control block and perform a read, write, or test operation and queue on that for I/O termination. The major advantage of the Auto I/O channel is its ability to handle the associated housekeeping of low to medium-speed devices (terminals, card readers, and line printers, for example) on the multiplexor bus.

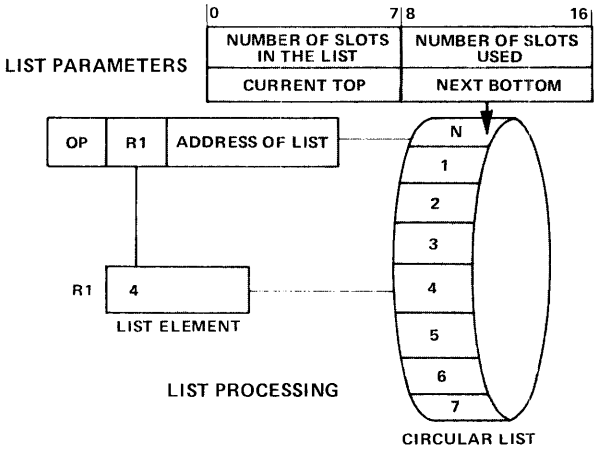
Instruction Repertoire

The basic 156 instructions provide large-machine capability which results in more time for application programming and less worry about routine functions. While the 8/16E instruction formats are similar to those of IBM 360/370 systems, Interdata has added several classes of instructions to increase memory utilization efficiency. The instruction set provides both 16-bit and 32-bit formats and permits operation between any two general registers (RR), a general register and a memory location (RX), a general register and a 16-bit data constant carried in the primary instruction word (RI), or a general register and a four-bit data constant (SF).



OP CODE = HEXADECIMAL REPRESENTATION OF FUNCTION TO BE PERFORMED (ADD, MULTI.)
R1 = ANY ONE OF 16 G.P. REGISTERS AS A FIRST OPERAND.
R2 = ANY ONE OF 16 G.P. REGISTERS AS A SECOND OPERAND.
X2 = ANY ONE OF 15 INDEX REGISTERS AS AN INDEX VALUE (ADD TO APPARENT ADDRESS OR DATA FIELD TO OBTAIN TRUE VALUE OF ADDRESS OR DATA).

The 8/16E has a list processing capability, provided by commands which manipulate any number of circular lists, each having up to 255 halfword slots. These instructions are useful for stacking and queueing functions. Elements can be added or deleted from the top or from the bottom of the list. Changes in the state of the list are effected in the Condition Code.



Arithmetic extensions including fixed and floating point instructions are available as an option. With the signed multiply/divide hardware, the number of instructions is increased to 162. Floating-point instructions provide a means of rapid manipulation of scientific data expressed as floating point numbers. Single precision and double precision instructions are implemented in hardware. Two

stacks, each containing eight registers, are dedicated to floating point operands. The comprehensive set of floating point instructions includes load, store, add, subtract, multiply, divide, compare, fix and float. The total complement of instructions, including all optional instructions, is 196.

Input/Output

The strength of the 8/16E's input/output system is based on its dual bus structure. High-speed devices can operate at a maximum of 2,666,000 bytes per second over the optional 16-bit Extended Memory Selector Channel. Medium and low-speed devices are connected to the standard Multiplexor Channel.

Operation over the Selector or Multiplexor channels may be in the 8-bit parallel or 16-bit parallel mode. Either channel operates on a request-response basis for simple, reliable device-controller design. Devices operating over the Multiplexor channel are generally interrupt-driven. Interrupts are automatically vectored for maximum machine efficiency and less software overhead.

Interdata offers a broad line of inexpensive peripherals for the Model 8/16E that are both program and interface-compatible with all members of the Interdata family. Interdata also offers standard low-cost interface modules to aid the user in designing special-purpose interfaces.

Main Memory

The Model 8/16E can accommodate up to 262,144 bytes of core memory. Memory access time is 275 nanoseconds and the memory cycle time is 750 nanoseconds.

Memory modules are contained on 15-inch printed circuit boards and are available in 32KB or 64KB increments. Parity is available as an option.

SOFTWARE

Interdata provides a comprehensive family of software products that provides support for all phases of system development, from program design and preparation through implementation and operational support of completed application systems.

The major software products are:

- OS/16 MT2 – Event-driven, multi-tasking operating system that supports a wide variety of environments and configurations, from small-scale 5/16 dedicated systems to large multi-purpose 8/16E extended memory systems.
- OS/EDIT – Flexible text editor, providing source preparation and correction facilities for any of the system programming languages.
- Extended FORTRAN IV – FORTRAN language system with a compact, efficient compiler, providing a superset of ANSI x3.9 – 1966 and an extensive Run Time Library which includes the ISA Real-Time Extensions.
- CAL – Common Assembler Language for all Interdata processors.
- * MACRO CAL – Companion product to CAL, provides powerful and flexible macro assembler facilities.
- BASIC Level II – BASIC interpreter providing a superset of the Dartmouth Standard Language. Available in two forms: single precision and double precision.
- OS AIDS – Automatic Interactive Debugging System, minimizes program and system integration times.
- SORT/MERGE – An efficient SORT/MERGE utility, optimized for 16-bit machines.
- System Utilities – A family of utilities that simplifies system operation and facilitates system maintenance and management.

All Interdata software is supported by an effective Customer Service organization, with a fully trained field staff backed by home office maintenance and support organizations.

BUILT-IN RELIABILITY

The Model 8/16E uses the latest techniques in logic design, solid-state technology, mechanical packaging, and manufacturing testing to ensure maximum hardware reliability.

A printed circuit back panel provides all interboard connections. Individual logic boards are connected to the back panel with in-line connectors.

Model 8/16E packaging is consistent with Interdata standards of ruggedness, durability, and reliability. Interboard connections are military-type pin and receptacle connectors for sure, positive connection. Separately mounted power supplies, readily accessable test points and fuses, and plug-in modules mean fewer failures and less time for repairs. Interdata's testing includes thermal shock testing of all integrated circuits. The Model 8/16E is vibration tested at 1.25 G's while running diagnostic programs. Finally, all processors are run for 52 hours at 50° C. The quality is burned in.

HARDWARE CONFIGURATION GUIDE

The Model 8/16E consists of a 19 inch-wide, 16-slot chassis, providing space for the processor board, one to four memory modules, and arithmetic and/or I/O device controllers. The 50-amp power supply is mounted externally. Standard with the 8/16E is Power Fail/Auto Restart, Automatic Bootstrap Loader, Binary Display Panel and Display Panel Interface. Each of the remaining slots can accommodate either one 15-inch board or two 7-inch boards.

A large selection of reliable peripherals and interfaces reduces risk and development costs. The Interdata peripheral family includes a complete range of magnetic tapes, discs, card and paper tape equipment, CRT displays, printers, analog and digital converters, data acquisition equipment, and communications hardware.

* EXTRA COST

Model 8/16E options provide extensive flexibility so that the hardware configuration can be tailored to the application and can be easily expanded in the field.

- Memory Protect Controller – Allows protection of selected blocks of memory.
- ✱ Memory Parity – Complete data and instruction protection.
- Hexadecimal Display Panel – Complete user control of the system. Includes hexadecimal LED readout and hexadecimal input keyboard.
- Signed Multiply/Divide – Hardware execution of 16-bit signed fixed point multiply/divide operations.
- ✱ Single Precision Floating Point – Hardware calculations using 32-bit floating point operands.
- ✱ Single/Double Precision Floating Point – Hardware calculations using 32-bit or 64-bit floating point operands.
- 16-bit Extended Memory Selector Channel – For high-speed I/O requirements, each provides completely autonomous block transfers on a cycle-stealing basis for high-speed I/O.

INTERDATA MODEL 8/16E INSTRUCTION EXECUTION TIMES

Type	Instructions	Format	Execution Time in usec
LOAD AND STORE INSTRUCTIONS	Load Halfword	RR	0.75
	Load Halfword	RX	~~2.00~~ 2.25
	Load Halfword Immediate	RI	1.50
	Load Immediate Short	SF	1.00
	Load Complement Short	SF	0.75
	Load Multiple	RX	2.75+1.00n*
	Store Multiple	RX	2.50+1.00n*
	Store Halfword	RX	2.75
FIXED POINT ARITHMETIC INSTRUCTIONS	Add Halfword	RR	0.75
	Add Halfword	RX	2.25
	Add Halfword Immediate	RI	1.50
	Add Immediate Short	SF	1.00
	Add Halfword to Memory	RX	3.25
	Add with Carry Halfword	RR	1.00
	Add with Carry Halfword	RX	2.50
	Subtract Halfword	RR	0.75
	Subtract Halfword	RX	2.25
	Subtract Halfword Immediate	RI	1.50
	Subtract Immediate Short	SF	1.00
	Subtract w/Carry Halfword	RR	1.00
	Subtract w/Carry Halfword	RX	2.50
	Compare Halfword	RR	1.25
	Compare Halfword	RX	2.75
	Compare Halfword Immediate	RI	2.00
	Multiply Halfword	RR	7.50
	Multiply Halfword	RX	9.00
	Multiply Halfword Unsigned	RR	5.75
	Multiply Halfword Unsigned	RX	7.25
	Divide Halfword	RR	10.25
	Divide Halfword	RX	12.25
FIXED POINT LOGICAL INSTRUCTIONS	AND Halfword	RR	0.75
	AND Halfword	RX	2.25
	AND Halfword Immediate	RI	1.50
	OR Halfword	RR	0.75
	OR Halfword	RX	2.25
	OR Halfword Immediate	RI	1.50
	Exclusive OR Halfword	RR	0.75
	Exclusive OR Halfword	RX	2.25
	Exclusive OR Halfword Immediate	RI	1.50
	Compare Logical Halfword	RR	0.75
	Compare Logical Halfword	RX	2.25
	Compare Logical Halfword Immediate	RI	1.50
	Test Halfword Immediate	RI	1.50

Type	Instructions	Format	Execution Time in usec
SHIFT AND ROTATE INSTRUCTIONS	Shift Right Halfword Logical	RI	4.00+.25(n-1)*
	Shift Right Logical Short	SF	2.25+.25(n-1)*
	Shift Right Logical (Fullword)	RI	5.00+.25(n-1)*
	Shift Left Halfword Logical	RI	3.75+.25(n-1)*
	Shift Left Logical Short	SF	2.00+.25(n-1)*
	Shift Left Logical (Fullword)	RI	4.75+.25(n-1)*
	Shift Right Halfword Arithmetic	RI	5.50+.25(n-1)*
	Shift Right Arithmetic (Fullword)	RI	6.25+1.5(n-1)*
	Shift Left Halfword Arithmetic	RI	4.75+.25(n-1)*
	Shift Left Arithmetic (Fullword)	RI	6.00+.25(n-1)*
	Rotate Right Logical (Fullword)	RI	5.00+.25(n-1)*
	Rotate Left Logical (Fullword)	RI	5.00+.25(n-1)*
SINGLE PRECISION FLOATING POINT INSTRUCTIONS	Load Floating Point Register	RX	2.25
	Load Floating Point	RX	5.00
	Load Floating Point Multiple	RX	5.75+2.75(n-1)*
	Store Floating Point	RX	4.50
	Store Floating Point Multiple	RX	4.75+2.75(n-1)*
	Add Floating Point Register	RR	3.50
	Add Floating Point	RX	5.75
	Subtract Floating Point Register	RR	3.50
	Subtract Floating Point	RX	5.75
	Compare Floating Point Register	RR	2.50
	Compare Floating Point	RX	5.25
	Multiply Floating Point Register	RR	10.25
	Multiply Floating Point	RX	12.25
	Divide Floating Point Register	RR	10.75
	Divide Floating Point	RX	13.00
	Fix Register	RR	6.25
	Float Register	RR	4.50
DOUBLE PRECISION FLOATING POINT INSTRUCTIONS	Load Floating Point Register	RR	2.25
	Load Floating Point	RX	7.00
	Load Floating Point Multiple	RX	7.75+4.75(n-1)*
	Store Floating Point	RX	6.25

✱EXTRA COST

INTERDATA MODEL 8/16E INSTRUCTION EXECUTION TIMES (Continued)

Type	Instructions	Format	Execution Time in usec
DOUBLE PRECISION FLOATING POINT INSTRUC-TIONS (CONT.)	Store Floating Point Multiple	RX	6.75+4.75(n-1)*
	Add Floating Point Register	RR	3.50
	Add Floating Point	RX	7.75
	Subtract Floating Point Register	RR	3.50
	Subtract Floating Point	RX	7.75
	Compare Floating Poin Register	RR	2.50
	Compare Floating Poin	RX	7.00
	Multiply Floating Point Register	RR	16.25
	Multiply Floating Point	RX	20.25
	Divide Floating Point Register	RR	16.75
	Divide Floating Point	RX	21.00
	Fix Register	RR	6.25
	Float Register	RR	4.25
BYTE PROCESSING INSTRUC-TIONS	Load Byte	RR	1.25
	Load Byte	RX	3.00
	Store Byte	RR	2.00
	Store Byte	RX	3.75
	Exchange Byte	RR	1.00
	Compare Logical Byte	RX	3.00
CONDITIONAL BRANCH INSTRUC-TIONS	Branch on True Condition	RR	1.25
	Branch on True Condition	RX	2.00
	Branch on True Condition Backward	SF	2.25
	Branch on True Condition Forward	SF	2.00
	Branch and Link	RR	1.25
	Branch and Link	RX	2.00
	Branch on Index Low or Equal	RX	3.00
	Branch on Index High	RX	3.25
	Branch on Zero	RR	1.25
	Branch on Zero	RX	2.00
	Branch on Zero Backward	RX	2.25
	Branch on Zero Forward	RX	2.00
	Branch on Not Zero	RR	1.25
	Branch on Not Zero	RX	2.00
	Branch on Not Zero Backward	SF	2.25
	Branch on Not Zero Forward	SF	2.00
	Branch on Plus	RR	1.25
	Branch on Plus	RX	2.00
	Branch on Plus Backward	SF	2.25
	Branch on Plus Forward	SF	2.00
	Branch on Not Plus	RR	1.25
	Branch on Not Plus	RX	2.00
	Branch on Not Plus Backward	SF	2.25
	Branch on Not Plus Forward	SF	2.00
	Branch on Minus	RR	1.25
	Branch on Minus	RX	2.00
	Branch on Minus Backward	SF	2.25
	Branch on Minus Forward	SF	2.00
	Branch on Not Minus	RR	1.25
	Branch on Not Minus	RX	2.00
	Branch on Not Minus Backward	SF	2.25
	Branch on Not Minus Forward	SF	2.00

Type	Instructions	Format	Execution Time in usec
CONDITIONAL BRANCH INSTRUC-TIONS (Continued)	Branch on Carry	RR	1.25
	Branch on Carry	RX	2.00
	Branch on Carry Backward	SF	2.25
	Branch on Carry Forward	SF	2.00
	Branch on No Carry	RR	1.25
	Branch on No Carry	RX	2.00
	Branch on No Carry Backward	SF	2.25
	Branch on No Carry Forward	SF	2.00
	Branch on Overflow	RR	1.25
	Branch on Overflow	RX	2.00
	Branch on Overflow Backward	SF	2.25
	Branch on Overflow Forward	SF	2.00
	Branch on No Overflow	RR	1.25
	Branch on No Overflow	RX	2.00
	Branch on No Overflow Backward	SF	2.25
	Branch on No Overflow Forward	SF	2.00
	Branch on Low	RR	1.25
	Branch on Low	RX	2.00
	Branch on Low Backward	SF	2.25
	Branch on Low Forward	SF	2.00
	Branch on Not Low	RR	1.25
	Branch on Not Low	RX	2.00
	Branch on Not Low Backward	SF	2.25
	Branch on Not Low Forward	SF	2.00
	Branch on Equal	RR	1.25
	Branch on Equal	RX	2.00
	Branch on Equal Backward	SF	2.25
	Branch on Equal Forward	SF	2.00
	Branch on Not Equal	RR	1.25
	Branch on Not Equal	RX	2.00
	Branch on Not Equal Backward	SF	2.25
	Branch on Not Equal Forward	SF	2.00
	Branch	RR	1.25
	Branch	RX	2.00
	Branch Backward	SF	2.25
	Branch Forward	SF	2.00
	No Operation	RR	1.00
	No Operation	RX	1.75
STATUS AND CONTROL INSTRUC-TIONS	Load Program Status Field	RX	4.25
	Load Program Status Field Register	RR	3.00
	Set Map	RX	5.75
	Set Map Register	RR	4.50
	Exchange Program Status Word	RR	3.00
	Load Status Word	RX	5.25
	Supervisor Call	RX	6.00
	Simulate Interrupt	RX	7.00
LIST PROCESSING INSTRUC-TIONS	Add to Top of List	RX	2.75
	Add to Bottom of List	RX	2.75
	Remove from Top of List	RX	2.50
	Remove from Bottom of List	RX	2.50

INTERDATA MODEL 8/16E INSTRUCTION EXECUTION TIMES (Continued)

Type	Instructions	Format	Execution Time in usec
INPUT/ OUTPUT INSTRUC- TIONS	Autoload	RX	4.75+3.75n*
	Read Data Byte	RR	2.50
	Read Data Byte	RX	4.50
	Read Halfword	RR	2.75
	Read Halfword	RX	5.50
	Read Block	RR	3.50+0.75r +3.75n
	Read Block	RX	4.25+3.75n*
	Write Data	RR	2.50
	Write Data	RX	3.75
	Write Halfword	RR	2.75
	Write Halfword	RX	4.00
	Write Block	RR	3.50+0.75r+ 3.75n*
	Write Block	RX	4.25+3.75n*
	Sense Status	RR	2.50
	Sense Status	RX	5.00
	Output Command	RR	3.25
	Output Command	RX	4.75
	Acknowledge Interrupt	RR	3.25
	Acknowledge Interrupt	RX	5.75

*Note: n = number of shifts or registers or number of bytes transferred
r = number of registers

SPECIFICATIONS

Technology	
Processor	STTL, LSTTL ROM Bipolar (60 ns access time)
Data Word Length	8, 16, 32, 64 bits
Instruction Word Length	16, 32 bits
Number of Basic Instructions	156
With Fixed Point Multiply/Divide	162
With Single Precision Floating Point	179
With Single/Double Precision Floating Point	196
Fixed Point Arithmetic	2's complement
Hardware Accumulators	
16 Fixed Point	16 bit
8 Single Precision Floating Point	32 bit
8 Double Precision Floating Point	64 bit
Hardware Index Registers	15
Address Modes	Direct, Indexed, Relative, and Extended
Input/Output	
DMA Capabilities	
Four High Speed DMA Channels standard	
Maximum 16 bit ESELCH transfer rate 2.66 megabytes/sec	
Input/Output word length - 8 or 16 bits	
Multiplexor Input/Output	
Programmed I/O loop rate - 90.9 KB	
255 priority interrupt levels	
Interrupt response time – 8.0 μsec	
Environmental	
Temperature	0 to 50° C
Humidity	0 to 90% (non-condensing)
Vibration	0 to 55 Hz at 1.25 G's
Operating Temp.	0°C to 50°C
Storage Temp.	–55°C to +85°C

The information contained herein is intended to be a general description and is subject to change with product enhancement

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INTERDATA PRODUCT NUMBERS

M81-010	8/16E Processor with 32KB Memory
M81-011	8/16E Processor with 64KB Memory
M81-012	8/16E Processor with 96KB Memory
M81-013	8/16E Processor with 128KB Memory
M81-014	8/16E Processor with 160KB Memory
M81-015	8/16E Processor with 192KB Memory
M81-016	8/16E Processor with 224KB Memory
M81-017	8/16E Processor with 256KB Memory
M81-020	8/16E Processor with 32KB Parity Memory
M81-021	8/16E Processor with 64KB Parity Memory
M81-022	8/16E Processor with 96KB Parity Memory
M81-023	8/16E Processor with 128KB Parity Memory
M81-024	8/16E Processor with 160KB Parity Memory
M81-025	8/16E Processor with 192KB Parity Memory
M81-026	8/16E Processor with 224KB Parity Memory
M81-027	8/16E Processor with 256KB Parity Memory
M83-300	32KB Expansion Memory Module
M83-301	32KB Expansion Memory Module with Parity
M83-302	64KB Expansion Memory Module
M83-303	64KB Expansion Memory Module with Parity
M81-113	Hexadecimal Display Panel
M81-109	OS/16MT2 Loader Program
M81-110	1024 Bytes Read-Only Memory
M81-112	Fixed Point Multiply/Divide
M81-100	Single Precision Floating Point
M81-101	Single/Double Precision Floating Point
M81-114	Programmable Memory Protect Controller
M81-115	16-bit Extended Selector Channel

RELATED DOCUMENTATION

29-633	8/16E Users Manual
29-618	8/16E Maintenance and Installation Manual
29-619	16-Bit Extended Selector Channel Maintenance and Installation Manual
29-620	16-Bit Extended Selector Channel Programming Manual
29-621	8/16E Memory Protect Controller Maintenance Manual
29-622	8/16E Memory Protect Controller Programming Manual

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