iSBC 534™ FOUR CHANNEL COMMUNICATIONS EXPANSION BOARD HARDWARE REFERENCE MANUAL

Manual Order Number: 9800450-02

Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Additional copies of this manual or other Intel literature may be obtained from:

Literature Department
Intel Corporation
3065 Bowers Avenue
Santa Clara, CA 95051

The information in this document is subject to change without notice.

Intel Corporation makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Intel Corporation assumes no responsibility for any errors that may appear in this document. Intel Corporation makes no commitment to update nor to keep current the information contained in this document.

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied.

The following are trademarks of Intel Corporation and may be used only to describe Intel products:

i
ICE
iCS
Insite
Intel
Intellec
iSBC
Library Manager
MCS
Megachassis
Micromap
Multibus
Multimodule
PROMPT
Promware
RMX
UPI
μScope

and the combination of ICE, iCS, iSBC, MCS, or RMX and a numerical suffix.

Printed in U.S.A./A61/479/5K/CP

PREFACE

This manual provides general information, preparation for use, programming information, principles of operation, and service information for the iSBC 534 Four Channel Communications Expansion Board. Supplementary information is provided in the following documents:

- *Intel MULTIBUS Interfacing,* Application Note AP-28.
- Intel 8080 Microcomputer Peripherals User's Manual, Order No. 98-364.
- Intel 8080/8085 Assembly Language Programming Manual, Order No. 98-301A.

CONTENTS

CHAPTER 1

GENERAL INFORMATION

CHAPTER 2

PREPARATION FOR USE

CHAPTER 3

PROGRAMMING INFORMATION

CHAPTER 4

PRINCIPLES OF OPERATION

CONTENTS (Continued)

ILLUSTRATIONS

TABLES

CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The iSBC 534 Four Channel Communications Expansion Board is a member of a complete line of Intel iSBC 80 system expansion modules. The iSBC 534, which provides an expansion of system serial communications capability, includes four fully programmable synchronous and asynchronous serial I/O channels with RS232C buffering. Each serial I/O channel can be optionally configured by the user for 20-milliampere optically isolated current-loop buffering. Baud rates, data formats, and interrupt priorities are individually software selectable for each channel. The iSBC 534 also includes 16 lines of RS232C buffered parallel I/O lines.

1-2. DESCRIPTION

The iSBC 534 (figure 1-1) is designed to be plugged into a standard iSBC 604/614 Modular Backplane and Cardcage to interface directly with an Intel iSBC 80 Single Board Computer or used with an Intel Microcomputer Development System. The iSBC 534 provides four serial I/O ports, one parallel I/O port, six programmable timers, and sixteen interrupt inputs with programmable priority.

1-3. SERIAL I/O PORTS

Each of the four serial I/O ports is fully RS232C plug compatible and is controlled and interfaced by an Intel 8251 USART (Universal Synchronous/Asynchronous Receiver/Transmitter) chip. Each USART is individually programmable for operation in most synchronous or asynchronous serial data transmission formats (including IBM Bi-Sync).

In the synchronous mode the following are programmable:

a. Character length,
b. Sync character (or characters), and
c. Parity.

In the asynchronous mode the following are programmable:

a. Character length,
b. Baud rate factor (clock divide ratios of 1, 16, or 64),
c. Stop bits, and
d. Parity.

In both the synchronous and asynchronous modes, each serial I/O port features half- or full-duplex, double-buffered transmit and receive capability. In addition, USART error detection circuits can check for parity, overrun, and framing errors. The USART transmit and receive clock rates are separately derived from one of six independently programmable Baud rate/time generators.

Each serial I/O port accepts optional user-supplied input and output optical isolators for applications that require isolated current loops. All other required components are supplied. Using the recommended optical isolators and internal voltage sources, the iSBC 534 can supply up to 20 mA to an external loop. Each serial I/O port is converted rapidly to a current loop by installing optical-isolators in sockets on the board, and then moving an 18-pin DIP header jumper assembly; one prewired DIP header jumper assembly is included for each serial I/O port.

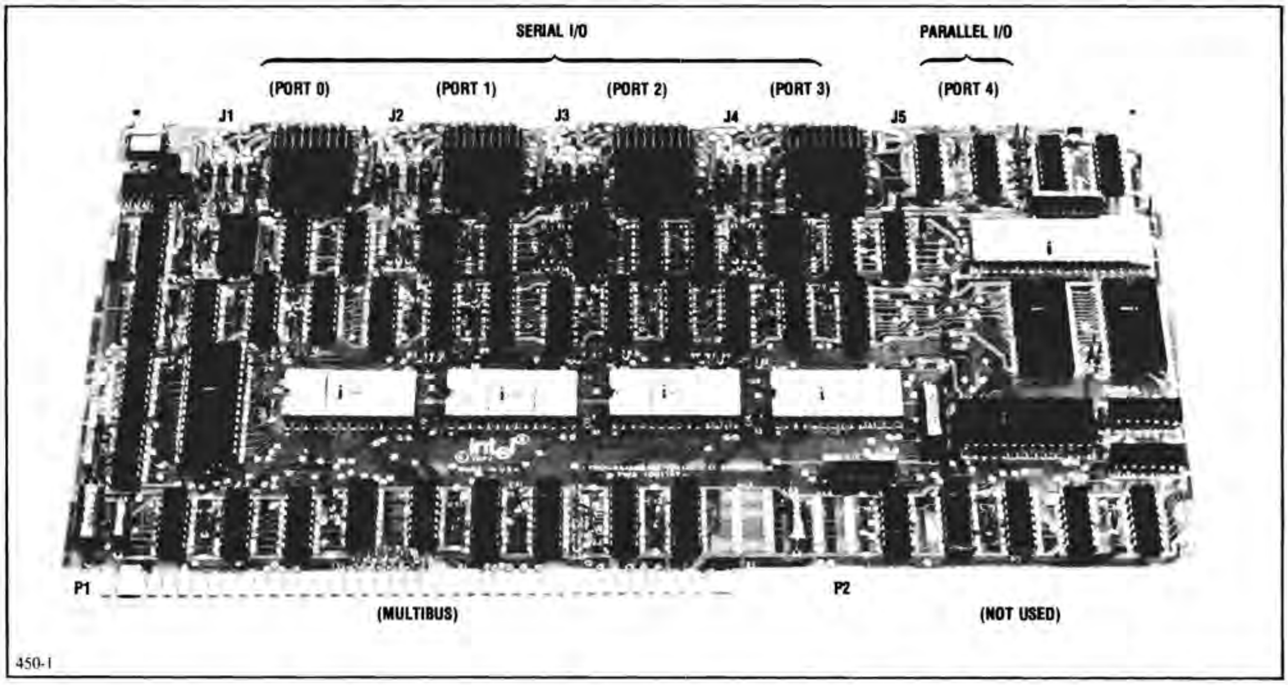


Figure 1-1. iSBC 534 Four Channel Communications Expansion Board

1-4. PARALLEL I/O PORT

The parallel I/O port has 16 buffered I/O lines controlled by an Intel 8255 Programmable Peripheral Interface (PPI) chip. The parallel I/O port is directly compatible with an Automatic Calling Unit (ACU) such as the Bell Model 801, or equivalent, and can also be used for auxiliary functions. All signals are RS232C compatible, and the interface cable signal assignments meet RS366 specifications.

If the system application does not require an interface to an ACU, the parallel I/O port can be used for any general purpose or auxiliary parallel interface that is RS232C compatible.

1-5. PROGRAMMABLE TIMERS

One of the primary features of the iSBC 534 is flexible clock programming. The iSBC 534 has two Intel 8253 Programmable Interval Timer (PIT) chips that provide a total of six separate time/rate generators. All six are independently software-programmable, and can generate different Baud rate clock signals for each USART chip.

Four of the timers are used as Baud rate clock generators; the two remaining timers can be used for miscellaneous functions such as generating different transmit and receive clock frequencies or real-time interrupt intervals.

1-6. INTERRUPT FUNCTIONS

The iSBC 534 has 16 interrupt functions managed by two Intel 8259 Programmable Interrupt Controller (PIC) chips: PIC 0 and PIC 1. Each PIC has eight input interrupt request lines as follows:

a. PIC 0
   (1) Transmit Ready (TXRDY) from each serial I/O port.
   (2) Receive Ready (RXRDY) from each serial I/O port.

b. PIC 1
   (1) Timer signal from each PIT chip.
   (2) Carrier Detect (CD) from each serial I/O port.
   (3) Logic OR of Ring Indicator (RI) from each serial I/O port.
   (4) Present Next Digit (PND) from parallel I/O port, or an external interrupt when this port is not used with an ACU.

Each PIC treats each true input signal condition as an interrupt request. After resolving the interrupt priority, the PIC issues a single interrupt request to the main processor. Interrupt priorities of both PIC chips are independently programmable under software control. Similarly, any interrupt can be masked under software control. The programmable interrupt priority modes are:

a. Fully Nested Priority. Each interrupt request has a fixed priority: input 0 is highest, input 7 is lowest.

b. Auto-Rotating Priority. Each interrupt request has equal priority. Each level, after receiving service, becomes the lowest priority level until the next interrupt occurs.

c. Specific Priority. Software assigns lowest priority. Priority of all other levels is in numerical sequence based on lowest priority.

The interrupt output from each PIC chip can be jumper-wired to drive one of nine interrupt lines on the Multibus.

NOTE

Since the PIC chips are remote from the system processor, they can be operated only in the polled mode.

1-7. EQUIPMENT SUPPLIED

The following are supplied with the iSBC 534 Four Channel Communications Expansion Board:

a. Schematic Diagram, dwg. no. 2001199.
b. Assembly Drawing, dwg. no. 1001197.

1-8. SPECIFICATIONS

Specifications for the iSBC 534 Four Channel Communications Expansion Board are provided in table 1-1.

Table 1-1. Specifications

SERIAL COMMUNICATIONS	
Synchronous:	5-, 6-, 7-, or 8-bit characters. Internal; 1 or 2 sync characters. Automatic sync insertion.
Asynchronous:	5-, 6-, 7-, or 8-bit characters. Break character generation. 1, 1½, or 2 stop bits. False start bit detection.

Table 1-1. Specifications (Continued)

Sample Baud Rate:

Frequency[1] (kHz, Software Selectable)	Baud Rate (Hz)[2]		
	Synchronous	Asynchronous	
		÷16	÷64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

Notes: 1. Frequency selected by I/O writes of appropriate 16-bit frequency factor to Baud Rate Register.

2. Baud rates shown here are only a sample subset of possible software-programmable rates available. Any frequency from 18.75 Hz to 614.4 kHz may be generated utilizing on-board crystal oscillator and 16-bit Programmable Interval Timer (used here as frequency divider).

INTERVAL TIMER AND BAUD RATE GENERATOR

Input Frequency: On board 1.2288 MHz ±0.1% crystal; 0.814 microsecond period, nominal.

Output Frequencies:

Function	Single Timer		Dual Timers (Two Timers Cascaded)	
	Min.	Max.	Min.	Max.
Real-Time Interrupt Interval	1.63 μsec	53.3 msec	3.26 μsec	58.25 minutes
Rate Generator (Frequency)	18.75 Hz	614.4 kHz	0.00029 Hz	307.2 kHz

INTERFACE COMPATIBILITY

Serial I/O: EIA Standard RS232C signals provided and supported:

Carrier Detect
Clear to Send
Data Set Ready
Data Terminal Ready
Request to Send
Receive Clock

Receive Data
Ring Indicator
Secondary Receive Data
Secondary Transmit Data
Transmit Clock
Transmit Data

Parallel I/O: 8 input lines and 8 output lines; all signals compatible with EIA Standard RS232C. Directly compatible with Bell Model 801 Automatic Calling Unit.

System Bus: Compatible with Intel iSBC 80 Multibus.

Table 1-1. Specifications (Continued)

I/O ADDRESSING: The USART, Interval Timer, Interrupt Controller, and Parallel Interface registers are configured as a block of 16 I/O address locations. The location of this block is jumper-selectable to begin at any 16-byte I/O address boundary (i.e., 00H, 10H, 20H, . . . F0H).

I/O ACCESS TIME: 400 nanoseconds.

COMPATIBLE CONNECTORS/CABLE:

Interface	No. of Pins	Centers (in.)	Mating Connectors	Cable
Multibus	86	0.156	EBY CD34AE013 EDAC 337086540202	N/A
Serial and Parallel I/O	26	0.1	3M 3462-000 or TI H312113	Intel iSBC 955

COMPATIBLE OPTO-ISOLATORS:
(20 mA current loop interface)

Function	Supplier	Part Number
Driver	Fairchild General Electric Monsanto	4N33
Receiver	Fairchild General Electric Monsanto	4N37

POWER REQUIREMENTS:

Voltage	Without Opto-Isolators	With Opto-Isolators[1]
$V_{CC} = +5V$	1.9A, max.	1.9A, max.
$V_{DD} = +12V$	275 mA, max.	420 mA, max.
$V_{AA} = -12V$	250 mA, max.	400 mA, max.

Note: 1. With four 4N33 and four 4N37 Opto-Isolator packages installed in sockets provided to implement four 20 mA current loop interfaces.

ENVIRONMENTAL REQUIREMENTS

Operating Temperature:	0° to 55°C (32° to 131°F).
Relative Humidity:	To 90% without condensation.

PHYSICAL CHARACTERISTICS

Width:	30.48 cm (12.00 inches).
Depth:	17.15 cm (6.75 inches).
Thickness:	1.27 cm (0.50 inch).
Weight:	397 gm (14 ounces).

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for installing the iSBC 534 Four Channel Communications Expansion Board. These instructions include unpacking and inspection; installation considerations such as power and cooling requirements, physical dimensions, and bus interface requirements; jumper configurations; optional component installation; data set conversion; external current loop considerations; device interface cabling; and board installation.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, contact the Intel Technical Support Center (see paragraph 5-4) to obtain a Return Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

2-3. INSTALLATION CONSIDERATIONS

The iSBC 534 is designed for interface with an Intel iSBC 80 Single Board Computer based system or an Intel Intellec Microcomputer Development System. Important installation and interfacing criteria are presented in following paragraphs.

2-4. POWER REQUIREMENT

The iSBC 534 requires +5V, +12V, and −12V power supply inputs. The currents required from these supplies are listed in table 1-1. For installation in an iSBC 80 Single Board Computer based system, ensure that the system power supply has sufficient current overhead to accommodate the additional requirements. For installation in an Intellec System, calculate the total +5V, +12V, and −12V current requirements for the standard modules and all installed optional modules. Ensure that the additional maximum current requirements will not exceed the capacity of the system power supply.

2-5. COOLING REQUIREMENT

The iSBC 534 dissipates 275 gram-calories/minute (1.11 Btu/minute) and adequate circulation of air must be provided to prevent a temperature rise above 55°C (131°F). The System 80 enclosures and the Intellec System include fans to provide adequate intake and exhaust of ventilating air.

2-6. PHYSICAL DIMENSIONS

Physical dimensions of the iSBC 534 are as follows:

a.	Width:	30.48 cm (12.00 inches)
b.	Height:	17.15 cm (6.75 inches)
c.	Thickness:	1.25 cm (0.50 inch)

2-7. BUS INTERFACE REQUIREMENT

The iSBC 534 is designed for installation in a standard Intel iSBC 604/614 Modular Backplane and Cardcage or in the Intellec System motherboard. As shown in figure 1-1, edge connector P1 provides interface to the Multibus. Connector P1 pin assignments are listed in table 2-1 and descriptions of the signal functions are given in table 2-2; an alternative mating connector is specified in table 1-1. Edge connector P2 is not used.

The ac and dc characteristics of the iSBC 534 are presented in tables 2-3 and 2-4, respectively. The bus exchange timing for I/O Read and Write operations is shown in figure 2-1.

Table 2-1. Connector P1 Pin Assignments

PIN*	SIGNAL	FUNCTION	PIN*	SIGNAL	FUNCTION
1	GND	Ground	44		
2	GND		45		
3	+5 VDC	Power input	46		
4	+5 VDC		47		
5	+5 VDC		48		
6	+5 VDC		49		
7	+12 VDC		50		
8	+12 VDC		51	ADR6/	Address bus
9			52	ADR7/	
10			53	ADR4/	
11	GND	Ground	54	ADR5/	
12	GND		55	ADR2/	
13			56	ADR3/	
14	INIT/	System Initialize	57	ADR0/	
15			58	ADR1/	
16			59		
17			60		
18			61		
19			62		
20			63		
21	IORC/	I/O Read Command	64		
22	IOWC/	I/O Write Command	65		
23	XACK/	Transfer Acknowledge	66		
24			67	DAT6/	Data bus
25	AACK/	Advanced Acknowledge	68	DAT7/	
26			69	DAT4/	
27			70	DAT5/	
28			71	DAT2/	
29			72	DAT3	
30			73	DAT0/	
31			74	DAT1/	
32			75	GND	Ground
33	INTR/	Direct Interrupt Request	76	GND	
34			77		
35	INT6/	Interrupt request on level 6	78		
36	INT7/	Interrupt request on level 7	79	−12 VDC	Power input
37	INT4/	Interrupt request on level 4	80	−12 VDC	
38	INT5/	Interrupt request on level 5	81	+5 VDC	
39	INT2/	Interrupt request on level 2	82	+5 VDC	
40	INT3/	Interrupt request on level 3	83	+5 VDC	
41	INT0/	Interrupt request on level 0	84	+5 VDC	
42	INT1/	Interrupt request on level 1	85	GND	Ground
43			86	GND	

*All unassigned pins are reserved.

Table 2-2. Multibus Signal Functions

SIGNAL	FUNCTIONAL DESCRIPTION
AACK/	*Advanced Acknowledge:* This signal is issued by the iSBC 534 in response to an I/O Read or an I/O Write Command. The AACK/signal allows the system controller to proceed with the current instruction cycle without waiting for the iSBC 534 to complete processing the I/O command.
ADR0/-ADR7/	*Address:* These eight lines transmit the address of the I/O function or port to be accessed. ADR7/ is the most-significant bit.
DAT0/-DAT7/	*Data:* These eight bidirectional data lines transmit and receive data to and from the addressed I/O function or port. DAT7/ is the most-significant bit.
INIT/	*Initialization:* Resets the iSBC 534 to a known internal state.
INTR/	*Direct Interrupt Request:* Supports coded interrupt requests in special applications of interrupt structure.
INT0/-INT7/	*Interrupt:* These eight lines are used for inputting interrupt requests to the system controller. INT0/ has the highest priority and INT7/ has the lowest priority.
IORC/	*I/O Read Command:* Indicates that the address of an I/O function or port is on the Multibus address lines and that the output of that function is to be read (placed) onto the Multibus data lines.
IOWC/	*I/O Write Command:* Indicates that the address of an I/O function or port is on the Multibus address lines and that the contents on the Multibus data lines are to be accepted by the addressed function.
XACK/	*Transfer Acknowledge:* Indicates that the addressed I/O function or port has completed the specified I/O Read or I/O Write operation. That is, data has been placed onto or accepted from the Multibus data lines.

Table 2-3. iSBC 534 AC Characteristics

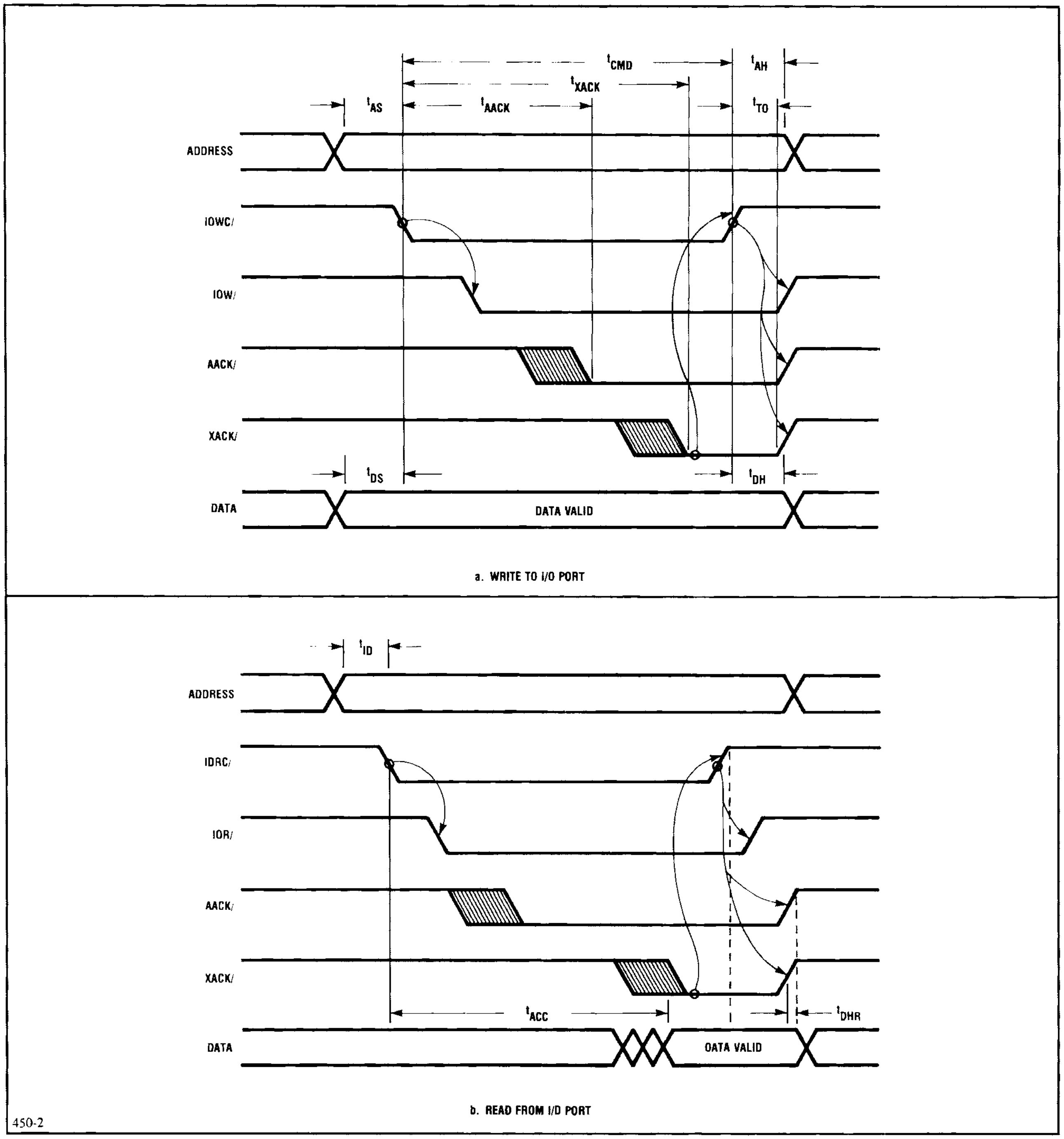
PARAMETER	MINIMUM (nsec)	MAXIMUM (nsec)	DESCRIPTION	REMARKS
t_{AS}	50		Address Setup to Command	
t_{DS}	50		Write Data Setup to Command	
t_{AACK}	69	165	Command to Advanced Acknowledge	Jumper 108-114
t_{XACK}		535	Command to Transfer Acknowledge	
t_{CMD}	420		Command	
t_{AH}	50		Address Hold Time	
t_{DH}	50		Write Data Hold Time	
t_{DHR}	0		Read Data Hold Time	
t_{TO}		60	Acknowledge Turn Off Delay	
t_{ACC}		397	Access Time to Read Data	
t_{CY}		595	Minimum Cycle Time	$t_{XACK} + t_{TO}$

Table 2-4. iSBC 534 DC Characteristics

SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
ADR0/-ADR7/	V_{I}	Input Low Voltage	V_{CC} = 5.0V		0.85	V
INIT/	V_{IH}	Input High Voltage	V_{CC} = 5.0V	2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		−0.25	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.7V		10	μA
	*C_{L}	Capacitive Load			6	pF
AACK/	$V\ _{L}$	Output Low Voltage	I_{OL} = 32 mA		0.4	V
XACK/	V_{OH}	Output High Voltage	I_{OH} = −5.2 mA	2.4		V
	I_{LH}	Output Leakage High	V_{O} = 2.4V		40	μA
	I_{LL}	Output Leakage Low	V_{O}= 0.4V		−40	μA
	*C	Capacitive Load			15	pF
DAT0/-DAT7/	V_{OL}	Output Low Voltage	I_{OL} = 50 mA		0.6	V
	V_{OH}	Output High Voltage	I_{OH} = −10 mA	2.4		V
	V_{IL}	Input Low Voltage			0.95	V
	V_{IH}	Input High Voltage		2.0		V
	I_{I}	Input Current at Low V	V_{IN} = 0.45 V		−0.25	mA
	I_{L}	Output Leakage High	V_{O} = 5.25V		100	μA
	*C_{L}	Capacitive Load			18	pF
INTR/	V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.4	V
INT0/-INT7/	V_{O}	Output High Voltage	OPEN COLLECTOR			
	*C_{L}	Capacitive Load			18	pF
IOWC/	V_{IL}	Input Low Voltage			0.8	V
IORC/	V_{I}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		−0.36	mA
	I_{I}	Input Current at High V	V_{IN} = 2.7V		20	μA
	*C_{L}	Capacitive Load			12	pF
RS232C	V_{TH}	Input High Threshold Voltage		1.75	2.25	V
Inputs	V_{TL}	Input Low Threshold Voltage		.75	1.25	V
	I	Input Current	V_{I} = +3V	+.43		mA
			V_{IN} = −3V	−.43		mA
RS232C	V_{O}	High Level Output Voltage		9.0		V
Outputs	V_{O}	Low Level Output Voltage		−9.0		V
	I_{O} +	High Level SS Output Current		−6.0	−12.0	mA
	I_{OS}−	Low Level SS Output Current		6.0	12.0	mA
†Current Loop	$I_{C\ ON}$	ON Current	V_{CE} = 2V	30	60	mA
Outputs						
TXD IN,OUT	$I_{C\ OFF}$	OFF Current	V_{CE} = 10V		10	μA
	$V_{CE\ SAT}$	ON Forward Voltage	I_{C} = 2 mA		1	V
†Current Loop	$I_{F\ ON}$	ON Input Current		8	80	mA
Inputs						
RXD IN, OUT	$I_{F\ OFF}$	OFF Input Current			2	mA
	V_{F}	Forward Input Voltage	I_{F} = 15 mA		1.5	V
Current Loop	$I_{TX\ R}$	TXD RETURN SS OUTPUT Current	V_{O} = 0V	−27	−34	mA
Return Outputs						
	$I_{RX\ R}$	RXD RETURN SS OUTPUT Current	V_{O} = 0V	19	23	mA

*Capacitance values are approximations only.

†Typical values using 4N33 Opto Isolator Drivers and 4N37 Opto Isolator Receivers.



a. WRITE TO I/O PORT

b. READ FROM I/O PORT

Figure 2-1. Bus Exchange Timing

2-8. JUMPER CONFIGURATION

The iSBC 534 provides the user with the capability of selecting the I/O base address, clock frequency, interval timer, advanced acknowledge, system interrupts, etc. Table 2-5 summarizes these jumper-selectable options and lists the grid reference locations of the jumpers as shown in figure 5-1 (parts location diagram) and figure 5-2 (schematic diagram). Because the schematic diagram consists of seven sheets, grid references to figure 5-2 consist of four alphanumeric characters. For example, grid reference 1ZB7 signifies sheet 1 Zone B7.

Study table 2-5 carefully while making reference to figure 5-2. If the default (factory configured) jumper wiring is appropriate for a particular function, no further action is required for that particular function. If, however, a different configuration is required, remove the default jumper(s) and install an optional jumper (or jumpers) as required. Clarification of jumper-selectable options is given in the following paragraphs.

Table 2-5. Jumper Selectable Options

FUNCTION	FIG. 5-1 GRID REF.	FIG. 5-2 GRID REF.	DESCRIPTION
I/O Base Address	ZB5,ZB6	1ZB7	One jumper wire to select hexadecimal I/O base address as follows (refer to paragraph 2-9): I/O BASE ADDRESS — JUMPER — I/O BASE ADDRESS — JUMPER 00 — 124-125 — 80 — 120-125 10 — 124-126 — 90 — 120-126 20 — 123-125 — A0 — 119-125 30 — 123-126 — B0 — 119-126 40 — 122-125 — C0 — *118-125 50 — 122-126 — D0 — 118-126 60 — 121-125 — E0 — 117-125 70 — 121-126 — F0 — 117-126
Counter Clock Frequency	ZC8	2ZB5, 2ZC5	One jumper wire to select counter clock frequency of 1.2288 MHz or 2.4576 MHz as follows (refer to paragraph 2-10): *62-63 = 1.2288 MHz 61-62 = 2.4576 MHz
Internal Timer	ZB3	2ZB6, 2ZC6	One jumper wire to connect timer sections of PIT 1 in parallel or series as follows (refer to paragraph 2-11): *105-106 = parallel 105-104 = series
Advanced Acknowledge	ZB7	2ZD2	One jumper wire to select either the normal Advanced Acknowledge (AACK/) or early AACK/ in response to Read and Write Commands (refer to paragraph 2-12). Jumper connection is as follows: *115-116 open = normal AACK/ 115-116 installed = early AACK/
Interrupts	ZB6,ZB7	2ZA2	One or more jumper wires as required to connect one or more of the six iSBC 534 interrupts to the nine Multibus interrupt lines (refer to paragraph 2-13). Factory wired as follows: *132-140 Connects INTR1 (PIC 0) and *131-140 INTR2 (PIC 1) to INT1/.
Serial I/O Clocks (Baud Rate)	ZB7	4ZC6,4ZC7	Jumper wires as required to connect Transmit Clock (TXC) and Receive Clock (RXC) to USART chips as follows (refer to paragraph 2-14): PORT 0 — TXC — RXC — SOURCE *80-81 — *80-79 — BDG0 from PIT 0 77-81 — 77-79 — BDG4 from PIT 1 78-81 — 78-79 — BDG5 from PIT 1 76-81 — 76-79 — REC CLK (external via J1) 82-81 — 82-79 — XMIT CLK (external via J1)

Table 2-5. Jumper Selectable Option (Continued)

FUNCTION	FIG. 5-1 GRID REF.	FIG. 5-2 GRID REF.	DESCRIPTION			
	ZB6	5ZC6,5ZC7	PORT 1	TXC	RXC	SOURCE
				*87-88	*87-86	BDG1 from PIT 0
				84-88	84-86	BDG4 from PIT 1
				85-88	85-86	BDG5 from PIT 1
				83-88	83-86	REC CLK (external via J2)
				89-88	89-86	XMIT CLK (external via J2)
	ZB5	6ZC6,6ZC7	PORT 2	TXC	RXC	SOURCE
				*94-95	*94-93	BDG2 from PIT 0
				91-95	91-93	BDG4 from PIT 1
				92-95	92-93	BDG5 from PIT 1
				90-95	90-93	REC CLK (external via J3)
				96-95	96-93	XMIT CLK (external via J3)
	ZB5	7ZC6,7ZC7	PORT 3	TXC	RXC	SOURCE
				*101-102	*101-100	BDG3 from PIT 1
				98-102	98-100	BDG4 from PIT 1
				99-102	99-100	BDG5 from PIT 1
				97-102	97-100	REC CLK (external via J4)
				103-102	103-100	XMIT CLK (external via J4)
Serial I/O Port Interface			One 18-pin DIP header jumper assembly supplied for each serial I/O port. These DIP header jumper assemblies allow serial I/O ports to interface with RS232C or optically isolated current loop devices as follows (refer to paragraph 2-15):			
	ZD7,ZC7	4ZD2,4ZB2	PORT 0	W1	W5	INTERFACE
				*IN	OUT	RS232C
				OUT	IN	Current Loop
	ZD6,ZC6	5ZD2,5ZB2	PORT 1	W2	W6	INTERFACE
				*IN	OUT	RS232C
				OUT	IN	Current Loop
	ZD5,ZC5	6ZD2,6ZB2	PORT 2	W3	W7	INTERFACE
				*IN	OUT	RS232C
				OUT	IN	Current Loop
	ZD4,ZC4	7ZB2,7ZD2	PORT 3	W4	W8	INTERFACE
				*IN	OUT	RS232C
				OUT	IN	Current Loop

Table 2-5. Jumper Selectable Option (Continued)

FUNCTION	FIG. 5-1 GRID REF.	FIG. 5-2 GRID REF.	DESCRIPTION		
Serial I/O Port Current Loop* *			Four jumpers for each serial I/O port that is used for optically isolated current loop devices. Jumpers are configured as follows (refer to paragraph 2-16):		
			PORT 0	JUMPERS IN	JUMPERS OUT
	ZD8,ZC8	4ZA3,4ZB3		*1-2, *4-5, *7-8, *9-10	53-54
			PORT 1	JUMPERS IN	JUMPERS OUT
	ZD7,ZC7	5ZA3,5ZB3		*11-12, *14-15, *17-18, *19-20	55-56
			PORT 2	JUMPERS IN	JUMPERS OUT
	ZD6,ZC6	6ZA3,6ZB3		*21-22, *24-25, *27-28, *29-30	57-58
			PORT 3	JUMPERS IN	JUMPERS OUT
	ZD5,ZC5	7ZA3,7ZB3		*31-32, *34-35, *37-38, *39-40	59-60
Parallel I/O Port Inputs			Four jumper wires allow inputs from the following sources (refer to paragraphs 2-17 and 2-18):		
				JUMPER	SOURCE
	ZC7	3ZC7,3ZD7		*65-64	SRXD0 (external via J1)
				65-66	AUX 1 (external via J5)
	ZC6			*68-67	SRXD1 (external via J2)
				68-69	AUX 2 (external via J5)
	ZC5			*71-70	SRXD2 (external via J3)
				71-72	AUX 3 (external via J5)
	ZC4			*74-75	PW1 (external via J5)
				74-73	SRXD3 (external via J4)
Parallel I/O Port Outputs			Four jumper wires allow outputs to the following destinations (refer to paragraphs 2-17 and 2-19):		
				JUMPER	DESTINATION
	ZC3,ZD3	3ZC1,3ZD1		*48-49	STXD0 (external via W1 and J1)
				48-47	AUX 4
				*51-52	STXD1 (external via W2 and J2)
				51-50	AUX 5
				*45-44	DPR
				45-46	STXD2
				*42-41	CRQ
				42-43	STXD3

*Default jumpers (configured at the factory).
* *Requires optical isolators (refer to paragraph 2-21).

2-9. I/O BASE ADDRESS

The host processor transmits and receives data to and from the iSBC 534 by issuing I/O Write and I/O Read Commands, respectively. The I/O addresses used for these commands are relative to an 8-bit hexadecimal I/O base address (X) that is a multiple of 16. The only consideration to be taken in assigning the I/O base address is to ensure that no two boards in the system share the same block of I/O addresses.

The block of 16 I/O addresses is jumper selectable to begin on any 16-byte I/O address boundary (i.e., 00, 10, 20, . . . F0). In the default configuration, the board will respond to the addresses C0-CF. If some other address block is desired, remove the jumper from 118-125 and install the jumper between the appropriate set of standoffs listed in table 2-5.

2-10. COUNTER CLOCK FREQUENCY

The normal counter clock frequency is 1.2288 MHz. To double this frequency for greater timing flexibility, remove the jumper from 62-63 and install it between 61-62.

2-11. INTERVAL TIMER

Timer sections 1 and 2 (outputs BDG4 and BDG5) of Programmable Interval Timer A36) (PIT 1) can be connected either in parallel or series for increased timing flexibility (such as timing interrupt intervals, etc.). Default jumper is 105-106, which connects both timers in parallel and both receive the same clock signal. When the two timer sections are connected in series, output BDG4 (from counter 1) serves as the clock for counter 2. This permits lower clock rates or longer time intervals. To connect the two timers in series, remove the jumper from 105-106 and install it between 105-104.

2-12. ADVANCED ACKNOWLEDGE

The Advanced Acknowledge (AACK/) signal is normally issued approximately 100 nanoseconds after the receipt of an I/O Read or an I/O Write Command. This 100-nanosecond delay can be further decreased so that AACK/ occurs almost immediately (with appropriate allowance for propagation delay) after the receipt of an I/O Read or I/O Write Command. To implement the early AACK/ feature, install a jumper between standoffs 115-116.

2-13. INTERRUPTS

The iSBC 534 has an interrupt matrix that can be used to connect any of the following six interrupts to the nine Multibus interrupt lines:

a. INTR1 from PIC 0.
b. INTR2 from PIC 1.
c. RXRDY from Port 0.
d. TXRDY from Port 0.
e. RXRDY from Port 1.
f. TXRDY from Port 1.

Each of the two PIC (Programmable Interrupt Controller) chips service eight interrupts as shown in figure 2-2. Note that the TXRDY and RXRDY interrupts from Port 0 and Port 1 can be wired (jumpered) directly to the Multibus interrupt lines. Note also that timer outputs BDG4 and BDG5 from Programmable Interval Timer 1 (PIT 1) are input as interrupts to PIC 1. These two inputs can be used to generate real-time interrupts at prescribed intervals. (Refer to paragraph 2-14.)

The default (factory connected) jumpers connect both INTR1 and INTR2 to the INT1/ line on the Multibus. Remove the default jumpers if interrupt reconfiguration is necessary.

NOTE

When using the iSBC 534 board in an Intellec Micro-computer Development System, remove the jumpers 131-140 and 132-140. This prevents unwanted interrupts on INT1/ which would interfere with the operation of ISIS.

2-14. SERIAL I/O CLOCKS

Each of the two Programmable Interval Timers (PIT 0 and PIT 1) has three independent time/rate (Baud rate) generator sections as follows:

TIMER	COUNTER	OUTPUT
PIT 0	0	BDG0
PIT 0	1	BDG1
PIT 0	2	BDG2
PIT 1	3	BDG3
PIT 1	4	BDG4
PIT 1	5	BDG5

There are four USART chips, one for each serial I/O port. Each USART chip, or serial I/O port, requires two clocks: a Transmit Clock (TXC) and a Receive Clock (RXC). These two clocks may be at the same frequency or at different frequencies.

The default (factory connected) clock for each serial I/O port is listed in table 2-5. Note that BDG0 serves as both the TXC and RXC clock for Port 0, and that BDG1 through BDG3 serve as both the TXC and RXC clocks for Port 1 through Port 3, respectively.

Examination of table 2-5 also shows that each port can accept clock inputs from five separate sources. Notice that each port can accept an externally supplied receive clock (REC CLK) and transmit clock (XMIT CLK). These clocks are input via the edge connector associated with each serial I/O port.

Clock signals BDG0 through BDG5 can be programmed for any integral submultiple of the iSBC 534 clock frequency (1.2288 MHz or 2.4576 MHz). Thus, the frequency range of BDG0 through BDG5 is from 18.75 Hz to 614.4 kHz. BDG4 and BDG5 can be connected in series so that the timer output range is 0.00029 Hz to 1.2288 MHz depending on (1) whether counter sections 1 and 2 are in parallel or series and (2) whether the clock frequency is 1.2288 MHz or 2.4576 MHz. (Refer to paragraphs 2-10 and 2-11.)

2-15. SERIAL I/O PORT INTERFACE

Each of the four serial I/O ports can be configured to accommodate RS232C or optically isolated current-loop-dependent devices. The iSBC 534 is supplied with four 18-pin DIP header jumper assemblies installed in sockets designated W1 through W4 to accommodate RS232C devices. (Refer to table 2-5.) If a particular port is to be interfaced to a current loop device, remove the associated DIP header jumper assembly and install it in its alternate position. Refer also to paragraphs 2-16 and 2-21.

2-16. SERIAL I/O PORT CURRENT LOOP

As described in paragraph 2-15, the serial I/O ports can be configured to accommodate RS232C or optically isolated

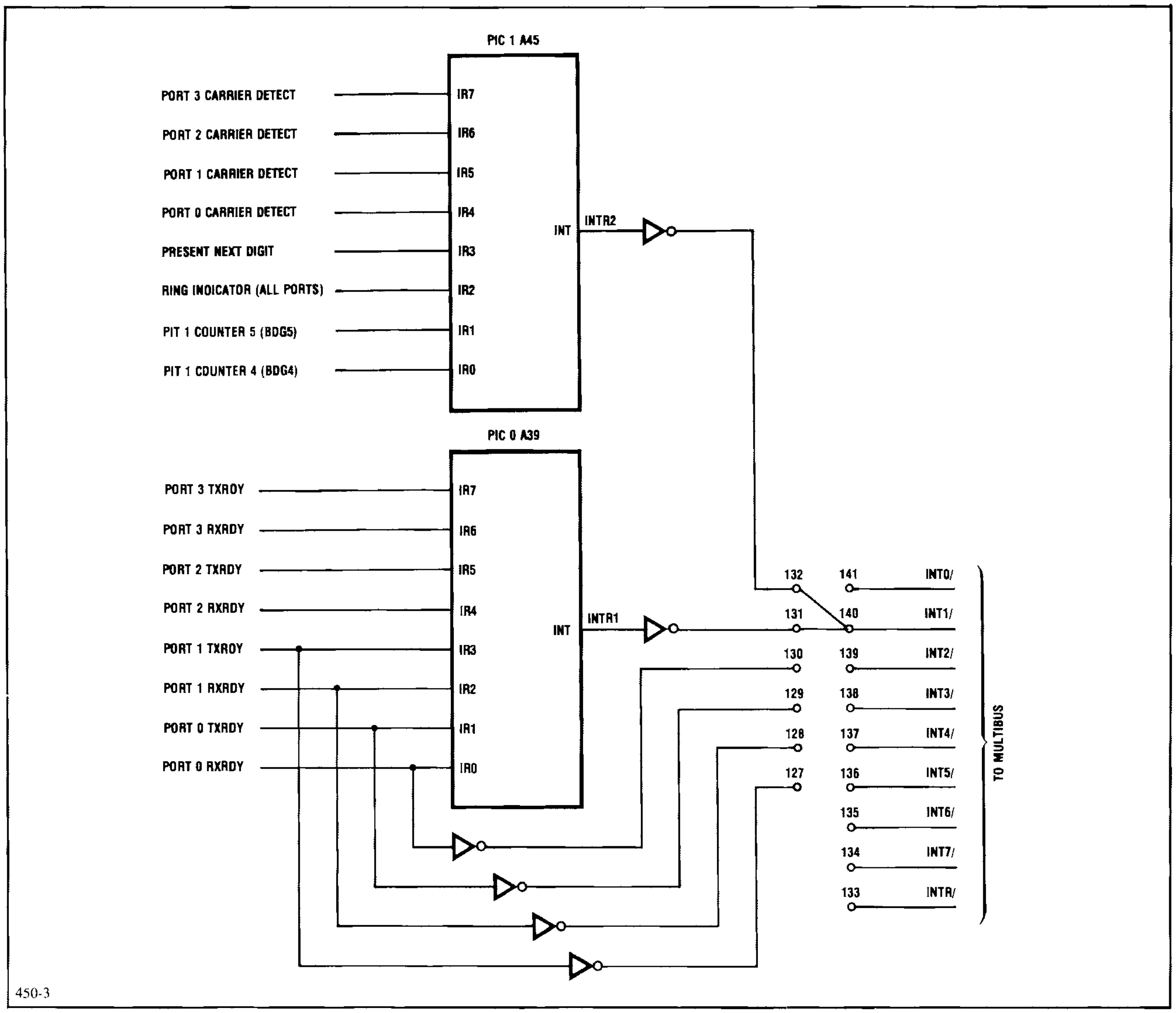


Figure 2-2. iSBC 534 Interrupt Jumpers

current-loop-dependent devices. If all serial I/O ports are to be interfaced to RS232C devices, no further jumper configuration is necessary for this function.

The basic current loop circuit shown in figure 2-3 consists of a receive isolator, a transmit isolator, and a current source. The loop can be connected in one of two basic configurations: a separate (or double) loop as shown in figure 2-4 or a series (or single) loop as shown in figure 2-5.

The basic jumper and external loop wiring for Port 0 are shown in figure 2-6. The voltage source, current source, and loop configuration jumpers are as follows:

a. Voltage Source. For internal ±12V source, leave jumpers 1-2 and 4-5 connected. For external ±12V source, remove and connect jumpers 2-3 and 5-6.

b. Current Source. The current source can use either internal or external voltages. For internal current source, leave jumpers 7-8 and 9-10 connected. For external current source, remove these two jumpers.

c. Loop Configuration. The presence or absence of jumper 53-54 depends on the current loop configuration. Leave jumper open for:

   (1) Separate (double) loop configurations.

   (2) Series (single) loop configurations with *internal* current source.

   Connect jumper 53-54 for series (single) loop configurations with *external* source current.

Jumper connections for the remaining ports (Ports 1, 2, 3) are configured in an identical manner except for the jumper standoff numbers. (Refer to table 2-5.)

2-17. PARALLEL I/O PORT

The parallel I/O port has eight parallel input and eight parallel output lines that are compatible with the Bell Model 801 Automatic Calling Unit (ACU), or equivalent. The inputs and outputs of the parallel I/O port are controlled by an Intel 8255A Programmable Peripheral Interface (PPI) chip (A22).

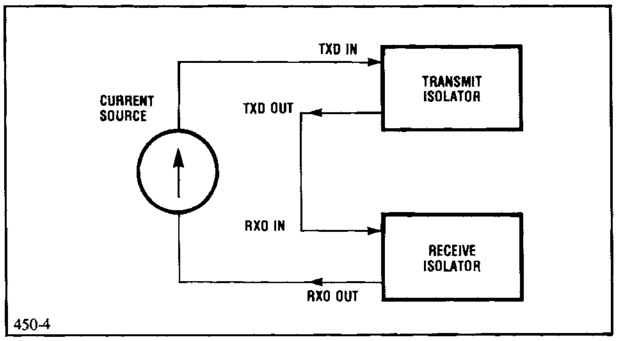


Figure 2-3. Basic Isolator Current Loop Circuit

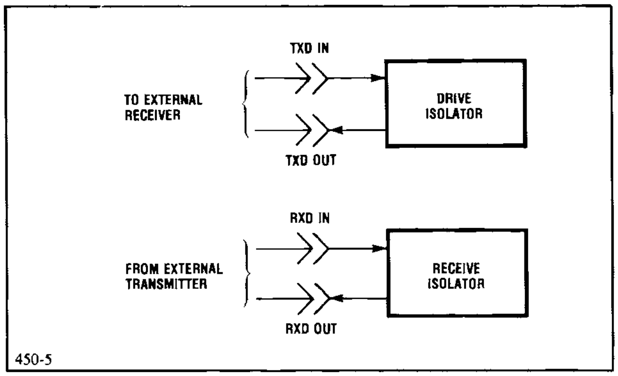


Figure 2-4. Basic Separate (or Double) Loop Circuit for Single Port

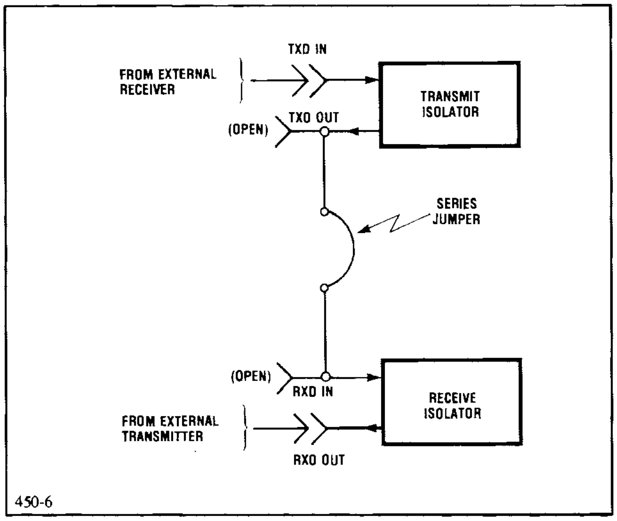


Figure 2-5. Basic Series (or Single) Loop Circuit for Single Port

2-18. INPUT OPTIONS. In addition to the standard ACU input signals (PND, DSS, DLO, and ACR), one input of each of the following pairs can be jumper-connected:

a. SRXD0* or AUX 1
b. SRXD1* or AUX 2
c. SRXD2* or AUX 3
d. SRXD3 or PWI*

*denotes default connection

The four SRXD inputs are from the four serial I/O ports, respectively; the AUX inputs can be used for any auxiliary function. The Power Indicator (PWI) input is from an ACU.

2-19. OUTPUT OPTIONS. In addition to the standard ACU outputs (number bits NB1 through NB8), one output of each of the following pairs can be jumper-connected:

a. STXD0* or AUX 4
b. STXD1* or AUX 5
c. STXD2 or DPR*
d. STXD3 or CRQ*

*denotes default connection

The four STXD outputs go to the four serial I/O ports, respectively; the AUX inputs can be used for any auxiliary function. The Digit Present (DPR) and Call Request (CRQ) outputs are to an ACU.

2-20. COMPONENT INSTALLATION

2-21. OPTICAL ISOLATORS

Optical isolators must be user furnished and installed for each serial I/O port that is to be used for current loop operation. Table 2-6 lists the location, type, and function of each optical isolator. Be sure to install the optical isolators with pin 1 adjacent to the white dot located near pin 1 of the IC socket.

The maximum expected speed when using type 4N33 and 4N37 optical isolators is 1200 Baud.

2-22. RISE-TIME/NOISE CAPACITORS

Each of the serial I/O ports has an optional connection for a rise-time or noise-control capacitor. These are:

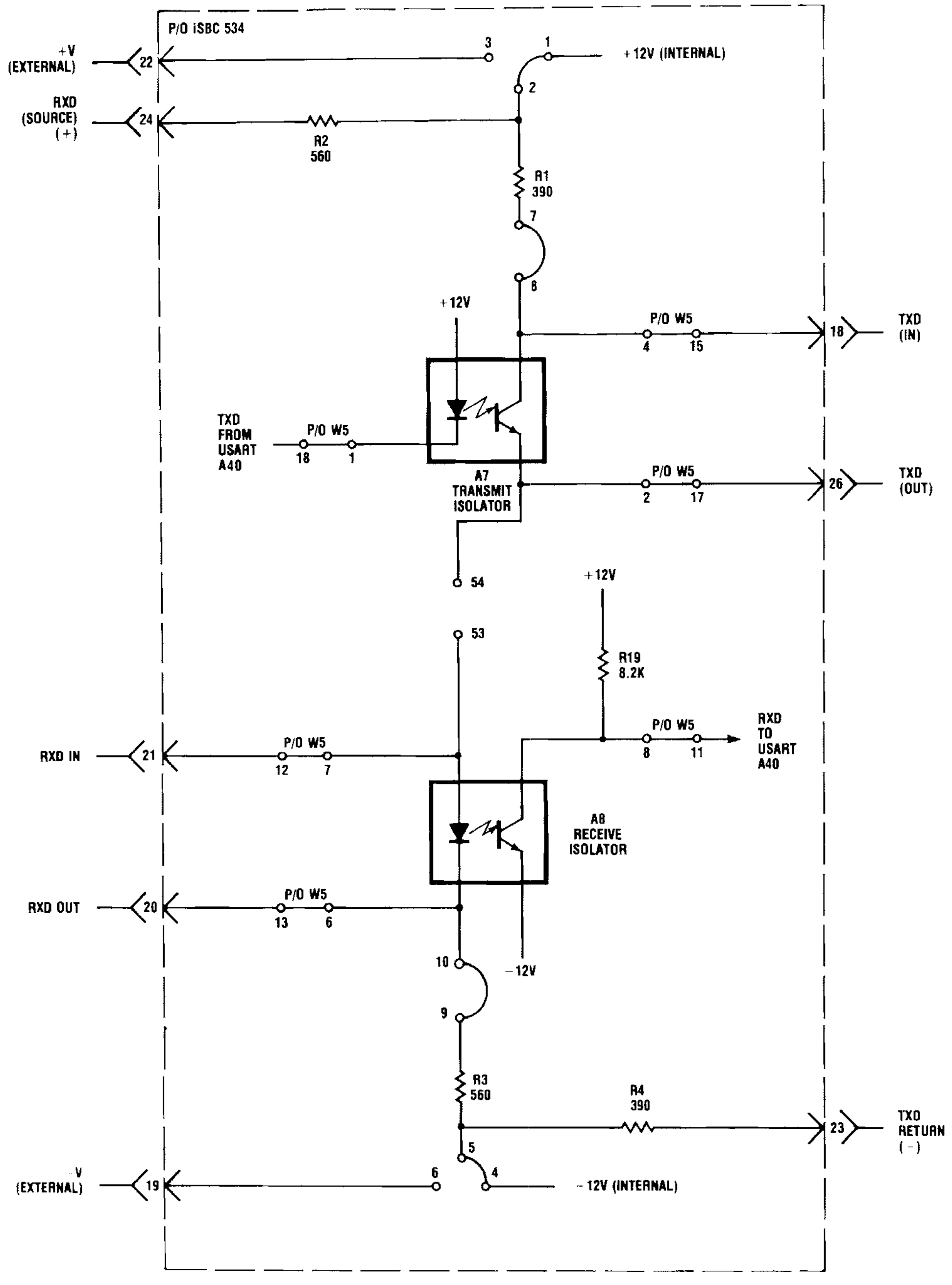
PORT	CAPACITOR	FIG. 5-1 GRID REF.
0	C7	ZC7
1	C8	ZC6
2	C9	ZC5
3	C4	ZC4

The selection of capacitor value is at the option of the user, and is normally a function of the application. At any given port, the capacitor can be left out, or any desired value can be inserted.

2-23. DATA SET CONVERSION

Ports 0 through 3 are configured for *data terminal* operation in conjunction with an external *data set*. For certain applications, it may be necessary to convert one or more ports for *data set* operation in conjunction with an external *data terminal*. To convert to data set operation, proceed as follows:

a. Select port to be converted and remove associated 18-pin DIP header jumper assembly; e.g., for Port 0, remove DIP header jumper assembly from W1 or W5. (Refer to table 2-5.)



450-7

NOTES:
- ALL COMPONENTS & JUMPERS SHOWN ARE FOR PORT 0 ONLY. OTHER PORTS ARE IDENTICAL EXCEPT FOR COMPONENTS & JUMPER STANDOFF NUMBERS.
- ALL JUMPERS SHOWN CONNECTED ARE DEFAULT JUMPERS.
- W5 IS PART OF 18-PIN DIP JUMPER ASSEMBLY.
- P/O = PART OF.

Figure 2-6. Current Loop Jumper Circuits (Port 0)

Table 2-6. Current Loop Optical Isolators

FIG. 5-1 GRID REF.	FIG. 5-2 GRID REF.	PORT	IC SOCKET	TYPE	FUNCTION
ZC7	4ZA4	0	A7	4N33	Transmit (XMIT)
ZC7	4ZB4	0	A8	4N37	Receive (RCV)
ZC6	5ZA4	1	A11	4N33	Transmit (XMIT)
ZC6	5ZB4	1	A12	4N37	Receive (RCV)
ZC5	6ZA4	2	A14	4N33	Transmit (XMIT)
ZC5	6ZB4	2	A15	4N37	Receive (RCV)
ZC4	7ZA4	3	A18	4N33	Transmit (XMIT)
ZC4	7ZB4	3	A19	4N37	Receive (RCV)

b. Wire a DIP header jumper assembly so that the following signals are reversed: (1) TXD and RXD, (2) RTS and CTS, and (3) DSR and DTR. (See figure 2-7.) Other signals may need to be reversed depending on the particular application.

c. Place reconfigured DIP header jumper assembly in the appropriate IC socket: W1 for Port 0, W2 for Port 1, W3 for Port 2, or W4 for Port 3.

2-24. EXTERNAL LOOP CONSIDERATIONS

There are four basic combinations of external loop parameters to be considered for serial I/O port interfacing:

a. Series (single) loop circuit with external current source (figure 2-8).

b. Series (single) loop circuit with internal or external voltage as internal current source (figure 2-9).

c. Separate (double) loop circuit with an external current source (figure 2-10).

d. Separate (double) loop circuit with internal or external voltage as internal current source (figure 2-11).

When using the internal ± 12V supplies, each serial I/O port will supply 20 mA minimum to an external current loop under the following conditions:

a. Single loop with one transmitter and one receiver in the external loop.

b. Double loops with one transmitter or one receiver in the external loop.

External voltage sources are recommended for single loops with more than one external element in each loop, or for double loops with more than two external elements. Each serial I/O port has connector pins for an external voltage source. The external voltage can be adjusted for an appropriate loop current (i.e., 20 mA).

2-25. SERIAL I/O CABLING

The four serial I/O ports can be used with either an RS232C device or a current-loop-dependent device. Connection details for both types of devices are given in following paragraphs. Compatible mating connectors for J1 through J4 are listed in table 1-1 (Specifications).

2-26. RS232C INTERFACE CABLING

Pin assignments and signal definitions for RS232C serial I/O communications are listed in table 2-7. Each of the four serial I/O ports is configured for data terminal operation. As described in paragraph 2-23, each port can alternatively be configured for data set operation by rewiring the DIP header jumper assembly.

The Intel iSBC 955 Cable Set, consisting of two cable assemblies, is recommended for RS232C interfacing. One cable assembly consists of a 25-wire flat cable with a 26-pin PC edge connector at one end and an RS232C interfacing connector at the other end. The second cable assembly includes an RS232C connector at one end and has spade lugs at the other end; the spade lugs are used to interface to a teletypewriter. See Appendix B for ASR-33 TTY interface instructions.

For OEM applications where cables will be made for the iSBC 534, it is important to note that the mating connectors for J1 through J4 have one more pin (26) than an RS232C interface connector (25), which is used with a 25-wire flat cable. Consequently, when wiring the 26-pin mating connector, be sure that the cable makes contact with pins 1 and 2 of the mating connector, and not with pin 26.

Similarly, when installing the iSBC 534 with a 26-pin mating connector (J1 through J4), be sure that the connector is oriented properly on the serial I/O ports. If the connector is installed backward, no damage will occur but the I/O port will be inoperative.

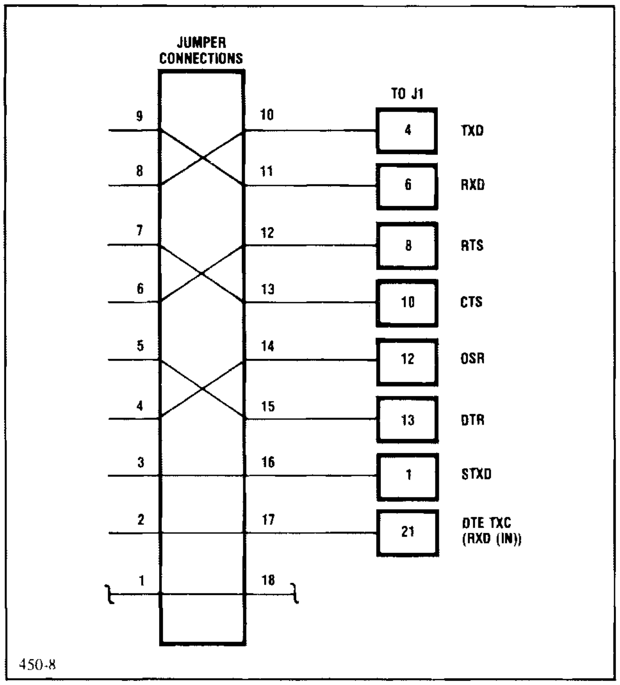


Figure 2-7. DIP Header Jumper Assembly Reconfiguration for Data Set Operation

2-27. CURRENT LOOP INTERFACE CABLING

When using the iSBC 534 serial I/O port(s) with optical isolators in a current loop, the interface cabling is wired differently. Pin assignments and signal definitions for current loop serial I/O communications are listed in table 2-8.

2-28. PARALLEL I/O CABLING

The parallel I/O port can be interfaced with the Intel iSBC 955 Cable Set described in paragraph 2-26. Pin assignments and signal definitions for the parallel I/O port are listed in table 2-9. Compatible mating connectors or J5 are listed in table 1-1 (Specifications).

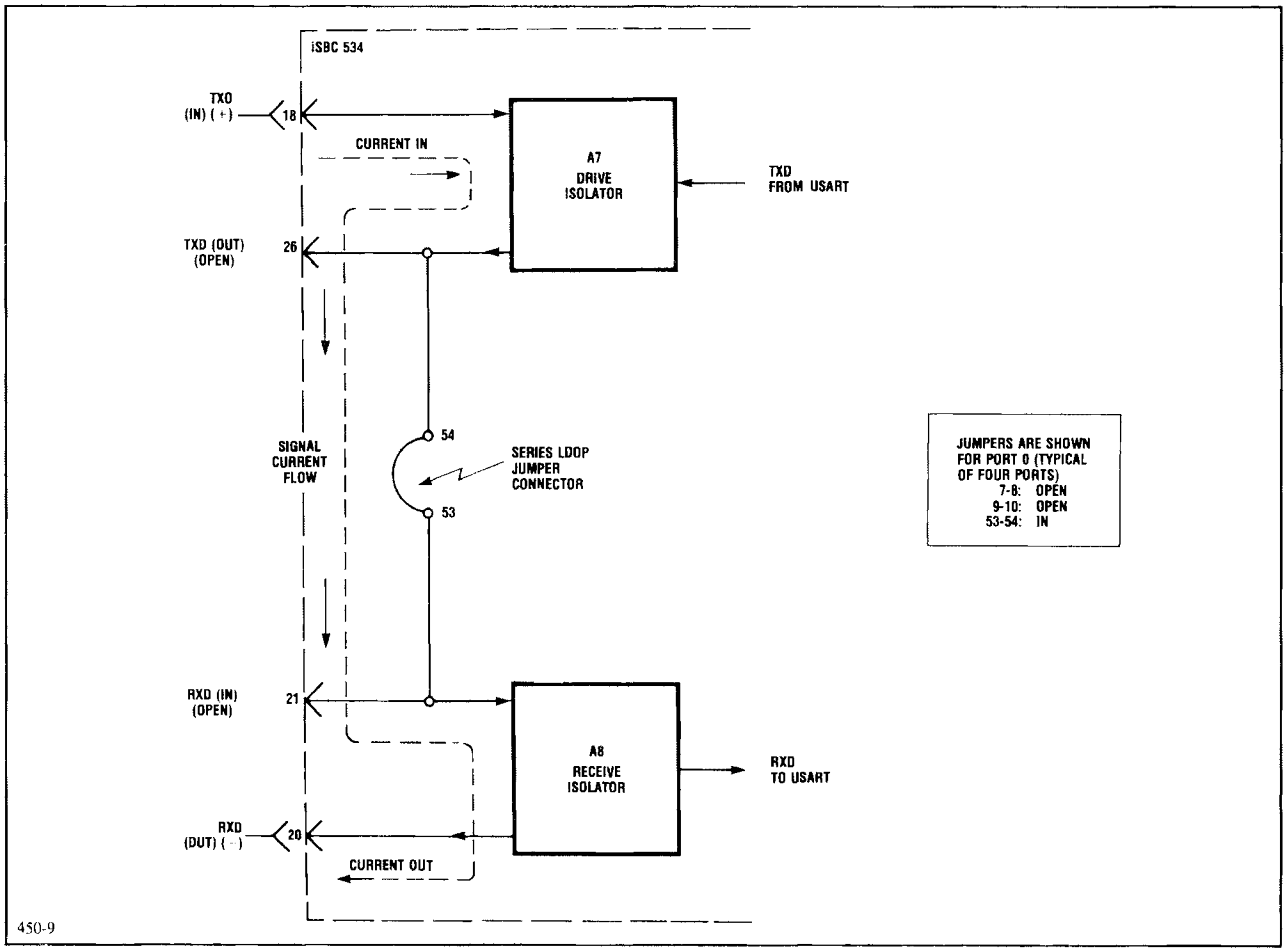


Figure 2-8. Series (Single) Loop Circuit With External Current Source

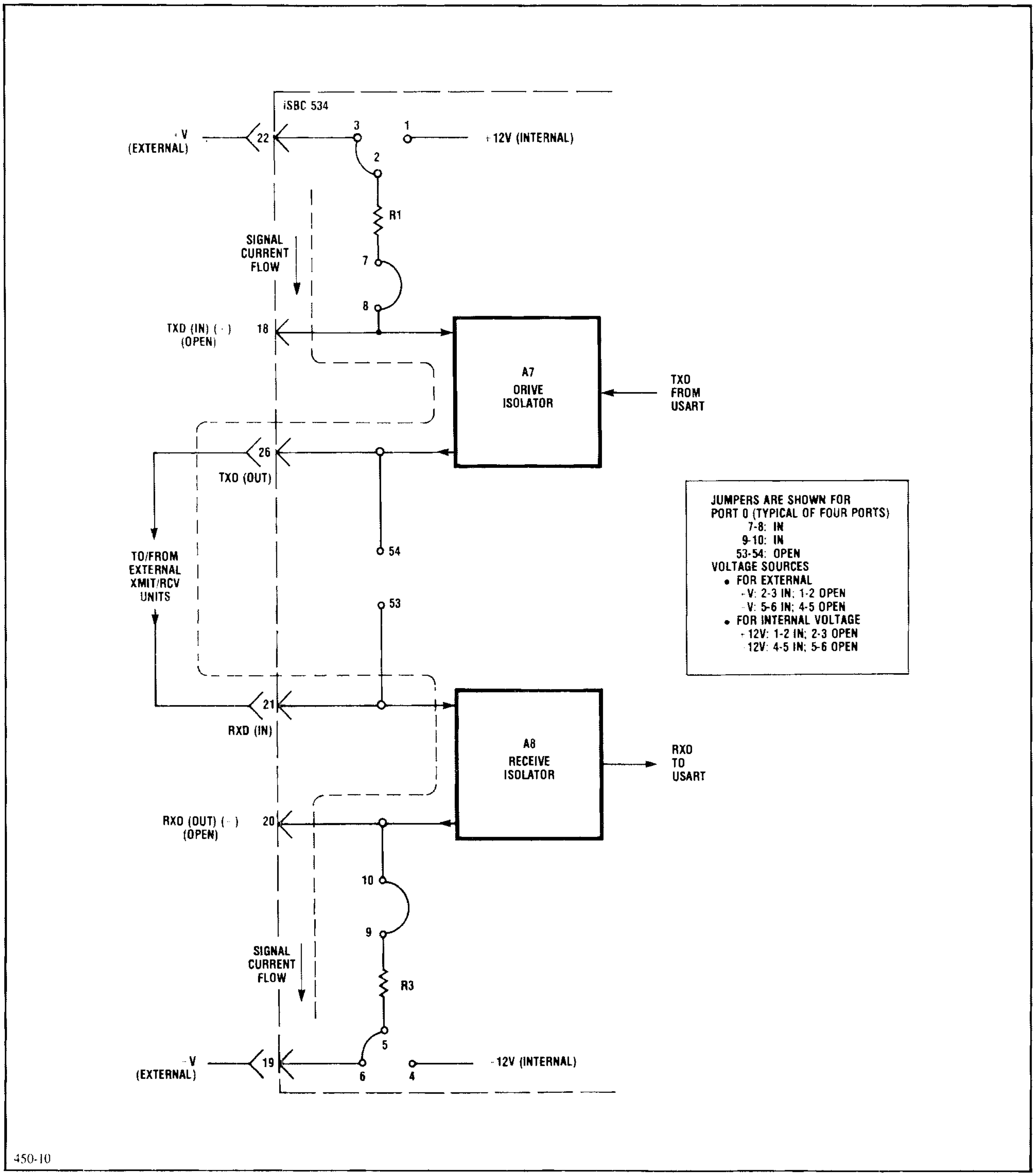


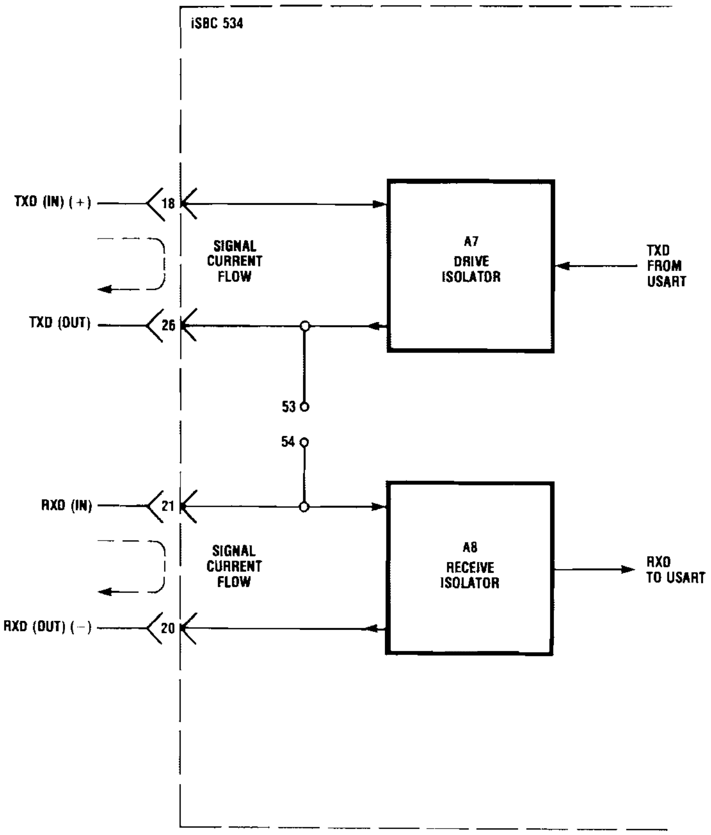
Figure 2-9. Series (Single) Loop Circuit With External Voltage Source

2-29. BOARD INSTALLATION

CAUTION

Always turn off the computer system power supply before installing or removing the iSBC 534 board and before installing or removing device interface cables. Failure to take these precautions can result in damage to the board.

In an iSBC 80 Single Board Computer based system, install the iSBC 534 in any slot that has not been wired for a dedicated function. In an Intellec Microcomputer Development System, install the iSBC 534 in any slot except slot 1 or 2. Attach the appropriate cable assemblies to connectors J1 through J5.

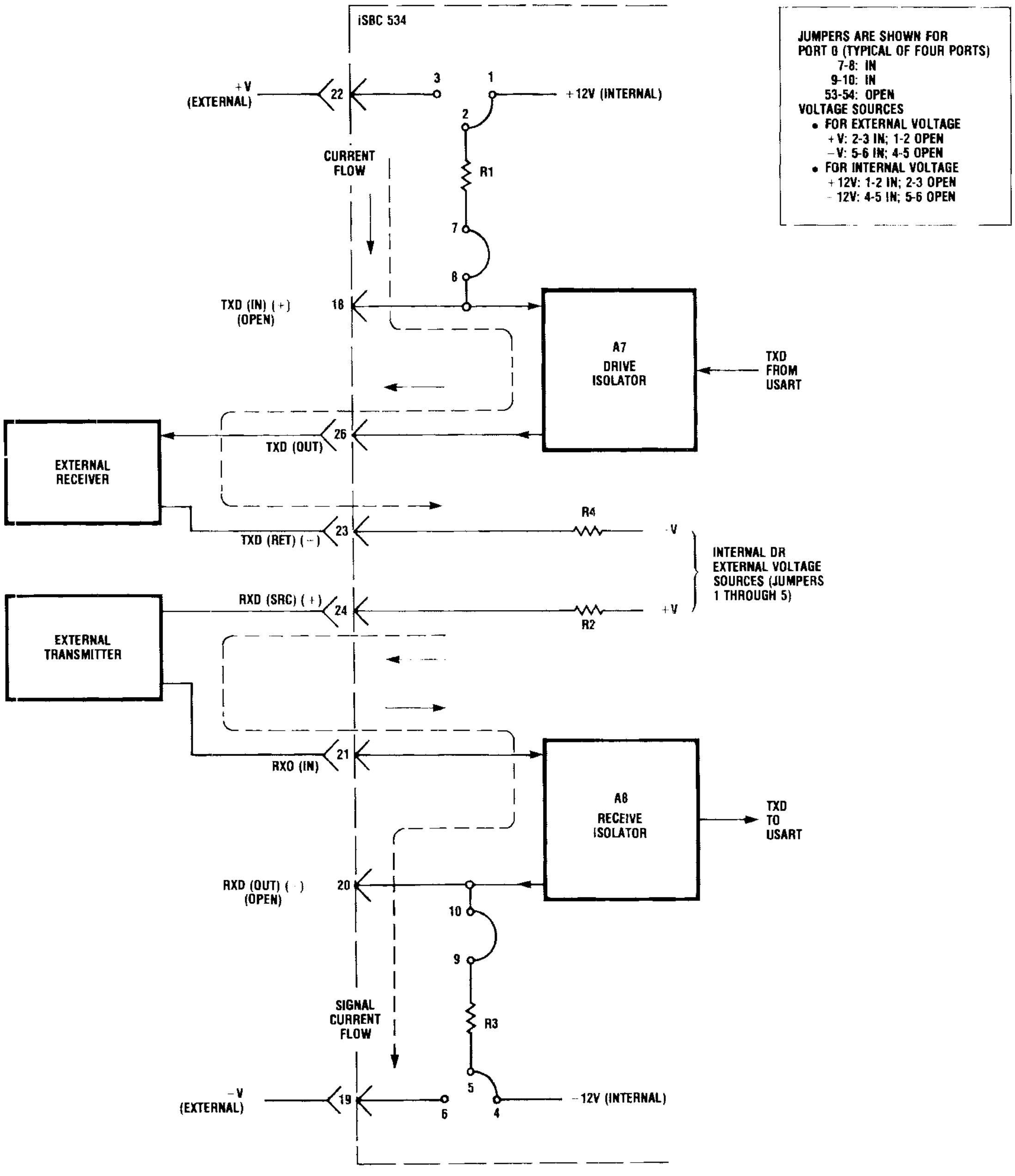


JUMPERS ARE SHOWN FOR PORT 0
(TYPICAL OF FOUR PORTS)

7-8 }
9-10 } OPEN
53-54 }

450-11

Figure 2-10. Separate (Double) Loop Circuit With External Current Sources



JUMPERS ARE SHOWN FOR
PORT 0 (TYPICAL OF FOUR PORTS)
7-8: IN
9-10: IN
53-54: OPEN
VOLTAGE SOURCES
- FOR EXTERNAL VOLTAGE
  +V: 2-3 IN; 1-2 OPEN
  −V: 5-6 IN; 4-5 OPEN
- FOR INTERNAL VOLTAGE
  +12V: 1-2 IN; 2-3 OPEN
  −12V: 4-5 IN; 5-6 OPEN

450-12

Figure 2-11. Separate (Double) Loop Circuit With Internal Current Sources

Table 2-7. Connector J1-J4 RS232C Signal Interface

J1-J4 PIN	RS232C PIN	SIGNAL MNEMONIC	DEFINITION
1	14	STXD	Secondary Transmit Data. Same as TXD except STXD is a secondary signal.
2	1	—	Not used on iSBC 534.
3	15	XMIT CLK	Transmit Clock. External input clock signal for transmit data timing.
4	2	TXD	Transmit Data. Data transmitted from data terminal to data set.
5	16	SRXD	Secondary Receive Data. Same as RXD except SRXD is a secondary signal.
6	3	RXD	Receive Data. Data received by data terminal from data set.
7	17	REC CLK	Receive Clock. External input clock signal for receive data timing.
8	4	RTS	Request To Send. Control signal from data terminal to data set; sets data set in transmit mode.
9	18	—	Not used on iSBC 534.
10	5	CTS	Clear To Send. Control signal from data set to data terminal to indicate that data set is ready to transmit data; enables TXD output mode.
11	19	—	Not used on iSBC 534.
12	6	DSR	Data Set Ready. Indicates to data terminal that data set is connected to a communications channel; i.e., data set is not in Test, Talk, or Dial mode and timing and/or answer signals have been completed.
13	20	DTR	Data Terminal Ready. Indicates to data set that data terminal is ready to transmit or receive data.
14	7	SGD	Signal Ground.
15	21	—	Not used on iSBC 534.
16	8	CD	Carrier Detect. Signal from data set; indicates that data set is receiving a suitable signal.
17	22	RI	Ring Indicator. Signal from data set; indicates that ringing signal has been received from a communications channel.
18	9	—	Not used for RS232C; for current loop only.
19	23	—	Not used for RS232C; for current loop only.
20	10	—	Not used for RS232C; for current loop only.
21	24	DTE TXC	Data Terminal Equipment Transmit Clock. Output from serial I/O port to data set to provide clock signal to transmitting signal converter.
22	11	—	Not used for RS232C; for current loop only.
23	25	—	Not used for RS232C; for current loop only.
24	12	—	Not used for RS232C; for current loop only.
25	N/C	SGD	Signal Ground.
26	13	—	Not used for RS232C; for current loop only.

NOTES:
1. J1-J4 pins 2, 9, 11, and 15 are not used on iSBC 534.
2. J1-J4 pins 18, 19, 20, 22, 23, 24, and 26 used only in current loop applications.

Table 2-8. Connector J1-J4 Current Loop Signal Interface

J1-J4 PIN	SIGNAL MNEMONIC	DEFINITION
18	TXD (IN) (+)	Transmit Data Input (+). Transmit optical isolator current loop input.
19	−V	External negative voltage input; requires jumper connection. Refer to paragraph 2-16.
20	RXD (OUT) (−)	Receive Data Output (−). Receive optical isolator current loop output.
21	RXD (IN)	Receive Data Input. Receive optical isolator current loop input.
22	+V	External positive voltage input; requires jumper connection. Refer to paragraph 2-16.
23	TXD (RET) (−)	Transmit Data Return (−). Transmit optical isolator current loop return; used in separate current loops as iSBC 534 internal current return.
24	RXD (SRC) (+)	Receive Data Source Current. Receive optical isolator current loop source; used in separate current loops as iSBC 534 internal current source.
26	TXD (OUT)	Transmit Data Output. Transmit optical isolator current loop output.

Table 2-9. Connector J5 Parallel Output Signal Interface

J5 PIN	RS232C PIN	SIGNAL MNEMONIC	DESCRIPTION
1	14	NB1	Number Bit Lines. Binary coded decimal (BCD) bits that indicate digits of number being called.
3	15	NB2	
5	16	NB4	
7	17	NB8	
4	2	DPR	Digit Present. Generated by data terminal; signal true indicates outputs NB1-NB8 have been set by data terminal and can be read by ACU.
6	3	ACR	Abandon Call; Retry. Generated by ACU to indicate that a preset time has elapsed since last change of state of PND signal. Signal true suggests that if call has not been completed, it should probably be abandoned and retried later.
8	4	CRQ	Call Request. Generated by data terminal; signal true indicates a request for ACU to originate a call.
10	5	PND	Present Next Digit. Generated by ACU during dialing; signal true indicates ACU is ready to accept next digit output on NB lines. Signal false indicates data terminal must reset DPR output. PND will not be set true as long as DPR remains true. PND will be set true after data terminal resets DPR false after last digit on NB lines. PND will be true for duration of any call placed by ACU. PND will be false throughout all calls placed manually and throughout all incoming calls.
12	6	PWI	Power Indication. Generated by ACU; signal true indicates power is available in ACU. If PWI is false and impedance to Signal Ground (SGD) is greater than 300 ohms, automatic calling equipment is inoperative due to loss of power.
14	7	SGD	Signal Ground.

Table 2-9. Connector J5 Parallel Output Signal Interface (Continued)

J5 PIN	RS232C PIN	SIGNAL MNEMONIC	DESCRIPTION
23	25	AUX 1	Auxiliary inputs; require jumper connection. (Refer to paragraph 2-18.)
21	24	AUX 2	
16	8	AUX 3	
22	11	AUX 4	Auxiliary outputs; require jumper connection. (Refer to paragraph 2-19.)
24	12	AUX 5	
17	22	DLO	Data Line Occupied. Generated by ACU; signal true indicates to data terminal that data channel is in use.
26	13	DSS	Data Set Status. Generated by ACU; signal true indicates telephone line is connected to data set and can be used for data communication; also indicates data set is in data mode.

Note:
ACU is Automatic Calling Unit.

CHAPTER 3
PROGRAMMING INFORMATION

3-1. INTRODUCTION

The iSBC 534 Four Channel Communications Expansion Board includes nine programmable chips as follows:

a. Four Intel 8251 USART (Universal Synchronous/Asynchronous Receiver/Transmitter) chips that control the four serial I/O ports.

b. One Intel 8255 PPI (Programmable Peripheral Interface) chip that controls the parallel I/O port.

c. Two Intel 8253 PIT (Programmable Interval Timer) chips that control frequency and timing functions.

d. Two Intel 8259 PIC (Programmable Interrupt Controller) chips that control the interrupt functions.

3-2. I/O BASE ADDRESS

The system computer communicates with the iSBC 534 through a sequence of I/O Read and I/O Write Commands. The I/O addresses used for these commands are relative to an 8-bit I/O base address (X) that must lie on a 16-bit boundary. The I/O base address is configured at the factory to C0; however, the I/O base address may be reconfigured as described in paragraph 2-11.

3-3. I/O ADDRESS ASSIGNMENTS

To conserve I/O address space, the iSBC 534 uses 12 dual-function addresses. As a result, only 16 I/O addresses are required for 28 separate functions. The I/O addresses are divided into two functional subsets, or blocks, of 12 addresses each. The two address blocks are:

a. The data block, which consists of the addresses for the USART and PIC chips.

b. The control block, which consists of the addresses for the PIT and PPI chips.

Since 12 addresses are shared by 24 functions, address ambiguities are eliminated by selecting one of the two address blocks *prior* to addressing a function within the block. In other words, it takes two operations to access a given function:

a. The first operation accesses either the data block or the control block.

b. The second operation accesses a function within the selected block.

Note that block-select addresses are required only when changing from one address block to the other. Once a block has been accessed, any or all functions within the block may be accessed without writing another block-select address.

All address functions are listed in table 3-1. The first 12 addresses (X+0 through X+B) in the block of 16 are used for dual functions. The two block-select addresses X+C and X+D select the control block and data block, respectively. Typical block-select subroutines are presented in tables 3-2 and 3-3. It should be noted that the data word associated with a Write to X+C and X+D is ignored.

3-4. BOARD INITIALIZATION

After the iSBC 534 has been installed, use the following steps to initialize the board:

a. Disable system interrupts. For systems based on Intel 8080/8085 microprocessor, use DI (Disable Interrupts) instruction.

> NOTE
>
> When power is initially applied to the system, or whenever the front panel "reset" switch is pressed, the system Initialize signal (INIT/) is automatically issued and the following step (step b) is not required. If the iSBC 534 is being reinitialized under program control, the reset operation in step b must be performed.

b. Reset iSBC 534 by performing a write to X+F (data is ignored).

c. If iSBC 534 is used with automatic calling unit (ACU), set iSBC 534 to test mode by writing 01 to X+E (this prevents initiation of outgoing calls).

d. Select control block by writing to X+C.

e. Initialize PPI chip (paragraph 3-18).

f. Determine Baud rate for the four serial I/O ports (paragraph 3-30).

g. Initialize PIT chips (paragraph 3-27).

> NOTE
>
> The first four counters (BDG0 through BDG3) are default jumper-wired to USART 0 through 3; unless otherwise jumper-wired, these counters must be programmed for Mode 3 using the 1.2288-MHz clock.

h. Initialize USART chips 0 through 3 for serial I/O ports 0 through 3, respectively (paragraph 3-11).

i. Initialize PIC chips (paragraph 3-45). Set up mode and interrupt mask bits as appropriate.

j. Perform appropriate user-designed system diagnostic routines using iSBC 534 test mode.

Table 3-1. I/O Address Assignments

HEX. I/O ADDR	DATA BLOCK		CONTROL BLOCK	
	CHIP SELECT	FUNCTION SELECT	CHIP SELECT	FUNCTION SELECT
X+0	8251 USART 0 PORT 0	Write: I/O Data Read: I/O Data	8253 PIT 0	Counter 0: BDG0 Load/Read Count (÷N)
X+1		Write: Mode or Command Read: Status		Counter 1: BDG1 Load/Read Count (÷N)
X+2	8251 USART 1 PORT 1	Write: I/O Data Read: I/O Data		Counter 2: BDG 2 Load/Read Count (÷N)
X+3		Write: Mode or Command Read: Status		Write: Control Read: None
X+4	8251 USART 2 PORT 2	Write: I/O Data Read: I/O Data	8253 PIT 1	Counter 3: BDG3 Load/Read Count (÷N)
X+5		Write: Mode or Command Read: Status		Counter 4: BDG4 Load/Read Count (÷N)
X+6	8251 USART 3 PORT 3	Write: I/O Data Read: I/O Data		Counter 5: BDG5 Load/Read Count (÷N)
X+7		Write: Mode or Command Read: Status		Write: Control Read: None
X+8	8259 PIC 0	Write: ICW1, OCW2, and OCW3 Read: Status and Poll	8255 PPI (PARALLEL I/O)	Write: None Read: Port A Data In
X+9		Write: ICW2 and OCW1 (Mask) Read: OCW1		Write: None Read: Port B Data In
X+A	8259 PIC 1	Write: ICW1, OCW2, and OCW3 Read: Status and Poll		Write: Port C Data Out Read: Port C Data Status
X+B		Write: ICW2 and OCW1 (Mask) Read: OCW1		Write: Control Read: None
X+C	Write: Select Control Block Read: None			
X+D	Write: Select Data Block Read: None			
X+E	Write: Select Test Mode (01); deselect Test Mode (00) Read: Determine if iSBC 534 is in Test Mode			
X+F	Write: Board Reset Read: None			

Table 3-2. Typical Control Block Select Subroutine

```
;SETC ACCESSES CONTROL BLOCK
;USES-NOTHING; DESTROYS-NOTHING

         PUBLIC  SETC
         EXTRN   BASAD

SETC:    OUT     BASAD+C
         RET

         END
```

Table 3-3. Typical Data Block Select Subroutine

```
;SETD ACCESSES DATA BLOCK
;USES-NOTHING; DESTROYS-NOTHING

         PUBLIC  SETD
         EXTRN   BASAD

SETD:    OUT     BASAD+D
         RET

         END
```

k. Enable system interrupts. For systems based on Intel 8080/8085 microprocessor, use EI (Enable Interrupts) instruction.

l. Clear iSBC 534 test mode by writing 00 to X+E. The iSBC 534 is now ready for operation.

If appropriate subroutines have been written (such as the samples in this chapter), the initialization procedure consists simply of calling subroutines. The following listing is typical:

```
CALL  RST534   (RESET 534)
CALL  INTURT   (INITIALIZE USART'S)
CALL  INTTMR   (INITIALIZE PIT'S)
CALL  INTAUX   (INITIALIZE PPI)
CALL  INBRG    (LOADS COUNT VALUES IN TIMERS)
CALL  INT59    (INITIALIZE PIC'S
```

Due to the wide variety of USART programs, no sample is given for INTURT. Refer to paragraph 3-11 which provides a sample subroutine for writing either mode or command words for USART initialization. Similarly, no sample is included for INBRG, which consists of a repeated sequence of initializing microprocessor registers D and E with the desired timer count values, and then calling subroutines for loading counter 0, counter 1, etc.

3-5. 8251 USART PROGRAMMING

Each of the four serial I/O ports is controlled by an Intel 8251 USART chip. The USART converts parallel output data into virtually any serial output data format (including IBM Bi-Sync) for half- or full-duplex operation. The USART also converts serial input data into parallel data format.

Prior to starting transmitting or receiving data, the USART must be loaded with a set of control words. These control words, which define the complete functional operation of the USART, must immediately follow a reset (internal or external) operation. The control words are either a Mode instruction or a Command instruction.

3-6. MODE INSTRUCTION FORMAT

The Mode instruction word defines the general characteristics of the USART and must follow a reset operation (internal or external). Once the Mode instruction word has been written into the USART, sync characters or command instructions may be inserted. The Mode instruction word defines the following:

a. For Sync Mode:
   (1) Character length
   (2) Parity enable
   (3) Even/odd parity generation and check
   (4) External sync detect (not supported by iSBC 534)
   (5) Single or double character sync

b. For Async Mode:
   (1) Baud rate factor (X1, X16, or X64)
   (2) Character length
   (3) Parity enable
   (4) Even/odd parity generation and check
   (5) Number of stop bits

Instruction word and data transmission formats for synchronous and asynchronous modes are shown in figures 3-1 through 3-4.

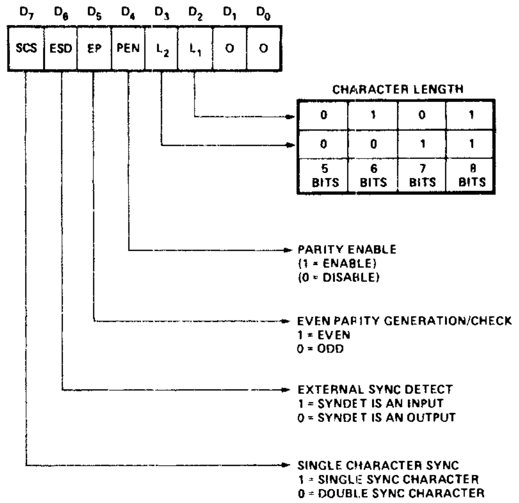

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
SCS ESD EP PEN L_2 L_1 0 0
CHARACTER LENGTH
0 1 0 1
0 0 1 1
5 BITS 6 BITS 7 BITS 8 BITS
PARITY ENABLE
(1 = ENABLE)
(0 = DISABLE)
EVEN PARITY GENERATION/CHECK
1 = EVEN
0 = ODD
EXTERNAL SYNC DETECT
1 = SYNDET IS AN INPUT
0 = SYNDET IS AN OUTPUT
SINGLE CHARACTER SYNC
1 = SINGLE SYNC CHARACTER
0 = DOUBLE SYNC CHARACTER

Figure 3-1. Synchronous Mode Instruction Word Format

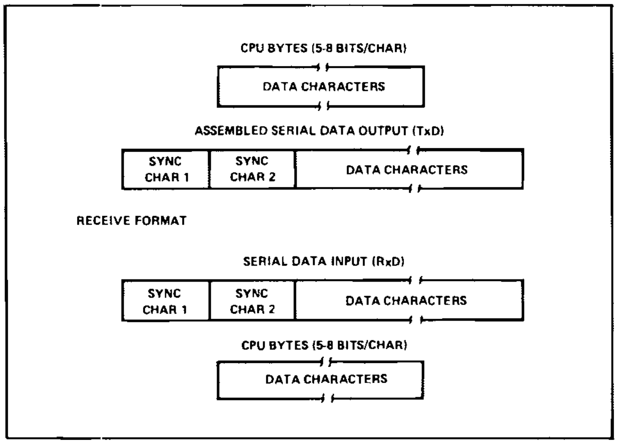


Figure 3-2. Synchronous Mode Transmission Format

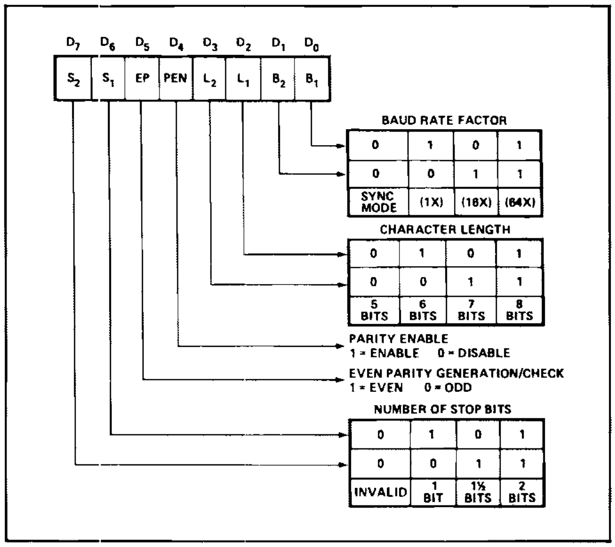


Figure 3-3. Asynchronous Mode Instruction Word Format

3-7. SYNC CHARACTERS

Sync characters are written to each USART in the synchronous mode only. The USART can be programmed for either one or two sync characters; the format of the sync characters is at the option of the programmer.

3-8. COMMAND INSTRUCTION FORMAT

The Command instruction word shown in figure 3-5 controls the operation of the addressed USART. A Command instruction must follow the mode and/or sync words. Once the Command instruction is written, data can be transmitted or received by the USART.

It is not necessary for a Command instruction to precede all data transactions; only those transmissions that require a change in the Command instruction. An example is a change in the enable transmit or enable receive bits. Command instructions can be written to the USART at any time after one or more data operations.

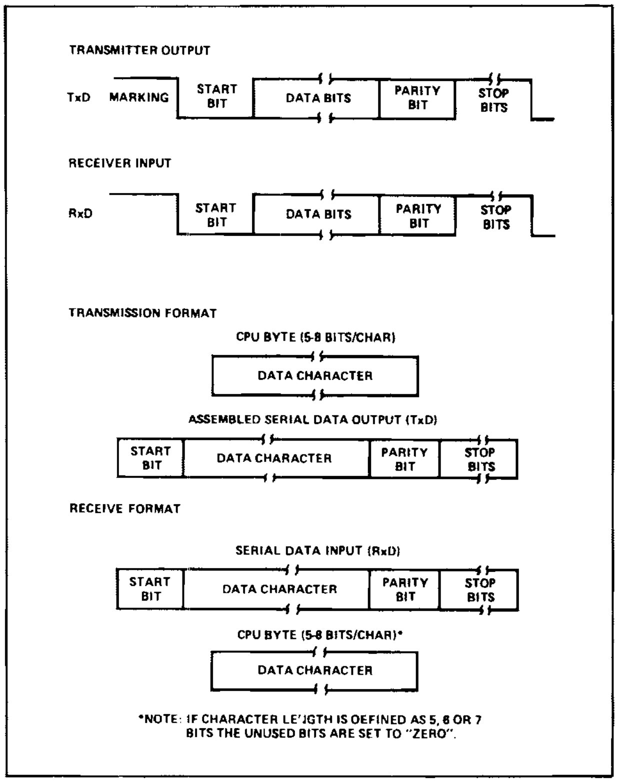


Figure 3-4. Asynchronous Mode Transmission Format

After initialization, always read the chip status and check for the TXRDY bit prior to writing either data or command words to the USART. This ensures that any prior input is not overwritten and lost. Note that issuing a Command instruction with bit 6 (IR) set will return the USART to the Mode instruction format.

With one exception, the Command instruction for optically isolated current loop operation and RS232C operation is identical. The exception is that for current loop operation the RTS bit must always be set (RTS= 1). The reason for this is that the RTS output has a loopback connection to the CTS input; thus, a CTS signal will not be received unless RTS is true.

3-9. RESET

To change the Mode instruction word, the USART must receive a Reset command. The next word written to the USART after a Reset command is assumed to be a Mode instruction. Similarly, for sync mode, the next word after a Mode instruction is assumed to be one or more sync characters. All control words written into the USART after the Mode instruction (and/or the sync character) are assumed to be Command instructions.

Note that an individual USART can be reset by bit 6 (IR) in the Command word; all four USART can be reset by a board reset or by a system reset operation.

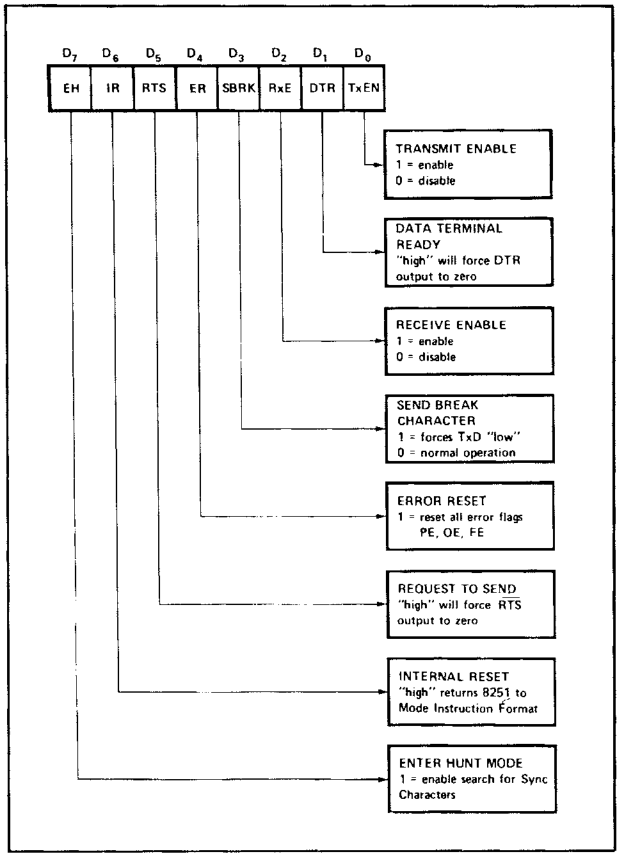


Figure 3-5. USART Command Instruction Word Format

3-10. ADDRESSING

Each of the four USART chips uses two consecutive addresses. The lower of the two addresses is used to read and write I/O data; the upper address is used to write mode and command words and to read the USART status. (Refer to table 3-1.)

3-11. INITIALIZATION

A typical USART initialization and I/O data sequence is presented in figure 3-6. Each USART chip is initialized in four steps:

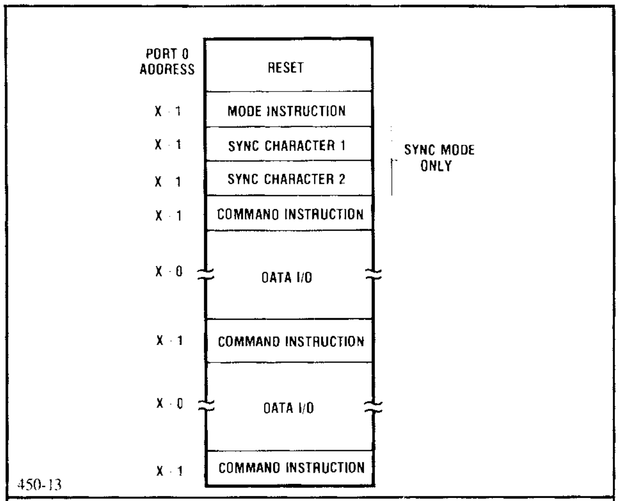
a. Reset USART to Mode instruction format.

b. Write Mode instruction word. One function of mode word is to specify synchronous or asynchronous operation.

c. If synchronous mode is selected, write one or two sync characters as required.

d. Write Command instruction word.

To avoid spurious interrupts during USART initialization, disable the corresponding USART interrupts. This can be done by either masking the appropriate interrupt request inputs at PIC 0 or by disabling the main processor interrupts.



*The second sync character is skipped if Mode instruction has programmed USART to single character internal sync mode. Both sync characters are skipped if Mode instruction has programmed USART to async mode.

Figure 3-6. Typical USART Initialization and Data I/O Sequence

First, reset the USART chips individually or reset all USART chips simultaneously as follows:

a. Individual USART Reset
   (1) Select iSBC 534 data block by performing a write to X+D.
   (2) Write Command instruction to desired USART. Command instruction word must have bit 6 set (IR= 1); all other bits are immaterial.
   (3) Repeat step (2) for remaining USART chips to be initialized.

NOTE

> The above procedure should be used only if the USART to be reset has been completely initialized, or the initialization procedure has reached the point that the USART is ready to receive a command word. If the initialization procedure has been started, it must be completed prior to an individual USART reset. For example, if the reset command is written when the initialization sequence calls for a sync character, then subsequent programming will be in error.
>
> If the initialization procedure is interrupted, ensure correct USART reset and programming by writing a series of four command words, with the contents of each word = 00. Then repeat the USART reset and initialization procedure.

b. Board Reset. Reset iSBC 534 by performing a write to X+F. In addition to resetting all four USART chips, this operation sets the board address logic to data block operation and resets the PPI.

Next, write a Mode instruction word to the desired USART. (See figures 3-1 through 3-4.) A typical subroutine for writing both Mode and Command instructions to USART 2 (Port 2) is given in table 3-4.

If the USART is programmed for the synchronous mode, write one or two sync characters depending on the transmission format.

Finally, write a Command instruction word to the desired USART. Refer to figure 3-5 and table 3-4.

3-12. OPERATION

Normal operating procedures use data I/O read and write, status read, and Command instruction write operations. Programming and addressing procedures for the above are summarized in following paragraphs.

> NOTE
>
> After the USART has been initialized, always check the status of the TXRDY bit *prior* to writing data or writing a new command word to the USART. The TXRDY bit *must* be *true* to prevent overwriting and subsequent loss of command or data words. The TXRDY bit is inactive until initialization has been completed; do not check TXRDY until after the command word, which concludes the initialization procedure, has been written.

Prior to any I/O read or write, status read, or Command instruction write operation, the iSBC 534 must be set for data block operation. If necessary, set to data block by performing a write operation to X+D.

Prior to any operating change, a new command word must be written with command bits changed as appropriate. (Refer to figure 3-5 and table 3-4).

3-13. DATA INPUT/OUTPUT. For data receive or transmit operations perform a read or write, respectively, to the desired USART. Tables 3-5 and 3-6 show examples of typical character read and write subroutines for USART 1.

During normal transmit operation, each USART generates a Transmit Ready (TXRDY) signal that indicates that the USART is ready to accept a data character for transmission. TXRDY is automatically reset when a character is loaded into the USART from the main processor.

Similarly, during normal receive operation, each USART generates a Receive Ready (RXRDY) signal that indicates that a character has been received and is ready for input to the main processor. RXRDY is automatically reset when a character is read by the processor.

The TXDRY and RXRDY outputs of each USART chip are connected to a Programmable Interrupt Controller chip (PIC 0), which resolves priority in case of simultaneous inputs and generates an interrupt for the main processor. (Refer to figure 2-2.) Note that TXRDY and RXRDY from the USART chips at Port 0 and Port 1 can be jumpered directly to the Multibus. TXRDY and RXRDY are also available in the status word. (Refer to paragraph 3-14.)

3-14. STATUS READ. The system processor can determine the status of a serial I/O port by issuing an I/O Read Command to the upper address of the appropriate USART chip. The format of the status word is shown in figure 3-7. A typical status read subroutine for Port 0 is given in table 3-7.

3-15. 8255 PPI PROGRAMMING

The parallel I/O port, which is controlled by an Intel 8255 Programmable Peripheral Interface (PPI) chip, is designed to interface directly with a Bell Model 801 Automatic Calling Unit (ACU).

Table 3-4. Typical USART Mode or Command Instruction Subroutine

```
;CMD2 OUTPUTS CONTROL WORD TO USART 2 (PORT 2)
;USES-A,STAT2; DESTROYS-NOTHING

        PUBLIC  CMD2
        EXTRN   BASAD,STAT2

CMD2:   PUSH    PSW
LP:     CALL    STAT2
        ANI     1               ;CHECK TXRDY
        JZ      LP              ;TXRDY MUST BE TRUE
        POP     PSW
        OUT     BASAD+5         ;ENTER HERE FOR INITIALIZATION
        RET

        END
```

Table 3-5. Typical USART Data Character Read Subroutine

```
;RX1 READS DATA CHARACTER FROM USART 1 (PORT 1)
;USES-STAT1; DESTROYS-A,FLAGS

        PUBLIC  RX1,RXA1
        EXTRN   STAT1,BASAD

RX1:    CALL    STAT1
        ANI     2               ;CHECK FOR RXRDY
        JZ      RX1
RXA1:   IN      BASAD+2         ;ENTER HERE IF RXRDY IS TRUE
        RET

        END
```

Table 3-6. Typical USART Data Character Write Subroutine

```
;TX1 WRITES DATA CHARACTER FROM REG A TO USART 1 (PORT 1)
;USES-STAT1; DESTROYS-A,FLAGS

        PUBLIC  TX1,TXA1
        EXTRN   STAT1,BASAD

TX1:    PUSH    PSW             ;SAVE DATA
TX11:   CALL    STAT1
        ANI     1               ;CHECK FOR TXRDY
        JZ      TX11
        POP     PSW
TXA1:   OUT     BASAD+2         ;ENTER HERE IF TXRDY IS TRUE
        RET

        END
```

The PPI chip has three 8-bit ports designated Ports A, B, and C. Ports A and B are input ports and Port C is an output port. Signals interfaced to the PPI chip are listed in table 3-8. These signals are described either in table 2-9 or table 2-7.

3-16. CONTROL WORD FORMAT

The control word format shown in figure 3-8 is used to initialize the PPI chip to define the operating mode of the three ports. Although the PPI has three operating modes, the iSBC 534 uses only Mode 0, which is defined as "basic input or output" (as opposed to strobed or bidirectional). In Mode 0, data is simply written to or read from the specified port.

3-17. ADDRESSING

The PPI uses four consecutive I/O addresses (X+8 through X+B) for data transfer, obtaining Port C status, and for chip control. (Refer to table 3-1.)

3-18. INITIALIZATION

To initialize the PPI chip, perform the following (a sample initialization subroutine is given in table 3-9):

a. Perform a write to X+C (selects control block).

b. If iSBC 534 is interfaced to ACU, enter test mode by writing 01 to X+E. (This masks Port C bits 6 and 7 to prevent outgoing call request during initialization).

c. Write 92 (hexadecimal) to X+B. Notice in figure 3-8 that this initializes PPI as follows:
   (1) Mode Set Flag Active
   (2) Mode 0 Selected
   (3) Port A = Input
   (4) Port B = Input
   (5) Port C = Output

d. If step b above was performed, write C0 to X+A. (This corrects the data on bits 6 and 7.)

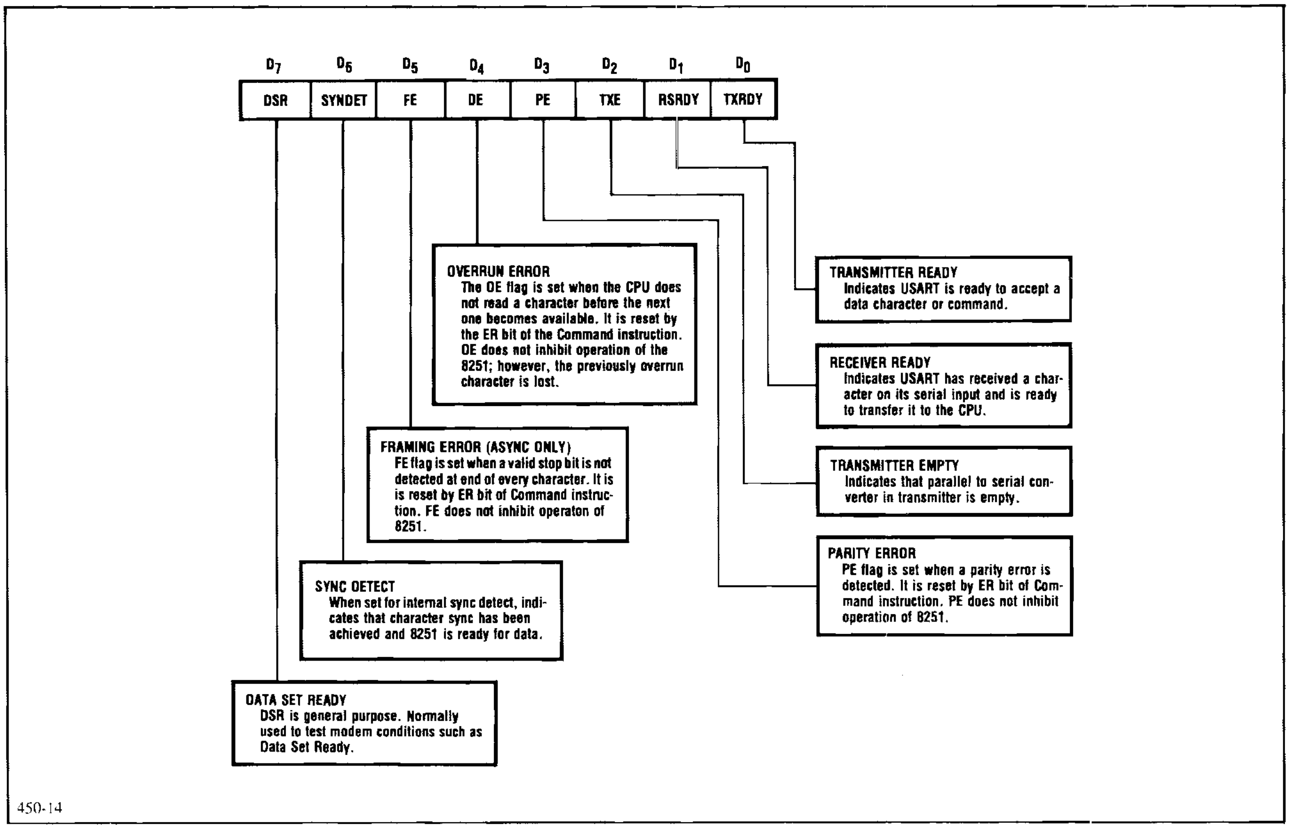

D7
D6
D5
D4
D3
D2
D1
D0
DSR
SYNDET
FE
OE
PE
TXE
RSRDY
TXRDY
OVERRUN ERROR The OE flag is set when the CPU does not read a character before the next one becomes available. It is reset by the ER bit of the Command instruction. OE does not inhibit operation of the 8251; however, the previously overrun character is lost.
TRANSMITTER READY Indicates USART is ready to accept a data character or command.
RECEIVER READY Indicates USART has received a character on its serial input and is ready to transfer it to the CPU.
FRAMING ERROR (ASYNC ONLY) FE flag is set when a valid stop bit is not detected at end of every character. It is is reset by ER bit of Command instruction. FE does not inhibit operaton of 8251.
TRANSMITTER EMPTY Indicates that parallel to serial converter in transmitter is empty.
PARITY ERROR PE flag is set when a parity error is detected. It is reset by ER bit of Command instruction. PE does not inhibit operation of 8251.
SYNC DETECT When set for internal sync detect, indicates that character sync has been achieved and 8251 is ready for data.
DATA SET READY DSR is general purpose. Normally used to test modem conditions such as Data Set Ready.
450-14

Figure 3-7. USART Status Read Format

Table 3-7. Typical USART Status Read Subroutine

```
;STAT0 READS STATUS FROM USART 0 (PORT 0)
;USES-SETD; DESTROYS-A

            PUBLIC   STAT0
            EXTRN    BASAD,SETD

;STAT0:      CALL     SETD              ;SET DATA MODE
            IN       BASAD+1
            RET

            END
```

e. Write 00 to X + E. (This deselects the Test Mode and unmasks bits 6 and 7.)

3-19. OPERATION

Operation of the PPI consists of reading from Ports A and B and writing to Port C. Any one of the eight bits of Port C can also be selectively set or cleared. Prior to any read or write operation, the control block must be selected. (Refer to paragraph 3-3.)

3-20. READ PORT A/B DATA. Data from Port A and Port B is read by performing a read of X+8 and X+9, respectively. A typical PPI read subroutine for Port A is given in table 3-10. Bit definitions for Ports A and B are given in figure 3-9.

3-21. WRITE PORT C DATA. Data is written to Port C, or a call is placed with the ACU, by performing a write to X+A. A typical PPI write subroutine to Port C is given in table 3-11. Bit definitions for Port C are given in figure 3-10.

3-22. READ PORT C STATUS. The status of the previous bits written to Port C is obtained by performing a read to X+A.

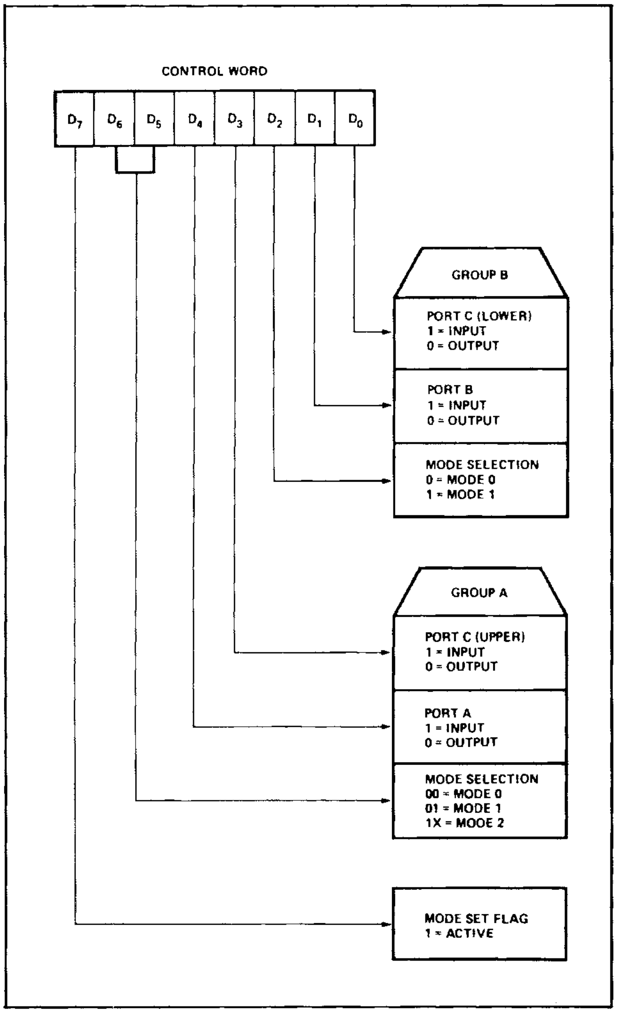
3-23. PORT C BIT SET/RESET. Any one of the eight bits of Port C can be selectively set or reset by writing a bit set/reset control word to X+B. (See figure 3-11.)

Table 3-8. PPI Interface Signals

PORT A INPUTS	PORT B INPUTS	PORT C OUTPUTS
PND	RI0 (Port 0)	NB1
DSS	RI1 (Port 1)	NB2
DLO	RI2 (Port 2)	NB4
ACR	RI3 (Port 3)	NB8
PWI or SRXD3	CD0 (Port 0)	DPR
SRXD0 or AUX 1	CD1 (Port 1)	CRQ
SRXD1 or AUX 2	CD2 (Port 2)	STXD0 or AUX 4
SRXD2 or AUX 3	CD2 (Port 3)	STXD1 or AUX 5

NOTES:

1. PND, RI, and CD signals are connected to interrupt circuit.
2. RI and CD are from serial I/O ports, which do not support these signals.
3. Dual inputs (e.g., PWI or SRXD3) are jumper wired. Refer to paragraph 2-17.



3-24. 8253 PIT PROGRAMMING

The timing functions of the iSBC 534 are controlled by a 22.1184-MHz crystal oscillator. This clock frequency is divided by 9 and by 18 to produce two jumper-selectable inputs (2.4576 and 1.2288 MHz) to the two Programmable Interval Timer chips (PIT 0 and PIT 1). Each PIT chip includes three counters, for a total of six counters designated Counters 0 through 5.

If the default (factory connected) jumpers are retained, all six counters receive the 1.2288-MHz clock. Default jumpers also connect the outputs of Counters 0 through 3 (BDG0 through BDG3) to USART chips 0 through 3, respectively. These signals are used as the TXC and RXC clocks for the respective USART chip. (Refer to paragraph 2-14.)

Counters 4 and 5 can be programmed for miscellaneous timing functions to suit the application. For example, either Counter 4 or Counter 5, or both, can be used to generate separate clock signals or real-time interrupt intervals.

Before programming, check the jumper connections for the appropriate counter clock frequency. For a clock frequency of 2.4576 MHz, a jumper is connected between posts 62 and 61. For a clock frequency of 1.2288 MHz, a jumper is connected between posts 62 and 63. These jumpers affect the Baud rate programming. Also, check the clock jumpers from each of the counter outputs (BDG0 through BDG3) to ensure that the programming for each of these counters is appropriate for the USART. Refer to paragraphs 2-11 and 2-14 for a description of jumper options.

3-25. MODE CONTROL WORD AND COUNT

All counters must be initialized separately prior to their use. The initialization for each counter consists of two steps:

a. A mode control word (figure 3-12) is written to the control register for each individual counter.

b. A down-count number is loaded into each counter; number is in one or two 8-bit bytes as determined by mode control word.

The mode control word (figure 3-12) does the following:

a. Selects counter (one of three per chip) to be loaded.

b. Selects counter operating mode (either Mode 0 or Mode 3 for iSBC 534).

c. Selects one of the following four counter read/load functions:
   (1) Counter latch (for stable read operation).
   (2) Read or load most-significant byte only.
   (3) Read or load least-significant byte only.
   (4) Read or load least-significant byte first, then most-significant byte.

d. Sets counter for either binary or BCD count.

Table 3-9. Typical PPI Initialization Subroutine

```
;INTAUX INITIALIZES AUX PARALLEL PORT.
;BITS 6&7 OF PORT C ARE MASKED BY TEST TO PREVENT CALL REQUEST
;DURING INITIALIZATION.PORT C IS THEN SET TO 0C0H.
;USES-SETC; DESTROYS-A

          PUBLIC    INTAUX
          EXTRN     SETC,STEST,CTEST,BASAD

INTAUX:   CALL      SETC
          CALL      STEST                   ;DISABLE BITS 6&7
          MVI       A,92H                   ;MODE WORD TO PPI PORT A&B IN,C OUT
          OUT       BASAD+0BH
          MVI       A,0C0H                  ;DATA WORD TO PORT C TO PREVENT CALL REQUEST
          OUT       BASAD+0AH
          CALL      CTEST                   ;REMOVE MASKING FROM BITS 6&7
          RET

          END
```

Table 3-10. Typical PPI Port Read Subroutine

```
;AREAD READS A BYTE FROM AUX. PORT A INTO REG A
;USES-SETC; DESTROYS-A

            PUBLIC  AREAD
            EXTRN   SETC,BASAD

AREAD:      CALL    SETC
            IN      BASAD+8
            RET

            END
```

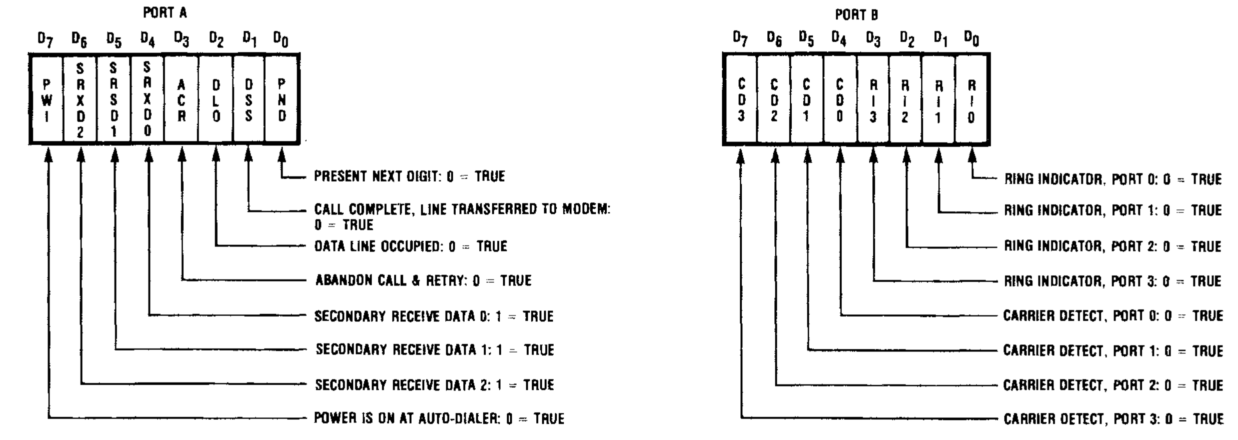

PORT A
D7 D6 D5 D4 D3 D2 D1 D0
PWI
SRXD2
SRSD1
SRXD0
ACR
DLO
DSS
PND
PRESENT NEXT DIGIT: 0 = TRUE
CALL COMPLETE, LINE TRANSFERRED TO MODEM: 0 = TRUE
DATA LINE OCCUPIED: 0 = TRUE
ABANDON CALL & RETRY: 0 = TRUE
SECONDARY RECEIVE DATA 0: 1 = TRUE
SECONDARY RECEIVE DATA 1: 1 = TRUE
SECONDARY RECEIVE DATA 2: 1 = TRUE
POWER IS ON AT AUTO-DIALER: 0 = TRUE
PORT B
D7 D6 D5 D4 D3 D2 D1 D0
CD3
CD2
CD1
CD0
RI3
RI2
RI1
RI0
RING INDICATOR, PORT 0: 0 = TRUE
RING INDICATOR, PORT 1: 0 = TRUE
RING INDICATOR, PORT 2: 0 = TRUE
RING INDICATOR, PORT 3: 0 = TRUE
CARRIER DETECT, PORT 0: 0 = TRUE
CARRIER DETECT, PORT 1: 0 = TRUE
CARRIER DETECT, PORT 2: 0 = TRUE
CARRIER DETECT, PORT 3: 0 = TRUE
450-15

Figure 3-9. PPI Port A/B Bit Definitions

Table 3-11. Typical PPI Port C Write Subroutine

```
;COUT OUTPUTS A BYTE FROM REG A TO AUX. PORT C
;USES-SETC,A; DESTROYS-NOTHING

          PUBLIC    COUT
          EXTRN     SETC,BASAD

COUT:     CALL      SETC
          OUT       BASAD+0AH
          RET

          END
```

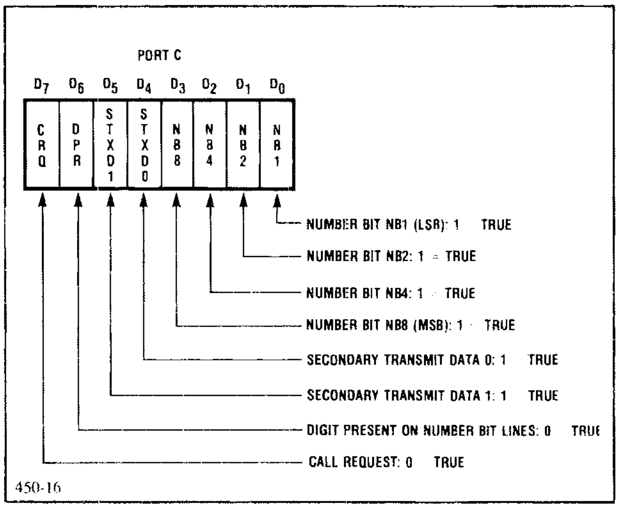

PORT C
D_7
D_6
D_5
D_4
D_3
D_2
D_1
D_0
CRQ
DPR
STXD1
STXD0
NB8
NB4
NB2
NB1
NUMBER BIT NB1 (LSR): 1 TRUE
NUMBER BIT NB2: 1 = TRUE
NUMBER BIT NB4: 1 TRUE
NUMBER BIT NB8 (MSB): 1 TRUE
SECONDARY TRANSMIT DATA 0: 1 TRUE
SECONDARY TRANSMIT DATA 1: 1 TRUE
DIGIT PRESENT ON NUMBER BIT LINES: 0 TRUE
CALL REQUEST: 0 TRUE
450-16

Figure 3-10. PPI Port C Bit Definitions

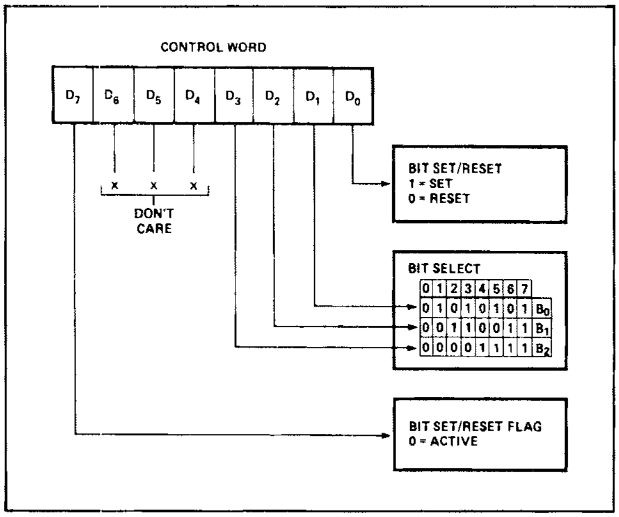


Figure 3-11. PPI Port C Bit Set/Reset Control Word Format

The mode control word and the count register bytes for any given counter must be entered in the following sequence:

a. Mode control word.
b. Least-significant count register byte.
c. Most-significant count register byte.

As long as the above procedure is followed*for each counter*, the chip can be programmed in any convenient sequence. For example, mode control words can be loaded into each of three counters per chip, followed by the least significant byte, etc. Figure 3-13 shows the two programming sequences described above.

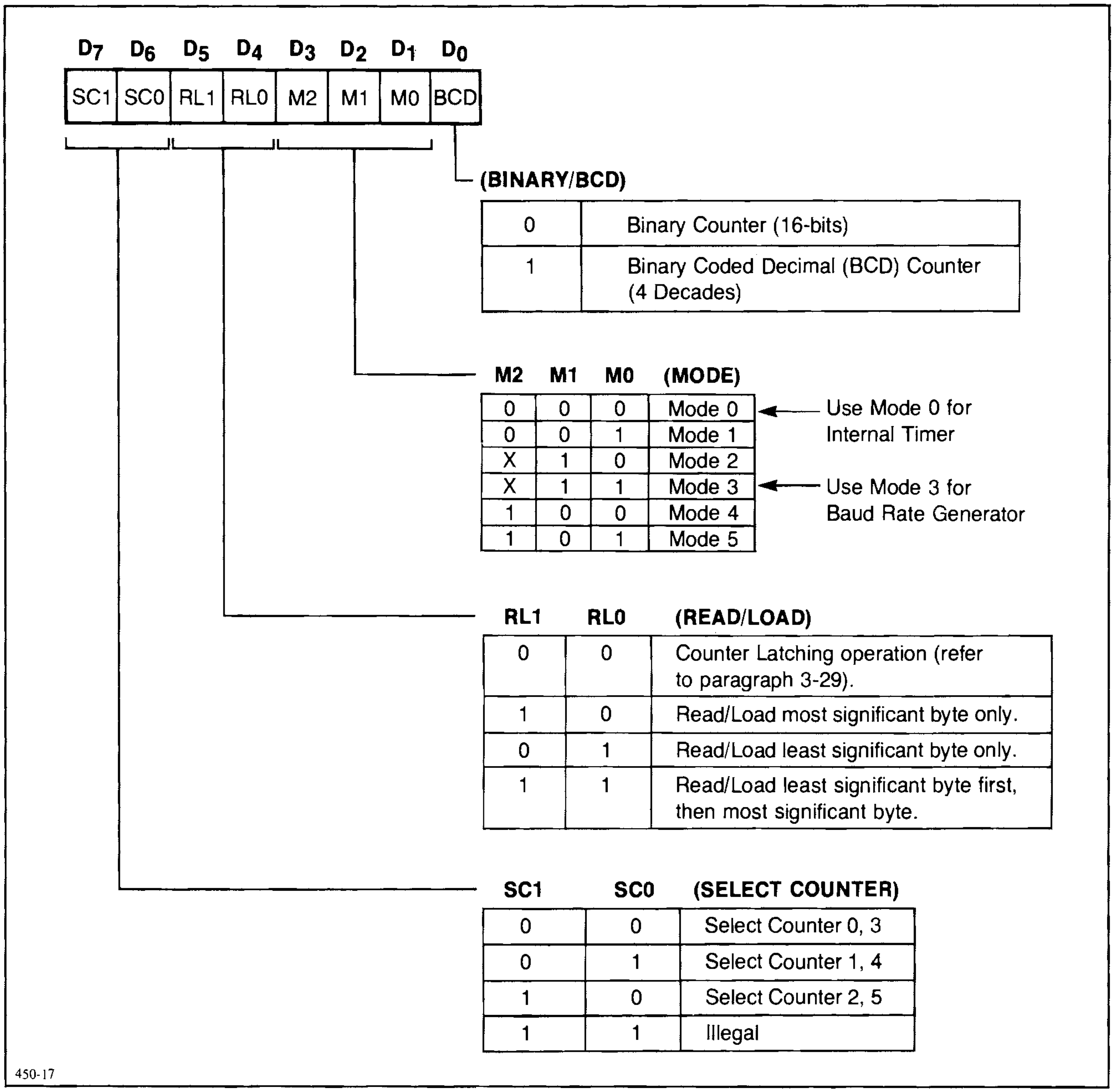
Since all counters in the PIT chip are downcounters, the value loaded in the count registers is decremented. Loading all zeroes into a count register results in a maximum count of 2^{16} for binary numbers or 10^4 for BCD numbers.

When a selected count register is to be loaded, it *must* be loaded with the number of bytes programmed in the mode control word. One or two bytes can be loaded, depending on the appropriate down count. These two bytes can be programmed at any time following the mode control word, as long as the correct number of bytes is loaded in order.

The count mode selected in the control word controls the counter output. As shown in figure 3-12, the PIT chip can operate in any of six modes; however, the iSBC 534 uses only Mode 3 and Mode 0 as follows:

a. Mode 3: Square wave generator. Mode 3, which is the primary operating mode used in the iSBC 534, is used for generating Baud rate clock signals. In this mode, the counter output remains high until one-half of the count value in the count register has been decremented (for even numbers). The output then goes low for the other half of the count. If the value in the count register is odd, the counter output is high for (N+1)/2 counts, and low for (N-1)/2 counts.

b. Mode 0: Interrupt on terminal count. This mode can be used for auxiliary functions, such as generating real-time interrupt intervals. After the count value is loaded into the count


D7 D6 D5 D4 D3 D2 D1 D0
SC1 SC0 RL1 RL0 M2 M1 M0 BCD
Use Mode 0 for Internal Timer
Use Mode 3 for Baud Rate Generator
450-17

(BINARY/BCD)

0	Binary Counter (16-bits)
1	Binary Coded Decimal (BCD) Counter (4 Decades)

M2	M1	M0	(MODE)
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RL1	RL0	(READ/LOAD)
0	0	Counter Latching operation (refer to paragraph 3-29).
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

SC1	SC0	(SELECT COUNTER)
0	0	Select Counter 0, 3
0	1	Select Counter 1, 4
1	0	Select Counter 2, 5
1	1	Illegal

Figure 3-12. PIT Mode Control Word Format

register, the counter output goes low and remains low until the terminal count is reached. The output then goes high until either the count register or the mode control register is reloaded.

NOTE

Mode 0 can be used only on Counters 4 and 5 (outputs BDG4 and BDG5).

3-26. ADDRESSING

As listed in table 3-1, each PIT chip uses four consecutive control block addresses for writing the chip mode control word and for loading and reading the count register. PIT 0 uses addresses X+0 through X+3; PIT 1 uses addresses X+4 through X+7.

3-27. INITIALIZATION

To initialize the PIT chips, perform the following:

a. Select control block by performing a write to X+C.

b. Write mode control word for PIT 0 Counter 0 to X+3. Note that *all* mode control words for PIT 0 are written to X+3, since mode control word must specify which counter is being programmed. (Refer to figure 3-12.) Table 3-12 provides a sample subroutine for writing mode control words to the six counters comprising PIT 0 and PIT 1.

c. Assuming mode control word has selected a 2-byte load, load least-significant byte of count into Counter 0 at X+0. (Count value to be loaded is described in paragraphs 3-30 through 3-32.) Table 3-13 provides a sample subroutine for loading 2-byte count value.

PROGRAMMING FORMAT

Step		
1		Mode Control Word Counter n
2	LSB	Count Register Byte Counter n
3	MSB	Count Register Byte Counter n

ALTERNATE PROGRAMMING FORMAT

Step		
1		Mode Control Word Counter 0
2		Mode Control Word Counter 1
3		Mode Control Word Counter 2
4	LSB	Counter Register Byte Counter 1
5	MSB	Count Register Byte Counter 1
6	LSB	Count Register Byte Counter 2
7	MSB	Count Register Byte Counter 2
8	LSB	Count Register Byte Counter 0
9	MSB	Count Register Byte Counter 0

450-18

Figure 3-13. PIT Programming Sequence Examples

Table 3-12. Typical PIT Control Word Subroutine

```
;INTTMR INITIALIZES INTERVAL TIMERS PIT 0 AND PIT 1
;FOUR OF THE COUNTERS ARE INITIALIZED AS BAUD RATE GENERATORS.
;THE OTHER TWO COUNTERS ARE SET UP AS INTERRUPT TIMERS.
;ALL SIX COUNTERS ARE SET UP FOR 16-BIT BINARY OPERATION.
;USES-SETC; DESTROYS-A

         PUBLIC  INTTMR
         EXTRN   SETC,BASAD

INTTMR:  CALL    SETC
         MVI     A,36H                ;MODE 3 CONTROL WORD FOR COUNTERS 0 & 3
         OUT     BASAD+3
         OUT     BASAD+7
         MVI     A,76H                ;MODE 3 CONTROL WORD FOR COUNTER 1
         OUT     BASAD+3
         MVI     A,0B6H               ;MODE 3 CONTROL WORD FOR COUNTER 2
         OUT     BASAD+3
         MVI     A,70H                ;MODE 0 CONTROL WORD FOR COUNTER 4
         OUT     BASAD+7
         MVI     A,0B0H               ;MODE 0 CONTROL WORD FOR COUNTER 5
         OUT     BASAD+7
         RET

         END
```

d. Load most-significant byte of count into Counter 0 at X+0.

NOTE

Be sure to enter the downcount in two bytes if the counter was programmed for a two-byte entry in the mode control word. Similarly, enter the downcount value in BCD if the counter was so programmed.

e. Repeat steps b, c, and d for PIT 0 Counters 1 and 2, and for PIT 1 counters as necessary. Refer to table 3-1 for control block addresses.

3-28. OPERATION

The following paragraphs describe operating procedures for a counter read, clock frequency divide/ratio selection, and interrupt timer count selection.

3-29. COUNTER READ. For Mode 3 operation, there usually is no requirement to reset or read the counters; however, it is possible to do so at any time. If a count register is reloaded during counting in Mode 3, the new value is reflected immediately following the output transition of the current count. For Mode 0 (interrupt on terminal count), reloading during counting has the following results:

a. Loading first byte stops current count.

b. Loading second byte starts new count.

If desired, it is possible to read the count register during the down count. The recommended procedure is to use a mode control word to latch the contents of the count register; this ensures that the count reading is accurate and stable. The latched value of the count can then be read by the main processor.

NOTE

If a counter is read during the down count, it is mandatory to complete the read procedure; that is, if two bytes were programmed to the counter, then two bytes *must* be read before any other operations are performed with that counter.

To read the count of a particular counter, select control block by performing a write to X+C and proceed as follows (a typical counter read subroutine is given in table 3-14):

a. Write counter register latch control word (figure 3-14) to X+3 (PIT 0) or to X+7 (PIT 1), as appropriate. Control word specifies desired counter and selects counter latching operation.

b. Perform a read operation of desired counter; refer to table 3-1 for counter addresses.

NOTE

Be sure to read one or two bytes, whichever was specified in the initialization mode control word. For two bytes, read in the order specified.

3-30. CLOCK FREQUENCY/DIVIDE RATIO SELECTION. The internal clock output-default jumper is connected so that the clock output frequency is 1.2288 MHz. The jumper can be changed so the output frequency is 2.4576 MHz. (Refer to paragraph 2-10.) This clock signal is divided by the counters in the two PIT chips to generate signals BDG0 through BDG5. The default wiring, in turn, connects signals BDG0 through BDG3 to the USART transmit clock (TXC) and receive clock (RXC) inputs as shown in table 2-5.

Each counter must be programmed with a downcount number, or count value N. When count value N is loaded into a PIT counter, it becomes the clock divisor. To derive N for either synchronous or asynchronous operation, use the procedures described in following paragraphs.

Table 3-13. Typical PIT Count Value Load Subroutine

```
;LOAD0 LOADS COUNTER 0 FROM D&E. D IS MSB, E IS LSB.
;USES-STC,D,E; DESTROYS-A

        PUBLIC  LOAD0
        EXTRN   SETC,BASAD

LOAD0:  CALL    SETC
        MOV     A,E          ;GET LSB
        OUT     BASAD+0
        MOV     A,D          ;GET MSB
        OUT     BASAD+0
        RET

        END
```

Table 3-14. Typical PIT Counter Read Subroutine

```
;READ5 READS COUNTER 5 ON-THE-FLY INTO D&E. MSB IN D, LSB IN E.
;USES-SETC; DESTROYS-A,D,E

        PUBLIC  READ5
        EXTRN   SETC,BASAD

READ5:  CALL    SETC
        MVI     A,80H           ;MODE WORD FOR LATCHING COUNTER 5 VALUE
        OUT     BASAD+7
        IN      BASAD+6         ;LSB OF COUNTER
        MOV     E,A
        IN      BASAD6          ;MSB OF COUNTER
        MOV     D,A
        RET

        END
```

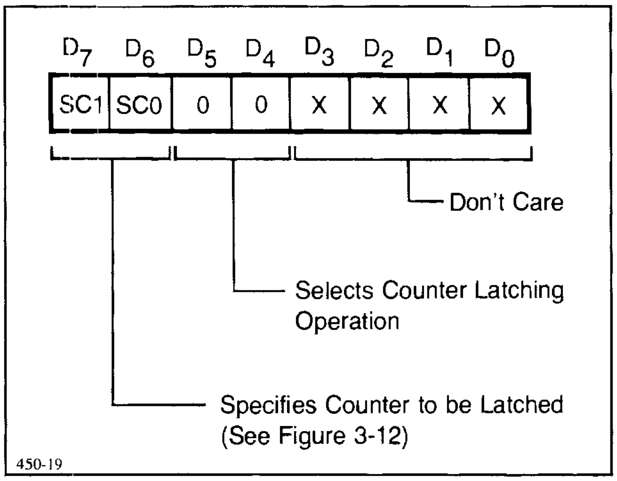

D7 D6 D5 D4 D3 D2 D1 D0
SC1 SC0 0 0 X X X X
Don't Care
Selects Counter Latching Operation
Specifies Counter to be Latched (See Figure 3-12)
450-19

Figure 3-14. PIT Counter Register Latch Control Word Format

3-31. *Synchronous Mode.* In the synchronous mode, the TXC and/or RXC rates equal the Baud rate. Therefore, the count value is determined by

$$N = C/B$$

where N is the count value,
B is the desired Baud rate, and
C is 1.2288 MHz, the internal clock frequency.

Thus, for a 4800 Baud rate, the required count value (N) is:

$$N = \frac{1.2288 \times 10^6}{4800} = \underline{\underline{256}}.$$

If the binary equivalent of count value N = 256 is loaded into Counter 0 of PIT 0, then the output frequency of BDG0 (for USART 0) is 4800 Hz, which is the desired clock rate for synchronous mode operation.

3-32. *Asynchronous Mode.* In the asynchronous mode, the TXC and/or RXC rates equal the Baud rate times of the following multipliers: X1, X16, or X64. Therefore, the count value is determined by

$$N = C/BM$$

where N is the count value,
B is the desired Baud rate,
M is the Baud rate multiplier (1, 16, or 64), and
C is 1.2288 MHz, the internal clock frequency.

Thus, for a 4800 Baud rate, the required count value (N) is

$$N = \frac{1.2288 \times 10^6}{4800 \times 16} = \underline{\underline{16}}.$$

If the binary equivalent of count value N = 16 is loaded into Counter 1 of PIT 0, then the output frequency of BDG1 (for USART 1) is 4800 × 16 Hz, which is the desired clock rate for asynchronous mode operation. Count values (N) versus rate multiplier (M) for each Baud rate are listed in table 3-15.

NOTE

During initialization, be sure to load the count value (N) into the appropriate PIT counter and the Baud rate multiplier (M) into the USART.

Table 3-15. PIT Count Value Vs Rate Multiplier for Each Baud Rate

BAUD RATE (B)	*COUNT VALUE (N) FOR		
	M = 1	M = 16	M = 64
75	16384	1024	256
110	11171	698	175
150	8192	512	128
300	4096	256	64
600	2048	128	32
1200	1024	64	16
2400	512	32	8
4800	256	16	4
9600	128	8	
19200	64	4	
38400	32	2	
76800	16		

*Count Values (N) assume clock is 1.2288 MHz. Double Count Values (N) for 2.4576 MHz clock. Count Values (N) and Rate Multipliers (M) are in decimal.

3-33. RATE GENERATOR/INTERVAL TIMER. Table 3-16 shows the maximum and minimum timer intervals when Counters 4 and 5 of PIT 1 are connected in parallel or series. These counters generate signals BDG4 and BDG5, which can be used either as auxiliary clock counters or to generate interrupt intervals.

Table 3-16. PIT Rate Generator Frequencies and Timer Intervals

FUNCTION	SINGLE TIMER (BDG0 THRU BDG5)		DUAL TIMER (BDG4 AND BDG5 IN SERIES)	
	Minimum	Maximum	Minimum	Maximum
Rate Generator (Frequency)	18.75 Hz	614.4 kHz	0.00029 Hz	307.2 kHz
Real-Time Interrupt (Interval)	1.63 μsec	53.3 msec	3.26 μsec	58.25 minutes

3-34. INTERRUPT TIMER. To program an interval timer for an interruption terminal count, program the appropriate PIT for the correct operating mode (Mode 0) in the control word. Then load the count value (N), which is derived by

$$N = TC$$

where

N is the timer count value
T is the desired interrupt time interval in seconds, and
C is the internal clock frequency (Hz).

Table 3-17 shows the count value (N) required for several time intervals (T) that can be generated for outputs BDG4 and BDG5.

Table 3-17. PIT Time Intervals Vs Timer Counts

T	N*
10 μsec	12
100 μsec	123
1 msec	1229
10 msec	12288
50 msec	61440

*Count Values (N) assume clock is 1.2288 MHz. Double Count Values (N) for 2.4576 MHz clock. Count Values (N) are in decimal.

3-35. 8259 PIC PROGRAMMING

As shown in figure 2-2, PIC 0 and PIC 1 each monitor input signals from eight separate sources. When one or more of the eight input signals are active (true), the PIC determines the following:

a. Which input signal has the highest priority.

b. Whether the input signal has a higher priority than the interrupt presently being serviced by the main processor. If so, the interrupt being serviced is interrupted; if not, the input signal is held for later output.

c. Whether the interrupt input bit is masked.

Thus, the basic functions of each PIC are (1) resolve the priority of interrupt requests and (2) issue a single interrupt request to the main processor based on that priority. As shown in figure 2-2, the outputs of both PIC 0 and PIC 1 are connected via default jumpers to INT1/ on the Multibus.

The PIC chips can be operated only in the polled interrupt mode. The interrupt sequence is:

a. The iSBC 534 logic generates an interrupt, which is received by the main processor.

b. The main processor polls one or both PIC chips by writing a polling command word to the PIC chip(s).

c. The main processor then performs a Read Command to the appropriate PIC chip.

d. The addressed PIC chip interprets the Read Command as an interrupt acknowledge, and responds by placing the following data on the data bus:
   (1) A "1" in the most significant bit (D7) if there is an interrupt.
   (2) A BCD code with a highest priority interrupt level that is requesting service; this code is in the three least-significant bits. The main processor then uses the encoded data to generate an interrupt vector.

e. The main processor responds by writing an End-Of-Interrupt (EOI) command.

f. The EOI command clears the output data from the PIC chip; if there is a second (lower priority) interrupt, the PIC will re-request service. The additional data is then available with the next polling routine.

g. If necessary, the above sequence can be performed for both PIC chips.

3-36. INTERRUPT PRIORITY MODES

Each PIC has two modes for resolving the priority of interrupt inputs: (1) fully nested mode and (2) rotating mode. The rotating mode has two variations: (1) auto-rotating and specific rotating.

3-37. FULLY NESTED MODE. In this mode the PIC input signals are assigned priority from 0 through 7. The PIC operates in this mode unless specifically programmed otherwise. Interrupt IR0 has the highest priority and IR7 has the lowest priority. When an interrupt is acknowledged, the highest priority request is available to the main processor. Lower priority interrupts are inhibited; higher priority interrupts will be able to generate an interrupt that will be acknowledged if the main processor has enabled its own interrupt input through its software. The End-Of-Interrupt (EOI) command from the main processor is required to reset the PIC for the next interrupt.

3-38. AUTO-ROTATING MODE. In this mode the interrupt priority rotates. Once an interrupt on a given input is serviced, that interrupt assumes the lowest priority. Thus, if there are a number of simultaneous interrupts, the priority will rotate among the interrupts in numerical order. For example, if interrupts IR4 and IR6 request service simultaneously, IR4 will receive the highest priority. After service, the priority level rotates so that IR4 has the lowest priority and IR5 assumes the highest priority. In the worst case, seven other interrupts are serviced before IR4 again has the highest priority. Of course, if IR4 is the only request, it is serviced promptly. In the Auto-Rotating Mode, priority shifts when the PIC chip receives an EOI command.

3-39. SPECIFIC ROTATING MODE. In this mode the software can change interrupt priority by specifying the bottom priority, which automatically sets the highest priority. For example, if IR5 is assigned the bottom priority, IR6 assumes the highest priority. In the specific rotating mode, the priority can be rotated by writing a Specific Rotate at EOI (SEOI) command to the PIC chip. This command contains the BCD code of the interrupt being serviced; that interrupt is reset as the bottom priority. In addition, the bottom priority interrupt can be fixed at any time by writing a command word to the PIC chip.

3-40. INTERRUPT MASK

One or more of the eight interrupt request inputs can be individually masked during the PIC initialization or at any subsequent time. If an interrupt is masked while it is being serviced, lower priority interrupts are inhibited. There are two ways to enable the lower priority interrupts:

a. Write an End-of-Interrupt (EOI) command.
b. Set the Special Mask Mode.

The Special Mask Mode is useful when one or more interrupts are masked. If for any reason an input is masked while it is being serviced, the lower priority interrupts are disabled. However, it is possible to enable the lower priority interrupt with the Special Mask Mode. In this mode, the lower priority lines are enabled until the Special Mask Mode is reset. Higher priorities are not affected.

3-41. STATUS READ

Interrupt request inputs is handled by the following two internal PIC registers:

a. Interrupt Request Register (IRR), which stores all interrupt levels that are requesting service.

b. In-Service Register (ISR), which stores all interrupt levels that are being serviced.

Either register can be read by writing a suitable command word and then performing a read operation.

3-42. INITIALIZATION COMMAND WORDS

Normal initialization for a PIC chip consists of writing two or three 8-bit Initialization Command Words as shown in figure 3-15. Since the iSBC 534 does not use the 8080 CALL sequence, and there are no slave PIC chips, the initialization sequence is greatly simplified in that only two Initialization Command Words are required:

a. The first Initialization Command Word (ICW1), which specifies:
   (1) Memory address intervals for the interrupt service routines for the eight interrupts serviced by the PIC. Since there are no memory address intervals, the address interval bits (D5 through D7) can be arbitrarily set to zero. Similarly, the CALL address interval is arbitrarily set to 4 (D2 = 1).
   (2) Whether or not there are slave (cascaded) PIC chips associated with the chip being programmed. The iSBC 534 has no slave PIC chips, therefore set D1 = 1.
   (3) Three fixed bits (D0, D3, D4) that identify the word as ICW1.

b. The second word (ICW2) specifies address bits A8 through A15 of the interrupt service routine vector; there is no vector, so ICW2 is arbitrarily set at zero.

NOTE

The third word (ICW3) is used only if there are "slave" PIC chips in the system; hence, ICW3 is omitted.

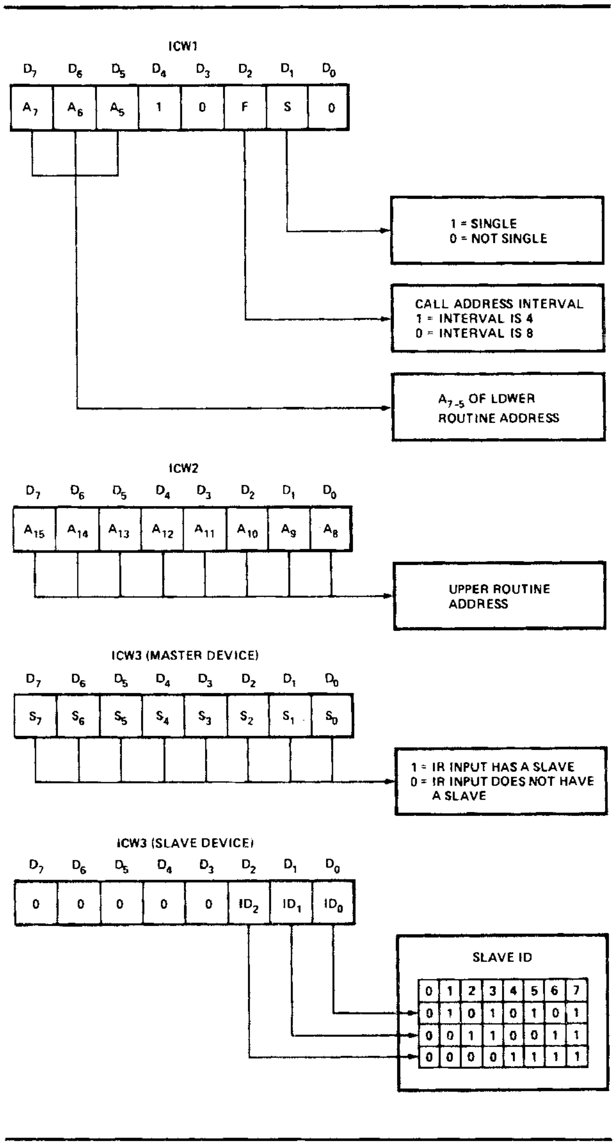

ICW1
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
A_7 A_6 A_5 1 0 F S 0
1 = SINGLE
0 = NOT SINGLE
CALL ADDRESS INTERVAL
1 = INTERVAL IS 4
0 = INTERVAL IS 8
A_{7-5} OF LOWER ROUTINE ADDRESS
ICW2
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8
UPPER ROUTINE ADDRESS
ICW3 (MASTER DEVICE)
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0
1 = IR INPUT HAS A SLAVE
0 = IR INPUT DOES NOT HAVE A SLAVE
ICW3 (SLAVE DEVICE)
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
0 0 0 0 0 ID_2 ID_1 ID_0
SLAVE ID
0 1 2 3 4 5 6 7
0 1 0 1 0 1 0 1
0 0 1 1 0 0 1 1
0 0 0 0 1 1 1 1

Figure 3-15. PIC Initialization Control Word Formats

As a result, the two PIC chips are initialized by writing ICW1 and ICW2 as follows:

a. ICW1 = 16H to PIC 0 (X+8) and PIC 1 (X+A).
b. ICW2 = 00H to PIC 0 (X+9) and PIC 1 (X+B).

3-43. OPERATION COMMAND WORDS

After being initialized, the PIC chips can be programmed at any time for various interrupt modes. The Operation Command Word (OCW) formats are shown in figure 3-16 and discussed in paragraph 3-46.

3-44. ADDRESSING

Each of the two PIC chips uses two consecutive addresses for writing to and reading internal registers. Address functions pertinent to iSBC 534 programming are identified in table 3-1.

3-45. INITIALIZATION

To initialize PIC 0 and PIC 1, proceed as follows (table 3-18 provides a typical initialization subroutine):

a. Disable system interrupts. For systems based on 8080/8085 microprocessor, use DI (Disable Interrupts) instruction.
b. Select iSBC 534 data block by performing a write to X+D.
c. Write ICW1 to PIC 0 at X+8 (for most applications, ICW1 = 16).
d. Write ICW2 to PIC 0 at X+9 (for most applications, ICW2 = 00).
e. Repeat steps c and d for PIC 1 as follows:
   (1) Write ICW1 to X+A.
   (2) Write ICW2 to X+B.
e. Enable system interrupts. For systems based on 8080/8085 microprocessor, use EI (Enable Interrupts) instruction.

NOTE

The PIC chips operate in the fully nested mode after the initialization sequence without requiring any Operation Control Word (OCW).

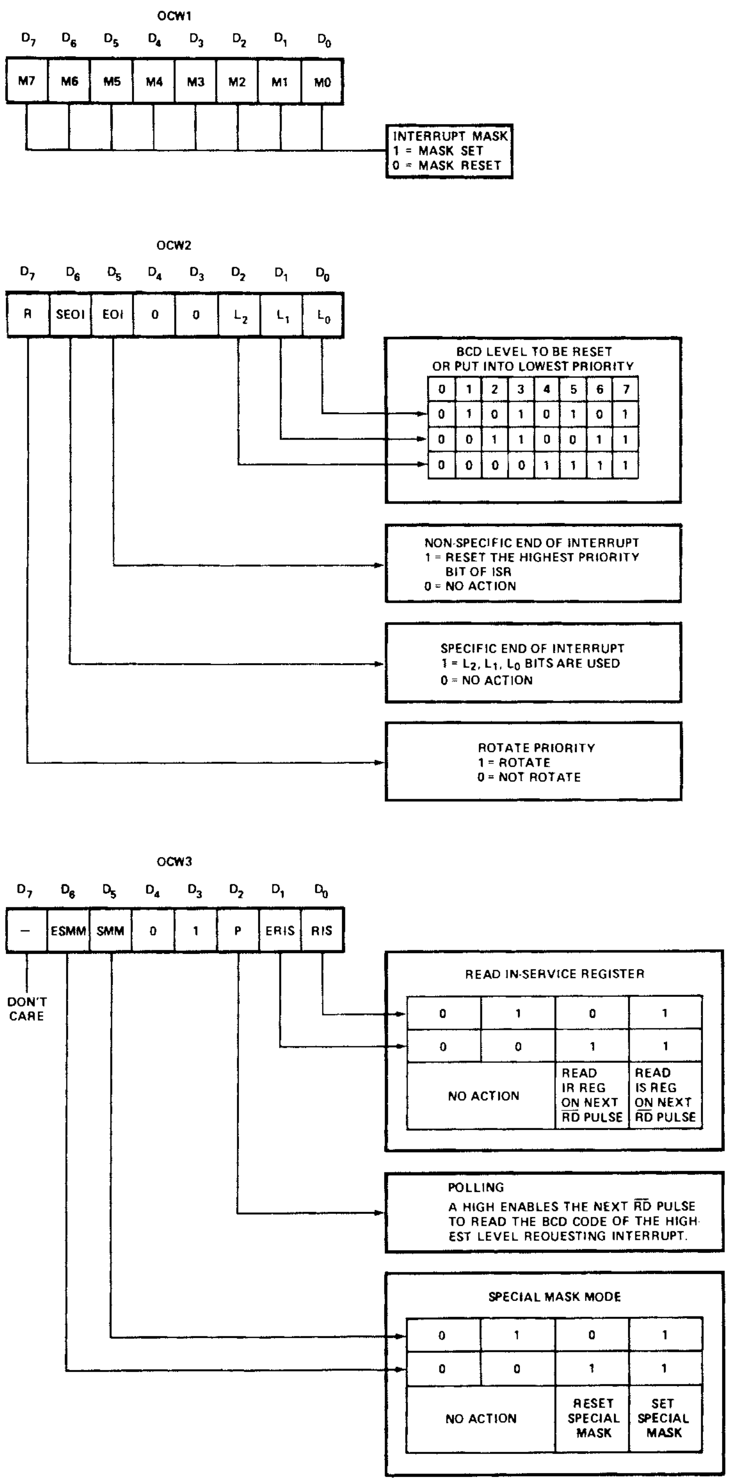
3-46. OPERATION

After initialization, the PIC chips can be programmed at any time for the following operations:

a. Auto-rotating priority.
b. Specific rotating priority.
c. Status read of Interrupt Request Register (IRR).
d. Status read of In-Service Register (ISR).
e. Interrupt mask bits set, reset, or read.
f. Special mask mode set or reset.

Table 3-19 lists details of the above operations. Note that an End-Of-Interrupt (EOI) or a Special End-Of-Interrupt (SEOI) command is required at the end of each interrupt service routine to reset the ISR. The EOI command is used in the fully nested and auto-rotating priority modes and the SEOI command, which specifies the bit to be reset, is used in the specific rotating priority mode. Tables 3-20 through 3-24 provide typical subroutines for the following:

a. Read IRR (table 3-20).
b. Read ISR (table 3-21).
c. Set mask register (table 3-22).
d. Read mask register (table 3-23).
e. Issue EOI command (table 3-24).


OCW1
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
M7 M6 M5 M4 M3 M2 M1 M0
INTERRUPT MASK
1 = MASK SET
0 = MASK RESET
OCW2
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
R SEOI EOI 0 0 L_2 L_1 L_0
BCD LEVEL TO BE RESET
OR PUT INTO LOWEST PRIORITY
NON-SPECIFIC END OF INTERRUPT
1 = RESET THE HIGHEST PRIORITY
BIT OF ISR
0 = NO ACTION
SPECIFIC END OF INTERRUPT
1 = L_2, L_1, L_0 BITS ARE USED
0 = NO ACTION
ROTATE PRIORITY
1 = ROTATE
0 = NOT ROTATE
OCW3
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
— ESMM SMM 0 1 P ERIS RIS
DON'T
CARE
READ IN-SERVICE REGISTER
POLLING
A HIGH ENABLES THE NEXT $\overline{RD}$ PULSE
TO READ THE BCD CODE OF THE HIGHEST LEVEL REQUESTING INTERRUPT.
SPECIAL MASK MODE

BCD LEVEL TO BE RESET OR PUT INTO LOWEST PRIORITY

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

READ IN-SERVICE REGISTER

0	1	0	1
0	0	1	1
NO ACTION		READ IR REG ON NEXT $\overline{RD}$ PULSE	READ IS REG ON NEXT $\overline{RD}$ PULSE

SPECIAL MASK MODE

0	1	0	1
0	0	1	1
NO ACTION		RESET SPECIAL MASK	SET SPECIAL MASK

Figure 3-16. PIC Operation Control Word Formats

Table 3-18. Typical PIC Initialization Subroutine

```
;INT59 INITIALIZES PIC0 AND PIC1.
;THE MASKS ON BOTH PIC'S ARE SET, DISABLING ALL INTERRUPTS
;USES-SETD,SMASK0,SMASK1; DESTROYS-A

        PUBLIC  INT59
        EXTRN   SETD,BASAD,SMASK0,SMASK1

INT59:  CALL    SETD
        MVI     A, 16H              ;ICW1 INSTRUCTION TO BOTH PIC'S
        OUT     BASAD+8
        OUT     BASAD+0AH
        XRA     A
        OUT     BASAD+9             ;ICW2 INSTRUCTION
        OUT     BASAD+0BH
        MVI     A,0FFH              ;SET MASKS
        CALL    SMASK0
        CALL    SMASK1
        RET

        END
```

Table 3-19. PIC Operation Procedures

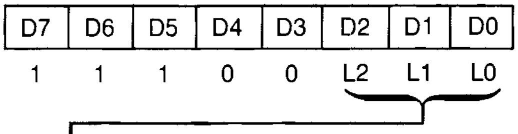
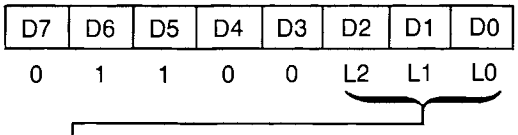
OPERATION	PROCEDURE
Auto-Rotating Priority Mode	To set: In OCW2, write a Rotate Priority at EOI command (A0H) to X+8 (PIC 0) or X+A (PIC 1). Terminate interrupt and rotate priority: In OCW2, write EOI command (20H) to X+8 (PIC 0) or X+A (PIC 1).
Specific Rotating Priority Mode	To set: In OCW2, write a Rotate Priority at SEOI command in the following format to X+8 (PIC 0) or X+A (PIC 1):  BCD of IR line to be reset and/or put into lowest priority. To terminate interrupt and rotate priority: In OCW2, write an SEOI command in the following format to X+8 (PIC 0) or X+A (PIC 1):  BCD of ISR flip-flop to be reset.

Table 3-19. PIC Operation Procedures (Continued)

<table>
<tr><th>OPERATION</th><th>PROCEDURE</th></tr>
<tr><td></td><td>To rotate priority without EOI:
In OCW2, write a command word in the following format to X+8 (PIC 0) or X+A (PIC 1):
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>L2</td><td>L1</td><td>L0</td></tr>
</table>
BCD of bottom priority IR line.</td></tr>
<tr><td>Interrupt Request Register (IRR) Status</td><td>The IRR stores a "1" in the associated bit for each IR input line that is requesting an interrupt. To read the IRR (refer to footnote):
(1) Write 0AH to X+8 (PIC 0) or X+A (PIC 1)
(2) Read X+8 (PIC 0) or X+A (PIC 1). Status format is:
<table>
<tr><td></td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>IR Line:</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>In-Service Register (ISR) Status</td><td>The ISR stores a "1" in the associated bit for priority inputs that are being serviced. The ISR is updated when an EOI command is issued. To read the ISR (refer to footnote):
(1) Write 0BH to X+8 (PIC 0) or X÷A (PIC 1).
(2) Read X+8 (PIC 0) or X+A (PIC 1). Status format is:
<table>
<tr><td></td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>IR Line:</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
</table>
Be sure to reset ISR bit at end-of-interrupt when in the following modes: Auto-Rotating (both types) and Special Mask. To reset ISR in OCW2, write:
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>L2</td><td>L1</td><td>L0</td></tr>
</table>
BCD identifies bit to be reset.</td></tr>
<tr><td>Interrupt Mask Register</td><td>To set mask bits in OCW1, write the following mask byte to X+9 (PIC 0) or X+B (PIC 1):
<table>
<tr><td></td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>IR Bit Mask:</td><td>M7</td><td>M6</td><td>M5</td><td>M4</td><td>M3</td><td>M2</td><td>M1</td><td>M0</td></tr>
</table>
1 = Mask Set, 0 = Mask Reset
To read mask bits, read X+9 (PIC 0) or X+B (PIC 1).</td></tr>
</table>

Table 3-19. PIC Operation Procedures (Continued)

OPERATION	PROCEDURE
Special Mask Mode	The Special Mask Mode enables desired bits that have been previously masked; lower priority bits are also enabled. To set, write 68H to X+8 (PIC 0) or X+A (PIC 1). To reset, write 48H to X+8 (PIC 0) or X+A (PIC 1).
NOTE: If previous operation was addressed to same register, it is not necessary to rewrite the OCW.	

Table 3-20. Typical PIC Interrupt Request Register Read Subroutine

```
;RR0 READS INTERRUPT REQUEST REG OF PIC 0
;USES-SETD; DESTROYS-A

          PUBLIC RR0
          EXTRN  SETD,BASAD

RR0:      CALL   SETD
          MVI    A,0AH              ;OCW3 RR INSTRUCTION TO PIC 0
          OUT    BASAD+8
          IN     BASAD+8
          RET

          END
```

Table 3-21. Typical PIC In-Service Register Read Subroutine

```
;RIS0 READS IN-SERVICE REGISTER OF PIC 0
;USES-SETD; DESTROYS-A

          PUBLIC RIS0
          EXTRN  SETD,BASAD

RIS0:     CALL   SETD
          MVI    A,08H              ;OCW3 RIS INSTRUCTION TO PIC 0
          OUT    BASAD+8
          IN     BASAD+8
          RET

          END
```

Table 3-22. Typical PIC Set Mask Register Subroutine

```
;SMASKO STORES A REG INTO MASK REG OF PIC 0
;A ONE MASKS OUT AN INTERRUPT,A ZERO ENABLES IT
;USES-A,SETD; DESTROYS-NOTHING

        PUBLIC    SMASKO
        EXTRN     SETD,BASAD

SMASKO: CALL      SETD
        OUT       BASAD+9
        RET

        END
```

Table 3-23. Typical PIC Mask Register Read Subroutine

```
;RMASKO READS MASK REG OF PIC 0 INTO A REG
;USES-SETD; DESTROYS-A

                PUBLIC      RMASKO
                EXTRN       SETD,BASAD

RMASKO:         CALL        SETD
                IN          BASAD+9
                RET

                END
```

Table 3-24. Typical PIC End-of-Interrupt Command Subroutine

```
;EOI0 ISSUES END-OF-INTERRUPT TO PIC 0
;USES-SETD; DESTROYS-A

            PUBLIC      EOI0
            EXTRN       SETD,BASAD

EOI0:       CALL        SETD
            MVI         A,20H           ;NON-SPECIFIC EOI
            OUT         BASAD+8
            RET

            END
```

3-47. POLLING PROCEDURE

The polled interrupt mode is described in paragraph 3-35. To conduct a poll, write OCW3 = 0CH to X+8 (PIC 0) or to X+A (PIC 1). Then perform a Read Command to X + 8 (PIC 0) or X + A (PIC 1). If an interrupt is present, the most-significant data bit will be set and the three least-significant data bits will be a BCD representation of the highest priority interrupt pending. Refer to Appendix A for a sample interrupt service routine. A typical polling subroutine for PIC 0 is given in table 3-25.

3-48. BOARD TEST MODE

The iSBC 534 test mode performs two functions. The first function is to check the transmit and receive operation of the iSBC 534 for diagnostic routines. Each of the four serial I/O ports can be exercised to check all iSBC 534 circuits except the parallel I/O port, the output drivers at each serial I/O port, and the current loop circuits. The iSBC 534 test mode is intended for use with system diagnostics to determine whether or not the iSBC 534 is operating properly; the test mode is not intended to troubleshoot the iSBC 534 itself.

The second function is to prevent the parallel I/O port from inadvertently making calls during board initialization or programming. The test mode disables the outputs for Digit Present (DPR) and the Call Request (CRQ) from the parallel I/O port.

3-49. OPERATION

The iSBC 534 test mode disables the following signals at the serial I/O ports:

a. Data Terminal Ready (DTR).
b. Request To Send (RTS).

In addition, the test mode connects the following outputs from each of the USART chips back to the respective USART inputs:

a. Transmit Data (TXD) output to the Receive Data input (RXD).
b. Data Terminal Ready (DTR) output to Data Set Ready (DSR) input.
c. Request To Send (RTS) output to the Clear To Send (CTS) input.
d. Transmit and Receive Clocks are connected together so that RXC and TXC are identical.

3-50. PROGRAMMING

Enter the test mode by writing 01 to X+E. Test the serial I/O ports as follows:

a. Initialize USART at I/O port under test.
b. Write USART command word that sets DTR and RTS bits.
c. Transmit a test word from port under test.
d. Read identical test word from port under test.
e. Repeat as required at other serial I/O ports.
f. Clear test mode by writing 00 to X+E.

3-51. STATUS READ

To determine if the iSBC is in the test mode, perform a read to X+E. If bit 0 = 1 in the returned data word, the iSBC 534 is in the test mode. The upper seven bits of the data word are undefined.

3-52. BOARD RESET

The iSBC 534 can be reset by performing a write to X+F. This function resets the PPI and USART chips and selects the data block addresses.

Table 3-25. Typical PIC Polling Subroutine

```
;POLL0 POLLS PIC 0 FOR HIGHEST PRIORITY INTERRUPT
;USES-SETD; DESTROYS-A

          PUBLIC    POLL0
          EXTRN     SETD,BASAD

POLL0:    CALL      SETD
          MVI       A,0CH
          OUT       BASAD+8         ;SET POLL MODE IN PIC 0
          IN        BASAD+8
          RET

          END
```

CHAPTER 4 PRINCIPLES OF OPERATION

4-1. INTRODUCTION

As shown in figure 4-1, the iSBC 534 Four Channel Communication Expansion Board has five major circuit functions:

a. Bus Interface
b. Clock and Timer Logic
c. Interrupt Logic
d. Four Serial I/O Ports
e. One Parallel I/O Port

Both active-high and active-low signals are shown on figure 4-1 and figure 5-2 (schematic diagram). A signal that ends with a slash (e.g., IOR/) denotes that the signal is active-low. Conversely, a signal without a slash denotes that the signal is active-high.

4-2. BUS INTERFACE CIRCUITS

The major functional circuits of the bus interface are shown in figure 4-2 and figure 5-2 sheet 1. These circuits perform the following:

a. Buffer Multibus I/O signals DAT0/ through DAT7/.

b. Decode address bits ADR4/ through ADR7/ to generate the board select signal.

c. Decode address bits ADR0/ through ADR3/ to generate various board control and chip select signals.

d. Decode control signals for reset, read, write, and initialization functions.

e. Generate Advanced Acknowledge XACK/ and Transfer Acknowledge XACK/ signals.

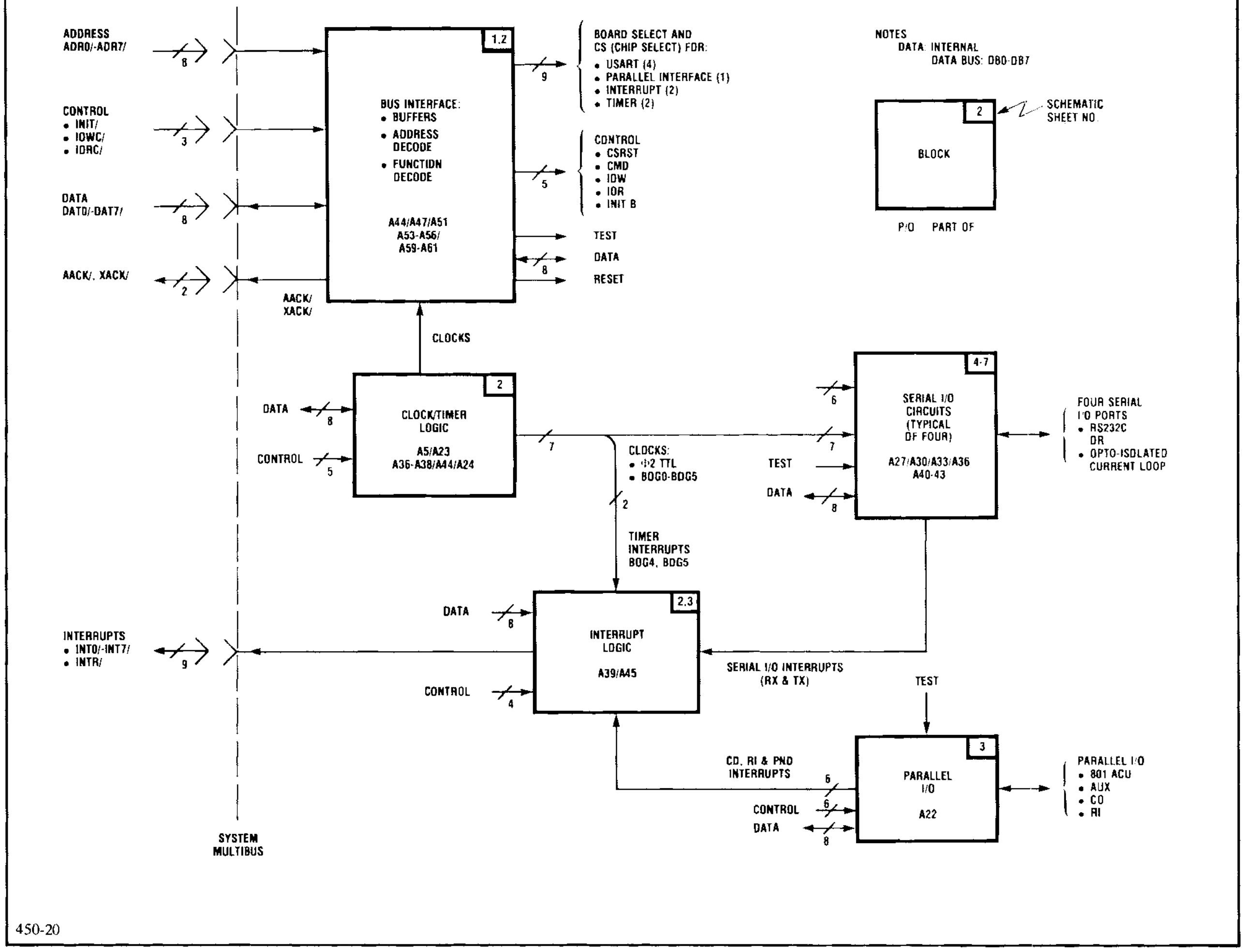


Figure 4-1. iSBC Functional Block Diagram

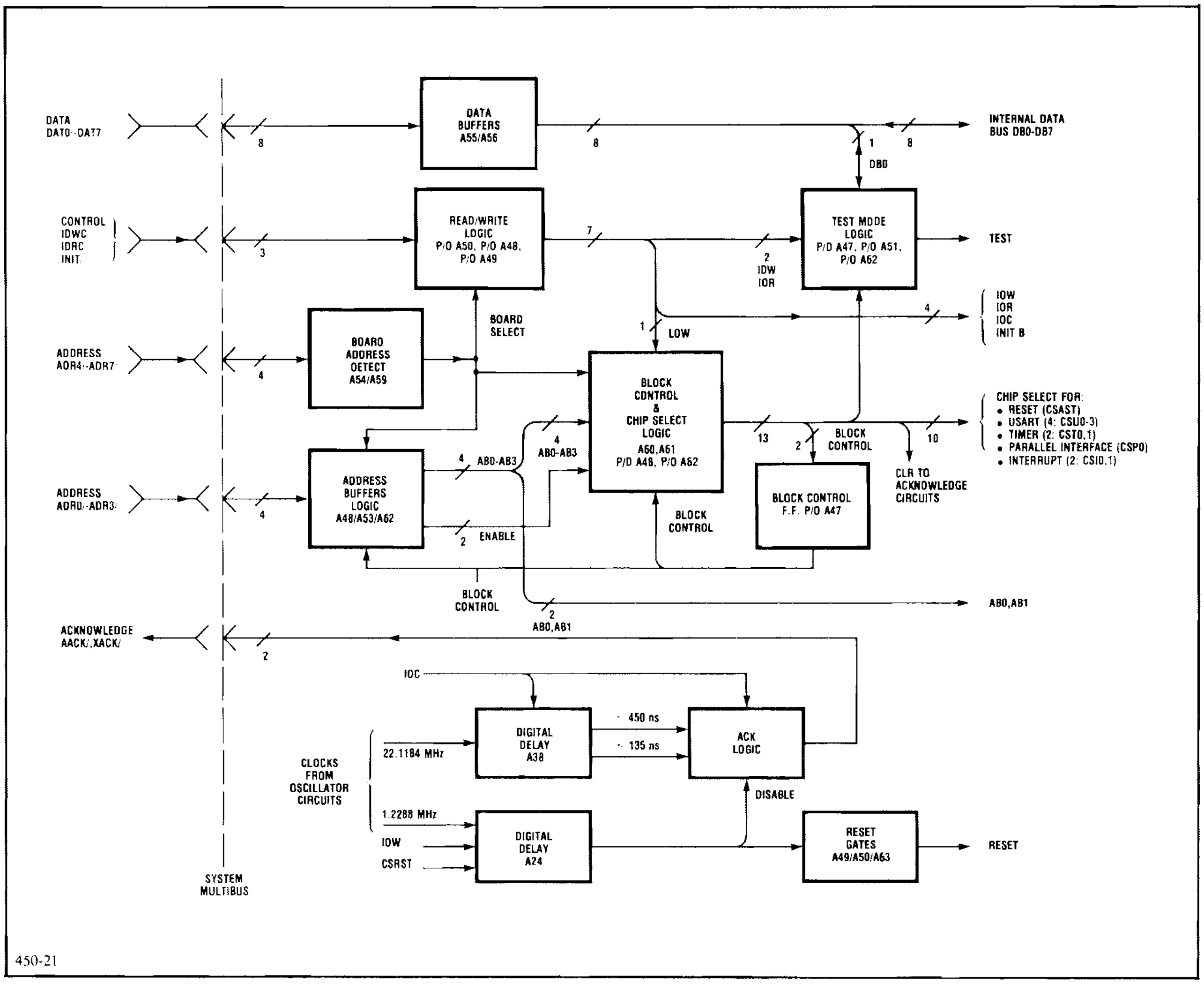


Figure 4-2. Bus Interface Functional Block Diagram

4-3. DATA BUFFERS

Data input lines DAT0/ through DAT7/ from the Multibus are buffered by the bidirectional data buffers A55 and A56 (Intel 8226 chips). The outputs of the data buffers go to the iSBC 534 internal data bus (DB0 through DB7).

4-4. BOARD ADDRESS DETECT

Most-significant address bits ADR4/ through ADR7/ from the Multibus are used in the board address detect logic. The logic consists of one section of Input Buffer A53 and Decoder A54.

Address bit ADR4/ is combined with the decoded output from A54 to generate the board select signal. The board select signal goes to the block control/ chip select logic and to the read/write logic.

4-5. ADDRESS BUFFERS

The inputs to the address buffers are least-significant address bits ADR0/ through ADR3/. The address buffer outputs are internal address bits AB0 through AB3, which go to the block control and chip select logic where they are used to generate block control and the chip select functions. Bits AB0 and AB1 bypass the chip select logic and go to the various programmable chips for function addressing.

Address bits ADR2 and ADR3 are also combined with board select and the block control bits in a logic circuit associated with the address buffers. The output of the logic is a pair of enable signals that go to the two 2-to-4 decode circuits on A61.

4-6. READ/WRITE LOGIC

The inputs to the read/write logic are IOWC/, IORC/ and INIT/ from the Multibus. These signals are used to generate internal read/write control and initialization signals. In addition, the internal IOR and IOW (read and write) signals go to the test mode logic block for generating the test mode drive signal. Finally, the internal IOW signal goes to the block control and chip select logic for generating the appropriate chip select and the block control functions.

4-7. BLOCK CONTROL/CHIP SELECT LOGIC

The block control and chip select logic circuits generate the following signals:

a. Chip select signals for the nine programmable chips.

b. Chip Reset signal CSRST.
c. A logic signal that drives the test mode logic block.
d. Two outputs that drive the block control flip-flop.

The block control/chip select logic consists of two chips:

a. Decoder chip A60 that decodes address bits AB1, AB2, and AB3; the decoded signals are the chip select signals for the four USART chips and the two interrupt controller chips (for data block addresses).

b. A dual-section 2-to-4 Decoder A61. The A section decodes address bits AB0 and AB1; the decoded signals are the Chip Select Reset (CSRST) and the drive signals for the test mode logic and the block select logic. The B section decodes address bits AB2 and AB3 to generate chip select signals for the programmable interval timers and the parallel interface chips. These chips are in the control block addresses.

4-8. BLOCK CONTROL FLIP-FLOP

The block control flip-flop receives complementary inputs from the A section of Decoder A61. The output of the block control flip-flop goes to the address buffer and logic circuit; its function is to direct two enable signals to select one of the two decoder circuits on Decoder A61 or select Decoder A60. In this manner, the block control flip-flop output enables decoder A60 or the B section of Decoder A61 for selecting either data or control block addresses. Note that the block control flip-flop is driven by the A section of the decoder A61. The output of the block control flip-flop does not affect the operation of the A section.

4-9. TEST MODE LOGIC

The test mode logic receives the following inputs:

a. Data bit DB0/.
b. Internal read and write commands IOR and IOW.
c. A control output from the block control/chip select logic.

The output of the test mode logic is a test signal that goes to all five I/O ports of the iSBC 534. In the parallel I/O port, the test signal disables certain signals in order to prevent outgoing calls when the iSBC 534 is in test mode (for this reason, the test mode is always used when initializing the iSBC 534). The test signal also goes to the four serial I/O ports where it is used to:

a. Disable certain outputs during test operations.
b. Enable loopback circuit for diagnostic routines.

The test mode logic receives read and write signals IOR/ and IOW/ and data bit DB0. The test mode is set when DB0 = 1 and IOW/ = 0; the test mode is reset when IOW = 0 and DBO = 0. Similarly, the main processor can read DB0 to check the test mode status.

4-10. ACKNOWLEDGE LOGIC

The acknowledge logic generates two acknowledge signals: Transfer Acknowledge XACK/ and Advanced Acknowledge AACK/. The acknowledge logic also generates the reset signal. The acknowledge signals are placed on the Multibus, and the reset signal is used internally in the iSBC 534.

The acknowledge logic is driven by the 22.1184-MHz signal from the clock oscillator. The clock signal goes to digital delay circuit A38, which is enabled by the IOC signal (IOC is generated by the read/write logic whenever either a read or a write command is received by the iSBC 534). When the digital delay receives IOC, it generates two separate output pulses:

a. The first pulse is delayed by 135 nanoseconds, or 2 to 3 clock periods.

b. The second pulse is delayed by 450 nanoseconds, or 9 to 10 clock periods.

Both pulses go to a logic block that contains two separate flip-flops. The first pulse generates AACK/, and the second pulse generates XACK/. These outputs go to the Multibus.

The advanced acknowledge logic can also generate an early acknowledge. (This requires an optional jumper connection.) When the jumper is in place, the advanced acknowledge circuit generates an output when the IOC command is received; this precedes the 135-nanosecond delay, since the only delay is the propagation time of the iSBC 534 logic.

Associated with the acknowledge circuit is the reset logic. The reset logic consists of a digital delay circuit and the reset gates. Digital delay A35 receives three signals:

a. 1.2288-MHz clock.
b. IOW (internal write).
c. CSRST (chip select reset).

The latter two signals drive an AND-gate that enables the digital delay. The IOW and CSRST signals turn on the reset signal and the digital delay. The reset remains on for five clock cycles; at the end of five cycles the digital delay turns off the reset signal. The signal that drives the reset gates also disables the acknowledge logic until the reset is complete at the end of the delay period.

4-11. CLOCK/TIMER LOGIC

The clock and timer logic circuits generate the Baud rate clock outputs BDG0 through BDG5. (See figure 5-2 sheet 2.) In addition, the clock circuits generate two other signals that are used as follows.

The clock circuit is controlled by a 22.1184-MHz crystal oscillator. The clock generator has two outputs: a 22.1184-MHz oscillator output and a Φ2 TTL output at 2.4576 MHz. The 22-MHz output goes to the acknowledge logic, and the Φ2 TTL output goes to a jumper matrix, a divide-by-two circuit, and the USART system clock inputs. The divider output (1.2288 MHz) also goes to the same jumper matrix as the Φ2 TTL output, and to the reset logic in acknowledge circuits.

The function of the jumper matrix is to connect one of the two clock signals (1.2288 or 2.4576 MHz) to the Baud rate generators.

The Baud rate generators consist of two Intel 8253 Programmable Interval Timer chips. Each of the PIT chips has three independent counters, each of which are separately programmable.

Four of the six independent counters are connected by default jumpers to the four USART chips. The remaining two counters serve as auxiliary timers or rate generators. A jumper matrix (pins 104 through 106) can be used to connect the timers in series. The default jumper connection is from 105 to 106, which connects the 1.2288-MHz clock signal to the clock inputs of both timers. When pin 105 is jumpered to pin 104, the output of Counter 4 (BDG4) becomes the clock input of Counter 5.

4-12. INTERRUPT CONTROL LOGIC

The iSBC 534 uses two Intel 8259 Programmable Interrupt Control chips. (PIC 0 and PIC 1 are shown on Figure 5-2 sheets 2 and 3, respectively.) Each chip has eight separate interrupt request inputs; the function of the chip is to resolve priorities among two or more simultaneous interrupt request inputs, and to deliver a single interrupt output in order of priority to the main processor. The interrupt output from each of the two chips is connected directly to the Multibus.

Each interrupt chip generates a single interrupt signal that goes to the interrupt buffer and jumper circuit. The buffer/jumper circuit connects the interrupt signal directly to the Multibus interrupt lines. Note that the transmit and receive ready signals of USART chips 0 and 1 also bypass PIC 0 and go directly to the interrupt buffer and jumper circuits. Thus, there are possible interrupts that can be jumpered to the Multibus. A default jumper ties the outputs of the two interrupt chips together to the INT1/ interrupt line. All other interrupt lines remain open.

In the iSBC 534, the preferred interrupt operation is the polled mode. The typical polling operation is summarized in the programming information in Chapter 3. The PIC chips can also be programmed for interrupt masks, and the status of the interrupt can be read by the main processor at any given time. Masking, status read, and control work programming are described in Chapter 3.

4-13. SERIAL I/O PORTS

The iSBC 534 has four completely independent serial I/O ports. (Serial I/O Ports 0 through 3 are shown in figure 5-2 sheets 4 through 7, respectively.) Each port provides either full or half-duplex communications with modems, data sets, or other serial devices. Each serial I/O port converts parallel format data into serial format for transmission; it also converts incoming serial data into a parallel format for use by the main processor. In addition, the serial I/O port deletes or inserts bits or characters that are functionally unique to the communication technique.

Each serial I/O port uses a single Intel 8251 programmable USART chip, which can support virtually any serial data technique currently in use, including IBM Bi-Sync. The programmable functions of the USART chip are described in Chapter 3.

In addition to the serial transmission and reception features of the serial I/O ports, each port has two additional circuit features:

a. A multiplexer circuit that is used for diagnostic testing. With the aid of the multiplexer in the loop-back circuit, it is possible to determine if the iSBC 534 has a malfunction.

b. The serial I/O ports also have input and output optical isolators that can be used for current loop transmission and reception.

4-14. LOOPBACK CIRCUITS

During normal transmit operation, the USART chip generates a DTR (data terminal ready) signal, an RTS (request to send) signal, plus the transmitted data (TXD). These signals are all available at the respective RTS, DTR, and TXD outputs for the serial I/O ports.

The loopback circuit is used during test mode. The test signal, which is received at the multiplexer and the test logic, does two things:

a. Disables the RTS and DTR output to the serial I/O port.

b. Drives the multiplexer so that the TXD, DTR, and RTS signals loop back to the inputs of the USART chip via the multiplexer. Thus, the data transmitted is returned to the data input (RXD); RTS is received at CTS, and DTR is received at DSR. The multiplexer also connects the transmit clock to the receive clock input so that TXC equals RXC.

In this manner, the USART chip can be programmed to transmit a test data word to itself. The data word can be received simultaneously, since the USART operates in full duplex mode. Thus, the data input can be compared with the data output, and the following control signals can be checked: RTS/CTS and DTR/DSR.

4-15. ISOLATED CURRENT LOOPS

Each USART port has the capability to operate with opto-isolated data transmit and data receive signals (TXD and RXD, respectively). See Chapter 2 for a discussion of the basic current loop circuits.

4-16. CLOCK JUMPER CONNECTIONS

The USART at each of the four ports requires two clock signals: RXC and TXC. Each USART chip has a jumper matrix with five clock input signals. (Refer to paragraph 2-14.) All ports are supplied with clock signals BDG4 and BDG5, the transmit and receive clocks. The only difference between Port 0 and the other ports is that the Port 0 jumper matrix receives clock signal BDG0, while Port 1 receives BDG1, etc. The default wiring connects BDG0 to both the transmit and receive clock inputs of the USART 0; similarly, default jumpers connect BDG1 to both clock inputs of USART 1, etc.

As noted previously, the multiplexer is controlled by the test signal; its function is to connect the same clock signal to both the transmit (TXC) and the receive (RXC) clock inputs on the USART to ensure a common clock signal. Otherwise, the transmit and receive clocks could be two different frequencies.

Note that the transmit clocks and the receive clock inputs are available from the modem via the serial I/O port connector. Similarly, the transmit clock rate is available at the data terminal transmit clock output (DTE TXC).

4-17. PARALLEL I/O PORT

The parallel I/O port is designed to support automatic calling units, such as the Bell Model 801, and certain other input signals that are not supported by serial I/O Ports 0 through 3. (Refer to figure 5-2 sheet 3.) The primary circuit in the parallel I/O port is an Intel 8255A Programmable Peripheral Interface (PPI) chip. This chip has three 8-bit ports (A, B and C), each of which is programmed to operate in the basic I/O mode.

Ports A and B are used as input ports, and port C is used as an output port. Port A supports either auxiliary inputs or an Automatic Calling Unit (ACU); Port B receives carrier detect (CD) and ring indicator (RI) signals. Note that the interrupts to PIC 1 from the parallel I/O port are the PND, RI, and CD signals.

Note that two of the Port C output signals (DPR and CRQ) go through a test disable circuit. This prevents the iSBC 534 from originating outgoing calls in the test mode.

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides a list of replaceable parts, service diagrams, and service and repair assistance instructions for the iSBC 534 Four Channel Communications Expansion Board.

5-2. REPLACEABLE PARTS

Table 5-1 provides a list of replaceable parts for the iSBC 534. Table 5-2 identifies and locates the manufacturers specified in the MFR CODE column in table 5-1. Intel parts that are available on the open market are listed in the MFR CODE column as "COML"; every effort should be made to procure these parts from a local (commercial) distributor.

5-3. SERVICE DIAGRAMS

The iSBC 534 parts location diagram and schematic diagram are provided in figures 5-1 and 5-2, respectively. On the schematic diagram, a signal mnemonic that ends with a slash (e.g., IOWC/) is active low. Conversely, a signal mnemonic without a slash (e.g., IOC) is active high.

5-4. SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance from Intel by contacting the MCSD Technical Support Center in Santa Clara, California at one of the following numbers:

Telephone:

From Alaska or Hawaii call—
(408) 987-8080

From locations within California call toll free—
(800) 672-3507

From all other U.S. locations call toll free—
(800) 538-8014

TWX: 910-338-0026
TELEX: 34-6372

Always contact the MCSD Technical Support Center before returning a product to Intel for service or repair. You will be given a "Repair Authorization Number", shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If the product is being returned because of damage sustained during shipment from Intel, or if the product is out of warranty, a purchase order is necessary in order for the MCSD Technical Support Center to initiate the repair.

In preparing the product for shipment to the MCSD Technical Support Center, use the original factory packaging material, if available. If the original packaging is not available, wrap the product in a cushioning material such as Air Cap TH-240 (or equivalent) manufactured by the Sealed Air Corporation, Hawthorne, N.J., and enclose in a heavy-duty corrugated shipping carton. Seal the carton securely, mark it "FRAGILE" to ensure careful handling, and ship it to the address specified by MCSD Technical Support Center personnel.

Customers outside of the United States should contact their sales source (Intel Sales Office or Authorized Intel Distributor) for directions on obtaining service or repair assistance.

Table 5-1. Replaceable Parts

REFERENCE DESIGNATION	DESCRIPTION	MFR. PART NO.	MFR. CODE	
A1,21,25,26,28,29,31,32,34	IC, 1489A Quad Line Driver	SN75189AN	TI	9
A2,10,17,50	IC, 74LS32 Quad 2-Input OR-Gate	SN74LS32N	TI	4
A3,4,9,13,16,20	IC, 1488A Quad Line Driver	SN75188AN	TI	6
A5	IC, 8224 Clock Generator	Intel 8224	COML	1
A6	IC, 7400 Quad 2-Input Pos. NAND-Gate	SN7400N	TI	1
A22	IC, 8255A Parallel I/O Interface	Intel 8255A	COML	1
A23,47	IC, 74109 Dual J-K Flip-Flop	SN74109N	TI	2
A24	IC, 74LS174 Hex/Quad D-Type Flip-Flop	SN74LS174N	TI	1
A27,30,33,35	IC, 74LS157 Data Selector/Multiplexer	SN74LS157N	TI	4
A36,37	IC, 8253 Programmable Interval Timer	Intel 8253	COML	2
A38	IC, 74S174 Hex/Quad D-Type Flip-Flop	SN74S174N	TI	1
A39,45	IC, 8259 Programmable Interrupt Ctrlr.	Intel 8259	COML	2
A40-43	IC, 8251 Serial I/O Interface	Intel 8251	COML	4
A44	IC, 74S74 Dual D-Type Flip-Flop	SN74S74N	TI	1
A46	IC, 7420 Dual Positive NAND-Gate	SN7420N	TI	1

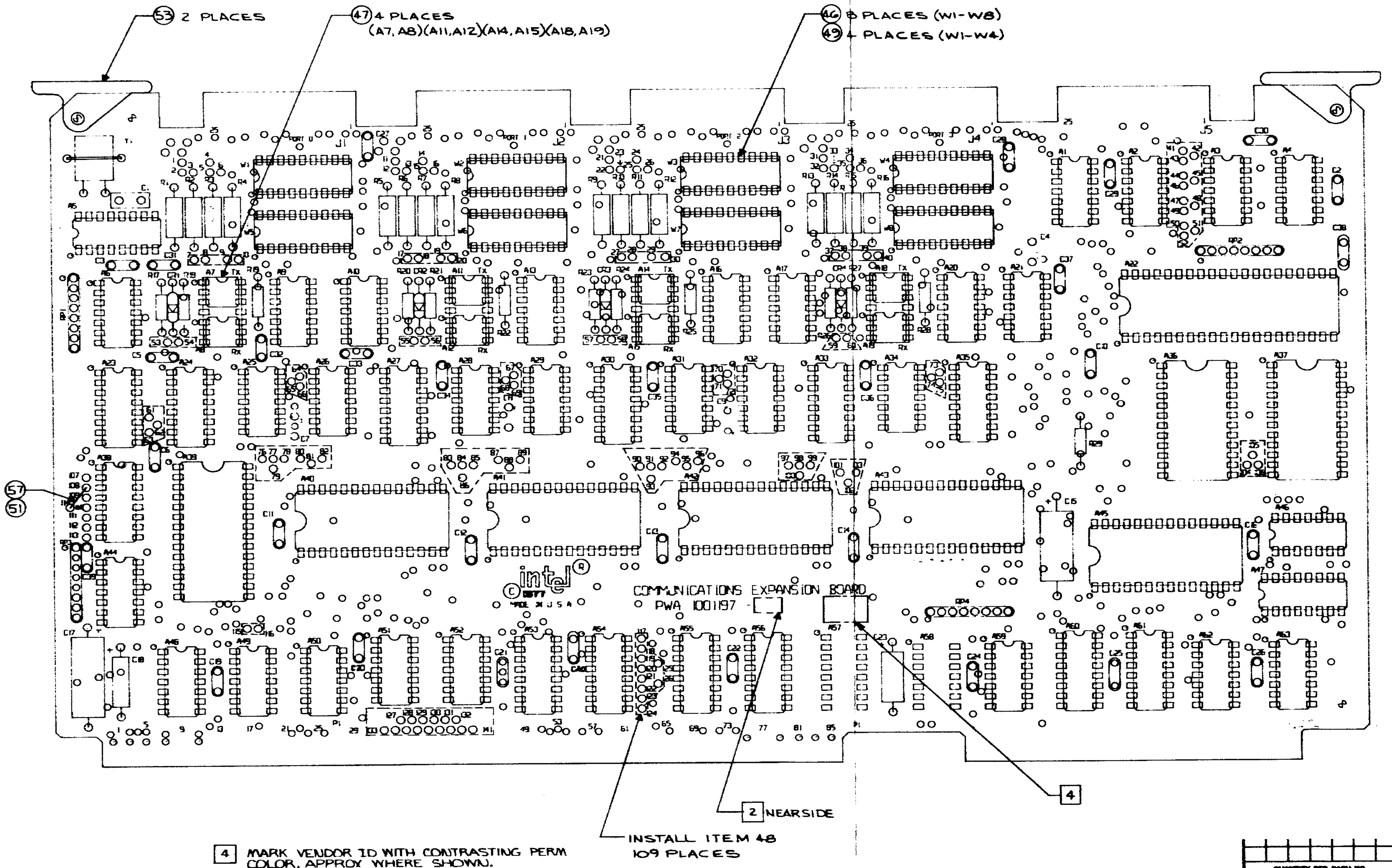
Table 5-1. Replaceable Parts (Continued)

REFERENCE DESIGNATION	DESCRIPTION	MFR. PART NO.	MFR. CODE	QTY
A48	IC, 74S00 Quad 2-Input Pos. NAND-Gate	SN74S00N	TI	1
A49	IC, 74S04 Hex Inverters	SN74S04N	TI	1
A51	IC, 74125 3-State Quad Bus Buffer Gate	SN74125N	TI	1
A52	IC, 7406 Hex Inverter Buffer/Driver	SN7406N	TI	1
A53	IC, 3404 High-Speed 6-Bit Latch	Intel 3404	COML	1
A54,60	IC, 8205 1-of-8 Binary Decoder	Intel 8205	COML	2
A55,56	IC, 8226 4-Bit Bidirectional Bus Driver	Intel 8226	COML	2
A59	IC, 74S02 Quad 2-Input Pos. NOR-Gate	SN74S02N	TI	1
A61	IC, 74S139 2-To-4 Decode/Demultiplex	SN74S139N	TI	1
A62	IC, 74S32 Quad 2-Input OR-Gate	SN74S32N	TI	1
A63	IC, 74LS04 Hex Inverters	SN74LS04	TI	1
CR1-4	Diode	1N914B	TI	4
C1	Capacitor, fxd, 10pF, ±5%, 500V	OBD	COML	31
C2,3,5,6,10-14,16,19-22, 24-40	Capacitor, fxd, 0.1μF, +80 −20%, 50V	OBD	COML	31
C15,17	Capacitor, fxd, 22μF, ±10%, 20V	OBD	COML	2
C18,23	Capacitor, fxd, 22μF, ±10%, 15V	OBD	COML	2
R1,4,5,8,9,12,13,16	Resistor, fxd, comp, 390 ohm, 5%, 1/2W	OBD	COML	8
R2,3,6,7,10,11,14,15	Resistor, fxd, comp, 560 ohm, 5%, 1/2W	OBD	COML	8
R17,20,23,26	Resistor, fxd, comp, 270 ohm, 5%, 1/4W	OBD	COML	4
R18,21,24,27	Resistor, fxd, comp, 560 ohm, 5%, 1/4W	OBD	COML	4
R19,22,25,28	Resistor, fxd, comp, 8.2K ohm, 5%, 1/4W	OBD	COML	4
R29	Resistor, fxd, comp, 430 ohm, 5%, 1/4W	OBD	COML	1
RP1-4	Resistor, pack, 8-pin, 10K	OBD	COML	4
W1-4	Jumpers, 18-Pin Interconnecting Posts	85931-6	AMP	4
XW1-8	Socket, DIP, 18-pin	C93-18-02	TI	8
Y1	Crystal, 22.1184 MHz fundamental	HW3	CTS	1
	Extractor, Card	S-203	SCA	2
	Socket, DIP, 14-pin	C93-14-02	TI	4
	Pins, Wire Wrap	OBD	COML	109

Table 5-2. List of Manufacturers' Codes

MFR. CODE	MANUFACTURER	ADDRESS	MFR. CODE	MANUFACTURER	ADDRESS
INTEL	Intel Corporation	Santa Clara, CA	AMP	AMP, Incorporated	Harrisburg, PA
TI	Texas Instruments	Dallas, TX	SCA	Scanbe, Incorporated	El Monte, CA
CTS	CTS Corporation	Elkhart, IN	COML	Any Commercial Source; Order by Description	

REVISIONS				
LTR	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGR
A	PRODUCTION RELEASE	4-25-77	5-9-77	
B	SEE ECO # 01018	8-15-77	8-15-77	8-17-77
C	SEE ECO #01648-2	11-2-78		
–	SEE ECO*2-3151	11-10-78		



4 MARK VENDOR ID WITH CONTRASTING PERM COLOR, APPROY WHERE SHOWN.

3. WORKMANSHIP PER MCSD QAW 007.

2 MARK DASH NO. AND REV LEVEL WITH CONTRASTING PERM COLOR, .12 HIGH, APPROX. WHERE SHOWN.

1. ASSEMBLY PART NO. IS 1001197-01. ASSY AND PL ARE TRACKING DOCUMENTS.

NOTES: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST

ITEM NO.	PART NUMBER	DESCRIPTION
PARTS LIST		
QUANTITY PER DASH NO.		

SCALE: 2:1	SIGNATURE	DATE	intel © INTEL 1977 3065 BOWERS AVE. SANTA CLARA CALIF. 95051
TOL. ± 2 PLC 3 PLC ANGLE	DRN BY D. MILLER	4-25-77	
	CHK BY	5-9-77	TITLE PRINTED WIRING ASSY. COMMUNICATIONS EXPANSION BOARD
MATERIAL:	DFT APPD		
	ENGR APPD		
FINISH:	AUTH BY	5-11-77	SIZE D DEPT MCSD DRAWING NO. P1001197 REV C
	CODE:	SHEET 1 OF 1	

4001407	SBC-534
NEXT ASSY	USED ON

©Intel Corporation 1977

98-253A

Figure 5-1. iSBC 534 Parts Location Diagram

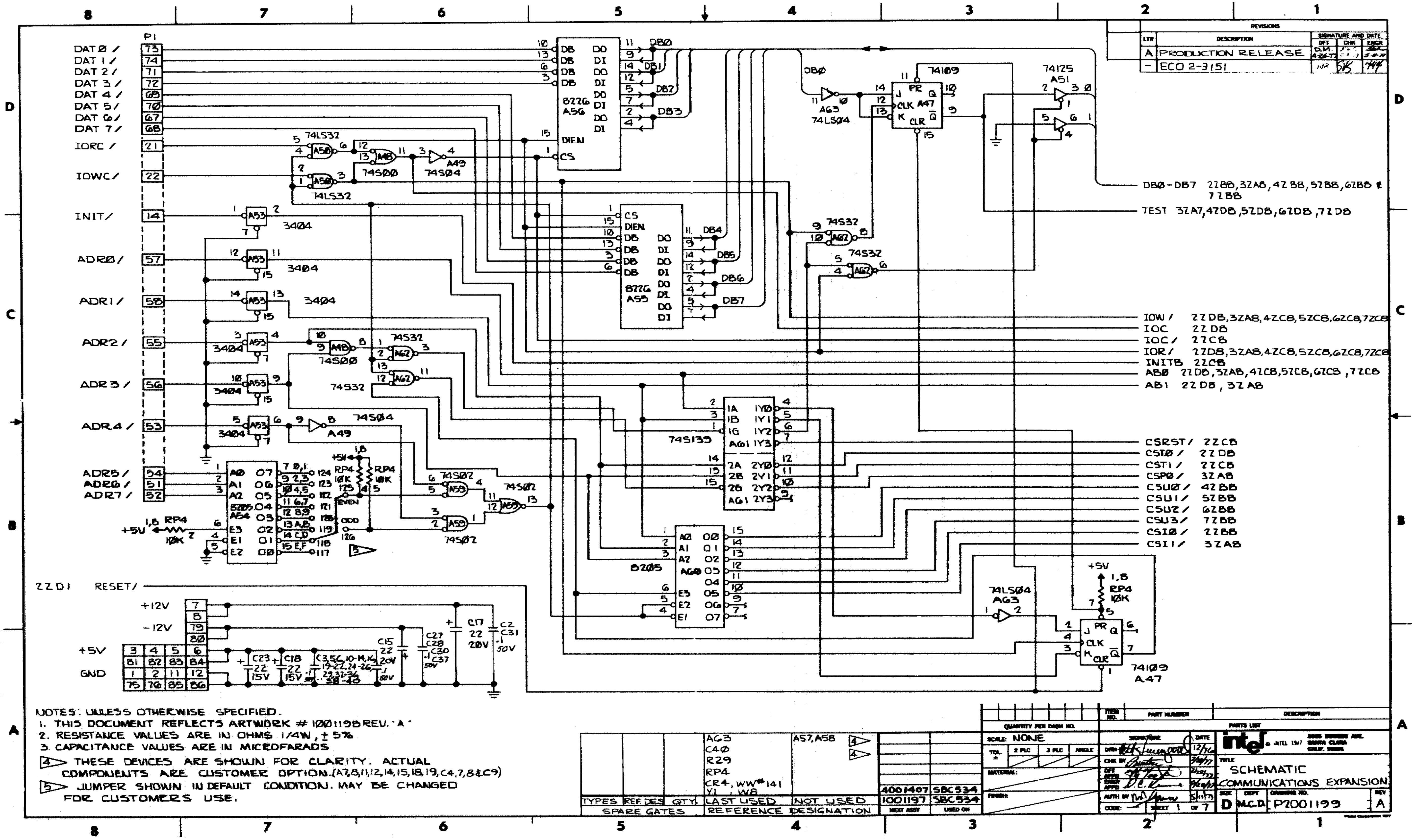


Figure 5-2. iSBC 534 Schematic Diagram (Sheet 1 of 7)

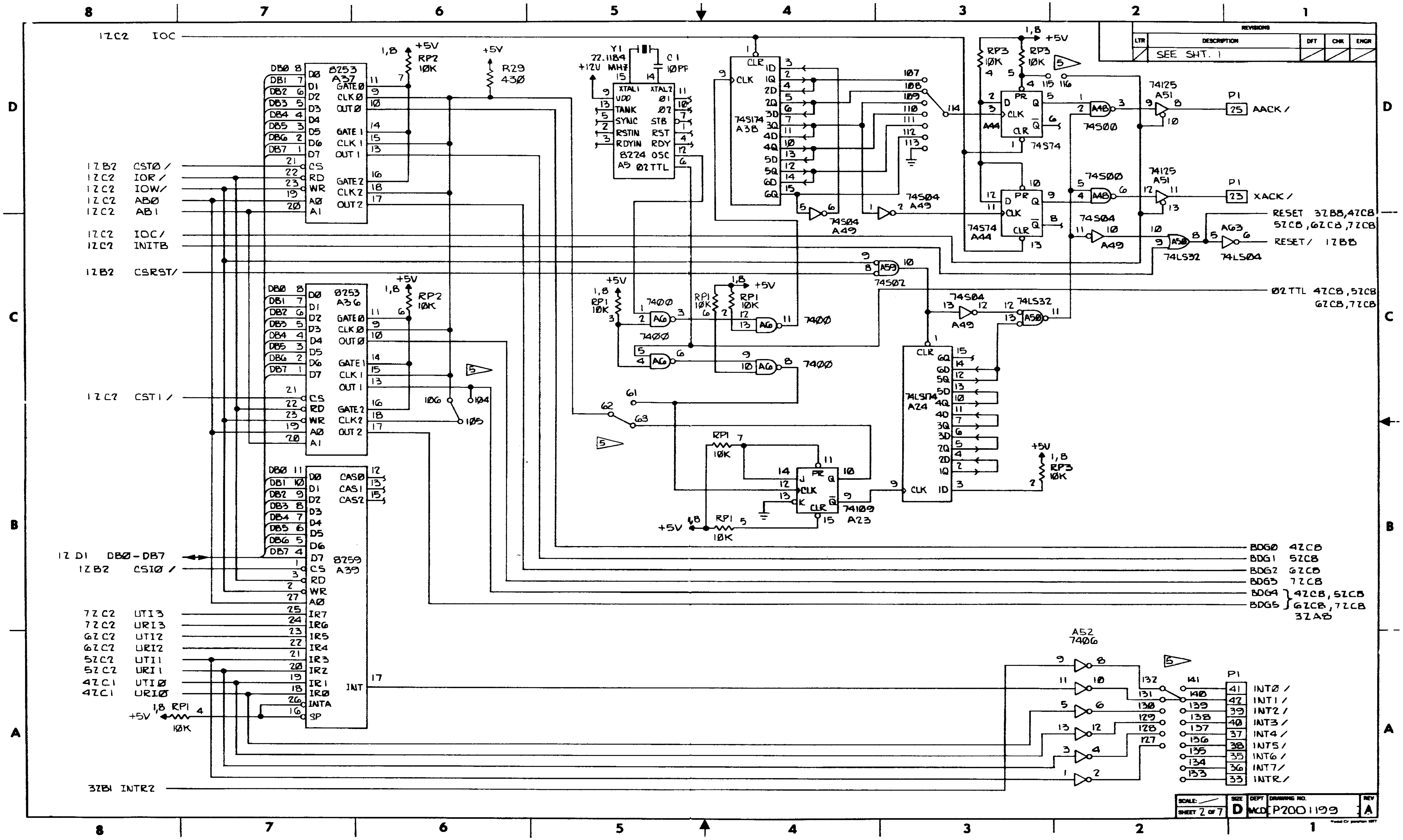


Figure 5-2. iSBC 534 Schematic Diagram (Sheet 2 of 7)

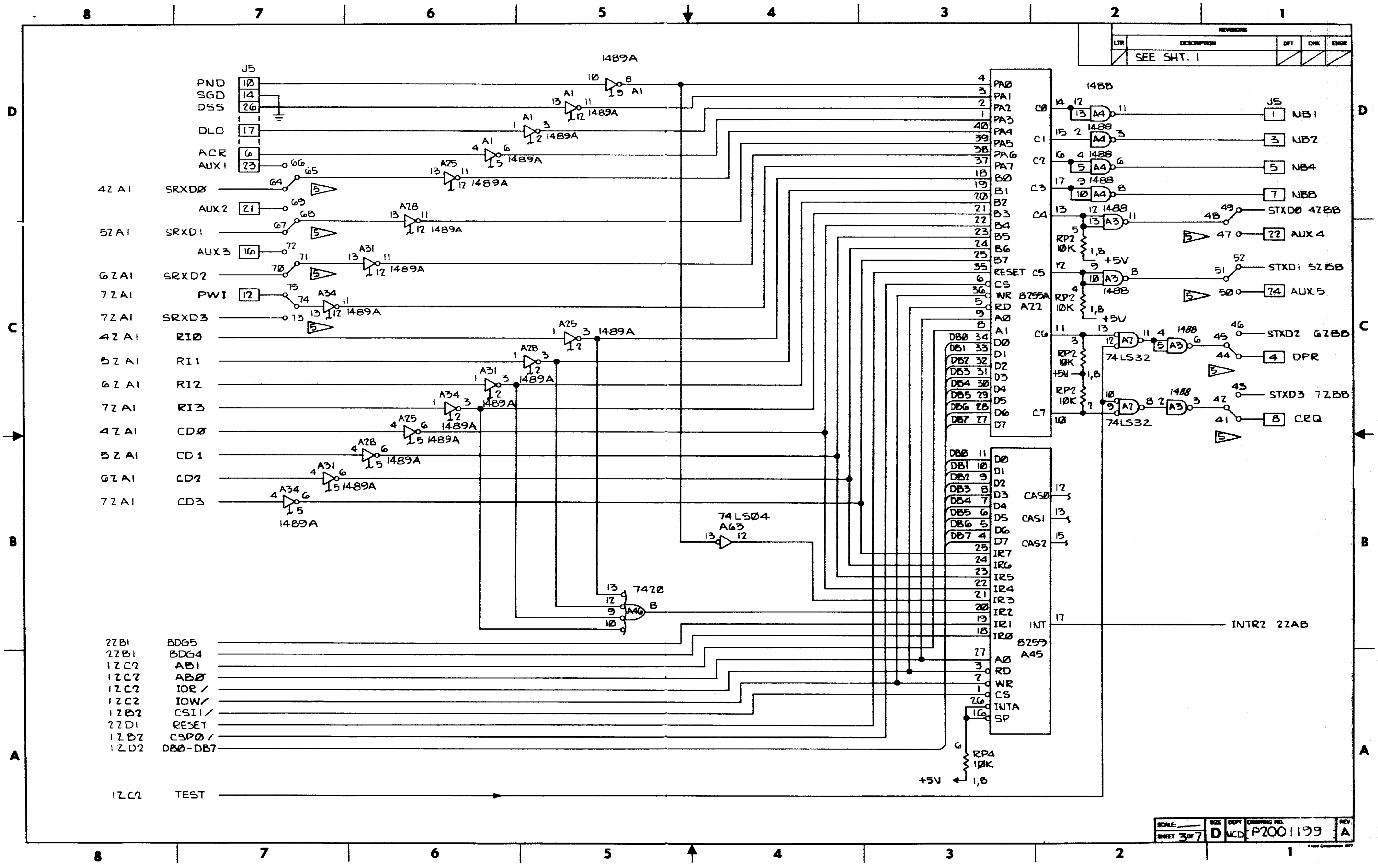


Figure 5-2. iSBC 534 Schematic Diagram (Sheet 3 of 7)

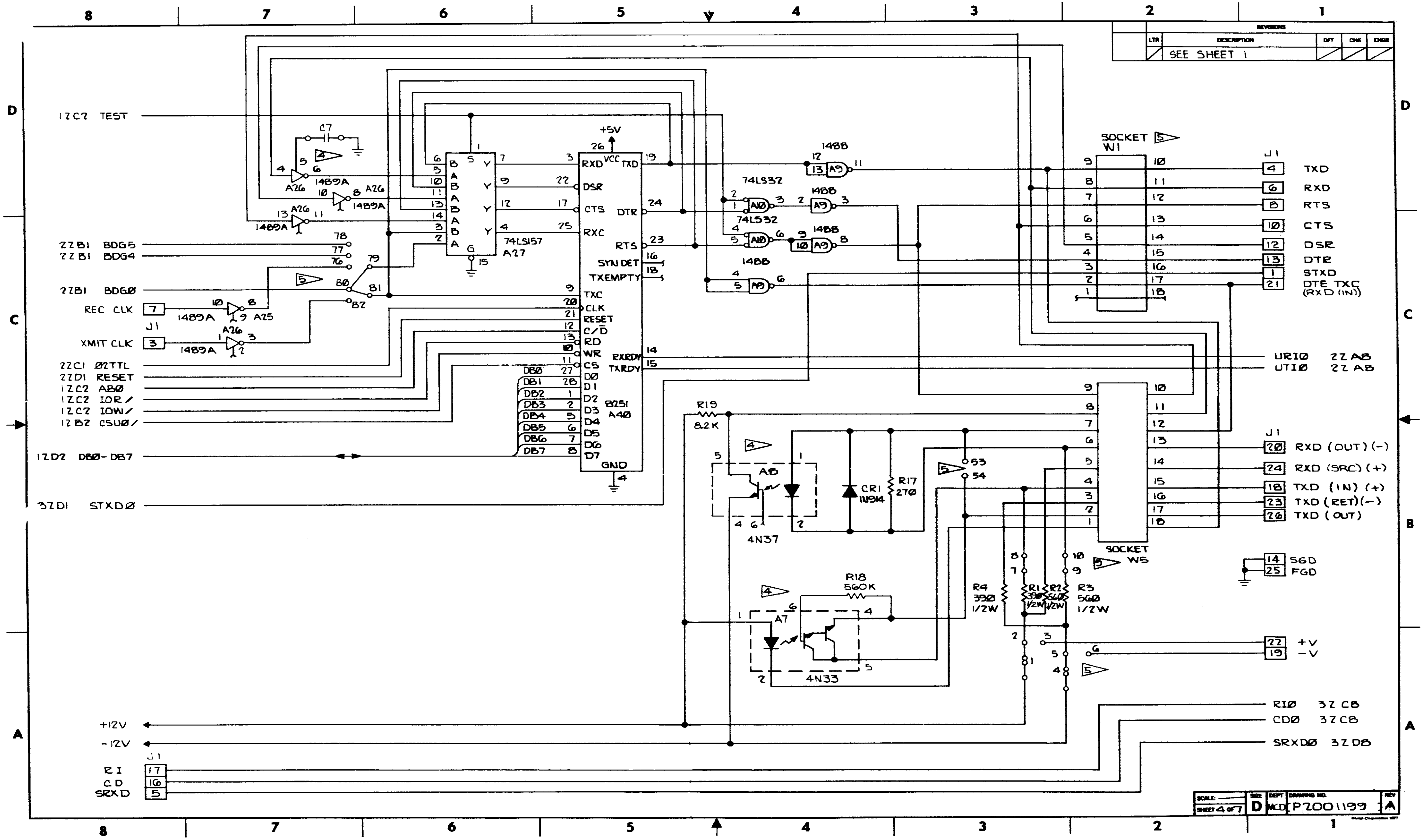


Figure 5-2. iSBC 534 Schematic Diagram (Sheet 4 of 7)

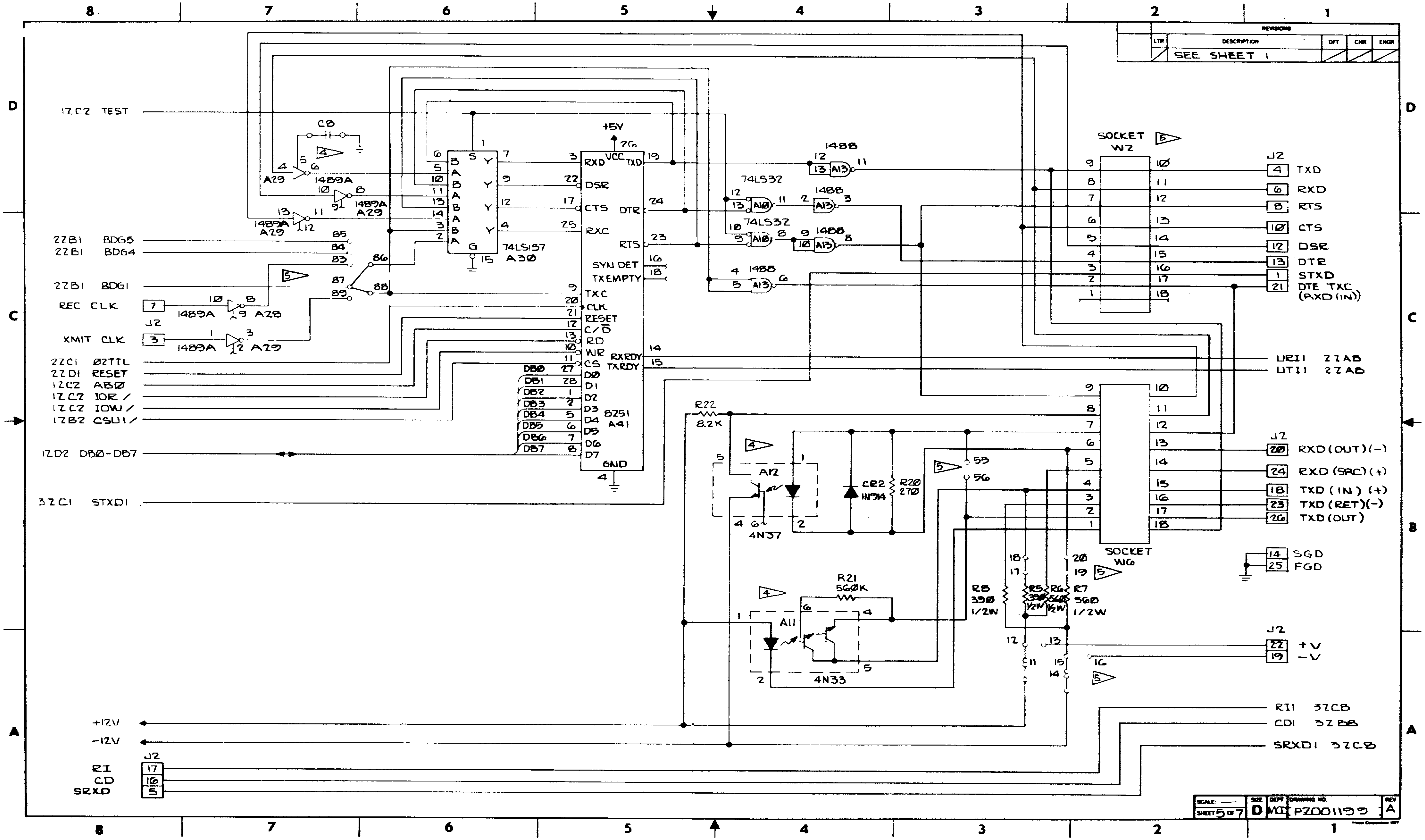


Figure 5-2. iSBC 534 Schematic Diagram (Sheet 5 of 7)

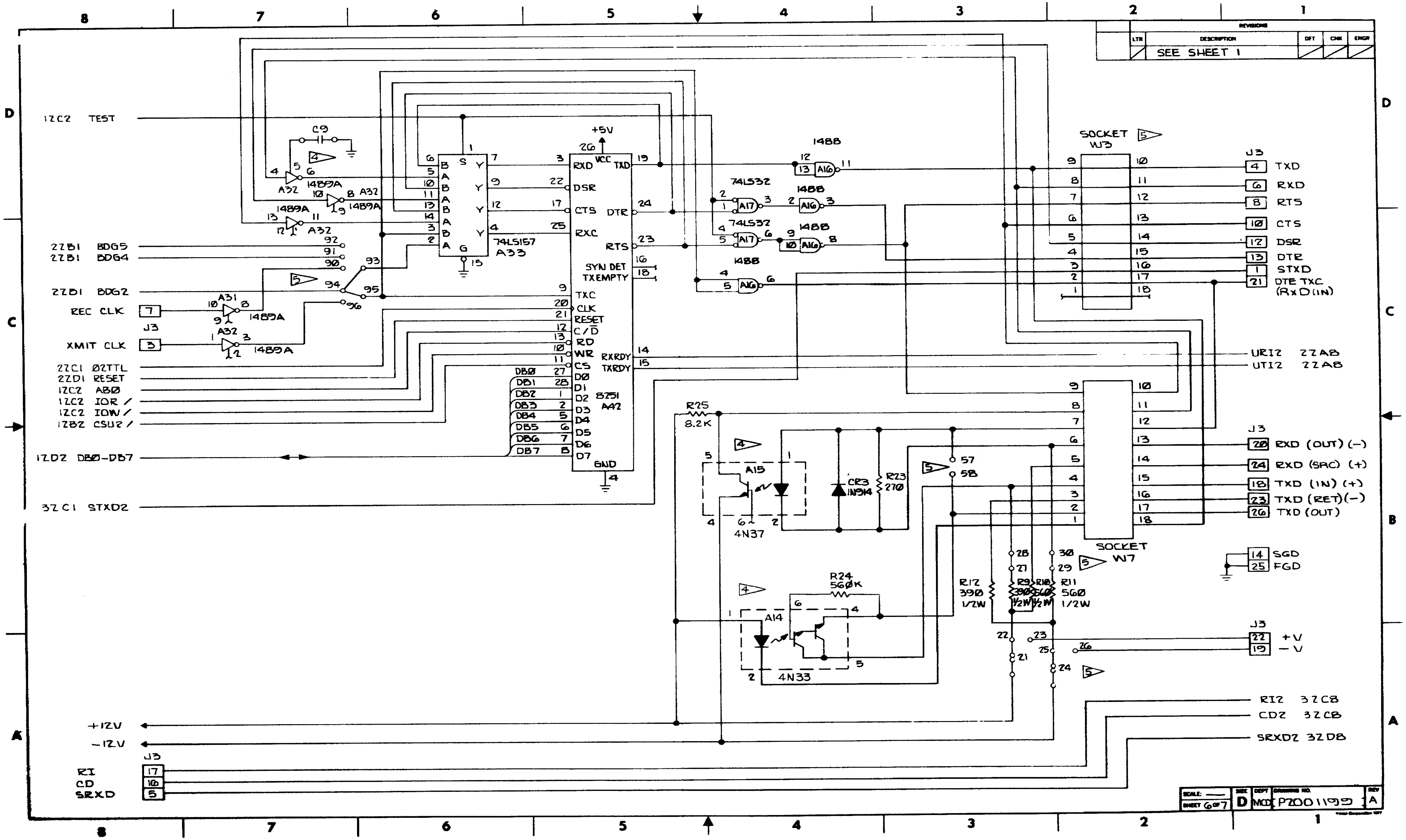


Figure 5-2. iSBC 534 Schematic Diagram (Sheet 6 of 7)

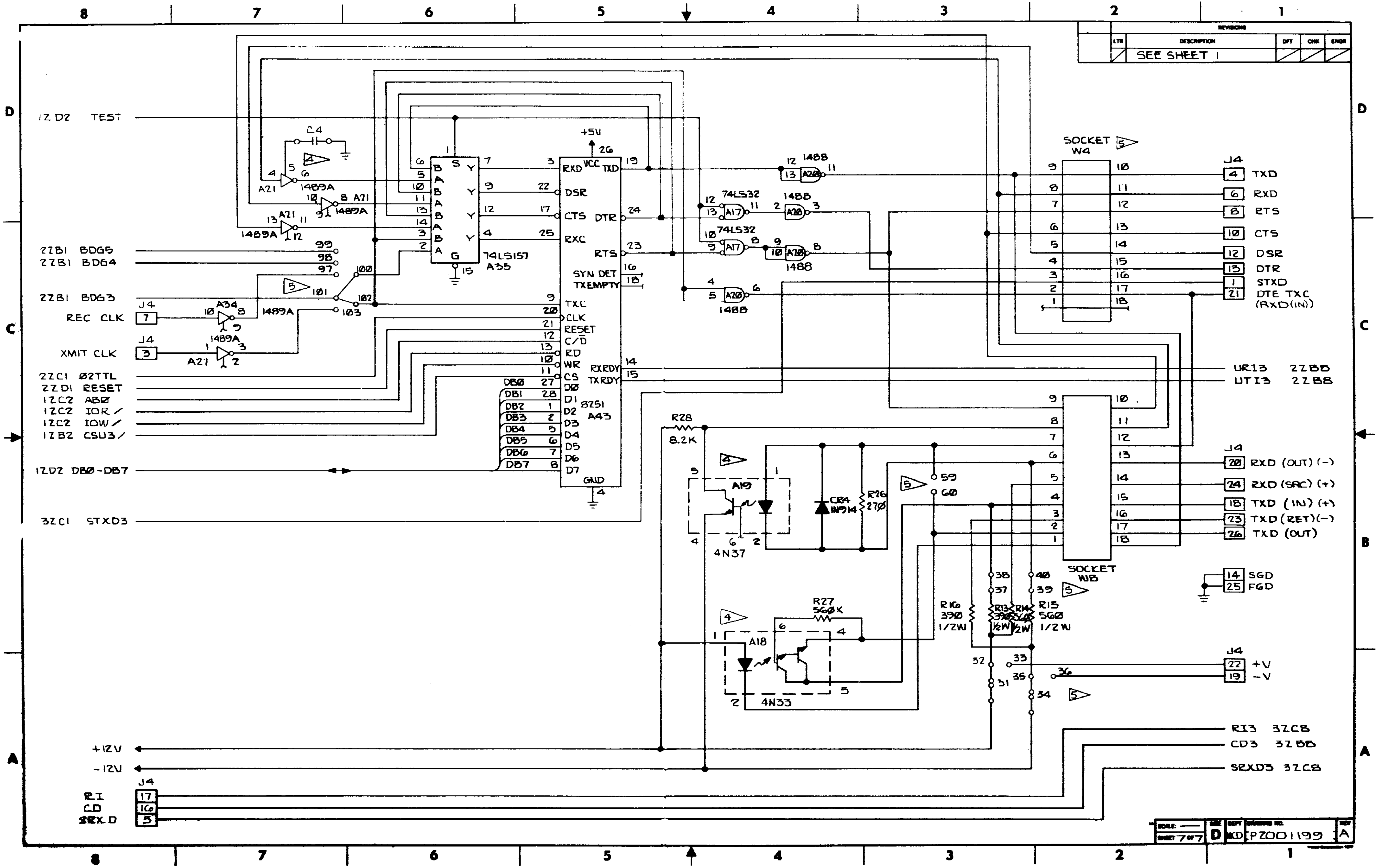


Figure 5-2. iSBC 534 Schematic Diagram (Sheet 7 of 7)

APPENDIX A
SAMPLE INTERRUPT SERVICE ROUTINE

A-1. INTRODUCTION

Appendix A contains a Sample Interrupt Service Routine (INTSR), which uses the following subroutines and tables:

POLL0, POLL1
INTBTL
LOOK2
EOI0, EOI1

POLL0 and POLL1 are polling subroutines for PIC 0 and PIC 1. (A typical polling subroutine for POLL0 is provided in paragraph 3-47.) INTBTL is a jump table that is defined in the routine description. LOOK 2 is an entry point in the LOOK jump table subroutine described in paragraph A-3. EOI1 and EOI2 are end-of-interrupt subroutines for PIC 0 and PIC 1. A sample subroutine for EOI0 is presented in table 3-24.

A-2. INTERRUPT SERVICE ROUTINE

INTSR is an interrupt master service routine that saves the processor status, POLLS the interrupt controllers, calls a selected routine, and then restores the processor status. The individual service routines are pointed to by a table referenced as 'INTBTL'. The first byte in 'INTBTL' must be 10H. The second byte must be 00H. Finally, sixteen 2-byte addresses must follow. The first address is for USART0 RXRDY, the last address is for USART3 carrier detect.

```
;USES-POLL0,POLL1,INTBTL,LOOK2,EOI0,EOI1; DESTROYS-NOTHING

        PUBLIC  INTSR
        EXTRN   POLL0,POLL1,INTBTL,LOOK2,EOI0,EOI1

INTSR:  PUSH    PSW           ;SAVE PROCESSOR STATE
        PUSH    B
        PUSH    D
        PUSH    H
        CALL    POLL0
        MOV     B,A
        ANI     80H           ;LOOK FOR ACTIVE INT IN USART CONTROLLER
        JZ      INT10
        MOV     A,B
        ANI     07H           ;KEEP ONLY INT NUMBER
        JMP     INT13
INT10:  CALL    POLL1
        MOV     B,A
        ANI     80H           ;LOOK FOR ACTIVE INTERRUPT IN AUX CONTROLLER
        JNZ     INT12         ;IF NEITHER, ERROR
        MVI     A,0FFH        ;FLAG IMPROPER INTERRUPT
        JMP     INT13
INT12:  MOV     A,B
        ANI     07H           ;SAVE LOWER 3 BITS
        ORI     08H           ;ADD IN BIT TO FLAG AUX CONTROLLER
INT13:  PUSH    PSW           ;SAVE INT NUMBER FOR EOI
        LXI     H,INTBTL      ;POINTER TO BRANCH TABLE
        CALL    LOOK2
        POP     PSW           ;GET INT NUMBER
        CPI     0FFH          ;SEE IF ERROR
        JZ      INT20
        ANI     08H           ;SEE IF INT WAS FROM USARTS OR AUX
        CNZ     EOI1
        CZ      EOI0          ;ISSUE END-OF-INTERRUPT
```

```
INT20:  POP     H               ;RESTORE STATE
        POP     D
        POP     B
        POP     PSW
        EI
        RET

        END
```

A-3. JUMP TABLE ROUTINE

LOOK is a branch table lookup routine. The table is pointed to by H&L. The first byte of the table must be the last allowed index+1. The second byte must be the first allowed index. An index out-of-range results in a direct return. The index is in register A. The individual routines are jumped to, thus they should be terminated with an 'RET'.

```
;USES-ECHO,A,H,L; DESTROYS-A,H,L,FLAGS

        PUBLIC  LOOK            ;START OF COMMAND LOOK-UP
        PUBLIC  LOOK1           ;SECONDARY ENTRY POINT
        PUBLIC  LOOK2
        PUBLIC  CTABLE          ;TABLE OF VALID COMMANDS

;THE FOLLOWING IS THE LIST OF ALL VARIABLES LISTED IN
;THIS MODULE WHICH MUST BE EXTERNALLY SATISFIED.

        EXTRN   CTABLE          ;DEFAULT TABLE POINTER
        EXTRN   ECHO            ;CONSOLE I/O SUBROUTINE
LOOK:   LXI     H,CTABLE        ;DEFAULT ADDRESS FOR TABLE
LOOK1:  CALL    ECHO            ;CRT IS INPUT DEVICE DEFAULT
LOOK2:  CMP     M               ;SEE IF IN TABLE
        RNC                     ;RETURN IF NOT IN TABLE
        INX     H               ;CHECK LOWER LIMIT
        CMP     M               ;SEE IF IN TABLE
        RC                      ;RETURN IF NOT IN TABLE
        SUB     M               ;SUBTRACT OFFSET INTO TABLE
        INX     H               ;POINT TO FIRST SUBROUTINE ADDRESS
        PUSH    B               ;SAVE B&C
        PUSH    D               ;SAVE D&E
        MOV     C,A             ;LOAD INDEX
        MVI     B,0             ;CLEAR B
        DAD     B               ;ADD INDEX TO BASE IN HL
        DAD     B
        MOV     E,M             ;LOAD LOW BYTE OF SUBROUTINE ADDRESS
        INX     H               ;POINT TO HIGH BYTE
        MOV     D,M             ;LOAD HIGH BYTE OF ADDRESS
        XCHG                    ;PUT ADDRESS INTO HL
        POP     D
        POP     B
        PCHL                    ;GO TO SUBROUTINE

        END
```

APPENDIX B
TELETYPEWRITER MODIFICATIONS

B-1. INTRODUCTION

This appendix provides information required to modify a Model ASR-33 Teletypewriter for use with certain Intel iSBC 80 computer systems.

B-2. INTERNAL MODIFICATIONS

WARNING

> Hazardous voltages are exposed when the top cover of the teletypewriter is removed. To prevent accidental shock, disconnect the teleprinter power cord before proceeding beyond this point.

Remove the top cover and modify the teletypewriter as follows:

a. Remove blue lead from 750-ohm tap on current source resistor, reconnect this lead to 1450-ohm tap. (Refer to figures B-1 and B-2.)

b. On terminal block, change two wires as follows to create an internal full-duplex loop (refer to figures B-1 and B-3):

   1. Remove brown/yellow lead from terminal 3; reconnect this lead to terminal 5.
   2. Remove white/blue lead from terminal 4; reconnect this lead to terminal 5.

c. On terminal block, remove violet lead from terminal 8; reconnect this lead to terminal 9. This changes the receiver current level from 60 mA to 20 mA.

A relay circuit card must be fabricated and connected to the paper tape reader drive circuit. The relay circuit card to be fabricated requires a relay, a diode, a thyractor, a small 'vector' board for mounting the components, and suitable hardware for mounting the assembled relay card.

A circuit diagram of the relay circuit card is included in figure B-4; this diagram also includes the part numbers of the relay, diode, and thyractor. (Note that a 470-ohm resistor and a 0.1 F capacitor may be substituted for the thyractor.) After the relay circuit card has been assembled, mount it in position as shown in figure B-5. Secure the card to the base plate using two self-tapping screws. Connect the relay circuit to the distributor trip magnet and mode switch as follows:

a. Refer to figure B-4 and connect a wire (Wire 'A') from relay circuit card to terminal L2 on mode switch. (See figure B-6.)

b. Disconnect brown wire shown in figure B-7 from plastic connector. Connect this brown wire to terminal L2 on mode switch. (Brown wire will have to be extended.)

c. Refer to figure B-4 and connect a wire (Wire 'B') from relay circuit board to terminal L1 on mode switch.

B-3. EXTERNAL CONNECTIONS

Connect a two-wire receive loop, a two-wire send loop, and a two-wire tape reader control loop to the external device as shown in figure B-4. The external connector pin numbers shown in figure B-4 are for interface with an RS232C device.

B-4. iSBC 530 TTY ADAPTER

The iSBC 530, which converts RS232C signal levels to an optically isolated 20 mA current loop interface, provides signal translation for transmitted data, received data, and a paper tape reader relay. The iSBC 530 interfaces an Intel iSBC 80 computer system to a teletypewriter as shown in figure B-8.

The iSBC 530 requires +12V at 98 mA and -12V at 98 mA. An auxiliary supply must be used if the iSBC 80 system does not supply this power. A schematic diagram of the iSBC 530 is supplied with the unit. The following auxiliary power connector (or equivalent) must be procured by the user:

Connector, Molex 09-50-7071
Pins, Molex 08-50-0106
Polarizing Key, Molex 15-04-0219

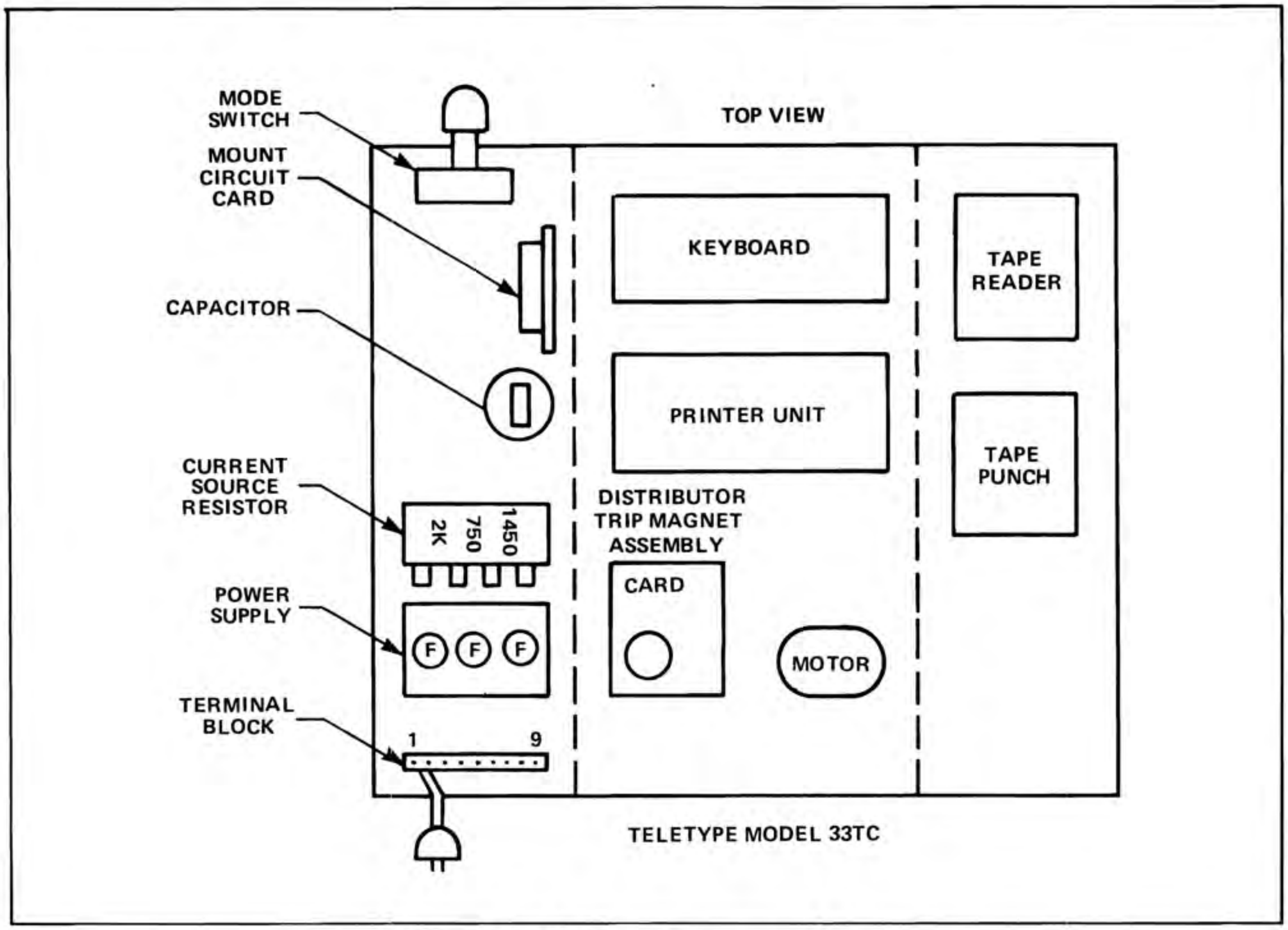


Figure B-1. Teletype Component Layout

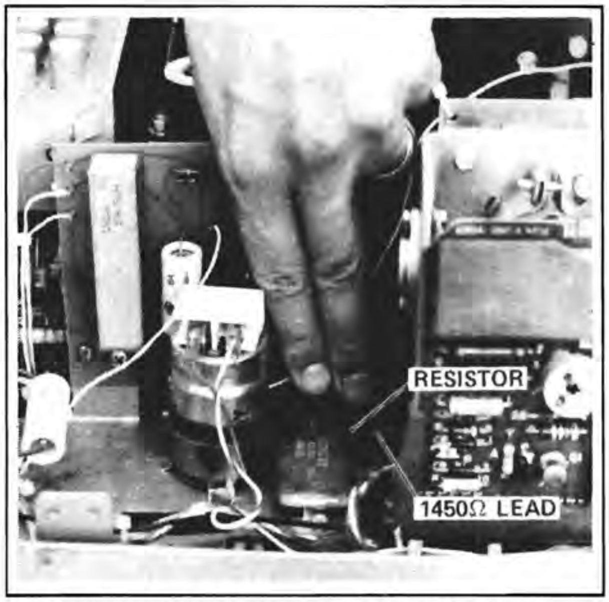


Figure B-2. Current Source Resistor

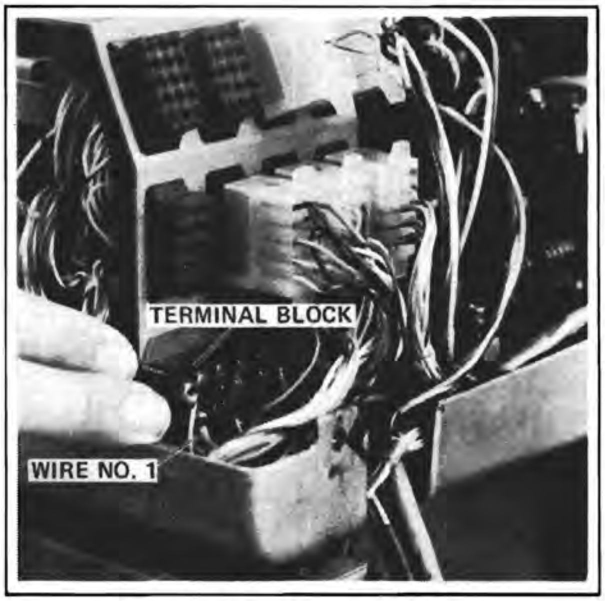


Figure B-3. Terminal Block

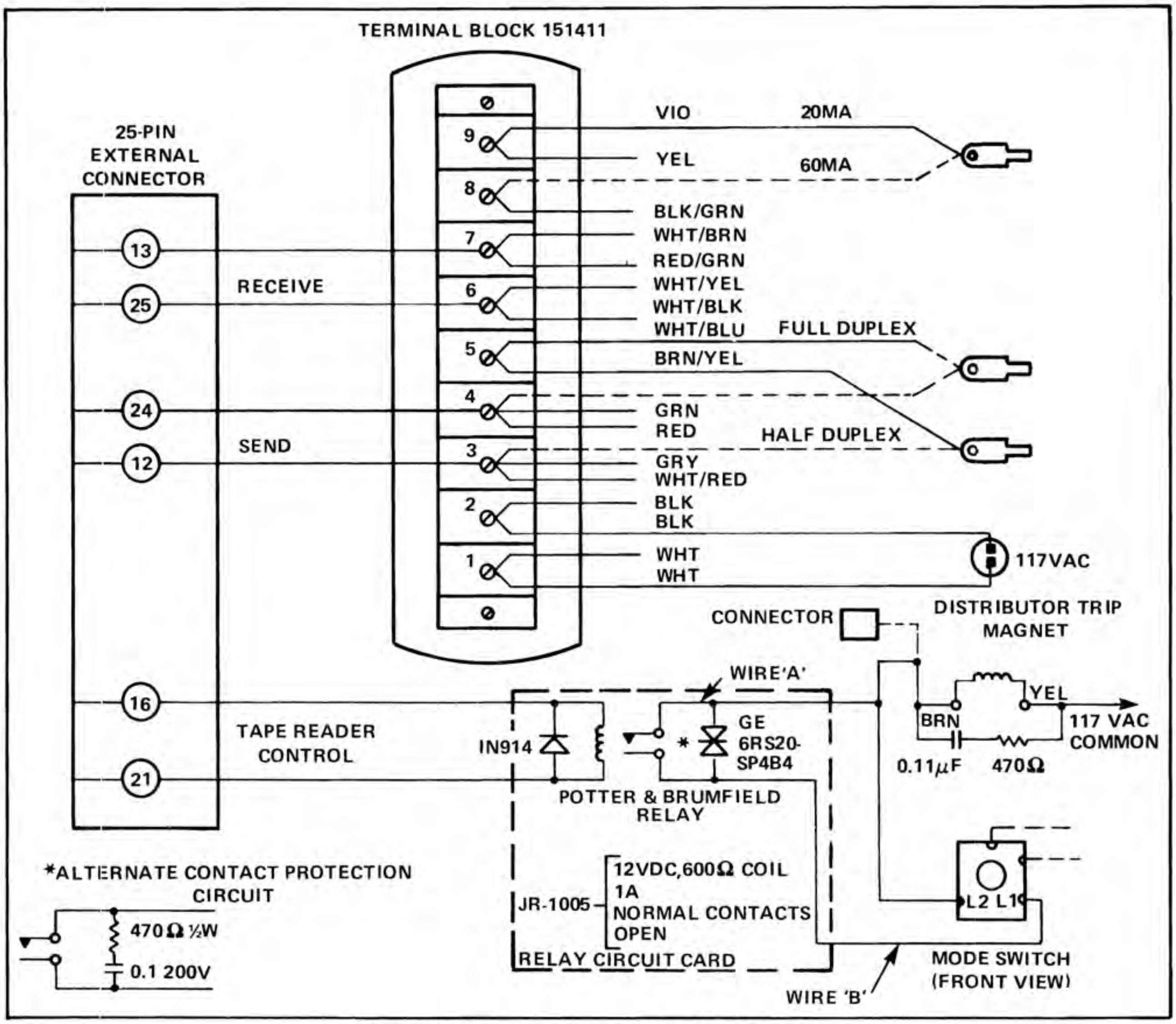


Figure B-4. Teletypewriter Modifications

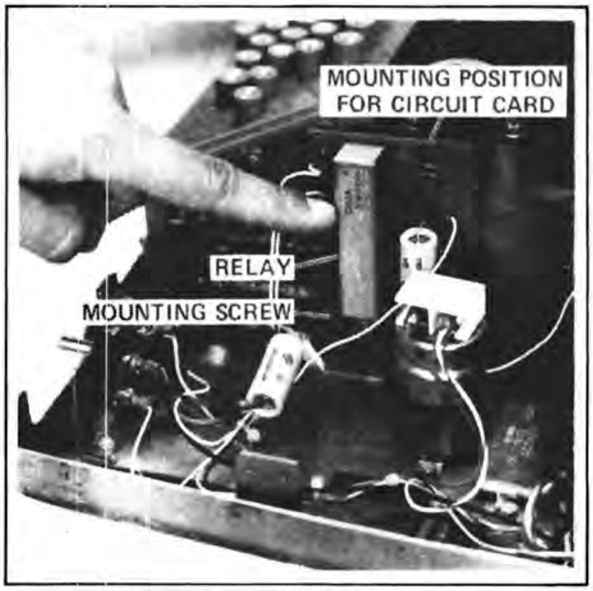


Figure B-5. Relay Circuit

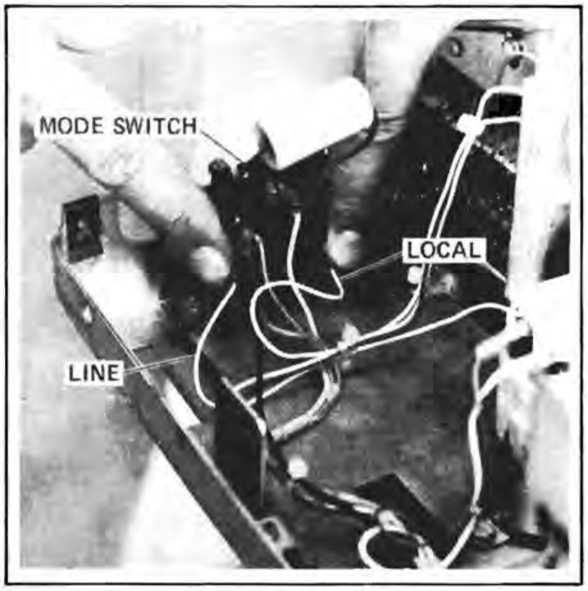


Figure B-6. Mode Switch

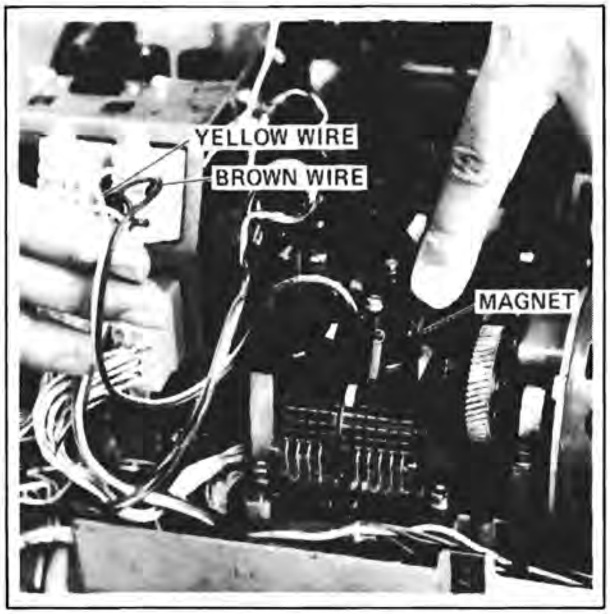


Figure B-7. Distributor Trip Magnet

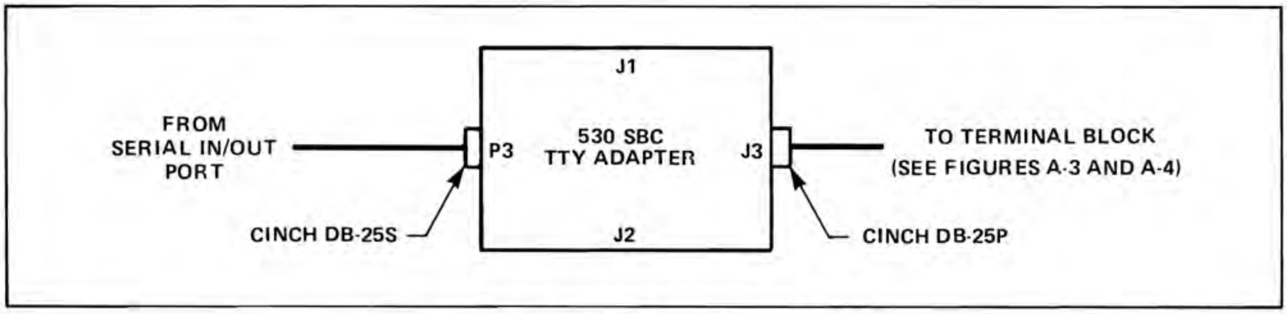


Figure B-8. TTY Adapter Cabling

iSBC 534 Four Channel Communications
Expansion Board Hardware Reference Manual
9800450-02

REQUEST FOR READER'S COMMENTS

Intel Corporation attempts to provide documents that meet the needs of all Intel product users. This form lets you participate directly in the documentation process.

Please restrict your comments to the usability, accuracy, readability, organization, and completeness of this document.

1. Please specify by page any errors you found in this manual.

2. Does the document cover the information you expected or required? Please make suggestions for improvement.

3. Is this the right type of document for your needs? Is it at the right level? What other types of documents are needed?

4. Did you have any difficulty understanding descriptions or wording? Where?

5. Please rate this document on a scale of 1 to 10 with 10 being the best rating. ______

NAME ______________________ DATE __________

TITLE ______________________

COMPANY NAME/DEPARTMENT ______________________

ADDRESS ______________________

CITY ______________ STATE ______ ZIP CODE ______

WE'D LIKE YOUR COMMENTS . . .

This document is one of a series describing Intel products. Your comments on the back of this form will help us produce better manuals. Each reply will be carefully reviewed by the responsible person. All comments and suggestions become the property of Intel Corporation.

Intel Corporation
Attn: Technical Publications
3065 Bowers Avenue
Santa Clara, CA 95051