SBC 80/20 AND SBC 80/20-4 SINGLE BOARD COMPUTERS HARDWARE REFERENCE MANUAL

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PREFACE

This manual provides general information, installation, programming information, principles of operation and service information for the Intel SBC 80/20 and 80/20-4 Single Board Computers. Unless specified otherwise references to the SBC 80/20 are valid for both systems. The areas where differences occur are identified as SBC 80/20 only or SBC 80/20-4 only. Additional systems information and Component Part details are available in the following documents:

- *Intel Microcomputer Systems Data Book*, 98-414
- *Intel 8080 Microcomputer Systems User's Manual*, 98-153

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CHAPTER 1

INTRODUCTION

The SBC 80/20 and SBC 80/20-4 are members of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer based solutions for OEM applications. The SBC 80/20 and SBC 80/20-4 are complete computer systems each on a single 6.75-by-12 inch printed circuit card. The CPU, system clock, read/write memory, non-volatile read-only-memory, I/O ports and drivers, serial communications interface, interval timer, interrupt controller, bus control logic and drivers all reside on the board.

Intel's powerful 8-bit n-channel MOS 8080A CPU, fabricated on a single LSI chip, is the central processor for both the SBC 80/20 and SBC 80/20-4. The 8080A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. The 8080A has a 16-bit program counter which allows direct addressing of up to 64K bytes of memory. An external stack, located within any portion of memory, may be used as a last in/first out stack to store and retrieve the contents of the program counter, flags, accumulator and all of the six general purpose registers. A sixteen bit stack pointer controls the addressing of this external stack. This stack provides almost unlimited subroutine nesting. Sixteen-line address and eight-line bi-directional data busses are used to facilitate easy interface to memory and I/O.

interface on the board in conjunction with the USART provides a direct interface to RS232C compatible devices and asynchronous and synchronous modems.

The RS232C, serial data lines and signal ground lines are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cables.

A programmable timing device, Intel's 8253 Interval Timer, is also included on the board. The 8253 can be programmed to generate accurate time delays. Instead of writing inefficient timing loops into the system software, the programmer can configure the 8253 to match his requirements, initialize one of the 8253 counters with the desired quantity, and command the 8253 to begin counting out the delay. The 8253 includes three counters that can be programmed to function independently in a variety of modes. In addition to providing an interrupt on terminal count (mode 0), an 8253 counter can be configured as a programmable one-shot (mode 1), a rate generator (mode 2) or a square-wave rate generator (mode 3). One of the counters is wired to provide the baud rate frequency to the Serial I/O Interface.

An interrupt may originate from any of 27 different sources: parallel I/O interface (4), serial I/O interface (3), interval timer (2), power fail logic (1) external modules (9) or external I/O (8). Any of the 27 interrupt lines can be jumpered to one of the eight priority level inputs to an Intel 8259 Interrupt Controller. The 8259 resolves priority among all eight levels according to an algorithm which is program-selected by the user. A variety of priority algorithms is available to the programmer so that the manner in which the interrupt requests are processed by the 8259 can be configured to match the system requirements. The priority assignments can be reconfigured dynamically at any time during the main program. The user can select any of the following modes:

- Fully nested
- Auto-rotating priority
- Specific priority
- Polled

The 8259 is programmed by the system software as an I/O peripheral.

Memory and I/O expansion may be achieved using standard Intel boards. Memory may be expanded to 65,536 bytes by adding user specified combinations of SBC-016 16K byte RAM board, SBC-406 6K byte PROM board, SBC-416 16K byte PROM board, and SBC 104/108 combination memory and I/O boards. Input/output capacity may be expanded in increments of 4 input ports and 4 output ports using SBC-508 Input/Output boards. Expandable backplanes and cardcages are available to support multi-board systems.

The development cycle of SBC 80/20 based OEM products may be significantly reduced using the Intellec Microcomputer Development System. The resident assembler, text editor, and system monitor greatly simplify the design, development, and debug of SBC 80/20 based system software. A unique In-Circuit Emulator (ICE-80) option provides the capability of executing and debugging OEM system software directly on the SBC 80/20.

Intel's high-level language, PL/M, can be used to significantly decrease the time required to develop OEM system software. PL/M is now available as a resident Intellec Microcomputer Development System option (PL/M-80).

CHAPTER 2

FUNCTIONAL/PROGRAMMING CHARACTERISTICS

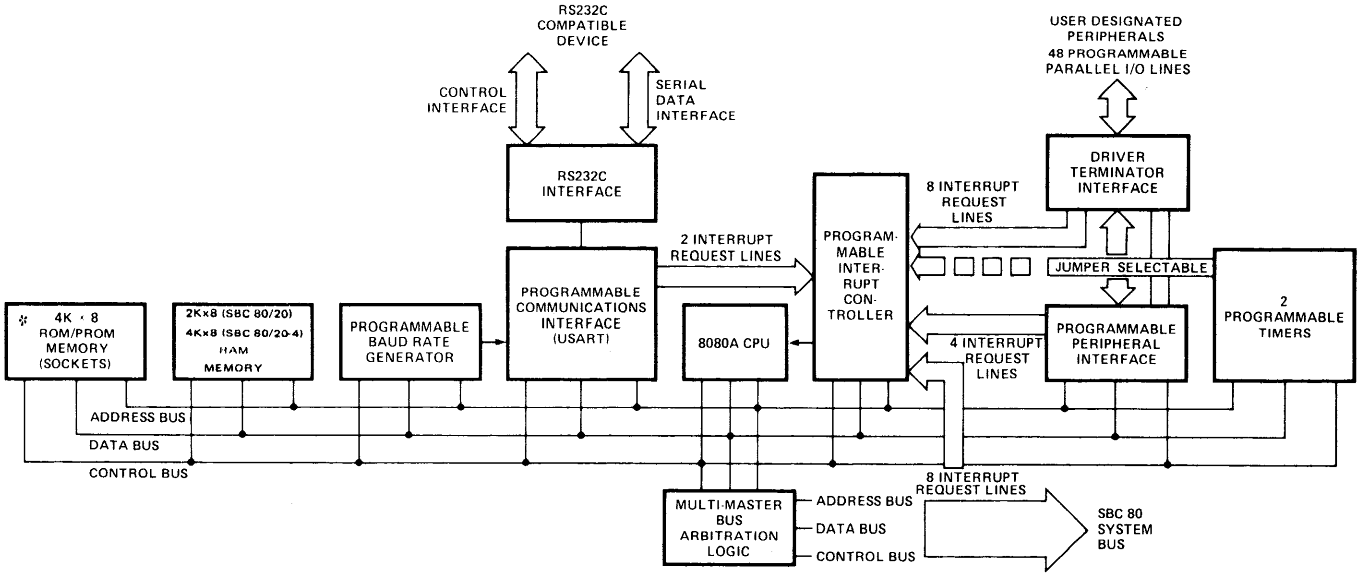
This chapter briefly describes the organization of the SBC 80/20's from two points of view. The principal functions performed by the hardware are identified and the general flow is illustrated in Section 2.1. This section is intended as an introduction to the detailed information provided in Chapter 3, Theory of Operations. Section 2.2 summarizes the information needed by the programmer to initialize and access the memory and I/O facilities on the SBC 80/20.

2.1 FUNCTIONAL DESCRIPTION

To facilitate the following description, the SBC 80/20 and SBC 80/20-4 can be divided into eight major functional blocks as shown in Figure 2-1:

1) CPU Set
2) Bus Interface (including Multi-Master Bus Control)
3) Random Access Memory (RAM)
4) Read Only Memory (ROM/PROM)
5) Serial I/O Interface
6) Parallel I/O Interface
7) Interval Timer
8) Interrupt Controller

The CPU Set consists of the 8080A Control Processor, the 8224 Clock Generator and the 8238 System Controller. The CPU Set is the heart of the SBC 80/20. It performs all system processing functions and provides a stable timing reference for all other circuitry



*8 X8 ROM/EPROM available using Intel's 2716 EPROM or Intel 8316B masked ROM on either board.

FIGURE 2-1. SBC 80/20 AND SBC 80/20-4 BLOCK DIAGRAM

in the system. The CPU generates all of the address and control signals necessary to access memory and I/O ports both on the SBC 80/20 and external to the SBC 80/20. The CPU Set is capable of fetching and executing any of the 8080's instructions. The CPU Set responds to interrupt requests originating both on and off the SBC 80/20, and to WAIT requests from memory or I/O devices having an access time which is slower than that required for the SBC 80/20's 8080A cycle time.

The Bus Interface allows the SBC 80/20 to use a common system bus with other master devices such as other CPU's or DMA devices, thus sharing common memory and I/O resources. The Bus Interface includes an Intel Bus Controller, as well as circuits for the generation of the Bus Clock (BLCK/) signal. The Bus Controller arbitrates all SBC 80/20 requests for use of the system bus, synchronously with respect to the Bus Clock. When the SBC 80/20 acquires control of the bus, the Bus Controller generates the appropriate memory or I/O command signal, gates the address onto the system address lines and gates data on/off the system bus. Operations between the CPU and onboard resources (i.e., RAM, PROM, I/O) require no use of the system Bus.

The Random Access Memory (RAM) section provides the user with 2048 (2K) X 8-bits (SBC 80/20) or 4096 (4K) X 8-bits (SBC 80/20-4) of read/write storage, using eight Intel 2113 (SBC 80/20) or 2114 (SBC 80/20-4) static RAM devices. The 2113 or 2114 RAM requires neither refreshing nor clock inputs to operate. All operations between the CPU and onboard RAM require no WAIT states.

The Read Only Memory (ROM/EPROM) section provides the user with the necessary provisions for installing 4096 X 8-bit or 8192 X 8-bits of ROM or EPROM. Each SBC 80/20 has four 24-pin sockets that can accept either

Intel 8708 Erasable and Electrically Programmable Read Only Memory (EPROM) chips (1024 X 8-bits each) or Intel 8308 Static MOS Read Only Memory (ROM) chips (also 1024 X 8-bits each). Each SBC 80/20 also includes the option of installing four 2048 X 8-bit Intel 2716 Erasable and Electronically Programmable Read Only Memory Chips. Both boards include the necessary acknowledgement and address decoding circuitry. All CPU accesses to this on-board ROM/EPROM area require no CPU WAIT states.

The Serial I/O Interface, using Intel's 8251 USART device, provides a full duplex RS232 serial data communications channel that can be programmed to operate with most of the current serial data transmission protocols. Synchronous or asynchronous mode, baud rate, character length, number of stop bits and the choice of even, odd or no parity are all program selectable.

The Parallel I/O Interface, using two Intel 8255 Programmable Peripheral interface devices, provides 48 signal lines for the transfer and control of data to or from peripheral devices. Sixteen lines already have a bi-directional driver and termination network permanently installed. This bi-directional network allows these sixteen lines to be inputs, outputs, or bi-directional (selected via jumpers). The remaining 32 lines, however, are uncommitted. Sockets are provided for the installation of drivers or termination networks as required to meet the specific needs of the user system.

The Interval Timer capability is implemented with an Intel 8253 Programmable Interval Timer. The 8253 includes three 16-bit BCD or binary counters which can be programmed by the user to perform a variety of timing functions. The outputs from the first two counters can be used as interrupt request lines, thus allowing easy implementation of such features as a real-time clock or a program monitor alarm. The output from the third counter is applied to the Serial I/O Interface. When properly programmed, this counter can provide the desired baud rate frequency for serial communications.

The SBC 80/20 also includes an Intel 8259 Interrupt Controller. The 8259 device resolves priority among eight different interrupt levels according to an algorithm that is programmed by the user. A jumper area in the interrupt section permits the user to connect any of nine external bus interrupt lines or 17 on-board interrupt requests to the eight priority level inputs to the 8259. Thus, by jumpering various interrupt lines to the appropriate priority levels and by programming the 8259 for the desired algorithm, the user can easily configure a custom interrupt structure.

2.2 PROGRAMMING SUMMARY

This section summarizes the SBC 80/20 memory and I/O addressing information that is necessary for a programmer to fully utilize the system's many features.

2.2.1 MEMORY ADDRESS ASSIGNMENT

The SBC 80/20 and 80/20-4 RAM can be assigned (via jumpers) to any one of the four 16K address boundaries within the total 64K address space supported by the 8080A. It will always reside at the end of the selected 16K block. Table 2-1 lists the blocks of address space that can be selected for the Random Access Memory (RAM).

Memory addresses for the ROM/EPROM on the SBC 80/20 always begin at memory location zero.

TABLE 2-1. RAM ADDRESS SPACE

JUMP CONNECTION	SELECTED RAM ADDRESS SPACE (hex)	
	2K (SBC 80/20)	4K (SBC 80/20-4)
120-121	3800-3FFF	3000-3FFF
119-121	7800-7FFF	7000-7FFF
118-121	B800-BFFF	B000-BFFF
117-121	F800-FFFF	F000-FFFF

2.2.2 DEDICATED I/O ADDRESSES

The SBC 80/20 includes a number of I/O devices that are accessed as dedicated I/O addresses. Table 2-2 summarizes the dedicated I/O port addresses, the I/O devices, the sections within the manual where each I/O device is described and the specific function which is accessed by an input or output instruction to a particular I/O address.

The Initialization Control Word (ICW1, ICW2 and ICW3) registers and the Operation Control Word (OCW1, OCW2 and OCW3) registers in the 8259 Interrupt Controller share several I/O addresses and are loaded in a particular sequence (indicated by various data bits in the control word). The 8259's Interrupt Requests Register (IRR) and In Service Register (ISR) also share an I/O address; the current contents of OCW3 dictate which can be read or whether the current interrupt level is read (See Section 3.10). Because this information could not be summarized within the format of Table 2-2, we have provided Table 2-3 as a summary of the 8259's basic operation.

TABLE 2-2. I/O PORT ADDRESSING

I/O PORT ADDRESS (hexadecimal)	I/O DEVICE (reference section)	INPUT FUNCTION	OUTPUT FUNCTION
D4	Power Fail (3.11)	Read Power Fail Status	Reset Power Fail latch.
D5	System Bus Override (3.2)	[1] Not used	Set or reset override control (using data bus line 0).
D6	LED Diagnostic Indicator (3.6)	[1] Not used	Flash LED for 1 millisecond
D7	[1] Not used	-	-
[2] D8 or DA [2] D9 or DB	8259 Interrupt Controller (3.10)	Various read functions (see Table 2-3)	Various write functions (see Table 2-3)
DC DD DE DF	8253 Interval Timer (3.9)	Read counter 0 Read counter 1 [3] Read counter 2 [1] Not used	Load counter 0 Load counter 1 [3] Load counter 2 Mode control
E4 E5 E6 E7	8255 #1 (3.8)	Read port A Read port B Read port C -	Write port A Write port B Write port C Control
E8 E9 EA EB	8255 #2 (3.8)	Read port A Read port B Read port C -	Write port A Write port B Write port C Control
[2] EC or EE [2] ED or EF	8251 USART (3.7)	Data in Read Status	Data out Control

[2] Either port address may be used.

[1] Though these port addresses are not used by the SBC 80/20, they are not available for use by external I/O devices.

[3] Baud Rate Generator Counter

TABLE 2-3. 8259 OPERATION SUMMARY

I/O PORT ADDRESS (hex)	DATA BITS		INPUT OPERATION
	D4	D3	
D8 or DA	-	-	Read IRR, ISR or current interrupt level (depending on contents of OCW3)
D9 or DB	-	-	Read Interrupt Mask Register (IMR)
			OUTPUT OPERATION
D8 or DA	0	0	Load OCW2
D8 or DA	0	1	Load OCW3
D8 or DA	1	X	Load ICW1
D9 or DB	X	X	Load OCW1, ICW2 or ICW3 (depending on sequence)

CHAPTER 3

THEORY OF OPERATION

In the preceding chapter we introduced and briefly defined each of the SBC 80/20 functional blocks. In this chapter we shall describe how each block performs its particular function(s). The text will constantly refer to the SBC 80/20 schematics, provided in Appendix A.

Note: Both active-high (positive true) and active-low (negative true) signals appear on the SBC 80/20 schematics. To eliminate any confusion when reading this chapter, the following convention will be adhered to: whenever a signal is active-low, its mnemonic is followed by a slash; for example, MRDC/ means that the level on that line will be low when the memory read command is true (active). If the signal is subsequently inverted, thus making it active-high, the slash is omitted; for example, MRDC means that the level on that line will be high when the memory read command is true.

3.1 THE CPU SET

The CPU Set consists of three Intel® integrated circuit devices:

- 8080A Central Processor Unit
- 8224 Clock Generator
- 8238 System Controller

and a 19.354 MHz crystal that establishes the frequency of oscillation for the 8224 device via a 10pF capacitor, as shown in Figure 3-1. Together, the elements in the CPU Set perform all central processing functions. The following paragraphs describe how the elements within the CPU Set interact with all other logic on the SBC 80/20. The interaction between IC's within the CPU Set, however, is not described. Instead, the reader is referred to the Intel® "8080 Microcomputer Systems User's Manual" for a detailed

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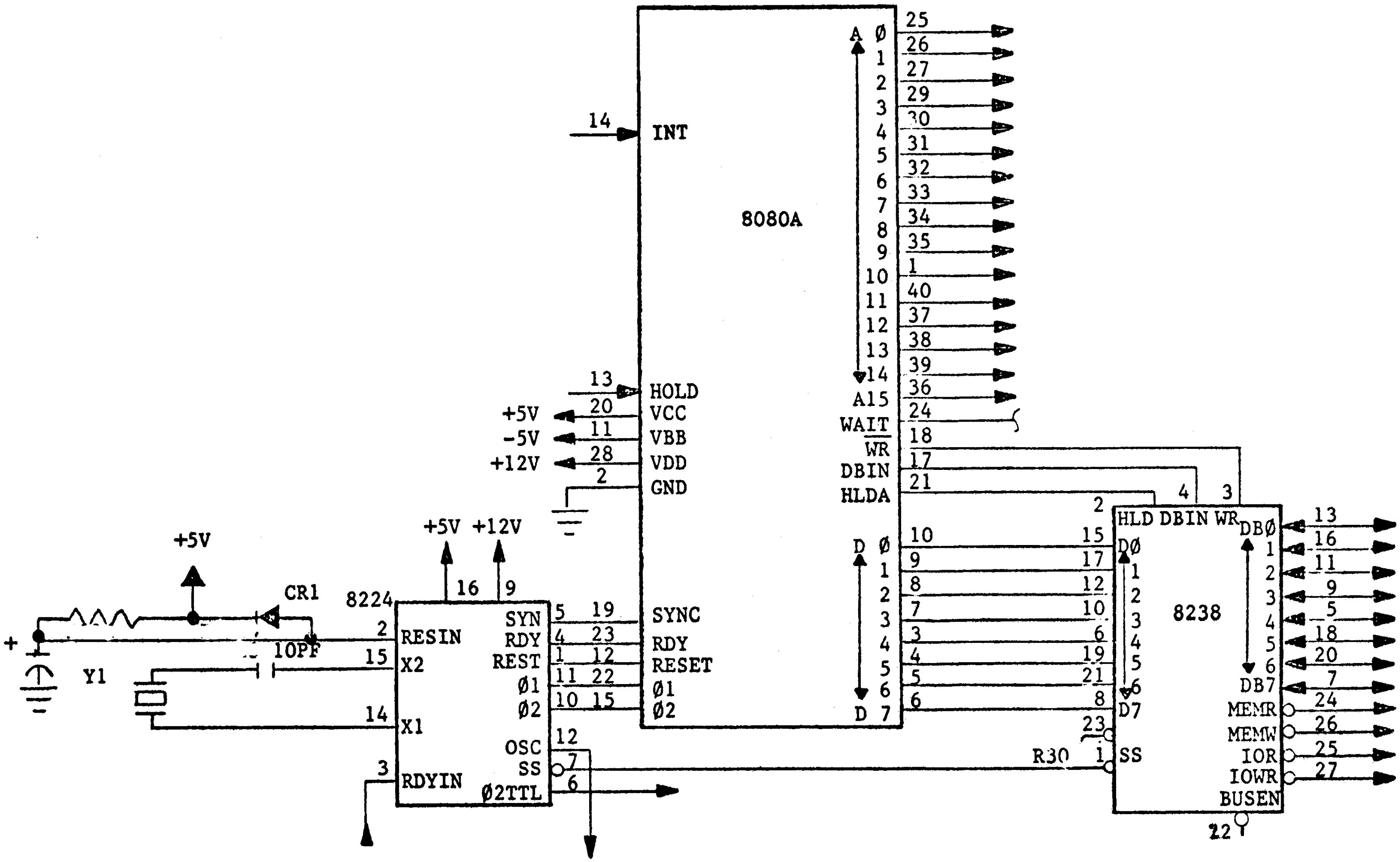


FIGURE 3-1. THE CPU SET

description of the 8080, 8224 and 8238 devices.

The CPU Set is shown on sheet 2 of the SBC 80/20 schematic (Appendix A).

3.1.1 INSTRUCTION TIMING

The activities of the CPU Set are cyclical. The CPU fetches an instruction, performs the operations required, fetches the next instruction, and so on. This orderly sequence of events requires precise timing. The 8224 Clock Generator, provides the primary timing reference for the CPU Set. The crystal in conjunction with a 10pF capacitor tunes an oscillator within the 8224 to precisely 19.354 MHz. The 8224 "divides" the oscillations by nine to produce two-phase timing inputs (Ø1 and Ø2) for the 8080. The Ø1 and Ø2 signals define a cycle of approximately 465 ns. duration. A TTL level phase 2 (Ø2T) signal is also derived and made available to external logic. All processing activities of the CPU Set are referred to the period of the Ø1 and Ø2 clock signals.

Within the 8080 CPU Set, an instruction cycle is defined as the time required to fetch and execute an instruction. During the fetch, a selected instruction (one, two or three bytes) is extracted from memory and deposited in the CPU's operating registers. During the execution part, the instruction is decoded and translated into specific processing activities.

Every instruction cycle consists of one, two, three, four or five machine cycles. A machine cycle is required each time the CPU accesses memory or an I/O port. The fetch portion of an instruction cycle requires one machine cycle for each byte to be fetched. The duration of the execution portion of the instruction cycle depends on the kind of instruction that has been fetched. Some instructions do not require any machine cycles other than those necessary to fetch the instruction; other instructions, however, require additional machine cycles to write or read data to/from memory or I/O devices.

Each machine cycle consists of three, four or five states. A state is the smallest unit of processing activity and is defined as the interval between two successive positive-going transitions of the Ø1 clock pulse.

There are three exceptions to the defined duration of a state. They are the WAIT state, the hold (HLDA) state and the halt (HLTA) state. Because the WAIT, the HLDA, and the HLTA states depend upon external events, they are by their nature of indeterminate length. Even these exceptional states, however, must be synchronized with the pulses of the driving clock. Thus the duration of all states, including these, are integral multiples of the clock pulse.

To summarize, then, each clock period marks a state; three to five states summarize a machine cycle; and one to five machine cycles comprise an instruction cycle. A full instruction cycle requires anywhere from four to seventeen states for its completion, depending on the kind of instruction involved.

There is just one consideration that determines how many machine cycles are required in any given instruction cycle: the number of times that the processor must reference a memory address or an I/O address, in order to fetch and execute the instruction. Like many processors, the 8080 is so constructed that it transmits one address per machine cycle. Thus, if the fetching and execution of an instruction requires two memory references, then the instruction cycle associated with that instruction consists of two machine cycles. If five such references are called for, then the instruction cycle contains five machine cycles.

Every instruction cycle has at least one reference to memory, during which the instruction is fetched. An instruction cycle must always have a fetch, even if the execution of instruction requires no further references to memory. The first machine cycle in every instruction cycle is therefore a FETCH. Beyond that, there are no fast rules. It depends on the kind of instruction. The input (INP) and the output (OUT), instructions each require three machine cycles: a FETCH, to obtain the instruction; a MEMORY READ, to obtain the address of the object peripheral; and an INPUT or an OUTPUT machine cycle, to complete the transfer.

Every machine cycle within an instruction cycle consists of three to five active states (referred to as T1, T2, T3, T4, and T5). The actual number of states depends upon the instruction being executed, and on the particular machine cycle within the greater instruction cycle. Figure 3-2 shows the timing relationships in a typical FETCH machine cycle. Events that occur in each state are referred to transitions of the Ø1 and Ø2 clock pulses.

At the beginning of each machine cycle (in state T1), the 8080 activates its SYNC output and issues status information on its data

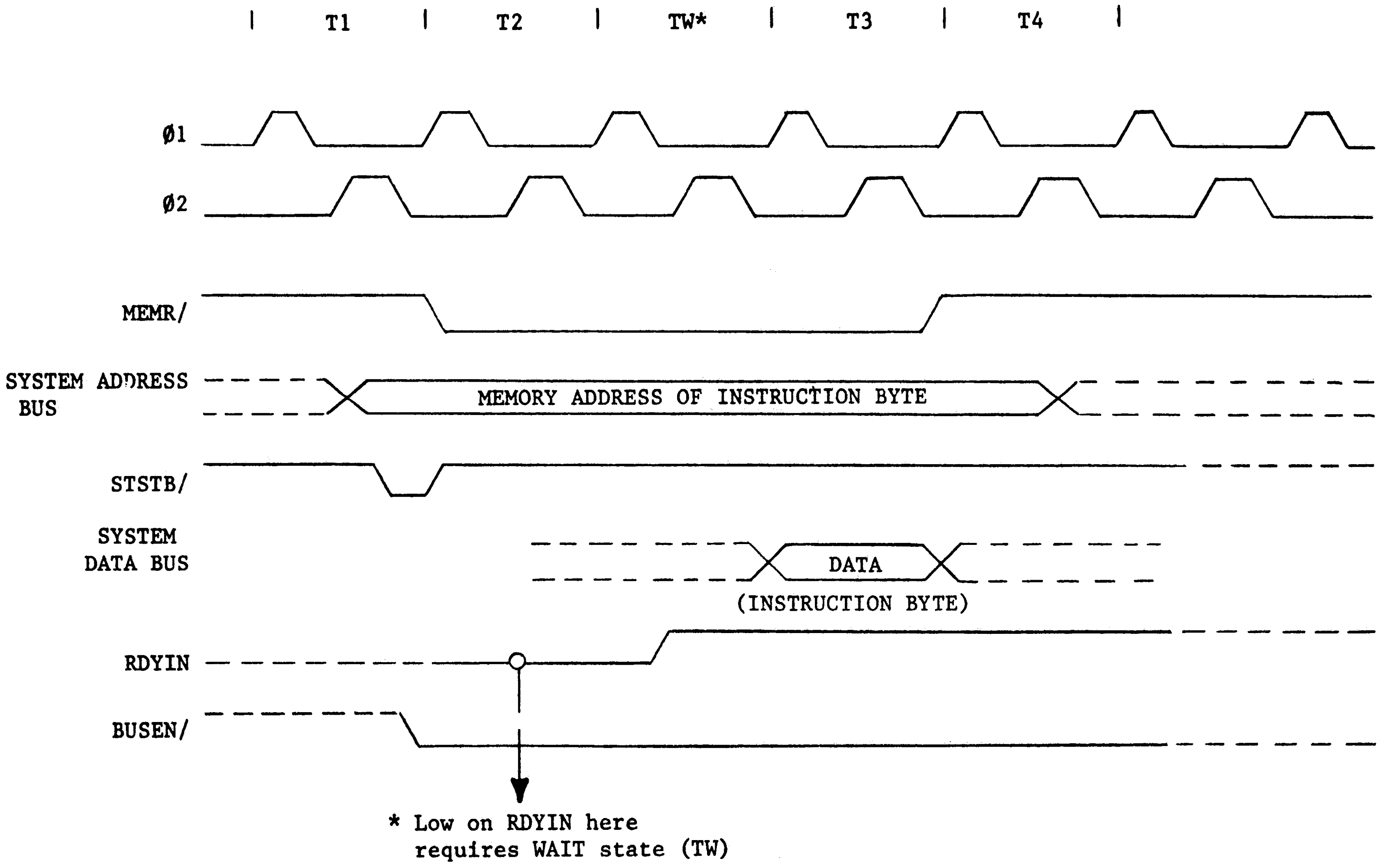


FIGURE 3-2. TYPICAL FETCH MACHINE CYCLE

bus. The 8224 accepts SYNC and generates an active-low status strobe (STSTB/) as soon as the status data is stable on the data bus. The status information indicates the type of machine cycle in progress. The 8238 System Controller accepts the status bits from the 8080 and STSTB/ from the 8224, and uses them to generate the appropriate control signals (MEMR/, MEMW/, IOR/ and IOW/) for the current machine cycle.

The rising edge of Ø2 during T1 loads the processor's address lines (ABO-ABF). These lines become stable within a brief delay of the Ø2 clocking pulse, and they remain stable until the first Ø2 pulse after state T3. This gives the processor ample time to read the data returned from memory.

Once the processor has sent an address to memory, there is an opportunity for the memory to request a WAIT. This it does by pulling the 8224's RDYIN line low. As long as the RDYIN line remains low, the CPU Set will idle, giving the memory time to respond to the addressed data request. The 8224 synchronizes RDYIN with internal processor timing and applies the result to the 8080's READY input. The processor responds to a wait request by entering an alternative state (TW) at the end of T2, rather than proceeding directly to the T3 state. A wait period may be of indefinite duration. The 8080 remains in the waiting condition until its READY line again goes high. The cycle may then proceed, beginning with the rising edge of the next Ø1 clock. A WAIT interval will therefore consist of an integral number of TW states and will always be a multiple of the clock period.

The events that take place during the T3 state are determined by the kind of machine cycle in progress. In a FETCH machine cycle, the CPU Set interprets the data on its data bus as an instruction. During a MEMORY READ, signals on the same bus are interpreted as a data word. The CPU Set itself outputs data on this bus during a MEMORY WRITE machine cycle. And during I/O operations, the CPU Set may either transmit or receive data, depending on whether an INPUT or an OUTPUT operation is involved. Consider the following two examples.

Figure 3-3 illustrates the timing that is characteristic of an input instruction cycle. During the first machine cycle (M1), the first byte of the two-byte IN instruction is fetched from memory. The 8080 places the 16-bit memory address on the system bus near the end of state T1. The 8238 activates the memory read control signal (MEMR/) during states T2 and T3 (and any intervening wait states, if required). During the next machine cycle (M2), the second byte of the instruction is fetched. During the third machine cycle (M3), the IN instruction is executed. The 8080 duplicates the 8-bit I/O address on address lines AB0-7 and AB8-F. The 8238 activates the I/O read control signal (IOR/) during states T2 and T3 of this cycle. The system bus enable input (BUSEN/) to the 8238 is always held low to allow for normal operation of the data bus buffers and the read/write control signals. If BUSEN/ goes high the data bus output buffers and control signal buffers are forced into a high-impedance state.

Figure 3-4 illustrates an instruction cycle during which the

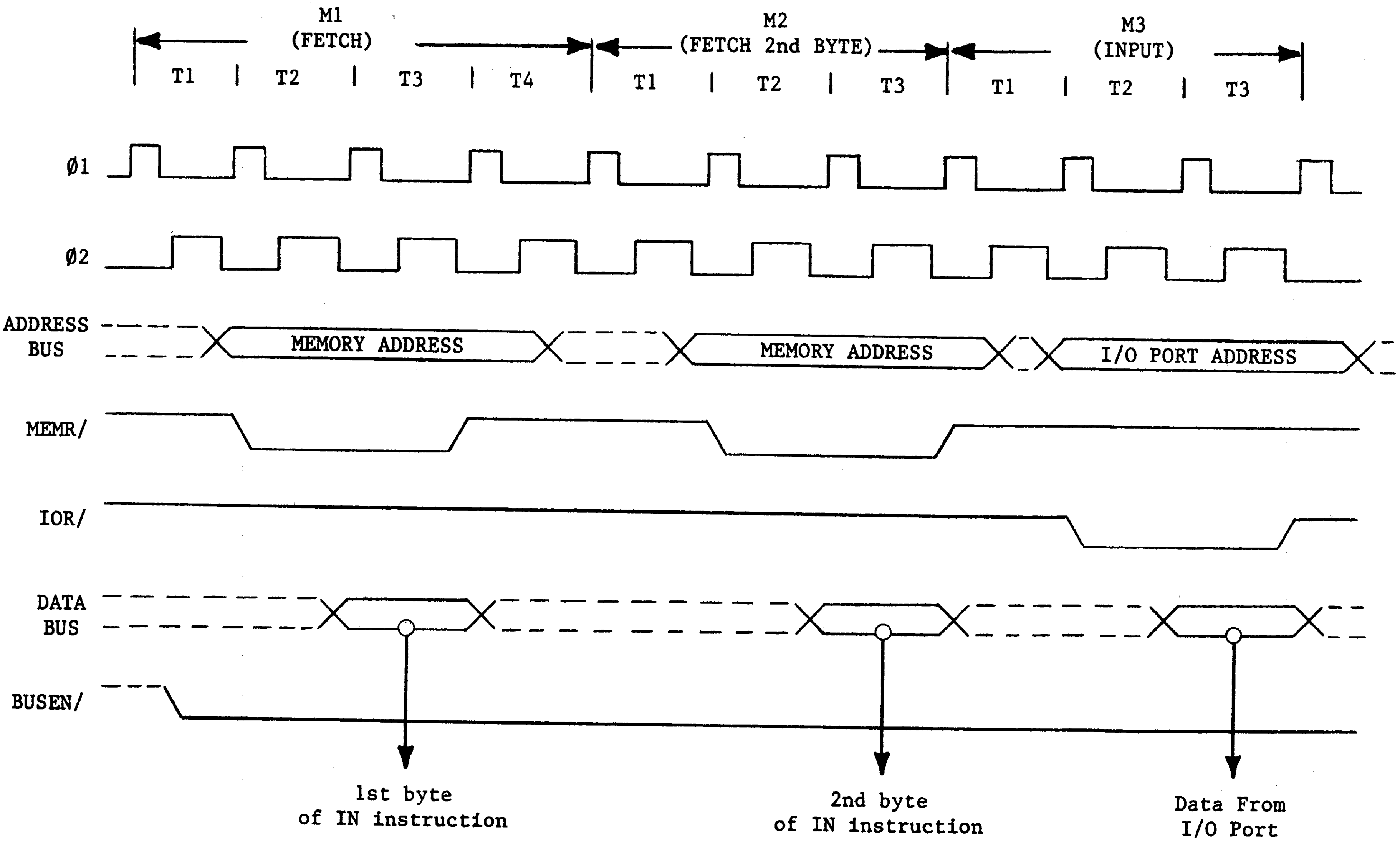


FIGURE 3-3. INPUT INSTRUCTION CYCLE

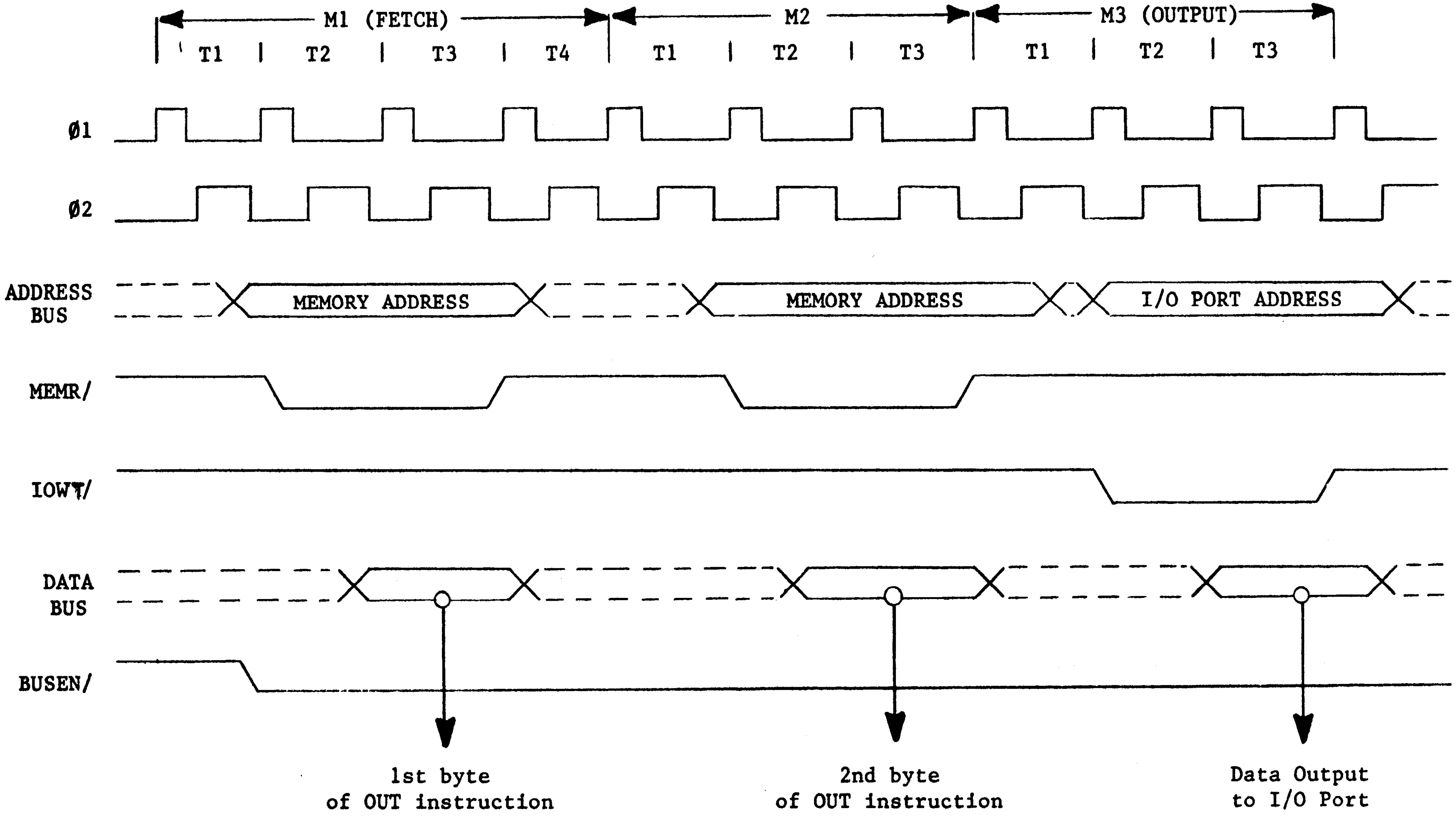


FIGURE 3-4. OUTPUT INSTRUCTION CYCLE

CPU Set outputs data. During the first two machine cycles (M1 and M2), the CPU Set fetches the two-byte OUT instruction. During the third machine cycle (M3), the OUT instruction is executed. The 8080 duplicates the 8-bit I/O address on lines AB0-7 and AB8-F. The 8238 activates the I/O write control signal (IOW/) at the beginning of state T2 of this cycle. The 8238 outputs the data onto the system bus at the end of state T2. Data on the bus remains stable throughout the remainder of the machine cycle.

Observe that a RDYIN signal is necessary for completion of an output machine cycle. Unless such an indication is present, the processor enters the TW state, following the T2 state. Data on the output lines remains stable in the interim, and the processing cycle will not proceed until the RDYIN line again goes high.

Note: The 8238 System Controller generates a write control signal (IOW/ or MEMW/) at the beginning of all write cycles. The IOW/ or MEMW/ signal occurs earlier than the 8080's WR/ output. IOW/ and MEMW/ are advanced write commands that can allow a ready indication to be returned to the CPU Set early enough to avoid an unnecessary wait state. The advanced write command (IOW/ or MEMW/) is subsequently synchronized with the 8080's WR/ output to produce a system write command (MWT/ or IOWT/) that causes the I/O or memory device to actually write the data, later in the cycle.

The negative-going leading edge of WR/ is referred to the rising edge of the first Ø1 clock pulse following T2. Thus, WR/ coincides with the appearance of stable data on the system bus. WR/ remains low until re-triggered by the leading edge of Ø2, during the state following T3. Note that any TW states intervening between T2 and T3 of the output machine cycle will necessarily extend WR/.

All processor machine cycles consist of at least three states: T1, T2, and T3 as just described. If the CPU Set has to wait for a RDYIN response, then the machine cycle may also contain one or more TW states. During the three basic states, data is transferred to or from the CPU Set.

After the T3 state, however, it becomes difficult to generalize. T4 and T5 states are available, if the execution of a particular instruction requires them. But not all machine cycles make use of these states. It depends upon the kind of instruction being executed, and on the particular machine cycle within the instruction cycle. The processor will terminate any machine cycle as soon as its processing activities are completed, rather than proceeding through the T4 and T5 states every time. Thus the 8080 may exit a machine cycle following the T3, the T4, or the T5 state and proceed directly to the T1 state of the next machine cycle.

3.1.2 INTERRUPT SEQUENCES

The 8080 has the built-in capacity to handle external interrupt requests. Peripheral logic can initiate an interrupt simply by driving the processor's interrupt (INT) line high. The interrupt (INT) input is asynchronous, and a request may therefore originate at any time during any instruction cycle. Internal logic re-clocks the external request, so that a proper correspondence with the driving clock is established. An interrupt request (INT) acts in coincidence with the ∅2 clock to set the internal interrupt latch. This event takes place during the last state of the instruction cycle in which the request occurs, thus ensuring that any instruction in progress is completed before the interrupt can be processed.

The INTERRUPT machine cycle which follows the arrival of an enabled interrupt request resembles an ordinary FETCH machine cycle in most respects. The contents of the program counter are latched onto the address lines during T1, but the counter itself is not incremented during the INTERRUPT machine cycle, as it otherwise would be. In this way, the pre-interrupt status of the program counter is preserved, so that data in the counter may be saved in the stack. This in turn permits an orderly return to the interrupted program after the interrupt request has been processed.

The 8238's INTA/ output (to connector pin P2-40) is normally used to gate an "interrupt instruction" onto the system data bus during state T3. The interrupt instruction is usually a one-byte RST but on the SBC 80/20 it is a three-byte CALL instruction which causes program control to branch to an interrupt routine. When the CALL interrupt instruction is supplied by the 8259 Interrupt controller, the 8238 generates an INTA/ pulse for each of the three bytes. INTA/ also acknowledges the arrival of the interrupt instruction at the RDYIN input on the 8224.

3.1.3 HALT SEQUENCES

When a halt instruction (HLT) is executed, the 8080 enters the halt state after state T2 of the next machine cycle. There are two ways in which the 8080 can exit the halt state:

- A high on the 8224 reset input (RESIN/) will always reset the 8080 to state T1; reset also clears the program counter.
- An interrupt (i.e., INT goes high while INTE is enabled) will cause the 8080 to exit the halt state and enter state T1 on the rising edge of the next Ø1 clock pulse.

  Note: The interrupt enable (INTE) flag must be set when the halt state is entered; otherswise, the 8080 will only be able to exit via a reset signal.

3.1.4 START-UP SEQUENCE

When power is applied initially to the 8080, the processor begins operating immediately. The contents of its program counter, stack pointer, and the other working registers are naturally subject to random factors and cannot be specified. For this reason, the CPU Set power-up sequence begins with a reset. An external RC network is connected to the 8224's RESIN/ input. The slow transition of the power supply rise is sensed by an internal Schmitt Trigger which converts the slow transition into a clean, fast edge on the RESIN/ line when the input level reaches a predetermined value.

An active RESIN/ input to the 8224 produces a synchronized RESET signal which restores the processor's internal program counter to zero. Program execution thus begins with memory location zero, following a reset. Systems which require the processor to wait for an explicit start-up signal will store an enable interrupt instruction (EI) and a halt instruction (HLT) in these locations. A manual or an automatic INTERRUPT will be used for starting. In other systems, the processor may begin executing its stored program immediately. Note, however, that the reset has no effect on status flags, or on any of the processor's working registers (accumulator, registers, or stack pointer). The contents of these registers remain indeterminate, until initialized explicitly by the program.

In addition to generating a RESET signal, the RESIN/ input causes the 8224's status strobe (STSTB/) output to remain true (low). This allows both the 8080 and 8238 to be reset by a power-up sequence or an externally generated RESET/ condition (input via connector pin P2-38).

3.2 SYSTEM BUS INTERFACE

The System Bus Interface allows the SBC 80/20 to use a common system bus with other master devices such as other CPU's, DMA devices or Peripheral Controllers, thus sharing memory and I/O resources. The System Bus Interface consists of a Bus Controller, a 74LS74 Override flip flop, six 8226 Bidirectional Bus Drivers, as well as an 8224 clock generator and a 74H74 D-type flip flop for generation of the Bus Clock and Constant Clock signals, as shown on sheet 1 of the SBC 80/20 schematic (Appendix A).

3.2.1 Bus Controller

The Bus Controller arbitrates all SBC 80/20 requests for use of the sytem bus, synchronously with respect to the Bus Clock (BCLK/). When the SBC 80/20 acquires control of the bus, the Bus Controller generates the appropriate memory or I/O command signal, gates the address onto the address lines, and gates data on/off the bus, at the appropriate times. An external RC network connected to the Bus Controller's Delay-Adjust (DLYADJ/) input guarantees the required setup and hold time relationships between the address/data lines and the control signals.

The negative-going edge of the Bus Clock (BCLK/) signal provides a timing reference for the Controller's bus arbitration logic. BCLK/ can be externally generated (and received at connector pin P1-13), or can be generated on the SBC 80/20 board (if jumper pair 110-111 is connected). An 18.432 MHz OSC output from the 8224 is applied to the clock input of a 74H74 D-type flip. The $\overline{Q}$ output from this latch is tied to its own D input. Consequently, the Q output exhibits half the frequency of the OSC input. If jumper pairs 112-113 and 110-111 are connected, this 9.216 MHz output is buffered and made available to external modules on the Constant Clock (CCLK/) line (via connector P1-31) and the Bus Clock (BCLK/) line (via connector P1-13), as well as the Bus Controller.

Bus arbitration activity begins when an external memory or I/O request (MBRQ/ or IORQ/) signal is generated and applied to the Bus request (BCR1) and Transfer Start Request (XSTR) inputs. The request is strobed in by RSTB/ (which is always enabled on the SBC 80/20). Following the next rising and falling edge of BCLK/ the Bus Controller outputs Bus Request, BREQ/ (connector pin P1-18) and forces Bus Priority Out, BPRO/ (connector pin P1-16) inactive (high). BREQ/ is used to request the system bus when priority is decided by a parallel priority resolution circuit such as an 8214 or a 3003 device. BPRO/ is used to allow lower priority masters to gain control of the bus when a serial priority resolution structure is used. BPRO/ would go to the Bus Priority In (BPRN/) input of the next lower priority master.

When control of the bus is granted to the SBC 80/20, a low level appears on its Bus Priority In (BPRN/) input. The Bus Controller activates its BUSY/ (connector pin P1-17) and Address and Data Enable (ADEN/) outputs. BUSY/ "locks" the SBC 80/20 onto the bus by prohibiting any other master from acquiring control of the bus. ADEN/ enables the 8226 devices which drive the system address (ADRO/-ADRF/) and data busses (DATO/-DAT7/). ADEN/ also enables the bus acknowledge gate at A28-13. When the external acknowledge signal (XACK/ or AACK/) is received it will be gated to the CPU section's RDYIN pin.

When one of the SBC 80/20 external access request lines (MBRQ/ or IORQ/) activates the Transfer Start Request input (XSTR) and ADEN/ is activated, the Bus Controller's timing logic starts the internal sequence which ultimately (depending on the RC network at DLYADJ/) generates the appropriate memory/IO read/write control output (MRDC/, MWTC/, IORC/, or IOWC/) based on the active command request input (MEMR/, MWT/, IOR/ or IOWT/) from the CPU section or Address Decoding logic.

The Bus Controller also provides two other outputs during external access operations. The Any Request output (ANYR) goes high (active) whenever one of the command request inputs (e.g., MWT) is active. The Read Data output (RDD) is always low (indicating write mode) except for read intervals that begin with the arrival of an active read command request (MEMR/ or IOR/) and end three gate delays after the read control output (MRDC/ or IORC/) goes inactive. RDD controls the direction of the two 8226 bidirectional devices which drive the System Data Bus (DATO/-DAT7/).

The SBC 80/20 can only lose control of the system bus if its BPRN/ input goes high or the bus request inputs (MBRQ/ and IORQ/) go inactive causing the Transfer Complete input (XCP/) to be activated. In either case, the SBC 80/20 will only lose the bus if it is not in the middle of a transfer and its override flip flop is not set (see below).

A low level on the Bus Controller's INIT/ input will initialze the device.

Bus Interface timing is illustrated in Figure 3-5.

3.2.2 SYSTEM BUS OVERRIDE FEATURE

If it is necessary to guarantee that the SBC 80/20 not lose control of the system bus, the override function can be invoked by executing an OUTPUT instruction to address D5 (hexadecimal). If data bit 0 is a "1" when this output instruction is executed, the Override flip flop (at A27) is set. While this flip flop is set, the SBC 80/20 cannot relinquish control of the system bus. If data bit 0 is "0" when the output instruction to address D5 is executed or if the Reset signal (RST/) is activated, the Override flip flop is reset. The SBC 80/20 must clear the Override capability

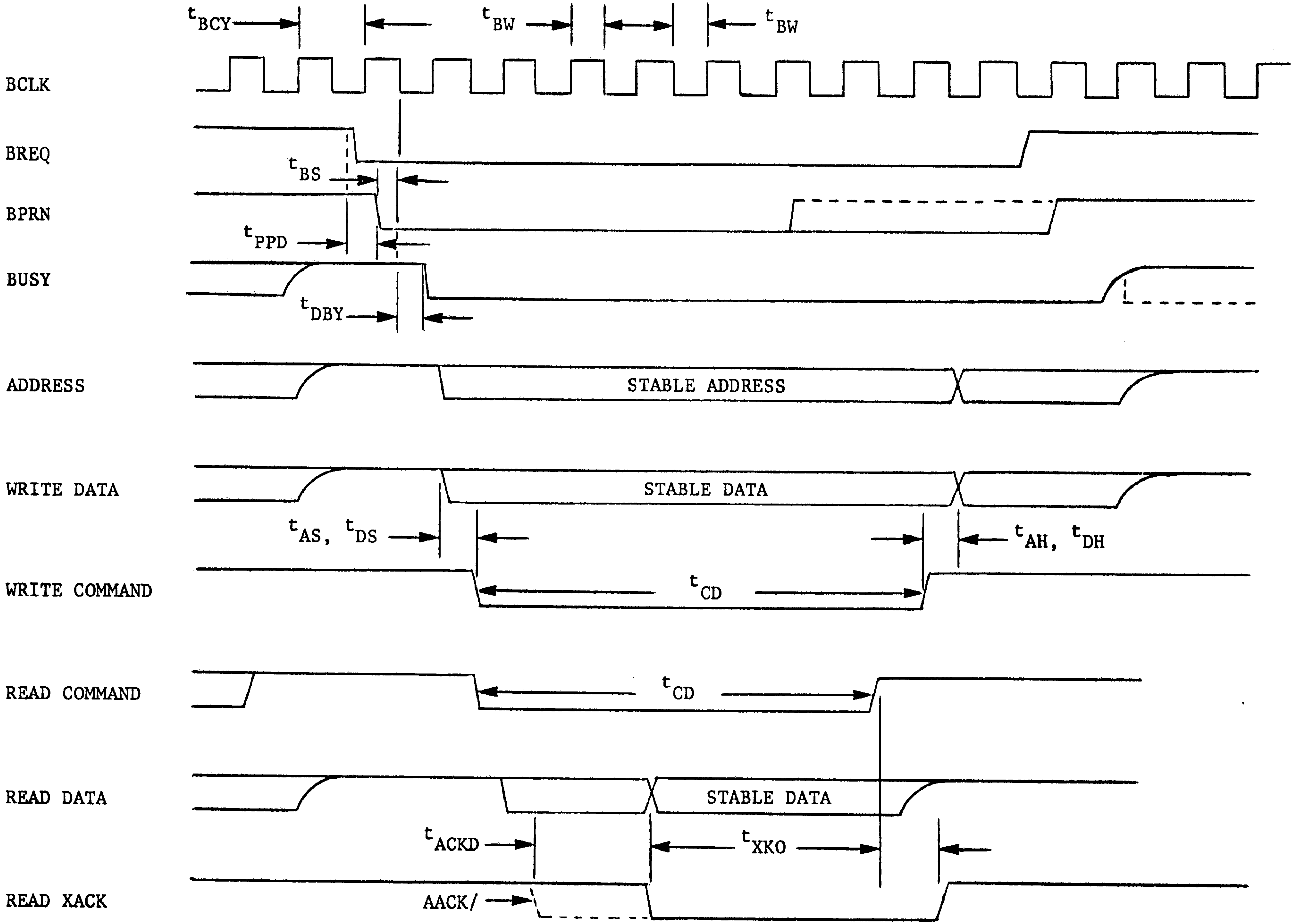


FIGURE 3-5. BUS INTERFACE TIMING (1 of 2 sheets)
(Exchange Mode)

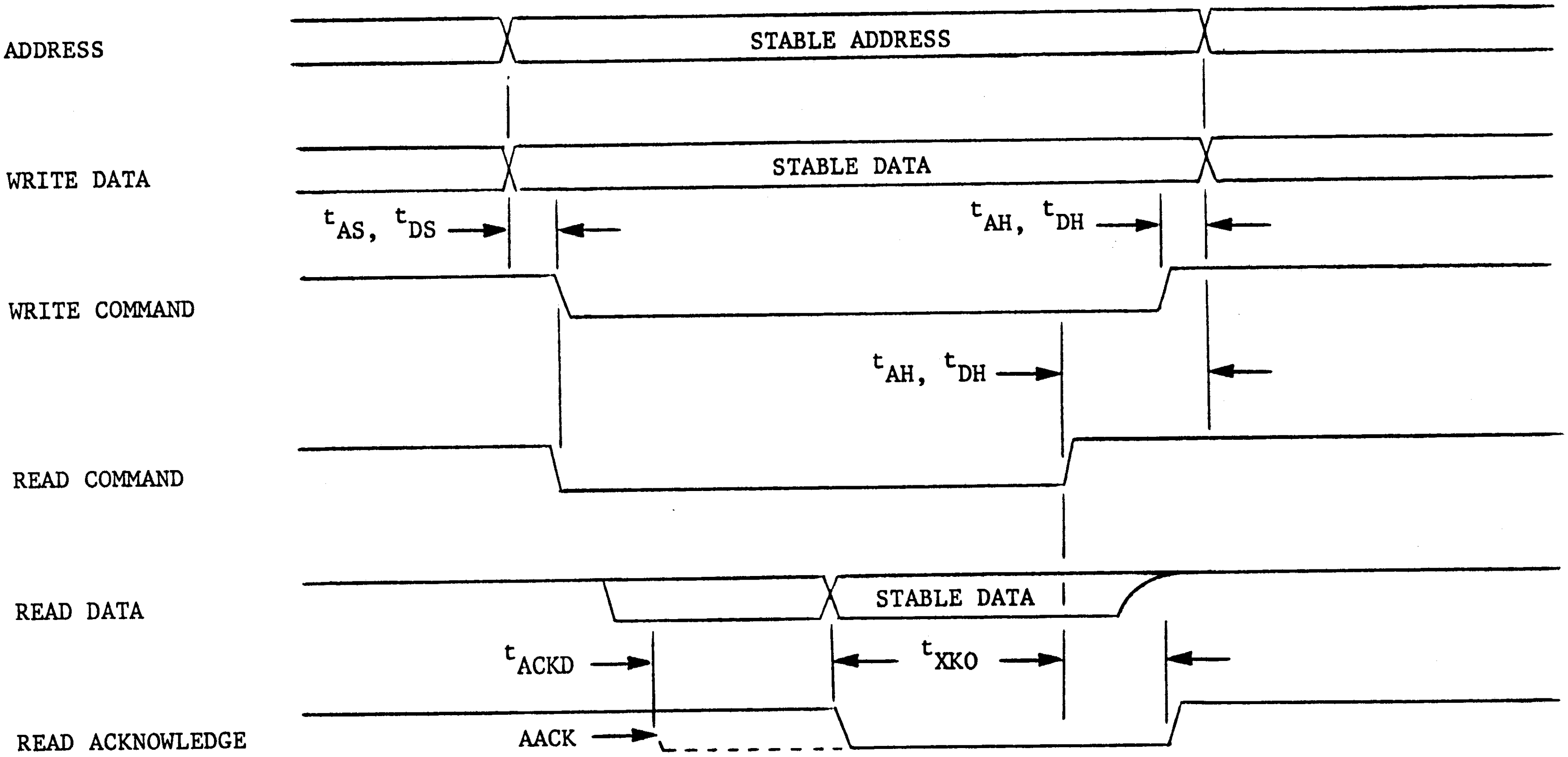


FIGURE 3-5. BUS INTERFACE TIMING (2 of 2 sheets)
(Override Mode)

when it is finished with exclusive use of the bus. This function is also useful in those cases where the SBC 80/20 is the only master in the system. In these applications, the SBC 80/20 can save an additional 216 nsec to get a command on the bus.

3.3 FAILSAFE TIMER

If the CPU section tries to access a memory or I/O device but that device, for whatever reason, does not return an acknowledgement (ready) indication, the 8080 remains in a wait state until ready is received. The Failsafe Timer is designed to prevent hanging the system up in this way. A 9602 one-shot (sheet 2 of schematic - Appendix A) is triggered by Status Strobe (STSTB), from the CPU 8224 Clock generator, at the beginning of each machine cycle. If the one-shot is not re-triggered (i.e., if another cycle does not begin) within approximately 10 m.s., the 9602 times out and its output is gated through to the RDYIN pin on the 8224, thus allowing the 8080 to exit the wait state. This feature can be very helpful during system debugging. The SBC 80/20 is shipped with the Failsafe enabled. To disable the Failsafe Timer remove jumper pair 137-138.

3.4 RANDOM ACCESS MEMORY (RAM)

The Random Access Memory (RAM section provides the SBC 80/20 or SBC 80/20-4 user with 2048 (2K) X 8-bits or 4096 (4K) X 8-bits of read/write storage respectively, using eight Intel 2113 (SBC

80-20) or eight Intel 2114 (SBC 80/20-4) static RAM devices. The 2113 or 2114 RAMs require neither refreshing nor clock inputs to operate. The RAM logic includes two 8216 four-bit bidirectional bus drivers, an 8205 one-of-eight decoder and a 74S139 one-of-four decoder (for address block and chip selection), as well as assorted gates and jumper pads as shown on sheet 3 of the schematic (Appendix A).

Each 2113 RAM device, on the SBC 80/20, stores 512 X 4-bits of data. Each 2114 RAM device, on the SBC 80/20-4, stores 1024 X 4-bits of data. Each chip has 10 address inputs (A0-A9) and four common data input/output pins (I/O_1-I/O_4), as well as active-low chip select (CS/) and write enable (WE/) inputs. Power inputs (+5V and ground) are also present. In the event of a power failure, power can be provided to the RAMs by a back-up battery input, thus ensuring that no memory data is lost.

The data input/output pins (I/O_1-I/O_4) are connected to the SBC 80/20 bus (DB0-DB7) through 8216 bidirectional bus drivers (at A25 and A26). During SBC 80/20 memory write cycles, the Memory Write control signal (MEMW/) causes the 8216 devices to accept data from the SBC 80/20 bus and make it available to the RAM devices. MEMW/ is also applied to the RAM write enable (WE/) inputs, permitting two selected RAM devices each to accept four bits of data and write them into the addressed location. During memory read cycles, the absence of a low level on MEMW/ causes the selected RAM's to output data from the addressed location. Likewise, the

8216 bidirectional bus drivers pass data from the RAM's onto the SBC 80/20 bus (DBØ-DB7).

When the on-board RAM is accessed, the nine least significant bits, AB0-AB8, of the 16-bit SBC 80/20 address bus specify the 4-bit segment to be accessed on the selected RAM's. Address bits AB9 and ABA specify which pair of RAM devices are to be selected. The next three address bits ABA, ABC, and ABD, must be high to allow the SBC 80/20 on-board RAM to be accessed.

The two most significant address bits, ABE and ABF, select one of the four 16K blocks within the total 64K memory address space that can be accessed by an 8080 microcomputer. Thus, SBC 80/20 RAM can be assigned to any one of the four 16K blocks of address space but it will always reside at the end of the selected 16K block.

The two most significant address lines, ABE and ABF, are applied to the address inputs on the 74S139 one-of-four decoder (at A78 pins 2 and 3). This decoder is enabled by the output from NAND gate at A45-8. Therefore address lines ABB, ABC and ABD must all be high to enable the 74S139 decoder. When enabled, the levels on ABE and ABF cause one of the four decoder outputs to go low. Each decoder output is tied to one half of a jumper pair, labeled "3", "7", "B" or "F" to represent the high order hexadecimal digit of the selected RAM address space. Table 3-1 correlates the four jumper connections with the selected RAM address space.

TABLE 3-1. RAM ADDRESS SELECTION JUMPERS

JUMPER CONNECTION	SELECTED RAM ADDRESS SPACE (hex)	
	2K (SBC 80/20)	4K (SBC) 80/20-4
120-121	3800-3FFF	3000-3FFF
119-121	7800-7FFF	7000-7FFF
118-121	B800-BFFF	B000-BFFF
117-121	F800-FFFF	F000-FFFF

When the jumper-selected decoder output is activated it allows the Memory Acknowledge signal (MACK/) to be generated (discussed below) and permits the 8216 bus drivers to be enabled. The active decoder output also enables the 8205 decoder at A24.

If the Memory Protect line, MPRO/ (connector pin P2-20), is inactive (high) and a memory read or write (MEMR/ or MEMW/) is indicated, the 8205 decoder will determine the two RAM chips to be selected. The low order four decoder outputs are each connected to the chip select (CS/) inputs on a pair of RAM devices. Thus, the active decoder output selects the two RAM chips to be accessed (A35 & A36, A38 & A39, A49 & A50 or A62 & A63). The least significant address bits (AB0-AB9) then specify the 4-bit segment to be accessed on each of the two selected RAM's.

The memory logic also includes several gates that are used to generate the following memory control signals: Memory Acknowledge (MACK/), Memory Bus Request (MBRQ) and Memory Write (MWT/).

During RAM access cycles, the Memory acknowledge signal (MACK/) is generated by the 7410 NAND gate at A47-8 when Memory read (MEMR/) or write (MEMW/) is true and the on-board RAM address space is selected (as described above). MACK/ is applied to the RDYIN input on the CPU Section and allows the 8080 to proceed with the access cycle without any wait states. When memory which is external to the SBC 80/20 is accessed, the external memory module must return a Transfer Acknowledge, XACK/ (connector pin P1-23). XACK/ and MACK/ indicate that data is available on the data bus during memory read cycles, or that data has been accepted from the data bus during memory write cycles. When a memory read command is issued for an external memory module, that module can return an advanced acknowledge AACK/ (connector pin P1-25), that will allow the data to be read without requiring any wait state. To summarize memory access acknowledgements: All SBC 80/20 on-board memory accesses (read and write) return MACK/ to the CPU Section and proceed without any wait states. All external memory accesses return XACK/ to the SBC 80/20 (even if AACK/ is also returned). During external memory read cycles, AACK/ can be returned before the data is actually read, allowing the read cycle to proceed with a minimum of one wait state. Otherwise, external accesses could require more than one wait state, as shown in Figure 3-6.

If MEMR/ or MEMW/ is true but the SBC 80/20 on-board memory is not selected, the System Memory Bus Request signal (MBRQ/) is generated (at A45-6). MBRQ/ is applied to the System Bus Interface and indicates that external memory is to be accessed.

The System Memory Write signal (MWT/) is also applied to the System Bus Interface. MWT/ is the result of NANDing the memory Write signal (MEMW/) from the 8238 System Controller with the Write pulse (WR/) from the 8080. Recall that MEMW/ is generated at the beginning of all memory write cycles (state T2). MEMW/ occurs earlier than WR/ and allows the memory acknowledge (MACK/) for on-board accesses to be returned early enough to avoid an unnecessary wait state. Thus, MEMW/ is synchronized with WR/ to produce MWT/. The MWT/ signal causes the data to be written into an external memory location, during state T3 of the memory cycle. Thus, all external writes will require at least one wait state.

Memory access timing is illustrated in Figure 3-6.

3.5 READ ONLY MEMORY (ROM/PROM)

The SBC 80/20 and SBC 80/20-4 have provision for installing 4096 (4K) X 8-bit words of read only memory in sockets on the PC board. Four Intel 8708 1K X 8-bit Erasable and Electronically Programmable Read Only Memory (EPROM) chips or four 8308 1K X 8-bit static MOS mask Read Only Memory (ROM) chips can be installed in the four 24-pin sockets. The SBC 80/20 and SBC 80/20-4 also have provisions

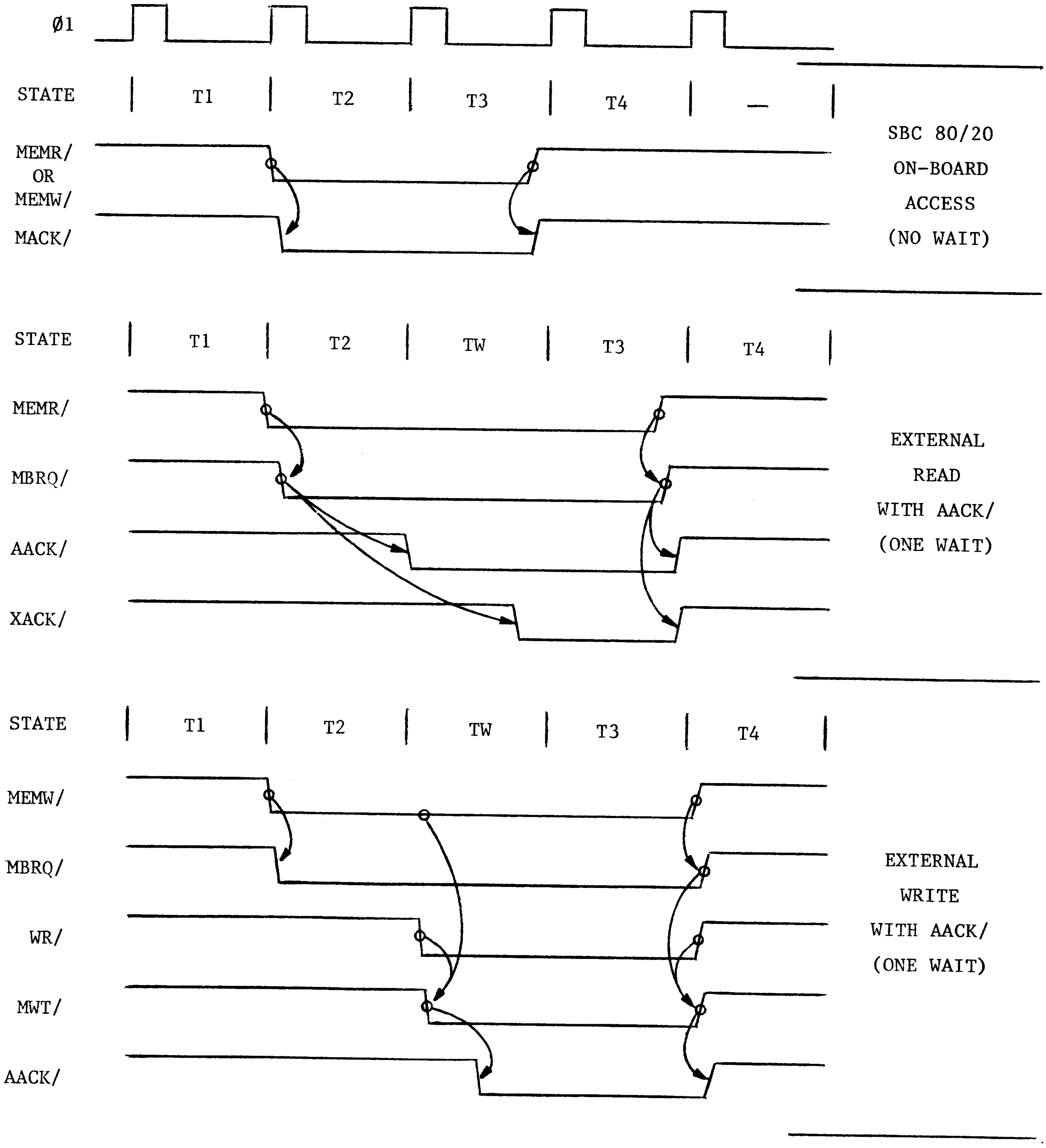


FIGURE 3-6. MEMORY ACCESS TIMING

for ·installing 8192 (8K) X 8-bit words of memory by using Intel 2716 2K X 8-bit Erasable and Electronically Programmable Read Only Memory or 8316B Masked ROM chips instead of 8708 or 8308 chips.

In addition to the four 24-pin sockets, the ROM/EPROM logic includes a 74S139 one-of-four decoder for chip selection and assorted gates as shown on sheet 3 of the schematic (Appendix A).

The ten least significant address lines, AB0-AB9 are applied to the address pins (A0-9) at each of the four sockets. Address lines ABA and ABB are applied to the two inputs of the 74S139 decoder at A78, pins 13 and 14. Unless the decoder is disabled by the line which specifies RAM selection (as described in the previous section) or the memory read signal (MEMR/) is inactive, the levels on ABA and ABB will cause one of the four decoder outputs to go low and enable one of the four ROM/EPROM chips in sockets A37, A51, A64 or A79.

The four most significant address lines, ABC-ABF, are gated together (all four must be low) and ORed with the RAM selection line to form the signal which indicates that an SBC 80/20 on-board memory access is to occur. Thus, the SBC 80/20 ROM/EPROM will always begin at memory address zero.

During on-board ROM/EPROM read cycles, the selection line is NANDed with Memory Read (MEMR/) to generate the Memory Acknowledge signal, MACK/ (at A47-8), as well as the signal (at A47-6) which enables the 8216 bidirectional bus drivers. The bus drivers gate data read from a ROM/EPROM chip onto the SBC 80/20 data bus (DB0-DB7). Notice on the schematic that the output from the NAND gate at A48-3 prevents MACK/ and the bus driver enable signal from being generated during memory write cycles addressed to the ROM/EPROM address space.

If neither SBC 80-20 on-board RAM nor ROM/EPROM is selected, the System Memory Bus Request signal (MBRQ/) is generated as described in the previous section.

ROM/EPROM read timing is as shown in Figure 3-6(A). All SBC 80/20 on-board ROM/EPROM reads proceed without any wait states.

3.6 I/O ADDRESS DECODING

The SBC 80/20 includes the following programmable devices which are accessed by I/O commands directed to particular addresses:

- Two 8255 Programmable Peripheral Interfaces
- 8251 USART Serial I/O Interface
- 8259 Interrupt Controller
- 8253 Interval Timer
- Power Fail Status/Interrupt latch
- System Bus override flip flop
- LED Diagnostic Indicator

The I/O Address Decoding logic accepts address lines AB2 through AB7 and generates the appropriate chip select/enable signal for the addressed device. This logic consists of two 8205 one-of-eight decoders and assorted gates as shown on sheet 5 of the schematic (Appendix A).

Address lines AB2-AB4 are applied to the address inputs of the first decoder (at A13). Address lines AB4-AB7 are gated through to the decoder enable inputs such that only I/O addresses between DO and EF (hexadecimal) will enable the decoder. Decoder output 0 is not used. Decoder output 1 is true (low) when the address lies between E4 and E7. This line is labeled PE47/, and is made available to the 8255 parallel I/O interface chip select input at A20-6, Decoder output 2 is true when the address lies between E8 and EB. This line is labeled PE8B/, and is made available to the other 8255 device chip select input at A21-6. Decoder output 3 is true when the address lies between EC and EF. This line is applied to the chip select input on the 8251 USART. Decoder output 4 is not used. Decoder output 5 is true when the address lies between D4 and D7. This line enables the second 8205 decoder (at A15) as described below. Decoder output 6 is true when the address lies between D8 and DB. This line enables the 8253 Interval Timer. Decoder output 7 is true when the address lies between DC and DF. This line, labeled INTP/, enables the 8259 Interrupt Controller.

The second 8205 decoder (at A15) further decodes I/O addresses between D4 and D7 (after one wait state, unless jumper pair 115-116 is disconnected) if one of the I/O control signals (IOR/ or IOW/) is true. Address lines ABO and AB1 are applied to decoder inputs AO and A1. IOW/ and WR/ are NANDed together at A30-3 and the result is applied to decoder input A3. Consequently output 0 from this decoder (OD4/) is true near the end of an I/O write to port D4 instruction. OD4/ resets the Power Fail status latch at A27-1. Decoder output 1 (OD5/) is true for an output to port D5. OD5/ clocks the System Bus override flip flop. Decoder output 2 is true for an output to port D6 which triggers a 1ms one-shot that flashes the light emitting diode (LED) at DS1. Decoder output 4 is true when I/O read to port 4 is executed. This line enables the Power Fail Status signal (PFS/) from connector pin P2-17 to data bus line 0 (DB0). None of the other outputs on the second decoder are used.

Table 3-2 summarizes I/O addressing for the SBC 80/20.

Whenever I/O Read (IOR/) or I/O Write (IOW/) is true and the address on the bus represents a value between D4-DF or E4-EF, the I/O Acknowledge signal (IOAK/) is generated when the 8080's WAIT/ output goes low, thus requiring one wait state during all SBC 80/20 on-board I/O cycles, as shown in Figure 3-7.

If IOR/ or IOW/ is true but the I/O address refers to an external port, the I/O Request signal (IORQ/) is generated and applied to System Bus Interface which will attempt to acquire control of the System Bus in order to execute the I/O instruction. The external I/O device must return a Transfer Acknowledge signal (XACK/) to complete the I/O cycle.

3.7 SERIAL I/O INTERFACE

The Serial I/O Interface logic provides the SBC 80/20 with a serial data communications channel that can be programmed to operate

TABLE 3-2. I/O PORT ADDRESSING

I/O PORT ADDRESS (hexadecimal)	I/O DEVICE	INPUT FUNCTION	OUTPUT FUNCTION
D4	Power Fail	Read Power Fail Status	Reset Power Fail latch
D5	System Bus Override	*Not used	Set or reset override control (using data bus line 0).
D6	LED Diagnostic Indicator	*Not used	Flash LED.
D7	*Not used	--	--
**D8 or DA **D9 or DB	8259 Interrupt Controller	Various read functions. (See Section 3.10)	Various write functions. (See Section 3.10)
DC DD DE DF	8253 Interval Timer	Read counter 0 Read counter 1 Read counter 2 *Not used	Load counter 0 Load counter 1 Load counter 2 Mode control
E4 E5 E6 E7	8255 PPI #1	Read port A Read port B Read port C --	Write port A Write port B Write port C Control
E8 E9 EA EB	8255 PPI #2	Read port A Read port B Read port C --	Write port A Write port B Write port C Control
**EC or EE **ED or EF	8251 USART	Data in Read Status	Data out Control

**Either port address may be used.
*Though these port addresses are not used by the SBC 80/20, they are not available for use by external I/O devices.

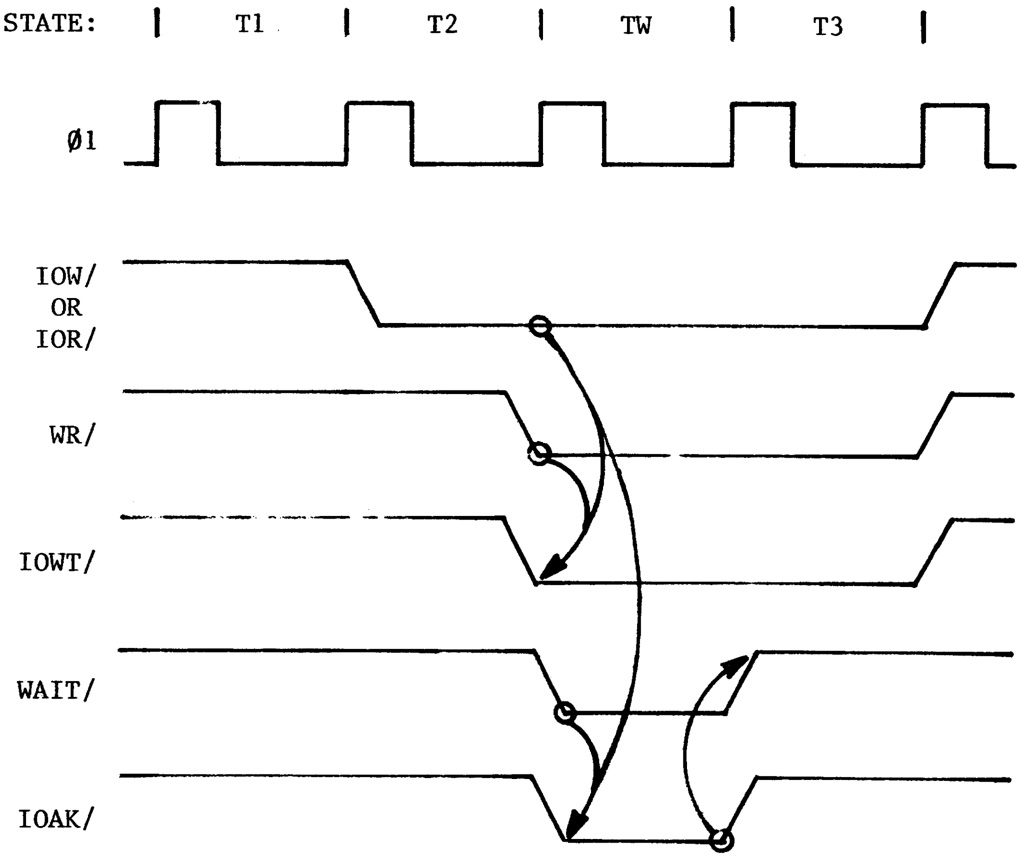


FIGURE 3-7. SBC 80/20 ON-BOARD I/O TIMING

with most of the current serial data transmission protocols, synchronous or asynchronous. Baud rate, character length, number of stop bits and even/odd parity are program selectable.

The Serial I/O Interface logic consists primarily of an Intel 8251 USART device and several driver/receiver circuits as shown on sheet 5 of the SBC 80/20 schematic (Appendix A). Before describing the specific operation of the Serial I/O logic however, we will summarize the general operational characteristics of the 8251 USART, because it essentially defines the character of the serial I/O Interface.

3.7.1 INTEL®8251 OPERATIONAL SUMMARY

The 8251 is a Universal Synchronous/Asynchronous Receiver/ Transmitter designed specifically for the 8080 Micro-computer System. Like other I/O devices in the 8080 Micro-computer System its functional configuration is programmed by the systems software for maximum flexibility. The 8251 can support virtually any serial data technique currently in use (including IBM "Bi-Sync").

Modem Control

The 8251 has a set of control inputs and outputs that can be used to simplify the interface to almost any Modem. The Modem control signals are general purpose in nature and can be used for functions other than Modem control, if necessary.

$\overline{\text{DSR}}$ (Data Set Ready)

The $\overline{\text{DSR}}$ input signal is general purpose in nature. Its condition can be tested by the CPU using a Status Read Operation. The $\overline{\text{DSR}}$ input is normally used to test Modem conditions such as Data Set Ready.

$\overline{\text{DTR}}$ (Data Terminal Ready)

The $\overline{\text{DTR}}$ output signal is general purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{\text{DTR}}$ output signal is normally used for Modem control such as Data Terminal Ready or Rate Select.

$\overline{\text{RTS}}$ (Request to Send)

The $\overline{\text{RTS}}$ output signal is general purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{\text{RTS}}$ output signal is normally used for Modem control such as Request to Send.

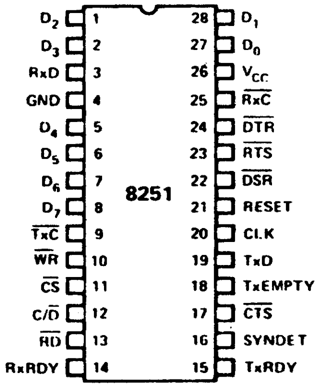
$\overline{\text{CTS}}$ (Clear to Send)

A "low" on this input enables the 8251 to transmit data (serial) if the TxEN bit in the Command byte is set to a "one". This is very important to remember!

TXRDY (Transmitter Ready)

This output signals the CPU that the transmitter is ready to accept a data character. It can be used as an interrupt to the system or for polled operation when the CPU can check TXRDY using a status read operation. TXRDY is active only when $\overline{\text{CTS}}$ is enabled.

USART
PIN CONFIGURATION


D_2 1
D_3 2
RxD 3
GND 4
D_4 5
D_5 6
D_6 7
D_7 8
$\overline{\text{TxC}}$ 9
$\overline{\text{WR}}$ 10
$\overline{\text{CS}}$ 11
C/$\overline{\text{D}}$ 12
$\overline{\text{RD}}$ 13
RxRDY 14
8251
28 D_1
27 D_0
26 V_{CC}
25 $\overline{\text{RxC}}$
24 $\overline{\text{DTR}}$
23 $\overline{\text{RTS}}$
22 $\overline{\text{DSR}}$
21 RESET
20 CLK
19 TxD
18 TxEMPTY
17 $\overline{\text{CTS}}$
16 SYNDET
15 TxRDY

Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
$\overline{\text{WR}}$	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{\text{TxC}}$	Transmitter Clock
TxD	Transmitter Data
$\overline{\text{RxC}}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

Pin Name	Pin Function
$\overline{\text{DSR}}$	Data Set Ready
$\overline{\text{DTR}}$	Data Terminal Ready
SYNDET	Sync Detect
$\overline{\text{RTS}}$	Request to Send Data
$\overline{\text{CTS}}$	Clear to Send Data
TxE	Transmitter Empty
Vcc	+5 Volt Supply
GND	Ground

FIGURE 3-8. 8251 PIN ASSIGNMENTS

TXRDY is automatically reset when a character is loaded from the CPU.

TXE (Transmitter Empty)

When the 8251 has no characters to transmit, the TXE output will go "high". It resets automatically upon receiving a charater from the CPU. TXE can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplexed operational mode.

In SYNChronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be transmitted automatically as "fillers".

$\overline{\text{TXC}}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the frequency of $\overline{\text{TXC}}$ is equal to the actual Baud Rate (1X). In Asynchronous transmission mode, the frequency of $\overline{\text{TXC}}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1X, 16X or 64X the Baud Rate.

For Example:

If Baud Rate equals 110 Baud,
$\overline{\text{TXC}}$ equals 110 Hz (1X)
$\overline{\text{TXC}}$ equals 1.76 kHz (16X)
$\overline{\text{TXC}}$ equals 7.04 kHz (64X).
If Baud Rate equals 9600 Baud,
TXC equals 153.6 kHz (16X).

The falling edge of $\overline{\text{TXC}}$ shifts the serial data out of the 8251.

RXRDY (Receiver Ready)

This output indicates that the 8251 contains a character that is ready to be input to the CPU. RXRDY can be connected to the interrupt structure of the CPU or for polled operation the CPU can check the condition of RXRDY using a status read operation. RXRDY is automatically reset when the character is read by the CPU.

$\overline{\text{RXC}}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the frequency of $\overline{\text{RXC}}$ is equal to the actual Baud Rate (1X). In Asynchronous Mode, the frequency of $\overline{\text{RXC}}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1X, 16X or 64X the Baud Rate.

For Example:

If Baud Rate equals 300 Baud,

$\overline{\mathrm{RXC}}$ equals 300 Hx (1X)

$\overline{\mathrm{RXC}}$ equals 4800 Hz (16X)

RXC equals 19.2 kHz (64X).

If Baud Rate equals 2400 Baud,

$\overline{\mathrm{RXC}}$ equals 2400 Hz (1X)

$\overline{\mathrm{RXC}}$ equals 38.4 kHz (16X)

$\overline{\mathrm{RXC}}$ equals 153.6 kHz (64X).

Data is sampled into the 8251 on the rising edge of $\overline{\mathrm{RXC}}$.

Note: In most communications systems, the 8251 will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{\mathrm{TXC}}$ and $\overline{\mathrm{RXC}}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

SYNDET (SYNC Detect)

This pin is used in SYNChronous Mode only. It is used as either input or output, programmable through the Control Word. It is reset to "low" upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251 has located the SYNC character in the Receive mode. If the 8251 is programmed to use double Sync characters, then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

When used as an input, (external SYNC detect mode), a positive going signal will cause the 8251 to start assembling data characters on the falling edge of the next $\overline{\text{RXC}}$. Once in SYNC, the "high" input signal can be removed. The duration of the high signal should be at least equal to the period of $\overline{\text{RXC}}$.

Programming the 8251

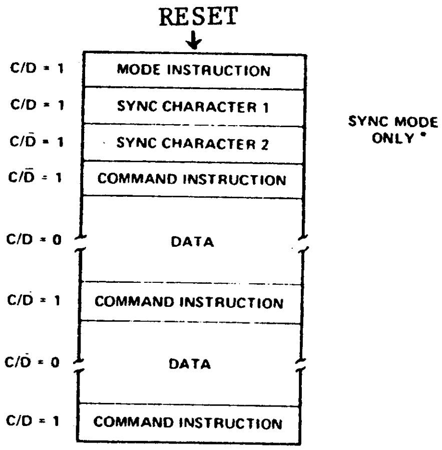
Prior to starting data transmission or reception, the 8251 must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251 and must immediately follow a System Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction,
2. Command Instruction.

Both the Mode and Command instructions must conform to a specified sequence for proper device operation. The Mode Instruction must be inserted immediately following a Reset operation, prior to using the 8251 for data communication.

All control words written into the 8251 after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251 at any time in the data block during the operation of the 8251. To return to the Mode Instruction format a bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the 8251 back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters (see Figure 3-9).



*The second SYNC character is skipped if MODE instruction has programmed the 8251 to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the 8251 to ASYNC mode.

FIGURE 3-9. TYPICAL 8251 DATA BLOCK

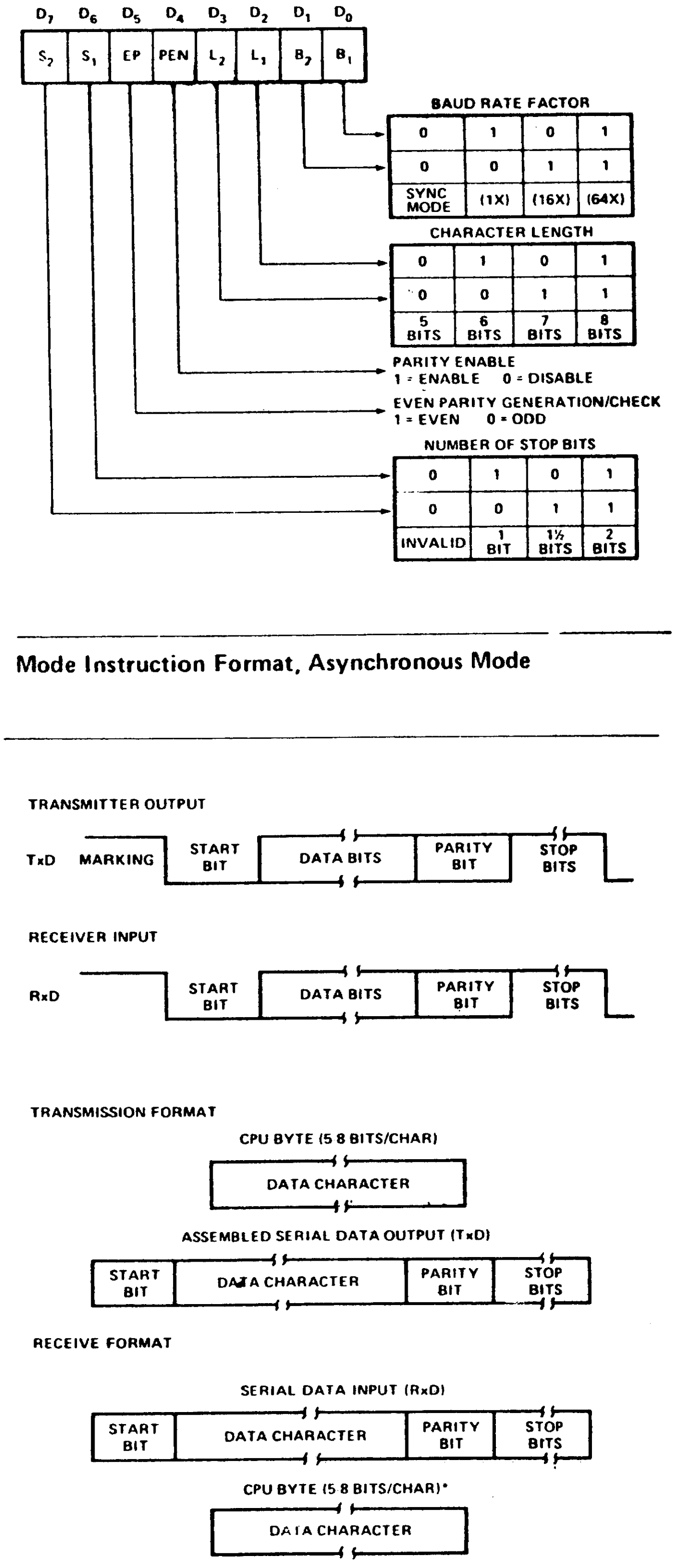
Mode Instruction:

This format defines the general operational characteristics of the 8251. It must follow a Reset operation (internal or external). Once the Mode instruction has been written into the 8251 by the CPU, SYNC characters or Command instructions may be inserted.

The 8251 can be used for either synchronous or asynchronous data communications. The two least significant bits of the Mode Instruction control word specify synchronous or asynchronous operation. The format for the remaining bits in the control word depends on the mode chosen by bits 0 and 1. Figure 3-10 shows the control word format for the asynchronous mode, while Figure 3-11 illustrates the control word format for the synchronous mode.

Command Instruction:

Once the functional definition of the 8251 has been programmed



0	1	0	1
0	0	1	1
SYNC MODE	(1X)	(16X)	(64X)

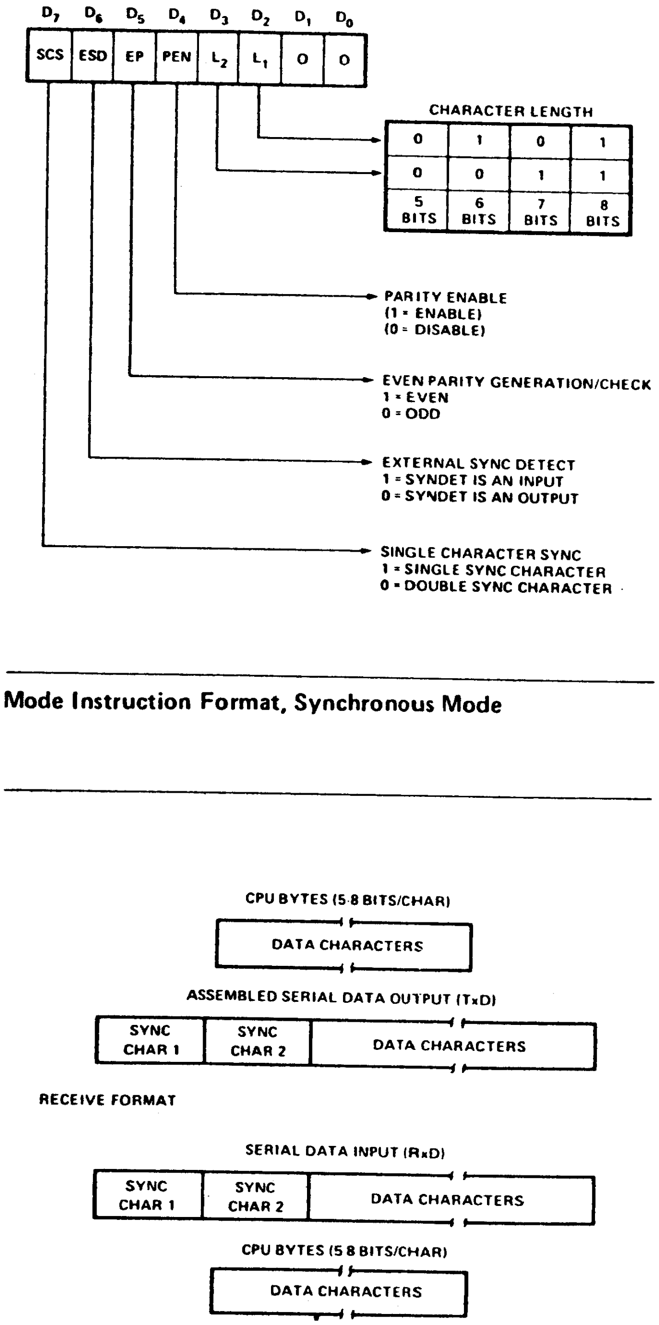
0	1	0	1
0	0	1	1
5 BITS	6 BITS	7 BITS	8 BITS

0	1	0	1
0	0	1	1
INVALID	1 BIT	1½ BITS	2 BITS

Mode Instruction Format, Asynchronous Mode

*NOTE: IF CHARACTER LENGTH IS DEFINED AS 5, 6 OR 7 BITS THE UNUSED BITS ARE SET TO "ZERO".

FIGURE 3-10. ASYNCHRONOUS MODE.



0	1	0	1
0	0	1	1
5 BITS	6 BITS	7 BITS	8 BITS

Mode Instruction Format, Synchronous Mode

FIGURE 3-11. SYNCHRONOUS MODE

by the Mode Instruction and the Sync Characters are loaded (if in Sync Mode) then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode instruction has been written into the 8251 and Sync characters inserted, if necessary, then all further "control writes" ($C/\overline{D} = 1$) will load the Command Instruction. A Reset operation (internal or external) will return the 8251 to the Mode Instruction Format.

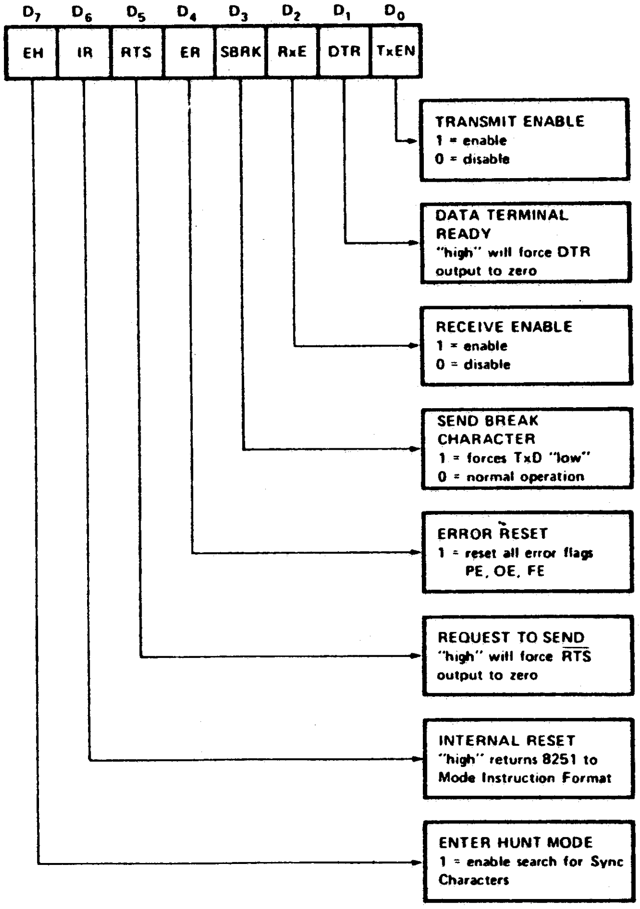
Figure 3-12 illustrates the format of a Command Instruction control word.

Status Read Definition

In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251 has facilities that allow the programmer to "read" the status of the device at any time during the functional operation.

A normal "read" command is issued by the CPU with the $C/\overline{D}$ input at one to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251 can be used in a completely Polled environment or in an interrupt driven environment (refer to Figure 3-13.

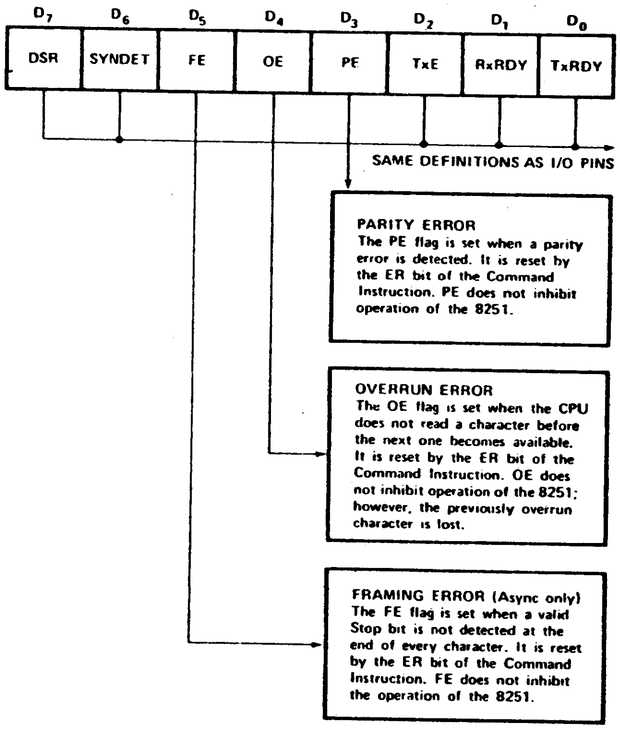


D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
EH
IR
RTS
ER
SBRK
RxE
DTR
TxEN
TRANSMIT ENABLE
1 = enable
0 = disable
DATA TERMINAL READY
"high" will force DTR output to zero
RECEIVE ENABLE
1 = enable
0 = disable
SEND BREAK CHARACTER
1 = forces TxD "low"
0 = normal operation
ERROR RESET
1 = reset all error flags PE, OE, FE
REQUEST TO SEND
"high" will force RTS output to zero
INTERNAL RESET
"high" returns 8251 to Mode Instruction Format
ENTER HUNT MODE
1 = enable search for Sync Characters

FIGURE 3-12. COMMAND INSTRUCTION FORMAT

8251 DATA TRANSFERS

Once programmed, the 8251 is ready to perform its communication functions. The TXRDY output is raised "high" to signal the CPU that the 8251 is ready to receive a character. This output (TXRDY) is reset automatically when the CPU writes a character into the 8251. On the other hand, the 8251 receives serial data from the MODEM or I/O device; upon receiving an entire character the RXRDY output is raised "high" to signal the CPU that the 8251 has



PARITY ERROR
The PE flag is set when a parity error is detected. It is reset by the ER bit of the Command Instruction. PE does not inhibit operation of the 8251.

OVERRUN ERROR
The OE flag is set when the CPU does not read a character before the next one becomes available. It is reset by the ER bit of the Command Instruction. OE does not inhibit operation of the 8251; however, the previously overrun character is lost.

FRAMING ERROR (Async only)
The FE flag is set when a valid Stop bit is not detected at the end of every character. It is reset by the ER bit of the Command Instruction. FE does not inhibit the operation of the 8251.

FIGURE 3-13. STATUS READ FORMAT

a complete character ready for the CPU to fetch. RXRDY is reset automatically upon the CPU read operation.

The 8251 cannot begin transmission until the TXEN (Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send (CTS) input. The TXD output will be held in the marking state upon Reset.

Asynchronous Mode (Transmission):

Whenever a data character is sent by the CPU the 8251 automatically adds a Start bit (low level) and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TXD output. The serial data is shifted out on the falling edge of $\overline{\text{TXC}}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{\text{TXC}}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TXD if commanded to do so.

When no data characters have been loaded into the 8251 the TXD output remains "high" (marking) unless a Break (continuously low) has been programmed.

Asynchronous Mode (Receive):

The RXD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center. If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RXD pin with the rising edge of $\overline{\text{RXC}}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. This character is then loaded into the parallel I/O buffer of the 8251. The RXRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN flag is raised (thus the previous character is lost). All of the error flags can be reset by a command instruction. The occurrence of any of these errors will not stop the operation of the 8251.

Synchronous Mode (Transmission):

The TXD output is continuously high until the CPU sends its first character to the 8251 which usually is a SYNC character. When the $\overline{\text{CTS}}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{\text{TXC}}$. Data is shifted out at the same rate as the $\overline{\text{TXC}}$.

Once transmission has started, the data stream at TXD output must continue at the $\overline{\text{TXC}}$ rate. If the CPU does not provide the 8251 with a character before the 8251 becomes empty, the SYNC characters (or character if in single SYNC word mode) will be automatically inserted in the TXD data stream. In this case, the TXEMPTY pin will momentarily go high to signal that the 8251 is empty and SYNC characters are being sent out. The TXEMPTY pin is internally reset by the next character being written into the 8251.

Synchronous Mode (Receive):

In this mode, character synchronization can be internally or externally achieved. If the internal SYNC mode has been programmed, the receive starts in a HUNT mode. Data on the RXD pin is then sampled in on the rising edge of $\overline{\text{RXC}}$. The content of the RX buffer is continuously compared with the first SYNC character until a match occurs. If the 8251 has been programmed for two SYNC characters, the subsequent received character is also compared. When both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ.

In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin. The high level can be removed after one $\overline{\text{RXC}}$ cycle.

Parity error and overrun error are both checked in the same way as in the Asynchronous receive mode.

The CPU can command the receiver to enter the HUNT mode if synchronization is lost.

3.7.2 Serial I/O Configurations

The 8251 USART presents a parallel, eight-bit interface to the CPU Set via the system data bus (DB0-DB7) and presents an EIA RS232C interface to an external device (via edge connector J3). The 8251's interface with the CPU Set is enabled by a low level on its chip select (CS/) pin. CS/ is low when the I/O address on the system address bus is between EC and EF (hexadecimal). Refer to Table 3-3. Address bits 2 through 7 are decoded to produce the CS/ input. The least significant address bit, ABØ, is applied to the 8251's C/$\overline{\text{D}}$ input (pin 12) thus indicating a control (if set) or data (if reset) byte on the data bus.

An output instruction (IOWT/ is true) to port ED or EF (CS/ is low and ABØ is high) causes the 8251 to accept a control byte through its data bus pins. The control byte can be either a mode

TABLE 3-3. SERIAL COMMUNICATION (8251) ADDRESS ASSIGNMENTS

I/O ADDRESS (BASE 16)	COMMAND	FUNCTION	DIRECTION
ED OR EF	OUTPUT	CONTROL WORD	CPU → USART
EC OR EE	OUTPUT	DATA	CPU → USART
ED OR EF	INPUT	STATUS	USART → CPU
EC OR EE	INPUT	DATA	USART → CPU

instruction or a command instruction, depending on the sequence in which it is sent. The various bits in the mode control word specify the baud rate multiplier, character length, parity and the number of stop bits as described in Section 3.7.1. Note that the actual baud rate selected is dependent on the baud rate input from the 8253 Interval Timer (refer to Section 3.9). The various bits in the command control word instruct the USART to enable/ disable the receiver and transmitter, to reset errors, to reset internal control and return to the mode control cycle, and to set/clear the Data Terminal Ready output.

An output instruction to port EC or EE (CS/ and ABØ are low) causes the 8251 USART to accept a data byte through its data bus pins. Bit 0 is the least significant bit and bit 7 is the most significant bit. The 8251 will subsequently transmit the data byte (if the transmitter is enabled), in serial fashion, to the external device as described in Section 3.7.1.

An input instruction (IOR/ is true) to port ED or EF (CS/ is low and ABØ is high) causes the 8251 USART to place a status byte onto the system bus. The status bits are the result of status and error checking functions performed within the USART (see Section 3.7.1).

An input instruction (IOR/ is true) to port EC or EE (CS/ and ABØ are low) causes the USART to output a data byte (previously received from the external device) from its data bus pins. Bit 0 is the least significant bit and bit 7 is the most significant bit.

Timing for the USART's internal function is provided by the Ø2T signal (see Section 3.1.1). The USART is reset by the occurrence of a high level on the RST line.

The 8251 USART transmits and receives serial data, synchronously or asynchronously, as described in Section 3.7.1.

3.7.3 SERIAL I/O INTERRUPTS

The Serial I/O logic can utilize several different interrupt request lines. The user can allow the 8251's Receiver Ready (RXRDY) output (pin 14) to generate an interrupt request to the CPU Set. RXRDY goes high whenever the receiver enable bit of the command word has been set and the 8251 contains a character that is ready to be input to the CPU Set. The user can also choose to have the 8251's Transmitter Ready (TXRDY) or the Transmitter Empty (TXE) outputs activate interrupt requests. TXE goes high when the 8251 has no characters to transmit. TXRDY is high when the 8251 is ready to accept a character from the CPU Set. Both TXE and TXRDY are enabled by setting the transmit enable bit of the command word. All three interrupt request lines are made available to the 8259 Interrupt controller (see Section 3.10).

Upon receiving an interrupt, the program can determine the actual condition which is responsible for the interrupt (RXRDY, TXRDY or TXE) by reading the status of the 8251 device as described in Section 3.7.1. The interrupt request will be removed when the data is transferred to/from the 8251, as required. Note that the TXE or TXRDY output will be high, and consequently maintain an interrupt request, during all idle periods, since the 8251's transmit buffer will remain empty. To disable the transmitter, and the resultant interrupt request, the program can issue a command instruction to the 8251 with the TXEN bit (bit 0) equal to zero (refer to Section 3.7.1). The transmitter should not be disabled until TXE is high.

3.7.4 RS232 INTERFACE FEATURES

The 8251 USART and associated logic allow the SBC 80/20 to function as a "data set" in an RS232-compatible serial communications network. The RS232 interface signals are summarized in Table 3-4.

The input and output paths between the 8251 and the RS232 interface at connector J3 contain a number of selectable features that the user should consider. Each of these features is briefly described below:

- Transmit and Receive Timing - The user has the option of using the baud rate generation capability of the 8253

Interval Timer or of utilizing an external timing reference for serial transmissions and receptions. If jumper pairs 16-18 and 19-21 are connected, the output of counter 2 on the 8253 Timer will provide timing at the USART's Receive ($\overline{\text{RXC}}$) and Transmit ($\overline{\text{TXC}}$) clock inputs. If jumpers 16-18 and 19-21 are deleted and jumper connection 17-18 and 20-21 are added, the REC. SIG. ELE. TIMING (connector pin J3-7) and TRANS. SIG. ELE. TIMING (connector pin J3-3) inputs will be tied to $\overline{\text{RXC}}$ and $\overline{\text{TXC}}$, respectively.

- Reading RS232 inputs via Parallel Interface Port 6* - Five RS232 input signals, RING INDICATOR (J3-17) REC. LINE SIG. DET. (J3-16), SEC. TRANS. DATA (J3-1), SEC RTS (J3-11) and can be connected to otherwise unused Port 6 bits so that they can be read by the user through that port. These inputs are available to Port 6 from the following jumper pins: (see sheet 4 of the schematic):

  RING INDICATOR - pin 96 (via line BRI/)
  REC. LINE SIG. DET. - pin 97 (via line BDET)

  SEC. TRANS. DATA
  (if jumper pins 6-8 are connected)
  SEC. RTS
  (if jumper pins 7-9 are connected)
  } - pin 89 (via line AUX1)

- Writing RS232 outputs via Parallel Interface Port 6* - The user can output signals on the SEC CTS (connector pin J3-26) or SEC. REC. DATA (J3-5) lines through Port 6 by connecting TRANS. SIG. ELE. TIMING (J3-21) jumper pin 90 (AUXØ), shown on sheet 4 of the schematic, to one of the unused Port 6 bits. To enable the SEC CTS output, jumper pins 13-14 must also be connected; to enable SEC. REC. DATA, jumper pins 14-15 must be connected.

3.8 PARALLEL I/O INTERFACE

The Parallel I/O Interface logic on the SBC 80/20 provides forty-eight (48) signal lines for the transfer and control of

*Refer to Section 3.8 concerning dedicated use of Port 6 bits.

TABLE 3-4. RS232 INTERFACE SIGNALS

J3 CONNECTOR PIN	SIGNAL NAME	DIRECTION	USART CONNECTION (PIN NO.)
6	RECEIVED DATA	USART → Terminal	TXD (19)
10	CLEAR TO SEND	USART → Terminal	RTS (23)
12	DATA SET READY	USART → Terminal	DTR (24)
26	SEC. CTS. or	Port 6 (AUXØ) → Terminal	*
5	SEC. REC. DATA		
21	TRANS. SIG. ELE. TIMING		
11	SEC. RTS.	Terminal → Port 6 (AUX1)	**
1	SEC. TRANS. DATA		
4	TRANSMITTED DATA	Terminal → USART	RXD (3)
7	***REC. SIG. ELE. TIMING	Terminal → USART	RXC (25)
3	***TRANS. SIG. ELE. TIMING	Terminal → USART	TXC (9)
8	REQUEST TO SEND	Terminal → USART	CTS (17)
13	DATA TERMINAL READY	Terminal → USART	DSR (22)
17	RING INDICATOR	Terminal → Port 6 (BRI/)	*
16	REC. LINE SIG. DET.	Terminal → Port 6 (BDET)	*

*These inputs are not connected to the 8251 USART but can be read through peripheral Interface Port 6.

**These outputs are not connected to the 8251 USART but can be written to the terminal through peripheral Interface Port 6.

***Optional; the user can jumper select the baud rate output from the 8253 Interval Timer instead of using those externally generated timing signals.

data to or from peripheral devices. Sixteen lines have a bidirectional driver and termination networks permanently installed. The remaining thirty-two lines are uncommitted. Sockets are provided for the installation of active driver networks or passive termination networks. The optional drivers and terminators are installed in groups of four by insertion into the 14-pin sockets.

All forty-eight signal lines emanate from the I/O ports on two Intel®8255 Programmable Peripheral Interface devices, as shown on sheet 4 of the SBC 80/20 schematic (Appendix A). The two 8255 devices allow for a wide variety of I/O configurations. Before describing the possible configurations, however, we will summarize the general operational characteristics of the 8255 device.

3.8.1 INTEL®8255 OPERATIONAL SUMMARY

The 8255 contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255.

<u>Port A</u>: One 8-bit data output latch/buffer and one 8-bit data input latch.

<u>Port B</u>: One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

<u>Port C</u>: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control.

Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with Ports A and B.

The 8080 CPU dictates the operating characteristics of the ports by outputting two different types of control words to the 8255:

1) mode definition control word (bit 7 = 1)

2) port C bit set/reset control word (bit 7 = 0)

Bit 7 of each control word specifies its format, as shown in Figures 3-15 and 3-16, respectively.

Mode Selection

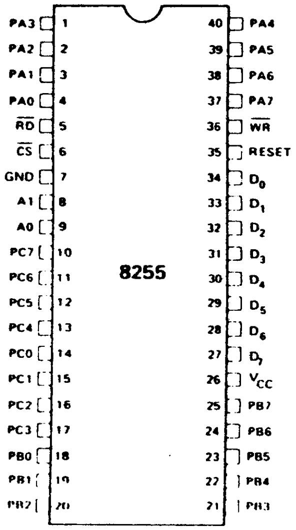
There are three basic modes of operation that can be selected by the system software:

Mode 0 - Basic Input/output
Mode 1 - Strobed Input/output
Mode 2 - Bi-directional Bus

When the RESET input goes "high" all ports will be set to the Input mode 0 (i.e., all 24 lines will be in the high impedance state). After the RESET is removed the 8255 can remain in the Input mode with no additional initialization required. During the execution of the system program, the other modes may be selected using a single OUTput instruction. This allows a single 8255 to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A

PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	Ø VOLTS

FIGURE 3-14. 8255 PIN ASSIGNMENTS

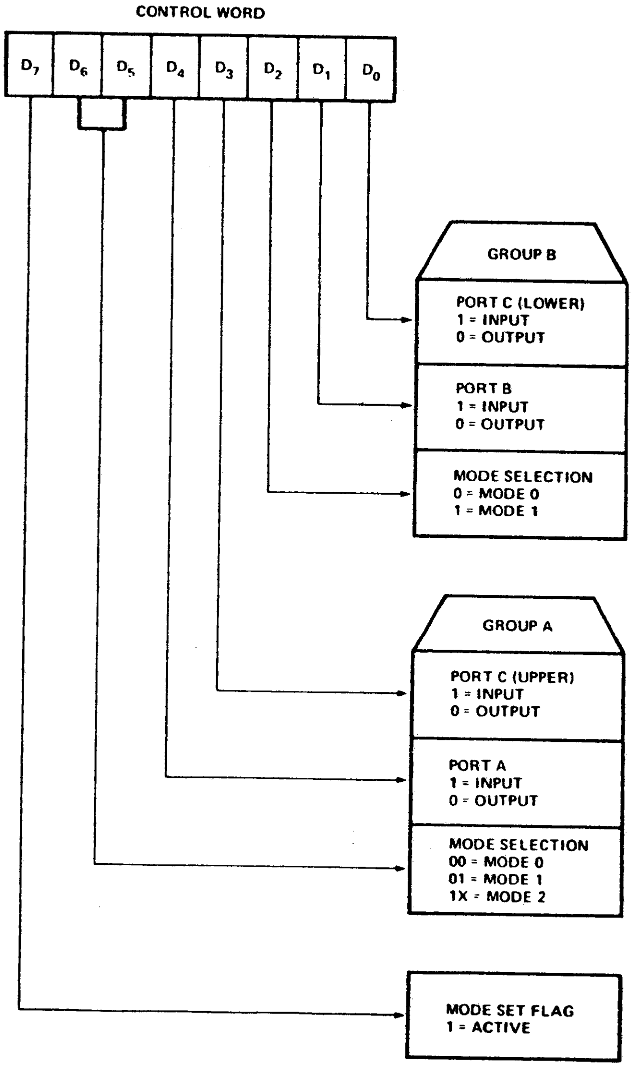


FIGURE 3-15. MODE DEFINITION CONTROL WORD FORMAT

and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed except for $\overline{\text{OBF}}$ in modes 1 and 2. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

Single Bit Set/Reset Feature

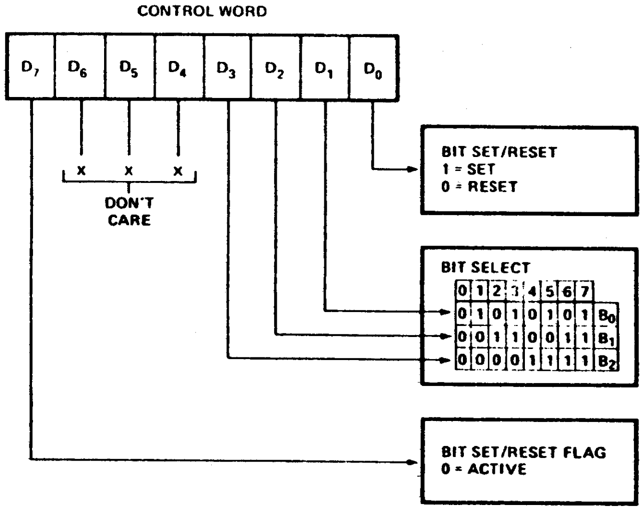
Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction (see Figure 3-16). This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255 is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the Bit set/reset function of Port C.

This function allows the Programmer to disallow or allow specific I/O devices to interrupt the CPU without effecting any other



0	1	2	3	4	5	6	7	
0	1	0	1	0	1	0	1	B_0
0	0	1	1	0	0	1	1	B_1
0	0	0	0	1	1	1	1	B_2

FIGURE 3-16. BIT SET/RESET CONTROL WORD FORMAT

device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) - INTE is SET - Interrupt enable
(BIT-RESET) - INTE is RESET - Interrupt disable

Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

Mode 0 (Basic Input/Output):

This functional configuration provides simple Input and Output operations for each of the three ports. No "hand-shaking" is required, data is simply written to or read from a specified port. Mode 0 timing is illustrated in Figure 3-17.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.

- Any port can be input or output.

- Outputs are latched.

- Inputs are not latched.

- 16 different Input/Output configurations are possible in this Mode.

Figure 3-18 shows two possible configurations.

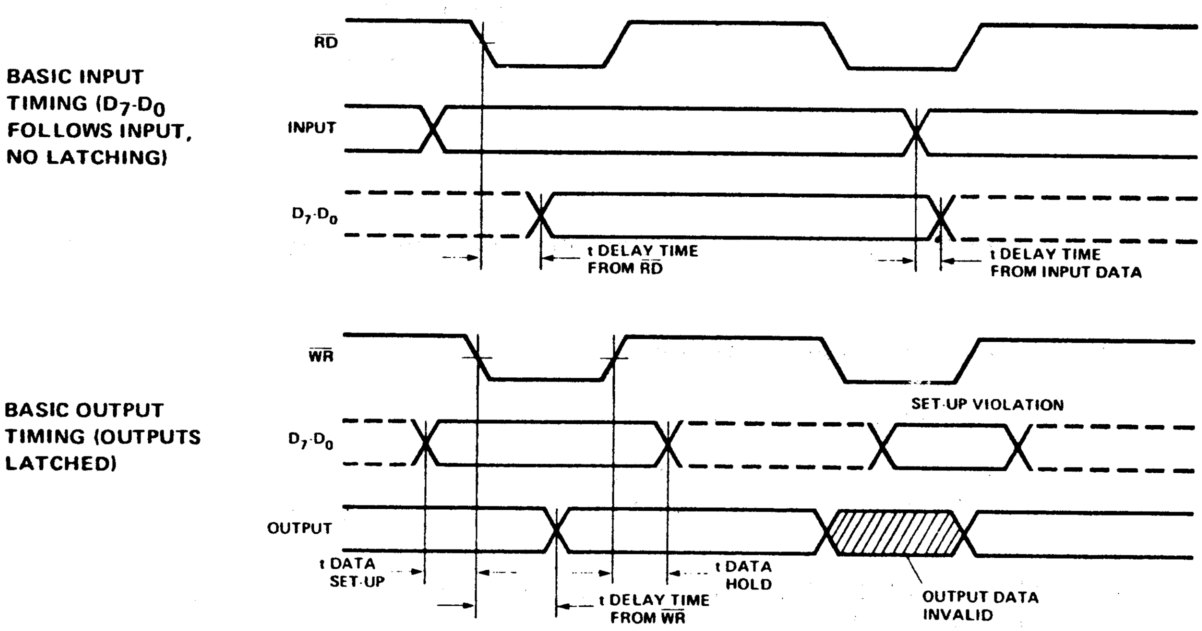


FIGURE 3-17. 8255 MODE 0 TIMING

Mode 1 (Strobed Input/Output):

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

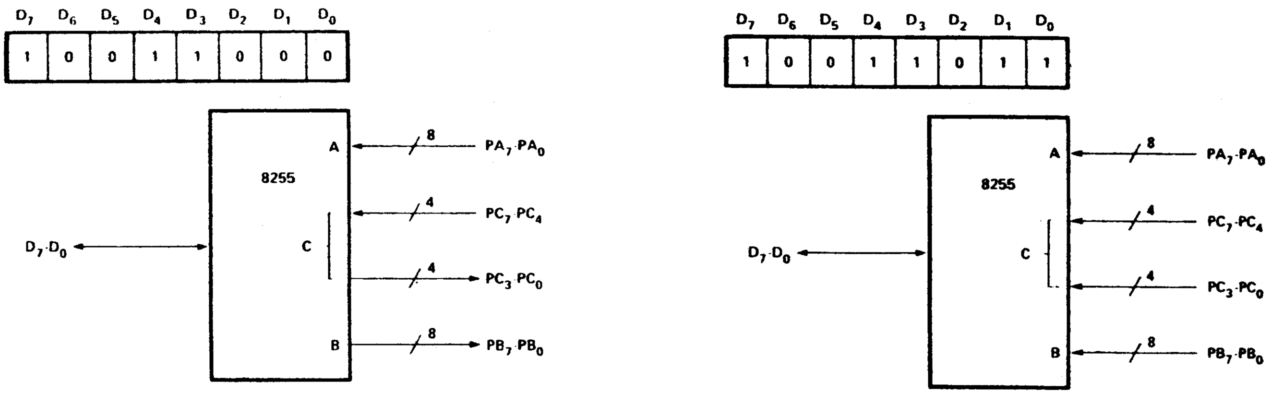


FIGURE 3-18. EXAMPLES OF MODE 0 CONFIGURATION

Mode 1 Basic Functional Definitions:

- Two transfer ports (A and B).
- Each transfer port contains one 8-bit data port and 4 bits from one half of the control/data port (Port C).
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.

Input Control Signal Definition for Mode 1

$\overline{\text{STB}}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by the falling edge of the STB input and is reset by the rising edge of the $\overline{\text{RD}}$ input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the rising edge of $\overline{\text{STB}}$ if IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{\text{RD}}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC4.

INTE B

Controlled by bit set/reset of PC2.

Figure 3-19 illustrates the Mode 1 input configuration, while Figure 3-20 shows the basic timing for Mode 1 input.

Output Control Signal Definition for Mode 1

$\overline{\text{OBF}}$ (Output Buffer Full F/F)

The $\overline{\text{OBF}}$ output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the $\overline{\text{WR}}$ input and reset by the falling edge of the $\overline{\text{ACK}}$ input signal.

$\overline{\text{ACK}}$ (Acknowledge Input)

A "low" on this input informs the 8255 that the data from Port A or Port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when

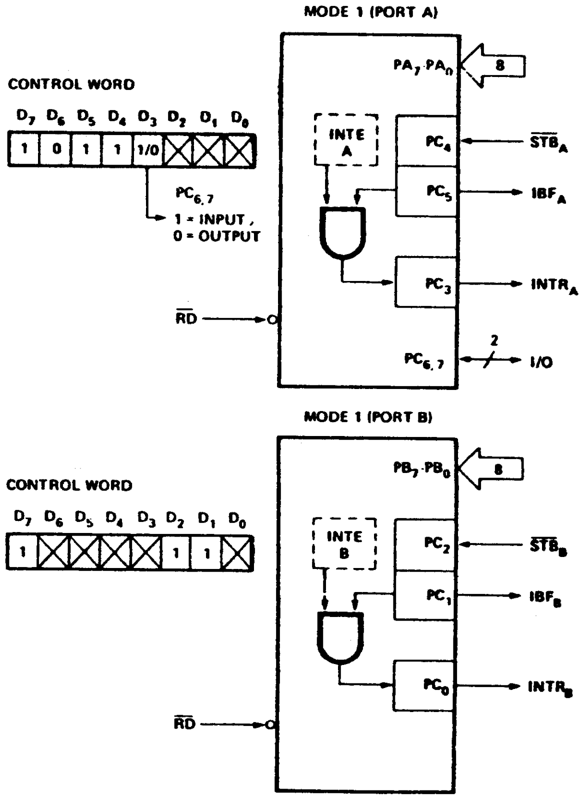


FIGURE 3-19. MODE 1 INPUT CONFIGURATION

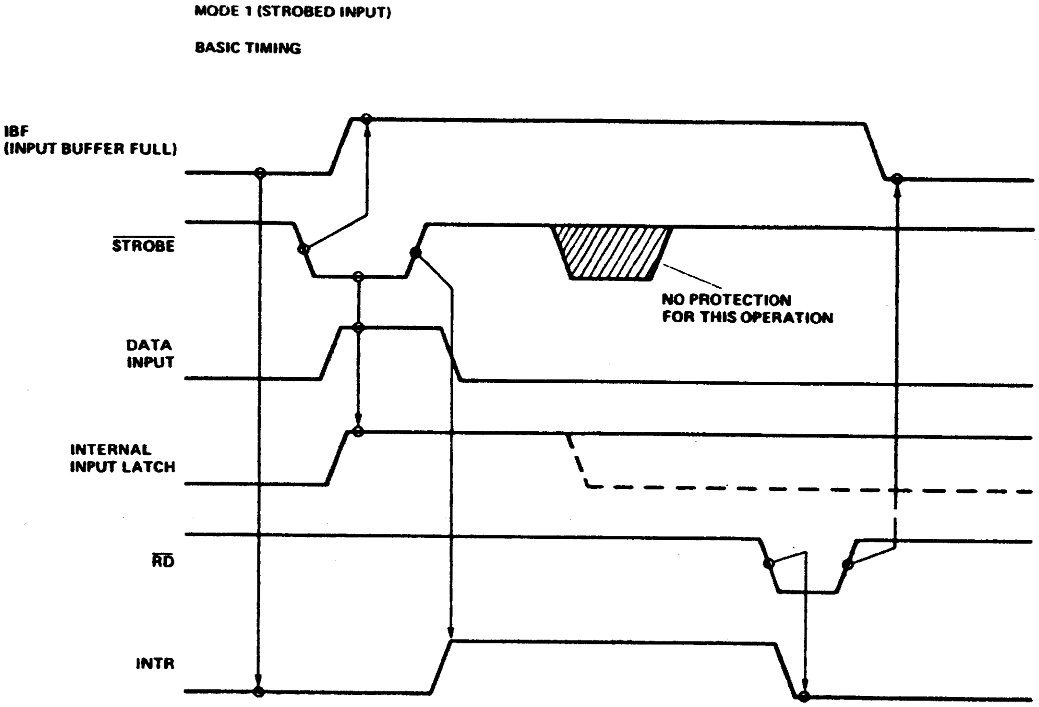


FIGURE 3-20. 8255 MODE 1 INPUT TIMING

an output device has accepted data transmitted by the CPU. INTR is set by the rising edge of $\overline{\text{ACK}}$ if $\overline{\text{OBF}}$ is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{\text{WR}}$.

INTE A

Controlled by bit set/reset of PC6.

INTE B

Controlled by bit set/reset of PC2

Figure 3-21 illustrates the Mode 1 output configuration, while Figure 3-22 shows basic Mode 1 output timing.

Mode 2 (Strobed Bi-Directional Bus I/O):

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Port A only.
- One 8-bit, bi-directional data Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional data port (Port A).

Bi-Directional Bus I/O Control Signal Definition

INTR (Interrupt Request)

A high on this output can be used to interrupt the CPU for both

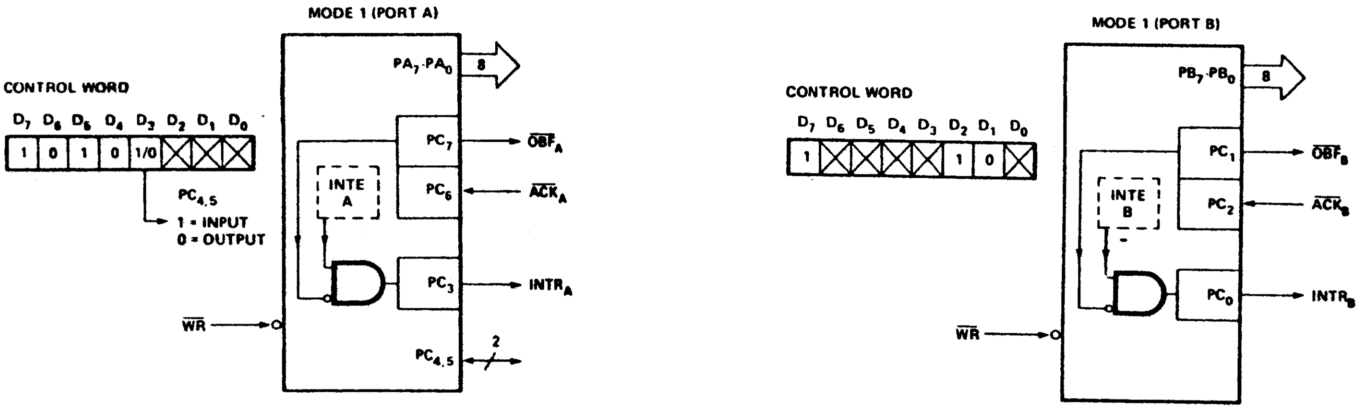


FIGURE 3-21. MODE 1 OUTPUT CONFIGURATION

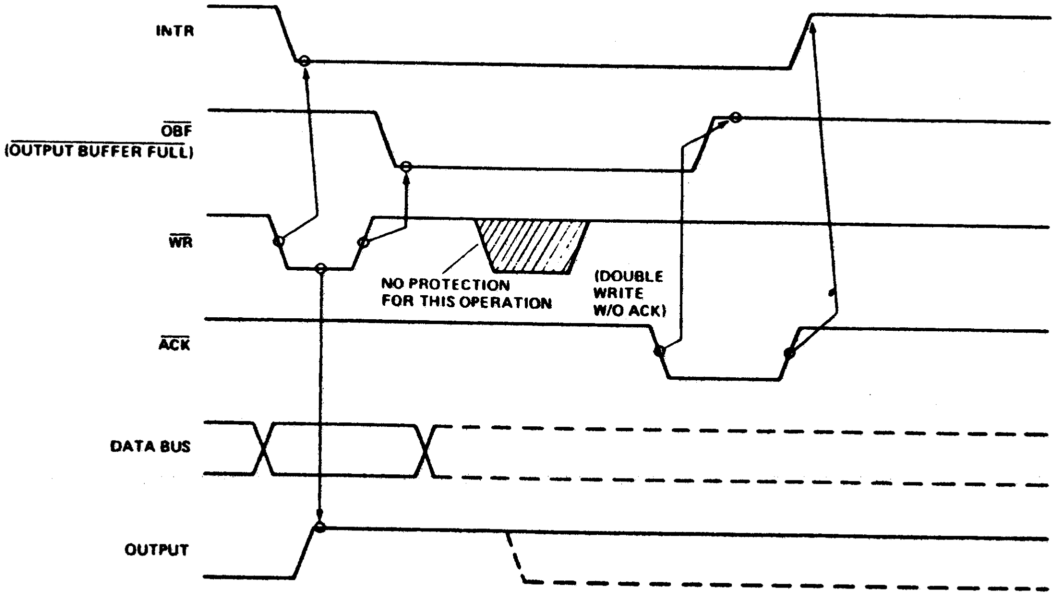


FIGURE 3-22. MODE 1 BASIC OUTPUT TIMING

input or output operations.

Output Operation Control Signals

$\overline{\text{OBF}}$ (Output Buffer Full)

The $\overline{\text{OBF}}$ output will go "low" to indicate that the CPU has written data out to Port A.

$\overline{\text{ACK}}$ (Acknowledge)

A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high-impedance state.

INTR A and B (The INTE flip-flop associated with $\overline{\text{OBF}}$)

Controlled by bit set/reset of PC6 (INTE1)

Input Operation Control Signals

$\overline{\text{STB}}$ (Strobed Input)

A "low" on this input indicates that data has been loaded into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE flip-flop associated with IBF)

Controlled by bit set/reset PC4 (INTE 2)

$$\text{INTR}_A = \text{PC6} \cdot \text{OBF}_A + \text{PC4} \cdot \text{INF}_A$$

Figure 3-23 illustrates the port configuration for Mode 2, Figure 3-24 shows Mode 2 timing, and Table 3-5 summarizes 8255 Mode definition.

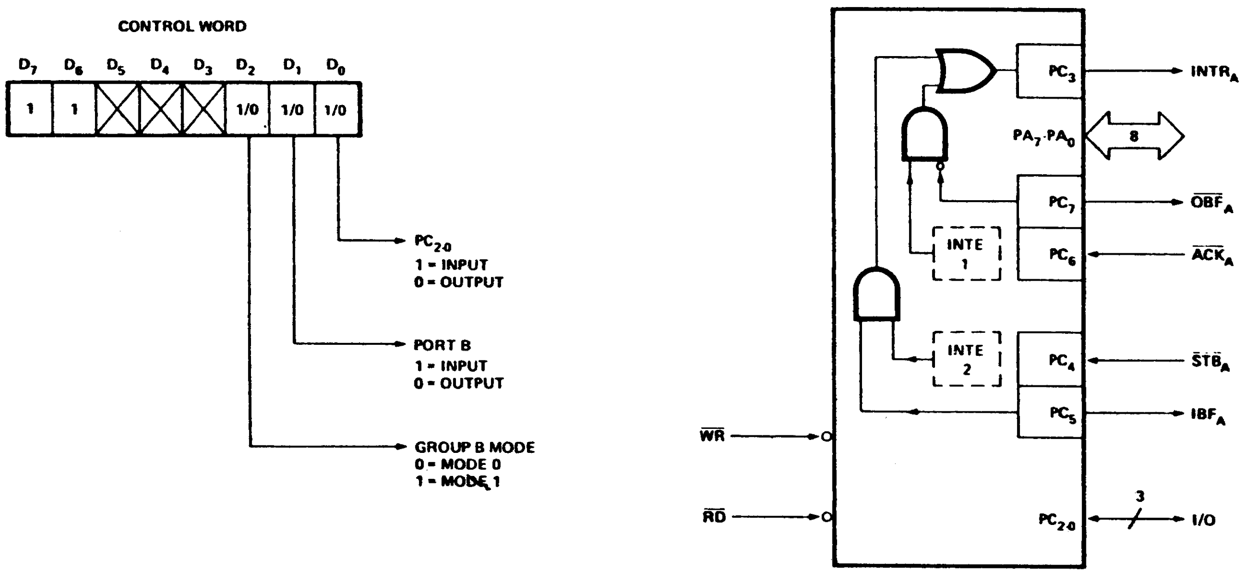


FIGURE 3-23. MODE 2 PORT CONFIGURATION

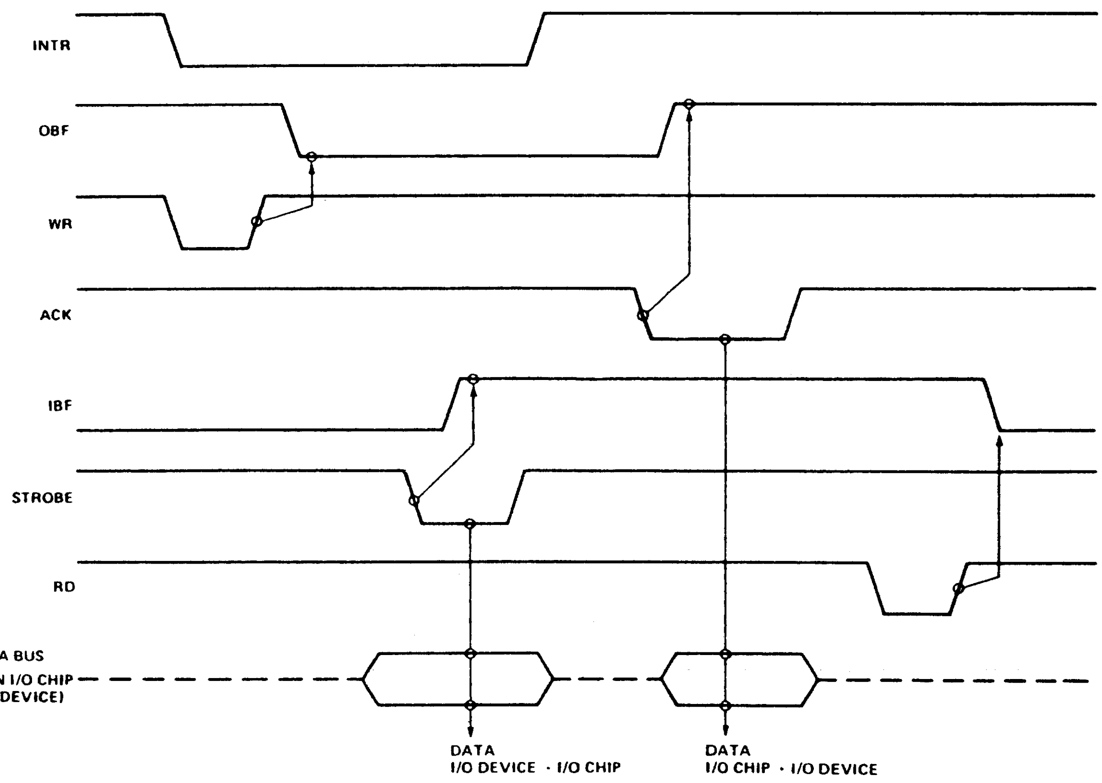


FIGURE 3-24. MODE 2 TIMING

MODE DEFINITION SUMMARY TABLE

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	←→	
PA_1	IN	OUT	IN	OUT	←→	
PA_2	IN	OUT	IN	OUT	←→	
PA_3	IN	OUT	IN	OUT	←→	
PA_4	IN	OUT	IN	OUT	←→	
PA_5	IN	OUT	IN	OUT	←→	
PA_6	IN	OUT	IN	OUT	←→	
PA_7	IN	OUT	IN	OUT	←→	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

TABLE 3-5. 8255 MODE DEFINITION SUMMARY

3.8.2 PARALLEL I/O CONFIGURATIONS

Referring to sheet 4 of the schematic, we see that there are two 8255 devices, one located at A20, the other at A21. For convenience the following device designations will be used: The device at A20 is called the "group 1" device, while the device at A21 is referred to as the "group 2" device. Each device has three eight-bit ports. The "group 1" ports are designated Ports 1, 2 and 3 while the "group 2" ports are designated Ports 4, 5 and 6.

The group 1 and group 2 devices both communicate with the CPU Set using the same signal lines: the 8-bit data bus, DB0-DB7, and seven control/address lines; ABØ, AB1, RST, IOR/, IOWT, PB47/ and PE8B/. The data lines bring control bytes or data bytes to an 8255 or deliver data from an 8255 to the CPU Set. The chip select control signals (PE47/ and PE8B/) select the group 1 and group 2 devices, respectively, when the proper I/O address appears on the system address bus. PE47/ and PE8B/ are the result of decoding address bits 2 through 7 (AB2-AB7), as described in Section 3.6. The two least significant address bits select the control register (when programming an 8255) or one of the three I/O ports (when reading or writing data). IOR/ (8255 → CPU Set) and IOWT/ (CPU Set → 8255) indicate the direction of data flow, as summarized in Table 3-6. Specific I/O addresses for the six ports and two 8255 control registers on the SBC 80/20 are listed in Table 3-7.

A high on the RST line clears all internal 8255 registers including the control register; all ports (A, B and C) are set for input.

TABLE 3-6. 8255 BASIC OPERATION

A1	A0	IOR/	IOW/	CS/	Input Operation (Read)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
					Output Operation (Write)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					Disable Function
x	x	x	x	1	Data Bus → High-Impedance
1	1	0	1	0	Illegal

TABLE 3-7. PARALLEL I/O PORT ADDRESSES

Port	8255 Device Location	*Eight-Bit Address (Hexadecimal)
1	8255 #1 Port (A)	E4
2	8255 #1 Port (B)	E5
3	8255 #1 Port (C)	E6
-	8255 #1 Control	E7 For I/O write only
4	8255 #2 Port (A)	E8
5	8255 #2 Port (B)	E9
6	8255 #2 Port (C)	EA
-	8255 #2 Control	EB For I/O write only

*Note: If address = 111001xx, PE47/ is activated.
If address = 111010xx, PE8B/ is activated.

Both parallel interface groups, 1 and 2, have the same interface characteristics with respect to the system bus. They are also both capable of the same range of configurations with respect to their peripheral interfaces. The only functional difference between group 1 and group 2 is that the two gate/trigger/reset lines (ITGO and and ITG1) associated with counters 0 and 1 in the 8253 Interval Timer can be made available to Port 3 (Port C of group 1), while four signal lines associated with the serial interface can be made available to Port 6 (Port C of group 2), via wire wrap jumper pins. Three of those serial I/O signals are RS232 inputs, which cannot be sampled by the user through the USART. They can, however, be connected by jumper to unused Port 6 bits and read through Port 6. The fourth serial I/O line allows the user to drive one of the serial I/O interface output signals by setting a bit in Port 6. Details regarding the use of the C ports by the serial interface and the interval timer are provided in Sections 3.7 and 3.9, respectively.

The operating characteristics of each port are determined by the mode and direction control information supplied by the CPU in its control word. In addition, certain mode/port relationships impose restrictions on the use of other ports in the group. These mode-related characteristics and restrictions are discussed briefly below. Details regarding mode implementation and the associated inter-port restrictions are presented in Chapter 4, User Selectable Options.

Because the two groups are functionally identical, we will refer to the ports as A, B or C. Statements made about Port A apply equally to Ports 1 and 4, statements made about Port B refer to Ports 2 and 5, and statements made about Port C refer to Ports 3 and 6. Where specific details are related (such as jumper connections), the information will be identified as applying to group 1 (Ports 1, 2 or 3) or group 2 (Ports 4, 5 or 6). The reader should keep in mind, however, that the peripheral interface consists of two sets of equally versatile ports, which are independently programmed.

The allowable port configurations for either group are summarized below:

Ports 1 and 4 (Port A)

Mode 0 Input
Mode 0 Output (Latched)
Mode 1 Input (Strobed)
Mode 1 Output (Latched)
Mode 2 Bidirectional

Ports 2 and 5 (Port B)

Mode 0 Input
Mode 0 Output (Latched)
Mode 1 Input (Strobed)
Mode 1 Output (Latched)

Ports 3 and 6 (Port C)

Mode 0 8 Bit Input
Mode 0 8 Bit Output (Latched)
Mode 0 Split 4 bit input and 4 bit output

Note: Control mode dependent upon Port A and B mode.

Port A is the most versatile of the three ports. It can be programmed to function in any one of the three 8255 operating modes. This first port is the only port in each group that already includes a permanent bidirectional driver/termination network, 8226 bus driver devices at A1 and A2 (group 1) and A7 and A8 (group 2).

Before Port A is programmed for input or output in any one of three operating modes (as described in Section 3.8.1), certain jumper connections must be made to allow the port to function properly in the chosen mode. The 51-52-53 (group 1) or 70-71-72 (group 2) jumper pad specifies the direction of data flow for the two 8226 bidirectional bus drivers. If input in mode 0 or mode 1 is to be programmed for Port A, jumper pair 51-52 (group 1) or 70-71 (group 2) should be connected. If output in mode 0 or mode 1 is to be used, jumper pair 52-53 (group 1) or 71-72 (group 2) should be connected. If Port A is to be programmed for bidirectional mode 2, then a wire can be run from jumper pin 52 to pin 57 (group 1) or pin 71 to pin 76. This connection allows the Port C acknowledge output ACK/, which is available at bit 6 of Port C, to dynamically dictate direction for the two 8226 devices.

When Port A is programmed for mode 1 or mode 2, interrupts can be used. The INTR output from bit 3 of Port C activates the peripheral I/O interrupt request, PIA1 or PIA2. PIA1 and PIA2 are forwarded to the interrupt logic (see Section 3.10).

Because the 8226 bus drivers are inverting devices, all data input to or output from Port 1 or Port 4 is considered to be negative true with respect to the levels at the J1 or J2 edge connector.

Port B can be programmed for input or output in either mode 0 or mode 1 (see Section 3.8.1). If Port B is to be used for input (in either mode), terminator networks must be installed in the sockets at A5 and A6 (group 1) or A11 and A12 (group 2). Because of the passive nature of termination networks, data that is input to Port B must be positive true. If Port B is to be used for output (in either mode), driver networks must be installed in the sockets at A5 and A6 or A11 and A12. Assuming that the drivers are inverting devices, then the data being output will be negative true at the J1 or J2 edge connector.

When Port B is programmed for mode 1, interrupts can be used. The INTR output from bit 0 of Port C activates the peripheral I/O interrupt request PIB1 or PIB2. PIB1 and PIB2 are forwarded to the interrupt logic (see Section 3.10).

As was described in Section 3.8.1, the use of Port C depends on the modes programmed for Ports A and B. If Port A is in mode 1 or mode 2, bits 3, 4, 5, 6 and 7 of Port C can have the following dedicated control functions.

Port C bit 3	→ INTR	(interrupt request)	- input or output
Port C bit 4	← STB/	(input strobe)	mode 1 input or mode 2
Port C bit 5	→ IBF	(input buffer full flag)	
Port C bit 6	← ACK/	(output acknowledge)	mode 1 output or mode 2
Port C bit 7	→ OBF/	(output buffer full flag)	

If Port B is in mode 1, bits 0, 1 and 2 of Port C have these dedicated control functions:

Port C bit 0	→ INTR	(interrupt request)	- input or output
Port C bit 1	→ IBF	(input buffer full)	input only
Port C bit 2	← STB/	(input strobe)	
Port C bit 1	→ OBF/	(output buffer full)	output only
Port C bit 2	← ACK/	(output acknowledge)	

While certain Port C bits are available if Port A is in mode 1 or if Port B is in mode 0, the use of Port C as an eight-bit data path is restricted to those configurations that have both Port A and Port B programmed for mode 0. In this case all 8 bits of Port C can be programmed for mode 0 input (termination networks must be installed in the sockets at A3 and A4 for group 1 or A9 and A10 for group 2 or output (driver networks must be installed at A3 and A4 or A9 and A10) or split 4 bits input and 4 bits output.

Note: If Port A and B are not both in mode 0, then a driver network should be installed in the sockets at A3 or A9 and a termination network must be installed at A4 or A10, so that the Port C control lines can function properly.

3.9 INTEL® 8253 PROGRAMMABLE INTERVAL TIMER

The SBC 80/20 includes an 8253 Programmable Interval Timer, as shown at A22 on sheet 5 of the SBC 80/20 schematic (Appendix A). The 8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the 8253 to match his requirements, initializes one of the counters of the 8253 with the desired quantity, then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253.

- Programmable Baud Rate Generator
- Event Counter

- Binary Rate Multiplier
- Real Time Clock
- Programmable One-Shot
- Complex Motor Controller

Before describing how the 8253 has been configured within the SBC 80/20 system, however, we will summarize the general operating characteristics of the 8253 device.

3.9.1 INTEL®8253 OPERATIONAL SUMMARY

The 8253 includes three separate counters (refer to Figure 3-25). Each counter is a single, 16-bit, pre-settable, DOWN counter. Each counter can operate in either binary or BCD and its input, gate and output are configured by the selection of functions stored in the Control Word Register and jumper configurations on the SBC 80/20.

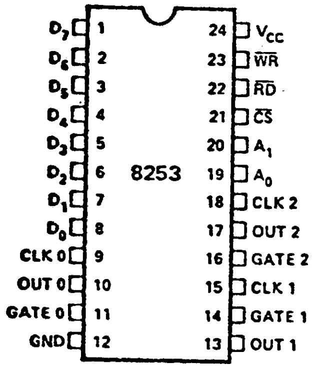
The counters are fully independent and each can have separate Mode configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

The complete functional definition of the 8253 is programmed by the systems software. A set of control words must be sent out

8253

PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (8 BIT)
CLK N	COUNTER CLOCK INPUTS
GATE N	COUNTER GATE INPUTS
OUT N	COUNTER OUTPUTS
$\overline{RD}$	READ COUNTER
$\overline{WR}$	WRITE COMMAND OR DATA
$\overline{CS}$	CHIP SELECT
A_0-A_1	COUNTER SELECT
V_{CC}	+5 VOLTS
GND	GROUND

BLOCK DIAGRAM

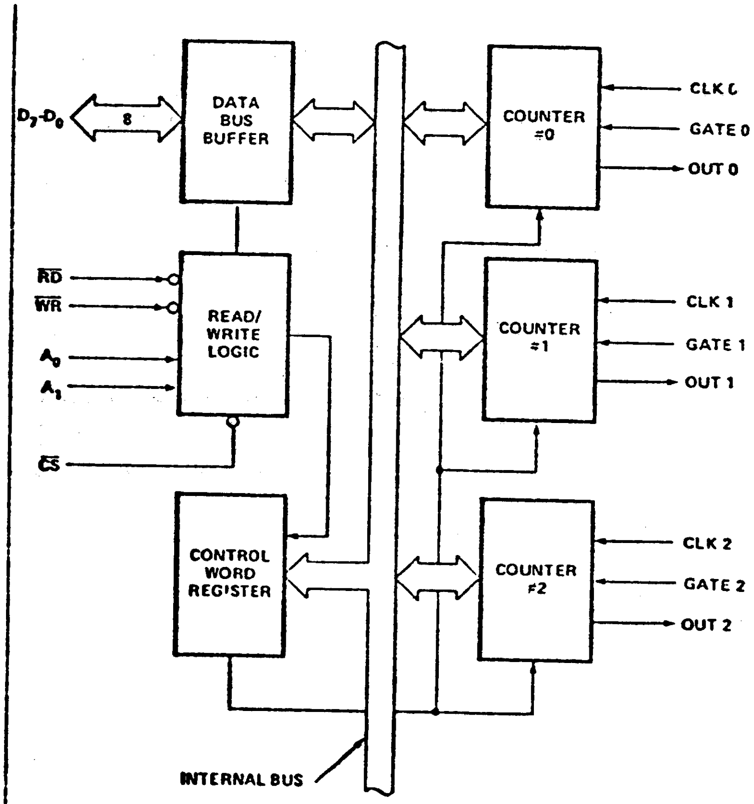


FIGURE 3-25. 8253 FUNCTIONAL DIAGRAM

by the CPU to initialize each counter of the 8253 with the desired function and quantity information. These control words program the function. Loading sequence and selection of binary or BCD counting. Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

Programming the 8253

All of the functions for each counter are programmed by the systems software by simple I/O operations. Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register. (A0, A1 = 11).

Control Word Format:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	0	M1	M0	BCD

Definition of Control Fields:

SC-Select Counter Bits

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL-Read/Load Bits

RL1	RL0	
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.
0	0	latch counter

M-MODE (Function) Bits

M1	M0	
0	0	Mode 0
0	1	Mode 1
1	0	Mode 2
1	1	Mode 3

BCD Selection Bit

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

MODE (Function) Definition:

MODE 0: Interrupt on Terminal Count

The 8253 counter output will be initially low after the Mode set operation. After the count is loaded into the selected count register, the Output will remain low and the counter to count. When terminal count is reached the Output will go high and remain high until the selected count register is reloaded, or the Mode set again.

Reloading a counter register during counting will restart the procedure. The Gate input will enable the counting when high and inhibit counting when low.

MODE 1: Programmable One-Shot

The Output will go low on the count following the rising edge of the Gate/Trigger input (there is no count gate in this Mode).

The Output will go high on the terminal count. If a new count value is loaded while the Output is low it will not affect the duration of the One-Shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

Mode 2: Rate Generator

Divide by N counter. The Output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The Gate/Reset input, when low, will force the Output high. When the Gate/Reset input goes high, the counter will start from the initial count. Thus, the Gate/Reset input can be used to synchronize the counter.

When this MODE is set, the output will remain high until after the count register is loaded. The Output then can also be synchronized by software.

Mode 3: Square Wave Rate Generator

Similar to MODE 2 except that when the Gate/Reset input goes high and the count register has been loaded, the OUTput will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. If the count is odd, the Output will be high for (N+1)/2 counts and low for (N-1)/2 counts.

Figure 3-26 illustrates the timing sequence generated by each mode. Table 3-8 summarizes the use of the GATE/TRIGGER/RESET pin for each of the four modes.

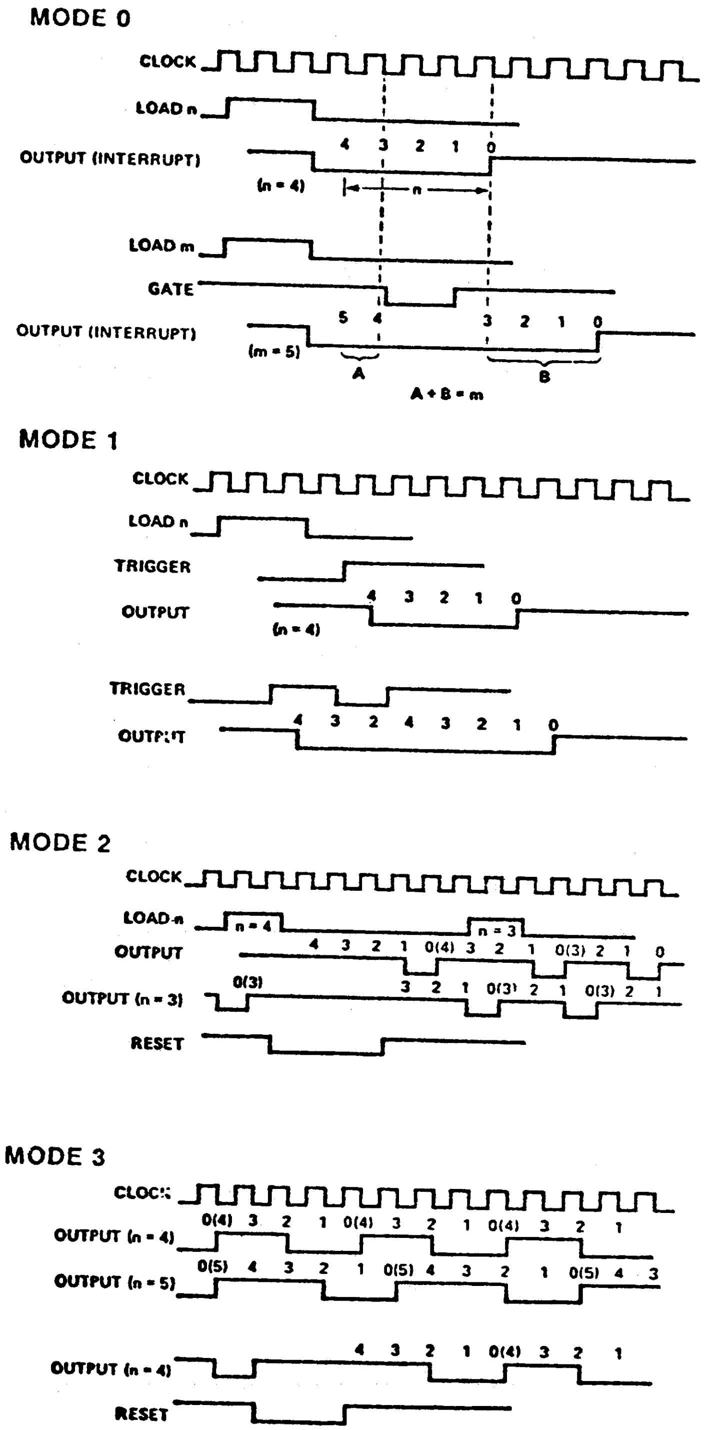


FIGURE 3-26. 8253 TIMING DIAGRAMS

TABLE 3-8. GATE/TRIGGER/RESET - PIN OPERATIONS

Signal Status / Modes	Low Or Going Low	Rising	High
0	Disables counting	---	Enables counting
1	---	1) Initiates counting 2) Resets output after next clock	---
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting

Write Operations

The systems software must program each counter of the 8253 with the mode and quantity desired. The programmer must write out to the 8253 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent (SC0, SC1).

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RLO, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it must be loaded with the number of bytes programmed in the MODE control word (RLO, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeroes into a count register will result in the maximum count (2^{16} for Binary or 10^{4} for BCD). In MODE 0 the count will not restart until the load has been completed. It will accept one or two bytes depending on how the MODE control words (RLO, RL1) are programmed. Then proceed with the restart operation.

Figure 3-27 illustrates a programming format for the 8253.

Read Operations

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The 8253 contains logic that will allow the programmer to easily read the contents of any of the

Programming Format

	MODE Control Word Counter n
LSB	Count Register byte Counter n
MSB	Count Register byte Counter n

Note: Format shown is a simple example of loading the 8253 and does not imply that it is the only format that can be used.

Alternate Programming Formats

Example:

			A1	A0
No. 1		MODE Control Word Counter 0	1	1
No. 2		MODE Control Word Counter 1	1	1
No. 3		MODE Control Word Counter 2	1	1
No. 4	LSB	Count Register Byte Counter 1	0	1
No. 5	MSB	Count Register Byte Counter 1	0	1
No. 6	LSB	Count Register Byte Counter 2	1	0
No. 7	MSB	Count Register Byte Counter 2	1	0
No. 8	LSB	Count Register Byte Counter 0	0	0
No. 9	MSB	Count Register Byte Counter 0	0	0

Note: The exclusive addresses of each counter's count register make the task of programming the 8253 a very simple matter, and maximum effective use of the device will result if this feature is fully utilized.

FIGURE 3-27. 8253 PROGRAMMING FORMAT EXAMPLE three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A0, A1 inputs to the 8253 the programmer can select the counter to be read (remember that no read operation of the mode register is allowed; A0, A1 = 11). The only requirement with this method is that in order to assure a stable count reading, the actual operation of the selected counter must be inhibited either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows:

- First I/O Read contains the least significant byte (LSB).
- Second I/O Read contains the most significant byte (MSB).

DUE TO THE INTERNAL LOGIC OF THE 8253 IT IS ABSOLUTELY NECESSARY TO COMPLETE THE ENTIRE READING PROCEDURE. If two bytes are programmed to be read then two bytes must be read before any loading WR command can be sent to the same counter.

Read Operation Chart:

A1	A0	RD	
0	0	0	Read Counter No. 0
0	1	0	Read Counter No. 1
1	0	0	Read Counter No. 2
1	1	0	Illegal

Reading While Counting:

In order for the programmer to read the contents of any counter without effecting or disturbing the counting operation the 8253 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter "on the fly" he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter and the content of the latched register is available.

MODE Register for Latching Count

A0, A1 = 11

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 - specify counter to be latched.
D5, D4 - 00 designates counter latching operation.
X - don't care.

THE SAME RULE APPLIES TO THIS MODE OF READING THE COUNTER AS THE PREVIOUS METHOD. THAT IS, IT IS MANDATORY TO COMPLETE THE ENTIRE READ OPERATION AS PROGRAMMED.

3.9.2 TIMER CONFIGURATIONS

As previously described, the 8253 includes three 16-bit counters but only one Control Word Register. Before use, each counter must be programmed by outputting a MODE Control Word to the 8253 Control

Word Register. The select bits (SC0-SC1) within the Control Word specify which counter is to be programmed. The Control Word Register is loaded when an output instruction directed to port DF (hexadecimal) is executed (WR/ and CS/ are low and A0 and A1 are high). The Control Word Register cannot be read however.

Before using a counter, the count value must also be initialized. Because the counters are 16-bits long, two I/O instructions are required to load or read an entire register. The read/load bits (RL0-RL1) in the MODE Control Word specify whether the upper byte or lower byte is to be loaded or read by a particular instruction, as described in Section 3.9.1. Table 3-9 lists I/O addresses for accessing each register within the 8253.

Each of the three counters includes clock and gate inputs and a single output. The clock input for each counter is supplied by dividing the TTL-level phase 2 timing pulse (Ø2T) from the CPU Section by 2 (see Section 3.1.1). The clock has a period of 930 nsec. The gate inputs for counters Ø and 1, ITG0 and ITG1 respectively, are jumper-selected. They are initially tied to +5V through jumpers 93-93-95 (see Schematic sheet 4). However, these jumper connections can be deleted and ITG0 (jumper pin 93) and ITG1 (jumper pin 95) can be connected to output lines eminating from Port 3 in the Parallel I/O Interface (see Section 3.8). The user program can then dictate the levels on ITG0 and ITG1 by outputting the desired logical value to the appropriate bits of Port 3. The outputs from counter Ø (OITØ) and counter 1

TABLE 3-9. 8253 REGISTER ADDRESSES

CS	RD	WR	A_1	A_0	ACTIVITY	I/O ADDRESS (hex)
0	1	0	0	0	Load Counter No. 0	DC
0	1	0	0	1	Load Counter No. 1	DD
0	1	0	1	0	Load Counter No. 2	DE
0	1	0	1	1	Write Mode Word	DF
0	0	1	0	0	Read Counter No. 0	DC
0	0	1	0	1	Read Counter No. 1	DD
0	0	1	1	0	Read Counter No. 2	DE
0	0	1	1	1	No-Operation 3-State	DF
1	X	X	X	X	Disable 3-State	--
0	1	1	X	X	No-Operation 3-State	--

X = Don't care

(OIT1) are made available to the Interrupt controller section where they can be jumpered to one of the eight interrupt priority request lines (see Section 3.10).

Counter 2 has a dedicated function on the SBC 80/20. This counter provides a baud rate clock to the Serial I/O Interface. The output from counter 2 is made available to the 8251 USART where it can be jumper-connected to the Receive ($\overline{RXC}$) and/or Transmit ($\overline{TXC}$) clock inputs (see Section 3.7). Counter 2 is always enabled (i.e., its gate input is tied to +5V).

If the user wishes to use counter 2 to generate the baud rate clock for Serial I/O, the counter must be programmed for Mode 3

Square wave rate generation (see below), and the appropriate binary or BCD count value must be loaded into the counter to produce the desired output frequency.

Counter 2 (Baud Rate Clock) Control Word:

D7	D6	D5	D4	D3	D2	D1	D0
1	0	RL1	RL2	0	1	1	BCD

See Section 3.9.1

3.10 INTEL® 8259 PROGRAMMABLE INTERRUPT CONTROLLER

The interrupt Controller logic consists of Intel's powerful 8259 Interrupt Controller device and a jumper pad that allows the user to connect any of 27 possible interrupt requests to the 8259's eight interrupt priority inputs. The 8259 resolves priority among all eight levels according to an algorithm which is program-selected by the user. The Interrupt Controller is shown on sheet 6 of the SBC 80/20 schematic (Appendix A).

Section 3.10.1 provides a basic functional description of the 8259, Section 3.10.2 summarizes the operational characteristics of the 8259, and Section 3.10.3 describes how the Interrupt Controller is configured on the SBC 80/20.

3.10.1 8259 BASIC FUNCTIONAL DESCRIPTION

The 8259 is a device specifically designed for use in real time interrupt driven, microcomputer systems. It manages eight levels of requests and has built-in features for expandability to other 8259s (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority algorithms is available to the programmer so that the manner in which the requests are processed by the 8259 can be configured to match his system requirements. The priority assignments and algorithms can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

A functional block diagram of the 8259 is shown in Figure 3-28. The various functional blocks are described below:

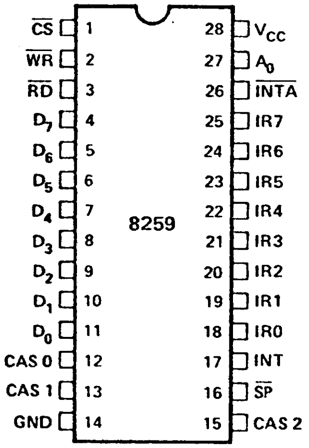
Interrupt Request Register (IRR) and In-Service Register (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

The IRR bit is set and INT line is raised high whenever there is a positive going edge at the IR input. More than one bit of the IRR can be set at once as long as they are not masked. The IRR is reset by the $\overline{\text{INTA}}$ sequence.

The ISR bit is set by the $\overline{\text{INTA}}$ pulse (at the same time the selected IRR bit is reset). This bit remains set during the subroutine until an EOI (End of Interrupt) command is received by the 8259.

8259
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
$\overline{\text{RD}}$	READ INPUT
$\overline{\text{WR}}$	WRITE INPUT
A_0	COMMAND SELECT ADDRESS
$\overline{\text{CS}}$	CHIP SELECT
CAS1-CAS0	CASCADE LINES
$\overline{\text{SP}}$	SLAVE PROGRAM INPUT
INT	INTERRUPT OUTPUT
$\overline{\text{INTA}}$	INTERRUPT ACKNOWLEDGE INPUT
IR0-IR7	INTERRUPT REQUEST INPUTS

BLOCK DIAGRAM

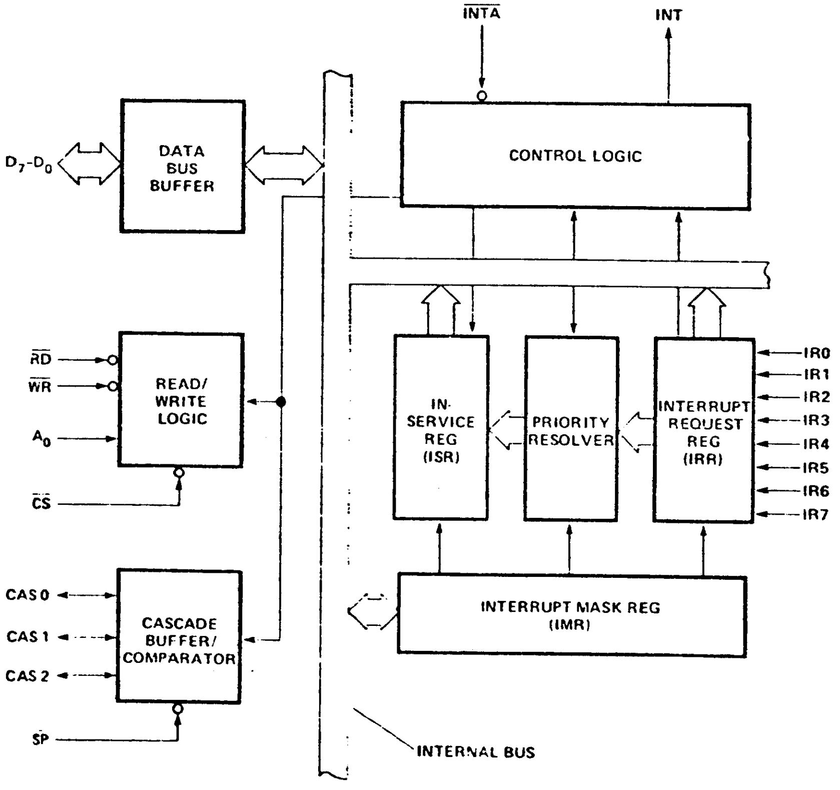


FIGURE 3-28. 8259 INTERRUPT CONTROLLER

The return from the subroutine to the main program may look like this:

```
OUT OCW2 (Send EOI command)
RET
```

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{\text{INTA}}$ pulse.

INT (Interrupt)

This output goes directly to the 8080 INT input. The VOH level on this line is designed to be fully compatible with the 8080 input level.

$\overline{\text{INTA}}$ (Interrupt Acknowledge)

This input generally comes from the 8238 of the CPU group. The 8238 will produce 3 distinct $\overline{\text{INTA}}$ pulses. The 3 INTA pulses will cause the 8259 to release a 3-byte CALL instruction onto the Data Bus. This CALL instruction is used to vector the CPU to the proper interrupt service routine as given by the priority algorithm and interrupt request conditions at the time.

Interrupt Mask Register (IMR)

The IMR stores the bits of the interrupt lines to be masked. The IMR operates on both the IRR and the ISR. Masking of a higher priority bit will not affect the interrupt request lines of lower priority.

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8259 to the 8080 system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

Read/Write Control Logic

The function of this block is to accept input commands from the 8080. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 8259 to be transferred onto the 8080 Data Bus.

$\overline{\text{CS}}$ (Chip Select)

A "low" on this input enables the 8259. No reading or writing of the chip will occur unless the device is selected.

$\overline{\text{WR}}$ (Write)

A "low" on this input enables the 8080 CPU to write control words (ICWs and OCWs) to the 8259.

$\overline{\text{RD}}$ (Read)

A "low" on this input enables the 8259 to send the status of the interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR) or the BCD of the interrupt level on to the Data Bus.

A0

This input signal is used in conjunction with $\overline{\text{WR}}$ and $\overline{\text{RD}}$ signals to write commands into the various command registers as well as reading the various status registers of the chip. This line can be tied directly to one of the 8080 address lines.

$\overline{\text{SP}}$ (Slave Program)

More than one 8259 can be used in the system to expand the priority interrupt scheme up to 64 levels. In such case, one 8259 acts as the master, and the others act as slaves. A "high" on the $\overline{\text{SP}}$ pin designates the 8259 as the master, a "low" designates it as a slave.

The Cascade Buffer/Comparator

This function block stores and compares the IDs of all 8259 used in the system. The associated three I/O pins (CASO-2) are outputs when the 8259 is used as a master ($\overline{\text{SP}}$ = 1), and are inputs when the 8259 is used as a slave ($\overline{\text{SP}}$ = 0). As a master, the 8259 sends the ID of the interrupting slave device onto the CASO-2 lines. The slave thus selected will send its preprogrammed subroutine addresses onto the Data Bus during next two consecutive $\overline{\text{INTA}}$ pulses.

3.10.2 8259 DETAILED OPERATIONAL SUMMARY

The powerful features of the 8259 in the 8080 microcomputer system are its programmability and its utilization of the 8080 CALL instruction to jump into any address in the memory map. The normal sequence of events that the 8259 interacts with the CPU is as follows:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high signaling the 8259 that the peripheral equipment(s) are demanding service.

2. The 8259 accepts these requests, resolves the priorities, and sends an INT to the 8080 CPU.

3. The 8080 CPU acknowledges the INT and responds with an $\overline{\text{INTA}}$ pulse.

4. Upon receiving the $\overline{\text{INTA}}$ from the CPU group (8238), the 8259 will release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7-0 pins.

5. This CALL instruction will initiate two more $\overline{\text{INTA}}$ pulses to be sent to the 8259 from the CPU group (8238).

6. These two $\overline{\text{INTA}}$ pulses allow the 8259 to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{\text{INTA}}$ pulse and the higher 8-bit address is released at the second $\overline{\text{INTA}}$ pulse.

7. This completes the 3-byte CALL instruction released by the 8259. The In-Service Register (ISR) is not reset until the end of the subroutine when an EOI (End of interrupt) command is issued to the 8259.

Programming the 8259

The 8259 accepts two types of command words generated by the CPU:

1. Initialization Command Words (ICWs):

   Before normal operation can begin, each 8259 in the system must be brought to a starting point--by a sequence of 2 or 3 bytes timed by $\overline{\text{WR}}$ pulses. This sequence is shown in Figure 3-29.

2. Operation Command Words (OCWs):

   These are the command words which command the 8259 to operate in various interrupt modes. These modes are:

   a. Fully nested mode

   b. Rotating priority mode

   c. Specific Priority mode

   d. Polled mode

The OCWs can be written into the 8259 at anytime during system operation.

Initialization Command Words 1 and 2: (ICW1 and ICW2)

Whenever a command is issued with A0 = 0 and D4 = 1 this is interpreted as Initialization Command Word 1 (ICW1), and initiates the initialization sequence. During this sequence, the following occur automatically:

a. The edge sense circuit is reset, which means that following initialization, and interrupt request (IR) input must make a low to high transition to generate an interrupt.

b. The interrupt Mask Register is cleared.

c. IR 7 input is assigned priority 7.

d. Special Mask Mode Flip-flop and status Read Flip-flop are reset.

Initialization Command Word 2 (ICW2) must be output right after ICW1. ICW1 provides two control bits and 2 or 3 of the interrupt CALL address bits. ICW2 provides 8 of the CALL address bits, as shown below.

The 8 requesting devices have 8 addresses equally spaced in memory. The addresses can be programmed at intervals of 4 or 8 bytes: the 8 routines thus occupying a page of 32 or 64 bytes respectively in memory.

The address format is:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

$$\underbrace{A_7 \quad A_6}_{\text{Defined by } D_{5-7} \text{ of ICW1}} \quad A_5 \quad \underbrace{A_4 \quad A_3 \quad A_2 \quad A_1 \quad A_0}_{\text{Automatically inserted by 8259}}$$

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8

Defined by ICW2

A0-4 are automatically inserted by the 8259, while A15-6 are programmed by ICW1 and ICW2. When interval = 8, A5 is fixed by the 8259. If interval = 4, A5 is programmed in ICW1. Thus, the interrupt service routines can be located anywhere in the memory space. The 8 byte interval will maintain compatibility with current 8080 RESTART instruction software, while the 4 byte interval is best for a compact jump table.

The address format inserted by the 8259 is described in Table 3-10.

The bits F and S are defined by ICW1 as follows:

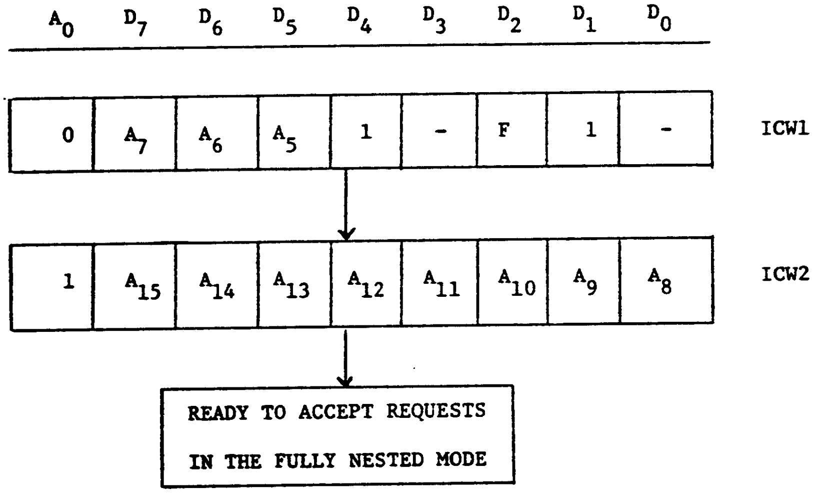
F: Call address interval. F = 1, then interval = 4; F = 0, then interval = 8.

S: Single. S = 1 means that this is the only 8259 in the system. It avoids the necessity of programming ICW3. As used on the SBC 80/20, this bit must always be set to a 1 since only one 8259 is allowed.

Example of Interrupt Acknowledge Sequence

Assume the 8259 is programmed with F = 1 (CALL address interval = 4), and IR5 is the interrupting level. The 3 byte sequence released by the 8259 timed by the $\overline{\text{INTA}}$ pulses is as follows:

	D7	D6	D5	D4	D3	D2	D1	D0	
1st $\overline{\text{INTA}}$	1	1	0	0	1	1	0	1	Call Instruction Code
2nd $\overline{\text{INTA}}$	A7	A6	A5	1	0	1	0	0	Lower Routine Address
3rd $\overline{\text{INTA}}$	A15	A 14	A13	A12	A11	A10	A9	A8	Higher Routine Address



A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	A_7	A_6	A_5	1	-	F	1	-	ICW1
1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	ICW2

READY TO ACCEPT REQUESTS
IN THE FULLY NESTED MODE

FIGURE 3-29. INITIALIZATION SEQUENCE
AS APPLICABLE TO SBC 80/20 IMPLEMENTATION

	INTERVAL = 4								INTERVAL = 8							
	LOWER MEMORY ROUTINE ADDRESS															
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
IR 7	A7	A6	A5	1	1	1	0	0	A7	A6	1	1	1	0	0	0
IR 6	A7	A6	A5	1	1	0	0	0	A7	A6	1	1	0	0	0	0
IR 5	A7	A6	A5	1	0	1	0	0	A7	A6	1	0	1	0	0	0
IR 4	A7	A6	A5	1	0	0	0	0	A7	A6	1	0	0	0	0	0
IR 3	A7	A6	A5	0	1	1	0	0	A7	A6	0	1	1	0	0	0
IR 2	A7	A6	A5	0	1	0	0	0	A7	A6	0	1	0	0	0	0
IR 1	A7	A6	A5	0	0	1	0	0	A7	A6	0	0	1	0	0	0
IR 0	A7	A6	A5	0	0	0	0	0	A7	A6	0	0	0	0	0	0

TABLE 3-10. CALL ADDRESS INSERTION

Initialization Command Word 3 (ICW3)

This command word is only used in systems with multiple 8259's. This word loads the 8-bit slave register of the 8259. As this function is not used on the SBC 80/20, no further information is necessary. If bit S is set in ICW1, there is no need to program ICW3.

The format for the applicable Initialization Control Words (ICW1 and ICW2) are summarized in Figure 3-30.

Operation Command Words (OCWs)

After the Initialization Command Words (ICWs) are programmed into the 8259, the chip is ready to accept interrupt requests at its input lines. However, during the 8259 operation, a selection of algorithms can command the 8259 to operate in various modes through the Operation Command Words (OCWs). These various modes and their associated OCWs are summarized in Table 3-11 and Figure 3-31, and are described below.

Interrupt Masks

Each Interrupt Request input can be masked individually by the Interrupt Masked Register (IMR) programmed through OCW1.

The IMR will operate on both the Interrupt Request Register and the In-Service Register. Note that if an interrupt is already acknowledged by the 8259 (an $\overline{\text{INTA}}$ pulse has occurred), then the

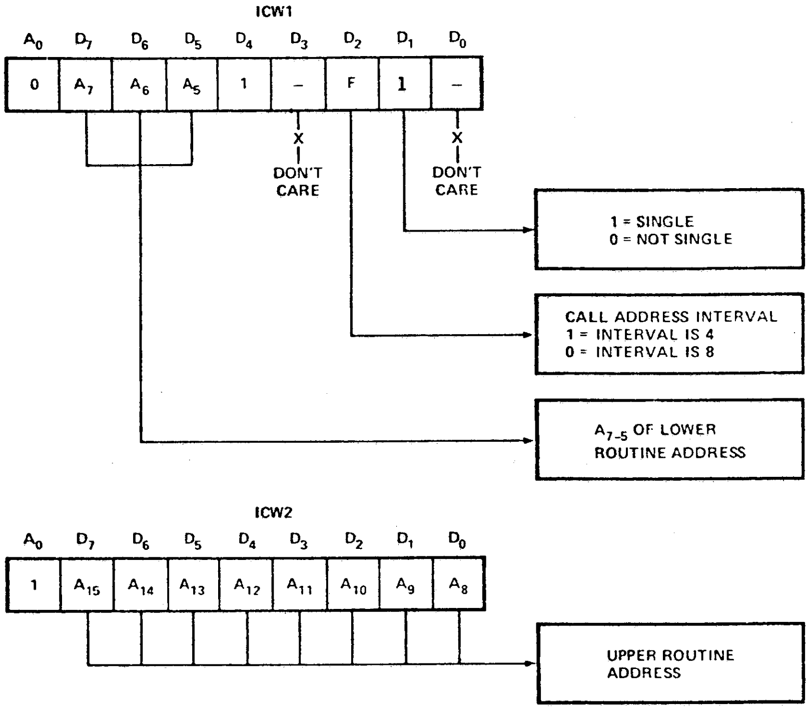
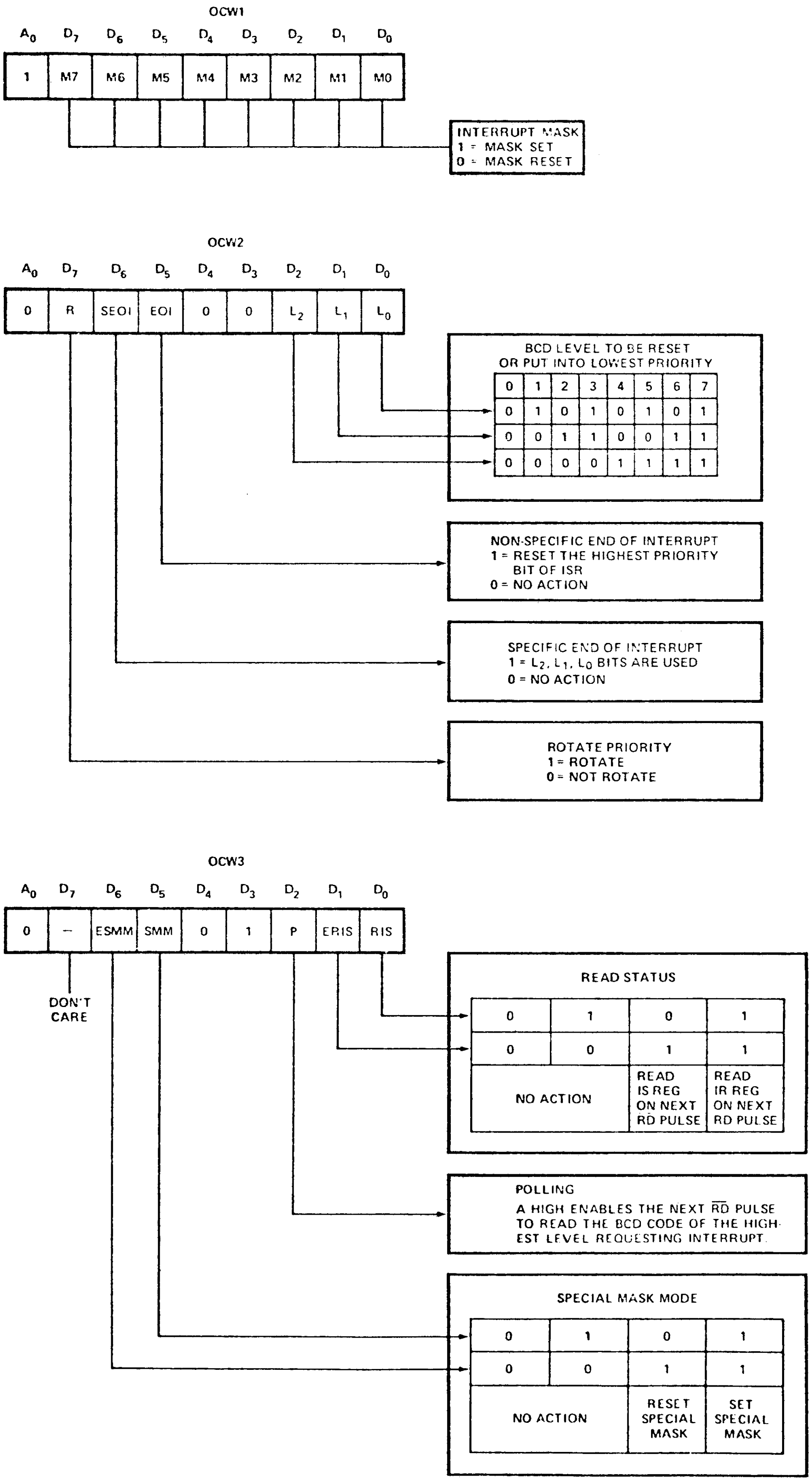


FIGURE 3-30. 8259 INITIALIZATION CONTROL WORD FORMATS



OCW1

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	M7	M6	M5	M4	M3	M2	M1	M0

INTERRUPT MASK
1 = MASK SET
0 = MASK RESET

OCW2

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	R	SEOI	EOI	0	0	L_2	L_1	L_0

BCD LEVEL TO BE RESET
OR PUT INTO LOWEST PRIORITY

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

NON-SPECIFIC END OF INTERRUPT
1 = RESET THE HIGHEST PRIORITY BIT OF ISR
0 = NO ACTION

SPECIFIC END OF INTERRUPT
1 = L_2, L_1, L_0 BITS ARE USED
0 = NO ACTION

ROTATE PRIORITY
1 = ROTATE
0 = NOT ROTATE

OCW3

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	–	ESMM	SMM	0	1	P	ERIS	RIS

DON'T CARE

READ STATUS

0	1	0	1
0	0	1	1
NO ACTION		READ IS REG ON NEXT $\overline{RD}$ PULSE	READ IR REG ON NEXT RD PULSE

POLLING
A HIGH ENABLES THE NEXT $\overline{RD}$ PULSE TO READ THE BCD CODE OF THE HIGHEST LEVEL REQUESTING INTERRUPT.

SPECIAL MASK MODE

0	1	0	1
0	0	1	1
NO ACTION		RESET SPECIAL MASK	SET SPECIAL MASK

FIGURE 3-31. 8259 OPERATION COMMAND WORD FORMATS

TABLE 3-11. SUMMARY OF OPERATION COMMAND WORD PROGRAMMING

	A0	D4	D3				
OCW1	1			M7-M0			IMR (Interrupt Mask Register). $\overline{WR}$ will load it while status can be read with $\overline{RD}$.
OCW2	0	0	0	R	SEOI	EOI	
				0	0	0	No Action.
				0	0	1	Non-specific End of Interrupt.
				0	1	0	No Action.
				0	1	1	Specific End of Interrupt. L2, L1, L0 is the BCD level to be reset.
				1	0	0	No Action.
				1	0	1	Rotate priority at EOI. (Auto Mode)
				1	1	0	Rotate priority, L2, L1, L0 becomes bottom priority without Ending of Interrupt.
				1	1	1	Rotate priority at EOI (Specific Mode), L2, L1, L0 becomes bottom priority, and its corresponding IS FF is reset.

NOTE: The 8080 must have its interrupts disabled during:
(i.e., by executing a DI instruction)

1. Initialization sequence for all 8259s in the system.
2. Any control command execution.

Interrupting level, although masked, will inhibit the lower priorities. To enable these lower priority interrupts, one can do one of the two things: (1) Write an End of Interrupt (EOI) command (OCW2) to reset the ISR bit or (2) Set the special mask mode using OCW3 (as will be explained later in the special mask mode.)

Fully Nested Mode

The 8259 will operate in the fully nested mode after the execution of the initialization sequence without any OCW being written. In this mode, the interrupt requests are ordered in priorities from 0 through 7. When an interrupt is acknowledged, the highest priority request is determined and its address vector placed on the bus. In addition, a bit of the Interrupt service register (IS 7-0) is set. This bit remains set until the 8080 issues an End of Interrupt (EOI) command immediately before returning from the service routine. While the IS bit is set, all further interrupts of lower priority are inhibited, while higher levels will be able to generate an interrupt (which will only be acknowledged if the 8080 has enabled its own interrupt input through software).

After the Initialization sequence, IRO has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained in the rotating priority mode.

Rotating Priority Mode.

The Rotating Priority Mode of the 8259 serves an application of interupting devices of equal priority such as communication channels. There are two variations of the rotating priority mode: the auto mode and the specific mode.

1. Auto-Rotating Mode -- In this mode, a device after being serviced receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case, until 7 other devices are serviced at most once each, i.e., if the priority and "in service" status is:

BEFORE ROTATE	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" STATUS	0	1	0	1	0	0	0	0
		LOWEST PRIORITY				HIGHEST PRIORITY		
PRIORITY STATUS	7	6	5	4	3	2	1	0

AFTER ROTATE	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" STATUS	0	1	0	0	0	0	0	0
		LOWEST PRIORITY				HIGHEST PRIORITY		
PRIORITY STATUS	4	3	2	1	0	7	6	5

In this example, the In-Service FF corresponding to line 4 (the highest priority FF set) was reset and line 4 became the lowest priority, while all the other priorities rotated correspondingly.

The Rotate command is issued in OCW2, where: R = 1, EOI = 1, SEOI = 0.

2. Specific Mode -- The programmer can change priorities by programming the bottom priority, and by doing this, to fix the

highest priority: i.e., if IR5 is programmed as the bottom priority device, the IR6 will have the highest one.

The Rotate command is issued in OCW2 where: R = 1, SEOI = 1, L2, L1, L0 are the BCD priority level codes of the bottom priority device.

Observe that this mode is independent of the End of Interrupt Command and priority changes can be executed during EOI command or independently from the EOI command.

End of Interrupt (EOI) and Specific End of Interrupt (SEOI)

An End of Interrupt command word must be issued to the 8259 before returning from a service routine, to reset the appropriate IS bit.

There are two forms of EOI command: Specific and non-Specific. When the 8259 is operated in modes which preserve the fully nested structure, it can determine which IS bit is to reset on EOI. When a non-Specific EOI command is issued the 8259 will automatically reset the highest IS bit of those that are set, since in the nested mode, the highest IS level was necessarily the last level acknowledged and will necessarily be the next routine level returned from.

However, when a mode is used which may disturb the fully nested structure, such as in the rotating priority case, the 8259 may no longer be able to determine the last level acknowledged. In this case, a specific EOI (SEOI) must be issued which includes the IS level to be reset as part of the command. The End of the Interrupt is issued whenever EOI = "1" in OCW2. For specific EOI, SEOI = "1", and EOI = 1, L2, L1, L0 is then the BCD level to be reset. As explained in the Rotate Mode earlier, this can also be the bottom priority code. Note that although the Rotate command can be issued during an EOI = 1, it is not necessarily tied to it.

Special Mask Mode (SMM)

This mode is useful when some bit(s) are set (masked) by the Interrupt Mask Register (IMR) through OCW1. If, for some reason, we are currently in a subroutine which is masked (this could happen in two manners. (1) $\overline{\text{INTA}}$ from CPU acknowledges the IR just before it is masked; (2) the subroutine intentionally masks itself off) it is still possible to enable the lower priority lines by setting the Special Mask mode. In this mode the lower priority lines are enabled until the SMM is reset. The higher priorities are not affected. (They may be individually masked as needed).

The special mask mode FF is set by OCW3 where ESMM = 1, SMM = 1, and reset where: ESSM = 1 and SMM = 0.

Polled Mode

In this mode, the 8080 disables its interrupt input. Service to devices is achieved by programmer initiative by a Poll command. The poll command is issued by setting P = "1" in OCW3 during a $\overline{\text{WR}}$ pulse.

The 8259 treats the next $\overline{\text{RD}}$ pulse as an interrupt acknowledge, sets the appropriate IS Flip-flop, if there is a request, and reads the priority level. The word enabled onto the data bus during $\overline{\text{RD}}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
1	-	-	-	-	W2	W1	W0

W0 - 2: BCD code of the highest priority level requesting service.

1: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels--so that the $\overline{\text{INTA}}$ sequence is not needed (and this saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

Reading 8259 Status

The input status of several internal registers can be read to update the user information on the system. The following registers can be read by issuing a suitable OCW and reading with $\overline{\text{RD}}$ for the data bus lines:

Interrupt Requests Register (IRR): 8-bit register which contains the priority levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged.

In Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when prior to the $\overline{\text{RD}}$ pulse, an $\overline{\text{WR}}$ pulse is issued with OCW3, and ERIS = 1, RIS = 0.

The ISR can be read in a similar mode, when ERIS = 1, RIS = 1.

There is no need to write an OCW3 before every status read operation as long as the status read corresponds with the previous one, i.e., the 8259 "remembers" whether the IRR or ISR has been previously selected by the OCW3. On the other hand, for polling operation, an

OCW3 must be written before every read.

For reading the IMR, a $\overline{WR}$ pulse is not necessary to precede the $\overline{RD}$. The output data bus will contain the IMR whenever $\overline{RD}$ is active and A0 = 1.

Polling overrides status read when P = 1, ERIS = 1 in OCW3.

Table 3-12 summarizes the 8259 Instruction Set.

3.10.3 SBC 80/20 INTERRUPT CONFIGURATION

The 8259 Programmable Interrupt Controller has been assigned dedicated I/O addresses within the SBC 80/20 system. The system software programs the 8259 and reads its status by executing I/O instructions directed to the appropriate addresses.

An output instruction to I/O address D8 or DA (hexadecimal) loads Initialization Command Word 1 (ICW1) or Operation Command Word 2 or 3 (OCW2 or OCW3) into the 8259. Bits 3 and 4 of the command word indicate whether the 8259 is to interpret the data as ICW1, OCW2 or OCW3 (see Table 3-13).

An output instruction to address D9 or DB (hex) loads Operation Command Word 1 (OCW1), or Initialization Command Word 2 or 3 (ICW2 or ICW3) into the 8259. On-chip sequence logic queues these commands into the proper sequence. The 8259 interprets the data as ICW2 or ICW3 if the 8259 is in an initialization sequence (i.e., ICW1 has been sent); otherwise, the data is interpreted as OCW1.

An input instruction to address D8 or DA (hex) causes the 8259 to output the contents of the Interrupt Requests Register (IRR), the In Service Register (ISR) or the current interrupting level. The

TABLE 3-12. 8259 INSTRUCTION SET[1]

INST. NO.	MNEMONIC	A0	D7	D6	D5	D4	D3	D2	D1	D0	OPERATION DESCRIPTION
1	ICW1 A	0	A7	A6	A5	1	–	1	1	–	Byte 1 initialization, format = 4, single.
2	ICW1 B	0	A7	A6	A5	1	–	1	0	–	Byte 1 initialization, format = 4, not single.[2]
3	ICW1 C	0	A7	A6	A5	1	–	0	1	–	Byte 1 initialization, format = 8, single.
4	ICW1 D	0	A7	A6	A5	1	–	0	0	–	Byte 1 initialization, format = 8, not single.[2]
5	ICW2	1	A15	A14	A13	A12	A11	A10	A9	A8	Byte 2 initialization (Address No. 2)
6	ICW3 M	1	S7	S6	S5	S4	S3	S2	S1	S0	Byte 3 initialization – master.[2]
7	ICW3 S	1	–	–	–	–	–	S2	S1	S0	Byte 3 initialization – slave.[2]
8	OCW1	1	M7	M6	M5	M4	M3	M2	M1	M0	Load mask reg, read mask reg.
9	OCW2 E	0	0	0	1	0	0	0	0	0	Non specific EOI.
10	OCW2 SE	0	0	1	1	0	0	L2	L1	L0	Specific EOI. L2, L1, L0 code of IS FF to be reset.
11	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate at EOI (Auto Mode).
12	OCW2 RSE	0	1	1	1	0	0	L2	L1	L0	Rotate at EOI (Specific Mode). L2, L1, L0, code of line to be reset and selected as bottom priority.
13	OCW2 RS	0	1	1	0	0	0	L2	L1	L0	L2, L1, L0 code of bottom priority line.
14	OCW3 P	0	–	0	0	0	1	1	0	0	Poll mode.
15	OCW3 RIS	0	–	0	0	0	1	0	1	1	Read IS register.
16	OCW3 RR	0	–	0	0	0	1	0	1	0	Read requests register.
17	OCW3 SM	0	–	1	1	0	1	0	0	0	Set special mask mode.
18	OCW3 RSM	0	–	1	0	0	1	0	0	0	Reset special mask mode.

NOTES:

1. (-) = do not care.
2. Not applicable to SBC 80/20 implementation.

selection of IRR, ISR or the interrupting level is based on the contents of the last OCW3 written before this read operation.

An input instruction to address D9 or DB (hex) causes the 8259 to output the contents of the Interrupt Mask Register (IMR) to the CPU.

Table 3-13 summarizes the 8259's I/O addresses and its basic operation.

TABLE 3-13. 8259 BASIC OPERATION[1,2]

A_0	D_4	D_3	$\overline{RD}$[3]	$\overline{WR}$[4]	$\overline{CS}$	INPUT OPERATION (READ)	I/O ADDRESS (hex)
0	-	-	0	1	0	IRS, ISR or Interrupting Level ⇒ DATA BUS (Note 1)	D8 or DA
1	-	-	0	1	0	IMR ⇒ DATA BUS	D9 or DB
						OUTPUT OPERATION (WRITE)	
0	0	0	1	0	0	DATA BUS ⇒ OCW2	D8 or DA
0	0	1	1	0	0	DATA BUS ⇒ OCW3	D8 or DA
0	1	X	1	0	0	DATA BUS ⇒ ICW1	D8 or DA
1	X	X	1	0	0	DATA BUS ⇒ OCW1, ICW2, ICW3 (Note 2)	D9 or DB
						DISABLE FUNCTION	
X	X	X	1	1	0	DATA BUS ⇒ 3-STATE	--
X	X	X	X	X	1	DATA BUS ⇒ 3-STATE	--

Note 1: Selection of IRR, ISR or Interrupting Level is based on the content of OCW3 written before the READ operation.

Note 2: On-chip sequencer logic queues these commands into proper sequence.

Note 3: Accomplished with 8080A IN instruction.

Note 4: Accomplished with 8080A OUT instruction.

The INT output from the 8259 is applied directly to the interrupt input pin on the 8080 CPU.

Seven of the 8259's Interrupt Request inputs (IR0-IR6) are connected to jumper pins 24-30. IR7 is connected to the wire-ORed output from two 7433 NOR gates (at A42) whose inputs are connected to jumper pins 36-39. Thus 11 different interrupt requests can be applied to the 8259's eight priority levels.

Nine external interrupt request lines, INTØ/-INT7/ and INTR/, enter the SBC 80/20 at connector P1 and are inverted and routed to jumper pins 50-42. In addition, 10 interrupt requests are generated by the various logic blocks on the SBC 80/20 and are routed to jumper pins in the Interrupt Controller section, three interrupt request lines eminate from the Serial I/O Interface:

Receive Ready (RXR) - pin 41,

Transmit Ready (TXR) - pin 40, and

Transmitter Empty (TXE) - pin 32.

Four interrupt lines originate in the Parallel I/O Interface: PIA1 from Port 1 (pin 63), PIB1 from Port 2 (pin 69), PIA2 from Port 4 (pin 92), and PIB2 from Port 5 (pin 88). The outputs from counters 0 and 1 on the 8253 Interval Timer (OIT0 and OIT1) are also applied to jumper pins (36 and 34, respectively) in the Interrupt Controller section. In addition 8 lines may be brought in thru C Port lines. Finally, the output from the Power Fail Interrupt latch is applied to jumper pin 33 in the interrupt section.

To configure a custom interrupt priority structure, the user need only jumper the external and/or on-board interrupt request lines to the desired priority level inputs (IR0-IR7) to the 8259. Then program the 8259 for the desired priority resolution algorithm, as previously described.

Note: If jumper pins 36, 37, 38 or 39 (leading to the IR7 input on the 8259) are not jumpered to interrupt request lines, they must be grounded by connecting the unused pin(s) to jumper pin 31.

3.11 POWER FAIL PROVISIONS

The SBC 80/20 has provisions for interrupting the CPU in the event of a system power failure, maintaining power fail status, and providing battery back-up power for RAM in the event of a drop in power.

The Power Fail Interrupt signal (PFI/) is received at connector pin P2-19 and clocks the Power Fail Interrupt latch at A27-3. The output from this latch is made available to the Interrupt Controller, as described in Section 3.10. When an output instruction to $D4_{16}$ is executed, the Power Fail Interrupt latch is reset.

A Power Fail Status signal (PFS/) is received at connector pin P2-17 and applied to an 8095 driver at A57-14. When an input instruction to address $D4_{16}$ is executed, the level on PFS/ is input on the least significant data bus line (DB0). The Power Fail Status signal is generated by the user's power fail circuitry. It allows the user's program to differentiate between power coming back up from a power failure or power being initially turned on. In other words the program can tell whether to restart where it left off or to initialize the system.

Connector pins P2-3 and 4 can be connected to a +5VDC back-up battery that will provide power to the SBC 80/20 RAM in the event of a power fail. Jumper pair W5,A-B must be disconnected when the battery back-up feature is used as shown on schematic sheet 6.

A Memory Protect (MPRO/) signal is received at connector pin P2-20 and applied to the RAM decoder. This signal is used to prevent the spurious signals, which may be generated on the memory command lines during power going down, from affecting the contents of memory.

The following is an example of how the various power fail signals should be used.

1. A power failure occurs. When the AC line voltage reaches some predetermined level (-10% typically) the power fail circuitry generates a Power Fail Interrupt (PFI/) signal.

2. The CPU is interrupted and goes into a program status saving routine. The routine should end with a HALT instruction.

3. After a predetermined length of time (5 ms for example) the power fail circuitry should generate Memory Protect (MPRO/) signal.

4. DC power goes down.

5. AC power returns. The power fail circuitry should generate a SYSTEM RESET signal and hold it until the power supplies are stable. Reset should also be held until Memory Protect signal is cleared.

6. The system program can now read the Power Fail Status signal and determine what type of restart procedure is to be executed.

CHAPTER 4

USER SELECTABLE OPTIONS

The SBC 80/20 and SBC 80/20-4 provide the user with a considerable memory storage capacity, as well as a powerful, but flexible interrupt-driven I/O capability for both parallel and serial transfers.

The 2K X 8-bit Random-Access-Memory (RAM) on the SBC 80/20 and the 4K X 8-bit Random-Access-Memory (RAM) on the SBC 80/20-4 can be jumper-assigned to the top address space in any one of the four 16K address blocks supported by an 8080A EPU. ROM/EPROM address space always begins at memory location zero.

The Serial I/O Interface, using Intel's 8251 USART, provides a serial data communications channel that can be programmed to operate with most of the current serial data transmission protocols. Synchronous or asynchronous mode, baud rate, character length, number of stop bits and even/odd parity are all program selectable.

The Parallel I/O Interface, using two Intel 8255 Programmable Peripheral Interface devices, provides 48 signal lines for the transfer and control of data to or from peripheral devices. Sixteen lines already have a bidirectional driver and termination network permanently installed. These lines may be programmed as input ports, output ports, or bidirectional ports. The remaining 32 lines are routed to sockets provided for the installation of active driver networks or passive termination networks as required to meet the specific needs of the user system.

A flexible interrupt structure, using Intel's 8259 Interrupt Controller, allows 10 on-board interrupt requests as well as 17 externally-generated interrupt requests to be applied to any of the

8259's eight priority level inputs. The 8259, in turn, resolves priority among the various requests according to a user-programmed scheme and interrupts 8080 program control, causing a branch in program execution to a location dedicated to the active interrupt priority level.

In this chapter, we will review each of the options available to the user and summarize, for easy reference, the specific information required to implement the user's tailored memory, I/O and interrupt configuration. Section 4.1 deals with memory address allocation. Sections 4.2 and 4.3 cover the Serial and Parallel I/O Interface options, respectively. Section 4.4 summarizes the interrupt priority options, while Section 4.5 describes various general options not covered in the other sections.

4.1 MEMORY ADDRESS ALLOCATION

The memory address decode logic is controlled in part by various jumpers. Certain of these jumper connections must be added or deleted (See Table 4-1) to properly configure the decode logic for the 2K or 4K of RAM (eight 512 x 4-bit or eight 1024 x 4-bit RAM devices).

These jumpers in the memory address decoding logic allow the user to specify the address space for the on-board RAM. The RAM can be assigned to any one of the four 16K blocks of address space (see Table 2-1) but it will always reside at the end of the selected block.

The installation of 8K 8-bits of ROM/EPROM requires jumper changes as outlined in Table 4-2. This configuration also requires the removal of capacitors C35, C53, and C72.

TABLE 4-1. RAM JUMPERS

2K		4K
2113A0L	2113A0H	2114
W1, C-H	-	W1, B-E*
W1, B-F*	W1, B-F*	W1, A-D*
W1, A-E*	W1, A-E*	W1, C-F*
W3, A-B	W3, A-B	
*Denotes default connection.		

TABLE 4-2. JUMPER CHANGES TO SELECT 8K PROM CAPABILITY

REMOVE	INSTALL
W2, A-C	W2, A-B
W4, B-D	W4, A-D
W4, C-E	W4, B-E
W7, A-B	W7, A-D
W8, A-C	W8, A-B

NOTE: Remove capacitors C35, C53, and C72.

4.2 SERIAL I/O OPTIONS

The Serial I/O Interface includes several programmable and jumper-selectable features that affect the 8251's mode of operation and determine the baud rate frequency to be used, as well as some jumper options that give the CPU access to certain RS232 signal lines via the Parallel I/O Interface rather than through the 8251.

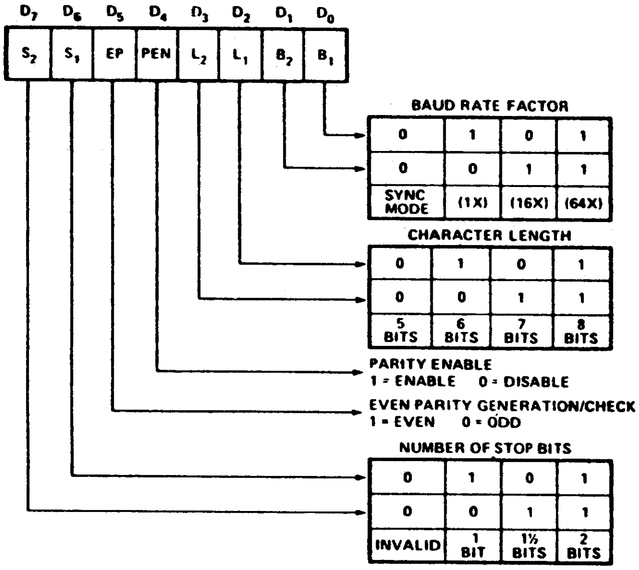
Implementation of each feature is summarized in the following sections.

4.2.1 BAUD RATE AND PROGRAM SELECTABLE SERIAL I/O OPTIONS

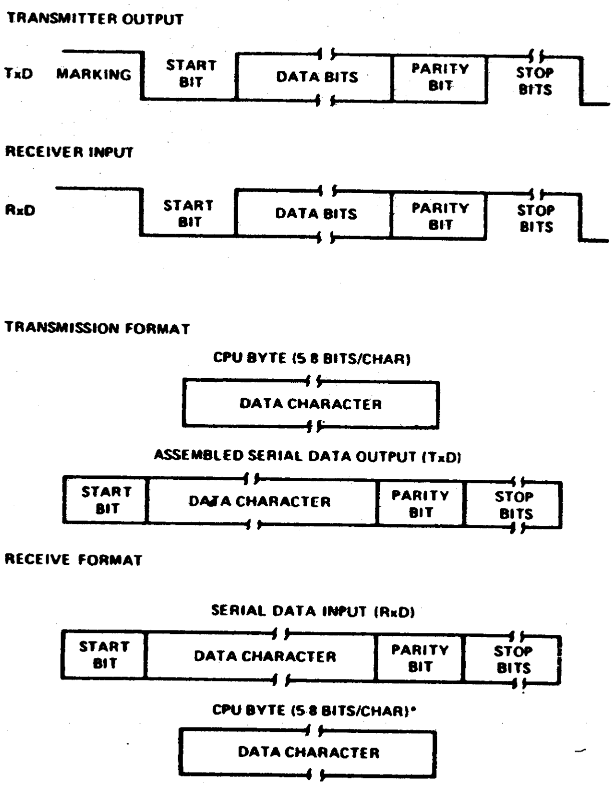
Before it can begin its serial I/O operations, the 8251 must be program-initialized to support the desired mode of operation. The CPU initializes the 8251 by outputting a set of control bytes to the USART device. These control words specify:

- synchronous or asynchronous operation,
- baud rate factor,
- character length,
- number of stop bits,
- even/odd parity,
- parity/no parity

As explained in Section 3.7.1, there are two types of control words: (1) Mode instruction and (2) Command instruction. The Mode instruction initializes the 8251 USART. Because the USART supports either synchronous or asynchronous operation, the Mode instruction has one format for synchronous operation and another for asynchronous. The two least significant bits of the Mode instruction byte specify the format. If DO and D1 both equal 0, synchronous operation is indicated; otherwise, it is asynchronous. The Mode instruction format for asynchronous operation is illustrated in Figure 4-1. The Mode instruction for synchronous operation is shown in Figure 4-2.



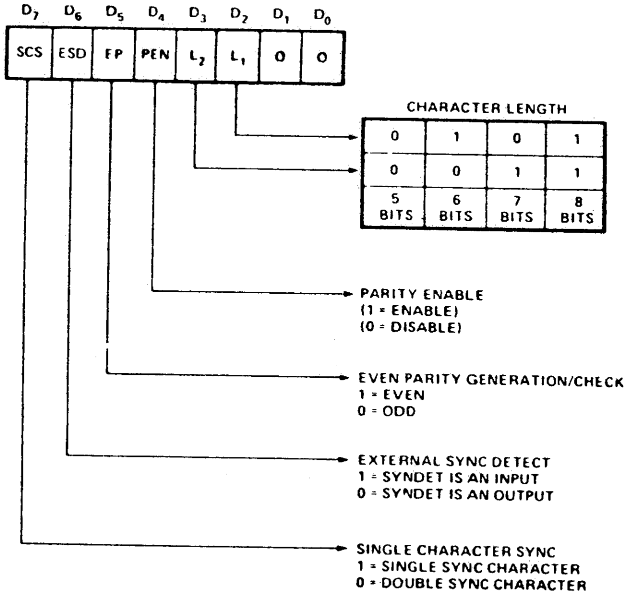
Mode Instruction Format, Asynchronous Mode



*NOTE: IF CHARACTER LENGTH IS DEFINED AS 5, 6 OR 7 BITS THE UNUSED BITS ARE SET TO "ZERO".

Asynchronous Mode

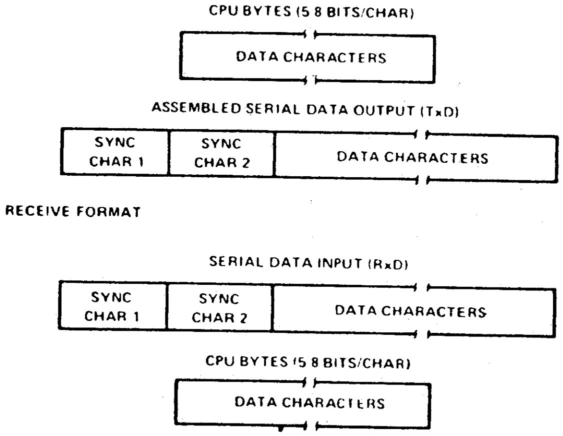
FIGURE 4-1. ASYNCHRONOUS OPERATION



CHARACTER LENGTH

0	1	0	1
0	0	1	1
5 BITS	6 BITS	7 BITS	8 BITS

Mode Instruction Format, Synchronous Mode



Synchronous Mode, Transmission Format

FIGURE 4-2. SYNCHRONOUS OPERATION

Notice in Figure 4-1 that the baud rate factor is specified by the two least significant bits of the instruction byte (labeled B1 and B2). During asynchronous communications, the baud rate frequency supplied to the 8251's $\overline{\text{TXC}}$ and $\overline{\text{RXC}}$ input pins is divided by the baud rate factor to produce the effective baud rate (i.e., the frequency at which data bits are serially transmitted by the 8251 USART). Consequently, the baud rate frequency, as well as the program-selected baud rate factor, must be considered in implementing the desired effective baud rate. The baud rate frequency can be provided by the 8253 Interval Timer. Counter 2 in the 8253 device, however, must be programmed to generate the desired baud rate frequency as described in Section 3.9. Baud Rate Factors for common communications frequencies are shown in Table 4-34.

Notice from the schematic that $\overline{\text{TXC}}$ and $\overline{\text{RXC}}$ inputs can be supplied by externally supplied clocks (via connector pins J3-3 and J3-7, respectively), instead of using the output from 8253 counter 2 if jumpers 20-21 and 17-18 are connected and jumpers 19-21 and 16-18 are disconnected.

4.2.2 OPTIONAL USE OF CERTAIN RS232 SIGNALS

The RS232 interface includes seven signal lines that can be jumper-selected such that four of them can be accessed through Port 6 in the Parallel I/O Interface. Table 4-3 summarizes the information needed to use these signal lines. The first column in the table lists the RS232 signal name and connector pin, column 2 specifies its direction relative to the SBC 80/20 (input to or output from

TABLE 4-3. RS232 SIGNAL OPTIONS

RS232 SIGNAL NAME (connector pin)	DIRECTION	SERIAL I/O INTERFACE JUMPER CONNECTIONS	LINE MNEMONIC	PARALLEL I/O INTERFACE JUMPER PIN
SEC. RTS (J3-11)	INPUT	7-8	AUX1	89
SEC. TRANS. DAT (J3-1)		6-8		
RING INDICATOR	INPUT	-	BRI/	96
REC. LINE SIG. DET. (J3-16)	INPUT	-	BDET	97
SEC. CTS (J3-26)	OUTPUT	13-14	AUXØ	90
SEC. REC. DATA (J3-5)		14-15		
TRANS. SIG. ELE. TIMEING (J3-21)		5-8		

All Mnemonics © 1976 Intel Corp.

the SBC 80/20), column 3 lists any jumper action that is required to select the signal in the Serial I/O Interface, column 4 shows the mnemonic for the line which presents or accepts the RS232 signal to/from the Parallel I/O Interface, and finally the last column lists the jumper pin that is to be connected to one of the Port 6 input jumper pins as shown on sheet 4 of the schematic (Appendix A).

4.3 PARALLEL I/O OPTIONS

The Parallel I/O Interface consists of six 8-bit I/O ports implemented with two Intel®8255 Programmable Peripheral Interface devices. The primary user considerations in determining how to use each of the six I/O ports are:

1) Choice of operating mode (as defined in Section 3.8.1),

2) direction of data flow (input, output or bidirectional),

3) choice of driver/termination networks for port's data path.

In the following paragraphs, we will define the capabilities of each port and summarize, in tables, that information which is necessary to use the port in each of its potential configurations. Each table will list the port I/O address, the control register address and the format for the control word which is output to the 8255 by the bus master and which specifies the particular configuration to be used. Each table will also summarize all of the relevant information concerning the choice and use of driver/termination networks, the data polarity, the connecting of jumpers and what they enable, and any restrictions on the use of the other two ports in each group. Examples of suitable driver/termination networks are listed in Section 5.1.

The configuration tables for group 2 ports are identical to those for group 1 ports except for I/O address, port numbers, component location numbers and jumper pin numbers. For this reason the tables are organized as three sets: Ports 1 and 4, Ports 2 and 5 and Ports 3 and 6.

At the beginning of each set, the general characteristics of that port are reviewed. Where port numbers are used in the text, the group 1 number is presented first and the corresponding group 2 number follows in parentheses. For example, when referring to B ports, the reference will appear as Port 2(5).

The introductory text is followed by a series of tables that cover all of the configurations that are possible for the ports under discussion. To simplify the search for specific tables, each table is presented on a separate page.

Table 4-4 summarizes the various mode combinations that are possible with Ports A and B and indicates how each Port C bit can or cannot be used for each mode combination. This table can serve as a useful starting point for selecting an I/O configuration for either group 1 or group 2 ports. Once the desired mode combination is selected and the Port C bit assignments are made, the appropriate configuration tables (Tables 4-5 through 4-30) can be referred to for implementation details.

TABLE 4-4. PARALLEL I/O INTERFACE CONFIGURATIONS

CONFIGURATION NUMBER	8255 PORT A	8255 PORT B	8255 PORT C Lower				8255 PORT C Upper			
			$C_{\emptyset}$	C_1	C_2	C_3	C_4	C_5	C_6	C_7
1	MODE Ø-I	MODE Ø-I/O	--- I/O ---				--- I/O ---			
2	MODE Ø-O	MODE Ø-I/O	--- I/O ---				--- I/O ---			
3	MODE Ø-I	MODE 1-I/O	R	R	R	I	O	O	O	U
4	MODE Ø-I	MODE 1-I/O	R	R	R	O	I	I	I	U
5	MODE Ø-O	MODE 1-I/O	R	R	R	I	O	O	O	U
6	MODE Ø-O	MODE 1-I/O	R	R	R	O	I	I	I	U
7	MODE 1-I	MODE Ø-I/O	I	I	I	R	R	R	O	O
8	MODE 1-I	MODE Ø-I/O	O	O	O	R	R	R	I	I
9	MODE 1-O	MODE Ø-I/O	I	I	I	R	O	O	R	R
10	MODE 1-O	MODE Ø-I/O	O	O	O	R	I	I	R	R
11	MODE 1-I	MODE 1-I/O	R	R	R	R	R	R	I	I
12	MODE 1-I	MODE 1-I/O	R	R	R	R	R	R	O	O
13	MODE 1-O	MODE 1-I/O	R	R	R	R	I	I	R	R
14	MODE 1-O	MODE 1-I/O	R	R	R	R	O	O	R	R
15	MODE 2-B	MODE Ø-I/O	U	I	I	R	R	R	R	R
16	MODE 2-B	MODE Ø-I/O	U	O	O	R	R	R	R	R
17	MODE 2-B	MODE 1-I/O	R	R	R	R	R	R	R	R

I = INPUT

O = OUTPUT

I/O = INPUT OR OUTPUT

B = BIDIRECTIONAL

R - Reserved

U - No unused drivers/terminators available. These bits may be used, however, to connect to the serial I/O interface or the Interval Timer.

4.3.1 PORTS 1 AND 4 (8255 PORT A)

Port 1(4) is the only port that already includes a permanent bidirectional driver/termination network (two 8226 Bidirectional Bus Drivers). Port 1(4) is also the only port which can be programmed to function in any one of the three 8255 operation modes, which were defined in Section 3.8.1. Before Port 1(4) is programmed for input or output in any one of the three modes, certain jumper connections must be made to allow the port to function properly in the chosen mode. In all, there are five potential configurations for Port 1(4). All of the necessary information for implementing each configuration has been summarized in the following tables:

	PORT 1(4) CONFIGURATIONS		TABLES	
	Mode	Direction	Group 1	Group 2
1.	Mode 0	Input	4-5	4-6
2.	Mode 0	Output (Latched)	4-7	4-8
3.	Mode 1	Input (Strobed)	4-9	4-10
4.	Mode 1	Output (Latched)	4-11	4-12
5.	Mode 2	Bidirectional	4-13	4-14

TABLE 4-5. PORT 1, MODE 0 INPUT CONFIGURATION

PORT 1 ADDRESS: E4, CONTROL REGISTER ADDRESS: E7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0	1				

DRIVER/TERMINATION NETWORKS: Two Intel®8226 Bidirectional Bus Drivers are factory-installed at A1 and A2.

DATA POLARITY AT J1: Negative

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	52-53*	51-52	Enable input at 8226's

PORT RESTRICTIONS - PORT 2: None; Port 2 can be programmed for mode 0 or mode 1, input or output.

PORT 3: None; Port 3 can be programmed for mode 0, 8-bit input or output, unless Port 2 is in mode 1.

TABLE 4-6. PORT 4, MODE 0 INPUT CONFIGURATION

PORT 4 ADDRESS: E8, CONTROL REGISTER ADDRESS: EB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0	1				

DRIVER/TERMINATION NETWORKS: Two Intel®8226 Bidirectional Bus Drivers are factory-installed at A7 and A8.

DATA POLARITY AT J2: Negative true

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	71-72*	70-71	Enable input at 8226's

PORT RESTRICTIONS - PORT 5: None; Port 5 can be programmed for mode 0 or mode 1, input or output.

PORT 6: None; Port 6 can be programmed for mode 0, 8-bit input or output, unless Port 5 is in mode 1.

TABLE 4-7. PORT 1, MODE 0 LATCHED OUTPUT CONFIGURATION

PORT 1 ADDRESS: E4, CONTROL REGISTER ADDRESS: E7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0	0				

DRIVER/TERMINATION NETWORKS: Two Intel®8226 Bidirectional Bus Drivers are factory-installed at A1 and A2.

DATA POLARITY AT J1: Negative true

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		52-53*	Enable output at 8226's

PORT RESTRICTIONS - PORT 2: None; Port 2 can be in mode 0 or mode 1, input or output.

PORT 3: None; Port 3 can be in mode 0, 8-bit input or output, unless Port 2 is in mode 1.

TABLE 4-8. PORT 4, MODE 0 LATCHED OUTPUT CONFIGURATION

PORT 4 ADDRESS: E8, CONTROL REGISTER ADDRESS: EB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0	0				

DRIVER/TERMINATION NETWORKS: Two Intel®8226 Bidirectional Bus Drivers are factory-installed at A7 and A8.

DATA POLARITY AT J2: Negative true

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		71-72*	Enable output at 8226's

PORT RESTRICTIONS: - PORT 5: None; Port 5 can be in mode 0 or mode 1, input or output.

PORT 6: None; Port 6 can be in mode 0, 8-bit input or output, unless Port 5 is in mode 1.

TABLE 4-9. PORT 1, MODE 1 INPUT STROBED

PORT 1 ADDRESS: E4, CONTROL REGISTER ADDRESS: E7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	1	1				

DRIVER/TERMINATION NETWORKS: Two Intel®8226 Bidirectional Bus Drivers are factory installed at A1 and A2. A terminatior network must be installed at A3 and a driver network must be installed at A4.

DATA POLARITY AT J1: Negative true. Polarity of Port 3 control outputs depends on whether driver at A4 is inverting or non-inverting.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	52-53*	51-52	Enable input at 8226's.
	68-69*		Disconnects Port 3, bit 3 (INTR) from driver at A4.
		60-61*	Connects STB_A/ input (J1-26) to bit 4 of Port 3.
	68-69* and 58-59*	59-68	Connects bit 5 of Port 3 (IBF_A) to J1-18.

PORT RESTRICTIONS - PORT 2: None; Port 2 can be in mode 0 or mode 1, input or output.

PORT 3: Port 3 bits perform the following dedicated functions:

- Bits 0,1 and 2 - provide control for Port 2 if Port 2 is in mode 1
- Bit 3 - INTR (interrupt request output for Port 1
- Bit 4 - STB/ (strobe) input for Port 1
- Bit 5 - IBF (input buffer full) output for Port 1
- Bits 6 and 7 - Can be used for input or output; both have same direction.

TABLE 4-10. PORT 4, MODE 1 INPUT STROBED

PORT 4 ADDRESS: E8, CONTROL REGISTER ADDRESS: EB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	1	1				

DRIVER/TERMINATION NETWORKS: Two Intel®8226 Bidirectional Bus Drivers are factory-installed at A7 and A8. A terminator network must be installed at A9 and a driver network must be installed at A10.

DATA POLARITY AT J2: Negative true. Polarity of Port 3 control outputs depends on whether driver at A10 is inverting or non-inverting.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	71-72*	70-71	Enable input at 8226's
	87-88*		Disconnects Port 6, bit 3 (INTR) from driver at A10.
		79-80*	Connects STB$_A$/ input (J2-26) to bit 4 of Port 6.
	77-78* and 87-88*	78-87	Connects bit 5 of Port 6 (IBF) to J2-18.

PORT RESTRICTIONS - PORT 5: None; Port 5 can be in mode 0 or mode 1, input or output.

PORT 6: Port 6 bits perform the following dedicated functions:

- Bits 0, 1 and 2 - provide control for Port 5 if Port 5 is in mode 1.
- Bit 3 - INTR (interrupt request) output for Port 4.
- Bit 4 - STB/ (strobe) input for Port 5
- Bit 5 - IBF (input buffer full) output for Port 4
- Bits 6 and 7 - can be used for input or output; both have same direction.

TABLE 4-11. PORT 1, MODE 1 LATCHED OUTPUT CONFIGURATION

PORT 1 ADDRESS: E4, CONTROL REGISTER ADDRESS: E7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	1	0				

DRIVER/TERMINATION NETWORKS: Two Intel®8226 Bidirectional Bus Drivers are factory-installed at A1 and A2. A terminator network must be installed at A3 and a driver network must be installed at A4.

DATA POLARITY AT J1: Negative true. The polarity of Port 3 control outputs depends on the type of driver installed at A4.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		52-53*	Enable output at 8226's
	68-69*		Disconnects Port 3, bit 3 (INTR) from driver at A4.
		56-57*	Connects ACK$_A$/ input (j1-30) to bit 6 of Port 3.
	54-55* and 68-69*	55-68	Connects bit 7 of Port 3 (OBF$_A$/) to J1-18.

PORT RESTRICTIONS - PORT 2: None; Port 2 can be in mode 0 or mode 1, input or output.

PORT 3: Port 3 bits perform the following dedicated functions:

- Bits 0, 1 and 2 - Dedicated to the control of Port 2 if Port 2 is in mode 1.
- Bit 3 - INTR (interrupt request) output for Port 1.
- Bits 4 and 5 - Can be used as input or output; both have same direction.
- Bit 6 - ACK/ (acknowledge) input for Port 1.
- Bit 7 - OBF/ (output buffer full) output for Port 1.

TABLE 4-12. PORT 4, MODE 1 LATCHED OUTPUT CONFIGURATION

PORT 4 ADDRESS: E8, CONTROL REGISTER ADDRESS: EB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	1	0				

DRIVER/TERMINATION NETWORKS: Two Intel® 8226 Bidirectional Bus Drivers are factory-installed at A7 and A8. A terminator network must be installed at A9 and a driver network must be installed at A10.

DATA POLARITY AT J2: Negative true. The polarity of Port 6 control outputs depends on the type of driver installed at A10.

JUMPER ACTION:

* = Default connection

DELETE	ADD	
	71-72*	Enable outputs at 8226's
87-88*		Disconnects Port 6, bit 3 (INTR) from driver at A10.
	75-76*	Connects ACK_A/ input (J2-30) to bit 6 of Port 6.
73-74* and 87-88*	74-87	Connects bit 7 of Port 6 (OBF_A/) to J2-18.

PORT RESTRICTIONS - PORT 5: None; Port 5 can be in mode 0 or mode 1, input or output.

PORT 6: Port 6 bits perform the following dedicated functions:

- Bits 0, 1 and 2 - Dedicated to the control of Port 5 if Port 5 is in mode 1.
- Bit 3 - INTR (interrupt request) output for Port 4.
- Bits 4 and 5 - Can be used as input or output; both have same direction.
- Bit 6 - ACK/(acknowledge) input for Port 4.
- Bit 7 - OBF/(output buffer full) output for Port 4.

TABLE 4-13. PORT 1, MODE 2 BIDIRECTIONAL CONFIGURATION

PORT 1 ADDRESS: E4, CONTROL REGISTER ADDRESS: E7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	1	X	X				

DRIVER/TERMINATION NETWORKS: Two Intel®8226 Bidirectional Bus Drivers are factory-installed at A1 and A2. A terminator network must be installed at A4.

DATA POLARITY AT J1: Negative true. The polarity of Port 3 control output depends on the type of driver installed at A4.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	52-53*	57-52	Allows ACK_A/ output of Port 3 to control 8226 direction mode.
	68-69*		Disconnects Port 3, bit 3 (INTR) from driver at A4.
		60-61*	Connects STB_A/ input (J1-26) to bit 4 of Port 3.
	58-59* and 62-63*	59-62	Connects bit 5 of Port 3 (IBF_A) to J1-24.
		56-57*	Connects ACK_A/ input (J1-30) to bit 6 of Port 3.
	54-55* and 68-69*	55-68	Connects bit 7 of Port 3 (OBF_A/) to J1-18.

PORT RESTRICTIONS - PORT 2: None.

PORT 3: Port 3 bits perform the following dedicated functions:

- Bit 0 - Cannot be used.
- Bits 1 and 2 - Can both be used in either input or output if Port 2 is in mode 0.
- Bit 3 - INTR (interrupt request) output for Port 1.
- Bit 4 - STB/ (strobe) input for Port 1.
- Bit 5 - IBF (input buffer full) output for Port 1.
- Bit 6 - ACK/ (acknowledge) input for Port 1.
- Bit 7 - OBF/ (output buffer full) output for Port 1.

TABLE 4-14: PORT 4, MODE 2 BIDIRECTIONAL CONFIGURATION

PORT 4 ADDRESS: E8, CONTROL REGISTER ADDRESS: EB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	1	X	X				

DRIVER/TERMINATION NETWORKS: Two Intel® 8226 Bidirectional Bus Drivers are factory-installed at A7 and A8. A terminator network must be installed at A9 and a driver network must be installed at A10.

DATA POLARITY AT J2: Negative true. The polarity of Port 6 control outputs depends on the type of driver used at A10.

JUMPER ACTION:

* = Default connection

DELETE	ADD	EFFECT
71-72*	76-71	Allows ACK$_A$/ output of Port 6 to control 8226 direction mode.
87-88*		Disconnects Port 6, bit 3 (INTR) from driver at A10.
	79-80*	Connects STB$_A$/ input (J2-26) to bit 4 of Port 6.
77-78* and 81-82*	78-81	Connects bit 5 of Port 6 (IFB$_A$) to J2-24.
	75-76*	Connects ACK$_A$/ input (J2-30) to bit 6 of Port 6.
73-74* and 87-88*	74-87	Connects bit 7 of Port 6 (OBF$_A$/) to J2-18.

PORT RESTRICTIONS - PORT 5: None

PORT 6: Port 6 performs the following dedicated functions:

- Bit 0 - Can be used to control bits on Serial I/O Interface; cannot be used otherwise.
- Bits 1 and 2 - Can both be used as either input or output if Port 5 is in mode 0.
- Bit 3 - INTR (interrupt request) output for Port 4.
- Bit 4 - STB/ (strobe) input for Port 4.
- Bit 5 - IBF (input buffer full) output for Port 4.
- Bit 6 - ACK/ (acknowledge) input for Port 4.
- Bit 7 - OBF) (output buffer full) output for Port 4.

TABLE 4-15. PORT 2, MODE 0 INPUT CONFIGURATION

PORT 2 ADDRESS: E5, CONTROL REGISTER ADDRESS: E7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1					0	1	

DRIVER/TERMINATION NETWORKS: Termination networks must be installed at A5 and A6.

DATA POLARITY AT J1: Positive true

JUMPER ACTION: None, other than to connect the data path between Ports 2 and the termination networks at A5 and A6.

PORT RESTRICTIONS - PORT 1: None

PORT 2: None; Port 3 can be in mode 0, input or output unless Port 1 is in mode 1 or mode 2.

4.3.2 PORTS 2 AND 5 (8255 PORT B)

Port 2(5) can be programmed for input or output in either mode 0 or mode 1. If Port 2(5) is to be used for input, in either mode, terminator networks must be installed in the sockets at A5(11) and A6(12). If port 2(5) is to be used for output, in either mode, driver networks must be installed in the sockets at A5(11) and A6(12). The four potential configurations for Port 2(5) are summarized in the following tables:

	PORT 2(5) CONFIGURATIONS		TABLES	
	Mode	Direction	Group 1	Group 2
1.	Mode 0	Input	4-15	4-16
2.	Mode 0	Output (Latched)	4-17	4-18
3.	Mode 1	Input (Strobed)	4-19	4-20
4.	Mode 1	Output (Latched)	4-21	4-22

TABLE 4-16. PORT 5, MODE 0 INPUT CONFIGURATION

PORT 5 ADDRESS: E9, CONTROL REGISTER ADDRESS: EB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1					0	1	

DRIVER/TERMINATION NETWORKS: Termination networks must be installed at A11 and A12.

DATA POLARITY AT J2: Positive true

JUMPER ACTION: None, other than to connect the data path between Port 5 and the termination networks at A11 and A12.

PORT RESTRICTIONS - PORT 4: None

PORT 6: None; Port 6 can be in mode 0, input or output unless Port 4 is in mode 1 or mode 2.

TABLE 4-17. PORT 2, MODE 0 LATCHED OUTPUT CONFIGURATION

PORT 2 ADDRESS: E5, CONTROL REGISTER ADDRESS: E7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1					0	0	

DRIVER/TERMINATION NETWORKS: Driver networks must be installed at A5 and A6.

JUMPER ACTION: None, other than to connect the data path between Port 2 and the drivers at A5 and A6.

PORT RESTRICTIONS - PORT 1: None

PORT 2: None, Port 3 can be in mode 0 input or output, unless Port 1 is in mode 1 or mode 2.

TABLE 4-18. PORT 5, MODE 0 LATCHED OUTPUT CONFIGURATION

PORT 5 ADDRESS: E9, CONTROL REGISTER ADDRESS: EB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1					0	0	

DRIVER/TERMINATION NETWORKS: Driver networks must be installed at A11 and A12.

DATA POLARITY AT J2: Negative true, assuming inverting drivers are used at A11 and A12.

JUMPER ACTION: None, other than to connect the data path between Port 5 and the drivers at A11 and A12.

PORT RESTRICTIONS - PORT 4: None

PORT 6: None; Port 6 can be in mode 0, input or output, unless Port 4 is in mode 1 or mode 2.

TABLE 4-19. PORT 2, MODE 1 STROBED INPUT CONFIGURATION

PORT 2 ADDRESS: E5, CONTROL REGISTER ADDRESS: E7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1					1	1	

DRIVER/TERMINATION NETWORKS: Terminator networks must be installed at A3, A5 and A6. A driver network must be installed at A4.

DATA POLARITY AT J1: Positive true. The polarity of Port 3 control outputs depends on the type of driver at A4.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	62-63*		Disconnects Port 3, bit 0 (INTR) from the driver at A4.
		64-65*	Connects bit 1 of Port 3 (IBF_B) to J1-22.
	54-55* and 66-67*	67-54	Connects STB_B/ input (J1-32) to bit 2 of Port 3.

PORT RESTRICTIONS - PORT 1: None

PORT 2: Port 3 bits perform the following dedicated functions:

- Bit 0 - INTR (interrupt request) output for Port 2.
- Bit 1 - IBF (input buffer full) output for Port 2.
- Bit 2 - STB/ (strobe) input for Port 2.
- Bit 3 - If Port 1 is in mode 0, bit 3 can be input or output; otherwise bit 3 is reserved.
- Bits 4 to 7 - Can be input or output if Port 1 is in mode 0 or in some mode combinations where Port 1 is in mode 1. These bits are always reserved when Port 1 is in mode 2. See Table 4-4 for details regarding bits 4 to 7.

TABLE 4-20. PORT 5, MODE 1 STROBED INPUT CONFIGURATION

PORT 5 ADDRESS: E9, CONTROL REGISTER ADDRESS: EB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1					1	1	

DRIVER/TERMINATION NETWORKS: Termination networks must be installed at A9, A11 and A12. A driver network must be installed at A10.

DATA POLARITY AT J2: Positive true. The polarity of Port 3 control outputs depends on the type of driver at A10.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	81-82*		Disconnects bit 0 of Port 6 (INTR) from driver at A10
		83-84*	Connects bit 1 of Port 6 (IBF$_B$) to J2-22.
	85-86* and 73-74*	86-73	Connects STB$_B$/ input (J2-32) to bit 2 of Port 6

PORT RESTRICTIONS - PORT 4: None

PORT 6: Port 6 bits perform the following dedicated functions:

- Bit 0 - INTR (interrupt request) output for Port 5.
- Bit 1 - IBF (input buffer full) output for Port 5.
- Bit 2 - STB/ (strobe) input for Port 5.
- Bit 3 - If Port 4 is in mode 0, bit 3 can be input or output; otherwise bit 3 is reserved.
- Bits 4 to 7 - Can be input or output if Port 4 is in mode 0 or in some mode combinations where Port 4 is in mode 1. These bits are always reserved when Port 4 is in mode 2. See Table 4-4 for details.

TABLE 4-21. PORT 2, MODE 1 LATCHED OUTPUT CONFIGURATION

PORT 2 ADDRESS: E5, CONTROL REGISTER ADDRESS: E7

CONTROL WORD FORMAT:	7	6	5	4	3	2	1	0
	1					1	0	

DRIVER/TERMINATION NETWORKS: Driver networks must be installed at A4, A5 and A6. A terminator network must be installed at A3.

DATA POLARITY AT J1: Negative true, assuming that inverting drivers are used at A4, A5 and A6.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	62-63*		Disconnects bit 0 of Port 3 (INTR) from the driver at A4.
		64-65*	Connects bit 1 of Port 3 (OBF$_B$) to J1-22.
	54-55* and 66-67*	67-54	Connects ACK$_B$/ input (J1-32) to bit 2 of Port 3

PORT RESTRICTIONS - PORT 1: None

PORT 2: Port 3 bits perform the following dedicated functions:

- Bit 0 - INTR (interrupt request input for Port 2.
- Bit 1 - OBF/ (output buffer full) output for Port 2.
- Bit 2 - ACK/ (acknowledge) input for Port 2.
- Bit 3 - If Port 1 is in mode 0, bit 3 can be input or output; otherwise bit 3 is reserved.
- Bits 4 to 7 - Can be input or output if Port 1 is in mode 0 or in some combinations where Port 1 is in mode 1. These bits are always reserved when Port 1 is in mode 2. See Table 4-4 for details.

TABLE 4-22. PORT 5, MODE 1 LATCHED OUTPUT CONFIGURATION

PORT 5 ADDRESS: E9, CONTROL REGISTER ADDRESS: EB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1					1	0	

DRIVER/TERMINATION NETWORKS: Driver networks must be installed at A10, A11 and A12. A terminator network must be installed at A9.

DATA POLARITY AT J2: Negative true, assuming that inverting drivers are used at A10, A11 and A12.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection	81-82*		Disconnects bit 0 of Port 6 (INTR) from the driver at A10.
		83-84*	Connects bit 1 of Port 6 (OBF$_B$) to J2-22.
	85-86* and 73-74*	86-73	Connects ACK$_B$/ input (J2-32) to bit 2 of Port 6.

PORT RESTRICTIONS - PORT 4: None

PORT 6: Port 6 bits perform the following dedicated functions:

- Bit 0 - INTR (interrupt request) output for Port 5.
- Bit 1 - OBF/ (output buffer full) output for Port 5.
- Bit 2 - ACK/ (acknowledge) input for Port 5.
- Bit 3 - If Port 4 is in mode 0, bit 3 can be input or output; otherwise bit 3 is reserved.
- Bits 4 to 7 - Can be input or output if Port 4 is in mode 0 or in some combinations where Port 4 is in mode 1. These bits are always reserved when Port 4 is in mode 2. See Table 4-4 for details

4.3.3 PORTS 3 AND6 (8255 PORT C)

The use of Port 3(6) depends on the modes programmed for Ports 1(4) and 2(5). It can be implemented as an 8-bit input or output data path or as two 4-bit I/O paths only if both Port 1(4) and Port 2(5) are programmed for mode 0. If Port 1(4) is in either mode 1 or mode 2 or if Port 2(5) is in mode 1, various individual Port 3(6) bits are available while the other Port 3(6) bits are either dedicated to control functions or are unavailable for any purpose.

Tables 4-23 through 4-30 specify the use of Port 3(6) bits as separate pairs of 4-bit I/O ports. As such, the two halves of Port 3(6) can both operate as input or output ports or they can have separate direction characteristics. The two halves are referred to as lower (bits 0 to 3) and upper (bits 4 to 7).

When Port 1(4) is in mode 1, it uses bit 3 of Port 3(6) and two upper bits of Port 3(6) for control functions. When Port 1(4) is in mode 2, it uses bit 3 of Port 3(6) and all four upper bits of Port 3(6) for control functions. Similarly, when Port 2(5) is in mode 1, it uses bit 0 of Port 3(6) and two lower bits from Port 3(6) for control.

Table 4-31 summarizes the use of Port 3 bits for control by Ports 1 and 2. Table 4-32 serves the same purpose for Port 6. These tables can be used as final check lists to verify the correct wiring of Port 3 and Port 6 control bits.

TABLE 4-23. PORT 3 (LOWER) MODE 0 INPUT CONFIGURATION

PORT 3 ADDRESS: E6, CONTROL REGISTER ADDRESS: E7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		☒	0		1

DRIVER/TERMINATION NETWORKS: A termination network must be installed at A4.

DATA POLARITY AT J1: Positive true

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		62-63*	Connects bit 0 to J1-24.
		64-65*	Connects bit 1 to J1-22.
		66-67*	Connects bit 2 to J1-20.
		68-69*	Connects bit 3 to J1-18.

PORT RESTRICTIONS - PORT 1: Port 1 must be in mode 0 for all four bits to be available.

PORT 2: Port 2 must be in mode 0 for all four bits to be available.

TABLE 4-24. PORT 6, (LOWER) MODE 0 INPUT CONFIGURATION

PORT 6 ADDRESS: EA, CONTROL REGISTER ADDRESS: EB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		☒	0		1

DRIVER/TERMINATION NETWORKS: A termination network must be installed at A10.

DATA POLARITY AT J2: Positive true.

JUMPER ACTION:

* = Default connection

DELETE	ADD	EFFECT
	81-82*	Connects bit 0 to J2-24.
	83-84*	Connects bit 1 to J2-22.
	85-86*	Connects bit 2 to J2-20.
	87-88*	Connects bit 3 to J2-18.

PORT RESTRICTION - PORT 4: Port 4 must be in mode 0 for all four bits to be available.

PORT 5: Port 5 must be in mode 0 for all four bits to be available.

TABLE 4-25. PORT 3,(UPPER) MODE 0 INPUT CONFIGURATION

PORT 3 ADDRESS: E6, CONTROL REGISTER ADDRESS: E7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		1	☒		☒

DRIVER/TERMINATION NETWORKS: A termination network must be installed at A3.

DATA POLARITY AT J1: Positive true

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		60-61*	Connects bit 4 to J1-26.
		58-59*	Connects bit 5 to J-28.
		56-57*	Connects bit 5 to J-30.
		54-55*	Connects bit 7 to J1-32.

PORT RESTRICTIONS - PORT 1: Port 1 must be in mode 0 for all four bits to be available.

PORT 2: No restriction.

TABLE 4-26. PORT 6, (UPPER) MODE 0 INPUT CONFIGURATION

PORT 6 ADDRESS: EA, CONTROL REGISTER ADDRESS: EB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		1	☒		☒

DRIVER/TERMINATION NETWORKS: A termination network must be installed at A9.

DATA POLARITY AT J2: Positive true

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		79-80*	Connects bit 4 J2-26.
		77-78*	Connects bit 5 to J2-28.
		75-76*	Connects bit 6 to J2-30.
		73-74*	Connects bit 7 to J2-32.

PORT RESTRICTION - PORT 4: Port 4 must be in mode 0 for all four bits to be available.

PORT 5: No restriction.

TABLE 4-27. PORT 3, (LOWER) MODE 0 LATCHED OUTPUT CONFIGURATION

PORT 3 ADDRESS: E6, CONTROL REGISTER ADDRESS: E7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		☒	0		0

DRIVER/TERMINATION NETWORKS: A driver network must be installed at A4.

DATA POLARITY AT J1: Negative true, assuming inverting drivers are used at A4.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		62-63*	Connects bit 0 to J1-24.
		64-65*	Connects bit 1 to J1-22.
		66-67*	Connects bit 2 to J1-20.
		68-69*	Connects bit 3 to J1-18.

PORT RESTRICTIONS - PORT 1: Port 1 must be in mode 0 for all four bits to be available.

PORT 2: Port 2 must be in mode 0 for all four bits to be available.

TABLE 4-28. PORT 6, (LOWER) MODE 0 LATCHED OUTPUT CONFIGURATION

PORT 6 ADDRESS: EA, CONTROL REGISTER ADDRESS: EB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		☒	0		0

DRIVER/TERMINATION NETWORKS: A driver network must be installed at A10.

DATA POLARITY AT J2: Negative true, assuming inverting drivers are used at A10.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		81-82*	Connects bit 0 to J2-24.
		83-84*	Connects bit 1 to J2-22.
		85-86*	Connects bit 2 to J2-20.
		87-88*	Connects bit 3 to J2-18.

PORT RESTRICTIONS - PORT 4: Port 4 must be in mode 0 for all four bits to be available.

PORT 5: Port 5 must be in mode 0 for all four bits to be available.

TABLE 4-29. PORT 3, (UPPER) MODE 0 LATCHED OUTPUT CONFIGURATION

PORT 3 ADDRESS: E6, CONTROL REGISTER ADDRESS: E7

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		0	☒		☒

DRIVER/TERMINATION NETWORKS: A driver network must be installed at A3.

DATA POLARITY AT J1: Negative true, assuming inverting drivers are used at A3.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		60-61*	Connects bit 4 to J1-26.
		58-59*	Connects bit 5 to J1-28.
		56-57*	Connects bit 6 to J1-30.
		54-55*	Connects bit 7 to J1-32.

PORT RESTRICTIONS - PORT 1: Port 4 must be in mode 0 for all four bits to be available.

PORT 2: No restriction.

TABLE 4-30. PORT 6, (UPPER) MODE 0 LATCHED OUTPUT CONFIGURATION

PORT 6 ADDRESS: EA, CONTROL REGISTER ADDRESS: EB

CONTROL WORD FORMAT:

7	6	5	4	3	2	1	0
1	0	0		0	☒		☒

DRIVER/TERMINATION NETWORKS: A driver network must be installed at A9.

DATA POLARITY AT J2: Negative true, assuming inverting drivers are used at A9.

JUMPER ACTION:	DELETE	ADD	EFFECT
* = Default connection		79-80*	Connects bit 4 to J2-26.
		77-78*	Connects bit 5 to J2-28.
		75-76*	Connects bit 6 to J2-30.
		73-74*	Connects bit 7 to J2-32.

PORT RESTRICTIONS - PORT 4: Port 1 must be in mode 0 for all four bits to be available.

PORT 5: No restriction.

TABLE 4-31. PORT 3 RESTRICTION SUMMARY (PORT 1/PORT 2 CONTROL FUNCTIONS)

PORT 3 BIT #	PORT 1 MODE	PORT 2 MODE	FUNCTION	JUMPER ACTION
0	-	1-I/O	Provides INTR$_B$ to PIB$_1$	Delete 62-63
0	2-B	0-I/O	Cannot be used; no drivers/terminators available	Delete 62-63*
1	-	1-I	Provides IBF$_B$ output to J1-22	Add 64-65*
1	-	1-0	Provides OBF$_B$ output to J1-22	Add 64-65*
2	-	1-I	Provides STB$_B$ input from J1-32	Delete 54-55* Delete 66-67* Add 67-54
2	-	1-0	Provides ACK$_B$/ input from J1-32	Delete 54-55* Delete 66-67* Add 67-54
3	1-I/0	-	Provides INTR$_A$ to PIA1	Delete 68-69*
3	2-B	-	Provides INTR$_A$ to PIA1	Delete 68-69*
4	1-I	-	Provides STB$_A$/ input from J1-26	Add 60-61*
4	2-B	-	Provides STB$_A$/ input from J1-26	Add 60-61*
5	1-I	-	Provides IBF$_A$/ output to J1-18	Delete 68-69* Add 59-68
5	2-B	-	Provides IBF$_A$ output to J1-18	Delete 68-69* and 58-59* Add 59-68
6	1-0	-	Provides ACK$_A$/ input from J1-30	Add 56-57*

(Table Continued on Next Page)

TABLE 4-31. PORT 3 RESTRICTION SUMMARY (Continued)

PORT 3 BIT #	PORT 1 MODE	PORT 2 MODE	FUNCTION	JUMPER ACTION
6	2-B	-	Provides ACK_A/ input from J1-30	Add 56-57*
7	0-I/O	1-I/O	Cannot be used; no drivers/terminators available	Delete 54-55*
7	1-0	-	Provides OBF_A output to J1-18	Delete 68-69* Delete 54-55* Add 55-68

NOTE 1: If a Port 3 pin is not shown in this table as having a prescribed function for certain Port 1/Port 2 modes and if a spare driver or termination network is available, that pin can be used as an input or output, as determined by the driver/terminator availability. Unused Port 3 pins can also be connected to the interval Timer input via jumper pins 93 and 95.

NOTE 2:
I = Input
O = Output
I/O = Input or Output
B = Bidirectional
* Denotes default connection

TABLE 4-32. PORT 6 RESTRICTION SUMMARY
(PORT 4/PORT 5 CONTROL FUNCTIONS)

PORT 6 BIT #	PORT 4 MODE	PORT 5 MODE	FUNCTION	JUMPER ACTION
0	-	1-I/O	Provides INTR$_B$ to PIB2	Delete 81-82*
0	2-B	0-I/O	Cannot be used; no drivers/terminators available	Delete 81-82*
1	-	1-I	Provides IBF$_B$ output to J2-22	Add 83-84*
1	-	1-0	Provides OBF$_B$ output to J2-22	Add 83-84*
2	-	1-I	Provides STB$_B$ input from J2-32	Delete 85-86* Delete 73-74* Add 86-73
2	-	1-0	Provides ACK$_B$/ input from J2-32	Delete 85-86* Delete 73-74* Add 86-73
3	1-I/O	-	Provides INTR$_A$ to PIA2	Delete 87-88*
3	2-B	-	Provides INTR$_A$ to PIA2	Delete 87-88*
4	1-I	-	Provides STB$_A$/ input from J2-26	Add 79-80*
4	2-B	-	Provides STB$_A$/ input from J2-26	Add 79-80*
5	1-I	-	Provides IBF$_A$ output to J2-18	Delete 77-78* and 87-88* Add 78-87
5	2-B	-	Provides IBF$_A$ output to J2-18	Delete 77-78* and 87-88* Add 78-87

(Table Continued on Next Page)

TABLE 4-32. PORT 6 RESTRICTION SUMMARY
(Continued)

PORT 6 BIT #	PORT 4 MODE	PORT 5 MODE	FUNCTION	JUMPER ACTION
6	1-0	-	Provides ACK_A/ input from J2-30	Add 75-76*
6	2-B	-	Provides ACK_A/ input from J2-30	Add 75-76*
7	0-I/O	1-I/O	Cannot be used; no drivers/terminators available	Delete 73-74*
7	1-0	-	Provides OBF_A output to J2-18	Delete 73-74* and 87-88* Add 74-87

NOTE 1: If a Port 6 pin is not shown in this table as having a prescribed function for certain Port 4/Port 5 modes and if a spare driver or termination network is available, that pin can be used as an input or output, as determined by the driver/terminator availability. Unused Port 6 pins can also be connected to certain control lines on the Serial I/O interface via jumper pins 89-90, 96 and 97. These include pins shown in the table as unavailable because of a lack of unused drivers and terminators.

NOTE 2: I = Input
O = Output
I/O = Input or Output
B = Bidirectional
* Denotes default connection.

4.4 INTERRUPT PRIORITY OPTIONS

There are two major considerations in configuring a custom interrupt structure on the SBC 80/20:

1) The connection of external and on-board interrupt requests to the eight interrupt priority level inputs (IR0-IR7) on the 8259,

2) The selection of a priority resolution algorithm.

The priority resolution algorithm is selected by programming the 8259 as described in Section 3.10. The assignment of interrupt requests to interrupt priority level inputs is made by connecting the appropriate jumper pins as summarized in Table 4-33.

The interrupt section jumper pad (shown on sheet 6 of the schematic) allows one interrupt request line to be connected directly to each of the first seven 8259 interrupt priority inputs (IR0-IR6). Four other interrupt request lines can be ORed together and applied to the priority seven input (IR7). Any of the four lines that are applied to IR7 must be tied to ground if not connected to an interrupt request line.

4.5 GENERAL OPTIONS

There are several other options that may be useful. Details are provided in the following paragraphs.

4.5.1 DISABLE BUS CLOCK SIGNALS

The bus clock BCLK/ (connector pin P1-13) or the constant clock CCLK/ (P-31) outputs can be disabled (if more drive, or a different

TABLE 4-33. INTERRUPT SECTION JUMPER CONNECTIONS

8259 PRIORITY LEVEL INPUTS	JUMPER[1] PIN (COLUMN A)
IR0	24
IR1	25
IR2	26
IR3	27
IR4	28
IR5	29
IR6	30
IR7	36 37 38 39

INTERRUPT REQUEST LINE	JUMPER[1] PIN (COLUMN B)	SOURCE OF INTERRUPT REQUEST
Transmitter Empty (TXE)	32	Serial I/O Interface
Transmitter Ready (TXR)	40	
Receiver Ready (RXR)	41	
Parallel I/O Port 1 (PIA1)	63	Parallel I/O Interface
Parallel I/O Port 2 (PIB1)	69	
Parallel I/O Port 4 (PIA2)	92	
Parallel I/O Port 5 (PIB2)	88	
INT7/	50	External Edge Connector P1 (P1-36)
INT6/	49	(P1-35)
INT5/	48	(P1-38)
INT4/	47	(P1-37)
INT3/	46	(P1-40)
INT2/	45	(P1-39)
INT1/	44	(P1-42)
INT0/	43	(P1-41)
INTR/	42	(P1-33)
Power Fail Interrupt	33	Power Fail Logic
Output From Counter 0 (OITØ)	35	8253 Interval Timer
Output From Counter 1 (OIT1)	34	
Ground	31	-

[1] Jumper appropriate pins from Column A to those in Column B to tie interrupt lines to desired interrupt request lines.

frequency is needed) by deleting jumpers 110-111 or 112-113, respectively. When connected, both BCLK/ and CCLK/ provide a 9.216 MHz timing reference to other modules. Both jumpers 110-111 and 112-113 are connected when the SBC 80/20 is delivered.

4.5.2 ADVANCED ACKNOWLEDGE INPUT

Certain OEM modules generate an advanced acknowledge, AACK/, in response to memory commands, which allow the memory to complete the access without requiring the CPU to wait. When such modules are used with the SBC 80/20, jumper 135-136 should be added to allow AACK/ to be accepted (at P1-25) and gated to the RDYIN pin on the 8224 Clock generator. Jumper 135-136 is not present when the SBC 80/20 is delivered. Note: With the 80/20, wait states can be reduced with the use of AACK but not eliminated. Also certain timing limits must be adhered to.

4.5.3 BATTERY BACK-UP POWER

If a battery back-up system is to be used with the SBC 80/20, the +5V battery power input must be connected to the SBC 80/20 at connector pins P2-3 and P2-4 and jumper W5 must be removed. Jumper W5 is present when the SBC 80/20 is delivered.

TABLE 4-34. BAUD RATE FACTORS FOR COMMON COMMUNICATION FREQUENCIES

Frequency (kHz, Software Selectable)	Baud Rate (Hz)			Baud Rate Factor (Hex Notation)	
	Synchronous	Asynchronous			
		÷16	÷64	MSB	LSB
153.6	--	9600	2400	00	07
76.8	--	4800	1200	00	0E
38.4	38400	2400	600	00	1C
19.2	19200	1200	300	00	38
9.6	9600	600	150	00	70
4.8	4800	300	75	00	E0
2.4	2400	150	-	01	C0
1.76	1760	110	-	02	63

CHAPTER 5

SYSTEM INTERFACING

This chapter identifies each of the SBC 80/20 external connections and defines all signals on the external system bus.

5.1 ELECTRICAL CONNECTIONS

The SBC 80/20 electronics are mounted on a 12.00 x 6.75 inch printed circuit board that requires maximum average DC current as specified in Table 7-1. Edge connectors at the top of the module are designed for compatibility with both flat cable and round cable hardware. All parallel I/O functions are paired with an independent signal pin (odd pins are ground). This allows flat cable implementation to utilize an alternate signal/ground scheme for reduction of cross talk. Round cables may easily be implemented as twisted pair with an individual ground pin for every return wire. The serial connection hardware has similar flexibility but ground return lines are not as extensive. The connector is wired for RS232C capability, thus, only one signal ground is provided.

The Parallel I/O Interface communicates with external I/O devices via two 50-pin double-sided PC edge connectors (J1 and J2), 0.1 inch centers. External devices can be attached to J1 or J2 using any of the following mating connectors:

J1 and J2 Mating Connectors

Connector Type	Vendor	Part No.
Flat Cable	3M AMP	3415-0001 2-86792-3
Soldered	AMP VIKING TI	2-583715-3 3VH25/1JV-5 H312125
Wire-wrap	TI VIKING CDC ITT	H312125 3VH25/1JND-5 VPB01E43A00A1 EC4A050A1A
Crimp	AMP	1-583717-1

Tables 5-1 and 5-2 provide pin lists for the J1 and J2 connectors, respectively. The following TTL line driver and Intel® terminators are all compatible with the I/O driver sockets in the Parallel I/O Interface:

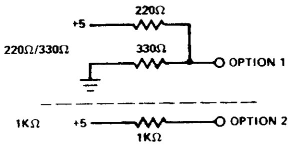
Note: All pin numbers listed in the following tables refer to numbers printed on the board, not to mating connector pin positions. When specifying pin numbers for cable harnesses, use caution since SBC 80/20 pin numbering is not necessarily the same as the connector pin numbering scheme.

Driver	Characteristic	Sink Current (ma)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note: I = inverting; N.I. = non-inverting
OC = open collector

I/O Terminators:

Terminators: 220Ω/330@ divider or 1 kΩ pull up



SBC-901

SBC-902

See Appendix B for schematics.

TABLE 5-1. PIN ASSIGNMENTS FOR CONNECTOR J1
(Parallel I/O Interface - Group 1)

PIN*	SIGNAL	PIN*	SIGNAL
1	GND	2	PORT 2 - BIT 7
3	↑	4	PORT 2 - BIT 6
5		6	PORT 2 - BIT 5
7		8	PORT 2 - BIT 4
9		10	PORT 2 - BIT 3
11		12	PORT 2 - BIT 2
13		14	PORT 2 - BIT 1
15		16	PORT 2 - BIT 0
17		18	PORT 3 - BIT 3
19		20	PORT 3 - BIT 2
21		22	PORT 3 - BIT 1
23		24	PORT 3 - BIT 0
25		26	PORT 3 - BIT 4
27		28	PORT 3 - BIT 5
29		30	PORT 3 - BIT 6
31		32	PORT 3 - BIT 7
33		34	PORT 1 - BIT 7
35		36	PORT 1 - BIT 6
37		38	PORT 1 - BIT 5
39		40	PORT 1 - BIT 4
41		42	PORT 1 - BIT 3
43		44	PORT 1 - BIT 2
45		46	PORT 1 - BIT 1
47	↓	48	PORT 1 - BIT 0
49	GND	50	

* Refers to pin numbers shown on SBC 80/20 at J1.

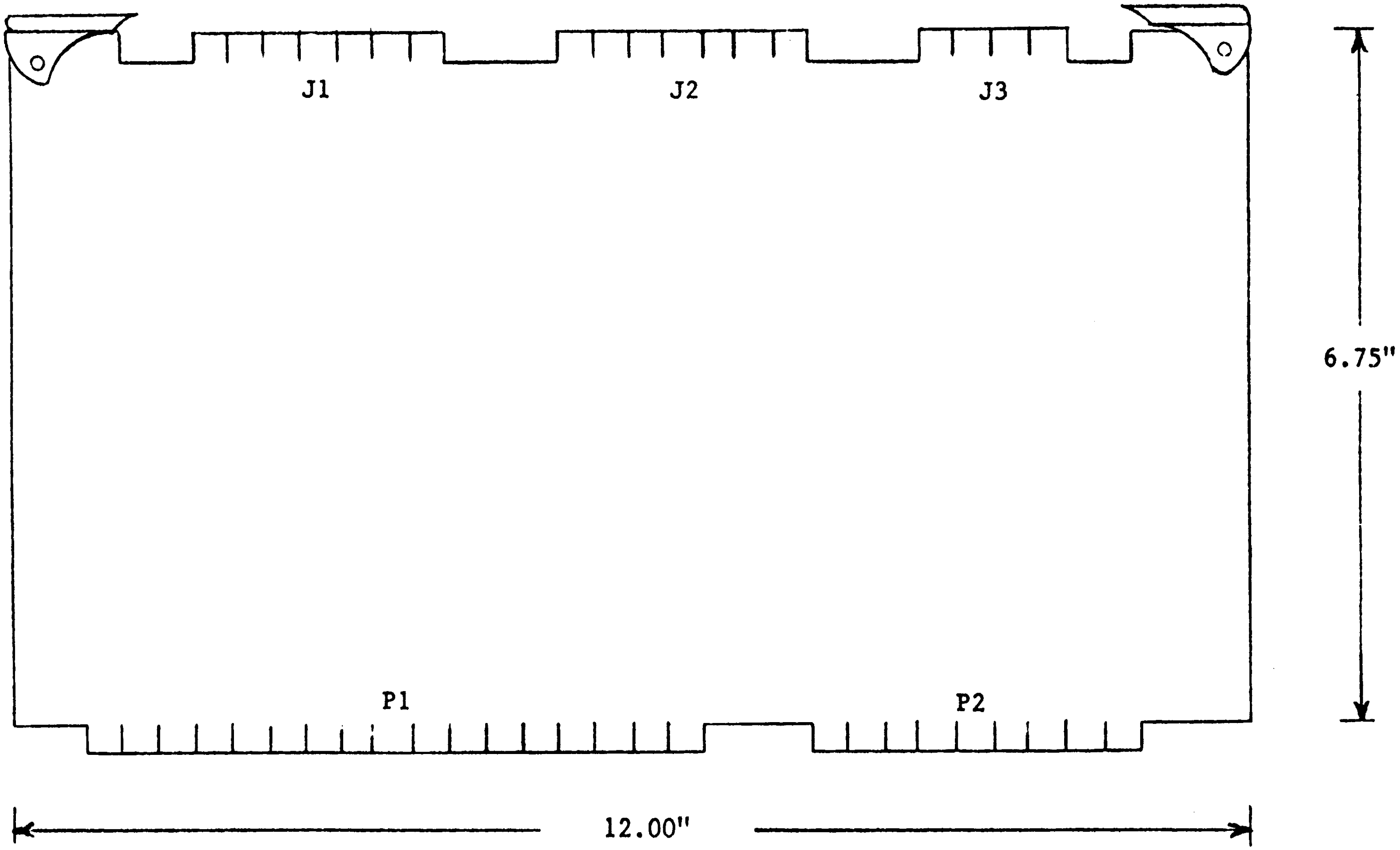


FIGURE 5-1. SBC 80/20 EDGE CONNECTORS

TABLE 5-2. PIN ASSIGNMENTS FOR CONNECTOR J2
(Parallel I/O Interface - Group 2)

PIN*	SIGNAL	PIN*	SIGNAL
1	GND	2	PORT 5 - BIT 7
3	↑	4	PORT 5 - BIT 6
5		6	PORT 5 - BIT 5
7		8	PORT 5 - BIT 4
9		10	PORT 5 - BIT 3
11		12	PORT 5 - BIT 2
13		14	PORT 5 - BIT 1
15		16	PORT 5 - BIT 0
17		18	PORT 5 - BIT 3
19		20	PORT 6 - BIT 2
21		22	PORT 6 - BIT 1
23		24	PORT 6 - BIT 0
25		26	PORT 6 - BIT 4
27		28	PORT 6 - BIT 5
29		30	PORT 6 - BIT 6
31		32	PORT 6 - BIT 7
33		34	PORT 6 - BIT 7
35		36	PORT 4 - BIT 6
37		38	PORT 4 - BIT 5
39		40	PORT 4 - BIT 4
41		42	PORT 4 - BIT 3
43		44	PORT 4 - BIT 2
45	↓	46	PORT 4 - BIT 1
47		48	PORT 4 - BIT 0
49	GND	50	

*Refers to pin numbers shown on SBC 80/20 at J2.

The Serial I/O Interface communicates with an external I/O device via a 26-pin double-sided PC edge connector (J3), 0.1 inch centers. An external device can be connected to J3 using a 3M 3462-0001 flat cable connector or one of the following soldered connectors: TI H312113 or AMP 1-583715-1. Table 5-3 provides a pin list for connector J3.

The SBC 80/20 connects to the system bus via an 86-pin double-sided edge connector (P1), 0.156 inch centers. This edge connector will accept any of the following mating connectors: CDC VPB01E43A000A1, Micro Plastics MP-0156-43-BW-4 or ARCO AE 443WP1. Section 5.2 defines each of the external system bus signals and includes a pin list for P1 (Table 5-5).

TABLE 5-3. PIN ASSIGNMENTS FOR CONNECTOR J3
(Serial I/O Interface)

PIN	SIGNAL	PIN	SIGNAL
1	SEC TRANSMIT DATA	2	PROTECTIVE GROUND
3	TRANS SIG ELE TIMING	4	TRANSMIT DATA
5	SEC RECEIVED DATA	6	RECEIVE DATA
7	REC SIG ELE TIMING	8	REQUEST TO SEND
9		10	CLEAR TO SEND
11	SEC REQUEST TO SEND	12	DATA SET READY
13	DATA TERMINAL READY	14	SIGNAL GND.
15		16	REC LINE SIG DET
17	RING INDICATOR	18	
19	* -12V (TTY ADAPTER POWER)	20	
21	TRANS SIG ELE TIMING	22	+12V (TTY ADAPTER POWER)
23	* +5V	24	
25	SIGNAL GND.	26	SEC CLEAR TO SEND

Note: These pin numbers refer to pin assignments on the SBC 80/20 board at J3. They do not apply to any pin numbers shown on the mating connector. See Table 5-6 for a correlation between J3 pin numbers and the RS232C connector pin numbers.

* Jumpers required to connect power to J3.

The 60-pin double-sided edge connector labeled P2 in Figure 5-1 connects various system signals to SBC 80/20 circuits (see Table 5-4). The mating connector for P2 is an Intel part number MDS-980.

TABLE 5-4. PIN ASSIGNMENTS FOR CONNECTOR P2
(Auxiliary Connector)

SIGNAL MNEMONIC	PIN ASSIGNMENT	COMMENT
BATT GND	P2-1 P2-2	Battery ground
+5V BATT	P2-3 P2-4	Battery power input
PFS/	P2-17	Power Fail Status
PFI/	P2-19	Power Fail Interrupt
MPRO/	P2-20	Memory Protect
HLT/	P2-28	Halt Indicator
WAIT/	P2-30	Processor Wait Indicator
BTMO	P2-34	Bus Timeout
INTA/	P2-36	Interrupt Acknowledge
RESET/	P2-38	System Reset switch input

5.2 SBC 80 SYSTEM BUS SUMMARY

A significant measure of the SBC 80/20's power and flexibility can be attributed to its external system bus. In expanded systems, the external bus structure allows for master-slave relationships between the various system modules. The bus includes its own clock (BCLK) which is derived independently from the processor clock. Actual transfers via the bus, however, proceed asynchronously with respect to the bus clock. Thus, the transfer speed is dependent on the transmitting and receiving devices only. Once a module has gained control of the bus, single or multiple read/write transfers can proceed at a maximum rate of 5 million data bytes per second. The 16 system address lines allow the SBC 80/20 to support up to

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65,536 bytes of storage. The signal lines on the external system bus are defined as follows:

BCLK/ Bus clock; used to synchronize bus control circuits on all master modules. BCLK/ has a period of 108.5 nanoseconds (9.216 MHz frequency), 30% - 70% duty cycle. BCLK/ may be slowed, stopped or single stepped if desired.

INIT/ Initialization signal; resets the entire system to a known internal state.

BPRN/ Bus priority input signal; indicates to the SBC 80/20 that no higher priority master module is requesting use of the system bus. BPRN/ must be synchronized with BCLK/ in multi-master system; BPRN/ must be connected to signal ground in a single-master system.

BPRO/ Bus priority out signal; used with serial (daisy chain) bus priority resolution schemes. BRPR/ is passed to the BPRN/ input of the master module with next lower bus priority.

BREQ/ Bus request signal; used with a parallel bus priority network to indicate that a particular master module requires use of the bus for one or more data transfers. BREQ/ is synchronized with BCLK/

BUSY/ Bus busy signal; indicates that the bus is currently in use. BUSY/ prevents all other master modules from gaining control of the bus.

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MRDC/ Memory read command; indicates that the address of a memory location has been placed on the system address lines and specifies that the contents of the addressed location are to be read and placed on the system data bus.

MWTC/ Memory write command; indicates that the address of a memory location has been placed on the system address lines and that a data word has been placed on the system data bus. MWTC/ specifies that the data word is to be written into the addressed memory location.

IORC/ I/O read command; indicates that the address of an input port has been placed on the system address bus and that the data at that input port is to be read and placed on the system data bus.

IOWC/ I/O write command; indicates that the address of an output port has been placed on the system address bus and that the contents of the system data bus are to be output to the addressed port.

XACK/ Transfer acknowledge signal; the required response of an external memory location or I/O port which indicates that the specified read/write operation has been completed. That is, data has been placed on, or accepted from, the system data bus lines.

AACK/ Advanced acknowledge signal; used with 8080 CPU-based systems. AACK/ is an advance acknowledge,

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in response to a memory read command, that allows the memory to complete the access without requiring the CPU to wait.

CCLK/ — Constant clock; provides a clock signal of constant frequency (9.216 MHz for use by optional memory and I/O expansion boards. CCLK/ coincides with BCLK/ and has a period of 108.5 nanoseconds, 30% - 70% duty cycle.

INT0/-INT7 and INTR — Externally generated interrupt requests.

ADR0/-ADRF/ — 16 Address lines; used to transmit the address of the memory location or I/O port to be accessed. ADRF/ is the most significant bit.

DAT0/-DAT7/ — Bi-directional data lines; used to transmit/receive information to/from a memory location or I/O port. DAT7/ is the most significant bit.

5.3 RS232C CABLING

The J3 edge connector can be cabled such that a RS232C pin-compatible connector is presented to the user's terminal or modem. A 26-pin mating connector, 3M 3462-0001, should be attached to the J3 edge connector on the SBC 80/20 and to a 25-wire flat cable, 3M 3349/25. The flat cable is, in turn, attached to the RS232C pin-compatible connector, 3M 3483-1000. Table 5-6 equates the J3 edge connector pins with the associated RS232-compatible pins on the 3M 3483-1000 connector.

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TABLE 5-5. PIN ASSIGNMENTS FOR CONNECTOR P1
(External System Bus)

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
	1	GND	Signal GND	2	GND	Signal GND
	3	VCC	+ 5VDC	4	VCC	+ 5VDC
POWER SUPPLIES	5	VCC	+ 5VDC	6	VCC	+ 5VDC
	7	VDD	+12VDC	8	VDD	+12VDC
	9	VBB	- 5VDC	10	VBB	- 5VDC
	11	GND	Signal GND	12	GND	Signal GND
	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	[2]BPRN/	Bus Pri. In	16	BPRO/	Bus Priority Out
BUS CONTROLS	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknow	24	[1]	
	25	AACK/	Advanced	26	[1]	
	27		Acknowledge	28		
SPARES	29			30		
	31	CCLK/	Constant Clock	32		
	33	INTR/	Direct Interrupt	34		
	35	INT6/	Parallel	36	INT7/	Parallel
INTERRUPTS	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/	Address	48	ADRB/	Address
ADDRESS	49	ADR8/	Bus	50	ADR9/	Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
	59	[1]		60	[1]	
	61	[1]		62	[1]	
DATA	63	[1]		64	[1]	
	65	[1]		66	[1]	
	67	DAT6/		68	DAT7/	
	69	DAT4/	Data Bus	70	DAT5/	Data Bus
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
	75	GND	Signal GND	76	GND	Signal GND
		[1]		78	[1]	
POWER SUPPLIES	79	VAA	-12VDC	80	VAA	-12VDC
	81	VCC	+ 5VDC	82	VCC	+ 5VDC
	83	VCC	+ 5VDC	84	VCC	+ 5VDC
	85	GND	Signal GND	86	GND	Signal GND

[1] Used by Intellec System Bus

[2] Connect to signal ground in single master systems

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TABLE 5-6. J3/RS232C CONNECTOR PIN CORRESPONDENCE

J3 CONNECTOR PIN NO.	RS232C CONNECTOR PIN NO.
1	14
2	1
3	15
4	2
5	16
6	3
7	17
8	4
9	18
10	5
11	19
12	6
13	20
14	7
15	21
16	8
17	22
18	9
19	23
20	10
21	24
22	11
23	25
24	12
25	--

Note: The J3 pin numbers refer to pin assignments shown on the SBC 80/20 board at J3.

CHAPTER 6

COMPATIBLE EQUIPMENT

The SBC 80/20 is designed to operate with several other OEM modules. It is mechanically compatible with both Intellec® System chassis requirements and SBC-604 and SBC-614 4-module card holder, designed specifically for OEM applications. Details are presented in the following sections.

6.1 MASTER MODULES

The SBC 80/20 module can operate in systems that include other master modules. The SBC 80/20's bus interface logic allows it to compete for control of the system bus, and its override capability permits it to retain control of the bus for multiple data transfers.

6.2 SBC-104 AND SBC-108 COMBINATION MEMORY AND I/O EXPANSION BOARDS

The SBC 80/20 is completely compatible with the SBC-104 and SBC-108 Combination Memory and I/O Boards. The SBC 80/20 can be interfaced with up to 10 such combination boards.

Each Combination Board includes 48 programmable I/O lines, an RS232C communications interface, and capacity for up to 4K bytes of EPROM/ROM memory. In addition, the SBC-104 provides 4K bytes of RAM memory and the SBC-108 provides 8K bytes of RAM memory. Eight interrupt request lines and a pending interrupt request register are on the board. Memory, I/O and interrupt register addresses are jumper selectable.

6.3 SBC-016 RAM MODULE

SBC-016 16K RAM modules allow the user to expand the read/write storage capability of this system in increments of 16,384 bytes. This RAM module includes thirty-two 2107 dynamic RAM elements (4096 bits each). Because the RAM elements are dynamic, they require periodic refreshing which is provided by logic on the module. Up to three 16K RAM modules can be interfaced to the SBC 80/20.

6.4 SBC-406 6K PROM MODULE

SBC-406 6K PROM modules allow the user to expand the read only storage capability of his system in increments of 2K, 4K or 6K bytes. This PROM module can include up to twenty-four 8702A PROM devices (256 X 8-bits each). Intel's 1702A PROM's or 1302 ROM's (both pin compatible with the 8702A) can also be used on the PROM module, in place of the 8702A's.

The 24 memory devices are organized into a 4K (4096) byte memory bank and a 2K (2048) byte memory bank. The user independently selects the address range for the 4K and 2K memory banks on 4K and 2K boundaries, respectively. Up to ten 6K PROM modules can be interfaced to the SBC 80/20.

Note: The 6K PROM module requires a -10V supply in addition to standard OEM voltages.

6.5 SBC-416 16K PROM MODULE

The SBC-416 allows the user to expand his nonvolatile memory with 8708 EPROMs or 8308 ROMs in 1K bytes. Address locations for memory on the board are jumper selectable in 4K blocks. Beginning addresses for any block of memory must start at a multiple of 4K (0, 4K, 8K, 12K, etc.). Up to four 16K PROM modules can be interfaced to the SBC 80/20.

6.6 SBC-508 GENERAL PURPOSE I/O MODULE

The SBC-508 GP I/O module includes four input and four output ports. Each output port latches 8-bit data words and issues a framed strobe pulse, of selectable duration, to the peripheral device. All outputs are driven by TTL level buffer drivers. Each input port also supports 8-bits of data, latched or unlatched. All inputs are terminated by dual-in-line socket-mounted resistor packs. The I/O module also includes provisions for accepting eight external interrupt requests, buffering them and driving them to a CPU module.

Up to nine GP I/O modules can be interfaced to the SBC 80/20. I/O addresses selected for the GP I/O module in this application which coincide with the SBC 80/20's dedicated addresses are not accessible to the SBC 80/20.

6.7 MODULAR BACKPLANE AND CARDCAGE

The SBC-604/614 Modular Backplane and Cardcage is designed specifically for OEM modules such as the SBC 80/20. Each card holder supports up to 4 modules. The modules may be electrically and mechanically "ganged" together for expanded capability. Provisions for power supply distribution, air circulation and bus exchange functions are featured on the OEM card holders.

6.8 INTELLEC®MICROCOMPUTER DEVELOPMENT SYSTEM CARDCAGE

The mechanical characteristics of the Intellec®Microcomputer Development System cardcage are compatible with the SBC 80/20.

Note: Intellec®Microcomputer Development System power supplies do not support a -5V supply although a -5V bus conductor is built into the cardcage motherboard. An auxiliary power supply or converter connected to this line will suffice.

CHAPTER 7

SBC 80/20 SPECIFICATIONS

7.1 DC POWER REQUIREMENTS

DC power requirements are given in Table 7-1.

7.2 AC CHARACTERISTICS

AC characteristics are given in Table 7-2 and Figures 7-1 and 7-2.

7.3 DC CHARACTERISTICS

DC characteristics are given in Tables 7-3, 7-4 and 7-5.

7.4 ENVIRONMENT

Temperature extremes can cause instability, or result in permanent damage to the circuits on the module. Ambient temperature must, therefore, be maintained within the limits of $0^{o}C$ to $55^{o}C$. Exercise caution in locating the module, giving particular attention to radiant and conducive sources of heat. Remember that the module itself, when installed, will contribute some heat to the environment. Maintain an adequate clearance to permit the convective dissipation of heat from the elements on the card.

Relative humidity should not exceed 90%, non-condensing.

7.5 SBC 80/20 BOARD OUTLINE

See Figure 7-3.

7.6 SBC 80/20 COMPATIBLE CONNECTORS

Table 7-6 lists compatible connectors which mate to the SBC 80/20 PC edge connectors.

Table 7-1. DC POWER REQUIREMENTS

	1	2	3	4	5
V_{CC} = +5V ± 5%	I_{CC} = 4.9A max.	I_{CC} = 4.0A max.	I_{CC} = 4.9A max.	I_{CC} = 800mA max.	I_{CC} = 5.2A max.
V_{DD} = +12V ± 5%	I_{DD} = 350mA max.	I_{DD} = 90mA max.	I_{DD} = 450mA max.		I_{DD} = 90mA max.
V_{BB} = -5V ± 5%	I_{BB} = 180mA max.	I_{BB} = 2mA max.	I_{BB} = 180mA max.		I_{BB} = 2mA max.
V_{AA} = -12V ± 5%	I_{AA} = 20mA max.	I_{AA} = 20mA max.	I_{AA} = 120mA max.		I_{AA} = 20mA max.

Notes:

1 The values assume that four 8708 PROM's are present and that eight optional 220/330 termination networks being driven low have been installed in the Parallel I/O Interface.

2 These values assume that the 8708 PROM's and optional termination networks are not present.

3 The same as 1 with the SBC 530 connected.

4 This value is for RAM only, used for battery backup requirements.

5 The same as 1 with four 2716 PROM's instead of 8708 PROM's.

TABLE 7-2. AC CHARACTERISTICS

PARAMETER	OVERALL		READ		WRITE		DESCRIPTION	REMARKS
	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)		
t_{AS}	50		50		50		Address Setup Time to Command	
t_{AH}	50		50		50		Address Hold Time from Command	
t_{DS}	50				50		Data Setup Time to Command	
t_{DH}	50				50		Data Hold Time from Command	
t_{CY}	464	466					CPU Cycle Time	
t_{CD}			586		695		Command Width	ASSUME BUS AVAILABLE
$t_{CS1,2}$			327		770		Command Separation	Read to Read Write to Write BUS EXCHANGE MODE
t_{CS3}			1157				Command Separation	Read to Write
t_{CS4}					471		Command Separation	Write to Read
$t_{ACKØ}$			-458	-156	-503	-452	First ACK Sampling Point from Command	No Wait States
t_{ACK1}			7	309	-38	13	Second ACK Sampling Point from Command	One Wait State
t_{ACK2}			472	774	427	478	Third ACK Sampling Point from Command	Two Wait States
			-111	0	-503	-452	First ACK Sampling Point from Command	No Wait States OVERRIDE MODE AFTER ACQUIRING THE BUS
			354	465	-38	13	Second ACK Sampling Point from Command	One Wait State
			819	930	427	478	Third ACK Sampling Point from Command	Two Wait States
t_{ACKD}			280				Advanced Acknowledge to Stable Data	When AACK is used.
t_{PPD}		63					Parallel Priority Resolution Delay	BREQ/ to BPRN/
t_{XKO}	0	100	0	100	0	100	AACK or XACK Turn Off Delay	
t_{BWS}	35	∞					Bus Clock Low or High Intervals	Supplied by system.
t_{BS}	23						BPRN to BCLK Setup Time	
t_{DBY}		55					BCLK to Busy Delay	
t_{PNO}		30					BPRN to BPRO Delay	
t_{BCY}	108	109					Bus Clock Period (BCLK)	From SBC 80/20 when properly terminated.
t_{BW}	35	74					Bus Clock Low or High Intervals	
t_{INT}	3000						Initialization Width	After all voltages have stabilized.

See Figures 7-1 and 7-2 in this section for timing diagrams.

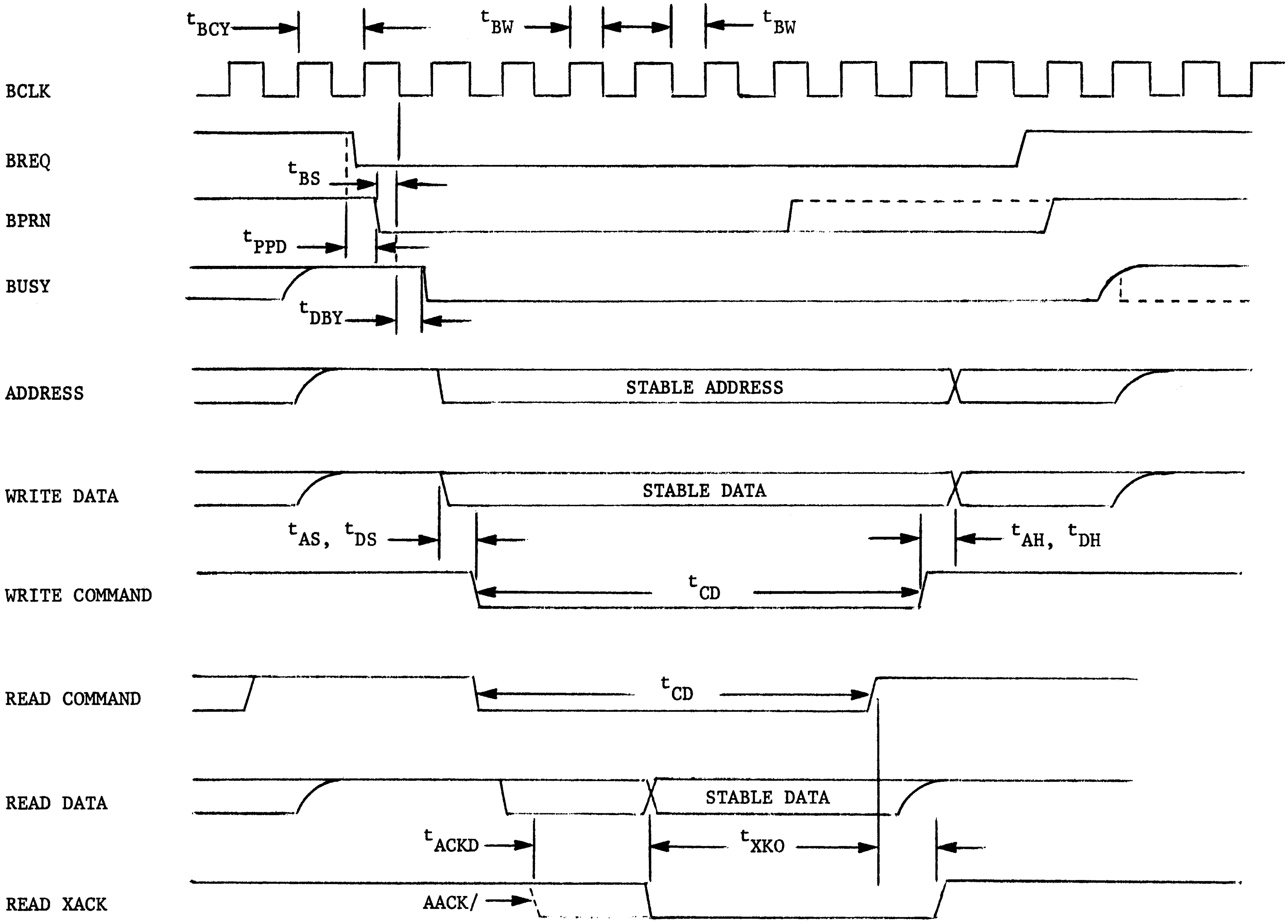


FIGURE 7-1. BUS EXCHANGE TIMING

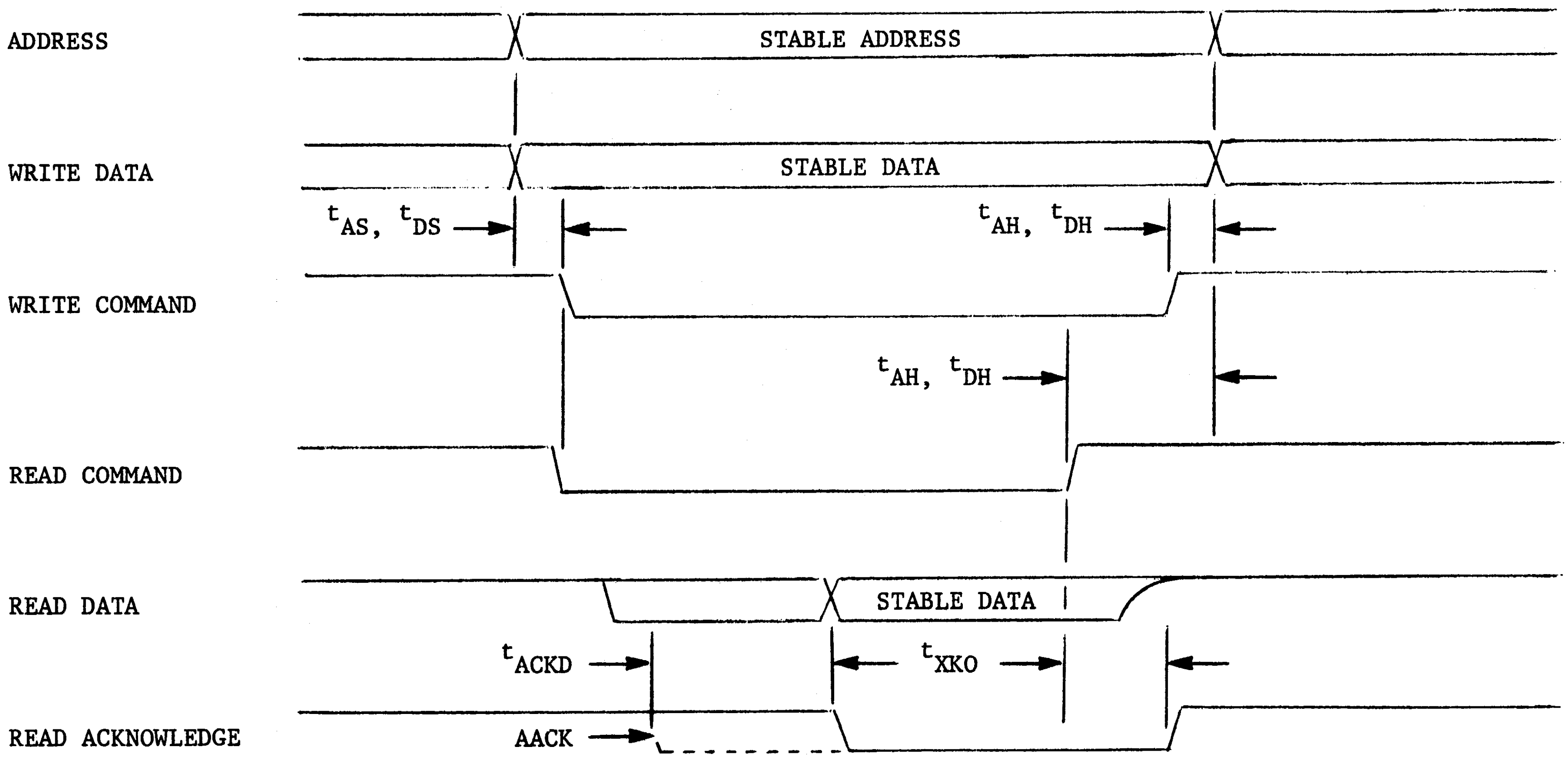


FIGURE 7-2. CONTINUOUS BUS CONTROL TIMING

TABLE 7-3. SBC 80/20 BUS DC CHARACTERISTICS (P1)

SIGNALS	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNITS
ADRØ/-ADRF/	V_{OL}	Output Low Voltage	I_{OL} = 50 mA		0.6	V
	V_{OH}	Output High Voltage	I_{OH} = -10 mA	2.4		V
	I_{LH}	Output Leakage High	V_O = 5.25V		100	µA
	I_{LL}	Output Leakage Low	V_O = 0.45V		100	µA
	C_L	Capacitive Load			18	pF
MROC/,MWTC/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.45	V
IORC/,IOWC/	V_{OH}	Output High Voltage	I_{OH} = -2 mA	2.4		V
	I_{LH}	Output Leakage High	V_O = 5.25V		100	µA
	I_{LL}	Output Leakage Low	V_O = 0.45V		100	µA
	C_L	Capacitive Load			15	pF
DATØ/-DAT7/	V_{OL}	Output Low Voltage	I_{OL} = 50 mA		0.6	V
	V_{OH}	Output High Voltage	I_{OH} = -10 mA	2.4		V
	V_{IL}	Input Low Voltage			0.95	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.25	mA
	I_{LH}	Output Leakage High	V_O = 5.25V		100	µA
	I_{LL}	Output Leakage Low	V_O = 0.45V		100	µA
	C_L	Capacitive Load			18	pF
INTØ/-INT7/	V_{IL}	Input Low Voltage			0.8	V
INTR/,XACK/	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-1.6	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		40	µA
	C_L	Capacitive Load			18	pF
AACK/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-3.9	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		-1.4	mA
	C_L	Capacitive Load			18	pF
BUSY/	V_{OL}	Output Low Voltage	I_{OL} = 20 mA		0.45	V
(OPEN COLLECTOR)	C_L	Capacitive Load			20	pF
INIT/	V_{OL}	Output Low Voltage	I_{OL} = 44 mA		0.4	V
(SYSTEM RESET)	V_{OH}	Output High Voltage	OPEN COLLECTOR			
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = .4V		-4.2	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		-1.4	mA
	C_L	Capacitive Load			15	pF

TABLE 7-3. SBC 80/20 BUS DC CHARACTERISTICS (P1) - CONTINUED

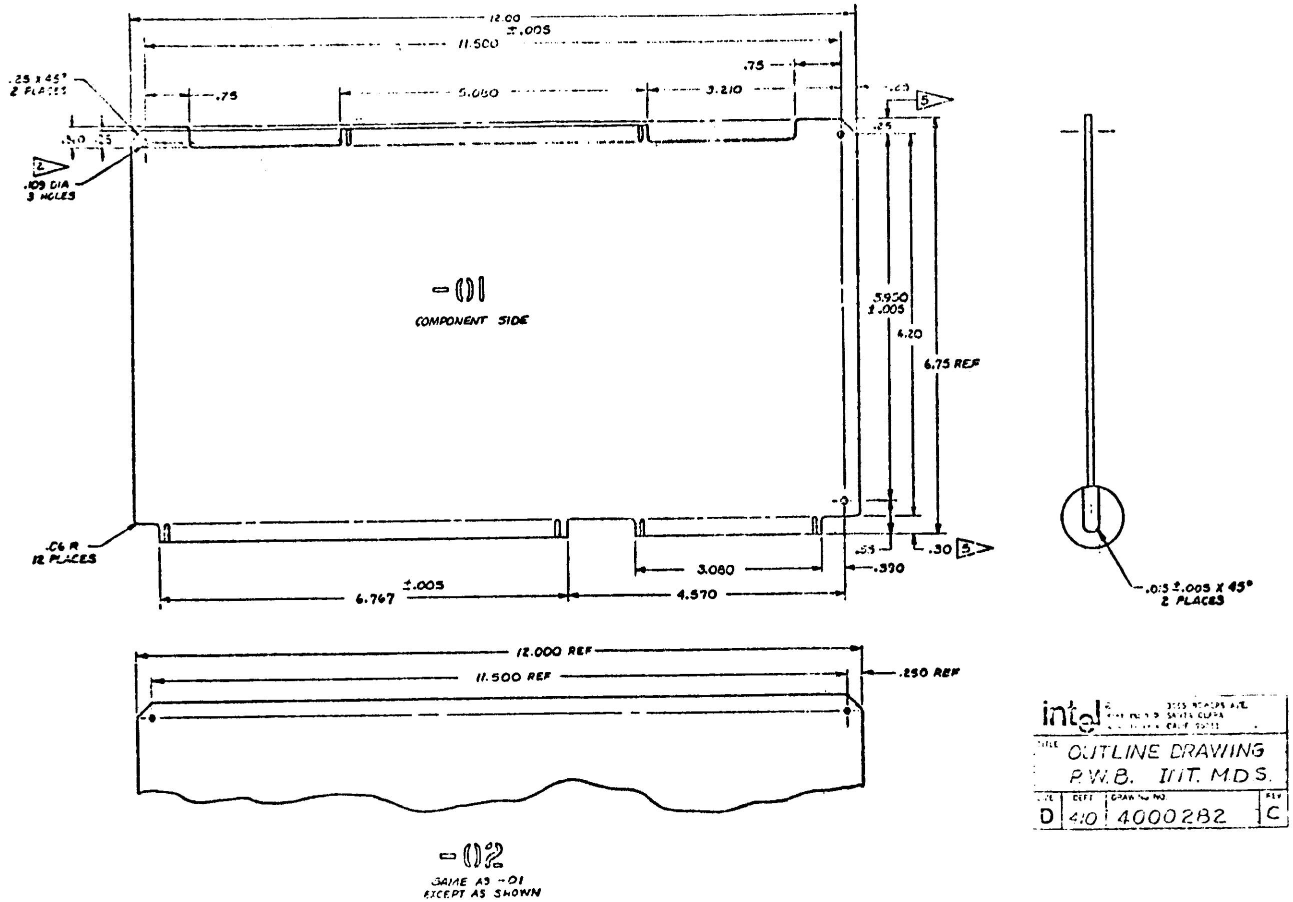
SIGNALS	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNITS
BCLK/	V_{OL}	Output Low Voltage	I_{OL} = 59.5 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -3 mA	2.7		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		40	μA
	C_L	Capacitive Load			15	pF
CCLK/	V_{OL}	Output Low Voltage	I_{OL} = 60 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -3 mA	2.7		V
	C_L	Capacitive Load			15	pF
BPRO/	V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -0.4 mA	2.4		V
	C_L	Capacitive Load			10	pF
BREQ/	V_{OL}	Output Low Voltage	I_{OL} = 20 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -0.4 mA	2.4		V
	C_L	Capacitive Load			10	pF

TABLE 7-4. SBC 80/20 AUXILIARY CONNECTOR DC CHARACTERISTICS (P2)

SIGNALS	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNITS
PFS/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.4		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-1,6	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		40	μA
	C_L	Capacitive Load			5	pF
RESET/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.6		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-.25	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		10	μA
	C_L	Capacitive Load			10	μF
HLT/	V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.4	V
	V_{OH}	Output High Voltage	I_{OH} = -400 μA	2.4		V
	C_L	Capacitive Load			20	pF
WAIT/	V_{OL}	Output Low Voltage	I_{OL} = 14.4 mA		0.4	V
	V_{OH}	Output High Voltage	I_{OH} = -360 μA	2.4		V
	C_L	Capacitive Load			20	pF
INTA/	V_{OL}	Output Low Voltage	I_{OL} = 8 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -1 mA	2.4		V
	C_L	Capacitive Load			20	pF
MPRO/	V_{IL}	Input Low Voltage			0.85	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-2.3	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		10	μA
	C_L	Capacitive Load			5	pF

TABLE 7-5. SBC 80/20 PARALLEL I/O DC CHARACTERISTICS (J1 and J2)

SIGNALS	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNITS
PORTS E4 AND E8	V_{OL}	Output Low Voltage	I_{OL} = 20 mA		.45	V
BIDIRECTIONAL	V_{OH}	Output High Voltage	I_{OH} = -12 mA	2.4		V
DRIVERS	V_{IL}	Input Low Voltage			.95	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45		-5.25	mA
	C_L	Capacitive Load			18	pF
8255	V_{OL}	Output Low Voltage	I_{OL} = 1.7 mA		.45	V
DRIVER/ RECEIVER	V_{OH}	Output High Voltage	I_{OH} = -50 μA	2.4		V
	V_{IL}	Input Low Voltage			.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45		10	μA
	I_{IH}	Input Current at High V	V_{IN} = 5.0		10	μA
	C_L	Capacitive Load			18	pF



NOTES:

1. MATERIAL : .062 THK, 1 OZ COPPER CLAD, NATURAL EPOXY GLASS, TYPE G10 (.062 AFTER PLATING THRU)
2. BOARD EDGES ARE LOCATED FROM INDEX HOLES. INDEX HOLES ARE ON .050 GRID INTERSECTION AND ARE USED FOR ARTWORK REGISTRATION AND MAY BE USED AS TOOLING HOLES, PLATING OPTIONAL.
3. HOLES ARE PLATED THRU WITH COPPER WALL THICKNESS OF .0007 MINIMUM.
4. HOLE SIZES SPECIFIED ARE AFTER PLATING; ±.003 TOLERANCE
5. CONTACT FINGERS ARE OVERPLATED WITH A MINIMUM OF 50 MILLIONTHS GOLD OVER NICKEL TO DIMENSION SHOWN.
6. APPLY SOLDER MASK OVER SOLDER PLATE USING MATERIAL; MECUMASK GREEN
7.
8. DRILL FROM CIRCUIT SIDE.
9. TRACE WIDTHS MUST BE WITHIN .004 OF ARTWORK NEGATIVES.
10. APPLY SILKSCREEN ON COMPONENT SIDE, AFTER SOLDER MASK IS APPLIED, USING WHITE EPOXY INK.

FIGURE 7-3. SBC 80/20 AND 80/20-4 BOARD OUTLINE
(1 of 2 sheets)

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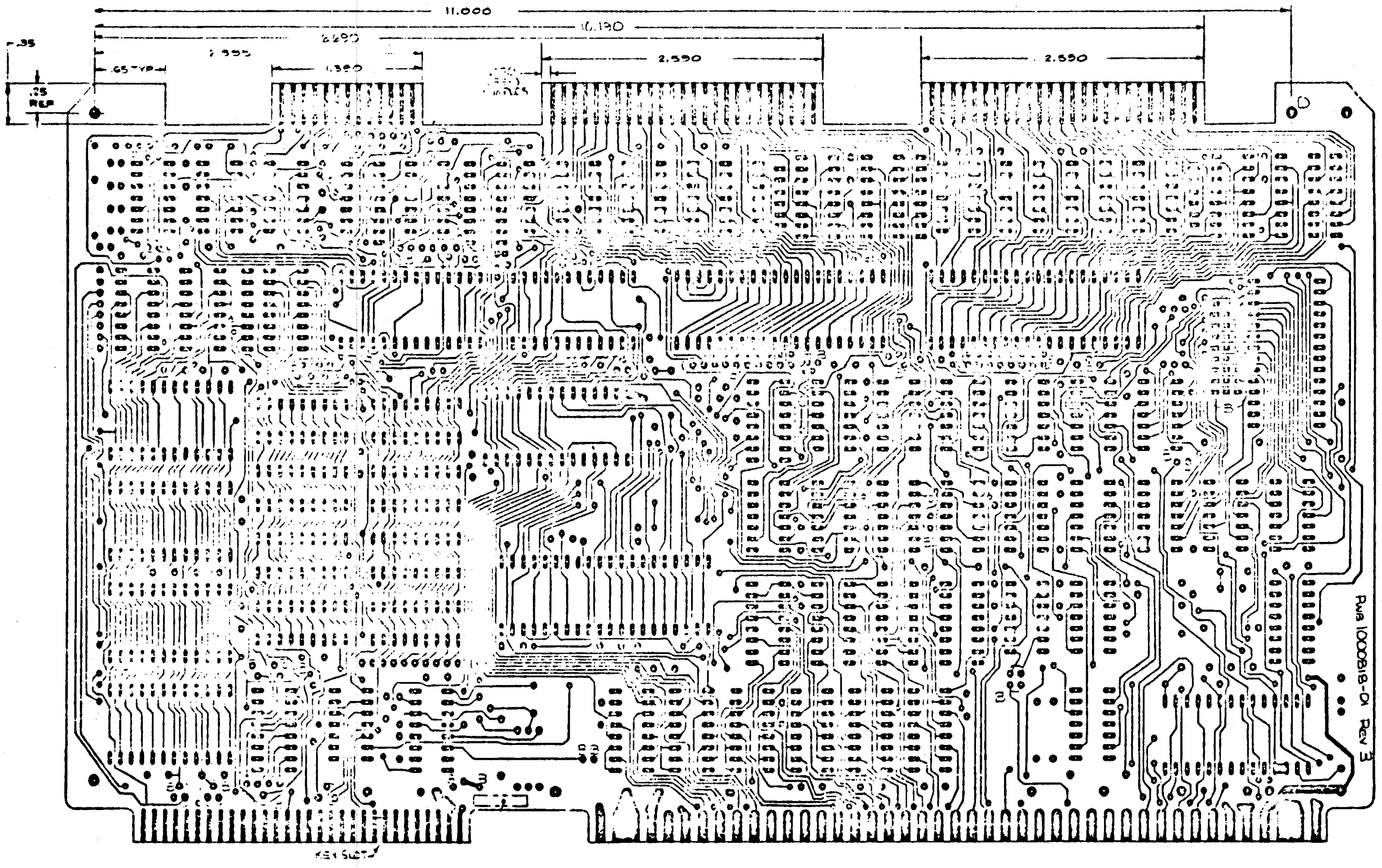

SOLDER SIDE

FIGURE 7-3. SBC 80/20 AND SBC 80/20-4 BOARD OUTLINE (2 of 2 sheets)

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intel
3065 BOWERS AVE
SANTA CLARA
CALIF 95051

PRINTED WIRING BOARD
SINGLE BOARD COMP. 80/20

SIZE	DEPT	DRAWING NO	REV
D	410	E1000818	3

TABLE 7-6. SBC BOARDS COMPATIBLE CONNECTOR HARDWARE

FUNCTION	# OF PINS	CENTERS (inches)	CONNECTOR TYPE	VENDOR	VENDOR PART #	INTEL PART #
PARALLEL I/O	25/50	0.1	FLAT CRIMP ↓	3M 3M AMP ANSLEY SAE	3415-0000 WITH EARS 3415-0001 W/O EARS 88083-1 609-5015 SD6750 SERIES	SBC-956 (CABLE ASSY.)
SERIAL I/O	13/26	0.1	FLAT CRIMP ↓	3M AMP ANSLEY SAE	3462-0001 CRIMP 88106-1 609-2615 SD6726 SERIES	SBC-955 (CABLE ASSY.)
PARALLEL I/O	25/50	0.1	SOLDERED ↓	AMP VIKING TI	2-583485-6 3VH25/1JV5 H312125	N/A
SERIAL I/O	13/26	0.1	SOLDERED ↓	TI AMP	H312113 1-583485-5	N/A
AUXILIARY [1]	30/60	0.1	SOLDERED ↓	VIKING TI	3VH30/1JN5 H312130	N/A
BUS [1]	43/86	0.156	SOLDERED ↓	CDC MICRO PLASTICS ARCO VIKING	VPB01E43D00A1 [3] MP-0156-43-BW-4 AE443WP1 LESS EARS 2VH43/1AV5	N/A
[1] PARALLEL I/O	25/50	0.1	WIREWRAP ↓	TI VIKING CDC ITT CANNON	H311125 3VH25/1JND5 VPB01B25D00A1 [3] EC4A050A1A	N/A
SERIAL I/O [1]	13/26	0.1	WIREWRAP	TI	H311113	N/A
AUXILIARY [2] [1]	30/60	0.1	WIREWRAP ↓	CDC TI	VPB01B30A00A2 [3] H311130	MDS-980
BUS [2] [1]	43/86	0.156	WIREWRAP ↓	CDC CDC VIKING	VFB01E43D00A1 or [3] VPB01E43A00A1 2VH43/1AND5	MDS-985
SBC 201 SBC 501 SBC 508 SBC 905, etc.	50/100	0.1	SOLDER TAIL	VIKING	3VH50/1JN5	MDS-990
			SOLDER PAK (RAYCHEM)	CDC	VPB04B50E00A1E [3]	N/A

[1] Connector heights are not guaranteed to conform to OEM packaging equipment. Intel OEM and Intellec® Development System motherboards offer complete mechanical compatibility.

[2] Wirewrap pin lengths are not guaranteed to conform to OEM packaging equipment. Intel connectors and OEM and Intellec® Development System motherboards offer complete mechanical compatibility.

[3] CDC VPB01 ..., VPB02 ..., VPB04 ..., etc. are identical connectors with different electroplating thicknesses or metal surfaces.

NOTE: See next page for vendor addresses, telephone numbers and TWX numbers.

VENDORS ADDRESSES

The following information is for our customers' convenience only. Intel does not represent these vendors, guarantee availability nor continued quality of their products.

CDC CONNECTOR DIVISION
31829 W. LaTienda Drive
Westlake Village, CA 91361

213-889-3535
TWX 910-494-1224

VIKING INDUSTRIES, INC.
21001 Nordhoff Street
Chatsworth, CA 91311

213-341-4330
TWX 910-494-2094

Connector Systems
TEXAS INSTRUMENTS, INC.
34 Forest Street
Attleboro, MA 02703

617-222-2800

AMP INCORPORATED
P.O. Box 3608
Harrisburg, PA 17105

717-564-0100
TWX 510-657-4110

T & B/ANSLEY
Subsidiary of Thomas & Betts Corp.
3208 Humbolt Street
Los Angeles, CA 90031

213-223-2331
TWX 910-321-3938

STANFORD APPLIED ENG., INC. (SAE)
340 Martin Street
Santa Clara, CA 95050

408-243-9200
TWX 910-338-0132

3M Connectors
Electronic Products Div., Bldg. 223-4E
3M COMPANY
3M Center
St. Paul, MN 55101

612-733-1110

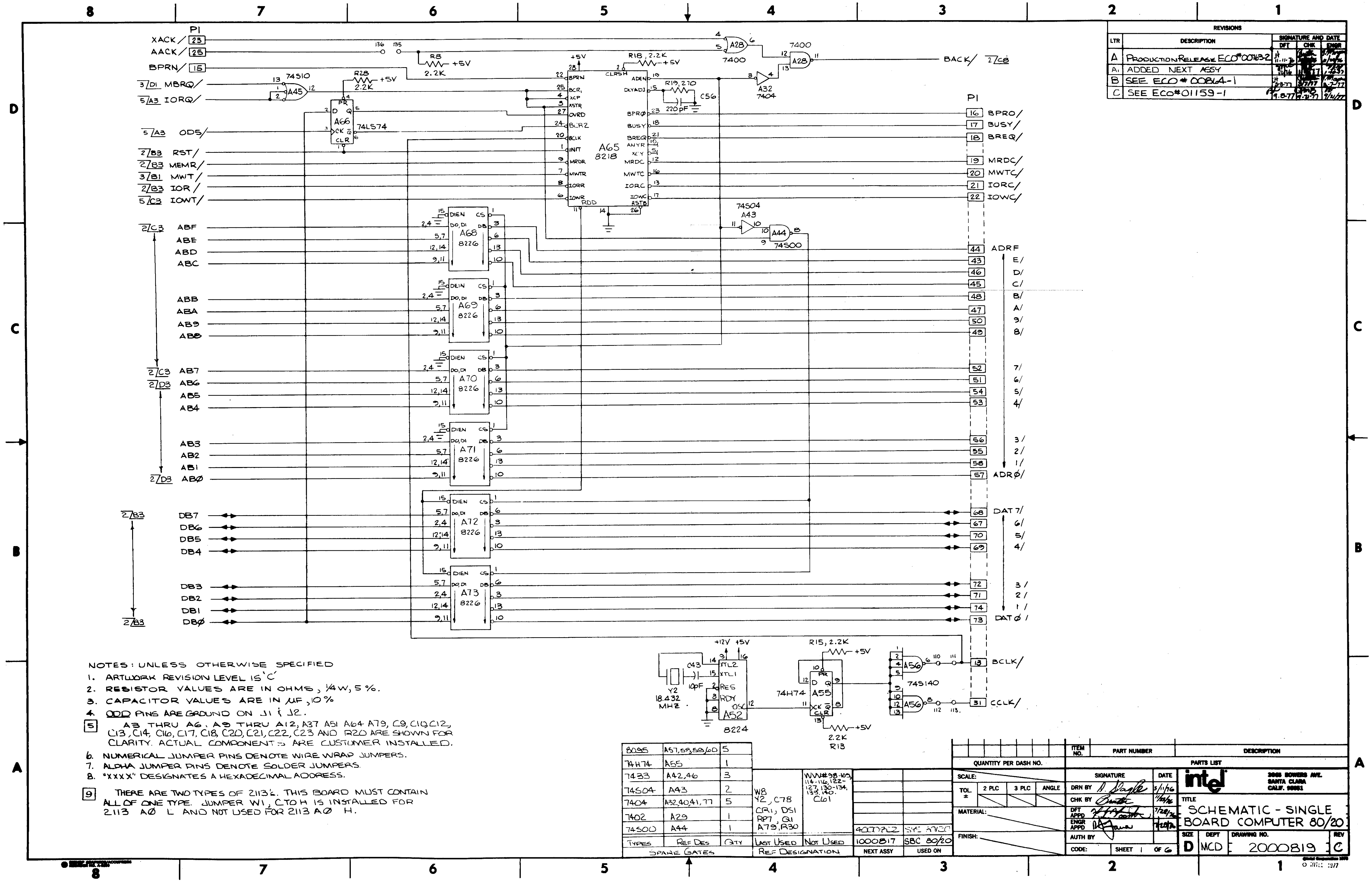
ITT CANNON ELECTRIC
666 East Dyer Road
Santa Ana, CA 92702

800-854-3573
800-432-7063 (in California)

APPENDIX A

SBC 80/20 and SBC 80/20-4 SCHEMATICS

Schematic drawings for the SBC 80/20 and SBC 80/20-4 are provided in this appendix. Information and diagrams in this section are subject to change without notice. References should be made to schematics shipped with this product.



NOTES: UNLESS OTHERWISE SPECIFIED

1. ARTWORK REVISION LEVEL IS 'C'
2. RESISTOR VALUES ARE IN OHMS, ¼W, 5%.
3. CAPACITOR VALUES ARE IN µF, 10%
4. ODD PINS ARE GROUND ON J1 & J2.

[5] A3 THRU A6, A9 THRU A12, A37 A51 A64 A79, C9, C10, C12, C13, C14, C16, C17, C18, C20, C21, C22, C23 AND R20 ARE SHOWN FOR CLARITY. ACTUAL COMPONENTS ARE CUSTUMER INSTALLED.

6. NUMERICAL JUMPER PINS DENOTE WIRE WRAP JUMPERS.
7. ALPHA JUMPER PINS DENOTE SOLDER JUMPERS.
8. "XXXX" DESIGNATES A HEXADECIMAL ADDRESS.

[9] THERE ARE TWO TYPES OF 2113's. THIS BOARD MUST CONTAIN ALL OF ONE TYPE. JUMPER W1, C TO H IS INSTALLED FOR 2113 AØ L AND NOT USED FOR 2113 AØ H.

REVISIONS				
LTR	DESCRIPTION	SIGNATURE AND DATE		
		DFT	CHK	ENGR
A	PRODUCTION RELEASE ECO#00763-2	JH 11-11-76	[illegible]	[illegible] 11/29/76
A1	ADDED NEXT ASSY	[illegible]	[illegible]	[illegible]
B	SEE ECO # 00864-1	JH 3-8-77	3/7/77	3-7-77
C	SEE ECO#01159-1	9.8-77	9-21-77	9/21/77

8095	A57,58,59,60	5
74H74	A55	1
7433	A42,46	3
74S04	A43	2
7404	A32,40,41,77	5
7402	A29	1
74S00	A44	1
TYPES	REF DES	QTY
SPARE GATES		

W8 Y2, C78 CR1, DS1 RP7, Q1 A79, R30	WW#98-109, 114-116, 122-127, 130-134, 139, 140. C61
LAST USED	NOT USED
REF DESIGNATION	

4000822	SYS 80/20
1000817	SBC 80/20
NEXT ASSY	USED ON

ITEM NO.	PART NUMBER	DESCRIPTION
PARTS LIST		

QUANTITY PER DASH NO.

SCALE:

TOL. ± | 2 PLC | 3 PLC | ANGLE

MATERIAL:

FINISH:

SIGNATURE		DATE
DRN BY	D. Stagle	5/11/76
CHK BY	Smith	11/29/76
DFT APPD		7/28/76
ENGR APPD		7/28/76
AUTH BY		
CODE:	SHEET 1 OF 6	

intel 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE SCHEMATIC - SINGLE BOARD COMPUTER 80/20

SIZE	DEPT	DRAWING NO.	REV
D	MCD	2000819	C

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Figure A-1. iSBC 80/20 Schematic Diagram (Sheet 1 of 6)

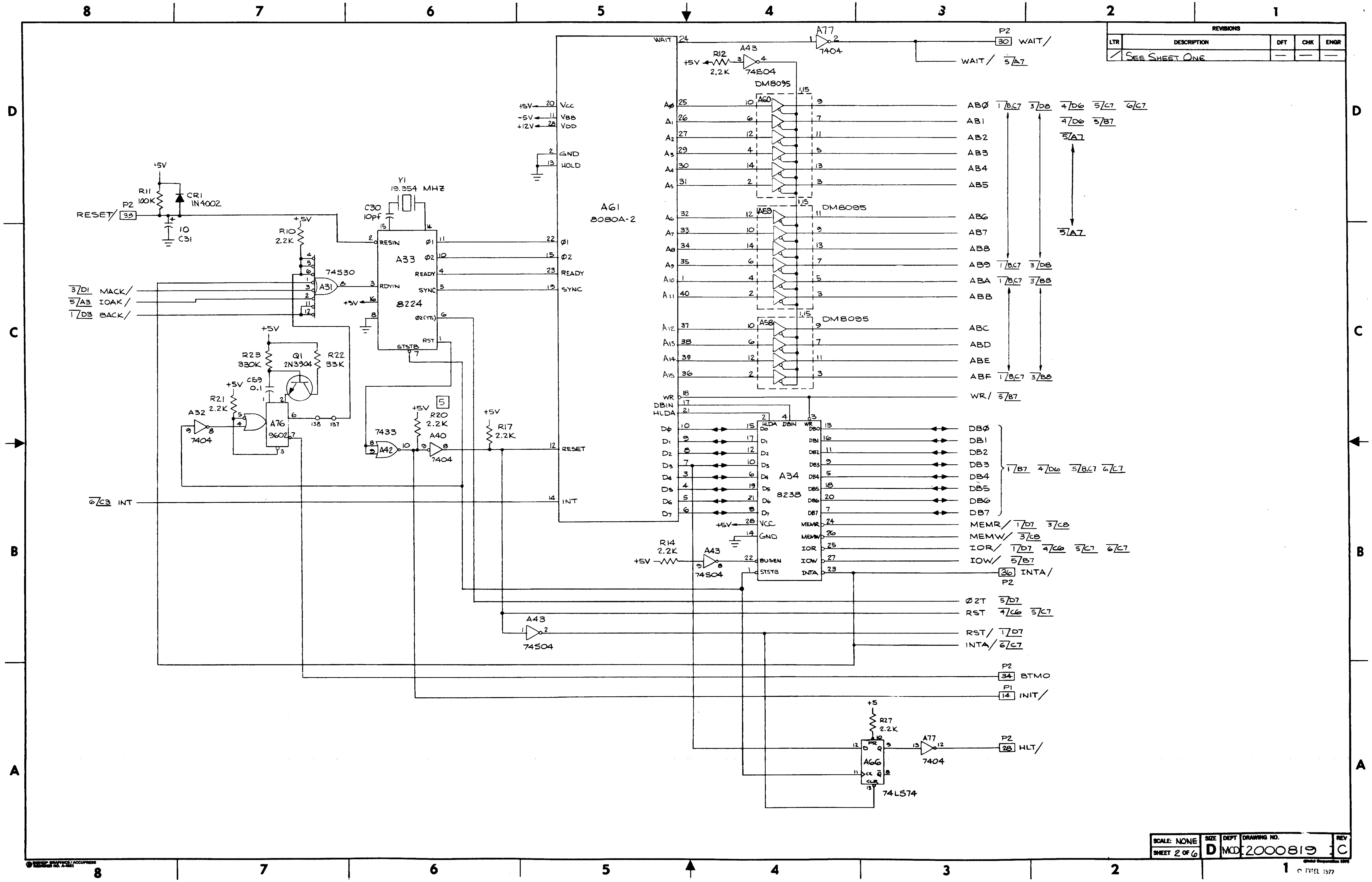


Figure A-1. iSBC 80/20 Schematic Diagram (Sheet 2 of 6)

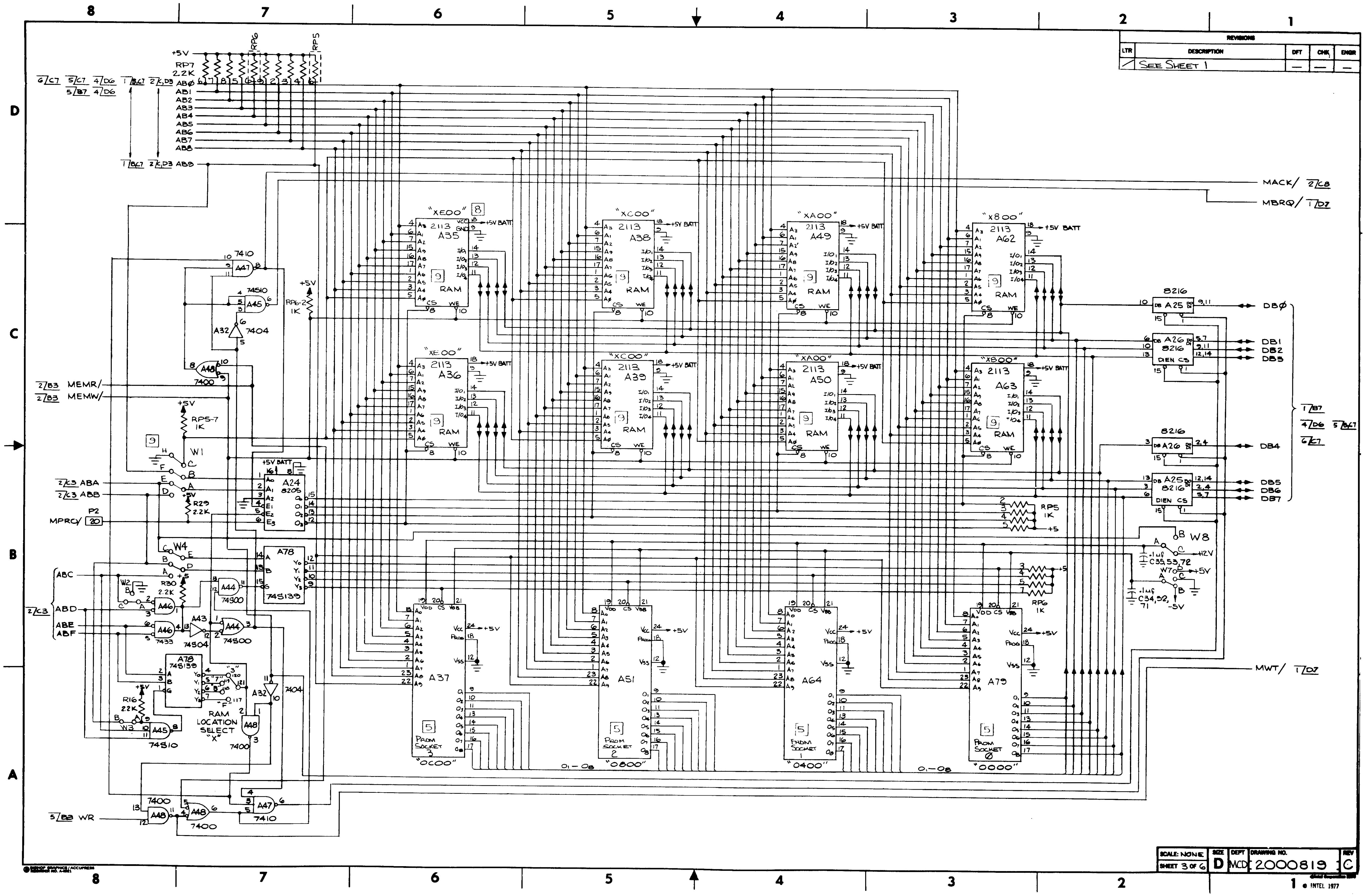


Figure A-1. iSBC 80/20 Schematic Diagram (Sheet 3 of 6)

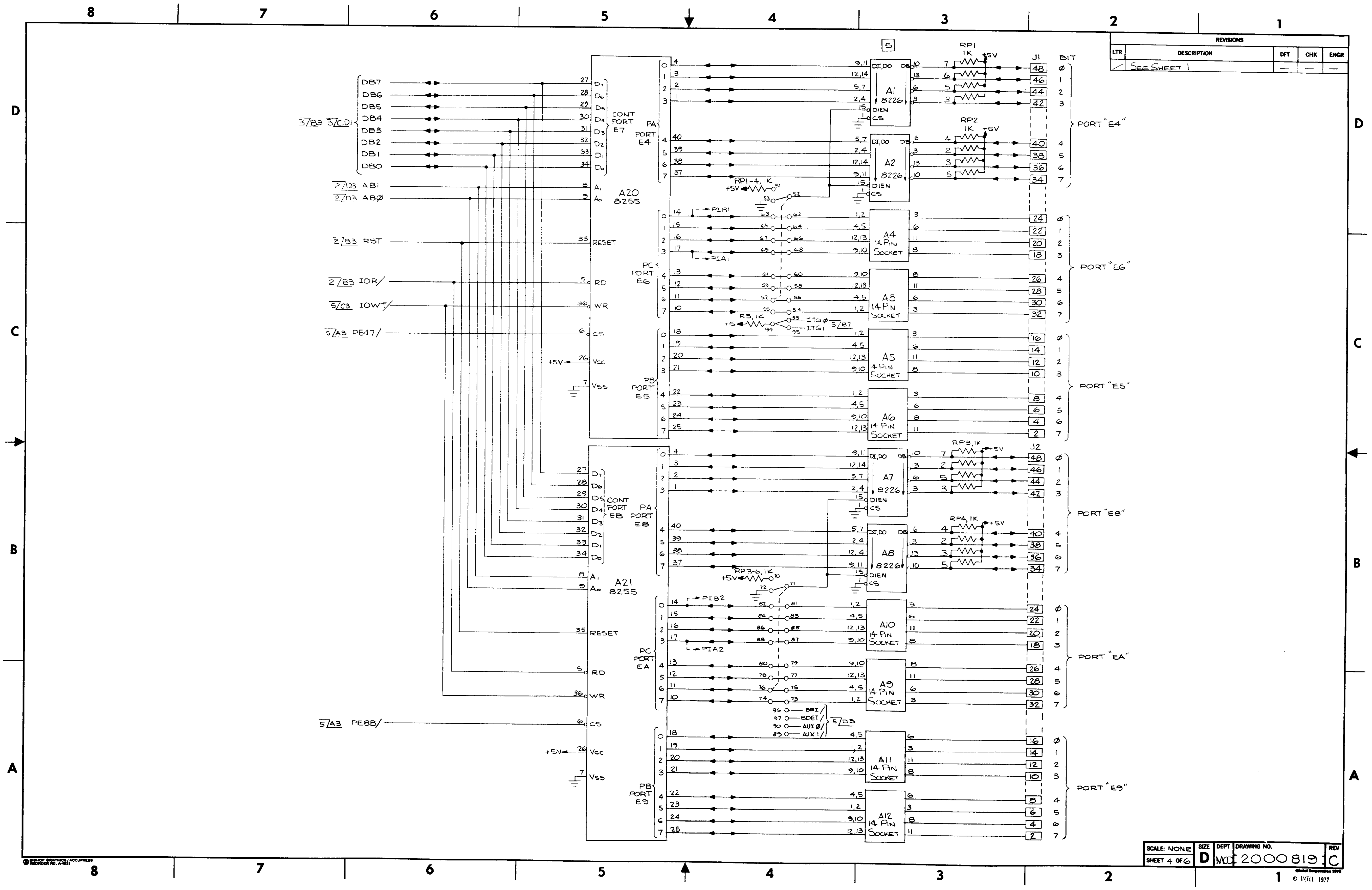


Figure A-1. iSBC 80/20 Schematic Diagram (Sheet 4 of 6)

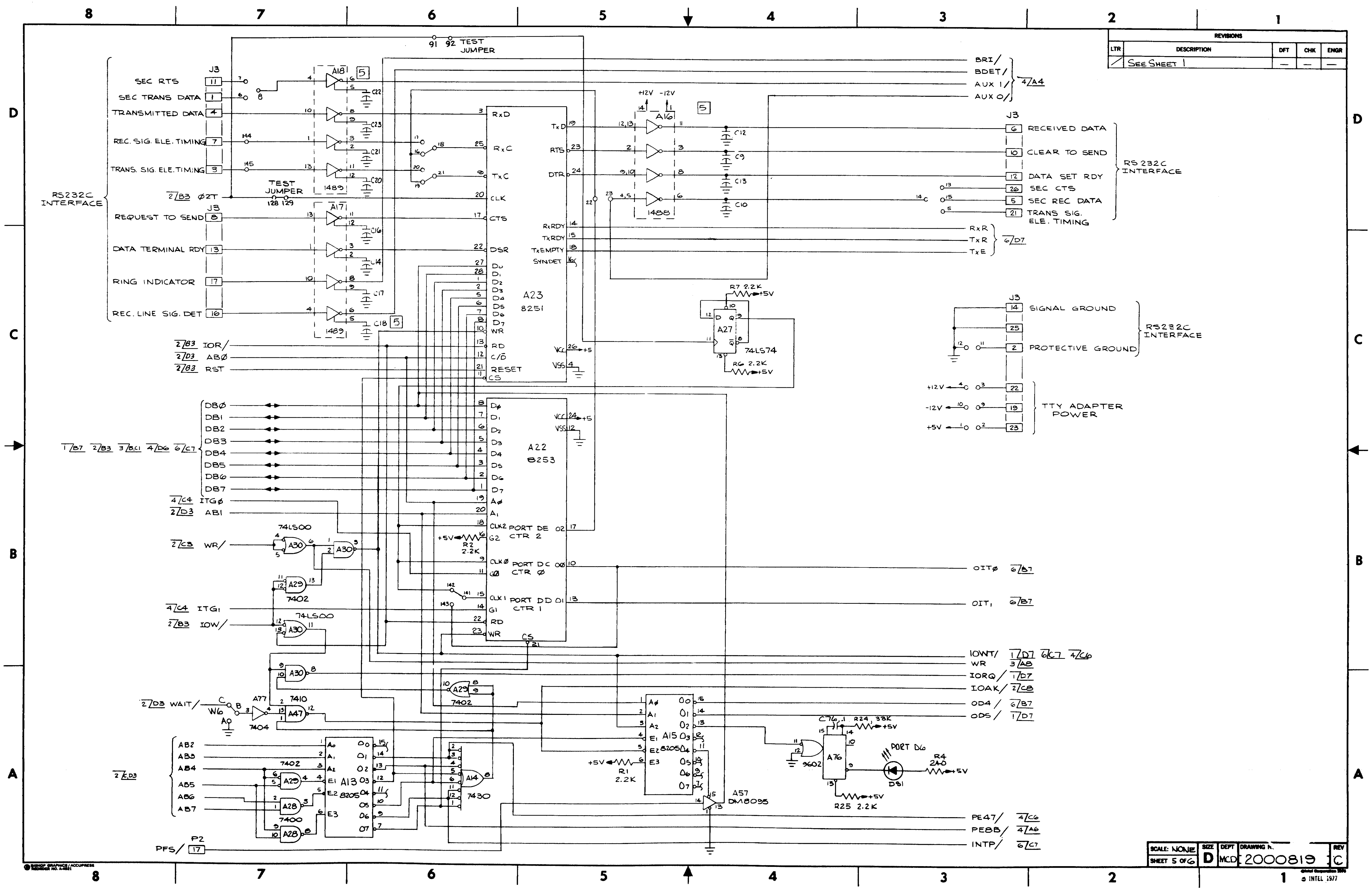


Figure A-1. iSBC 80/20 Schematic Diagram (Sheet 5 of 6)

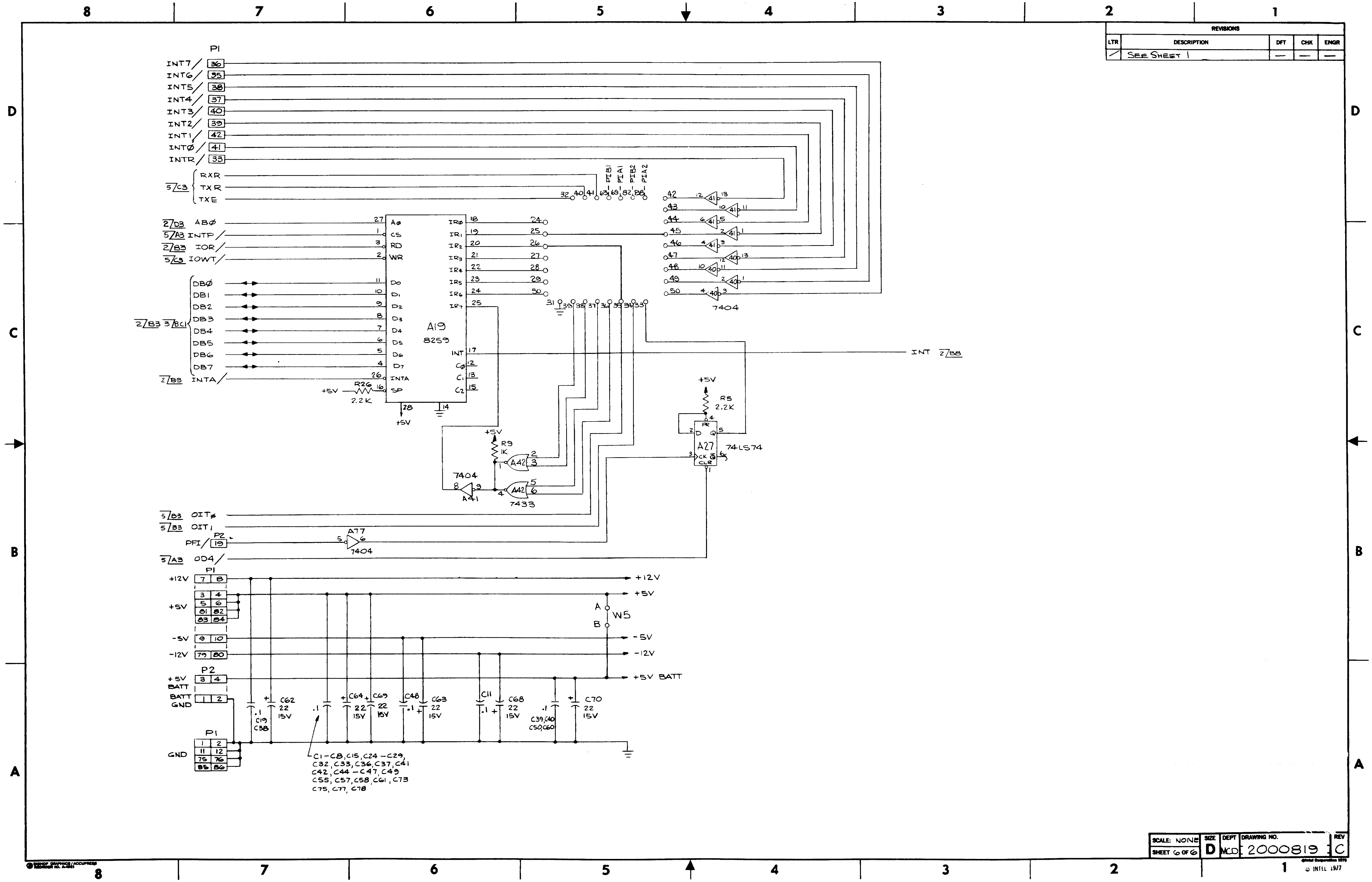
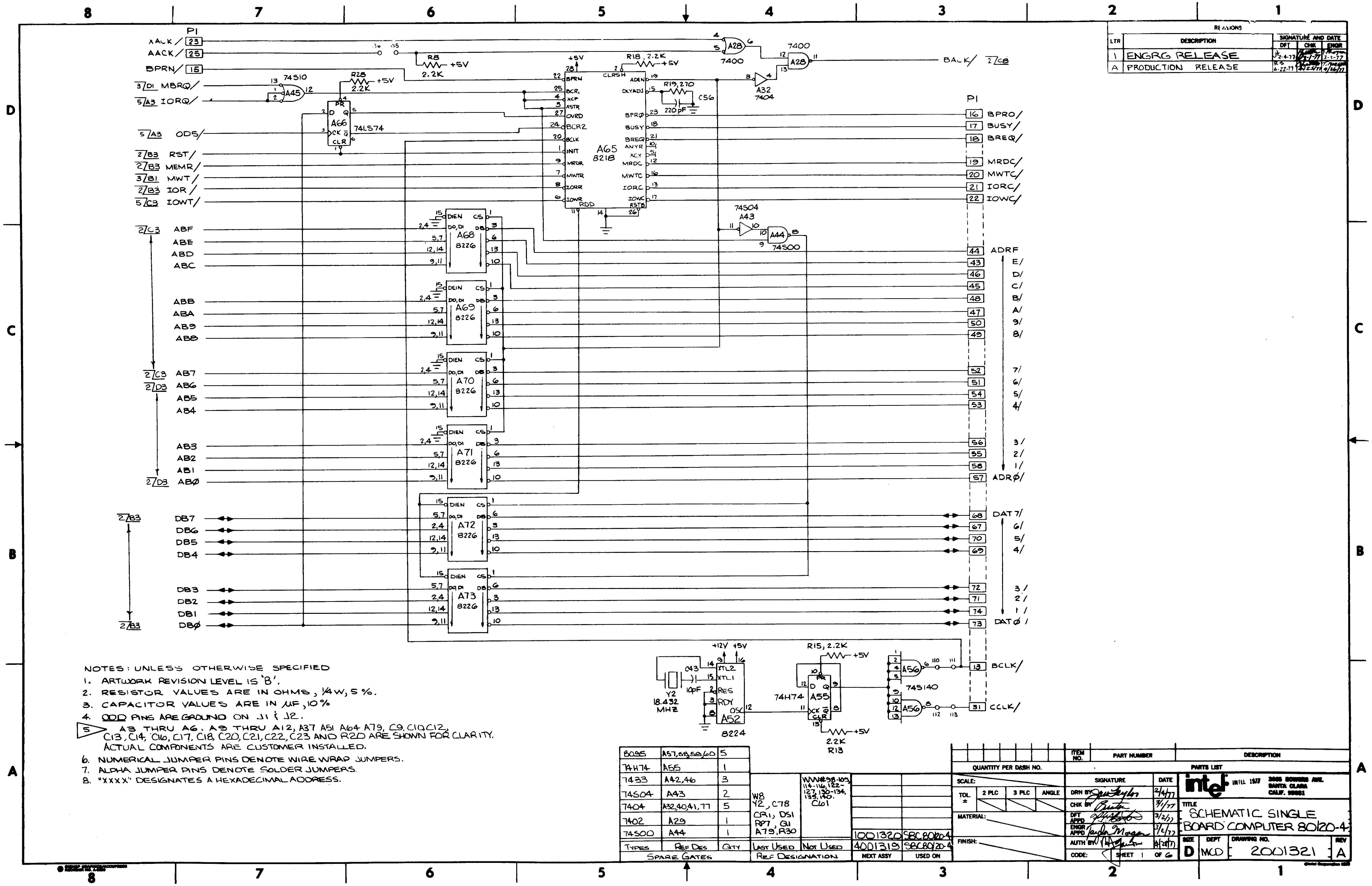


Figure A-1. iSBC 80/20 Schematic Diagram (Sheet 6 of 6)



NOTES: UNLESS OTHERWISE SPECIFIED

1. ARTWORK REVISION LEVEL IS 'B'.
2. RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
3. CAPACITOR VALUES ARE IN µF, 10%
4. ODD PINS ARE GROUND ON J1 & J2.
5. A3 THRU A6. A9 THRU A12, A37 A51 A64 A79, C9, C10,C12, C13, C14, C16, C17, C18, C20, C21, C22, C23 AND R20 ARE SHOWN FOR CLARITY. ACTUAL COMPONENTS ARE CUSTOMER INSTALLED.
6. NUMERICAL JUMPER PINS DENOTE WIRE WRAP JUMPERS.
7. ALPHA JUMPER PINS DENOTE SOLDER JUMPERS.
8. "XXXX" DESIGNATES A HEXADECIMAL ADDRESS.

REVISIONS

LTR	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGR
1	ENGRG RELEASE	JT 2-4-77	3-1-77	T. Morgan 3-2-77
A	PRODUCTION RELEASE	RS 4-22-77	4/25/77	T. Morgan 4/26/77

SPARE GATES

TYPES	REF DES	QTY
8095	A57,58,59,60	5
74H74	A55	1
7433	A42,46	3
74S04	A43	2
7404	A32,40,41,77	5
7402	A29	1
74S00	A44	1

REF DESIGNATION

LAST USED	NOT USED
W8 Y2, C78 CR1, DS1 RP7, Q1 A79, R30	WW#98-105, 114-116, 122-127, 130-134, 135, 140. C61

NEXT ASSY	USED ON
1001320	SBC80/20-4
4001319	SBC80/20-4

QUANTITY PER DASH NO.

ITEM NO.	PART NUMBER	DESCRIPTION

PARTS LIST

SCALE:

TOL. ± 2 PLC 3 PLC ANGLE

MATERIAL:

FINISH:

SIGNATURE	DATE
DRN BY Jan Taylor	2/4/77
CHK BY Burton	3/1/77
DFT APPD	3/2/77
ENGR APPD Taylor Morgan	3/2/77
AUTH BY	4/28/77

CODE: SHEET 1 OF 6

intel INTEL 1977 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE SCHEMATIC SINGLE BOARD COMPUTER 80/20-4

SIZE D DEPT MCD DRAWING NO. 2001321 REV A

Figure A-2. iSBC 80/20-4 Schematic Diagram (Sheet 1 of 6)

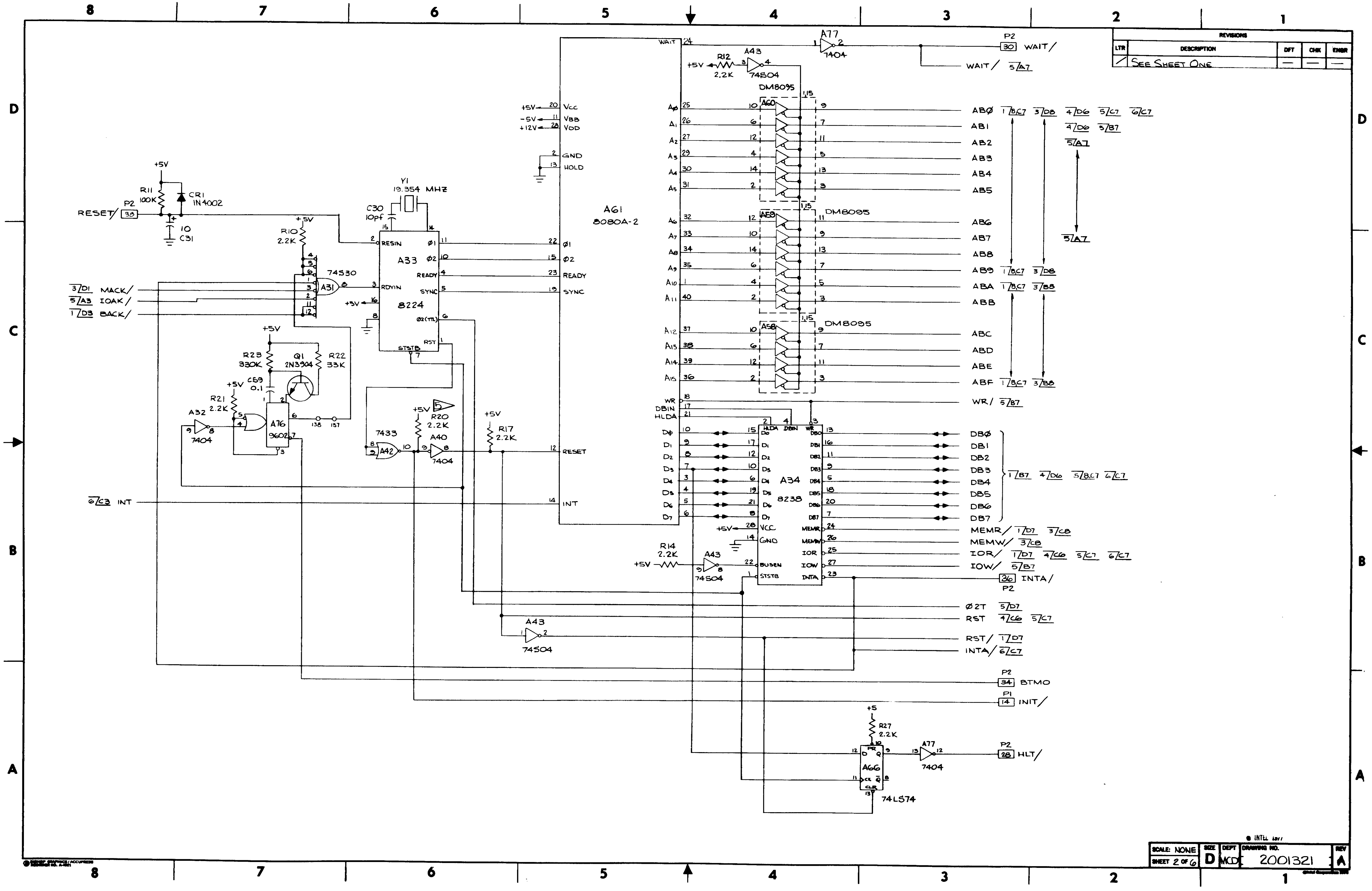


Figure A-2. iSBC 80/20-4 Schematic Diagram (Sheet 2 of 6)

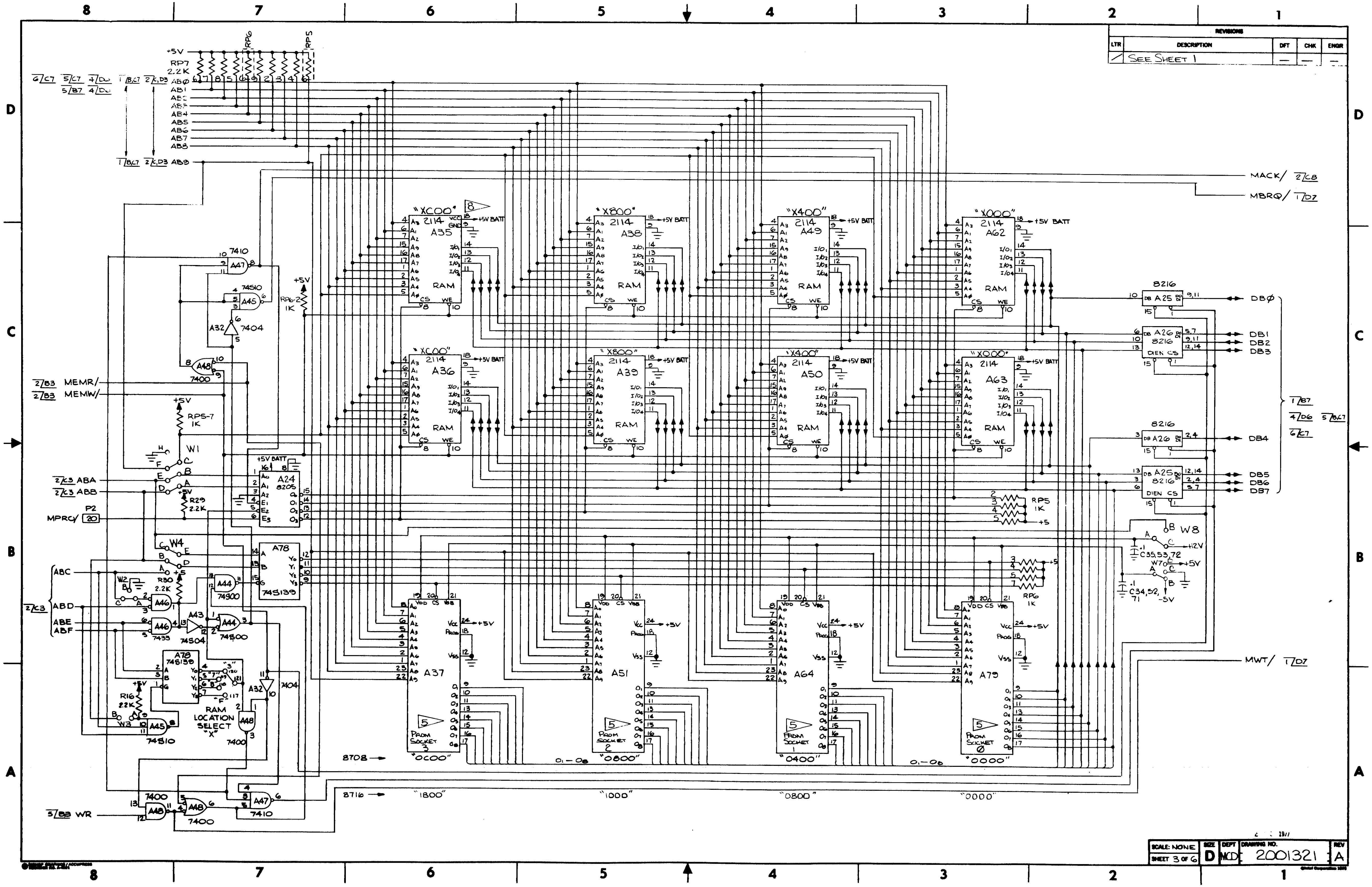


Figure A-2. iSBC 80/20-4 Schematic Diagram (Sheet 3 of 6)

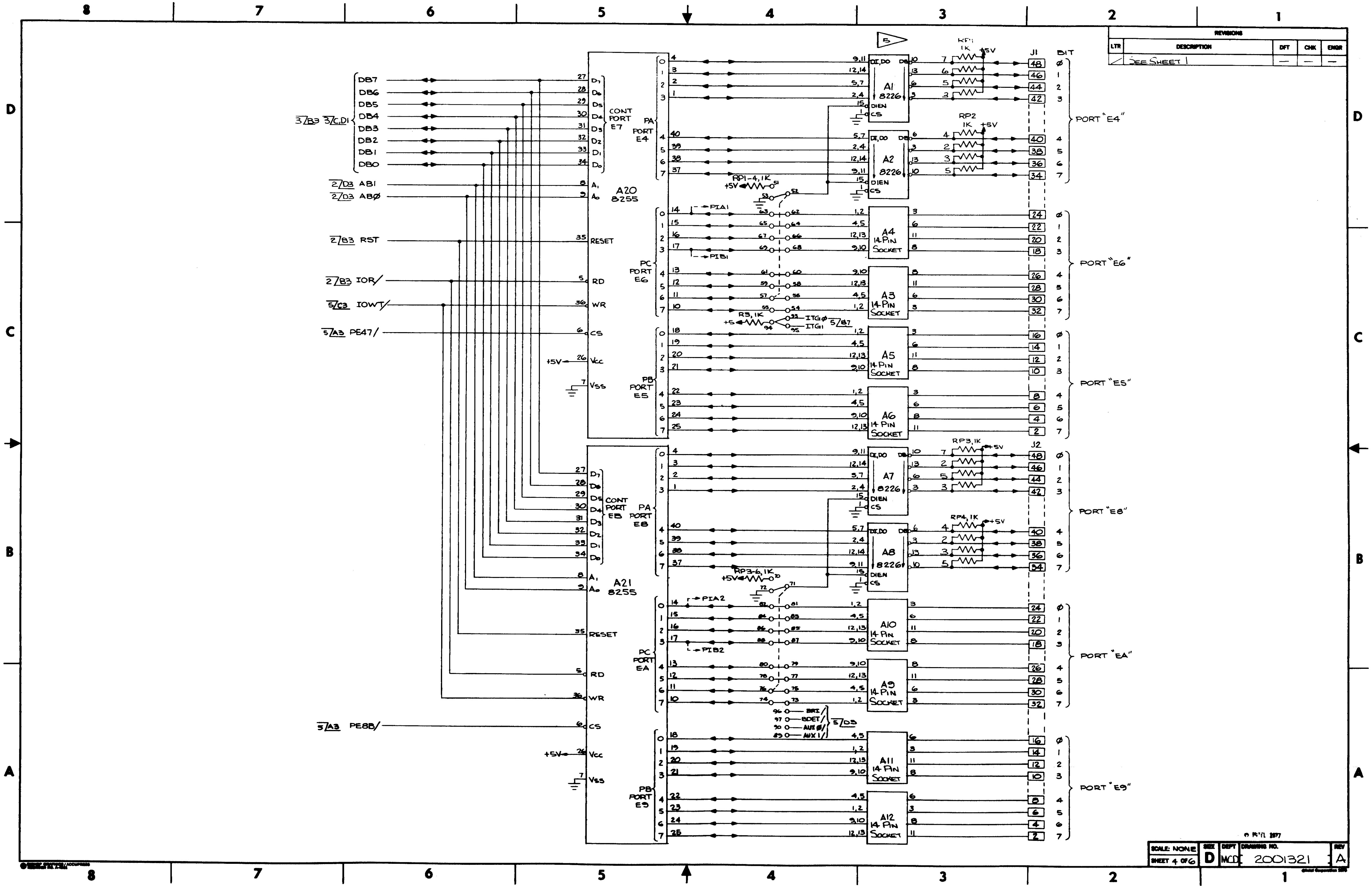


Figure A-2. iSBC 80/20-4 Schematic Diagram (Sheet 4 of 6)

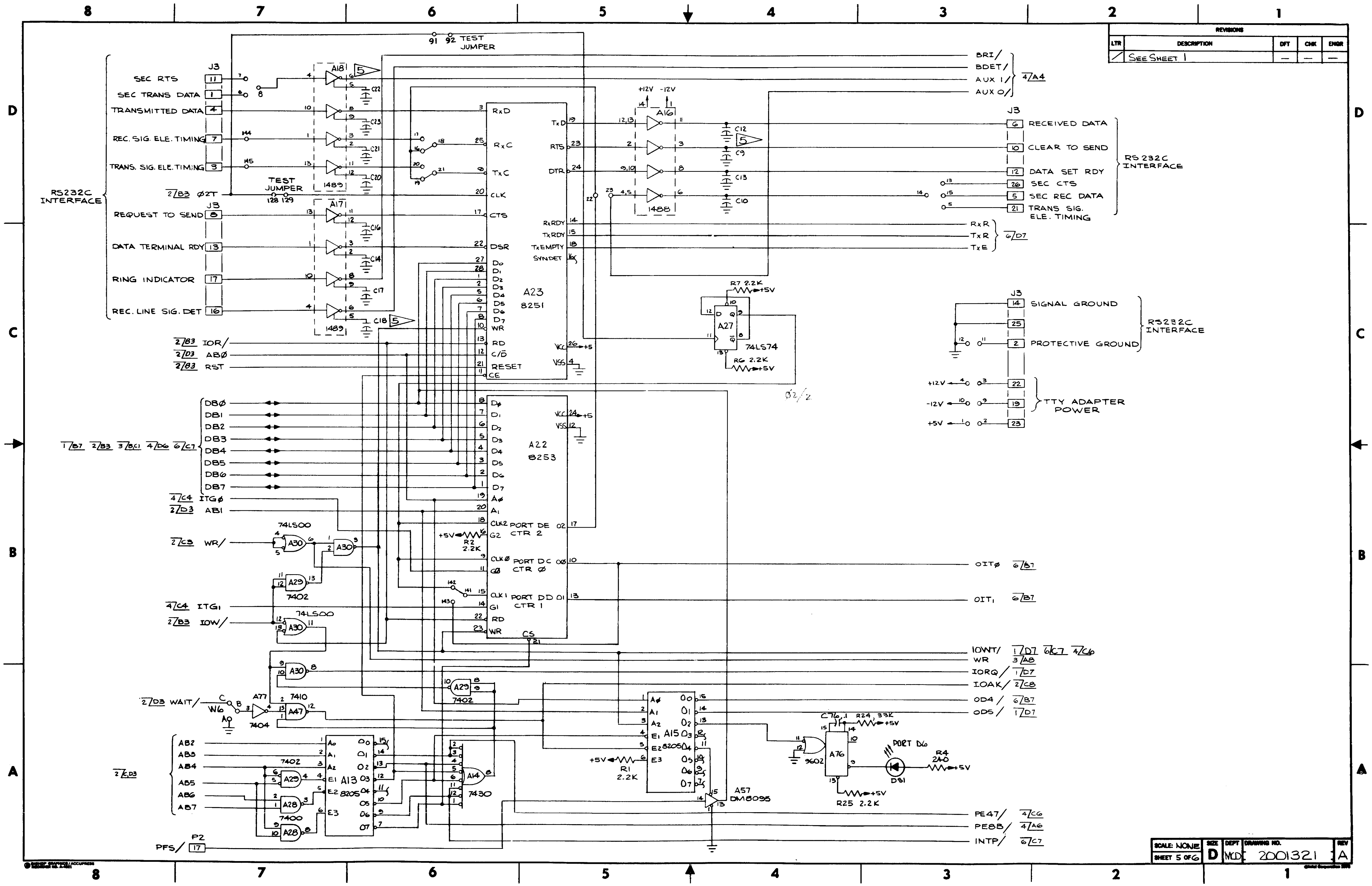


Figure A-2. iSBC 80/20-4 Schematic Diagram (Sheet 5 of 6)

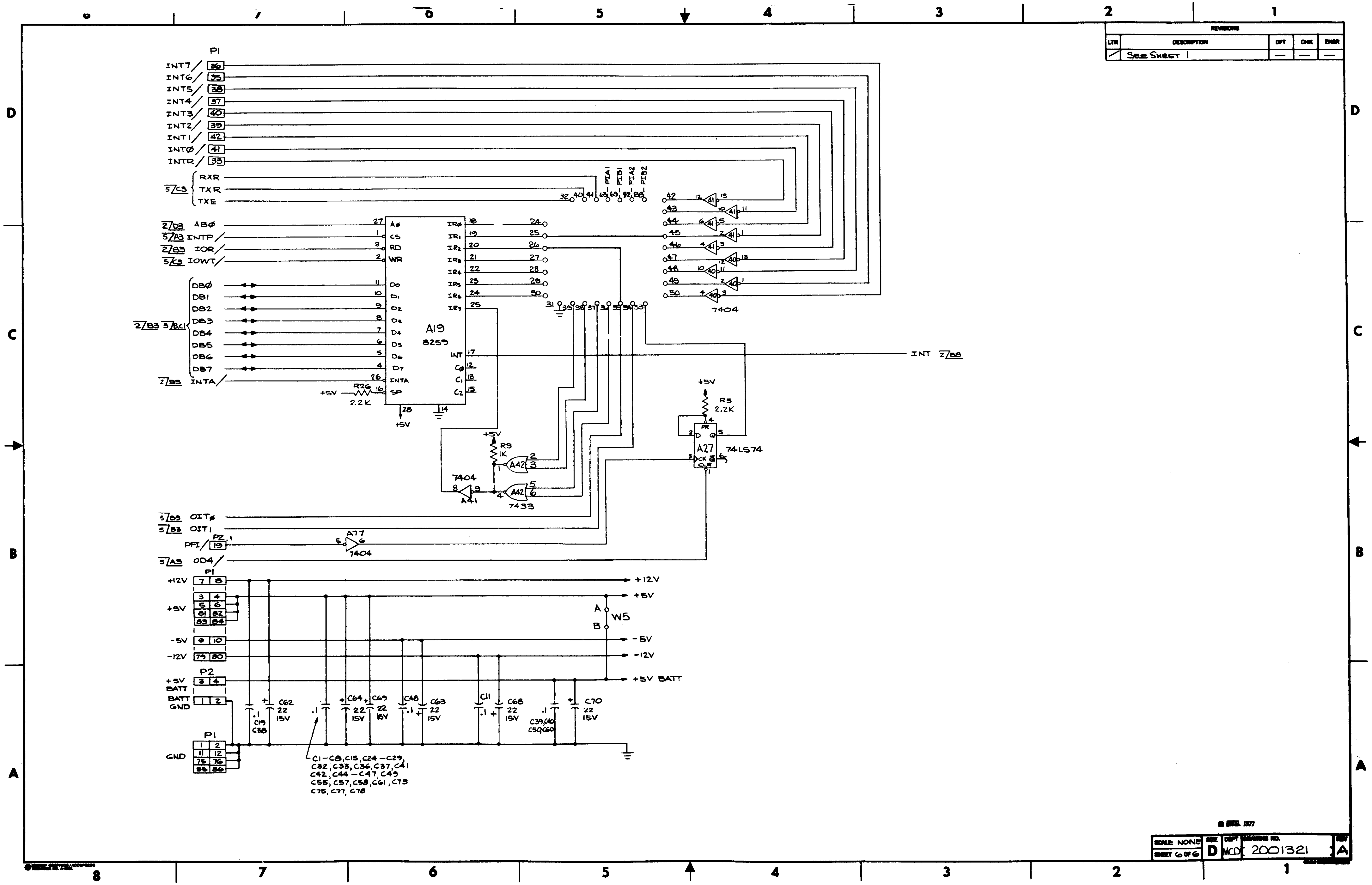


Figure A-2. iSBC 80/20-4 Schematic Diagram (Sheet 6 of 6)

APPENDIX B

SBC-901, SBC-902 SCHEMATICS

Schematic drawings for the SBC-901 and SBC-902 are provided in this appendix. Information and diagrams are subject to change without notice. References should be made to schematics shipped with these products.

RESISTOR NETWORK SPECIFICATIONS:

RESISTANCE VALUES:
±2% (MAX)

OPERATING TEMPERATURE:
0°C TO +70°C

TEMPERATURE COEFFICIENT:
±[illegible] PPM/°C OVER TEMPERATURE
RANGE OF 0°C TO +70°C

OPERATING VOLTAGE:
5.0 V[illegible] (MAX)

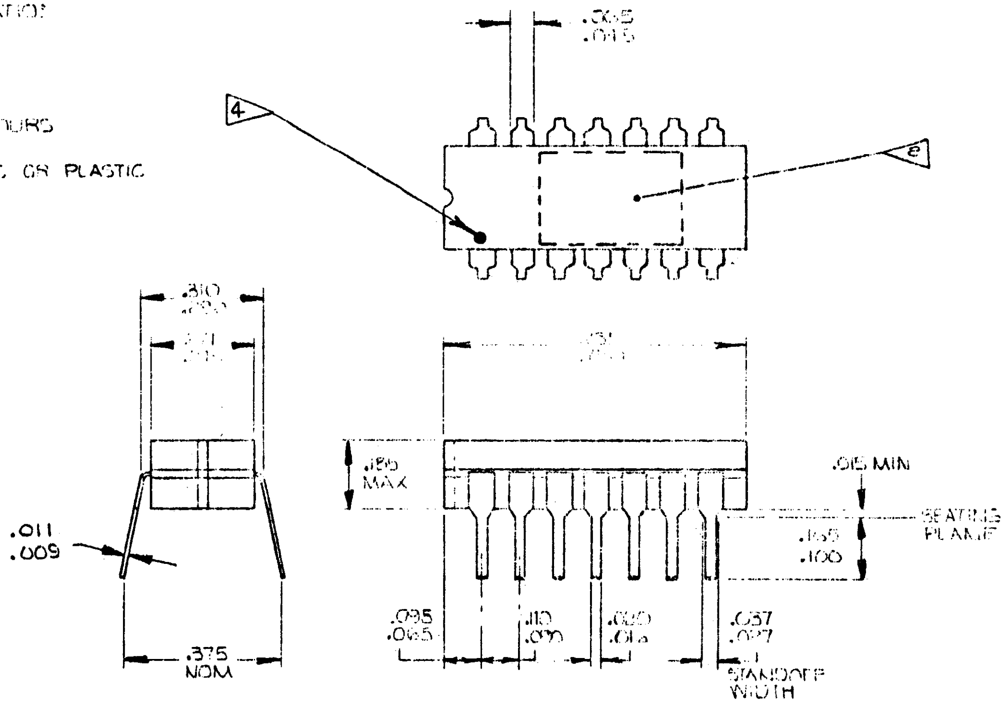
POWER RATING:
AT 70°C, 0.7 WATT PER PACK

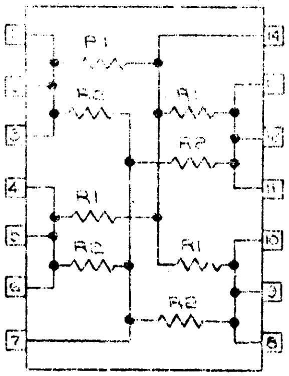
TRACKING RESISTANCE RATIO:
± 1.0% (MAX)

STABILITY:
± 1% YEAR (MAX)

LOAD LIFE:
±1% (ΔR) OVER 1000 HOURS

PACKAGE:
DUAL IN LINE - CERAMIC OR PLASTIC





NOTES:
UNLESS OTHERWISE SPECIFIED,

1. PART NO. IS 4500644-01.

2 INK STAMP PRODUCT CODE, RESISTOR VALUE, PART NO, AND DASH NUMBER WITH CONTRASTING COLOR INK USING MIN .05 HIGH CHARACTERS. NO OTHER MARKINGS PERMITTED EXCEPT MANUF BATCH NO.

E.G.) SBC-901
R220/330
4500644-01

3. FOR PROCUREMENT SEE
LV 4500644-01.

4 IDENTIFY PIN ONE CLEARLY ON TOP OF PACKAGE.

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3065 BOWERS AVE
SANTA CLARA
CALIF

TERMINATING PACK
PULL UP / PULL DOWN

C 4500644 B

RESISTOR NETWORK SPECIFICATIONS:

RESISTANCE VALUES:
±2% (MAX)

OPERATING TEMPERATURE:
0°C TO +70°C

TEMPERATURE COEFFICIENT:
±200 PPM/°C OVER TEMPERATURE
RANGE OF 0°C TO +70°C

OPERATING VOLTAGE:
6.0 VDC (MAX)

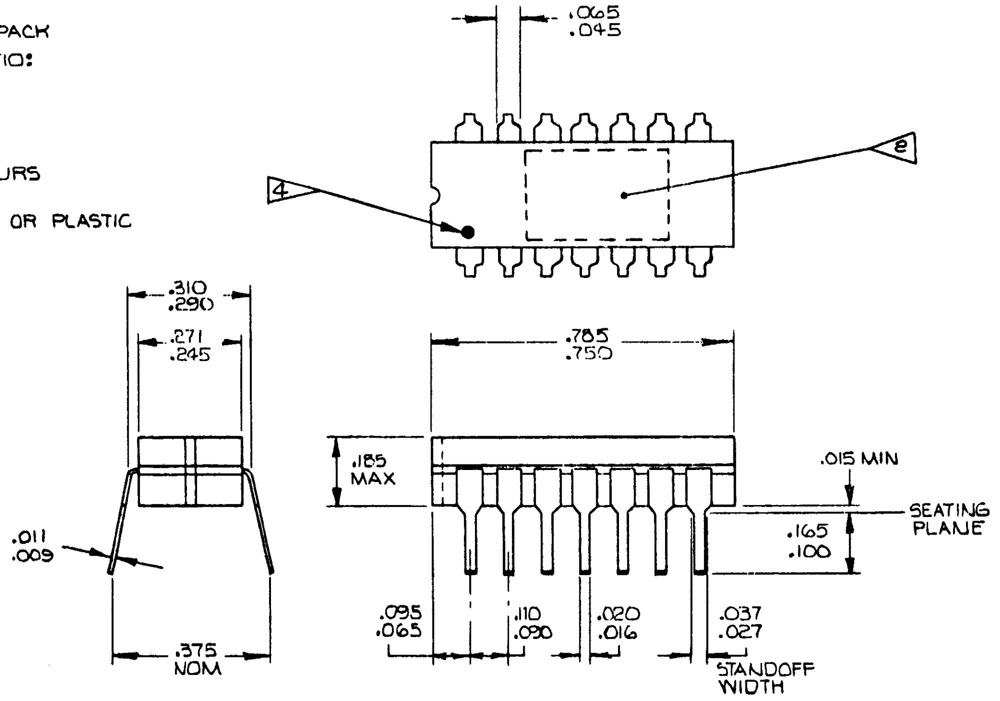
POWER RATING:
AT 70°C, 0.7 WATT PER PACK

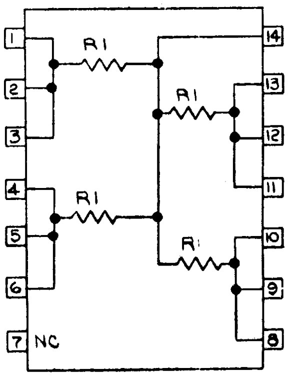
TRACKING RESISTANCE RATIO:
± 1.0% (MAX)

STABILITY:
± 1% YEAR (MAX)

LOAD LIFE:
±1% (ΔR) OVER 1000 HOURS

PACKAGE:
DUAL IN LINE - CERAMIC OR PLASTIC





NOTES:
UNLESS OTHERWISE SPECIFIED,

1. PART NO IS 4500645-01.

2. INK STAMP PRODUCT CODE, RESISTOR VALUE, PART NO AND DASH NUMBER WITH CONTRASTING COLOR AND MIN .12 HIGH CHARACTERS. NO OTHER MARKINGS ARE PERMITTED EXCEPT FOR MANUF BATCH NO.

E.G.) SBC-902
R 1K
4500645-01

3. FOR PROCUREMENT SEE LV4500645

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TITLE TERMINATING PACK
PULL UP

SIZE	DEPT	DRAWING NO.	REV
C	410	4500645	B

APPENDIX C

8080 INSTRUCTION SET SUMMARY

A computer, no matter how sophisticated, can only do what it is "told" to do. One "tells" the computer what to do via a series of coded instructions referred to as a Program. The realm of the programmer is referred to as Software, in contrast to the Hardware that comprises the actual computer equipment. A computer's software refers to all of the programs that have been written for that computer.

When a computer is designed, the engineers provide the Central Processing Unit (CPU) with the ability to perform a particular set of operations. The CPU is designed such that a specific operation is performed when the CPU control logic decodes a particular instruction. Consequently, the operations that can be performed by a CPU define the computer's Instruction Set.

Each computer instruction allows the programmer to initiate the performance of a specific operation. All computers implement certain arithmetic operations in their instruction set, such as an instruction to add the contents of two registers. Often logical operations (e.g., OR the contents of two registers) and register operate instructions (e.g., increment a register) are included in the instruction set. A computer's instruction set will also have instructions that move data between registers, between a register and memory, and between register and an I/O device. Most instruction sets also provide Conditional Instructions. A conditional instruction specifies an operation to be performed only if certain conditions have been met; for example, jump to a particular instruction if the result of the last operation was zero. Conditional instructions provide a program with a decision-making capability.

By logically organizing a sequence of instructions into a coherent program, the programmer can "tell" the computer to perform a very specific and useful function.

The computer, however, can only execute programs whose instructions are in a binary coded form (i.e., a series of 1's and 0's), that is called Machine Code. Because it would be extremely cumbersome to program in machine code, programming languages have been developed. There are programs available which convert the programming language instructions into machine code that can be interpreted by the processor.

One type of programming language is Assembly Language. A unique assembly language mnemonic is assigned to each of the computer's instructions. The programmer can write a program (called the Source Program) using these mnemonics and certain operands; the source program is then converted into machine instructions (called the Object Code). Each assembly language instructions is converted into one machine code instruction (1 or more bytes) by an Assembler program. Assembly languages are usually machine dependent (i.e., they are usually able to run on only one type of computer).

THE 8080 INSTRUCTION SET

The 8080 instruction set includes five different types of instructions:

- *Data Transfer Group* – move data between registers or between memory and registers.
- *Arithmetic Group* – add, subtract, increment or decrement data in registers or in memory.
- *Logical Group* – AND, OR, EXCLUSIVE-OR, compare, rotate or complement data in registers or in memory.
- *Branch Group* – conditional and unconditional jump instructions, subroutine call instructions and return instructions.
- *Stack, I/O and Machine Control Group* – includes I/O instructions, as well as instructions for maintaining the stack and internal control flags.

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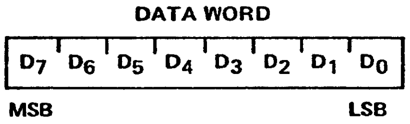
Instruction and Data Formats

Memory for the 8080 is organized into 8-bit quantities, called Bytes. Each byte has a unique 16-bit binary address corresponding to its sequential position in memory.

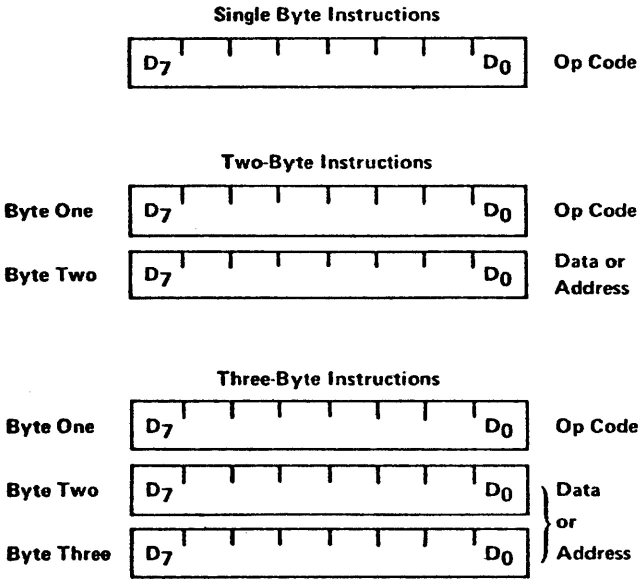
The 8080 can directly address up to 65,536 bytes of memory, which may consist of both read-only memory (ROM) elements and random-access memory (RAM) elements (read/write memory).

Data in the 8080 is stored in the form of 8-bit binary integers:



When a register or data word contains a binary number, it is necessary to establish the order in which the bits of the number are written. In the Intel 8080, BIT 0 is referred to as the Least Significant Bit (LSB), and BIT 7 (of an 8-bit number) is referred to as the Most Significant Bit (MSB).

The 8080 program instructions may be one, two or three bytes in length. Multiple byte instructions must be stored in successive memory locations; the address of the first byte is always used as the address of the instructions. The exact instruction format will depend on the particular operation to be executed.



Addressing Modes

Often the data that is to be operated on is stored in memory. When multi-byte numeric data is used, the data, like instructions, is stored in successive memory locations, with the least significant byte first, followed by increasingly significant bytes. The 8080 has four different modes for addressing data stored in memory or in registers:

- *Direct* – Bytes 2 and 3 of the instruction contain the exact memory address of the data item (the low-order bits of the address are in byte 2, the high-order bits in byte 3).

- *Register* – The instruction specifies the register-pair in which the data is located.

- *Register Indirect* – The instruction specifies a register-pair which contains the memory address where the data is located (the high-order bits of the address are in the first register of the pair, the low-order bits in the second).

- *Immediate* – The instruction contains the data itself. This is either an 8-bit quantity or a 16-bit quantity (least significant byte first, most significant byte second).

Unless directed by an interrupt or branch instruction, the execution of instructions proceeds through consecutively increasing memory locations. A branch instruction can specify the address of the next instruction to be executed in one of two ways:

- *Direct* – The branch instruction contains the address of the next instruction to be executed. (Except for the 'RST' instruction, byte 2 contains the low-order address and byte 3 the high-order address.)

- *Register Indirect* – The branch instruction indicates a register-pair which contains the address of the next instruction to be executed. (The high-order bits of the address are in the first register of the pair, the low-order bits in the second.)

The RST instruction is a special one-byte call instruction (usually used during interrupt sequences).

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RST includes a three-bit field; program control is transferred to the instruction whose address is eight times the contents of this three-bit field.

Condition Flags

There are five condition flags associated with the execution of instructions on the 8080. They are Zero, Sign, Parity, Carry, and Auxiliary Carry, and are each represented by a 1-bit register in the CPU. A flag is "set" by forcing the bit to 1; "reset" by forcing the bit to 0.

Unless indicated otherwise, when an instruction affects a flag, it affects it in the following manner:

Zero: If the result of an instruction has the value 0, this flag is set; otherwise it is reset.

Sign: If the most significant bit of the result of the operation has the value 1, this flag is set; otherwise it is reset.

Parity: If the modulo 2 sum of the bits of the result of the operation is 0 (i.e., if the result has even parity), this flag is set; otherwise it is reset (i.e., if the result has odd parity).

Carry: If the instruction resulted in a carry (from addition), or a borrow (from subtraction of a comparison) out of the high-order bit, this flag is set; otherwise it is reset.

Auxiliary Carry: If the instruction caused a carry out of bit 3 and into bit 4 of the resulting value, the auxiliary carry is set; otherwise it is reset. This flag is affected by single precision additions, subtractions, increments, decrements, comparisons, and logical operations, but is principally used with additions and increments preceding a DAA (Decimal Adjust Accumulator) instruction.

Symbols and Abbreviations

The following symbols and abbreviations are used in the subsequent description of the 8080 instructions:

SYMBOLS	MEANING
accumulator	Register A
addr	16-bit address quantity
data	8-bit data quantity
data 16	16-bit data quantity
byte 2	The second byte of the instruction
byte 3	The third byte of the instruction
port	8-bit address of an I/O device
r,r,1,r2	One of the registers A,B,C,D,E,H,L
DDD,SSS	The bit pattern designating one of the registers A,B,C,D,E,H,L. (DD= destination, SSS=source):

DDD or SSS	REGISTER NAME
111	A
000	B
001	C
010	D
011	E
100	H
101	L

rp	One of the register pairs:
	B represents the B,C pair with B as the high-order register and C as the low-order register;
	D represents the D,E pair with D as the high-order register and E as the low-order register;
	H represents the H,L pair with H as the high-order register and L as the low-order register;
	SP represents the 16-bit stack pointer register.

RP	The bit pattern designating one of the register pairs B,D,H,SP:

RP	REGISTER PAIR
00	B-C
01	D-E
10	H-L
11	SP

rh	The first (high-order) register of a designated pair.
rl	The second (low-order) register of a designated register pair.

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PC — 16-bit program counter register (PCH and PCL are used to refer to the high-order and low-order 8 bits, respectively).

SP — 16-bit stack pointer register (SPH and SPL are used to refer to the high-order and low-order 8 bits, respectively).

r_m — Bit m of the register r (bits are number 7 through 0 from left to right).

Z,S,P,CY,AC — The condition flags:

Zero,
Sign,
Parity,
Carry, and
Auxiliary Carry, respectively.

( ) — The contents of the memory location or registers enclosed in the parentheses.

← — "Is transferred to"A

∧ — Logical AND

⊻ — Exclusive OR

∨ — Inclusive OR

+ — Addition

– — Two's complement subtraction

* — Multiplication

↔ — "Is exchanged with"

—— — The one's complement (e.g., $(\overline{A})$)

n — The restart number 0 through 7

NNN — The binary representation 000 through 111 for restart number 0 through 7, respectively.

Description Format

The following pages provide a detailed description of the instruction set of the 8080. Each instruction is described in the following manner:

1. The MAC 80 assembler format, consisting of the instruction mnemonic and operand fields, is printed in BOLDFACE on the left side of the first line.

2. The name of the instruction is enclosed in parenthesis on the right side of the first line.

3. The next line(s) contain a symbolic description of the operation of the instruction.

4. This is followed by a narative description of the operand of the instruction.

5. The following line(s) contain the binary fields and patterns that comprise the machine instruction.

6. The last four lines contain incidental information about the execution of the instruction. The number of machine cycles and states required to execute the instruction are listed first. If the instruction has two possible execution times, as in a Conditional Jump, both times will be listed, separated by a slash. Next, any significant data addressing modes (see Page A-2) are listed. The last line lists any of the five Flags that are affected by the execution of the instruction.

Data Transfer Group

This group of instructions transfer data to and from registers and memory. Condition flags are not affected by any instruction in this group.

MOV r1, r2 (Move Register)

(r1) ← (r2)

The content of register r2 is moved to register r1.

0	1	D	D	D	S	S	S

Cycles:	1
States:	5
Addressing:	register
Flags:	none

MOV r,M (Move from memory)

(r) ← ((H) (L))

The content of the memory location, whose address is in registers H and L, is moved to register r.

0	1	D	D	D	1	1	0

Cycles:	2
States:	7
Addressing:	reg. indirect
Flags:	none

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MOV M, r (Move to memory)
((H)(L)) ← (r)
The content of register r is moved to the memory location whose address is in registers H and L.

0	1	1	1	0	S	S	S

Cycles:	2
States:	7
Addressing:	reg. indirect
Flags:	none

MVI r, data (Move Immediate)
(r) ← (byte 2)
The content of byte 2 of the instruction is moved to register r.

0	0	D	D	D	1	1	0
data							

Cycles:	2
States:	7
Addressing:	immediate
Flags:	none

MVI M, data (Move to memory immediate)
((H)(L)) ← (byte 2)
The content of byte 2 of the instruction is moved to the memory location whose address is in registers H and L.

0	0	1	1	0	1	1	0
data							

Cycles:	3
States:	10
Addressing:	immed./reg. indirect
Flags:	none

LXI rp, data 16 (Load register pair immediate)
(rh) ← (byte 3),
(rl) ← (byte 2)
Byte 3 of the instruction is moved into the high-order register (rh) of the register pair rp. Byte 2 of the instruction is moved into the low-order register (rl) of the register pair rp.

0	0	R	P	0	0	0	1
low-order data							
high-order data							

Cycles:	3
States:	10
Addressing:	immediate
Flags:	none

LDA addr (Load Accumulator direct)
(A) ← ((byte 3)(byte 2))
The content of the memory location, whose address is specified in byte 2 and byte 3 of the instruction, is moved to register A.

0	0	1	1	1	0	1	0
low-order addr							
high-order addr							

Cycles:	4
States:	13
Addressing:	direct
Flags:	none

STA addr (Store Accumulator direct)
((byte 3)(byte 2)) ← (A)
The content of the accumulator is moved to the memory location whose address is specified in byte 2 and byte 3 of the instruction.

0	0	1	1	0	0	1	0
low-order addr							
high-order addr							

Cycles:	4
States:	13
Addressing:	direct
Flags:	none

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LHLD addr (Load H and L direct)

(L) ← ((byte 3)(byte 2))

(H) ← ((byte 3)(byte 2) + 1)

The content of the memory location, whose address is specified in byte 2 and byte 3 of the instruction, is moved to register L. The content of the memory location at the succeeding address is moved to register H.

0	0	1	0	1	0	1	0
low-order addr							
high-order addr							

Cycles:	5
States:	16
Addressing:	direct
Flags:	none

SHLD addr (Store H and L direct)

((byte 3)(byte 2)) ← (L)

((byte 3)(byte 2) + 1) ← (H)

The content of register L is moved to the memory location whose address is specified in byte 2 and byte 3. The content of register H is moved to the succeeding memory location.

0	0	1	0	0	0	1	0
low-order addr							
high-order addr							

Cycles:	5
States:	16
Addressing:	direct
Flags:	none

LDAX rp (Load accumulator indirect)

(A) ← ((rp))

The content of the memory location, whose address is in the register pair rp, is moved to register A. Note: Only register pairs rp=B (registers B and C) or rp=D (registers D and E) may be specified.

0	0	R	P	1	0	1	0

Cycles:	2
States:	7
Addressing:	reg. indirect
Flags:	none

STAX rp (Store accumulator indirect)

((rp)) ← (A)

The content of register A is moved to the memory location whose address is in the register pair rp. Note: Only register pairs rp=B (registers B and C) or rp=D (registers D and E) may be specified.

0	0	R	P	0	0	1	1

Cycles:	2
States:	7
Addressing:	reg. indirect
Flags:	none

XCHG (Exchange H and L with D and E)

(H) ↔ (D)

(L) ↔ (E)

The contents of registers H and L are exchanged with the contents of registers D and E.

1	1	1	0	1	0	1	1

Cycles:	1
States:	4
Addressing:	register
Flags:	none

DCR M (Decrement memory)

((H)(L)) ← ((H)(L)) – 1

The content of the memory location whose address is contained in the H and L registers is decremented by one. Note: All condition flags except CY are affected.

0	0	1	1	0	1	0	1

Cycles:	3
States:	10
Addressing:	reg. indirect
Flags:	Z,S,P,AC

INX rp (Increment register pair)

(rh)(rl) ← (rh)(rl) + 1

The content of the register pair rp is incremented by one. Note: No condition flags are affected.

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0	0	R	P	0	0	1	1

Cycles:	1
States:	5
Addressing:	register
Flags:	none

Arithmetic Group

This group of instructions performs arithmetic operations on data in registers and memory.

Unless otherwise indicated, all instructions in this group affect the Zero, Sign, Parity, Carry, and Auxiliary Carry flags according to the standard rules.

All subtraction operations are performed via two's complement arithmetic, and set the carry flag to one to indicate a borrow and clear it to indicate no borrow.

ADD r (Add Register)

(A) ← (A) + (r)

The content of register r is added to the content of the accumulator. The result is placed in the accumulator.

1	0	0	0	0	S	S	S

Cycles:	1
States:	4
Addressing:	register
Flags:	Z,S,P,CY,AC

ADD M (Add Memory)

(A) ← (A) + ((H)(L))

The content of the memory location whose address is contained in the H and L register is added to the content of the accumulator. The result is placed in the accumulator.

1	0	0	0	0	1	1	0

Cycles:	2
States:	7
Addressing:	reg. indirect
Flags:	Z,S,P,CY,AC

ADI data (Add Immediate)

(A) ← (A) + (byte 2)

The content of the second byte of the instruction is added to the constant of the accumulator. The result is placed in the accumulator.

1	1	0	0	0	1	1	0
data							

Cycles:	2
States:	7
Addressing:	immediate
Flags:	Z,S,P,CY,AC

ADC r (Add Register with Carry)

(A) ← (A) + (r) + (CY)

The content of register r and the content of the carry bit are added to the content of the accumulator. The result is placed in the accumulator.

1	0	0	0	1	S	S	S

Cycles:	1
States:	4
Addressing:	register
Flags:	Z,S,P,CY,AC

ADC M (Add Memory with Carry)

(A) ← (A) + ((H)(L)) + (CY)

The content of the memory location whose address is contained in the H and L registers and the content of the CY flag are added to the accumulator. The result is placed in the accumulator.

1	0	0	0	1	1	1	0

Cycles:	2
States:	7
Addressing:	reg. indirect
Flags:	Z,S,P,CY,AC

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ACI data (Add Immediate with Carry)

(A) ← (A) + (byte 2) + (CY)

The content of the second byte of the instruction and the content of the CY flag are added to the contents of the accumulator. The result is placed in the accumulator.

1	1	0	0	1	1	1	0
data							

Cycles:	2
States:	7
Addressing:	immediate
Flags:	Z,S,P,CY,AC

SUB r (Subtract Register)

(A) ← (A) – (r)

The content of register r is subtracted from the content of the accumulator. The result is placed in the accumulator.

1	0	0	1	0	S	S	S

Cycles:	1
States:	4
Addressing:	register
Flags:	Z,S,P,CY,AC

SUB M (Subtract Memory)

(A) ← (A) – ((H)(L))

The content of the memory location whose address is contained in the H and L registers is subtracted from the content of the accumulator. The result is placed in the accumulator.

1	0	0	1	0	1	1	0

Cycles:	2
States:	7
Addressing:	reg. indirect
Flags:	Z,S,P,CY,AC

SUI data (Subtract Immediate)

(A) ← (A) – (byte 2)

The content of the second byte of the instruction is subtracted from the content of the accumulator. The result is placed in the accumulator.

1	1	0	1	0	1	1	0
data							

Cycles:	2
States:	7
Addressing:	immediate
Flags:	Z,S,P,CY,AC

SBB r (Subtract Register with Borrow)

(A) ← (A) – (r) – (CY)

The content of register r and the content of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

1	0	0	1	1	S	S	S

Cycles:	1
States:	4
Addressing:	register
Flags:	Z,S,P,CY,AC

SBB M (Subtract Memory with Borrow)

(A) ← (A) – ((H)(L)) – (CY)

The content of the memory location whose address is contained in the H and L registers and the content of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

1	0	0	1	1	1	1	0

Cycles:	2
States:	7
Addressing:	reg. indirect
Flags:	Z,S,P,CY,AC

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SBI data (Subtract Immediate with Borrow)

(A) ← (A) – (byte 2) – (CY)

The contents of the second byte of the instruction and the contents of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

1	1	0	1	1	1	1	0
data							

Cycles:	2
States:	7
Addressing:	immediate
Flags:	Z,S,P,CY,AC

INR r (Increment Register)

(r) ← (r) + 1

The content of register r is incremented by one. Note: All condition flags except CY are affected.

0	0	D	D	D	1	0	0

Cycles:	1
States:	5
Addressing:	register
Flags:	Z,S,P,AC

INR M (Increment Memory)

((H)(L)) ← ((H)(L)) + 1

The content of the memory location whose address is contained in the H and L registers is incremented by one. Note: All condition flags except CY are affected.

0	0	1	1	0	1	0	0

Cycles:	3
States:	10
Addressing:	reg. indirect
Flags:	Z,S,P,AC

DCR r (Decrement Register)

(r) ← (r) – 1

The content of register r is decremented by one. Note: All condition flags except CY are affected.

0	0	D	D	D	1	0	1

Cycles:	1
States:	5
Addressing:	register
Flags:	Z,S,P,AC

DCX rp (Decrement register pair)

(rh)(rl) ← (rh)(rl) – 1

The content of the register pair rp is decremented by one. Note: No condition flags are affected.

0	0	R	P	1	0	1	1

Cycles:	1
States:	5
Addressing:	register
Flags:	none

DAD rp (Add register pair to H and L)

(H)(L) ← (H)(L) + (rh)(rl)

The content of the register pair rp is added to the content of the register pair H and L. The result is placed in the register pair H and L. Note: Only the CY flag is affected. It is set if there is a carry out of the double precision add; otherwise it is reset.

0	0	R	P	1	0	0	1

Cycles:	3
States:	10
Addressing:	register
Flags:	CY

DAA (Decimal Adjust Accumulator)

The 8-bit number in the accumulator is adjusted to form two 4-bit Binary-Coded-Decimal digits by the following process:

1. If the value of the least significant 4 bits of the accumulator is greater than 9 or if the AC flag is set, 6 is added to the accumulator.

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2. If the value of the most significant 4 bits of the accumulator is now greater than 9, or if the CY flag is set, 6 is added to the most significant 4 bits of the accumulator.

NOTE: All flags are affected.

0	0	1	0	0	1	1	1

Cycles: 1
States: 4
Flags: Z,S,P,CY,AC

Logical Group

This group of instructions performs logical (Boolean) operations on data in registers and memory and on condition flags.

Unless indicated otherwise, all instructions in this group affect the Zero, Sign, Parity, Auxiliary Carry, and Carry flags according to the standard rules.

ANA r (AND Register)
(A) ← (A) ∧ (r)
The content of register r is logically ANDed with the content of the accumulator. The result is placed in the accumulator. The CY flag is cleared.

1	0	1	0	0	S	S	S

Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

ANA M (AND memory)
(A) ← (A) ∧ ((H)(L))
The contents of the memory location whose address is contained in the H and L registers is logically ANDed with the content of the accumulator. The CY flag is cleared.

1	0	1	0	0	1	1	0

Cycles: 2
States: 7
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

ANI data (AND immediate)
(A) ← (A) ∧ (byte 2)
The content of the second byte of the instruction is logically ANDed with the contents of the accumulator. The result is placed in the accumulator. The CY flag is cleared.

1	1	1	0	0	1	1	0
data							

Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

XRA r (Exclusive OR Register)
(A) ← (A) ∀ (r)
The content of register r is exclusive-ORed with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

1	0	1	0	1	S	S	S

Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

XRA M (Exclusive OR Memory)
(A) ← (A) ∀ ((H)(L))
The content of the memory location whose address is contained in the H and L registers is exclusive-ORed with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

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1	0	1	0	1	1	1	0

Cycles:	2
States:	7
Addressing:	reg. indirect
Flags:	Z,S,P,CY,AC

XRI data (Exclusive OR immediate)

(A) ← (A) V (byte 2)

The content of the second byte of the instruction is exclusive-ORed with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

1	1	1	0	1	1	1	0
data							

Cycles:	2
States:	7
Addressing:	immediate
Flags:	Z,S,P,CY,AC

ORA r (OR Register)

(A) ← (A) V (r)

The content of register r is inclusive-ORed with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

1	0	1	1	0	S	S	S

Cycles:	1
States:	4
Addressing:	register
Flags:	Z,S,P,CY,AC

ORA M (OR Memory)

(A) ← (A) V ((H)(L))

The content of the memory location whose address is contained in the H and L registers is inclusive-ORed with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

1	0	1	1	0	1	1	0

Cycles:	2
States:	7
Addressing:	reg. indirect
Flags:	Z,S,P,CY,AC

ORI data (OR Immediate)

(A) ← (A) V (byte 2)

The content of the second byte of the instruction is inclusive-ORed with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

1	1	1	1	0	1	1	0
data							

Cycles:	2
States:	7
Addressing:	immediate
Flags:	Z,S,P,CY,AC

CMP r (Compare Register)

(A) – (r)

The content of register r is subtracted from the accumulator. The accumulator remains unchanged. The condition flags are set as a result of the subtraction. The Z flag is set to 1 if (A) = (r). The CY flag is set to 1 if (A) < (r).

1	0	1	1	1	S	S	S

Cycles:	1
States:	4
Addressing:	register
Flags:	Z,S,P,CY,AC

CMP M (Compare memory)

(A) – ((H)(L))

The content of the memory location whose address is contained in the H and L registers is subtracted from the accumulator. The accumulator remains unchanged. The condition flags are set as a result of the subtraction. The Z flag is set to 1 of (A) = ((H)(L)). The CY flag is set to 1 if (A) < ((H)(L)).

1	0	1	1	1	1	1	0

Cycles:	2
States:	7
Addressing:	reg. indirect
Flags:	Z,S,P,CY,AC

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CPI data (Compare immediate)

$(A) - (\text{byte } 2)$

The content of the second byte of the instruction is subtracted from the accumulator. The condition flags are set by the result of the subtraction. The Z flag is set to 1 if (A) = (byte 2). The CY flag is set to 1 if (A) < (byte 2).

1	1	1	1	1	1	1	0
data							

Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

RLC (Rotate left)

$(A_{n+1}) \leftarrow (A_n); (A_0) \leftarrow (A_7)$

$(CY) \leftarrow (A_7)$

The content of the accumulator is rotated left one position. The low-order bits and the CY flag are both set to the value shifted out of the high-order bit position. Only the CY flag is affected.

0	0	0	0	0	1	1	1

Cycles: 1
States: 4
Flags: CY

RRC (Rotate right)

$(A_n) \leftarrow (A_{n-1}); (A_7) \leftarrow (A_0)$

$(CY) \leftarrow (A_0)$

The content of the accumulator is rotated right one position. The high-order bit and the CY flag are both set to the value shifted out of the low-order bit position. Only the CY flag is affected.

0	0	0	0	1	1	1	1

Cycles: 1
States: 4
Flags: CY

RAL (Rotate left through carry)

$(A_{n+1}) \leftarrow (A_n); (CY) \leftarrow (A_7)$

$(A_0) \leftarrow (CY)$

The content of the accumulator is rotated left one position through the CY flag. The low-order bit is set equal to the CY flag and the CY flag is set to the value shifted out of the high-order bit. Only the CY flag is affected.

0	0	0	1	0	1	1	1

Cycles: 1
States: 4
Flags: CY

RAR (Rotate right through carry)

$(A_n) \leftarrow (A_{n+1}); (CY) \leftarrow (A_0)$

$(A_7) \leftarrow (CY)$

The content of the accumulator is rotated right one position through the CY flag. The high-order bit is set to the CY flag and the CY flag is set to the value shifted out of the low-order bit. Only the CY flag is affected.

0	0	0	1	1	1	1	1

Cycles: 1
States: 4
Flags: CY

CMA (Complement accumulator)

$(A) \leftarrow (A)$

The contents of the accumulator are complemented (zero bits become 1, one bits become 0). No flags are affected.

0	0	1	0	1	1	1	1

Cycles: 1
States: 4
Flags: none

CMC (Complement carry)

$(CY) \leftarrow (CY)$

The CY flag is complemented. No other flags are affected.

0	0	1	1	1	1	1	1

Cycles: 1
States: 4
Flags: CY

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STC (Set carry)

(CY) ← 1

The CY flag is set to 1. No other flags are affected.

0	0	1	1	0	1	1	1

Cycles:	1
States:	4
Flags:	CY

Branch Group

This group of instructions alter normal sequential program flow.

Condition flags are not affected by an instruction in this group.

The two types of branch instructions are unconditional and conditional. Unconditional transfers simply perform the specified operation on register PC (the program counter). Conditional transfers examine the status of one of the four processor flags to determine if the specified branch is to be executed. The conditions that may be specified are as follows:

CONDITION		CCC
NZ	– not zero (Z=0)	000
Z	– zero (Z = 1)	001
NC	– no carry (C = 0)	010
C	– carry (CY = 1)	011
PO	– parity odd (P = 0)	100
PE	– parity even (P = 1)	101
P	– plus (S = 0)	110
M	– minus (S = 1)	111

JMP addr (Jump)

(PC) → (byte 3)(byte 2)

Control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction.

1	1	0	0	0	0	1	1
low-order addr							
high-order addr							

Cycles:	3
States:	10
Addressing:	immediate
Flags:	none

Jcondition addr (Conditional jump)

If (CCC),

(PC) ← (byte 3)(byte 2)

If the specified condition is true, control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction; otherwise, control continues sequentially.

1	1	C	C	C	0	1	0
low-order addr							
high-order addr							

Cycles:	3
States:	10
Addressing:	immediate
Flags:	none

CALL addr (Call)

((SP) – 1) ← (PCH)

((SP) – 2) ← (PCL)

(SP) ← (SP) – 2

(PC) ← (byte 3)(byte 2)

The high-order 8 bits of the next instruction address are moved to the memory location whose address is one less than the content of register SP. The low-order 8 bits of the next instruction address are moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by 2. Control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction.

1	1	0	0	1	1	0	1
low-order addr							
high-order addr							

Cycles:	5
States:	17
Addressing:	immed./reg. indirect
Flags:	none

Ccondition addr (Condition call)

If (CCC),

$((SP) - 1) \leftarrow (PCH)$

$((SP) - 2) \leftarrow (PCL)$

$(SP) \leftarrow (SP) - 2$

$(PC) \leftarrow (\text{byte } 3)(\text{byte } 2)$

If the specified condition is true, the actions specified in the CALL instruction (see above) are performed; otherwise, control continues sequentially.

1	1	C	C	C	1	0	0
low-order addr							
high-order addr							

Cycles:	3/5
States:	11/17
Addressing:	immed./reg. indirect
Flags:	none

RET (Return)

$(PCL) \leftarrow ((SP));$

$(PCH) \leftarrow ((SP) + 1);$

$(SP) \leftarrow (SP) + 2;$

The content of the memory location whose address is specified in register SP is moved to the low-order 8 bits of register PC. The content of the memory location whose address is one more than the content of register SP is moved to the high-order 8 bits of register PC. The content of register SP is incremented by 2.

1	1	0	0	1	0	0	1

Cycles:	3
States:	10
Addressing:	reg. indirect
Flags:	none

Rcondition (Conditional return)

If (CCC),

$(PCL) \leftarrow ((SP))$

$(PCH) \leftarrow ((SP) + 1)$

$(SP) \leftarrow (SP) + 2$

If the specified condition is true, the actions specified in the RET instruction (see above) are performed; otherwise, control continues sequentially.

1	1	C	C	C	0	0	0

Cycles:	1/3
States:	5/11
Addressing:	reg. indirect
Flags:	none

RST n (Restart)

$((SP) - 1) \leftarrow (PCH)$

$((SP) - 2) \leftarrow (PCL)$

$(SP) \leftarrow (SP) - 2$

$(PC) \leftarrow 8 * (NNN)$

The high-order 8 bits of the next instruction address are moved to the memory location whose address is one less than the content of register SP. The low-order 8 bits of the next instruction address are moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by two. Control is transferred to the instruction whose address is eight times the content of NNN.

1	1	N	N	N	1	1	1

Cycles:	3
States:	11
Addressing:	reg. indirect
Flags:	none

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	N	N	N	0	0	0

Program Counter After Restart

PCHL (Jump H and L indirect – move H and L to PC)

$(PCH) \leftarrow (H)$

$(PCL) \leftarrow (L)$

The content of register H is moved to the high-order 8 bits of register PC. The content of register L is moved to the low-order 8 bits of register PC.

1	1	1	0	1	0	0	1

Cycles:	1
States:	5
Addressing:	register
Flags:	none

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Stack, I/O, and Machine Control Group

This group of instructions performs I/O, manipulates the Stack, and alters internal control flags.

Unless otherwise specified, condition flags are not affected by any instructions in this group.

PUSH rp (Push)

$((SP) - 1) \leftarrow (rh)$
$((SP) - 2) \leftarrow (rl)$
$(SP) \leftarrow (SP) - 2$

The content of the high-order register of register pair rp is moved to the memory location whose address is one less than the content of register SP. The content of the low-order register of register pair rp is moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by 2. Note: Register pair rp=SP may not be specified.

1	1	R	P	0	1	0	1

Cycles:	3
States:	11
Addressing:	reg. indirect
Flags:	none

PUSH PSW (Push processor status word)

$((SP) - 1) \leftarrow (A)$
$((SP) - 2)_0 \leftarrow (CY, ((SP) - 2)_1 \leftarrow 1$
$((SP) - 2)_2 \leftarrow (P), ((SP) - 2)_3 \leftarrow 0$
$((SP) - 2)_4 \leftarrow (AC), ((SP) - 2)_5 \leftarrow 0$
$((SP) - 2)_6 \leftarrow (Z), ((SP) - 2)_7 \leftarrow (S)$
$(SP) \leftarrow (SP) - 2$

The content of register A is moved to the memory location whose address is one less than register SP. The contents of the condition flags are assembled into a processor status word and the word is moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by two.

1	1	1	1	0	1	0	1

Cycles:	3
States:	11
Addressing:	reg. indirect
Flags:	none

FLAG WORD

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z	0	AC	0	P	1	CY

POP rp (Pop)

$(rl) \leftarrow ((SP))$
$(rh) \leftarrow ((SP) + 1)$
$(SP) \leftarrow (SP) + 2$

The content of the memory location, whose address is specified ~~by~~ the content of register SP, is moved to the low-order register of register pair rp. The content of the memory location, whose address is one more than the content of register SP, is moved to the high-order register of register pait rp. The content of register SP is incremented by 2. Note: Register pair rp=SP may not be specified.

1	1	R	P	0	0	0	1

Cycles:	3
States:	10
Addressing:	reg. indirect.
Flags:	none

POP PSW (Pop processor status word)

$(CY) \leftarrow ((SP))_0$
$(P) \leftarrow ((SP))_2$
$(AC) \leftarrow ((SP))_4$
$(Z) \leftarrow ((SP))_6$
$(S) \leftarrow ((SP))_7$
$(A) \leftarrow ((SP) + 1)$
$(SP) \leftarrow (SP) + 2$

The content of the memory location whose address is specified by the content of register SP is used to restore the condition flags. The content of the memory location whose address is one more than the content of register SP is moved to register A. The content of register SP is incremented by 2.

1	1	1	1	0	0	0	1

Cycles:	3
States:	10
Addressing:	reg. indirect
Flags:	Z,S,P,CY,AC

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XTHL (Exchange stack top with H and L)

(L) ↔ ((SP))

(H) ↔ ((SP) + 1)

The content of the L register is exchanged with the content of the memory location whose address is specified by the content of register SP. The content of the H register is exchanged with the content of the memory location whose address is one more than the content of register SP.

1	1	1	0	0	0	1	1

Cycles:	5
States:	18
Addressing:	reg. indirect
Flags:	none

SPHL (Move HL to SP)

(SP) ← (H)(L)

The contents of registers H and L (16 bits) are moved to register SP.

1	1	1	1	1	0	0	1

Cycles:	1
States:	5
Addressing:	register
Flags:	none

IN port (Input)

(A) ← (data)

The data placed on the 8-bit bidirectional data bus by the specified port is moved to register A.

1	1	0	1	1	0	1	1
port							

Cycles:	3
States:	10
Addressing:	direct
Flags:	none

OUT port (Output)

(data) ← (A)

The content of register A is placed on the 8-bit bidirectional data bus for transmission to the specified port.

1	1	0	1	0	0	1	1
port							

Cycles:	3
States:	10
Addressing:	direct
Flags:	none

EI (Enable interrupt)

The interrupt system is enabled following the execution of the next instruction.

1	1	1	1	1	0	1	1

Cycles:	1
States:	4
Flags:	none

DI (Disable interrupts)

The interrupt system is disabled immediately following the execution of the DI instruction.

1	1	1	1	0	0	1	1

Cycles:	1
States:	4
Flags:	none

HLT (Halt)

The processor is stopped. The registers and flags are unaffected.

0	1	1	1	0	1	1	0

Cycles:	1
States:	7
Flags:	none

NOP (No op)

No operation is performed. The registers and flags are unaffected.

0	0	0	0	0	0	0	0

Cycles:	1
States:	4
Flags:	none

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INSTRUCTION SET

Summary of Processor Instructions

MNEMONIC	DESCRIPTION	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CLOCK[2] CYCLES
MOV$_{r1,r2}$	Move register to register	0	1	D	D	D	S	S	S	5
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7
HLT	Halt	0	1	1	1	0	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVL M	Move immediate memory	0	0	1	1	0	1	1	0	10
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11

MNEMONIC	DESCRIPTION	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CLOCK[2] CYCLES
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RST	Restart	1	1	A	A	A	1	1	1	11
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
XTHL	Exchange top of stock H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4

NOTES: 1. DDD or SSS – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.
2. Two possible cycle times, (5/11) indicate instruction cycles dependent on condition flags.

All Mnemonics © 1976, 1977, Intel Corp.

SERIAL I/O WIRING FOR SBC 80/20

SBC 80/20 TO RS232C ADAPTER CABLE WIRING CONNECTIONS

SBC 80/20 PWA 1000817		OEM RS232C I/O CABLE PWA 4000677		
	J3	P3		PX*
▷ Protective Ground	2	1	——	1
▷ Secondary Transmitted Data	1	2	——	14
Transmitted Data	4	3	——	2
Transmitter Signal Element Timing	3	4	——	15
Received Data	6	5	——	3
▷ Secondary Received Data	5	6	——	16
Request to Send	8	7	——	4
Receiver Signal Element Timing	7	8	——	17
Clear to Send	10	9	——	5
(No connection)	9	10	——	18
Data Set Ready	12	11	——	6
▷ Secondary Request to Send	11	12	——	19
Signal Ground	14	13	——	7
Data Terminal Ready	13	14	——	20
Received Line Signal Detect	16	15	——	8
(No connection)	15	16	——	21
(No connection)	18	17	——	9
Ring Indicator	17	18	——	22
(No connection)	20	19	——	10
▷ TTY Adapter Power (-12V)	19	20	——	23
▷ TTY Adapter Power (+12V)	22	21	——	11
▷ Transmitter Signal Element Timing	21	22	——	24
(No connection)	24	23	——	12
▷ (+5V)	23	24	——	25
▷ Secondary Clear to Send	26	25	——	13
Signal Ground	25	26		

▷ Jumper Option

* PX is the commonly used 25 pin connector.

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