

gni-909

---

**character  
input/output  
interface**



**GRI Computer Corporation**

320 NEEDHAM STREET, NEWTON, MASSACHUSETTS 02164

GRI-909

CHARACTER INPUT/OUTPUT INTERFACE MANUAL

GRI Computer Corporation, 320 Needham Street, Newton, Massachusetts 02164

© May 1971 by GRI Computer Corporation

10-40-004-A

# CHARACTER INPUT/OUTPUT INTERFACE MANUAL

## TABLE OF CONTENTS

### CHAPTER ONE

1.0	Introduction . . . . .	1-1
1.1	Specifications . . . . .	1-1
1.2	Installation and Testing . . . . .	1-4
1.3	Programming . . . . .	1-4
1.4	Character Input Interface Operation . . . . .	1-7

### CHAPTER TWO

2.0	Introduction . . . . .	2-1
2.1	Specifications . . . . .	2-1
2.2	Installation and Testing . . . . .	2-4
2.3	Programming . . . . .	2-5
2.4	Theory of Operation . . . . .	2-7

## CHAPTER ONE

### CHARACTER INPUT INTERFACE

#### 1.0 Introduction:

The Character Input Interface card is a generalized serial asynchronous receiver card. The card contains its own clock circuit and is capable of full duplex operation (4 wire operation) from 110 baud to 9600 baud by simple changes to the timing components in the clock circuit. It is primarily used as a teletype or data communications interface.

Figure 1-1 is a block diagram of the Character Input Interface.

#### 1.1 Specifications:

##### Input:

- A. Control signals from the processor as shown in Figure 2-1, the block diagram of the Character Output Interface.
- B. The 8-bit data word to be sent to the output device. This word is stored in the parallel to serial converter until transmission has started.
- C. Power: 0.5 amps of +5v (average).

##### Output:

- A. Control signals from the processor.
- B. A serial train of the data being sent to the output device. This can be either the
  - 1) 20 ma required to complete the current loop provided by the teletype.

- 2) The current necessary to drive the CRT displays (S42-015 through S42-018) display.
- 3) The voltages conforming to the RS-232 Interface Specification.

Sequence:

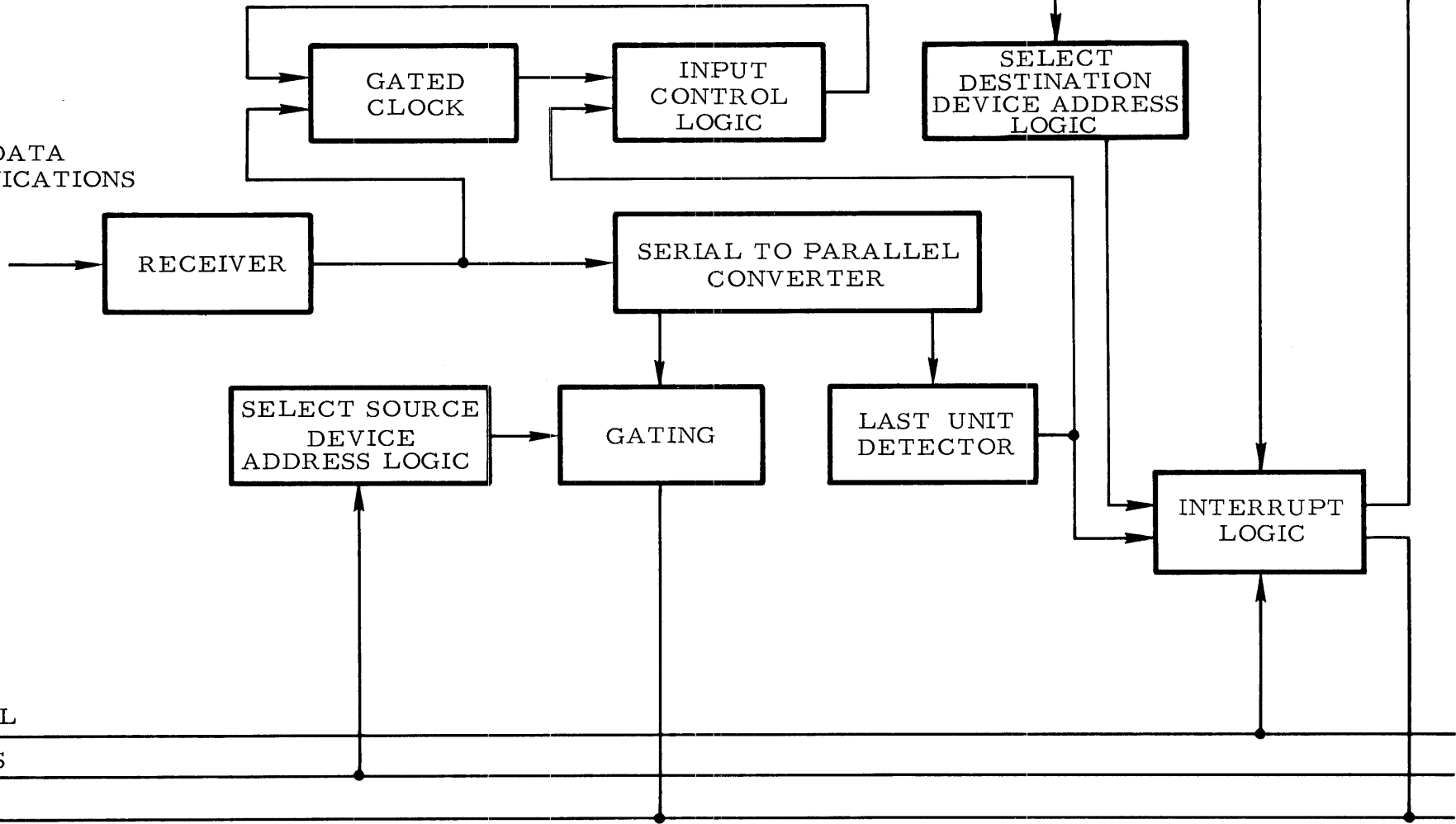
In use, the character to be sent to the output device is transmitted to the Character Output Interface under program control. When the interface receives the character, it starts the output device, transmits the character, and when the transmission is complete, causes an interrupt to occur.

SOURCE BUS  
DATA

ADDRESS

CONTROL

FROM  
SERIAL DATA  
COMMUNICATIONS  
DEVICE



CONTROL

ADDRESS

DATA

DESTINATION BUS

Figure 1-1 CHARACTER INPUT INTERFACE

## 1.2 Installation and Testing:

The Character Input Interface is plugged into the rear of the computer (components facing to the right). For priority purposes, it should be installed to the right of any other interfaces that have interrupts, since it and the Character Output Interface are the lowest speed devices in the product line. The Character Input Interface should be to the left of the Character Output Interface, since the input side of a device is considered as a higher priority than the output. Any unused slots to the left of the boards should be jumpered with shorting pins (S40-215) in positions S-5, E and S-6, F in order to permit proper operation of the interrupt system. NOTE: This includes the option slots 01 and 02 in the processor.

Connections to the Character Input Interface are made through AMP 583167-1 connectors. Standard cables are available for connecting to an ASR-33 teletype and the CRT keyboard displays.

Teletype usage requires a modification to the teletype to allow remote selection of the reader. This is done with a modification kit S40-212, which contains the necessary hardware and instructions for the modification. All teletypes obtained from GRI, of course, have the modification in them.

Connections to other devices should use the complete cable clamp assembly available (S40-203) which includes the connector.

## 1.3 Programming:

### Instructions:

The Character Input Interface is a source of data only. The

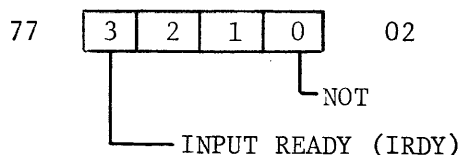
standard system address is

SDA = 77

and has been assigned the mnemonic Character Input Interface. Data is removed from the device over DB bits 0-7 (one byte's worth) by any register or memory reference instruction. The data in the Character Input Interface may also be tested via a data test instruction for 0. The flag must be cleared after servicing the device. A character transmitted to the Character Input Interface in standard 11 bits, asynchronous code will be accumulated in parallel form, causing the Character Input Interface flag to set when the serial to parallel conversion is complete. The following sense function and function output commands are available on the Character Input Interface. A start function command is also provided for remote operation of a teletype reader.

SF Commands

Machine Format



FAST:

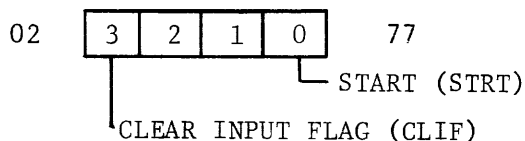
SKIP IF CHARACTER INPUT INTERFACE [NOT] READY

BASE:

SF CHARACTER INPUT INTERFACE, [NOT]IRDY

FO Commands

Machine Format





FAST:

CLIF TO CHARACTER INPUT INTERFACE  
STRT TO CHARACTER INPUT INTERFACE  
CLIF STRT TO CHARACTER INPUT INTERFACE

BASE:

FO CLIF, CHARACTER INPUT INTERFACE  
FO STRT, CHARACTER INPUT INTERFACE  
FO CLIF STRT, CHARACTER INPUT INTERFACE

The START function command provides a separate control pulse out of the interface for remote control of a device like a teletype reader. The pulse is used to signal for the transmission of a character or stream of characters.

#### Interrupt Functions:

The basic Character Input Interface is assigned to status bit 1 (ISR1). When an interrupt occurs, the Character Input Interface generates address  $14_8$  for saving the sequence counter. Control is transferred to address  $15_8$  during the interrupt. When power is turned on, or the start key is depressed, the Character Input Interface flag is cleared and the status bit is cleared.

#### Programming:

Programmed operation of the interface is very simple. When data is available in the Character Input Interface buffer, the flag will set. If the program waits for the setting of the flag, it may remove data each time the flag sets. This is often referred to as a wait

loop. A typical service routine for handling the keyboard and delivering the character to AX would be:

BASE:

```
GETC: SF CHARACTER INPUT INTERFACE,IRDY ;CHARACTER INPUT INTERFACE ready
      MRI GETC-1,SC ;no, wait
      RR CHARACTER INPUT INTERFACE,AX ;yes, fetch character
      FO CLIF,CHARACTER INPUT INTERFACE ;clear flag
      RR TRP,SC ;return from subroutine
```

FAST:

```
GETC: SKIP IF CHARACTER INPUT INTERFACE IRDY ;ready?
      I GETC-1 TO SC ;no, wait
      CHARACTER INPUT INTERFACE TO AX ;yes, fetch
      CLIF TO CHARACTER INPUT INTERFACE ;clear flag
      TRP TO SC ;return from subroutine
```

#### 1.4 Character Input Interface Operation:

The Character Input Interface character is based on eleven unit code consisting of 1 start bit, 8 data bits, and 2 stop bits. The 8 data bits are shifted into a serial to parallel converter. The operational detail that follows is a discussion of logic print D-17-49-003.

The Character Input Interface clock is idle whenever the incoming line is held in the marking condition. When the line shifts from mark to space (the start bit), the clock is turned on and the DIV flip flop (H1-12) starts dividing the clock rate by two. A single pulse is produced at A1-3 which causes the ACT (A2-12) flip flop to set. ACT will now be used to keep the clock running after the start unit is gone. This single start pulse (A1-3) also clears all bits in serial-parallel converter (G2,E2) to 0's. These devices

are used in their reverse sense (i.e. to 0 output is used as a 1's output), and the act of clearing them is logically equivalent to setting the flip flops to all 1's. The start unit (a space element) is equivalent to a 0 and is entered into the left hand end of the serial-parallel converter on the first shift pulse that is gated out at L0-10. This 0 will become the stop signal when it arrives at the far right hand end of the serial-parallel converter (E2-11). Each shift pulse shifts another code element into the register. As the 8th element enters the register, the start element leaves the 8th bit of the register and shifts into LU (C1-9), causing it to set, signaling the end of shifting operations on the register. The flag TIF sets at the same time.

The two stop codes will be marked off by the LU and ACTIVE flip flops. Now that LU is set, the next clock pulse resets ACT. The clock, however, is kept running by the LU flip flop which is still set. The next clock pulse, which represents the second stop unit, will cause LU to reset, which finally stops the clock. Note that the flag TIF (C1-12) sets as soon as the 8th code element has been shifted into the register. The data will remain stable through the two unit stop codes before another start element may be received. The timing diagram for the Character Input Interface operation is C-13-49-000.

The Character Input Interface receiver B-11-49-001 provides a loop bias current from -A in the processor. This is intended for switching by a dry switch such as the commutator in the teletype. The input is clamped to ground through a diode to prevent back

swings from injuring the input circuit. The receiver may be used as a voltage actuated device by referencing the voltage to ground. If the 1K resistor in series with the base is changed to 3K, the receiver will now function as an RS-232 receiver. A nominal input of +12 volts may be used with -12 volts = MARK and +12 volts = SPACE. Note that the circuit may also be driven by TTL levels with 0V = MARK and +5v = SPACE.

The baud rate of the board may be changed by altering the values of R1 and C1 of the Character Input Interface clock (B-11-40-023). For higher frequencies, R4 has to be changed also. The table of 1.4 also applies to the Character Input Interface circuit.

The trimmer R2 is used to give a limited adjustment capability for final tuning of the clock frequency. This adjustment need only be made once for a given set of R1 and C1 components. The adjustment should then be glyptol'd in place.

\*For baud rates above 300, the .22uf filter capacitor on the Character Input Interface receiver (B-11-49-001) must be removed or decreased.

## CHAPTER TWO

### CHARACTER OUTPUT INTERFACE

#### 2.0 Introduction:

The Character Output Interface card is a generalized asynchronous transmitter card. The card contains its own clock circuit and is capable of full duplex operation (4 wire operation) from 110 baud to 9600 baud by simple changes to the timing components in the clock circuit. It is primarily used as a teletype or data communications interface.

A block diagram of the Character Output Interface card is shown in Figure 2-1.

#### 2.1 Specifications:

##### Input:

- A. Control signals from the processor as shown in Figure 2-1.
- B. A serial train of data pulses being sent from the input device. These can be either the
  - 1) 20 ma required to complete the current loop provided by the teletype.
  - 2) Current from a display.
  - 3) Voltages conforming to the RS-232 Interface Specification.
- C. Power: 0.5 amps of +5v (average).

##### Output:

- A. Control signals as shown on the block diagram.

- B. The 8-bit data word received from the input device. This word is stored in the serial to parallel converter until it is transferred into the processor under program control.

Sequence:

In use, the character input interface interrupts the processor when its 8-bit serial to parallel converter slant buffer is filled. The program transfers the contents of the buffer either to memory or to another register and clears the flag. The interface is then ready to receive another character.

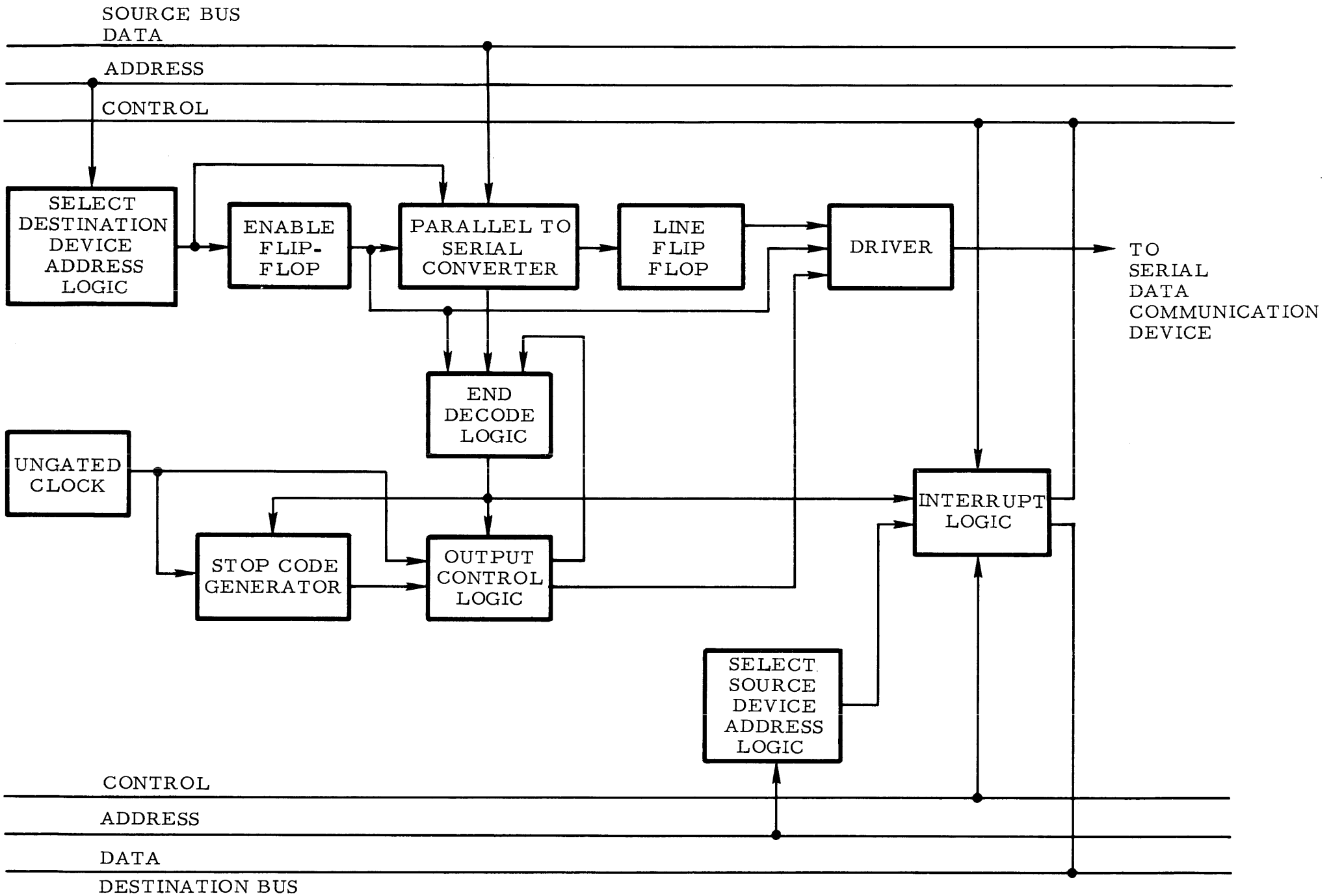


Figure 2-1. CHARACTER OUTPUT INTERFACE

## 2.2 Installation and Testing:

The Character Output Interface is plugged into the rear of the computer (components facing to the right). For priority purposes, it should be installed to the right of any other interfaces that have interrupts, since it and the Character Input Interface are the lowest speed devices in the product line. The Character Input Interface should be to the left of the Character Output Interface, since the input side of a device is considered as a higher priority than the output. Any unused slots to the left of the boards should be jumpered with shorting pins (S40-215) in positions S-5, E and S-6, F in order to permit proper operation of the interrupt system. NOTE: This includes the option slots 01 and 02 in the processor.

Connections to the Character Output Interface are made through AMP 583167-1 connectors. Standard cables are available for connection to an ASR-33 teletype and the CRT keyboard displays.

Teletype usage requires a modification to the teletype to allow remote selection of the reader. This is done with a modification kit S40-212, which contains the necessary hardware and instructions for the modification. All teletypes obtained from GRI, of course, have the modification in them.

Connections to other devices should use the complete cable clamp assembly available (S40-203) which includes the connector.



### 2.3 Programming:

#### Instructions:

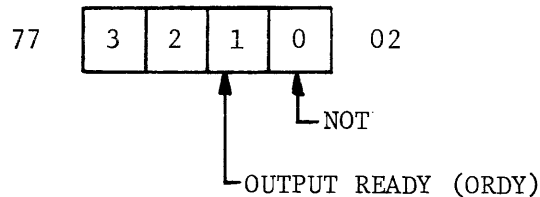
The Character Output Interface is a destination of data only.  
The standard system address is

$$DDA = 77$$

and has been assigned the mnemonic Character Output Interface. Data is delivered to the device over SB bits 0-7 (one byte's worth) by any register or memory reference instruction. The delivery of data automatically clears the flag and starts an output operation. During the output operation, the parallel byte of information is delivered as an eleven bit serial stream of data. When the serialization process is complete, the flag is set to notify the computer of completion. The following sense function and function output commands are available on the Character Output Interface.

SF Commands

Machine Format



FAST:

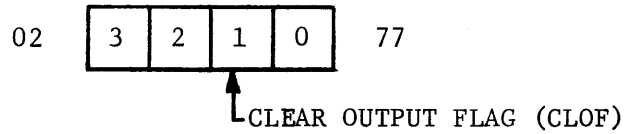
SKIP IF CHARACTER OUTPUT INTERFACE NOT ORDY

BASE:

SF CHARACTER OUTPUT INTERFACE, NOT ORDY

FO Commands

Machine Format



FAST:

CLOF TO CHARACTER OUTPUT INTERFACE

BASE:

FO CLOF, CHARACTER OUTPUT INTERFACE

Interrupt Functions:

The basic Character Output Interface is assigned to status bit 0 (ISR 0). When an interrupt occurs, the Character Output Interface generates address  $11_8$  for saving the sequence counter. Control is transferred to address  $12_8$  during the interrupt. When power is turned on or the start key is depressed, the Character Output Interface flag is set, and the status bit is cleared.

Programming:

Programmed operation of the interface is very simple. Prior to delivering a data word to the Character Output Interface, its flag should be checked to see if the device is still in operation from the last output operation. Thus, a simple service subroutine to output the contents of AX would be:

BASE

```

PUTC: SF CHARACTER OUTPUT INTERFACE,ORDY ;CHARACTER OUTPUT INTERFACE busy?
      MRI PUTC-1,SC ;yes, wait
      RR AX,CHARACTER OUTPUT INTERFACE ;no, output character in AXO-7
      RR TRP,SC ;return from subroutine
    
```

FAST

```

PUTC: SKIP IF CHARACTER OUTPUT INTERFACE ORDY ;busy?
    
```

#### 2.4 Theory of Operation:

The timing of the Character Output Interface is based on the eleven unit code consisting of 1 start bit, 8 data bits, and 2 stop bits. The 8 data bits are stored in a parallel to serial converter. The serial shift register is extended by a bit in front of the register called ENABLE (EN) and a bit behind called LINE. Drawing C-13-49-001 is a timing diagram showing the transmission of the 8 bit character 01010101. The output is formed least significant bit first. The data communications terminology for a "1" is "MARK" and for a "0" is "SPACE". An asynchronous data stream carries with it a timing synchronizing marker to allow a receiver to synchronize its clock with the incoming data stream. The start bit (first shift from MARK to SPACE) provides that sync function. The Character Output Interface clock free runs at twice the baud rate.

A character is loaded by transferring data to the register. This also causes ENABLE (E2-12) to set. The ACTIVE (ACT) flip flop (F2-12) sets on the trailing edge of the next Character Output Interface clock pulse. ACT, however, is not permitted to set unless the two

stop codes (STOP 1 and STOP 2) have been completed. When ACT sets, the DIV flip flop is enabled and it begins complementing, thus dividing the clock frequency by 2. The DIV flip flop output is gated against the clock to produce shift pulses (A1-3) at the proper baud rate. The EN and ACT states are gated together to produce the start bit at the output of the Character Output Interface line (C1-6). The EN bit is shifted into bit 7 of the shift register and the least significant bit of the character enters the LINE flip flop and thus presents the first unit of code on the Character Output Interface line. The shift pulses continue to empty the shift register. When bits 7-1 and EN have emptied, the END DECODE signal is produced (B1-4) which permits the flag TOF to set (H1-12) as the eighth data bit is shifted out on the line. The END DECODE also enables the STOP 1 flip flop (G2-12). The STOP 2 flip flop (G2-9) sets on the next clock pulse and enables the resetting of STOP 1 on the next clock pulse. This sequence guarantees 2 stop units at the end of the bit stream. The logic print for the Character Output Interface is D-17-49-007. The interrupt logic shown is explained in greater detail in the reference manual section on interfacing.

The output circuit for Character Output Interface is shown in B-11-49-000. The output provides a switch (03) for completing the 20ma MARK current loop provided by the teletype. The switch may also be used to drive the Infoton terminal current loop by providing a bias to -A through 1K (see B-11-49-000).

The baud rate of the board may be changed by altering the values of R1 and C1 of the Character Output Interface clock (B-11-40-022). For higher frequencies, R4 has to be changed also. The following table gives values of R1 and C1 for various baud rates.

<u>Baud</u>	<u>TTOF</u> Hz	<u>R1</u> ohms	<u>C1</u> uf	<u>R4</u> ohms
110	220	20K	0.22	56
*300	600	20K	0.082	56
600	1200	20K	0.04	56
1200	2400	10K	0.022	100
1800	3600	10K	0.015	100
2400	4800	10K	0.01	100
4800	9600	4.7K	0.01	100
9600	19200	3.3K	0.0047	100

The trimmer R2 is used to give a limited adjustment capability for final tuning of the clock frequency. This adjustment need only be made once for a given set of R1 and C1 components. The adjustment should then be glyptol'd in place.

\*For baud rates above 300, the small filter capacitor C2 on the output circuit B-11-49-000 must be removed to prevent excessive filtering of the output signal.



 **GRI Computer Corporation**

320 NEEDHAM STREET, NEWTON, MASSACHUSETTS 02164

TEL: (617) 969-0800