gri-909

interval timer manual

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INTERVAL TIMER

MANUAL

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INTERVAL TIMER MANUAL

1.0 Introduction:

The interval timer is used to time the period between control actions in a process or to measure an elapsed time interval.

A watchdog timer may be used to indicate that a control program is operating correctly.

This manual describes the combination watchdog/interval timer. When it is necessary, a characteristic of either will be described separately.

1.1 Specifications:

Input:

a. Timing signals can come from three sources

   1) Oscillator with a frequency specified by the user but within the range 25 KHz to 10 MHz.

   2) Timing signals obtained from the power line (not to exceed 14v AC).

   3) Timing signals obtained directly from the process (not to exceed ±14v).

b. Control signals from the computer as shown in Figure 1-1, the block diagram of the interval timer.

c. Power: 0.3 amperes at +5v.

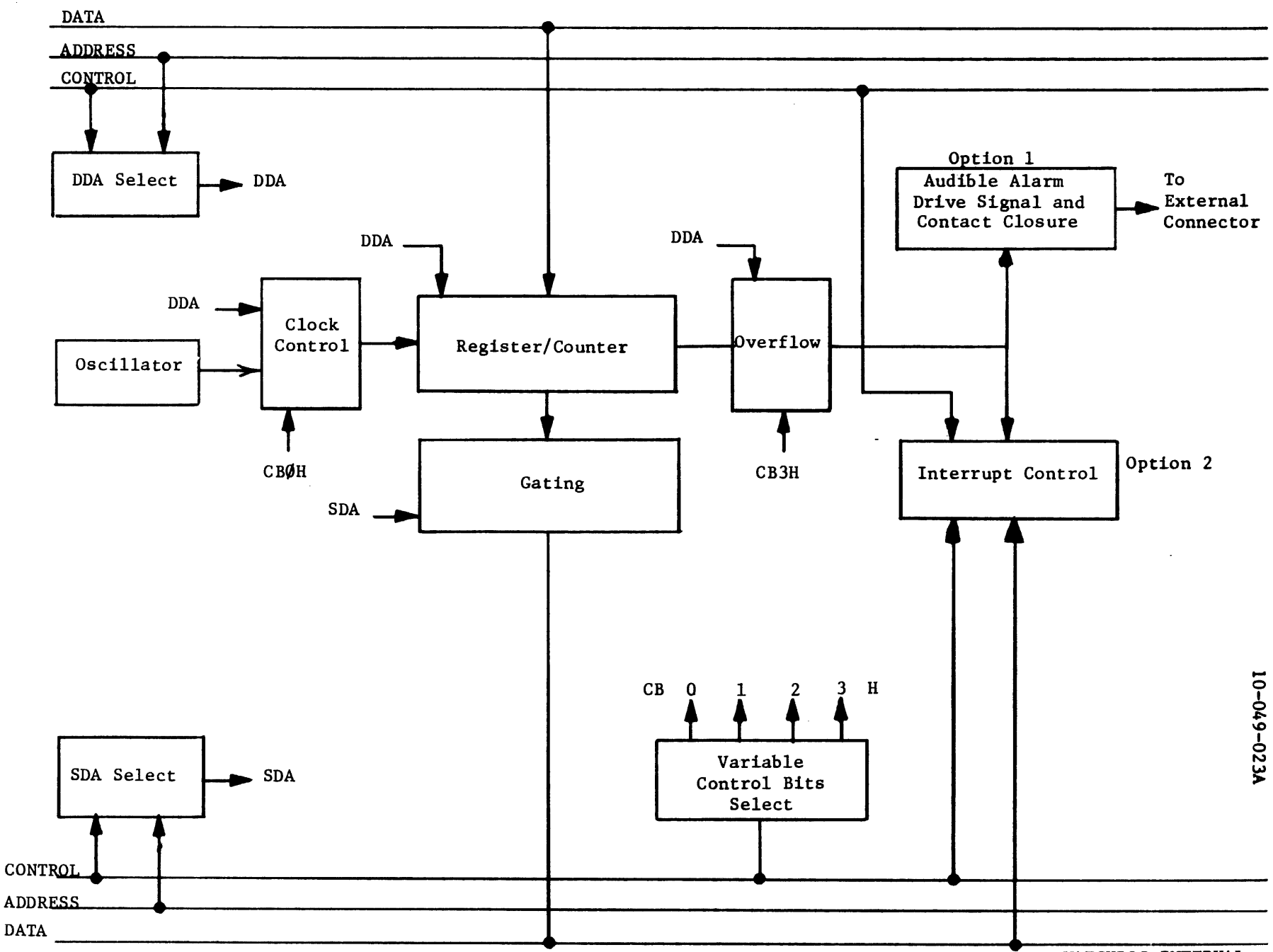

Fig. 1-1 BLOCK DIAGRAM OF THE INTERVAL TIMER

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Interval Timer
10-049-023A

Output:

a. The output from the interval timer is an interrupt which diverts the main program to a subroutine designed to handle the interval timer.

b. The watchdog timer output is a signal to drive a Mallory Sonalert or equivalent and a contact closure rated as follows:

1) Form: SPDT

2) Current: 1/4 amp

3) Voltage: 28v

4) Resistance: 0.15 ohms

5) Power: 3w

Sequence:

INTERVAL TIMER

(Measurement of an elapsed time interval)
Load the timer with the two's complement of a predetermined count under program control. Then, start the clock. The interrupt causes the program to transfer to a routine to perform some action. (when an overflow occurs).

WATCHDOG TIMER

This timer is used in a similar manner except that the predetermined count depends on the iteration time of the application program. It should never overflow, because such an occurrence indicates that the program is malfunctioning and is not controlling the process. If this overflow occurs, a contact closure occurs which may be

used to sound an audible or visual alarm (user supplied).

1.2 Installation and Testing:

The WIT is installed in any location in the I/O bus at the rear of the chassis. Since the Interval Timer uses the priority system, it is necessary to add jumpers between PINL and POUTL (Source Bus pins 5 and E) and DINL and DOUTL (Source bus pins 6 and F) in vacant slots to the left of the WIT board. Location does not matter for the Watchdog Timer.

The WIT is normally wired for system address 60, but the user may easily change the address to any unused source and destination address according to the instructions in Appendix A of this manual.

FO command bits are used to control the WIT, therefore, staples on the printed circuit board must be clipped as described in Appendix A. Note that two or more interval timers can be installed, but the source and destination addresses must be different. The interrupt trap locations could be the same (the program then tests their flags) or two different locations may be used.

External Connections:

Connections to an from the WIT are as follows:

External timing signal	Ec
Relay contact - common	Ez
Relay contact - NO	Ey
Relay contact - NC	Eb
Audible alarm	Ea

Testing:

The best way to test WIT is to use the diagnostic DWIT. Keyed in loops can be used to see if the device interrupts to the correct address but only under program control can the correct operation of the operator be insured.

A suggested keyed-in loop is as follows:

Location	Code	Instruction	
00	06 0010 04	I 100000 to ISR	;Set ISR bit
01	100000		
02	02 0010 04	ICO	;Turn on Interrupt
03	00 0010 60	C ZERO TO WIT	;Set WIT to -1
04	02 1001 60	CLEAR START TO WIT	
05	00 0100 03	GO TO .-1	;Wait for Interrupt
06	00005		
25	000000		
26	02 0000 60	STOP TO WIT	;Stop timer
27	02 0100 00	HLT	;Stop machine

1.3 Programming:

Coding the operator to time out an interval should be as follows:

```
06 0010 60        I -10 TO WIT              ;Set count in WIT
  177770
06 0010 04        I 100000 TO ISR           ;Set ISR bit
  100000
02 0010 04        ICO                       ;Interrupt control on
02 1001 60        CLEAR START TO WIT        ;Turn on counter
   XXXX
```

at Location 25

```
  000000          NOP                       ;TRP stored here
02 0000 60        STOP TO WIT
   YYYY
```

where the section called XXXX might be the main function(s) being performed under program control and the section YYYY might be a series of tests which need to be performed periodically such as: is there any more need for functionXXXX?

Example: If a timer with a period of one second were being used with this program function, XXXX would be stopped after ten (octal) seconds of operation and function YYYY would be executed.

1.4 Theory of Operation:

This discussion incorporates only the highlights of device operation. Troubleshooting can be facilitated through

use of detailed logic diagram D-17-049-023.

Load the two's complement of the predetermined count into the WIT's counter, utilize a programmed data transfer. Turn on the clock control (CLC) with a function generator instruction to deliver a pulse to a D-type flip-flop.

Initially, the counter contains a negative number; hence, Bit 15 is high. An overflow occur, i.e., Bit 15 goes low when the number of pulses from the timing source equals the count. The overflow sets the OV flip-flop (J1-9) if the clock control is on. OV is gated with the clock control because Bit 15 could also switch from high to low when the device is being used as a general purpose register. An interrupt should occur. When the device is being used as an interval timer, the output from OV (1) sets the device interrupt request flip flop at ISYNH time, and an interrupt request will occur.

If the device is being used as a Watchdog Timer, the output from OV (1) will operate a relay and a customer-supplied audio alarm if the alarm is connected to the device.

For complete operational details refer to the GRI 909 System Reference Manual.

APPENDIX A

INSTRUCTIONS FOR DEVICE ADDRESS AND INTERRUPT SELECTION

Device Address Selection (Figure 1):

The device address selection consists of a dual row of staples marked "1" and "0" surrounding decoders (7430) in positions AL (DAB decode) and L1 (SAB decode). To set an address in a board, insert staples in row "1" for those SAB or DAB bits which are to be decoded as 1's. Insert staples in row "0" for those SAB or DAB bits which are to be decoded as 0's. The example shown is for an address 65_8.

Device Interrupt Control (Figure 2):

Some devices provide for a choice of interrupt status bit and interrupt address generation. Where the interrupt status bit is to be chosen, the same SB and DB bits must be chosen. Interrupt address generation provides for up to four 1's to be generated on any of the 16 DB lines. For example, assume that the desired interrupt address for a device is 45_8, 46_8, 47_8. The first address of the group is the only one that needs to be generated, and this will be the address that the SC is stored in when the interrupt occurs. The generated address plus 1 (46_8) will be the location in which program operation resumes after the interrupt. To generate 45_8, we need three 1's generated, e.g:

$$45_8 = 100101_2$$

DB bits 0, 2, 5 must be connected to the address generator gates. note that one of the four gates is not required and is, therefore, left open.

The wiring of interrupt functions is described in each device manual in a tabular form.

All device operators are set at the factory, for a specific device address and interrupt controls, to facilitate testing of the boards. The user may alter these address, if he so desires, by following the instructions in the device manual. In systems where multiples of the same operator are used, the user must, of course, change the addresses and interrupt controls.

The interrupt controls, however, need not all be different. The same status bit, for example, is often assigned to a group of like devices. For example, 5 general output registers are put into a system. They may all be assigned to the same status bit, but each one will generate a unique interrupt address. When all boards are on the same status bit level, there is a hardware priority imposed by the order in which the boards are plugged into the rear of the GRI-909. This priority is determined by the PINL-POUTL chain and runs from left to right (highest to lowest) looking at the rear of the machine.

5.0 Debugging Aid:

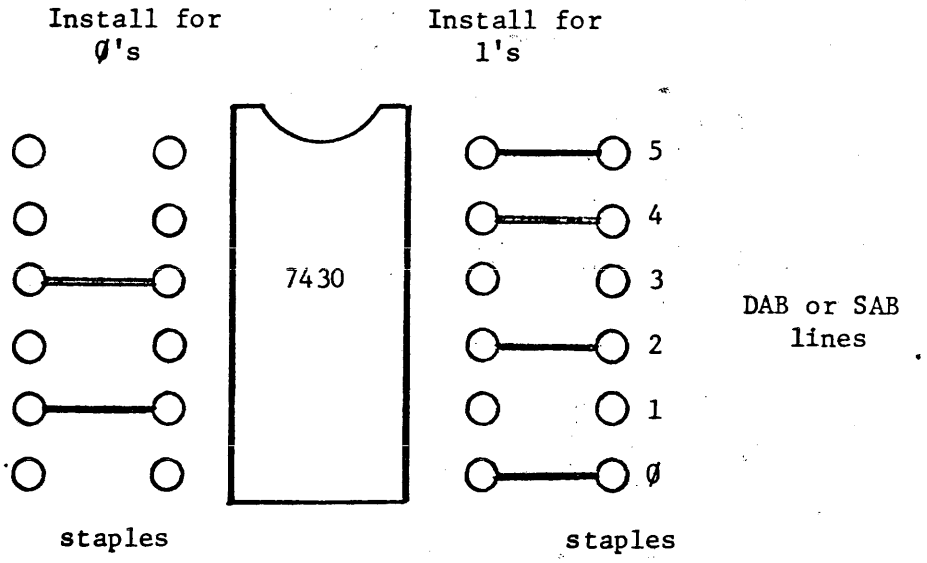
The following loop is helpful when using a scope on the timer.

Location	Code	Instruction	
000020	06 0010 04	MRI 100000,ISR	;Turn on
000021	100000		;Interrupt
000022	02 0010 04	FOI ICO	
000023	00 0010 60	ZRC 60	;Set to -1
000024	02 1001 60	FO clear start, 60	
000025	000000	NOP	
000026	02 0000 60	FO stop, 60	
000027	00 0000 06	ZM 25	
000030	000025		
000031	00 0100 03	JU 20	
000032	000020		

Example Address = 65_8

DAB/SAB 5 4 3 2 1 Ø

1 1 0 1 0 1

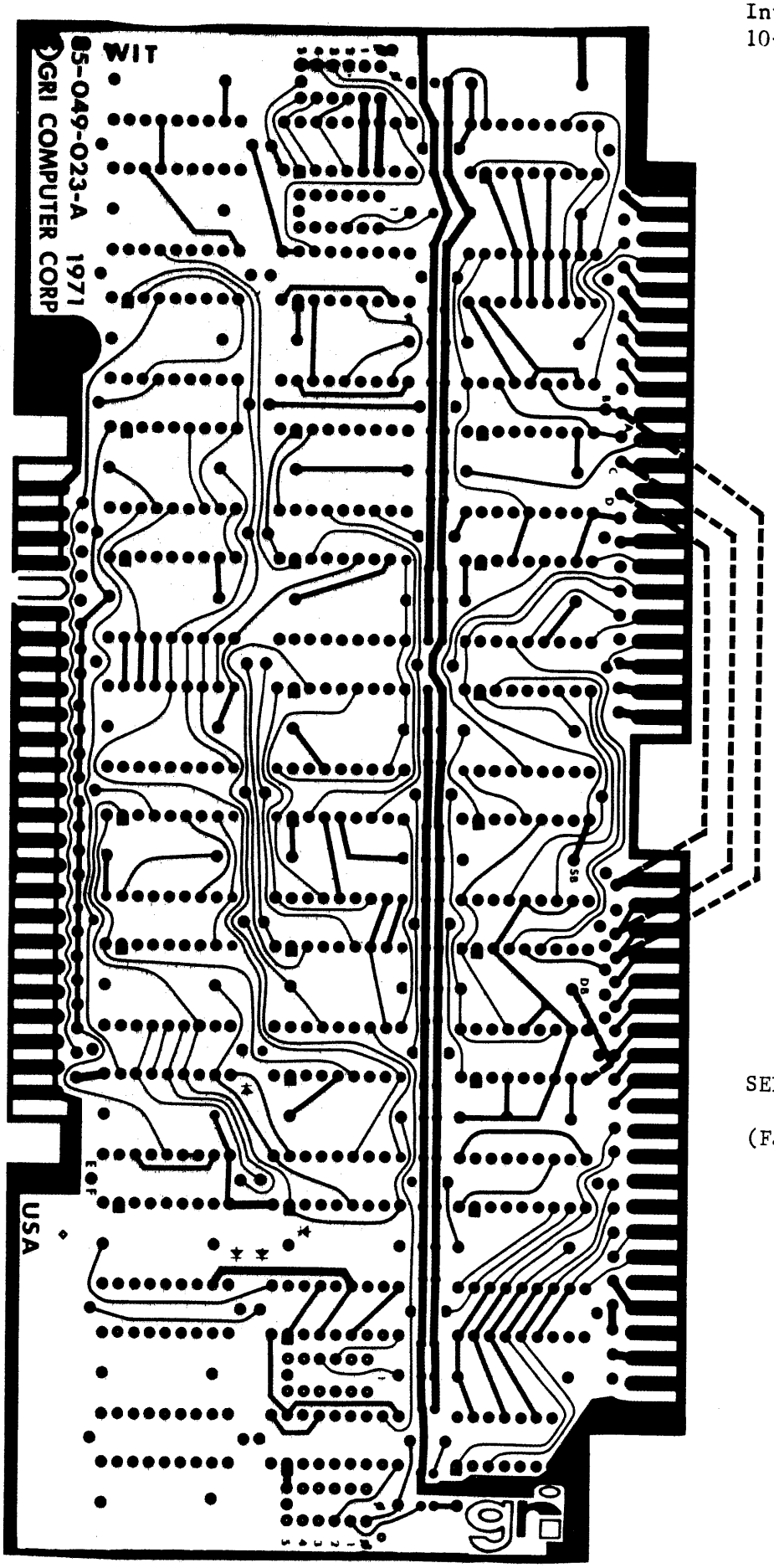


Al-destination address (DAB)
Ll-source address (SAB)

VARIABLE ADDRESS SELECTION

FIGURE 1

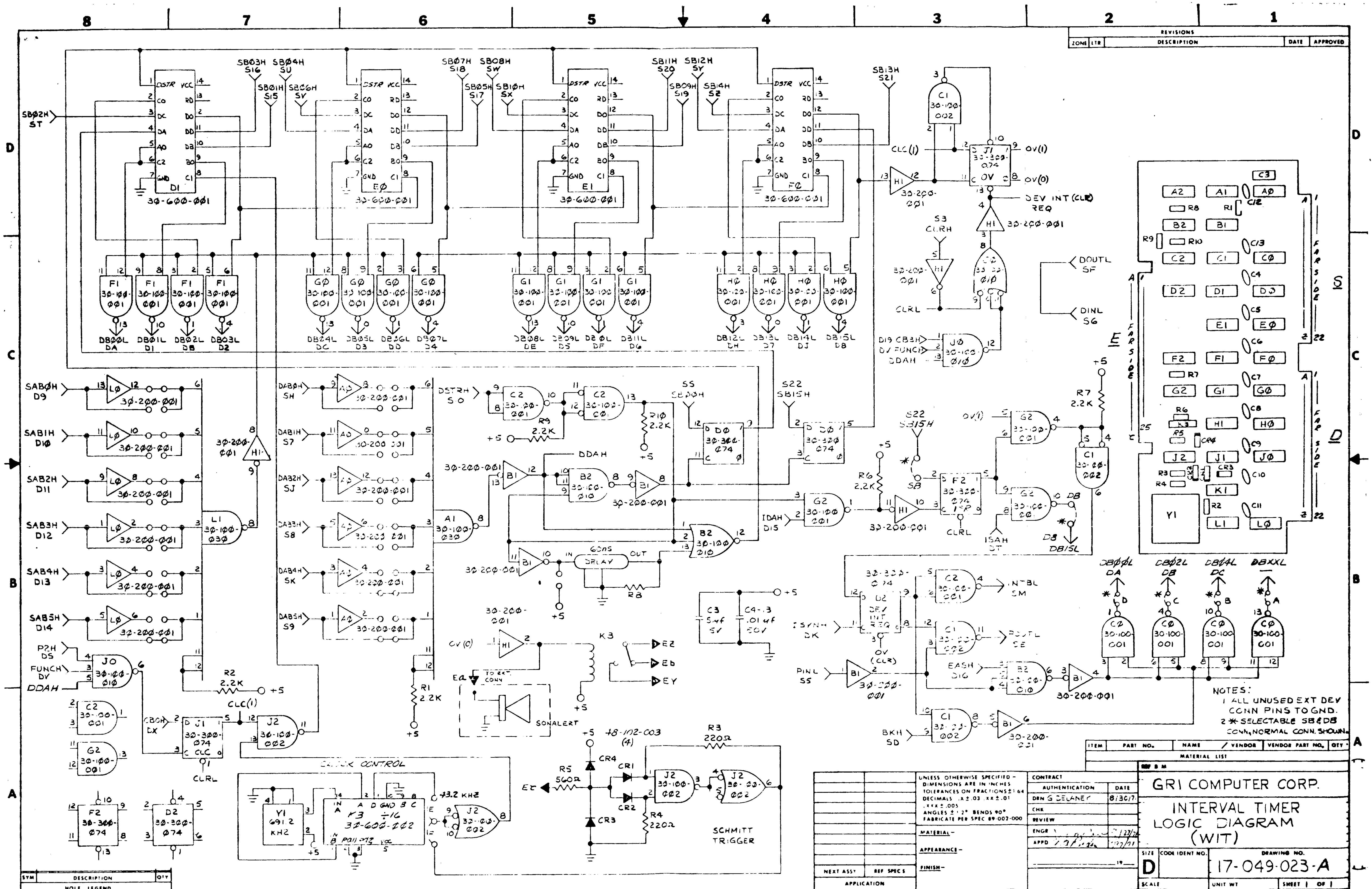
Interval Timer
10-049-023A



SELECTABLE JUMPERS

(Factory settings shown)

FIGURE 2


GRI COMPUTER CORP.
INTERVAL TIMER
LOGIC DIAGRAM
(WIT)
17-049-023-A
SIZE D
SHEET 1 OF 1
DRN G DELANEY 8/30/71
NOTES:
1 ALL UNUSED EXT DEV CONN PINS TO GND.
2 ✱ SELECTABLE SB & DB CONN, NORMAL CONN. SHOWN.
UNLESS OTHERWISE SPECIFIED — DIMENSIONS ARE IN INCHES
CLOCK CONTROL
SCHMITT TRIGGER
SONALERT
60NS DELAY
MATERIAL LIST
REVISIONS
HOLE LEGEND
NEXT ASSY
APPLICATION

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