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HARDWARE REFERENCE MANUAL

MICROCOMPUTER
SYSTEMS

GenRad Corp.
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HARDWARE REFERENCE MANUAL

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futuredata

5730 Buckingham Parkway
Culver City, CA 90230

TABLE OF CONTENTS

Section

TABLE OF CONTENTS

Section

TABLE OF CONTENTS (Concluded)

Section 1

Introduction

1.0 Introduction

This manual contains reference material for the AMDS-FD and AMDS-AFD Development System Hardware. An equivalent manual "Programming the AMDS", is available for the System Software.

Section 2

System Bus

2.0 GenRad/futuredata System Bus

All communication between system modules takes place throuth the system bus. This bus is wired in parallel to all of the card edge connectors. The edge connector pins, therefore, have the same signal at all card slots. This feature allows any system module to plug into any card slot, which provides flexibility and eliminates the possibility of error in installing cards. The three power supplies, +5, +12 and -12, are distributed in parallel to all edge connectors.

The signal lines of the bus can be divided into four categories: (1) address lines, (2) data lines, (3) data control lines, and (4) system status and control lines.

2.1 Address Lines

The system bus contains 24 address lines. For 8 bit processors, such as the 8080, only the lower 16 lines are used.

2.2 Data Lines

The system provides for a data bus up to 16 bits wide. These lines are bidirectional and accommodate data going to and coming from the CPU. For 8 bit processors the low order 8 lines of this bus are used.

2.3 Data Control Lines

The data control lines provide information about the signals on the address and data buses, and give timing information which indicates when the other signals are valid.

In particular, the control lines, MEM' and IO' indicate whether the address lines contain a memory address, or I/O device address. R/W' indicates a read (input) or write (output) cycle. Read and write strobes synchronize transfers on the data bus. The read strobe line (RD') indicates when the data from the memory or an input device should be enabled on the data bus. The write strobe line (WR') indicates when valid data is available on the data bus for the memory or an output device. A ready line (RDY), and delay lines (MEMD1', MEMD2') are provided to synchronize the CPU to slower memory. These lines delay the CPU for accessing 1.0 and 1.5 us memories respectively.

2.4 System Control and Status Lines

System restart and interrupt are controlled by the reset request line (RESRQ') the bootstrap request line (BOOTRQ') are the eight interrupt lines (INTRQ0' to INTRQ7'). The reset causes a master reset of the CPU and sends out a system reset signal (RES') which is used to clear logic on other modules. The bootstrap line also causes a system reset and then invokes the bootstrap loader.

Each of the interrupt lines cause a vectored interrupt, when the CPU'S interrupt system is enabled. The eight interrupt lines are priority encoded with line 0 having the highest priority and 7 having the lowest. The interrupt lines cause vectoring to the respective eight restart instruction (RST) addresses.

Direct memory acdess is controlled by the DMARQ' line. When the CPU suspends execution and relinquishes the address, data, and data control lines, the DMAEN' signal provides acknowledgement.

Two status lines, one for interrupts enabled (INTE) and one for halt (HLT') are provided. These lines are used for the operator status displays.

2.5 Bus Signal Description

A summary of the function of each bus signal follows. In this summary, inverted signals denoted by a prime (') are normally at a high logic level, and are taken to a low logic level when active. True signals are normally in the low logic state, and are active when high.

ADDR0-ADDR23	23 Bit Address Bus. ADDR0 is the low order bit.
DATA0-DATA15	16 Bit Bidirectional Data Bus. All 8 bit versions of the system use only the low order 8 bits (DATA0-DATA7). DATA0 is the lower order bit.
SEL0'-SEL7'	Bank Select. The high-order three address bits (ADDR13, 14 and 15) are decoded into 8 select lines to simplify decoding of memory and I/O addresses.
BOOTSEL'	Bootstrap Select. Selects the bootstrap PROM.
MEM'	Memory Cycle. Address, data, and data control lines are valid for a memory cycle during MEM'.

IO'	Input/Output Cycle. Address, data and data control lines are valid for an Input/Ouput cycle during IO'.
R/W'	Read/Not Write. Read or input cycle when high. Write or output cycle when low.
DEN'	Data Enable. Data is transferred on the data bus during DEN'. DEN' is the "OR" combination of RD' and WR'.
RD'	Read Enable. Data is received by the CPU during RD'. Memory and input devices are enabled to drive the data bus during RD'.
WR'	Write Enable. Data is transmitted by the CPU during WR'. Memory and output devices accept data from the data bus during WR'.
INTE	Interrupt Enable Status. Indicates that CPU interrupts are enabled.
INTRQ0'-INTRQ7'	Interrupt Requests. Priority encoded interrupt request lines. INTRQ0' has the highest priority and vectors the program to location 0000. INTRQ7' has the lowest priority and vectors the program to 0038.
DMARQ'	Direct Memory Access Request.
DMAEN'	Direct Memory Access Acknowledgement.
DMAD151'	Disable Direct Memory Access. Shuts down the CRT refresh. Memory refresh is user's responsibility.
RDY	Ready. CPU runs without delay when RDY line is high.
HLT'	Halt Status. Indicates that the processor is in the halt state.
MEMD1'	Memory Delay 1. Generates a 1 us delay for slower memory. Delay can be enabled during entire MEM' cycle.

MEMD2'	Memory Delay 2. Generates a 1.5 us delay for slower memory. Delay can be enabled during entire MEM' cycle.
RESRQ'	System Reset Request. Master reset is generated, synchronized to memory access so that memory cycles are not affected.
BOOTRQ'	Bootstrap Request. Activates bootstrap ROM after LOAD.
RES'	System Reset. System reset is generated in response to RESRQ' or BOOTREQ'. It is used to initialize system status registers and flags.
CLK	System Clock. The system clock is 1, 2 or 4 MHz depending on processor.

NOTES:

1. The following lines are tri-state, have resistor pullups, and are in the high-impedance state during DMAEN':

ADDR0-ADDR23
DATA0-DATA7
MEM'
IO'
R/W'
DEN'
RD'
WR'

2. The following lines are open collector and have resistor pullups so that they can be wire OR-ed :

INTRQ0'-INTRQ7'
DMARQ'
RDY

3. The following lines are standard TTL :

SEL0'-SEL7'
BOOTSEL'
INTE
DMAEN'
HLT'
RES'
CLK

Table 2.0 GenRad/futuredata Bus Pin Assignments

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	34	BOOTSEL'	68	DMARQ'
2	GND	35	MEM'	69	DMAEN'
3	+5v	36	IO'	70	DMADI51'
4	+5v	37	R/W'	71	WR
5	+12v	38	M1'	72	RDY
6	+12v	39	WAIT(8080 ONLY)	73	MEMD1' (8080 ONLY)
7	-12v	40	DATA0	74	MEMD2' (8080 ONLY)
8	-12v	41	DATA1	75	-
9	HLT'	42	DATA2	76	DBIN (8080 ONLY)
10	ADDR0	43	DATA3	77	SYNC (8080 ONLY)
11	ADDR1	44	DATA4	78	CRTRQ'
12	ADDR2	45	DATA5	79	CRTEN'
13	ADDR3	46	DATA6	80	-
14	ADDR4	47	DATA7	81	ADDR16
15	ADDR5	48	DATA8	82	ADDR17
16	ADDR6	49	DATA9	83	ADDR18
17	ADDR7	50	DATA10	84	ADDR19
18	ADDR8	51	DATA11	85	ADDR20
19	ADDR9	52	DATA12	86	ADDR21
20	ADDR10	53	DATA13	87	ADDR22
21	ADDR11	54	DATA14	88	ADDR23
22	ADDR12	55	DATA15	89	MEM H'
23	ADDR13	56	DEN'	90	-
24	ADDR14	57	RD'	91	RESRQ'
25	ADDR15	58	WR'	92	BOOTRQ'
26	SEL0'	59	INTE	93	RES'
27	SEL1'	60	INTRQ0'	94	CLK
28	SEL2'	61	INTRQ1'	95	-
29	SEL3'	62	INTRQ2'	96	HLDA' (8080), ¢2 (6800 ONLY)
30	SEL4'	63	INTRQ3'	97	+5v
31	SEL5'	64	INTRQ4'	98	+5v
32	SEL6'	65	INTRQ5'	99	GND
33	SEL7'	66	INTRQ6'	100	GND
		67	INTRQ7'		

Section 3

CRT Display Units

3.0 Introduction

Two CRT display units are currently being used inter-changeably in the Advanced Microprocessor Development Systems. Each CRT unit has a name-plate which will indicate which manufacturer produced it.

The manuals supplied by the manufacturers are reproduced in this section:

MOTOROLA

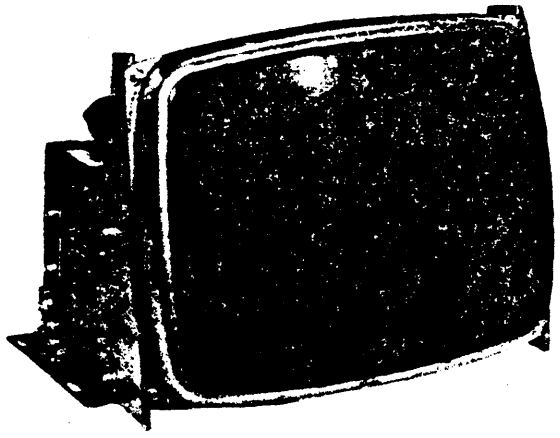
SERVICE MANUAL
VP27

MODELS*

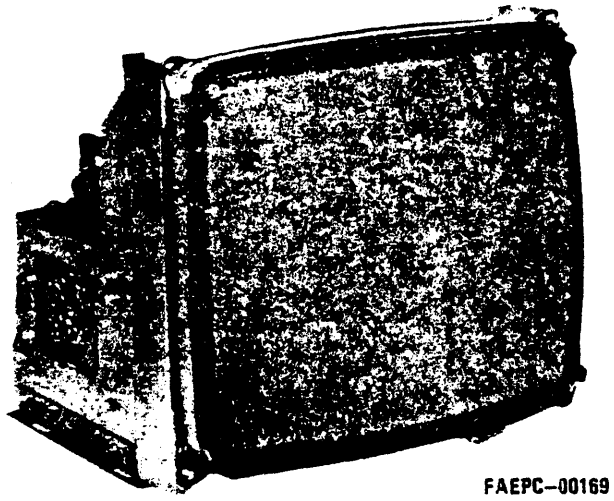
M3000-140, 240, 340
M3003-140, 240, 340
M4000-140, 240, 440
M4003-140, 240, 440

*INCLUDES StepScan™ MOTOROLA

TABLE OF CONTENTS



Model M3000/M3003 (12" – CRT)



FAEPC-00169

Model M4000/M4003 (15" – CRT)

CAUTION
NO WORK SHOULD BE ATTEMPTED ON ANY EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

MOTOROLA INC.
Data Products
CAROL STREAM, ILLINOIS 60187

2/78

PART NO. 68P25253A57
PRINTED IN U.S.A.
PRICE $2.00

SAFETY WARNING

CAUTION: NO WORK SHOULD BE ATTEMPTED ON AN EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

1. SAFETY PROCEDURES should be developed by habit so that when the technician is rushed with repair work, he automatically takes precautions.

2. A GOOD PRACTICE, when working on any unit, is to first ground the chassis and to use only one hand when testing circuitry. This will avoid the possibility of carelessly putting one hand on chassis or ground and the other on an electrical connection which could cause a severe electrical shock.

3. Extreme care should be used in HANDLING THE PICTURE TUBE as rough handling may cause it to implode due to atmospheric pressure (14.7 lbs. per sq. in.). Do not nick or scratch glass or subject it to any undue pressure in removal or installation. When handling, safety goggles and heavy gloves should be worn for protection. Discharge picture tube by shorting the anode connection to chassis ground (not cabinet or other mounting parts). When discharging, go from ground to anode or use a well insulated piece of wire. When servicing or repairing the monitor, if the cathode ray tube is replaced by a type of tube other than that specified under the Motorola Part Number as original equipment in this Service Manual, then avoid prolonged exposure at close range to unshielded areas of the cathode ray tube. Possible danger of personal injury from unnecessary exposure to X-ray radiation may result.

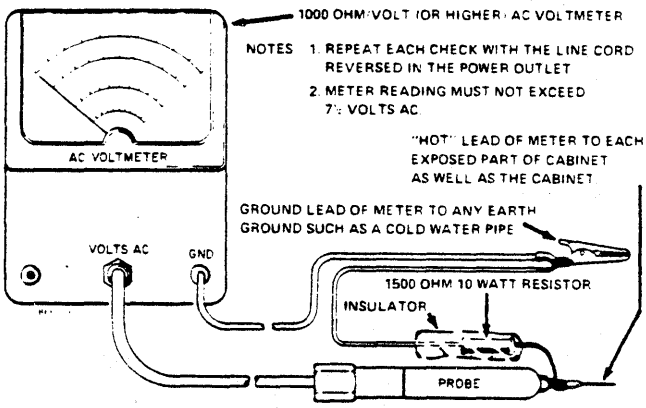
4. An ISOLATION TRANSFORMER should always be used during the servicing of a unit whose chassis is connected to one side of the power line. Use a transformer of adequate power rating as this protects the serviceman from accidents resulting in personal injury from electrical shocks. It will also protect the chassis and its components from being damaged by accidental shorts of the circuitry that may be inadvertently introduced during the service operation.

5. Always REPLACE PROTECTIVE DEVICES, such as fishpaper, isolation resistors and capacitors and shields after working on the unit.

6. If the HIGH VOLTAGE is adjustable, it should always be ADJUSTED to the level recommended by the manufacturer. If the voltage is increased above the normal setting, exposure to unnecessary X-ray radiation could result. High voltage can accurately be measured with a high voltage meter connected from the anode lead to chassis.

7. BEFORE RETURNING A SERVICED UNIT, the service technician must thoroughly test the unit to be certain that it is completely safe to operate without danger of electrical shock. DO NOT USE A LINE ISOLATION TRANSFORMER WHEN MAKING THIS TEST.

In addition to practicing the basic and fundamental electrical safety rules, the following test, which is related to the minimum safety requirements of the Underwriters Laboratories should be performed by the service technician before any unit which has been serviced is returned.



Voltmeter Hook-up for Safety Check

A 1000 ohm per volt AC voltmeter is prepared by shunting it with a 1500 ohm, 10 watt resistor. The safety test is made by contacting one meter probe to any portion of the unit exposed to the operator such as the cabinet trim, hardware, controls, knobs, etc., while the other probe is held in contact with a good "earth" ground such as a cold water pipe.

The AC voltage indicated by the meter may not exceed 7½ volts. A reading exceeding 7½ volts indicates that a potentially dangerous leakage path exists between the exposed portion of the unit and "earth" ground. Such a unit represents a potentially serious shock hazard to the operator.

The above test should be repeated with the power plug reversed, when applicable.

NEVER RETURN A MONITOR which does not pass the safety test until the fault has been located and corrected.

ELECTRICAL SPECIFICATIONS *

	MODEL M3000/M3003	MODEL M4000/M4003
PICTURE TUBE:	12" measured diagonally (305 mm); 74 sq. in. viewing area (477 sq. cm); 110° deflection angle; integral implosion protection; M3000/3003–140: P4 phosphor without anti-reflective faceplate M3000/3003–240: P4 phosphor with anti-reflective faceplate M3000/3003–340: P31 phosphor without anti-reflective faceplate	15" measured diagonally (381 mm); 100 sq. in. viewing area (645 sq. cm); 110° deflection angle; integral implosion protection; M4000/4003–140: P4 phosphor without anti-reflective faceplate M4000/4003–240: P4 phosphor with anti-reflective faceplate M4000/4003–440: P31 phosphor with anti-reflective faceplate
POWER INPUT:	115/230V AC, 60 watts (nominal), or 70V DC	
FUSES:	0.8 Amp Slo-Blo	0.8 Amp Slo-Blo
LOW VOLTAGE POWER SUPPLY:	Electronically regulated over AC inputs from 107V to 135V, or 214V to 270V	
INPUT SIGNALS:	TTL SEPARATE HORIZONTAL, VERTICAL, VIDEO: 2.5V to 5.0V P-P, video drive, sync positive at input (input impedance: 75 ohms to 250 ohms video termination, > 2K ohms vertical and horizontal)	
PULSE RISE TIME (TYPICAL):	30V rise in less than 20 nSec	
RESOLUTION (TYPICAL):	800 lines center, 600 lines corners	
VIDEO RESPONSE (TYPICAL):	Within –3 dB, 10 Hz to 22 MHz	
LINEARITY:	Within 2% as measured with standard EIA ball chart and dot pattern	
HIGH VOLTAGE:	14kV nominal at 20 uAmp beam current	17kV nominal at 20 uAmp beam current
HORIZONTAL RETRACE TIME:	11.0 uSec maximum at 15.72 kHz – M3000/M4000 Models 11.0 uSec maximum at 18.72 kHz – M3003/M4003 Models	
SCANNING FREQUENCY:	Horizontal: 15.72 kHz ± 500 Hz; Vertical: 50/60 Hz – M3000/M4000 Models Horizontal: 18.72 kHz ± 500 Hz; Vertical: 50/60 Hz – M3003/M4003 Models	
ENVIRONMENT:	Operating temperature: 0°C to 50°C Storage temperature: –40°C to +65°C Operating altitude: 10,000 feet maximum (3048 meters) Designed to comply with applicable DHEW rules on X-Radiation Designed to enable listing under UL Specification 478	
TYPICAL DIMENSIONS:	9.12" H, 11.40" W, 8.84" D (232 x 290 x 225 mm)	10.94" H, 12.84" W, 10.22" D (278 x 326 x 260 mm)

* Specifications and descriptions subject to change without notice.

GENERAL INFORMATION

The monitors described herein are fully transistorized (except CRT) and applicable for displaying alphanumeric characters. The M3000/M3003 series monitors use a 12-inch CRT and the M4000/M4003 series monitors use a 15-inch CRT. All monitors utilize a non-composite video signal with separate TTL horizontal and vertical sync pulses. (See Schematic diagram.)

The CRT's employed are of the magnetic deflection type with integral implosion protection. An operating voltage of +70 volts DC is required from the regulated power supply for both models. A universal power transformer permits operating the monitor from either 115 or 230 volts AC, 50/60 Hz.

Input and output connections for the monitor are made through a 10-pin edge or header connector on the vertical/video circuit card. Inputs consist of video, horizontal/vertical sync, and signal ground. One additional input, TTL level StepScan, is also connected to the monitor via the 10-pin edge connector. Output connections are provided for an optional remote brightness control.

Circuitry consists of two stages for video amplification, five stages for vertical sync and deflection processing, five stages for horizontal sync and deflection processing, and a regulated +70 volt power supply. Both models also have dynamic focusing and StepScan amplifier. (See Schematic diagram.)

Three etched circuit cards are utilized, containing the vertical/video circuit, horizontal circuit, and power supply circuit. An optional low voltage logic power supply is available when a remote power source is required for logic interface circuitry. Components are mounted on the top of the circuit cards and plating copper foil on the bottom. Schematic reference numbers are printed on the top and bottom of each circuit card to aid in the location and identification of components for servicing. All standard operating/adjustment controls are mounted in a convenient manner on the three circuit cards. Refer to Motorola Service Manual VP20, Part No. 68P25253A40 for complete service information on the low voltage logic power supplies.

SERVICE NOTES

CIRCUIT TRACING

Component reference numbers are printed on the top and bottom of the three circuit cards to facilitate circuit tracing. In addition, control names and circuit card terminal numbers are also shown and referenced on the schematic diagram in this manual.

Transistor elements are identified as follows:

E – emitter, B – base, and C – collector.

COMPONENT REMOVAL

Removing components from an etched circuit card is facilitated by the fact that the circuitry (copper foil) appears on one side of the circuit card only and the component leads are inserted straight through the holes and are not bent or crimped.

It is recommended that a solder extracting gun be used to aid in component removal. An iron with a temperature controlled heating element would be desirable since it would reduce the possibility of damaging the circuit card foil due to over-heating.

The nozzle of the solder extracting gun is inserted directly over the component lead and when sufficiently heated, the solder is drawn away leaving the lead free from the copper foil. This method is particularly suitable in removing multi-terminal components.

When replacing "plug-in" transistors, please observe the following precautions:

1. The transistor sockets are not "captive", which means that the transistor mounting screws also secure the socket. When installing the transistor, the socket must be held in its proper position.

2. When replacing a plug-in transistor, silicone grease (Motorola Part No. 11M490487) should be applied evenly to the top of the heat sink and bottom of the transistor. In addition, be sure a mica insulator is positioned properly between the transistor and heat sink.

3. The transistor mounting screws must be tight before applying power to the monitor. This insures proper cooling and electrical connections. NON-COMPLIANCE WITH THESE INSTRUCTIONS CAN RESULT IN FAILURE OF THE TRANSISTOR AND/OR ITS RELATED COMPONENTS.

NOTE

Use caution when tightening transistor mounting screws. If the screw threads are stripped by excessive pressure, a poor electrical and mechanical connection will result.

CRT REPLACEMENT

Use extreme care in handling the CRT as rough handling may cause it to implode due to high vacuum pressure. Do not nick or scratch glass or subject it to any undue pressure in removal or installation. Use goggles and heavy gloves for protection. In addition, be sure to disconnect the monitor from all external voltage sources.

1. Discharge CRT by shorting 2nd anode to ground; then remove the CRT socket, deflection yoke and 2nd anode lead.

2. Remove CRT from the front of the chassis by loosening and removing four screws; one in each corner of the CRT.

REGULATOR ADJUSTMENT

NOTE

Misadjustment of the low voltage regulator, or the horizontal oscillator may result in damage to the horizontal output transistor or pulse limiter diode. The following procedure is recommended to insure reliable operation.

1. Connect the monitor to an AC line supply; then adjust supply to 120 volts (240 volts in some applications).

2. Apply test signal to proper input. Signal should be of same amplitude and sync rate as when monitor is in service.

3. Adjust HOR. SET coil L50 (on the horizontal circuit card) until display is stable.

4. Connect a DC digital voltmeter or equivalent precision voltmeter to the emitter of the regulator output transistor, Q150 (or any +70 volt test point on the power supply circuit card).

5. Adjust the 70V ADJUST. control, R158, on the power supply circuit card for an output of +70 volts. DO NOT rotate the control through its entire range; damage to the monitor may result.

6. When adjustment is complete, the AC line supply can be varied between 105 and 130 volts AC to check for proper regulator operation. With the regulator operating properly, changes in display size should be negligible.

HORIZONTAL HOLD/OSCILLATOR ADJUSTMENT

Adjust the core of HOR. SET coil L50 until the horizontal blanking lines are vertical, or the CRT display is stable (synced).

DYNAMIC FOCUS ADJUSTMENT

The DYNAMIC FOCUS coil is factory set and should not normally require further adjustment. However, if it becomes necessary, use Procedure No. 1 for touching up the overall focus. Procedure No. 2 is provided if the CRT (V1) and/or DYNAMIC FOCUS coil (L52) is replaced in the field.

PROCEDURE NO. 1

1. Adjust FOCUS control R70 (on horizontal circuit card) for best focus in the center of the CRT.

2. Adjust DYNAMIC FOCUS coil L52 for best edge focus.

3. Alternate between adjusting R70 and L52 until overall CRT focus is optimized.

PROCEDURE NO. 2

1. Connect an oscilloscope (DC coupled) between the junction of R71 and C63 (on horizontal circuit card) and signal ground.

CAUTION

High voltage is present.

2. Adjust the oscilloscope controls until one cycle of the horizontal rate sinewave appears as shown in Figure 1.

3. Adjust the DYNAMIC FOCUS coil, L52 for a minimum sinewave amplitude of not more than 125 volts P-P.

NOTE

Be sure that the one cycle appearing on the oscilloscope is not a harmonic of the horizontal rate sinewave. This may occur if the DYNAMIC FOCUS coil, L52, is misadjusted to the extent that L52 will produce the second harmonic. The coil must be adjusted to produce the minimum amplitude of the fundamental frequency only. Confirm the preceding by momentarily connecting the oscilloscope across the primary of T50. Only one cycle or pulse should appear.

4. Observe the center of the CRT display and adjust the FOCUS control, R70, for optimum focus; then record the DC voltage (represented as amplitude "A" in Figure 1) between the DC 0 volt reference and the negative peak of the sinewave.

5. Observe the edges of the CRT display and adjust the FOCUS control, R70, for optimum focus; then record the DC voltage (represented as amplitude "B" in Figure 1) between the DC 0 volt reference and the positive peak of the sinewave .

6. Subtract the negative peak voltage from the positive peak voltage. The difference becomes the voltage value to which the DYNAMIC FOCUS coil, L52, must be adjusted.

7. While observing the sinewave, adjust the DYNAMIC FOCUS coil, L52, until amplitude "C" (see Figure 1) equals the difference voltage value determined in step 6.

8. While observing the oscilloscope, readjust the FOCUS control, R70, until the negative peak of the sinewave is positioned above the DC 0 volt reference line equal to the voltage value recorded in step 4.

Amplitude "A" – Represents adjusting FOCUS control, R70, for best CRT center FOCUS.

Amplitude "B" – Represents adjusting FOCUS control, R70, for best CRT edge FOCUS.

Amplitude "C" – Represents adjusting DYNAMIC FOCUS coil, L52, for final P-P setting that is equal to difference between amplitude "A" and "B".

NOTE: After amplitude "C" is adjusted, amplitude "A" must be reset to the original voltage value that provided best CRT center FOCUS.

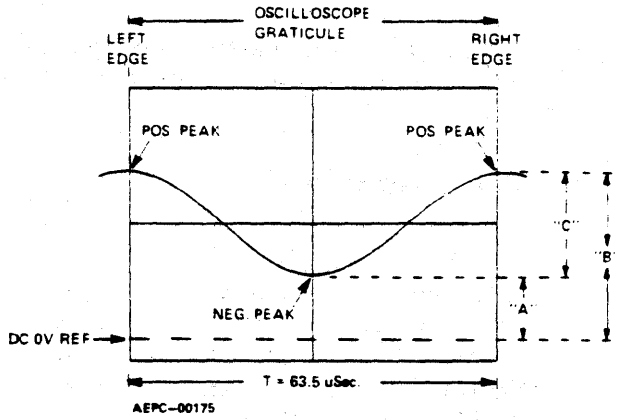
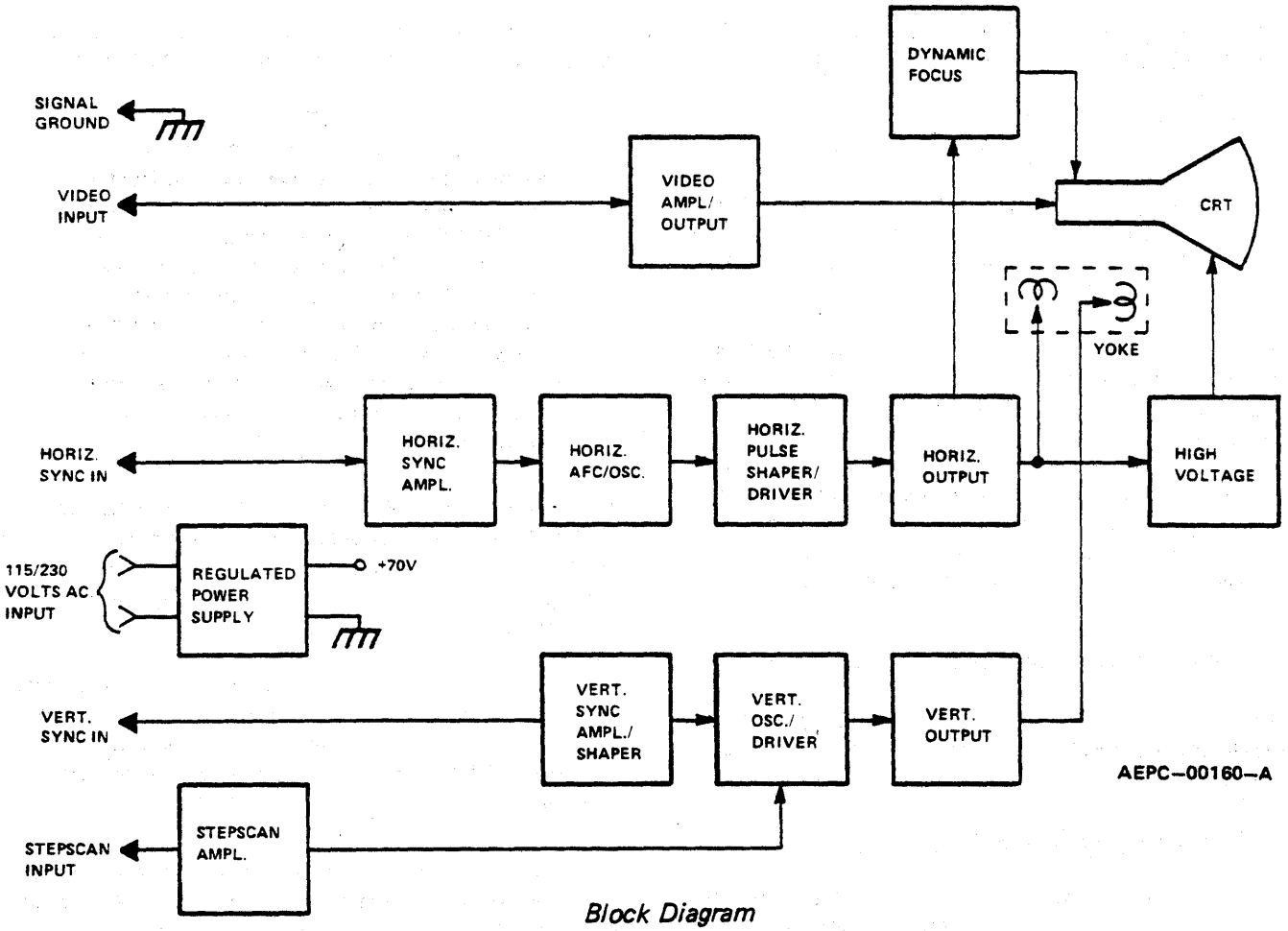


Figure 1. Adjusting Dynamic Focus with an Oscilloscope



Block Diagram

THEORY OF OPERATION

POWER SUPPLY

(Refer to Figure 2.)

The power supply is a transformer operated, full wave, regulated series pass circuit that maintains a constant output voltage with line input variations of ±12.5%. Depending on how connector S2 is wired, operation from 115 or 230 volts, 50/60 Hz is possible. Integrated circuit IC150 is the reference amplifier, transistor Q152 is a regulator buffer, transistor Q151 is the regulated output driver, and Q150 is the series pass transistor.

The output voltage, +70V, appears at the emitter of Q150. This voltage is divided between R157, R158 and R159. The voltage appearing on the arm of potentiometer R158 (70V ADJ. control) is the reference input to the non-inverting input of reference amplifier IC150.

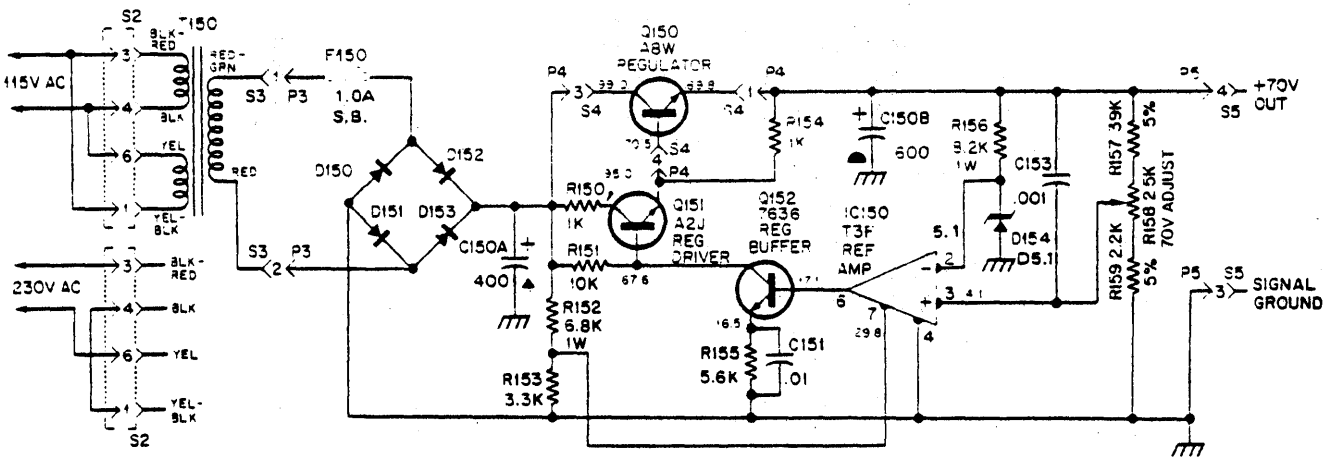


Figure 2. Power Supply Circuit

A temperature compensated zener diode, D154, establishes a fixed reference voltage at the inverting input to IC150. Resistor R156 provides a bias current for D154, which establishes its operating point. Capacitor C153 is a high frequency filter. Operating voltage for IC150 is derived from a voltage divider consisting of R152 and R153. Components R155 and C151 set the voltage gain of Q152.

An increase in output voltage will result in an increase of voltage at the base of Q152 via the non-inverting input of IC150. The change in base voltage will turn Q152 on harder, reducing its collector voltage. This reduces the forward bias to Q151, which results in less emitter current for Q150. With Q150 conducting less, the output voltage will be lowered.

VIDEO AMPLIFIER

(Refer to Figure 3.)

The linear video amplifier consists of two stages, Q100 and Q101, which are connected in a cascode configuration. This common emitter-common base arrangement greatly reduces the effect of Miller capacity (when compared to a conventional single transistor video amplifier/output stage).

A TTL compatible non-composite video signal, approximately 4.0 volts P-P, is DC coupled to the base of Q100 via R100. Resistor R112 provides proper termination for the high frequency input video signal. Capacitor C100 provides high frequency compensation to maintain a flat response when Q100 and Q101 conduct.

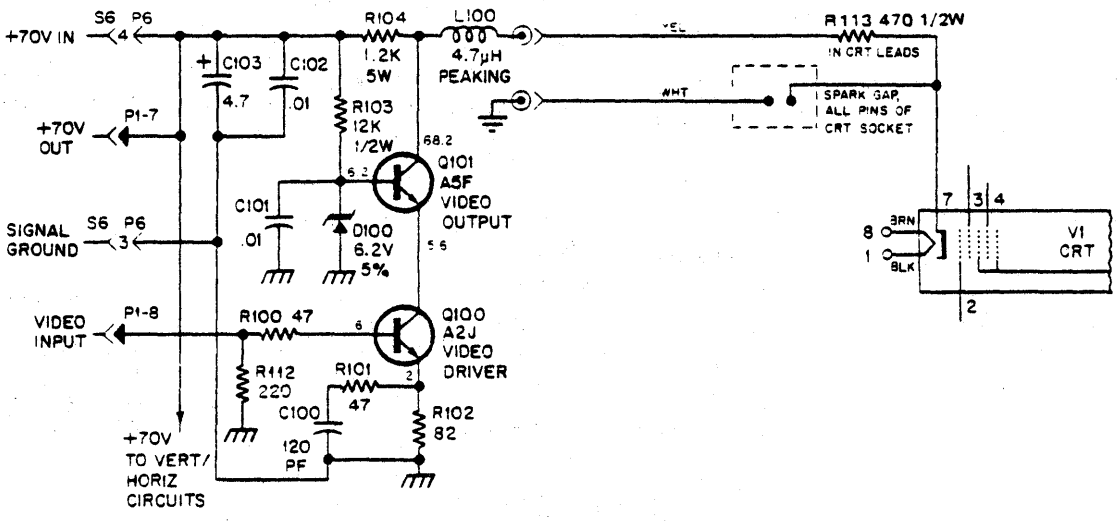


Figure 3. Video Amplifier Circuit

During no-signal conditions, Q100 is off. Transistor Q101, however, is forward biased by the 6.2 volts on its base, which is established by zener diode D100. When a video signal is applied to the base of Q100, it conducts, which causes forward biased Q101 to conduct. The resultant output is developed across R104 at the collector of Q101; then DC coupled to the cathode of V1 (CRT) via peaking coil L100 and R113. Resistor R113 isolates Q101 from transients that may occur as a result of CRT arcing. Capacitor C101 shunts to ground high frequency video that may appear on the base of Q101. Peaking coil L100 boosts the high frequencies of the video signal. Capacitor C103 provides additional filtering of the +70V, while C102 is a high frequency AC bypass capacitor.

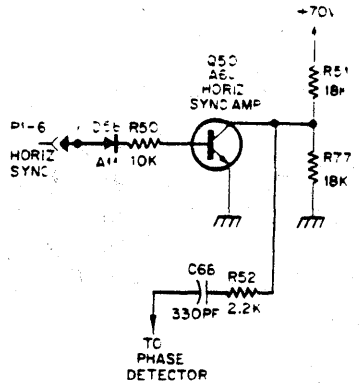


Figure 4. Horizontal Sync Amplifier Circuit

HORIZONTAL SYNC AMPLIFIER

(Refer to Figure 4.)

The horizontal sync amplifier consists of one stage, Q50, which operates as a switch. During a no-signal condition, Q50 is off. When a positive-going horizontal sync signal, approximately 4.0 volts P-P, is applied (DC coupled) to the base of Q50, it goes into saturation. The amplified output is developed across load resistor R51, approximately 35V, which forms a voltage divider with R77. The negative-going horizontal sync pulses are AC coupled to the phase detector circuit via the R-C network consisting of R52 and C68, a high frequency pass filter.

PHASE DETECTOR

(Refer to Figure 5.)

The phase detector consists of two diodes (D50 and D51) in a keyed clamp circuit. Two inputs are required to generate the required output, one from the horizontal sync amplifier, Q50, and one from the horizontal output circuit, Q54. The required output must be of the proper polarity and amplitude to correct phase differences between the input horizontal sync pulses and the horizontal time base. The horizontal output (Q54) collector pulse is integrated into a sawtooth by R56 and C69. During horizontal sync time, diodes D50 and D51 conduct, which shorts C69 to ground. This effectively clamps the sawtooth on C69 to ground at sync time. If the horizontal time base is in phase with the sync (waveform A), the sync pulse will occur when the sawtooth is passing through its AC axis and the net charge on C69 will be zero (waveform B). If the horizontal time base is lagging the sync, the sawtooth on C69 will be clamped to ground at a point negative from the AC axis. This will result in a positive DC charge on C69 (waveform C). This is the correct polarity to cause the horizontal oscillator to speed up to correct the phase lag. Likewise, if the horizontal time base is leading the sync, the sawtooth on C69 will be clamped at a point positive from its AC axis. This results in a net negative charge on C69, which is the required polarity to slow the horizontal oscillator (waveform D). Components R55, C52, R58 and C53 comprise the phase detector filter. The bandpass of this filter is chosen to provide correction of horizontal oscillator phase without ringing or hunting. Capacitor C50 times the phase detector for correct centering of the picture on the raster.

HORIZONTAL OSCILLATOR

(Refer to Figure 5.)

The horizontal oscillator consists of Q51, which is employed as a modified type of Hartley oscillator. The

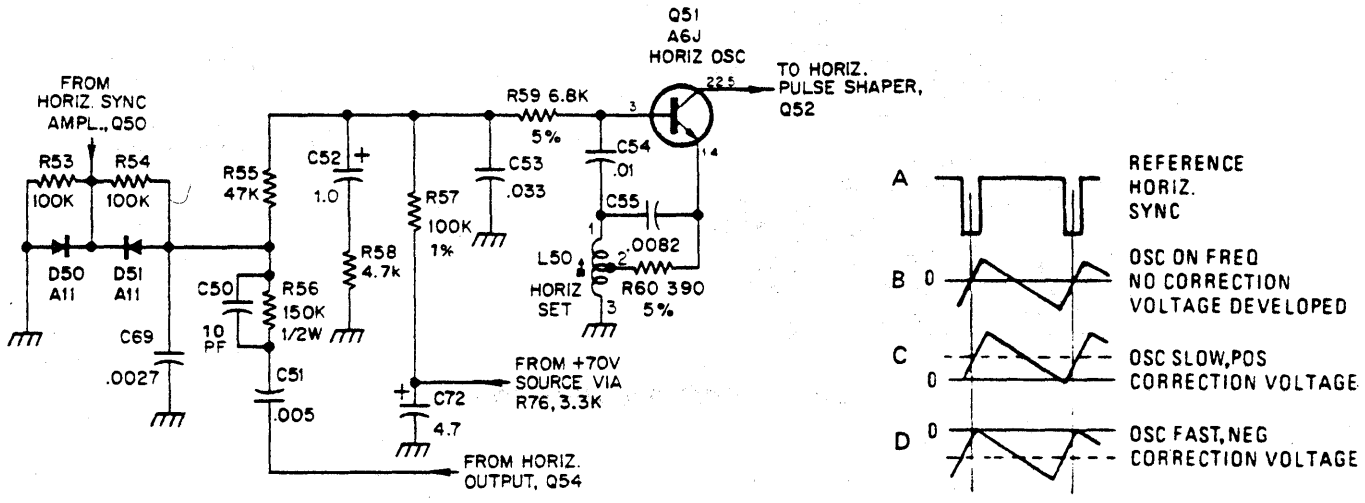


Figure 5. Phase Detector and Horizontal Oscillator Circuits

operating frequency of this oscillator is sensitive to its base input voltage. This permits control by the output of the phase detector. Resistor R57 provides DC bias to turn on Q51 and start the oscillator. The free-running horizontal frequency is adjusted with the HORIZ. SET coil, L50, which along with C54 are the frequency determining components. Capacitor C55 and resistor R60 are feedback components for the oscillator circuit.

HORIZONTAL PULSE SHAPER & DRIVER

(Refer to Figure 6.)

Transistor Q52 is a buffer stage between the horizontal oscillator and horizontal driver. It provides isolation for the horizontal oscillator as well as a low impedance drive for the horizontal driver. Components R62 and C56 form a time constant that shapes the oscillator output to the required duty cycle, approximately 50%, to drive the horizontal output circuitry. The horizontal driver stage, Q53, operates as a switch to drive the horizontal output transistor (Q54) through T50. Because of the low impedance drive and fast switching times furnished by Q52, very little power is dissipated in Q53. Components R66 and C57 provide damping to suppress ringing in the primary of T50 when Q53 goes into cutoff. (Reference Figure 8 – Resistor R68 provides current limiting for Q53 while C58 is an AC bypass capacitor.)

HORIZONTAL OUTPUT

(Refer to Figure 7.)

The secondary of T50 provides the required low drive impedance for Q54. Components R67 and C59 form a time constant for fast turn-off of the base of Q54. Once during each horizontal period, Q54 operates as a switch that connects the supply voltage across the parallel combination of the horizontal deflection yoke and the primary of the high

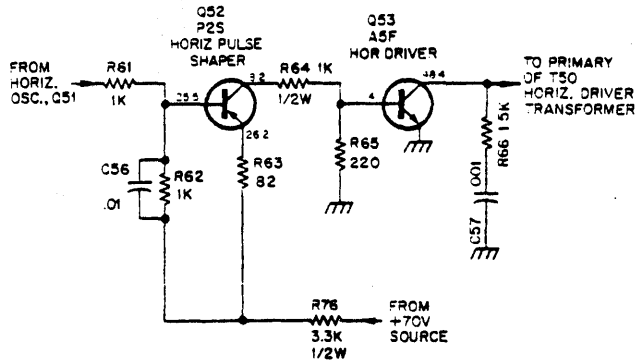


Figure 6. Horizontal Pulse Shaper and Driver Circuits

voltage transformer. The required sawtooth deflection current (through the horizontal yoke) is formed by the L-R time constant of the yoke and primary winding of the H.V. transformer, T51. The horizontal retrace pulse charges C62 through D54 to provide operating voltage for G2 of the CRT. Momentary transients at the collector of Q54, should they occur, are limited to the voltage on C62 since D54 will conduct if the collector voltage exceeds this value.

The damper diode, D53, conducts during the period between retrace and turn on of Q54. Capacitor C65 is the retrace tuning capacitor, while C61 blocks DC from the

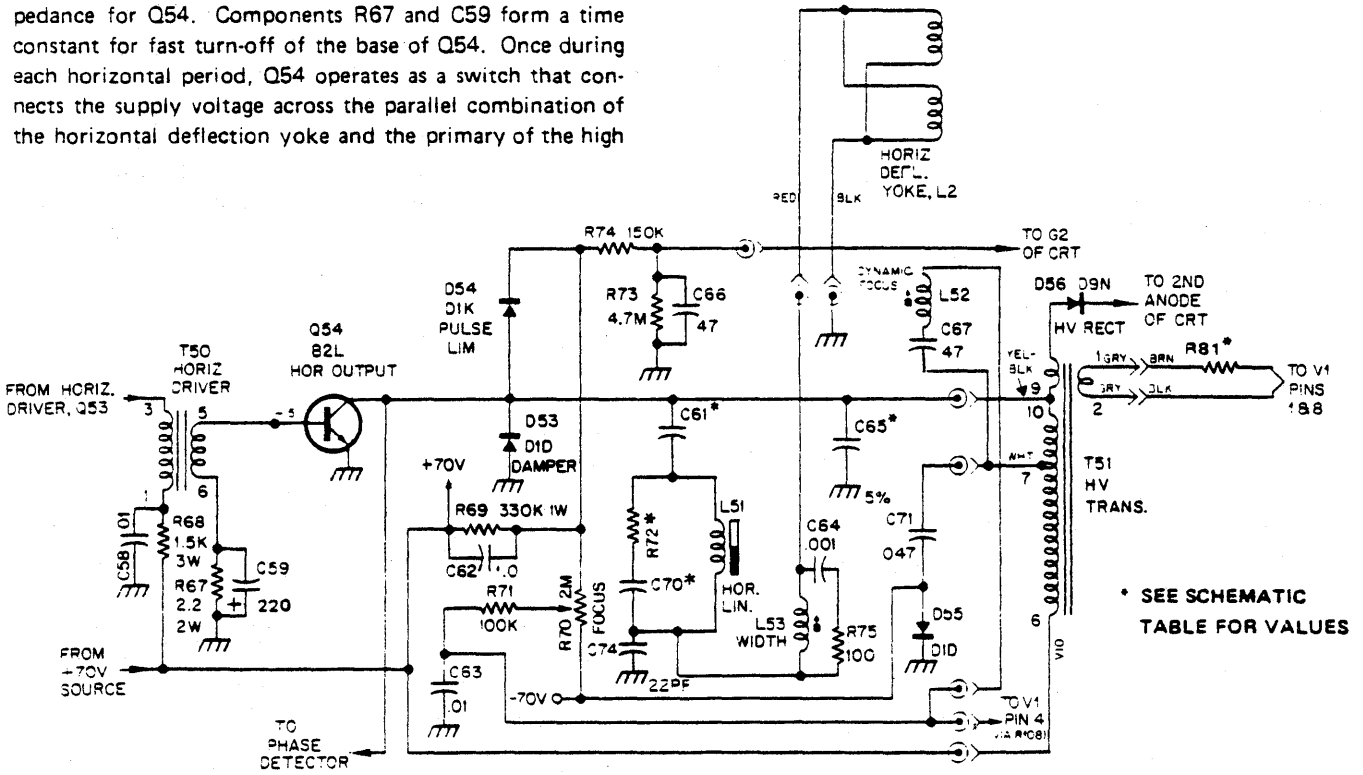


Figure 7. Horizontal Output Circuit

deflection yoke. Coil L51 is a magnetically biased linearity coil that shapes the deflection current for optimum trace linearity. Coil L53 is a series horiz. width control. Components R72 and C70, C64 and R75 are damping network components for the horizontal linearity (L51) and width (L53) controls. Capacitor C71 couples horizontal sync pulses from pin 7 of T51 to diode clamp D55, which maintains the −70V reference voltage.

DYNAMIC FOCUS

(Refer to Figure 8.)

Due to the geometry of a CRT, the electron beam travels a greater distance when deflected to a corner as compared to the distance traveled at the center of the CRT screen. As a result of these various distances traveled, optimum focus can be obtained at only one point. For general applications, an adequate adjustment can be realized by setting the focus while viewing some point mid-way between the center of the CRT screen and a corner, thus optimizing the overall screen focus. When an application requires a tighter specification, one of the simplest methods for improvement is to modulate the focus voltage at a horizontal sweep rate. Now optimum focus voltage is made variable on the horizontal axis of the CRT, which compensates for the beam travel along this axis.

The AC component focus voltage is developed by a series resonant circuit consisting of L52 and C63. This voltage is an 80V P-P horizontal rate pulse coupled from a tap on the horizontal output transformer, T51, via C67. The normal DC component of the G4 focus voltage is set by adjusting the FOCUS control, R70. When the DYNAMIC FOCUS coil, L52, is optimized for best edge focus, a sinusoidal voltage of approximately 200V P-P is developed across C63. This mixed AC and DC voltage results in a waveform of proper phase and amplitude, which is coupled through isolating resistor R108 to the CRT focus anode.

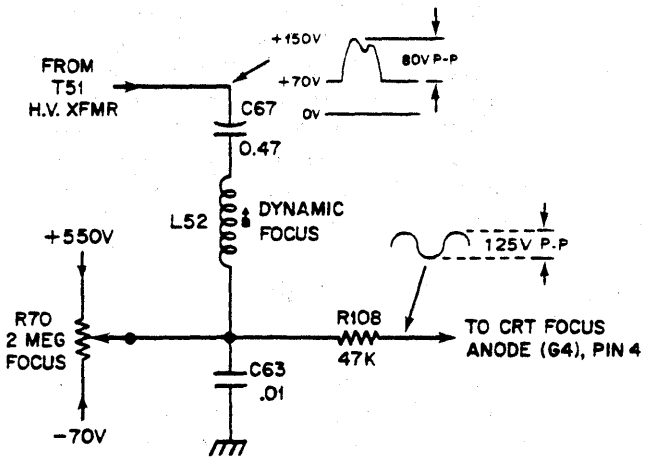


Figure 8. Simplified Dynamic Focus Circuit Diagram

VERTICAL SYNC AMPLIFIER

(Refer to Figure 9.)

The vertical sync amplifier consists of one stage, Q1, which operates as a switch. During no-signal conditions, Q1 is off. When a positive-going vertical sync signal, approximately 4.0 volts P-P, is applied (direct coupled) to the base, Q1 goes into saturation. The amplified output is developed across load resistor R3 to approximately 11 volts.

SYNC SHAPER

(Refer to Figure 9.)

The negative-going vertical sync pulses (from Q1) are direct coupled to the non-inverting input of the sync shaper stage, IC1. The combined action of an integrating network, consisting of C1, C2, C3, R5, R6, and R7, removes high frequency noise from the vertical sync pulses. Capacitor C3 performs the actual integrating, while resistors R5—R7 provide biasing for IC1. Capacitors C1 and C2 provide a bypass function.

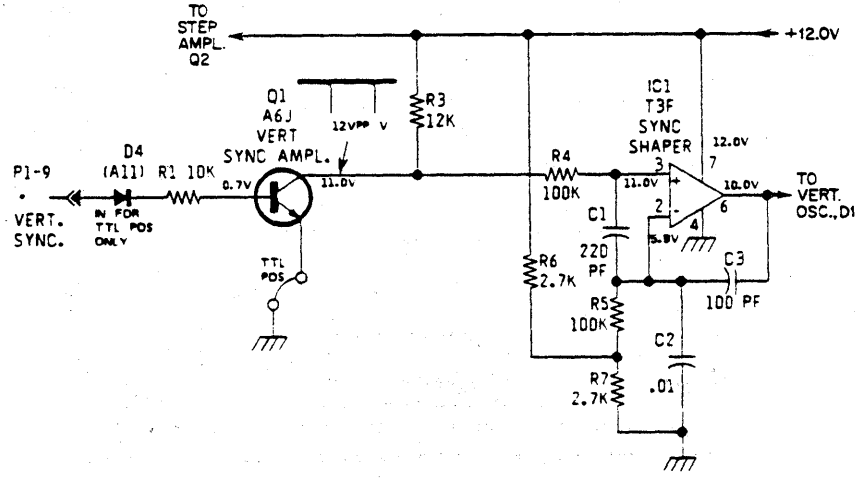
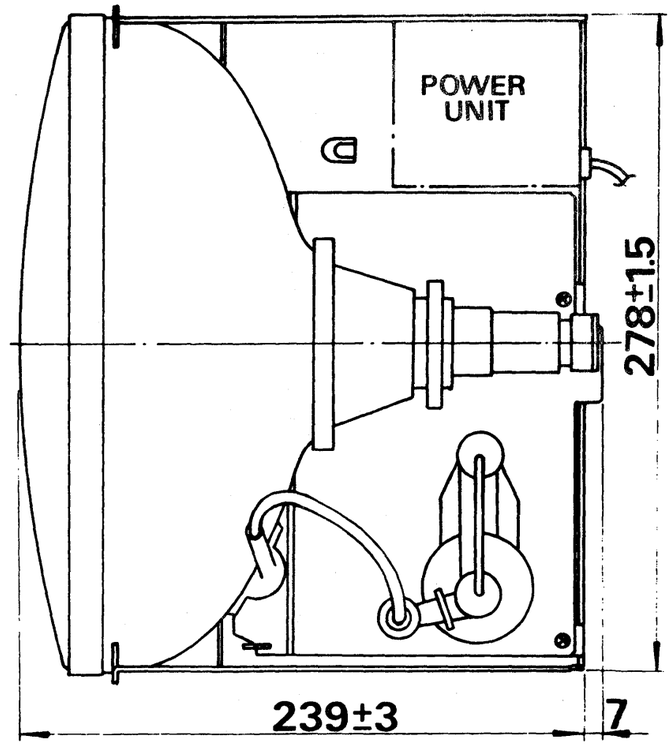


Figure 9. Vertical Sync Amplifier and Sync Shaper Circuits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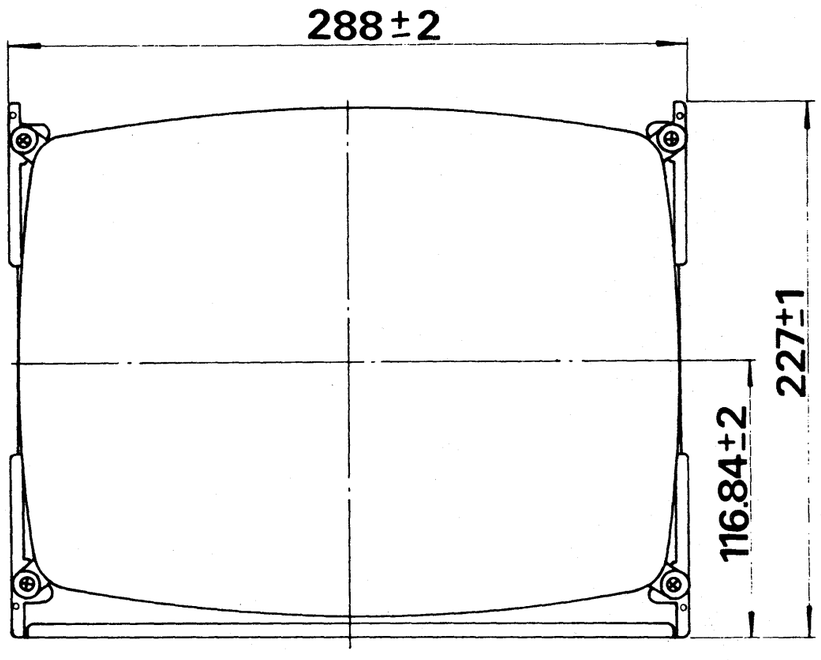
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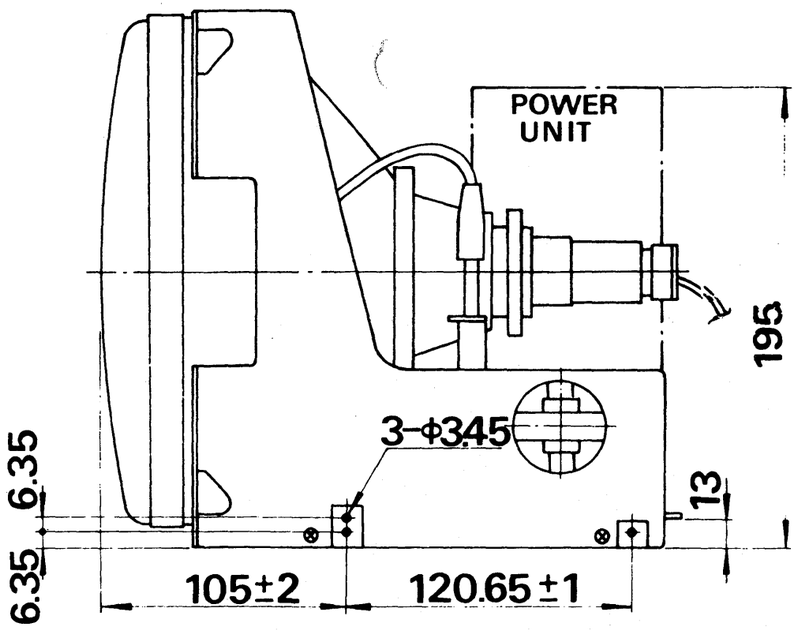
116.84±2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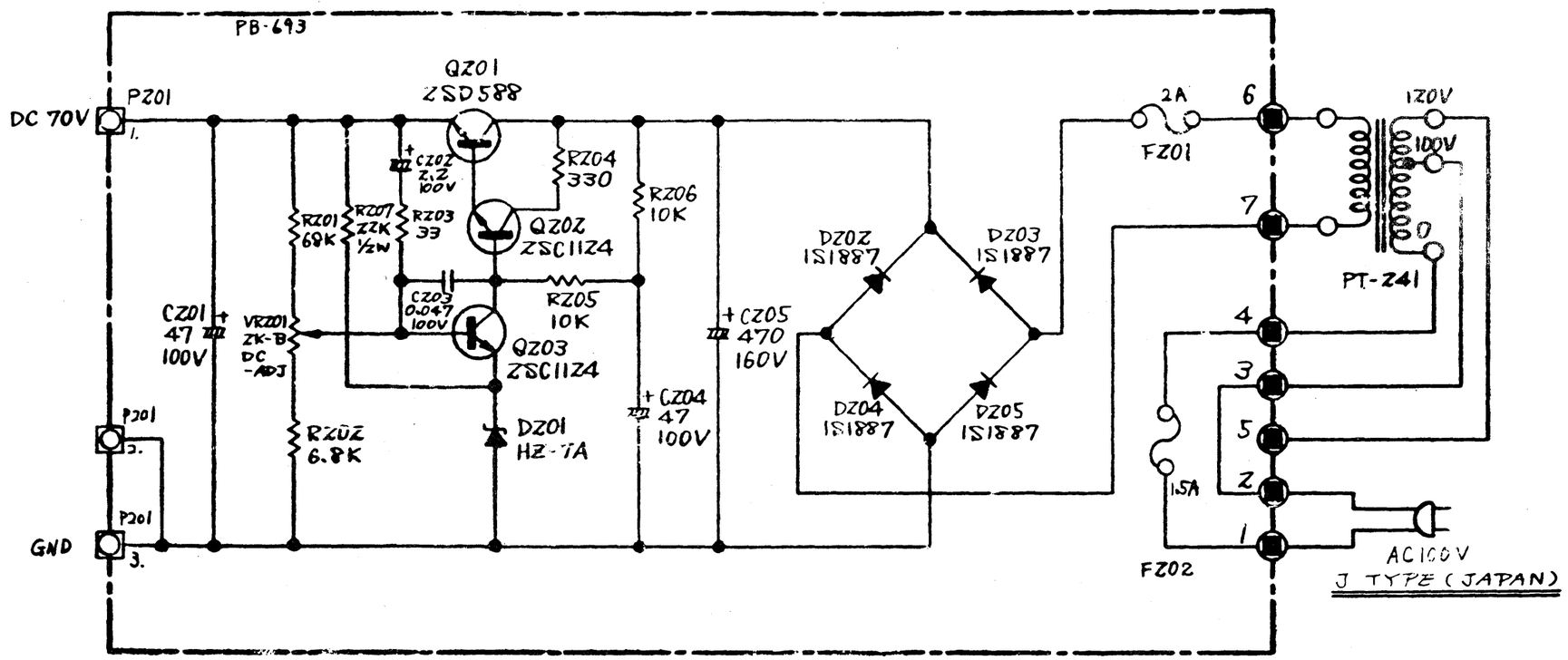
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GND
PZ01
3.
PZ01
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2SC1124
RZ01
68K
RZ07
22K
½W
RZ03
33
RZ04
330
RZ05
10K
RZ06
10K
RZ02
6.8K
CZ01
47
100V
VRZ01
2K-B
DC
-ADJ
CZ02
2.2
100V
CZ03
0.047
100V
CZ04
47
100V
CZ05
470
160V
DZ01
HZ-7A
DZ02
1S1887
DZ03
1S1887
DZ04
1S1887
DZ05
1S1887
2A
FZ01
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FZ02
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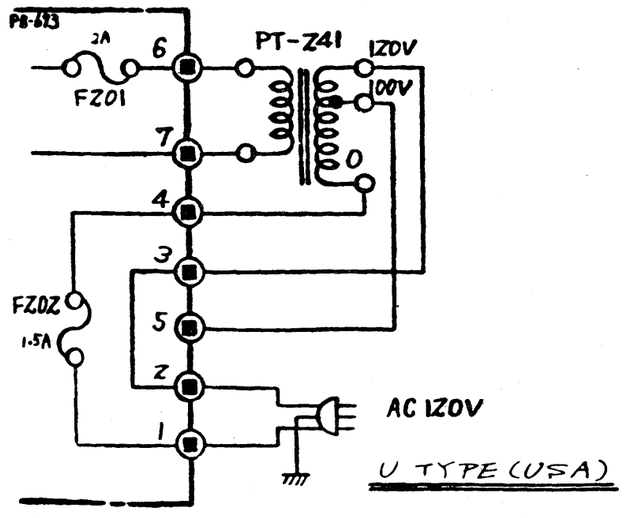
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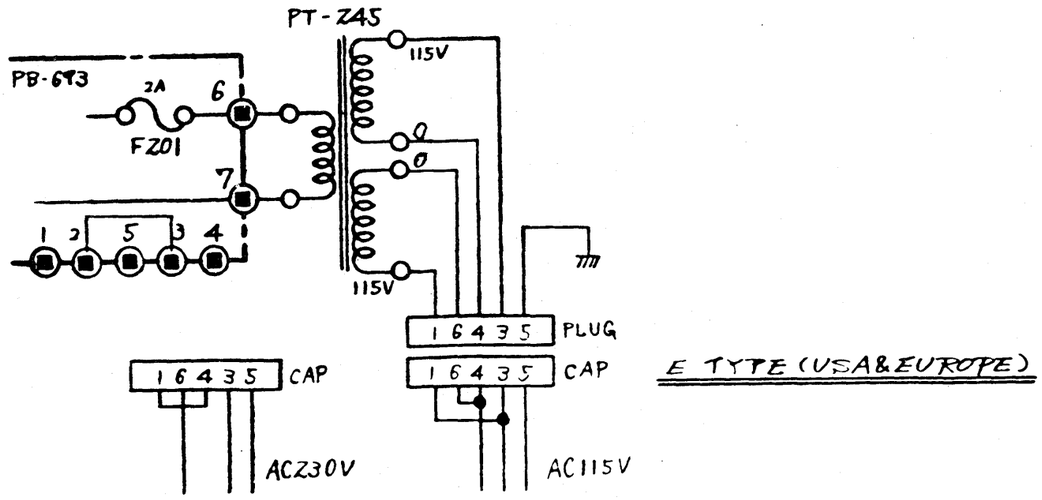
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1 6 4 3 5
PLUG
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CAP
AC230V
1 6 4 3 5
CAP
AC115V
E TYPE (USA&EUROPE)

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B	回路番号変更 ZC790-202A → ZC781-201B	EM1596	77.12.5	K.T	
C	C127 挿絵追加変更 CHG: R167, R153, C132 ADD: R165, R166 CHG L102	— EM1597 EM1600	77.12.15	Yasuda	
D	ADD: R167, D110 CHG: R129, R109, C120 DEL: C109	EM1688	78.2.23	K.T	
E	ADD : SG103, SG104	EM1680	78.3.3	S.T	

PB-743

Q102 2SC1514

Q101 2SC1741

IC101 μPC-370C

Q103 2SC1124

Q104 2SC1170B

Q105 2SC1641

Q106 2SA854

Q107 2SA678

Q108 2SC1124

Q109 2SD401A

Q110 2SB546A

CRT C15M05-P4 (15") C12M07-P4 (12") m fg.

T101 DT-Z98

T102 DH-1191 FBT

DY-1191

EXT-BRT IM-B

VR101 1M H INT-BRT

VR102 5K-B H.FREQ

VR103 1M-B V.FREQ

VR104 20K-B HEIGHT

VR105 20K-B V.LIN

VR106 1M-B FOCUS

L101 DL-Z04 H.LIN

L102 DL-3344 WIDTH

L103 3μH

VIDEO +4V 0 CONTRAST 500-B

HD +4V 0 5μs 18.5 kHz

VD +4V 0 0.5±0.2ms 50, 60Hz

N.C. P103 1 2 3 4

ARC GND

SG101 G1

SG102 K

SG104 H H

SG103

ANODE G4 G2

16 kV(15") 14 kV(12")

+70V

-100V

VIDEO GND (10)

HD GND (1)

DC RTN (1)

FRAME GND

DC RTN P101 3

DC RTN P101 2

+70V DC P101 1 (7)

VD GND (10)

P102 5 4 3 N.C.

NOTES

○ : INTERFACE CONNECTOR (10P)

◉ : PIN CONNECTOR (P101 : 3P, P102 : 5P) P103 : 4P)

■ : WRAPPING TERMINAL

RESISTORS UNLESS OTHERWISE NOTED ¼W

CAPACITORS UNLESS OTHERWISE NOTED 50V

※ ADJUSTED

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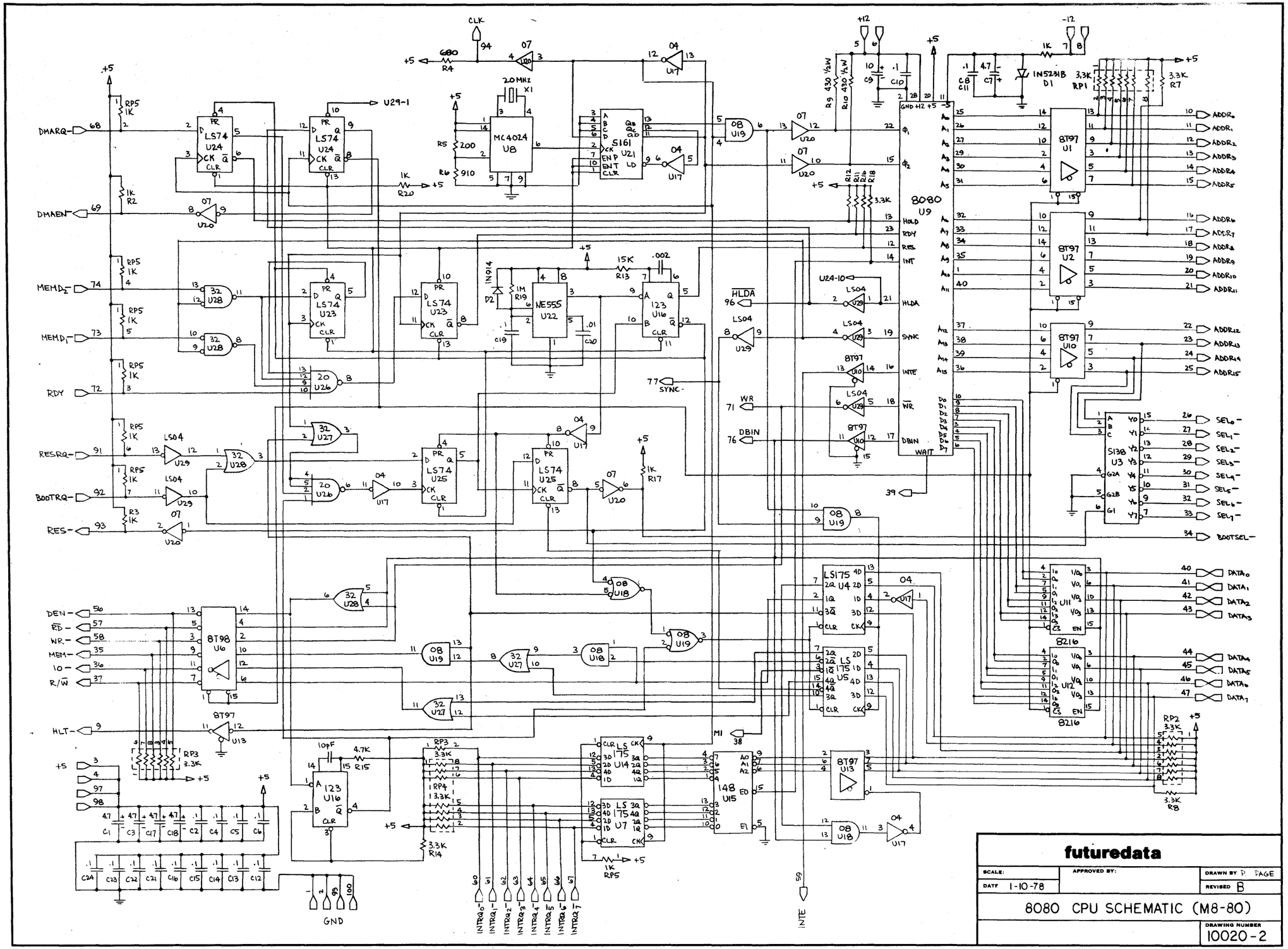
	R. Sena 77.8.22			A2		



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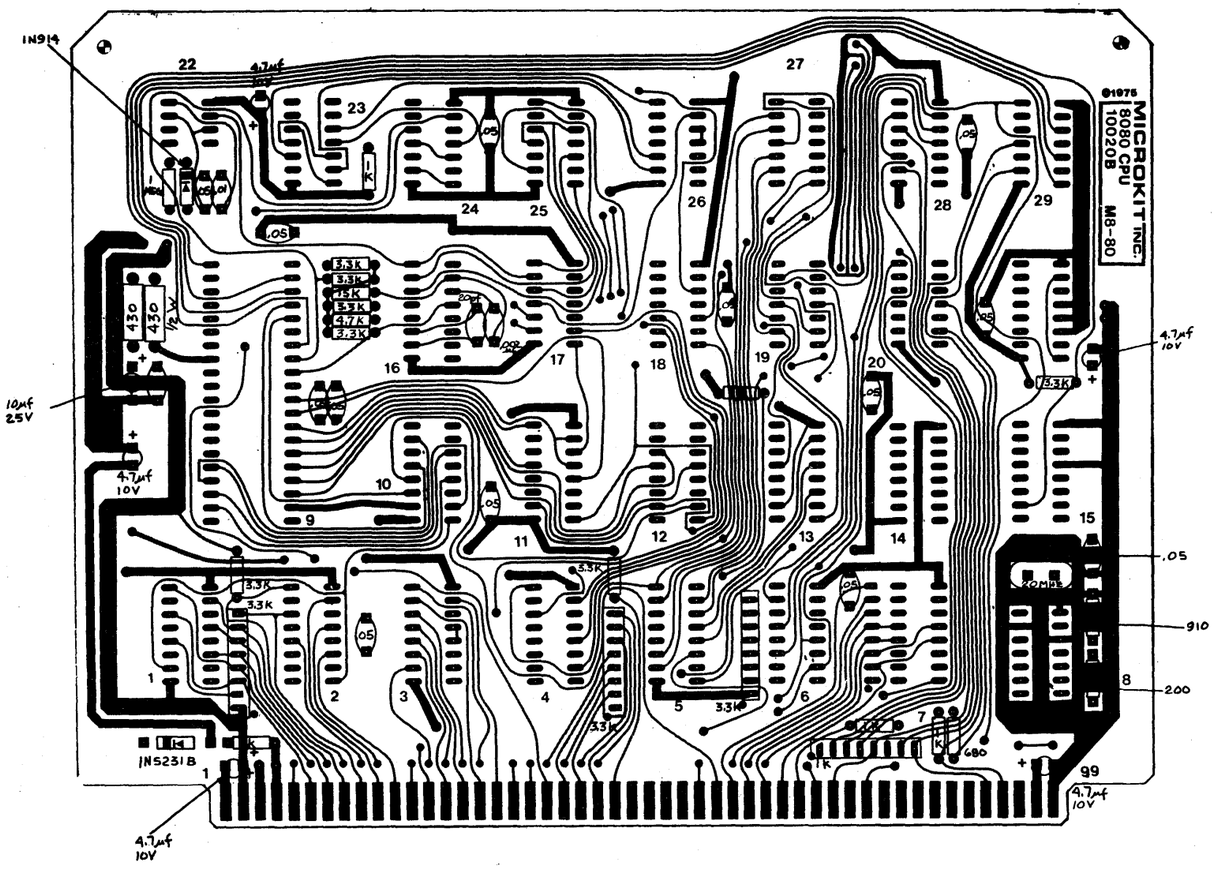

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MICROKIT INC.

TITLE
COMPONENT LAYOUT
8080 CPU

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10020-3 B

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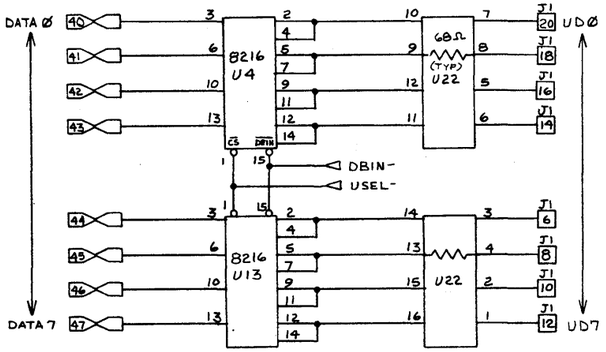

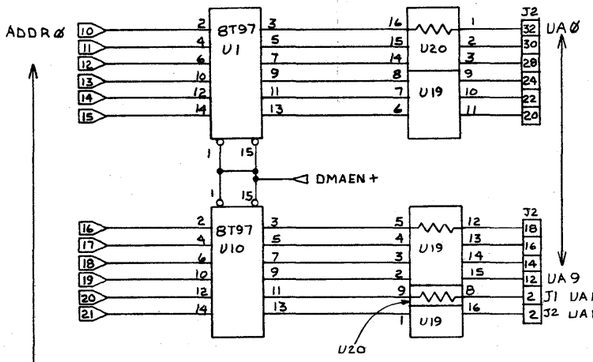

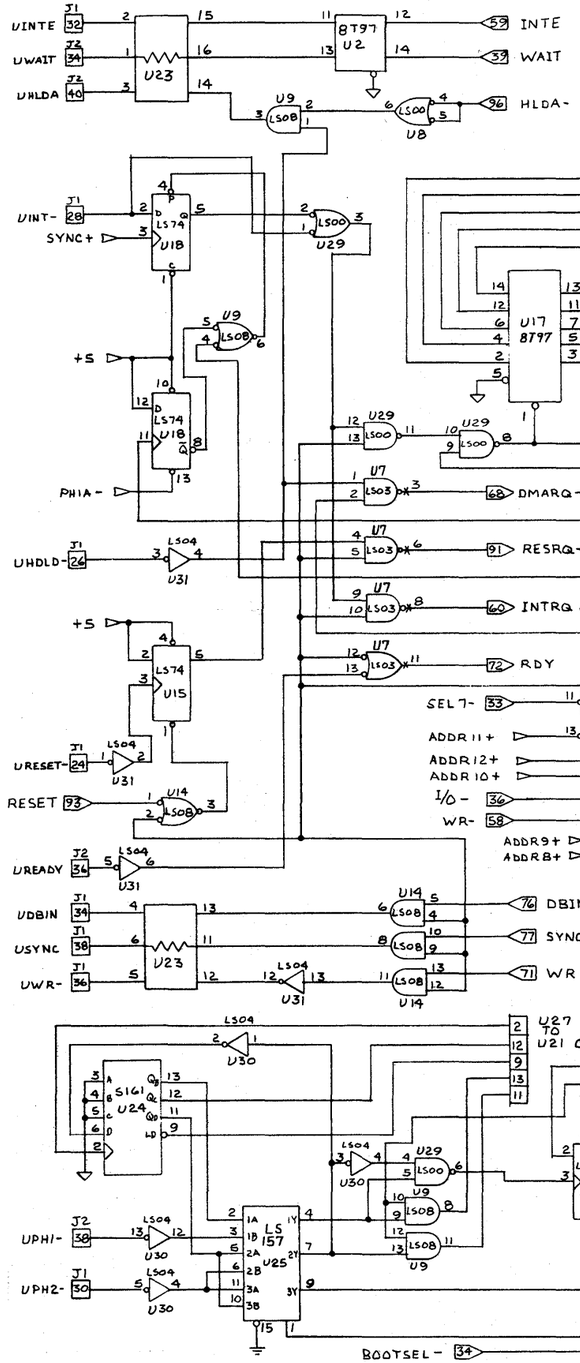

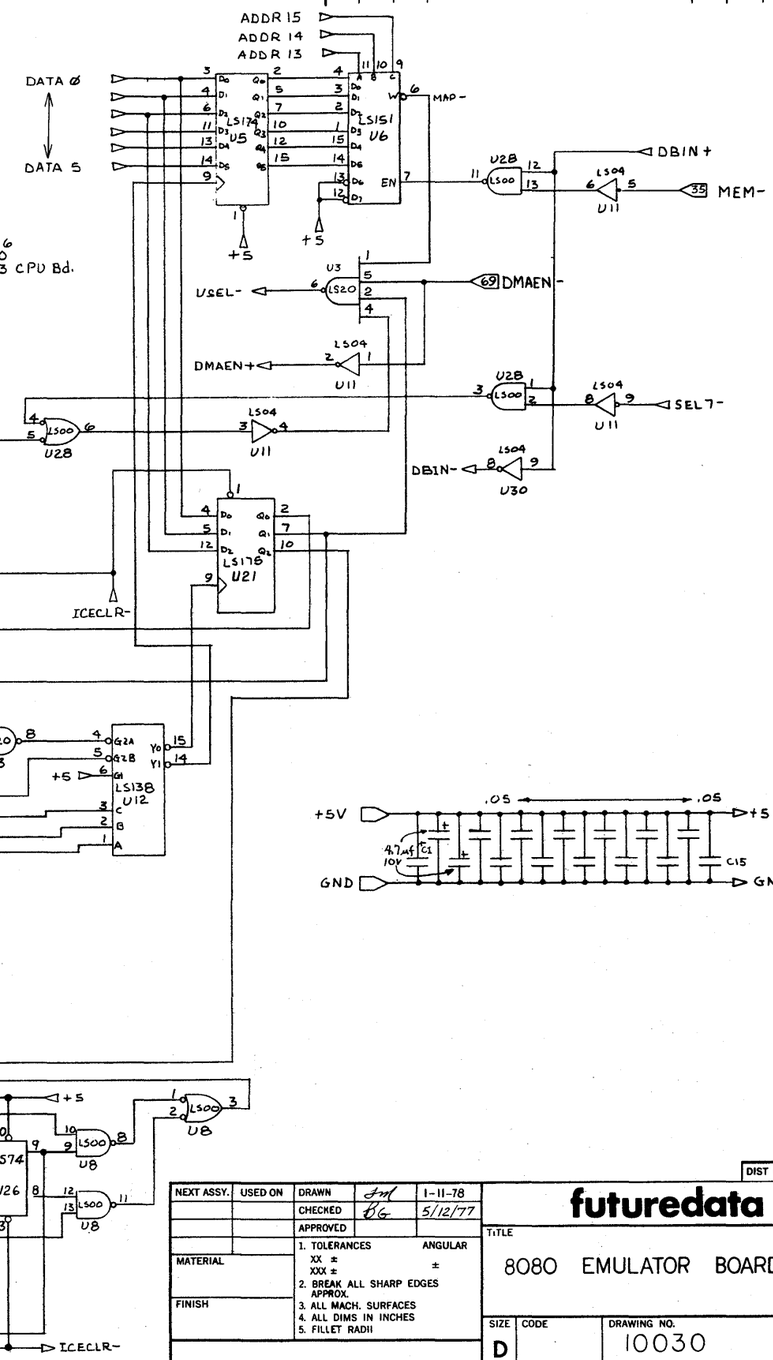

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futuredata

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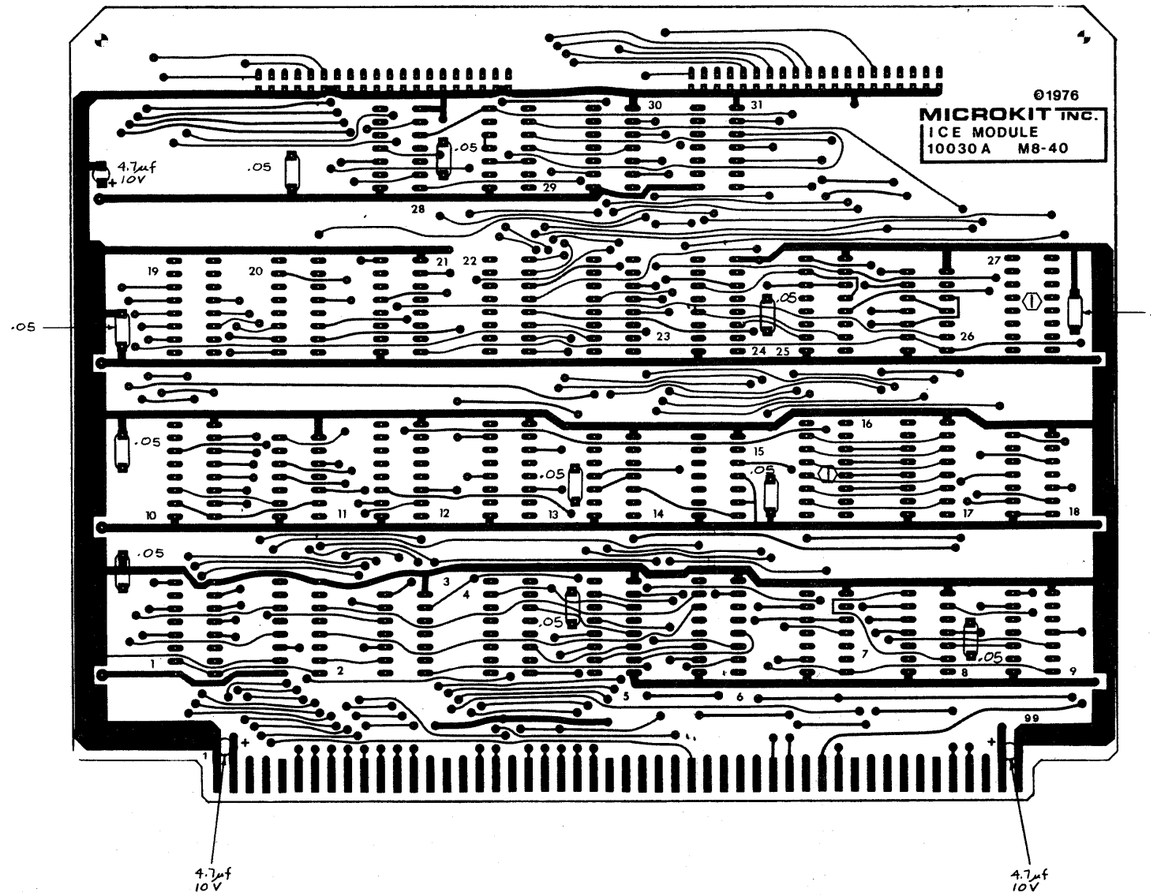

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U8	74LS00
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U10	8T97
U11	74LS04
U12	74LS138
U13	8216
U14	74LS08
U15	74LS74
U16	C9316-02 MOUNT ON BACK OF BOARD
U17	8T97
U18	74LS74
U19	R PACK
U20	R PACK
U21	74LS175
U22	R PACK
U23	R PACK
U24	74S161
U25	74LS157
U26	74LS74
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U28	74LS00
U29	74LS00
U30	74LS04
U31	74LS04

R PACK (Beckman 898-3-R68) 4EA.

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MICROKIT INC.

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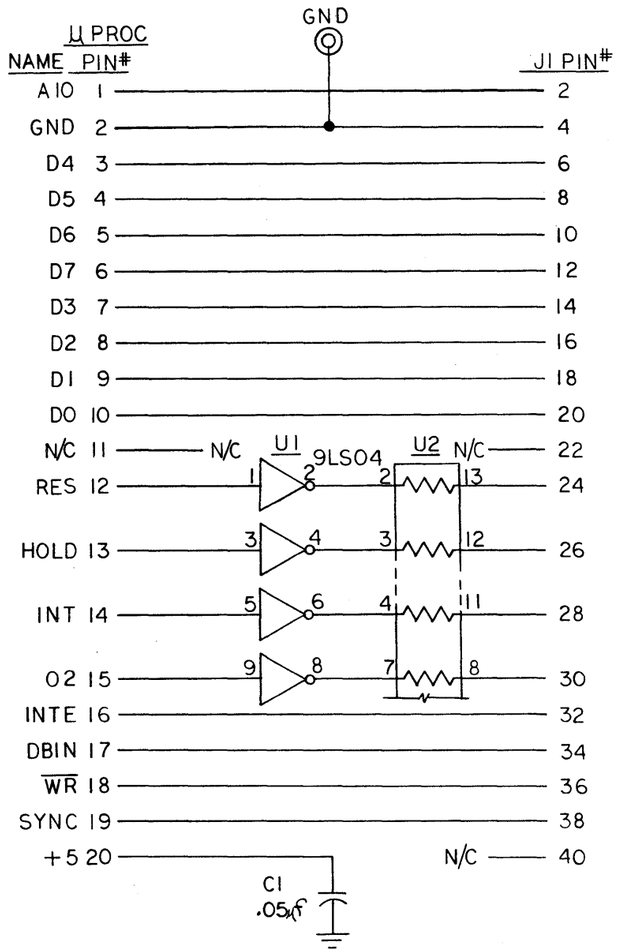

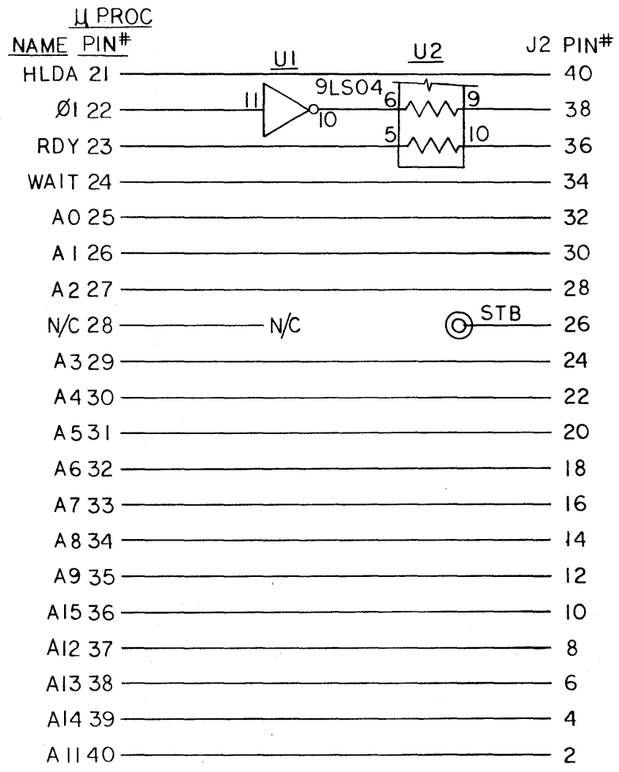

2. U2 RESISTORS ARE 68Ω'S TYPICAL.
1. ALL ODD NUMBERED PINS ON J1 & J2 ARE GROUND.
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PARTS LIST					

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APPLICATION		MATERIAL	DR BY J. Davis 12Nov77
		FINISH	CHK BY
		DO NOT SCALE DRAWING	APPROVED BY

FUTUREDATA

SCHEMATIC, 8080 PROBE

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SCALE | SHEET | OF

10029-6 B

DIETZGEN/POST CLEARPRINT 1020-15

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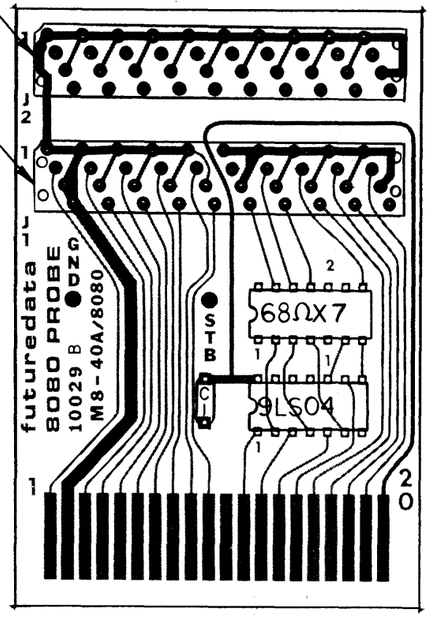

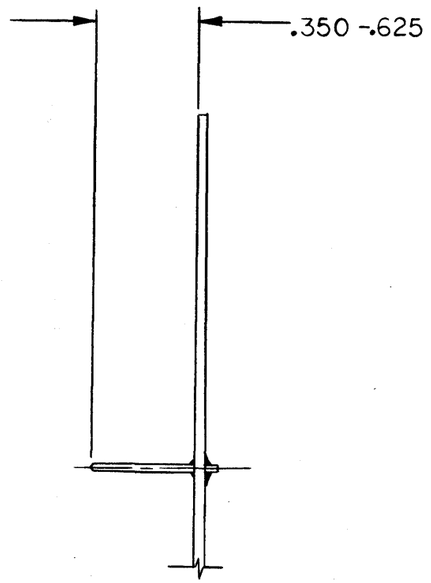

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3	2			.025 SQ. WIRE WRAP PIN	
2	1		899-3-R68	I.C., 68ΩX7 R-PACK-BECKMAN	U2
1	1		9LS04	I.C., HEX INVERTER	U1

PARTS LIST

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ASSEMBLY, 8080 PROBE
M8-40A/8080

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futuredata

TITLE: 6800 CPU

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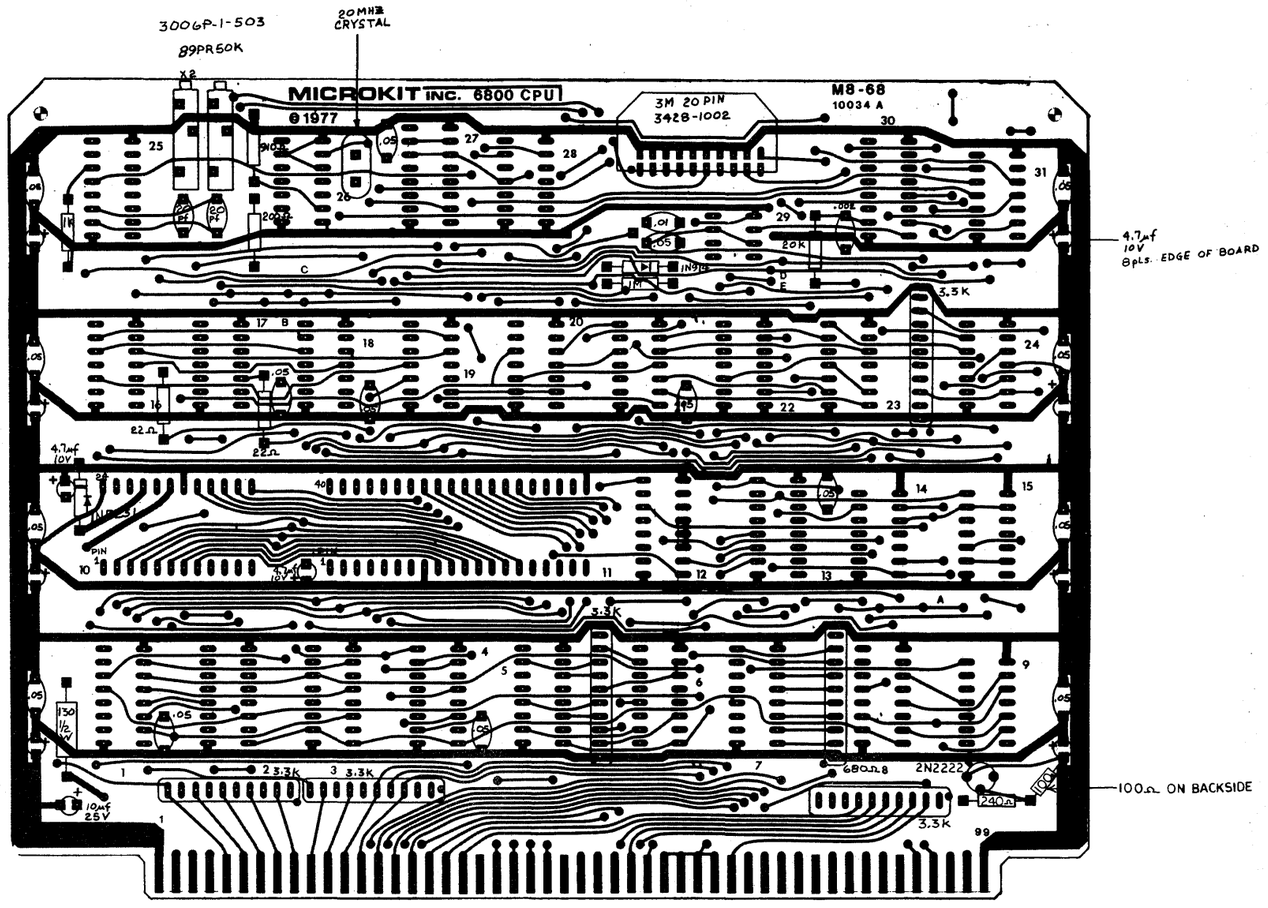

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M8-68		CHECKED		11-10-78
		APPROVED		
MATERIAL		1 TOLERANCES ANGULAR XX · XXX · · BREAK ALL SHARP EDGES APPROX 3 ALL MACH SURFACES 4 ALL DIMS IN INCHES 5 FILLET RADII		
FINISH				

DIST CODE

MICROKIT INC.

TITLE
COMPONENT LAYOUT
6800 CPU

SIZE	CODE	DRAWING NO	
D		10034	-3 A

SHEET

10034 3 A

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

2. ALL EVEN NUMBERED PINS 2 THRU 18 ON J3 ARE GROUND.
ALL ODD NUMBERED PINS ON J1 & J2 ARE GROUND, J1 PIN 2 AND J2 PIN 40 ARE GROUND.
1. R1 THRU R6 VALUES ARE IN OHMS, ±5%, ¼W.

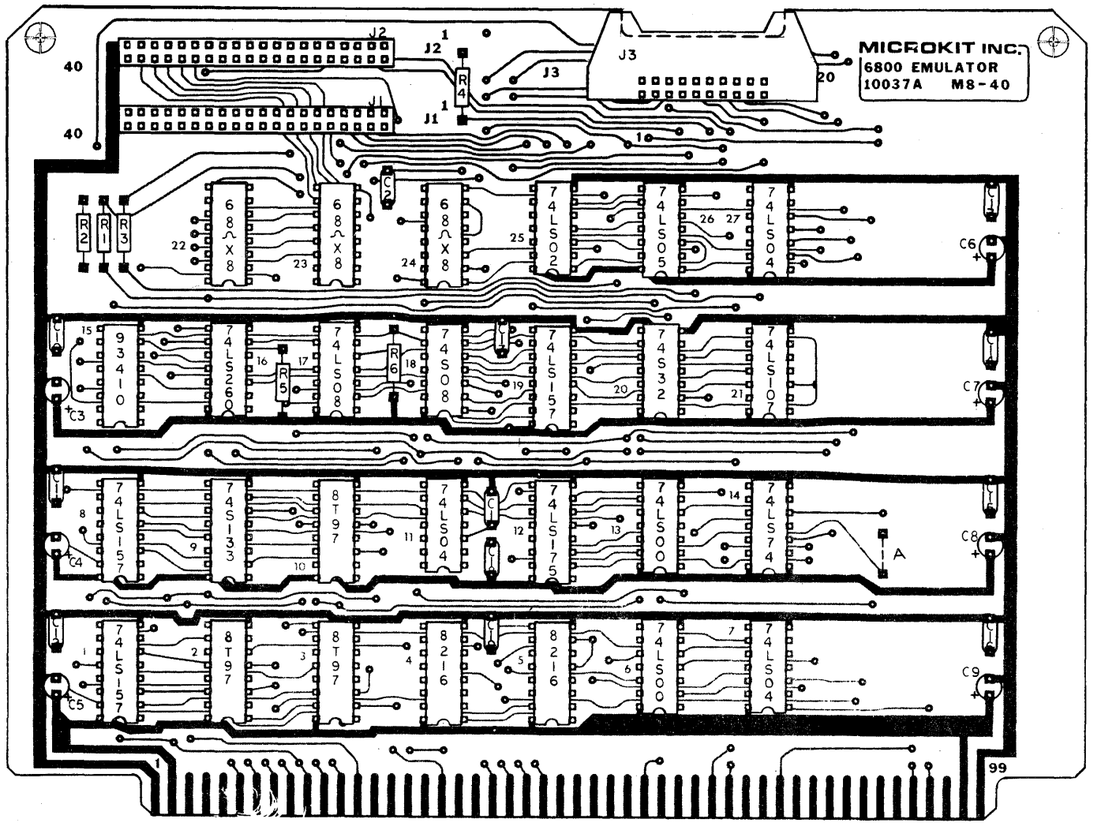
NOTE: UNLESS OTHERWISE SPECIFIED:

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION		ZONE

PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± / DECIMALS .X ± .XX ± .XXX ± / ANGLES ±	CONTRACT NO.	futuredata	
	DR BY T. WADE 7-10-77	SCHEMATIC 6800 EMULATOR	
	CHK BY		
	APPROVED BY		
MATERIAL		SIZE D	CODE IDENT NO.
FINISH		DWG NO. 10037-6 A	
NEXT ASSY	USED ON	SCALE	SHEET 1 OF 1
APPLICATION	DO NOT SCALE DRAWING		

DIETRICH-POST CLEARPRINT 1020-10



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	
27	1		3428-1002	CONN. 20 PIN -3M	J3
26	2		2-87227-0	CONN. 40 PIN HEADER-AMP	J1 & J2
25	1			RES, 1K, ±5%, 1/4W	R6
24	1			RES, 3.3K, ±5%, 1/4W	R5
23	1			RES, 560Ω, ±5%, 1/4W	R4
22	3			RES, 68Ω, ±5%, 1/4W	R1,2,3
21	10			CAP, .05UF CER DISK	C10-19
20	7			CAP, 4.7UF, 10V TANT	C3-9
19	1			CAP, .01 UF CER DISK	C2
18	1			CAP, 100pf CER DISK	C1
17	1		74LS05	I.C., HEX INVERTER O.C.	U26
16	1		74LS02	QUAD 2-IN NOR	U25
15	3		898-3-R68	68ΩX8 R-PACK-BECKMAN	U22,23,24
14	1		74LS107	DUAL JK FF	U21
13	1		74S32	QUAD 2-IN OR	U20
12	1		74S08	QUAD 2-IN AND	U18
11	1		74LS08	QUAD 2-IN AND	U17
10	1		74LS260	DUAL 5-IN NOR	U16
9	1		93410	256 BIT RAM	U15
8	1		74LS74	DUAL-D FF	U14
7	1		74LS175	HEX/QUAD-D FF	U12
6	1		74S133	13-IN NAND	U9
5	3		74LS04	HEX INVERTER	U7,11,27
4	2		74LS00	QUAD 2-IN NAND	U6,13
3	2		8216	BI-DIRECTIONAL BUS DR.	U4,5
2	3		8T97	TRI-STATE HEX BUFF.	U2,3,10
1	3		74LS157	I.C., QUAD 2 TO 1 MUX	U1,8,19

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J. Razio	7-10-77
CHECKED	

MICROKIT INC.

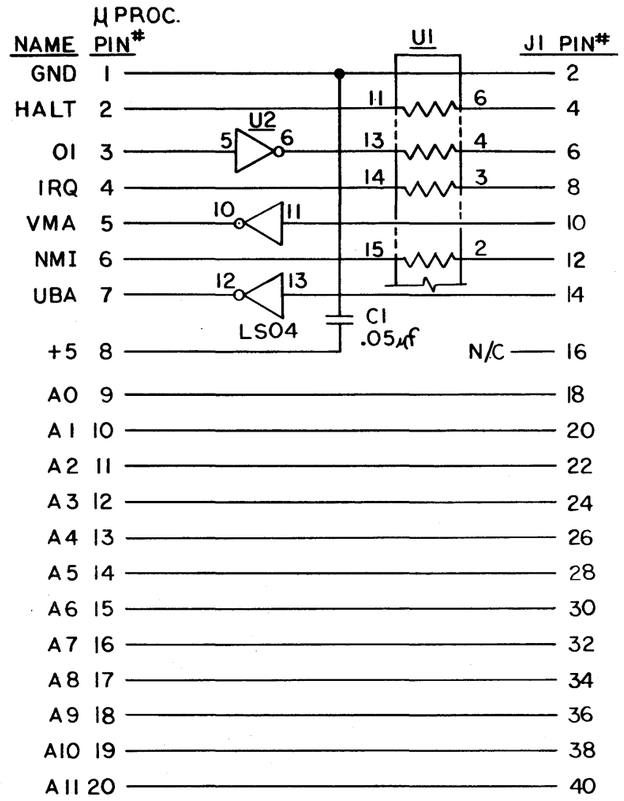
ASSEMBLY, 6800 EMULATOR M8-40

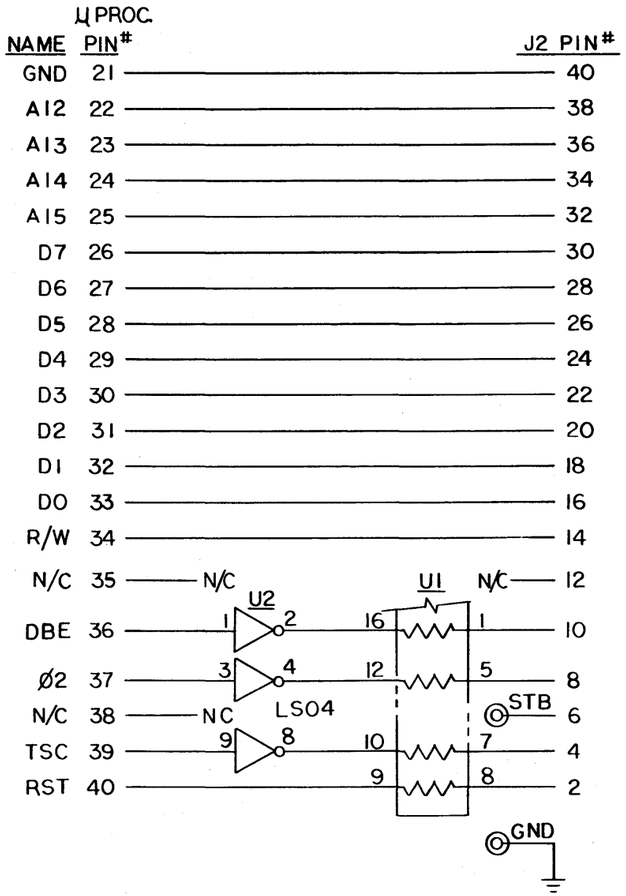
SIZE	CODE IDENT NO.	DRAWING NO.	
D		10037-5	A

SCALE 2/1 SHEET 1 OF 1

100375 A

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED





2. U1 RESISTORS ARE 68Ω'S TYPICAL.
1. ALL ODD NUMBERED PINS ON J1 & J2 ARE GROUND.

NOTES: UNLESS OTHERWISE SPECIFIED.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION			ZONE
PARTS LIST						

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS X .XX .XXX ANGLES ± ± ± ±	CONTRACT NO.
MATERIAL	DR BY J. Sabo 7-5-77
FINISH	CHK BY
DO NOT SCALE DRAWING	APPROVED BY

NEXT ASSY	USED ON
APPLICATION	

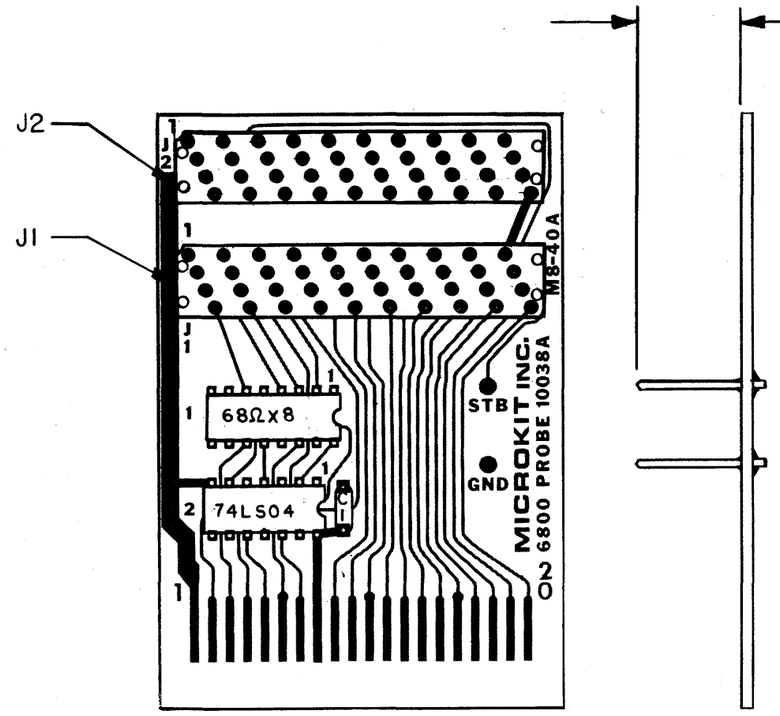
futuredata

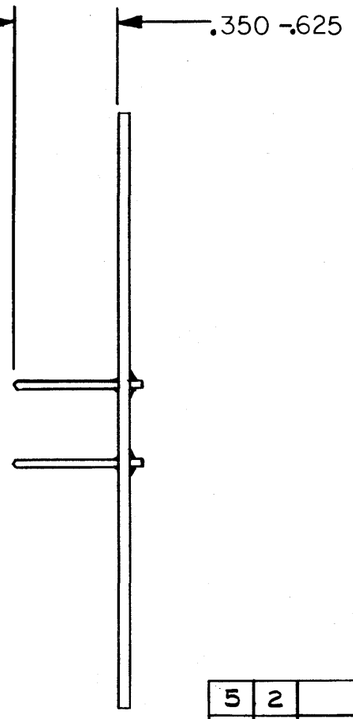
SCHEMATIC,
6800 PROBE

SIZE	CODE IDENT NO.	DWG NO.	
D		10038-6	A
SCALE		SHEET	OF

10038-6 A

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED





ITEM	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REF DES
5	2		3418-0000T	CONNECTOR-3M 40 PIN	J1, J2
4	1			CAP, .05UF, 20V, CER DISK	C1
3	2			.025 SQ. WIRE WRAP PIN	
2	1		898-3-R68	I.C., 68ΩX8 R-PACK-BECKMAN	U1
1	1		74LS04	I.C., HEX INVERTER	U2

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J. TABOR	7-7-77
CHECKED	

MICROKIT INC.

ASSEMBLY, 6800 PROBE
M8-40A

SIZE	CODE IDENT NO.	DRAWING NO.	
C		10038-5	A

SCALE 2/1 SHEET | OF |

10038-5 A B

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION		ZONE
PARTS LIST					

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± DECIMALS .X ± .XX ± .XXX ± ANGLES ± ± ± ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

DR BY

CHK BY R. YOUNKIN 11-10-76

APPROVED BY

NEXT ASSY | USED ON

APPLICATION

futuredata

SCHEMATIC, Z80-CPU BOARD M8-Z80

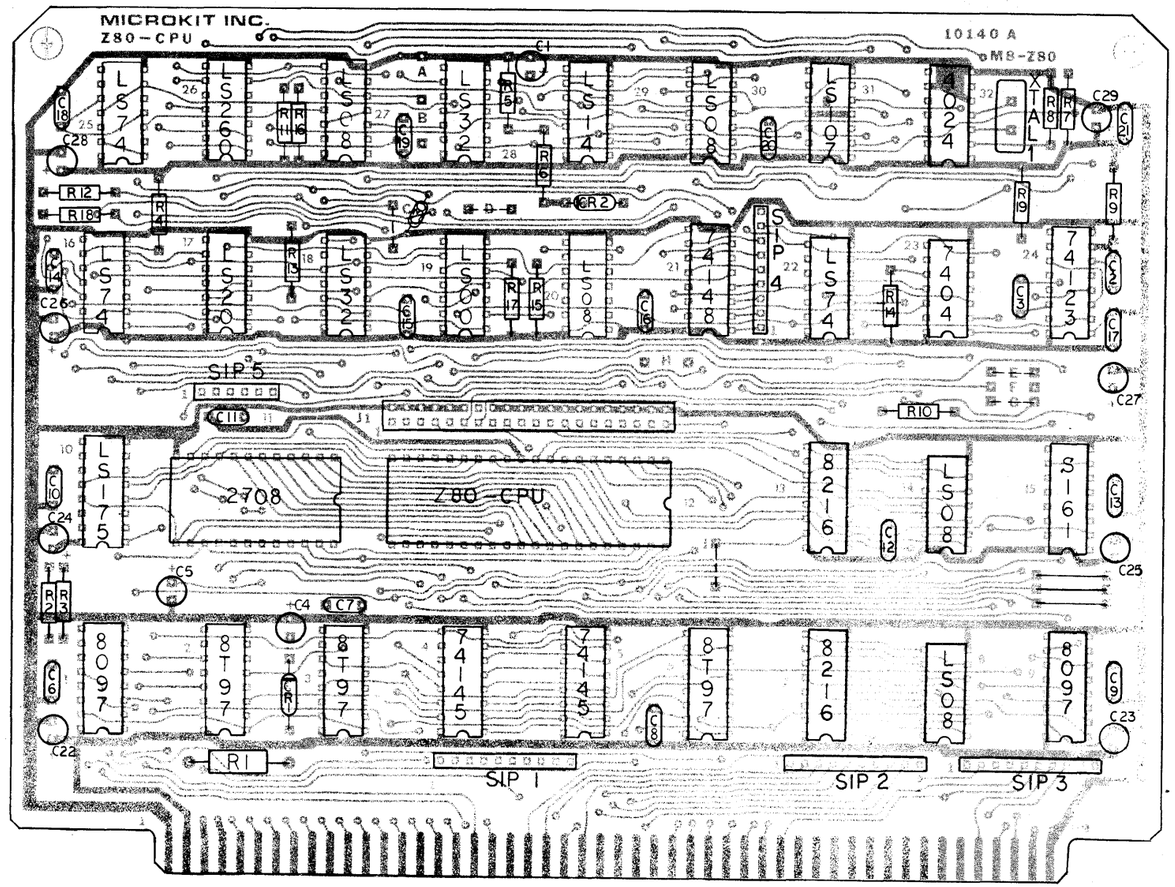
SIZE	CODE IDENT NO.	DWG NO.	
D		10140-6	C
SCALE		SHEET 1 OF 1	

10140-6 B

NOTE: UNLESS OTHERWISE SPECIFIED:

1. ALL EVEN NUMBERED PINS ON J1 ARE GROUND.
2. ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4 W.
3. -X- = 3.3K PULL-UP.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	
43					
42	1			CAP. 100pf CER DISK	C30
41	1		2-87227-0	CONNECTOR-40 PIN (AMP)	J1
40	1		4306R-101-103	RES NETWK, 10K (BOURNS)	SIP 5
39	2		4310R-101-332	RES NETWK, 3.3K (BOURNS)	SIP 4,3
38	1		4310R-101-102	RES NETWK, 1K (BOURNS)	SIP 2
37	1		4310R-101-681	RES NETWK, 680Ω (BOURNS)	SIP 1
36	1			CRYSTAL, 16 MHZ	XTAL 1
35	1			DIODE, IN914	CR2
34	1			DIODE, IN5231B	CR1
33	1			RES., 330Ω, 5%, 1/4W	R14
32	1			RES., 1K, 5%, 1/4W	R10
31	1			RES., 910Ω, 5%, 1/4W	R8
30	1			RES., 200Ω, 5%, 1/4W	R7
29	9			RES., 10K, 5%, 1/4W	R5,6,9,12,13,15-19
28	4			RES., 3.3K, 5%, 1/4W	R2,3,4,11
27	1			RES., 130Ω, 5%, 1/2W	R1
26	16			CAP., .05UF CER DISK	C6-21
25	1			CAP, 10UF, 25V TANT	C5
24	9			CAP, 4.7UF, 10V TANT	C4, 22-29
23	1			CAP, 30pf CER DISK	C3
22	1			CAP., .001UF CER DISK	C2
21	1			CAP, 33uf 10v. TANT	C1
20	1		4024	I.C., CRYSTAL OSC	U32
19	1		74LS107	I.C., DUAL J-K FF	U31
18	1		74LS14	I.C., SCHMITT HEX INVERT	U29
17	1		74LS260	I.C., DUAL 5-IN NOR	U26
16	1		74123	I.C., MONOSTABLE VIBRATOR	U24
15	1		7404	I.C., HEX INVERTER	U23
14	1		74148	I.C., 8 TO 3 PRIORITY ENCDR	U21
13	1		74LS00	I.C., QUAD 2-IN NAND	U19
12	2		74LS32	I.C., QUAD 2-IN OR	U18,28
11	1		74LS20	I.C., DUAL 4-IN POS NAND	U17
10	3		74LS74	I.C., DUAL-D FF	U16,22,25
9	1		74S161	I.C., SYNCHRO 4-BIT CNTR	U15
8	1		Z80-CPU	I.C., C.P.U.	U12
7	1		2708	I.C., PROM	U11
6	1		74LS175	I.C., QUAD-D FF	U10
5	2		8216	I.C., BI-DIRECTION BUS DRVR	U7,13
4	5		74LS08	I.C., QUAD 2-IN AND	U8,14,20,27,30
3	2		74145	I.C., BCD TO DECIMAL DRVR	U4,5
2	3		8T97	I.C., TRI-STATE HEX BUFF	U2,3,6
1	2		8097	I.C., TRI-STATE HEX BUFF	U1,9

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± — DECIMALS .XX ±. .XXX ±. ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J. Fazio	8.25.77
CHECKED	11-10-77

MICROKIT INC.

ASSEMBLY, Z80-CPU M8-Z80

SIZE	CODE IDENT NO.	DRAWING NO.
D		10140-5 C

SCALE 2/1 SHEET 1 OF 1

10140-5 C

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL ODD NUMBERED PINS ON J1, J2 & J3 AND J2 PIN 24 ARE GROUND.
2. ALL RESISTORS VALUES ARE OHMS ±5%, 1/4 W.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± DECIMALS .X ± .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

DR BY	T WADE	1NOV77
CHK BY	R. YOUNKIN	5 JUL 78
APPROVED BY		

NEXT ASSY | USED ON

APPLICATION

futuredata

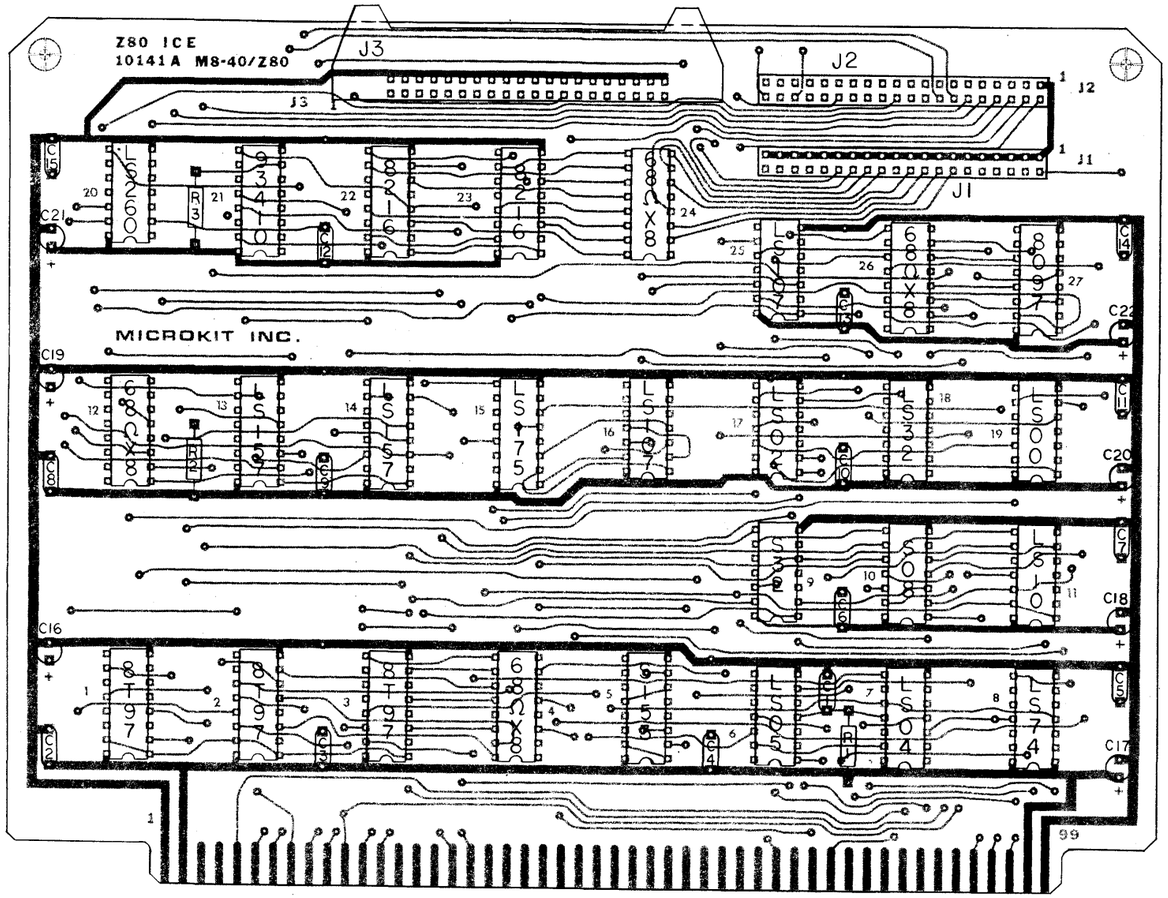
SCHEMATIC, Z80 I.C.E.

SIZE	CODE IDENT NO.	DWG NO.	REV
D		10141-6	D

SCALE | SHEET 1 OF 1

10141-6 A

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	
25	3		RES., 1K, ±5%, 1/4W	R1,2,3
24	1	3432-1002	CONNECTOR, 40 PIN-3M	J3
23	2	2-87227-0	CONNECTOR, 50 PIN-AMP	J1, 2
22	7		CAP. 4.7 UF 10V TANT	C16-22
21	14		CAP., .05 UF CER DISK	C2-15
20	1		CAP., 330 PF CER DISK	C1
19	1	93410	I.C., 256 BIT RAM	U21
18	1	8097	TRI-STATE HEX BUFF.	U27
17	2	8216	BI-DIRECTION BUS DR	U22,23
16	1	74LS260	DUAL 5-IN NOR	U20
15	1	74LS00	QUAD 2-IN NAND	U19
14	1	74LS32	QUAD 2-IN OR	U18
13	1	74LS02	QUAD 2-IN NOR	U17, 8A
12	2	74LS107	DUAL JK FF	U16, 25
11	1	74LS175	QUAD - D FF	U15
10	2	74LS157	QUAD 2 TO 1 MUX	U13, 14
9	1	74LS10	TRIP. 3-IN NAND	U11
8	1	74S08	QUAD 2-IN AND	U10
7	1	74S32	QUAD 2-IN OR	U9
6	1	74LS74	DUAL-D FF	U8
5	1	74LS04	HEX INVERTER	U7
4	1	74LS05	HEX INVERTER O.V.	U6
3	1	74S153	DUAL, 4 TO 1 SELECT/MUX	U5
2	4	898-3-R68	68Ω X8 R-PACK BECKMAN	U4,12,24,26
1	3	8T97	I.C., TRI-STATE HEX BUFF.	U1,2,3

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± — DECIMALS .XX ±. .XXX ±. ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J. Razio	9-12-77
CHECKED	

MICROKIT INC.

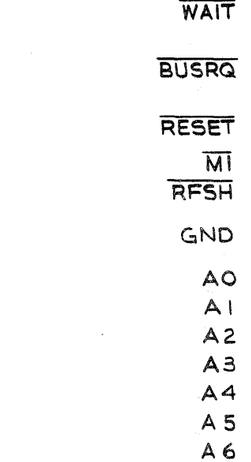
ASSEMBLY, Z80 ICE M8-40/Z80

SIZE	CODE IDENT NO.	DRAWING NO.	
D		10141-5	A

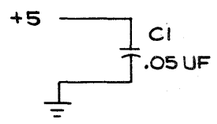
SCALE 2/1 SHEET 1 OF 1

10141-5 A

NAME	µPROC. PIN NO.	J1 PIN NO.
A11	1	2
A12	2	4
A13	3	6
A14	4	8
A15	5	10
CLK	6	12
D4	7	14
D3	8	16
D5	9	18
D6	10	20
+5	11	22
D2	12	24
D7	13	26
DØ	14	28
D1	15	30
$\overline{INT}$	16	32
$\overline{NMI}$	17	34
$\overline{HLT}$	18	36
$\overline{MREQ}$	19	38
$\overline{IORQ}$	20	40



NAME	µPROC. PIN NO.	J2 PIN NO.
$\overline{DR}$	21	40
$\overline{WR}$	22	38
$\overline{BUSAK}$	23	36
$\overline{WAIT}$	24	34
$\overline{BUSRQ}$	25	32
$\overline{RESET}$	26	30
$\overline{M1}$	27	28
$\overline{RFSH}$	28	26
GND	29	24
A0	30	22
A1	31	20
A2	32	18
A3	33	16
A4	34	14
A5	35	12
A6	36	10
A7	37	8
A8	38	6
A9	39	4
A10	40	2



3. PINS 1 AND 15 OF U1 ARE GROUNDED.
2. U2 IS 14 PIN R-PACK, 68Ω.
1. ALL ODD NUMBERED PINS ON J1 & J2 ARE CONNECTED TO GROUND.

NOTES: UNLESS OTHERWISE SPECIFIED.

M8-40A/Z80

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION		ZONE
			PARTS LIST		

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± DECIMALS X ± XX ± XXX ± ANGLES ±

CONTRACT NO.

DR BY J. Sasio 9-8-77

CHK BY

APPROVED BY

MATERIAL

FINISH

DO NOT SCALE DRAWING

NEXT ASSY | USED ON

APPLICATION

futuredata

SCHEMATIC, Z80 PROBE

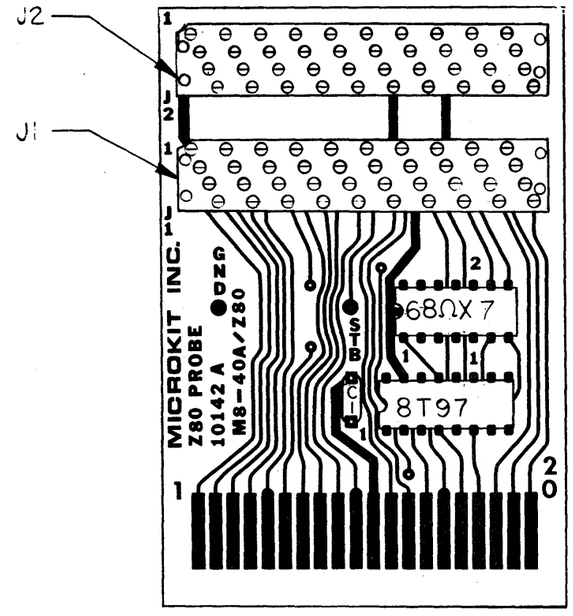
SIZE D | CODE IDENT NO. | DWG NO. 10142-6 | A

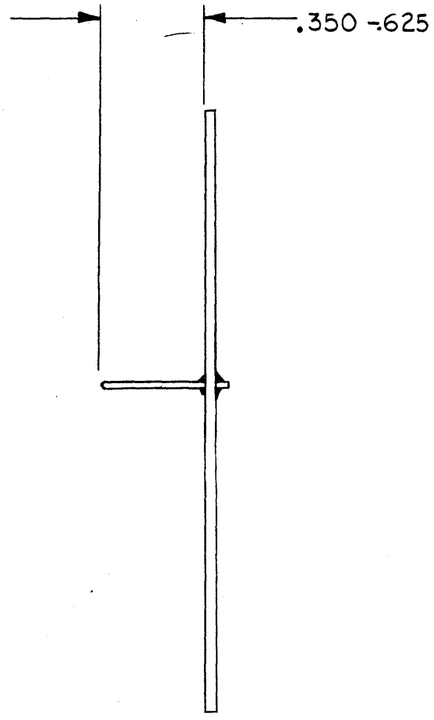
SCALE | SHEET 1 OF 1

10142-6 A

DIETZGEN-PORT CLEARPRINT 1020-14

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED





ITEM	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REF DES
5	2		3418-0000T	CONNECTOR-3M 40 PIN	J1, J2
4	1			CAP, .05UF, 20V, CER DISK	C1
3	2			.025 SQ. WIRE WRAP PIN	
2	1		899-3-R68	I.C., 68Ω X7 R-PACK-BECKMAN	U2
1	1		8T97	I.C., TRI-STATE HEX BUFF	U1

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J. Lazio	10 SEP 77
CHECKED	

MICROKIT INC.

ASSEMBLY, Z80 PROBE
M8-40A/Z80

SIZE	CODE IDENT NO.	DRAWING NO.	
C		10142-5	A

SCALE 2/1 SHEET 1 OF 1

10142-5 A

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

680Ω PULL-UP

1K PULL-UP

3.3K PULL-UP

NOTES: UNLESS OTHERWISE SPECIFIED.
1. IF 8085 IS USED, A 'MEM' WILL BE GENERATED DOING INTERRUPT ACKNOWLEDGE, SINCE DATA BUS STATUS IS SAME AS OP CODE FETCH.
2. ALL RESISTOR VALUES ARE IN OHMS ± 5% 1/4 W.
3. J3-ALL EVEN PINS ARE GROUND; J4-2 THRU 18 ARE GROUND.

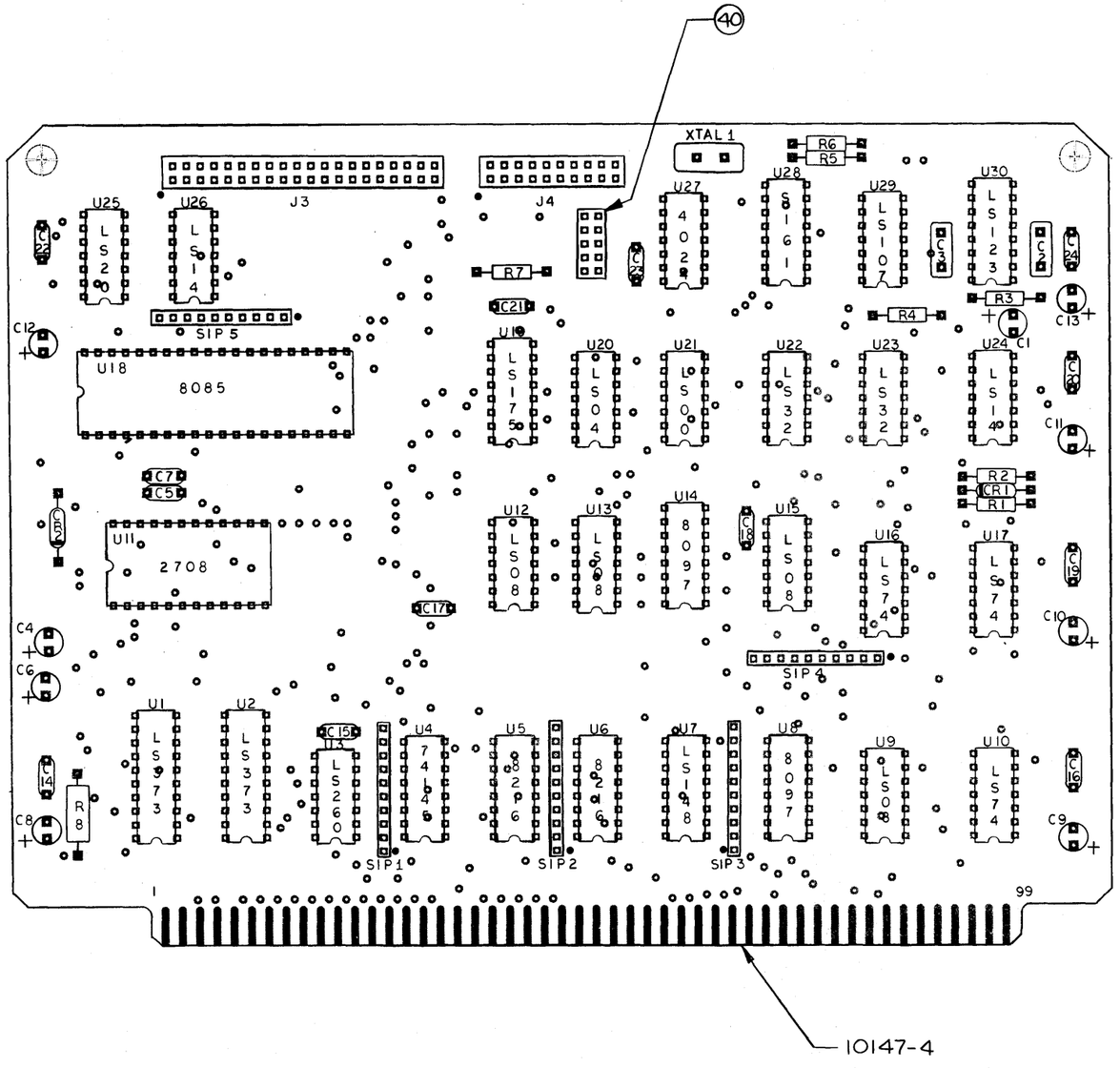
QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION		ZONE

PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± .X ± .XX ± .XXX ± ANGLES ±	CONTRACT NO.	FUTUREDATA	
MATERIAL	DR BY		
FINISH	CHK BY SUK YOUNKIN 7-31-78	SCHEMATIC, 8085A	
DO NOT SCALE DRAWING	APPROVED BY	SIZE D · CODE IDENT NO. · DWG NO. 10147-6 · REV D	
NEXT ASSY · USED ON APPLICATION		SCALE · SHEET OF	

10147-6 A

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



ITEM NO.	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	
40	1		87227-5	CONNECTOR-10 PIN JUMP HDR (AMP)	
39	1		1-87227-0	CONNECTOR-30 PIN (AMP)	J4
38	1		2-87227-0	CONNECTOR-40 PIN (AMP)	J3
37	1			CRYSTAL, 16 MHZ	XTAL1
36	1		4310R-101-103	RES NETWK, 10K (BOURNS)	SIP5
35	2		4310R-101-332	RES NETWK, 3.3K	SIP3,4
34	1		4310R-101-102	RES NETWK, 1K	SIP2
33	1		4310R-101-681	RES NETWK, 680Ω (BOURNS)	SIP1
32	1			RES, 130Ω, 5%, 1/2W	R8
31	1			RES, 910Ω, 5%, 1/4W	R6
30	1			RES, 200Ω, 5%, 1/4W	R5
29	5			RES, 10K, 5%, 1/4W	R1-4,7
28	1		IN5231B	DIODE, ZENER	CR2
27	1		IN914 •	DIODE, SIGNAL	CR1
26	1	•		CAP, 10μf, 25V TANT	C6
25	13			CAP, .05μf CER DISK	C5,7,14-24
24	7			CAP, 4.7μf, 10V TANT	C4,8-13
23	1			CAP, 30pf CER DISK	C3
22	1			CAP, .001μf CER DISK	C2
21	1			CAP, 33μf TANT	C1
20	1		74LS123	I.C, MONOSTABLE VIBRATOR	U30
19	1		74LS107	DUAL J-K FF	U29
18	1		745161	SYNCHRO 4-BIT CNTR	U28
17	1		4042	CRYSTAL OSC.	U27
16	1		74LS20	DUAL 4-IN NAND	U25
15	2		74LS14	SCHMITT HEX INV	U24,26
14	2		74LS32	QUAD 2-IN OR	U22,23
13	1		74LS00	QUAD 2-IN NAND	U21
12	1		74LS04	HEX BUFFER	U20
11	1		74LS175	QUAD-D FF	U19
10	1		8085A	C.P.U.	U18
9	1		2708	PROM	U11
8	3		74LS74	DUAL-D FF	U10,16,17
7	4		74LS08	QUAD 2-IN AND	U9,12,13,15
6	2		8097	TRI-STATE HEX BUFFER	U8,14
5	1		74LS148	8 TO 3 PRIORITY ENCODER	U7
4	2		8216	BI-DIRECTIONAL BUS DRVR	U5,6
3	1		74145	BCD TO DEC. DECODE/DR.	U4
2	1		74LS260	DUAL 5-IN NOR	U3
1	2		74LS373	I.C, OCTAL LATCH, TRI-STATE OUT	U1,2

PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± DECIMALS .X ± .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

DR BY J. Akio 10 JUNE

CHK BY

APPROVED BY

NEXT ASSY | USED ON

APPLICATION

FUTUREDATA

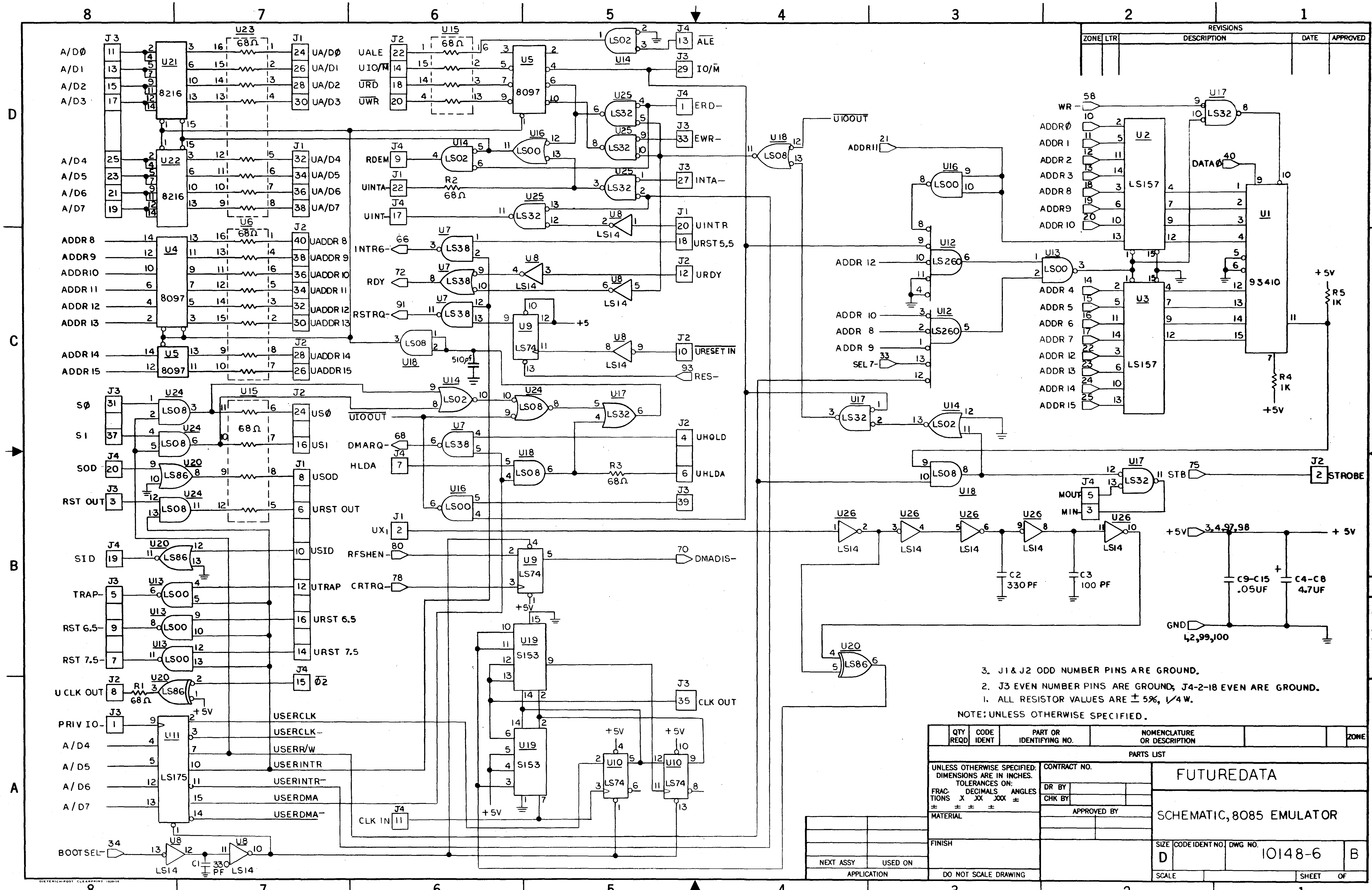
ASSEMBLY, 8085A (CPU)

SIZE	CODE IDENT NO.	DWG NO.	REV
D		10147-5	A

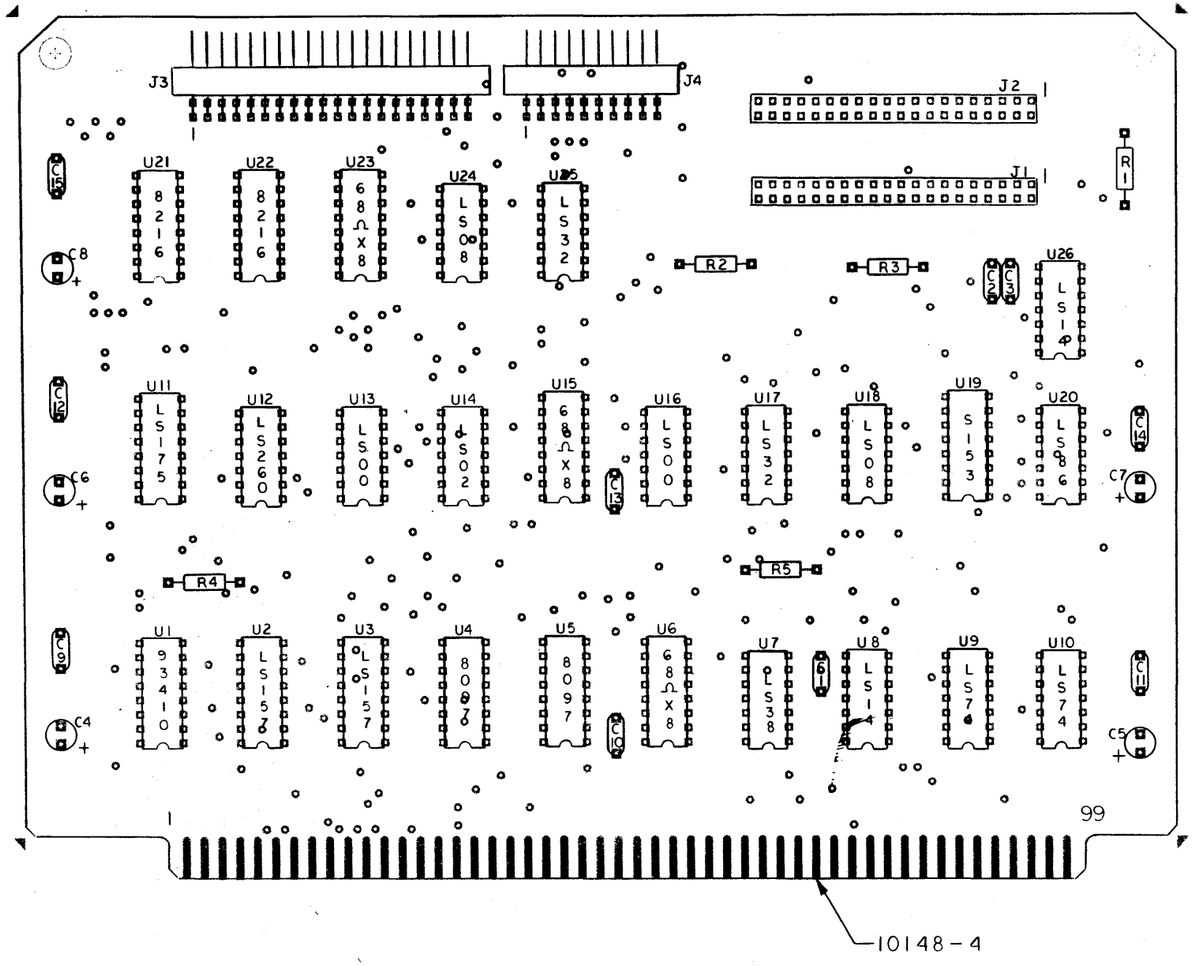
SCALE 2/1 SHEET 1 OF 1

10147-5

DIETZGEN-POST CLEANPRINT 102-13


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
3. J1 & J2 ODD NUMBER PINS ARE GROUND.
2. J3 EVEN NUMBER PINS ARE GROUND; J4-2-18 EVEN ARE GROUND.
1. ALL RESISTOR VALUES ARE ± 5%, 1/4 W.
NOTE: UNLESS OTHERWISE SPECIFIED.
QTY REQD
CODE IDENT
PART OR IDENTIFYING NO.
NOMENCLATURE OR DESCRIPTION
ZONE
PARTS LIST
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON:
FRACTIONS ± DECIMALS X ± XX ± XXX ± ANGLES ±
CONTRACT NO.
DR BY
CHK BY
APPROVED BY
MATERIAL
FINISH
NEXT ASSY
USED ON
APPLICATION
DO NOT SCALE DRAWING
FUTUREDATA
SCHEMATIC, 8085 EMULATOR
SIZE D
CODE IDENT NO.
DWG NO. 10148-6
B
SCALE
SHEET OF
10148-6 A

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



10148-4

ITEM	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REF DES
26	1			CAP, 510 pf CER DISK	
25	1			CAP., 100 pf CER DISK	C3
24	7			CAP. .05 UF CER DISK	C9-15
23	5			CAP., 4.7 UF, 10V TANT	C4-8
22	1		1-87230-0	CONN. 40 PIN RT. ANGLE-AMP	J4
21	1		2-87230-0	CONN. 40 PIN RT. ANGLE-AMP	J3
20	2		2-87227-0	CONN. 40 PIN HEADER-AMP	J1,J2
19	2			RES, 1K, ± 5% 1/4 W	R4,5
18	3			RES, 68Ω, ± 5%, 1/4 W	R1,2,3
17	2			CAP, 330PF CER DISK	C1,2
16	2		8216	I.C., BI-DIRECTION BUS DR	U21,22
15	1		74LS86	QUAD 2-IN EXCLUSIVE OR	U20
14	1		74S153	DUAL, 4 TO 1 SELECT/MUX	U19
13	2		74LS08	QUAD 2-IN AND	U18,24
12	2		74LS32	QUAD 2-IN OR	U17,25
11	1		74LS02	QUAD 2-IN NOR	U14
10	2		74LS00	QUAD 2-IN NAND	U13,16
9	1		74LS260	DUAL 5-IN NOR	U12
8	1		74LS175	QUAD-D FF	U11
7	2		74LS74	DUAL-D FF	U9,10
6	2		74LS14	HEX INV-SCHMITT	U8,26
5	1		74LS38	QUAD 2-IN NAND BUFF O.C.	U7
4	3		898-3-R68	68ΩX8 R-PACK BECKMAN	U6,15,23
3	2		8097	TRI-STATE HEX BUFF.	U4,5
2	2		74LS157	QUAD 2 TO 1 MUX	U2,3
1	1		93410	I.C., 256 BIT RAM	U1

PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± DECIMALS .X ± .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

DR BY

CHK BY

APPROVED BY

NEXT ASSY | USED ON

APPLICATION

FUTUREDATA

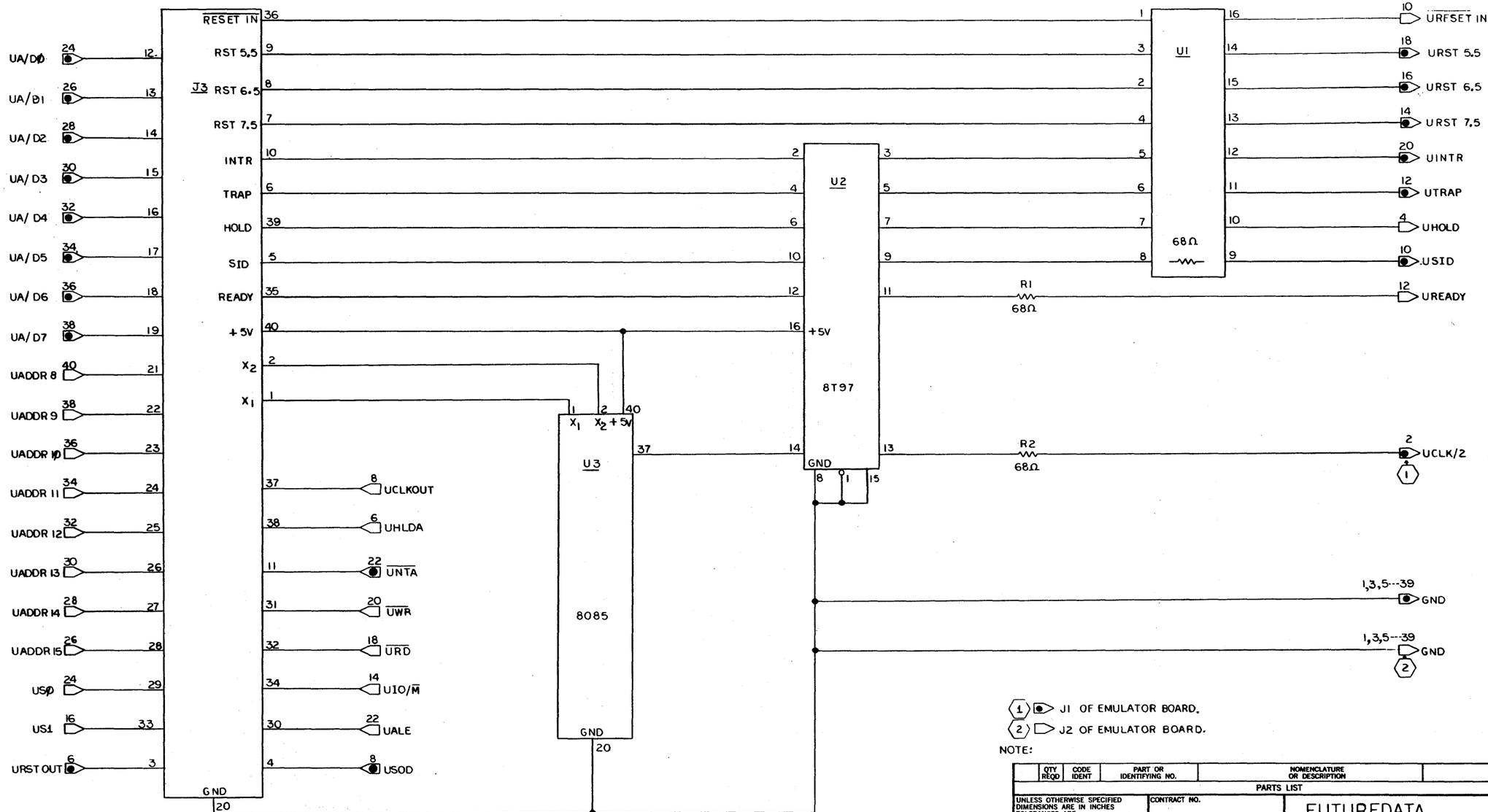
ASSEMBLY, 8085 EMULATOR

SIZE	CODE IDENT NO.	DWG NO.	
D		10148-5	A

SCALE | SHEET OF

10148-5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



1 J1 OF EMULATOR BOARD.

2 J2 OF EMULATOR BOARD.

NOTE:

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN	
CHECKED	

NEXT ASSY | USED ON
APPLICATION

FUTUREDATA

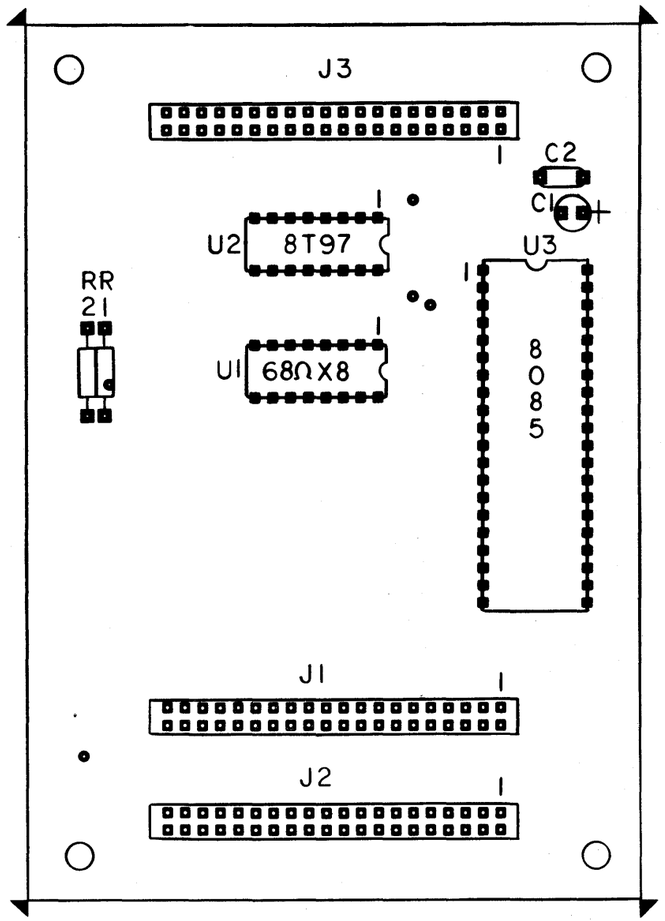
SCHEMATIC, 8085 PROBE

SIZE	CODE IDENT NO.	DRAWING NO.	
D		10149-6	A

SCALE | SHEET OF

10149-6 A

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REF DES
11					
10					
9					
8					
7	3		2-87227-0	CONNECTOR, 40 PIN AMP	J1,2,3
6	2			RES, 68Ω, ±5%, 1/4W	R1, R2
5	1			CAP, .05μf CER DISK	C2
4	1			CAP, 4.7μf, 10V TANT	C1
3	1		8085	I.C., CPU	U3
2	1		8T97	I.C., TRI-STATE HEX BUFF	U2
1	1		898-3-R68	I.C., 68ΩX8 R-PACK-BECKMAN	U1

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J. FAZIO	6-26-78
CHECKED	

FUTUREDATA

ASSEMBLY,
8085 PROBE

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C		10149-5	A

SCALE 2/1 SHEET OF 1

10149-5 A B

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED

ADDR 2 ADDR 3 ADDR 4 ADDR 5 ADDR 6 ADDR 7 ADDR 8 ADDR 9 ADDR 10 ADDR 11 ADDR 12 SEL 6- WR

U13 LS04 U3 S133 J3 PRIVIO- U11 LS175 D2 D1 D0 CLR I/O ENABLE BOOTEN I/O ENABLE- BOOTSEL- 8 X SIP4 INTE- 59

SEL 7 I/O ENABLE- U9 LS08 R6 240Ω Q1 ITT 2N2222 SEL7- 100Ω

16MHZ XTAL1 U26 4024 R2 200 R3 910 +5V

U23 S161 A B C D QC QD

J3 37 Ø OUT J3 39 Ø IN C

96 Ø2 94 2MHZ CLOCK

DMAEN- HLT- DMARQ- 68 3.3K SIP3 U17 LS14 U15 LS74 Ø2 DMA-

J3 31 HALT- INTRQ2- INTRQ1- INTRQ3- INTRQ5- INTRQ7- INTRQØ- INTRQ4- INTRQ6- SIP4 X 3 SIP2-10X X2 SIP4

72 RDY SIP4 X 4

+5V 35 VCC STANDBY N.C. 38 XTAL NMI- IRQ- HALT- U18 6802 BA 7 37 Q2 39 EXTAL 40 RESET- 34 R/W 5 VMA

DMAEN U19 S74 ADS U9 LS08 J3 7 BA

U22 S04 Ø2 U13 LS04

U1 LS374 U2 LS374 A Ø A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 ADS DMAEN ADDR Ø ADDR 1 ADDR 2 ADDR 3 ADDR 4 ADDR 5 ADDR 6 ADDR 7 ADDR 8 ADDR 9 ADDR 10 ADDR 11 ADDR 12 ADDR 13 ADDR 14 ADDR 15

SIP1 U4 U12 74145 MC SEL Ø- SEL 1- SEL 2- SEL 3- SEL 4- SEL 5- SEL 6- SEL 7- 680Ω PULL-UP

U5 U6 LS173 LD ØD DO R/W RD DMAEN SIP2 DATA Ø DATA 1 DATA 2 DATA 3 DATA 4 DATA 5 DATA 6 DATA 7 3.3K PULL-UP

U7 LS373 U8 8098 U10 2708 PGM RDT- D7 D6 D5 D4 D3 D2 D1 DØ

SIP3 RD- WR- R/W- DEN- MEM- I/O-

R4 15K CR1 IN914 C1 33UF 10V R5 15K U17 LS14 C2 .001 R7 15K U28 LS123 >6 μs U22 S04

SEL7 ADDR12 BOOTEN ADDR11 U13 LS04 U21 LS20 U14 LS00 BOOT BTRD RAM EN- J3 35 SIP4 U13 LS04

STB DMA- DMA SIP4 91 RESRQ- BOOTRQ- U9 LS08 U20 LS74 U19 S74 BOOTSEL- 10X SIP4 34 6 SIP4 93 RES-

R9 20K C4 20pf U28 230ms LS123 BOOT MC U25 LS74 ADS Ø2 U14 LS00 MEM- IO- C5 330pf U17 LS14 Ø0 ØD U16 LS08 VMA R/W MO MT M U24 LS174 CLR

R1 1/2W 130Ω CR2 IN5231B C6 4.7μF -12V 5V 7,8

+5V 3.3K BTRD I/O ENABLE SEL7 ADDR12 680Ω LS20 X

3,4,97,98 +5V C7 .05 C19 C20 4.7UF C25 GND 1,2,99,100

5,6 +12V C26 10UF 25V

R8 20K 20pf C3 U27 170ms 74123 R10 5.1K 50ms

2. J3 EVEN NUMBERED PINS ARE GROUND.
1. ALL RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.

NOTES: UNLESS OTHERWISE SPECIFIED.

DIST CODE

NEXT ASSY.	USED ON	DRAWN		
		CHECKED	R.D.Y.	10-27-78
		APPROVED		
MATERIAL		1. TOLERANCES ANGULAR XX ± ± XXX ± 2. BREAK ALL SHARP EDGES APPROX. 3. ALL MACH. SURFACES 4. ALL DIMS IN INCHES 5. FILLET RADII		
FINISH				

futuredata

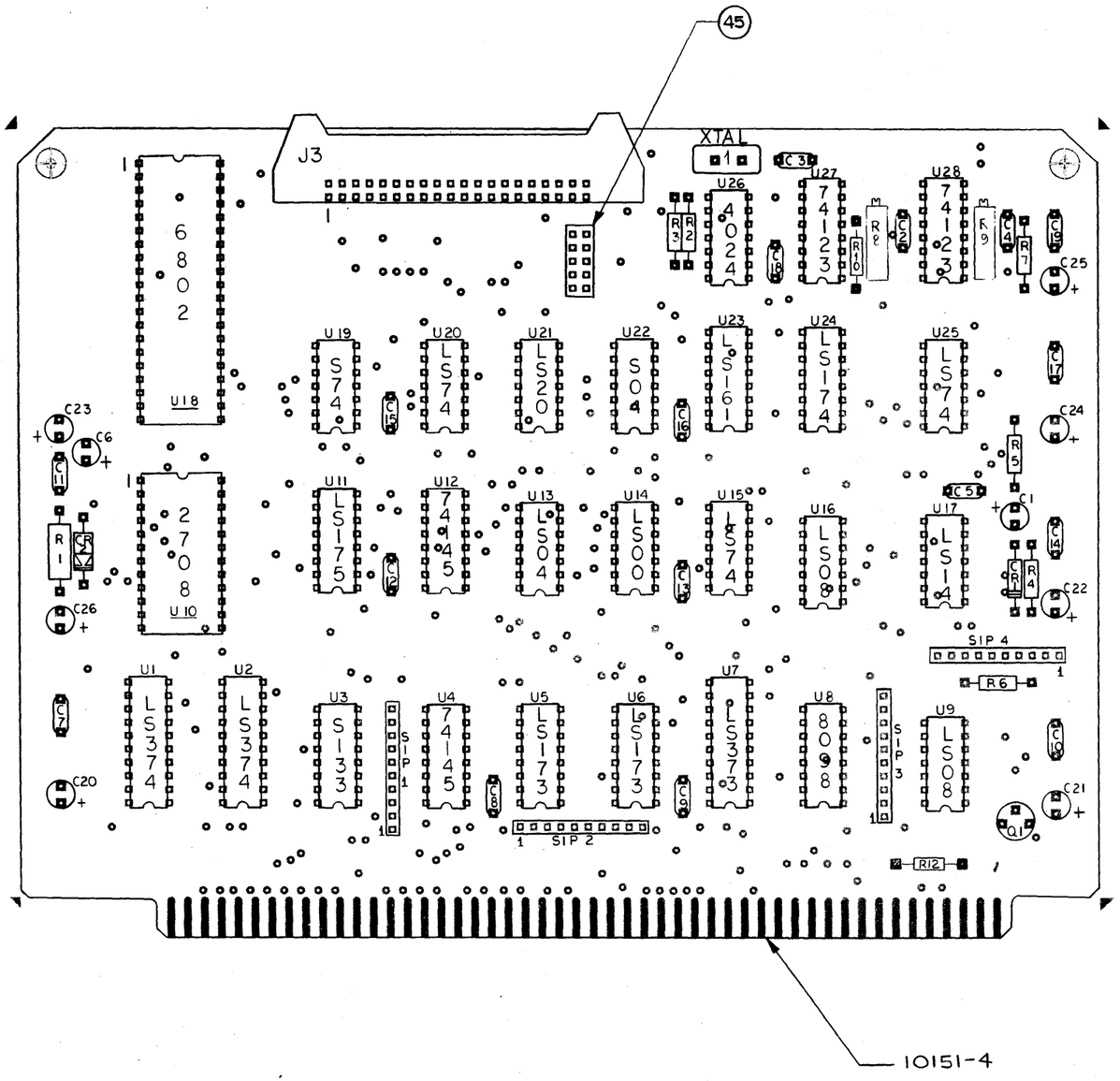
TITLE: SCHEMATIC, 6802 CPU

SIZE	CODE	DRAWING NO.	REV.
D		10151-6	B

SCALE | SHEET

10151-6 | A | B

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



ITEM NO.	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REF DES
47					
46	1		3432-1002	CONNECTOR-40 PIN (3M	J3
45	1		0-87227-5	CONNECTOR-10 PIN (AMP)	
44	1			CRYSTAL, 16 MHZ	XTAL1
43	1		2N2907	TRANSISTOR PNP	Q2,3
42	1		2N2222	TRANSISTOR, NPN	Q1
41	3		4310R-101-332	RES NETWK, 3.3K (BOURNS)	SIP2,3,4
40	1		4310R-101-681	RES NETWK, 680Ω (BOURNS)	SIP1
39	1		1N5231B	DIODE, ZENER	CR2
38	1		1N914	DIODE, SIGNAL	CR1
37	1			RES., 620Ω, 5%, 1/4W	R11
36	1			RES., 5.1K, 5%, 1/4W	R10
35	2			RES., POT 20K 20 TURN	R8,9
34	1			RES., 1K, 5%, 1/4 W	R6
33	3			RES., 15K, 5%, 1/4 W	R4,5,7
32	1			RES., 910Ω, 5%, 1/4W	R3
31	1			RES., 200Ω, 5%, 1/4W	R2
30	1			RES., 130Ω, 5%, 1/2W	R1
29	1			CAP., 10μf, 25V TANT	C26
28	13			CAP., .05μf CER DISK	C7-19
27	7			CAP., 4.7μf, 10V TANT	C6,20-25
26	1			CAP., 330pf CER DISK	C5
25	1			RES., 100Ω, 5%, 1/4W	R12
24	2			CAP., 20pf CER DISK	C3,4
23	1			CAP., .001μf CER DISK	C2
22	1			CAP., 33μf, 10V TANT	C1
21	2		74123	I.C., MONOSTABLE VIBRATOR	U27,28
20	1		4024	CRYSTAL OSC	U26
19	1		74LS174	HEX D FF	U24
18	1		74LS161	SYNCHRO 4-BIT CNTR	U23
17	1		74S04	HEX INVERTER	U22
16	1		74LS20	DUAL 4-IN NAND	U21
15	1		74S74	DUAL-D FF	U19
14	1		6802	CPU	U18
13	1		74LS14	SCHMITT HEX INV	U17
12	3		74LS74	DUAL D FF	U15,20,25
11	1		74LS00	QUAD 2-IN NAND	U14
10	1		74LS04	HEX INVERTER	U13
9	1		74LS175	QUAD D FF	U11
8	1		2708	PROM	U10
7	2		74LS08	QUAD 2-IN AND	U9,16
6	1		8098	3-STATE HEX BUFF-INV	U8
5	1		74LS373	OCTAL LATCH 3-ST OUT	U7
4	2		74LS173	4 BIT D-REG W/3-STATE OUT	U5,6
3	2		74145	BCD TO DECIMAL DRIVER	U4,12
2	1		74S133	13-IN NAND	U3
1	2		74LS374	I.C., OCTAL-FF-3-ST	U1,2

PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± | DECIMALS .X ± .XX ± .XXX ± | ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

DR BY L. Sasio 19 JUL 78

CHK BY R. Yuthasin 2-19-9

APPROVED BY

NEXT ASSY | USED ON

APPLICATION

FUTUREDATA

ASSEMBLY, 6802 CPU

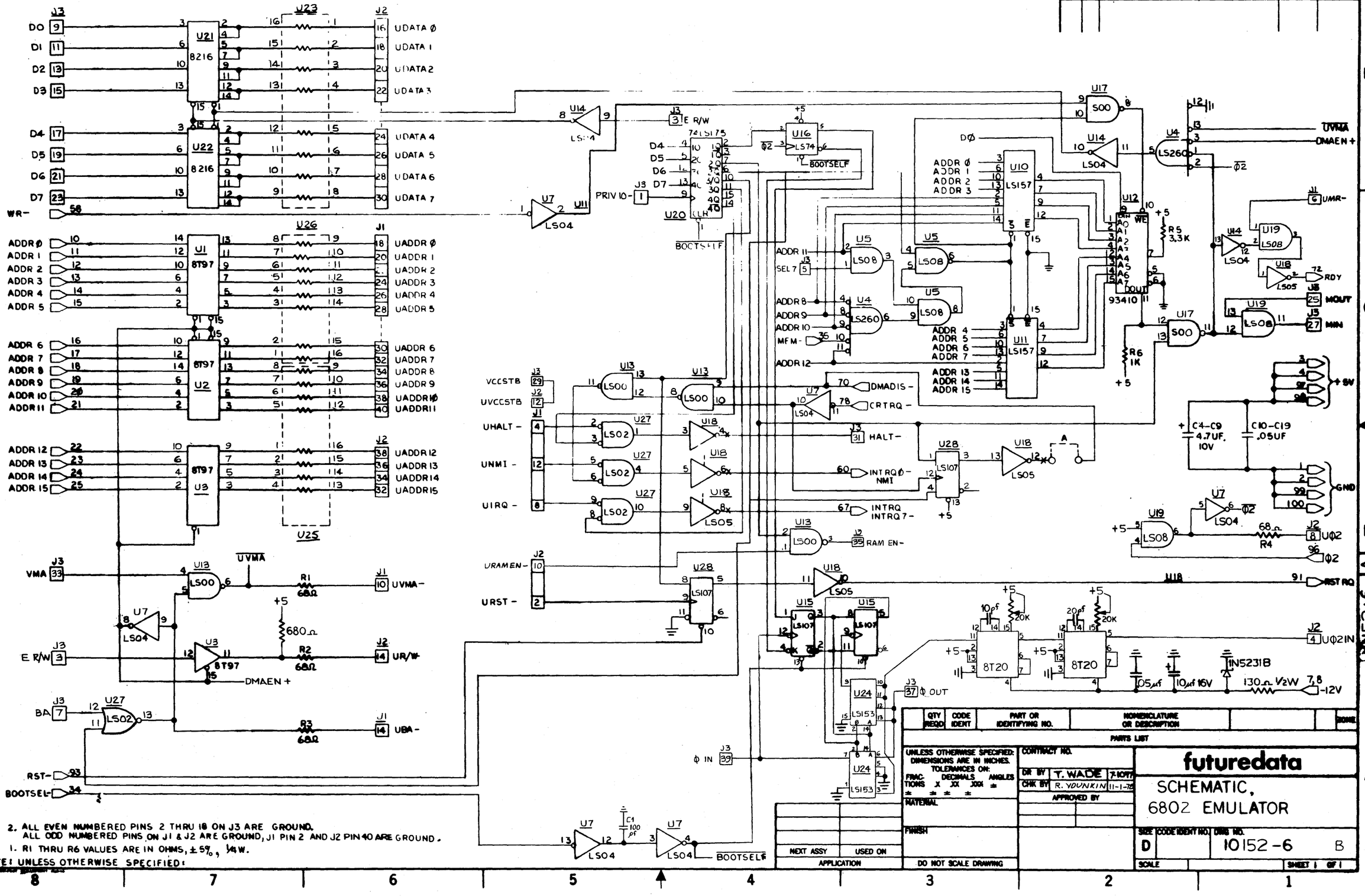
SIZE	CODE IDENT NO.	DWG NO.	REV.
D		10151-5	A

SCALE 2/1 | SHEET 1 OF 1

10151-5 | A

DIETZGEN-POST CLEARPRINT 122x10

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



2. ALL EVEN NUMBERED PINS 2 THRU 18 ON J3 ARE GROUND.
ALL ODD NUMBERED PINS ON J1 & J2 ARE GROUND, J1 PIN 2 AND J2 PIN 40 ARE GROUND.
1. RI THRU R6 VALUES ARE IN OHMS, ±5%, ¼W.

NOTE: UNLESS OTHERWISE SPECIFIED:

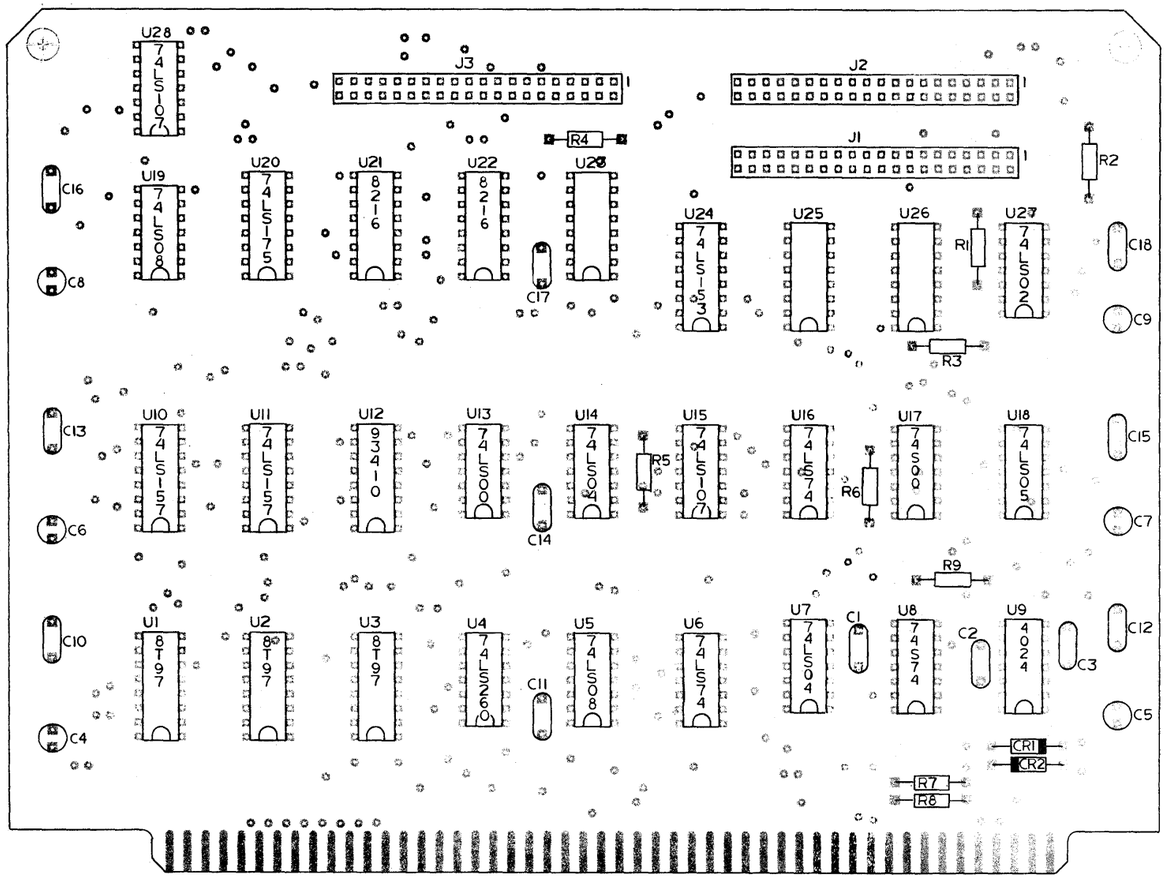
QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION			ZONE

PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRAC. ± / DECIMALS .X ± / .XX ± / .XXX ± / ANGLES ±	CONTRACT NO.	futuredata
	DR BY T. WADE 7-10-77	SCHEMATIC, 6802 EMULATOR
	CHK BY R. YOUNKIN 11-1-78	
MATERIAL	APPROVED BY	
FINISH		SIZE D · CODE IDENT NO. · DWG NO. 10152-6 · B
NEXT ASSY · USED ON		SCALE · SHEET 1 OF 1
APPLICATION	DO NOT SCALE DRAWING	

10152-6 B

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	.		



	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REF DES
31	3		2-87227-0	CONN. 40 PIN HEADER-AMP	J1,2,3
30	1			RES, 240Ω ±5% ¼W	R9
29	1			RES, 2K ±5% ¼W	R8
28	1			RES, 150Ω ±5% ¼W	R7
27	1			RES, 1K ±5% ¼W	R6
26	1			RES, 3.3K ±5% ¼W	R5
25	4			RES, 68Ω ±5% ¼W	R1-4
24	2			DIODE,	CR1,2
23	9			CAP, .05 UF CER DISK	C10-18
22	6			CAP, 4.7 UF 10V TANT	C4-9
21	1			CAP, .002 UF CER DISK	C3
20	1			CAP, 30 PF CER DISK	C2
19	1			CAP, 100 PF CER DISK	C1
18	1		74LS02	I.C., QUAD 2-IN NOR	U27
17	1		74LS153	4 LINE TO 1 MUX	U24
16	3		898-3-R68	68Ω X8 R-PACK BECKMAN	U23,25,26
15	2		8216	BI-DIRECTIONAL BUS DR	U21,22
14	1		74LS175	HEX QUAD D FF	U20
13	1		74LS05	HEX INVERTER O.C.	U18
12	1		7400	QUAD 2-IN NAND	U17
11	2		74LS107	DUAL J-K FLIP FLOP	U15,28
10	1		74LS00	QUAD 2-IN NAND	U13
9	1		93410	256 BIT RAM	U12
8	2		74LS157	QUAD 2 TO 1 MUX	U10,11
7	1		4024		U9
6	1		7474	DUAL D FLIP FLOP	U8
5	2		74LS04	HEX INVERTER	U7 14
4	2		74LS74	DUAL D-FLIP FLOP	U6,16
3	2		74LS08	QUAD 2-IN AND	U5,19
2	1		74LS260	DUAL 5-IN NOR	U4
1	3		8T97	I.C., TRI STATE HEX BUFFER	U1,2,3

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± DECIMALS .X ± .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

DR BY

CHK BY

APPROVED BY

future data

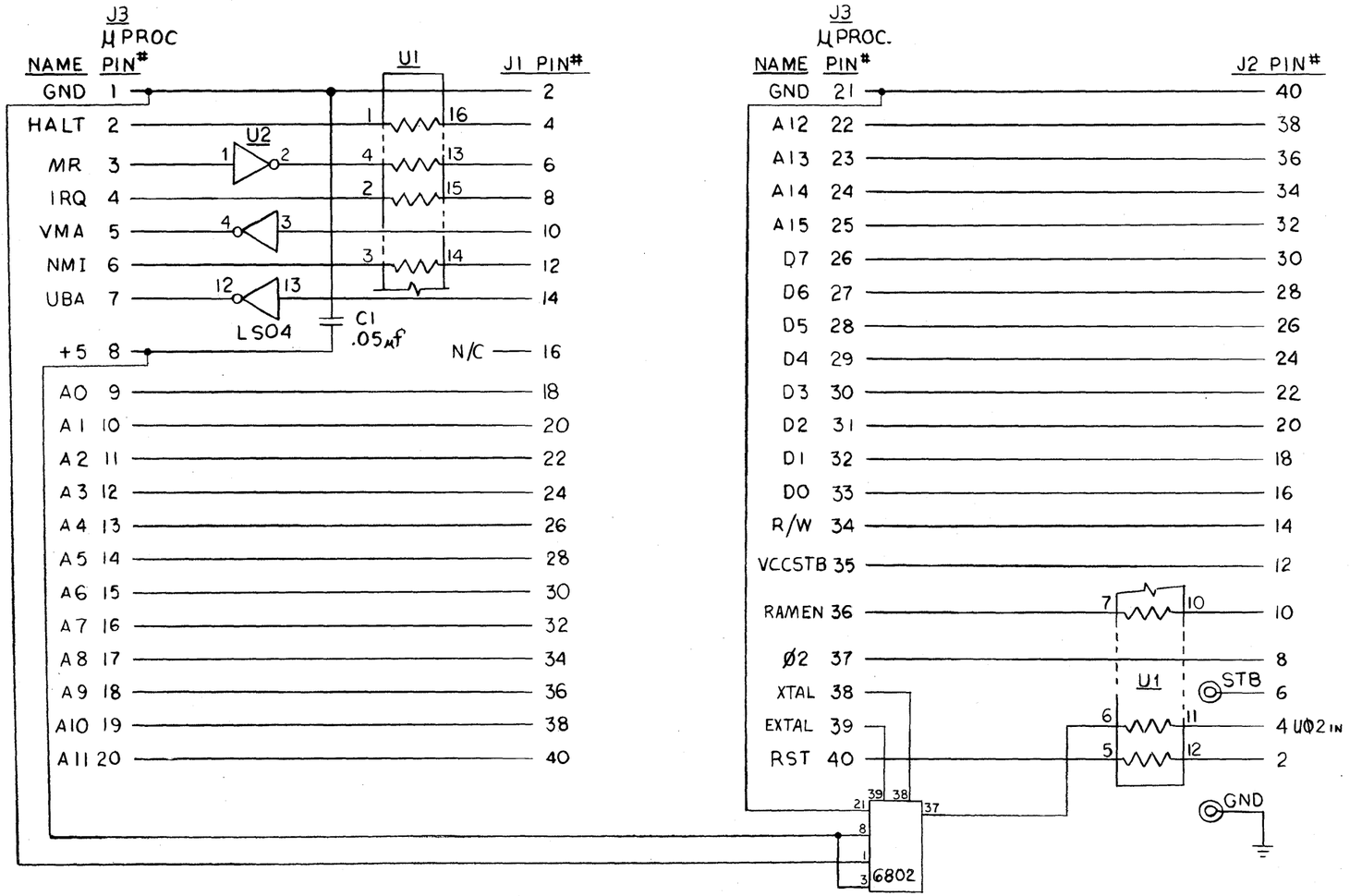
ASSEMBLY 6802 EMULATOR M8-40/6802

SIZE	CODE IDENT NO.	DWG NO.	
D		10152-5	A

SCALE 2/1 SHEET 1 OF 1

10152-5 A

DIETZGEN-POST CLEARPRINT 10Q-10



2. UI RESISTORS ARE 68 Ω'S TYPICAL.
1. ALL ODD NUMBERED PINS ON J1 & J2 ARE GROUND.

NOTES: UNLESS OTHERWISE SPECIFIED.

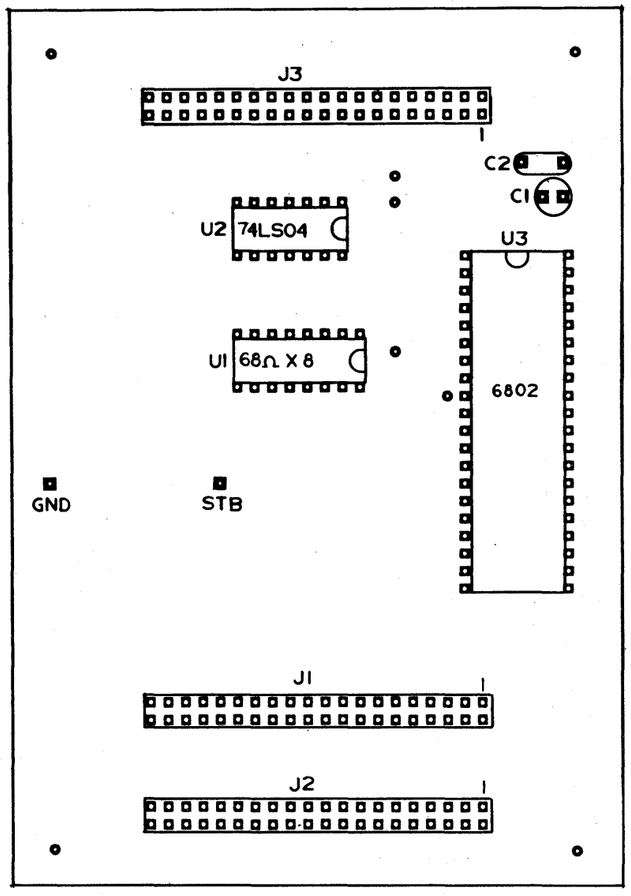
R. YOUNKIN 4-10-79

SCHEMATIC,
6802 PROBE

10153-6 C

10153-6 C SCH

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A			



7					
6	3		2-87227-0	CONN 40 PIN AMP	J1,2,3
5	1			CAP. .05UF CER DISK	C2
4	1			CAP. 4.7UF 10V TANT	C1
3	1		6802	I.C., MICROPROCESSOR	U3
2	1		74LS04	I.C., HEX INVERTER	U2
1	1		898-3-R68	I.C., 68Ω X 8 R-PACK BECKMAN	U1
	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REF DES

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN	
CHECKED	

futuredata

ASSEMBLY
6802 PROBE

SIZE	CODE IDENT NO.	DRAWING NO.	
C		10153-5	A

SCALE 2/1 SHEET 1 OF 1

10153-5 A

RECEIVED AUG 28 1978

			MS	PROTO RELEASE
			MS	PROD. RELEASE
ALL	B	4824	MS	CHG C12 TO 32-00333-000
ALL	C	4937	MS	SEE ECO
	D	5010	MS	SEE ECO
	E	5044	MS	SEE ECO
	F	5257	JB	ADDED R9 PIN NOS
	G	5496	JB	ADDED C18
	H	5850A	MS	SEE ECO

.156 CENTER/0 DIN, DUAL R/O EDGE CONNECTOR

+5 R14 10K

C14 220 pf 28-00221-004

Z12 20-04592-014 (SEE 36-0693 FOR CODES)

RX2-7 52 53 54 35 36 37 17 18 13 14 1 19 69 70 12
RX2-6 4 6 8 9 10 11 12 2
RX2-5 3 5 7 68
RX2-8 22 24 25 26 27 28 32 71
RX2-3 55 21 23 43 45 46 29 30 50 31 20 34
RX2-2 41 42 44 62 47 49 51
RX2-4 39 40 58 60 63 48 66 33 38 15
56 57 59 61 72 64 65 67 16

Z13

C12 (.33μf) 32-00333-000

Z10 9334

C13 390PF 28-00391-004

680 R10

R16, 33K RX2-8

C17

R1 24K

C2 .001 (28-00102-004)

LS 123 Z1

Z8 UNUSED GATES: 7400, 7400, 7400

STB

Z3 10

FR

Z9

ETCH TIED FOR NKRO

R3 680

R4 1.5M

R6 130

R5 33K

CR1 21-04148

C3 .1μf 28-00109-001

Z2

Z8 7400

Z3 10

3.3K R7

32-00103 C5 .01

E1 E2 E3 E4 E5 E6

Z11 04

SLI

AKD

KRO

Z9 37

R15 130

SHIFT LOCK LED CR3 21-057152-000

CUSTOM SELECTIVE AUTO REPEAT PROM

8574 PROM Z4

8574/3601 PROM Z6

8574/3601 PROM Z5

1702A PROM Z7

ETCH TIED JUMPERS

ADDRESS (8 PLCS)

R8 3.3K (8 PLCS) RX1

RX1-1
RX1-2
RX1-3
RX1-4
RX1-7
RX1-6
RX1-5

STB

E STROBE (5-15 μSEC)
F STROBE

CR2 21-52258-000

R9 470

C1 .1μf 37-01203

C7 .01 32-0103

(5 PLCS) C8, C9, C10, C11, C16, C18

4	B1
3	B2
2	B3
1	B4
8	B5
7	B6
6	B7
5	B8
10, A	
9, B	
C, D	

JUL 10 1978

[6] MATRIX NOS 7-70-69-19-18-17-37-36 .01
35-54-53-52 NOT APPLICABLE TO 007 ASSY

[5] INSTALL JUMPER E1 TO E6 IF BIT 8 OF CUSTOM ENCODING PROMS IS TO PROGRAM AUTO REPEAT. INSTALL E1 TO E2, E3, OR E5 FOR DESIRED AUTO REPEAT SCHEME PROGRAMMED BY 8574 PROM.

[4] INSTALL IF USING 3601 PROMS

[3] INSTALL THESE COMPONENTS IF USING 1702A PROM.

[2] TO USE THIS PROM FOR CUSTOM CODING, CUT TRACES (8 PLCS) WHICH TIED A0 TO O1, A1 TO O2, ECT ON CIRCUIT SIDE OF 1702A PROM.

NOTES:

REPT. DLY. – 650 m.SEC ±30 %
REPT. RATE – 10 HZ ±3) % (PERIOD = 80-133 MS)

ETP 38-0763

KTC STD (ASI OF 55-01449)

SCHEMATIC 35-01660

KEYBOARD MODULE 10083-6

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

220Ω/330Ω TERMINATION

FROM POD

1. J1-1 TO 47ODD & J2 1-39ODD ARE GND.
NOTE: UNLESS OTHERWISE SPECIFIED.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS | DATE

DRAWN

CHECKED

NEXT ASSY | USED ON

APPLICATION

FUTUREDATA

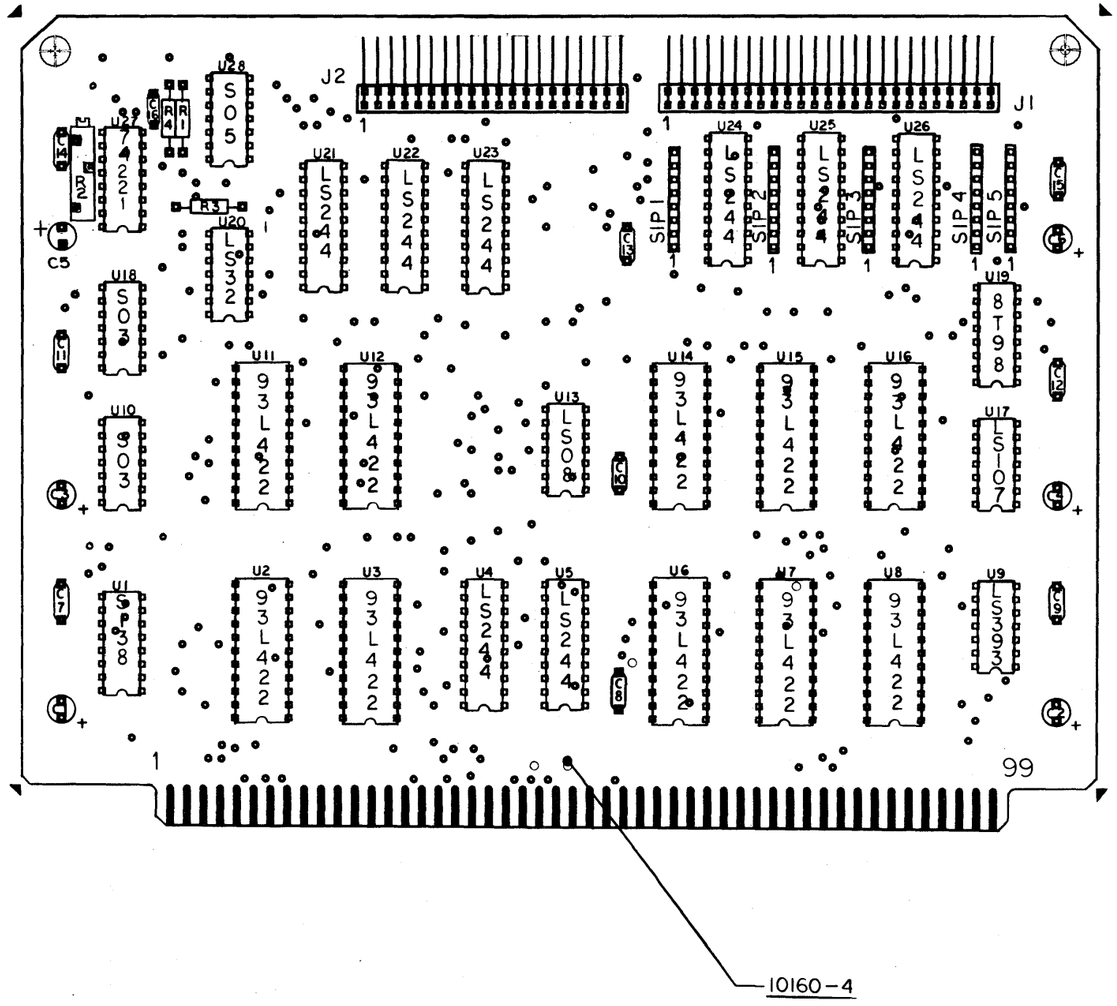
SCEMATIC, ANALYZER A

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		10160-6	B

SCALE | SHEET 1 OF 1

9-09101 B

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A			



ITEM No.	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REF DES
	1			CAP, 20pf CER DISK	C16
26	2	3M	3425	50 PIN CONNECTOR	
25	1			5' 50-COND CABLE	
24	10			22-PIN SOCKET	
23	8			20-PIN SOCKET	
22	3			16-PIN SOCKET	
21	7			14-PIN SOCKET	
20	1			RES., 20K POT (BOURNS)	R2
19	1		2-87230-0	CONN. 40 PIN RT. ANGLE-AMP	J2
18	1		2-87230-5	CONN. 50 PIN RT. ANGLE-AMP	J1
17	5	BOURNS	4308R-103-221/331	RES NETWK, 220/330Ω TERM.	SIP1-5
16	1			RES., 200Ω, 5%, 1/4W	R4
15				RES., 20K, 5%, 1/4W	R3
14	1			RES., 680Ω, 5%, 1/4W	R1
13	9			CAP, .05μf CER DISK	C7-15
12	6			CAP, 4.7μf, 10V TANT	C1-6
11	1		74S05	I.C., HEX INVERTER O.C.	U28
10	1		74221	DUAL, MONOSTABLE VIBRT	U27
9	1		74LS32	QUAD 2-IN OR	U20
8	1		8T98	TRI-STATE, HEX BUFF, INV	U19
7	1		74LS107	DUAL J-K FF	U17
6	1		74LS08	QUAD 2-IN AND	U13
5	2		74S03	QUAD 2-IN NAND O.C.	U10,18
4	1		74LS393	DUAL 4-BIT COUNTER	U9
3	8		74LS244	OCTAL BUS DRIVER 3ST.	U4,5,21-26
2	10		93L422XC	256X4 RAM	U2,3,6-8,11,12,14-16
1	1		74S138	I.C., DECODE/DEMUX	U1

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± .X ± .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

DR BY J. Fazio 12-8-8

CHK BY [illegible] 5-19-9

APPROVED BY

FUTUREDATA

ASSEMBLY, ANALYZER A

SIZE	CODE IDENT NO.	DWG NO.	REV
D		10160-5	B

SCALE 2:1 SHEET OF

10160-5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

220Ω/330Ω TERMINATION

FROM POD

1. J1-1 TO 490DD & J2 1-390DD ARE GND.
NOTE: UNLESS OTHERWISE SPECIFIED.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN	
CHECKED R. Yamben	4-2-79

FUTUREDATA

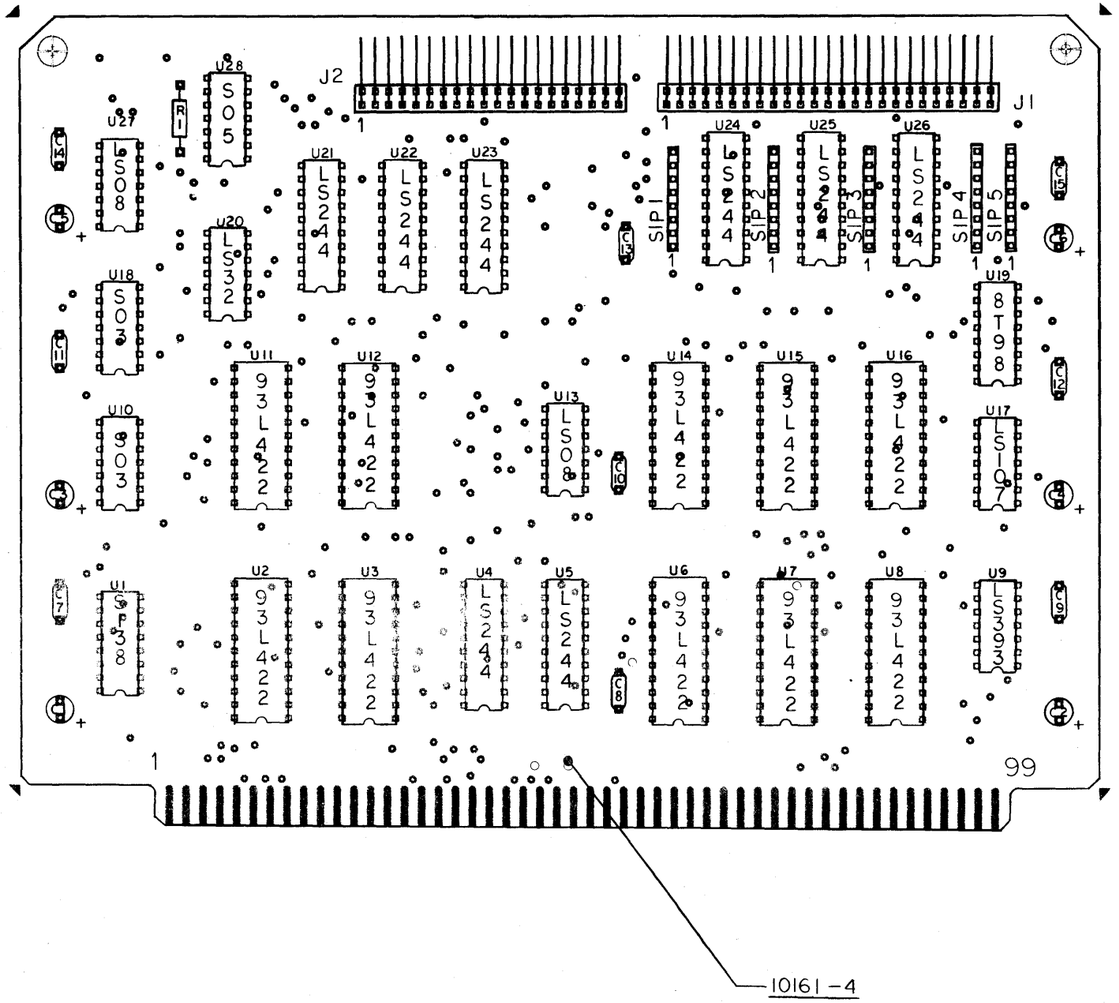
SCEMATIC, ANALYZER B

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		10161-6	B

SCALE | SHEET 1 OF 1

10161-6 R1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A			



ITEM No.	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REF DES
26					
25	2	3M	3425	50 PIN CONNECTOR	
24	1			5' 50-COND FLAT CABLE	
23	10			22-PIN SOCKET	
22	8			20-PIN SOCKET	
21	2			16-PIN SOCKET	
20	8			14-PIN SOCKET	
19	1		2-87230-0	CONN. 40 PIN RT. ANGLE-AMP	J2
18	1		2-87230-5	CONN. 50 PIN RT. ANGLE-AMP	J1
17	5	BOURNS	4308R-103-221/331	RES NETWK, 220/330Ω TERM.	SIP1-5
16					
15					
14	1			RES., 680Ω, 5%, 1/4W	R1
13	9			CAP., .05μf CER DISK	C7-15
12	6			CAP., 4.7μf, 10V TANT	C1-6
11	1		74S05	I.C., HEX INVERTER O.C.	U28
10	1				
9	1		74LS32	QUAD 2-IN OR	U20
8	1		8T98	TRI-STATE, HEX BUFF, INV	U19
7	1		74LS107	DUAL J-K FF	U17
6	1		74LS08	QUAD 2-IN AND	U13,27
5	2		74S03	QUAD 2-IN NAND O.C.	U10,18
4	1		74LS393	DUAL 4-BIT COUNTER	U9
3	8		74LS244	OCTAL BUS DRIVER 3ST.	U4,5,21-26
2	10		93L422XC	256X4 RAM	U2,3,6-8,11,12,14-16
1	1		74S138	I.C., DECODE/DEMUX	U1

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± | DECIMALS .X ± .XX ± .XXX ± | ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

DR BY J. Fazio 12-9-8

CHK BY M. Brandin 1-11-9

APPROVED BY

FUTUREDATA

ASSEMBLY, ANALYZER B

SIZE	CODE IDENT NO.	DWG NO.	REV
D		10161-5	A

SCALE 2:1 SHEET 1 OF

10161-5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

NOTE: UNLESS OTHERWISE SPECIFIED:
1. J2 1 TO 39 ODD ARE GND.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN	
CHECKED	4-2-79

FUTUREDATA

SCHEMATIC, ANALYZER C

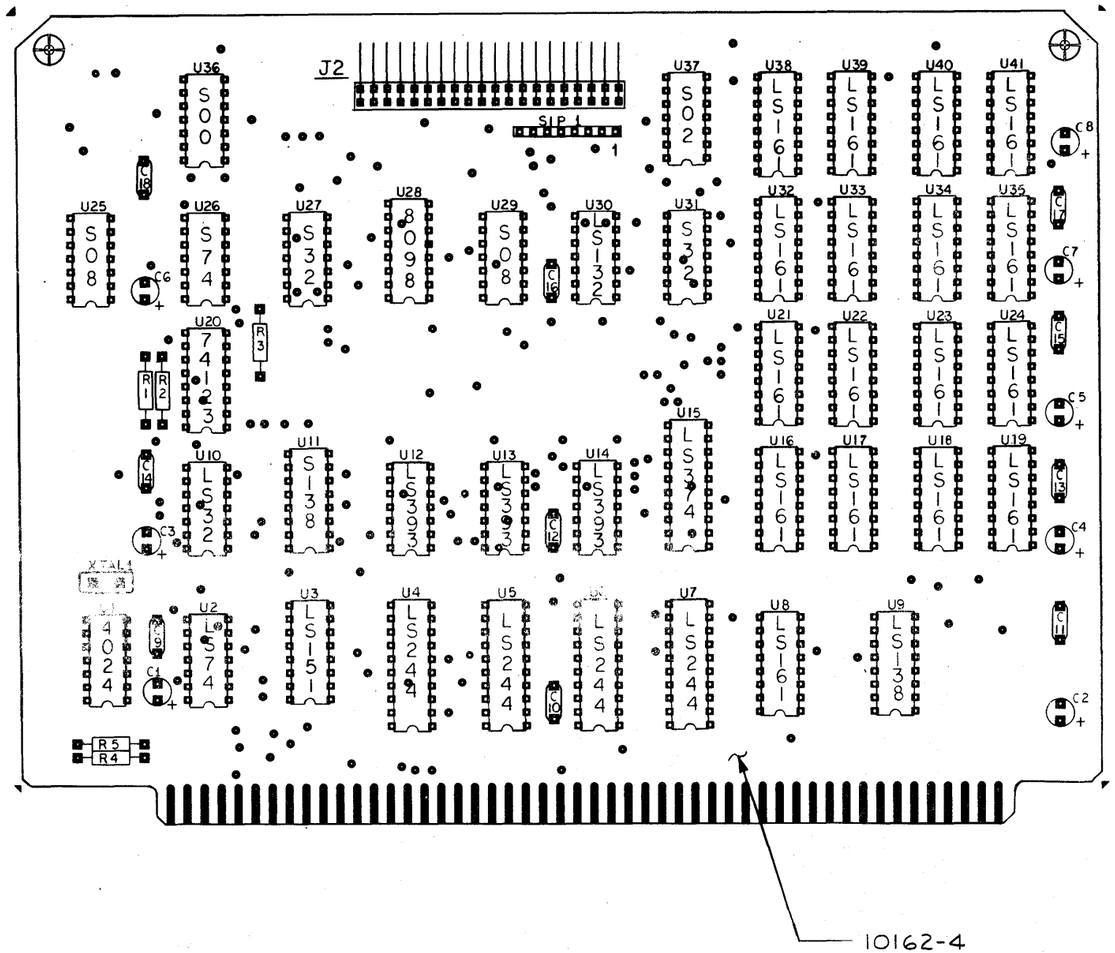
SIZE	CODE IDENT NO	DRAWING NO.	REV
D		10162-6	B

SCALE | SHEET

10162-6 | B

BISHOP GRAPHICS/ACCUPRESS REORDER NO. 20505

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



ITEM No.	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	
26	1		2-87230-0	CONN. 40 PIN RT. ANGLE-AMP.	J2
25	1			CRYSTAL 20 MHZ	XTAL 1
24	1	BOURNS	4308R-10322/331	RES NETWK, 220 330Ω TERM	SIP 1
23	1			RES., 910Ω 5% ¼ W	R5
22	1			RES., 200Ω 5% ¼ W	R4
21	3			RES., 5.1K, 5% ¼W	R1-3
20	10			CAP, .05μf CER DISK	C9-18
19	8			CAP, 4.7μf 10V TANT	C1-8
18	1		74S02	I.C., QUAD 2-IN NOR	U37
17	1		74S00	QUAD 2-IN NAND	U36
16	1		74LS132	QUAD 2-IN NAND-SCHMITT	U30
15	1		8098	INV 3ST. HEX BUFF	U28
14	2		74S32	QUAD 2-IN OR	U27,31
13	1		74S74	DUAL-D FF	U26
12	2		74S08	QUAD 2-IN AND	U25,29
11	1		74123	DUAL, MONOSTABLE VIBRT.	U20
10	1		74LS374	OCTAL D FF 3ST.	U15
9	3		74LS393	DUAL 4-BIT COUNTER	U12,13,14
8	1		74S138	DECODE, DEMUX	U11
7	1		74LS32	QUAD 2-IN OR	U10
6	1		74LS138	DECODE, DEMUX	U9
5	17		74LS161	SYNC. 4-BIT COUNTER	U8, 16-24, 32-35, 38-41
4	4		74LS244	OCTAL BUS DRIVER 3ST.	U4,5,6,7
3	1		74LS151	DATA SEL, MUX	U3
2	1		74LS74	DUAL-D FF	U2
1	1		4024	I.C., CRYSTAL OSC	U1

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± .X ± .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

DR BY J. Fazio 24 JAN 78

CHK BY

APPROVED BY

FUTUREDATA

ASSEMBLY, ANALYZER C

SIZE	CODE IDENT NO.	DWG NO.	REV.
D		10162-5	B

SCALE 2/1 SHEET 1 OF 1

10162-5 B

DIETRICH-POST CLEARPRINT 150/10

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

SIP1 680Ω PIN 1 = +5V

NOTE: UNLESS OTHERWISE SPECIFIED.

1. J4 PINS 20 THRU 46, 48, 50, & ODD PINS 1 THRU 19 ARE GND.
2. J2, J3 & J5 ALL EVEN PINS ARE GND. J1 & J6 ALL ODD PINS ARE GND.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION			ZONE

PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± | DECIMALS X ± .XX ± .XXX ± | ANGLES ± ± ±

MATERIAL

FINISH

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CONTRACT NO.

DR BY

CHK BY R. Yamashiro 3-29-79

APPROVED BY

NEXT ASSY | USED ON

APPLICATION

FUTUREDATA

SCHEMATIC, INTF/POD

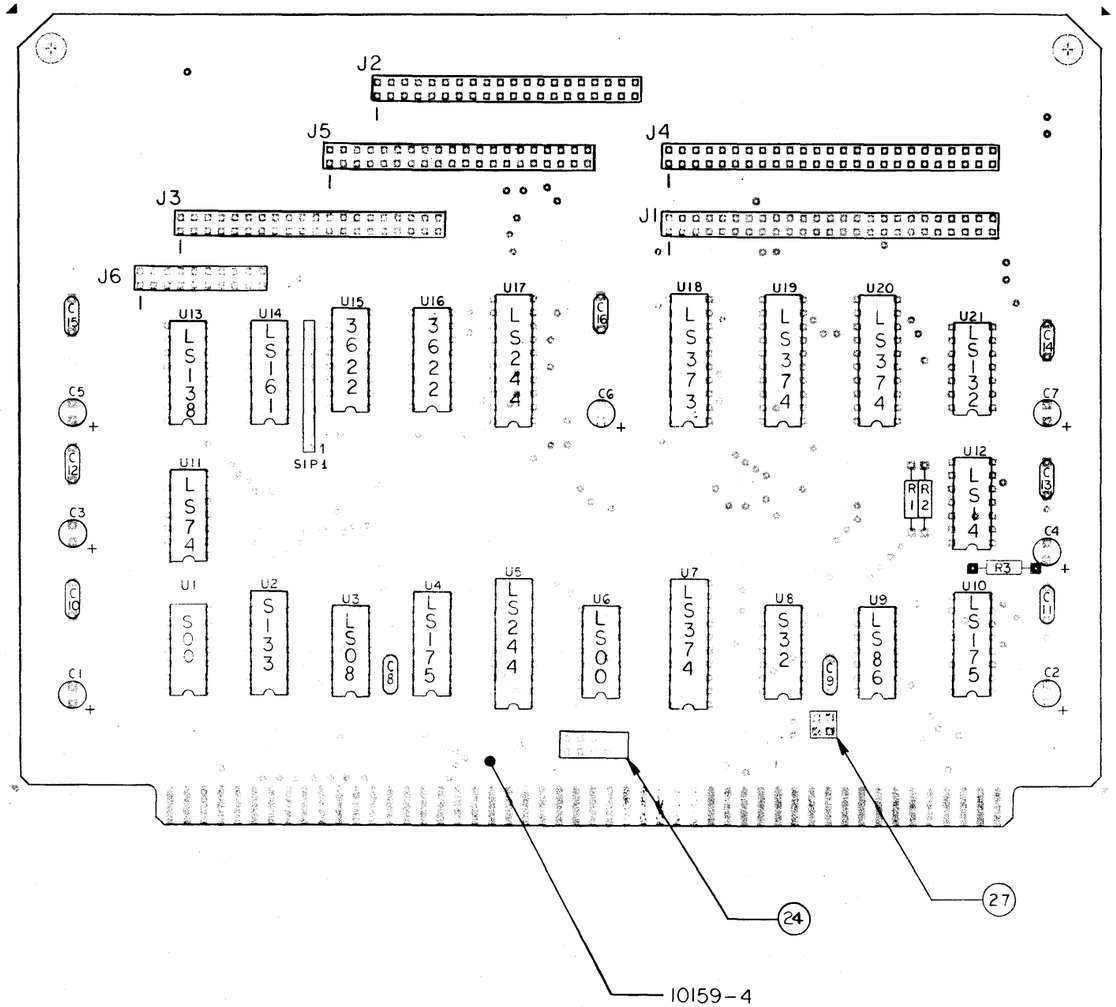
SIZE	CODE IDENT NO.	DWG NO.	REV.
D		10159-6	B

SCALE | SHEET OF

10159-6 B

DIETRICH-POST CLEARPRINT 1020-10

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



ITEM No.	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REF DES
27	1			CONN., 4-PIN HEADER (AMP)	
26	1		74S00	IC, QUAD 2-IN NAND	U1
25	1			RES., 3.3KΩ 5% ¼W	R3
24	1		0-87227-5	CONN.,10-PIN HEADER(AMP)	
23	1		1-87227-0	CONN.,20-PIN HEADER(AMP)	J6
22	3		2-87227-0	CONN.,40-PIN HEADER(AMP)	J2,3,5
21	2		2-87227-5	CONN.,50-PIN HEADER(AMP)	J1,4
20	1		4310R-101-681	RES NETWK,680Ω(BOURN)	SIP1
19	1			RES,330Ω,5%,¼W	R2
18	1			RES,200Ω,5%,¼W	R1
17	9			CAP.,.05μf CER DISK	C8-16
16	7			CAP.,4.7μf,10V TANT	C1-7
15	1		74LS132	I.C., QUAD 2-IN NAND S.T.	U21
14	1		74LS373	OCTAL XPARENT D LTCH 3ST	U18
13	2		3622	512X4 PROM	U15,16
12	1		74LS161	BINARY COUNTER,SYNC	U14
11	1		74LS138	DECODE/DEMUX	U13
10	1		74LS14	SCHMITT HEX INVERT	U12
9	1		74LS74	DUAL D FF	U11
8	1		74LS86	QUAD 2-IN EXCLUSIVE OR	U9
7	1		74S32	QUAD 2-IN OR	U8
6	3		74LS374	OCTAL D FF 3 ST	U7,19,20
5	1		74LS00	QUAD 2-IN NAND	U6
4	2		74LS244	OCTAL BUS DRIVER 3ST.	U5,17
3	2		74LS175	QUAD D FF	U4,10
2	1		74LS08	QUAD 2-IN OR	U3
1	1		74S133	I.C.,13-IN NAND	U2

PARTS LIST

10159-5 B

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± .X ± .XX ± .XXX ± ANGLES ±

MATERIAL

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CONTRACT NO.

DR BY J.TA3/0 2-2-79

CHK BY [illegible] 3-29-79

APPROVED BY

NEXT ASSY | USED ON

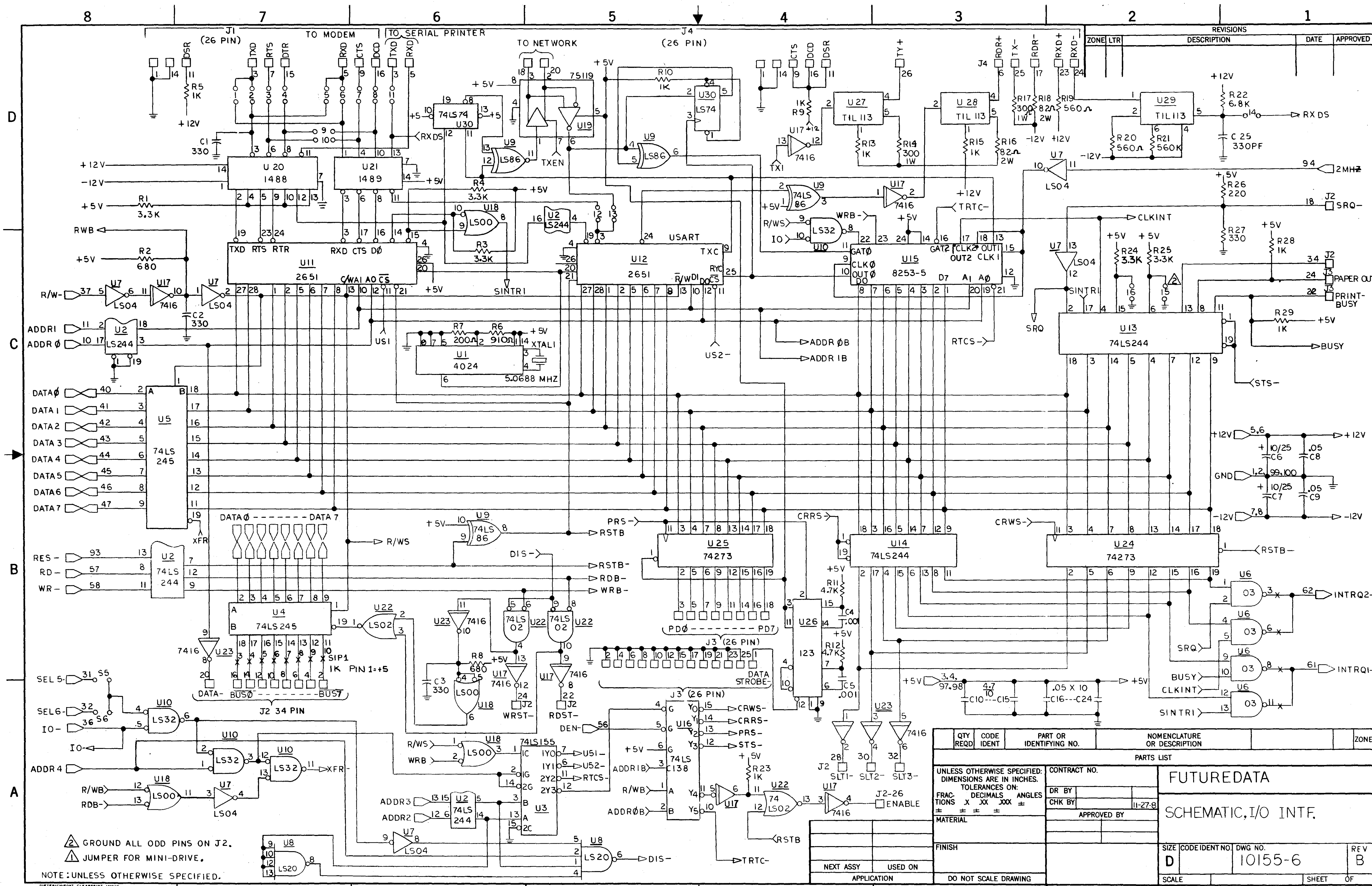
APPLICATION

FUTUREDATA

ASSEMBLY, INTF/POD

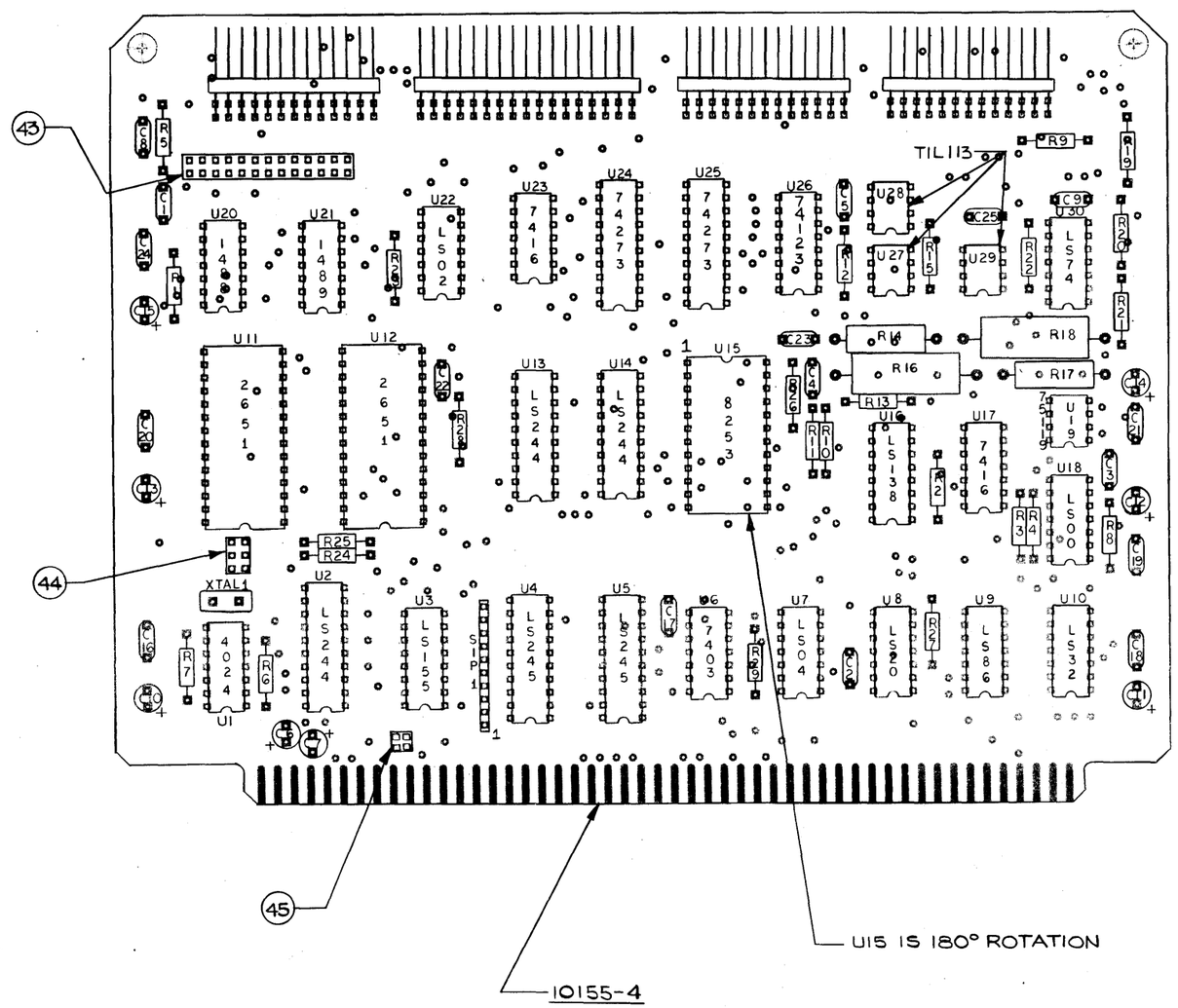
SIZE	CODE IDENT NO.	DWG NO.	REV
D		10159-5	B

SCALE 2/1 SHEET 1 OF 1



FUTUREDATA
SCHEMATIC, I/O INTF.
SIZE D
DWG NO. 10155-6
REV B
10155-6 B
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
QTY REQD | CODE IDENT | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | ZONE
PARTS LIST
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± DECIMALS .X ± .XX ± .XXX ± ANGLES ±
MATERIAL
FINISH
DO NOT SCALE DRAWING
CONTRACT NO.
DR BY
CHK BY 11-27-8
APPROVED BY
NEXT ASSY USED ON
APPLICATION
SCALE SHEET OF
2 GROUND ALL ODD PINS ON J2.
1 JUMPER FOR MINI-DRIVE.
NOTE: UNLESS OTHERWISE SPECIFIED.
J1 (26 PIN) TO MODEM
TO SERIAL PRINTER
J4 (26 PIN)
TO NETWORK
USART
J3 (26 PIN)
J2 34 PIN
5.0688 MHZ
XTAL1
SIP1 1K PIN 1=+5
DATA STROBE

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



ITEM No.	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REF DES
47	1		1-87230-7	CONN., 34 PIN RT ANGLE-AMP	J2
46	3		1-87230-3	CONN., 26 PIN RT ANGLE-AMP	J1,3,4
45	1		87227-2	CONN., 4 PIN HEADER-AMP	
44	1		87227-3	CONN., 6 PIN HEADER-AMP	
43	1		1-87227-3	CONN., 26 PIN HEADER-AMP	
42	1			CRYSTAL, 5.0688 MHZ	XTAL 1
41	1		4310R-101-102	RES NETWK, 1K (BOURNS)	SIP1
40	1			330Ω, ±5%, 1/4W	R27
39	1			220Ω, ±5%, 1/4W	R26
38	1			6.8K, ±5%, 1/4W	R22
37	1			560K, ±5%, 1/4W	R21
36	2			560Ω, ±5%, 1/4W	R19,20
35	2			82Ω, ±5%, 2W	R16,18
34	2			300Ω, ±5%, 1W	R14,17
33	2			4.7K, ±5%, 1/4W	R11,12
32	1			910Ω, ±5%, 1/4W	R6
31	1			200Ω, ±5%, 1/4W	R7
30	8			1K, ±5%, 1/4W	R5,9,10,13,15,23,28
29	2			680Ω, ±5%, 1/4W	R2,8
28	5			RES., 3.3K ±5%, 1/4W	R1,3,4,24,25
27	6			CAP, 4.7μf, 10V TANT	C10-15
26	10			.05μf CER DISK	C8,9,16-24
25	2			10μf, 25V TANT	C6,7
24	2			.001μf CER DISK	C4,5
23	4			CAP, 330 p.f CER DISK	C1,2,3,25
22	1		74LS74	I.C., DUAL-D FF	U30
21	3		TIL113	OPTO ISOLATOR	U27,28,29
20	1		74123	DUAL MONOSTABLE VIBRATOR	U26
19	2		74273	OCTAL-D FF	U24,25
18	1		74LS02	QUAD 2-IN NOR	U22
17	1		1489	QUAD LINE RECEIVER	U21
16	1		1488	QUAD LINE DRIVER	U20
15	1		75119	LINE DR/REC'R TRI-STATE	U19
14	1		74LS00	QUAD 2-IN NAND	U18
13	2		7416	HEX BUFFER, INVERTER, O.C.	U17,23
12	1		74LS138	3 TO 8 DECODE, DEMUX	U16
11	1		8253	COUNTER/TIMER	U15
10	2		2651	PROGRAMMABLE COMM INTF	U11,12
9	1		74LS32	QUAD 2-IN OR	U10
8	1		74LS86	QUAD 2-IN EXCLUSIVE OR	U9
7	1		74LS20	DUAL 4-IN NAND	U8
6	1		74LS04	HEX INVERTER	U7
5	1		7403	QUAD 2-IN NAND O.C.	U6
4	2		74LS245	BI-DIREC. OCTAL BUFFER	U4,5
3	1		74LS155	DUAL 2 TO 4 DECODE, DEMUX	U3
2	3		74LS244	OCTAL BUS DRIVER	U2,13,14
1	1		4024	I.C., CRYSTAL ØSC	U1

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± | DECIMALS .X ± .XX ± .XXX ± | ANGLES ±

MATERIAL

FINISH

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CONTRACT NO.

DR BY J. FAZIO 10-18-78

CHK BY

APPROVED BY

FUTUREDATA

ASSEMBLY, I/O INTF.

SIZE	CODE IDENT NO.	DWG NO.	REV.
D		10155-5	A

SCALE 2/1 SHEET 1 OF 1

10155-5 A

DIETZGEN-POST CLEARPRINT 1038-19

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION		ZONE

PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± DECIMALS .X ± .XX ± .XXX ± ANGLES ± MATERIAL FINISH DO NOT SCALE DRAWING

CONTRACT NO.

DR BY

CHK BY

APPROVED BY

NEXT ASSY | USED ON

APPLICATION

FUTUREDATA

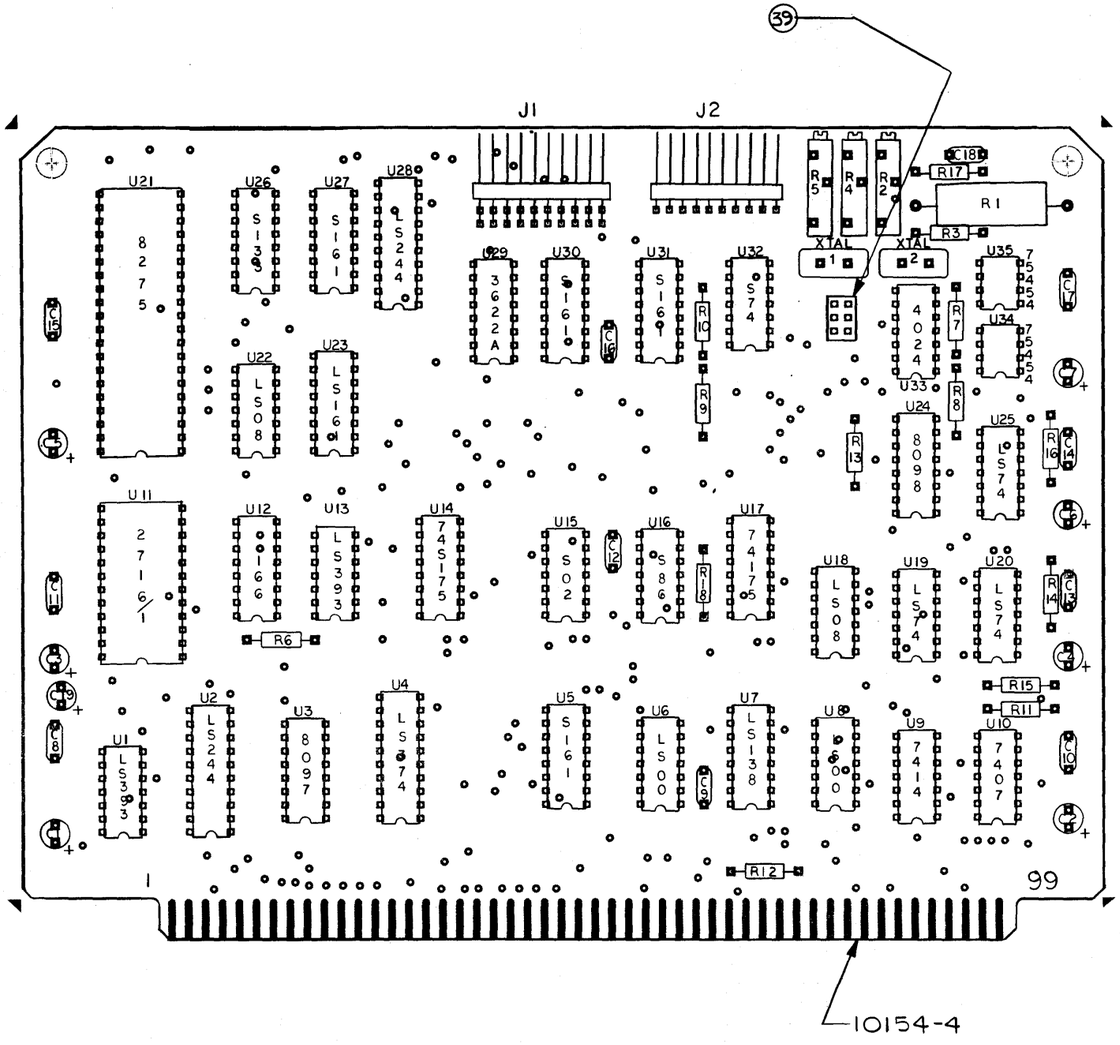
SCHEMATIC, 80 CHARACTER C.R.T.

SIZE	CODE IDENT NO.	DWG NO.	REV
D		10154-6	B

SCALE | SHEET 1 OF 1

10154-6 | B

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



	ITEM No.	QTY REQ'D	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REF DES
	43	1		CRYSTAL, 14.8824	XTAL2
	42	1		CAP, 10UF, 25V (TANT)	C19
	41	1	1-87230-0	CONN. 20 PIN RT ANGLE (AMP)	J1
	40	1	1-87233-0	CONN. 10 PIN RT ANGLE (AMP)	J2
	39	1	87227-3	CONN. 6 PIN HEADER (AMP)	
	38	1		CRYSTAL, 17.85888 MHZ	XTAL1
	37	1		RES, 100Ω, ±5%, 1/4W	R18
	36	1		3.3K, ±5%, 1/4W	R17
	35	2		330Ω, ±5%, 1/4W	R9,10
	34	1		910Ω, ±5%, 1/4W	R8
	33	1		200Ω, ±5%, 1/4W	R7
	32	7		1K, ±5%, 1/4W	R6,11-16
	31	3		500Ω POT (BOURNS)	R4,5,2
	30	1		22Ω, ±5%, 1/4W	R3
	29				
	28	1		RES, 120Ω, ±5%, 2W	R1
	27	11		CAP., .05UF CER DISK	C8-18
	26	7		CAP., 4.7UF, 10V (TANT)	C1-7
	25	1	74LS138	I.C., 3 TO 8 DECODE/DEMUX	U7
	24	2	75454	DUAL PERIPHERAL DRIVER	U34,35
	23	1	4024	CRYSTAL OSC	U33
	22	1	74574	QUAD-D FF	U32
	21	1	3622A	PROM (512X4) TRI-ST O.C.	U29
	20	1	74S133	13-IN NAND	U26
	19	1	8098	TRI-STATE HEX BUFF-INV	U24
	18	1	74LS161	SYNCHRO 4-BIT COUNTER	U30
	17	1	8275	CRT CONTROLLER	U21
	16	3	74LS74	DUAL-D FF	U19,20,25
	15	2	74LS08	QUAD 2-IN AND	U18,22
	14	1	74175	QUAD-D FF	U17
	13	1	74586	QUAD 2-IN EXCLUSIVE OR	U16
	12	1	74502	QUAD 2-IN NOR	U15
	11	1	74S175	QUAD-D FF	U14
	10	1	74166	8 BIT SHIFT REGIS.	U12
	9	1	2716-1	PROM	U11
	8	1	7407	HEX BUFF/DR, O.C.	U10
	7	1	74LS14	HEX INVERTER - SCHMITT	U9
	6	2	74LS00	QUAD 2-IN NAND	U6,8
	5	4	74S161	SYNCHRO 4 BIT COUNTER	U5,23,27,31
	4	1	74LS374	OCTAL D-FF TRI-STATE	U4
	3	1	8097	TRI-STATE HEX BUFF	U3
	2	2	74LS244	OCTAL BUS DRIVER	U2,28
	1	2	74LS393	I.C., DUAL 4-BIT BINARY CTR	U1,13

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± .X ± .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

DR BY JS 9-27-78

CHK BY

APPROVED BY

FUTUREDATA

MS-25

ASSEMBLY, 80 CHARACTER C.R.T.

SIZE	CODE IDENT NO.	DWG NO.	REV
D		10154-5	A

SCALE 2/1 SHEET 1 OF 1

10154-5

DIETZGEN-POST CLEARPRINT 1000-10

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED

WPAL-
WPAH-
WPD-
PDATA Ø+
PDATA 7+
PPRG+
PREAD+
PREAD-
PRED-
+27V
GND
+5
+12
-12
SEL 7-
WR-
ADDR2+
ADDR1+
ADDRØ+
U1 LS138
OUT X'FB'
OUT X'FC'
OUT X'FD'
OUT X'FE'
OUT X'FF'
OUT X'FA'
ADDR4+
ADDR3+
I/O-
U2 LS08
U9 LS04
DATA Ø+
DATA 1+
DATA 2+
DATA 3+
DATA 4+
DATA 5+
DATA 6+
DATA 7+
8216 U3
8216 U4
PRDE-
DEIN
CS
DEN-
HLDA
SEL 7-
RD-
ADDR 2+
ADDR 1+
ADDR Ø+
U8 LS138
RSTAT- IN
RBKPT- IN
PPN- IN
PPF- IN
PRD- IN
PWR- IN
PRDE- IN
M1-
LS193 U20
LS193 U19
TP1
RBKPT-
STB
LS175 U16
LS175 U10
LS175 U12
LS175 U13
LS175 U11
RES
LS85 U17
LS85 U5
LS85 U6
LS85 U18
ADDR Ø+
ADDR 15+
PPN-
PPF-
PRD-
PWR-
U15 LS00
U2 LS08
LS74 U21
LS03 U7
INTRQ6-
8797 U14
DATA Ø+
DATA 1+
RSTAT-
1N914B Typ 6 plc.
100
C1 10uf 25V Typ 6 pls.
1N5245A
1uf 50V
C2
C3
C4
C5
C6
+12
1K
10K
555 U22
.002 C7
.01 C8
-12
3,4,97,98
+5
C9 4.7
C10 4.7
C11 .05
C12 .05
C13 .06
C14 .05
C15 .05
C16 .05
C17 .05
C18 .05
1,2,99,100
GND
C19 10/25
5,6
+12
C20 10/25
C21 .05
7,8
-12

NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY.	USED ON	DRAWN		11/23/71
		CHECKED	BG	5/12/17
		APPROVED		
MATERIAL		1. TOLERANCES ANGULAR XX ± XXX ± ± 2. BREAK ALL SHARP EDGES APPROX. 3. ALL MACH. SURFACES 4. ALL DIMS IN INCHES 5. FILLET RADII		
FINISH				

DIST CODE

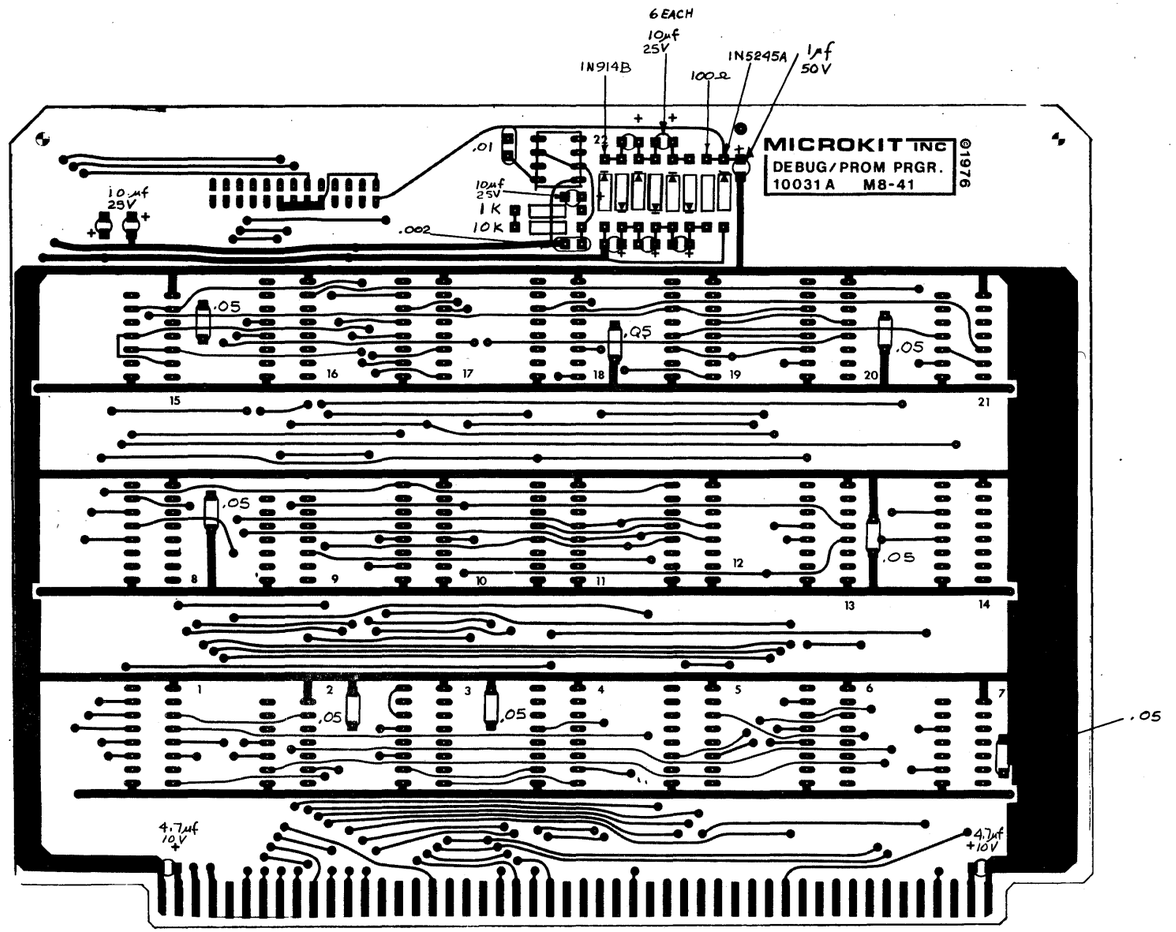
futuredata

TITLE: DEBUG/PROM PRGR. BD.

SIZE	CODE	DRAWING NO.	
D		10031	A

SCALE | SHEET

2/73 DIETERICH-POST CLEARPRINT 1088



U1	74LS138
U2	74LS08
U3	8216
U4	8216
U5	74LS85
U6	74LS85
U7	74LS03
U8	74LS138
U9	74LS04
U10	74LS175
U11	74LS175
U12	74LS175
U13	74LS175
U14	8T97
U15	74LS00
U16	74LS175
U17	74LS85
U18	74LS85
U19	74LS193
U20	74LS193
U21	74LS74
U22	NE555

REVISIONS

ZONE	LAL	REV	DESCRIPTION	CHECK DATE	APPROVED

NEXT ASSY. USED ON — FSM 8-5-76

MATERIAL

FINISH

DIST CODE

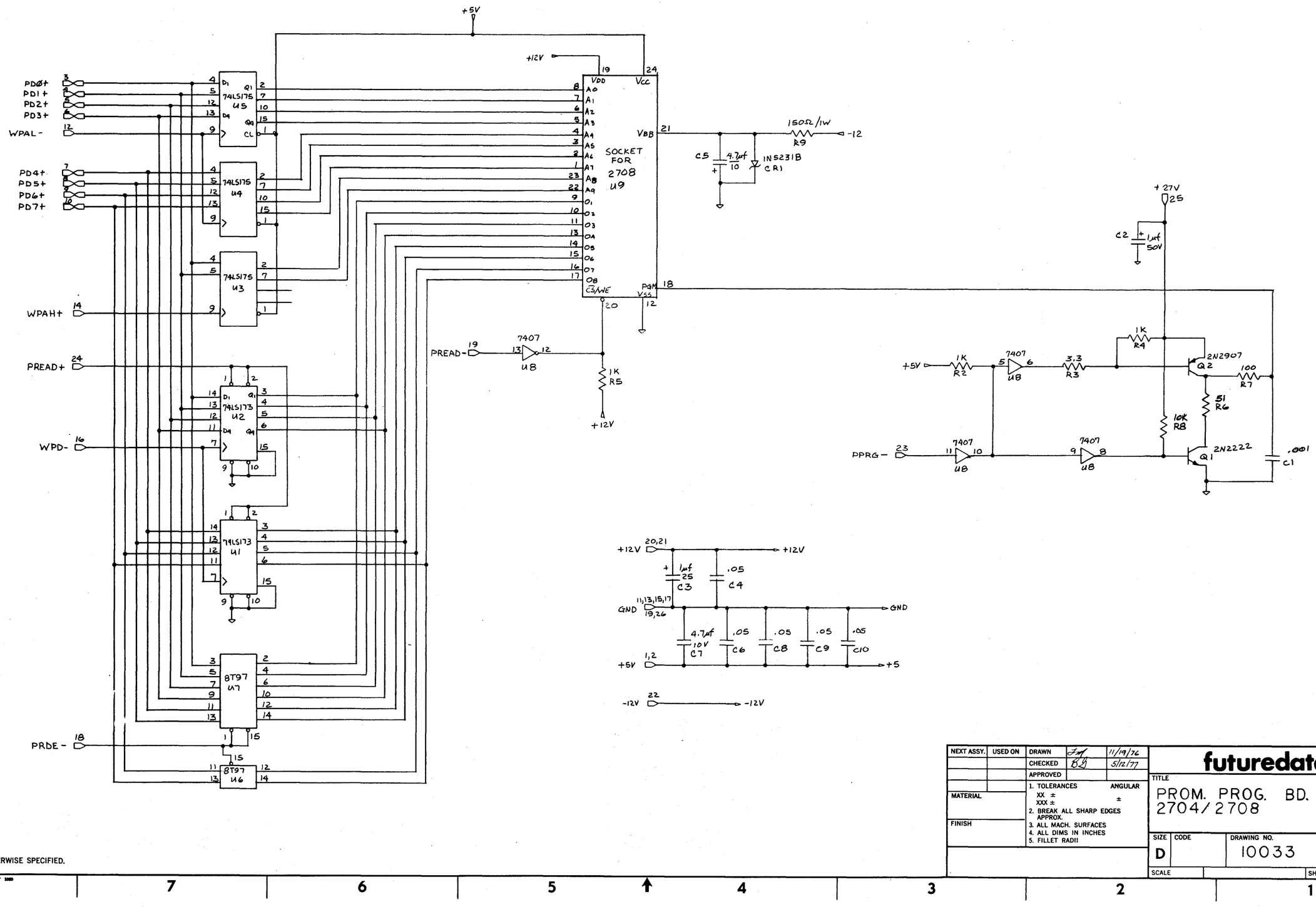
MICROKIT INC.

COMPONENT LAYOUT
DEBUG/PROM PRGR.

D 10031 -3 A

10031-3 A

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED



NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY.	USED ON	DRAWN		11/19/76
		CHECKED	BB	5/12/77
		APPROVED		

1. TOLERANCES ANGULAR
   XX ±
   XXX ± ±
2. BREAK ALL SHARP EDGES APPROX.
3. ALL MACH. SURFACES
4. ALL DIMS IN INCHES
5. FILLET RADII

MATERIAL

FINISH

DIST CODE

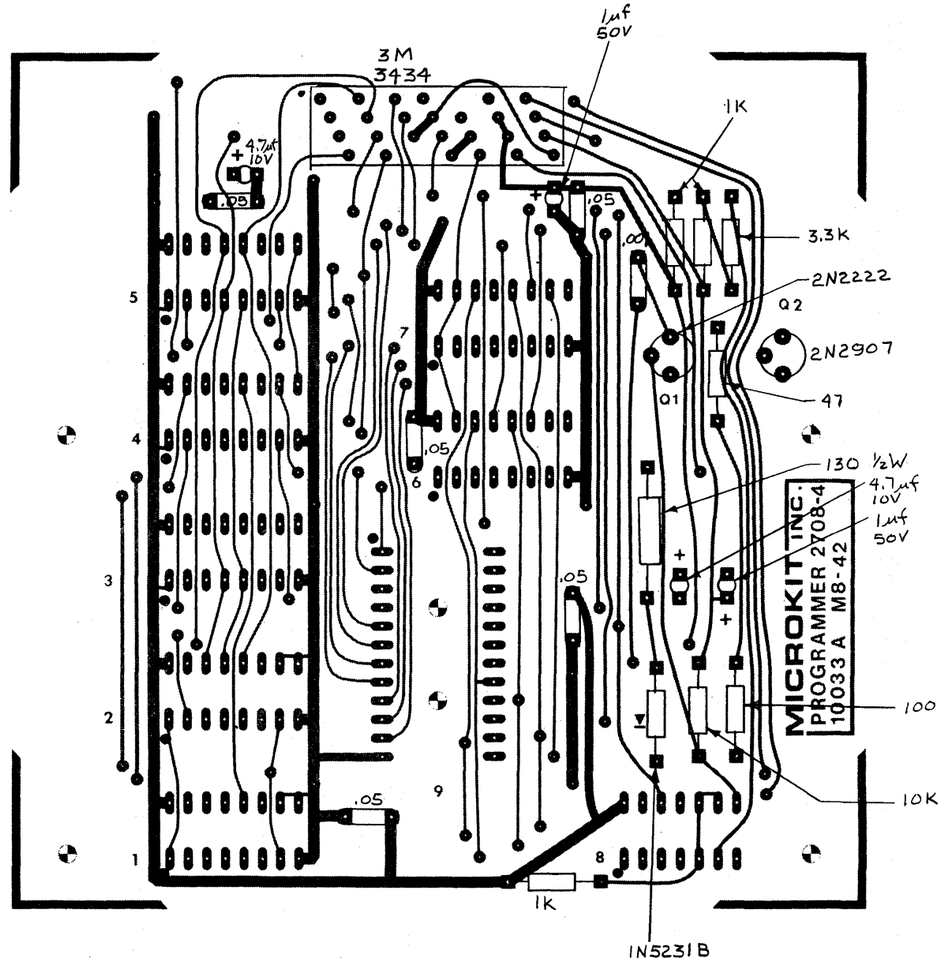
futuredata

TITLE
PROM. PROG. BD.
2704/2708

SIZE	CODE	DRAWING NO.
D		10033 A

SCALE SHEET

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED



NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY.	USED ON	DRAWN	JM	12-1-76
		CHECKED		
		APPROVED		
		1. TOLERANCES		ANGULAR
MATERIAL		XX ±		±
		XXX ±		
FINISH		2. BREAK ALL SHARP EDGES APPROX.		
		3. ALL MACH. SURFACES		
		4. ALL DIMS IN INCHES		
		5. FILLET RADII		

DIST CODE

MICROKIT INC.

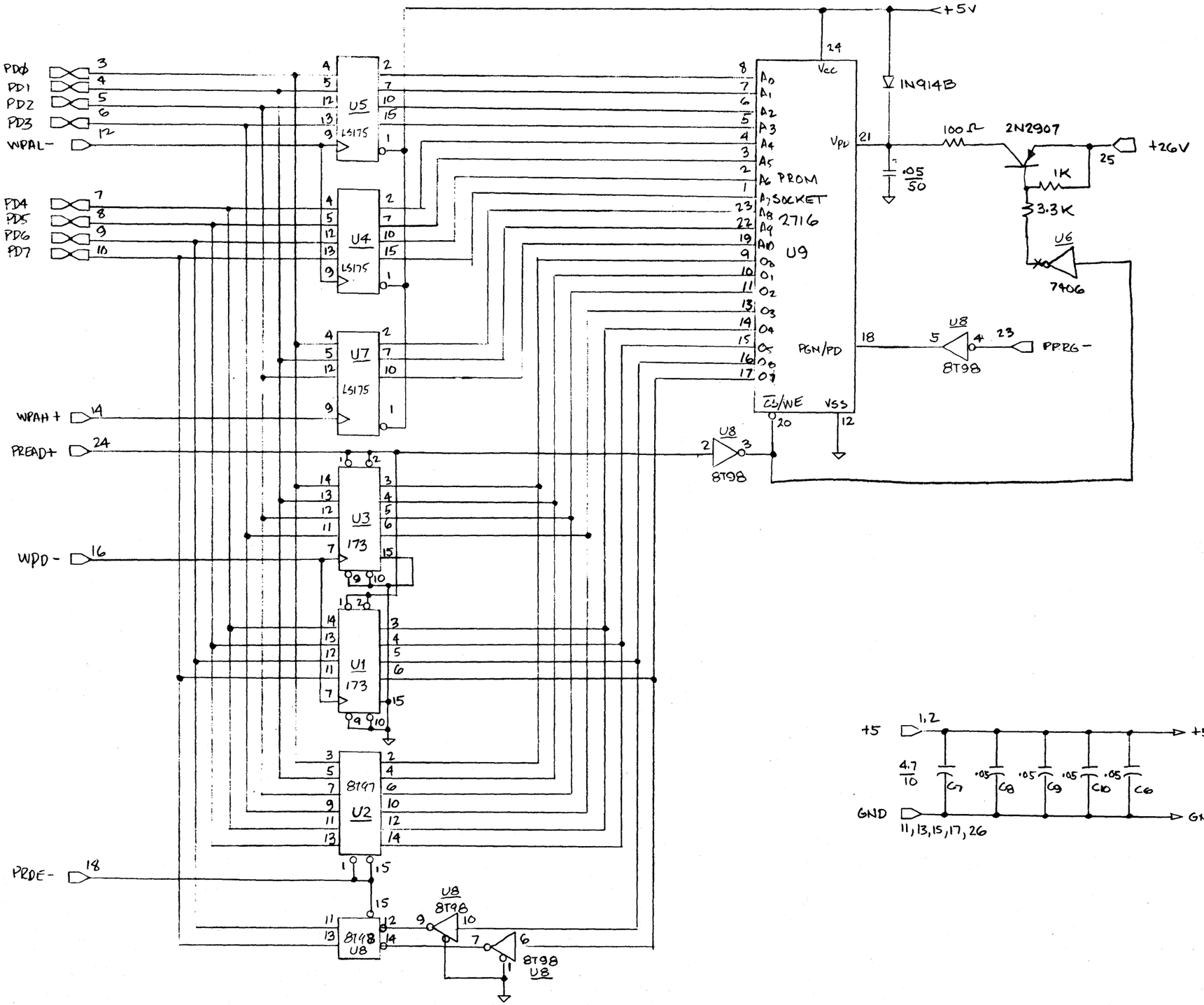
TITLE

PROGRAMMER 2708-4
COMPONENT LAYOUT

SIZE	CODE	DRAWING NO.
C		10033-5 A

SCALE | SHEET

10033-5 A

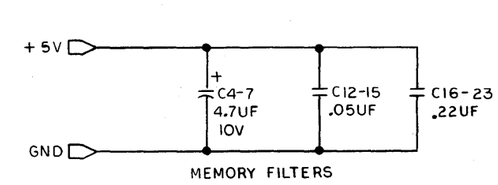


10086-6

2716 PROM PROGRAMMER

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

ROW	PIN	Ø	1	2	3	4	5	6	7
0-3	11	DIØ	DI1	DI2	DI3	DI4	DI5	DI6	DI7
	7	DOØ	DO1	DO2	DO3	DO4	DO5	DO6	DO7
Ø	8	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$
	10	$\overline{CSØ}$	$\overline{CSØ}$	$\overline{CSØ}$	$\overline{CSØ}$	$\overline{CSØ}$	$\overline{CSØ}$	$\overline{CSØ}$	$\overline{CSØ}$
1	8	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$
	10	$\overline{CS1}$	$\overline{CS1}$	$\overline{CS1}$	$\overline{CS1}$	$\overline{CS1}$	$\overline{CS1}$	$\overline{CS1}$	$\overline{CS1}$
2	8	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$
	10	$\overline{CS2}$	$\overline{CS2}$	$\overline{CS2}$	$\overline{CS2}$	$\overline{CS2}$	$\overline{CS2}$	$\overline{CS2}$	$\overline{CS2}$
3	8	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$
	10	$\overline{CS3}$	$\overline{CS3}$	$\overline{CS3}$	$\overline{CS3}$	$\overline{CS3}$	$\overline{CS3}$	$\overline{CS3}$	$\overline{CS3}$



1. ALL RESISTOR VALUES ARE IN OHMS ¼W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED.

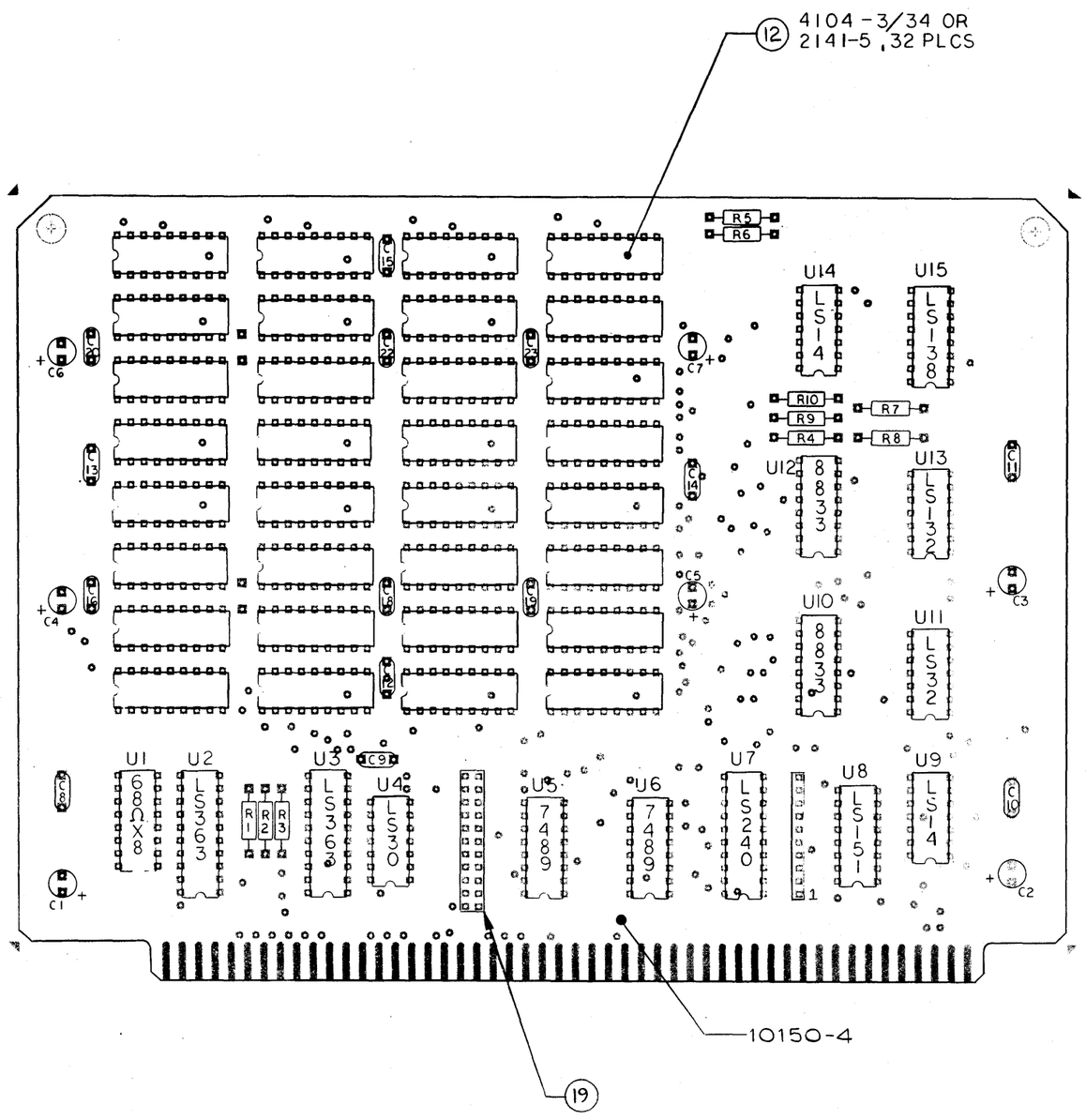
QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION		ZONE
PARTS LIST					

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS X, DECIMALS XX ±, XXX ±, ANGLES ±	CONTRACT NO.	FUTUREDATA	
	DR BY		
	CHK BY A. Yonkers 3-4-9	(M8-15)	
	APPROVED BY	SCHEMATIC, 16K STATIC MEMORY	
MATERIAL			
FINISH		SIZE D / CODE IDENT NO. / DWG NO. 10150-6 / REV C	
NEXT ASSY / USED ON APPLICATION	DO NOT SCALE DRAWING	SCALE / SHEET / OF	

10150-6 C

DIETERICH-POST CLEARPRINT 1020-10

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	C	REVISED AND REDRAWN	5DEC78	



ITEM NO.	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REF DES
23					
22					
21					
20					
19	1		1-87227-1	CONN, 22 PIN HEADER(AMP)	
18	1			RES, 3.3K, ±5%, 1/4W	R3
17	9			RES, 68Ω, ±5%, 1/4W	R1,2,4-10
16	8			CAP, .22μf CER DISK	C16-23
15	8			CAP, .05μf CER DISK	C8-15
14	7			CAP, 4.7μf, 25V TANT	C1-7
13	1		4310R-101-332	SIP, RES NETWK, 3.3K(BOURNS)	SIP1
12	32		4104-3/34 OR 2141-5	I.C., STATIC RAM 4KX1	Ø,Ø/3,7
11	1		74LS138	DECODE, DEMUX	U15
10	1		74LS132	QUAD, 2-IN NAND (SCHMITT)	U13
9	1		74LS32	QUAD, 2-IN OR	U11
8	2		8833	QUAD, 3 ST XCEIVER	U10,12
7	2		74LS14	SCHMITT HEX INVERT	U9,14
6	1		74LS151	DATA SEL, MUX	U8
5	1		74LS240	OCTAL, 3 STATE BUFFER	U7
4	2		7489	64 BIT R/W MEMORY	U5,6
3	1		74LS30	8-IN NAND	U4
2	2		74LS363	OCTAL D-FF, 3 ST. BUFFER	U2,3
1	1		898-3-R68	I.C., 68ΩX8 R-PACK (BECKMAN)	U1

PARTS LIST

10150-5

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

DR BY J.FAZIO

CHK BY

APPROVED BY

FUTUREDATA

ASSEMBLY,
16 K STATIC RAM

SIZE	CODE IDENT NO.	DWG NO.	REV
D		10150-5	C

SCALE 2/1 SHEET 1 OF 1

DILTERICH-FOST CLEARPRINT 1000F

NOTE: CUT SEL 6- ETCH AT P1-32 IF BOARD IS USED IN LOWER 32K RANGE ONLY.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

	1	2	3	4	5	6	7	8
DOØ-7	DOØ	DO1	DO2	DO3	DO4	DO5	DO6	DO7
DIØ-7	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7

1. ALL RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.

NOTE: UNLESS OTHERWISE SPECIFIED:

DIETZGEN-POST CLEARPRINT 1020-10

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION		ZONE

PARTS LIST

NEXT ASSY	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± | .X ± | .XX ± | .XXX ± | ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

DR BY		
CHK BY	RON YOUNKIN	2-21-79
APPROVED BY		

FUTUREDATA

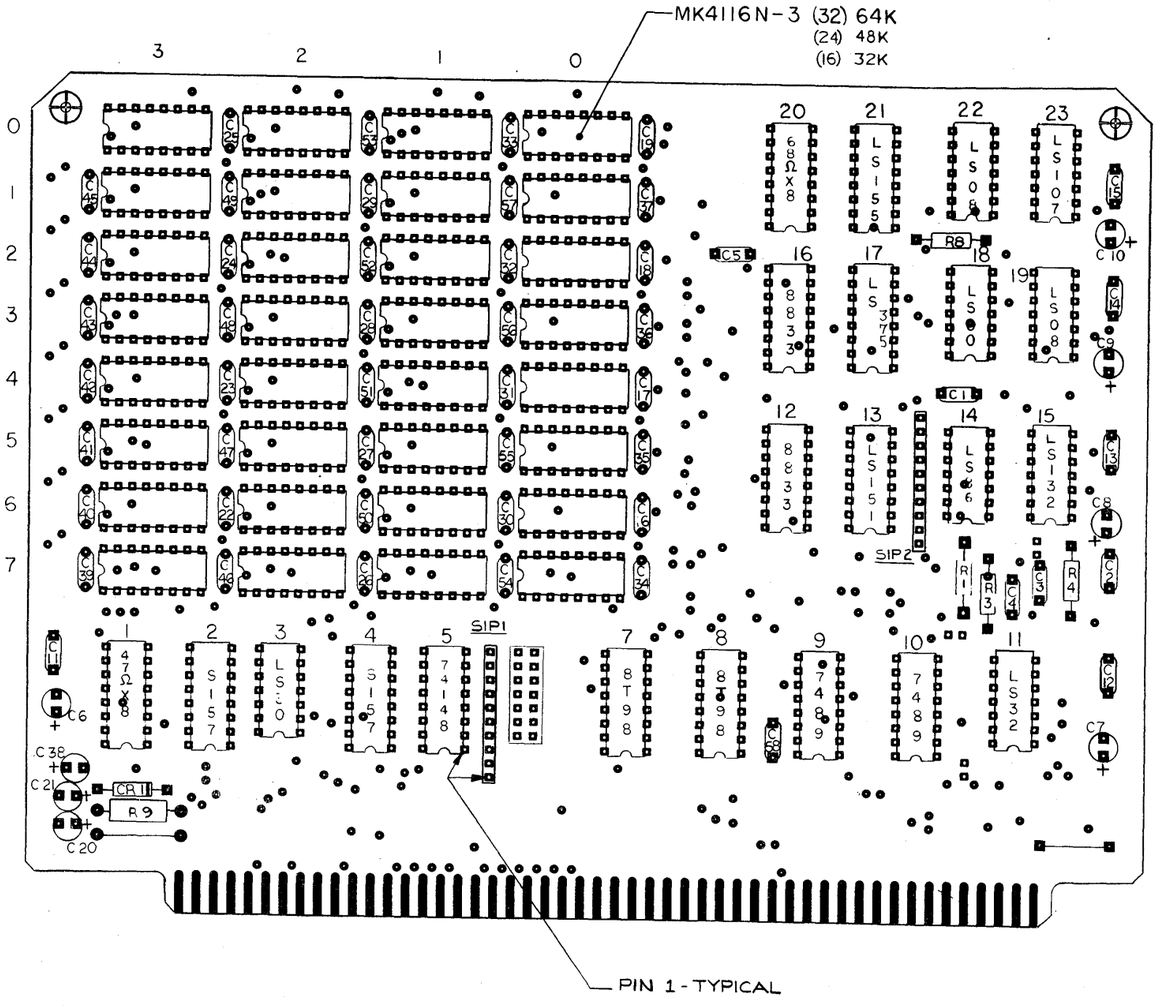
SCHEMATIC, 64 K MEMORY

SIZE	CODE IDENT NO.	DWG NO.	REV
D		10144-6	C

SCALE | SHEET 1 OF 1

10144-6

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



ITEM	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REF DES
36					
35					
34	2		4306R-101-332	RES NETWK, 3.3K (BOURNS)	SIP1,2
33	1		1N5231	DIODE, ZENER	CR1
32					
31	1			RES, 130Ω, 5%, 1/2W	R9
30	1			RES, 68Ω, 5%, 1/4W	R8
29	1			RES, 240Ω, 5%, 1/4W	R4
28	3			RES, 3.3K, 5%, 1/4W	R1,3
27					
26	1			CAP, 150 pf	C5
25	3			CAP, 22 UF, 16V TANT	C20,21,38
24	45			CAP, .05UF CER DISK	C11-19,22-37,39-58
23	5			CAP, 4.7UF, 10V TANT	C6-10
22	1			CAP, 330 pf	C4
21	1			CAP, .001 pf	C3
20	1			CAP, 100 pf CER DISK	C2
19	1			CAP, OPTIONAL	C1
18	1		74LS107	I.C., DUAL J-K FF	U23
17	1		74LS08	, QUAD, 2-IN AND	U22,19
16	1		74LS155	, 2 TO 4 DECODE, DEMUX	U21
15	1		898-3-R68	, 68ΩX8 R-PACK BECKMAN	U20
14					
13	1		74LS00	, QUAD, 2-IN NAND	U18
12	1		74LS375	, QUAD-D, F.F.	U17
11	1		74LS132	, QUAD, 2-IN, NAND (S.T.)	U15
10	1		74LS86	, QUAD, 2-IN, EXC. OR	U14
9	1		74LS151	, DATA SEL-MUX	U13
8	2		8833	, QUAD, TRI-STATE TRANSCEIVE	U12,16
7	1		74LS32	, QUAD, 2-IN OR	U11
6	2		7489	, 64 BIT R/W MEM	U9,10
5	2		8T98	, TRI-STATE HEX BUFF (INV)	U7,8
4	1		74148	, 8 TO 3 PARITY ENCODER	U5
3	2		74LS30	, 8-IN NAND	U3
2	2		74S157	, QUAD, 2 TO 1 MUX	U2,4
1.	1		898-3-R47	I.C., 47ΩX8 R-PACK BECKMAN	U1

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± — DECIMALS .XX ±. .XXX ±. ANGLES ±
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J. Razio	12-19-77
CHECKED RON YOUNKIN	1-21-79

FUTUREDATA

ASSEMBLY, 64K MEMORY

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		10144-5	C

SCALE 2/1 SHEET 1 OF 1

10144-5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

RESET 93

DATA Ø 40
DATA 1 41
DATA 2 42
DATA 3 43
DATA 4 44
DATA 5 45
DATA 6 46
DATA 7 47

ADDR4
ADDR3
ADDR2
ADDR1
ADDRØ
WR- 58
IO- 36
PD- 57

SEL Ø- 26
SEL 1- 27
SEL 2- 28
SEL 3- 29
SEL 4- 30
SEL 5- 31
SEL 6- 32
SEL 7- 33

U1 8T97 · U2 74S 138 · U3 74S 138 · U4 · U5 8T97 · U6 8T97 · U7 74 LS02 · U8 74 LS04 · U9 · U10 74LS 74 · U11 74LS 03 · U12 74LS 174 · U13 8T97 · U14 74173 · U15 74173 · U16 8T97 · U17 74173 · U18 74173 · U19 8T97 · U20 74173 · U21 8T97 · U22 8T97 · U23 74173 · U24 74173 · U25 8T97

R1 3.3K · R2 3.3K · R3 3.3K · +5

J1 · J2 · J3 · J4

INTCL3-
INTCL2-
RSTAT-

INTRQ1-
DATA Ø
DATA 1
RSTAT-

C1-C5 4.7UF 10V
C6-16 .05UF
+5V
GND

2. RI THRU R3 VALUES ARE IN OHMS ±5%, ¼W.
1. J1, J2, J3, & J4. ALL EVEN NUMBERED PINS ARE GROUND.
NOTE: UNLESS OTHERWISE SPECIFIED:

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	ZONE

PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± · DECIMALS X ± .XX ± .XXX ± · ANGLES ± ± ± ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

NEXT ASSY | USED ON APPLICATION

CONTRACT NO.

DR BY Tony Wade 7.21.77

CHK BY

APPROVED BY

futuredata

SCHEMATIC, 4 PORT I/O

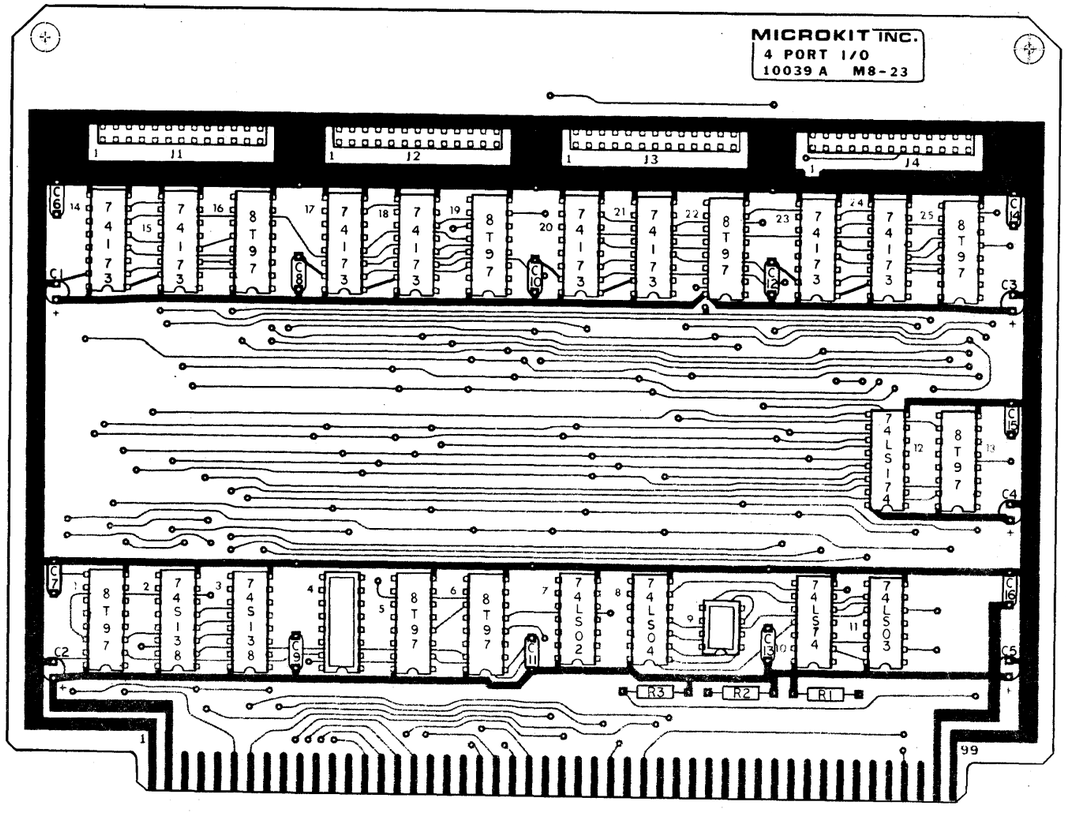
SIZE D · CODE IDENT NO. · DWG NO. 10039-6 · B

SCALE · SHEET OF

10039-6 B

DIETZGEN/POST CLEARPRINT 102010

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



ITEM	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REF DES
14	4		1-87227-3	CONN. 26 PIN HEADER-AMP	J1-4
13	11			CAP. .05UF CER DISK	C6-16
12	5			CAP. 47UF, 10V TANT	C1-5
11	3			RES. 33K, ±5%, ¼ W	R1,2,3
10	1			SOCKET, I.C. 16 PIN	U4
9	1			SOCKET, I.C. 8 PIN	U9
8	8		74173	I.C., 4-BIT D REG. TRI-STATE	U14,15,17,18,20,21,23,24
7	1		74LS174	HEX D FF	U12
6	1		74LS03	QUAD, 2-IN. NAND O.C.	U11
5	1		74LS74	DUAL-D FF	U10
4	1		74LS04	HEX BUFFER	U8
3	1		74LS02	QUAD, 2-IN. NOR	U7
2	2		74S138	DECODER/DEMUX	U2,3
1	8		8T97	I.C. TRI-STATE HEX BUFFER	U1,5,6,13,16,19,22,25

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ±. .XXX ±. ANGLES ±
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J. Lazio	7-24-77
CHECKED	

MICROKIT INC.

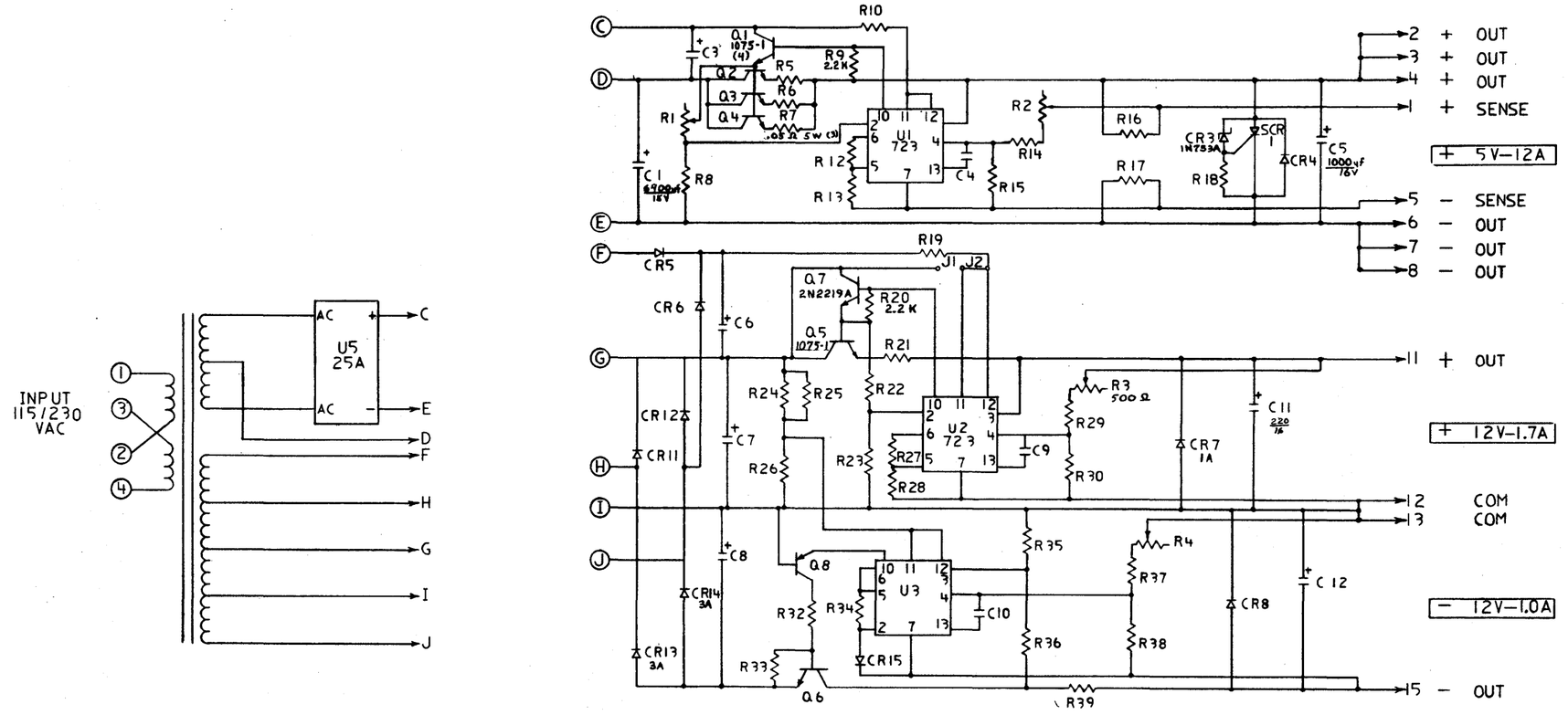
ASSEMBLY,
4 PORT I/O

SIZE	CODE IDENT NO.	DRAWING NO.	
D		10039-5	A

SCALE 2/1 SHEET 1 OF 1

10039-5 A

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED



NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY.	USED ON	DRAWN BY CAF
		CHECKED
		APPROVED

MATERIAL

FINISH

1. TOLERANCES ANGULAR
   XX ±
   XXX ± ±
2. BREAK ALL SHARP EDGES APPROX.
3. ALL MACH. SURFACES
4. ALL DIMS IN INCHES
5. FILLET RADII

DIST CODE

G.R. FUTUREDATA

TITLE
SCHEMATIC,
AMDS POWER SUPPLY

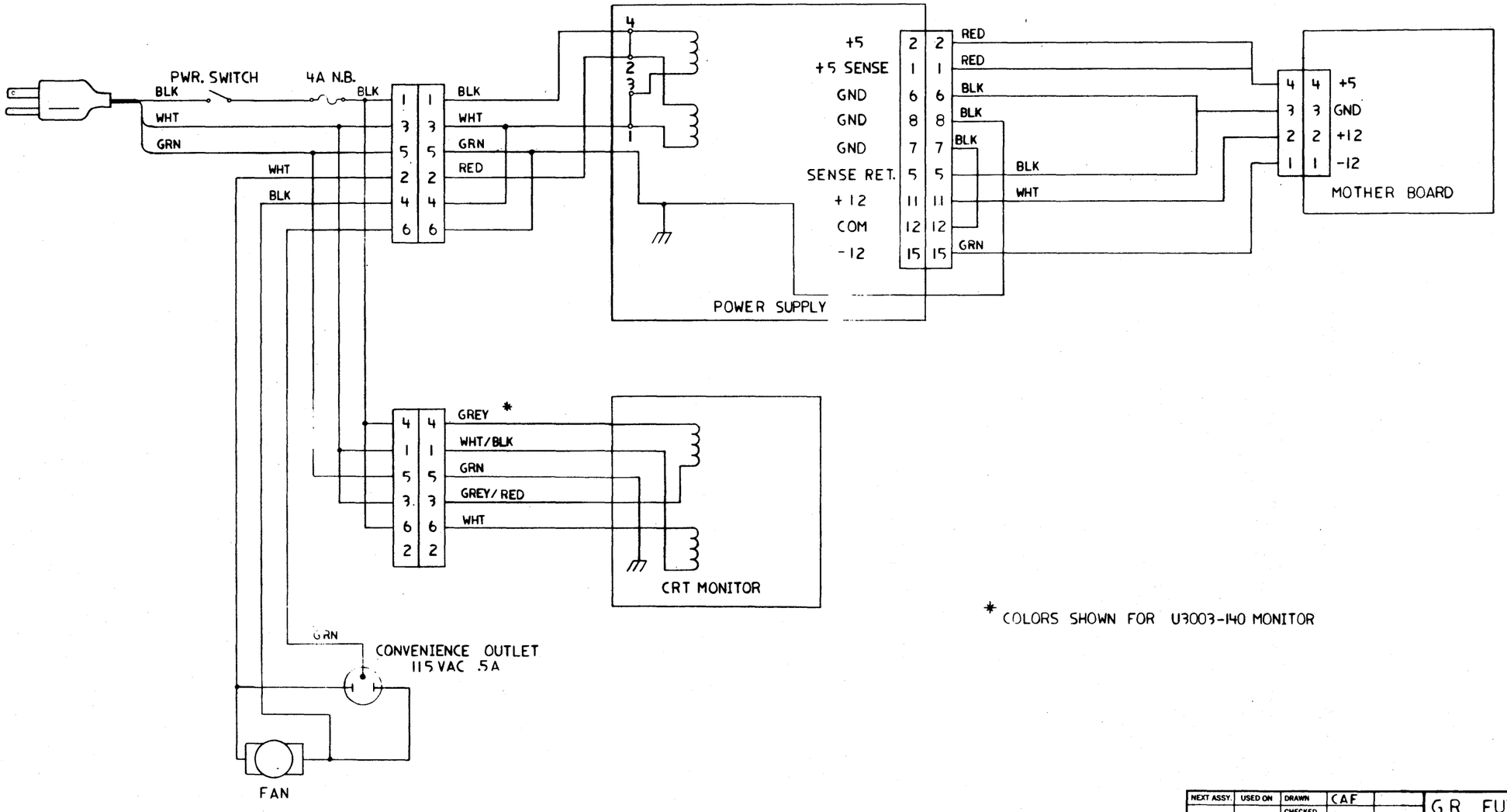
SIZE	CODE	DRAWING NO.
D		10080 - 6

SCALE SHEET

10080-6 A

3/73 DIETERICH-POST CLEARPRINT 1000

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED



* COLORS SHOWN FOR U3003-140 MONITOR

UNLESS OTHERWISE SPECIFIED

NEXT ASSY.	USED ON	DRAWN	CAF	
		CHECKED		
		APPROVED		

MATERIAL

FINISH

1. TOLERANCES — ANGULAR
XX ±
XXX ±
±
2. BREAK ALL SHARP EDGES APPROX
3. ALL MACH SURFACES
4. ALL DIMS IN INCHES
5. FILLET RADII

DIST CODE

GR FUTUREDATA

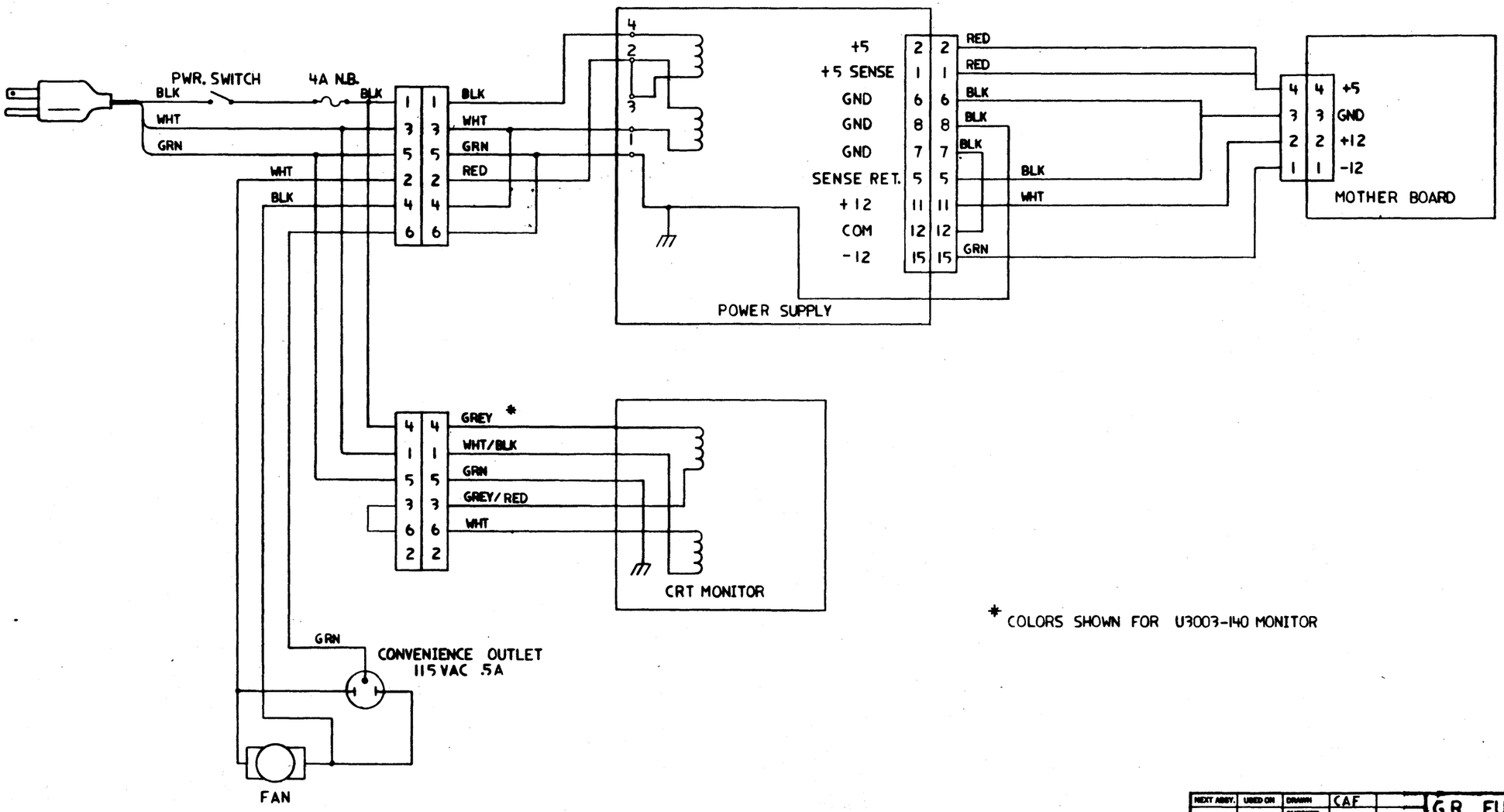
TITLE SCHEMATIC:
AMDS CHASSIS WIRING
110 V

SIZE	CODE	DRAWING NO
D		10081-6

SCALE — SHEET

10081-6 A

REVISIONS						
ZONE	LAL	REV.	DESCRIPTION	CHECK	DATE	APPROVED



* COLORS SHOWN FOR U3003-140 MONITOR

NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY.	USED ON	DRAWN	CAF		
		CHECKED			
		APPROVED			

1. TOLERANCES ANGULAR
   XX ±
   XXX ± ±
2. BREAK ALL SHARP EDGES APPROX.
3. ALL MACH. SURFACES
4. ALL DIMS IN INCHES
5. FILLET RADII

MATERIAL

FINISH

NEXT CODE

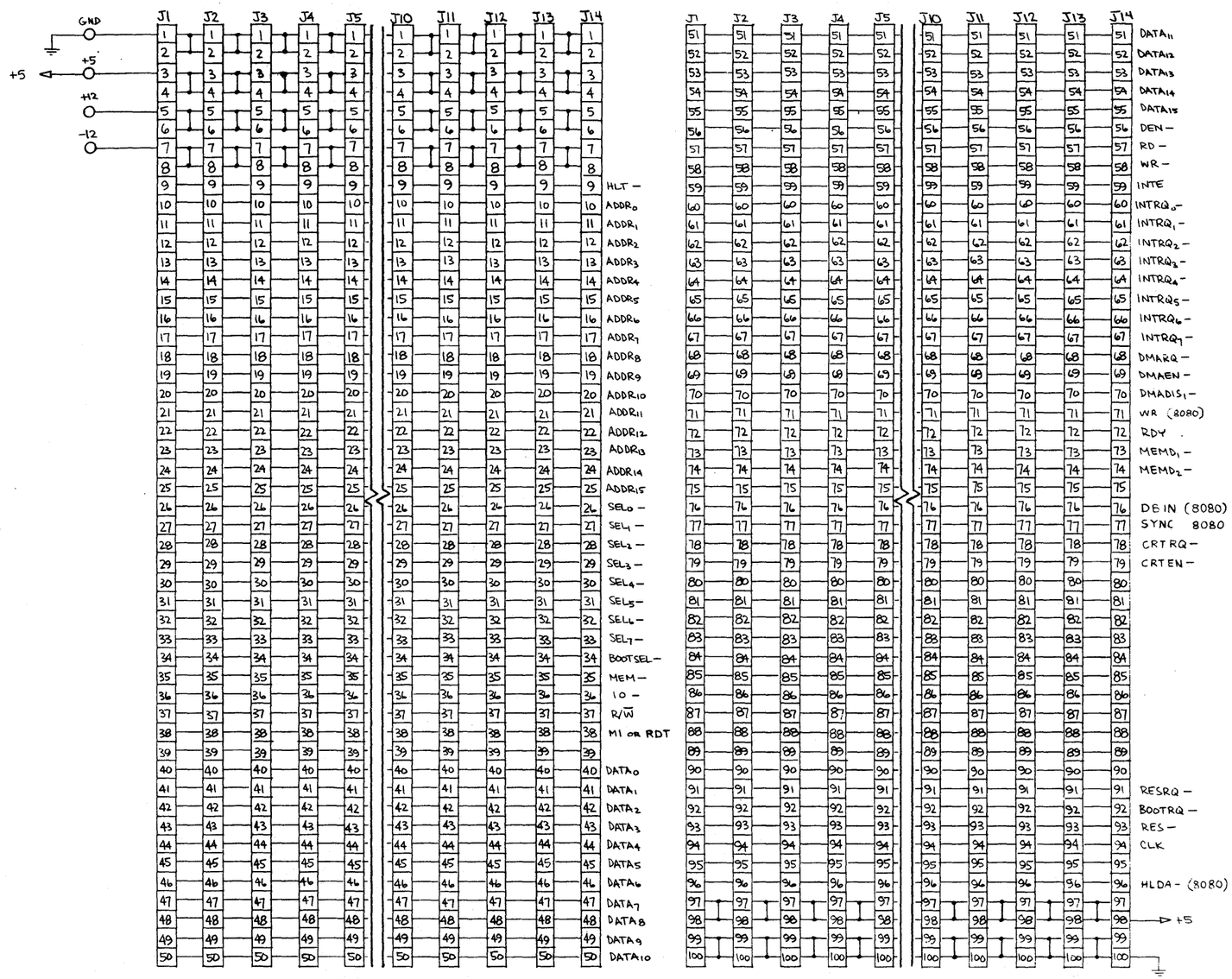
GR FUTUREDATA

TITLE SCHEMATIC:
AMDS CHASSIS WIRING
220 V

SIZE	CODE	DRAWING NO.
D		10082 - 6

SCALE SHEET

10082-6 A



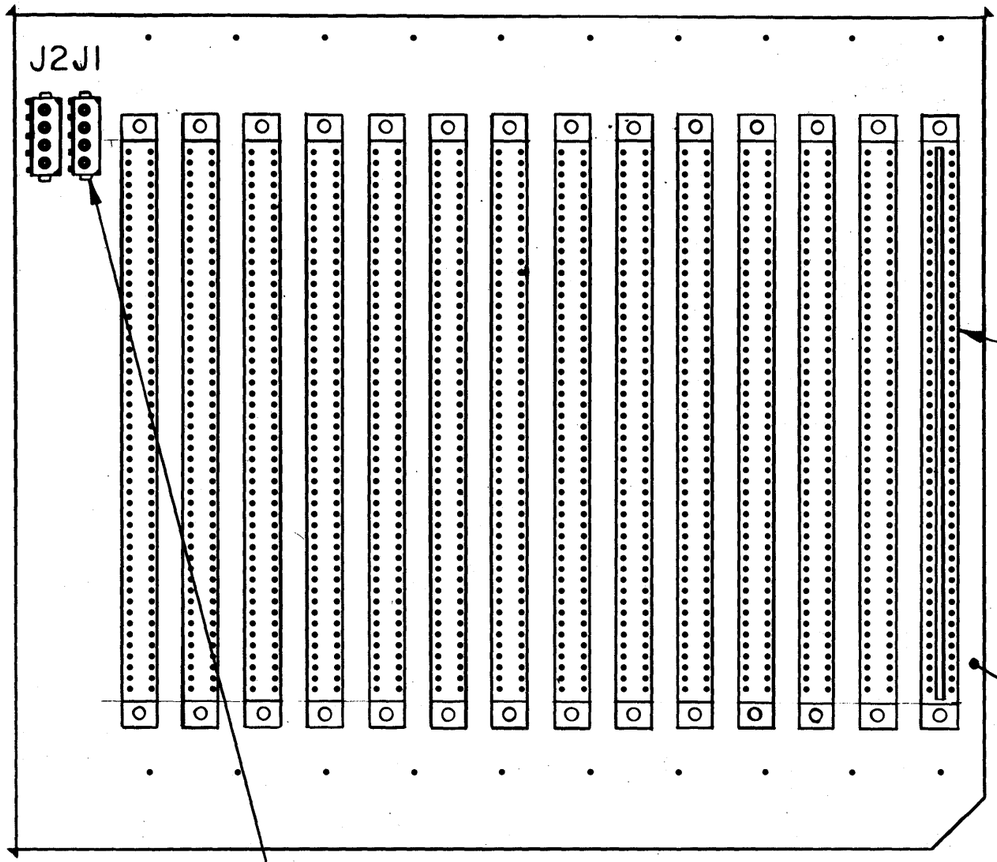
futuredata

SCALE:	APPROVED BY:	DRAWN BY D. DAVE
DATE:		REVISED A

MOTHER BOARD SCHEMATIC

DRAWING NUMBER 10157 - 6

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



CPH 8100-100 SST
14 PLACES

10157-4

350211-1 (AMP)
2 PLACES

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

NEXT ASSY	USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN [illegible]	10.25.78
CHECKED	

FUTUREDATA

ASSEMBLY, MOTHER BOARD

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C		10157-5	A

SCALE FULL SHEET 1 OF 1

10157-5 A

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED

CRT BOARD

CRT-P2 — NO. 22 ALPHA WIRE — CRT-P3

GND	1	10
VIDEO	2	8
HORIZ	3	6
VERT	4	9
LED+5	6	
ACTLED-	7	
KBDLED-	8	
RUNLED-	9	
ONLED-	10	

CRT
KEY BETWEEN 9&10

CRT-P4

6
7
8
9
10

LED DISPLAY

ITEM NO.	QTY.	CODE	PART NO.	DESCRIPTION	DESIG.
7	30"			NO. 22 ALPHA WIRE BLACK	
6	5			CRIMP FEMALE TERMS	
5					CRT-P4
4	4			CRIMP EDGE TERMS	
3	1				CRT-P3
2	9			CRIMP FEMALE TERMS	
1	1			10 PIN	CRT-P2

DIST CODE

NEXT ASSY.	USED ON			
		DRAWN	J Fowler	5-16-79
		CHECKED		
		APPROVED		

MATERIAL

FINISH

1. TOLERANCES — ANGULAR
   XX ±
   XXX ± ±
2. BREAK ALL SHARP EDGES APPROX.
3. ALL MACH. SURFACES
4. ALL DIMS IN INCHES
5. FILLET RADII

GR-FUTUREDATA

TITLE

CRT I/O TO LED & MONITOR CABLE

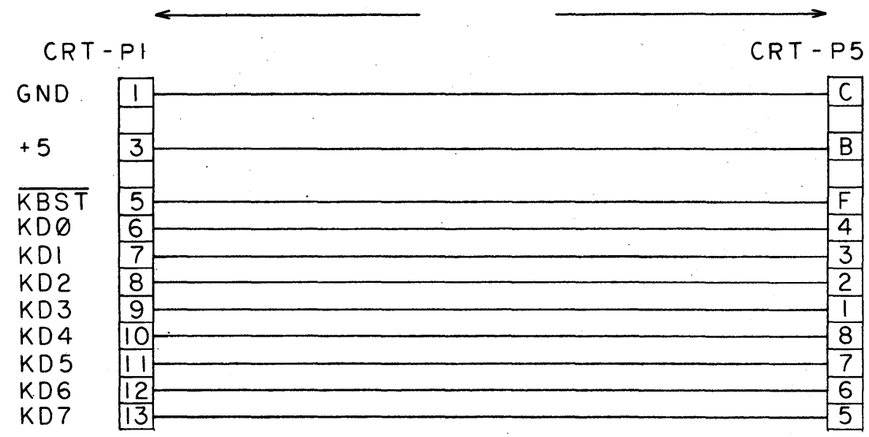
SIZE	CODE	DRAWING NO.
D		10088-6

SCALE — SHEET 1 OF 1

10088-6 A

NOTES: UNLESS OTHERWISE SPECIFIED.

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED



ITEM NO.	QTY.	CODE	PART NO.	DESCRIPTION	DESIG.
					DIST CODE
4	13			CRIMP CARD EDGE CONNECTOR	
3	1			20 PIN CARD EDGE CONNECTOR	CRT-5
2	13			CRIMP FEMALE TERMS	
1	1			20 PIN	CRT-P1

NEXT ASSY.	USED ON	DRAWN	J Fowler	3-4-79
		CHECKED		
		APPROVED		

MATERIAL

FINISH

1. TOLERANCES ANGULAR
   XX ±
   XXX ± ±
2. BREAK ALL SHARP EDGES APPROX.
3. ALL MACH. SURFACES
4. ALL DIMS IN INCHES
5. FILLET RADII

TITLE: GR-FUTUREDATA

CRT I/O TO KEYBOARD CABLE

SIZE	CODE	DRAWING NO.
D		10089-6

SCALE | SHEET 1 OF 1

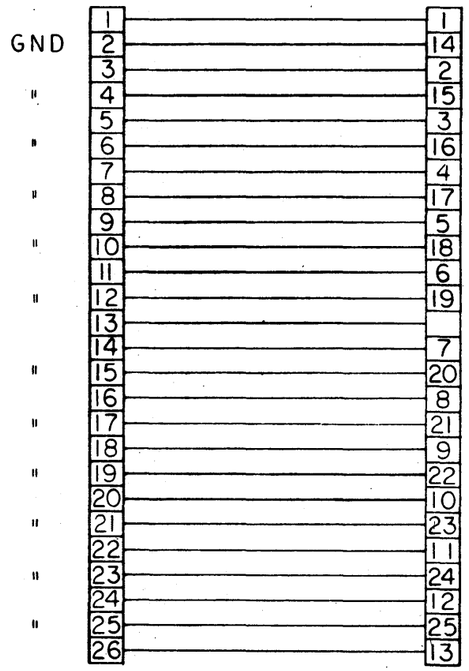
10089-6 A

NOTES: UNLESS OTHERWISE SPECIFIED.

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED

MPIO-P3
26 POS FLAT CABLE
CONNECTOR

DB-25 STYLE
REARPANEL RECEPTACLE
AMP P/N 206653-1



DATA STROBE-

PRINTER DATA Ø (PDØ)

" " 1 (PDI)

" " 2 (PD2)

" " 3 (PD3)

" " 4 (PD4)

" " 5 (PD5)

" " 6 (PD6)

" " 7 (PD7)

PRINTER BUSY

PAPER OUT

26 COND FLAT CABLE
3M 3365/26

NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY.	USED ON	DRAWN	J Fowler	3-15-79
		CHECKED		
		APPROVED		
MATERIAL		1. TOLERANCES XX ± XXX ±		ANGULAR ±
FINISH		2. BREAK ALL SHARP EDGES APPROX. 3. ALL MACH. SURFACES 4. ALL DIMS IN INCHES 5. FILLET RADII		

DIST CODE

GR-FUTUREDATA

TITLE: SCHEMATIC, "CENTRONICS" PRINTER DATA

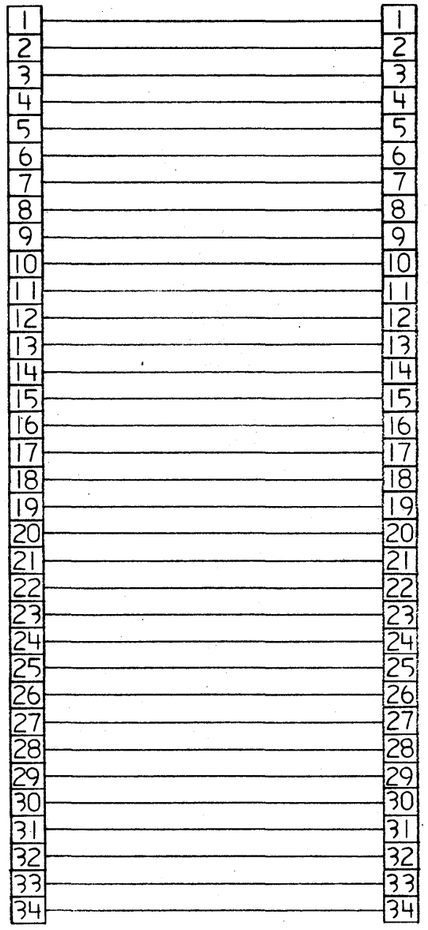
SIZE	CODE	DRAWING NO.
D		10090-6

SCALE

SHEET 1 of 1

10090-6 A

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED



ALL ODD PINS GND

NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY.	USED ON	DRAWN	J FOWLER	
		CHECKED		
		APPROVED		
MATERIAL		1. TOLERANCES		ANGULAR
		XX ±		±
FINISH		XXX ±		
		2. BREAK ALL SHARP EDGES APPROX.		
		3. ALL MACH. SURFACES		
		4. ALL DIMS IN INCHES		
		5. FILLET RADII		

DIST CODE

GR/FUTUREDATA

TITLE
SCHEMATIC
DISK I/O CABLE

SIZE	CODE	DRAWING NO.
D		10093-6

SCALE | SHEET

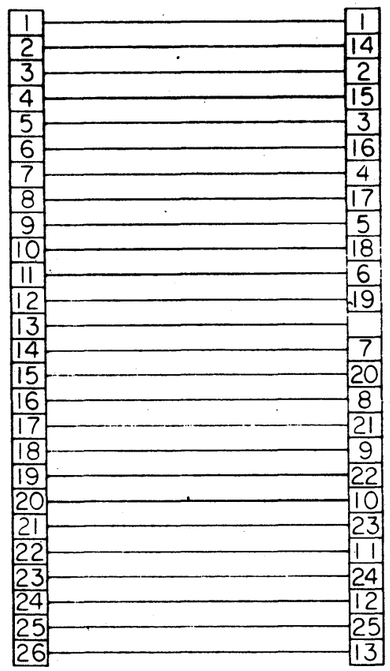
10093-6 A

2/73 DIETERICH-POST CLEARPRINT 5080

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED

MPIO-PI
26 POS FLAT CABLE
CONNECTOR

DB-25 STYLE
REARPANEL RECEPTACLE
AMP P/N 206653-1



1 – 1	GND.
2 – 14	TRANS. DATA (TXD)
3 – 2	REC. DATA (RXD)
4 – 15	REQ. TO SEND (RTS)
5 – 3	CLEAR TO SEND (CTS)
6 – 16	DATA SET RDY. (DSR)
7 – 4	
8 – 17	
9 – 5	
10 – 18	
11 – 6	
12 – 19	
13 –	
14 – 7	GND.
15 – 20	DATA TERM. RDY. (DTR)
16 – 8	CARRIER DET. (DCD)
17 – 21	
18 – 9	
19 – 22	
20 – 10	
21 – 23	
22 – 11	
23 – 24	
24 – 12	
25 – 25	
26 – 13	

26 COND FLAT CABLE
3M 3365/26

10091-6 A

NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY.	USED ON			
		DRAWN	J. Fowler	3-14-79
		CHECKED		
		APPROVED		

1. TOLERANCES — ANGULAR
   XX ±
   XXX ± — ±
2. BREAK ALL SHARP EDGES APPROX.
3. ALL MACH. SURFACES
4. ALL DIMS IN INCHES
5. FILLET RADII

MATERIAL

FINISH

DIST CODE

TITLE: GR-FUTUREDATA

SCHEMATIC
SERIAL PORT NO. 1

SIZE	CODE	DRAWING NO.
D		10091-6

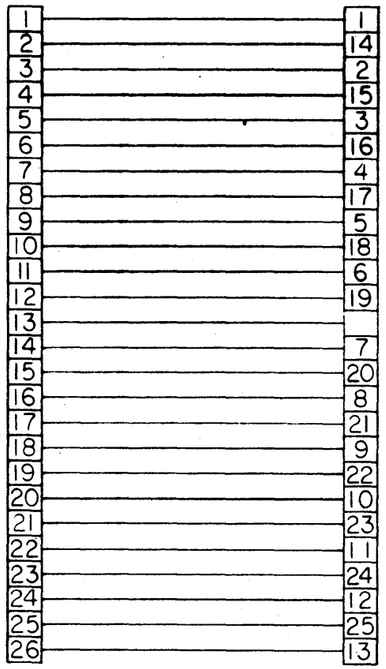
SCALE — SHEET 1 1

5/73 DIETERICH-POST CLEARPRINT 3889

REVISIONS						
ZONE	LAL	REV	DESCRIPTION	CHECK	DATE	APPROVED

MPIO-P4
26 POS FLAT CABLE
CONNECTOR

DB-25 STYLE
REARPANEL RECEPTACLE
AMP P/N 206653-1



1	1	GND
2	14	
3	2	TRANS. DATA (TXD)
4	15	
5	3	REC DATA (RXD)
6	16	RDR+ (TTY)
7	4	
8	17	
9	5	CLEAR TO SEND (CTS)
10	18	
11	6	DATA SET RDY. (DSR)
12	19	
13		
14	7	GND
15	20	
16	8	CARRIER DET. (DCD)
17	21	RDR- (TTY)
18	9	NET+
19	22	
20	10	NET-
21	23	
22	11	
23	24	RXD+ (TTY)
24	12	RXD- (TTY)
25	25	TX- (TTY)
26	13	TX+ (TTY)

26 COND FLAT CABLE
3M 3365/26

NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY.	USED ON	DRAWN	J. Fowler	3-15-79	DIST CODE
		CHECKED			GR-FUTUREDATA
		APPROVED			TITLE
MATERIAL		1. TOLERANCES XX ± XXX ± ANGULAR ±			SCHEMATIC, SERIAL PORT NO. 2
FINISH		2. BREAK ALL SHARP EDGES APPROX. 3. ALL MACH. SURFACES 4. ALL DIMS IN INCHES 5. FILLET RADII			SIZE D / CODE / DRAWING NO. 10092-6
					SCALE / SHEET 1 of 1

10092-6 A

3/73 DIETERICH-POST CLEARPRINT 3889

GenRad

futuredata

11205 SOUTH LA CIENEGA BOULEVARD LOS ANGELES CALIFORNIA 90045 TWX 910-328-7202 TEL (213) 641-7700