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DEUCE: A HIGH-SPEED GENERAL-PURPOSE COMPUTER

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SUMMARY

Deuce is a high-speed general-purpose binary digital computer, operating throughout in the serial mode at a digit frequency of 1 Mc/s, and using mercury delay lines as its primary storage system. It is a development from the Ace Pilot Model, which was developed by the National Physical Laboratory and has had an outstandingly successful career since it was commissioned in 1952. Many features of Deuce are common to this earlier machine, but a number of operational improvements have been made, together with additional features to facilitate maintenance and also to reduce the problems of testing new programmes.

Input to and output from the computer are by means of high-speed punched-card machines, and a large-capacity (8 192 words) magnetic-drum store augments the main mercury-delay-line storage system.

The internal organization of the machine is discussed, followed by a more detailed account of some of the novel features incorporated. Other sections describe briefly the construction of the machine and refer to typical applications.

(1) INTRODUCTION

To a substantial degree, the design of an electronic computer represents a compromise between speed of operation, storage capacity and economy in equipment. All these aspects are mutually conflicting, and all have some influence on the important question of reliability. A further factor to be considered is the relative difficulty of programme construction for the computer. However, this is frequently over-stressed, as it represents only a small fraction of the time which must be spent in the preparation of a mathematical investigation of any size, and diminishes steadily in importance as a library of programmes and subroutines is accumulated. It is therefore of significant importance only to the extent that a suitable choice of instruction code can lead to an increase in effective machine speed.

For the N.P.L. Ace Pilot Model, mercury delay lines operating in the serial mode were chosen as the storage elements, and a magnetic-drum store was subsequently added to augment the total storage capacity. Deuce, based largely on this earlier machine, uses the same storage systems, and their reliability, in conjunction with the economy in equipment through the use of serial arithmetic units, is reflected in the performance records of machines of this type. Fast operation is achieved by the choice of a digit rate of 1 Mc/s, and the major operational defect of acoustic lines, that of poor access time, is overcome by the use of optimum coding.

(2) LOGICAL DESIGN

Mercury delay lines have been used as the storage medium of digital computers for many years,[1,2] and have been developed to give high performance and great reliability. Their obvious disadvantages of variation of delay time with temperature and lack of portability are of no consequence in this application, the necessary degree of temperature control being obtainable by a simple thermostat. A more serious disadvantage when used in the conventional manner is the fact that access to any item of the stored information is possible only at intervals equal to the delay time of the unit. Unless the uneconomic solution is adopted of storing only a small amount of information per unit, fast operation must be achieved by a combination of two methods:

(*a*) Provision of a graded sequence of delay units, storing, for example, 1, 2, 4, 8, 16 and 32 words.[3]

(*b*) Location of instructions and data within the delay units in such a way that a minimum of time is wasted in obtaining access to the next item required.[4]

Both of these devices have been adopted in the present machine, and it has been found that the full range of storage capacities suggested above is not essential. The main storage system consists of a set of 12 mercury lines (referred to as DL1–12), which are used for storage of instructions and data of that part of the programme currently being executed. These lines each have a capacity of 32 words, the word length throughout the machine being 32 binary digits. Since the digit frequency is 1 Mc/s, any item of information is accessible at intervals of 1 024 microsec. This period of time will be referred to as a 'major cycle'.

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Temporary storage is provided for numbers being processed by the machine at any time in a group of four single-word delay lines (TS13–16), which are associated with the arithmetic functions of the machine. The access time to these is effectively instantaneous in a serial machine, and their delay time of 32 microsec is referred to as a 'minor cycle'. This unit is the fundamental unit of machine operating time, as it is the shortest time in which a single item of information can be transferred between two storage positions.

Each of the single-word registers is not only available as a storage position, but is also operated in conjunction with one or more of the arithmetic or logical units of the computer. The single-word store TS13, for example, can be used merely as a temporary store for a number, but it also acts as the accumulating register for addition and subtraction operations. These are performed by the use of 'functional addresses'. A number sent to address 13 replaces any information already stored in TS13, but if it is sent instead to address 25 the new number is algebraically added to that already stored in the register. Similarly a transfer to address 26 causes the number sent to be subtracted from that already stored in TS13.

The facilities associated with TS14 and TS15 are of a somewhat different type in that they permit manipulation of numbers stored therein. Use of addresses 14 and 15 as sources of information makes available for transfer elsewhere the information which has previously been sent there, but if address 25 be used as a source of information, the output is that obtained by collating the two numbers in TS14 and TS15; i.e. a '1' is obtained only in those digit positions in which TS14 and TS15 both contain a '1'. A number of other logical operations, including left and right shifts, are available from further functional addresses associated with TS14 and TS15.

To accommodate the double-length products of multiplication operations a two-word delay line DS21 is provided. This line is also provided with additive and subtractive inputs, permitting its use as an accumulating register for double-length arithmetic; two further double-word lines DS19 and DS20 are included as temporary stores to facilitate such work, although they can, of course, be used in normal operation to store two independent single words.

(3) INSTRUCTION CODE

It is apparent that, if the single-word lines are provided with output and input gates (referred to subsequently as 'source' and 'destination' gates), transfers between these lines, together with arithmetic and logical operations using their special facilities, are possible merely by specifying the source and destination number associated with the required transfer. For example, the instruction 'source 16 to destination 13' (normally written as 16–13) replaces the number in TS13 by that in TS16, the contents of the latter remaining unaltered.

Similarly, the instruction 16–25 results in the addition to the previous content of TS13 of the word in TS16, while execution of the transfer 25–16 causes collation of the contents of TS14 and TS15, the result being placed in TS16. In each of these examples it is assumed that the appropriate gates are open for one minor cycle only.

Additional information must, however, be carried in the instruction if transfers are to be made to and from the multi-word delay lines, and it is also necessary to specify the position of the next instruction, unless the instructions are to be placed in some regular sequence. As previously indicated, the latter solution has been rejected on account of the unavoidable loss of time involved.

The necessary elements of the instruction word are therefore as listed below. Two other items of information are included and will be described subsequently.

(*a*) *Source Number.*—This defines the source of information to be transferred. It may, as illustrated previously, indicate a storage position or it may emit a number resulting from an operation on one or more storage positions.

(*b*) *Destination Number.*—This similarly defines the position to which information is to be sent, and may be functional or a normal storage position.

(*c*) *Next Instruction Source.*—This defines the long delay line from which the next instruction is to be taken. Of the twelve 32-word lines, those numbered 1–8 are available as instruction sources.

(*d*) *Wait Number.*—After an instruction reaches the control circuits of the computer, one minor cycle is occupied in setting up the specified transfer path. The wait number determines the number of additional minor cycles which are allowed to elapse before the transfer gates are actually opened.

(*e*) *Timing Number.*—This number determines the time at which the next instruction source gate is opened to allow the specified next instruction to enter the control circuits.

An example, referring to Fig. 1, will illustrate the way in

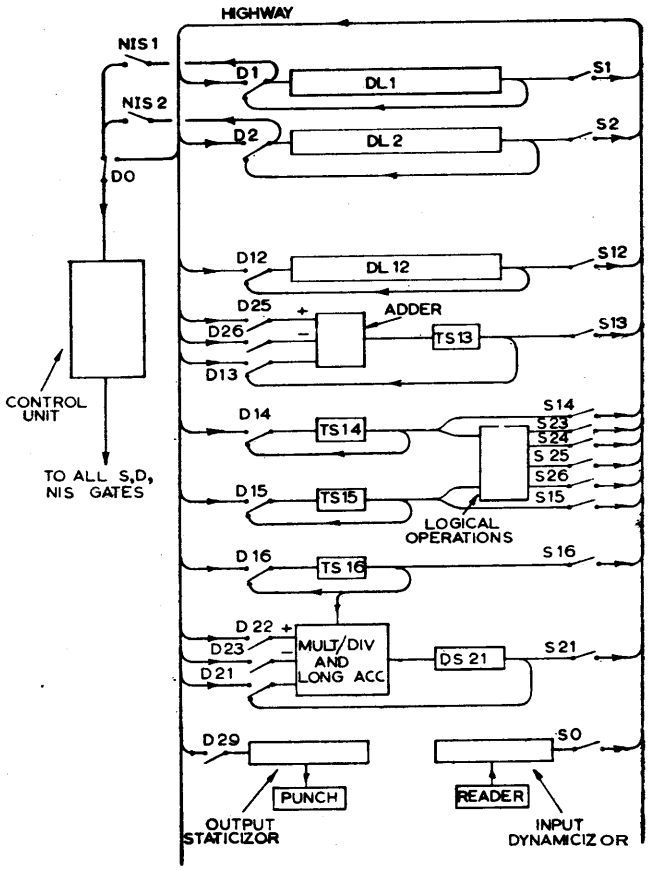

Fig. 1.—High-speed storage system.

which the various parts of the instruction word are used. This Figure presents, in schematic form, some of the principal elements of the computer. It will be seen that each delay line communicates with a main busbar ('highway') through two gates. These are shown as switches, and those on the right-hand side of the diagram represent the source gates associated with the storage. These do not affect the circulation paths of the delay lines, whereas the switches representing destination gates, on the left-

hand side, break the circulation path when operated to allow new information to flow in, so that the existing information is lost, or effectively overwritten. Some of the additional source and destination gates associated with arithmetic and logical operations are also shown.

A second busbar, the 'next instruction highway', is connected through a further set of gates to the first eight long delay lines, and also through a special destination gate, D0, to the main highway, so that instructions can be sent direct to the control circuits from, for example TS13, where an instruction may have been built up by arithmetic operations.

Since all delay lines are sub-multiples of 32 words in length, the position of information in the store, in the absence of arithmetic operations, is repeated every major cycle. The 32 word positions in any long delay line can therefore be arbitrarily numbered 0, 1 . . ., 31, position 0 being assigned to the first word loaded into the machine. Suppose that a current instruction in position 0 is required to transfer the word in position 5 of delay line DL7 into the short accumulator TS13, adding it to the word already present; the next instruction is to be taken from delay line 1, position 11. The required instruction is:

Source	7
Destination	25
Next instruction source	1
Wait number	3
Timing number	9

Since a minor cycle is used to set up the gates after the instruction has entered control, the wait and timing numbers are less by two than the difference in relative positions of the words concerned.

It will be observed that, if the timing number is made equal to 31, the next instruction is taken from position 33 (i.e. position 1) of the delay line. By making all timing numbers equal to 31 and retaining the same next instruction source, instructions will be obeyed sequentially through a delay line. This procedure is unnecessarily wasteful of time, as only one instruction is obeyed every 33 minor cycles, and in practice it is possible, without appreciable effort, to locate data and instructions in such a way that the majority have wait and timing numbers equal to zero. Under these conditions each is executed in 64 microsec—an increase in speed of 16 times over a machine in which instructions are performed in sequence. In normal scientific computations an average gain in speed of about five times is readily achieved. This reduction on the optimum figure arises principally from the fact that multiplication and division occupy two major cycles, so that the improvement in access time is relatively less important for these functions than for additions, transfers, etc., having an execution time of one minor cycle.

The instruction word is normally written

NIS	*S*	*D*	*C*	*W*	*T*	*G*
1	7 —	25	0	3	9	1

Two additional items have been introduced. The column headed *C* represents the 'characteristic' of the instruction, and permits variation of the single-word transfer assumed above. This single-word transfer occurs if $C = 0$. If $C = 2$, transfer is for two minor cycles, permitting ready use of double-length numbers where additional precision is required. If $C = 1$, the length of transfer is determined as $(T - W + 1)$ minor cycles. This provides the valuable facility of block transfer. For example, if the above instructions were amended to have $C = 1$, $W = 10$ and $T = 9$, transfer would continue for 32 minor cycles, since T is interpreted as $T + 32$ if a transfer of negative duration would otherwise be required. The resulting operation therefore adds into the accumulator all 32 words from DL7.

The column headed *G* above is a 'Go' digit. If this digit of an instruction is present, the computer proceeds automatically. When the digit is zero, operation is halted and the instruction is not obeyed until an external stimulus is received. Apart from its obvious value in allowing computation to be stopped at any desired point, as an aid, for example, in testing a new programme, this facility is essential to the input and output through punched-card machinery and is discussed further in Section 4.

Reference to the list of source and destination numbers in Appendix 11.1 shows that many of these are of the types discussed in the preceding Section. Certain special operations are described in a further section of the Appendix.

(4) INPUT AND OUTPUT

Data and instructions are transmitted to and from the computer through an 'input dynamicizor' (source 0) and an 'output staticizor' (destination 29). These normally operate in conjunction with modified punched-card accounting machines which are used as the principal input and output organs. Each input card has 80 columns of 12 rows available for punching, but of these only 32 columns are used for input to the computer. When reading decimal data, the first two rows (Y and X rows) are normally used only for algebraic-sign designation, the remaining ten being used for the decimal digits 0–9. The cards pass a set of reading brushes, one for each column, as each row of the card reaches the reading station. For a period of about 5 millisec, as each row is in position under the brushes, the circuits of the input dynamicizor are set up by contact from the brushes through any holes punched in the card to a metal roller, and the input dynamicizor generates, in serial form, a 32-digit word corresponding to the pseudo-binary word punched in that row of the card. At this time the computer is normally halted by a stop instruction (i.e. one in which the Go digit is zero), calling for transfer from source 0 to a storage location. Near the middle of the 5 millisec reading period the card reader emits a signal to the computer allowing execution of the instruction. A further 16 millisec are now available during which the computer proceeds at speed through the instructions of the decimal-binary conversion routine. It then halts again at another stop instruction which is obeyed when the next row is in position for reading. By this process the conversion of input data to binary form proceeds as the cards pass (at the rate of 200 per minute) through the reader, the conversion being completed immediately after the last row has been read. This allows a further period of about 90 millisec before the arrival of the first row of the subsequent card, during which time it is possible to perform a substantial amount of calculation using the data just converted.

Conversion routines have been constructed to read a variety of arrangements of data within the 32-column field of the input cards. Typical examples convert and store three 9-digit decimal numbers, eight 4-digit decimal numbers or a variety of decimal and sterling amounts as encountered, for example, in pay-roll calculation.

When the input card reader is not running, the input dynamicizor circuits are automatically disconnected from the reader and connected instead to a manual input key-board. This enables a 32-digit binary number to be fed manually to the machine.

A corresponding set of operations is used to link the computer to the output card punch. A number sent to destination 29 sets up a group of 32 d.c.-coupled trigger circuits which feed the punch magnets of the output machine. It is again usual to control the output by the use of stop instructions, which halt the computer until a signal from the punch indicates that a card is in the correct position for punching the current row. The punch runs at 100 cards per minute, and adequate time is again

available for binary-decimal or other conversions of any arrangement of fields on the card between the rows of the card as they pass the punching station.

As each row is punched, the output staticizor trigger circuits are reset by a further signal from the punch in readiness for receipt of the digits to be punched on the next row.

A group of lamps, also operated by the trigger circuits, provides a means for visual display when the punch is not running. Under these conditions the triggers can be reset manually or by the special instruction 8–24.

Dependent on the number of characters punched in the available 32-column field of the card, input and output rates up to a maximum of 6400 and 3200 decimal digits per minute, respectively, can be achieved. These speeds are well matched to the actual computing speed of the machine for the majority of scientific and technical calculations.

It will be noted from earlier paragraphs that the instruction word is made up of a number of independent elements, none of which exceeds 31 in numerical value. Such numbers can readily be translated mentally into binary notation, and instructions are therefore invariably punched on cards in this form, each instruction occupying one of the 12 rows of a card. By adopting this practice, instructions can be loaded into the machine at rates of up to 2400 per minute.

In some extended computations, of which manipulation of very large matrices is typical, the output data from one section of the work are of no direct interest, but are required only as the input for a subsequent stage. In such operations it is clearly unnecessary to perform conversion to and from decimal notation, particularly as each card can accommodate up to twelve 32-digit binary numbers. Use of binary-punched cards in this manner provides equivalent input and output rates up to 20000 and 10000 digits of decimal information per minute.

(5) MAGNETIC-DRUM STORE

The provision of large storage capacities using mercury delay lines or other forms of quick-access storage is uneconomic in equipment, and in most modern high-speed computers a compromise is made by providing a relatively small amount of quick-access memory, backed by a much larger-capacity store having longer access time.[5,6] This compromise is satisfactory if the following requirements are met:

(*a*) The capacity of the quick-access store is adequate to allow a reasonable amount of computation without reference to the backing store.

(*b*) The access time to information in the backing store is sufficiently rapid to avoid undue loss of speed due to the time occupied in making transfers into the computing store.

The first of these requirements is clearly met by Deuce, which has a high-speed store exceeding 400 words. This capacity is, for example, sufficient to store data and instructions for inversion of a 10×10 matrix without using the backing store.

The second requirement is readily met by the use of a magnetic-drum store with certain special features.[7] This drum has a capacity of 8192 words (over 250000 binary digits) stored on 256 tracks, each having the same 32-word capacity as one of the long mercury lines. Transfers to and from the drum are made in blocks of this size, thus avoiding the association of comparatively slow access with single items of information.

Since the drum rotates at approximately 6500 r.p.m., a complete track can be transferred to or from one of the long delay lines in about 12 millisec. A specific line, DL11, is reserved for such transfers, although it is, of course, available as a normal storage element when transfers are not in progress.

To effect a further economy in equipment, individual reading and writing heads are not provided for each of the 256 tracks on the drum. Instead, two sets of 16 heads and associated amplifiers are provided, one set for reading and one for writing. Each set is mounted on an independently movable assembly capable of taking up any one of 16 positions to give access to the 256 tracks by a double selection process.

Special instructions, using destinations 30 and 31, are used to effect magnetic transfer operations.

(*a*) $S_1 - 31$ ($C = 0$) causes the block of reading heads to move into position S_1, where S_1 can have values in the range 0–15.

(*b*) $S_2 - 30$ ($C = 0$) causes the information on the track now read by head number S_2 to be transferred into DL11.

(*c*) Similar instructions with $C = 1$ effect the corresponding operations of the set of writing heads.

This process is equivalent to defining the track required by two co-ordinates S_1 and S_2, which are selected by separate instructions.

The time required to move the head assemblies into a new position is 35 millisec, followed on the second instruction by a transfer time of 12 millisec. During these times, all other facilities are available for normal computation, so that in general it is possible to anticipate, for example, a reading requirement and to commence the transfer at such a time that the information is available from DL11 when required. Interlocks are provided to halt the computer temporarily if, for example, an attempt is made to use information in DL11 while a magnetic transfer is in progress.

Using the methods outlined above, experience over a wide range of problems indicates that there is no significant loss of speed (less than 5% in almost all cases) through the use of a magnetic-drum backing store rather than a mercury-delay-line store of the same large capacity. The latter, however, would require about 6000 valves against less than 200 used in the complete magnetic-drum system.

(6) CIRCUIT DESIGN FEATURES

The types of circuit element used in the computer have been described in an earlier paper.[1] They have in common the determination of valve current by large cathode-feedback resistors, thus permitting the generation of anode signals of accurately determined amplitude without the use of limiting diodes and without drawing grid current. Combinations of double-triode valves are used for gating purposes, and they have the virtue of presenting a substantially constant load on the supply lines. This enables the present machine to be operated from completely unstabilized rectified supplies. In some installations it has, however, been thought desirable to use a servo-controlled variable auto-transformer to reduce the variation in input supply voltage to reasonable proportions.

(6.1) Marginal Checking

Circuits of this type also allow the use of an effective marginal checking system. This has been incorporated throughout the machine in a form which permits immediate measurement of the margin of safety of an individual circuit element or allows the entire computer to be checked to ensure that no safety margin is less than a preset amount.

The operation of the system is typified by reference to the bistable trigger circuit of Fig. 2. The direction of current flow through the valve when the trigger is in the normal ('off') conditions is indicated by the arrow, and the left- and right-hand grid potentials are then zero and $+13{\cdot}6$ volts, respectively. The cathode potential will be slightly above that of the right-hand grid, i.e. about $+15\frac{1}{2}$ volts. This gives a current of $11{\cdot}5$ mA

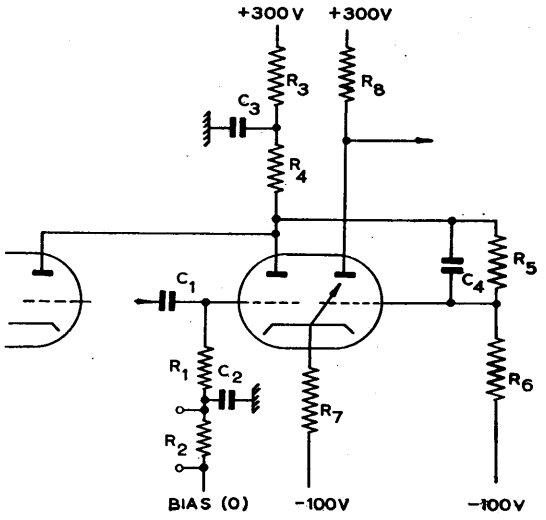

Fig. 2.—Bistable trigger circuit.

R_1 = 100 kilohms	R_7 = 10 kilohms
R_5 = 1 kilohm	R_8 = 2·7 kilohms
R_3 = 6·8 kilohms	C_1 = 1 000 $\mu\mu$F
R_4 = 2·7 kilohms	C_2 = 0·01 μF
R_5 = 220 kilohms	C_3 = 0·05 μF
R_6 = 91 kilohms	C_4 = 1 500 $\mu\mu$F

in the load resistor R_8, and provides a margin of safety against conduction to the left-hand anode of $(15{\cdot}5 - V_c)$ volts, where V_c is the cut-off grid potential appropriate to an anode–cathode potential of nearly 300 volts, and is about 10 volts for the type of valve used. The safety margin is therefore 5½ volts.

When the trigger circuit is set, by means of a narrow current pulse through a valve sharing the left-hand anode load R_3 and R_4, conduction is switched to this anode, and the right-hand grid potential falls to −13·9 volts. Since the cathode potential is now held at about +2 volts by the left-hand grid, a similar safety margin of 6 volts is now available.

The two margins of safety may be directly measured under operating conditions by injecting a measured current into a known resistor R_2, thus altering the left-hand grid potential until failure, using a suitable test programme, occurs.

It should be noted that the bias potential (in this case zero) applied to the left-hand grid is derived not from earth but from a cathode-follower valve, common to many such circuits, whose grid potential is determined by a stable potential divider connected between the +300 and −100-volt lines. The need for relative stabilization of these lines is therefore eliminated. A number of keys permit the bias lines generated by a number of cathode-followers to be varied simultaneously or independently by a preset amount (±2½ volts) to facilitate detection of any circuit which is approaching the limit of safe operation. This can arise through a number of causes, of which the following are the most important:

(*a*) Loss of emission in the valve, causing a reduction in grid-cathode potential, and subsequently lowering the grid potential of the conducting side through grid current.

(*b*) Loss of amplitude of driving or resetting pulses.

(*c*) Drift in values of R_5, R_6 or in extreme cases of R_3, R_4.

(6.2) The Magnetic-Drum Store

The magnetic drum[7] has a rotation speed of one revolution in nine major cycles, corresponding to about 6 500 r.p.m., and is driven by a 3-phase hysteresis motor fed in turn by a hard-valve amplifier. Since the main computer is controlled by a crystal oscillator it is necessary to provide accurate control of the rotor position, as no buffer store is used between the drum and the mercury store. A disc having around its periphery 1 024 teeth, each located within 2′ of arc of its nominal position, generates a waveform in an inductive pick-up head. After amplification this waveform is compared in phase with a corresponding one derived from the crystal oscillator. The resultant error signal is used to control the phase of the 3-phase supply to the drum motor, which runs at synchronous speed.

The drum itself is 4 in in diameter and 4½ in long, and consists of a centrifugally-cast phosphor-bronze sleeve, ground to a concentricity and parallelism better than 0·0002 in (total). The magnetic coating is a dispersion of magnetic iron oxide in a cold-setting epoxy resin, and is applied by spraying the drum as it revolves slowly.

The reading and writing heads are similar, and are constructed of laminated Mumetal. Each head consists of three washers, the two outer ones being cut back so that the thickness at the nose is that of one lamination only. The centre lamination is 0·006 in thick in the case of the writing heads, but is reduced to 0·004 in for the reading heads to ensure that the latter are not influenced by spurious signals outside the written track. All heads have a nominal gap at the nose of 0·001 in determined by an insert of beryllium–copper foil.

The heads are cemented to aluminium-alloy supports, which in turn are secured to a tube forming the movable assembly for a set of 16 heads. This latter process is carried out under a microscope to ensure that the tolerances of 0·000 25 in on gap alignment and spacing between heads are not exceeded. A complete head block assembly is shown in Fig. 3. This assembly is mounted with the cylindrical end shafts in linear bearings attached to top and bottom of the fixed sleeve which is visible to the right of the drum in Fig. 4. A similar sleeve at the left-hand side of the drum carries the other head assembly.

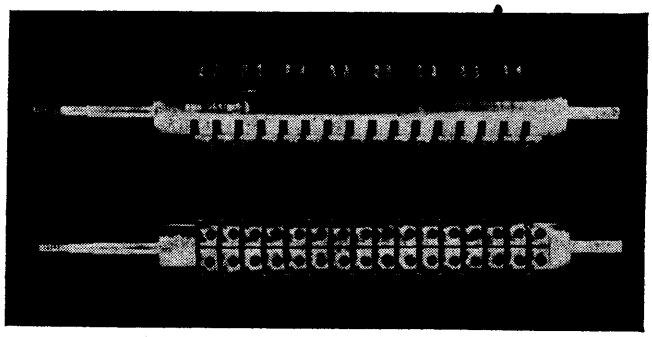

Fig. 3.—Magnetic-drum head assembly.

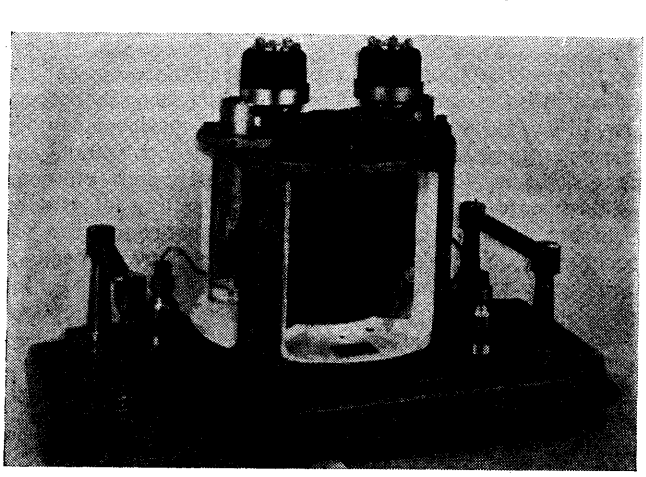

Fig. 4.—Magnetic-drum store.

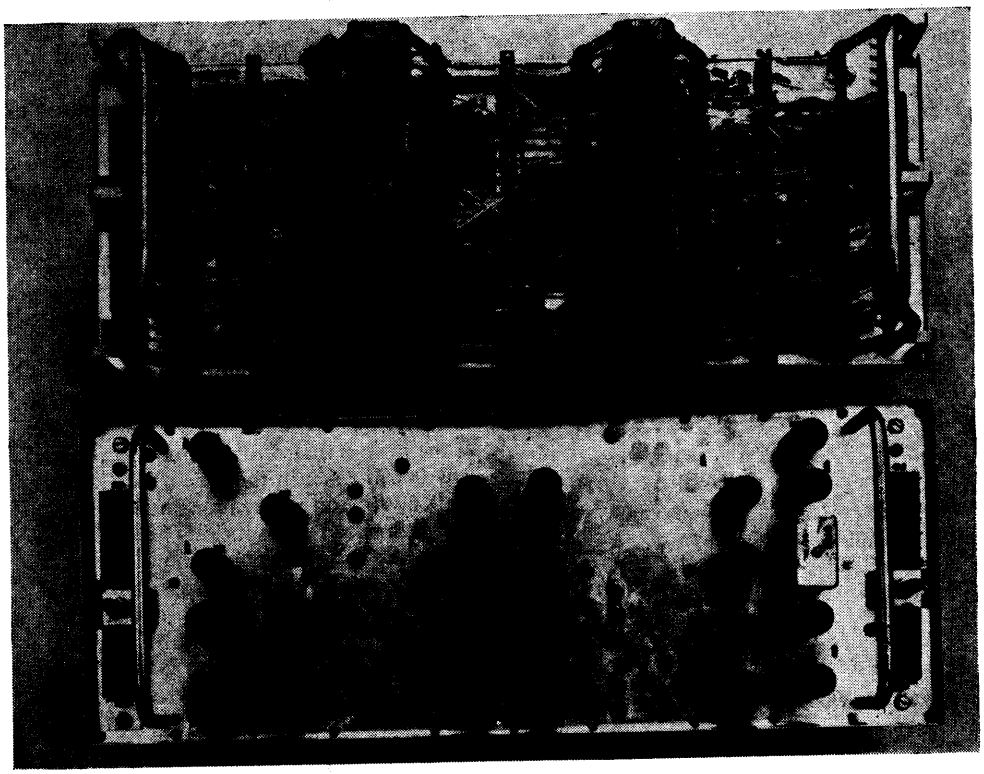

Fig. 5.—A typical pair of units in the computer.

The vertical position of each head stick is determined by a servo system whose position-sensing element is a contact on a lever arm picking off a voltage from a wire-wound potentiometer. The 4 : 1 mechanical magnification of the lever arm is necessary to give the required discrimination on the potentiometer. The voltage sensed by the contact arm is compared with a voltage obtained by analogue determination of the position demanded, and drives a moving-coil permanent-magnet linear motor through a valve amplifier.

The heads in each assembly are spaced vertically at intervals of $\frac{1}{4}$ in, and the assembly can be moved through $\frac{5}{64}$ in to provide access to the groups of 16 recording tracks, which are spaced $\frac{1}{64}$ in centre-to-centre, and have an actual recording width of approximately 0·006 in determined by the thickness of the head lamination. The gain and stability of the servo system are such that alignment of corresponding reading and writing heads is maintained within ±0·000 5 in over a period of weeks. The permissible misalignment before faulty operation ensues is approximately 0·003 in, so that readjustment of the d.c. amplifier, whose drift is the cause of such misalignment, is rarely necessary.

It will be observed from Fig. 4 that both mechanisms use the same potentiometer sensing element. Relative positional errors due to slight non-linearity of the winding are thereby eliminated.

Adjustments are provided to permit setting of the head assemblies at the correct angular spacing around the drum circumference, and also to adjust the gap between heads and drum surface to its nominal value of 0·000 75 in.

(7) PHYSICAL FORM OF THE COMPUTER

No effort has been made to minimize the space occupied by the computer. Instead, attention has been given to full accessibility of all components under operating conditions, with the object of making possible rapid location and repair of faults. The circuits of the computer fall conveniently into groups of 20 to 30 valves, and a typical pair of units, each accommodating one of these groups, is shown in Fig. 5. It will be seen that the valves are mounted in three double rows on one side of the chassis, together with relays, screened transformers and other bulky components. On the other side are mounted resistors, capacitors and other small items, on inclined tag strips. Below the tag strips are placed bias-line decoupling capacitors and similar trouble-free components. A mounting-board above the tag strips carries the sockets associated with the marginal checking system described in Section 6.1.

Groups of these units are mounted, with the plane of the chassis vertical, in racks, each of which can accommodate up to eight units. The depth of the racks is 11 in, and two groups of five are mounted back-to-back with a corridor 2 ft 8 in wide between them giving access to the valve side of the units. The floor space occupied is about 11 ft 6 in × 4 ft 6 in, with an additional 2 ft 6 in at one end where the control desk is positioned.

Fig. 6 is a photograph of a typical installation, showing the control-desk end of the main assembly with the two punched-card machines on either side. On the right is the power supply unit, containing metal rectifiers for the h.t. supplies, together with protective circuits. In the background is the cylindrical thermostatic enclosure containing the long delay lines, which are operated at a nominal temperature of 50° C. Head amplifiers connected to the quartz crystals of the delay lines are mounted on the gallery surrounding the top of the enclosure.

Because of the generous spacing and conservative rating of components, forced cooling of the computer is unnecessary. However, unless the computer room is adequately ventilated the power dissipated in the machine (approximately 7 kW) may cause discomfort to the operators, and it is therefore usual to draw air through the computer from an outside source and to exhaust it outside the machine room, unless the location of the computer renders this method of ventilation impracticable.

The form of construction adopted and the philosophy of

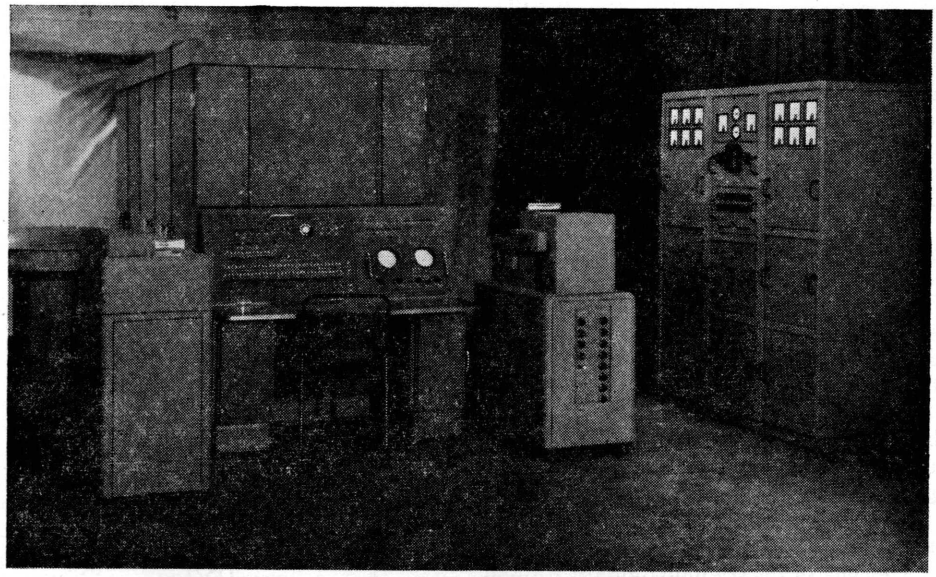

Fig. 6.—A Deuce installation.

carrying out fault location and repair with the units *in situ* have been amply justified by experience. Use of the marginal checking features permits detection of incipient faults before these are serious enough to affect normal work. The great majority of faults occurring during scheduled operating periods are therefore complete failures, such as failure of valve heaters. It is found that, by use of the very comprehensive set of diagnostic test programmes, faults of this type are rapidly localized, and the accessibility of all components for waveform examination or repair has reduced the average loss of time per fault to about 10 min.

This factor was somewhat uncertain when development of the computer commenced, and for this reason all units were designed to permit rapid replacement from a stock of spares should it be found that servicing occupied an undue proportion of machine time. No spare units are, however, maintained with any of the present installations, thus avoiding also the requirements for provision of special test equipment for servicing units removed from the computer.

The computer uses a total of about 1 450 valves, the numbers of various types being shown in Table 1.

Table 1

DISTRIBUTION OF VALVE TYPES

	Quantity
ECC91	732
Z77	375
6CH6	130
EB91	34
2D21	33
EL81	4
12AT7	90
12E1	6
12BH7	50

With the exception of the 12AT7, all valves are of standard commercial types, as these are found to have very satisfactory performance in this application. Supplies of type 12AT7 were found unduly prone to failure of one or both halves of the series-connected heater, and have therefore been replaced by a premium version which has given complete satisfaction. The rate of valve failure from all causes corresponds to an average life of some 40 000 hours. No machine has yet been in operation for more than 3 000 hours, so that this mean life is not conclusive but no indications have appeared that the rate of failure is increasing.

Before being incorporated in a computer, all valves are subjected to ageing for 100 hours, during which time alternating voltages are applied to anode and grid to give operating conditions near the manufacturers' limits. Before and after this ageing period all valves are subjected to static tests, corresponding in most cases to the equivalent CV specifications, but types ECC91 and Z77 are subjected to special tests under conditions representative of those encountered in the machine. About 10% of the total number of valves tested are rejected, the majority being type ECC91 which are unsuitable because of unbalance between the two triode sections. In addition, a number fail during the 100-hour test.

(8) APPLICATIONS

Deuce was designed primarily for scientfiic and technical calculations, which, in general, are characterized by large amounts of computation per unit of input and output information. In such applications its great speed is used to the best advantage. This work also demonstrates clearly the benefit of a large high-speed storage system in enabling the computer to work effectively at the speed of which its arithmetic system is capable, and also in reducing the number of instructions (and therefore the programming effort) involved purely in organizing the data stored in a manner leading to efficient computation.

Where some sacrifice in speed for the sake of ease of programming is permissible the large overall capacity of the store permits the use of large-scale interpretive routines. The construction of such a routine, of course, requires considerable effort, but effects great economies in total programming time when many problems of the same class are to be solved. A typical example is a set of matrix manipulative routines which permit almost any long sequence of matrix operations to be performed, only a few minutes being required to assemble the programme for any particular sequence.

Other examples of the use of the computer in engineering applications are described elsewhere.[8,9,10,11]

Problems in commerce and accountancy, by contrast, usually

involve large quantities of input and output data, with a relatively trivial amount of computation per item. Here the speed of Deuce can only be usefully employed if the rate of input and output can be matched to the computing speed. Fortunately in most of these problems the whole of the input data is not new, nor is the whole of the output required in punched card or printed form. A typical example is that of factory stock control. In its simplest form, this requires a number of items of information relevant to each of a large number of parts or materials to be stored in semi-permanent form. This information corresponds to the bin cards of conventional stores accounting, but can also include a number of matters previously dealt with by separate procedures. The whole of this information is never required simultaneously, so that it can conveniently be stored on magnetic tape—alterations to stock, indications of necessary action, etc., being communicated to and from the tape by means of punched cards. To enable Deuce to be used for work of this type, provision has been made in its design for the addition of magnetic-tape units, to be controlled in a manner similar to the punched-card input and output. The provision of these tape units permits the extension of the storage capacity of the computer almost without limit, and allows transfers to and from the computing store at rates very much higher than can be achieved by the use of punched cards.

It is also possible to extend the instruction code of Deuce to enable it to control directly other means of input and output, of which punched paper tape, electric typewriters and high-speed direct printers are examples.

(9) ACKNOWLEDGMENTS

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(11) APPENDIX

(11.1) Source and Destination Numbers

No.	Source	Destination
0	Input Dynamicizor	Control Register
1	DL1	DL1
2	DL2	DL2
3	DL3	DL3
4	DL4	DL4
5	DL5	DL5
6	DL6	DL6
7	DL7	DL7
8	DL8	DL8
9	DL9	DL9
10	DL10	DL10
11	DL11	DL11
12	DL12	DL12
13	TS13	TS13
14	TS14	TS14
15	TS15	TS15
16	TS16	TS16
17	QS17	QS17
18	QS18	QS18
19	DS19	DS19
20	DS20	DS20
21	DS21	DS21
22	DS21 ÷ 2	Add into DS21
23	TS14 ÷ 2	Subtract from DS21
24	TS14 × 2	Trigger circuits
25	TS14 & TS15	Add into TS13
26	TS14 ≠ TS15	Subtract from TS13
27	P1	Discriminate (positive/negative)
28	P17	Discriminate (zero/non-zero)
29	P32	Output staticizor
30	Zero	Magnetics head select
31	Ones (i.e. − P1)	Magnetics position select

Long Delay Lines DL1–8 are available as 'Next Instruction Sources' and have *NIS* numbers 1, 2 . . ., 7, 0, respectively.

(11.2) Trigger Instructions

The operation performed by a transfer to destination 24 is determined by the source number as follows:

Instruction	Operation
0–24	Multiply
1–24	Divide
2–24	TIL to discriminator
3–24	TCA on
4–24	TCB off
5–24	TCB on
6–24	Alarm off
7–24	Alarm on
8–24	Clear output staticizor
9–24	Stop card reader and punch
10–24	Start card punch
12–24	Start card reader

(11.3) Explanatory Notes

Many of the sources and destinations listed above operate as described in Section 3. Certain others do not effect normal transfers, and these are described in subsequent paragraphs.

(*a*) *Destination Triggers.*—Operations of the type discussed in Section 3, whether involving arithmetic operations or not, have in common the necessity of transferring information within the store. Certain other necessary facilities do not require such transfer, and are grouped together with a 'pseudo-destination' numbered 24. A 'transfer' to this destination sets up some required circuit condition dependent on the source number chosen. For example, the operation 12–24 starts the motor of the punched card reader which is the primary source of input information, and 7–24 causes an alarm buzzer at the operator's console to b

sounded. This latter facility can be used, for instance, to give warning of the failure of a programme check.

When destination 24 is selected, the main source gate specified by the instruction is also opened, allowing information from some delay line to flow on to the main highway, but no transfer takes place, as none of the normal destination gates are open.

(*b*) *Multiplication and Division.*—Both multiplication and division are performed by the long accumulator DS21 in conjunction with single-word store TS16. To carry out a multiplication the multiplicand is placed in TS16 and the multiplier in one position in DS21, the other half being cleared. Multiplication is then initiated by the instruction 0–24 (using destination Triggers) and proceeds automatically during the subsequent 65 minor cycles. In this time all other facilities of the machine are available for independent use. Since the multiplier does not produce automatically a product having the correct sign, this time is frequently used to generate by subroutine the appropriate correcting term which is added to the product immediately it becomes available. Such subroutines also contain the necessary instructions for shift and round-off of the corrected product if these operations are required. The multiplier is lost in the course of the multiplication as the double-length product is built up in DS21, but the multiplicand remains available in TS16.

The sequence of operations for division is similar, the divisor being stored in TS16 with the single-length dividend in DS21. Division is initiated by the instruction 1–24, and results in generation of the quotient in DS21 in 66 minor cycles. In this case the result carries the appropriate sign, and the time occupied by division is again available for parallel operations.

(*c*) *Trigger TCB.*—The principal function of DS21 is in connection with multiplication and division operations, and for addition and subtraction of double-length numbers using destinations 22 and 23. Stimulation of a trigger circuit TCB by the instruction 5–24 introduces carry suppression between the two words of the store, and allows it to be used for two independent single-length numbers. Under these conditions all facilities other than multiplication remain available, so that DS21 then operates as two additional single-word accumulators, with additive and subtractive inputs.

The 'right shift' (division by 2) facility provided by source 22 is similarly operative, treating the content of DS21 as a 64-digit number if TCB is off, and as two independent 32-digit numbers if TCB is on. Under the latter condition it is, of course, possible to shift both or only one of the two numbers by a transfer lasting for the appropriate period.

The instruction 4–24 restores the trigger TCB to its normal condition.

(*d*) *Trigger TCA.*—The long delay line DL10 and the single-word line TS16 normally operate as completely independent stores. Execution of the instruction 3–24, however, connects the two lines in series; DL10 retains its circulation path, but that of TS16 is broken, so that source 16 now emits the information stored in DL10 but delayed by one word time. If, therefore, the instruction 16–10 is obeyed for 32 consecutive minor cycles, using the block transfer instruction previously described, the words stored in DL10 will be re-stored in positions one removed from their previous position.

This facility is of value, for example, in calculations producing successive results by repeated execution of the same group of instructions. Suppose that a first result y_0 has been computed and is placed in storage location 10_0 (i.e. in minor cycle 0 of DL10). The instruction 16–10, occupying 32 minor cycles with TCA switched on now shifts y_0 to position 10_1.

Repetition of the group of instructions will place the second result y_1 in the now vacant space 10_0, and a further shift leaves y_0 in 10_2, y_1 in 10_1. The process may be continued until 32 results have been obtained, when y_0 will be in 10_{31}, y_1 in 10_{30}, etc.

At this stage the whole content of DL10 may be transferred elsewhere for storage while further results are computed, or, alternatively, further shifting operations interlaced with output instructions will make the stored results available in the order $y_0, y_1, \ldots, y_{32}$ from minor cycle 0 of DL10 for binary-decimal conversion and output.

Trigger TCA is restored to its normal condition by any transfer to destination 16.

(*e*) *Discrimination Operations.*—Two separate instructions are provided to permit branching out of iterative loops of instructions. These are associated with destination 27 and 28. A number may be sent from any source to either of these destinations, and the normal sequence of instructions is broken if certain conditions are fulfilled. If, for example, a number is sent to D28, the next instruction is taken from the normal position only if the digits of the number sent are all '0'. If any non-zero digit is present (i.e. if the number itself is other than zero) the next instruction is taken from one position later in the specified delay line than would otherwise have been the case.

Destination 27 operates in a similar manner, but examines only the most significant digit of the number sent to it. Throughout the computer, negative numbers are represented in complement form, so that a '0' in the most significant position corresponds to a positive number, while a '1' in this position indicates a negative number. This destination therefore permits discrimination between positive and negative numbers, and again chooses either the normal next instruction or the subsequent one.

A further special discrimination instruction uses destination Triggers. The instruction 2–24 enables a special signal (TIL), emitted by card reader and punch at a time corresponding to the last row of a card, to be sent to the discriminator, so that the programme can be made to branch after reading or punching the last row.

(*f*) *Useful Constants.*—Sources 27–31 provide the following fixed numbers:

S27	P_1, the least significant digit.
S28	P_{17}, a digit in the 17th position of the word.
S29	P_{32}, the most significant digit.
S30	0
S31	'1's (i.e. − 1 in complement notation).

The usefulness of each of these sources is self-evident except in the case of S28. This digit is made available from a separate source as it is the least significant digit of that part of the instruction word representing the wait number. By successive addition of this digit to the instruction it is therefore possible to cause it to refer to successive storage positions in a long delay line. This affords a second method of carrying out operations of the type exemplified in (*d*), and is preferable in many circumstances as it is not restricted to a particular delay line.

(*g*) *Delay Lines QS17 and QS18.*—These two delay lines (quadruple stores) each provide storage for four words. They provide a valuable addition to the quick-access storage, which is particularly useful in some types of calculation. Each has a source and destination, but no additional facilities are associated with these lines.