MB01

MULTIBUS HOST ADAPTER

TECHNICAL MANUAL

PRELIMINARY

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WARNING

This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions in this technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Commission (FCC) Rules, which are designed to provide reasonable protection against such interference in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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EMULEX PRODUCT WARRANTY

CONTROLLER WARRANTY: Emulex warrants for a period of twelve (12) months from the date of shipment that each Emulex Controller Product supplied shall be free from defects in material and workmanship.

During this period, if the customer experiences difficulties with an Emulex controller and is unable to resolve the problem via the phone with Emulex Technical Support, a Return Authorization will be issued. Following receipt of a Return Authorization, the customer is responsible for returning the product to Emulex, freight prepaid. Emulex, upon verification of warranty will, at its option, repair or replace the controller in question, and return to the customer freight prepaid.

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Section 1
GENERAL DESCRIPTION

1.1 OVERVIEW

The MB01 Host Adapter was designed by Emulex Corporation to interface Multibus host computer systems with Small Computer Standard Interface (SCSI) device controllers. The MB01 Host Adapter integrates a variety of 5.25-inch Winchester-type disk drives and/or 0.25-inch cartridge tape drives into a Multibus host system. These additional disk drives or tape drives greatly expand Multibus system storage and backup capabilities. This manual is designed to help you install and program your MB01 Host Adapter, and to provide information about buffering and signal translation capabilities. The contents of the seven sections are described briefly below.

Section 1 General Description: This section contains an overview of the major factors that contribute to the characteristics of the MB01 Host Adapter.

Section 2 MB01 Host Adapter Specifications: This section contains specifications for the major parameters of the MB01 Host Adapter.

Section 3 Installation: This section contains information necessary to install the MB01 Host Adapter in your system.

Section 4 Registers and Programming: This section provides general programming information and contains a description of the registers in the MB01 Host Adapter.

Section 5 Functional Description: This section describes the architecture of the MB01 Host Adapter.

Section 6 Interfaces: This section describes the Multibus and SCSI bus interfaces; it includes information on SCSI bus signals and timing.

Section 7 SCSI Bus Protocol: This section describes phases, phase sequencing, and bus conditions necessary for the SCSI bus protocol.

For reference convenience, Section 1 is divided into eight subsections, as listed in the following table:

Subsection	Title
1.1	Overview
1.2	Physical Description
1.3	Functional Description
1.4	SCSI Bus Description
1.5	Multibus Description
1.6	Models and Options
1.7	Features
1.8	Compatibility

1.1.1 RELATED DOCUMENTS

This manual is designed for MB01 Host Adapter users, including O.E.M. system programmers who are writing programs for operating system drivers and support utilities. Familiarity with the SCSI standard and the IEEE 796 specification is assumed.

The SCSI command set for the MB01 Host Adapter is based on the ANSI X3T9.2/82-2 Rev. 14 (01 May 84) SCSI Specification. SCSI bus protocol supported by the MB01 Host Adapter is the same as specified in the ANSI SCSI specification.

Multibus protocol supported by the MB01 Host Adapter is the same as specified in the IEEE Microcomputer System 796 bus standard.

1.1.2 TECHNICAL MANUAL CONVENTIONS

To avoid possible confusion with other uses of the same words, throughout this manual we use the following conventions:

- All SCSI commands (such as **READ**, **WRITE**, and **INQUIRY**) are printed in uppercase boldface.
- All SCSI status codes and error messages (such as CHECK CONDITION and DRIVE NOT READY) are printed in uppercase.
- All SCSI bus phases and conditions (such as Arbitration Phase) and SCSI Command Descriptor Block names (such as Inquiry Data Format) are printed in initial caps.
- All Multibus register offsets and SCSI command and message codes are printed in hexadecimal notation.

1.2 PHYSICAL DESCRIPTION

The MB01 Host Adapter, shown in Figure 1-1, is assembled on a single board (approximately 7-inches by 12-inches) and plugs directly into the backplane of the Multibus host system.

The MB01 Host Adapter contains two major integrated circuits (ICs):

- an Intel 8237 Direct Memory Access (DMA) Controller which controls DMA operations for the MB01 Host Adapter
- an NCR 5385 SCSI Protocol Controller which controls SCSI bus protocol between the MB01 Host Adapter and SCSI bus devices.

The MB01 Host Adapter also contains a 20-Megahertz (MHz) on-board clock. All MB01 Host Adapter timing control circuitry uses this on-board clock, except for the Multibus arbitration circuitry. That circuitry is synchronized with the Bus Clock on the Multibus host system.

The MB01 Host Adapter is a standard Multibus Printed Circuit Board Assembly (PCBA). Connector P1 provides the main standard interface to the Multibus backplane. Connector P2 provides connections for the auxiliary signals that are necessary if a 24-bit address extension is required. A connector keying slot is located on connector P2 between pins 15-16 and 17-18.

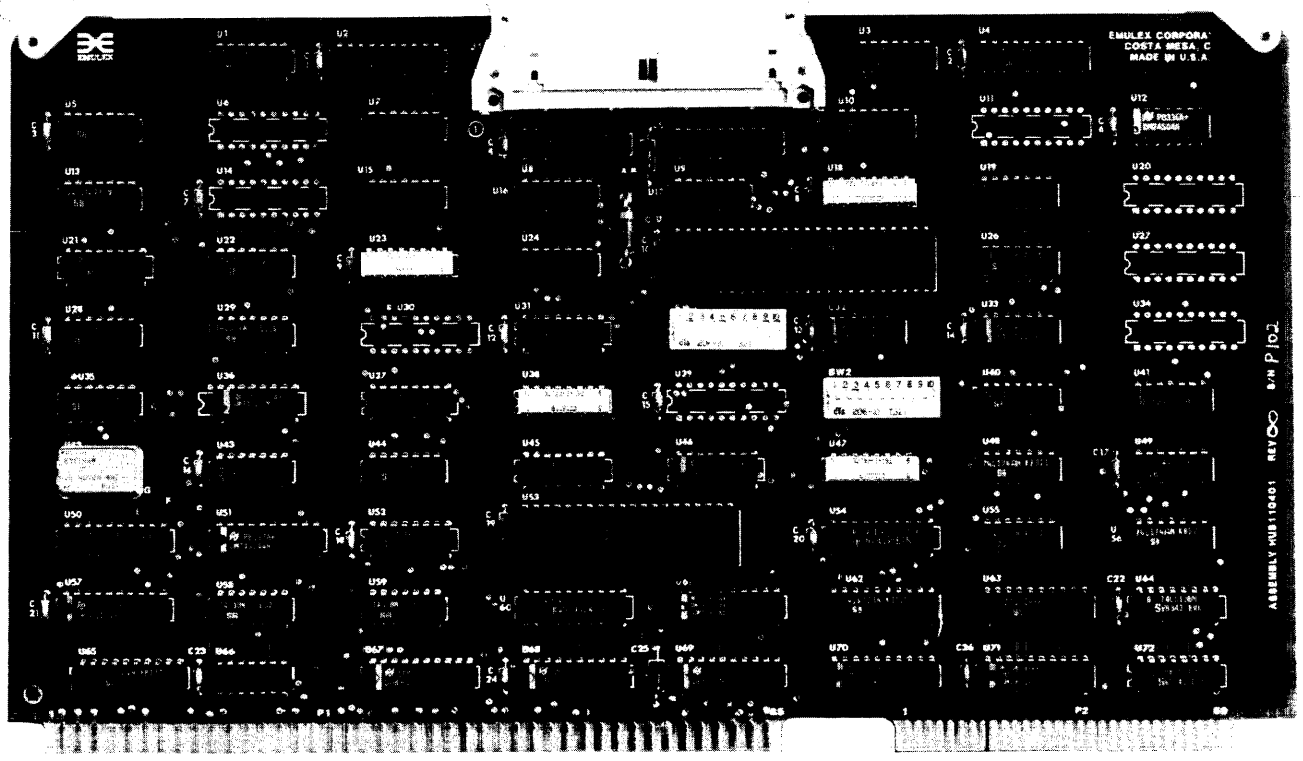


Figure 1-1. MB01 Host Adapter

The MB01 Host Adapter contains a 50-pin SCSI bus DB50 connector, reference designated J1. The MB01 Host Adapter complies with the FCC limits for a Class A computing device. A shielded cable must be used to connect the MB01 Host Adapter with SCSI Bus devices.

1.3 FUNCTIONAL DESCRIPTION

The MB01 Host Adapter is designed to allow Multibus host computers to interface with several different kinds of SCSI bus disk and tape controllers. The MB01 Host Adapter provides signal translation between the Multibus and the SCSI bus. The SCSI bus supports up to eight controller devices and their associated peripheral devices. The controller devices are daisy-chained together.

The MB01 Host Adapter provides the Multibus host system with peripheral device independence, accomplished via the SCSI bus. The protocol used on the SCSI bus does not distinguish between different kinds of mass-storage-device controllers; e.g., to the SCSI bus, tape drive controllers resemble hard disk drive controllers. Thus, device-drive software programs for SCSI bus disk drive controllers and tape drive controllers can be supplied by the user. Once such programs are supplied, SCSI bus controllers connected to the MB01 Host Adapter without further modification of the hardware or software for the Multibus host system. Because the MB01 Host Adapter controls the SCSI bus protocol, the Multibus CPU is freed from overhead that would otherwise be required to process SCSI bus protocol. (SCSI bus protocol is described in Section 7.)

1.4 SCSI BUS DESCRIPTION

The SCSI bus supports up to eight host adapters or controllers for disk or tape devices. The MB01 Host Adapter hardware supports any combination of host systems, intelligent controllers, and intelligent peripheral devices. SCSI bus configurations that can be connected to the Multibus via the MB01 Host Adapter and SCSI bus are described in subsection 7.2. Since the MB01 Host Adapter hardware supports multiple host adapters and devices, O.E.M. users can write software to support an environment for multiple SCSI bus host adapters.

SCSI bus signals and timing are described in Section 6 (Interfaces). SCSI bus protocol, including bus phases and phase sequencing, is described in Section 7 (SCSI Bus Protocol).

The SCSI command set supported by the MB01 Host Adapter is independent from the type of controller for the peripheral device (disk drive or tape drive) attached to the SCSI bus, because it masks the internal structure of the device (cylinders, tracks, data blocks, etc.) from the SCSI bus. To determine the I/O task to be performed during SCSI bus I/O operations, the device controller uses the MB01 Host Adapter to initially read the contents of a command descriptor

block (CDB) from the Multibus host memory. The controller then reads from or writes to a host memory data block (via the MB01 Host Adapter) as an I/O task proceeds. At the end of an I/O operation, the controller writes the status information to a status block located in host memory.

1.5 MULTIBUS DESCRIPTION

The Multibus is a commercial-quality bus designed for use with microcomputer systems. The Multibus is a backplane in the host system. Printed circuit boards, called modules, are connected to the Multibus backplane. The modules act as master devices and/or slave devices on the Multibus.

Master modules are able to control the Multibus; they contain either a Central Processing Unit (CPU) or logic dedicated to Multibus Data Transfer operations between the master module and other devices. Master modules are usually CPU boards and/or controller boards. Slave modules are not capable of controlling the Multibus; they execute the commands issued by master modules. Slave devices are usually memory boards or I/O boards.

Multibus Handshake operations (the exchange of predetermined signals) between master and slave modules allow modules with different data-throughput rates to be interfaced via the Multibus. During a typical Handshake operation, a master module gains control of the Multibus, specifies the address of a slave module attached to the Multibus, and issues commands to that slave module. The slave module then decodes its address and executes the commands issued by the master module.

1.6 FEATURES

This subsection describes the major features which the MB01 Host Adapter hardware provides for use with SCSI-compatible device controllers.

1.6.1 MB01 HOST ADAPTER SCSI BUS FEATURES

MB01 Host Adapter hardware provides a bidirectional information path between the SCSI bus and the Multibus. It also ensures data integrity and proper performance of the SCSI I/O subsystems by controlling SCSI bus protocol (see Section 7). MB01 Host Adapter hardware communicates via the SCSI bus with any controller for disk drives or tape drives that is compatible with the SCSI Specification.

The MB01 Host Adapter can act as either a SCSI bus Target or as a SCSI bus Initiator. It supports the SCSI optional disconnect and reconnect feature. This capability allows the MB01 Host Adapter, when it acts as a Target, to disconnect from the SCSI bus, perform its operation, reconnect to the SCSI bus, and then continue the operation.

The MB01 Host Adapter provides SCSI bus controllers with a DMA path to and from the Multibus host memory. This DMA path enables those controllers to perform the following functions:

- Read contents of command descriptor blocks (CDBs) from Multibus host memory. Each CDB describes one of the commands in the SCSI command set (SCSI commands are defined in the ANSI SCSI Specification listed in subsection 1.1.1).

- Read from and write to addressed disk or tape on the associated disk or tape drive during Read and Write operations.

1.6.2 MB01 HOST ADAPTER MULTIBUS FEATURES

The MB01 Host Adapter allows multiple master modules to be connected to the Multibus for support of multiprocessing operations. The Multibus provides control signals for connecting multiple masters in one of two priority techniques: serial or parallel. The priority technique is switch selectable (by using switch SW1-4 on the MB01 Host Adapter) and determines the method by which master modules arbitrate for control of the Multibus. For more information on the Multibus arbitration techniques supported by the MB01 Host Adapter, see subsection 4.9.1.3).

The Multibus supports two independent address spaces: memory and I/O. During Memory Addressing operations, the Multibus allows up to 16 megabytes of memory to be directly addressed by using a 24-bit addressing procedure. During I/O operations, the Multibus allows up to 64 kilobytes of I/O addresses to be addressed by using a 16-bit addressing procedure.

The Multibus supports a 8-bit or 16-bit address path during Data Transfer operations. These Data Transfer operations occur during Memory Addressing or I/O operations. The address path is switch selectable by using switch SW1-8 on the MB01 Host Adapter.

The MB01 Host Adapter supports Multibus Vectored and Nonvectored Interrupt operations. During Vectored interrupt operations, the slave module transfers the Interrupt Vector Address via the Multibus to the Multibus CPU. During Nonvectored Interrupt operations, the Interrupt Vector Address is not transferred via the Multibus; the master module performs and processes its own Interrupt operation. For more information about Multibus Interrupt operations supported by the MB01 Host Adapter, see subsection 4.9.1.2.

1.6.3 DMA OPERATION

The MB01 Host Adapter supports DMA Data Transfer operations for transferring data, status, and commands between the Multibus CPU and SCSI bus controllers. The DMA path from the MB01 Host Adapter to Multibus host memory allows the SCSI bus controller to use the designated DMA channel (specified in the General Status Register, see subsection 4.8) to read the contents of the CDB and to move data. The MB01 Host Adapter supports a DMA burst speed of up to 500 kilobytes/second and has a DMA address capacity of up to 16 megabytes. MB01 Host Adapter DMA Data Transfer operations are controlled by the on-board DMA Controller.

1.6.4 MB01 HOST ADAPTER I/O OPERATIONS

The MB01 Host Adapter supports standard Multibus I/O operations. When the MB01 Host Adapter is operating in the Programmed I/O mode (see subsection 4.9.1.1), the Multibus CPU reads from or writes to MB01 Host Adapter I/O registers. Dual In-line Package (DIP) switch SW2 on the MB01 Host Adapter is used to select the starting base I/O address for MB01 Host Adapter registers. These registers include the internal registers for the SCSI Protocol Controller and for the DMA Controller.

1.6.5 CONFIGURATION SWITCHES

Two DIP switch packages are on the MB01 Host Adapter. Switch SW1 is a ten-pole general-control switch pack used to configure the following functional criteria:

- SCSI device IDs
- the Interrupt Channel to be used by the MB01 Host Adapter
- the Address Path selection (8-bits or 16-bits)
- the Multibus Arbitration Technique (serial or parallel)
- a Software Programming Option.

Switch SW2 is the ten-pole switch pack used to configure the base address for MB01 Host Adapter registers. For more information about configuration switches, see Section 3, (Installation).

1.7 COMPATIBILITY

This section describes compatibility characteristics of MB01 Host Adapter hardware and software with Multibus host systems and SCSI device controllers.

1.7.1 SCSI BUS COMPATIBILITY

Compatibility of the MB01 Host Adapter with SCSI bus controllers and related peripheral devices is described in the following subsections.

1.7.1.1 Hardware Compatibility

The MB01 Host Adapter supports the SCSI bus single-ended option. A DB50 connector, reference designated J1 on the MB01 Host Adapter, plugs directly into the SCSI bus. The cumulative length of the daisy-chain cable that connects the SCSI peripheral devices should be not longer than 6 meters. All SCSI signals in the cable are terminated at each end to +5 Volts direct current (Vdc) with 220-Ohm resistors and to ground with 330-Ohm resistors. Terminator installation is optional and depends on the physical profile of the SCSI bus (e.g., terminators would be installed if the MB01 Host Adapter is to be used in an environment that includes one or more Emulex subsystems). The MB01 Host Adapter complies with the FCC limits for a Class A computing device (see subsection 3.5).

1.7.1.2 Software Compatibility

The MB01 Host Adapter and **user-supplied software** controls SCSI bus protocol and the signal translation between the Multibus and SCSI bus. The MB01 Host Adapter supports the SCSI arbitration capability, reselection capability, data bus parity, and all standard SCSI commands described in the ANSI X3T9.2 SCSI specification.

1.7.2 MULTIBUS COMPATIBILITY

Compatibility of the MB01 Host Adapter with the Multibus hardware and software is described in the following subsections.

1.7.2.1 Hardware Compatibility

The MB01 Host Adapter plugs directly into the Multibus backplane. The MB01 Host Adapter follows the physical and mechanical requirements described for Multibus printed circuit boards in the IEEE Microcomputer System 796 bus standard.

1.7.2.2 Software Compatibility

The MB01 Host Adapter follows standard Multibus protocol. As a Multibus element, it can act as either a master module or as a slave module. It matches all IEEE 796 Specification slave module (board) requirements. As a Multibus master, the MB01 Host Adapter can perform only the direct access of Multibus host memory during a DMA Data Transfer operation.

The MB01 Host Adapter supports both an 8-bit and 16-bit address path (the address path selection is switch selectable by using switch SW1-3 on the MB01 Host Adapter). The MB01 Host Adapter supports the two Multibus Interrupt operation techniques (Vectored and Nonvectored) outlined in the IEEE 796 Specification. The MB01 Host Adapter can be used in a Multibus arbitration mode with either the serial technique or the parallel technique (for more information about these techniques, see subsection 4.9.1.2).

1.7.3 COMPATIBILITY WITH OTHER EMULEX PRODUCTS

Emulex currently offers three microcontrollers that can be used on the SCSI bus with the MB01 Host Adapter: the Titleist, Medalist, and Champion. The Titleist tape controller interfaces with the SCSI bus and with the Cipher 540 Streaming Cartridge Tape Drive. The Medalist disk controller interfaces with the SCSI bus and with all 5.25-inch Winchester-type disk drives that use the standard ST506 interface. The Champion disk controller interfaces with the SCSI bus and with all 5.25-inch disk drives that use the Enhanced Small Disk Interface (ESDI).

In addition to basic stand-alone controller products, Emulex also offers complete packaged subsystems for micro-applications that use disk drives and tape drives compatible with the SCSI bus.

Section 2
MB01 HOST ADAPTER SPECIFICATIONS

2.1 OVERVIEW

This section contains the general, electrical, and physical specifications for the parameters of the MB01 Host Adapter. A general description of each parameter is included under **FUNCTIONAL** in the General and Electrical Specifications table. For a detailed description of the overall functional relationships applicable to the MB01 Host Adapter, see Section 4, Registers and Programming. The general, electrical, and physical specifications for MB01 Host Adapter are described in separate subsections as listed in the following table:

Subsection	Title
2.1	Overview
2.2	General and Electrical Specifications
2.3	Physical Specifications

2.2 GENERAL AND ELECTRICAL SPECIFICATIONS

Table 2-1 lists and describes the general and electrical specifications for the MB01 Host Adapter.

Table 2-1. General and Electrical Specifications

Parameter	Description
FUNCTIONAL	
Design	Host adapter for integration of SCSI peripheral disk and tape device controllers with Multibus host CPU
Option Switches	On-board DIP switches for selection of configuration options
INTERFACES	
Multibus Interface	Standard Multibus interface (IEEE 796 Microcomputer Standard). All signals have loads less than three TTL.
DMA Address Range	Up to 16 megabytes
DMA Data Transfer Operations	8-bit word. DMA burst speed can be up to 1.05 microseconds/byte in Single-Byte DMA Data Transfer mode
Host Adapter Address	Switch selectable to cover all host adapter assignments
Peripheral Interface	SCSI (ANSI X3T9.2 Specification). Up to 7 controllers
ELECTRICAL	
SCSI Interface	SCSI (ANSI X3T9.2 Specification); approximately 6 meters (20 feet) maximum cable length
Power Required	+5 Volts Vdc ± 5%, 1.1 Amperes (A) maximum

2.3 PHYSICAL SPECIFICATIONS

Table 2-2 lists and describes the physical specifications for the MB01 Host Adapter.

Table 2-2. Physical Specifications

Parameter	Description
Packaging	One printed circuit board assembly (PCBA) with standard Multibus interface
Dimensions	approximately 17.78 cm by 30.48 cm (7-inches by 12-inches)
Mounting	Any standard slot in the backplane of the Multibus host system cabinet

3.1 OVERVIEW

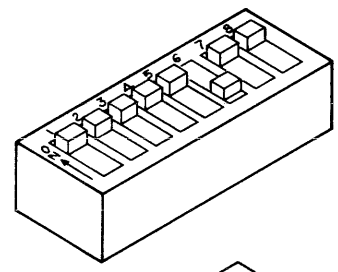
This section describes the step-by-step procedure for installing the MB01 Host Adapter, including switch-setting data and physical installation instructions. This section is divided into five subsections, as listed in the following table:

Subsection	Title
3.1	Overview
3.2	Inspection
3.3	MB01 Host Adapter Preparation
3.4	MB01 Host Adapter Installation
3.5	FCC Compliance

If not familiar with the MB01 Host Adapter installation procedures, read this Installation Section before beginning installation.

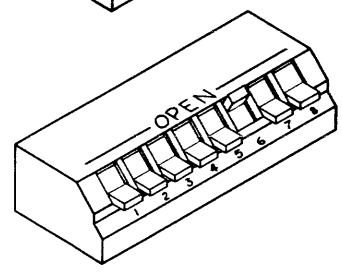
3.1.1 DIP SWITCH TYPES

DIP switch packs used in this product may be either of two types:



Slide Switch:

To place a slide switch in the ON position, simply slide the switch in the direction marked ON or CLOSED. To place a slide switch in the OFF position, simply slide the switch in the direction marked OFF or OPEN.



Piano Switch:

To place a piano switch in the ON position, move the switch toward the ON or CLOSED position. To place a piano switch in the OFF position, move the switch toward the OFF or OPEN position.

Except where noted, switch-setting tables in this manual use numeral one (1) to indicate the ON (closed) position and numeral zero (0) to indicate the OFF (open) position.

3.2 INSPECTION

Emulex products are shipped in special containers designed to provide full protection under normal transit conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

Unpack the MB01 Host Adapter and verify that all components listed on the shipping invoice are present. Verify that the model or part number (P/N) designation, revision level, and serial numbers agree with those on the shipping invoice. These verifications are important to confirm warranty. If evidence of physical damage or identity mismatch is found, notify an Emulex representative immediately.

A visual inspection of the MB01 Host Adapter is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage.

3.3 MB01 HOST ADAPTER PREPARATION

The switches in DIP switch packs SW1 and SW2 on the MB01 Host Adapter allow configuration of various options available with the MB01 Host Adapter. They are also used to establish the starting base address of the Input/Output (I/O) registers in the MB01 Host Adapter. All switches on the MB01 Host Adapter are set to a standard configuration before the MB01 Host Adapter is shipped from the factory. DIP switch functions are listed and described in applicable tables in this section. Table 3-1 lists the function and factory configuration of all switches on the MB01 Host Adapter.

Table 3-1. DIP Switch Settings, MB01 Host Adapter

Switch	Factory Setting	Function	Section
SW1-1	1 (ON/CLOSED)	SCSI Device Address (LSB)	3.3.1
SW1-2	1 (ON/CLOSED)	SCSI Device Address	3.3.1
SW1-3	1 (ON/CLOSED)	SCSI Device Address (MSB)	3.3.1
SW1-4	0 (ON/CLOSED)	Arbitration Technique Selection	3.3.2
SW1-5	0 (OFF/OPEN)	Interrupt Channel Number (LSB)	3.3.3
SW1-6	0 (OFF/OPEN)	Interrupt Channel Number	3.3.3
SW1-7	0 (OFF/OPEN)	Interrupt Channel Number (MSB)	3.3.3
SW1-8	1 (ON/CLOSED)	Address Path Selection	3.3.4
SW1-9	0 (OFF/OPEN)	Programming Option Bit 0	3.3.5
SW1-10	0 (OFF/OPEN)	Programming Option Bit 1	3.3.5
SW2-1	0 (OFF/OPEN)	I/O Address Bit 6	3.3.6
SW2-2	0 (OFF/OPEN)	I/O Address Bit 7	3.3.6
SW2-3	0 (OFF/OPEN)	I/O Address Bit 8	3.3.6
SW2-4	0 (OFF/OPEN)	I/O Address Bit 9	3.3.6
SW2-5	0 (OFF/OPEN)	I/O Address Bit 10	3.3.6
SW2-6	0 (OFF/OPEN)	I/O Address Bit 11	3.3.6
SW2-7	0 (OFF/OPEN)	I/O Address Bit 12	3.3.6
SW2-8	0 (OFF/OPEN)	I/O Address Bit 13	3.3.6
SW2-9	0 (OFF/OPEN)	I/O Address Bit 14	3.3.6
SW2-10	0 (OFF/OPEN)	I/O Address Bit 15	3.3.6
1 = ON/CLOSED		0 = OFF/OPEN	

Figure 3-1 shows the locations of the components referenced in this manual. Since the configuration switches are not accessible after installation, they must be set before the MB01 Host Adapter is installed in the Multibus backplane.

3.3.1 SCSI DEVICE ADDRESS SELECTION (SW1-1:SW1-3)

Switches SW1-1, SW1-2, and SW1-3 are used to select any one of eight possible SCSI bus device addresses. The device address establishes the SCSI bus identity of the MB01 Host Adapter in the system. The eight possible MB01 Host Adapter device address identities are listed in Table 3-2. Do not assign the same device address to two separate SCSI host adapters or controllers.

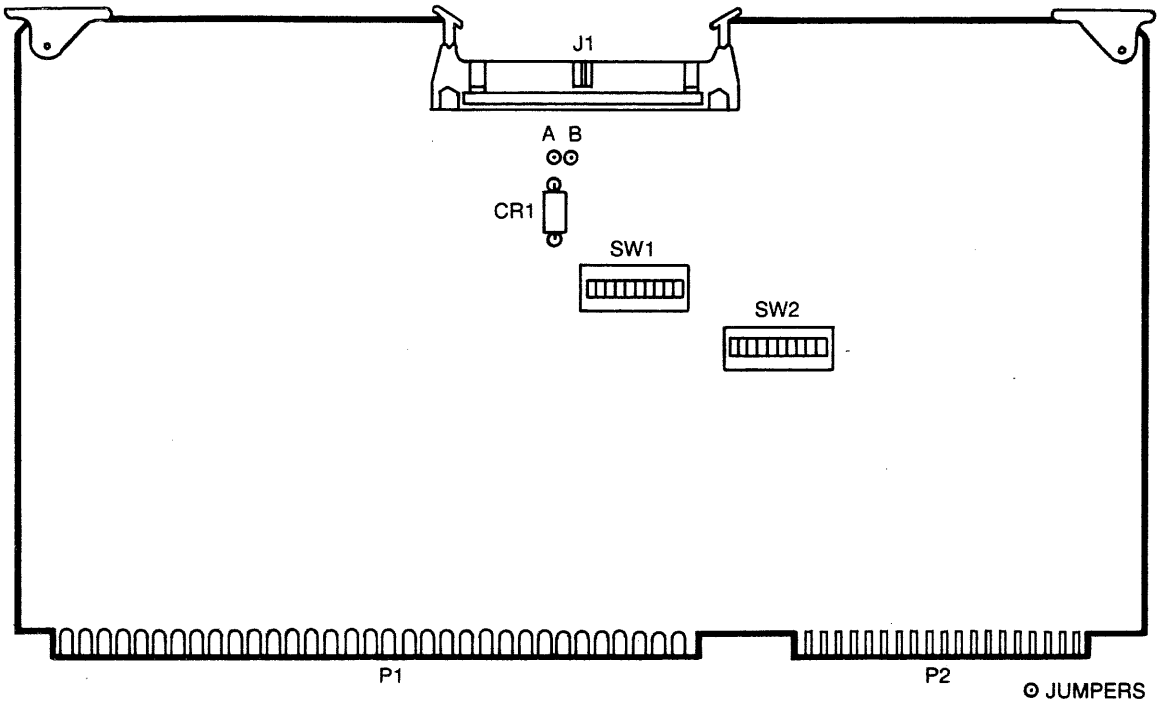


Figure 3-1. MB01 Host Adapter Component Locations

Table 3-2. SCSI Bus Device Address Selection Switches

SW1-3 (MSB)	Switch SW1-2	SW1-1 (LSB)	SCSI Bus Device Address Number
0	0	0	00
0	0	1	01
0	1	0	02
0	1	1	03
1	0	0	04
1	0	1	05
1	1	0	06
1	1	1	07
1 = ON/CLOSED 0 = OFF/OPEN			

3.3.2 ARBITRATION TECHNIQUE SELECTION (SW1-4)

The setting of switch SW1-4 determines the Arbitration Technique (serial or parallel) used by the MB01 Host Adapter. Setting this switch in the ON (closed) position causes the MB01 Host Adapter to use the Serial Arbitration Technique when contending for control of the Multibus. Setting this switch in the OFF (open) position causes the MB01 Host Adapter to use the Parallel Arbitration Technique when contending for control of the Multibus.

The Arbitration Technique is selected by switch SW1-4. Normally, switch SW1-4 is set in the OFF position, as listed in the following table:

Switch	OFF	ON	Factory
SW1-4	Parallel	Serial	OFF

3.3.3 INTERRUPT REQUEST LINE SELECTION (SW1-5:SW1-7)

Switches SW1-5, SW1-6, and SW1-7 are used to select any one of eight possible Interrupt Request Lines on the Multibus host system. Multibus Interrupt Request Lines are listed in Table 3-3.

Table 3-3. Multibus Interrupt Request Line Selection Switches

SW1-7 (MSB)	Switch SW1-6	SW1-5 (LSB)	Multibus Interrupt Channel
0	0	0	INT7*
1	0	0	INT6*
0	1	0	INT5*
1	1	0	INT4*
0	0	1	INT3*
1	0	1	INT2*
0	1	1	INT1*
1	1	1	INT0*
1 = ON/CLOSED 0 = OFF/OPEN			
* indicates signal assertion is at low voltage level			

3.3.4 ADDRESS PATH SELECTION (SW1-8)

The setting of switch SW1-8 determines the Address Path (8-bit or 16-bit) used by the MB01 Host Adapter during Data Transfer operations. Setting this switch in the ON (closed) position causes the MB01 Host Adapter to use a 16-bit address path. Setting this switch in the OFF (open) position causes the MB01 Host Adapter to use an 8-bit address path.

The Address Path is selected by switch SW1-8. Normally, switch SW1-8 is set in the OFF position, as listed in the following table:

Switch	OFF	ON	Factory
SW1-8	8-bit	16-bit	OFF

3.3.5 PROGRAMMING OPTION (SW1-9:SW1-10)

Switches SW1-9 and SW1-10 are reserved for software options to be provided by the O.E.M. user. The Programming Option selection is software-defined. SW1-9 is associated with program switch 0 and SW1-10 is associated with program switch 1.

The Programming Option is selected by switches SW1-9 and SW1-10. Normally, switches SW1-9 and SW1-10 are set in the OFF position, as listed in the following table:

Switch	OFF	ON	Factory
SW1-9	Software-Determined	Software-Determined	OFF
SW1-10	Software-Determined	Software-Determined	OFF

3.3.6 MB01 HOST ADAPTER BASE I/O REGISTER ADDRESS SELECTION (SW2-1:SW2-10)

Host adapter or controller devices connected to the Multibus have several command and status registers. The Multibus host CPU uses those registers to command and monitor these devices. The registers in the MB01 Host Adapter are sequentially addressed, beginning with a starting I/O address located in Multibus host memory. This address is called the Register Base Address. All MB01 Host Adapter I/O registers are located at a fixed offset from the Register Base Address. The Register Base Address is established with switches on DIP switch pack SW2. (For more information on MB01 Host Adapter registers, see Section 4.)

3.4 MB01 HOST ADAPTER INSTALLATION

To install the MB01 Host Adapter in the Multibus host system, see Figure 3-2 and use the general procedure described below. The actual procedure followed is dependent on the configuration of the host system.

1. Power down Multibus host system.

2. Remove cover from Multibus host system.

3. Verify the configuration of the MB01 Host Adapter is completed (see subsection 3.3). Configuration involves setting switches SW1-1 through SW1-10 and SW2-1 through SW2-10 before inserting MB01 Host Adapter in selected Multibus backplane slot. All switches have been set at the factory; however, resetting of certain switches may be necessary to satisfy specific needs of the system.

4. Plug MB01 Host Adapter into Multibus backplane slot (see Figure 3-2). The component side of the MB01 Host Adapter must face in the same direction as the other modules in the Multibus backplane. Verify the edge connectors on the PCBA are properly positioned in the throat of the backplane connector, then seat the PCBA by pressing on the extractor handles.

5. Connect the SCSI bus cable to the MB01 Host Adapter.

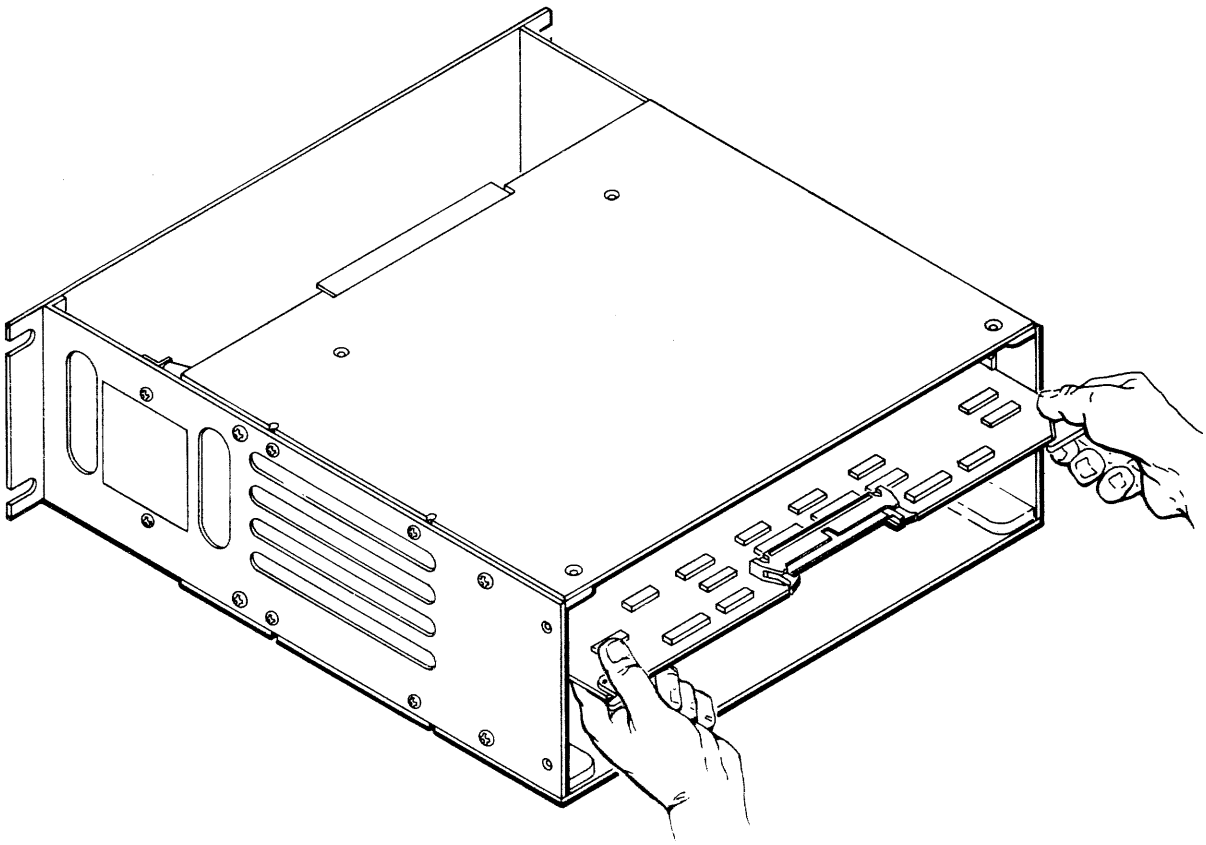


Figure 3-2. Installing MB01 Host Adapter in Multibus Backplane

3.5 FCC COMPLIANCE

The Federal Communications Commission (FCC) has established technical standards for limiting emission of radio-frequency interference (RFI) by computing devices. The MB01 Host Adapter has been type tested and found to comply with the emission limits for a Class A computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules. There is no guarantee, however, that RFI may not occur in a particular installation.

The MB01 Host Adapter was tested for FCC compliance in a compliant Multibus host system that was properly shielded (enclosed so that no FRI escapes). During testing, the MB01 Host Adapter was installed in a system that provided a ground for the SCSI bus cable. The system was connected to other SCSI bus port devices via a shielded SCSI cable. For information about SCSI bus cable and connector requirements, see subsection 6.3.1.

Since the MB01 Host Adapter equipment generates and uses radio frequency energy, it may cause RFI with radio and television reception in a residential environment. The user is responsible for taking whatever measures are required to prevent RFI. Emulex is not responsible for any RFI caused by unauthorized modifications to the MB01 Host Adapter.

4.1 OVERVIEW

This section contains a detailed description of the MB01 Host Adapter I/O registers used to temporarily hold Input/Output (I/O) data. This section also includes general programming information designed to aid the programmer in writing software to be compatible with the MB01 Host Adapter. This section is divided into nine subsections, as listed in the following table:

Subsection	Title
4.1	Overview
4.2	MB01 Host Adapter Registers Description
4.3	MB01 Host Adapter DMA Registers
4.4	MB01 Host Adapter SCSI Bus Registers
4.5	SCSI Bus Reset Register
4.6	Release SCSI Bus Reset Register
4.7	Interrupt Mode Registers
4.8	General Status Register
4.9	General Programming Information

4.2 MB01 HOST ADAPTER REGISTERS DESCRIPTION

When the MB01 Host Adapter is operating in the Programmed I/O mode, the Multibus CPU (hereafter called CPU) writes to or reads from MB01 Host Adapter registers. In this mode, MB01 Host Adapter registers must occupy 48 contiguous locations of the Multibus host system I/O space. The 48 contiguous locations of I/O space (which correlate to the MB01 Host Adapter registers) must stay within a boundary of 64 locations, but they can be biased to any 64 boundaries of free Multibus host I/O address space. The MB01 Host Adapter registers include the internal registers for the on-board NCR 5385 SCSI Protocol Controller and the internal 8237 DMA Controller.

A Multibus host system can have an 8-bit wide or 16-bit wide I/O address path. The MB01 Host Adapter can accommodate either one of these structures. MB01 Host Adapter registers are sequentially addressed beginning with an I/O base address, called the Register Base Address. An MB01 Host Adapter register address is issued in terms of an offset from the Register Base Address. To obtain the correct address for a specific MB01 Host Adapter register, add the offset of the register to the Register Base Address (The Register Base Address and the offsets are specified in hexadecimal notation.)

The Register Base Address is established by setting switches SW2-1 through SW2-10 on the MB01 Host Adapter (see Table 3-1). The Multibus host system determines the MB01 Host Adapter Register Base Address by comparing Address lines A15 through A6 with the settings of switches SW2-1 through SW1-10 on the MB01 Host Adapter. In an 8-bit wide I/O address path system, the Multibus host system ignores Address lines A15 through A8.

For quick reference, Figure 4-1 shows the entire MB01 Host Adapter register set. The mnemonic terms for the bits are the same as those used in the more complete descriptions that follow. The subsection numbers in Figure 4-1 reference the appropriate descriptions for the register.

4.3.1 CURRENT ADDRESS REGISTER (CAR) +0

07	06	05	04	03	02	01	00
Current Address							

Read-Only

4.3.2 BASE ADDRESS REGISTER (BAR) +0

07	06	05	04	03	02	01	00
Base Address							

Write-Only

4.3.3. CURRENT WORD COUNT REGISTER (CWCR) +1

07	06	05	04	03	02	01	00
Current Word Count							

Read-Only

4.3.4 BASE WORD COUNT REGISTER (BWCR) +0

07	06	05	04	03	02	01	00
Base Word Count							

Write-Only

4.3.5 COMMAND REGISTER (CMDR) +8

07	06	05	04	03	02	01	00
SDA	SDR	WRS	0	TMS	CLE	X	0

Write-Only

4.3.6 STATUS REGISTER (STR) +8

07	06	05	04	03	02	01	00
0	0	0	DRQ	0	0	0	CTC

Read-Only

Figure 4-1. MB01 Host Adapter Registers (Sheet 1 of 5)

4.3.7 REQUEST REGISTER (RQR) +9

07	06	05	04	03	02	01	00
X	X	X	X	X	SR	0	0

Write-Only

4.3.8 MASK REGISTER (MSKR) +A

07	06	05	04	03	02	01	00
X	X	X	X	X	CSM	0	0

Write-Only

4.3.9 MODE REGISTER (MODE) +B

07	06	05	04	03	02	01	00
MDS		IDS	APE	TRT		0	0

Write-Only

4.3.10 CLEAR BYTE POINTER (CBP) +C

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X

Write-Only

4.3.11 TEMPORARY REGISTER (TEMP) +D

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X

Read-Only

Figure 4-1. MB01 Host Adapter Registers (Sheet 2 of 5)

4.3.12 MASTER CLEAR (MSCL) +D

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X

Write-Only

4.3.13 CLEAR MASK REGISTER (CMSK) +E

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X

Write-Only

4.3.14 MASK REGISTER (MASK) +F

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	SMB

Write-Only

4.3.15 DMA ADDRESS REGISTER (DAR) +23

07	06	05	04	03	02	01	00
DMA Address (Top 8 bits)							

Write-Only

4.4.1 DATA REGISTER (DATR) +10

07	06	05	04	03	02	01	00
SCSI Command, Data, Status, or Message							

4.4.2 COMMAND REGISTER (CMDR) +11

07	06	05	04	03	02	01	00
DMO	SBT	0	Command Code				

Figure 4-1. MB01 Host Adapter Registers (Sheet 3 of 5)

4.4.3 CONTROL REGISTER (CTRLR) +12

07	06	05	04	03	02	01	00
X	X	X	X	X	PEN	REN	SEN

4.4.4 DESTINATION ID REGISTER (DIDR) +13

07	06	05	04	03	02	01	00
0	0	0	0	0	Destination ID		

4.4.5 AUXILIARY STATUS REGISTER (ASR) +14

07	06	05	04	03	02	01	00
DRF	PER	MSG	C/D	I/O	PS	TCZ	X

Read-Only

4.4.6 ID REGISTER (IDR) +15

07	06	05	04	03	02	01	00
0	0	0	0	0	Device ID		

Read-Only

4.4.7 INTERRUPT REGISTER (IR) +16

07	06	05	04	03	02	01	00
X	IVC	X	RES	SE	DSC	BUS	FNC

Read-Only

4.4.8 SOURCE ID REGISTER (SIDR) +17

07	06	05	04	03	02	01	00
IDV	X	X	X	X	Source ID		

Read-Only

Figure 4-1. MB01 Host Adapter Registers (Sheet 4 of 5)

4.4.9 DIAGNOSTIC STATUS REGISTER (DSR) +19

07	06	05	04	03	02	01	00
SDC	X	Diagnostic Command Status				Self-Test Status Code	

Read-Only

4.4.10 TRANSFER COUNTERS +1C, +1D, +1E

4.5 SCSI BUS RESET REGISTER (SBR) +20

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X

Write-Only

4.6 RELEASE SCSI BUS RESET REGISTER (RSR) +27

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X

Write-Only

4.7.1 VECTOR 0 REGISTER +21

07	06	05	04	03	02	01	00
Vector 0 Data							

Write-Only

4.7.2 VECTOR 1 REGISTER +22

07	06	05	04	03	02	01	00
Vector 1 Data							

Write-Only

4.8 GENERAL STATUS REGISTER (GSR) +24

07	06	05	04	03	02	01	00
POSW		ICS			SPV	SBRF	DTO

Read-Only

Figure 4-1. MB01 Host Adapter Registers (Sheet 5 of 5)

4.3 MB01 HOST ADAPTER DMA REGISTERS

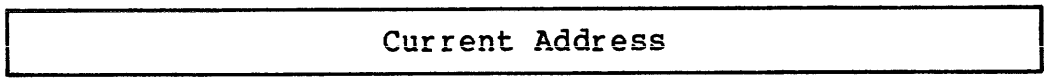
Twenty-one MB01 Host Adapter registers are used by the CPU to direct DMA Data Transfer operations on DMA Channel 0, the DMA channel used by the MB01 Host Adapter. DMA Data Transfer operations allow SCSI bus peripheral devices to directly transfer information to or from Multibus host memory. The registers are listed in Table 4-1 and described in the following subsections. The offset from the Register Base Address for each register is listed in Table 4-1 and is shown next to the register name in Figure 4-1 and in each detailed register description.

When the MB01 Host Adapter has no valid DMA requests pending, it is in the Idle (inactive) state. During this state, it can be in the Program Condition in which the CPU is programming it for a DMA Data Transfer operation. When the MB01 Host Adapter is performing a DMA Data Transfer operation, it is in the Active state.

Table 4-1. MB01 Host Adapter DMA Operation Register Summary

Offset	Operation	Register Name
+0	Read-Only	Current Address Register (CAR)
+0	Write-Only	Base Address Register (BAR)
+1	Read-Only	Current Word Count Register (CWCR)
+1	Write-Only	Base Word Count Register (BWCR)
+2	Read/Write	Reserved
+3	Read/Write	Reserved
+4	Read/Write	Reserved
+5	Read/Write	Reserved
+6	Read/Write	Reserved
+7	Read/Write	Reserved
+8	Write-Only	Command Register (CMDR)
+8	Read-Only	Status Register (STR)
+9	Write-Only	Request Register (RQR)
+A	Write-Only	Mask Register (MSKR)
+B	Write-Only	Mode Register (MODE)
+C	Write-Only	Clear Byte Pointer (CBP)
+D	Read-Only	Temporary Register (TEMP)
+D	Write-Only	Master Clear Command (MSCL)
+E	Write-Only	Clear Mask Register Command (CMSK)
+F	Write-Only	Mask Register (MASK)
+23	Write-Only	DMA Address Register (DAR)

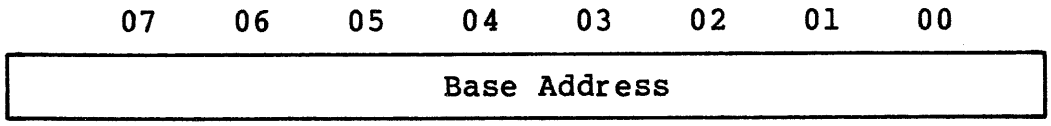
4.3.1 CURRENT ADDRESS REGISTER (CAR) +0



Read-Only

The 8-bit, Read-only Current Address Register (CAR) contains the current address for DMA Channel 0. MB01 Host Adapter hardware automatically increments or decrements the current address after each DMA Data Transfer operation. Intermediate values of the current address are stored in the CAR during the Data Transfer operation. The CPU reads the contents of this register in successive 8-bit bytes. The CAR may also be reinitialized to its original value after an Autoinitialize procedure occurs (see APE bit description in subsection 4.3.9). An Autoinitialize procedure occurs only after an End-of-Process (EOP) signal is asserted. (An EOP signal terminates an active DMA service.)

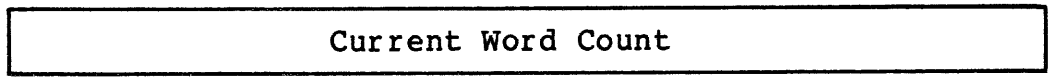
4.3.2 BASE ADDRESS REGISTER (BAR) +0



Write-Only

The 8-bit, Write-only Base Address Register (BAR) is used to store the original value of the CAR. During the Autoinitialize procedure, the MB01 Host Adapter uses the values in the BAR to restore the CAR to its original value. The CPU writes the contents of the BAR simultaneously with the contents of the corresponding CAR in two 8-bit bytes (for a total of 16 bytes) when the MB01 Host Adapter is in the Program Condition (the CPU is programming it for a DMA Data Transfer operation).

4.3.3 CURRENT WORD COUNT REGISTER (CWCR) +1



Read-Only

The 8-bit, Read-only Current Word Count Register (CWCR) is used to determine the number of words to be transferred (designated the Word Count) in a DMA Data Transfer operation which uses DMA Channel 0. The actual number of DMA Data Transfer operations is one more than the number programmed in the CWCR; i.e., if a Word Count of 100 has been programmed, 101 words are transferred by the DMA Data Transfer operation. The Word Count is decremented after each Data Transfer operation is completed. The intermediate value of the Word Count is stored in the CWCR during the Data Transfer operation. When the value in the CWRC goes from zero to FFFF (hexadecimal), a Terminal Count (TC) is generated.

The CPU reads the contents of the CWCR in successive 8-bit bytes in the Program Condition. At the end of a DMA service, the CWCR may also be reinitialized by an Autoinitialize procedure to its original value. If an Autoinitialize procedure does not occur after a TC is generated, the CWCR has a Word Count of FFFF (hexadecimal).

4.3.4 BASE WORD COUNT REGISTER (BWCR) +0

07	06	05	04	03	02	01	00
Base Word Count							

Write-Only

The 8-bit, Write-only Base Word Count Register (BWCR) is used to store the original value of the CWCR. During an Autoinitialize procedure, the values in the BWCR are used to restore the CWCR to its original value. The CPU writes to the BWCR, when it reads the contents of the corresponding CWCR in 8-bit bytes in the Program Condition.

4.3.5 COMMAND REGISTER (CMDR) +8

07	06	05	04	03	02	01	00
SDA	SDR	WRS	0	TMS	CLE	X	0

Write-Only

The 8-bit, Write-only Command Register (CMDR) is used to control the operation of the internal DMA Controller. The CPU programs the CMDR when the MB01 Host Adapter is in the Program Condition. A Reset condition or Master Clear instruction (see section 4.3.12) clears the CMDR.

Sense of DMA Acknowledge (SDA) - Bit 07

The SDA bit status indicates which state of the DMA Acknowledge (DACK) signal for DMA Channel 0 is to be active. The DACK signal is used to notify a SCSI bus Target device when it has been granted a DMA cycle to perform a Data Transfer operation. When the SDA bit status is set to one, the DACK signal is active high. When the SDA bit is reset to zero, the DACK signal is active low. A Reset condition causes the DACK signal lines to be initialized to active low.

Sense of DMA Request (SDR) - Bit 06

The SDR bit status indicates which state of the DMA Request (DREQ) signal for DMA Channel 0 is to be active. The DREQ signal is used by SCSI bus Target devices to obtain DMA service. A request is generated by activating the DREQ line of DMA Channel 0. A DACK signal acknowledges the recognition of a DREQ signal. The DREQ signal must be asserted until the corresponding DACK signal is asserted. A Reset condition initializes the DREQ signal to active high. When the SDR status bit is set to one, the DREQ signal is active low. When the SDR status is reset to zero, the DREQ signal is active high.

Write Selection (WRS) - Bit 05

The WRS bit status indicates one of two Write Selection types: Extended Write Selection, and Late Write Selection.

During DMA Data Transfer operations, the Extended Write Selection function takes one cycle longer to complete than the Late Write Selection function. When the WRS bit status is set to one, the Extended Write Selection function is active. When the WRS bit status is reset to zero, the Late Write Selection function is active. If the Timing Selection (TMS) bit status (CMDR bit 03) is set to one, the WRS bit status can be either one or zero. If the TMS bit is reset to zero, the WRS bit status must be zero.

Timing Selection (TMS) - Bit 03

The MB01 Host Adapter has two modes of timing for DMA Data Transfer operations: Compressed Timing and Normal Timing.

Compressed Timing is used to achieve faster data throughput where Multibus host system characteristics permit. It compresses the Data Transfer operation time to one clock cycle less than normal. Normal Timing is the standard timing used by the internal DMA Controller on the MB01 Host Adapter. It is the timing mode **recommended** for use unless the Block Transfer mode is being used, see the status of the MDS bits (MODE bits <07:06>). When the TMS bit status is set to one, Compressed Timing is in effect. When the TMS bit status is reset to zero, Normal Timing is in effect.

When the compressed Timing and Block Transfer modes are used, the fastest DMA burst speed becomes available. The obtainable data-throughput rate is a function of the data-throughput rates supported by the Multibus and the SCSI bus.

Controller Enable (CLE) -Bit 02

The CLE bit indicates whether the DMA Controller is or is not to begin the DMA Data Transfer operation by starting at the location specified in the CAR. When the CLE bit status is set to one, the DMA Controller is disabled; when the CLE bit status is reset to zero, the DMA Controller is enabled.

Not Used - Bit 01

The status of this bit may be either one or zero.

NOTE

Throughout this manual, bit positions designated by a zero state are not defined.

4.3.6 STATUS REGISTER (STR) +8

07	06	05	04	03	02	01	00
0	0	0	DRQ	0	0	0	CTC

Read-Only

The 8-bit, Read-only Status Register (STR) contains information about the status of the selected SCSI bus device during a DMA Data Transfer operation by that device. This information indicates when DMA Channel 0 has reached a Terminal Count (TC) and/or when DMA Channel 0 has a pending DMA request.

DMA Channel 0 DMA Request (DRQ) - Bit 04

When the DRQ bit status is set to one, DMA Channel 0 is requesting service.

DMA Channel 0 Terminal Count (CTC) - Bit 00

When the CTC bit status is set to one, DMA Channel 0 has reached a TC. The CTC bit is set to one whenever a TC is reached by DMA Channel 0 or whenever an external End-of-Process (EOP) is generated. A Reset condition clears the CTC bit.

4.3.7 REQUEST REGISTER (RQR) +9

07	06	05	04	03	02	01	00
X	X	X	X	X	SR	0	0

Write-Only

The 4-bit, Write-only Request Register (RQR) enables the MB01 Host Adapter to respond to requests for DMA service that are initiated by software as well as by a hardware DREQ signal. DMA Channel 0 has a non-maskable software request bit (SR) associated with it in the RQR. The SR bit is set or reset separately under software control to indicate a software-initiated request for DMA service. The SR bit is cleared when a TC signal or an external EOP signal is generated. A Reset condition clears the entire RQR.

Not Used - Bits <07:03>

The status of these bits may be either one or zero.

Software Request (SR) - Bit 02

The SR bit status indicates when a software-initiated DMA request for the use of DMA Channel 0 is or is not active. When the SR bit status is set to one, software has requested the use of DMA Channel 0. When the SR bit status is reset to zero, software has not requested the use of DMA Channel 0.

4.3.8 MASK REGISTER (MSKR) +A

07	06	05	04	03	02	01	00
X	X	X	X	X	CSM	0	0

Write-Only

The 4-bit, Write-only Mask Register (MSKR) is used to indicate when DMA Channel 0 has been programmed to set the Mask Bit to disable any incoming DREQ signal. The Mask Bit is set to one when DMA Channel 0 produces an EOP (provided DMA channel 0 is not programmed to perform the Autoinitialize procedure). Each bit of the 4-bit MSKR may also be set or cleared separately under software control. A Reset condition clears the entire MSKR, which disables all DMA Data Transfer requests until a clear MSKR instruction is issued (by resetting the CSM bit to zero, see below) to allow such requests to occur. Instructions can also be issued to separately set or clear the Mask Bit by using SMD (bit 00) in the other Mask Register (MASK); see subsection 4.3.14.

Not Used - Bits <07:03>

The status of these bits may be either one or zero.

Clear/Set Mask (CSM) - Bit 02

The CSM bit status indicates when a Mask Bit is or is not set to disable any incoming DREQ signals on DMA Channel 0. When the CSM bit status is set to one, the Mask Bit is set. When the CSM bit status is reset to zero, the Mask Bit is cleared.

4.3.9 MODE REGISTER (MODE) +B

07	06	05	04	03	02	01	00
MDS		IDS	APE	TRT		0	0

Write-Only

The 8-bit, Write-only Mode Register (MODE) is associated with DMA Channel 0. When the MB01 Host Adapter is in the Program Condition, the CPU writes to the MODE to establish the Transfer Type and Transfer Mode of the DMA Data Transfer operation on DMA Channel 0.

Mode Select (MDS) - Bits <07:06>

The status of the MDS bits determines the mode of the DMA Data Transfer operation. When the MB01 Host Adapter is in the Idle Cycle (no valid DMA requests are pending) and a Target on the SCSI bus requests a DMA service on DMA Channel 0, the MB01 Host Adapter requests control of the Multibus and enters the Active Cycle. (In the Active Cycle, the MB01 Host Adapter has requested control of the Multibus, or it has control and is performing a DMA Data Transfer operation.) In the Active cycle, the DMA service can operate in one of three modes:

- Single Transfer
- Block Transfer
- Demand Transfer.

In the Single Transfer Mode, the CPU programs the MB01 Host Adapter to perform only one Data Transfer operation. The Word Count is decremented, and the address is incremented or decremented after each DMA Data Transfer operation. When the Word Count rolls over, from zero to FFFF (hexadecimal), the TC status causes an Autoinitialize procedure to occur if DMA Channel 0 has been programmed to perform that procedure.

In the Block Transfer Mode, the MB01 Host Adapter detects the asserted DREQ signal and continues to perform DMA Data Transfer operations during the DMA service until a TC status occurs, which is caused by a Word Count going to FFFF (hexadecimal), or by an external EOP signal. The DREQ signal is asserted as long as the Data Register Full (DRF) bit status in the SCSI bus Auxiliary Status Register (ASR bit 07) is set to one. If DMA Channel 0 has been programmed (in the MODE) as a channel for the Autoinitialize procedure, at the end of DMA service, an Autoinitialize procedure occurs.

In the Demand Transfer Mode, the CPU programs the MB01 Host Adapter to continue to perform DMA Data Transfer operations until a TC status occurs or until an external EOP is encountered, or until the DREQ signal is deasserted. Thus, DMA Data Transfer operations may continue as long as the data-throughput rate of the SCSI bus device continues to match the rate required for the operation to continue. After the SCSI bus device has caught up, the MB01 Host Adapter re-establishes DMA service. During the time between DMA services, the intermediate values, of Address Count and Word Count are stored in the CAR and CWCR respectively, of the MB01 Host Adapter. Only an asserted EOP signal can cause an Autoinitialize procedure to occur at the end of a DMA service. (The EOP signal is generated either by the TC status signal or by an external signal.)

NOTE

The Single Transfer mode is **recommended** as the standard mode to use with the MB01 Host Adapter. The Block Transfer mode should be used only if software can be programmed to determine the exact number of data bytes to be transferred. The Demand Transfer mode is not recommended for use unless the SCSI bus device can support a data-throughput rate of at least 750 kilobytes/second. If this last condition is met, the data-throughput rate in a Demand Transfer mode should be higher than that in the Single Transfer mode.

Address Increment/Decrement Select (IDS) - Bit 05

The CPU sets the status of this bit to indicate when the addresses for a DMA Data Transfer operation should be incremented or decremented from the starting address as the operation proceeds. When the IDS bit status is set to one, the addresses are decremented each time; when the IDS bit status is reset to zero, the addresses are incremented each time.

Autoinitialize Procedure Enable (APE) - Bit 04

The Autoinitialize procedure allows programming of DMA Channel 0 to return to its initial condition. With this feature enabled, during initialization, but after an asserted EOP signal, the original values in the CAR and CWCR for DMA Channel 0 are automatically restored from the DMA Channel 0 values residing in the BAR and BWCR. The CPU simultaneously loads the base registers with the contents of the current registers. The base registers remain unchanged throughout the DMA service. The DMA Channel 0 Mask Bit is not set (in the MASK) when the channel is in the Autoinitialize state.

When the APE bit status is set to one, the Autoinitialize procedure is enabled; when the APE bit status is reset to zero, the Autoinitialize procedure is disabled.

Transfer Type (TRT) - Bits <03:02>

Each of the three active DMA service modes (defined in the paragraphs describing the MDS bits) can perform three different types of Data Transfer operations: Write, Read, and Verify. Write Data Transfer operations move data from a SCSI bus Target device to host memory. Read Data Transfer operations move data from host memory to a SCSI bus Target device. Verify Data Transfer operations are pseudo-transfer operations. The MB01 Host Adapter operates in the Verify Transfer mode as it does in Read or Write Data Transfer operations. It generates addresses, responds to EOP, etc; however, the memory and I/O control lines all remain deasserted.

The TRT bits contain the code for the type of the DMA Data Transfer operation; the bit pattern results are listed in Table 4-2.

Table 4-2. Mode Register Transfer Type Codes

Bits 03	Bits 02	Result
0	0	Verify Transfer
0	1	Write Transfer
1	0	Read Transfer
1	1	Illegal Code

4.3.10 CLEAR BYTE POINTER (CBP) +C

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X

Write-Only

The 8-bit, Write-only Clear Byte Pointer (CBP) is used to contain a Master Clear Pointer that is one of several additional special software commands the MB01 Host Adapter can execute when it is in the Program Condition. Execution of the Master Clear Pointer command does not depend on any specific bit pattern on the internal Data Bus. The command is executed before the CPU writes or reads new Address Count or Word Count information to or from the appropriate MB01 Host Adapter register. The command initializes the internal flip-flop to a known state so that when the CPU subsequently accesses the DMA registers in the MB01 Host Adapter, the contents of the upper and lower bytes are addressed in the correct sequence.

NOTE

The internal Data Bus, Control Bus, and Address Bus (referred to in these subsections) are part of the circuitry in the DMA Controller IC on the MB01 Host Adapter.

4.3.11 TEMPORARY REGISTER (TEMP) +D

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X

Read-Only

The 8-bit, Read-only Temporary Register (TEMP) is currently not used. It may contain any bit pattern.

4.3.12 MASTER CLEAR (MSCL) +D

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X

Write-Only

The 8-bit, Write-only Master Clear Register (MSCL) is used to contain one of the special software commands executed by the MB01 Host Adapter when it is in the Program Condition. Execution of the command does not depend on any specific bit pattern on the internal Data Bus. This software instruction has the same effect on the MB01 Host Adapter as a Reset condition. It causes the Command, Status, Request, Temporary, and Clear Byte Pointer Registers to be cleared and the CSM bit (MSKR bit 02) to be set. After the software instruction is executed, the MB01 Host Adapter enters the Idle cycle.

4.3.13 CLEAR MASK REGISTER (CMSK) +E

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X

Write-Only

The 8-bit, Write-only Clear Mask Register (CMSK) is used to contain another special software command that clears the Mask Bit for DMA Channel 0; thus enabling DMA Channel 0 to accept DMA requests. This command does not depend on any specific bit pattern on the internal Data Bus.

4.3.14 MASK REGISTER (MASK) +F

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	SMB

Write-Only

The 8-bit, Write-only version of the Mask Register (MASK) allows all four bits of the Mask Register to be written by using a single software command.

Not Used - Bits <07:01>

The status of these bits may be either one or zero.

Set/Clear DMA Channel 0 Mask Bit (SMB) - Bit 00

When the SMB bit status is set to one, the Mask Bit for DMA channel 0 is set (which disables any incoming DMA requests to that DMA channel). When the SMB bit status is reset to zero, the Mask Bit for DMA channel 0 is cleared.

4.3.15 DMA ADDRESS REGISTER (DAR) +23

07	06	05	04	03	02	01	00
DMA Address (Top 8 bits)							

Write-Only

The 8-bit, Write-only DMA Address Register (DAR) holds the eight high-order address bits (A16-A23) for a DMA Data Transfer operation. Once the the MB01 Host Adapter gains control of the MUltibus to perform a DMA Data Transfer operation, the MB01 Host Adapter gains control of the Address Bus, the Data Bus, and the Control Bus (all on the Multibus). The address for the first DMA Data Transfer operation is sent in two bytes: the least significant byte (LSB) on the eight Address Bus lines (address lines A0-A7) and the most significant byte (MSB) on the internal Data Bus (D7-D0). The MB01 Host Adapter then latches the contents on address lines A8-A15 with the contents on the internal Data Bus to complete the full 16 bits of the Address Bus. After the initial DMA Data Transfer operation occurs, the latch is updated only after a carry or borrow is generated in the LSB on the address lines. The top byte (8 bits) of the DMA Address is set into this register.

4.4 MB01 HOST ADAPTER SCSI BUS REGISTERS

Sixteen MB01 Host Adapter registers are used by the CPU to transfer data, commands, and status information to and from the SCSI bus. The registers appear to the host CPU as standard I/O ports. The 16 registers are listed in Table 4-3 and described in the following subsections. The offset from the Register Base Address (selectable as listed in Table 3-2) for each register is listed in Table 4-3 and shown next to the register name in Figure 4-1 and in each detailed register description.

Table 4-3. MB01 Host Adapter SCSI Bus Register Summary

Offset	Type	Register Name
+10	Read/Write	Data Register (DATR)
+11	Read/Write	Command Register (COMD)
+12	Read/Write	Control Register (CTRLR)
+13	Read/Write	Destination ID (DIDR)
+14	Read/Write	Auxiliary Status (ASR)
+15	Read-Only	ID Register (IDR)
+16	Read-Only	Interrupt Register (IR)
+17	Read-Only	Source ID (SID)
+18	--	Reserved
+19	Read-Only	Diagnostic Status (DSR)
+1A	--	Reserved
+1B	--	Reserved
+1C	Read/Write	Transfer Counter (MSB)
+1D	Read/Write	Transfer Counter (2nd byte)
+1E	Read/Write	Transfer Counter (LSB)
+1F	--	Reserved

4.4.1 DATA REGISTER (DATR) +10

07	06	05	04	03	02	01	00
SCSI Command, Data, Status, or Message							

Read/Write

The 8-bit Read/Write Data Register (DATR) is used to store SCSI bus commands, data, status, and message bytes that are to be transferred between the Multibus host Data Bus and the SCSI bus. It is double-buffered to support the maximum data-throughput rate. In the non-DMA mode, the CPU reads from or writes to the DATR. A bit is provided in the Auxiliary Status Register (see subsection 4.4.5) to indicate when the DATR is full.

In the DMA mode, the DMA Controller in the MB01 Host Adapter reads from or writes to the DATR by responding to a DMA request with first a DACK (DMA Acknowledge) signal, and then by issuing a Read or Write signal. The SCSI bus controllers read from or write to the DATR when the MB01 Host Adapter is connected as an Initiator or Target and the SCSI bus is in one of the Information Transfer Phases (see subsection 7.3.3).

4.4.2 COMMAND REGISTER (COMD) +11

07	06	05	04	03	02	01	00
DMO	SBT	0	Command Code				

Read/Write

The 8-bit, Read/Write Command Register (COMD) is used to specify SCSI bus operations. To execute one of these operations, write to the COMD that command code which corresponds with the operation.

The contents of the COMD can be read. The MB01 Host Adapter resets the COMD when it sets an Interrupt. Therefore, data in the COMD cannot be guaranteed as being correct after an Interrupt-type of command (defined in the following paragraph) is loaded or after the Selection or Reselection command is issued. A copy of the last issued command should be stored in Multibus host memory. Immediate commands (described in the following paragraph) are not stored in the COMD.

Two types of commands are issued: Immediate and Interrupt. All Immediate command types, except Pause, cause results within three clock cycles from the time the COMD is loaded. (The Pause command is explained in subsection 4.4.2.3.) Interrupt-type commands do not result in such immediate action. When they are completed, their completion is flagged by an Interrupt Request.

DMA Mode (DMO) - Bit 07

The DMO bit status is applicable only for commands that use the Data Register. When the DMO bit status is set to one, data is transferred to or from the Data Register by using the DACK and DREQ DMA signals. When the DMO bit status is reset to zero, the CPU must monitor the DRF bit status in the Auxiliary Status Register (ASR bit 07). Data is then transferred by specifying the appropriate command code (COMD bits <04:00>). For more information on MB01 Host Adapter DMA registers, see subsection 4.3.

Single Byte Transfer (SBT) - Bit 06

When the SBT bit status is set to one, only one byte of data is to be transferred by the command. The Transfer Counter (see subsection 4.4.10) is not used or altered by the MB01 Host Adapter. Therefore, for common Single-Byte Message Transfer operations or Status Transfer operations, the Transfer Counter does not need to be loaded before issuing a command with this bit set. When the SBT bit status is reset to zero, the Transfer Counter is used by the MB01 Host Adapter to determine the number of data bytes to be transferred by the command.

Reserved - Bit 05

This bit is not used and must remain zero.

Command Code - Bits <04:00>

These bits are used to specify the hexadecimal code for the command to be executed. The commands and their corresponding bit patterns are listed in Table 4-4. The system uses two types of commands: Immediate and Interrupt.

Command codes 00000 through 00111 designate Immediate-type commands. Command codes 01000 through 10101 designate Interrupt-type commands. When an Interrupt-type command is loaded into the COMD, a second Interrupt-type command code should not be loaded until after the Interrupt requested by the first command has occurred, but an Immediate-type command may be loaded before the Interrupt requested an Interrupt-type command occurs.

Table 4-4. Command Register (COMD) Command Codes

Bits 04	03	02	01	00	Command Type	Command Code	MB01 Host Adapter Function *
0	0	0	0	0	IMM	Chip Reset	Tar/Init/Dis
0	0	0	0	1	IMM	Disconnect	Target/Init
0	0	0	1	1	IMM	Pause	Target/Dis
0	0	0	1	1	IMM	Set ATN	Initiator
0	0	1	0	0	IMM	Message Accepted	Initiator
0	0	1	0	1	IMM	Chip Disable	Tar/Init/Dis
0	0	1	1	0	--	Reserved	
0	0	1	1	1	--	Reserved	
0	1	0	0	0	INT	Select with ATN	Disconnected
0	1	0	0	1	INT	Select without ATN	Disconnected
0	1	0	1	0	INT	Reselect	Disconnected
0	1	0	1	1	INT	Diagnostic (Data Turnaround)	Disconnected
0	1	1	0	0	INT	Receive Command	Target
0	1	1	0	1	INT	Receive Data	Target
0	1	1	1	0	INT	Receive Message Out	Target
0	1	1	1	1	INT	Receive Unspecified Information Out	Target
1	0	0	0	0	INT	Send Status	Target
1	0	0	0	1	INT	Send Data	Target
1	0	0	1	0	INT	Send Message In	Target
1	0	0	1	1	INT	Send Unspecified Information In	Target
1	0	1	0	0	INT	Transfer Information	Initiator
1	0	1	0	1	INT	Transfer Pad	Initiator

IMM = Immediate INT = Interrupt ATN = Attention
Tar = Target Init = Initiator Dis = Disconnected

* The MB01 Host Adapter can function in either the Initiator or Target role if the O.E.M. user supplies appropriate software.

4.4.2.1 Chip Reset

The Chip Reset command causes all SCSI bus operations to stop and all SCSI bus registers, counters, etc. to be reset. When the CPU issues this command, that action affects the system in the same way as does the Hard Reset condition (see subsection 7.7.1).

4.4.2.2 Disconnect

When the Disconnect command is issued, all SCSI bus signal lines are immediately released and the MB01 Host Adapter returns to a Disconnected (idle) state. When the MB01 Host Adapter is connected as a Target, the Disconnected state is the normal method of disconnecting from the SCSI bus when a Data Transfer operation is completed. When the MB01 Host Adapter is connected as an Initiator, the Disconnect command may be used to release SCSI bus signal lines as a result of a timeout condition. In this last-mentioned situation, the MB01 Host Adapter ignores the Target and remains in the Disconnected state even if reselected by the Target. When the MB01 Host Adapter is in the Disconnected state, a Disconnect command cannot be issued and accepted, because such a command is not valid. If that command is issued, the MB01 Host Adapter ignores it.

4.4.2.3 Pause

When the MB01 Host Adapter is logically connected to the SCSI bus as a Target, the Pause command allows the MB01 Host Adapter to halt a Send or Receive command without having to wait for the Data Transfer operation to be completed. The Pause command is not valid when the MB01 Host Adapter is connected as an Initiator. The Pause command is a valid Immediate-type command when the MB01 Host Adapter is in the Disconnected state. A valid Pause command establishes conditions governed by the following criteria:

- When the Pause command is issued, it immediately sets a the Paused status bit in the Auxiliary Status Register (ASR bit 02). Within a one-byte Data Transfer cycle, the MB01 Host Adapter recognizes the flag, aborts the Send or Receive operation, and sets the PS status bit (ASR bit 02). Although the Paused bit is set, the MB01 Host Adapter is still connected to the SCSI bus as a Target and waits for another command.

- When the Pause command is issued, execution of the Send or Receive command is stopped, and the Transfer Counter is left in a valid state to indicate the remaining number of bytes to be transferred. Once an operation has stopped because the Pause command was issued, it may be resumed by reloading the original command into the COMD.

- After the Pause command is issued while a Send or Receive command is being executed, the MB01 Host Adapter must continue to transfer data (due to double-buffering) until the PS bit (ASR bit 02) is set or until an Interrupt occurs.

- When the Pause command is issued while the MB01 Host Adapter is in the Disconnected state after a Select or Reselect command has been issued, but before an Interrupt occurs, the Select or Reselect command is aborted by any one of two processes:

  1) If the MB01 Host Adapter has not yet won arbitration, it sets the PS bit (ASR bit 02) and waits in the Disconnected state for another command.

  2) If the MB01 Host Adapter has won arbitration, it drops the signal level on the two SCSI bus Identification (ID) lines (for the Initiator and the Target) while asserting the -SELOUT signal on the SCSI bus for not less than 100 microseconds, then checks for the absence of the -BSYIN signal on the SCSI bus, then releases the SCSI bus. After executing this event sequence that releases the SCSI bus, the MB01 Host Adapter sets the PS bit (ASR bit 02) and waits in the Disconnected state for another command.

- When the Pause command is issued while the MB01 Host Adapter is in the Disconnected state, but before a Select or Reselect command is issued, the PS bit (ASR bit 02) is immediately set and the MB01 Host Adapter waits in the Disconnected state for another command.

- Since the Pause command is an Immediate-type command, it does not cause an Interrupt to be generated. As previously explained, the MB01 Host Adapter sets the PS bit (ASR bit 02) to indicate the Pause command has been executed, but if an Interrupt-causing event occurs before the MB01 Host Adapter can set the PS bit (ASR bit 02), the MB01 Host Adapter issues an Interrupt to the CPU. In this situation, the PS bit (ASR bit 02) is never set by the MB01 Host Adapter. In all circumstances, an Interrupt-causing event takes precedence over the Pause command. For example, if the MB01 Host Adapter is connected as a Target and the -ATN signal is asserted when the Pause command is issued, a Bus Service Interrupt occurs, specified by the status of the Bus Service (BUS) bit (IR bit 01) and the PS bit (ASR bit 02) is not set.

4.4.2.4 Set ATN

The Set ATN (Attention) command causes the -ATN signal (on the SCSI bus) to be asserted immediately if the MB01 Host Adapter is connected as an Initiator. This command is invalid and ignored if issued when the MB01 Host Adapter is disconnected or when it is operating as a Target. The -ATN signal is deasserted in the Message Out Phase (see subsection 7.3.3.4) when the Transfer Counter contents become zero, or when one byte has been transferred (in a One-Byte Transfer command) during execution of a Transfer Information command (see subsection 4.4.2.13).

The MB01 Host Adapter automatically asserts the -ATN signal for two situations:

- A Select w/ATN command is issued and the MB01 Host Adapter has won arbitration.
- A parity error is detected on an input byte during execution of a Transfer Information command.

4.4.2.5 Message Accepted

The Message Accepted command is used after a Transfer Information or Transfer Pad command to notify the MB01 Host Adapter that the -ACK signal can be deasserted for the last byte. The Message Accepted command is an Immediate-type command that is valid only when the MB01 Host Adapter is connected to the SCSI bus as an Initiator.

The CPU receives a message via the Transfer Information or Transfer Pad command. If the Data Transfer operation is to be input to the CPU (-I/O signal on the SCSI bus is set to one), and if the information to be input is a message (-MSG and -C/D signals on the SCSI bus are set to one), after the MB01 Host Adapter receives the last byte, it interrupts by setting the Function Complete (FNC) bit in the Interrupt Register (IR bit 00, see subsection 4.4.7) and also asserts the -ACK signal line on the SCSI bus. By interrupting and leaving the -ACK signal line asserted, the MB01 Host Adapter allows the CPU to interpret the message and assert the -ATN signal before deasserting the -ACK signal. This action allows the MB01 Host Adapter to properly request a Message Out Phase on the SCSI bus if the Initiator wants to send a MESSAGE REJECT message (see Table 7-2) to the Target.

To enable the MB01 Host Adapter to deassert the -ACK signal, the Message Accepted command must always be issued after a Transfer Information command for a Message In Phase on the SCSI bus (regardless of whether the Set ATN command is or is not issued). If the CPU rejects the message, the Set ATN command is issued first, followed by the Message Accepted command. If the CPU accepts the message, only the Message Accepted command is issued.

NOTE

Since the -ACK signal is still asserted, the Target does not assert another -REQ signal on the SCSI bus until the Message Accepted command is issued.

4.4.2.6 Chip Disable

The Chip Disable command immediately stops all MB01 Host Adapter operations and logically disconnects it from the SCSI bus. All outputs are placed in a high-impedance state and the MB01 Host Adapter does not respond to any commands, except the Chip Reset command. When so disabled, the MB01 Host Adapter also does not respond to any activity on the SCSI bus. The only way to exit from this condition is to assert the -RST signal on the SCSI bus or to issue a Reset command.

4.4.2.7 Select with ATN

The Select with ATN command causes the MB01 Host Adapter, acting as an Initiator, to attempt to select a Target. Before the CPU issues this command, it must perform two load operations:

1. Load the Destination ID Register (DIDR) with the three-bit code for the Target that is to be selected.

2. Load the Transfer Counter for a Timeout value to begin when the selected Target responds. The Timeout value is computed by using the following equation:

   Transfer Counter = Desired Timeout/146 microseconds

If the Transfer Counter is loaded with the value zero, the MB01 Host Adapter waits indefinitely for a response from the Target that is selected.

The Select with ATN command may be used only if the MB01 Host Adapter is in the Disconnected state. If the CPU attempts to issue the Select with ATN command while the MB01 Host Adapter is not in the Disconnected state, the Invalid Command Interrupt (IVC) bit is set (IR bit 06).

When the MB01 Host Adapter detects the Select with ATN command, it attempts to arbitrate for control of the SCSI bus. If, at any time during the Arbitration Phase, the MB01 Host Adapter becomes selected or reselected by another Initiator, the Select with ATN command is aborted and the MB01 Host Adapter interrupts with a message about one of the three conditions:

- Selected
- Selected and Bus Service
- Reselected.

If the MB01 Host Adapter wins arbitration, the MB01 Host Adapter places the SCSI bus in the Selection Phase with the -ATN signal asserted, and uses the Destination ID Register (DIDR) to identify the desired Target. At the same time, the MB01 Host Adapter begins a timer based on the value for the Transfer Counter timeout computed above. If the Target does not respond within the timeout period, the MB01 Host Adapter disconnects from the SCSI bus and interrupts by setting the Disconnected (DSC) bit (IR bit 02).

NOTE

The CPU should **not** monitor the Transfer Counter Zero (TCZ) bit (ASR bit 01) to determine when a Timeout condition has occurred.

If the Target responds within the allotted time, the MB01 Host Adapter interrupts by setting the FNC status bit (IR bit 00). Control of the SCSI bus then belongs to the selected Target and after the Interrupt status has been read, another interrupt condition may occur to indicate the Target has disconnected or to indicate the Target is requesting a Data Transfer operation.

If the Timeout function is disabled and the Target does not respond, or if arbitration is not won, the only way to abort the Select with ATN command is to issue the Pause command. After the Pause command is issued, Interrupts that cause the FNC bit (IR bit 00) or Disconnect (DSC) bit (IR bit 02) to be set may still occur. These Interrupts occur if any one of these interrupt bits is set before the MB01 Host Adapter detects the Pause command, or if the Target responds while the MB01 Host Adapter is sequencing off the SCSI bus in a Timeout condition. If the MB01 Host Adapter does not set either interrupt (IR bit 00 or 02), it sets the PS bit (ASR bit 02). If this PS bit is detected after the Pause command, then the MB01 Host Adapter aborts the Select with ATN command and no connection exists.

4.4.2.8 Select without ATN

The Select without ATN command has the same effect on the system as the Select with ATN command, except the -ATN signal is not asserted during the SCSI bus Selection Phase.

4.4.2.9 Reselect

The Reselect command causes the MB01 Host Adapter, acting as a Target, to attempt to reselect an Initiator. Before the CPU issues this command, it must perform two load operations:

1. Load the DIDR with the three-bit code for the Initiator that is to be reselected.

2. Load the Transfer Counter for a Timeout value to begin when the selected Initiator responds. The Timeout value is computed by using the following equation:

   Transfer Counter = Desired Timeout/146 microseconds

If the Transfer Counter is loaded with the value zero, the MB01 Host Adapter waits indefinitely for a response from the Initiator that is reselected.

The Reselect command may be used only if the MB01 Host Adapter is in the Disconnected state. If the CPU attempts to issue the Reselect command while the MB01 Host Adapter is not in the Disconnected state, the IVC bit (IR bit 06) is set.

When the MB01 Host Adapter detects the Reselect command, it attempts to arbitrate for control of the SCSI bus. If, at any time during arbitration, the MB01 Host Adapter becomes selected or reselected, the Reselect command is aborted and the MB01 Host Adapter interrupts with a message about one of three conditions:

- Selected
- Selected and Bus Service
- Reselected.

If the MB01 Host Adapter wins arbitration, it places the SCSI bus in the Reselection Phase and uses the DIDR to identify the desired Initiator. At the same time, the MB01 Host Adapter begins a timer based on the value for the Transfer Counter timeout computed above. If the Initiator does not respond within the timeout period, the MB01 Host Adapter disconnects from the SCSI bus and interrupts by setting the DSC bit (IR bit 02).

NOTE

The CPU should **not** monitor the TCZ bit (ASR bit 01) to determine when a timeout has occurred.

If the Initiator responds within the allotted time, the MB01 Host Adapter interrupts by setting the FNC status bit (IR bit 00). The MB01 Host Adapter, acting as the Target, is then in control of the SCSI bus and waits for the IR contents to be read by the CPU. After the IR contents have been read, the MB01 Host Adapter waits until it detects a command from the CPU, or until the -ATN signal is asserted by the Initiator. If the -ATN signal is asserted, the MB01 Host Adapter sets the Bus Service (BUS) interrupt status bit (IR bit 01). This Interrupt condition may occur immediately after a command has been issued due to internal timing. In this situation, the MB01 Host Adapter waits for the IR contents to be read and the command is ignored. The MB01 Host Adapter then waits for a new command.

If the timeout is disabled and the Initiator does not respond, or if arbitration is not won, the only way to abort the Reselect command is to issue the Pause command. After the Pause command is issued, Interrupt conditions that cause the FNC bit (IR bit 00) or the DSC bit (IR bit 02) to be set may still occur. These Interrupts occur if one of the Interrupt bits is set before the MB01 Host Adapter detects the Pause command. The Interrupt can also occur if the Initiator responds while the MB01 Host Adapter is sequencing off the SCSI bus in a Timeout condition. If the MB01 Host Adapter does not set either of these interrupt bits, it sets the PS bit (ASR bit 02). When the CPU detects the set PS bit after issuing the Pause command, the MB01 Host Adapter aborts the Reselect command and no connection exists.

4.4.2.10 Diagnostic (Data Turnaround)

The Diagnostic (Data Turnaround) command is an Interrupt-type command that causes the MB01 Host Adapter to attempt to turn a data byte around through its internal data paths. When the Diagnostic command is loaded into the COMD, the Data Register Full bit (DRF) bit (ASR bit 07) is reset. The CPU then writes one byte into the DATR (see subsection 4.4.1). The MB01 Host Adapter moves the byte to another internal register and compares the contents of that register with the contents of the DATR. The byte is then moved to a third internal register and parity is checked for that byte. Finally, the MB01 Host Adapter moves the byte back to the DATR and compares it with the contents of the second internal register.

Based on these comparisons and parity checking, the MB01 Host Adapter stores a result in the Diagnostic Status Register (DSR) (see subsection 4.4.9) and sets the FNC interrupt bit (IR bit 00). After reading the IR contents, the CPU should verify the DRF bit status is one and then read the contents of the DATR. If the DRF bit status is zero, an error has occurred. Table 4-5 lists the codes which are loaded into the Diagnostic Command Status bits (DSR bits <06:03>) as a result of the Diagnostic (Data Turnaround) command.

Table 4-5. Diagnostic Status Register Codes

Bits 06	05	04	03	Result
0	0	0	1	Data Miscompare (Initial)
0	0	1	0	Data Miscompare (Final)
0	0	1	1	Good Parity Detected
0	1	0	0	Bad Parity Detected

4.4.2.11 Receive Commands

The Receive commands are Interrupt-type commands used by the CPU to receive commands, data, and message information from an Initiator during one of the Information Transfer Phases. These commands are valid only when the MB01 Host Adapter is connected as a Target device.

The Receive commands transfer data; therefore, the Single Byte Transfer (SBT) bit (COMD bit 06) and DMA mode (DMO) bit (COMD bit 07) are valid for these commands. If the SBT bit status is zero, the Transfer Counter must be loaded before a Receive command is issued to the MB01 Host Adapter. In this situation, the MB01 Host Adapter uses the Transfer Counter (see subsection 4.4.10) to determine the number of bytes to receive.

When a Receive command is issued, the MB01 Host Adapter immediately resets the DRF bit (ASR bit 07). The MB01 Host Adapter then drives the SCSI bus -I/O, -C/D, and -MSG signal lines for the proper information phase as listed and determined in Table 4-6.

Table 4-6. -I/O, -C/D, and -MSG Signal Lines for Receive Commands

-I/O	-C/D	-MSG	Command Name
0	1	0	Receive Command
0	0	0	Receive Data
0	1	1	Receive Message Out
0	0	1	Receive Unspecified Info Out

The MB01 Host Adapter then requests and receives the specified number of information bytes. The DMO bit (COMD bit 07) determines how these bytes are transferred from the DATR to the host CPU.

When a Receive command is terminated, the MB01 Host Adapter generates an Interrupt message. Termination can be caused by two events:

- The operation is completed successfully and the Transfer Counter is zero. This event results in setting the FNC bit (IR bit 00) to one and resetting the Parity Error (PER) bit (ASR bit 06) to zero. If the Initiator asserted the -ATN signal on the SCSI bus during the operation, the BUS bit (IR bit 01) status is also set to one.

- A Parity Error occurs. The last byte transferred is the byte that caused the error. This event causes the FNC bit (IR bit 00) status and the PER bit (ASR bit 06) status to be set to one. If the Initiator asserted the -ATN signal during the operation, the BUS bit (IR bit 01) status is also set to one.

After any of the interrupts, the MB01 Host Adapter is always left in the connected Target state. The Transfer Counter indicates the number of bytes remaining to be transferred (zero if the operation completed successfully), and the DATR is empty (the last byte received is sent to the CPU). Also, the -ACK and -REQ signals on the SCSI bus are deasserted.

A Receive command may be stopped before an interrupt-causing event by issuing a Pause command (see subsection 4.4.2.3.) If the Initiator does not respond, or if it stops responding, the MB01 Host Adapter cannot respond to a Pause command. For this situation, a Disconnect command can be used to abort the command and the connection (see subsection 4.4.2.2).

NOTE

If a Bus Service Interrupt condition occurs after a Send command, the Initiator activated the -ATN signal on the SCSI bus before the MB01 Host Adapter began executing the command. In this situation, the command is ignored by the MB01 Host Adapter.

4.4.2.12 Send Commands

Send commands are used by the CPU to send status, data, and message information to an Initiator during one of the Information Transfer Phases. The Send commands are Interrupt-type commands that are valid only when the MB01 Host Adapter is connected to the SCSI bus in the Target role.

The Send commands transfer data; therefore, the SBT bit 06 and DMO bit 07 in the COMD are valid for these commands. If the SBT bit status is zero, the Transfer Counter must be loaded before a Send command is issued to the MB01 Host Adapter. In this situation, the MB01 Host Adapter uses the Transfer Counter to determine the number of bytes to send.

When a Send command is issued, the MB01 Host Adapter immediately resets the DRF bit (ASR bit 07). Therefore, the first byte of data for the Data Transfer operation cannot be placed in the DATR until after a Send command is loaded in the COMD.

When it executes a Send command, the MB01 Host Adapter drives the -I/O, -C/D, and -MSG signal lines for the proper SCSI bus Information Transfer Phase. These lines are logically driven for each Send command as listed and described in Table 4-7.

Table 4-7. -I/O, -C/D, and -MSG Signal Lines for Send Commands

-I/O	-C/D	-MSG	Command Name
1	1	0	Send Status
1	0	0	Send Data
1	1	1	Send Message In
1	0	1	Send Unspecified Info In

After the MB01 Host Adapter resets the DRF bit and asserts the -I/O, -C/D, and -MSG signal lines, the MB01 Host Adapter monitors the status of the DRF bit. It takes data from the DATR and sends it to the Initiator. The DMO bit (COMD bit 07) specifies how the data is to be loaded into the MB01 Host Adapter.

After the MB01 Host Adapter has set any Interrupt bit in the IR, it is left in the connected Target state, and the -ACK and -REQ signals on the SCSI bus are inactive (deasserted). When the Data Transfer operation is complete, the MB01 Host Adapter interrupts by setting the FNC interrupt bit (IR bit 00). If the Initiator activated the -ATN signal during the Data Transfer operation, a BUS interrupt bit (IR bit 01) is also set by the MB01 Host Adapter.

NOTE

If the Bus Service (BUS) Interrupt condition is the only Interrupt condition that occurs after a Send command is issued, it indicates the Initiator activated the -ATN signal on the SCSI bus before the MB01 Host Adapter began executing the command. In this situation, the command is ignored by the MB01 Host Adapter.

To abort a Send command before an interrupt-causing event occurs, the CPU can issue a Pause command. If the Initiator does not respond to the Send command, or if it stops responding to the Send command, the MB01 Host Adapter cannot issue a Pause command. In this situation, a Disconnect command can be issued to abort the Send command and the connection.

4.4.2.13 Transfer Information

The Transfer Information command is used by the MB01 Host Adapter (when it is connected as the Initiator on the SCSI bus) for all Data Transfer operations via the SCSI bus. The Transfer Information command is an Interrupt-type command that is valid only when the MB01 Host Adapter is connected to the SCSI bus in the Initiator role. A Transfer Information command is issued by the CPU in response to a Bus Service Interrupt condition (see subsection 4.4.7).

The CPU should not issue a Transfer Information command without first detecting a Bus Service Interrupt condition, because the Target requests and controls all Data Transfer operations. The MB01 Host Adapter permits only one Transfer Information or Transfer Pad command to be issued per Bus Service Interrupt.

After the CPU receives a Bus Service Interrupt condition, and before it issues a Transfer Information command, it should read the status of the I/O, C/D, and MSG bits in the ASR before it reads the contents of the IR. This action allows it to determine the SCSI bus Information Transfer Phase type and the direction of transfer requested by the Target. The CPU then prepares for the Data Transfer operation. If the SBT bit is not to be set in the COMD, the Transfer Counter must be loaded before the Transfer Information command is issued. This action indicates to the MB01 Host Adapter the maximum number of bytes to be transferred.

When a Transfer Information command is issued, the MB01 Host Adapter immediately resets the DRF bit (ASR bit 07). For this reason, the first byte of data for an output Data Transfer operation cannot be loaded into the DATR until after the Transfer Information command is loaded into the COMD. The MB01 Host Adapter then proceeds with the Data Transfer operation. Data is read from (input), or written to (output), its appropriate DATR by using the mode indicated by the DMO bit (COMD bit 07). The MB01 Host Adapter automatically detects the direction of the Data Transfer operation by checking the status of the I/O bit (ASR bit 03).

NOTE

The DMA Controller on the MB01 Host Adapter must be set by the CPU to transfer data in the proper direction. The state of the I/O bit (ASR bit 03) indicates the direction of the Data Transfer operation.

The MB01 Host Adapter continues the Data Transfer operation until an interrupt-causing event occurs. The MB01 Host Adapter can interrupt and terminate a Data Transfer operation if there occurs any of the following four events:

- The maximum number of bytes specified have been transferred, and the Target asserted the -REQ signal on the SCSI bus or the Information Phase changed. This event results in a Bus Service Interrupt condition. Either the Single Byte Transfer mode was specified (COMD bit 06) or the Transfer Counter is zero as indicated by the TCZ bit (ASR bit 01) status. The Target may have changed the Information Transfer Phase type. The status of the I/O, C/D, and MSG bits in the ASR need to be examined at the time of the Interrupt condition to determine which phase the Target is requesting.

NOTE

Due to any early notice of phase change, a phase may be selected spuriously and not transfer any data. The CPU should not consider this spurious phase selection an error condition.

- The Target changes the SCSI bus Information Transfer Phase type before the maximum number of bytes has been transferred. This event also causes a Bus Service Interrupt condition. The new Information Transfer Phase may be determined by examining the status of the I/O, C/D, and MSG bits in the ASR. The Transfer Counter may be read at the time of the Interrupt condition to determine the number of bytes remaining to be transferred. When this Interrupt condition occurs for an output Data Transfer operation, the MB01 Host Adapter may take one more byte from the host CPU than it transfers, due to pre-fetching, but the Transfer Counter contents still reflect the number of bytes remaining to be transferred.

- The Target releases the SCSI bus by de-asserting the -BSY signal line. This event results in setting the DSC interrupt bit (IR bit 02). Once this Interrupt condition occurs, the MB01 Host Adapter is no longer in the Initiator role and it remains in the Disconnected state.

- The MB01 Host Adapter received the last byte of a SCSI bus Message In Phase message from the Target. This event sets the FNC interrupt bit (IR bit 00). For this situation, the -ACK signal line on the SCSI bus is left asserted to allow the CPU to issue the Set ATN command so the message can be rejected. After this Interrupt message is received and a Set ATN command is issued (if desired), a Message Accepted command must be issued to de-assert the -ACK signal for the last byte of the Message In Phase.

For input Data Transfer operations (-I/O signal level is set to one), the MB01 Host Adapter checks parity for each byte received if the Parity Enable (PEN) bit in the Control Register (CTRLR bit 02) is set to one. If the MB01 Host Adapter checks parity and determines a parity error has occurred, the MB01 Host Adapter asserts the -ATN signal line before it deasserts the -ACK signal line for the byte that caused the error. It also sets the PER bit (ASR bit 06) to one, but the parity error does not result in an Interrupt condition. The MB01 Host Adapter waits for one of the four events listed above before interrupting. Therefore, the state of the PER bit should be examined when servicing any Interrupt condition after issuing a Transfer Information command for an input Data Transfer operation.

If the -ATN signal line is asserted by the MB01 Host Adapter (either because a parity error is detected or because a Set ATN command is issued), the -ATN signal line remains asserted until the end of the connection or until a Message Out Data Transfer operation occurs. Therefore, during each cycle of a Transfer Information operation for output, the MB01 Host Adapter checks for the SCSI bus for three conditions:

1. Message Phase in which the -MSG and -C/D bits (ASR bits 05 and 04, respectively) are set to one

2. Operation was a Single-Byte Transfer; i.e, the SBT bit (COMD bit 06) status is set to one

3. Transfer Counter is set at zero.

If any of these conditions exists, the MB01 Host Adapter deasserts the -ATN signal line before it asserts the -ACK signal for the last byte of the message.

As previously stated, a Transfer Information command usually terminates with an Interrupt condition. If a Transfer Information command must be aborted (possibly because of a timeout violation) either a Chip Reset command or a Disconnect command can be used. Although these commands can force the MB01 Host Adapter into a Disconnected state, the Target device is left on the SCSI bus. The only way an Initiator can force a Target to disconnect is to initiate a SCSI bus Reset condition, which is not a function of the MB01 Host Adapter.

4.4.2.14 Transfer Pad

The Transfer Pad command can be used by the CPU to cause the MB01 Host Adapter to continue handshaking with a Target even though a Data Transfer operation is not occurring. The Transfer Pad command has a similar effect on the system as the Transfer Information command, except the Data Transfer operation between the MB01 Host Adapter and the Multibus is different. The Transfer Pad command is an Interrupt-type command that is valid only when the MB01 Host Adapter is connected to the SCSI bus as an Initiator.

The Transfer Pad command may be useful when the Target requests an invalid Information Transfer Phase. The MB01 Host Adapter responds to this command as it does to a Transfer Information command, except for output Data Transfer operations only one byte of data is taken from the host CPU and the same byte is sent repeatedly until the Data Transfer operation terminates. For input Data Transfer operations, the MB01 Host Adapter accepts data from the SCSI bus but does not check parity or send it the CPU. Although data is not exchanged with the CPU, the Transfer Counter is still used by the MB01 Host Adapter so that a maximum number of pad bytes can be specified.

Protocol for using a Transfer Pad command is the same as that used for the Transfer Information command, except the DMO bit (COMD bit 07) has significance only for output Data Transfer operations. The Transfer Pad command terminates because of the same four event sequences that cause a Transfer Information command to terminate (see subsection 4.4.2.13). Also, as with the Transfer Information command, the Reset and Disconnect commands can be used to abort the command.

4.4.3 CONTROL REGISTER (CTRLR) +12

07	06	05	04	03	02	01	00
X	X	X	X	X	PEN	REN	SEN

Read/Write

The 8-bit, Read/Write Control Register (CTRLR) is used for enabling certain modes of operation for the MB01 Host Adapter. After being reset and after the MB01 Host Adapter has completed Self-Test diagnostic routines, the CTRLR contains all zeros.

Not Used - Bits <07:03>

The status of these bits can be either one or zero.

Parity Enable (PEN) - Bit 02

When the Parity Enable (PEN) bit status is set to one, the MB01 Host Adapter generates and checks parity on all Data Transfer operations being conducted via the SCSI bus. When the PEN bit status is reset to zero, the MB01 Host Adapter generates but does not check parity on SCSI bus Data Transfer operations.

Reselect Enable (REN) - Bit 01

When the REN bit status is set to one, the MB01 Host Adapter responds to any attempt by a Target to reselect it. When the REN bit status is set to zero, the MB01 Host Adapter ignores all attempts to reselect it.

Select Enable (SEN) - Bit 00

When the SEN bit status is set to one, the MB01 Host Adapter responds to attempts to select it as a Target. When the SEN bit status is set to zero, the MB01 Host Adapter ignores all selection attempts.

4.4.4 DESTINATION ID REGISTER (DIDR) +13

07	06	05	04	03	02	01	00
0	0	0	0	0	Destination ID		

Read/Write

The 8-bit Read/Write Destination ID Register (DIDR) is used to program the SCSI bus address of the destination Target device before the CPU issues a Select or Reselect command to the MB01 Host Adapter. Bits <02:00> specify the hexadecimal address and bits <07:03> are always zeroes.

4.4.5 AUXILIARY STATUS REGISTER (ASR) +14

07	06	05	04	03	02	01	00
DRF	PER	MSG	C/D	I/O	PS	TCZ	X

Read-Only

The bits in the 8-bit, Read-only Auxiliary Status Register (ASR) are used to indicate the status of the MB01 Host Adapter or to determine the reason for Interrupt conditions. Therefore, when servicing Interrupt conditions, the ASR contents should always be read before reading the IR contents. After the IR contents are read, the ASR bits needed to service the Interrupt condition may change. The individual bits in the ASR are defined in the following paragraphs.

NOTE

After a Reset condition and after the MB01 Host Adapter has completed the Self-Test Diagnostic Routines, the ASR should contain the following bit pattern:

Bit 07	06	05	04	03	02	01	00
0	0	X	X	X	0	1	0

where 0 is not set, 1 is set, and X is equal to either 1 or 0.

Data Register Full (DRF) - Bit 07

The DRF bit indicates the status of the DATR and must be monitored by the host CPU during execution of non-DMA mode commands in which the DMO bit (COMD bit 07) is reset to zero. Data for Send commands, Receive commands, or Transfer Information commands is transferred to or from the MB01 Host Adapter by writing to or reading from the DATR. The DRF bit status is set to one when the register is full and set to zero when the register is empty. Therefore, the DRF bit status should be set to one before taking data from the DATR, and it should be reset to zero when sending data to the DATR.

The DRF bit status is always reset to zero at the time an Interrupt-type command is loaded into the COMD. Therefore, when issuing such commands, the COMD should be loaded before loading the DATR and before monitoring the status of the DRF bit.

Parity Error (PER) - Bit 06

When the PER bit status is set to one, the MB01 Host Adapter has detected a parity error on a byte of data received via the SCSI bus. It can be set when the MB01 Host Adapter is executing one of the Receive commands or when it is executing the Transfer Information command (when the Data Transfer operation is an Input operation). This bit is reset to zero after the IR contents are read.

MSG, C/D, I/O - Bits <05:03>

These bits indicate the status of the -I/O, -C/D, and -MSG signal lines on the SCSI bus at all times. The bits define the Information Transfer Phase type requested by the Target. These signal levels are significant when servicing Interrupt conditions while the MB01 Host Adapter is logically connected to the SCSI bus in an Initiator role. An Interrupt condition occurs with any phase change on the SCSI bus. This Interrupt condition allows the CPU to prepare for the next phase of the Data Transfer operation. The status of these bits are held asserted only while the -INT signal is active. the MSG, C/D, and I/O bits are phase-coded as listed and defined in Table 4-8.

Table 4-8. Auxiliary Status Register MSG, C/D, and I/O Bits

I/O	C/D	MSG	SCSI Bus Phase
0	0	0	Data Out
0	0	1	Unspecified Information Out
0	1	0	Command
0	1	1	Message Out
1	0	0	Data In
1	0	1	Unspecified Information In
1	1	0	Status
1	1	1	Message In

Paused (PS) - Bit 02

When set to one, the PS bit indicates the MB01 Host Adapter has responded to the Pause command and has aborted the command being executed. This bit is reset to zero when an Interrupt-type Command code is loaded into the COMD.

Transfer Counter Zero (TCZ) - Bit 01

The TCZ bit indicates the status of the 24-bit Transfer Counter. When set to one, it indicates the Transfer Counter is equal to zero. The TCZ bit is provided to make servicing of Interrupt conditions easier.

Not Used - Bit 00

The status of this bit can be either one or zero.

4.4.6 ID REGISTER (IDR) +15

07	06	05	04	03	02	01	00
0	0	0	0	0	Device ID		

Read-Only

The 8-bit, Read-only ID Register (IDR) is used to indicate the logical SCSI bus address identification (ID) code assigned to the MB01 Host Adapter. Bits in the IDR are active high whereas the ID input signals are active low. The IDR allows the CPU to read the SCSI bus address of the MB01 Host Adapter that would normally be strapped in hardware. Bits <07:03> of the IDR are always zeroes.

Device ID - Bits <02:00>

These bits indicate the SCSI bus address ID assigned to the MB01 Host Adapter by setting switches SW1-1 through SW1-3. For more information about SCSI bus device address selection, see subsection 3.3.1.

4.4.7 INTERRUPT REGISTER (IR) +16

07	06	05	04	03	02	01	00
X	IVC	X	RES	SE	DSC	BUS	FNC

Read-Only

The 8-bit, Read-only Interrupt Register (IR) is used in conjunction with the ASR to determine the reason for an Interrupt condition. When the contents of the IR are read, the IR resets itself automatically (after the Read operation is completed). This Reset function enables the MB01 Host Adapter to monitor the IR for a new Interrupt condition. Since the Parity Error bit in the ASR is reset after reading the IR contents, and since the -I/O, -C/D, and -MSG signals are only asserted while the -INT signal is active, the contents of the ASR should always be read before the IR contents are read.

If a Selected or Reselected Interrupt occurs after issuing a command that would normally cause an Interrupt condition, the MB01 Host Adapter ignores the last command issued. This action allows the CPU to service the Selected or Reselected Interrupt condition before it proceeds with another operation. For example, the host CPU issues a command to select a Target at about the same time another Target reselects the MB01 Host Adapter. If the MB01 Host Adapter detects the Reselection command first, the CPU receives a Reselection Interrupt message. The MB01 Host Adapter ignores the Select command, which has become invalid because the MB01 Host Adapter is logically connected to another device.

Individual Interrupt conditions are described in the following paragraphs. For all such conditions, an Interrupt condition is ON when the corresponding bit is set to one, and OFF when that bit is reset to zero.

Not Used - Bit 07

The status of this bit may be either one or zero.

Invalid Command (IVC) - Bit 06

When the IVC bit status is set to one, the last command loaded into the COMD is not valid.

Not Used - Bit 05

The status of this bit can be either one or zero.

Reselected (RES) - Bit 04

The RES interrupt bit status is set to one when the MB01 Host Adapter is reselected by another device on the SCSI bus. After setting this interrupt bit, the MB01 Host Adapter is logically connected to the SCSI bus in an Initiator role and is waiting for the Target to assert the -REQ signal or to disconnect from the SCSI bus.

Selected (SE) - Bit 03

The SE interrupt bit status is set to one whenever the MB01 Host Adapter is selected by another device on the SCSI bus. After setting this interrupt bit, the MB01 Host Adapter is logically connected to the SCSI bus in the Target role and is waiting for a command to be loaded into the COMD.

NOTE

The MB01 Host Adapter is Selected or Reselected only if the ID data byte placed on the SCSI bus during the Selection or Reselection Phase has good parity, and when not more than one ID, except the ID for the MB01 Host Adapter is on the SCSI bus.

Disconnected (DSC) - Bit 02

The DSC interrupt bit status is set to one when the MB01 Host Adapter is connected to the SCSI bus in the Initiator role and the Target disconnects, or when the MB01 Host Adapter is executing a Select or Reselect command and the destination device does not respond before the Transfer Counter times out.

Bus Service (BUS) - Bit 01

When the MB01 Host Adapter is logically connected to the SCSI bus in the Initiator role, the BUS interrupt bit status is set to one whenever the Target sends a -REQ signal that the MB01 Host Adapter cannot handle automatically. This event occurs when the first -REQ signal for the connection is received, or when the MB01 Host Adapter is executing a Transfer Information or Transfer Pad command and either the Transfer Counter is zero or the Target changes the type of Information Transfer Phase.

The Bus Service interrupt bit may also be set if a SCSI bus phase change occurs before the -REQ signal is detected. This early notice allows the Initiator extra time to prepare for a SCSI bus phase change in some unbuffered systems. The MB01 Host Adapter may generate Bus Service Interrupt conditions for SCSI bus phases that never request Data Transfer operations. This Interrupt process is not the result of an error condition, but merely represents the transitional status of the -I/O, -C/D, and -MSG signals.

If the MB01 Host Adapter is logically connected in the Target role, the BUS bit is set to one whenever the Initiator asserts the -ATN signal. While the -ATN signal is asserted, the Bus Service Interrupt may occur by itself, with a selected Interrupt bit asserted, or with a FNC interrupt bit asserted.

Function Complete (FNC) - Bit 00

When the FNC interrupt bit status is set to one, it indicates execution of the last Interrupt-type command has been completed. The FNC interrupt bit is set when the Select, Reselect, Send, and Receive commands are completed successfully. During any of the Receive commands, the FNC bit status is set to one along with the Parity Error (PER) bit (ASR bit 06) status as soon as a parity error is detected. A Bus Service Interrupt condition may also occur simultaneously with the set FNC interrupt bit if an -ATN signal was activated during execution of a Send or a Receive command.

The set FNC interrupt status bit is also set to one at the end of a Message In Phase for a Transfer Information command.

4.4.8 SOURCE ID REGISTER (SIDR) +17

07	06	05	04	03	02	01	00
IDV	X	X	X	X	SOURCE ID		

Read-Only

The 8-bit, Read-only Source ID Register (SIDR) contains the three-bit identification (ID) code for the last device that selected or reselected the MB01 Host Adapter.

ID Valid (IDV) - Bit 07

The set status of the IDV bit indicates the source device placed its own ID bit on the SCSI bus during the Selection Phase.

Not Used - Bits <06:03>

The status of these bits can be either one or zero.

Source ID - Bits <02:00>

The MB01 Host Adapter encodes the source ID and places it in bits <02:00>. This information remains valid until the MB01 Host Adapter disconnects from the SCSI bus, at which time the IDV bit is reset to zero.

4.4.9 DIAGNOSTIC STATUS REGISTER (DSR) +19

07	06	05	04	03	02	01	00
SDC	X	Diagnostic Command Status			Self-Test Status Code		

Read-Only

The 8-bit Read-only Diagnostic Status Register (DSR) indicates when the Self-Test Diagnostic routines of the MB01 Host Adapter have been completed successfully. The DSR contains bits that encode the status of the Diagnostic command being executed, and it contains the status code of the Self-Test Diagnostic routine.

Self-Diagnostic Complete (SDC) - Bit 07

When this bit status is set to one, it indicates the MB01 Host Adapter Self-Test Diagnostic routines have been completed successfully. If a Reset command is issued to the MB01 Host Adapter, bits <06:03> are cleared if possible. After a Reset command is issued to the MB01 Host Adapter, the CPU should examine the DSR and ensure the DSR contains the following code: 10000000. This code indicates the MB01 Host Adapter Self-Test Diagnostic routines are completed and that no errors were detected. After the MB01 Host Adapter executes a Diagnostic command, bits <06:03> contain the resulting status, but bit 07 and bits <02:00> are not affected.

If an error is detected during Self-Test Diagnostic routines, the proper status is loaded into the DSR and the MB01 Host Adapter halts until a Reset command or a Reset signal is asserted. Table 4-9 lists and describes the individual error codes.

When a Diagnostic command is issued to the MB01 Host Adapter, the MB01 Host Adapter attempts to perform the function, loads a status into bits <06:03>, and initiates a Function Complete Interrupt condition.

Table 4-9. Diagnostic Status Register Self-Test Status Codes

Bits 02 01 00	Self-Test Status
0 0 0	Successful Completion The MB01 Host Adapter executed all Self-Test Diagnostic routines following a Reset operation and detected no errors.
0 0 1	Unconditional Branch Fail The internal sequencer in the MB01 Host Adapter attempted an Unconditional Branch operation and failed to reach the desired location.
0 1 0	Data Register Full Failed The MB01 Host Adapter attempted to set and reset the DRF status bit in the IR and failed.
0 1 1	Initial Conditions Incorrect The MB01 Host Adapter detected one of its internal initial conditions in the wrong state.
1 0 0	Initial Command Bits Incorrect The MB01 Host Adapter tested bits 06, 04, 02, 01, and 00 of the COMD and found the status of at least one of these bits was not zero.
1 0 1	Diagnostic Flag Failed The MB01 Host Adapter failed in its attempt to set and reset its Internal Diagnostic flag.
1 1 0	Data Turnaround Failed During Self-Test Diagnostic Routines, the MB01 Host Adapter attempts to flush several bytes of data through its internal data paths. It also attempts to set and reset the Parity Error bit in the IR. This status code indicates one of these attempted operations failed.
1 1 1	Not Used.

Not Used - Bit 06

The status of this bit can be either one or zero.

Diagnostic Command Status - Bits <05:03>

These bits contain the status that results after a Diagnostic command has been executed; the bit patterns and status are listed in Table 4-10.

Table 4-10. Diagnostic Command Status

Bits 05	04	03	Diagnostic Command Status
0	0	1	Turnaround Miscompare (Initial)
0	1	0	Turnaround Miscompare (Final)
0	1	1	Turnaround Good Parity
1	0	0	Turnaround Bad Parity

Self-Test Status Code - Bits <02:00>

If an error is detected during Self-Test Diagnostic routines, these bits indicate the type of failure. The status codes are listed and described in Table 4-9.

4.4.10 TRANSFER COUNTERS +1C, +1D, +1E

The Transfer Counter is comprised of three, eight-bit register/counters. The Transfer Counter is used by the MB01 Host Adapter for Send, Receive, and Transfer commands that require more than a single byte of data to be transferred. It may also be used with the Select and Reselect commands to set a timeout limit for no response. The Transfer Counter is addressed as listed and defined in Table 4-11. Each offset is a hexadecimal number.

Table 4-11. Addresses for the Transfer Counters

Offset	Selected Byte
+C	Most Significant Byte
+D	Middle Byte
+E	Least Significant Byte

For Send, Receive, and Transfer commands with the Single-Byte Transfer mode bit (COMD bit 06) status is reset to zero, the Transfer Counter specifies to the MB01 Host Adapter the maximum number of bytes to be sent or received before interrupting. The Transfer Counter must be loaded before issuing the command. When the Single-Byte Transfer mode bit status is set to one, the MB01 Host Adapter neither uses nor alters the Transfer Counter. To ease servicing Interrupt conditions for commands that use the Transfer Counter, the TCZ bit is provided in the ASR to indicate when the Transfer Counter is zero.

For Select and Reselect commands, the Transfer Counter specifies the number of time intervals (1024 CLK periods) the MB01 Host Adapter is to wait before automatically aborting the command because no response (BSY) from the destination device (Initiator or Target) has been detected. The Transfer Counter must be loaded before issuing the command. If the Transfer Counter is loaded with all zeroes, the timeout logic in the MB01 Host Adapter is disabled, and the MB01 Host Adapter does not abort the command automatically when no response is received from the destination device.

4.5 SCSI BUS RESET REGISTER (SBR) +20

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X

Write-Only

The 8-bit, Write-only SCSI Bus Reset register (SBR) is used to set any 8-bit pattern from the CPU. Any 8-bit pattern set in this SBR causes a SCSI bus Reset (-RST) signal to be asserted.

4.6 RELEASE SCSI BUS RESET REGISTER (RSR) +27

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X

Write-Only

The 8-bit, Write-only Release SCSI Bus Reset register (RSR) is used to set any 8-bit pattern from the CPU. Any 8-bit pattern set in this RSR causes the current SCSI bus -RST signal to be deasserted.

4.7 INTERRUPT MODE REGISTERS

The MB01 Host Adapter Vector 0 and Vector 1 Registers are used t store information which describes the procedure for servicing Multibus Interrupt conditions. During an Interrupt Acknowledge cycle, the CPU can assert two or three Interrupt Acknowledge (INTA) signals. The contents of the Vector 0 Register are sent when the second INTA signal is asserted. The contents of the Vector 1 Register are sent when the third INTA signal is asserted.

The data in the two Interrupt Mode registers can be interpreted as any of the following items:

- a Restart instruction
- an Interrupt Table pointer
- the lower byte of an Interrupt Subroutine Address
- the higher byte of an Interrupt Subroutine Address.

For more information about the MB01 Host Adapter Interrupt mode, see subsection 4.9.3.

4.7.1 VECTOR 0 REGISTER +21

07	06	05	04	03	02	01	00
Vector 0 Data							

Write-Only

The contents of the 8-bit, Write-only Vector 0 Register are sent to the Multibus lower data byte along with the proper Transfer Acknowledge signal when the second INTA signal is asserted.

4.7.2 VECTOR 1 REGISTER +22

07	06	05	04	03	02	01	00
Vector 1 Data							

Write-Only

The contents of the 8-bit, Write-only Vector 1 Register are sent to the Multibus lower data byte along with the proper Transfer Acknowledge signal when the third INTA signal is asserted.

4.8 GENERAL STATUS REGISTER (GSR) +24

07	06	05	04	03	02	01	00
POSW		ICS			SPV	SBRF	DTO

Read-Only

The 8-bit, Read-only General Status Register (GSR) contains MB01 Host Adapter status information. Contents of the GSR are read by the CPU after an Interrupt request has been issued to the MB01 Host Adapter.

Program Option Switch (POSW) - Bits <07:06>

The status of these bits are reserved for software options to be provided by the OEM user. These options are selected by setting switches SW1-9 and SW1-10 on the MB01 Host Adapter. Bit 07 corresponds with program switch 1; bit 06 corresponds with program switch 2. For more information about programming option selection, see subsection 3.3.5.

Interrupt Channel Selection (ICS) - Bits <05:03>

The status of these bits determines the Interrupt Channel used by the CPU to service an Interrupt request generated by the MB01 Host Adapter. The Interrupt Channel is established by setting switches SW1-5 through SW1-7 on the MB01 Host Adapter. For more information about Interrupt Channel selection, see subsection 3.3.3.

SCSI Bus Phase Valid (SPV) - Bit 02

The SPV bit status indicates whether the type of SCSI bus phase is or is not valid. When the SPV bit status is set to one, the SCSI bus phase is valid. When the SPV bit status is reset to zero, the SCSI bus phase is not valid.

SCSI Bus Reset Flag (SBRF) - Bit 00

The SBRF bit status indicates when an Interrupt message from the MB01 Host Adapter to the CPU occurred because a device on the SCSI bus asserted a SCSI bus Reset (-RST) signal. The SBRF bit status is set to one if a device on the SCSI bus asserted the -RST signal. The SBRF bit status is reset to zero if the -RST signal was not asserted by a device on the SCSI bus.

DMA Operation Timeout (DTO) - Bit 00

During a DMA Data Transfer operation, the MB01 Host Adapter has control of the Multibus. If the time required to transfer data to or from host memory exceeds the timeout value of 1.6 milliseconds, the set state of this bit flags the condition. Therefore, if a DMA timeout occurs, the flag is set and the DMA Data Transfer operation continues with the next step. When the DTO bit status is set to one, a DMA Data Transfer operation timeout occurred; when the DTO bit status is reset to zero, no DMA timeout occurred. The DTO bit status is reset to zero when the CPU reads the contents of the GSR.

4.9 GENERAL PROGRAMMING INFORMATION

Information about specific MB01 Host Adapter programming functions are described in the following subsections.

4.9.1 MB01 HOST ADAPTER MODES

The MB01 Host Adapter supports four modes of operation:

- Programmed I/O mode
- Interrupt mode
- Bus Arbitration mode
- Bus Master mode.

4.9.1.1 Programmed I/O Mode

When the MB01 Host Adapter is in the Programmed I/O mode, the CPU can read from or write to an MB01 Host Adapter register. In this mode, MB01 Host Adapter registers must occupy 48 contiguous locations of I/O space in the host Multibus system. For more information about MB01 Host Adapter registers, see subsection 4.2.

4.9.1.2 Interrupt Mode

When the MB01 Host Adapter is in the Interrupt mode, the MB01 Host Adapter interrupts the CPU to obtain service and directs it to branch to a pre-defined Interrupt subroutine. (These subroutines are loaded in the Vector 0 and Vector 1 Registers; see subsections 4.7.1 and 4.7.2.) The MB01 Host Adapter generates an Interrupt request to the CPU when a flag is set for any of the following conditions:

- a Reset signal (-RST) is detected on the SCSI bus and status is flagged by the set SBRF status signal (GSR bit 00)

- a device on the SCSI bus sent an invalid SCSI command to the MB01 Host Adapter, and status is flagged by the set IVC status bit (IR bit 06)
- the MB01 Host Adapter is reselected as a Target, and status is flagged by the set RES status bit (IR bit 04)
- the MB01 Host Adapter is selected by an Initiator, and status is flagged by the set SE status bit (IR bit 03)
- a SCSI bus Target device disconnects from an Initiator, and status is flagged by the set DCS status bit (IR bit 02)
- a SCSI bus service is required, and status is flagged by the set BUS status bit (IR bit 01)
- a SCSI bus function is completed, and status is flagged by the set FNC status bit (IR bit 00).

All interrupt conditions listed above, except -RST with SBRF flag, are flagged in the IR.

Observe that no Interrupt request is generated when an MB01 Host Adapter DMA Data Transfer operation is completed. A completed DMA cycle is indirectly implied by the other interrupt conditions. Typically in a DMA Data Transfer cycle, the end of the cycle is determined by the following methods:

- poll of the CTC status bit (STR bit 00)
- get a Function Complete Interrupt when flagged by the FNC status bit (IR bit 00)
- wait until the Target count down and switch the SCSI bus phase so the MB01 Host Adapter generates a Bus Service Interrupt request, flagged by the BUS status bit (IR bit 01)

4.9.1.2.1 Vectored and Nonvectored Interrupt Operations. The MB01 Host Adapter supports the two types of Multibus Interrupt operations described in the IEEE Microcomputer System 796 Bus Standard: Vectored Interrupts and Nonvectored Interrupts.

Vectored Interrupts transfer the Interrupt Vector Address on Multibus data lines from the MB01 Host Adapter to the CPU using the Multibus Interrupt Acknowledge (INTA) command signal. After the first INTA signal occurs, the CPU puts an interrupt code on the Multibus address lines. This code is the address of the highest priority Interrupt Request line that is active. At this time, once the CPU receives an interrupt request, it can generate either two INTA signals or three INTA signals on the Multibus.

If the CPU generates two INTA signals, it transfers the two INTA signals, with the Interrupt I.D. number, on the Address Bus. After the MB01 Host Adapter receives the first INTA signal, it monitors the Interrupt I.D. number and the INTA signal. Once the MB01 Host Adapter detects the second INTA signal (with the correct Interrupt I.D. number), it issues the contents of the Vector 0 Register (see subsection 4.7.1). The Interrupt Vector Address detected by the CPU is normally used as a pointer in the Interrupt Vector Address table. (The location of the Interrupt Vector Address table is dependent on the configuration of the Multibus system.)

If the CPU generates three INTA signals, it transfers the three INTA signals, with the Interrupt I.D. number, on the internal Address Bus. The MB01 Host Adapter ignores the first INTA signal, but it responds to the second INTA signal by issuing the contents of the Vector 0 Register. Once the MB01 Host Adapter detects the third INTA signal, it issues the contents of the Vector 1 Register (see subsection 4.7.2). The two INTA signals allow the MB01 Host Adapter to put a two-byte Interrupt Vector Address on the Multibus data lines (one byte for each INTA signal). The two-byte Interrupt Vector Address can be programmed by any Multibus master that has I/O processing capability.

Nonvectored Interrupt requests are handled by the CPU and do not require the use of the Multibus interface for transfer of the Interrupt Vector Address. The MB01 Host Adapter uses the Multibus Interrupt Request lines (INT0 through INT7) to generate an interrupt request for an I/O device on the SCSI bus to the CPU. The Interrupt Vector Address is generated by the Interrupt Controller on the CPU module and that Interrupt Controller causes a branch to the appropriate subroutine to service the Interrupt request. In the Interrupt Service routine, the Interrupt flag must be reset (by reading the contents of the IR) before the software re-enables the Interrupt request.

4.9.1.3 Bus Arbitration Mode

In the Bus Arbitration mode, the MB01 Host Adapter sets the procedure for gaining control of the Multibus. The Bus Arbitration mode is implemented by using either the Serial Arbitration Technique or the Parallel Arbitration Technique. As defined in the IEEE 796 Specification, priorities of the Multibus Arbitration operation depend on either the physical location of the master module PCBAs (Serial Arbitration Technique) or on the physical circuitry of the master module PCBAs (Parallel Arbitration Technique) which contend for control of the Multibus. The technique to be used with the MB01 Host Adapter is switch selectable by using switch SW1-4 (see subsection 3.3.2).

In the Serial Arbitration Technique, the DMA priority signal is daisy-chained through the entire Multibus system. Up to four Bus Master candidates can be accommodated. The daisy-chain structure does not allow physical gaps to exist between Multibus master module PCBAs.

In the Parallel Arbitration Technique, the Multibus arbiter determines the Bus Master from those candidates that contend for control of the Multibus.

The MB01 Host Adapter can gain control of the Multibus only when all of four conditions are present:

- No device is current Bus Master, so the Multibus is in the Bus Free Cycle
- No Bus Master candidate requesting control of the Multibus has higher priority than the MB01 Host Adapter
- No back-to-back LOCK request is in the Arbitration Cycle
- The MB01 Host Adapter is requesting control of the Multibus.

The current Bus Master can keep control of the Multibus or release it. The timeout value used when trying to gain control of the Multibus is system-dependent and is not predictable.

4.9.1.4 Bus Master Mode

The MB01 Host Adapter can be programmed to gain control of the Multibus during a DMA Data Transfer operation to enhance the data-throughput rate. In the Bus Master mode, the MB01 Host Adapter has control of the Multibus and transfers data between the SCSI bus and Multibus host memory. When the MB01 Host Adapter has control of the Multibus, all Multibus Interrupt requests are suspended until the CPU becomes bus master.

The MB01 Host Adapter asserts both the Bus Request (BREQ) signal and the Common Bus Request (CBRQ) signal, on the Multibus interface. These asserted signals allow the MB01 Host Adapter to request control of the Multibus from a temporary Bus Master as well as from the CPU.

If the MB01 Host Adapter is forced to release control of the Multibus before a DMA Data Transfer operation is completed, after the condition that caused the operation to be aborted is corrected, it tries again to gain control of the Multibus to continue the interrupted DMA Data Transfer operation. When the Multibus is again available, the MB01 Host Adapter automatically requests control of the Multibus to continue the DMA Data Transfer operation; no software trigger is required to complete the DMA Data Transfer operation.

The MB01 Host Adapter DMA Base Address width is 16 bits. The capacity of the Current Address Counter is limited to 16 bits. If the target memory is not ranged in a 64-kilobyte boundary, before the DMA Data Transfer operation is performed, the controlling software should slice the operation so as to fit the 64-kilobyte boundary.

If the MB01 Host Adapter has been programmed to operate in the Single-Byte Transfer mode or Demand Transfer mode as specified by the status of the TRT bits (MODE, bits <03:02>), then when it gains control of the Multibus, it automatically provides DMA bursts to the Target Memory until the DMA Data Transfer operation is completed. The width of the data path is 8 bits but the MB01 Host Adapter operates in a 16-bit wide data path with no modification.

The MB01 Host Adapter can accept programming from the CPU to perform DMA Data Transfer operations any time a Hold Acknowledge (HLDA) signal is deasserted (which indicates the CPU has not yet released control of the Multibus to the MB01 Host Adapter). This action occurs even if a Hold Request (HRQ) signal is asserted; i.e., the MB01 Host Adapter has requested control of the Multibus for a DMA Data Transfer operation.

After power-up of the Multibus system, all internal registers, especially the Mode Register (MODE), should be loaded with some valid value. These load operations should be performed even though only DMA Channel 0 is currently used for DMA Data Transfer operations.

5.1 OVERVIEW

This section describes MB01 Host Adapter architecture. For reference convenience, this section is divided into two subsections, as listed in the following table:

Subsection	Title
5.1	Overview
5.2	MB01 Host Adapter Architecture

5.2 MB01 HOST ADAPTER ARCHITECTURE

Figure 5-1 is a block diagram of the major functional elements of the MB01 Host Adapter. The MB01 Host Adapter is organized around an 8273 DMA Controller IC and an NCR 5385 SCSI Protocol Controller IC.

5.2.1 DMA CONTROLLER

The DMA Controller is used to control DMA Data Transfer operations between the SCSI bus peripheral devices and the Multibus host system. DMA Data Transfer operations allow SCSI bus peripheral devices to directly transfer information to or from Multibus host memory.

5.2.2 SCSI BUS PROTOCOL CONTROLLER

The SCSI bus Protocol Controller is used to control the exchange of data, commands, and status information between the Multibus host CPU and the SCSI bus.

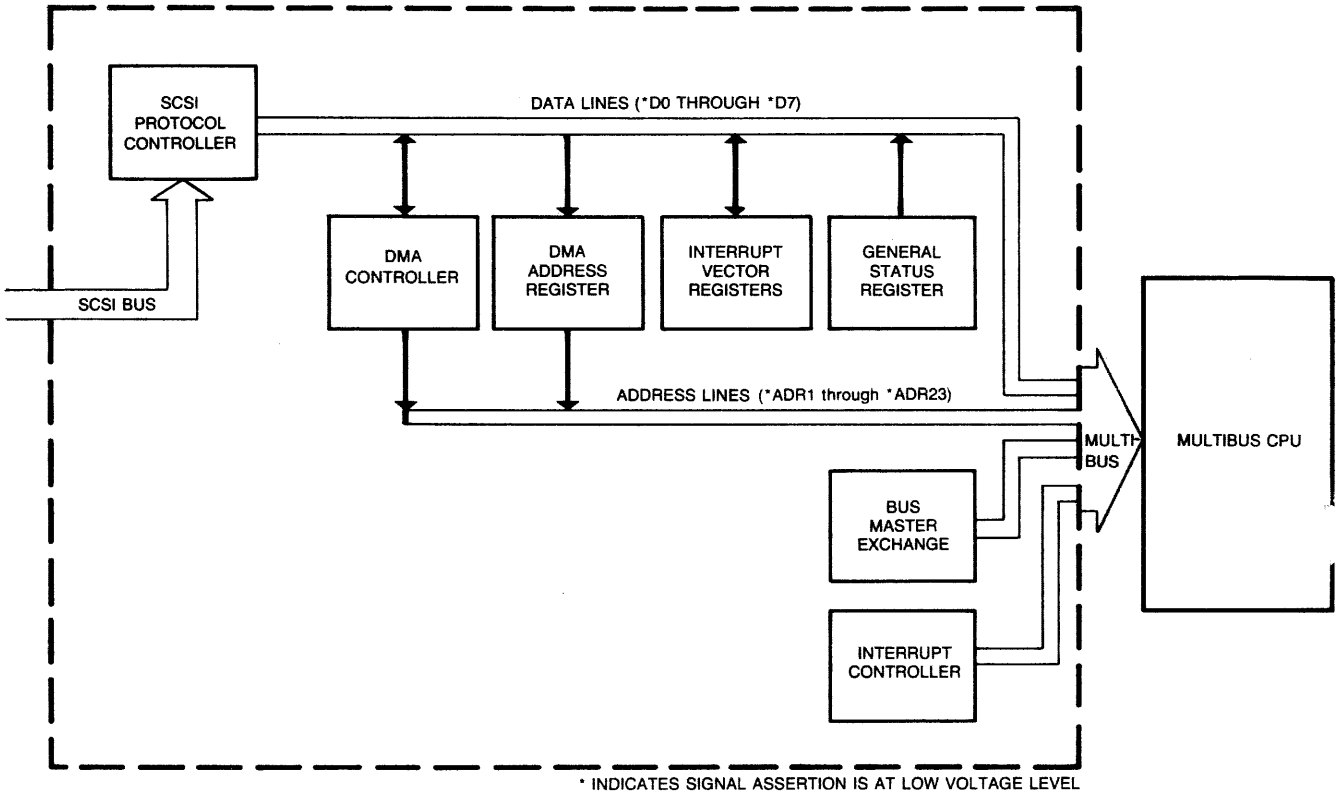


Figure 5-1. Block Diagram, MB01 Host Adapter

5.2.3 DMA ADDRESS REGISTER

The DMA Address Register holds the eight high-order address bits (A16-A23) for a DMA Data Transfer operation. The MB01 Host Adapter gains control of the Multibus to perform a DMA Data Transfer operation. The address for the first DMA Data Transfer operation is sent in two bytes: the least significant byte (LSB) on the eight Address Bus lines (address lines A0-A7) and the most significant byte (MSB) on the internal Data Bus (D7-D0). The MB01 Host Adapter then latches the contents on address lines A8-A15 with the contents on the Data Bus to complete the 16 bits of the Address Bus. The top byte (8 bits) of the DMA Address is set into the DMA Address Register to produce the full 24-bits of the Address Bus.

5.2.4 GENERAL STATUS REGISTER

The General Status Register (GSR) contains MB01 Host Adapter status information. Contents of the GSR are read by the Multibus CPU after an Interrupt request has been issued to the MB01 Host Adapter.

5.2.5 INTERRUPT VECTOR REGISTERS

The MB01 Host Adapter Interrupt Vector Registers are used to store the address od the pointer to the Interrupt Service procedure for servicing Multibus Interrupt conditions.

5.2.6 BUS MASTER EXCHANGE

The Bus Master Exchange circuitry is used to control the process used by the MB01 Host Adapter to arbitrate for control of the Multibus. The MB01 Host Adapter can use either the Serial Arbitration Technique or the Parallel Arbitration Technique. The technique to be used with the MB01 Host Adapter is switch selectable by using switch SW1-4 (see subsection 3.3.2).

5.2.7 INTERRUPT CONTROLLER

The Interrupt Controller is used to control the process used by the the MB01 Host Adapter to interrupt the Multibus CPU. The MB01 Host Adapter interrupts the CPU to obtain service and to direct it to branch to a pre-defined Interrupt Service procedure. The MB01 Host Adapter generates an Interrupt request to the CPU when a flag is set in one of the internal registers of the MB01 Host Adapter.

6.1 OVERVIEW

This section describes the interfaces used by the MB01 Host Adapter. It includes information about how the MB01 Host Adapter implements the electrical and mechanical requirements of the Multibus and the SCSI bus. This section is divided into subsections, as listed in the following table:

Subsection	Title
6.1	Overview
6.2	Multibus Interface
6.3	SCSI Bus Interface

6.2 MULTIBUS INTERFACE

Two edge connectors on the MB01 Host Adapter interface with the Multibus: Connector P1 provides the main interface signal paths and Connector P2 carries the auxiliary signal paths for the optional 24-bit address extension. Pin/signal assignments for connector P1 are listed and described in Table 6-1; pin/signal assignments for connector P2 are listed and described in Table 6-2.

Table 6-1. Pin/Signal Assignments at Connector P1 for Multibus Interface

Function	Pin	Signal Name	I/O	Description
POWER SUPPLIES	1	GND		
	2	GND		
	3	+5V		
	4	+5V		
	5	+5V		
	6	+5V		
	7	+12V		N/C
	8	+12V		N/C
	9	Reserved		N/C
	10	Reserved		N/C
	11	GND		
	12	GND		
BUS CONTROLS	13	-BCLK	I	Bus Clock
	14	-INIT	I	Initialize
	15	-BPRN	I	Bus Priority In
	16	-BPRO	O	Bus Priority Out
	17	-BUSY	O	Bus Busy
	18	-BREQ	O	Bus Request
	19	-MRDC	O	Memory Read Command
	20	-MWTC	O	Memory Write Command
	21	-IORC	I	I/O Read Command
	22	-IOWC	I	I/O Write Command
	23	-XACK	I/O	Transfer Acknowledge
	24	-INH1		No connection
	25	-LOCK	I	Lock
	26	-INH2	O	Inhibit ROM
	27	-BHEN	O	Byte High Enable
	28	-AD16	O	Address Bit 16
	29	-CBRQ	I/O	Common Bus Request
	30	-AD17	O	Address Bit 17
	31	-CCLK		N/C
	32	-AD18	O	Address Bit 18
	33	-INTA	I	Interrupt Acknowledge
	34	-AD19	O	Address Bit 19

N/C = No Connection I/O = Input/Output

All odd-numbered pins are on component side, all even-numbered pins are on the solder side.

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Table 6-1. Pin/Signal Assignments at Connector P1 for Multibus Interface (continued)

Function	Pin	Signal Name	I/O	Description
INTERRUPT CONTROL	35	-INT6	O	Interrupt Request 6
	36	-INT7	O	Interrupt Request 7
	37	-INT4	O	Interrupt Request 4
	38	-INT5	O	Interrupt Request 5
	39	-INT2	O	Interrupt Request 2
	40	-INT3	O	Interrupt Request 3
	41	-INT0	O	Interrupt Request 0
	42	-INT1	O	Interrupt Request 1
ADDRESS	43	-AD14	I/O	Address Bit 14
	44	-AD15	I/O	Address Bit 15
	45	-AD12	I/O	Address Bit 12
	46	-AD13	I/O	Address Bit 13
	47	-AD10	I/O	Address Bit 10
	48	-AD11	I/O	Address Bit 11
	49	-AD8	I/O	Address Bit 8
	50	-AD9	I/O	Address Bit 9
	51	-AD6	I/O	Address Bit 6
	52	-AD7	I/O	Address Bit 7
	53	-AD4	I/O	Address Bit 4
	54	-AD5	I/O	Address Bit 5
	55	-AD2	I/O	Address Bit 2
	56	-AD3	I/O	Address Bit 3
	57	-AD0	I/O	Address Bit 0
	58	-AD1	I/O	Address Bit 1
DATA	59	-D14	I/O	Data Bit 14
	60	-D15	I/O	Data Bit 15
	61	-D12	I/O	Data Bit 12
	62	-D13	I/O	Data Bit 13
	63	-D10	I/O	Data Bit 10
	64	-D11	I/O	Data Bit 11
	65	-D8	I/O	Data Bit 08
	66	-D9	I/O	Data Bit 09
	67	-D6	I/O	Data Bit 06
	68	-D7	I/O	Data Bit 07
	69	-D4	I/O	Data Bit 04
	70	-D5	I/O	Data Bit 05
	71	-D2	I/O	Data Bit 02
	72	-D3	I/O	Data Bit 03
	73	-D0	I/O	Data Bit 00
	74	-D1	I/O	Data Bit 01

N/C = No Connection I/O = Input/Output

All odd-numbered pins are on the component side, all even-numbered pins are on the solder side.

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Table 6-1. Pin/Signal Assignments at Connector P1 for Multibus Interface (continued)

Function	Pin	Signal Name	I/O	Description
POWER SUPPLIES	75	GND		
	76	GND		
	77	Reserved		
	78	Reserved		
	79	-12V		N/C
	80	-12V		N/C
	81	+5V		
	82	+5V		
	83	+5V		
	84	+5V		
	85	GND		
	86	GND		
N/C = No Connection			I/O = Input/Output	
All odd-numbered pins are on the component side, all even-numbered pins are on the solder side.				

Table 6-2. Pin/Signal Assignments at Connector P2 for Multibus Interface

Pin	Signal Name	Description
1	GND	N/C
2	GND	N/C
3	+5V	N/C
4	+5V	N/C
5	Reserved	N/C
6	EEVPP	N/C (EEPROM Power)
7	-5V	N/C
8	-5V	N/C
9	Reserved	N/C
10	Reserved	N/C
11	+12V	N/C
12	+12V	N/C
13	-PFSR	N/C (Power Fail Sense Reset)
14	Reserved	N/C
N/C = No Connection		
All odd-numbered pins are on the component side, all even-numbered pins are on the solder side.		

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Table 6-2. Pin/Signal Assignments at Connector P2 for Multibus Interface (continued)

Pin	Signal Name	Description
15	-12V	N/C
16	-12V	N/C
17	-PFSN	N/C (Power Fail Sense)
18	ACLO	N/C (AC Low)
19	-PFIN	N/C (Power Fail Interrupt)
20	-MPRO	N/C (Memory Protect)
21	GND	N/C
22	GND	N/C
23	+15V	N/C
24	+15V	N/C
25	-15V	N/C
26	-15V	N/C
27	-PAR1	N/C (Parity 1)
28	-HALT	N/C (Bus Master HALT)
29	-PAR2	N/C (Parity 2)
30	-WAIT	N/C (Bus Master WAIT STATE)
31	PLC	N/C (Power Line Clock)
32	ALE	N/C (Bus Master ALE)
33	Reserved	N/C
34	Reserved	N/C
35	Reserved	N/C
36	-BDRSY	N/C (Board Reset)
37	Reserved	N/C
38	-AUXRST	N/C (Reset Switch)
39	Reserved	N/C
40	Reserved	N/C
41	Reserved	N/C
42	Reserved	N/C
43	Reserved	N/C
44	Reserved	N/C
45	Reserved	N/C
46	Reserved	N/C
47	Reserved	N/C
48	Reserved	N/C
49	Reserved	N/C
50	Reserved	N/C
51	Reserved	N/C
52	Reserved	N/C
53	Reserved	N/C
54	Reserved	N/C

N/C = No Connection

All odd-numbered pins are on the component side, all even-numbered pins are on the solder side.

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Table 6-2. Pin/Signal Assignments at Connector P2 for Multibus Interface (continued)

Pin	Signal Name	Description
55	-ADR22	Address Bit 22
56	-ADR23	Address Bit 23
57	-ADR20	Address Bit 20
58	-ADR21	Address Bit 21
59	Reserved	N/C
60	Reserved	N/C
N/C = No Connection		
All odd-numbered pins are on the component side, all even-numbered pins are on the solder side.		

6.3 SCSI BUS INTERFACE

This subsection describes the SCSI bus, as used by the MB01 Host Adapter, and the physical and electrical requirements for proper functioning of that bus.

6.3.1 SCSI BUS INTERFACE PHYSICAL DESCRIPTION

All peripherals on the SCSI bus are daisy chained with a common cable; all signals at connector pins on the cable are common (one-to-one), and both ends of the cable are terminated. The drivers and receivers on the MB01 Host Adapter support the ANSI SCSI specification single-ended option. The maximum cumulative cable length in a daisy chain should not be more than six meters (20 feet). The daisy chain is used primarily to interconnect the MB01 Host Adapter with subsystem components outside the CPU cabinet; e.g., controller for SCSI bus peripheral device in extension cabinet or enclosure).

6.3.1.1 Cable Requirements

A 50-conductor flat-ribbon cable or a 25-twisted-pair flat cable must be used to connect SCSI bus host adapters and controllers. The maximum cumulative cable length is six meters (20 feet). Each SCSI bus connection must have a 0.1-meter maximum stub length. SCSI bus termination can be located internally at the ends of the SCSI bus cable next to the peripheral devices (such as the subsystem that contains the SCSI bus device controller and peripheral mass data storage device).

6.3.1.2 Shield/Ground Requirements

The connector for the shielded SCSI bus cable is a 50-pin connector that contains two rows of 25 female contacts on 100-mil centers. The grounding conductor for the system shielding via the connector ground pin must provide a direct current (dc) resistance not greater than 10 milliohms from the termination point of the connector ground pin to the enclosure for the SCSI bus device.

6.3.2 SCSI INTERFACE ELECTRICAL DESCRIPTION

The MB01 Host Adapter interfaces with SCSI host adapters and other controllers via the SCSI bus (see Figure 7-1). A 50-pin male (IDC) connector, reference designated J1 on the MB01 Host Adapter, plugs directly into the SCSI bus. Component locations for the MB01 Host Adapter are shown in Figure 6-1. All signals use open collector or three-state drivers.

6.3.2.1 Output Signal Characteristics

When measured at the connection for the SCSI device, each signal driven by a SCSI device has the following output characteristics:

- Signal assertion = 0.0 Vdc to 0.4 Vdc
- Minimum driver output current = 48 milliamperes (mA) (sinking) at 0.5 Vdc
- Signal negation = 2.5 Vdc to 5.25 Vdc.

All assigned signals in the SCSI cable are terminated at each end to +5 Vdc (nominal) with 220-Ohm resistors and to ground with 330-Ohm resistors, as shown in Figure 6-2.

6.3.2.2 Input Signal Characteristics

When measured at the connection for the SCSI device, each signal received by a SCSI device has the following input characteristics:

- Signal true = 0.0 Vdc to 0.8 Vdc
- Maximum total input load current = -0.4 mA at 0.4 Vdc
- Signal false = 2.0 Vdc to 5.25 Vdc
- Minimum input hysteresis = 0.2 Vdc.

6.3.2.3 Terminator Power (Optional)

The MB01 Host Adapter supports the single-ended SCSI option that provides pin 26 with termination power that has the following characteristics:

V_{cc} = 4.0 Vdc to 5.25 Vdc (through diode)
800 mA minimum source drive capability
1.0 mA maximum sink capability

To implement this option, diode #IN5820 must be installed at reference designator CR1 on the MB01 Host Adapter PCBA. Also connect a wire-wrap jumper between jumper posts A and B on the MB01 Host Adapter to supply +5 Vdc for the SCSI bus termination.

- - - - - - - -
C A U T I O N
- - - - - - - -

If diode leads are reversed so that positive lead is in wrong hole, system does not function properly.

If diode CR1 is to be installed, insert diode leads in holes provided at upper right corner of PCBA (see Figure 6-1). The positive lead must be inserted in hole next to reference designator CR1. After proper insertion of diode, secure it in place by soldering its leads on reverse (circuit) side of PCBA.

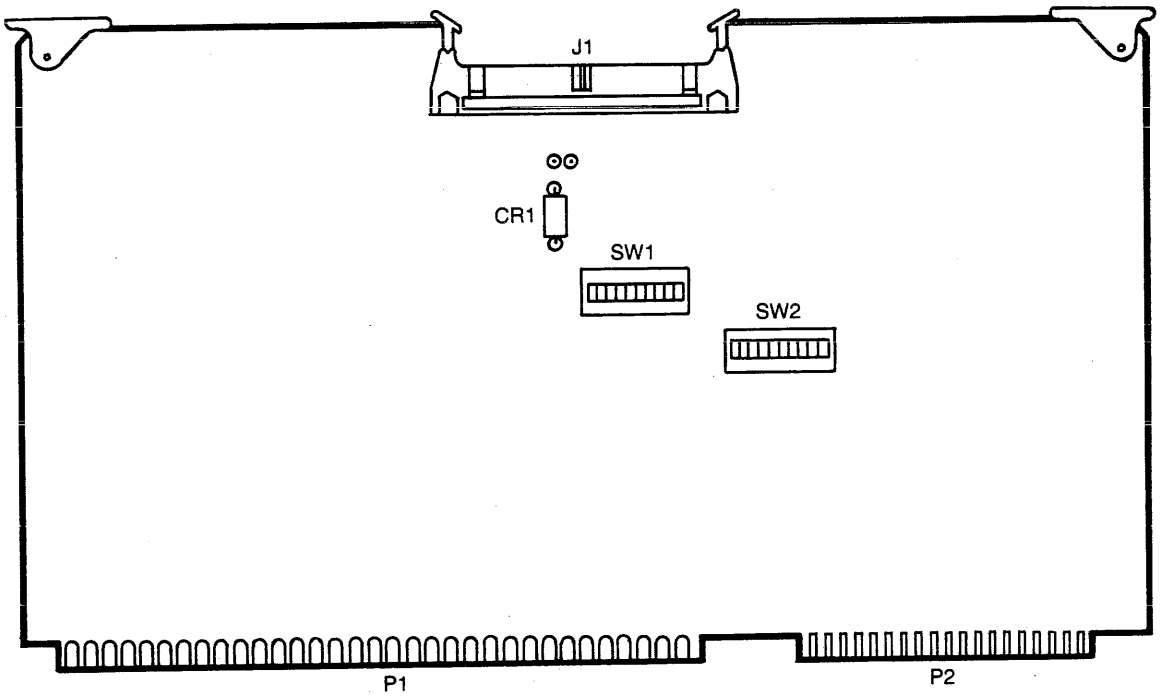

Figure 6-1. Component Locations, MB01 Host Adapter

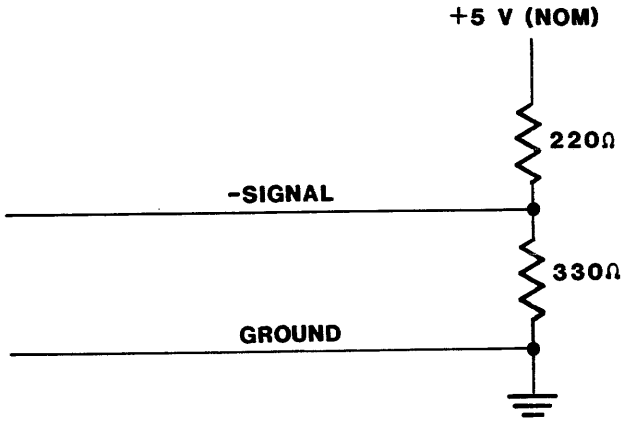

Figure 6-2. SCSI Bus Signals Termination

6.3.3 SCSI BUS SIGNALS AND TIMING

SCSI bus activities involve one or more of the following SCSI phases of operation:

- Arbitration Phase
- Selection Phase
- Reselection Phase
- Command Phase
- Data Phase
- Status Phase
- Message Phase.

These phases are described in Subsection 7.3. When the SCSI bus is not operating in one of the above phases, it is in the Bus Free Phase. SCSI phase sequencing is accomplished by asserting or de-asserting the SCSI signals; the signals are described in Subsection 6.3.3.1.

6.3.3.1 SCSI Bus Signals

There are 18 signals on the SCSI bus. Nine signals are control signals that coordinate transfer of control and status information between SCSI host adapters/controllers; nine signals are for the eight-bits plus parity that constitute the data-transfer portion of the SCSI bus. The signals are listed and described in Table 6-3.

In Table 6-3, the eight data bit signals are represented by DB0 through DB7; DB7 is the most significant bit and has the highest priority during the Arbitration Phase. Bit number, significance, and priority decrease downward to DB0. The parity, represented by the DBP signal, is always odd. All host adapters/controllers on the SCSI bus generate Parity bits and have Parity Detection enabled. During the Arbitration Phase, Parity is not guaranteed to be valid.

Pin/signal assignments for the SCSI bus interface are listed in Table 6-4; they support only the SCSI single-ended option.

Table 6-3. SCSI Bus Signals

Mnemonic Name	Signal	Description
DB0	Data Bus	Data Bus Bit 0
DB1	Data Bus	Data Bus Bit 1
DB2	Data Bus	Data Bus Bit 2
DB3	Data Bus	Data Bus Bit 3
DB4	Data Bus	Data Bus Bit 4
DB5	Data Bus	Data Bus Bit 5
DB6	Data Bus	Data Bus Bit 6
DB7	Data Bus	Data Bus Bit 7
DBP	Data Bus	Data Bus Parity
ACK	Acknowledge	Indicates acknowledgement for a REQ/ACK Data-Transfer Handshake operation
REQ	Request	Indicates a request for a REQ/ACK Data-Transfer Handshake operation
ATN	Attention	Indicates ATTENTION condition (i.e., the Initiator has a message to send to the Target). The ATTENTION condition is described in subsection 7.7.2.
RST	Reset	Indicates RESET condition (i.e., clears the SCSI bus of all activity). The RESET condition is described in subsection 7.7.1.
SEL	Select	Used to select/reselect a SCSI bus device
BSY	Busy	Indicates the SCSI bus is being used
C/D	Control/Data	Indicates transfer of command/status information or transfer of data in/data out information
I/O	Input/Output	Indicates direction of data movement on the Data Bus with respect to an Initiator
MSG	Message	Indicates the SCSI bus is in the Message Phase

Table 6-4. Pin/Signal Assignments at SCSI Bus Interface

Pin	Signal Name	Input/Output
1	GND	--
2	-D0	Input/Output
3	GND	--
4	-D1	Input/Output
5	GND	--
6	-D2	Input/Output
7	GND	--
8	-D3	Input/Output
9	GND	--
10	-D4	Input/Output
11	GND	--
12	-D5	Input/Output
13	GND	--
14	-D6	Input/Output
15	GND	--
16	-D7	Input/Output
17	GND	--
18	-DP (Data parity)	Input/Output
19	GND	--
20	GND	--
21	GND	--
22	GND	--
23	GND	--
24	GND	--
25	Optional GND	--
26	Optional Vcc	--
27	GND	--
28	GND	--
29	GND	--
30	GND	--
31	GND	--
32	-ATN	Input/Output
33	GND	--
34	GND	--
35	GND	--
36	-BSY	Input/Output
37	GND	--
38	-ACK	Input/Output
39	GND	--
40	-RST	Input/Output
41	GND	--
42	-MSG	Input/Output
43	GND	--
44	-SEL	Input/Output
45	GND	--
46	-C/D	Input/Output
47	GND	--
48	-REQ	Input/Output
49	GND	--
50	-Input/Output	Input/Output

6.3.3.2 SCSI Bus Timings

Except where noted, the time-delay measurements for each SCSI device (host adapter or controller) is calculated from signal conditions existing at the SCSI bus connection for that device. Normally, these measurements do not include delays in the SCSI bus cable. The SCSI bus timing criteria are listed and described in Table 6-5.

Figure 6-3 is a timing diagram that shows the typical relationship between SCSI bus signals and SCSI phase sequencing.

Table 6-5. SCSI Bus Timings

Timing	Duration	Description
Arbitration Delay	2.2 μs	The minimum time a SCSI host adapter or controller needs from the time the -BSY signal is asserted for arbitration until the MB01 Host Adapter can examine the Data Bus to determine if arbitration has been won. There is no maximum time.
Bus Clear Delay*	800 ns	The maximum time a SCSI host adapter or controller requires to stop driving all SCSI bus signals after: 1) a Bus Free Phase is detected 2) the -SEL signal is received from another SCSI host adapter or controller during the Arbitration Phase.
Bus Free Delay	800 ns	The minimum time a SCSI host adapter or controller waits after it has detected the Bus Free Phase until it asserts the -BSY signal when going to the Arbitration Phase.

* In the Bus Clear Delay, for condition 1) the maximum time allowed for a SCSI device to clear the SCSI bus is 1200 ns from the time the -BSY and -SEL signals both first become false. If a SCSI device requires more than a Bus Settle Delay to detect the Bus Free Phase, it clears the SCSI bus within the time duration of a Bus Clear Delay minus the excess time.

continued on next page

Table 6-5. SCSI Bus Timings (continued)

Timing	Duration	Description
Bus Set Delay	1.8 μs	The maximum time a SCSI host adapter or controller needs after it detects a Bus Free Phase to assert the -BSY signal and the SCSI ID bit on the Data Bus as a requirement for entering the Arbitration Phase.
Bus Settle Delay	400 ns	The maximum time the SCSI bus needs to settle after changing certain control signals.
Cable Skew Delay	10 ns	The maximum difference allowed in propagation time between any two SCSI bus signals when measured between any two SCSI bus devices.
Deskew Delay	45 ns	The maximum time needed to calculate the minimum time required for deskew of certain signals.
Reset Hold Time	25 μs	The minimum time the -RST signal is to be asserted. There is no maximum time.
Selection Abort Time	200 μs	The maximum timeout duration a Target (or Initiator) must take from its most recent detection of being selected (or reselected) until it asserts the -BSY signal. This timeout is required to ensure a Target (or Initiator) does not assert the -BSY signal after a Selection (or Reselection) Phase has been aborted. This timeout is not the same time as the Selection Timeout Delay.
Selection Timeout Delay	250 ms	The minimum recommended time an Initiator (or Target) should wait for a -BSY signal response, during the Selection or Reselection Phase, before starting the Selection Timeout procedure.

ms = milliseconds
μs = microseconds
ns = nanoseconds

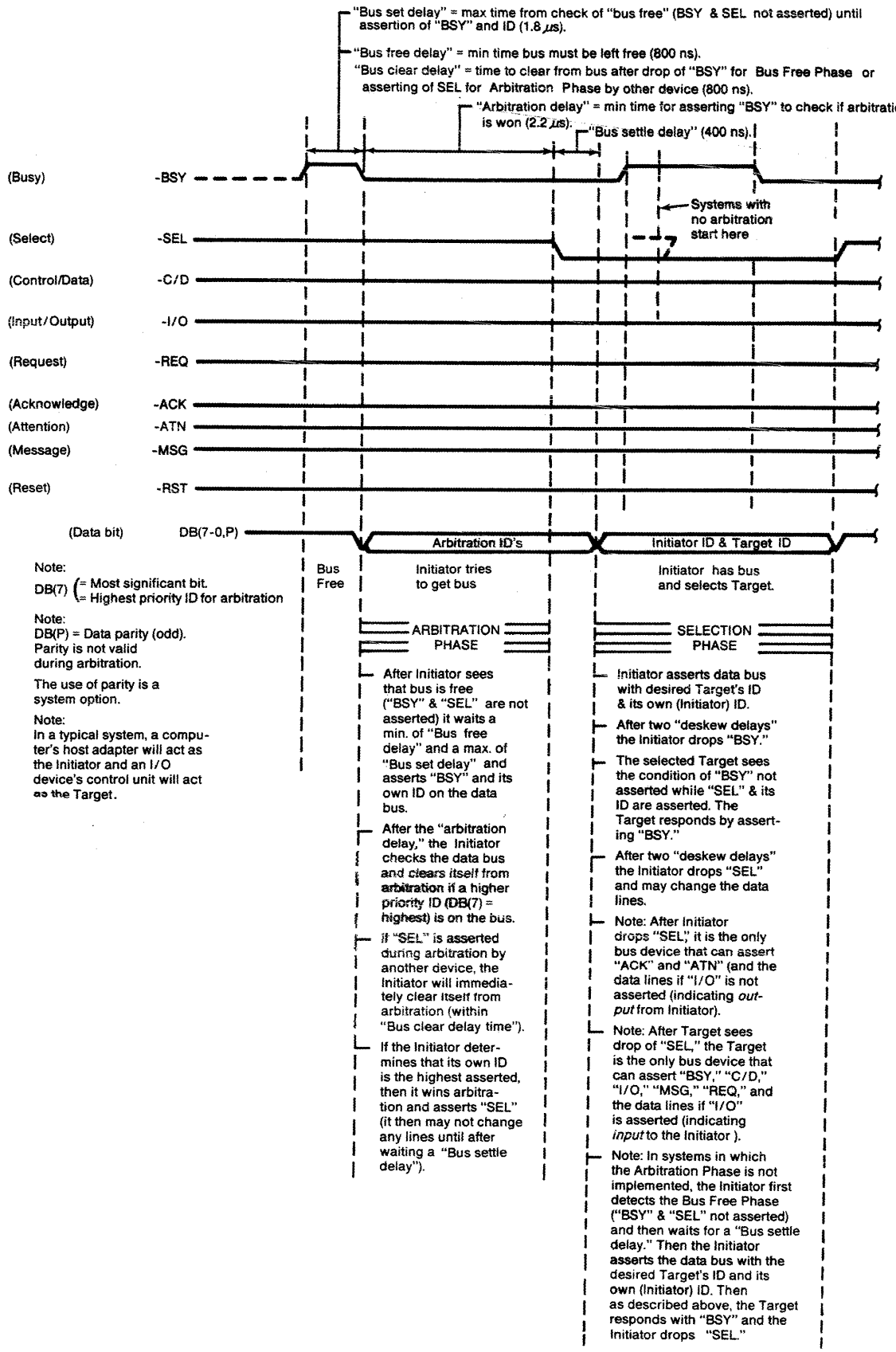

Figure 6-3. SCSI Bus Timing Diagram (Sheet 1 of 3)

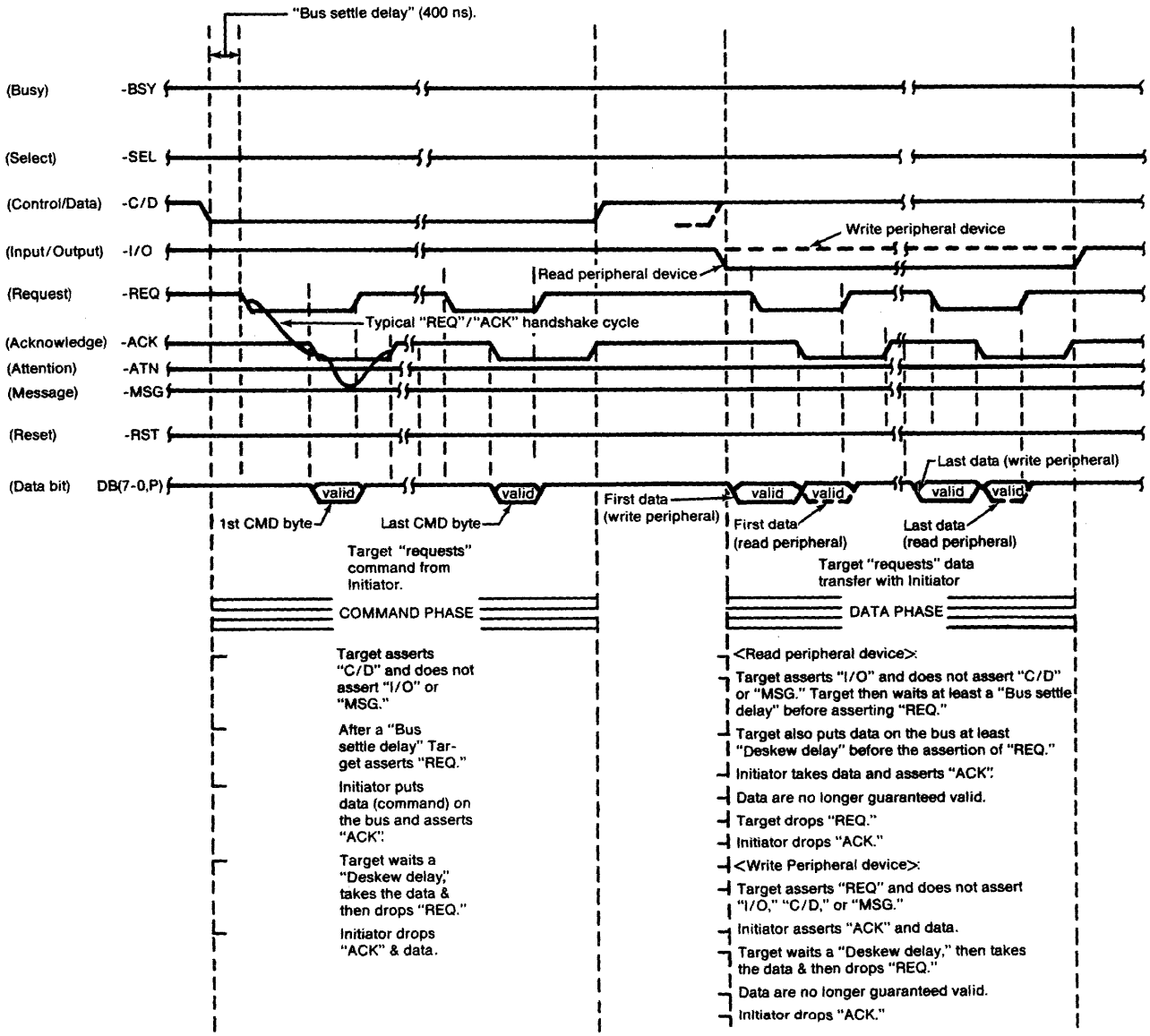

Figure 6-3. SCSI Bus Timing Diagram (Sheet 2 of 3)

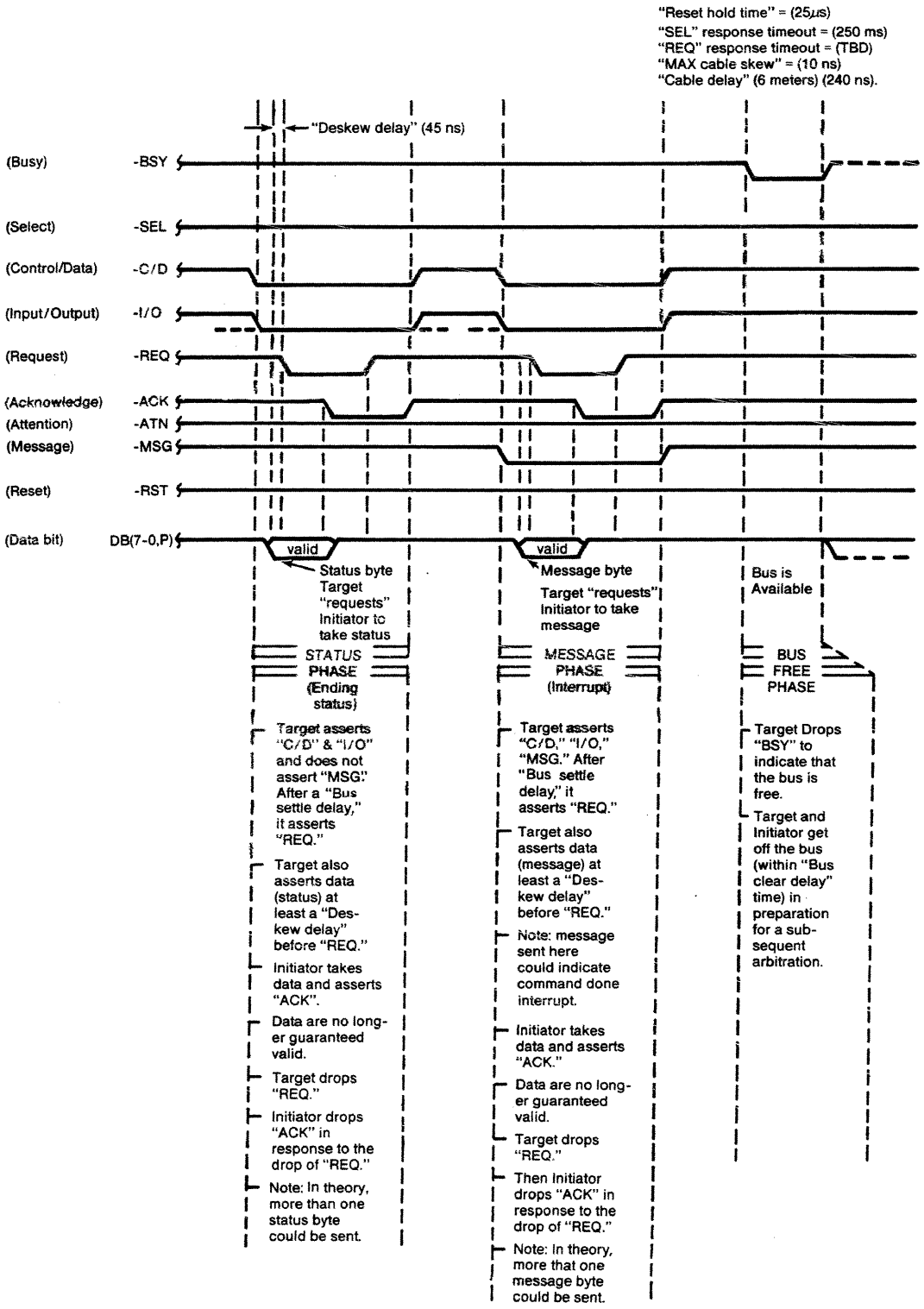

Figure 6-3. SCSI Bus Timing Diagram (Sheet 3 of

7.1 OVERVIEW

This section describes the SCSI bus protocol; it includes information on SCSI bus phases and phase sequencing, procedures for queuing SCSI bus commands, and procedures for passing control and status information between SCSI bus host adapters and controllers by using SCSI memory address pointers. This section is divided into seven subsections, as listed in the following table:

Subsection	Title
7.1	Overview
7.2	SCSI Bus Overview
7.3	SCSI Bus Phases
7.4	SCSI Bus Phase Sequencing
7.5	SCSI Memory Address Pointers
7.6	SCSI Command Queuing
7.7	SCSI Bus Conditions

7.2 SCSI BUS DESCRIPTION

The Small Computer System Interface (SCSI) is a standard interface established to support mass storage, printer output, and network communication for microcomputers and minicomputers. The interface is an eight-port, daisy-chained bus. The SCSI command standard for the MB01 Host Adapter is based on the ANSI X3T.2/82-2 Revision 14 (24 April 84) SCSI Interface Specification (see in subsection 1.1.1).

Up to eight SCSI host adapters and/or controllers can be supported by the SCSI bus. Each controller can be connected to a maximum of eight devices (called Logical Unit Numbers, or LUNs). The MB01 Host Adapter hardware supports any combination of host adapters, intelligent controllers, or intelligent peripherals. Three basic SCSI configurations are supported by the MB01 Host Adapter hardware and SCSI bus:

- single Initiator, single Target
- single Initiator, multiple Target
- multiple Initiator, multiple Target.

Communication via the SCSI bus occurs between a host adapter and a controller. (The MB01 Host Adapter also supports communication between two controllers, as in a SCSI Copy operation.) When a host adapter and a controller communicate, one acts as the Initiator and one acts as the Target. The Initiator (usually a host adapter) originates an operation and the Target (usually a peripheral controller such as an Emulex disk controller or tape controller) performs the operation. Sample system configurations supported by MB01 Host Adapter hardware are shown in Figure 7-1.

Some SCSI bus functions are assigned to the Initiator and some functions are assigned to the Target. The Initiator can arbitrate for control of the SCSI bus and select a specific Target. The Target can request the transfer of command, data, status, or other information via the SCSI bus. In some circumstances, the Target can arbitrate for control of the SCSI bus to reselect an Initiator and continue an operation. Sometimes, the Target becomes an Initiator and arbitrates for control of the SCSI bus; e.g., when it performs a Copy operation.

SCSI bus Data Transfers operations are asynchronous and follow a defined REQ/ACK (request/acknowledge) handshake protocol. (This protocol is defined in the ANSI SCSI specification.) One eight-bit byte of information can be transferred with each handshake.

The SCSI bus contains 18 signal lines. Nine signal lines are for an eight-bit data bus with parity; the other nine signal lines are for control and status signals that coordinate Data Transfer operations between the MB01 Host Adapter and SCSI controllers. SCSI bus signals are described in detail in subsection 6.3.3.1.

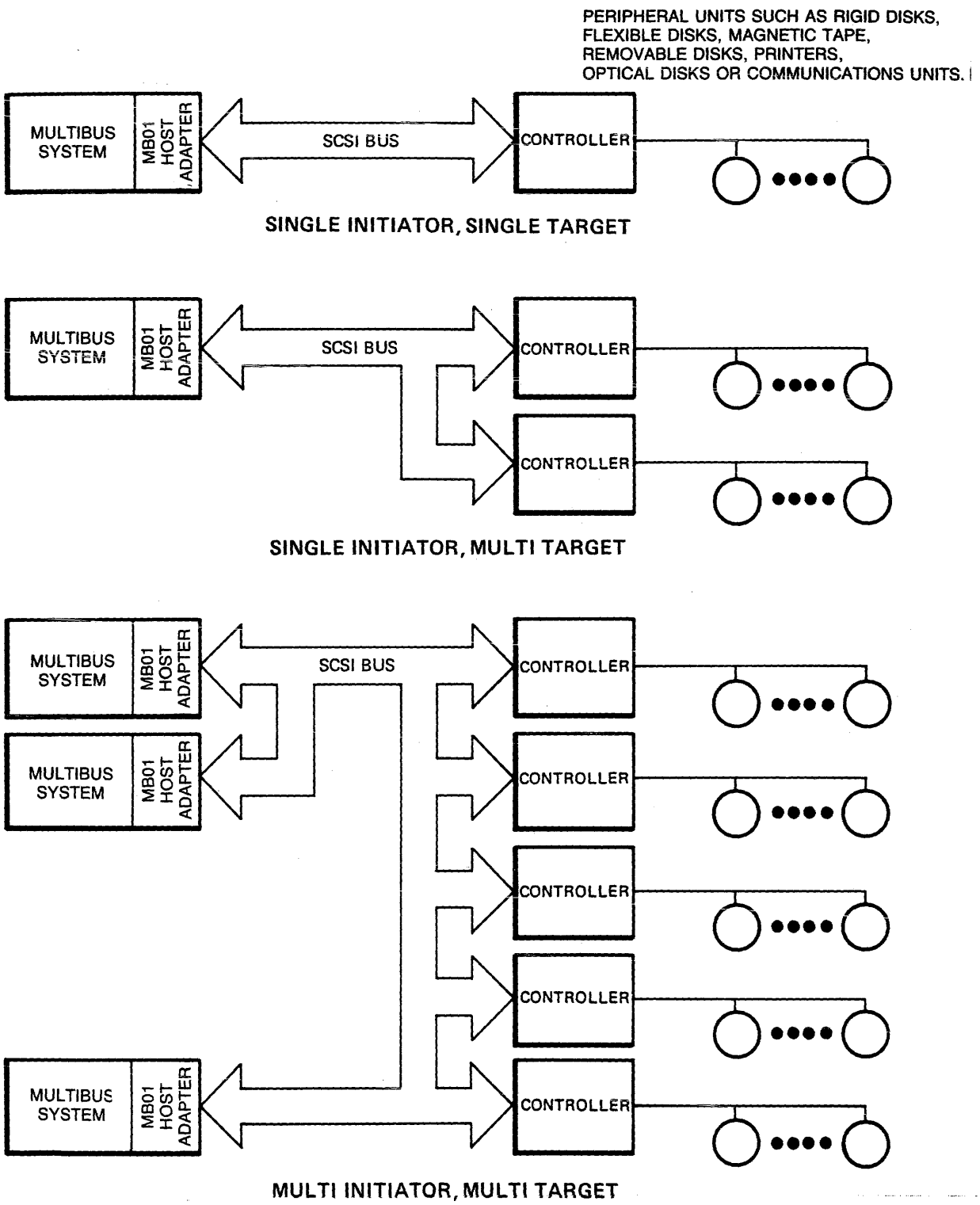

Figure 7-1. Sample SCSI Bus Configurations

7.3 SCSI BUS PHASES

The activities on the SCSI bus can be divided into seven phases of operation:

- Arbitration Phase
- Selection Phase
- Reselection Phase
- Command Phase
- Data Phase
- Status Phase
- Message Phase.

These phases are supported as specified by the ANSI SCSI specification, and are individually described in subsequent subsections, The last four phases (Command, Data, Status, and Message) are grouped together as Information Transfer Phases.

When the SCSI bus is not operating in one of the SCSI bus phases, it is in a Bus Free Phase. The Bus Free Phase indicates no host adapter or controller is actively using the SCSI bus and the SCSI bus is available for subsequent users.

The SCSI bus activities, executed by the MB01 Host Adapter, include Disconnect and Reselection. Overlapped operations on multiple controllers and multiple LUNs are supported.

In the following subsections, no attempt is made to detail the SCSI bus signal sequences; the signals are listed in subsection 6.3.3.1. If detailed signal sequence information is required, refer to the ANSI SCSI specification and the timing diagram in Figure 6-3.

7.3.1 ARBITRATION PHASE

The Arbitration Phase is an optional function sequence performed via the SCSI bus. This phase is used when multiple controllers/processors vie for SCSI bus ownership. Since multiple host adapters and/or controllers may desire control of the SCSI bus concurrently, the MB01 Host Adapter supports the Arbitration Phase for the SCSI bus.

7.3.2 SELECTION AND RESELECTION PHASES

The SCSI Selection and Reselection Phases provide methods for establishing a link between the Initiator and a desired Target.

Usually a SCSI controller for a disk drive or tape drive is selected by an Initiator to perform some function (e.g., Read or Write data). The controller, acting as the Target, then has the option of disconnecting from the SCSI bus. When the Target needs to re-establish the link to its original Initiator, it enters the Reselection Phase to reselect that Initiator.

For the SCSI Copy function, however, the SCSI controller can behave as an Initiator and select another controller as a Target source or destination for the Copy operation. While in the Initiator mode, the SCSI controller always issues an IDENTIFY message (see Table 7-2) after selecting a Target.

The SCSI Selection and Reselection Phases can be terminated when any one of the three following conditions occur:

- The preceding Selection or Reselection Phase is successfully completed by using the Selection/Reselection handshake protocol.
- A Selection/Reselection timeout occurs. The timeout results if any Target or Initiator does not respond to the Selection/Reselection Phase within a timeout period of 250 milliseconds.
- A Reset (-RST) signal occurs on the SCSI bus. When this signal is asserted, all SCSI bus sequences are immediately terminated and the SCSI bus signals are released by all Initiators and Targets.

The Initiator can use the Attention (-ATN) signal to notify a SCSI Target that a message from the Initiator is ready. To guarantee the Target recognizes the Attention condition before the Command Phase is entered, the -ATN signal level must be true before the Selection or Reselection Phase is completed.

If an IDENTIFY message is used during the Selection Phase sequence, the specified LUN has precedence over the LUN field in the Command Descriptor Block (CDB). (CDB's are described in detail in the ANSI SCSI specification.) The IDENTIFY message also informs the Target if the Initiator supports the Disconnect function (see subsection 7.6, SCSI Command Queuing).

NOTE

If the Initiator selects a non-existent LUN, a vendor-unique status of non-existent device (NED bit) and a CHECK CONDITION error status message is returned in the Status Byte (see subsection 7.3.3.3.1). Selected LUNs that have not been initialized by the SCSI device controller report a BUSY status; e.g., at startup, or when not connected to the controller.

7.3.3 INFORMATION TRANSFER PHASES

The Command, Data, Status, and Message Phases are grouped together as Information Transfer Phases because they are all used to transfer data, control, or status information via the SCSI bus. The Information Transfer Phases are described in the following subsections.

7.3.3.1 Command Phase

The Command Phase allows the Target to request command information from the Initiator. An Initiator issues SCSI commands to a Target by transferring a command packet, called a Command Descriptor Block (CDB). The length of the SCSI command and the meaning of the information in the CDB depends on which command is being transferred. (Refer to the ANSI SCSI specification for definitions of SCSI commands and all SCSI CDBs.)

The last byte of every CDB is a control byte and can be differentiated into the following bit groups:

- The low order two bits control the ability of linking commands in a sequence and notifying the host adapter when a particular command (CDB) step is completed. These two bits are designated Flag and Link in the descriptions of command packets described in the ANSI SCSI specification.
- The remaining bits in the control byte are reserved bits, and are always zero.

The remainder of the bytes of the CDB are primarily command-dependent.

The Command Phase is interrupted only for the following exception conditions:

- Reset Condition - This condition can occur when the SCSI Reset (-RST) signal is asserted or when a power fail/power-off condition occurs in the Target. In this circumstance, the Command Phase, and the connection established during the Select/Reselect Phase, is terminated by the Target when it releases the -BSY signal.

- Parity Error Condition - The Target detects a Parity error on the SCSI bus during the Command Transfer operation. At this time, the MB01 Host Adapter issues a RESTORE POINTERS message (see subsection 7.3.3.4) and tries once again to retrieve the command. If it cannot, the -BSY signal is released and the connection is terminated.

7.3.3.2 Data Phase

The Data Phase of a connection controls the transfer of data between the Initiator and Target devices. The Data Phase includes both the Data In and the Data Out Phases. The Data In Phase allows the Target to request sending data to the Initiator from the Target. The Data Out Phase allows the Target to request sending data from the Initiator to the Target. The direction of the Data Transfer operation depends on the command being processed. Some commands may have no data to be transferred and therefore have a null Data Phase. Only the Asynchronous Data Transfer mode is supported by the MB01 Host Adapter.

The Data Phase is interrupted only for the following exception conditions:

- Reset Condition - This condition can occur when the SCSI Reset (-RST) signal is asserted or when a power fail/power-off condition occurs in the Target. In this condition, the Data Phase and the connection established during the Select/Reselect Phase is terminated by the Target when it releases the -BSY signal.

- Data In Parity Error Condition - The Target detects a parity error on the SCSI bus during the Data Transfer operation from the Initiator to the Target. While in the Data Phase, the Target periodically issues SAVE DATA POINTER messages to the Initiator. If the Target detects a Parity error, a RESTORE DATA POINTER message is sent to the Initiator to attempt error recovery. For details about the SCSI Memory Address Pointers, see subsection 7.5.

- Data Out Parity Error Condition - The Initiator detects a parity error on the SCSI bus during the Data Transfer operation from the Target to the Initiator. The Initiator can then assert the Attention (-ATN) signal along with the Acknowledge (-ACK) signal. The Target detects this condition and enters the Message mode to receive a message. The Initiator sends an Initiator-detected error message in response. The Target immediately terminates the command with a CHECK CONDITION status message indicated in the status byte. An optional response to an Initiator-detected Data Phase Parity error is to flag the Data Transfer operation as an error and reissue the command when the current command has terminated.

7.3.3.3 Status Phase

The Status Phase is used by the Target to send command completion information to the Initiator. The status is sent in a single byte, the format of which is defined in subsection 7.3.3.3.1.

The Target can initiate the Status Phase when any one of the following conditions occur:

- Busy Status - The Selection Phase is completed and the Target is in a BUSY state and unable to process any commands for an extended period of time. The Target can initiate the Status Phase immediately after this condition occurs. The status byte transferred has the BUSY status code set.

- Reservation Conflict Status - The Command or Reselection Phase is completed and the specified LUN is reserved for another Initiator. The status byte transferred has the RESERVATION CONFLICT status code set.

- Terminated Status - The current command has completed. The status byte transferred has the GOOD STATUS code set to indicate the success of the command.

NOTE

In multi-Initiator environments, the Initiator delays a minimum of 200 microseconds before attempting another selection of a Target if a BUSY status for that Target is received.

7.3.3.3.1 Status Byte Format. The format of the status byte used by the Target to send completion information to the Initiator is defined below.

Byte	Bit	07	06	05	04	03	02	01	00
00		0	0	0	Status Code				NED

Status Code - Bits <04:01>

These bits are used to specify the Status message. Table 7-1 lists and describes the status codes.

Non-Existent Device (NED) - Bit 00

When the NED bit is set to one, the Initiator selected a LUN which is not configured in the system.

Table 7-1. SCSI Bus Status Codes

Bits 04	03	02	01	Status	Description
X	0	0	0	GOOD STATUS	The SCSI controller successfully completed the command.
0	0	0	1	CHECK CONDITION	An error, exception, or abnormal condition occurred.
X	0	1	0	CONDITION MET	A search condition is satisfied.
0	1	0	0	BUSY	The SCSI controller is busy.
1	0	X	0	INTERMEDIATE STATUS	Sent for every command in a series of linked commands (see subsection 7.3.3.1) unless a CHECK CONDITION or RESERVATION CONFLICT status message is detected.
1	1	0	0	RESERVATION CONFLICT	Sent to an Initiator that attempts to access a SCSI controller when another Initiator has reserved the controller.

1 = Set 0 = Cleared X = Don't Care

7.3.3.4 Message Phase

The Message Phase is used to transfer information about exception conditions between the Initiator and the Target. The Message Phase includes both the Message In and the Message Out Phases. The Message In Phase allows a Target to request that messages be sent to the Initiator from the Target. The Message Out Phase allows a Target to request that messages be sent from the Initiator to the Target. Messages from the Target consist of a single byte; they (and their corresponding hexadecimal codes) are listed and described in Table 7-2.

Table 7-2. SCSI Bus Messages

Code	Message	Description
00	COMMAND COMPLETE	Issued by the Target just before releasing the -BSY signal at the end of a command execution. This message is generally sent immediately after a Status Phase.
02	SAVE DATA POINTER	Issued by the Target to direct the Initiator to save a copy of the present active Data Pointer. This message is issued periodically during multiple block transfers.
03	RESTORE POINTERS	Issued by the Target to direct the Initiator to restore the most recently saved command, data, and Status pointers in the corresponding current pointers. Command and status pointers are restored to the beginning of the current command in the absence of a SAVE DATA POINTER message. The Data pointer is restored to the value it had at the beginning of the command, or to the point where the last SAVE DATA POINTER message occurred. Pointers are described in subsection 7.5.
04	DISCONNECT	Issued by the Target just before releasing the -BSY signal to indicate to the Initiator that the present physical connection is temporarily broken with this message. The current Data, Command, and Status pointers are not saved.
05	INITIATOR DETECTED ERROR	Issued by an Initiator to inform the Target that an error has occurred during a Read operation. At this time, the Target retries the operation.
06	ABORT	Issued by the Initiator to the Target to clear the specified LUN and cause the SCSI bus to go to the Bus Free Phase.

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Table 7-2. SCSI Bus Messages (continued)

Code	Message	Description
07	MESSAGE REJECT	Issued by the Initiator or Target in response to a received message that was undefined.
08	NO OPERATION	A null message issued by the Initiator if the Target requests a message from the Initiator but the Initiator has no message to convey.
09	MESSAGE PARITY ERROR	Issued by the Initiator to inform the MB01 Host Adapter that a Parity error has occurred on a Message Receive operation from the Target to the Initiator.
0A	LINKED COMMAND COMPLETE	Issued by the Target to the Initiator to indicate the completion of a linked command (see subsection 7.3.3.1).
0B	LINKED COMMAND COMPLETE WITH FLAG	Issued by the Target to the Initiator to indicate the completion of a linked command that had the Flag bit set.
0C	BUS DEVICE RESET	Issued by the Initiator to the Target to reset all current I/O on the SCSI bus Target. This message generates a hard Reset Condition (see subsection 7.7.1).
80-FF	IDENTIFY	Issued by the Target or Initiator to establish a connection to a particular LUN. The following bits have particular meaning: Bit 07 - Always set to one. Bit 06 - Set if the Initiator can support Disconnect and Reconnect sequences. **NOTE** If the Disconnect function is supported, this message is issued to the Target at the beginning of every command sequence. Bits <02:00> - Specify (hexadecimal) LUN address in a Target.

7.4 SCSI BUS PHASE SEQUENCING

The status of the SCSI bus is a function of the control signals. (The control signals are described in subsection 6.3.3.1.) These signals place the SCSI bus in one of four phases: Arbitration, Selection/Reselection, Information Transfer, or Bus Free (see subsection 7.3). The order in which SCSI bus phases are used follows the prescribed sequence shown in Figure 7-2.

All SCSI command sequences start with the Bus Free Phase. The normal progression is from the Bus Free Phase to the Arbitration Phase. During arbitration, host adapters/controllers contest for control of the SCSI bus; priority is given to the contestant that has the highest SCSI bus address.

Once a host adapter or controller has control (i.e., is the bus master) of the SCSI bus, the SCSI bus enters the Selection/Reselection Phase. This phase allows the bus master to select a specific device for communication. An Initiator can select a Target to initiate an operation, or a Target can reselect an Initiator to continue an operation.

After a physical path between an Initiator and a Target is established, the SCSI bus enters one of the Information Transfer Phases. These phases include six types of information exchange:

- Data Out Phase
- Data In Phase
- Command Phase
- Status Phase
- Message In Phase
- Message Out Phase.

These types of SCSI bus information exchange are described in more detail in subsection 7.3.

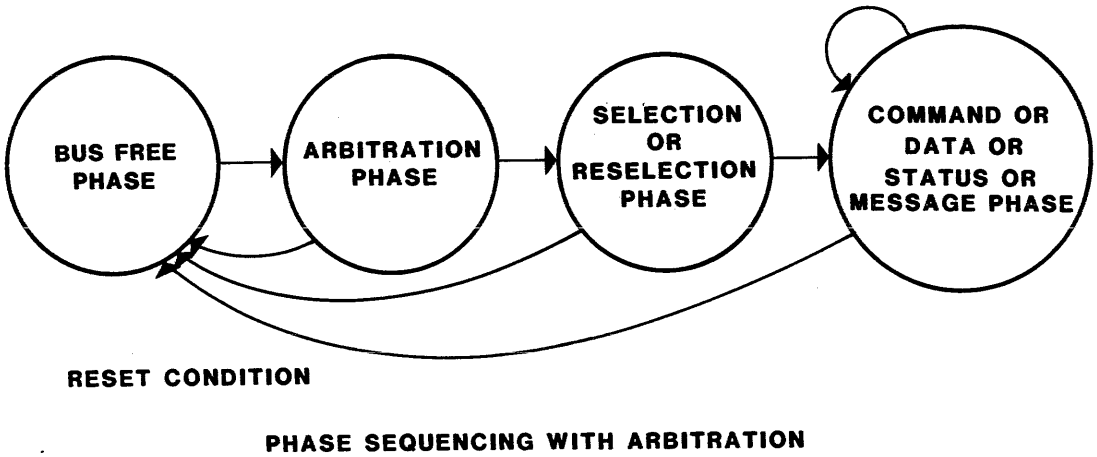

Figure 7-2. SCSI Bus Phase Sequences

7.5 SCSI MEMORY ADDRESS POINTERS

To provide an efficient means of error retry and recovery during large data exchanges via the SCSI bus, the SCSI architecture uses current pointers and saved memory address pointers that reside in the MB01 Host Adapter memory. There are three "conceptual" memory address pointers, located in MB01 Host Adapter memory, that point to the next byte of command, data, or status information to be accessed. The pointers are used to represent the state of the interface. After the pointers are initially loaded by the Initiator, their movement is under control of the Target. When the Target transfers a byte of information to or from one of the three pointers, the position of that pointer is incremented.

The SCSI command set is independent of the type of host adapters and peripheral device controllers (tape drives or disk drives) attached to the SCSI bus. The SCSI command set masks the internal structure of the device (cylinders, tracks, sectors, data blocks, etc.) from the SCSI bus. (The SCSI command set is defined in the ANSI SCSI specification.) IBM PC host memory contains three I/O blocks: command, data, and status. During SCSI bus I/O operations, the SCSI controller uses the MB01 Host Adapter to initially read the contents of the CDB located in host memory to determine the I/O operation to be performed. The SCSI controller then reads from, or writes to, a data block in host memory (via the MB01 Host Adapter) as the I/O operation proceeds. At the end of an I/O operation, the SCSI controller writes a status message (as applicable) to a status block in host memory.

There are two sets of three pointers within the MB01 Host Adapter. The first set, the Current Pointer Values, addresses the next command, status, or data byte to be transferred to the SCSI controller. The second set, the Saved Pointer Values, always addresses the start of the command and status block in host memory, but is incremented for the data block (located in host memory).

During a Data Transfer operation, the Target periodically enters the Message Phase and issues a SAVE DATA POINTER message to the Initiator. If an error occurs, the Target can attempt a Recovery procedure. When the error is detected, the Target goes into the Message Phase and issues a RESTORE DATA POINTER message. The Initiator then backs up its Command, Data, and Status pointers to the last saved state. The Target attempts a Recovery procedure (i.e., performs a Retry operation) by transferring the data from the last saved state.

The frequency of SAVE DATA POINTER messages depends on the block size of the addressed SCSI peripheral device and the dynamically assigned internal buffers used by the SCSI controller. A SAVE DATA POINTER operation usually occurs every 10 blocks. The Target also issues a SAVE DATA POINTER message every time it disconnects from the SCSI bus.

7.6 SCSI COMMAND QUEUING

The Command Queuing feature improves SCSI bus bandwidth by allowing the SCSI controller to queue commands from multiple Initiators rather than requiring these Initiators to continually reissue the commands. If an Initiator indicates it supports the Disconnect function in the IDENTIFY message sent to the Target (SCSI controller), the Target may queue the command if the LUN is busy. The Target saves the Initiator bus device ID and disconnects from the SCSI bus. After the Target has completed execution of the current command, it can reselect the Initiator waiting at the top of its queue, if it is not reserved by a different Initiator.

The Target issues a BUSY message instead of queuing the command if there exists either of two conditions:

- The Initiator does not support the Disconnect function and the addressed LUN is busy
- The addressed LUN is not busy but the SCSI controller is busy because some other LUN is active.

This method of avoiding command queuing avoids deadlocks if the non-disconnecting Initiator requires internal controller resources which are not available when the SCSI bus is in use (connected).

If the same Initiator sends a second command to the same LUN, the Target ignores the second command and continues to execute the original command. The Target sends a BUSY status message to the Initiator in response to the second command.

7.7 SCSI BUS CONDITIONS

The SCSI bus has the following asynchronous conditions:

- Reset Condition
- Attention Condition.

These conditions cause certain SCSI device actions and can alter the phase sequence. The two conditions are described in the subsections below.

7.7.1 RESET

The Reset Condition is used to immediately clear all bus masters from the SCSI bus. This condition takes precedence over all other SCSI bus phases and conditions. During the Reset Condition, no SCSI bus signal except -RST is guaranteed to be valid.

The MB01 Host Adapter supports the SCSI Hard Reset option (the SCSI Soft Reset option is not supported); when a Target (SCSI controller) detects a Reset Condition, it performs the following event sequences:

- Clears all uncompleted commands
- Releases device reservations
- Returns device operating modes (such as the **MODE SELECT** command) to their default conditions.

The Hard Reset condition has the same affect on the Target as power-on; therefore, all Initiator-defined parameters must be resubmitted to the MB01 Host Adapter.

7.7.2 ATTENTION

The Attention Condition allows an Initiator to inform a Target that the Initiator has a message ready. The Target can obtain this message in the Message Phase.