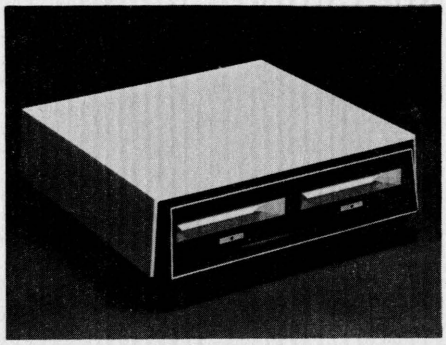
# Diskette Drive
## 1401, 1403, 1404



*Datapoint 1403 Diskette Drive*

August 1981 Document No. 61031



## 1.0 General Description

The Datapoint® 140X series diskette drives provide data storage capability to users of Datapoint 1550 processors. Diskette media is ideal for program and data storage in a DATASHARE® system business processing environment, or for document storage in a word processing environment.

The 1401 unit, designed specifically to provide backup to the Datapoint 9310/9320 10MB Cartridge Disk Drives, contains a single diskette drive (1MB) and handles data on double-sided, double-density diskettes. The 1404 unit supports two single-sided, double-density diskettes (1MB). And the 1403 supports two double-sided, double-density diskettes (2MB). The 1550 Processor can support up to four 140X devices.

Specific diskette drive format and timing characteristics are detailed in section 3.1.1.

## 2.0 System Requirements

All communications between the 140X Diskette Drive controller and the 1550 processor are via the I/O microbus. The I/O microbus is composed of an 8-bit command and address bus, an 8-bit data bus, 2 command strobes, an interrupt request line, and an interrupt acknowledge line.

The cable used on the I/O microbus is a 26-connector flat cable having an integral ground plane. The connectors are 26-pin locking sockets with integral strain relief. The daisy-chaining of peripherals is accomplished by having two connectors on each 140X controller. The connectors on the flat cable are female at both ends.

The maximum I/O microbus length is 10 feet, measured from the microbus connector of the processor to the microbus connector of the last peripheral on line.

## 3.0 Technical Description

### 3.1 Technical Specifications

#### 3.1.1 Diskette Timing and Format Characteristics

| Characteristics | 1401 | 1404 | 1403 |
|---|---|---|---|
| Rotational Speed (RPM): | 360 | 360 | 360 |
| Average Rotational Latency Time (milliseconds): | 83 | 83 | 83 |
| Access Time (max.) (milliseconds) (track to track) | 10 | 10 | 10 |
| Transfer Rate to buffer (bytes/second, max.): | | | |
| from Diskette: | 500K | 500K | 500K |
| from Processor: | 500K | 500K | 500K |
| Settling Time after Head Load (milliseconds): | 50 | 50 | 50 |
| Bytes/Sector: | 256 | 256 | 256 |
| Sectors/Track: | 26 | 26 | 26 |
| Tracks/Diskette: | 77 | 77 | 77 |
| Diskette Recording Surfaces: | two | one | two |
| Recording Density: | double | double | double |
| Bytes/Diskette: | 1,025,024 | 512,512 | 1,025,024 |
| Bits per Inch (inner track): | 6600 | 6600 | 6600 |
| Diskette Drives per module: | 1 | 2 | 2 |
| Bytes/Unit: | 1,025,024 | 1,025,024 | 2,050,048 |
| Buffer Size: | 256 | 256 | 256 |
| Error Detection on Diskette Transfers: | CRC | CRC | CRC |

#### 3.1.2 Diskette Media

| | 1401 | 1404 | 1403 |
|---|---|---|---|
| Media Model Code: | 80498 | 80431 | 80498 |
| Media Diameter (all models): | 7.875 in. (20 cm) | | |
| Envelope Size (all models): | 8 x 8 in. (20.3 x 20.3 cm) | | |

### 3.2 Diskette Loading and Unloading

Figure 3-1 shows a diskette being loaded. Slide the diskette into the slot until a slight click is heard and the diskette no longer pushes back. Push the handle down until it clicks and locks into position.

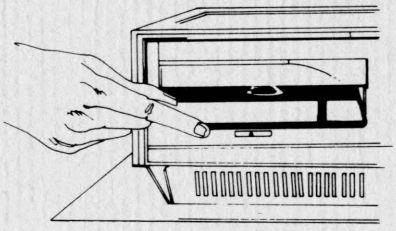


*Figure 3-1: Diskette Insertion*

*Continued....*

### 3.3 Diskette Operations

### 3.3.1 Writing Single Density Data

When single-density data is written to a sector, the first nine bytes of hex FF in the ID Gap are skipped, then 8 bytes of hex 00 are written. This ensures erasure of any D.C. Gap previously written to the sector for double-density data. The 128 bytes of hex E5 in the data field are written over by FM data. All information in a single-density sector is written using the double frequency FM recording scheme.

### 3.3.2 Writing Double Density Data

Before double density data is written to a sector, a two-byte D.C. Gap is written to the ID GAP to identify the sector as a double density sector.

When writing a D.C. Gap to a sector, the first nine bytes of hex FF in the ID Gap are identified and skipped, then the Write Gap is enabled for a period of two bytes (FM). During this period, no pulses will be on the Write Data output. When writing double density data to a double density sector, the controller will search for a D.C. Gap. After the D.C. Gap is found, 12 bytes of hex AA (MFM) will be written, followed by a two byte (MFM) Data Address Mark. The controller will then write 256 bytes of MFM data followed by two CRC bytes (FM, computed from the Data Address Mark through the last data byte) and one byte of hex FF. Note: The Data Address Mark and the two byte CRC will be written in FM mode, the equivalent of 2 and 4 bytes respectively in MFM mode.

Figure 3-2 contains a diagram of sector formats after initialization and after writing double density data.

### 3.3.3 Buffering

The internal data buffer in the controller matches transfer speeds of the I/O microbus and diskette drive electronics. The buffer holds 256 eight-bit bytes and can be randomly or sequentially accessed.

Addressing is accomplished with two pointers called the Processor Pointer and the Disk Pointer. The Processor Pointer can be loaded from the I/O microbus using the OUTPUT PROCESSOR POINTER command ( see Section 3.4). After each processor access of the buffer, the processor pointer is incremented.

The Disk Pointer can be initialized to the beginning of either of the two 128 byte pages. Execution of the OUTPUT DISK PAGE COMMAND (Section 3.4) loads the value of bit 7 of the I/O microbus into the Disk Page Register and resets the Disk Pointer to zero.

When either buffer pointer is incremented by the diskette controller from location 255, the new location will become 0. Do not depend on this wrap-around for resetting the pointers to zero, since any addressing error will affect every buffer access following the error.

Data transfers to or from the processor can occur at the same time that transfers are being made to or from the diskette. Contention for buffer accesses is resolved by the diskette controller.

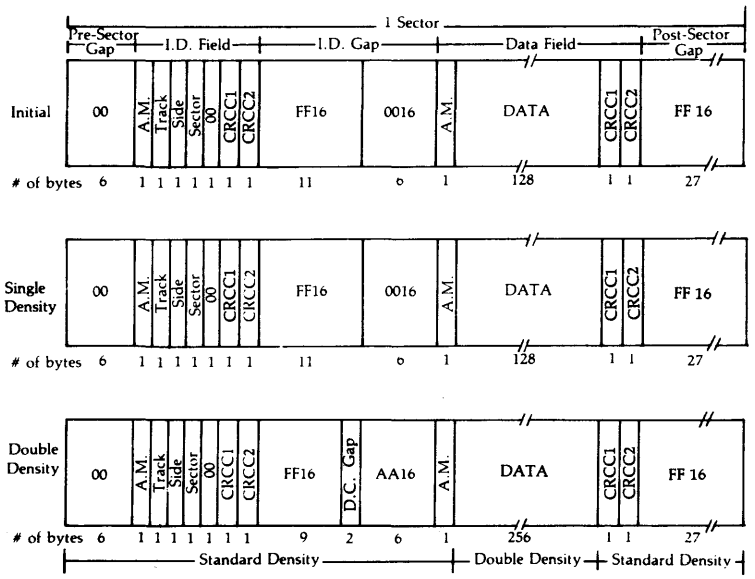



*Figure 3-2. Diagram of Sector Formats*

### 3.3.4 Command and Address Bus

The command and address bus presents four bits of address and four bits of command from the processor to the peripheral. This bus is not-tri-state, is always active, and is low true. Bits zero through three contain a four bit address used to specify one of sixteen peripheral devices.

Selection of the address to which the Dual Diskette subsystem will respond is done through the use of four pluggable jumpers located on the diskette controller board.

These jumpers correspond to the 1550 Address/Command Byte, bits A0 through A3. The decoding process is such that the module responds to one and only one of the 16 unique addreses that can be formed through the binary combination of address bits A0 through A3.

Bits four through seven specify one of sixteen commands. The contents of the command and address bus will always be stable for 100 nanoseconds prior to the leading edge of any strobe and will hold for 100 nanoseconds after the trailing edge of a strobe.

### 3.4 Dual Diskette Commands

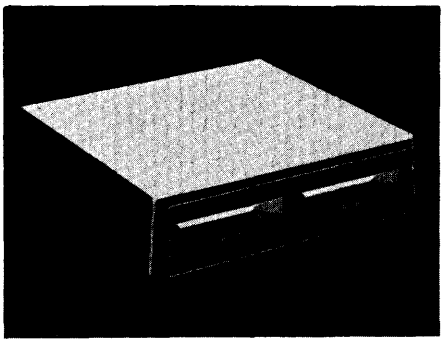
Actual control of the diskette is provided by a controller chip which contains track, sector, command, and data registers referred to in Table 3-2.

### 3.4.1 INPUT STATUS

Places device status on the I/O microbus data lines. Definition of status bits depends upon the previously executed instruction. (Also see Sections 3.4.5, 3.4.6, 3.4.7, 3.4.8 and 3.5.)

### 3.4.2 Input I.D. Byte

The I.D. Byte is defined as follows:
Octal 041 for 1404 Diskette Drive.
Octal 042 for the 1401 and 1403 Diskette Drives.



### 3.4.3 OUTPUT DATA

Transfers the contents of the I/O microbus data lines to the buffer location specified by the processor pointer. The pointer is incremented at the completion of the instruction.

### 3.4.4 INPUT DATA

Transfer data from the buffer location specified by the processor pointer to the microbus data lines. The processor pointer is incremented at the completion of that instruction.

| D7 | D6 | D5 | D4 | Command |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | INPUT STATUS |
| 0 | 0 | 0 | 1 | INPUT DATA |
| 0 | 0 | 1 | 0 | OUTPUT SECTOR NUMBER |
| 0 | 0 | 1 | 1 | INPUT I.D. BYTE |
| 0 | 1 | 0 | 0 | FETCH STATUS |
| 0 | 1 | 0 | 1 | FETCH TRACK |
| 0 | 1 | 1 | 0 | FETCH SECTOR |
| 0 | 1 | 1 | 1 | FETCH DATA |
| 1 | 0 | 0 | 0 | MASTER COMMANDS |
| 1 | 0 | 0 | 1 | OUTPUT TRACK NUMBER |
| 1 | 0 | 1 | 0 | OUTPUT DATA |
| 1 | 0 | 1 | 1 | OUTPUT SEEK NUMBER |
| 1 | 1 | 0 | 0 | OUTPUT PROCESSOR POINTER |
| 1 | 1 | 0 | 1 | OUTPUT DISK PAGE |
| 1 | 1 | 1 | 0 | SELECT DRIVE |
| 1 | 1 | 1 | 1 | INTERRUPT MASK |

*Table 3-2: Command/Address Bus Bits*

### 3.4.5 FETCH STATUS

Sets up the status word for the INPUT STATUS command. FETCH STATUS must precede an INPUT STATUS command for valid status.

### 3.4.6 FETCH TRACK

When followed by the INPUT STATUS command, allows the processor to examine the track register in the controller chip.

### 3.4.7 FETCH SECTOR

When followed by the INPUT STATUS command, allows the processor to examine the sector register on the controller chip.

### 3.4.8 FETCH DATA

When followed by the INPUT STATUS command, allows the processor to examine the data register in the controller chip.

### 3.4.9 MASTER COMMAND

Transfers the contents of the I/O microbus data lines to the command register of the controller chip. Do not issue the MASTER COMMAND if Status Bit 0 (Busy) is set or an undetermined condition will result. Loading the command register causes Status Bit 0 to be set until the specified operation is completed. (Minimum duration of the busy state is 12 microseconds.) The operations that are performed are determined by the value of the data lines. For a detailed description of these operations and their corresponding codes, see Section 3.5.

### 3.4.10 OUTPUT TRACK NUMBER

Writes the value on the I/O microbus data lines into the track register in controller chip.

### 3.4.11 OUTPUT SECTOR NUMBER

Writes the value on the I/O microbus data lines into the sector register in controller chip.

### 3.4.12 OUTPUT SEEK NUMBER

Loads the value of the I/O microbus data lines into a temporary disk register. The value is desired track position when executing a SEEK command.

### 3.4.13 OUTPUT PROCESSOR POINTER

Loads the value of the I/O microbus data lines into the Processor Pointer register. Following execution of the command, the contents of the buffer are transferred to the input data register. The processor pointer is not incremented.

### 3.4.14 OUTPUT DISK PAGE

Loads the value of I/O microbus line 7 into the disk page register and resets the disk pointer to zero.

### 3.4.15 SELECT DRIVE

Loads the value of the I/O microbus data lines 0, 1, 2, and 3 into the Drive Select/Light Register. A zero on data line 0 selects drive 0; a one on data ine 0 selects drive 1. Data line 1 must be zero. A one on data line 2 illuminates the drive 0 indicator; a one on data line 3 illuminates the drive 1 indicator.

*Continued....*

### 3.4.16 INTERRUPT MASK

The interrupt sources will be either enabled or disabled, depending on the value of the I/O microbus data lines. A one bit will enable interrupting, and a zero bit will inhibit interrupts from that source. Interrupts are inhibited at power-up, until enabled by the processor. For an explanation of interrupt sources, see Section 3.5.6. Interrupt bit assignments are as follows:

**Bit Interrupt**
0 Controller chip
1 Processor pointer equal to disk pointer
2 Not used
3 Enable interrupt mask (Mask flip-flops will be unchanged except when bit 3 is a one)
4 Clear controller chip interrupt request flip-flop

## 3.5 Master Commands

The controller chip in the 140X diskette drive accepts master commands from the processor. Command words should not be loaded into the command register when the Busy status bit is on (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is executed, the Busy status bit is set.

When a command is completed, an interrupt is generated and the Busy status bit is reset. The status register indicates whether the completed command encountered an error or was fault free. For ease of discussion,commands are divided into four types and are summarized in Table 3-3.

### 3.5.1 TYPE (I) MASTER COMMANDS

The Type I Commands include the RESTORE, SEEK, STEP IN, and STEP OUT commands. The head is loaded at the beginning of the command. If the controller is idle or 15 revolutions of the diskette, the head will be automatically disengaged.

The RESTORE command contains a verification (V) flag which determines if a verification operation is to take place on the destination track. If V=1, a verification is performed.

If V = 0, no verification is performed.

After a SEEK, STEP IN, or STEP OUT is finished, the firs encountered ID field is read off the diskette. IThe track address of the ID field is then compared the track register. If there is amatch and a valid ID CRC, the verification complete, an interrupt is generated, and the Seek Error status bit (0) is reset. If there is a match but not a valid CRC, the CRC error status bit (Status Bit 3) is set, and the next encountered ID field is read from the diskete for the verification operaion. If an ID field with a valid CRC cannot be found after four revolutions of the diskette, the controller chip terminates the operation and sends an interrupt (INTRQ).

The STEP IN and STEP OUT commands update the track register by one for each step.

#### 3.5.1.1 RESTORE

Upon receipt of this command, the Track 00 Detector is sampled. If the Read-Write head is positioned over track 0, the track register is loaded with zeroes and an interrupt is generated. If the input is not active low, stepping pulses are issued until track 0 is detected. At this time the track register is loaded with zeroes and an interrupt is generated. If the input does not go active low after 255 stepping pulses, the controller will terminate the operation and set the Seek Error status bit.

#### 3.5.1.2 SEEK

The SEEK command assumes that the track register contains the track number of the current position of the Read-Write head and the data register contains the desired track number. The controller will update the track register and issue stepping pulses in the appropriate direction until the contents of the track register are equal to the contents of the data register (the desired track location). A verification operation then takes place.

The head will be loaded at the start of the command. An interrupt is generated at the completion of the command.

If a SEEK command is issued to the current track, the busy status bit will be set and will remain set for approximately 250 microseconds. When the operation is complete, the busy status bit will be reset and a command-complete controller chip interrupt will be generated.

If a SEEK command is attempted to a track number greater than 76, the head will be moved to track 76 and step pulses will be generated as if the track number is valid with the motor against a hard stop. If the verify flag is set, a seek error status bit will be set. If the verify flag is not set, the next read or write operation will probably fail.

#### 3.5.1.3 STEP IN

Upon receipt of this command, the controller will issue one stepping pulse in the direction toward track 76. The track register is incremented by one. After a 30 msec delay, a verification takes place. The head will be loaded at the completion of the command.

#### 3.5.1.4 STEP OUT

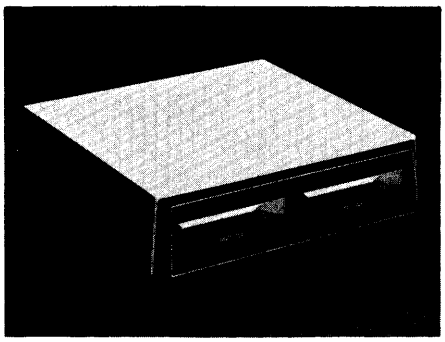
Upon receipt of this command, the controller will issue one stepping pulse in the direction toward track 0. The track register is decremented by one. After a 30 msec delay, a verification takes place. The head will be loaded at the completion of the command.

### 3.5.2 TYPE II MASTER COMMANDS

The Type II commands are the READ SECTOR and WRITE SECTOR commands. Prior to loading the Type II command into the command register, the processor must load the sector register with the desired sector number. Upon receipt of the type II command, the busy status is set.

| TYPE | COMMAND | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| I | RESTORE | 0 | 0 | 0 | 0 | 1 | V | 1 | 0 |
| I | SEEK | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| I | STEP IN | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| I | STEP OUT | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| II | READ SECTOR FM | 1 | 0 | 0 | 0 | $\overline{s}$ | 0 | 0 | 0 |
| II | READ SECTOR MFM | 1 | 0 | 0 | 0 | $\overline{s}$ | 0 | 1 | 0 |
| II | WRITE SECTOR FM | 1 | 0 | 1 | 0 | $\overline{s}$ | 0 | 0 | a0 |
| II | WRITE SECTOR MFM | 1 | 0 | 1 | 0 | $\overline{s}$ | 0 | 1 | 0 |
| II | WRITE DC GAP | 1 | 1 | 1 | 0 | $\overline{s}$ | 0 | 0 | 0 |
| III | READ ADDRESS | 1 | 1 | 0 | 0 | $\overline{s}$ | 0 | 0 | 0 |
| IV | FORCE INTERRUPT | 1 | 1 | 0 | 1 | I3 | I2 | I1 | I0 |
| Note: Bits shown in TRUE form. | | | | | | | | | |

*Table 3-3: Master Command Summary*



When an ID field is located on the diskette, the controller compares the track number of the ID field with the track register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there is a match, the sector number of the ID field is compared with the sector register. If there is not a sector match, the next encountered ID field is read off the diskette and comparisons again are made. If the ID field CRC is correct, the data field is then located and either written into or read from, depending on the command. The controller must find an ID field with a track number, sector number, and CRC within five revolutions of the diskette; otherwise, the Record Not Found status bit (status bit 4) is set and the command is terminated with an interrupt.

### 3.5.2.1 READ FM SECTOR

Upon receipt of this command, the head is loaded and the Busy status is set. When an ID field is encountered that has the correct track number, correct side bit, correct sector number, and correct CRC, the 128 bytes are transferred to the buffer. The data address mark of the data field must be found within 30 bytes of the last ID field CRC byte. If not, the Record Not Found status bit is set and the operation is terminated.

If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated. At the end of the read operation, the type of data address mark encountered in the data field is recorded in the status register (bit 5) as shown below:

Status Bit 5 Type of Address Mark

1 Deleted Data Mark
0 Data Mark

### 3.5.2.2 READ MFM SECTOR

Upon receipt of this command, the head is loaded and the busy status bit is set, and when an ID field is encountered that has the correct track number, correct side bit, correct sector number, and correct CRC, the controller then searches for a field at least 32 microseconds long having no transitions (DC field). If this gap is located within 30 MFM bytes (480 microseconds) after the header CRC, the controller then searches for a Data ID Sync byte. This byte must be found within 20 MFM bytes (320 microseconds) after DC. If neither DC gap nor sync is found in time, the Record Not Found status bit is set and the operation is terminated. When the controller finds a sector which has a correct track number, correct side bit, correct sector number, correct CRC, a proper DC gap,and correct data ID mark, then 256 bytes of data are transferred to the buffer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated.

### 3.5.2.3 WRITE FM SECTOR

Upon receipt of this command, the head is loaded and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct side bit, correct sector number, and correct CRC, a data sector is written. The controller counts off 9 bytes from the CRC field, the Write Gate (WG) output is made active, and 8 bytes of zeroes are then written on the diskette. At this time the data address mark is written on the diskette as determined by the a0 field of the command as shown below:

a0 Type of Address Mark
1 Deleted Data Mark
0 Data Mark

The controller then writes the data field from the buffer. After the last data byte has been written on the diskette, the two byte CRC is computed internally and written on the diskette followed by one byte of logic ones. The Write Gate output is then deactivated.

### 3.5.2.4 WRITE MFM SECTOR

Upon receipt of this command, the head is loaded, the Read Gate is set, and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct side bit, correct sector number, and correct CRC, the controller then counts off the equivalent of 11 bytes (FM) from the CRC field and the Write Gate output is made active if a Wide Gap has been detected (at least 32 microseconds with no transitions). If a Wide Gap is not detected, the command is terminated and the Record Not Found status bit is set. If a Wide Gap has been detected, the Write Gate is made active and 12 bytes of hex AA are written on the diskette. This is followed by a two-byte MFM data address mark.

The controller then writes the data field. After the last data byte has been written on the diskette, the two-byte CRC is computed internally and written on the diskette followed by one byte of hex FF. The Write Gate output is then deactivated.

Note: The address mark and the two-byte CRC are written in FM mode, the equivalent of 2 and 4 bytes, respectively, in MFM. The CRC calculation includes the one byte FM data address mark.

### 3.5.2.5 WRITE DC GAP

Upon receipt of this command, the head is loaded, the Busy status bit is set, and the Read Gate is enabled. When the ID field is encountered that has the correct track number, correct side bit, correct sector number, and correct CRC, the controller counts off 9 bytes (FM) and turns on the Write Gate for a period of 2 bytes (64 usec). During the period that the Write Gate is on, there are no pulses on the Write Data output.

Table 3-4 summarizes type II flag bits.

| Bit | Description |
|---|---|
| a0 | Data Address Mark (Bit 0) |
| | a0= 0, FB (Data Mark) |
| | a0= 1, F8 (Deleted Data Mark) |
| $\bar{s}$ | Side Bit (Bit 3) (negative true) |
| | $\bar{s}$= 0, Side One |
| | $\bar{s}$= 1, Side Zero |

*Table 3-4: Type II Commands Flag Summary*

*Continued....*

### 3.5.3 TYPE III MASTER COMMANDS

#### 3.5.3.1 READ ADDRESS

Upon receipt of this command, the head is loaded and the Busy status bit is set. The next encountered ID field is then read in from the diskette, and the six data bytes of the ID field are assembled and transferred to the buffer at the location addressed by the disk pointer. The six bytes of the ID are as follows:

1 Track Address
2 Side Number (0 = side zero; 1 = side one)
3 Sector Address
4 Sector Length
5 CRC1
6 CRC2

Although the CRC characters are transferred to the buffer, the controller checks for validity and the CRC error status bit is set if there is a CRC error. The track address of the ID field is written into the sector register in the controller chip. At the end of the operation, an interrupt is generated and the Busy status bit is reset.

The only flag bit for a Type III command is the Side Bit (bit 3). The side bit equals 0 for side one; one for side zero.

### 3.5.4 TYPE IV MASTER COMMANDS

#### 3.5.4.1 FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy status bit set), the command will be terminated and an interrupt generated when the condition specified in the I0 through I3 field is detected. The interrupt conditions are shown in Table 3-5.

| Interrupt Flags | Description |
|---|---|
| I0=1 | Not-ready to ready transition |
| I1=1 | Ready to Not-ready transition |
| I2=1 | Index Pulse |
| I3=1 | Immediate Interrupt |

Note: If I0 through I3 are zero, there is no interrupt generated, but the current command is terminated and the Busy status bit is reset. FORCE INTERRUPT is the only command that will clear the immediate interrupt.

*Table 3-5: Type IV Commands Summary*

### 3.5.5 STATUS DESCRIPTION

Upon receipt of any command, except the FORCE INTERRUPT command, the Busy status bit is set and the rest of the status bits are updated or cleared for the new command. If the FORCE INTERRUPT command is received when there is a current command under execution, the Busy status bit is reset and the rest of the status bits remain unchanged. If the FORCE INTERRUPT command is received when there is not a current command under execution, the Busy status bit is reset and the rest of the status bits are updated or cleared. In this case, the Busy status bit reflects the Type I commands.

The significance of each bit in the status register varies with the command being executed. Status bits, when set, have the following meanings:

#### 3.5.5.1 TYPE I COMMAND

| Status Bit | Meaning |
|---|---|
| 7 | Drive not ready |
| 6 | Write protection is activated |
| 5 | Head is loaded and engaged |
| 4 | SEEK ERROR - desired track not verified |
| 3 | CRC error in either the ID or data field |
| 2 | Read/Write head positioned to track 0 |
| 1 | Index mark detected from the drive (true only for duration of index pulse) |
| 0 | Busy - command is in progress |

#### 3.5.5.2 READ SINGLE

| Status Bit | Meaning |
|---|---|
| 7 | Drive not ready |
| 6 | Same as bit 5 |
| 5 | Indicates the record type code from the data field address mark |
| 4 | Record not found (desired track and sector not found) |
| 3 | CRC error in either the ID or data field |
| 2 | Lost data |
| 1 | DRQ |
| 0 | Busy - command is in progress |

#### 3.5.5.3 READ DOUBLE

| Status Bit | Meaning |
|---|---|
| 7 | Drive not ready |
| 6 | Same as bit 5 |
| 5 | Indicates the record type code from the data field address mark |
| 4 | Record not found (track and sector not found) |
| 3 | CRC error in either the ID or data field |
| 2 | Lost data |
| 1 | DRQ |
| 0 | Busy - command is in progress |

### 3.5.5.4 WRITE SINGLE

| Status Bit | Meaning |
|---|---|
| 7 | Drive not ready |
| 6 | Write protection activated |
| 5 | Write fault |
| 4 | Record not found (track and sector not found) |
| 3 | CRC error in either the ID or data field |
| 2 | Lost data |
| 1 | DRQ |
| 0 | Busy - command in progress |

### 3.5.5.5 WRITE DOUBLE

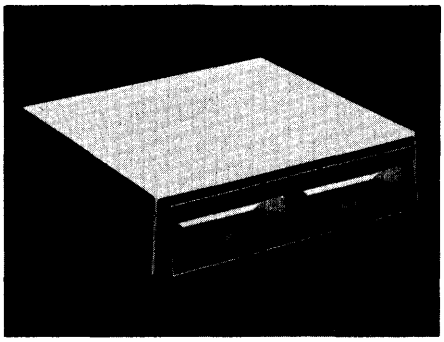
| Status Bit | Meaning |
|---|---|
| 7 | Drive not ready |
| 6 | Write protection activated |
| 5 | Write fault |
| 4 | Record not found (track and sector not found) |
| 3 | CRC error in either ID or data field |
| 2 | Lost data |
| 1 | DRQ |
| 0 | Busy - command in progress |

### 3.5.5.6 READ ADDRESS

| Status Bit | Meaning |
|---|---|
| 7 | Drive not ready |
| 6 | Two-sided diskette inserted in drive |
| 5 | Wide Gap detected within 11 byte times (FM) following the last address field CRC byte |
| 4 | Record not found (track and sector not found) |
| 3 | CRC error in either the ID or data field |
| 2 | Lost data |
| 1 | DRQ |
| 0 | Busy - command in progress |

### 3.5.5.7 WRITE DC GAP

| Status Bit | Meaning |
|---|---|
| 7 | Drive not ready |
| 6 | Write protection activated |
| 5 | Write fault |
| 4 | Record not found (track and sector not found) |
| 3 | CRC error in either ID or data field |
| 2 | Always 0 |
| 1 | DRQ |
| 0 | Busy - command in progress |



# Diskette Drive
## 1401, 1403, 1404

### 3.5.6 Interrupt Requests

There are two sources for the "Interrupt Request" signal in the 140X controller.

### 3.5.6.1 Controller Chip Interrupt

This interrupt request is generated from the controller chip if mask bit 0 is set and any of the following conditions occur:

1. Not-ready to Ready transition
2. Ready to Not-ready transition
3. Index pulse
4. Immediate
5. Command complete

With the exception of the command complete interrupt, these interrupts can be individually masked with a FORCE INTERRUPT master command. If any of the preceding conditions occurs, or a controller chip interrupt master command is completed, an Interrupt Request will be generated.

### 3.5.6.2 Interrupt Acknowledge

The diskette controller will respond to the Interrupt Acknowledge signal from the processor if it has previously generated an Interrupt Request by not forwarding the Interrupt Acknowledge (IACK) signal to additional peripheral devices and by placing an interrupt status byte on the I/O microbus data lines as follows:

| | |
|---|---|
| Bit 0 - 3 | Peripheral device address |
| Bit 4 | Processor pointer unequal to disk pointer interrupt |
| Bit 5 | Controller chip interrupt |
| Bit 6 | Drive number |
| Bit 7 | Head number |

If no Interrupt Request signal is generated, the diskette controller will generate an IACK OUT signal in response to the IACK IN signal. The IACK OUT then becomes an IACK IN to the next device on the I/O microbus. The priority of interrupting devices on the I/O microbus is the same as the order in which they appear on the micro bus daisy chain beginning at the processor.

The peripheral device address jumpers can be field modified. Address 00 is assigned to the first diskette module.

### 3.5.7 Strobes

There are two strobes on the 140X I/O microbus: Strobe 1 (USTB1) and Strobe 3 Interrupt Acknowledge (IACK). Strobe 1 is 400 nanoseconds long and its function is defined according to the requirements of the peripheral. The bi-directional data bus is controlled by the strobes according to the specific needs of each peripheral. The strobes are unique and will never occur simultaneously. The minimum spacing between strobes is at least 100 nanoseconds.

### 3.5.8 Data Bus

The data bus is an 8-bit bi-directional bus used to communicate data to and from the 1550 processor. It is an open collector bus and is in the off state between strobes. The direction of data transfer on the data bus is defined by the control processor. For all output instructions, the data bus will be valid from 100 nanoseconds before the start of the strobe to 100 nanoseconds after the trailing edge of the strobe. For input data, the peripheral should place its data or status on the data bus as soon as the strobe is received and remove the data when the strobe is complete. The data bus is ground true.

# Diskette Drive
## 1401, 1403, 1404

*Continued....*

## 4.0 Physical Description

Figure 4-1 shows the dimensions of the 140X Diskette Drive, which weighs approximately 66 pounds (30 kg).

Height: 7.2 in. (18.3 cm)
Width: 21.8 in. (55.4 cm)
Depth: 23.9 in. (60.7 cm)

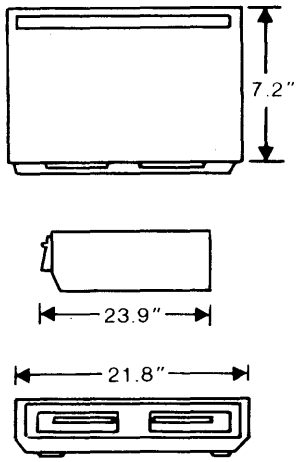



*Figure 4-1: 140X Diskette Dimensions*

## 5.0 Environmental Requirements

Temperature: 50 to 100 degrees F
10 to 38 degrees C
Humidity: 20 to 80 % relative, non-condensing
Heat Dissipation: 530 BTU/Hr

WARNING: This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

## 6.0 Interface Requirements

### 6.1 I/O Microbus Pin Assignments

| Pin | Signal |
|---|---|
| 1 | Ground |
| 2 | Strobe 1 |
| 3 | Ground |
| 4 | Strobe 2 |
| 5 | Ground |
| 6 | IACK |
| 7 | Ground |
| 8 | Address 0 |
| 9 | Address 1 |
| 10 | Address 2 |
| 11 | Address 3 |
| 12 | Comm 0 |
| 13 | Comm 1 |
| 14 | Comm 2 |
| 15 | Comm 3 |
| 16 | Spare |
| 17 | Interrupt Request |
| 18 | Data 0 |
| 19 | Data 1 |
| 20 | Data 2 |
| 21 | Data 3 |
| 22 | Data 4 |
| 23 | Data 5 |
| 24 | Data 6 |
| 25 | Data 7 |
| 26 | +5 V (Power Indicator) |

### 6.2 Primary Power

The 140X Diskette Drive, as supplied from Datapoint, is designed to operate at 120 VAC (+10% -15%), 60 HZ, +/ - 2%. However, it is field configurable for operation with an input voltage of 100, 120, 220, 230, 240 VAC, 50 or 60 Hz (+/-2%). Note that conversion from 50 to 60 Hz operation requires the changing of the drive pulley and belt.

Power consumption is 155 Watts.

The Diskette Drive draws 1.33 amps at 120 VAC.

## 7.0 Options

## 8.0 Shipping List

| Quantity | Item |
|---|---|
| 1 | 140X Dual Diskette drive |
| 1 | Product specification (Document No. 61031) |
| 1 | I/O Microbus Cable |
| 1 | Power Cord |

Note: This shipping list is provided for information purposes only and may be amended for time to time by Datapoint Corporation.

DATAPOINT

Datapoint recommends that its customers use Datapoint Customer Supplies. These disks, diskettes, cassettes and ribbons are certified by Datapoint to meet all Datapoint hardware specifications for consistent optimum performance. Reference Document No. 80000, the Customer Supplies Catalog, for ordering information.