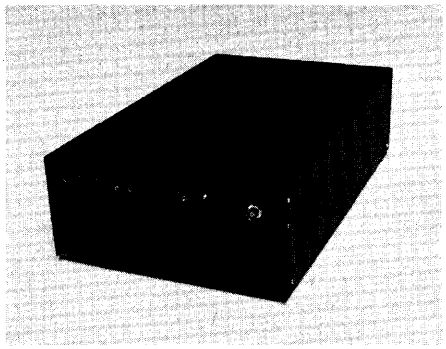
DATAPOINT
Product Specifications

Resource Interface Module

9483



The 9483 Resource Interface Module (RIM).

July 20, 1981 Document No. 60911

1.0 General Description

The 9483 RIM (Resource Interface Module) is a special purpose communications interface designed to provide high speed communications between a number of Datapoint processors (throughout this specification the term "processor" denotes any Datapoint processor with an I/O bus compatible with the Datapoint 5500). Data is carried over coaxial cable at 2.5 million bits per second in a unique Datapoint format, and includes error checking. The system incorporates a self-polling feature that eliminates the need for a master station in the system. Each RIM has a unique identification number and packets may be sent to one specific RIM or broadcast to all RIMs in the system. RIMs receive only those packets addressed to them or broadcast to all RIM's (reception of BROADCAST may be inhibited under processor control). Packets are interleaved so that the system can simultaneously support a number of independent communication paths without the processors realizing that they do not have exclusive use of the system.

2.0 System Requirements

2.1 System Components

The 9483 RIM has its own power supply and may be mounted on the back of any Datapoint console table or on any flat surface. Interface to the processor is via a Universal I/O Cable.

If there are more than two RIMs in a system a 9485 Passive Hub or one or more 9484 Active Hubs will be required to interconnect the RIMs (see section 2.2).

2.2 System Configuration

RIM units are interconnected with lengths of RG62/U coaxial cable fitted with a male BNC type connector at each end.

If a system consists of only two RIMs they may be interconnected with a single cable up to 2000 feet in length. If more than two RIMs are included, however, a single Passive Hub, or one or more Active Hubs, will be required.

A Passive Hub may be used to interconnect up to four RIMs with the restriction that the sum of the longest two lengths of cable connected to the Passive Hub be less than 200 feet. Unused ports on the Passive Hub must be terminated into 93 ohms with the terminators provided.

One or more Active Hubs are used in systems with more than four RIMs or where the distance between RIMs exceeds the 200 foot Passive Hub limitation. When Active Hubs are used the maximum cable length between Active Hub ports and RIM ports or other Active Hub ports cannot be greater than 2000 feet, and there may be no more than 10 Active Hub ports in the path between any two RIM ports in the system.

The number of RIMs in a system cannot exceed 255.

3.0 Technical Description

3.1 RIM Description

The RIM consists of six sections: BUFFER, STATUS WORD, CONTROLLER, TRANSMITTER, RECEIVER, and LINE INTERFACE. The processor can transfer data to and from the BUFFER and test and reset bits in the STATUS WORD. The LINE INTERFACE interfaces the TRANSMITTER and RECEIVER to the coaxial LINE.

The RIM contains a 1024 byte memory which is used as a random access speed buffer between the processor and the RIM's transmitter and receiver. The buffer memory is divided into 4 pages of 256 bytes each.

There are three page registers: one each for the processor, the TRANSMITTER, and the RECEIVER. All INPUT, PIN, and MIN instructions when the RIM is in DATA mode and all EX WRITE and MOUT instructions act on the buffer page selected by the processor page register. The TRANSMITTER reads data from the buffer page selected by the transmitter page register. The RECEIVER writes data into the buffer page selected by the receiver page register. The page registers are independent and remain set until changed by EX COM1 commands.

Data transfers to or from the processor may be made at any time, whether or not the transmitter or receiver is busy and independent of any status bits. These transfers may be made at the full MIN/MOUT rate of the Datapoint 5500 processor. Care should be taken that transfers not be made from the processor to the page accessed by the transmitter when the transmitter is not available or to the processor from the page accessed by the receiver until the receiver is inhibited. Unless a specific address is provided, the buffer memory will automatically address sequentially and wrap around within a page.

Each RIM in a system has a unique ID (IDentification) from 1 to 0377 selected by switches in the RIM. (ID 0 may not be assigned to any RIM since destination 0 is used to indicate a BROADCAST to all RIMs.)

Two LED indicators are located near the BNC connector along with a reset button.

The "local reconfigure" indicator (nearest the BNC connector) is turned on to indicate that an excessive number (more than 16 per minute) of reconfigurations are being initiated by this RIM.

Reconfigurations occur when the RIM is not included in the system polling and can be caused by damaged cable, line noise, or a defective RIM. Excessive reconfiguration can be an indication that the RIM is disconnected from the system or that there are no other operating RIMs on line. Once the LED has been triggered it will remain on until the reset button is depressed (see Figure 4-1).

The "excessive mark" LED indicates that the RIM has transmitted an abnormal number (greater than 10) of consecutive marks. This

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might indicate a failure in the RIM transmitter which could inhibit system operation until the RIM is disconnected from the line.

3.2 Programming Considerations

All communication between the RIM and the processor is via the input/output bus using the External Command, INPUT, PIN, MIN, and MOUT instructions. (See Processor Reference Manual.)

3.2.1 EX ADDRESS

This strobe sets ADDRESSED and STATUS modes in the RIM if the proper address is present on the processor I/O bus. ADDRESSED mode remains set until another I/O device is addressed with another EX ADDRESS. EX ADDRESS is the only command recognized by the RIM when ADDRESSED mode is not set.

3.2.2 EX STATUS

This strobe sets STATUS mode in the RIM so that the status word will be transferred to the processor when an INPUT instruction is executed. See section on EX COM1 and section 3.3 for use of the status word. The status word format is as follows:

Bit

0...TA : Transmitter Available

1...TMA : Transmitted Message Acknowledged

2...RECON: System Reonfiguration has occurred

3...TPE : Transmitter Parity Error

4...POR : Power-On-Reset occurred

5...DA : Device Available (always 1)

6...IPE : Interface Parity Error

7...RI : Receiver Inhibited

3.2.3 EX DATA

This strobe sets DATA mode in the RIM so that data from the buffer will be transferred to the processor when an INPUT instruction is executed.

3.2.4 INPUT

This strobe transfers the status word or data to the processor. Data transfer is from the current processor page and address in buffer memory. Address wrap-around, within the selected page, occurs when byte 0377 is transferred. The RIM also supports the PIN and MIN instructions implemented in certain processors in both STATUS and DATA modes.

3.2.5 EX WRITE

This strobe transfers a word from the processor to the currently selected processor page and address in the RIM buffer. On completion of the transfer the address is incremented. Address wrap around, within the selected page, occurs after location 0377 is accessed. The RIM also supports the MOUT instruction implemented in certain processors.

3.2.6 EX COM1

EX COM1 is a general RIM command whose purpose is defined by the contents of the processor output bus as follows:

00 000 000	Clear IPE: clears Interface Parity Error status bit.
00 000 001	Disable TRANSMITTER: causes TRANSMITTER to cancel any previous uncompleted command to transmit. TA (TRANSMITTER AVAILABLE) will come true within 500 ms. to indicate acceptance of this command. (TA will be set the next time the RIM receives an INVITATION TO TRANSMIT, and failure to do so within 400 ms. would be an indication that there are no other operating RIMs in the system).
00 000 010	Disable RECEIVER: causes RECEIVER to cancel any previous uncompleted command to receive. RI (Receiver Inhibited) will come true within 400 ms. to indicate acceptance of this command. (Note that RI comes true in response to this command the next time the RIM receives an INVITATION TO TRANSMIT and that its failure to do so within 400 ms. would be an indication that there are no other operating RIM's in the system.)
00 0nn 011	Select Processor Page: sets processor buffer page to nn. All INPUT, PIN, and MIN instructions when the RIM is in DATA mode and all EX WRITE and MOUT instructions act on the buffer page selected by this command.
00 0nn 100	Enable transmit from page nn: sets transmitter buffer page to nn, clears TA (Transmitter Available), TMA (Transmitted Message Acknowledged), and TPE (Transmitter Parity Error) status bits and causes the RIM to start a transmit sequence. Status bit 0 (TA) returns true upon completion of the transmit sequence. Status bit 1 (TMA) will have been set by this time if the RIM has received an acknowledgement from the destination RIM. (Note that this is strictly a hardware level acknowledgement which is sent by the receiving RIM before its host processor is even aware that a packet has been received. Note also the acknowledgement may get lost due to line errors so that TMA not being set is not a guarantee that the packet was not received.) Status bit 3 (TPE) will have been set by this time if the transmitter read a byte with bad parity from the buffer while sending the packet, in which case the transmission was aborted without sending a CRC, insuring that the destination RIM did not receive a packet containing errors. This command should not be executed unless TA (status bit 0) is true.
00 0nn 101	Enable receive to page nn: sets receiver buffer page to nn, clears RI (Receiver Inhibited) status bit, and allows the RIM to receive. Status bit 7 (RI) will return true only when a packet addressed to the RIM, or a BROADCAST (if reception of BROADCASTs has been enabled), has been received and, except in the case of BROADCASTs, acknowledged. This command should not be executed unless RI (status bit 7) is true.
00 000 110	Clear POR: clears Power-On-Reset status bit. If either the RIM or its host processor loses its operating power this status bit is set upon resumption of power. The RIM sets the TA and RI status bits after a Power-On-Reset, but the state of the TMA, TPE, and IPE status bits and the contents of the buffer (and buffer parity) are indeterminate.
00 000 111	Clear RECON: clears system RECON status bit. This status bit (bit 2) is set whenever a system reconfiguration occurs.

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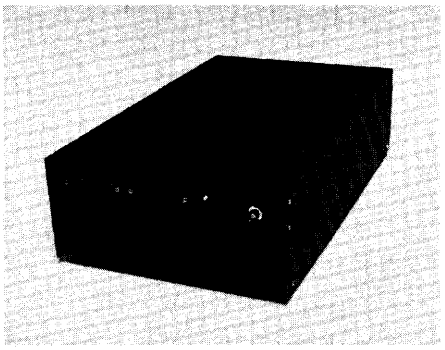

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3.2.7 EX COM4

Sets buffer address to the contents of the processor output bus and sets DATA mode in the RIM. All three page registers remain unchanged. The next EX WRITE or INPUT instruction executed will access the location in the buffer memory specified by this address and the processor page register.

3.3 RIM Operation

To transmit a message the processor selects a buffer for its use (EX COM1 with A=0N3 where N is 0, 1, 2, or 3), and writes into the buffer (EX COM4 and EX WRITE) in the following format:

ADDR	0000	XXX - Unused
ADDR	0001	DID - Destination IDentifier (000 for BROADCAST)
ADDR	0002	COUNT - 2's complement of DATA length
ADDRs	COUNT-0377	DATA - Data to be sent

The processor then waits for TA (status bit 0) to be true and gives the transmit command (EX COM1 with A=0N4). At the completion of its transmit sequence the RIM conditionally sets TMA (status bit 1) and TPE (status bit 3) and then sets TA.

If the DID is non-zero (the PACKET is not a BROADCAST) the RIM will wait for a free buffer (RI false) at the destination (without locking out other users) before sending the packet. Note that if the host processor at the destination is not servicing its RIM the RIM at the source may never find a free buffer and never set TA. There must, therefore, be a software time-out on TA. When this timer times out, the processor should disable the TRANSMITTER (EX COM1 with A=001) to force the RIM to abandon the transmission.

Note that if the disable TRANSMITTER command does not cause TA to return true within 400 ms. it is an indication that there are no other operating RIMs in the system.

To enable the receiver, the processor assigns a buffer for its own use (EX COM1 with A=0N3), sets the buffer address to 001 (EX COM4 with A=001), writes a 000 to enable reception of BROADCASTs or any non-zero byte to inhibit reception of BROADCASTs, waits for RI (status bit 7) to be true, and gives the receive command (EX COM1 with A=0N5). When a packet addressed to the local RIM or sent as a BROADCAST (if reception of BROADCASTs was enabled) is completely and correctly received the RIM sets RI. The processor selects the buffer used by the receiver (EX COM1 with A=0N3) and reads the buffer (EX COM4, and IN). The buffer contents are as follows:

ADDR	0000	SID - Source IDentifier
ADDR	0001	DID - Local ID or 000 (BROADCAST)
ADDR	0002	COUNT - 2's complement of DATA length
ADDRs	COUNT-0377	DATA - Received Data

Note that the usual range of the COUNT is 0377 (1 DATA byte) to 003 (253 DATA bytes). The COUNT may also be set to 002 or 001 in which case 253 DATA bytes will be sent (buffer locations 0003 to 0377), just as if the COUNT were 3. Thus the COUNT may be used to carry "extra" information, such as a binary sequence number, on full length packets.

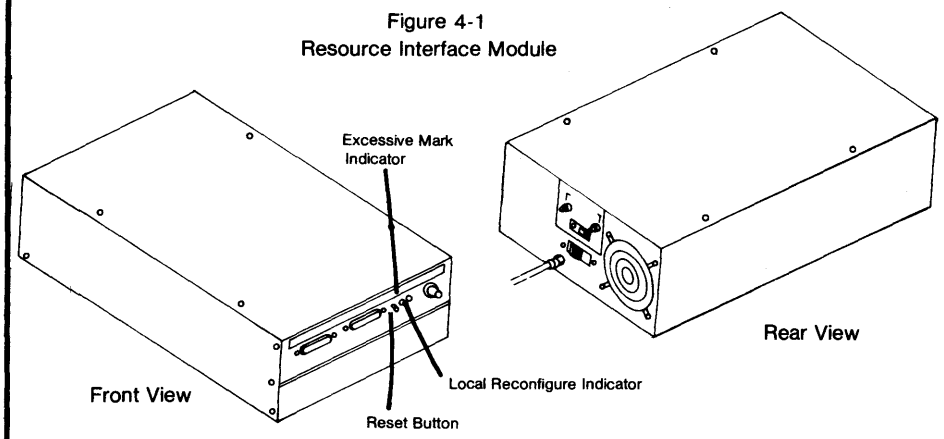
4.0 Physical Description

Figure 4-1 shows the RIM, its controls and interface connectors.

Equipment Dimensions:

Width:	10.5 in.	(26.7 cm.)
Height:	5.25 in.	(13.3 cm.)
Depth:	17.0 in.	(43.2 cm.)
Weight:	17.0 lbs.	(7.7 kg.)

Figure 4-1
Resource Interface Module



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5.0 Environmental Requirements

Temperature:
10° to 38°C (50° to 100°F) operating ambient
Humidity:
20% to 90% relative (non-condensing)
Heat Dissipation: 222 BTU/hr

WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

6.0 Interface Requirements

6.1 Input/Output Requirements

The RIM interfaces with the I/O bus through J1 (see figure 4-1). J2 has the same pin assignments as J1 so that additional external device controllers and RIMs may be connected to the processor parallel I/O bus by daisy-chaining the devices with Universal I/O Cables.

The RIM interfaces to the other RIMs in the system through BNC connector J3.

6.2 Power Requirements

The RIM contains its own power supply which may be strapped for any common-line voltage as described in section 7.1.

An ON/OFF switch and an INTERLOCK switch are provided. When the ON/OFF switch is in the ON position and the INTERLOCK switch in the ENABLE position the RIM is "slaved" to the processor and is turned on and off automatically when the processor is turned on and off. When the INTERLOCK switch is in the DEFEAT position the RIM is turned on and off by the ON/OFF switch without regard for the state of the processor.

7.0 Field Selectable Options

7.1 Power

Field alterable straps are provided to allow operation from 100, 120, 200, 220, or 240 VAC ± 10%, 47 to 63 Hz.

7.2 Address

The RIM device address may be set to any of the available addresses in the field by means of jumpers. The RIM is wired for address 0234 at the factory. Addresses 0232, 0231, 0254, 0252 and 0251 are reserved for the second, third, fourth, fifth, and sixth RIMs connected to the same processor.

7.3 ID

The RIM's unique ID may be set to any number from 1 to 0377 in the field by means of switches. NO TWO ADAPTORS IN THE SAME SYSTEM MAY HAVE THE SAME ID, NOR MAY ANY ADAPTOR HAVE IT ID=000.

Refer to the 9483 first level maintenance manual for a discussion on RIM ID number assignment.

7.4 Processor Selection

A jumper is provided to inhibit I/O parity checking for use with processors which do not generate parity on the I/O bus.

8.0 Shipping List

The following items are shipped with each RIM:

Quantity	Item
1	RIM Product Specification

NOTE: The following items should be ordered with each RIM:

Quantity	Item
2	Male BNC connectors
1	Coax cable (specify length)

NOTE: These lists are for information only; the current appropriate Datapoint shipping list prevails in all cases.

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