Honeywell

SERIES 16

H316 GENERAL PURPOSE DIGITAL COMPUTER INSTRUCTIONS AND LOGIC BLOCK DIAGRAMS

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REVISION HISTORY

New Revision Level of Manual	Change No.	Effective Date	Number and New Revision Level of Affected Drawings	Pages Affected by Revision
B	7275	Sept. 1969	70024526A 70024527A 70024528A	3-44 3-45 3-46
C	7414	Sept. 1969	70024522B	3-40
D	7227A	Oct. 1969	70024276C 70024517B 70024523B	3-2 3-35 3-41
E	7496	Oct. 1969	70024276D	3-2
F	7350A	Oct. 1969	70024276E	3-2
G	7748	Feb. 1970	70024276J 70024485B through 70024519B 70024522C 70024524B 70024525B 70024527B 70024529B	3-2 3-3 through 3-37 3-40 3-42 3-43 3-45 3-47
H	8302	May 1970	70024276M 70024486C 70024488C 70024527C	3-2 3-4 3-6 3-45
J	8654	Oct. 1970	70024503C 70024507C 70024513C 70024517D 70024518C	3-21 3-25 3-31 3-35 3-36
K	8666	Oct. 1970	70024523C	3-41
L	9086	April 1971	70024276N 70024525C	3-2 3-43
M	9365A	May 1971	70024518D 70024524D	3-36 3-44
N	9505	June 1971	70024509C 70024512C 70024517E 70024519C 70024522D 70024525D	3-27 3-30 3-35 3-37 3-41 3-45
P	9689	July 1971	-- -- -- 70030115A -- 70030116A --	iv v 1-1 3-40 3-41 3-42 3-43 through 3-49
Q	9645A	July 1971	70030115B 70030116B	3-40 3-42
R	9726	Oct. 1971	C70024276S C70024502B C70024503C C70024504B C70024511B C70024513C C70024517E	3-2 3-20 3-21 3-22 3-29 3-31 3-35
S	10228	Apr. 1972	-- C70024503E C70024504C C70024514C C70024517F C70030115B C70030116C C70024523D C70024524D -- C70032515A	iii, iv 3-21 3-22 3-32 3-35 3-39 3-40 3-41, 3-42 3-43 3-44 deleted 3-45
T	10229	Apr. 1972	C70024525E --	3-44 3-45, 3-46, 3-47, 3-48, 3-49 and 3-50 deleted
U	20049	May 1972	C70024503E	3-21
V	20593	Oct. 1972	C70024514D	3-32
W	20706	Feb. 1973	C70024276T C70024512D	3-2 3-30
X	20519	Sept. 1972	C70024276U	3-2
Y	20783	March 1973	C70024517G	3-35
Z	30014	April 1973	--	iii through vi, 1-1 through 1-5, 2-1, 2-3, 2-4, 2-5, 2-7 through 2-46, 2-59, 2-60 and 2-61 added, 3-1, 4-1 through 4-49 added
AA	30189	June 1973	C70024493C C70024519D C70030116D C70024525F	3-11 3-37 3-40 3-45
AB	30216	Nov. 1973	-- C70030116E C70024510C C70024523E	2-6, 2-11 3-40, 4-42 3-28 3-41

REVISION HISTORY (Cont)

New Revision Level of Manual	Change No.	Effective Date	Number and New Revision Level of Affected Drawings	Pages Affected by Revision
AC	40528	June 1974	C70024526B C70024527D	3-46 3-47

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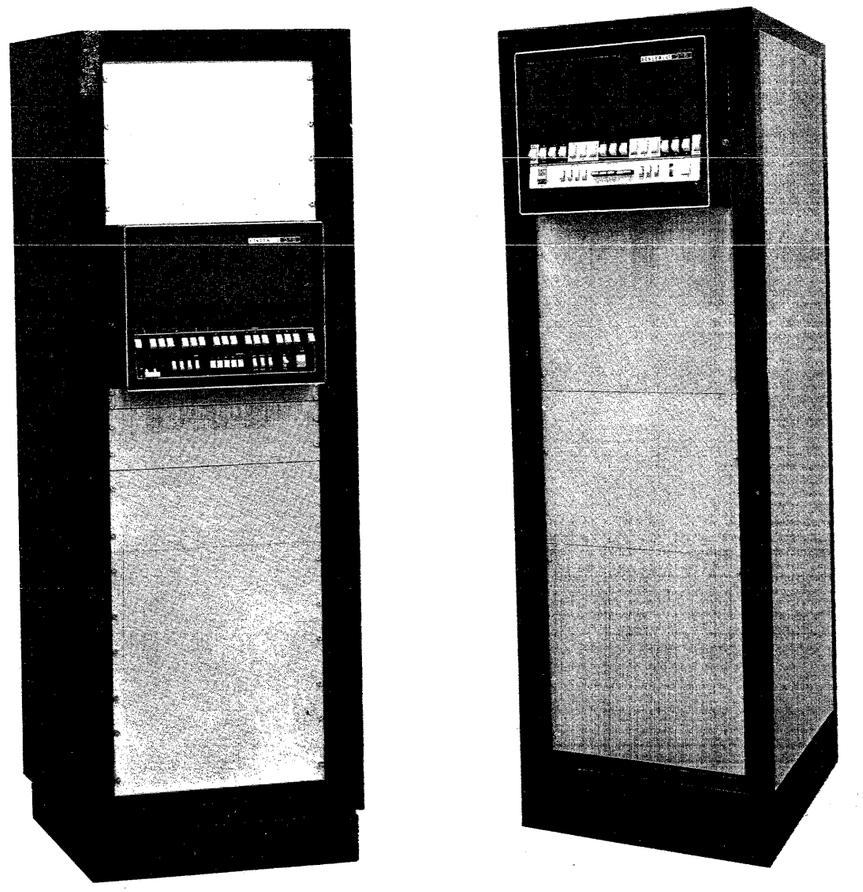


71-0035A

Type 316-01

Types 316-0100 and 316-0110

SECTION I
INTRODUCTION

This volume contains flow charts and analyses of all H316 instructions and the logic block diagrams for Types 316-01, 316-0100, and 316-0110. These types differ primarily in mechanical design and configuration. Type 316-0110 contains the improved memory module. Separate coverage is provided for the memory reference fetch cycle. The instructions are presented in groups (i.e., load and store, arithmetic, logical, etc.). For convenient reference, the mnemonic, number of cycles, and op code appear on each page. Symbols and abbreviations used in the flow charts are defined in Table 1-1. A function index is provided as an aid in determining function sources and definitions (Table 1-2).

Signal Mnemonics

The electrical characteristics of the computer circuits are called: passive (+6 vdc) and active (0 vdc). The logical functions are true (logic ONE) and false (logic ZERO). In general, there are two ways of relating the electrical characteristic and logical function for each signal mnemonic:

a. An assertion signal (for example, A01FF+) is logically true when it is at +6 vdc and is logically false when it is at 0 vdc.

b. A negation signal (for example, A01FF–) is logically true when it is at 0 vdc and is logically false when it is at +6 vdc.

A particular signal mnemonic can be labeled assertion or negation arbitrarily. The signal mnemonic convention uses the sixth character to specify assertion or negation.

TABLE 1-1.
SYMBOLS AND DEFINITIONS

Symbol	Definition
∧ or .	Logical AND
∨	Logical OR
⊻ or ⊕	Exclusive OR
→	Replaces
⇌	Is exchanged with
⟶	Is discarded
( )$_{\#}$	Contents of a hardware register
[EA]	Contents of a core location specified by the effective operand address
A	A register
ADB	Address bus
B	B register
C	Carry flip-flop (CB1TF)
E	E register
EA	Effective operand address; the address from which the operand is obtained
F	Flag (indirect address indicator) or F register
INB	Input bus
IW	Instruction word
M	M register
N	Two's complement of number of shifts to be performed
OTB	Output bus
P	P register
X	X register

TABLE 1-2.
FUNCTION INDEX

Mnemonic	LBD No. (Signal Source)	Definition
OxxPA	101–116–05	Adder input OR gates (G&H), bits 1 through 16
OCPLS	134–K11	Output control pulse
OCPRC	147–F3	Output control pulse, real-time clock
OPG00	120–F5	Op group 00
OPG3C	120–P5	Op group for three cycle instructions (JST v IRS v CAS v IMA v LDX v DOUBLE PRECISION)
OPGAA	127–G9	Op group, A-cycle utilization of A register
OPGDP	124–E9	Op group, double precision arithmetic operation (ADD v SUB v LDA v STA)
OPGJS	129–P11	Op group, jump or skip (JMP v JST v IRS v (SKIP ENABLED))
OPGMD	123–B7	Op group, multiply or divide (MPY v DIV)
OPGNS	125–A12	Op group, negative sum. Control ENSHL/ ENSLL for subtractive process (SUB v IRS v CASAM)
OPGSM	128–A12	Op group, sum to M register control (STA v IMA v LDX v STX)
OPGWR	126–G8	Op group, write/read control (STA v IMA v LDX v STX v IRS v JST)
OTBxx	138–XX	Output bus, bits 1 through 16
OTPMA	240–H6	Output transfer pulse, DMA option
IOGRP	120–P3	Op group, I/O group
IAD61	135–F2	Interrupt address 61 (RTC location 00061)
IAD63	135–F7	Interrupt address 63 (Standard interrupt location 00063)
IADX2	135–F5	Interrupt address, location 00XX1 through 00XX7
ICYEF	119–G8	I-cycle early flip-flop (Indirect address)
ICYLF	119–N8	I-cycle late flip-flop (Indirect address)
ICYS1	263–E7	I-cycle and sector zero not selected
1Gxxx	200–XX	Interrupt address greater than 063 or 067 or 077 or 107 or 117 or 127 or 137 (as applicable)
IMAOP	120–J2	IMA op code
INBxx	101–116–F4	Input bus, bits 1 through 16
INCSC	126–P5	Increment shift counter if not 00_8
INDxx	132–XX	Console indicator lamp drivers, bits 1 through 16
INHPF	135–K1	Inhibit power failure interrupt
INKOP	122–P9	INK op code
INSTR	241–L2	Input strobe, DMA option
IRSOP	120–M3	IRS op code
1YBxx	223–XX, 135–XX	Input-to-Y bus, bits 2 through 16. DMC option, and program interrupt
AxxFF	101–116–M5	A register flip-flops, bits 1 through 16
A00FF	124–P5	A00 flip-flop
A0QM1	124–L8	A00FF equals M01FF
A1QA2	126–B4	A01FF equals A02FF, normalize signal
ACKAx	241–B4	Acknowledge for DMA channels 1 through 4
ACKPF	135–F1	Acknowledge for power failure interrupt
ACKRC	135–F4	Acknowledge for real-time clock
ACTxx	244–XX	DMA address count bits 1 through 16
ACYEF	119–G5	A-cycle early flip-flop
ACYLF	119–N6	A-cycle late flip-flop
ACYNX	129–F1	A-cycle is next main frame cycle
ADBxx	138–XX	Address bus, bits 7 through 16

TABLE 1-2. (CONT)
FUNCTION INDEX

Mnemonic	LBD No. (Signal Source)	Definition
ADDOP	120–F7	ADD op code
ANAOP	120–F2	ANA (logical AND to A) op code
AZERO	126–P9	A register equals zero, bits 1 through 16
AZZZZ	125–E7	A general control flip-flop
BxxFF	101–116–M1	B register flip-flop, bits 1 through 16
BANKx	138–A12	Memory bank select A, B, C, or D
BRICY	134–A8	BREAK and i-cycle
BREAK	134–G2	BREAK flip-flop. Set by program interrupt, RTC, memory increment, or DMC operation, etc.
BRREQ	134–D1	BREAK request (sync-in to BREAK operation)
CASOP	120–M4	CAS op code (compare A and SKIP)
CASAM	126–P6	A01FF equals M01FF in CAS instruction
CBITF	124–P2	C-bit flip-flop (arithmetic overflow, etc.)
CHENx	241–B9	Channel enable for DMA option (channels 1 through 4)
CHSLx	241–D3	Channel select for DMA option (channels 1 through 4)
CLAIL	130–K11	Clear A register bit 1 (clock level)
CLAMP	141–M7	Clear A register with manual pushbutton switch
CLATL	122–G6	Clear A register, total (clock-level)
CLATR	122–K8	Clear A register, total (clock-reset)
CLBMP	141–K7	Clear B register with manual pushbutton switch
CLBTR	123–M6	Clear B register, total (clock-reset)
CLCHS	241–J5	Clear DMA channel select flip-flops (clock-reset)
CLDTR	125–K5	Clear D register to ONEs, total (clock-reset)
CLETR	125–K2	Clear E register to ONEs, total (clock-reset)
CLFTL	125–K8	Clear F register, total (clock-level)
CLLTR	241–L10	Clear L register, DMA option, total (clock-reset)
CLMMP	141–C7	Clear M register with manual pushbutton switch
CLMTR	128–P9	Clear M register, total (clock-reset)
CLPIL	134–P6	Clear program interrupt and memory increment request lines
CLPMP	141–E7	Clear P and Y registers with manual push-button switch
CLPTR	129–M10	Clear P register, total (clock-reset)
CLRDR	126–L1	Clear D register when master clock oscillator has stopped
CLRF5	134–G8	Clear bit 5 of F register on program interrupt
CLSEX	134–P8	Clear single execute (program interrupt and memory increment) request flip-flops
CLSZR	262–H9	Clear sector zero relocation
CLXTR	128–M8	Clear X register, total (clock-reset)
CLYTR	129–P3	Clear Y register, total (clock-reset)
CLZTL	241–L5	Clear Z register (DMA option) total (clock-level)
CMEXT	136-HM	Clear extended addressing mode
CMK09	122–P8	Clear mask flip-flops for OTK instruction
CMKXX	134–G10	Clear mask, I/O control pulse
COXXX	150–D2	Memory cycle initiate flip-flop
D00DJ	130–D1	Fictitious D00 bit to take care of right shift end effects
D00FF	130–K8	D00 control flip-flop, extension of D register
DxxFF	101–116–G11	D register flip-flops, bits 1 through 16

TABLE 1-2. (CONT)
FUNCTION INDEX

Mnemonic	LBD No. (Signal Source)	Definition
DOGFF	124–P9	Divide termination control flip-flop for arithmetic option
D17DJ	130–G4	Fictitious D17 bit (end effect) of left shift
DILAx	245–F8	Device interrupt line, DMA channels 1 through 4
DIQAZ	123–B3	D01FF equals AZZZZ flip-flop
DIVOP	120–J6	DIV op code
DALEN	224–	DMC address line enable
DCY2X	221–D10	DMC cycle 2
DCY3X	221–K5	DMC cycle 3
DCYXX	221–B10	DMC cycle 1, 2, and 3
DGONE	126–D9	D register equals zero, bits 1 through 16
DMAIN	259–XX	DMA input mode
DMACY	241–L7	DMA cycle
DMARQ	241–B5	DMA request
DMAWR	241–G9	DMA write/read control
DMCCY	138–B11	DMC cycle 1, 2, 3, and 4
DMCRQ	220–F6	DMC request
DMCRR	221–F2	DMC reset ready line
DMCWR	221–L2	DMC write/read control
DPOLX	124–P12	Double precision or LDX op code
DPMOD	124–B10	Double precision mode flip-flop
DRFLP	125–E10	Data ready flip-flop
DRLIN	342–	Device ready line
DSPLO	141–G4	Display operating indicators
DSPLA	141–M4	Display A register
DSPLB	141–K4	Display B register
DSPLM	141–C4	Display M register
DSPLX	141–K7	Display X register
DSPLY	141–E4	Display Y register
ExxFF	101–116–P2	E register flip-flops, bits 1 through 16
EOINS	119–G2	End of instruction
EOADJ	130–E10	Fictitious E register bit for shift end effect
EOBDJ	130–H1	Fictitious E register bit for shift end effect
EOCDJ	130–D8	Fictitious E register bit for shift end effect
EODDJ	130–D11	Fictitious E register bit for shift end effect
EOY16	124–L9	Enable zero to Y-register, bit 16
EICHL	125–H10	Enable ONE to shift counter bit 11 (clock-level)
EICTS	125–K9	Enable ONEs to shift counter, total (clock-set)
EIDTS	125–P6	Enable input bus to D register, bits 1 through 16 (clock-set)
EIK17	127–P5	Enable 1 carry-in from fictitious bit 17 (end inject carry)
EIYHS	129–P6	Enable IYB, bits 2 through 9, to Y register (clock-set)
EIYLS	129–P5	Enable IYB, bits 10 through 16, to Y register (clock-set)
E40SC	121–C2	Enable 40 (octal) to shift counter. Setup for NRM instruction
E57SC	124–J3	Enable 57 (octal) to shift counter. Setup for DIV instruction
E70SC	124–H3	Enable 70 (octal) to shift counter. Setup for MPY instruction
EASTL	127–P1	Enable A register to sum network, bits 1 through 16 (clock-level)
EBETS	125–M1	Enable B register to E register, bits 1 through 16 (clock-set)
ECETS	125–M3	Enable shift counter to E register, bits 11 through 16 (clock-set)

TABLE 1-2. (CONT)
FUNCTION INDEX

Mnemonic	LBD No. (Signal Source)	Definition
EDAIL	130–K10	Enable D register to A register, bit 1 (clock-level)
EDAHS	122–P1	Enable D register to A register, bits 1 through 8 (clock-set)
EDALS	122–P3	Enable D register to A register, bits 9 through 16 (clock-set)
EDBTS	123–P2	Enable D register to B register, bits 1 through 16 (clock-set)
EDMxx	101–116–K8	Enable D register to M register, bits 1 through 16 (DJs with ESM – gates).
EDMAY	241–L3	Enable DMA bus (address count or Z register) to Y register, bits 1 through 16 (clock-set)
EDMTS	128–K12	Enable D register to M register, bits 1 through 16 (clock-set)
EDPTR	129–J9	Enable D register to P register (clock-level)
EDPTS	129–P9	Enable D register to P register, bits 1 through 16 (clock-set)
EDYTS	129–P1	Enable D register to Y register, bits 1 through 16 (clock-set)
EEALS	122–K5	Enable E register to A register, bits 11 through 16 (clock-set)
EEATS	122–P4	Enable E register to A register, bits 1 through 10 (clock-set)
EMCxx	121–X11	Enable M register to shift counter, bits 11 through 16, respectively.
EMCTL	125–P12	Enable M register to shift counter, bits 11 through 16 (clock-level)
EMFTL	128–P4	Enable M register to F register, bits 3 through 6 (clock-level)
EMSHL	127–P9	Enable M register to sum network, bits 1 through 7 (clock-level)
EMSLL	127–P11	Enable M register to sum network, bits 8 through 16 (clock-level)
EMXTS	128–P7	Enable M register to X register, bits 1 through 16 (clock-set)
ENSHL	127–P8	Enable M register (negation) to sum network, bits 1 through 7 (clock-level)
ENSKI	150–K2,3	Selection Sink Enable Pulse
ENSLL	127–P7	Enable M register (negation) to sum network, bits 8 through 16 (clock-level)
ENTRA	141–M2	Enter A register (manual console op)
ENTRB	141–K2	Enter B register (manual console op)
ENTRM	141–B2	Enter M register (manual console op)
ENTRP	141–E2	Enter P register (manual console op)
ENYSW	150–K4,5	Digit Selection Switch Enable Pulse
EPARB	133-D3	Memory parity error strobe
EPSLL	128–K4	Enable P register to sum network, bits 3 through 16 and enable M register bits 1 and 2 to sum network (clock-level)
EPYTS	129–P4	Enable P register to Y register, bits 1 through 16 (clock-set)
ERAOP	120–P1	ERA op code (exclusive OR to A)
ERLAX	259–XX	End of range for DMA
ERLXX	222–L11	End of range line for DMC
ESDTS	125–M4	Enable adder sum to D register, bits 1 through 16 (clock-set)
ESMTS	128–G11	Enable sum network input to M register, bits 1 through 16 (clock-set)

TABLE 1-2. (CONT)
FUNCTION INDEX

Mnemonic	LBD No. (Signal Source)	Definition
ETAHS	122—P6	Enable transposed D register, bits 9 through 16 into A register, bits 1 through 8 (clock-set)
ETALS	122—P7	Enable transposed D register, bits 1 through 8 into A register, bits 9 through 16 (clock-set)
EXSTL	128—P5	Enable X register to sum network, bits 1 through 16 (clock-level)
EXTMD	136—H1	Extended addressing mode flip-flop
EYSHL	128—P3	Enable Y register to sum network, bits 1 through 7 (clock-level)
EYSLL	128—P2	Enable Y register to sum network, bits 8 through 16 (clock-level)
EYZTL	241—L6	Enable Y register to Z register, bits 1 through 16 (clock-level)
EZYTL	241—J7	Enable Z register to Y register via ACT − + − lines, bits 1 through 16 (clock-level)
FOICY	119—A8	F or I cycle control flip-flops are set
F0xFF	120—CX	Function register, bits 3 through 6
FCX00	134—D12	Function control indicating address bus lines 08, 09, 10, and 14 are all zero
FCYEF	119—G10	F-cycle early flip-flop
FCYLF	119—N10	F-cycle late flip-flop
FCYM2	136—F4	F-cycle/M02FF (tag store flip-flop for extended addressing mode)
FCYSO	127—G10	F-cycle sector zero specified in memory reference instruction addressing
GxxDJ	101—116—C5	Adder network input (A v X), bits 1 through 16, respectively
GENOA	120—P11	Generic operation, class A
GENOB	120—P9	Generic operation, class B
GENOP	120—J11	Generic operation
HxxDJ	101—116—C9	Adder network input (M v P v Y v M −), bits 1 through 16, respectively
HOLDM	128—M9	Hold M register contents (inhibit CLMTR−)
JAMKN	127—G4	Jam carry network (suppress carries)
JMPOP	120—M1	JMP op code
JSTOP	120—M2	JST op code
LDAOP	120—F3	LDA op code
LMPRN	132—C3	Lamp, run indicator
LMRxx	153—161—E5, 11	Selection Switch Discharge Resistor Line
LSXOP	120—P2	Load/store X register op code
LXACY	263—D9	Load X register/A-cycle
MxxFF	101—116—M8	M register, bits 1 through 16
M01ML	262—K7	M01 control from memory lockout
M02DJ	136—H5	M02 DJ gates for extended addressing
M17FF	133—K10	Parity bit flip-flop of memory parity option
M5G4G	123—G2	Minterm control in DP and IAB instructions
MACYL	128—D2	Multiply control in A-cycle

TABLE 1-2. (CONT)
FUNCTION INDEX

Mnemonic	LBD No. (Signal Source)	Definition
MADFF	124—P7	Multiply and divide control flip-flop
MASTO	141—G9	Memory access, store mode
MBSYL	150—B2	End of Memory Busy pulse
MCRST	118—G2	Master clock, reset phase
MCSET	118—K3	Master clock, set phase
MCTLG	118—P2	Master clock, timing level generator phase
MDA2A	123—D3	MPY/DIV option, A-cycle, TL2, control minterm A
MDA2C	123—G10	MPY/DIV option, A-cycle, TL2, control minterm C
MDG2E	123—D2	MPY/DIV option, timing level 2, control minterm E
MDG4D	123—G7	MPY/DIV option, timing level 4, control minterm D
MD01X to MD17X	153 to 161 C4, 5	Memory data output signals
MDSLA	122—E8	MPY/DIV option, shift left A register
MDSRA	123—G8	MPY/DIV option, shift right A register
MELOV	262—K3	Memory lockout violation flip-flop
MEMAC	141—H8	Memory access mode control
MEMCI	126—K12	Memory cycle initiate
MFG2E	122—D12	Main frame, general cycle, TL2, minterm E
MMxxx	142—XX	Memory to M register data bits 1 through 16, from memory bank A through D and combinations
MPAFF	133-J3	Memory parity mask flip-flop
MPEFF	133—J7	Memory parity error flip-flop
MPYOP	120—F5	MPY op code
MSTCL	141—C11	Master clear (overall initialization)
NxxPA	101—116—D9	Adder network input AND gates (G ∧ H), bits 1 through 16, respectively
NOSTO	262—D3	No store. Protected memory area is being accessed.
NRMOP	128—D1	NRM op code
PxxFF	101—116—M11	P register flip-flops, bits 1 through 16
P02BS	136—D5	P02 storage flip-flop for bank control extended addressing
PIL00	133—L6	Program interrupt line 00 (standard)
PIREQ	143—XX	Program interrupt request
PISEX	134—B1	Program interrupt or single execute request
PAGEO	133-A2	Parity generator output
PAMEO	133-A3	Parity memory bit output
PARCK	143—B4	Parity check indicator from I/O
PERMI	134—G4	Permit interrupt flip-flop
PFINT	135—H11	Power failure interrupt signal
PFHLT	141—K8	Power failure halt mode control
PMIND	136—K1	Previous mode indicator flip-flop for extended-addressing mode
PROTx	264—XX	Accessing protected sector 0 through 3 00—07 or 40—47 10—17 or 50—57 20—27 or 60—67 30—37 or 70—77
RxxPA	101—116—D7	Adder network or gates (G v H−), bits 1 through 16, respectively
READY	141—L10	Prestart signal from console pushbutton switch

TABLE 1-2. (CONT)
FUNCTION INDEX

Mnemonic	LBD No. (Signal Source)	Definition
REMOK	123—B2	Remainder OK to terminate divide
RESTR	262—F5	Restricted mode flip-flop for memory lockout option
RPTT2	126—G5	Repeat TL2 timing level
RRCXX	126—P8	Read-regenerate cycle control to memory
RRLIN	134—M10	Reset ready line signal to I/O device
RSKA1	150—E2	Selection sink read command timing pulse
RTCAD	147—F9	Real-time clock address decoder
RTCLK	147—H2	Real-time clock service request
RUNFF	126—M3	RUN control flip-flop
RUNMD	141—E11	RUN mode console switch control
SxxCx	117—XX	Sum network outputs from carry gating, bits 1 through 16, respectively
SCxxF	121—X7	Shift counter flip-flops, bits 11 through 16
SCQ70	121—M2	Shift counter equals octal 70
SCQ77	121—M3	Shift counter equals octal 77
SCZR0	121—M4	Shift counter equals zero
SCZR1	121—P3	Shift counter equals zero or minus one (77)
SDARS	123—P10	Shift (double) A register, right shift (clock-set)
SDBRS	123—P9	Shift (double) B register, right shift (clock-set)
SDBxx	130—AXX	End effects for SDBRS to B register, bits 1 and 2
SDRxx	140—X7	Set data register, bits 1 through 16, from console pushbutton switches
SECxx	272-xx	Sector (00-77) is unprotected in memory lockout option
SENSx	140—X10	Sense switches on console, 1 through 4, respectively
SETAO	125—C10	Set A00FF control signal
SETAZ	125—M7	Set AZZZZ control signal
SETF5	134—G7	Set bit 5 of register for memory increment
SEX00	135—D10	Standard interrupt priority network flip-flop
SEXLV	135—D7	Memory lockout violation interrupt priority network flip-flop
SEXPF	135—D1	Power failure interrupt priority network flip-flop
SEXRC	135—D4	Real-time clock service request priority network flip-flop
SEXRQ	200-XX	Single execute memory increment request
SEXTF	136-G2	Extended addressing mode flip-flop
SHAOP	120-P8	Shift A register op code
SHASC	120—P7	Shift A register and shift counter do not equal zero
SKGRP	120—P6	Skip group op code
SLATS	122—P11	Shift left to A register (clock-set)
SLBTS	123—P4	Shift left to B register (clock-set)
SMK01	134—K12	Set mask group No. 1 (standard devices)
SMK09	122—M10	Set mask group No. 9 (OTK instruction)
SMKXX	134—D9	Set mask general output strobe
SMPIL	135—H2	Sample program interrupt lines
SPMOD	135—M1	Single pulse mode control (service jumper)
SRATS	122—P12	Shift right to A register (clock-set)
SRBTS	123—P8	Shift right to B register (clock-set)
SRSTL	128—K1	Shift right from A register to sum network (clock-level)
STAOP	120—F9	STA op code
START	141—L9	Start pushbutton switch release
STEPP	141—G10	Step P register in MEMAC mode
STEXT	136—H9	Set extended addressing mode
SUBOP	120—F6	SUP op code
SW01 to SW17	(Core stack)	Sense amplifier core stack sense winding inputs

TABLE 1-2. (CONT)
FUNCTION INDEX

Mnemonic	LBD No. (Signal Source)	Definition
TL13F	118—D5	Timing level mid-TL1 through mid-TL3
TL1FF	118—K11	Timing level TL1
TL23F	118—D8	Timing level mid-TL2 through mid-TL3
TL24F	118—D10	Timing level mid-TL2 through mid-TL4
TL2FF	118—K9	Timing level TL2
TL3FF	118—K7	Timing level TL3
TL4FF	118—K5	Timing level TL4
TLATE	118—A8	Timing level, late, TL2 and TL3 inclusive
VAC00	148—E9	0 vac, transformer center tap
VAC03	148—E9	3 vac, PFI transformer
VDC06		-6 vdc
WRINH	126—G10	Write inhibit
YxxFF	101—116—P11	Y register flip-flops, bits 1 through 16
Y04XX to Y16XX	104—116—L10	Double rail memory address signals

SECTION II
FLOW CHARTS/INSTRUCTION ANALYSES

The instruction analyses are detailed presentations of some key signals generated within the Central Processor unit (CPU) from the time an instruction operation code is recognized until the execution is complete and the next instruction's fetch cycle is initiated. The instruction fetch cycle and I-cycle are covered on pages 2–2 and 2–3. Included in an analysis are the source, destination, and operational description of the signal. The location of the logic making up the signal is also given. Within each instruction class, the definitions of Instruction Analyses are presented in alphabetical order of their mnemonic code as follows:

CODE	INSTRUCTION
Generic	
ACA	Add C to A
AOA	Add ONE to A
CAL	Clear Left Half
CAR	Clear Right Half
CHS	Complement A Sign
CMA	Complement A
CRA	Clear A register
CSA	Copy Sign and Set Sign Plus
ENB	Enable Program Interrupt
HLT	Halt
IAB	Interchange A and B
ICA	Interchange Halves
ICL	Interchange and Clear Left Half
ICR	Interchange and Clear Right Half
INH	Inhibit Program Interrupt
INK	Input Keys
NOP	No Operation
OTK	Output Keys
RCB	Reset C to ZERO
SCB	Set C to ONE
S–	(Skip Group)
SSM	Set Sign Minus
SSP	Set Sign Plus
TCA	Two's Complement A
Input-Output	
INA	Input to A
OCP	Output Control Pulse
OTA	Output from A
SMK	Set Mask
SKS	Skip if Sense Line Set

CODE	INSTRUCTION
Memory Reference	
ADD	Add
ANA	Logical AND
CAS	Compare
ERA	Exclusive OR
IMA	Interchange memory and A
IRS	Increment, Replace, and Skip
JMP	Unconditional Jump
JST	Jump and Store Location
LDA	Load A
LDX	Load Index Register
STA	Store A
STX	Store Index Register
SUB	Subtract
Extended Addressing	
EXA	Enable Extended Addressing
DXA	Disable Extended Addressing
Memory Parity	
RMP	Reset Memory Parity
Shift	
ALR	Logical Left Rotate
ALS	Arithmetic Left Shift
ARR	Logical Right Rotate
ARS	Arithmetic Right Shift
LGL	Logical Left Shift
LGR	Logical Right Shift
LLL	Long Left Logical Shift
LLR	Long Left Rotate
LLS	Long Arithmetic Left Shift
LRL	Long Right Logical Shift
LRR	Long Right Rotate
LRS	Long Arithmetic Right Shift

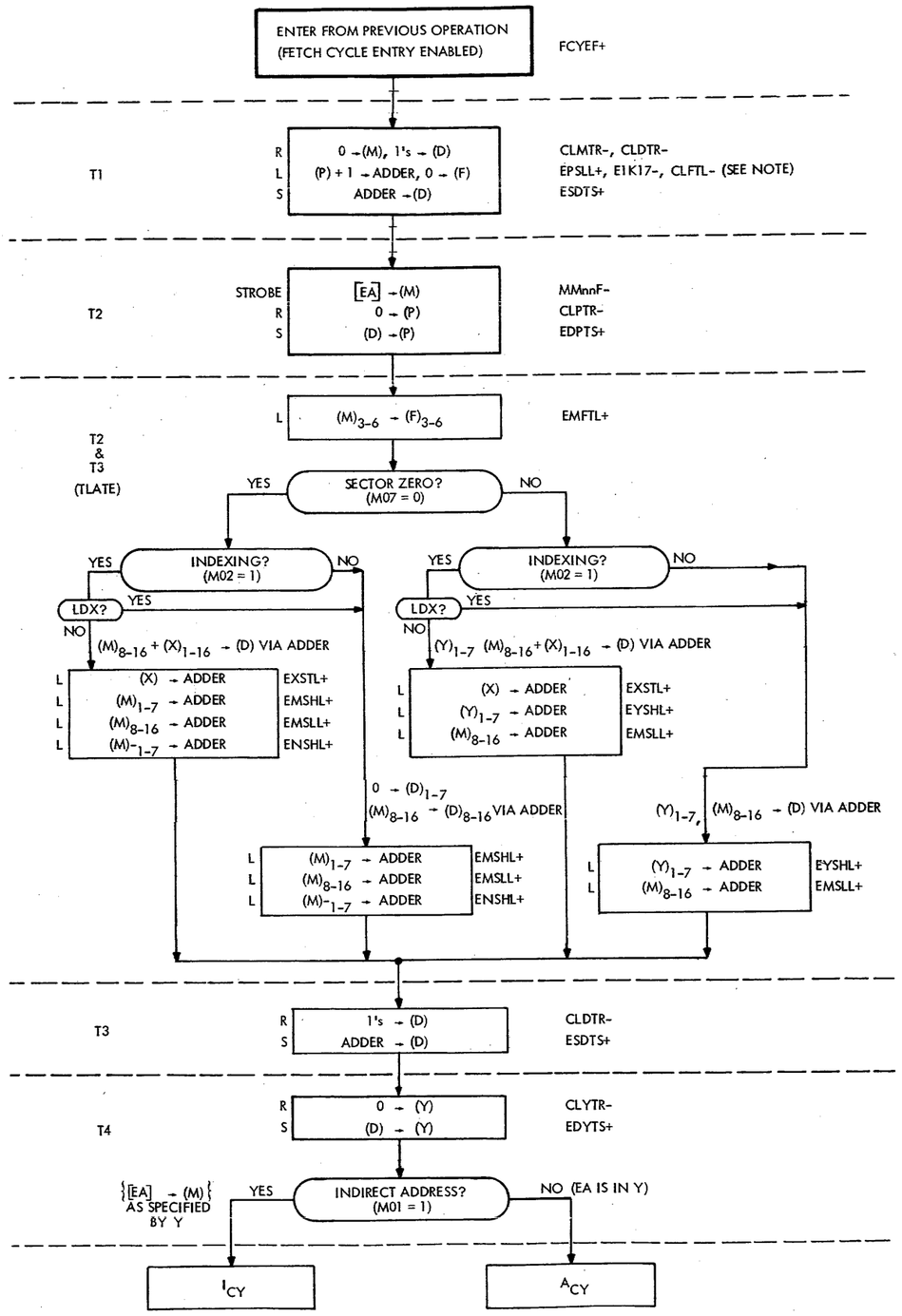
The flow charts summarize the sequence of events that occur within the CPU during the execution of each instruction. The flow charts are easy to use if the reader applies the following general analysis.

With reference to the Clear A (CRA) flow chart, note that to the left of each box is an alphanumeric (such as T1) and columns of letter codes (such as R, L, S). The alphanumeric is the time during which operations within the horizontal dashed lines occur. The letter codes specify whether the functions in the same horizontal plane are levels (L), controlled by the reset clock MCRST (R), or controlled by the set clock MCSET (S).

The information within a box is in abbreviated text form, that is to say that certain key phrases have been replaced with symbology. An example is 0 → (M), which means that the contents of the M register is replaced with zeros (cleared). Another method of clearing registers used in the H316 is 1's → (D). Rather than replacing the contents of the D register with zeros, the contents are replaced with 1's. This method only applies to the D, E, and X registers. All other registers are cleared to all zeros.

The mnemonics to the right of the box are the signals that implement the operation described in the box. In the case of 0 → (M), it is clear M register totally on reset clock (CLMTR–) which causes the register to be cleared.

In some cases, mnemonics are deliberately omitted from the flow chart for simplicity. In these cases, reference to the analyses of instructions is required.



NOTE: MISSING SIGNALS CAN BE FOUND IN F-CYCLE ANALYSIS

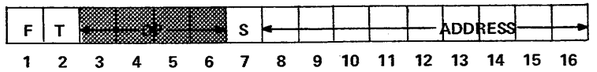
MEMORY REFERENCE F-CYCLE (EXCLUDING JMP)

Memory Reference F-Cycle (excluding JMP)

Instruction:

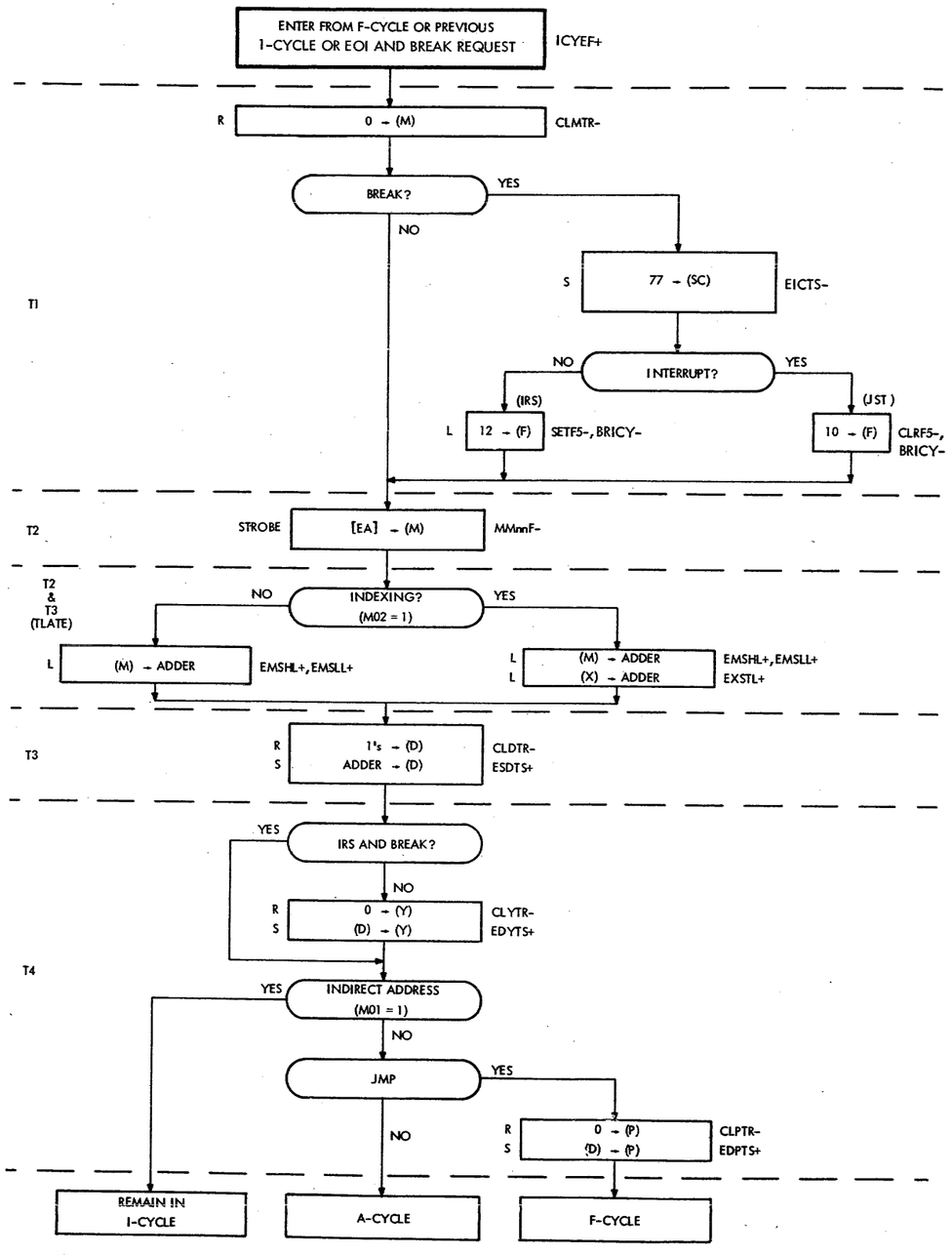
Op Code: **Type:**

Description:



Execution Time (μs):

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE+)	127–K6	116–F7/F9 117–A1	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+) (MCRST+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125-K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8 124–N6 124–N8	Clear F register Clear shift counter Clear AZZZZ FF Clear MAD FF Clear D0G FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+) (MCSET+)	125–A5	101–116–F5-F9	Enable adder sum to D register
CLSEX+	134–P8	F	TL1	L	(TL1FF+)(ICYEF–)	134–L8	135–G8	Clear single execute FF
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(EDPTR+)(MCRST+)	129–L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(EDPTR+)(MCSET+)	129–L9	101–116–J11	Enable D register into P register
EMFTL+	128–P4	F	TLATE	L	(M07FF–)(MEMAC–)(FCYLF+) (TLATE+)(GENOP–) or (M07FF+)(MEMAC–)(FCYLF+) (TLATE+)(GENOP–)	127–F10 128–K3	120–A2 136–B4 136–D3	Enable M(3-6) into F(3-6) Bank switching control
EMFTL–	128–K3	F	TLATE	L	See EMFTL+	128–J3	127–L9	Generate EMSLL+
EXSTL+	128–P5	F	TLATE	L	(FOICY+)(TLATE+)(M02FF+) (GENOP–)(MEMAC–) (M03FF+ or M04FF+ or M05FF– or M06FF+)	128–K6	101–116–A5	Enable X register to adder
EMSHL+	127–P9	F	TLATE	L	(M07FF–)(MEMAC–)(FCYLF+) (TLATE+)(GENOP–)	127–F10	101–107–A9	Enable M(1-7) to adder
EMSLL+	127–P11	F	TLATE	L	(EMFTL–)	128–K3	108–116–A9	Enable M(8-16) to adder
ENSHL+	127–P8	F	TLATE	L	(M07FF–)(MEMAC–)(FCYLF+) (TLATE+)(GENOP–)	127–F9	101–107–A10	Enable M–(1-7) to adder
EYSHL+	128–P3	F	TLATE	L	(FCYLF+)(TLATE+)(GENOP+) (MEMAC–)(M07FF+)	128–J3	101–107–A12	Enable Y register (1-7) to adder
CLDTR–	125–K5	F	TL3	R	(ANAOP–)(TL3FF+)(MCRST+) or (ACYLF–)(TL3FF+)(MCRST+)	125–B7 125–B6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(IOGRP–)(TL3FF+)	125–B5/H5	101–116–F5-F9	Enable adder sum to D register
CLYTR–	129–P3	F	TL4	R	(ACYLF–)(TL4FF+) (MCRST+)	129–E1, H3,N3	101–116–N12	Clear Y register
EDYTS+	129–P1	F	TL4	S	(ACYNX–)(MCSET+)(TL4FF+) (BRREQ–)(PISEX+)	129–M1	101–116–J10	Enable D register into Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+) (IGACY+) (SPMOD–)	126–F12	150–A2	Enable start memory



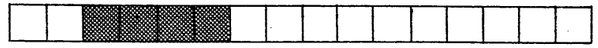
STANDARD I-CYCLE

Standard I-Cycle With Breaks

Instruction:

OP Code: **Type:**

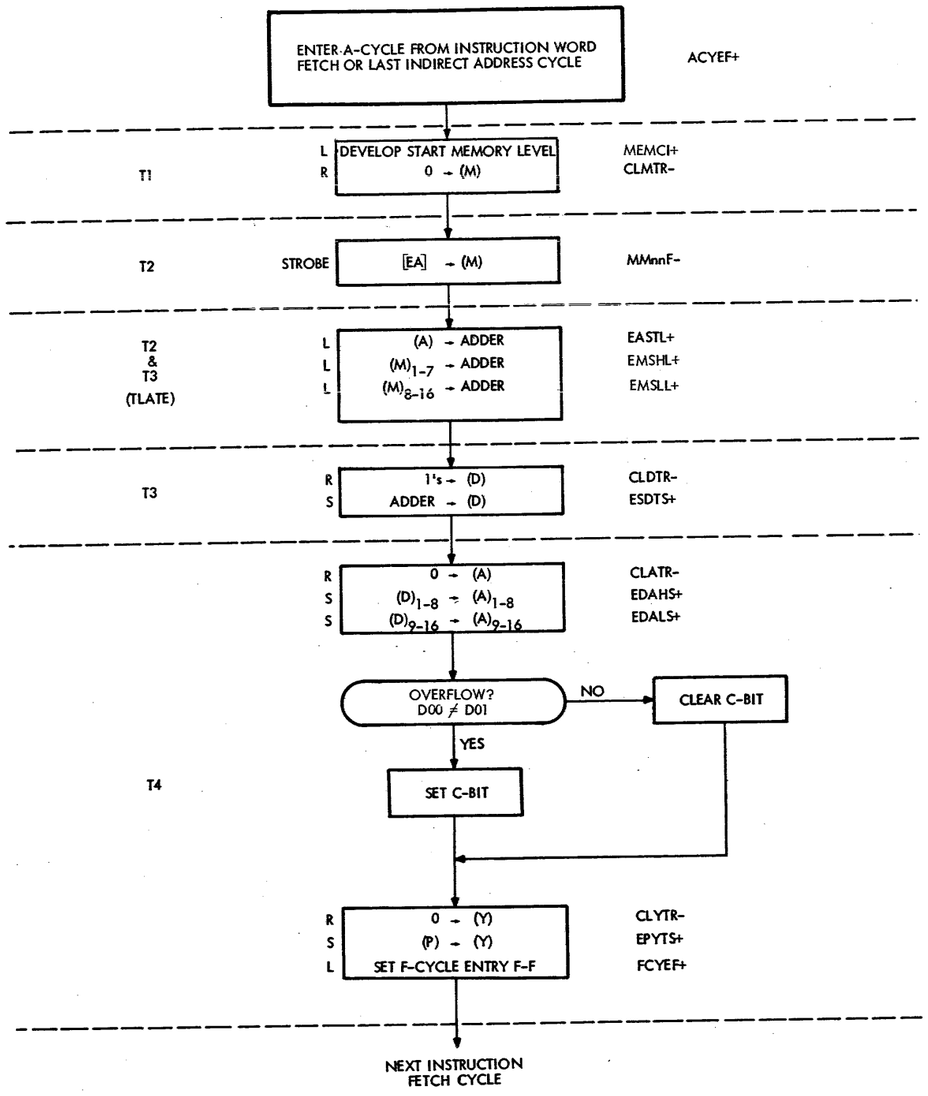
Description:



Execution Time (μs):

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EMSHL+	127–P9				(ICYEF–)	127–N11	101–107–A9	Enable M(1-7) to adder
EMSLL+	127–P11				(ICYEF–)	127–N10	108–116–A9	Enable M(8-16) to adder
EIK17–	127–P5	I	TLATE	L	(TLATE–)	127–K6	116–F7/F9	Force carry to adder
CLRF5+	134–G8	I	TL1	L	[(SEXRQ–) V(IG063–)] Λ [(IAD61–)(BREAK+) (ICYEF+)(TL1FF+)]	134–A7/ C8	134–F4 120–C3	Reset PERMI FF Clear F register bit 5
SETF5–	134–G7	I	TL1	L	[(SEXRQ+)(IG063+)V (IAD61–)] Λ [(BREAK+) (ICYEF+)(TL1FF+)]	134–C8, F7,A7	120–C5	Set F register bit 5
BRICY–	134–A8	I	TL1	L	(BREAK+)(ICYEF+)(TL1FF+)	134–A8	120–B1–B9	Force F register to JSTOP– or IRSOP– depending on F05
CLMTR–	128–P9	I	TL1	R	(MCRST+)(ACYEF–)(TL1FF+)	128–N9	101–116–L9	Clear M register
EICTS–	125–K9	I	TL1	S	(BRICY+)(MCSET+)(AZZZZ–)	125–H9	126–F5	Generate RPTT2+ (Don't care)
							126–F10	Set WRINH FF
							121–A8	Set shift counter to 77_8
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
EXSTL+	128–P5	I	TLATE	L	(ICYLF+)(F01CY+)(TLATE+) (M02FF+)(GENOP–)(MEMAC–)	128–J6	101–116–A5	Enable X register to adder
CLDTR–	125–K5	I	TL3	R	(ACYLF–)(TL3FF+)(MCRST+)	125–B6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	I	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5	101–116–F5-F9	Enable adder sum to D register
CLPTR	129–M10	I	TL4	R	(OPGJS+)(EOINS+)(TL4FF+) (MCRST+)	129–E8	101–116–L12	Clear P register
CLYTR–	129–P3	I	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	129–G1/ H1	101–116–N12	Clear Y register*
EDPTS+	129–P9	I	TL4	S	(OPGJS+)(EOINS+)(TL4FF+) (MCSET+)	129–E8	101–116–J11	Enable D register into P register
EDYTS+	129–P1	I	TL4	S	[(MCSET+)(TL4FF+) (ACYNX–)] Λ [(BRREQ–)V (DCYXX–)(EOINS–)]	129–L1/ D5	101–116–J10	Enable D register into Y register
EIYLS+	129–P5	I	TL4	S	(TL4FF+)(BRREQ+) Λ [(DCYXX–)(EOINS–)]–Λ (MCSET+)	129–D5/ F5	110–116–N12	Enable 1YB(10-16) into Y(10-16)
MEMCI+	126–K12	I	TL1	L	(IGACY+)(SPMOD–)(TL1FF+)	126–F11	150–A2	Enable memory cycle

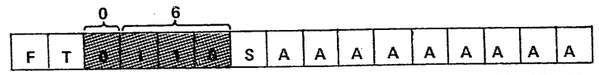
*Y register changed except when [(FOICY+)(BREAK+)(BREAK+)(IRSOP+)] is TRUE



Instruction: Add (ADD)

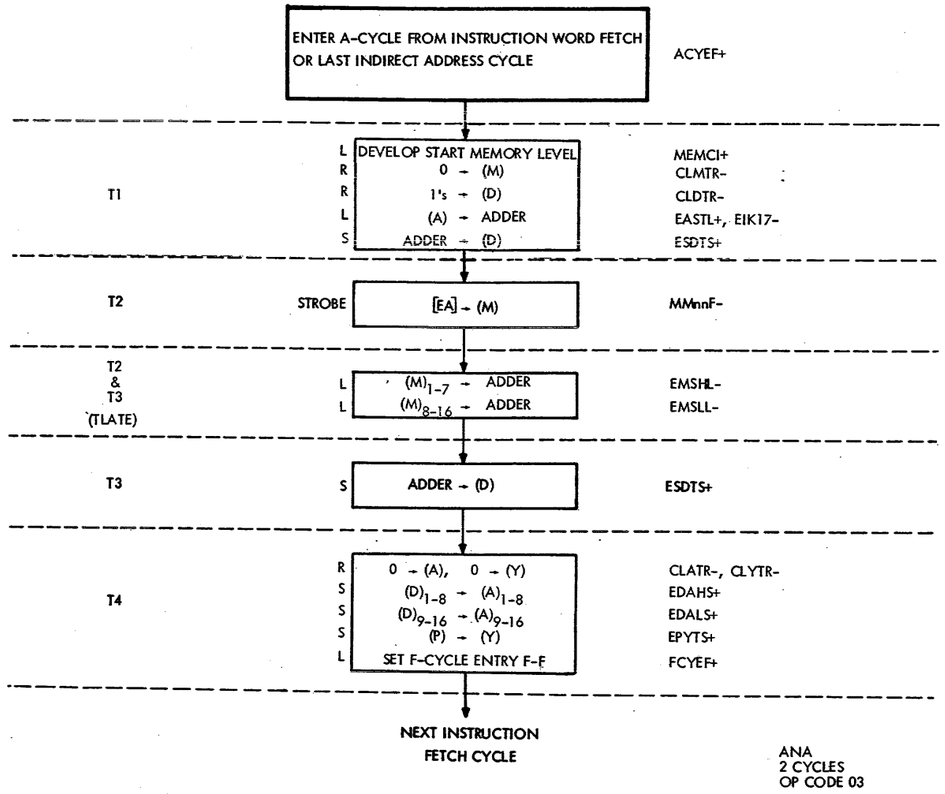
OP Code: 06 **Type:** MR, 2 cycles

Description: (A) + [EA] → A
OVF → (C)



Execution Time (μs): 3.2

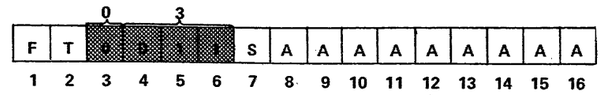
Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
CLMTR-	128–P9 •	A	TL1	R	(MCRST+)(HOLDM-)(TL1FF+)	128–K8	101–116–L9	Clear M register
MMnnF-	142				(SWnn±)(STRB-)	80.04	101–116–A4	Memory data set into M register
EASTL+	127–P1	A	TLATE	L	(ADDOP+)(ACYLF+) (TLATE+)	127–A1/ C1	101–116–A4	Enable A register to adder
EMSHL+	127–P9	A	TLATE	L	(ACYLF+)(TLATE+)(SUBOP-) (OPGAA+)	127–K9	101–107–A9	Enable M register (1-7) to adder
EMSLL+	127–P11	A	TLATE	L	(ACYLF+)(TLATE+)(SUBOP-) (OPGAA+)	127–K9	108–116–A9	Enable M(8-16) to adder
CLDTR-	125–K5	A	TL3	R	(ANAOP-)(TL3FF+)	125–B7	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	A	TL3	S	(IOGRP-)(TL3FF+)	125–B5	101–116–F5-F9	Enable adder sum to D register
CLATR-	122–K8	A	TL4	R	(ACYLF+)(OPGAA+)(TL4FF+)	122–C2	101–116–L6	Clear A register
EDAHS+	122–P1	A	TL4	S	(ACYLF+)(OPGAA+)(TL4FF+)	122–C2	101–108–J7	Enable D register to A(1-8)
EDALS+	122–P3	A	TL4	S	(ACYLF+)(OPGAA+)(TL4FF+)	122–C2	109–116–J7	Enable D register to A(9-16)
CB1TF+	124–P2	A	TL4	S	(ADDOP+)(D00≠D01)	124–A3	124–P2	Set CB1TF
CB1TF-	124–P1	A	TL4	R	(ADDOP+)(DIVOP-)(TL4FF+) (MCRST)	124–A1	124–L1	Reset CB1TF
CLYTR-	129–P3	A	TL4	R	(SCZRO+)(TL4FF+)(MCRST+)	129–E1/ H3	101–116–N12	Clear Y register
EPYTS+	129–P4	A	TL4	S	(PISEX-)(EOINS+)(OPGJS-)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	A	TL1	L	(TL1FF+)(SPMOD-)(IGACY+)	126–F12 J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX-)	150–A2	150–D2	Start memory cycle



Instruction: Logical AND (ANA)

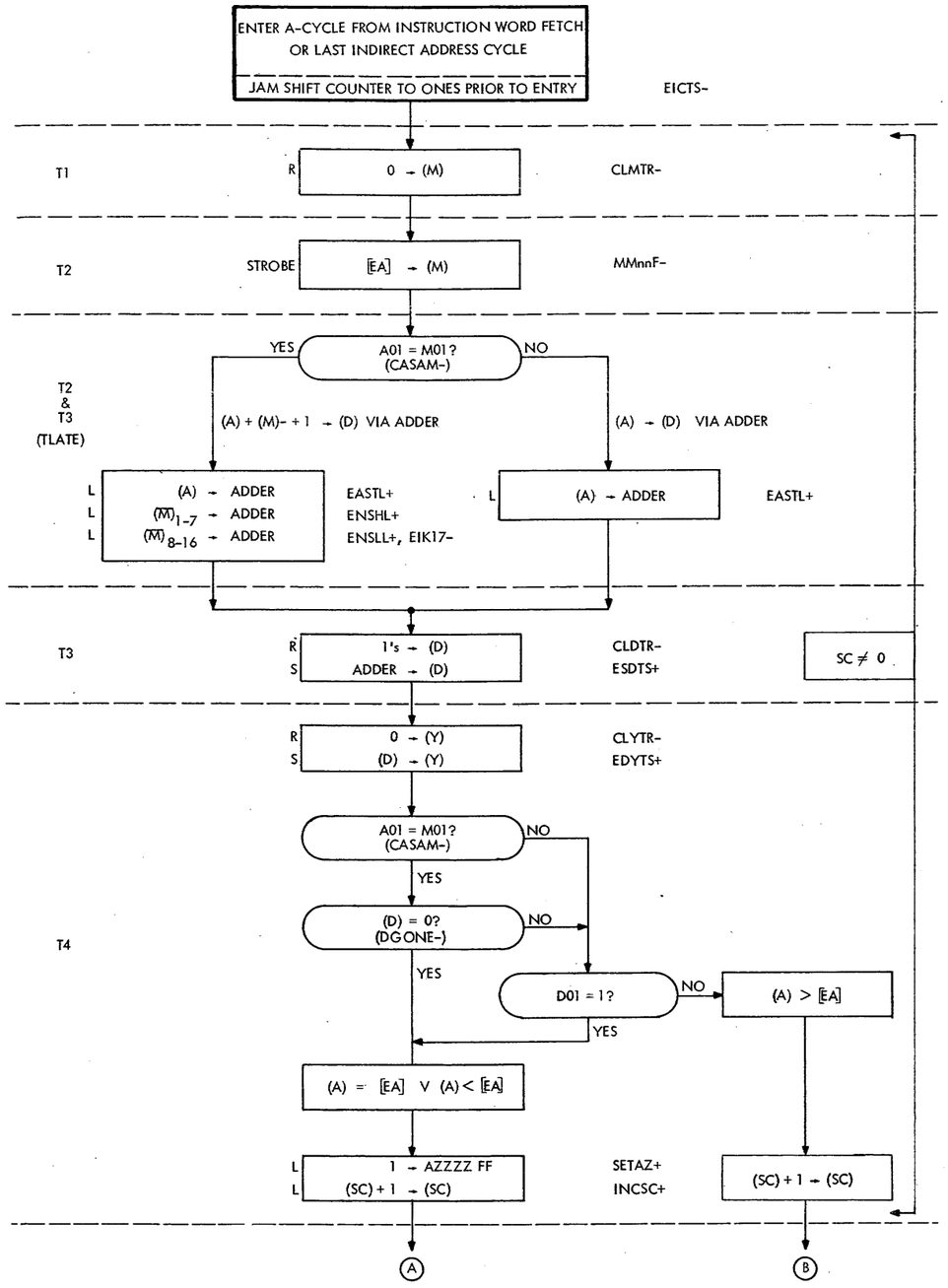
OP Code: 03 **Type:** MR, 2 cycles

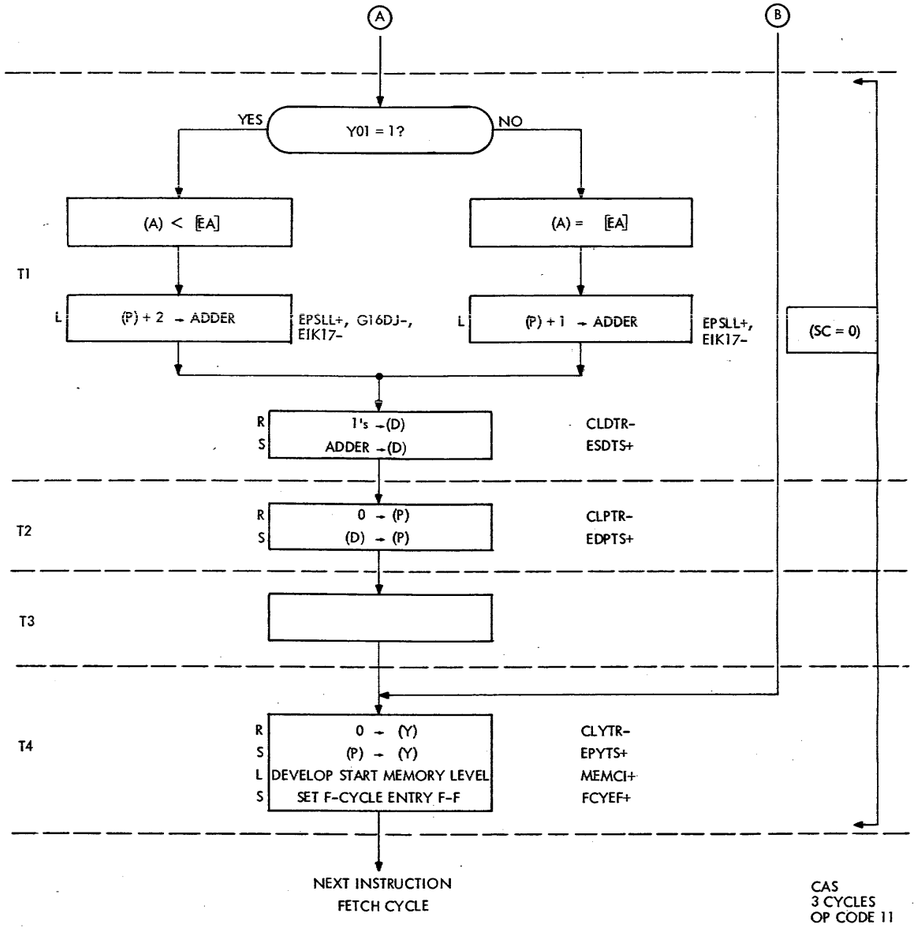
Description: (A) ∧ [EA] → (A)



Execution Time (μs): 3.2

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EIK17+	127–P5	A	TL1	L	(TLATE–)	127–K6	116–F7/F9	Force carry-in to bit 16
CLMTR–	128–P9	A	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–N9	101–116–L9	Clear M register
CLDTR–	125–K5	A	TL1	R	(ACYEF+)(TL1FF+)(JSTOP–)(IRSOP–)(IMAOP–)	125–B4	101–116–F11	Clear D register to ONEs
EASTL+	127–P1	A	TL1	L	(ACYEF+)(TLATE–)(CASOP–)(LSXOP–)(IOGRP–)	127–K1	101–116–A4	Enable A register to adder
ESDTS+	125–M4	A	TL1	S	(ACYEF+)(TL1FF+)(JSTOP–)(IRSOP–)(IMAOP–)	125–B4	101–116–F5-F9	Enable adder to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
EMSHL+	127–P9	A	TLATE	L	(ACYLF+)(TLATE+)(SUBOP–)(OPGAA+)	127–K9	101–107–A9	Enable M(1-7) to adder
EMSLL+	127–P11	A	TLATE	L	(ACYLF+)(TLATE+)(SUBOP–)(OPGAA+)	127–K9	108–116–A9	Enable M(8-16) to adder
ESDTS+	125–M4	A	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5/J5	101–116–F5-F9	Enable adder sum to D register
CLATR–	122–K8	A	TL4	R	(ACYLF+)(TL4FF+)(OPGAA+)(IMAOP–)	122–C2	101–116–L6	Clear A register
EDAHS+	122–P1	A	TL4	S	(ACYLF+)(TL4FF+)(OPGAA+)(IMAOP–)	122–C2	101–108–J7	Enable D register to A(1-8)
EDALS+	122–P3	A	TL4	S	(ACYLF+)(TL4FF+)(OPGAA+)(IMAOP–)	122–C2	109–116–J7	Enable D register to A(9-16)
CLYTR–	129–P3	A	TL4	R	(SCZR0–)	129–A1	101–116–E1	Clear Y register
EPYTS+	129–P4	A	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)	129–D4	101–116–K11	Enable P register to Yregister
MEMCI+	126–K12	A	TL1	L	(TL1FF+)(SPMOD–)(IGACY+)	126–F12/J12	150–A2	Enable memory cycle
COXXX+	150–D2		TL1	S	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle

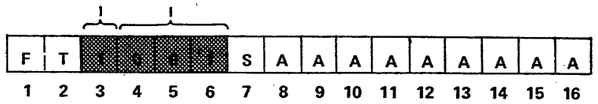

ENTER A-CYCLE FROM INSTRUCTION WORD FETCH OR LAST INDIRECT ADDRESS CYCLE
JAM SHIFT COUNTER TO ONES PRIOR TO ENTRY
EICTS-
T1
R
0 → (M)
CLMTR-
T2
STROBE
[EA] → (M)
MMnnF-
YES
A01 = M01? (CASAM-)
NO
T2 & T3 (TLATE)
(A) + (M)- + 1 → (D) VIA ADDER
(A) → (D) VIA ADDER
L
(A) → ADDER
(M)1-7 → ADDER
(M)8-16 → ADDER
EASTL+
ENSHL+
ENSLL+, EIK17-
L
(A) → ADDER
EASTL+
T3
R
S
1's → (D)
ADDER → (D)
CLDTR-
ESDTS+
SC ≠ 0
R
S
0 → (Y)
(D) → (Y)
CLYTR-
EDYTS+
T4
A01 = M01? (CASAM-)
NO
YES
(D) = 0? (DGONE-)
NO
YES
D01 = 1?
NO
YES
(A) > [EA]
(A) = [EA] V (A) < [EA]
L
L
1 → AZZZZ FF
(SC) + 1 → (SC)
SETAZ+
INCSC+
(SC) + 1 → (SC)
A
B


A
B
YES
Y01 = 1?
NO
T1
(A) < [EA]
(A) = [EA]
L
(P) + 2 → ADDER
EPSLL+, G16DJ-, EIK17-
L
(P) + 1 → ADDER
EPSLL+, EIK17-
(SC = 0)
R
S
1's → (D)
ADDER → (D)
CLDTR-
ESDTS+
T2
R
S
0 → (P)
(D) → (P)
CLPTR-
EDPTS+
T3
T4
R
S
L
S
0 → (Y)
(P) → (Y)
DEVELOP START MEMORY LEVEL
SET F-CYCLE ENTRY F-F
CLYTR-
EPYTS+
MEMCI+
FCYEF+
NEXT INSTRUCTION FETCH CYCLE
CAS
3 CYCLES
OP CODE 11

Instruction: Compare (CAS)

OP Code: 11 **Type:**

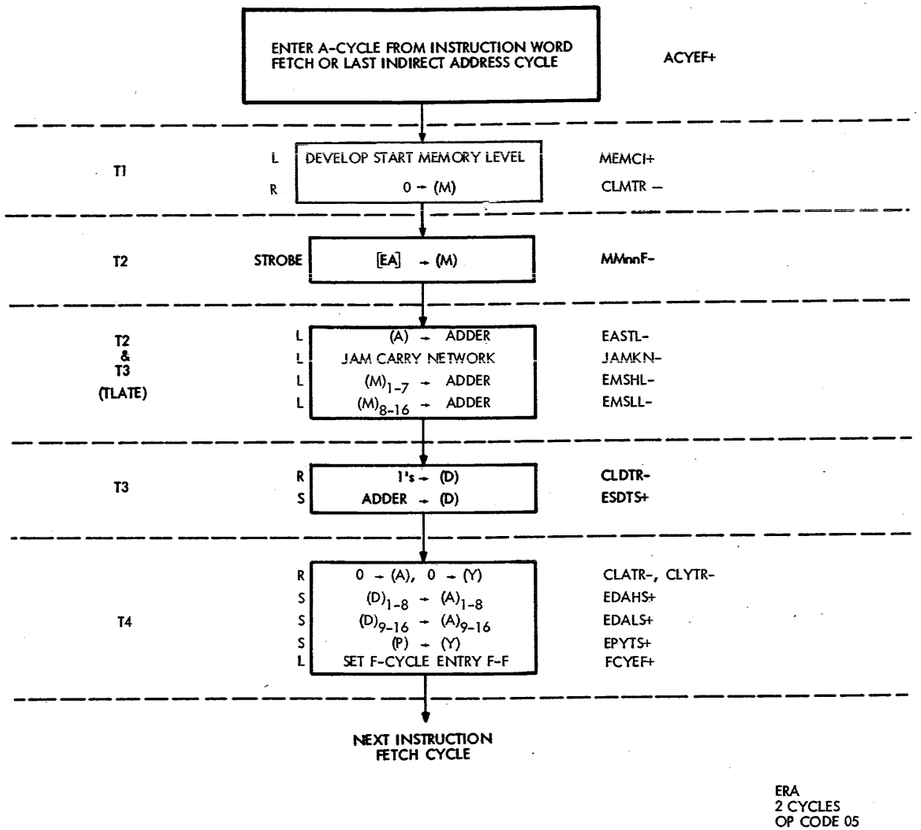
Description: If: (A) > [EA] = No operation
(A) = [EA] = Skip next instruction
(A) < [EA] = Skip two instructions



Execution Time (μs): 4.8

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
CASAM–	126–P6				(CASOP+)∧[(A01FF–(M01FF–)V(A01FF+)(M01FF+)]	126–N6	125–A12	M01 = A01
ACYEF+	119–G4	F	TL4	L	(TL4FF+)(EOINS–)(FOICY+)[(M01FF–) at 119–A5]	119–C5	119–J5	Set A-cycle
EICTS–	125–K9	F	TL4	S	(FCYLF+)(TL4FF+)(OPG3C+)	125–A7	121–A8	ONEs to shift counter
CLMTR–	128–P9	A	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–N9	101–116–L9	Clear M register
MMnnF–	142				(SWnn.±)(STRB–)	80.04	101–116–H8	Memory data set into M register
EASTL+	127–P1	A	TLATE	L	(ACYLF+)(TLATE+)(CASOP–)–	127–C1	101–116–A4	Enable A register to adder
ENSHL+	127–P8	A	TLATE	L	(ACYLF+)(TLATE+)(OPGNS+)(IRSOP–)	127–C12	101–107–A10	Enable M–(1-7) to adder
ENSLL+	127–P7	A	TLATE	L	(ACYLF+)(TLATE+)(OPGNS+)(IRSOP–)	127–C12	108–116–A10	Enable M–(8-16) to adder
EIK17–	127–P5	A	TLATE	L	(CASOP+)(ACYLF+)	127–A8/F8	116–F7-F9	Force carry to adder
								SC ≠ 0
CLDTR–	125–K5	A	TL3	R	(ANAOP–)(TL3FF+)(MCRST+)	125–B7	101–116–F11	ONEs to D register
ESDTS+	125–M4	A	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5	101–116–F5-F9	Enable adder sum to D register
CLYTR–	129–P3	A	TL4	R	(CASOP+)(TL4FF+)(MCRST+)	129–E1/H3	101–116–N12	Clear Y register
EDYTS+	129–P1	A	TL4	S	(BRREQ–)(EOINS–)(CASOP+)(MCSET+)(TL4FF+)	129–D5/F1/F5	101–116–J10	Enable D register to Y register
DGONE–	126–D9				(D01FF–) through (D16FF–)	126–A9	125–B12	D register equals ZERO
SETAZ+	125–M7	A	TL4	L	(ACYLF+)(TL4FF+)(CASOP+)∧(DGONE+)V(D01FF+)	125–A11 125–B12	125–D7	SET AZZZZ F-F
INCSC+	126–P5	A	TL4	L	(ACYLF+)(TL4FF+)*	126–L6	121–A4	Increment shift counter
G16DJ–	116–C6	A	TL1	L	(TLATE–)(ACYEF+)(CASOP+)(Y01FF+)	116–A2	116–F7 117–A8	If (A) < [EA], force additional carry to adder
EPSLL+	128–K4	A	TL1	L	(CASOP+)(TLATE–)	128–F4	101–116–A9	Enable P register to adder
EIK17–	127–P5	A	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7–F9	Force carry to adder
CLDTR–	125–K5	A	TL1	R	(ACYEF+)(TL1FF+)(JSTOP–)(IRSOP–)(IMAOP–)(MCRST+)	125–B4	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	A	TL1	S	(ACYEF+)(TL1FF+)(JSTOP–)(IRSOP–)(IMAOP–)(MCSET+)	125–B4	101–116–D4-D8	Enable adder sum to D register
CLPTR–	129–M10	A	TL2	R	(ACYEF+)(TL2FF+)(CASOP+)(AZZZZ+)(MCRST+)	129–E9	101–116–L12	Clear P register
								SC = 0
EDPTS+	129–P9	A	TL2	S	(ACYEF+)(TL2FF+)(CASOP+)(AZZZZ+)(MCSET+)	129–E9	101–116–J11	Enable D register to P register
CLYTR–	129–P3	A	TL4	R	(CASOP+)(TL4FF+)(MCRST+)	129–E1/H3	101–116–N12	Clear Y register
EPYTS+	129–P4	A	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	A	TL1	L	(TL1FF+)(SPMOD–) (IGACY+)	126–F11/H11	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150– D2	Start memory cycle

*(SC) = 1 from previous F-cycle)

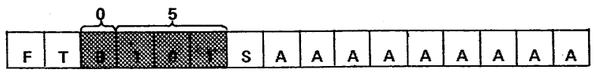


ERA
2 CYCLES
OP CODE 05

Instruction: Exclusive OR (ERA)

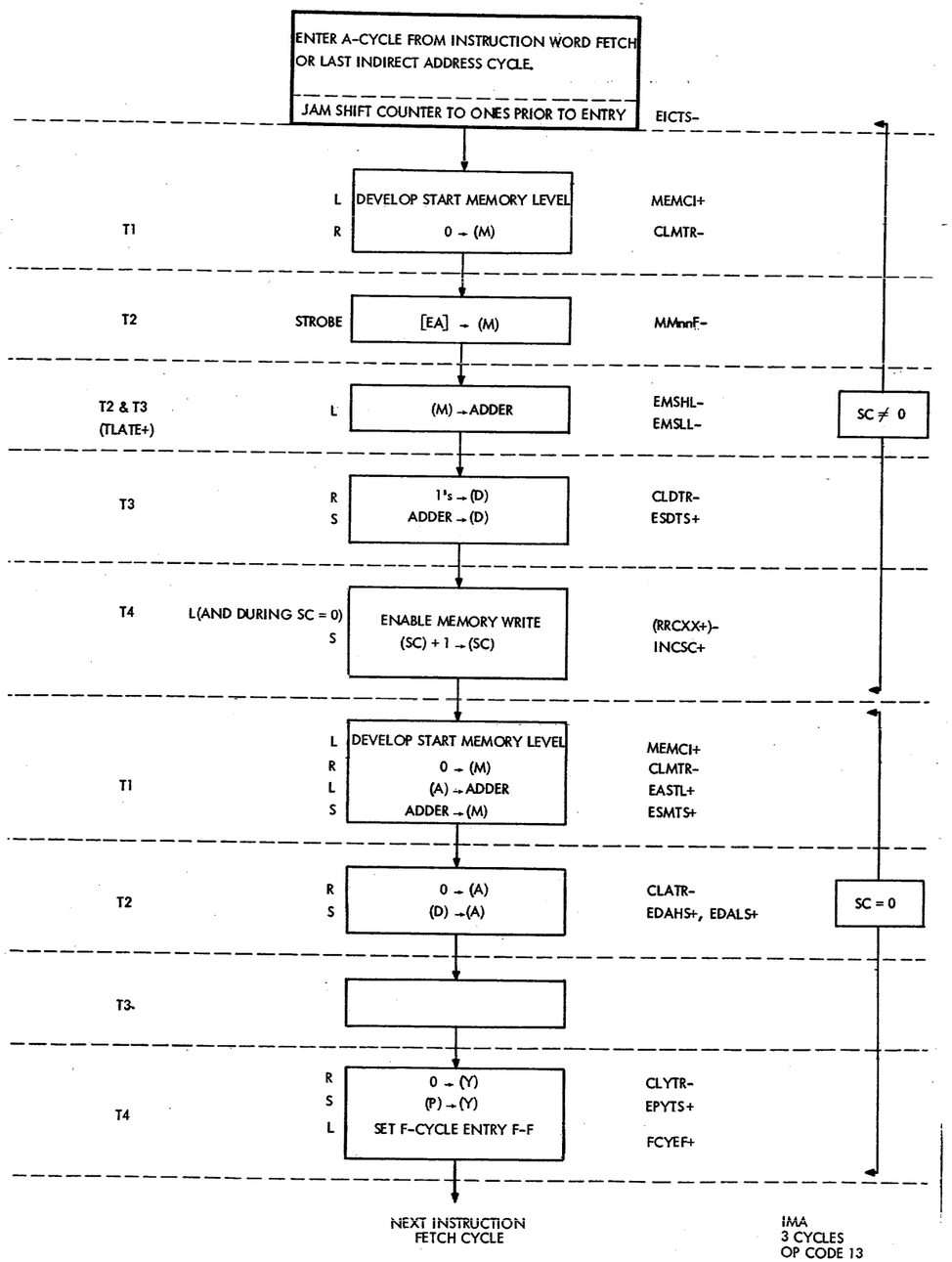
OP Code: 05 **Type:** MR, 2 cycle

Description: (A) ∀ [EA] → (A)



Execution Time (μs): 3.2

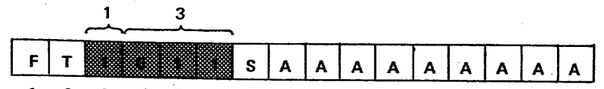
Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
CLMTR–	128–P9	A	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
EASTL+	127–P1	A	TLATE	L	(ERAOP+)(TLATE+)(ACYLF+)	127–C1	101–116–A4	Enable A register to adder
JAMKN–	127–L4	A	TLATE	L	(ACYEF+)(ERAOP+)	127–C4	101–116–C9	Jam carry network
EMSHL+	127–P9	A	TLATE	L	(ACYLF+)(TLATE+)(SUBOP–)(OPGAA+)	127–K9	101–107–A9	Enable M(1-7) to adder
EMSLL+	127–P11	A	TLATE	L	(ACYLF+)(TLATE+)(SUBOP–)(OPGAA+)	127–K9	108–116–A9	Enable M(8-16) to adder
CLDTR–	125–K5	A	TL3	R	(ANAOP–)(TL3FF+)(MCRST+)	125–B7	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	A	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5	101–116–F5-F9	Enable adder sum to D register
CLATR–	122–K8	A	TL4	R	(ACYLF+)(TL4FF+)(OPGAA+)(IMAOP–)	122–C2	101–116–L6	Clear A register
EDAHS+	122–P1	A	TL4	S	(ACYLF+)(TL4FF+)(OPGAA+)(IMAOP–)	122–C2	101–108–J7	Enable D register to A register (1-8)
EDALS+	122–P3	A	TL4	S	(ACYLF+)(TL4FF+)(OPGAA+)(IMAOP–)	122–C2	109–116–J7	Enable D register to A(9-16)
CLYTR–	129–P3	A	TL4	R	(SCZR0+)(TL4FF+)(MCRST+)	129–E1/H3	101–116–N12	Clear Y register
EPYTS+	129–P4	A	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	A	TL1	L	(TL1FF+)(SPMOD–)(IGACY+)	126–F12/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



Instruction: Interchange Memory and A (IMA)

OP Code: 13 **Type:** MR, 3 cycle

Description: (EA) ⇌ (A)

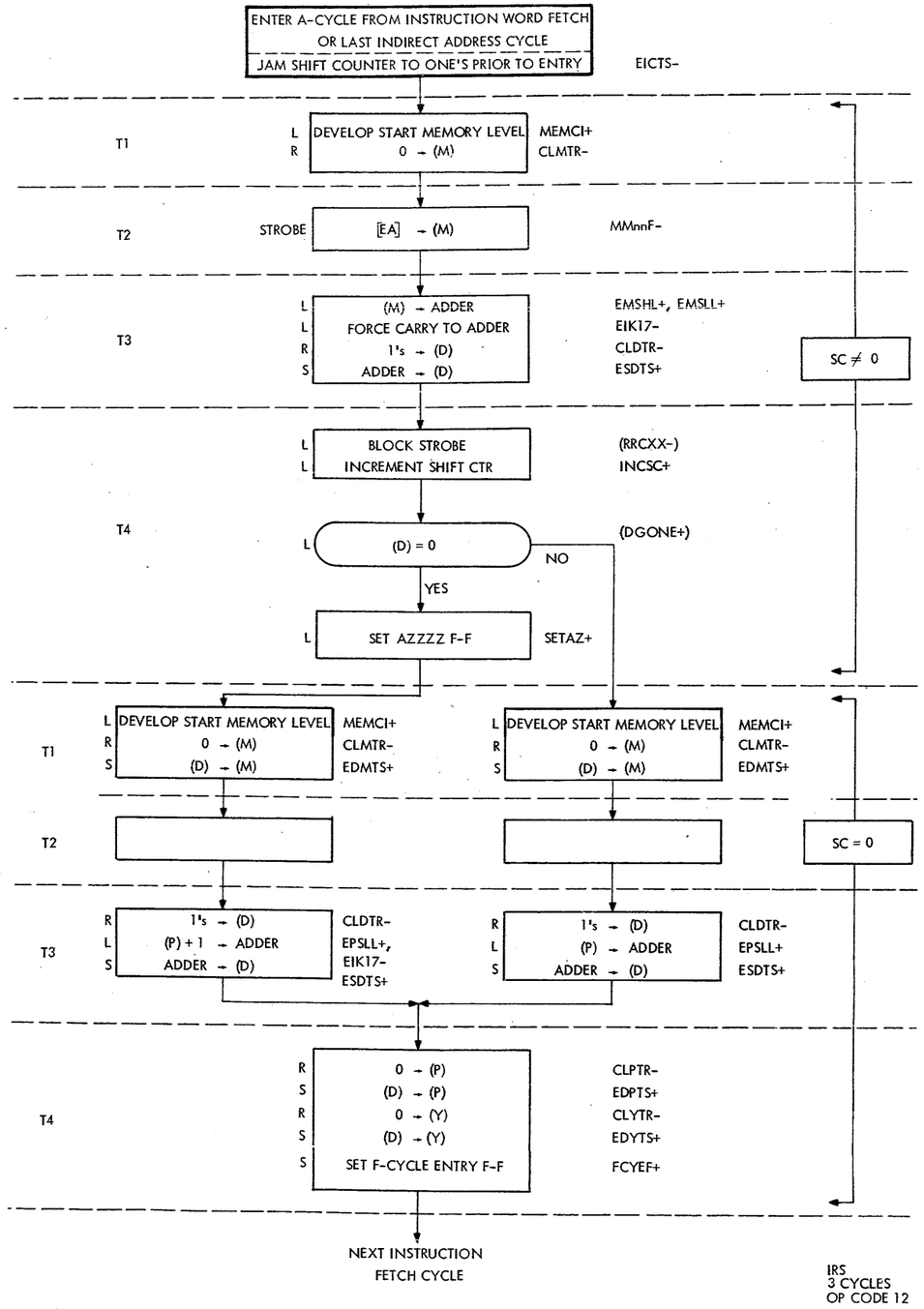


Execution Time (μs): 4.8

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
ACYEF+	119–G4	F	TL4	L	(TL4FF+)(EOINS–)(FOICY+) [(M01FF–)@119–A5]	119–C5	119–J5	Set A-cycle at next TL1
EICTS–	125–P9	F	TL4	S	(FCYLF+)(TL4FF+)(OPG3C+)*	125–A7	121–A8	Jam shift counter to ONEs
CLMTR–	128–P9	A	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–N9	101–116–L9	Reset M register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
EMSHL+	127–P9	A	TLATE		[(ACYLF+)(TLATE+)(SUBOP–)	127–K9	101–107–A9	Enable M(1-8) to adder
EMSLL+	127–P11	A	TLATE		(OPGAA+)]	127–K9	108–116–A9	Enable M(9-16) to adder
CLDTR–	125–K5	A	TL3	R	(ANAOP–)(TL3FF+)	125–B7	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	A	TL3	S	(TL3FF+)(IOGRP–)	125–B5	101–116–F5-F9	Enable adder sum to D register
MEMCI+	126–K12	A	TL4	L	(MEMCI–)	126–G12	150–A2	Enable memory cycle
INCSC+	126–P5	A	TL4	L	(ACYLF+)(TL4FF+)	126–L6	121–A4	Enable step shift counter
COXXX+	150–D2		TL4	S	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle
[SCSTP+]	121–C4	A	TL4	S	(INCSC+)(SCZR0–)(MCSET+)	121–A4	121–X6	Step shift counter to ZERO
RRCXX–	126–N8	A*	TL4	L–	(ACYEF+)(OPGWR+)(WRINH–)	126–G8	150–D6	Block STRB1+ to enable memory write cycle
		As*	TL3	L				
CLMTR–	128–P9	As	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Reset M register
EASTL+	127–P1	As	TL1	L	(ACYEF+)(TLATE–)(CASOP–) (LSXOP–)(IOGRP–)	127–K1	101–116–A4	Enable A register to adder
ESMTS+	128–G11	As	TL1	S	(RRCXX–)(MASTO–)(OPGSM+) (TL1FF+)(MCSET+)	128–C11	101–116–J9	Enable adder RnnPA+ output into M register
CLATR–	122–K8	As	TL2	R	(CLATL+)(MCRST+)*	122–G6	101–116–L6	Reset A register
EDAHS+	122–P1	As	TL2	S	[(EOINS+)(TL2FF+)(OPGAA+)	122–A3	101–108–J7	Enable D(1-8) into A(1-8)
EDALS+	122–P3	As	TL2	S	OPGSM+)]	122–A3	109–116–J7	Enable D(9-16) into A(9-16)
CLYTR–	129–P3	As	TL4	R	(TL4FF+)(ACYNX–)*	129–H3	101–116–N12	Reset Y register
FCYEF+	119–G10	As	TL4	L	(Set: (TL4FF+)(EOINS+))	119–C10	119–K10	Enable set FCYLF+at next TL1FF+
EPYTS+	129–P4	As	TL4	S	(PISEX–)(EOINS+)(TL4FF+) (OPGJS–)	129–D4	101–116–L10	Enable P register into Y register
MEMCI+	126–K12	As	TL1	L	(TL1FF+) (SPMOD–) (IGACY+)	126–G12	150–A2	Enable memory cycle
COXXX+	150–D2		TL4	S	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle

*OPG3C+ @ 120–N4 = (IMAOP–), etc.
*A/TL4/L – As/TL3/L≡ (ACYLF+)(TL4FF+) (SCZR0–) V (ACYEF+)(SCZR0+)
*A/ = A-cycle + SC ≠ 0, As/ = A-cycle + SC = 0

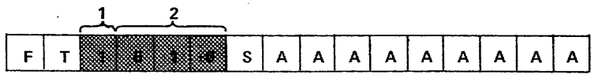
*(CLATL+) = (EOINS+)(TL2FF+)(OPGAA+)(OPGSM+) @ 122–A3
*(ACYNX=) = ((ACYLF+)(LSXOP–)(CASOP–)(SCZR0–)) @ 129–E1



Instruction: Increment, Replace, and Skip (IRS)

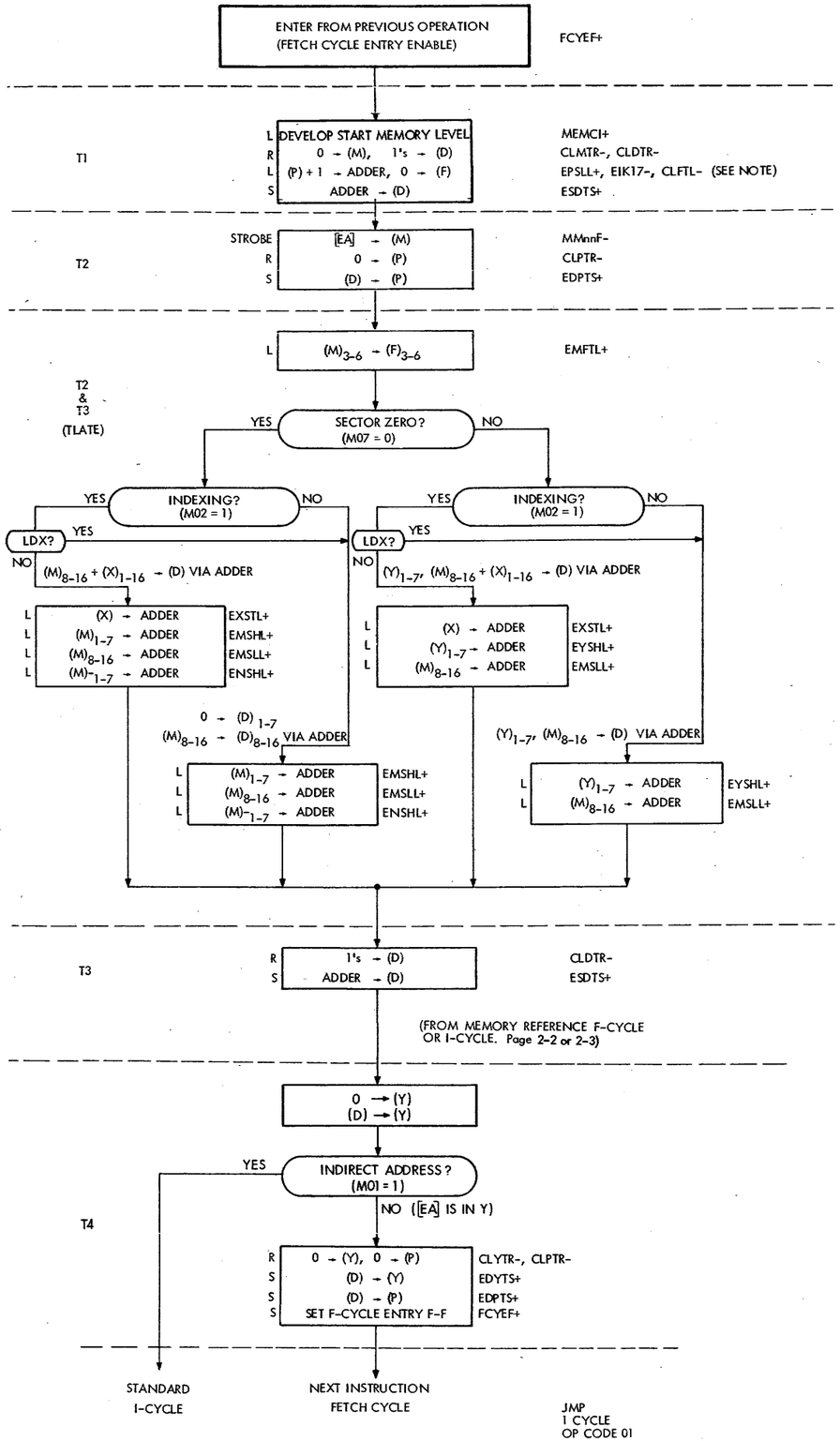
OP Code: 12 **Type:** MR, 3 cycles

Description: [EA] + 1 → [EA]



Execution Time (μs): 4.8

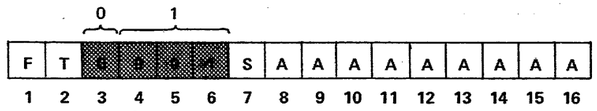
Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
ACYEF+	119–G5	F	TL4	L	(TL4FF+)(EOINS–)(M01ML–)(FCYLF+)	119–A6	119–K5	Set A-cycle FF at next TL1
EICTS–	125–K9	F	TL4	S	(FCYLF+)(TL4FF+)(OPG3C+)(MCSET+)(AZZZZ–)	125–A7/J9	121–A8	Jam shift counter to ONEs
CLMTR–	128–P9	A	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–N9	101–116–L9	Clear M register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
EMSHL+	127–P9	A	TL3	L	(ACYEF+)(IRSOP+)(SCZR0–)	127–F11	101–107–A9	Enable M(1-7) to adder
EMSLL+	127–P11	A	TL3	L	(ACYEF+)(IRSOP+)(SCZR0–)	127–F11	108–116–A9	Enable M(8-16) to adder
EIK17–	127–P5	A	TL3	L	(ACYEF+)(IRSOP+)(SCZR0–)	127 F11	116–F7–F9	Force carry to adder
CLDTR–	125–K5	A	TL3	R	(ANAOP–)(TL3FF+)	125 B7	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	A	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5/J5	101–116–F5-F9	Enable adder sum to D register
MEMCI+	126–K12	A	TL4	L	(TL1FF+)(SPMOD–) (IGACY+)	126–F12/J12	150–C1	Enable set RCYF1+
INCSC+	126–P5	A	TL4	L	(ACYLF+)(TL4FF+)	126–L6	121–A4	Increment shift counter
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle
SCSTP+	121–C4	A	TL4	S	(INCSC+)(SCZR0–)(MCSET+)	121–A4	121–X6	Step shift counter to ZERO
RRCXX–	126–N8	A	TL4	L	(ACYEF+)(OPGWR+)(WRINH–)	126–G8	150–D6	Block STRB1+ to enable memory write cycle
DGONE+	126–D9	A	TL4	L	(D01FF–) through (D16FF–)	126–A9	125–B12	D register 1-16 equals ZERO
SETAZ+	125–M7	A	TL4	L	(OPGNS+)(ACYLF+)(DGONE+)	125–B12	125–D7	Set AZZZZ+ FF
CLMTR–	128–P9	A	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–N9	101–116–L9	Clear M register
EDMTS+	128–K12	A	TL1	S	(RRCXX–)(OPGSM–)(TL1FF+)	128–F12	101–116–J8	Enable D register to M register
EIK17–	127–P5	A	TL3	L	(ACYEF+)(IRSOP+)(AZZZZ+)	127–F6	116–F7–F9	Force carry to adder
EPSLL+	128–K4	A	TL3	L	(EOINS+)(IRSOP+)	128–C4	101–116–A9	Enable P register to adder
CLDTR–	125–K5	A	TL3	R	(ANAOP–)(TL3FF+)(MCRST+)	125–B7	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	A	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5	101–116–F5-F9	Enable adder sum to D register
CLPTR–	129–M10	A	TL4	R	(OPGJS+)(EOINS+)(TL4FF+)	129–E8	101–116–E8	Clear P register
EDPTS+	129–L9	A	TL4	S	(OPGJS+)(EOINS+)(TL4FF+)	129–E8	101–116–J11	Enable D register into P register
CLYTR–	129–P3	A	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	129–H3/N3	101–116–N12	Clear Y register
EDYTS+	129–P1	A	TL4	S	(MCSET+)(TL4FF+)(SCZR0–)(EOINS–)(OPGJS–)	129–E1 D4	101–116–J10	Enable D register into Y register
MEMCI+	126–K12	A	TL1	L	(TL1FF+)(SPMOD–) (IGACY+)	126–F12/J12	150–C1	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



Instruction: Unconditional Jump (JMP)

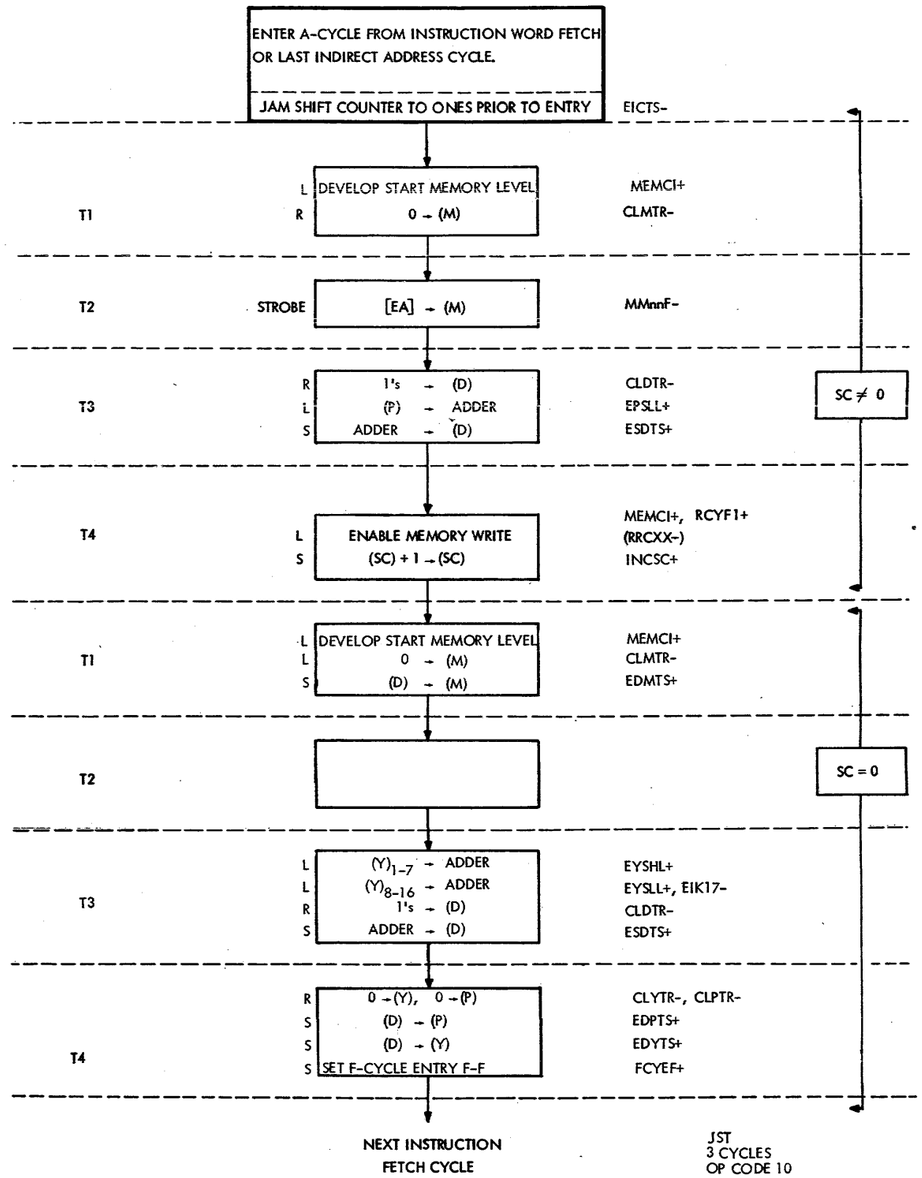
OP Code: 01 **Type:** MR, 1 cycle

Description: EA → (P)



Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–F3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7–F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–N9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+) (MCRST+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+) (MCRST+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+) (MCSET+)	125–A6	101–116–D4-F9	Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(EDPTR+)(MCRST+)	129–L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(EDPTR+)(MCSET+)	129–L9	101–116–J11	Enable D register into P register
EMFTL+	128–P4	F	TLATE	L	[(M07FF+)V(M07FF–)]Λ [(FCYLF+)(TLATE+)(GENOP–) (MEMAC–)]	128–J4	120–A2	Enable M(3-6) into F(3-6)
EMFTL–	128–K3	F	TLATE	L	See EMFTL+(M07FF+)	128–G4	127–L9	Generate EMSHL+ and ENSHL+
EXSTL+	128–P5	F	TLATE	L	(FOICY+)(MEMAC–)(M02FF+) (GENOP–)(EXSTR+)	128–H6	101–116–A5	Enable X register to adder
EMSHL+	127–P9	F	TLATE	L	(FCYSO–)	127–G10	101–107–A9	Enable M(1-7) to adder
ENSHL+	127–P8	F	TLATE	L	(FCYSO–)	127–G10	101–107–A10	Enable M–(1-7) to adder
EMSLL+	127–P11	F	TLATE	L	(FCYSO–)	127–G10	108–116–A9	Enable M(8-16) to adder
EYSHL+	128–P3	F	TLATE	L	(FCYLF+)(TLATE+)(GENOP–) (MEMAC–)(M07FF+)	128–J3	101–107–A12	Enable Y(1-7) to adder
CLDTR–	125–K5	F	TL3	R	(ACYLF–)(TL3FF+)(MCRST+)	125–B6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(IOGRP–)(TL3FF+)(MCSET+)	125–B5	101–116–F5-F8	Enable adder sum to D register
CLYTR–	129–P3	F	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	129–H3/N3	101–116–N12	Clear Y register
CLPTR–	129–M10	F	TL4	R	(OPGJS+)(EOINS+)(TL4FF+) (MCRST+)	129–E8/L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL4	S	(OPGJS+)(EOINS+)(TL4FF+) (MCSET+)	129–E8/L9	101–116–J11	Enable D register into P register
EDYTS+	129–P1	F	TL4	S	(ACYNX–)(MCSET+)(TL4FF+) (BREQ–)(OPGJS–)	129–L1	101–116–J10	Enable D register into Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–) (IGACY+)	126–F12/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle

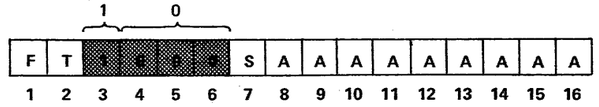


NOTE: FLAG AND TAG BITS ARE PRESERVED BY H02DJ+, 136-F6 FOR EXTENDED ADDRESSING

Instruction: Jump and Store Location (JST)

OP Code: 10 **Type:** MR, 3 cycles

Description: $(P)_{3-16} \rightarrow [EA]_{3-16}$
$[EA] + 1 \rightarrow (P)$

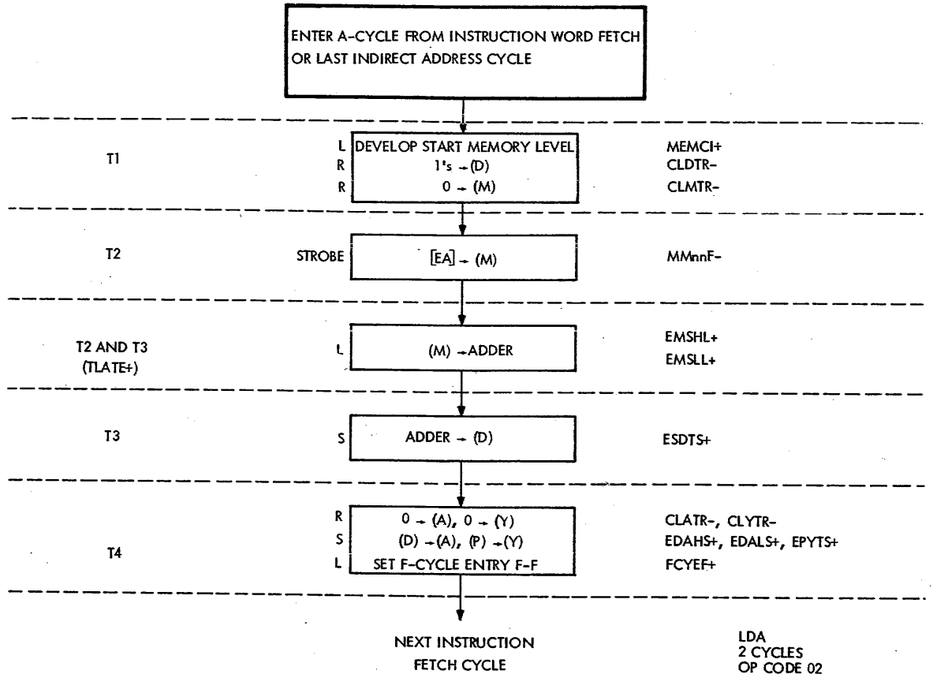


Execution Time (μs): 4.8

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
ACYEF+	119–G5	F	TL4	L	(TL4FF+)(EOINS-)(FOICY+) [(M01FF-) at 119–A5]	119–D5	119–K5	Set A-cycle at next TL1
EICTS-	125–K9	F	TL4	S	(FCYLF+)(TL4FF+)(OPG3C+)	125–A7	121–L9	ONEs to shift counter
CLMTR-	128–P9	A	TL1	R	(MCRST+)(HOLDM-)(TL1FF+)	128–N9	101–116–H9	Clear M register
MMnnF-	142				(SWnn±)(STRB-)	80.04	101–116–H8	Memory data set into M register
CLDTR-	125–K5	A	TL3	R	(ANAOP-)(TL3FF+)(MCRST+)	125–B7	101–116–F11	Clear D register to ONEs
								SC ≠ 0
EPSLL+	128–K4	A	TL3	L	(ACYEF+)(JSTOP+)(SCZR0-)	128–F5	101–116–A9	Enable P register to adder
ESDTS+	125–M4	A	TL3	S	(TL3FF+)(IOGRP-)(MCSET+)	125–B5	101–116–F5-F9	Enable adder sum to D register
INCSC+	126–P5	A	TL4	L	(ACYLF+)(TL4FF+)	126–L6	121–A4	Enable step shift counter
SCSTA-	121–A4	A	TL4	S	(INCSC+)(SCZR0-)(MCSET+)	121–A4	121–A4	Shift counter to ZEROs
MEMCI+	126–K12	A	TL1	L	(TL1FF+) (SPMOD-) (IGACY+)	126–G12	150–C1	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX-)	150–A2	150–D2	Start memory cycle
RRCXX-	126–P8	A	TL4	L	(ACYEF+)(OPGWR+)(WRINH-)	126–J8	150–D6	Block STRB1+ and enable MWC*
CLMTR-	128–P9	A	TL1	R	(See CLMTR- above)			
EDMTS+	128–K12	A	TL1	S	(RRCXX-)(OPGSM-)(MASTO-) (TL1FF+)(MCSET+)	128–F12	101–116–J8	Enable D register into M register
EYSHL+	128–P3	A	TL3	L	(ACYEF+)(JSTOP+)(SCZR0+)	128–L2	101–107–A12	Y(1-7) to adder
EYSLL+	128–P2	A	TL3	L	(ACYEF+)(JSTOP+)(SCZR0+)	128–L2	108–116–A12	Y(8-16) to adder
EIK17-	127–P5	A	TL3	L	(EYSLL-)	127–K6	116–F7	Force carry to adder
CLDTR-	125–K5	A	TL3	R	(ANAOP-)(TL3FF+)(MCRST+)	125–B7	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	A	TL3	S	(TL3FF+)(IOGRP-)(MCSET+)	125–B5	101–116–F5-F9	Enable adder sum to D register
CLYTR-	129–P3	A	TL4	R	(ACYNX-)(TL4FF+)(MCRST+)	129–H3/N3	101–116–N12	Clear Y register
								SC = 0
CLPTR-	129–M10	A	TL4	R	(OPGJS+)(EOINS+)(TL4FF+)(MCRST+)	129–E8/L9	101–116–L12	Clear P register
EDPTS+	129–P9	A	TL4	S	(OPGJS+)(EOINS+)(TL4FF+)(MCSET+)	129–E8/L9	101–116–J11	Enable D register into P register
EDYTS+	129–P1	A	TL4	S	(ACYNX-)(MCSET+)(TL4FF+)(BRREQ-)(OPGJS-)	129–L1/D4/F5	101–116–J10	Enable D register into Y register
MEMCI+	126–K12	A	TL1	L	(TL1FF+)(SPMOD-) (IGACY+)	126–F12/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX-)	150–A2	150–D2	Start memory cycle

*MWC = Memory write cycle

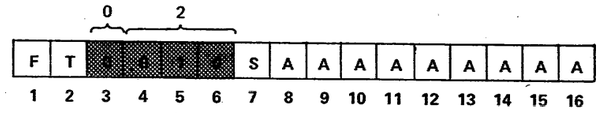
NOTE: Bit 02 of the P-register is stored when the memory expansion option is present and the computer is in the extended mode.



Instruction: Load A (LDA)

OP Code: 02 **Type:** MR, 2 cycles

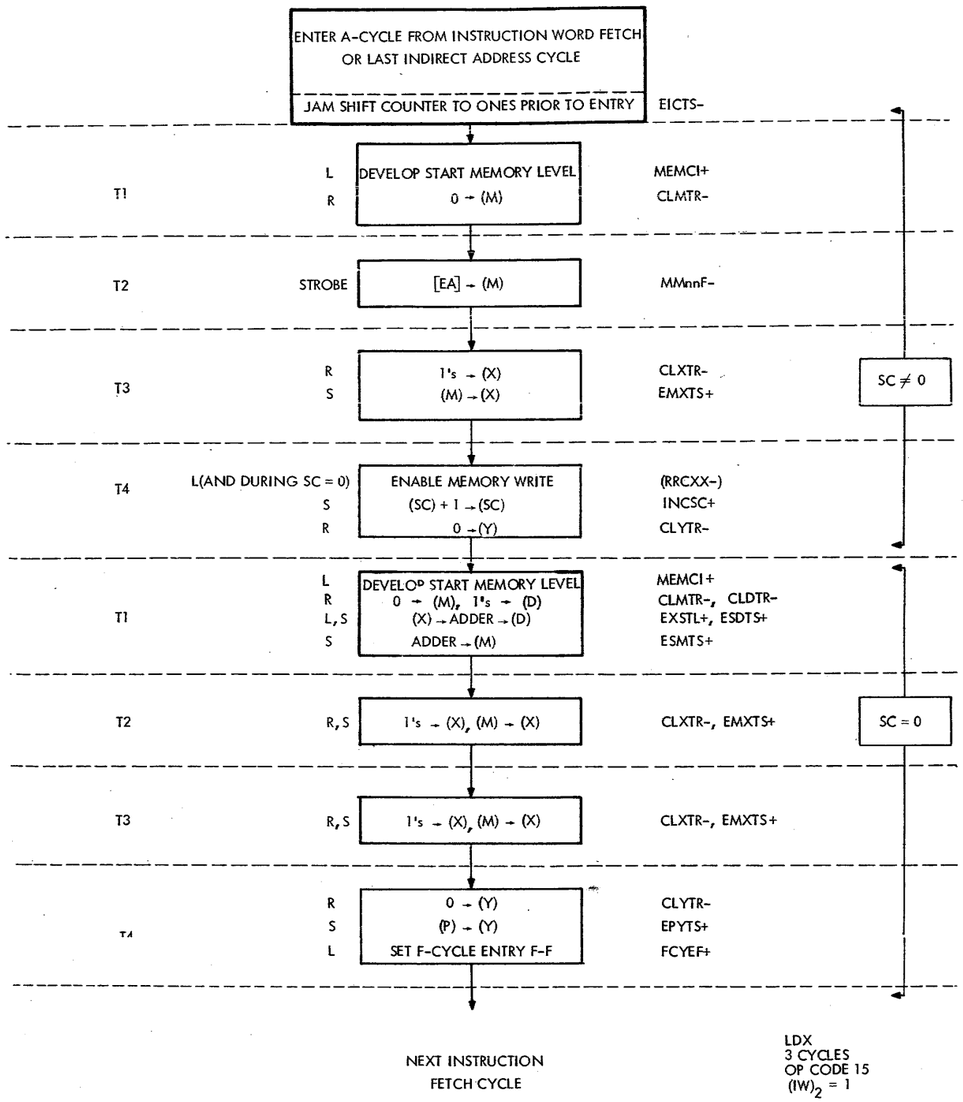
Description: (EA) → (A)



Execution Time (μs): 3.2

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
ACYEF+	119–G5	F	TL4	L	(TL4FF+)(EOINS–)(FOICY+) [(M01FF–) @ 119–A5]	119–C5	119–J5	Set A-cycle at next TL1
CLDTR–	125–K5	A	TL1	R	(ACYEF+)(TL1FF+)(JSTOP–) (IRSOP–)(IMAOP–)	125–B4	101–116–F11	Clear D register to ONEs
CLMTR–	128–P9	A	TL1	R	(MCRST+)(HOLDM+)(TL1FF+)	128–K8	101–116–H9	Reset M register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
EMSHL+	127–P9	A	TLATE		[(ACYLF+)(TLATE+)	127–K9	101–107–A9	Enable M(1-7) to adder
EMSLL+	127–P11	A	TLATE		(SUBOP–)(OPGAA+)]	127–B5	108–116–A9	Enable M(8-16) to adder
ESDTS+	125–M4	A	TL3	S	(TL3FF+)(IOGRP–)	125–B5	101–116–F5-F9	Enable adder sum to D register
CLATR–	122–K8	A	TL4	R	(CLATL+)(MCRST+)*	122–J8	101–116–L6	Reset A register
CLYTR–	129–P3	A	TL4	R	(TL4FF+)(ACYNX–)**	129–H3	101–116–N12	Reset Y register
EDAHS+	122–P1	A	TL4	S	[(ACYLF+)(TL4FF+)	122–C2	101–108–J7	Enable D(1-8) into A(1-8)
EDALS+	122–P3	A	TL4	S	(OPGAA+)(IMAOP–)]	122–L2	109–116–J7	Enable D(9-16) into A(9-16)
EPYTS+	129–P4	A	TL4	S	(PISEX–)(EOINS+)(TL4FF+) (OPGJS–)	129–D4	101–116–J11	Enable P register into Y register
FCYEF+	119–G10	A	TL4	L	[Set: (TL4FF+)(EOINS+) (DMCRQ–)(PISEX–)]	119–D10	119–C10	Enable set FCYLF+ at next TL1FF+
MEMCI+	126–K12	A	TL1	L	(TL1FF+) (SPMOD–) (IGACY+)	126–G12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+) (MBSYX–)	150–A2	150–D2	Start memory cycle

*(CLATL+) @ 122–G6 = (ACYLF+)(TL4FF+)(OPGAA+)(IMAOP–) @ 122–C2
**(ACYNX–) @ 129–F1 = ((ACYLF+)(LSXOP–)(CASOP–)(SCZR0–)) – @ 129–E1

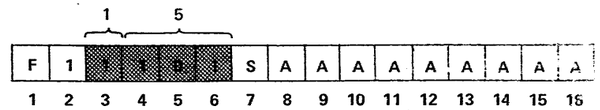


Instruction: Load Index Register (LDX)

OP Code: 15 **Type:** MR, 3 cycles

Description: (EA) → X
X → (0)

Note: Bit 2 of IW must be set



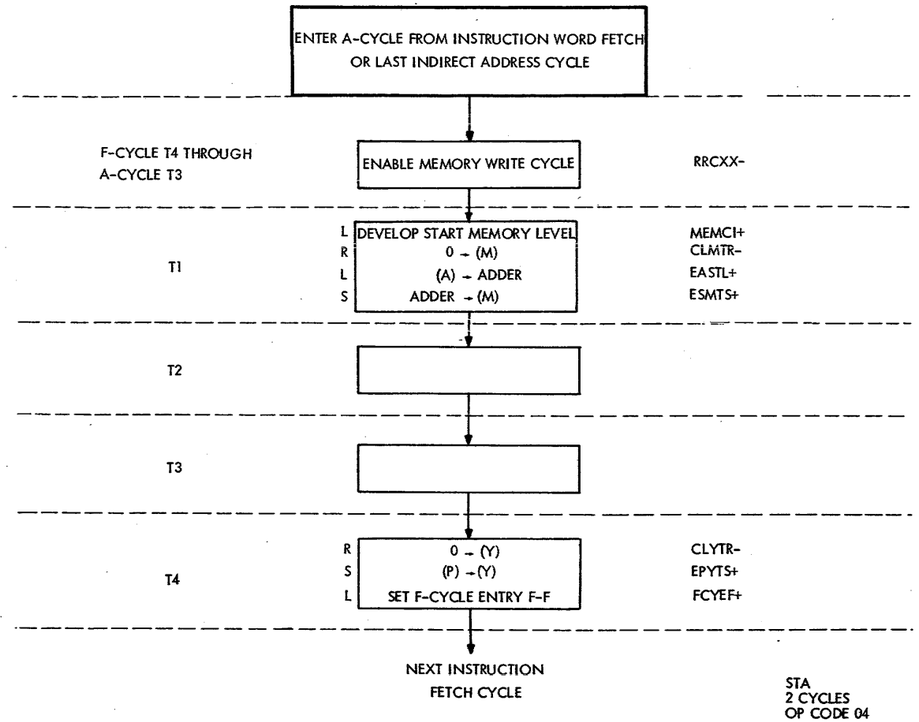
Execution Time (μs): 4.8

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
ACYEF+	119–C5	F	TL4	L	(TL4FF+)(EOINS–)(FOICY+) [(M01FF–) @ 119–A5]	119–L5	119–H3	Set A-cycle at next TL1
EICTS–	125–K9	F	TL4	A	(FCYLF+)(TL4FF+)(OPG3C+)*	125–A7	121–A8	Jam shift counter to ONEs
CLMTR–	128–P9	A	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Reset M register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLXTR–	128–M8	A	TL1	R	(ACYLF+)(TL3FF+)(LSXOP+)	128–F8	101–116–N8	Clear X register to ONEs
EMXTS+	128–P7	A	TL3	S	(ACYLF+)(TL3FF+)(LSXOP+)	128–F8	101–116–N9	Enable M register into X register
INCSC–	126–M5	A	TL4	L	(ACYLF+)(TL4FF+)	126–L6	126–N5	Reset WRINH+ FF
INCSC+	126–P5	A	TL4	L	(INCSC–)	126–N5	121–A4	Enable step shift counter from all ONEs to ZEROs
MEMCI+	126–K12	A	TL4	L	(MEMCI–)	126–G12	150–C1	Enable set RCYF1+
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle
RRCXX–	126–M8	A	**	L	(ACYEF+)(OPGWR+)(WRINH–)	126–J8	150–D6	Block STRB1+ to enable memory write cycle
CLYTR–	129–P3	A	TL4	R	(ACYNX–)(TL4FF+)***	129–H3	101–116–N12	Reset Y register (address location ZERO in memory)
EXSTL+	128–P5	A	TL1	L	(ACYEF+)(TLATE–)(LSXOP+)	128–J5	101–116–A5	Enable X register to adder
CLMTR–	128–P9	A	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Reset M register
CLDTR–	125–K5	A	TL1	R	(ACYEF+)(TL1FF+)(JSTOP–)(IRSOP–)(IMAOP–)	125–B4	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	A	TL1	S	(ACYEF+)(TL1FF+)(JSTOP–)(IRSOP–)(IMAOP–)	125–B4	101–116–F5-F9	Enable adder sum to D register
ESMTS+	128–G11	A	TL1	S	(RRCXX–)(MASTO–)(OPGSM+)(TL1FF+)(MCSET+)	128–D11	101–116–J9	Enable adder RnnPA+ output into M register
CLXTR–	128–M8	A	TL3	R	(ACYLF+)(TL3FF+)(LSXOP+)	128–F8	101–116–N8	Clear X register to ONEs
EMXTS+	128–P7	A	TL3	S	(ACYLF+)(TL3FF+)(LSXOP+)	128–F8	101–116–N9	Enable M register into X register
CLYTR–	129–P3	A	TL4	R	(TL4FF+)(ACYNX–)***	129–N3	101–116–N12	Reset Y register
FCYEF+	119–G10	A	TL4	L	(Set: (TL4FF+)(EOINS+)	119–D10	119–K10	Enable set FCYLF+ at next TL1FF+
EPYTS+	129–P4	A	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)	129–D4	101–116–L10	Enable P register into Y register
MEMCI+	126–K12	A	TL1	L	(TL1FF+) (SPMOD–) (IGACY+)	126–G12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+) (MBSYX–)	150–A2	150–D2	Start memory cycle

*(OPG3C+) @ 120–P4 = (DPOLX–), etc.
(DPOLX–) = (LSXOP+)(M02FF+) @ 124–N12

**See WRINH Set and reset timing

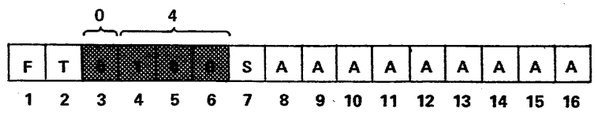
***(ACYNX–) = ((ACYLF+)(LSXOP–)(CASOP–)(SCZRO–)) – @ 129–E^1



Instruction: Store A (STA)

OP Code: 04 **Type:** MR, 2 cycles

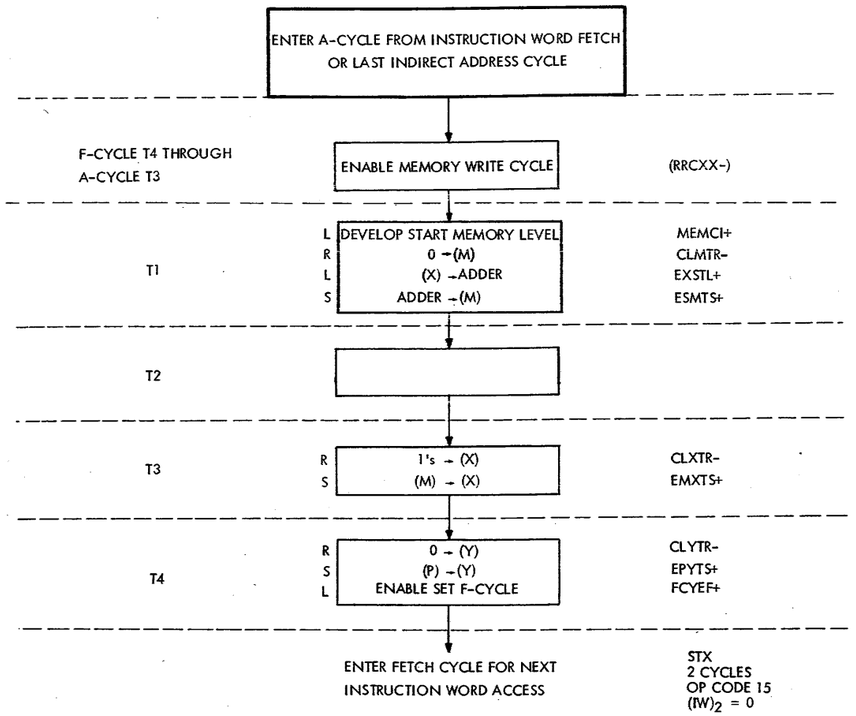
Description: (A) → (EA)



Execution Time (μs): 3.2

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
ACYEF+	119–G5	F	TL4	L	(TL4FF+)(EOINS–)(FOICY+) [(M01FF–) @ 119–A5]	119–C5	119–J5	Set A-cycle at next TL1
RRCXX–	126–M8	F	TL4 thru	L	(ACYEF+)(OPGWR+)(WRINH–)	126–J8	150–D6	Block STRB– to enable memory write cycle
		A	TL3	L				
CLMTR–	128–P9	A	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–N9	101–116–L9	Reset M register
EASTL+	127–P1	A	TL1	L	(ACYEF+)(TLATE–)(CASOP–) (LSXOP–)(IOGRP–)	127–K1	101–116–A4	Enable A register to adder
ESMTS+	128–G11	A	TL1	S	(RRCXX–)(MASTO–)(OPGSM+) (TL1FF+)(MCSET+)	128–C11	101–116–G9	Enable adder RnnPA+ output into M register
		A	TL2	L				
		A	TL3	L				
CLYTR–	129–P3	A	TL4	R	(TL4FF+)(ACYNX–)*	129–L1	101–116–N12	Reset Y register
EPYTS+	129–P4	A	TL4	S	(PISEX–)(EOINS+)(TL4FF+) (OPGJS–)	129–D4	101–116–L10	Enable P register into Y register
FCYEF+	119–G10	A	TL4	L	(Set: (TL4FF+)(EOINS+))	119–C10	119–J10	Enable set FCYLF+ at next TL1FF+
MEMCI+	126–K12	A	TL1	L	(TL1FF+) (SPMOD–) (IGACY–)	126–G12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle

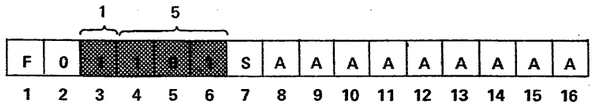
*(ACYNX–) = ((ACYLF+)(LSXOP–)(CASOP–)(SCZRO–)) – @ 129–E1



Instruction: Store Index Register (STX)

OP Code: 15 **Type:** MR, 2 cycles

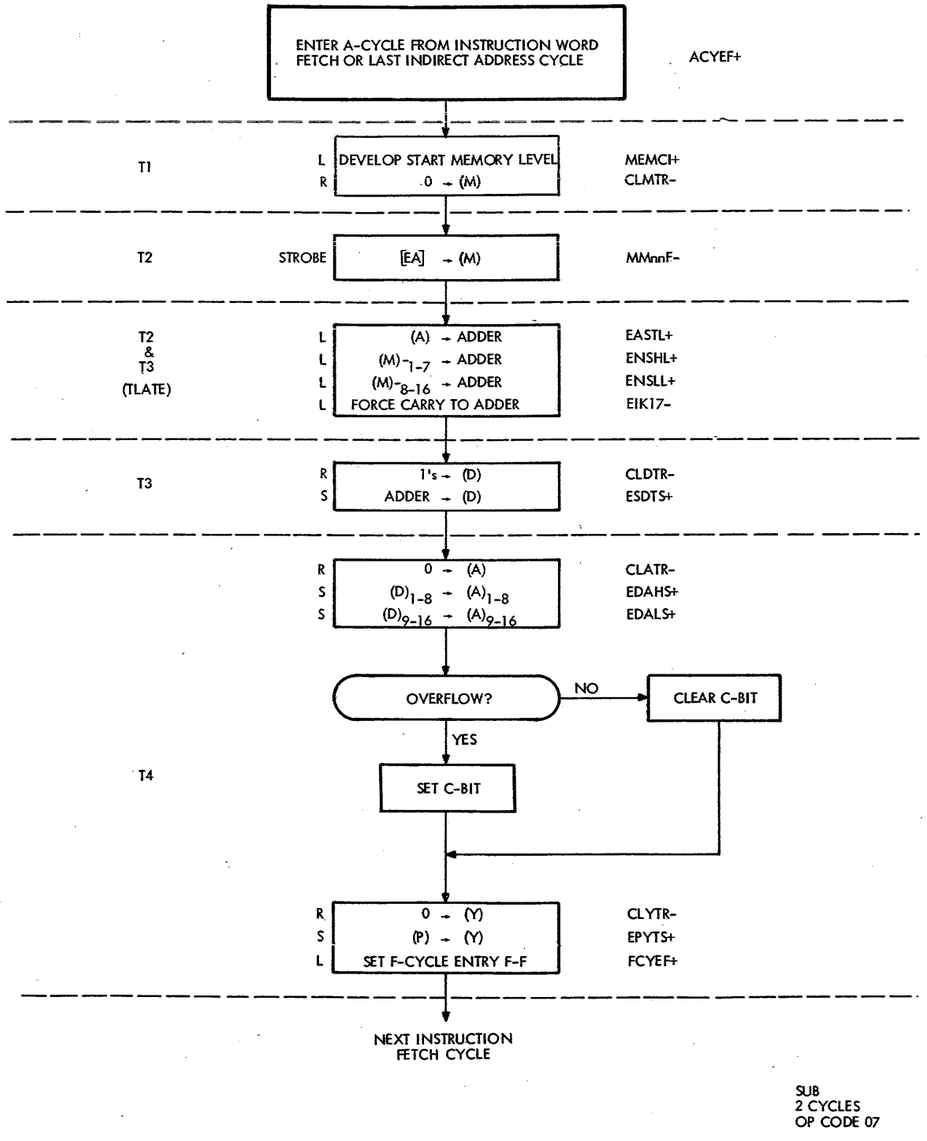
Description: (X) → (EA) **Note:** Bit 2 of IW must be reset



Execution Time (μs): 3.2

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
ACYEF+	119–G5	F	TL4	L	(TL4FF+)(EOINS-)(FOICY+) [(M01FF-) @ 119–A5]	119–C5	119–J5	Set A-cycle at next TL1
RRCXX-	126–M8	F	TL4	L-	(ACYEF+)(OPGWR+)(WRINH-)	126–J8	150–D6	Block STRB- to enable memory write cycle
		A	TL3	L				
EXSTL+	128–P5	A	TL1	L	(ACYEF+)(TLATE-)(LSXOP+)	128–J5	101–116–A5	Enable X register to adder
CLMTR-	128–P9	A	TL1	R	(MCRST+)(HOLDM-)(TL1FF+)	121–N9	101–116–L9	Reset M register
ESMTS+	128–G11	A	TL1	S	(RRCXX-)(MASTO-)(OPGSM+) (TL1FF+)(MCSET+)	128–C11	101–116–J9	Enable adder RnnPA+ output into M register
CLXTR-	128–M8	A	TL3	R	(ACYLF+)(TL3FF+)(LSXOP+)	128–F8	101–116–N8	Clear X register to ONEs
EMXTS+	128–P7	A	TL3	S	(ACYLF+)(TL3FF+)(LSXOP+)	128–F8	101–116–N9	Enable M register into X register
CLYTR-	129–P3	A	TL4	R	(TL4FF+)(ACYNX-)*	129–H3	101–116–N12	Reset Y register
FCYEF+	119–G10	A	TL4	L	(Set: (TL4FF+)(EOINS+))	119–C10	119–J10	Enable set FCYLF+ at next TL1FF+
EPYTS+	129–P4	A	TL4	S	(PISEX-)(EOINS+)(TL4FF+) (OPGJS-)	129–D4	101–116–L10	Enable P register into Y register
MEMCI+	126–K12	A	TL1	L	(TL1FF+) (SPMOD–) (IGACY+)	126–G12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX-)	150–A2	150–D2	Start memory cycle

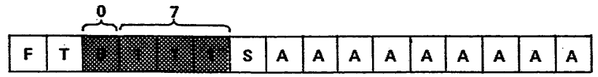
*(ACYNX–) = ((ACYLF+)(LSXOP–)(CASOP–)(SCZRO–)) – @ 129–E1



Instruction: Subtract (SUB)

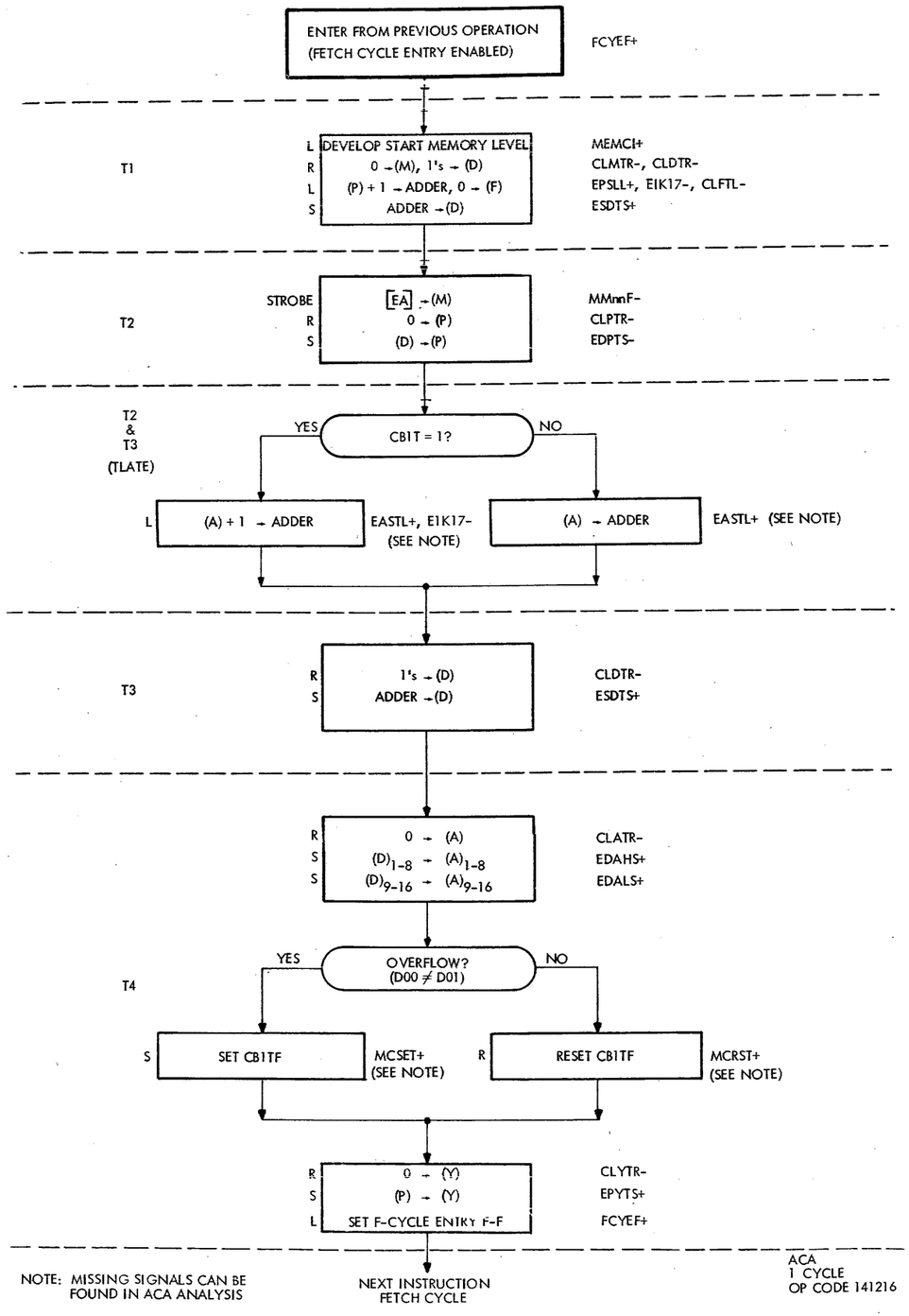
OP Code: 07 **Type:** MR, 2 cycles

Description: (A) – (EA) → (A)
OVF → (C)



Execution Time (μs): 3.2

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
CLMTR-	128–P9	A	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
MMnnF-	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
EASTL+	127–P1	A	TLATE	L	[(SUBOP–)]–(ACYLF+)(TLATE+)	127–A1/C1	101–116–A4	Enable A register to adder
ENSHL+	127–P8	A	TLATE	L	(ACYLF+)(OPGNS+)(IRSOP–)	127–C12	101–107–A10	Enable M–(1-7) to adder
ENSLL+	127–P7	A	TLATE	L	(ACYLF+)(OPGNS+)(IRSOP–)	127–C12	108–116–A10	Enable M–(8-16) to adder
EIK17–	127–P5	A	TLATE	L	(EIK17+)	127–L6	116–F7–F9 117–A1	Force carry to adder
CLDTR–	125–K5	A	TL3	R	(ANAOP–)(TL3FF+)(MCRST+)	125–B7	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	A	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5	101–116–F5-F9	Enable adder sum to D register
CLATR–	122–K8	A	TL4	R	(ACYLF+)(OPGAA+)(TL4FF+)	122–C2	101–116–L6	Clear A register
EDAHS+	122–P1	A	TL4	S	(ACYLF+)(OPGAA+)(TL4FF+)	122–C2	101–108–J7	Enable D register to A(1-8)
EDALS+	122–P3	A	TL4	S	(ACYLF+)(OPGAA+)(TL4FF+)	122–C2	109–116–J7	Enable D register to A(9-16)
CB1TF+	124–P2	A	TL4	S	(SUBOP+)(TL4FF+)(D00 = D01)(MCSET+)	124–A4	124–P2	Set CB1TF
CB1TF–	124–P1	A	TL4	R	(SUBOP+)(DIVOP–)(TL4FF+)(MCRST+)	124–A1	124–P1	Reset CB1TF
CLYTR–	129–P3	A	TL4	R	(SCZR0+)(TL4FF+)(MCRST+)	129–H3/N3	101–116–N12	Clear Y register
EPYTS+	129–P4	A	TL4	S	(PISEX–)(EOINS+)(OPGJS–)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	A	TL1	L	(TL1FF+)(SPMOD–)(IGACY+)	126–G12 K12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



Instruction: Add C to A (ACA)

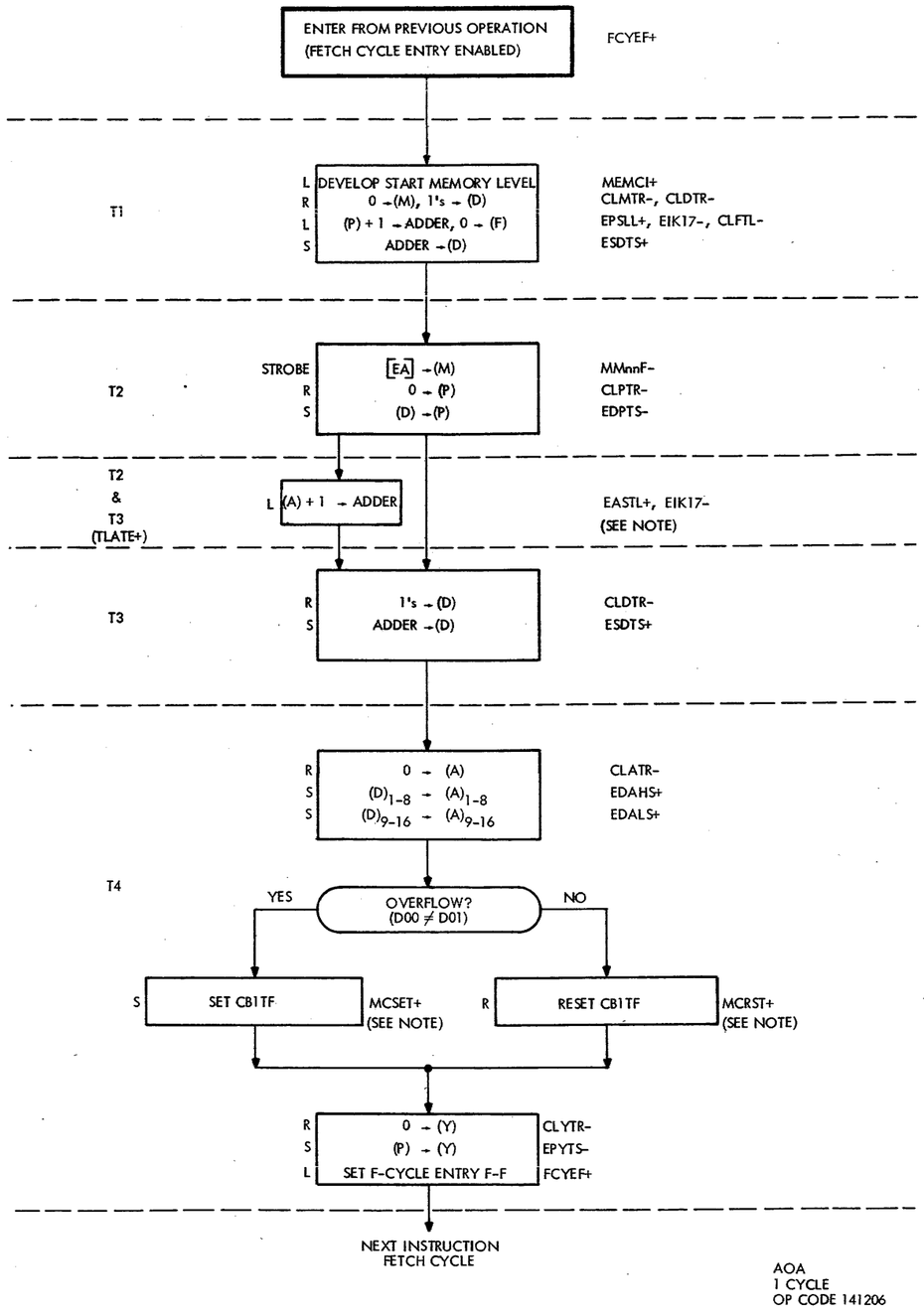
OP Code: 141216 **Type:** G, 1 cycle

Description: (A) + (C) → (A)
OVF → (C)

1	1	a	a	a	a	1	0	1	0	0	0	1	1	1	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7/F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F9	Enable adder sum to D register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZR0+)(MEMAC–)(MCRST+)	129–E7	101–116–L12	Clear P register
EIK17–	127–P5	F	TLATE	L	(CB1TF+)(GENOP+)(M01FF+)(M15FF+)	127–C11/F5	116–F7/F9 117–A1	Force carry to adder
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF+)(SCZR0+)(MEMAC–)(MCSET+)	129–C7	101–116–J11	Enable adder sum to D register
EASTL+	127–P1	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	101–116–A4	Enable A register to adder
EMSHL+	127–P9	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	101–107–A9	Enable M(1-7) to adder
ENSHL+	127–P8	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	101–107–A10	Enable M–(1-7) to adder
EMSLL+	127–P11	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	108–116–A9	Enable M(8-16) to adder
ENSLL+	127–P7	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	108–116–A10	Enable M–(8-16) to adder
CLDTR–	125–K5	F	TL3	R	(TL3FF+)(ACYLF–)(MCRST+)	125–B6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5	101–116–F5-F9	Enable adder sum to D register
CLATR–	122-K8	F	TL4	R	(M15FF+)(GENOA+)(TL4FF+)	122–A2	101–116–L6	Clear A register
EDAHS+	122–L1	F	TL4	S	(M15FF+)(GENOA+)(TL4FF+)	122–A2	101–108–J7	Enable D register to A(1-8)
EDALS+	122–P3	F	TL4	S	(M15FF+)(GENOA+)(TL4FF+)	122–A2	109–116–J7	Enable D register to A(9-16)
CB1TF–	124–P1	F	TL4	R	(TL4FF+)(DIVOP–)(GENOA+)(M09FF+)(M11FF–)(MCRST+)	124–A1/A2	124–L1	Clear CB1TF at TL4 with reset clock
CB1TF+	124–P2	F	TL4	S	(D00 ≠ D01)(TL4FF+)(GENOA+)(M09FF+)(M11FF–)(MCSET+)	124–A1/A2	124–L2	Set CB1TF when D00 ≠ D01
CLYTR–	129–P3	F	TL4	R	(SCZR0+)(TL4FF+)(MCRST+)	129–E1/H3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–)(IGACY+)	126–F12/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



AOA
1 CYCLE
OP CODE 141206

NOTE: MISSING SIGNALS CAN BE FOUND IN AOA ANALYSIS

Instruction: Add ONE to A (AOA)

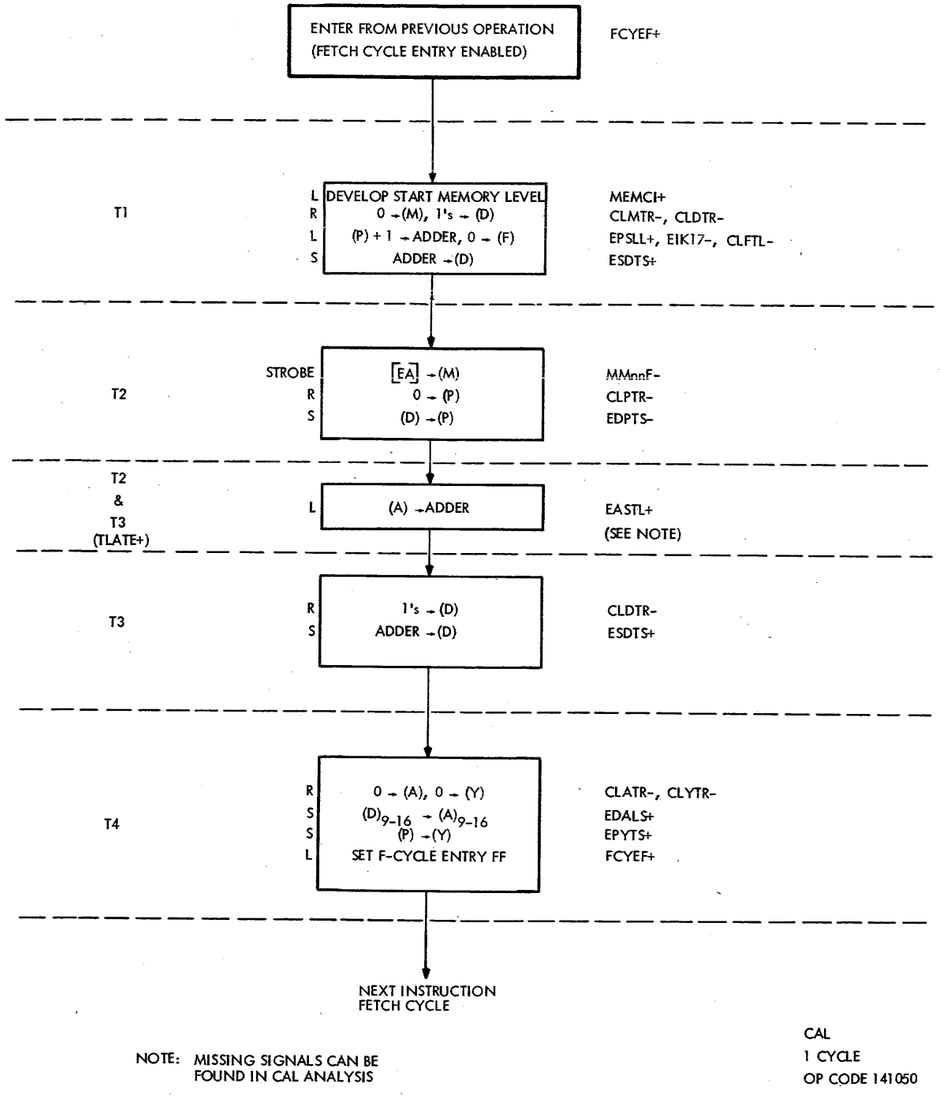
OP Code: 141206 **Type:** G, 1 cycle

Description: (A) + 1 → (A)
OVF → (C)

1	1	0	0	0	0	1	0	1	0	0	0	0	1	1	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7/F9 117–A1	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnnF–	142				(SWnn↓)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZR0+)(MEMAC–)(MCRST+)	129–E7	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF+)(SCZR0+)(MEMAC–)(MCSET+)	129–E7	101–116–J11	Enable D register to P register
EASTL+	127–P1	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	101–116–A4	Enable A register to adder
EMSHL+	127–P9	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	101–107–A9	Enable M(1-7) to adder
ENSHL+	127–P8	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	101–107–A10	Enable M–(1-7) to adder
EMSLL+	127–P11	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	108–116–A9	Enable M(8-16) to adder
ENSLL+	127–P7	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	108–116–A10	Enable M–(8-16) to adder
EIK17–	127–P5	F	TLATE	L	(M13FF–)(GENOP+)(M01FF+)(M15FF+)	127–C11 F5	116–F7/F9 117–A1	Force carry to adder
CLDTR–	125–K5	F	TL3	R	(TL3FF+)(ACYLF–)(MCRST+)	125–B6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5	101–116–F5-F9	Enable adder sum to D register
CLATR–	122–K8	F	TL4	R	(M15FF+)(GENOA+)(TL4FF+)	122–A2	101–116–L6	Clear A register
EDAHS+	122–P1	F	TL4	S	(M15FF+)(GENOA+)(TL4FF+)	122–A2	101–108–J7	Enable D register to A(1-8)
EDALS+	122–P3	F	TL4	S	(M15FF+)(GENOA+)(TL4FF+)	122–A2	109–116–J7	Enable D register to A(9-16)
CB1TF–	124–P1	F	TL4	R	(TL4FF+)(DIVOP–)(GENOA+)–(M09FF+)(M11FF–)(MCRST+)	124–A2	124–L1	Clear C-bit with reset clock
CB1TF+	124–P2	F	TL4	S	(D00 ≠ D01)(GENOA+)(M09FF+)(M11FF–)(TL4FF+)(MCSET+)	124–A1 A2	124–L2	Set C-bit when D00 ≠ D01
CLYTR–	129–P3	F	TL4	R	(SCZR0+)(TL4FF+)(MCRST+)	129–E1/H3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–)(IGACY+)	126–F2/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



Instruction: Clear Left Half (CAL)

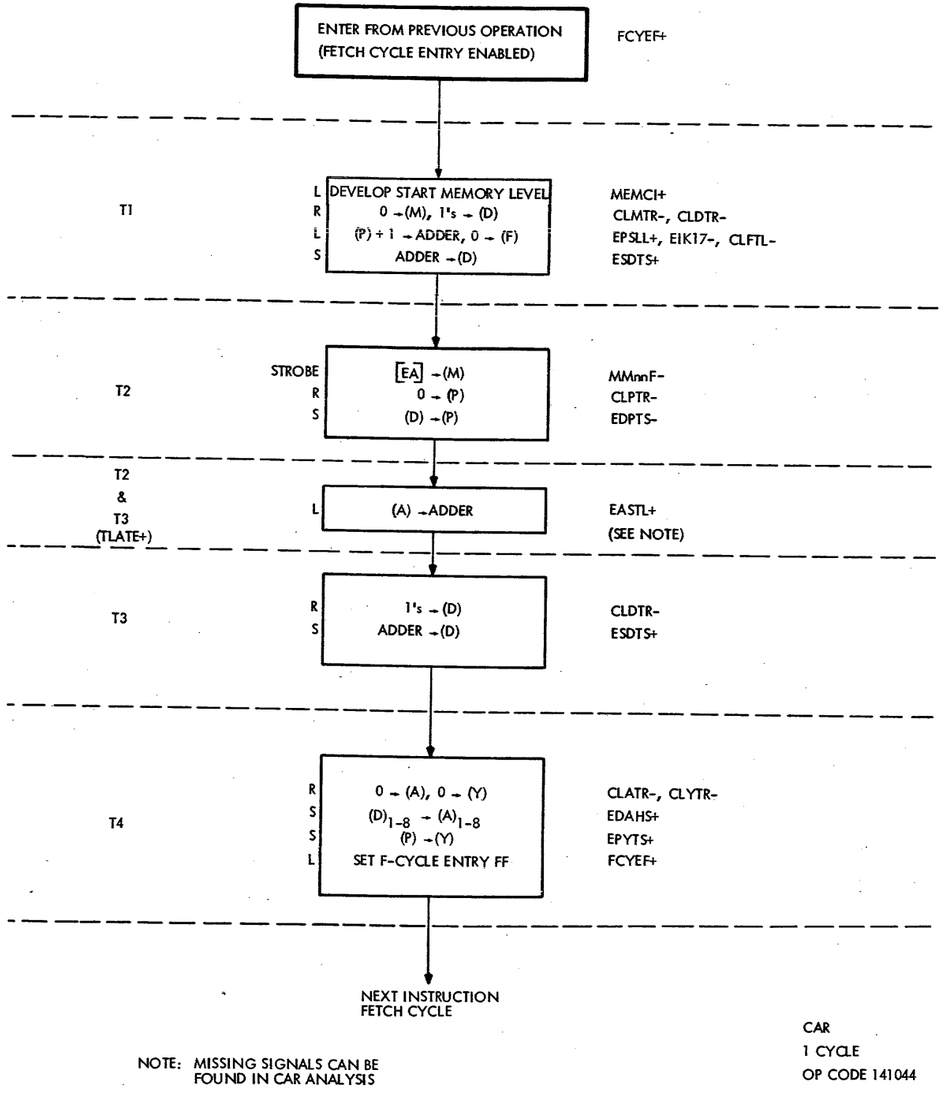
OP Code: 141050 **Type:** G, 1 cycle

Description: $0 \rightarrow (A)_{1-8}$

1	1	◀	◀	◀	◀	1	0	0	0	1	0	1	0	0	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7-F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear Shift Counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(EDPTR+)(MCRST+)	129–L9	101–116–L12	Clear P register
EDPTS–	129–P9	F	TL2	S	(EDPTR+)(MCSET+)	129–L9	101–116–J11	Enable D register into P register
EASTL+	127–P1	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	101–116–A4	Enable A register to adder
EMSHL+	127–P9	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	101–107–A9	Enable M(1-7) to adder
ENSHL+	127–P8	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	101–107–A10	Enable M–(1-7) to adder
EMSLL+	127–P11	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	108–116–A9	Enable M(8-16) to adder
ENSLL+	127–P7	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	108–116–A10	Enable M–(8-16) to adder
JAMKN–	127–L5	F	TLATE	L	(GENOP+)(M01FF+)(M02FF+)	127–L3	101–116–C9	Force carry network to ZERO
CLDTR–	127–K5	F	TL3	R	(TL3FF+)(ACYLF–)	125–B6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(TL3FF+)(IOGRP–)	125–B5	101–116–F5-F9	Enable adder sum to D register
CLATR–	122–K8	F	TL4	R	(GENOA+)(M11FF+)(TL4FF+)	122–C4	101–116–L6	Clear A register
CLYTR–	129–P3	F	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	129–H3	101–116–N12	Clear Y register
EDALS+	122–P3	F	TL4	S	(GENOA+)(M11FF+)(M13FF+)	129–D5/H2	109–116–J7	Enable D register to A(9-16)
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(OPGJS–)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–)(IGACY+)	126–F2/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



Instruction: Clear Right Half (CAR)

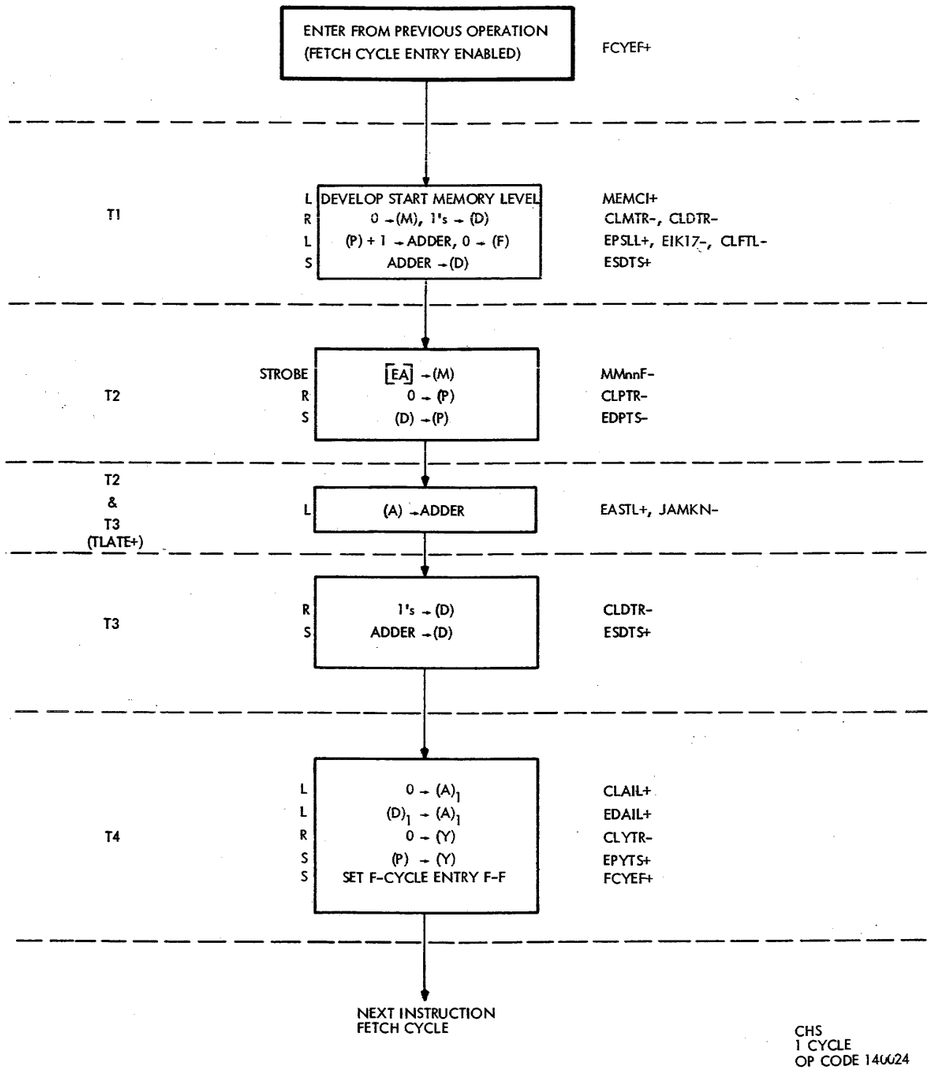
OP Code: 141044 **Type:** G, 1 cycle

Description: $0 \rightarrow (A)_{9-16}$

1	1	0	0	0	0	1	0	0	0	1	0	0	1	0	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7-F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–B1	Clear F register
							121–A5	Clear shift counter
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	125–D8 101–116–F5-F9	Clear AZZZZ FF Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(EDPTR+)(MCRST+)	129–L10	101–116–L12	Clear P register
EDPTS–	129–P9	F	TL2	S	(EDPTR+)(MCSET+)	129–L9	101–116–J11	Enable D register into P register
EASTL+	127–P1	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	129–K12	101–116–A4	Enable A register to adder
EMSHL+	127–P9	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	101–107–A9	Enable M(1-7) to adder
ENSHL+	127–P8	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	101–107–A10	Enable M–(1-7) to adder
EMSLL+	127–P11	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	108–116–A9	Enable M(8-16) to adder
ENSLL+	127–P7	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K12	108–116–A10	Enable M–(8-16) to adder
JAMKN–	127–L5	F	TLATE	L	(GENOP+)(M01FF+)(M02FF+)	127–L3	101–116–C9	Force carry network to ZERO
CLDTR–	127–K5	F	TL3	R	(TL3FF+)(ACYLF–)	125–B6	117-C1-C4-K5 101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(TL3FF+)(IOGRP–)	125–B5	101–116–F5-F9	Enable adder sum to D register
CLATR–	122–K8	F	TL4	R	(GENOA+)(M11FF+)(TL4FF+)	122–C4	101–116–L6	Clear A register
CLYTR–	129–P3	F	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	129–H3	101–116–N12	Clear Y register
EDAHS+	122–P1	F	TL4	S	(GENOA+)(M11FF+)(M14FF+)	122–C4/J2	101–108–J7	Enable D register to A register 1-8
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(OPGJS–)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–) (IGACY+)	126–F2/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



Instruction: Complement A Sign (CHS)

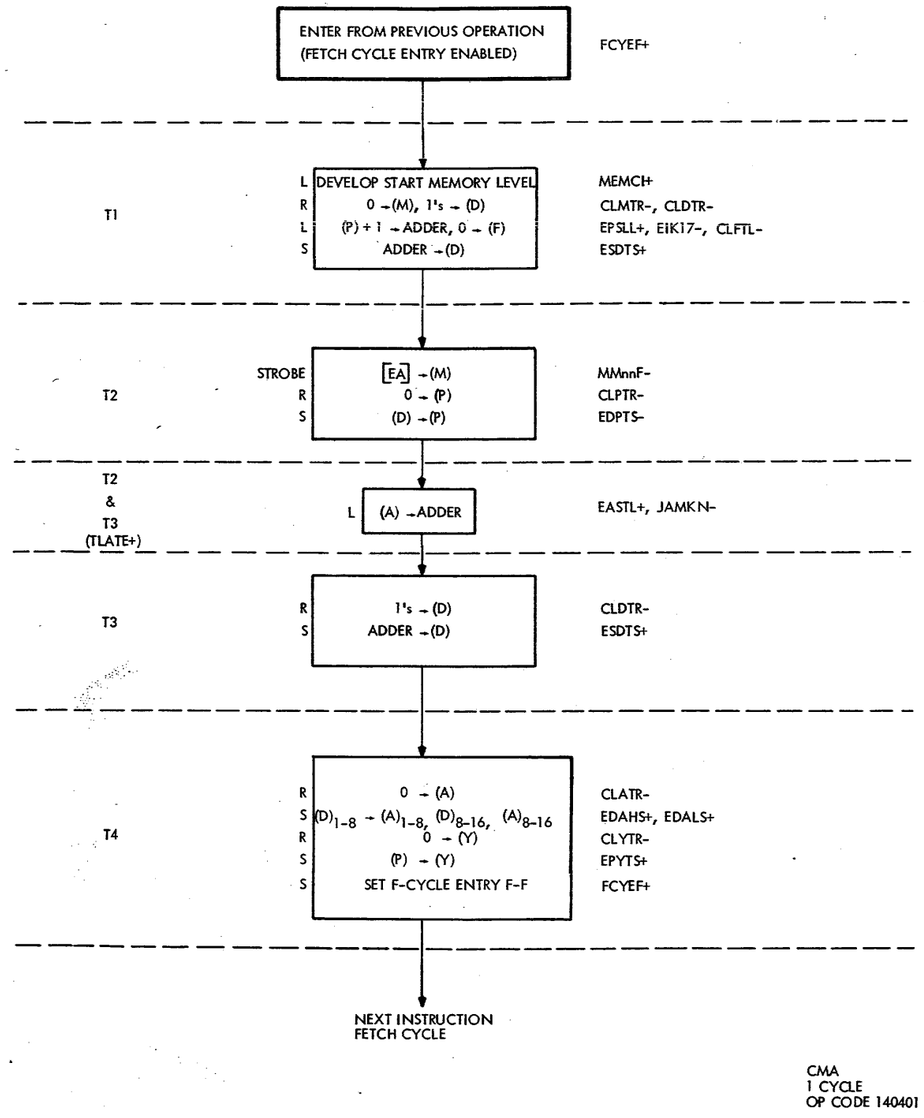
Op Code: 140024 **Type:** G, 1 cycle

Description: ONE's complement of $(A_1) \rightarrow (A_1)$

1	1	a	a	a	a	0	0	0	0	0	1	0	1	0	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time: (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7/F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZR0+)(MEMAC–)(MCRST+)	129–E7/L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF+)(SCZR0+)(MEMAC–)(MCSET+)	129–E7/L9	101–116–J11	Enable D register to P register
EASTL+	127–P1	F	TLATE	L	(EASAL–)	127–D3	101–116–A4	Enable A register to adder
JAMKN–	127–L5	F	TLATE	L	(EASAL–)	127–D3	101–116–C9 117–C1-C4-K5	Jam carry network
CLDTR–	125–K5	F	TL3	R	(TL3FF+)(ACYLF–)(MCRST+)	125–B6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5	101–116–F5-F9	Enable adder sum to D register
CLAIL+	130–K11	F	TL4	L	(GENOA+)(TL4FF+)(M14FF+)	130–F9	101–L4	Clear A register bit 1
EDAIL+	130–K10	F	TL4	L	(GENOA+)(TL4FF+)(M14FF+)	130–F9	101–L7	Enable D register bit 1 into A register bit 1
CLYTR–	129–P3	F	TL4	R	(SCZR0+)(TL4FF+)(MCRST+)	129–E1-H3-N5	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)	129–D4/L4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+) (SPMOD–) (IGACY+)	126–F2/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



CMA
1 CYCLE
OP CODE 140401

Instruction: Complement A (CMA)

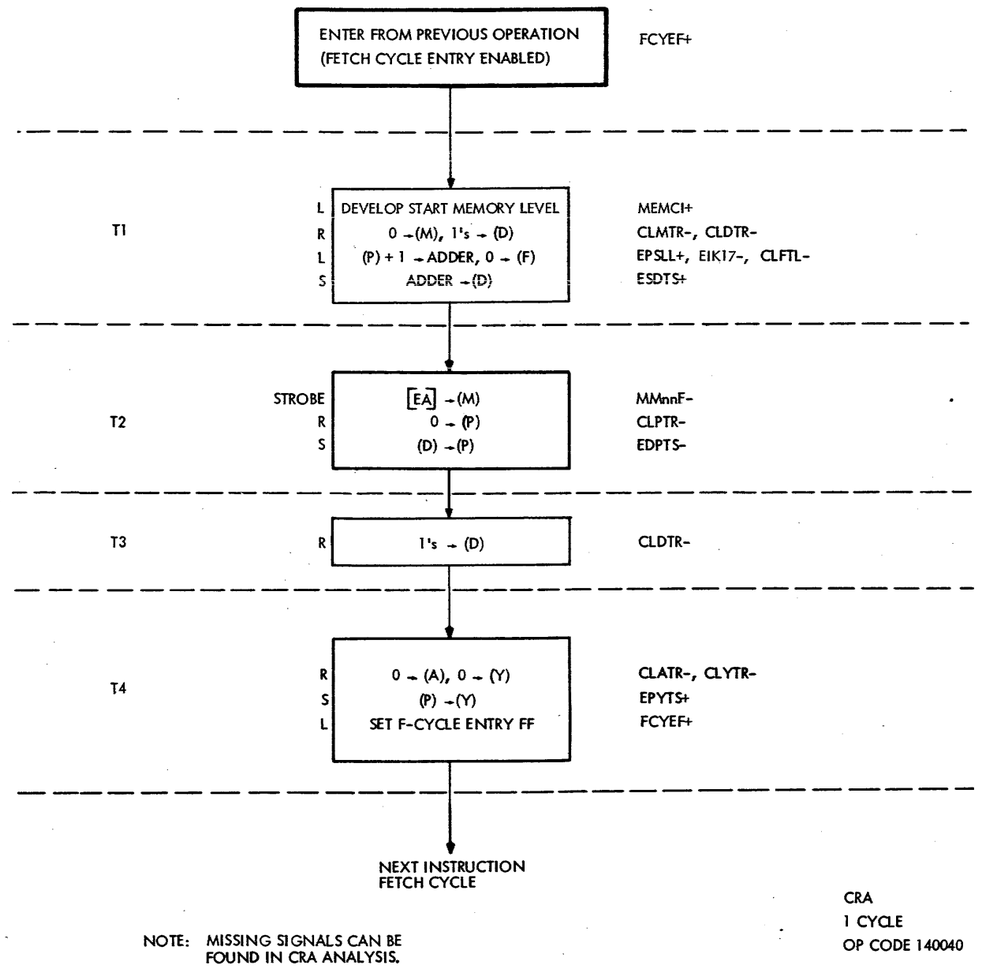
OP Code: 140401 **Type:** G, 1 cycle

Description: ONE's complement of (A) → (A)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	1

Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7-F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnn F–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZR0+)(MEMAC–)(MCRST+)	128–E7/L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF†)(SCZR0+)(MEMAC–)(MCSET+)	129–E7/L10	101–116–J11	Enable D register to P register
EASTL+	127–P1	F	TLATE	L	(EASAL–)	127–D3	101–116–A4	Enable A register to adder
JAMKN–	127–L5	F	TLATE	L	(EASAL–)	127–D3	101–116–C9 117–C1-C4-K5	Jam carry network
CLDTR–	125–K5	F	TL3	R	(TL3FF+)(ACYLF–)(MCRST+)	125–B6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5	101–116–F5-F9	Enable adder sum to D register
CLATR–	122–K8	F	TL4	R	(M16FF+)(GENOA+)(TL4FF+)(MCRST+)	122–A1/J8	101–116–L6	Clear A register
EDAHS+	122–P1	F	TL4	S	(M16FF+)(GENOA+)(TL4FF+)(MCSET+)	122–A1/J1	101–108–J7	Enable D register to A(1-8)
EDALS+	122–P3	F	TL4	S	(M16FF+)(GENOA+)(TL4FF+)(MCSET+)	122–A2	108–116–J7	Enable D register to A(9-16)
CLYTR–	129–P3	F	TL4	R	(SCZR0+)(TL4FF+)(MCRST+)	129–E1-H3-N3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)	129–D4/L4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+) (SPMOD–) (IGACY+)	126–F2 J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	F	(MEMCI+)(MBSYX+)	150–A2	150–D2	Start memory cycle



NOTE: MISSING SIGNALS CAN BE FOUND IN CRA ANALYSIS.

Instruction: Clear A-register (CRA)

OP Code: 140040 **Type:** Generic, 1 cycle

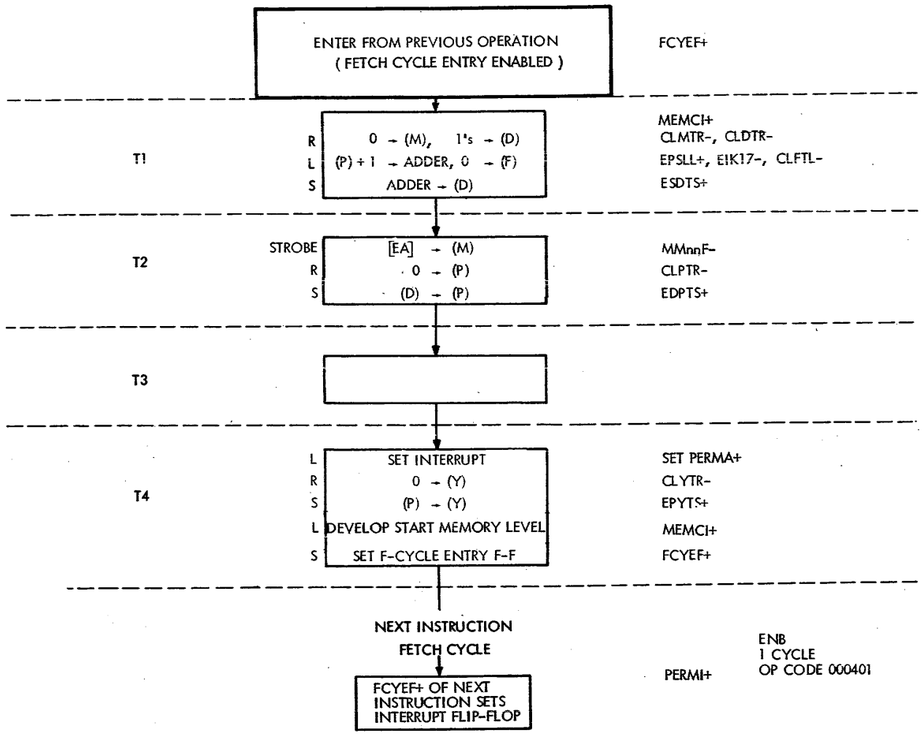
Description: $0s \rightarrow (A)_{1-16}$

1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time: (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17+	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7/F9	Force carry-in to bit 16
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Reset M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Reset F register Reset shift counter Reset AZZZZ+
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A5	101–116–F5-F9	Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(EDPTR+)*	129–J9	101–116–L12	Reset P register
EDPTS+	129–P9	F	TL2	S	(EDPTR+)*	129–J9	101–116–J11	Enable D register into P register
CLDTR–	125–K5	F	TL3	R	(TL3FF+)(ACYLF–)	125–C6	101–116–F11	Clear D register to ONEs
CLATR–	122–K8	F	TL4	R	(CLATL+)(MCRST+)**	122–J8	101–116–L6	Reset A register
CLYTR–	129–P3	F	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	129–H3/N3	101–116–N12	Reset Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)	129–D4/L4	101–116–L10	Enable P register into Y register
MEMCI+	126–K12	F	TL1	L	(MEMCI–)***	126–G11	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle
FCYEF+	119–F10	F	TL4	L	(Set: (TL4FF+)(EOINS+))	119–D10	119–H9	Enable set FCYLF+ at next TL1FF+

*(EDPTL+) @ 129–J9 = (FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–) @ 129–E7
**(CLATL+) @ 122–G6 = (GENOA+)(M11FF+)(TL4FF+) @ 122–C4
***(MEMCI–) @ 126–G2 = (TL1FF+)(SPMOD–)((IOGRP+)(FCYLF+)–) @ 126–F12/C12



Instruction: Enable Program Interrupt (ENB)

OP Code: 000401 **Type:** G, 1 cycle

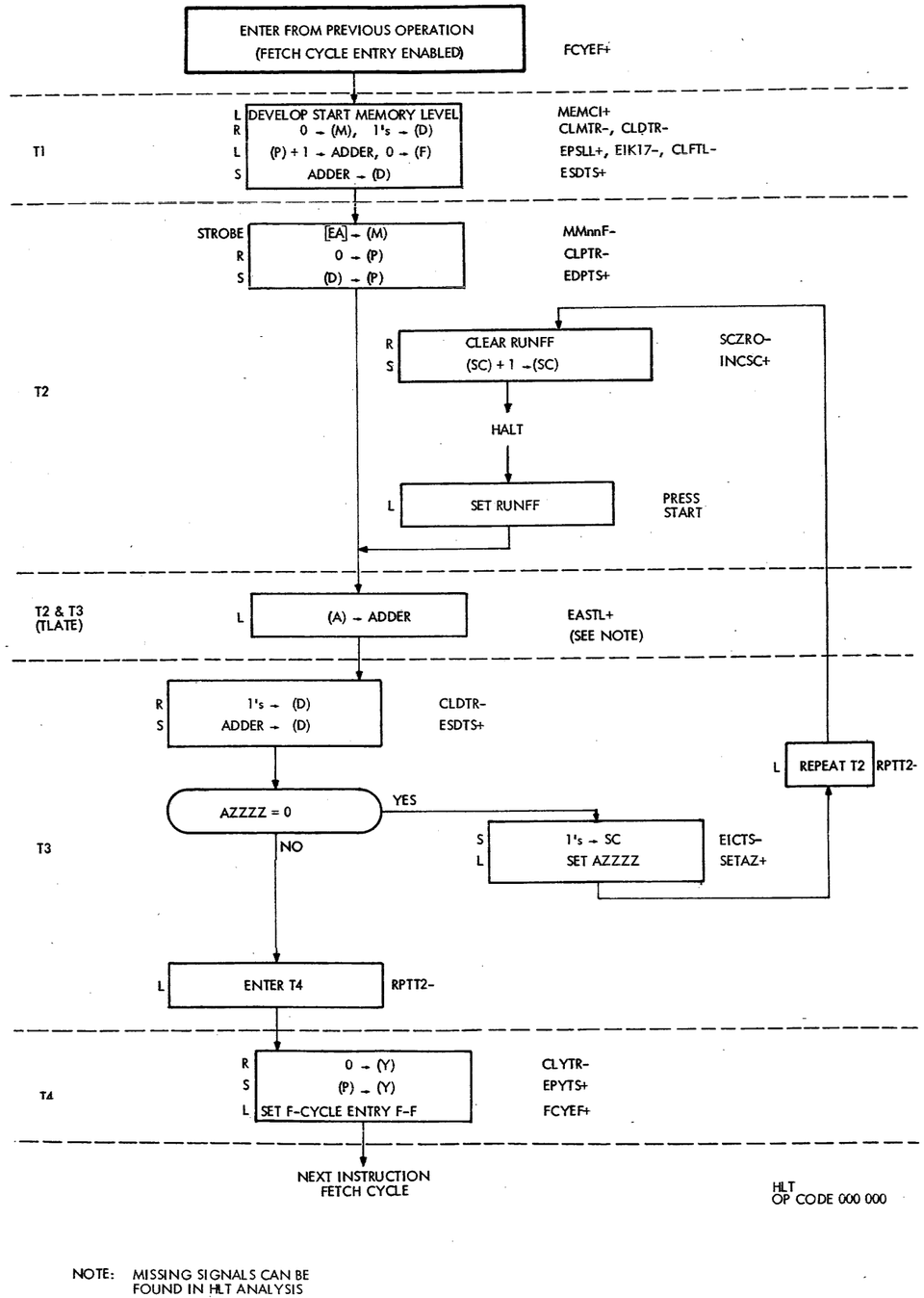
Description: Set machine status to permit interrupt

0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7-F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCRST+)	129–E7/L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCSET+)	129–E7/L10	101–116–J11	Enable D register to P register
PEMIL–	134–A4	F	TL4	L	(GENOB+)(TL4FF+)(M08FF+)	134–A4	134–C4	Permit interrupt
CLYTR–	129–P3	F	TL4	R	(SCZRO+)(TL4FF+)(MCRST+)	129–E1/H3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–) (IGACY+)	126–F12/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MCSET+)(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle

2-25 MISSING



NOTE: MISSING SIGNALS CAN BE FOUND IN HLT ANALYSIS

Instruction: Halt (HLT)

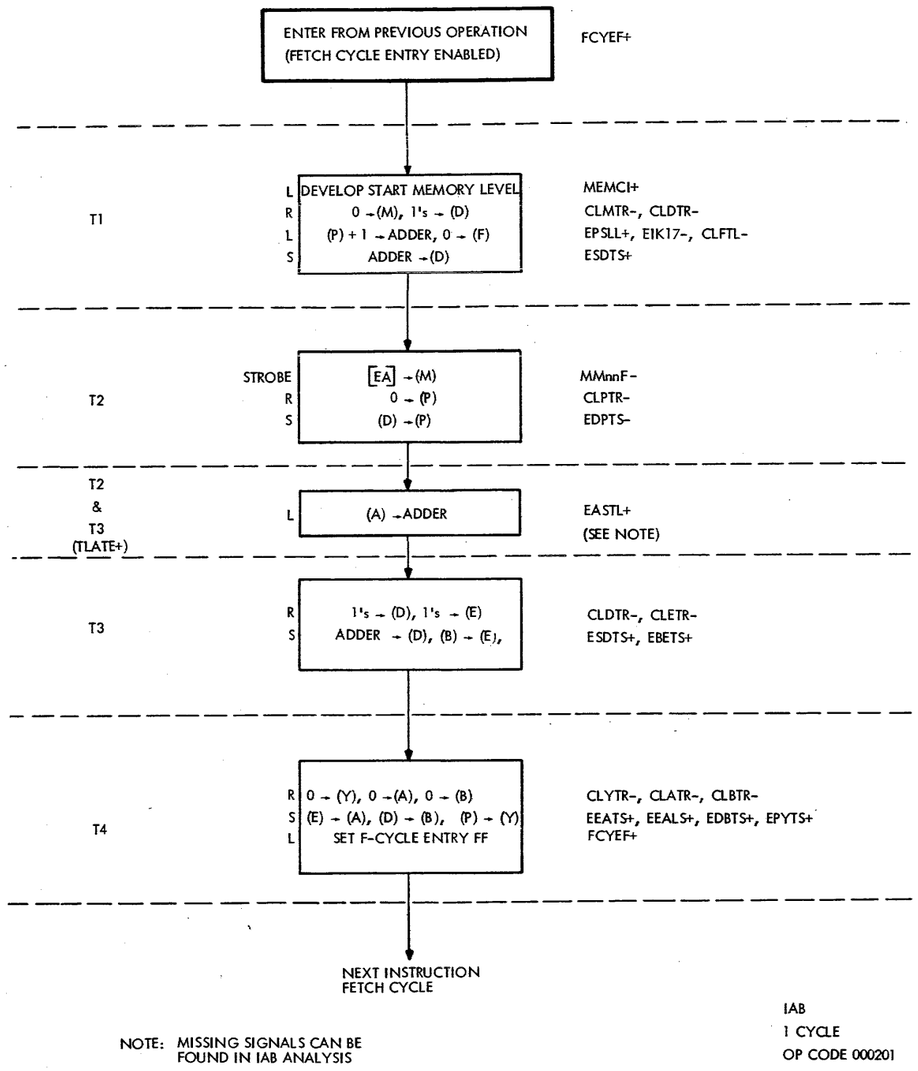
OP Code: 000000 **Type:** G, 1.5 cycles

Description: Set machine to halt mode

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs): 2.4

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7/F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	121–A5	Clear shift counter
							120–A1	Clear F register
							125–D8	Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnn F–	142				(SWnn±)(STRB–)	80,04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(EDPTR+)(MCRST+)	129–J9	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(EDPTR+)(MCSET+)	129–J9	101–116–J11	Enable D register to P register
EASTL+	127–P1	F	TLATE	L	(GENOP+)(TLATE+)(M01FF–)	127–C3	101–116–A4	Enable A register to adder
EMSHL+	127–P9	F	TLATE	L	(GENOP+)(TLATE+)(M01FF–)	127–K10	101–107–A9	Enable M(1-7) to adder
ENSHL+	127–P8	F	TLATE	L	(GENOP+)(TLATE+)(M01FF–)	127–K10	101–107–A10	Enable M–(1-7) to adder
EMSLL+	127–P11	F	TLATE	L	(GENOP+)(TLATE+)(M01FF–)	127–K10	108–116–A9	Enable M(8-16) to adder
ENSLL+	127–P7	F	TLATE	L	(GENOP+)(TLATE+)(M01FF–)	127–K10	108–116–A10	Enable M–(8-16) to adder
CLDTR–	125–K5	F	TL3	R	(TL3FF+)(ACYLF–)(MCRST+)	125–B6/J5	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5/J4	101–116–F5-F9	Enable adder sum to D register
EICTS–	125–K9	F	TL3	S	(GENOB+)(TL3FF+)(M16FF–)(MCSET+)(AZZZZ–)	125–B9/J9	121–A8	Set shift counter to all ONEs
							126–F10	Repeat TL2 (RPTT2+)
SETAZ+	125–M7	F	TL3	L	(GENOB+)(TL3FF+)(M16FF–)	125–B9	125–L8	Set AZZZZ FF
RUNFF–	126–M2	F	TL2	R	(MCRST+)(TL2FF+)(GENOB+)(M16FF–)(SCZRO–)(RESTR–)	126–J3	126–N2	Reset RUNFF
INCSC+	126–P5	F	TL2	L	(FCYEF+)(TL2FF+)	126–L5	121–A4	Enable increment shift counter
					Depress and release START button			
RUNFF+	126–M3				(RDYFF–)(START–)	126–D3	126–L3	Set RUNFF
					Repeat TLATE and TL3 with entry to TL4 (SCZRO+)(RPTT2–)			
CLYTR–	129–P3	F	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	129–H3/N3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(OPGJS–)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–)(IGACY+)	126–F2/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



Instruction: Interchange A and B (IAB)

OP Code: 000201 **Type:** Generic, 1 cycle

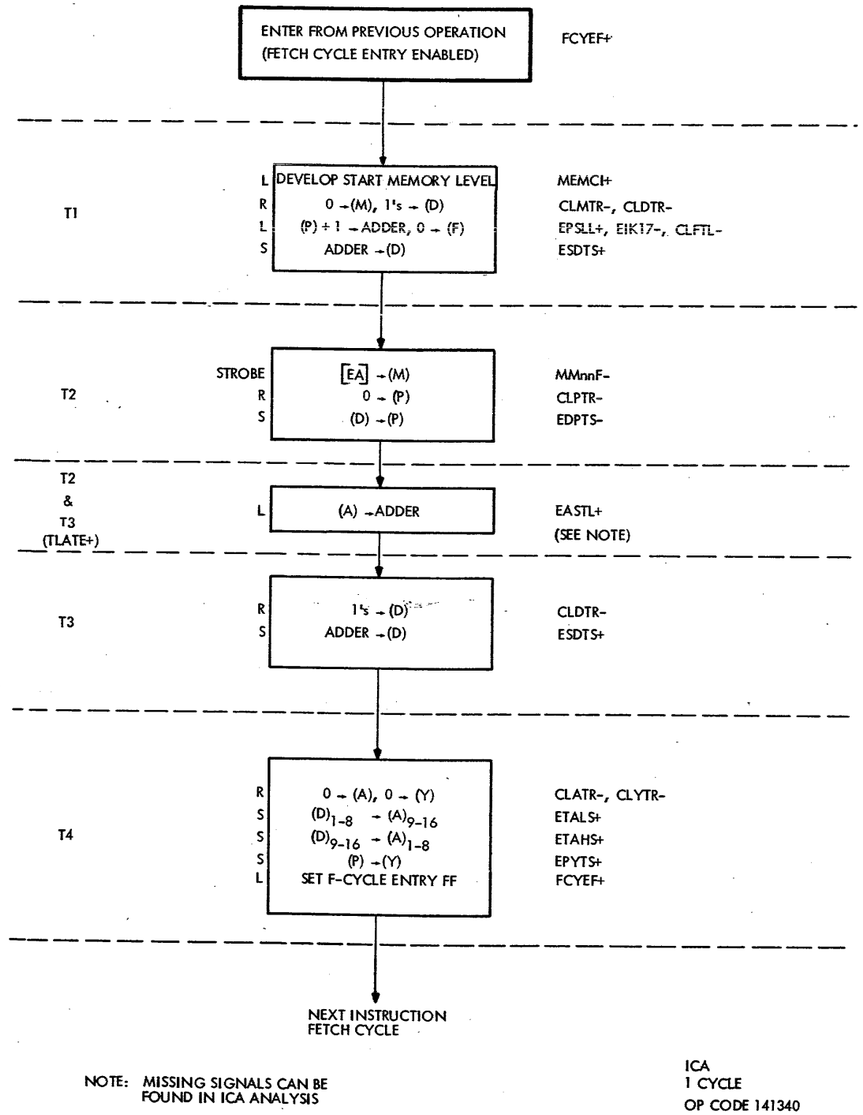
Description: (A) ⇌ (B)

0	0	c	b	a	a	0	0	1	0	0	0	0	0	0	1
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7/F9	Force carry-in to bit 16
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Reset M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Reset F register Reset shift counter Reset AZZZZ+ FF
ESDTS+	125–M4	F	TLATE	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnn F–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(EDPTR+)*	129–J9	101–116–L12	Reset P register
EDPTS+	129–P9	F	TL2	S	(EDPTR+)*	129–J9	101–116–J11	Enable D register into P register
EASTL+	127–P1	F	TLATE*		(GENOP+)(TLATE+)(M01FF–)	127–C3	101–116–A4	Enable A register to adder
EMSLL+	127–P11	F	TLATE*		(GENOP+)(TLATE+)(M01FF–)	127–K10	108–116–A9	Enable M(8-16) to adder
EMSHL+	127–P9	F	TLATE*		(GENOP+)(TLATE+)(M01FF–)	127–K10	101–107–A9	Enable M(1-7) to adder
ENSLL+	127–P7	F	TLATE*		(GENOP+)(TLATE+)(M01FF–)	127–K10	108–116–A10	Enable M–(8-16) to adder
ENSHL+	127–P8	F	TLATE*		(GENOP+)(TLATE+)(M01FF–)	127–10	101–107–A10	Enable M–(1-7) to adder
CLDTR–	125–K5	F	TL3	R	(TL3FF+)(ACYLF–)	125–B6	101–116–F11	Clear D register to ONEs
CLETR–	125–K2	F	TL3	R	(TL3FF+)(GENOP+)(M01FF–)(M09FF+)	125–B1/A1	101–116–N2	Reset E register
ESDTS+	125–M4	F	TL3	S	(TL3FF+)(IOGRP–)	125–B5	101–116–F5-F9	Enable adder sum into D register
EBETS+	125–M1	F	TL3	S	(TL3FF+)(GENOP+)(M01FF–)[(M09FF+) @ 125–A1]	125–B1	101–116–L3	Enable B register into E register
CLYTR–	129–P3	F	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	129–H3/N3	101–116–N12	Reset Y register
CLATR–	122–K8	F	TL4	R	(CLATL+)***	122–G6	101–116–L6	Reset A register
CLBTR–	123–M6	F	TL4	R	(M5G4G–)***	122–G2	101–116–L2	Reset B register
EEATS+	122–P4	F	TL4	S	(M5G4G–)***	122–G2	101–110–J4	Enable E(1-10) into A(1-10)
EEALS+	122–K5	F	TL4	S	(M5G4G–)***	122–G2	111–116–J4	Enable E(11-16) into A(11-16)
EDBTS+	123–P2	F	TL4	S	(M5G4G–)***	123–G2	101–116–J3	Enable D register into B register
FCYEF+	119–G10	F	TL4	L	(Set: (TL4FF+)(EOINS+))	119–C10	119–J10	Enable set FCYLF+ at next TL1FF+
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)	129–D4	101–116–L10	Enable P register into Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+) (SPMOD–) (IGACY+)	126–G11	150–A2	Enable set RCYF1+
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle

*EDPTR+ @ 129–J9 = (FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–) @ 129–E7
**TLATE+ = ((TL2FF–) V (TL3FF–)) @ 118–B7
***CLATL+ @ 122–F7 = (M5G4G–) @ 122–F6 = (GENOB+)(TL4FF+)(M09FF+) @ 123–F2



NOTE: MISSING SIGNALS CAN BE FOUND IN ICA ANALYSIS

ICA
1 CYCLE
OP CODE 141340

Instruction: Interchange Halves (ICA)

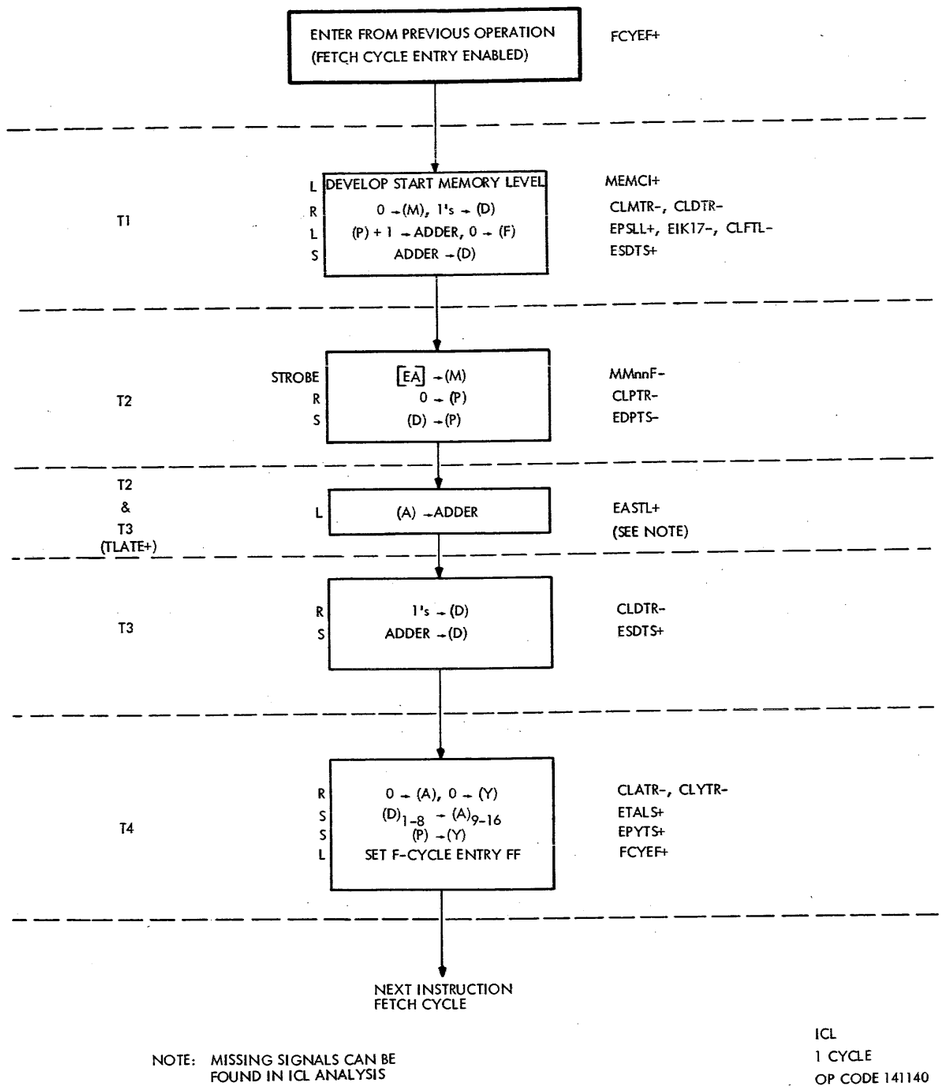
OP Code: 141340 **Type:** G, 1 cycle

Description: $(A)_{1-8} \rightarrow (A)_{9-16}$
$(A)_{9-16} \rightarrow (A)_{1-8}$

1	1	c	c	c	c	1	0	1	1	1	0	0	0	0	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7/F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
JAMKN–	127–L5	F	TL1	L	[(TLATE+)(ACYEF+)]–	127–C3	127–N5	Implement EIK17–
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	121–A5 120–A1	Clear shift counter Clear F register
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	125–D8 101–116–F5-F9	Clear AZZZZ FF Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(EDPTR+)(MCRST+)	129–J9/M10	101–116–L12	Clear P register
EDPTS–	129–P9	F	TL2	S	(EDPTR+)(MCSET+)	129–J9/M9	101–116–J11	Enable D register into P register
EASTL+	127–P1	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	129–C3	101–116–A4	Enable A register to adder
CLDTR–	125–K5	F	TL3	R	(TL3FF+)(ACYLF–)	125–P6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(TL3FF+)(IOGRP–)	125–B5	101–116–F5-F9	Enable adder sum to D register
EMSHL+	127–P9	F	TLATE+	L	(GENOP+)(TLATE+)(M02FF+)	127–K10	101–108–A9	Enable M(1-7) to adder
ENSHL+	127–P8	F	TLATE+	L	(GENOP+)(TLATE+)(M02FF+)	127–K10	101–108–A10	Enable M–(1-7) to adder
EMSLL+	127–P11	F	TLATE+	L	(GENOP+)(TLATE+)(M02FF+)	127–K10	109–116–A9	Enable M(8-16) to adder
ENSLL+	127–P7	F	TLATE+	L	(GENOP+)(TLATE+)(M02FF+)	127–K10	109–116–A10	Enable M–(8-16) to adder
JAMKN–	127–L5	F	TLATE+	L	(GENOP+)(M01FF+)(M02FF+)	127–L3	101–116–C9 117–C1-C4-K5	Force carry network to ZERO
CLATR–	122–K8	F	TL4	R	(GENOA+)(M11FF+)(TL4FF+)	122–C4	101–116–L6	Clear A register
CLYTR–	129–P3	F	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	129–H3	101–116–N12	Clear Y register
ETALS+	122–P7	F	TL4	S	(GENOA+)(M10FF+)(M11FF+)	122–C4/J7	109–116–J7	Enable D(1-8) into A(9-16)
ETAHS+	122–P6	F	TL4	S	(GENOA+)(M09FF+)(M11FF+)	122–C4/J6	101–108–J7	Enable D(9-16) into A(1-8)
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(OPGJS–)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL4FF+)(SPMOD–) (IGACY+)	126–F2/J12	150– A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



NOTE: MISSING SIGNALS CAN BE FOUND IN ICL ANALYSIS

ICL
1 CYCLE
OP CODE 141140

Instruction: Interchange and Clear Left Half (ICL)

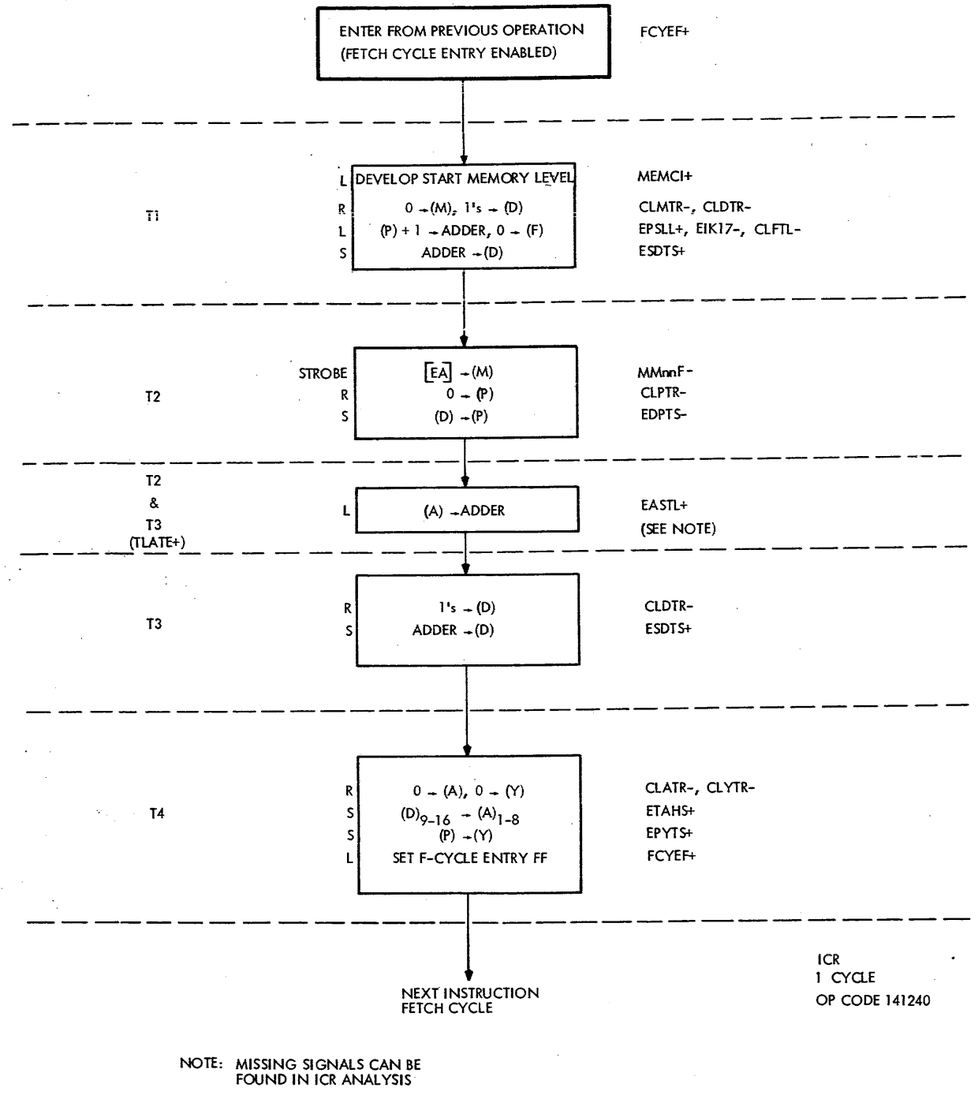
OP Code: 141140 **Type:** G, 1 cycle

Description: $(A)_{1-8} \rightarrow (A)_{9-16}$
$0 \rightarrow (A)_{1-8}$

1	1	1	0	0	0	1	0	0	1	1	0	0	0	0	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7-F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80,04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(EDPTR+)(MCRST+)	129–J9/M10	101–116–L12	Clear P register
EDPTS–	129–P9	F	TL2	S	(EDPTR+)(MCSET+)	129–J9/M9	101–116–J11	Enable D register into P register
ESDTS+	125–M4	F	TL3	S	(TL3FF+)(IOGRP–)	125–B5	101–116–F5-F9	Enable adder sum to D register
EMSHL+	127–P9	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K10	101–108–A9	Enable M(1-7) to adder
ENSHL+	127–P8	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K10	101–108–A10	Enable M–(1-7) to adder
EMSLL+	127–P11	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K10	109–116–A9	Enable M(8-16) to adder
ENSLL+	127–P7	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	127–K10	109–116–A10	Enable M–(8-16) to adder
JAMKN–	127–L5	F	TLATE	L	(GENOP+)(M01FF+)(M02FF+)	127–L3	101–116–C9 117–C1-C4-K5	Force carry network to ZERO
EASTL+	127–P1	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)	129–L3	101–116–A4	Enable A register to adder
CLDTR–	127–K5	F	TL3	R	(TL3FF+)(ACYLF–)	125–P6	101–116–F11	Clear D register to ONEs
CLATR–	122–K8	F	TL4	R	(GENOA+)(M11FF+)(TL4FF+)	122–C4	101–116–L6	Clear A register
CLYTR–	129–P3	F	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	129–H3	101–116–N12	Clear Y register
ETALS+	122–P7	F	TL4	S	(GENOA+)(M10FF+)(M11FF+)	122–C4/J7	109–116–J7	Enable D register (1-8) into A register (9-16)
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(OPGJS–)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–J11	F	TL1	L	(TL4FF+)(SPMOD–) (IGACY+)	126–F2/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



NOTE: MISSING SIGNALS CAN BE FOUND IN ICR ANALYSIS

Instruction: Interchange and Clear Right Half (ICR)

OP Code: 141240 **Type:** G, 1 cycle

Description: $(A)_{9-16} \rightarrow (A)_{1-8}$
$0 \rightarrow (A)_{9-16}$

1	1	0	0	0	0	1	0	1	0	1	0	0	0	0	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

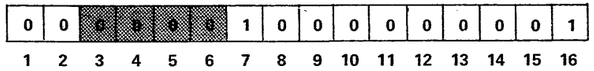
Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7/F9	Force carry to adder
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(EDPTR+)(MCRST+)	129–J9/M10	101–116–L12	Clear P register
EDPTS–	129–P9	F	TL2	S	(EDPTR+)(MCSET+)	129–J9/M10	101–116–J11	Enable D register into P register
EASTL+	127–P1	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–K12	101–116–A4	Enable A register to adder
EMSHL+	127–P9	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–K12	101–108–A9	Enable M(1-7) to adder
ENSHL+	127–P8	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–K12	101–108–A10	Enable M–(1-7) to adder
EMSLL+	127–P11	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–K12	109–116–A9	Enable M(8-16) to adder
ENSLL+	127–P7	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–K12	109–116–A10	Enable M–(8-16) to adder
CLDTR–	127–K5	F	TL3	R	(TL3FF+)(ACYLF–)	125–B6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(T03FF+)(IOGRP–)	125–B5	101–116–F5-F9	Enable adder sum to D register
CLATR–	122–K8	F	TL4	R	(GENOA+)(M11FF+)(TL4FF+)	122–C4	101–116–L6	Clear A register
ETAHS+	122–P6	F	TL4	S	(GENOA+)(M09FF+)(M11FF+)	122–C4/J6	101–108–J7	Enable D(9-16) into A(1-8)
CLYTR–	129–P3	F	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	129–H3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(OPGJS–)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–)(IGACY+)	126–F2/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle

Instruction: Inhibit Program Interrupt (INH)

OP Code: 001001 **Type:** G, 1 cycle

Description: Set machine status to inhibit interrupt



Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7/F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P8	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnn F–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCRST+)	129–E7/L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCSET+)	129–E7/L9	101–116–J11	Enable D register to P register
CLPMI	134–A5	F	TL3	S	(GENOB+)(M07FF+)(TL3FF+)(MCSET+)	134–A5	134–F5	Inhibit interrupt
CLYTR–	129–P3	F	TL4	R	(SCZRO–)(TL4FF+)(MCRST+)	129–E1-H3-N3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–) (IGACY+)	126–F2/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle

FCYEF+

MEMCI+
CLMTR–, CLDTR–
EPSLL+, EIK17–, CLFTL–
ESDTS+

MMnnF–
CLPTR–
EDPTS+

EASTL+ (SEE NOTE)

CLDTR–
ESDTS+

INKOP+
EEALS+
CLATR–, CLYTR–
EPYTS+

INK
1 CYCLE
OP CODE 000043

Instruction: Input Keys (INK)

OP Code: 000043 **Type:** G, 1 cycle

Description: (C) → A_1; (PM1) → A_3; 0 → (A)$_{4-11}$; (DP Mode) → A_2; Shift count → (A)$_{12-16}$

0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs): 1.6

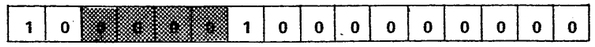
Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	TLATE–	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	TLATE–	L	(TLATE–)	127–K6	116–F7/F9	Force carry to adder
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Reset F register Reset shift counter Reset AZZZZ FF
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P8	101–116–L9	Reset M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)(MCRST+)	125–A6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)(MCSET+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCRST+)	129–E7/L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCSET+)	129–E7/L10	101–116–J11	Enable D register into P register
EASTL+	127–P1	F	TLATE	L	(GENOP+)(TLATE+)(M01FF–)	127–K10	101–116–A4	Enable A register to adder
EMSHL+	127–P9	F	TLATE	L	(GENOP+)(TLATE+)(M01FF–)	127–K10	101–107–A9	Enable M(1-7) to adder
ENSHL+	127–P8	F	TLATE	L	(GENOP+)(TLATE+)(M01FF–)	127–K10	101–107–A10	Enable M–(1-7) to adder
EMSLL+	127–P11	F	TLATE	L	(GENOP+)(TLATE+)(M01FF–)	127–K10	107–116–A9	Enable M(8-16) to adder
ENSLL+	127–P7	F	TLATE	L	(GENOP+)(TLATE+)(M01FF–)	127–K10	108–116–A10	Enable M–(8-16) to adder
CLDTR–	125–K5	F	TL3	R	(TL3FF+)(ACYLF–)(MCRST+)	125–B6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(ESDTB–)(MCSET+)	125–C5/J4	101–116–F5-F9	Enable adder sum to D register
INKOP+	122–P9	F	TL4	L	(GENOB+)(M11FF+)(M15FF+)(TL4FF+)	122–J9	101–103–N6	CB1TF into A_1 DPMOD into A_2 PMIND into A_3*
EEALS+**	122–K5	A	TL4	L	(GENOB+)(M11FF+)(TL4FF+)	122–C5	111–116–J4	Enable E(11-16) into A(11-16)
CLATR–**	122–K8	A	TL4	R	(GENOB+)(M11FF+)(TL4FF+)(MCRST+)	122–C5/J8	101–116–L6 124–N4	Clear A register
CLYTR–	129–P3	F	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	128–H3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(OPGJS–)(MCSET+)	129–D4/L4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–)(IGACY–)	126–F2/J12	150–C1	Enable set RCYF1+
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle

*Applicable only when computer is equipped with Memory Expansion Option.
**Applicable only when computer is equipped with high speed Arithmetic Unit Option.

Instruction: No Operation (NOP)

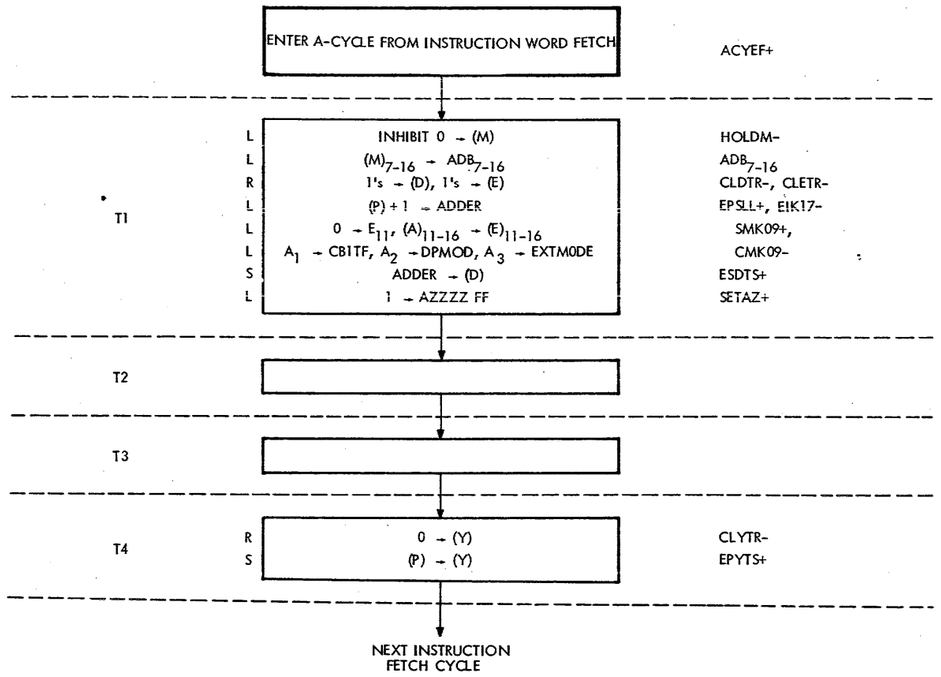
OP Code: 101000 **Type:** G, 1 cycle

Description: No operation



Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7-F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P8	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnn F–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCRST+)	129–E7/L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCSET+)	129–E7/L10	101–116–J11	Enable D register to P register
EPSLL+	128–K4				(SKGRP+)	128–J4	101–116–A9	Enable P register to adder
EIK17–	127–P5				(SKGRP+)	127–K6	116–F7-F9	Force carry to adder
CLDTR–	125–K5	F	TL3	R	(TL3FF+)(ACYLF–)(MCRST+)	125–B6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(IOGRP–)(TL3FF+)(MCSET+)	125–B5/J5	101–116–F5-F9	Enable adder sum to D register
CLYTR–	129–P3	F	TL4	R	(ACYLF–)(TL4FF+)(MCRST+)	129–E1/N3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)	129–D4/L4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–) (IGACY+)	126–F2/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



OTK
2 CYCLES
OP CODE 171020

Instruction: Output Keys (OTK)

OP Code: 171020 **Type:** I/O, 2 cycles

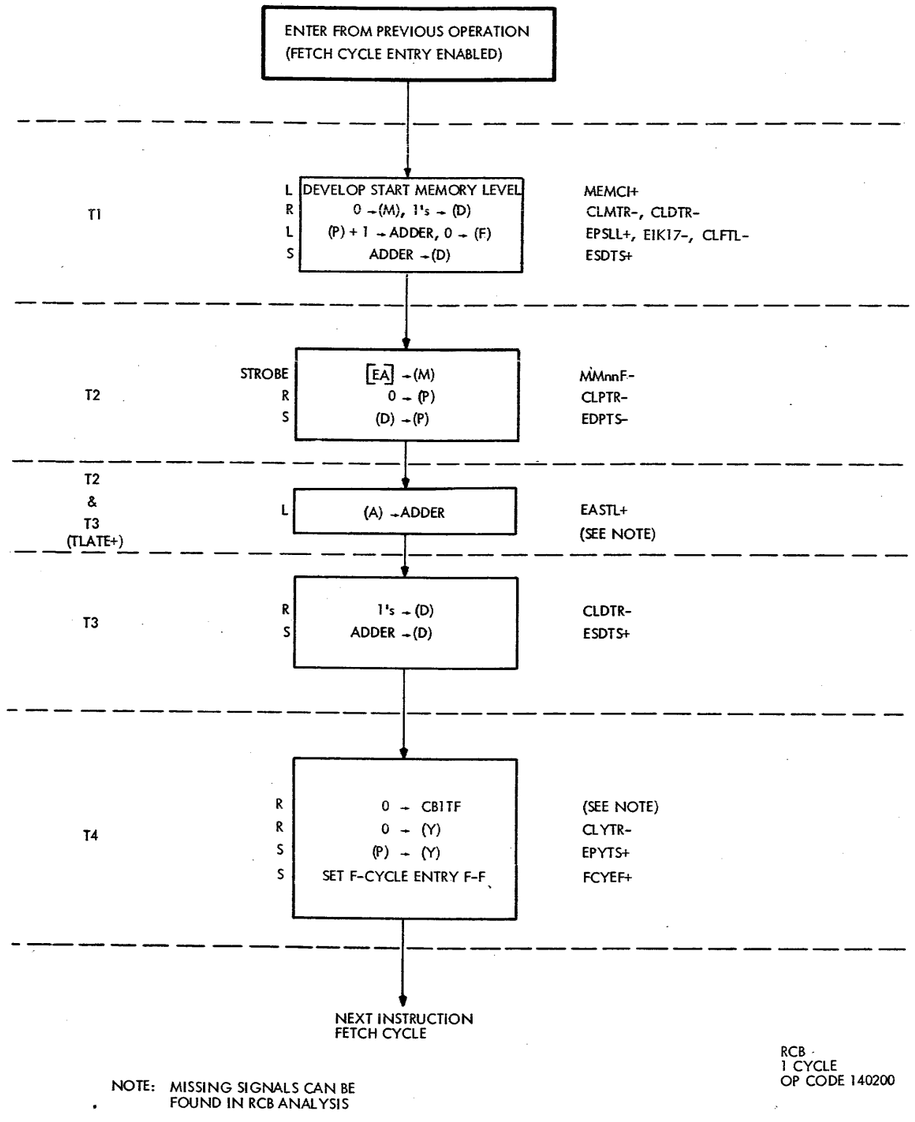
Description: $A_1 \rightarrow$ (C) $A_3 \rightarrow$ (Ext mode)
$A_2 \rightarrow$ (DP Mode) $0 \rightarrow E_{11}$
$(A)_{11-16}$ = Shift count $\rightarrow (E)_{11-16}$

1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	1	?	?	?	?	?	1	0	0	0	0	1	0	0	0	0

Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
ADB07-16	138–11				(DMCCY–)(M__FF+)	138–11	(See main frame wire list.)	
OTB01-16	138–B/F				(A01FF+) through (A16FF+)	138–C/J	(See main frame wire list.)	
EPSLL+	128–K4				(IOGRP+)	128–A5	101–116–A9	Enable P register to adder
SMK09+	122–M10				(SMKXX+)(FCX00+)(ADB07+)	122–J10	122–N8	Enable generate CMK09–
							111–P4	Reset E register bit 11
							112–116–P4	Enable A(11-16) into E(11-16)
							124–F2	Enable reset CB1TF
							136-K10/11	Set/Reset SEXTF*
HOLDM–	128–M9				(IOGRP+)(ACYEF+)	128–L9	128–N9	Inhibit M register clear
CLDTR–	125–K5	A	TL1	R	(ACYEF+)(TL1FF+)(JSTOP–)(IROSP–)(IMAOP–)(MCRST+)	125–B4/J5	101–116–F11	Clear D register to ONEs
EIK17–	127–P5	A	TL1	L	(ACYLF+)(SUBOP–)	127–A6/F7	116–F7-F9	Force carry to adder
							117–A1	
CMK09–	122–P8	A	TL1	L	(SMK09+)(TL1FF+)	122–N8	124–G2	Enable set CB1TF
							125–G2	Enable generate CLETR–
ESDTS+	125–M4	A	TL1	S	(ACYEF+)(TL1FF+)(JSTOP–)(IRSOP–)(IMAOP–)(MCSET+)	125–B4/J4	101–116–F5-F9	Enable adder sum to D register
SETAZ+	125–M7	A	TL1	L	(SMKXX–)	125–L7	125–D7	Set AZZZZ on trailing edge of MCSET
CLYTR–	129–P3	A	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	129–H3	101–116–N11	Clear Y register
EPYTS+	129–P4	A	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)(DMCRQ–)	129–D4/L4	101–116–L10	Enable P register into Y register
MEMCI+	126-K12	F	TL1	L	(TL1FF+) (SPMOD–) (IGACY+)	126-K12	150-K12	Enable Memory Cycle

*Applicable only when computer is equipped with memory expansion option.



NOTE: MISSING SIGNALS CAN BE FOUND IN RCB ANALYSIS

Instruction: Reset C to ZERO (RCB)

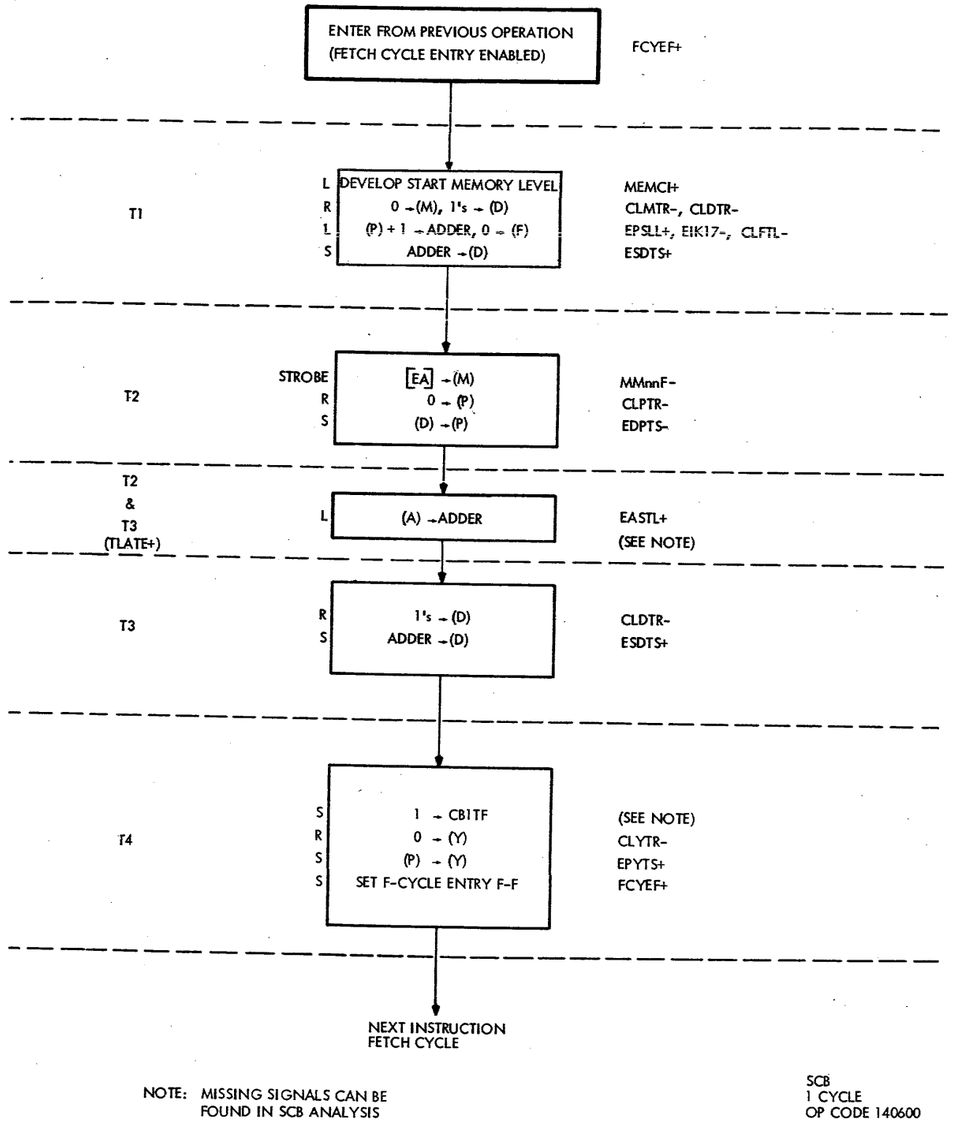
OP Code: 140200 **Type:** G, 1 cycle

Description: 0 → (C)

1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7-F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P8	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCRST+)	129–E7/L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCSET+)	129–E7/L10	101–116–J11	Enable D register to P register
EASTL+	127–P1	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–K12	101–116–A4	Enable A register to adder
JAMKN–	127–L4	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–G12/K12	101–116–C9 117–D/K	Jam carry network
EMSHL+	127–P9	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–G12/K12	101–107–A9	Enable M(1-7) to adder
ENSHL+	127–P8	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–G12/K12	101–107–A10	Enable M–(1-7) to adder
EMSLL+	127–P11	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–G12/K12	108–116–A9	Enable M(8-16) to adder
ENSLL+	127–P7	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–G12/K12	108–116–A10	Enable M–(8-16) to adder
CLDTR–	125–K5	F	TL3	R	(TL3FF+)(ACYLF–)(MCRST+)	125–B6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5	101–116–F5-F9	Enable adder sum to D register
CBITF	124–P2	F	TL4	R	(GENOA+)(M09FF+)(M11FF–)(TL4FF+)(DIVOP–)(MCRST+)	124–A3	124–P1	Reset CBITF
CLYTR–	129–P3	F	TL4	R	(SCZRO+)(TL4FF+)(MCRST+)	129–E1, H3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)	129–D4/L4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–)(IGACY+)	126–F2/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



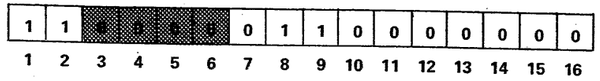
NOTE: MISSING SIGNALS CAN BE FOUND IN SCB ANALYSIS

SCB
1 CYCLE
OP CODE 140600

Instruction: Set C to ONE (SCB)

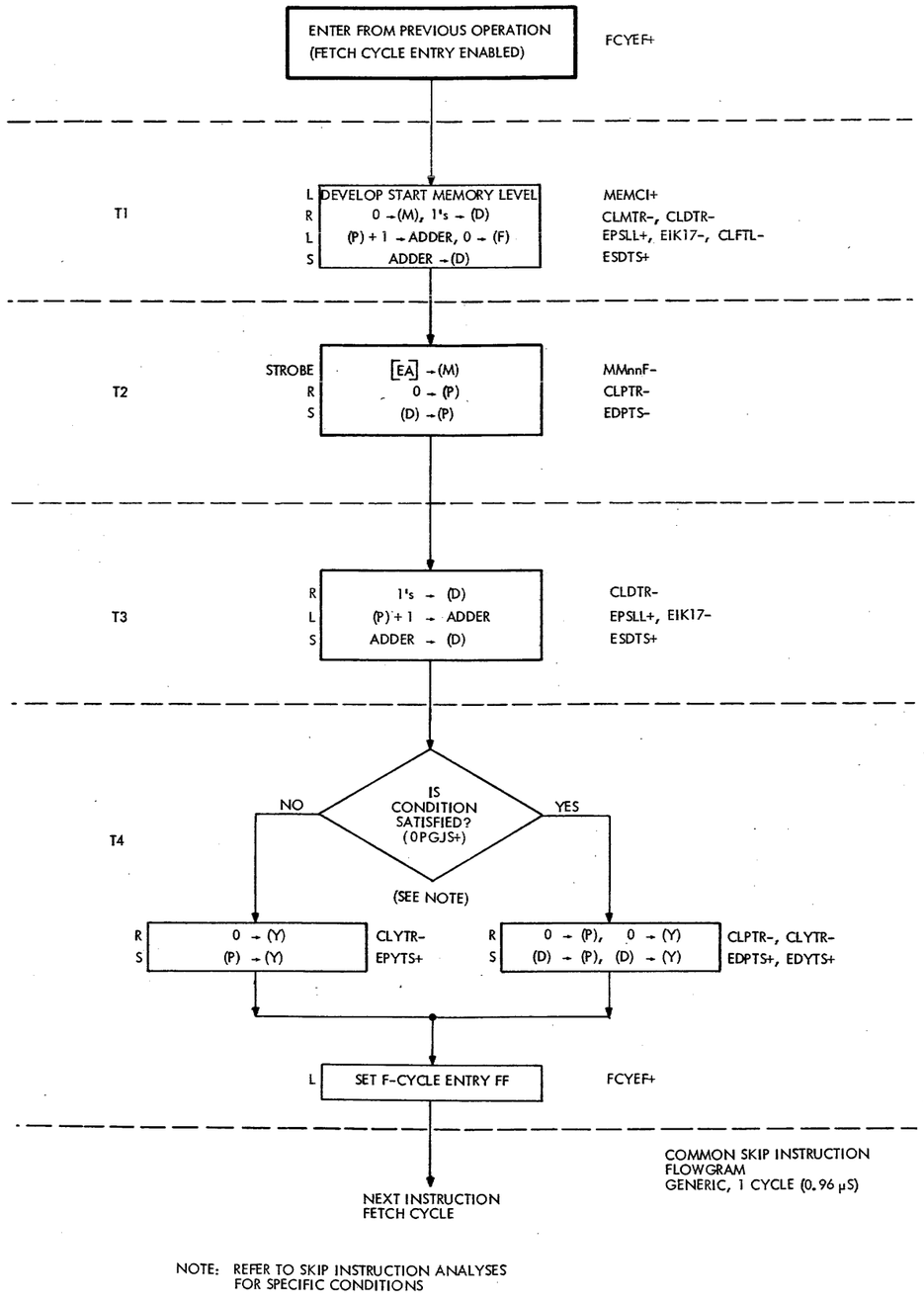
OP Code: 140600 **Type:** G, 1 cycle

Description: 1 → (C)



Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7-F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P8	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCRST+)	129–E7/L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCSET+)	129–E7/L10	101–116–J11	Enable D register to P register
EASTL+	127–P1	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–K12	101–116–A4	Enable A register to adder
JAMKN–	127–L4	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–G12/K12	101–116–C9 117–D/K	Jam carry network
EMSHL+	127–P9	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–G12/K12	101–107–A9	Enable M(1-7) to adder
ENSHL+	127–P8	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–G12/K12	101–107–A10	Enable M–(1-7) to adder
EMSLL+	127–D11	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–G12/K12	108–116–A9	Enable M(8-16) to adder
ENSLL+	127–P7	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(M09FF+)	127–G12/K12	108–116–A10	Enable M–(8-16) to adder
CLDTR–	125–K5	F	TL1	R	(TL3FF+)(ACYLF–)(MCRST+)	125–B6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5	101–116–F5-F9	Enable adder sum to D register
CB1TF	124–P2	F	TL4	S	(MCSET+)(GENOA+)(TL4FF+)(M08FF+)(M09FF+)	124–D6	124–P1	Set CB1TF
CLYTR–	129–P3	F	TL4	R	(SCZRO+)(TL4FF+)(MCRST+)	129–E1/H3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–) (IGACY+)	126–F2/J12	150–A2	Enable memory cycle
COXXX+	150-D2	F	TL1	L	(MEMCI+)(MBSYX+)	150–A2	150–D2	Start memory cycle



NOTE: REFER TO SKIP INSTRUCTION ANALYSES FOR SPECIFIC CONDITIONS

Common Entry and Exit for Skip Instructions

Instruction:

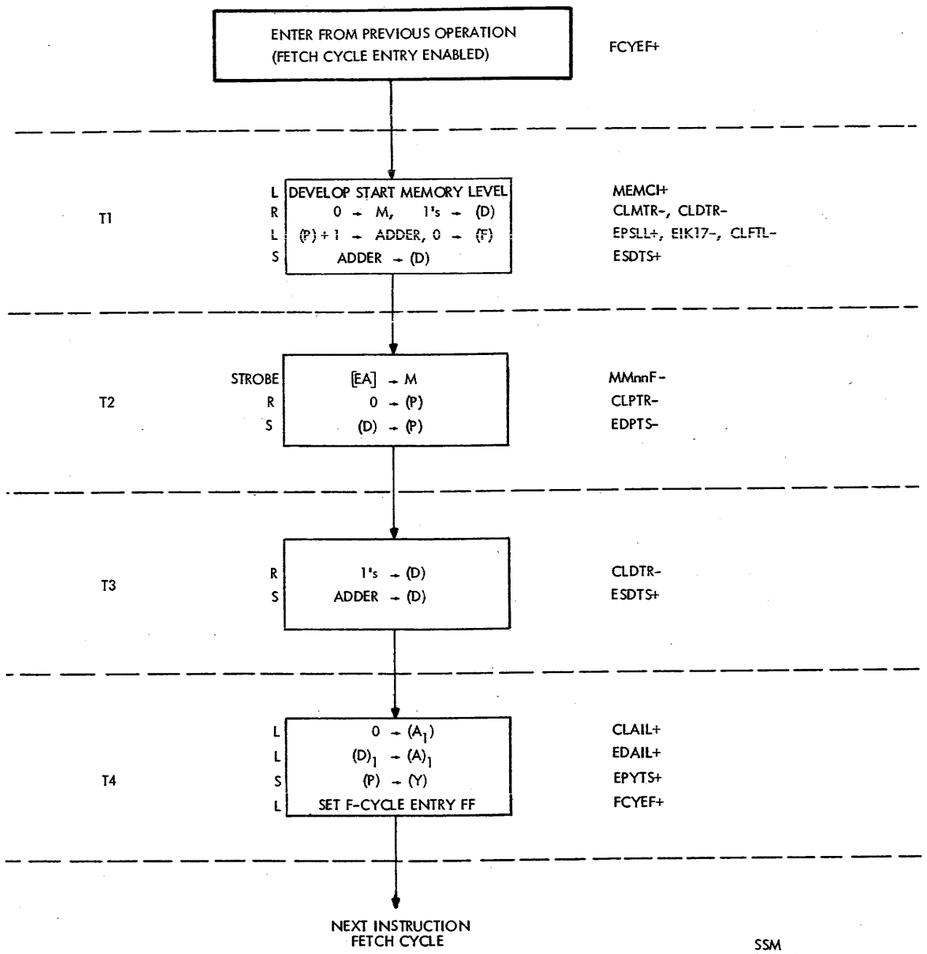
OP Code: **Type:**

Description:

1	0	e	e	e	f	X	X	X	X	X	X	X	X	X	X
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs):

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4				(SKGRP–)V(TLATE–) (FCYEF+)	128–F3/ J4	101–116–A9	Enable P register to adder
EIK17–	127–P5				(SKGRP–)V(TLATE–)	127–K6	116–F7-F9	Force carry to adder
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P8	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZRO+) (MEMAC–)(MCRST+)	129–E7/ L10	101–116–J10	Clear P register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF+)(SCZRO+) (MEMAC–)(MCSET+)	129–E7/ L10	101–116–J11	Enable D register to P register
CLDTR–	125–K5	F	TL3	R	(TL3FF+)(ACYLF–)(MCRST+)	125–B6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(IOGRP–)(TL3FF+)(MCSET+)	125–B5	101–116–F5-F9	Enable adder sum to D register
OPGJS+	129–M11				(See Table 2-1 for conditions)		129–D4–D8	Condition satisfied?
CLPTR–	129–M10	F	TL4	R	(OPGJS+)(EOINS+)(TL4FF+) (MCRST+)	129–E8/ L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL4	S	(OPGJS+)(EOINS+)(TL4FF+) (MCSET+)	129–E8/ L9	101–116–J11	Enable D register into P register
CLYTR–	129–P3	F	TL4	R	(ACYLF+)–(TL4FF+)(MCRST+)	129–E1/ H3	101–116–N12	Clear Y register
EDYTS+	129–P1	F	TL4	S	(ACYNX–)(MCSET+)(TL4FF+) (BRREQ–)(OPGJS–)	129–G1/ D4/F5	101–116–J10	Enable D register into Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+) (OPGJS–)(MCSET+)	129–E1/ H3	101–116–L10	Enable P register to Y register
MEMCI+	126–J11	F	TL1	L	(TL1FF+)(SPMOD–) (IGACY+)	126–F2/ J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



Instruction: Set Sign Minus (SSM)

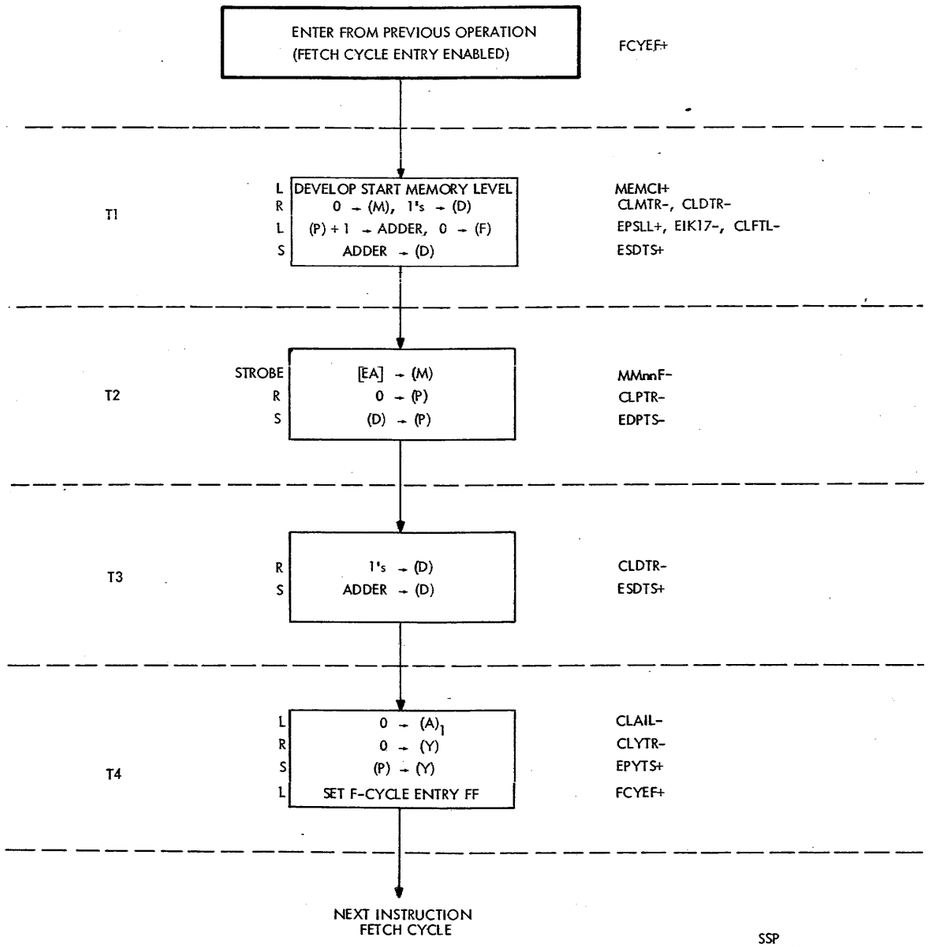
OP Code: 140500 **Type:** G, 1 cycle

Description: $1 \rightarrow (A)_1$

1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	TLATE	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	TLATE	L	(TLATE–)	127–K6	116–F7/F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCRST+)	129–E7/L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCSET+)	129–E7/L9	101–116–J11	Enable D register to P register
CLDTR–	125–K5	F	TL3	R	(TL3FF+)(ACYLF–)(MCRST+)	125–B6/J5	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5/J4	101–116–F5-F9	Enable adder sum to D register
CLAIL+	130–K11	F	TL4	L	(GENOA+)(TL4FF+)(M10FF+)	130–F11	101–L4	Clear A register bit 1
EDAIL+	130–K10	F	TL4	L	(GENOA+)(TL4FF+)(M08FF+)(M10FF+)	130–F10	101–L7	Enable D register bit 1 to A register bit 1
CLYTR–	129–P3	F	TL4	R	(SCZRO+)(TL4FF+)(MCRST+)	129–E1/H3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)	129–D4/L4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–) (IGACY+)	126–F12/J12	150–A2	Enable memory cycle
QOXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



SSP
1 CYCLE
OP CODE 140100

Instruction: Set Sign Plus (SSP)

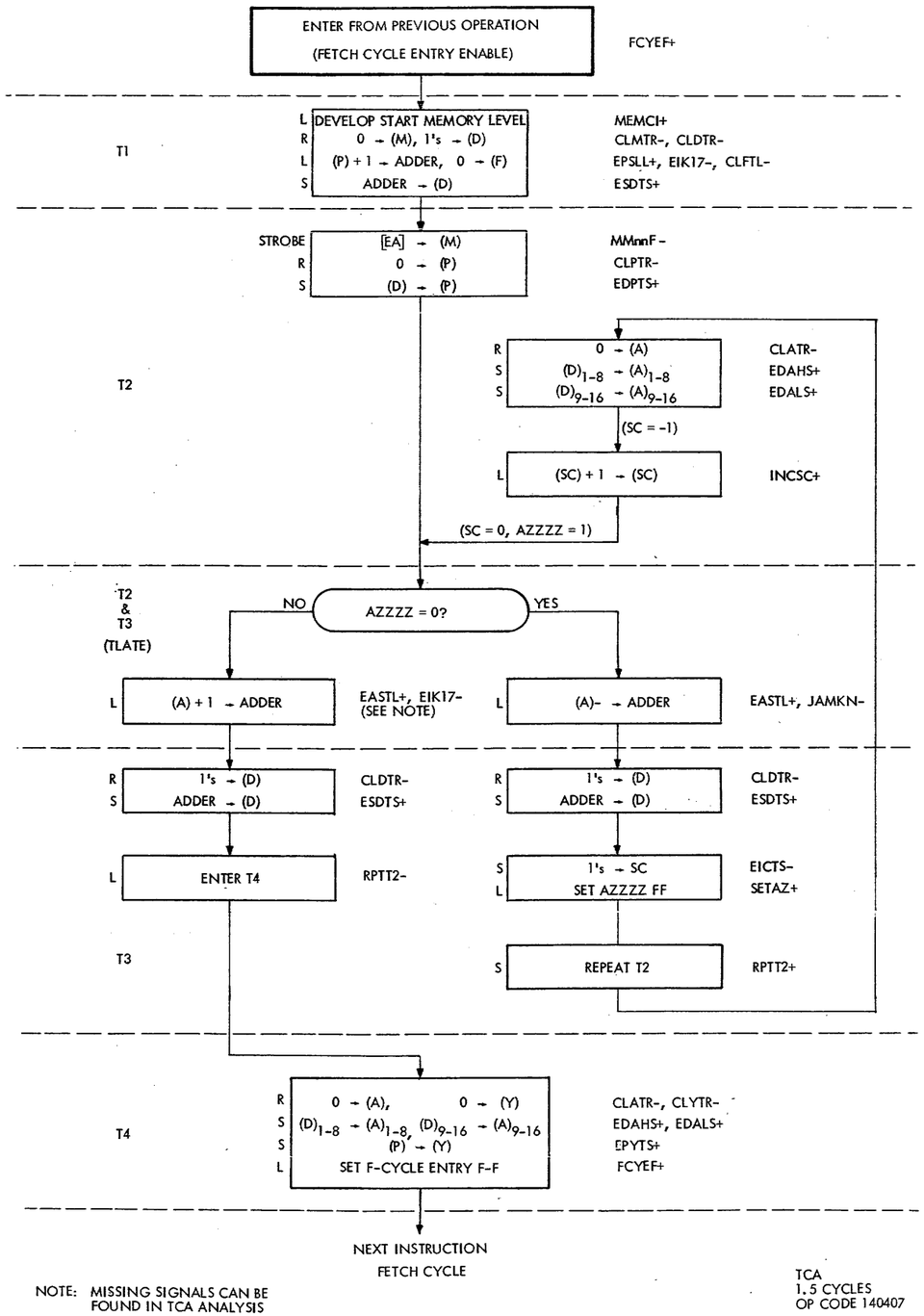
OP Code: 140100 **Type:** G, 1 cycle

Description: $0 \rightarrow (A)_1$

1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7-F9	Force carry to adder
CLMTR–	129–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCRST+)	129–E7/L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCSET+)	129–E7/L9	101–116–J11	Enable D register to P register
CLAIL+	130–K11	F	TL4	L	(GENOA+)(TL4FF+)(M10FF+)	130–F11	101–L4	Clear A register bit 1
CLYTR–	129–P3	F	TL4	R	(SCZRO+)(TL4FF+)(MCRST+)	129–E1/H3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)	129–D4/L4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–) (IGACY+)	126–F12/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



NOTE: MISSING SIGNALS CAN BE FOUND IN TCA ANALYSIS

TCA
1.5 CYCLES
OP CODE 140407

Instruction: Two's Complement of A (TCA)

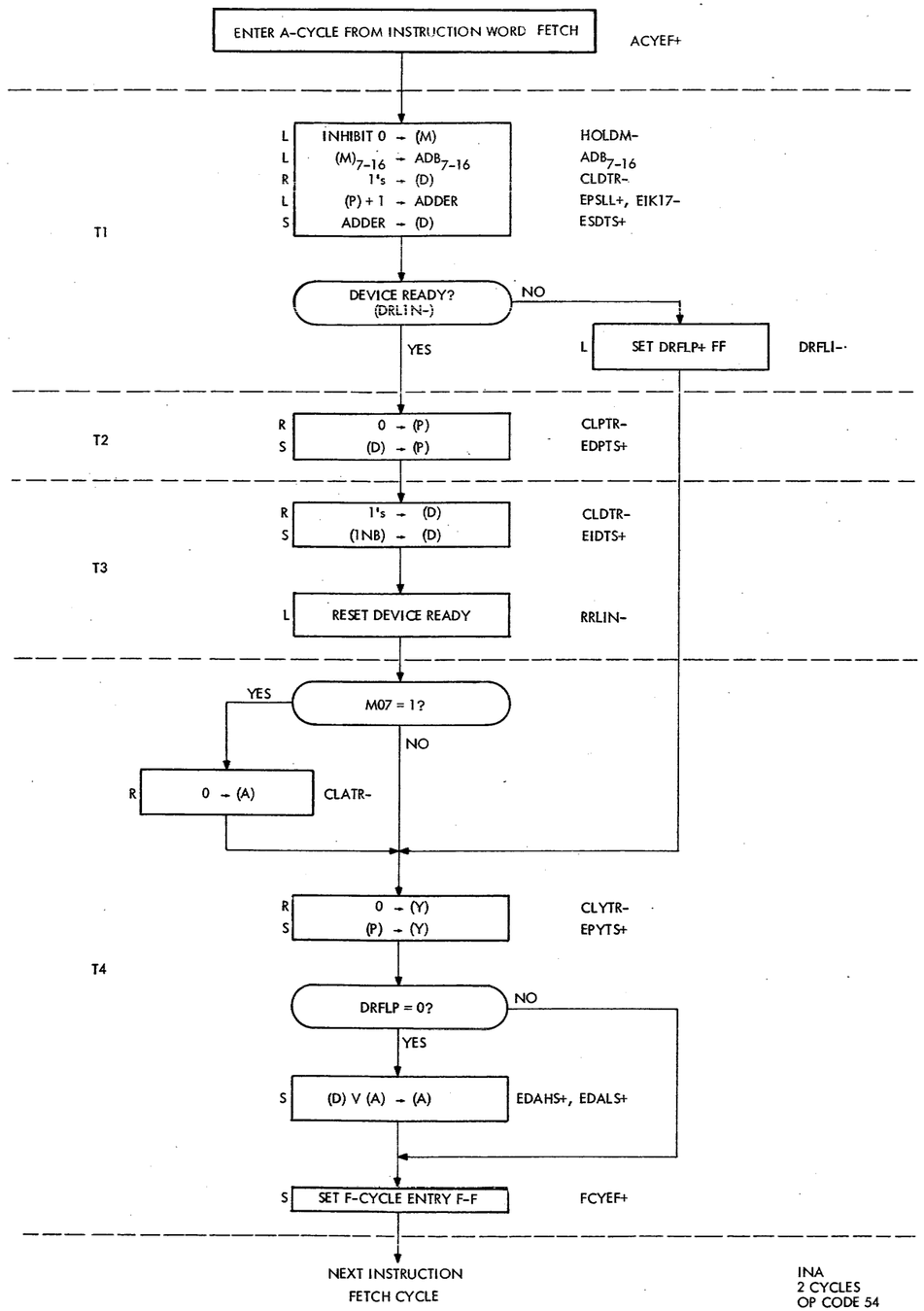
OP Code: 140407 **Type:** G, 1.5 cycles

Description: Two's Complement of (A) → (A)

1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs): 2.4

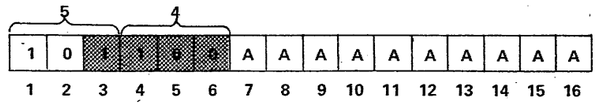
Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7-F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P8	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCRST+)	129–E7/L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCSET+)	129–E7/L10	101–116–J11	Enable D register to P register
EASTL+	127–P1	F	TLATE	L	(AZZZZ–)(TLATE+)(GENOP+)(M16FF+)(M02FF+)(M01FF+)	127–C3	101–116–A4	Enable A register to adder
JAMKN–	127–L4	F	TLATE	L	(AZZZZ–)(TLATE+)(GENOP+)(M16FF+)(M02FF+)(M01FF+)	127–C3	101–116–C9 117 D/K	Jam carry network
CLDTR–	125–K5	F	TL3	R	(TL3FF+)(ACYLF–)(MCRST+)	125–B6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5	101–116–F5-F9	Enable adder sum to D register
SETAZ+	125–M7	F	TL3	L	(GENOA+)(TL3FF+)(M08FF+)(M15FF+)	125–A8	125–L8	Set AZZZZ FF
EICTS–	125–K9	F	TL3	S	(GENOA+)(TL3FF+)(M08FF+)(M15FF+)(AZZZZ–)(MCSET+)	125–A9/J9	121–A8 126–F5	Set shift counter to all ONEs generate RPTT2+
RPTT2+	126–G5	F	TL3	S	EICTS–	126–G4	126–G4	Repeat T2
CLATR–	122–K8	F	TL2	R	(GENOA+)(TL2FF+)(AZZZZ+)(MCRST+)	122–A5/H7	101–116–L6	Clear A register
EDAHS+	122–P1	F	TL2	S	[(GENOA+)(TL2FF+)(AZZZZ+)	122–A4/	101–108–J7	Enable D(1-8) into A(1-8)
EDALS+	122–P3	F	TL2	S	└ (MCSET+)]	J1	109–116–J7	Enable D(9-16) into A(9-16)
INCSC+	126–P5	F	TL2	L	(FCYEF+)(TL2FF+)	126–J5	121–A4	Increment shift counter
EASTL+	127–P1	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(AZZZZ+)	127–K10	101–116–A4	Enable A register to adder
EMSHL+	127–P9	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(AZZZZ+)	127–K10	101–107–A9	Enable M(1-7) to adder
ENSHL+	127–P8	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(AZZZZ+)	127–K10	101–107–A10	Enable M–(1-7) to adder
EMSLL+	127–P11	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(AZZZZ+)	127–K10	108–116–A9	Enable M(8-16) to adder
ENSLL+	127–P7	F	TLATE	L	(GENOP+)(TLATE+)(M02FF+)(AZZZZ+)	127–K10	108–116–A10	Enable M–(8-16) to adder
EIK17–	127–P5	F	TLATE	L	(JAMKN–)	127–L4	116–F7	Force carry to adder
CLATR–	122–K8	F	TL4	R	(GENOA+)(M16FF+)(TL4FF+)	122–A2	101–116–L6	Clear A register
EDAHS+	122–P1	F	TL4	S	(GENOA+)(M16FF+)(TL4FF+)	122–A2	101–108–J7	Enable D(1-8) into A(1-8)
EDALS+	122–P3	F	TL4	S	(GENOA+)(M16FF+)(TL4FF+)	122–A2	109–116–J7	Enable D(9-16) into A(9-16)
CLYTR–	129–P3	F	TL4	R	(SCZRO+)(TL4FF+)(MCRST+)	129–E1/H3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–) (IGACY+)	126–F12/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle



Instruction: Input to A (INA)

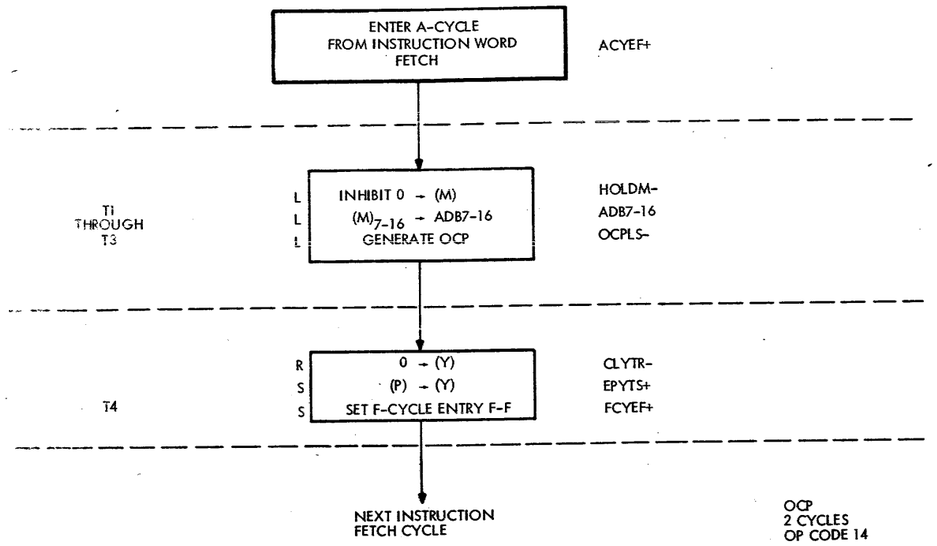
OP Code: 54 **Type:** I/O, 2 cycles

Description: (INB) → (A), $(IW)_7 = 1$
(INB) V (A) → (A), $(IW)_7 = 0$



Execution Time (μs): 3.2

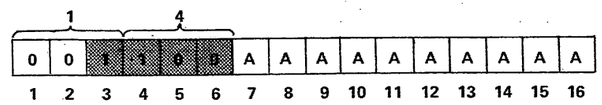
Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
MEMCI–	126–G12	F	TL4	L	(IOGRP+)(ACYEF+)	126–C12	126–J12	Block start memory
HOLDM–	128–M9	A			(IOGRP+)(ACYEF+)	128–L9	128–N9	Inhibit M register clear
ADB7-16	138–9/10	A			(ADBST–)(M__FF+)	138–A9	143–XX	(See main frame wire list)
CLDTR–	125–K5	A	TL1	R	(ACYEF+)(TL1FF+)(JSTOP–)(IRSOP–)(IMAOP–)(MCRST+)	125–B4	101–116–F11	Clear D register to ONEs
EPSLL+	128–K4	A	TL1	L	(IOGRP+)	128–A5	101–116–A9	Enable P register to adder
EIK17–	127–P5	A	TL1	L	(TLATE–)	127–K6	116–F7-F9 117–A1	Force carry to adder
ESDTS+	125–M4	A	TL1	S	(ACYEF+)(TL1FF+)(JSTOP–)(RISOP–)(IMAOP–)(MCSET+)	125–B4	101–116–F5-F9	Enable adder sum to D register
DRLIN–	143–B3	A			Function of IO option		125–D10	Device ready line
DRFLP–	125–E10	A	TL1	S	(DRFL1–)	125–L11	125–E10	Reset DRFLP+
DRFLP+	125–E9	A	TL1	L	(SMKXX–)	134–G9	125–D9	Set DRFLP+
CLPTR–	129–M10	A	TL2	R	(TL2FF+)(IOGRP+)(DRFLP–)(OCPLS–)(MCRST+)	129–E6	101–116–L12	Clear P register
EDPTS+	129–P9	A	TL2	S	(TL2FF+)(IOGRP+)(DRFLP–)(OCPLS–)(MCSET+)	129–E6	101–116–J11	Enable D register to P register
CLDTR–	125–K5	A	TL3	R	(ANAOP–)(TL3FF+)(MCRST+)	125–B7	101–116–F11	Clear D register to ONEs
EIDTS+	125–P6	A	TL3	S	(MCSET+)(RRLIN–)	125–L6	101–116–F4	Enable INB_{1-16} to D register
RRLIN†	134–P10	A	TL24	L	(M01FF+)(TL24F+)(DRFLP–)	134–J10	143–D5	Reset ready to device
CLATR–	122–K8	A	TL4	R	(ACYLF+)(TL4FF+)(IOGRP+)(DRFLP–)(M02FF–)(M07FF+)(M01FF+)(MCRST+)	122–C6	101–116–L6	Clear A register if $1W_7 = 1$
EDAHS+	122–P1	A	TL4	S	(ACYLF+)(TL4FF+)(IOGRP+)(DRFLP–)(M01FF+)(M02FF–)(MCSET+)	122–C1	101–108–J7	Enable D register to A(1-8)
EDALS+	122–P3	A	TL4	S	(DRFLP–)(M01FF+)(M02FF–)(MCSET+)(ACYLF+)(TL4FF+)(IOGRP+)	122–C1	109–116–J7	Enable D register to A(9-16)
CLYTR–	129–P3	A	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	129–H3/N3	101–116–N12	Clear Y register
EPYTS+	129–P4	A	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)(DMCRQ–)	129–D4/L4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	A	TL1	L	(TL1FF+)(SPMOD–)(IGACY+)	126–F12/J12	150– A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150– A2	150–D2	Start memory cycle



Instruction: Output Control Pulse (OCP)

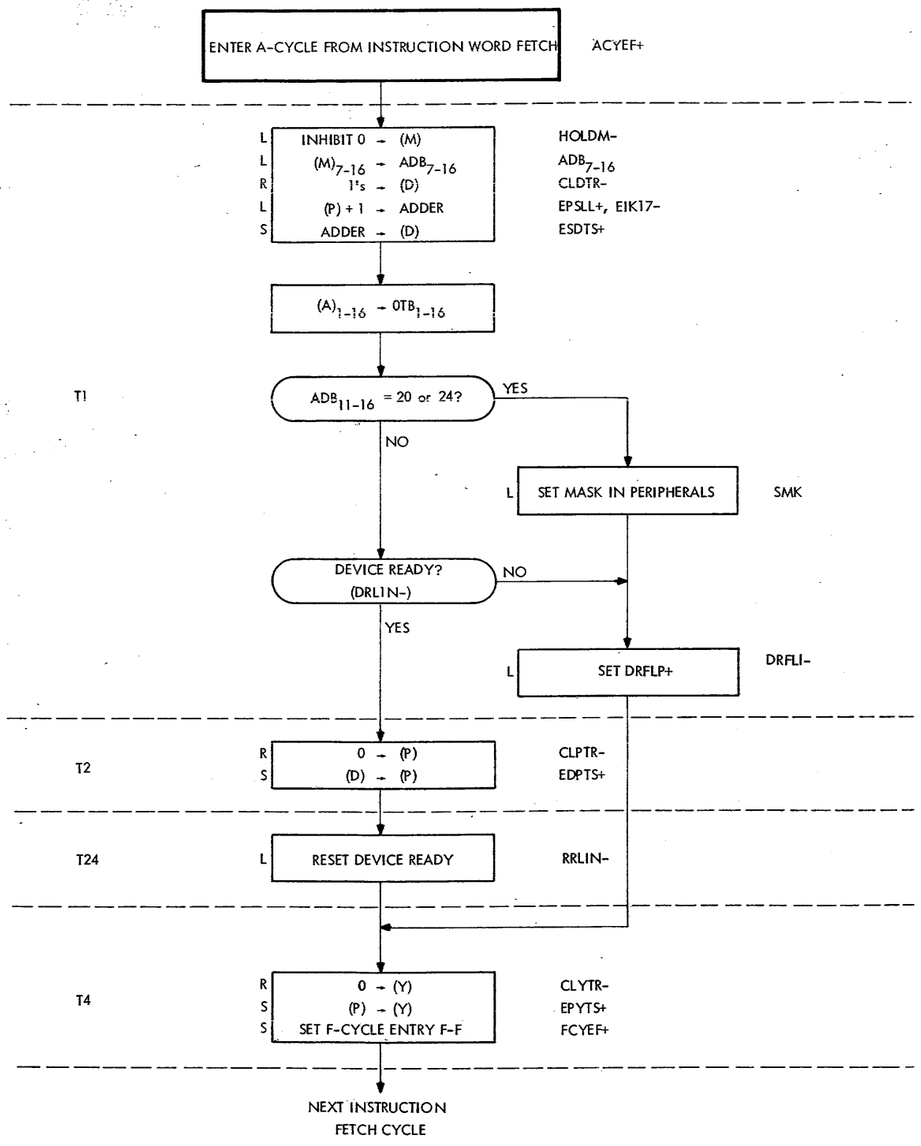
OP Code: 14 **Type:** I/O, 2 cycles

Description: Set or reset function of specified device



Execution Time (μs): 3.2

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
MEMCI-	126–G12	F	TL4	L	(IOGRP+)(ACYEF+)	126–C12	126–J12	Block start memory
HOLDM-	128–M9				(IOGRP+)(ACYEF+)	128–L9	128–N9	Inhibit M register clear
ADB7-16	138–9/10				(ADBST-)(M__FF+)	138–9		(See main frame wire list)
OCPLS-	134–N11				(RESTR-)(ACYEF-)(IOGRP+) (M01FF-)(M02FF-)	134–A11/ F11	143–B4	Control pulse to device
CLYTR-	129–P3	A	TL4	R	(ACYNX-)(TL4FF+)(MCRST+)	129–H3/ N3	101–116–N12	Clear Y register
EPYTS+	129–P4	A	TL4	S	(PISEX-)(EOINS+)(TL4FF+) (OPGJS-)(MCSET+)(DMCRQ-)	129–D4/ L4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	A	TL1	L	(TL1FF+)(SPMOD-) (IGACY+)	126–F12/ J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX-)	150–A2	150–D2	Start memory cycle



OTA/SMK
2 CYCLES
OP CODE 74

Instruction: Output from A (OTA)

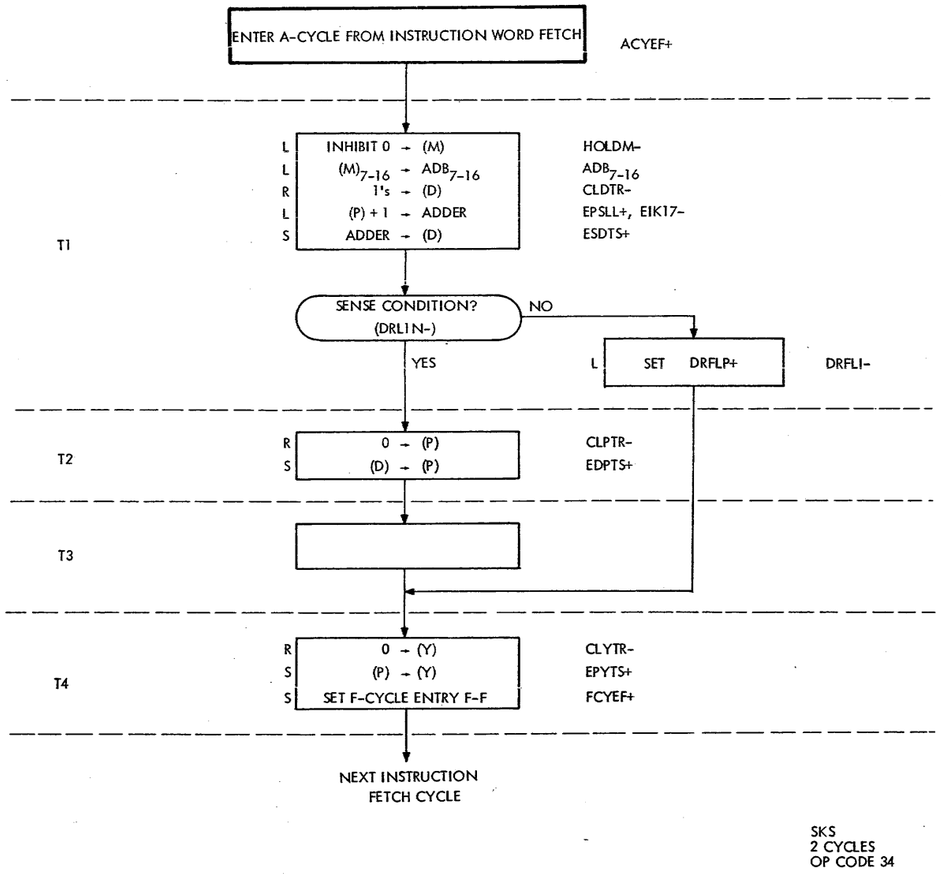
OP Code: 74 **Type:** I/O, 2 cycles

Description: If ready: (A) → (OTB) and skip
If not ready: No output and no skip

7			4													
1	1	1	1	0	0	0	A	A	A	A	A	A	A	A	A	A
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Execution Time (μs): 3.2

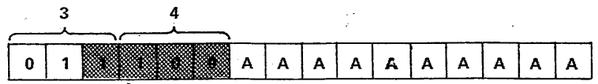
Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
MEMCI-	126–G12	F	TL4	L	(IOGRP+)(ACYEF+)	126–L12	126–K12	Block start memory
HOLDM-	128–M9	A			(IOGRP+)(ACYEF+)	128–L9	128–N9	Inhibit M register clear
EPSLL+	128–K4				(IOGRP+)	128–A5	101–116–A9	Enable P register to adder
EIK17-	127–P5	A	TL1	L	(TLATE-)	127–K6	116–F7-F9 117–A1	Force carry to adder
ADB7-16	138–9/10	A			(ADBST-)(M FF+)	138–A9	(See main frame wire list)	
CLDTR-	125–K5	A	TL1	R	(ACYEF+)(TL1FF+)(JSTOP-) (IRSOP-)(IMAOP-)(MCRST+)	125–B4	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	A	TL1	S	(ACYEF+)(TL1FF+)(JSTOP-) (IRSOP-)(IMAOP-)(MCSET+)	125–B4	101–116–F5-F9	Enable adder sum to D register
OTB01-16	138–B/F	A			(A01FF+) through (A16FF+)	138–A/E	(See main frame wire list)	
SMK01+	134–K12	A			(SMKXX+)(ADB07-)(FCX00+)	134–F12	143–B5	ADB 7-16 = 0020_8 (Set mask)
DRLIN-	143–B3	A			Function of I/O option		125–B11	Device ready line
DRFLP-	125–E10	A	TL1	S	(DRFL1-)	125–G11	125–G10	Reset DRFLP+
DRFLP+	125–E9	A	TL1	L	(SMKXX-)	125–G9	125–D9	Set DRFLP+
CLPTR-	129–M10	A	TL2	R	(TL2FF+)(IOGRP+)(DRFLP-) (OCPLS-)(MCRST+)	129–E6	101–116–L12	Clear P register
EDPTS+	129–P9	A	TL2	S	(TL2FF+)(IOGRP+)(DRFLP-) (OCPLS-)(MCSET+)	129–E6	101–116–J11	Enable D register to P register
RRLIN-	134–P10	A	TL24	L	(M01FF+)(TL24F+)(DRFLP-)	134–J10	143–D5	Reset ready to device
CLYTR-	129–P3	A	TL4	R	(ACYNX-)(TL4FF+)(MCRST+)	129–H3/N3	101–116–N12	Clear Y register
EPYTS+	129–P4	A	TL4	S	(PISEX-)(EOINS+)(TL4FF+) (OPGJS-)(MCSET+)(DMCRQ-)	129–D4/L4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	A	TL1	L	(TL4FF+)(SPMOD-) (IGACY+)	126–F12/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX-)	150–A2	150–D2	Start memory cycle



Instruction: Skip if Ready Line Set (SKS)

OP Code: 34 **Type:** I/O, 2 cycles

Description: If f (device) is satisfied, device is ready and next instruction is skipped.



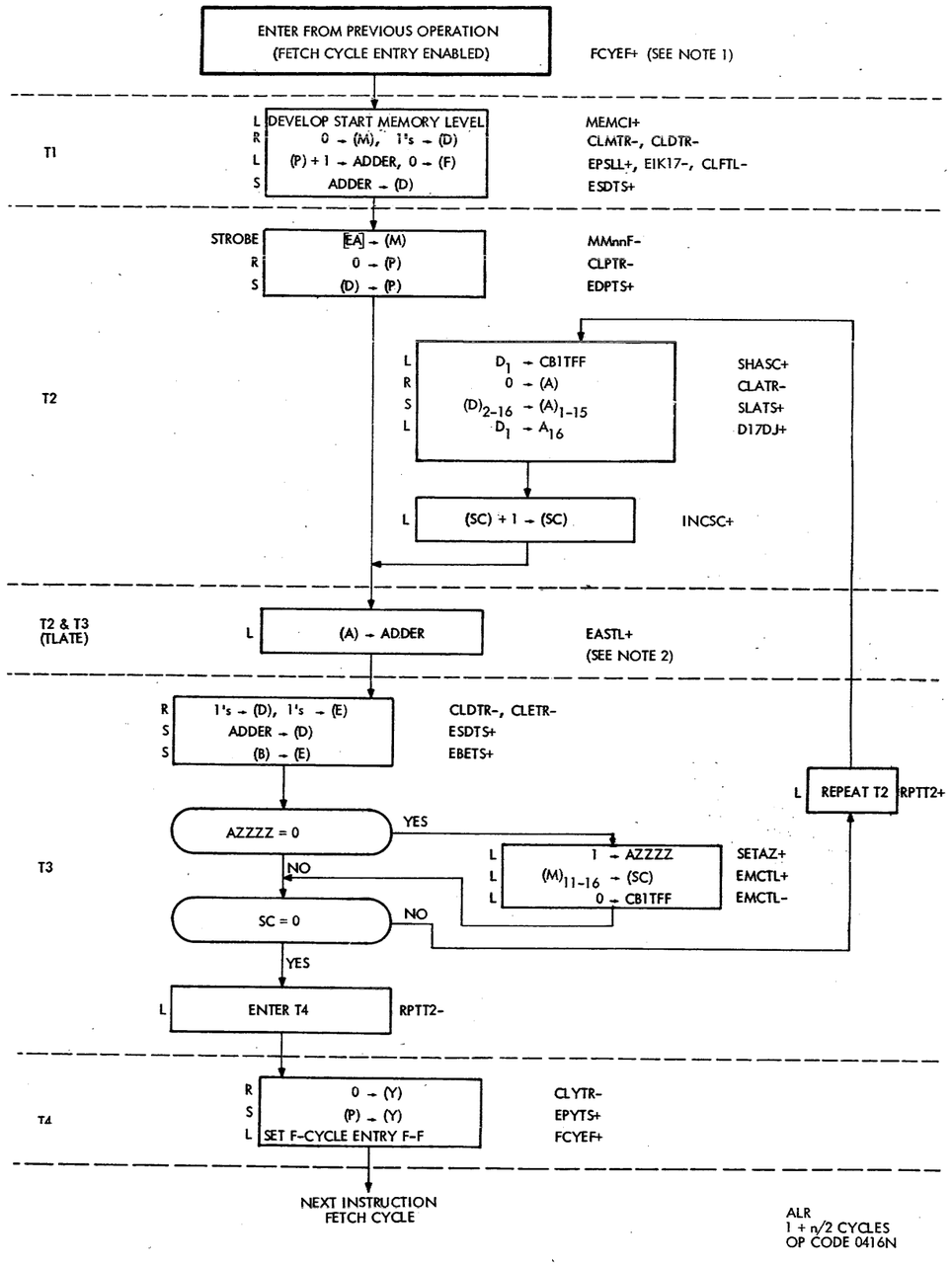
Execution Time (μs): 3.2

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
HOLDM–	128–M9	A			(IORGP+)(ACYEF+)	128–L9	128–N9	Inhibit M register clear
ADB7-16	128–9/10	A			(ADBST–)(M___FF+)	138–P9	(See main frame wire list.)	
CLDTR–	125–K5	A	TL1	R	(ACYEF+)(TL1FF+)(JSTOP–)(IRSOP–)(IMAOP–)(MCRST+)	125–B4	101–116–F11	Clear D register to ONEs
EPSLL+	128–K4	A	TL1	L	(IOGRP+)	128–A5	101–116–A9	Enable P register to adder
EIK17–	127–P5	A	TL1	L	(ACYLF+)(CASOP–)(LSXOP–)(SUBOP–)	127–K6	117–A1	Force carry to adder
ESDTS+	125–M4	A	TL1	S	(ACYEF+)(TL1FF+)(JSTOP–)(IRSOP–)(IMAOP–)(MCSET+)	125–B4	101–116–D4-D8	Enable adder sum to D register
DRLIN–	143–B3	A			Function of I/O option		125–D10	Device ready line
DRFLP–	125–E10	A	TL1	S	(DRFL1–)	125–G11	125–G10	Reset DRFLP+
DRFLP+	125–E9	A	TL1	L	(SMKXX–)	125–G9	125–D9	Set DRFLP+
CLPTR–	129–M10	A	TL2	R	(TL2FF+)(IOGRP+)(DRFLP–)(OCPLS–)(MCRST+)	129–E6	101–116–L12	Clear P register
EDPTS+	129–P9	A	TL2	S	(TL1FF+)(IOGRP+)(DRFLP–)(OCPLS–)(MCSET+)	129–E6	101–116–J11	Enable D register to P register
CLYTR–	129–P3	A	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	129–H3/N3	101–116–N12	Clear Y register
EPYTS+	129–P4	A	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)(DMCRQ–)	129–D4/L4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	A	TL1	L	(TL1FF+)(SPMOD–) (IGACY+)	126–F12/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle

Common shift instruction entry

Function	Origin	Cyc	Tim	Clk	Boolean Expression	Origin	Destination	Operation Description
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7/F9	Force carry to adder
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	121–A5 120–A1 125–D8	Clear shift counter Clear F register Clear AZZZZ FF
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnn F–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(EDPTR+)(MCRST+)	129–J9	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(EDPTR+)(MCSET+)	129–J9	101–116–J11	Enable D register to P register
EASTL+	127–P1	F	TLATE	L	(GENOP+)(TLATE+)(M01FF–)	127–K10	101–116–A4	Enable A register to adder
EMSHL+	127–P9	F	TLATE	L	(GENOP+)(TLATE+)(M01FF–)	127–K10	101–108–A9	Enable M(1-7) to adder
ENSHL+	127–P8	F	TLATE	L	(GENOP+)(TLATE+)(M01FF–)	127–K10	101–107–A10	Enable M–(1-7) to adder
EMSLL+	127–P11	F	TLATE	L	(GENOP+)(TLATE+)(M01FF–)	127–K10	108–116–A9	Enable M(8-16) to adder
ENSLL+	127–P7	F	TLATE	L	(GENOP+)(TLATE+)(M01FF–)	127–K10	108–116–A10	Enable M–(8-16) to adder
SETAZ+	125–M7	F	TL3	L	(SHAOP+)(TL3FF+)(AZZZZ–)	125–J12	125–D7	Set AZZZZ FF
EMCTL+	125–P12	F	TL3	L	(SHAOP+)(TL3FF+)(AZZZZ–)	125–J12	121–A11	Enable M register to shift counter
EMCTL–	125–K12	F	TL3	L	(SHAOP+)(TL3FF+)(AZZZZ–)	125–J12	124–G1	Clear CB1TF
SCZRO–	121–M4				(SC16F–) through (SC11F–)	121–X6	126–C4	Shift counter equals ZERO
RPTT2+	126–G5	F	TL3	L	NOR of EMC16 through EMC11–	126–F7	118–A4	Repeat TL2 timing level
CLDTR–	125–K5	F	TL3	R	(TL3FF+)(ACYLF–)(MCRST+)	125–B6/J4	101–116–F11	Clear D register to ONEs
CLETR–	125–K2	F	TL3	R	(TL3FF+)(GENOP+)(M01FF–)(M02FF+)(MCRST+)	125–B1	101–116–N2	Clear E register
ESDTS+	125–M4	F	TL3	S	(TL3FF+)(IOGRP–)(MCSET+)	125–B5/J4	101–116–F5-F9	Enable adder sum to D register
EBETS+	125–M1	F	TL3	S	(TL3FF+)(GENOP+)(M01FF–)(M02FF+)(MCSET+)	125–B1	101–116–L3	Enable B register to E register

See Page 2-59 for Common Shift Instruction Exit.



NOTES: 1. THIS INSTRUCTION IDENTICAL TO LGL EXCEPT FOR STATE OF D17DJ

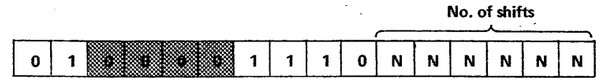
2. MISSING SIGNALS CAN BE FOUND IN ALR ENTRY ANALYSIS

Instruction: Logical Left Rotate (ALR)

OP Code: 0416N **Type:** SH, 1 + n/2 cycles

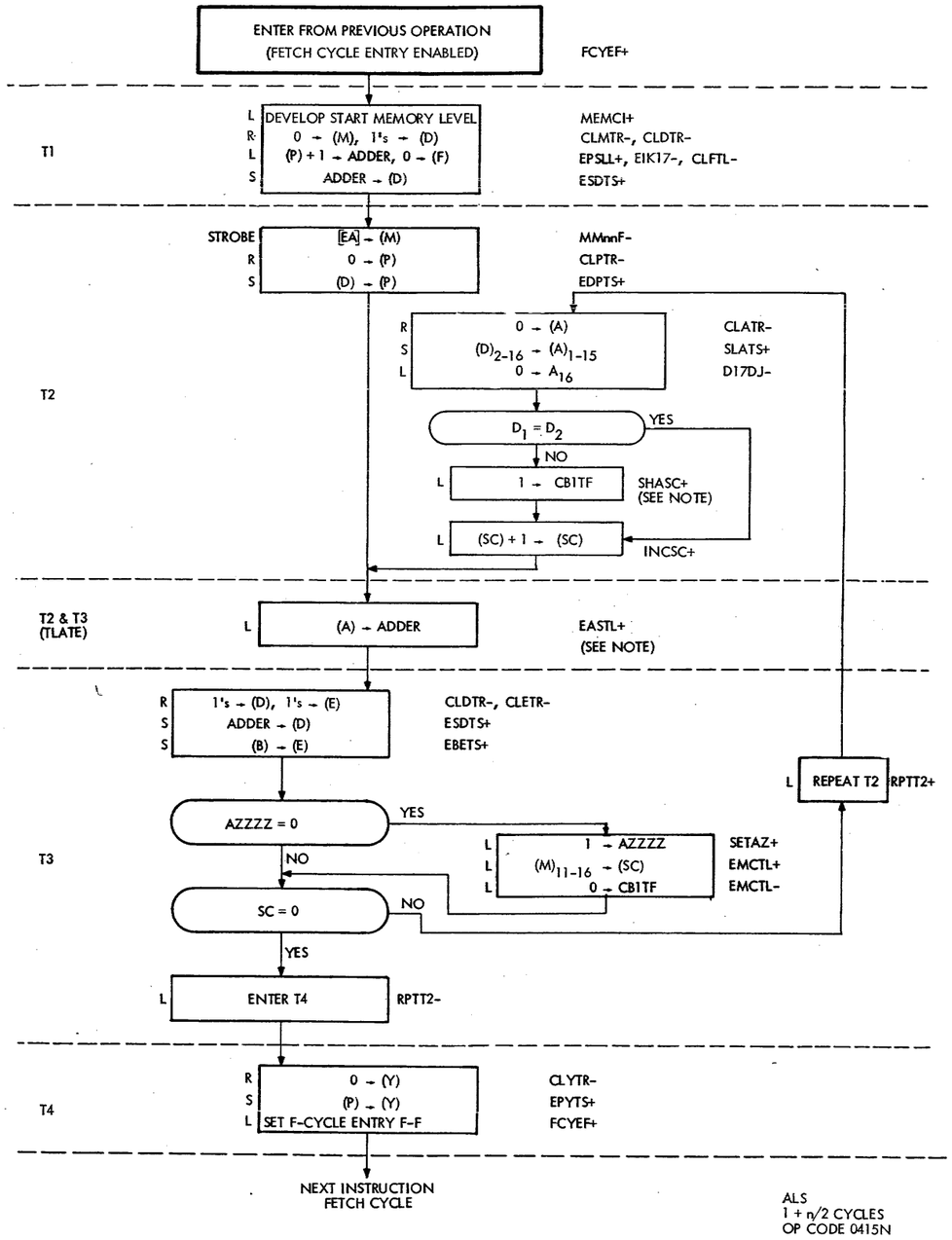
n = no. of shifts

Description: C ↔ 1 A 16



Execution Time (μs): 1.6 + 0.8n

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
					Common Entry (See Common Entry for Shift Instructions, Page 2-46)			
SHASC+	120–P7	F	TL2	L	(SHAOP+)(SCZRO–)	120–L7	122–D11/D12 124–D1/D3/D5	Shift A register and shift counter not equal to ZERO
CB1TF	124–P1	F	TL2	S	(SHASC+)(TL2FF+)(M07FF+)(M10FF–)(D01FF+)(MCSET+)	124–D3	124–P2	Set D1 into CB1TF
CLATR–	122–K8	F	TL2	R	(SHASC+)(TL2FF+)(M07FF+)(MCRST+)	122–C11/J8	101–116–L6	Clear A register
D17DJ+	130–G4	F	TL2	L	(SHAOP+)(M09FF+)(M08FF+)(D01FF+)	130–C3	116–J5	Left shift end effect
SLATS+	122–P11	F	TL2	S	(SHASC+)(TL2FF+)(M07FF+)(MCSET+)	124–C11/J11	101–116–J5	Shift left A register
					Common Exit (See Common Exit for Shift Instructions, Page 2-59)			



NOTE: MISSING SIGNALS CAN BE FOUND IN ALS ENTRY ANALYSIS

Instruction: Arithmetic Left Shift (ALS)

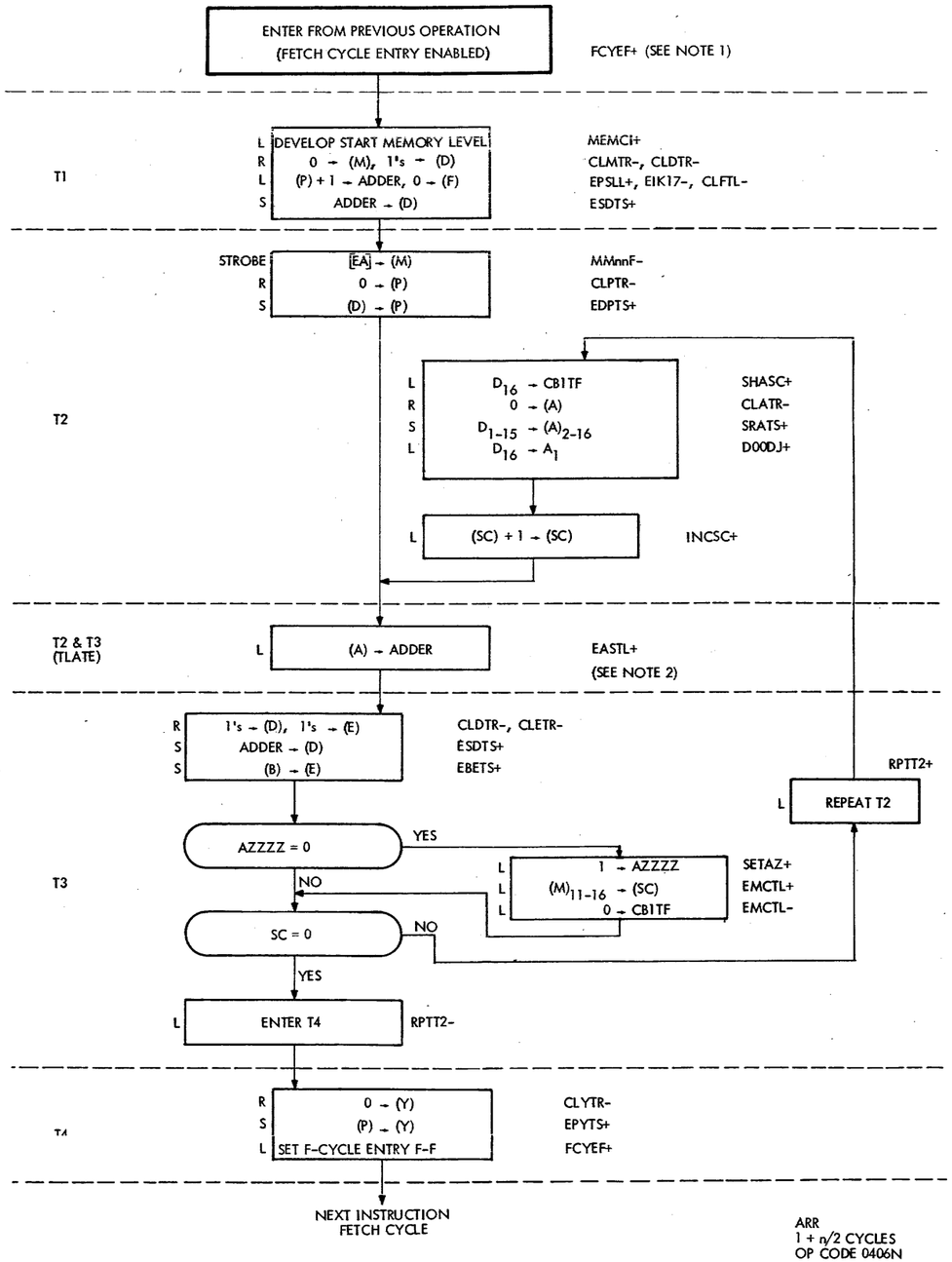
OP Code: 0415N **Type:** SH, 1 + n/2 cycles
n = no. of shifts

Description: 1 A 16 ← 0; OVF → (C)

											No. of shifts					
0	1	C	B	A	9	8	1	1	0	1	N	N	N	N	N	N
1	2	3	4	5	6	7	8	9	10		11	12	13	14	15	16

Execution Time (μs): 1.6 + 0.8n

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
			Common Entry (See Common Entry for Shift Instructions, Page 2-46)					
SHASC+	120–P7	F	TL2	L	(SHAOP+)(SCZRO–)	120–L7	122–D11/D12 124–D1/D3/ D5	Shift A register and shift counter not equal to ZERO
CLATR–	122–K8	F	TL2	R	(SHASC+)(TL2FF+)(M07FF+) (MCRST+)	122–C11/ J8	101–116–L6	Clear A register
D17DJ–	130–G4	F	TL2	L	(M08FF+)	130–C3	116–J5	Clear A register bit 16
SLATS+	122–P11	F	TL2	S	(SHASC+)(TL2FF+)(M07FF+) (MCSET+)	122–C11/ J11	101–116–J5	Shift left A register
D1 ≠ D2	124–E7	F	TL2	L	See inputs to gate CB1TF–	124–E7	124–P2	Set CB1TF with SHASC+
			Common Exit (See Common Exit for Shift Instructions, Page 2-59)					



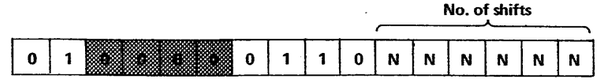
NOTES: 1. THIS INSTRUCTION IDENTICAL TO LGR EXCEPT FOR STATE OF D00DJ

2. MISSING SIGNALS CAN BE FOUND IN ARR ENTRY ANALYSIS

Instruction: Logical Right Rotate (ARR)

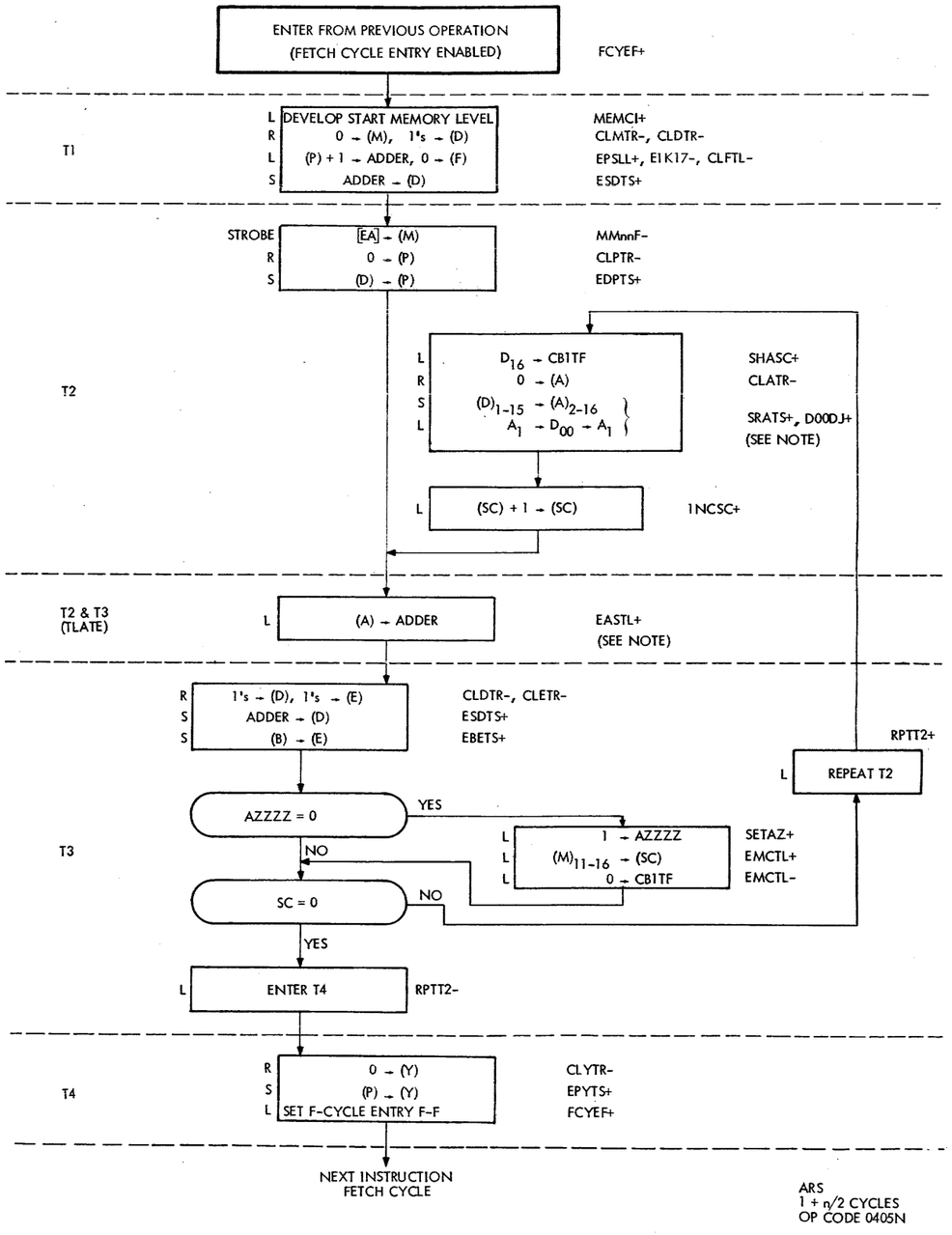
OP Code: 0406N **Type:** SH, 1 + n/2 cycles
n = no. of shifts

Description: 1 A 16 → C



Execution Time (μs): 1.6 + 0.8n

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
					Common Entry (See Common Entry for Shift Instructions, Page 2-46)			
SHASC+	120—P7	F	TL2	L	(SHAOP+)(SCZRO–)	120—L7	122—D11/D12 124—D1/D3/D5	Shift A register and shift counter not equal to ZERO
CB1TF	124—P1	F	TL2	S	(SHASC+)(M07FF–)(M08FF+)(TL2FF+)(D16FF+)(MCSET+)	124—D4	124—P2	Set D16 into CB1TF
CLATR–	122—K8	F	TL2	R	(SHASC+)(TL2FF+)(M07FF–)(MCRST+)	122—C11/J8	101—116—L6	Clear A register
D00DJ+	130—D1	F	TL2	L	(SHAOP+)(M08FF+)(M09FF+)(D16FF+)	130—A2	101—J6	Right shift end effect
SRATS+	122—P12	F	TL2	S	(SHASC+)(TL2FF+)(M07FF–)(MCSET+)	122—C12/J12	101—116—J6	Shift right A register
MFG2E–	122—D12	F	TL2	L	(SHASC+)(TL2FF+)(M07FF–)	122—C12	124—G1	Clear CB1TF
					Common Exit (See Common Exit for Shift Instructions, Page 2-59)			

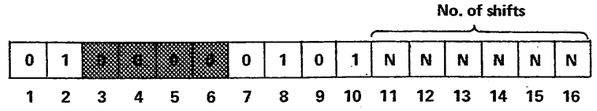


NOTE: MISSING SIGNALS CAN BE FOUND IN ARS ENTRY ANALYSIS

Instruction: Arithmetic Right Shift (ARS)

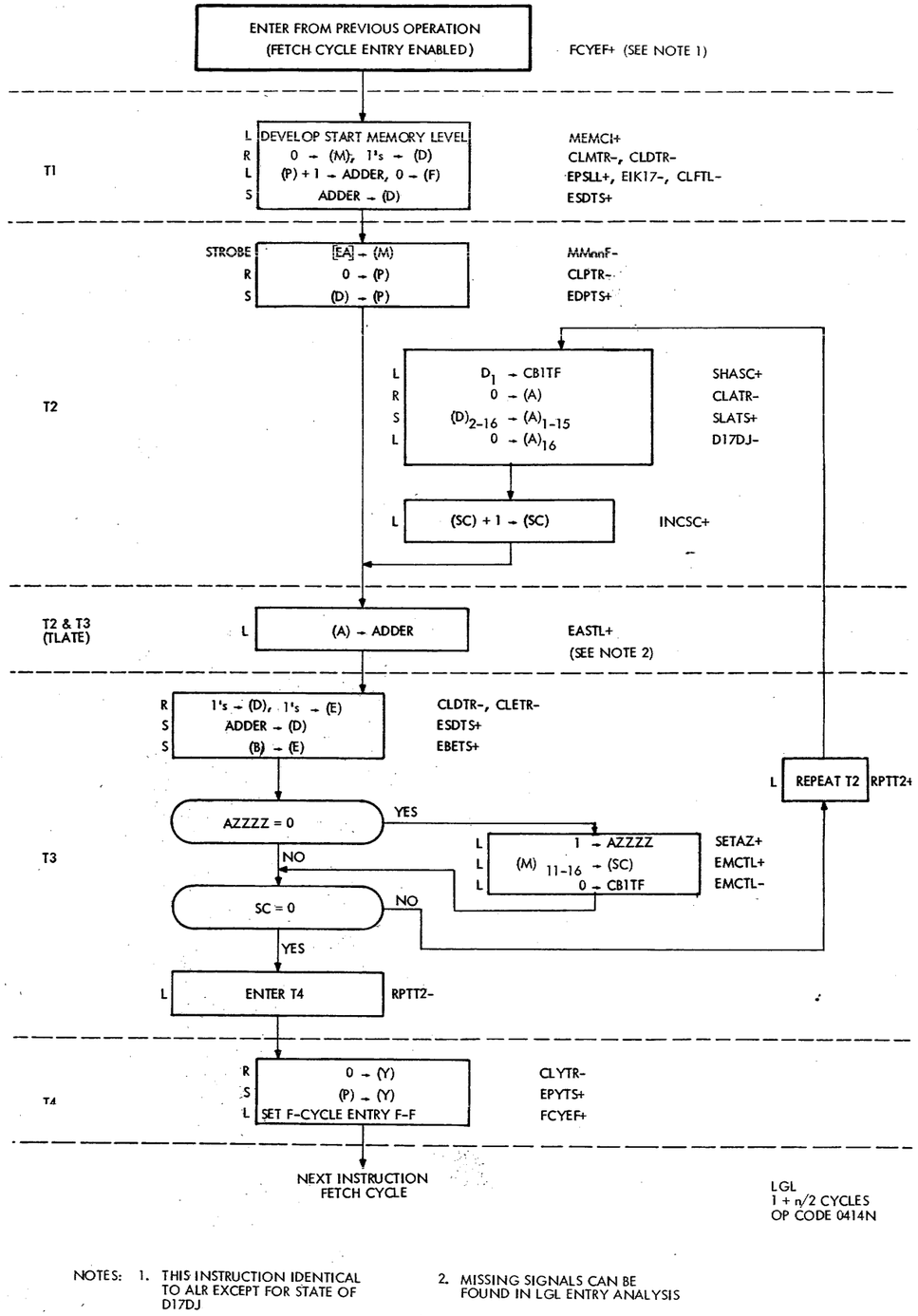
OP Code: 0405N **Type:** Sh, 1 + n/2 cycles

Description: A1 → 2 A 16 → C (n = no. of shifts)



Execution Time (μs): 1.6 + 0.8n

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
					Common Entry (See Common Entry for Shift Instructions, Page 2-46)			
SHASC+	120—P7	F	TL2	L	(SHAOP+)(SCZRO−)	120—L7	122—D11/D12 124—D1/D3/D5	Shift A register and shift counter not equal to ZERO
CB1TF	124—P1	F	TL2	S	(SHASC+)(M07FF−)(M08FF+)(TL2FF+)(D16FF+)(MCSET+)	124—D4	124—P2	Set D16 into CB1TF
MFG2E−	122—D12	F	TL2	L	(SHASC+)(M07FF−)(TL2FF+)	122—C12	124—G1	Clear CB1TF
CLATR−	122—K8	F	TL2	R	(SHASC+)(TL2FF+)(M07FF−)(MCRST+)	122—C11/J8	101—116—L6	Clear A register
SRATS+	122—P12	F	TL2	S	(SHASC+)(TL2FF+)(M07FF−)(MCSET+)	122—C12/J12	101—116—J6	Shift right A register
D00DJ+	130—D1	F	TL2	L	(M10FF+)(D00FF+)	122—A1	101—J6	Maintain sign bit
D00FF+	130—K8	F	TL2	S	(ESDTS+)(R01PA+)(G01DJ−)	130—F6	130—F6	Extension of D register
R01PA+	101—D7	F	TL2	L	(H01DJ−)	101—C7	101—D7	Adder network OR gate
G01DJ−	101—C5	F	TL2	L	(EASTL+)(A01FF+)	101—A4	101—C5	Adder network OR gate
					Common Exit (See Common Exit for Shift Instructions, Page 2-59)			



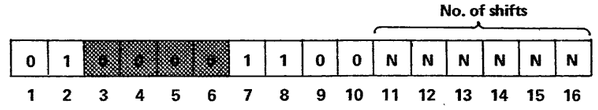
NOTES: 1. THIS INSTRUCTION IDENTICAL TO ALR EXCEPT FOR STATE OF D17DJ

2. MISSING SIGNALS CAN BE FOUND IN LGL ENTRY ANALYSIS

Instruction: Logical Left Shift (LGL)

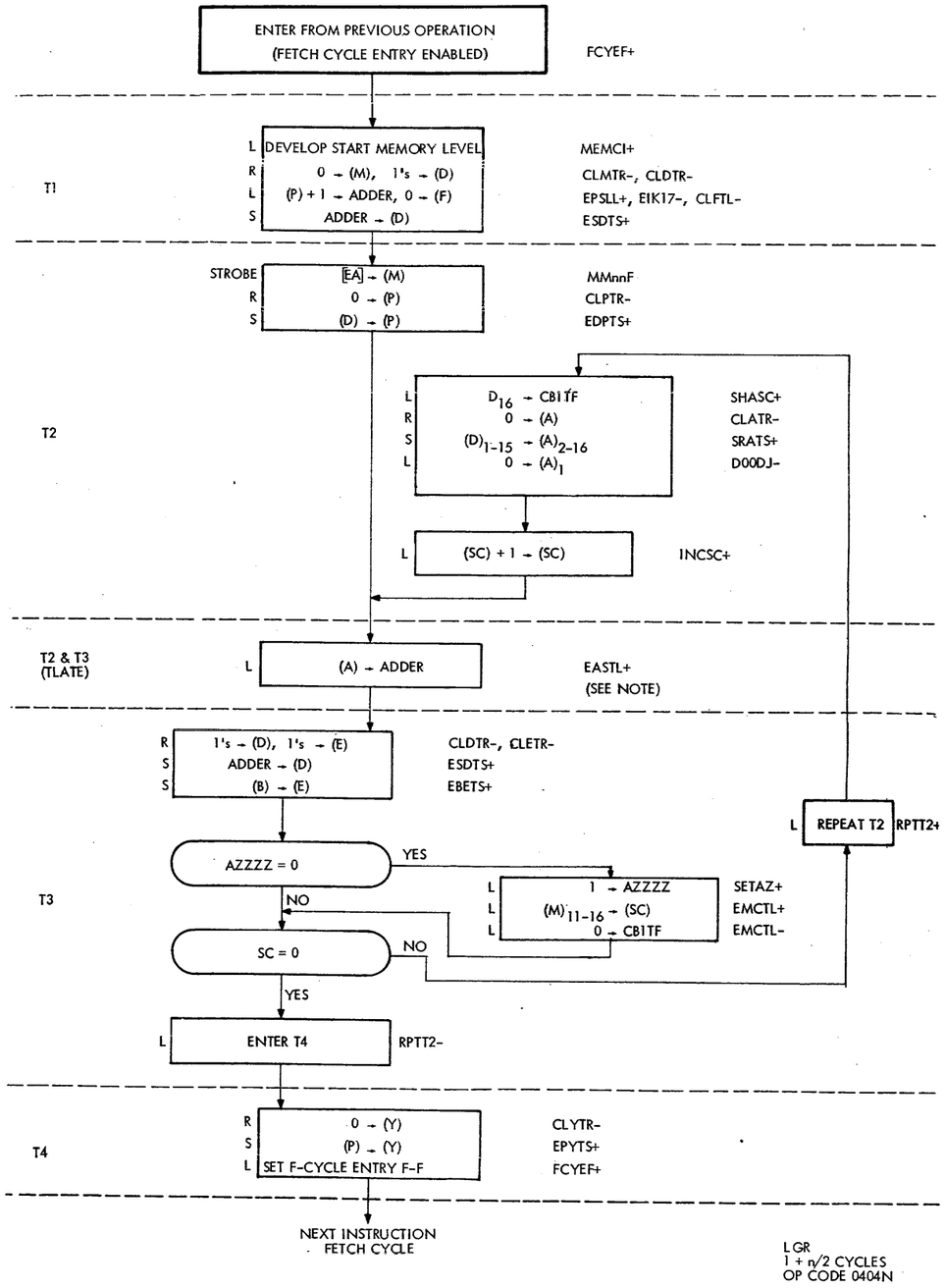
OP Code: 0414N **Type:** SH, 1 + n/2 cycles
n = no. of shifts

Description: C ← 1 A 16 ← 0



Execution Time (μs): 1.6 + 0.8n

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
			Common Entry (See Common Entry for Shift Instructions, Page 2-46)					
SHASC+	120—P7	F	TL2	L	(SHAOP+)(SCZRO−)	120—L7	122—D11/D12 124—D1/D3/D5	Shift A register and shift counter not equal to ZERO
CB1TF	124—P1	F	TL2	S	(SHASC+)(TL2FF+)(M07FF+)(M10FF−)(D01FF+)(MCSET+)	124—D3	124—P2	Set D1 into CB1TF
CLATR−	122—K8	F	TL2	R	(SHASC+)(TL2FF+)(M07FF+)(MCRST+)	122—C11/J8	101—116—L6	Clear A register
D17DJ− SLATS+	130—G4 122—P11	F F	TL2 TL2	L S	(M08FF+) (SHASC+)(TL2FF+)(M07FF+)(MCSET+)	130—C3 122—C11/J11	117—J5 101—116—J5	Clear A register bit 16 Shift left A register
			Common Exit (See Common Exit for Shift Instructions, Page 2-59)					



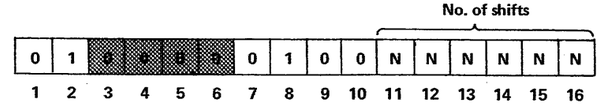
NOTES: 1. THIS INSTRUCTION IDENTICAL TO ARR EXCEPT FOR STATE OF D00DJ

2. MISSING SIGNALS CAN BE FOUND IN LGR ENTRY ANALYSIS

Instruction: Logical Right Shift (LGR)

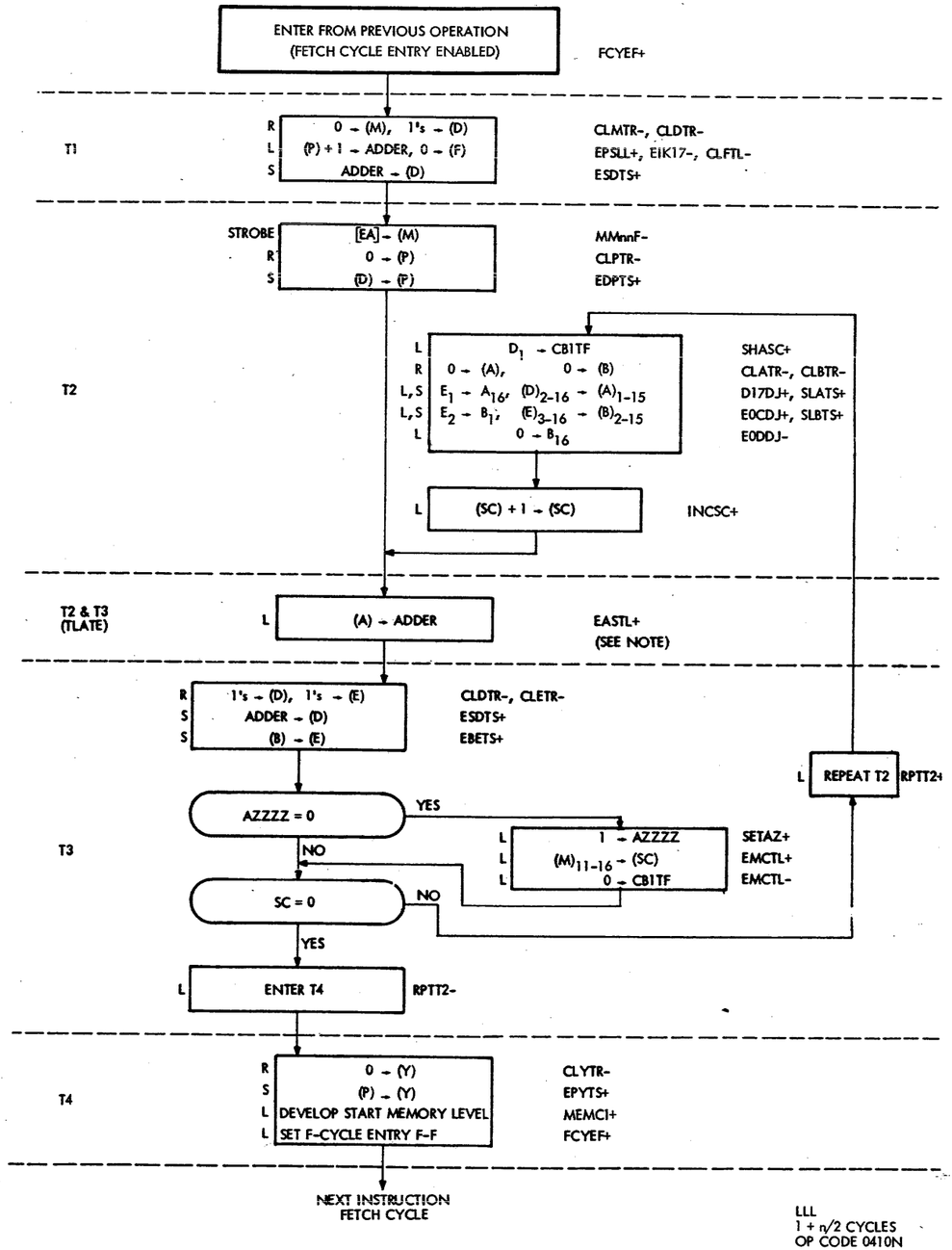
OP Code: 0404N **Type:** Sh, 1 + n/2 cycles
n = no. of shifts

Description: 0 → 1 A 16 → C



Execution Time (μs): 1.6 + 0.8n

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
					Common Entry (See Common Entry for Shift Instructions, Page 2-46)			
SHASC+	120—P7	F	TL2	L	(SHAOP+)(SCZRO-)	120—L7	122—D11/D12 124—D1/D3/D5	Shift A register and shift counter not equal to ZERO
CB1TF	124—P1	F	TL2	S	(SHASC+)(M07FF-)(M08FF+)(TL2FF+)(D16FF+)(MCSET+)	124—D4	124—P2	Set D16 into CB1TF
CLATR-	122—K8	F	TL2	R	(SHASC+)(M07FF-)(TL2FF+)(MCRST+)	122—C11/J8	101—116—L6	Clear A register
SRATS+	122—P12	F	TL2	S	(SHASC+)(TL2FF+)(M07FF-)(MCSET+)	122—C12/J12	101—116—J6	Shift right A register
MFG2E- D00DJ-	122—D12 130—D1	F F	TL2 TL2	L L	(SHASC+)(TL2FF+)(M07FF-) (M10FF-)(M08FF+)	122—C12 130—A2	124—G1 101—J6	Clear CB1TF Clear A register bit 1
					Common Exit (See Common Exit for Shift Instructions, Page 2-59)			



NOTES: 1. THIS INSTRUCTION IDENTICAL TO LLR EXCEPT FOR STATE OF E0DDJ

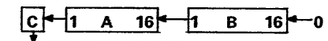
2. MISSING SIGNALS CAN BE FOUND IN LLL ENTRY ANALYSIS

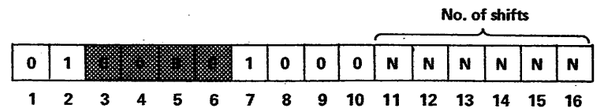
Instruction: Long Left Logical Shift (LLL)

OP Code: 0410N **Type:** SH, 1 + n/2 cycles

n = no. of shifts

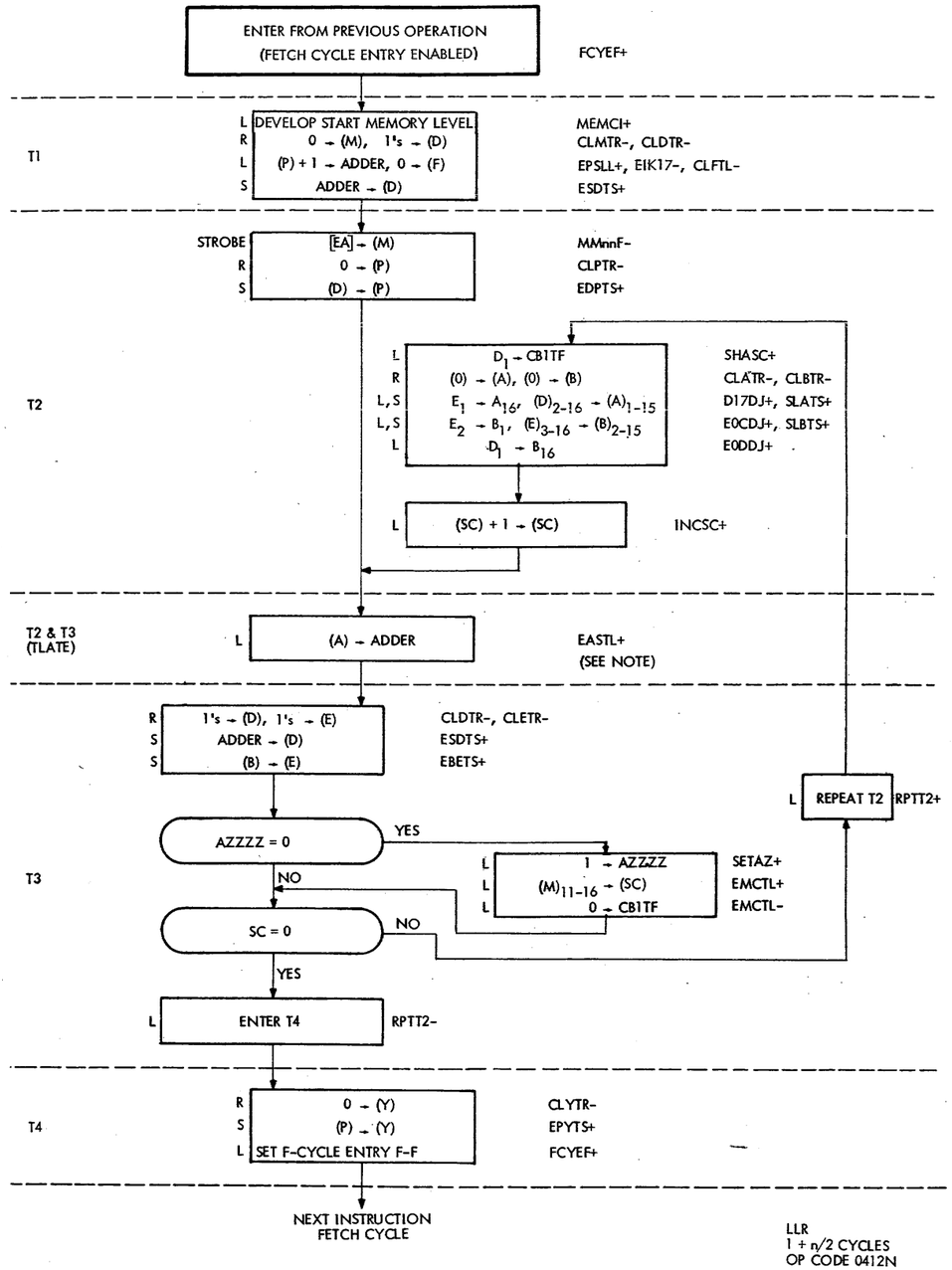
Description:





Execution Time (μs): 1.6 + 0.8n

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
					Common Entry (See Common Entry for Shift Instructions, Page 2-46)			
SHASC+	120—P7	F	TL2	L	(SHAOP+)(SCZRO−)	120—L7	122—D11/D12 123—F4 124—D1/D3	Shift A register and shift counter not equal to ZERO
CB1TF	124—P1	F	TL2	S	(SHASC+)(TL2FF+)(M07FF+)(M10FF−)(D01FF+)(MCSET+)	124—D3/K2	124—P2	Set D1 into CB1TF
CLATR−	122—K8	F	TL2	R	(SHASC+)(TL2FF+)(M07FF+)(MCRST+)	122—C12	101—116—L6	Clear A register
CLBTR−	123—M6	F	TL2	R	(SHASC+)(TL2FF+)(M07FF+)(M08FF−)(MCRST+)	123—F4/L6	101—116—L2	Clear B register
D17DJ+	130—G4	F	TL2	L	(ACYLF−)(M08FF−)(M10FF−)(E01FF+)	130—C4	116—J5	Left shift end effect
SLATS+	122—P11	F	TL2	S	(SHASC+)(TL2FF+)(M07FF+)	122—C11	101—116—J5	Shift left A register
E0CDJ+	130—E8	F	TL2	L	(E02FF+)	130—E8	101—J1	Set E2 into B1
SLBTS+	123—P4	F	TL2	S	(SHASC+)(TL2FF+)(M07FF+)(M08FF−)(MCSET+)	123—F4/L4	101—116—J1	Shift left B register
E0DDJ+	130—D12	F	TL2	L	(M09FF+)(D01FF+)	130—A12	116—J	Set B16
					Common Exit (See Common Exit for Shift Instructions, Page 2-59)			



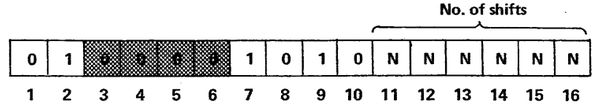
NOTES: 1. THIS INSTRUCTION IDENTICAL TO LLL EXCEPT FOR STATE OF E0DDJ

2. MISSING SIGNALS CAN BE FOUND IN LLR ENTRY ANALYSIS

Instruction: Long Left Rotate (LLR)

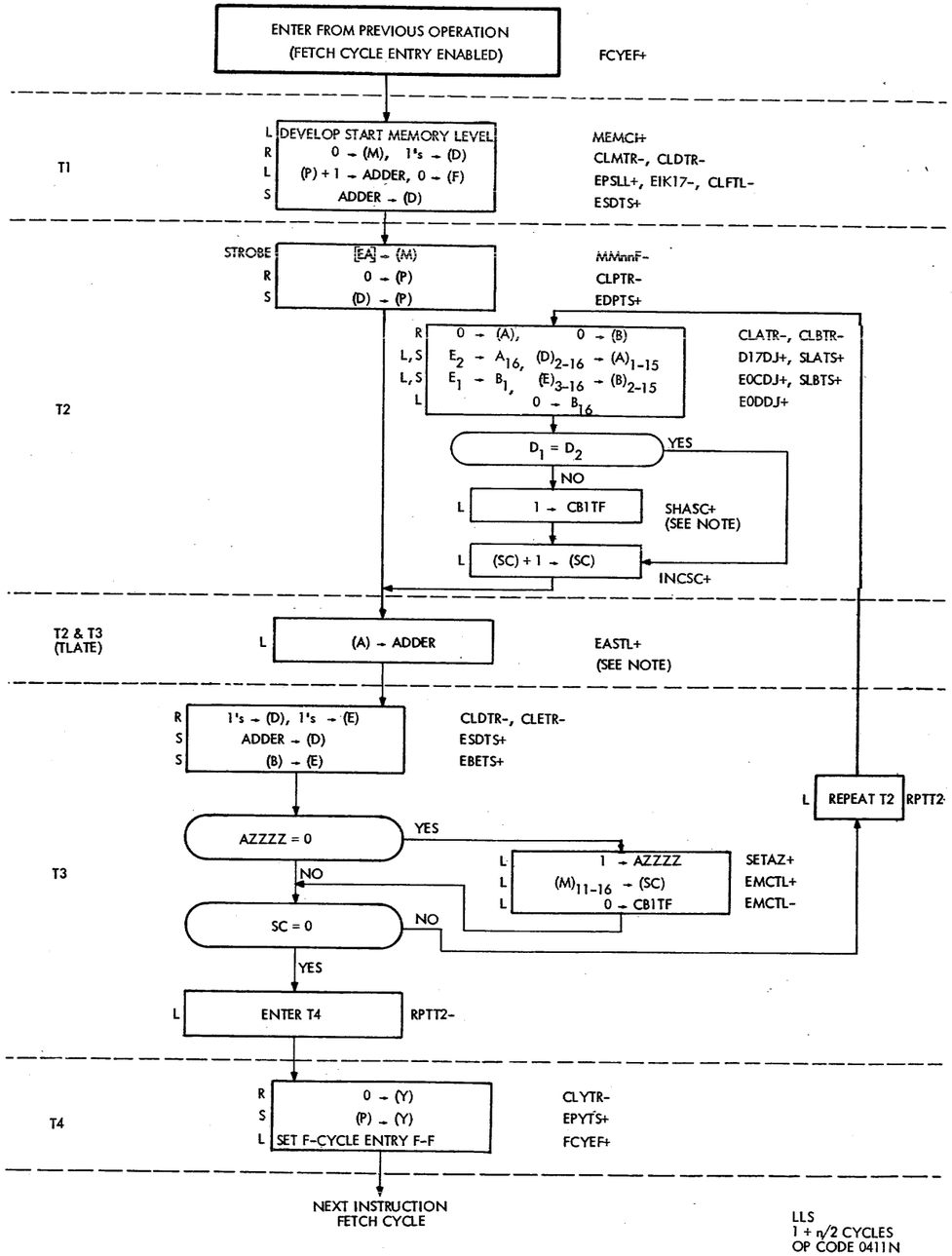
OP Code: 0412N **Type:** SH, 1 + n/2 cycles

Description:



Execution Time (μs): 1.6 + 0.8n

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
					Common Entry (See Common Entry for Shift Instructions, Page 2-46)			
SHASC+	120—P7	F	TL2	L	(SHAOP+)(SCZRO−)	120—L7	122—D11/D12 123—F4 124—D1/D3	Shift A register and shift counter not equal to ZERO
CB1TF	124—P1	F	TL2	S	(SHASC+)(TL2FF+)(M07FF+)(M10FF−)(D01FF+)(MCSET+)	124—D3/K2	124—P2	Set D1 into CB1TF
CLATR−	122—K8	F	TL2	R	(SHASC+)(TL2FF+)(M07FF+)(MCRST+)	122—C12	101—116—L6	Clear A register
CLBTR−	123—M6	F	TL2	R	(SHASC+)(TL2FF+)(M07FF+)(M08FF−)(MCRST+)	123—F4/L6	101—116—L2	Clear B register
D17DJ+	130—G4	F	TL2	L	(ACYLF−)(M08FF−)(M10FF−)(E01FF+)	130—C4	116—J5	Left shift end effect
SLATS+	122—P11	F	TL2	S	(SHASC+)(TL2FF+)(M07FF+)(MCSET+)	122—C11	101—116—J5	Shift left A register
E0CDJ+	130—E8	F	TL2	L	(E02FF+)	130—E8	101—J1	Set E2 and B1
SLBTS+	123—P4	F	TL2	S	(SHASC+)(TL2FF+)(M07FF+)(M08FF−)(MCSET+)	123—F4/L4	101—116—J1	Shift left B register
E0DDJ+	130—D12	F	TL2	L	(SHAOP+)(M09FF+)(D01FF+)	130—A12	116—J1	Set D1 into B16
					Common Exit (See Common Exit for Shift Instructions, Page 2-59)			

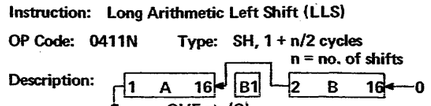


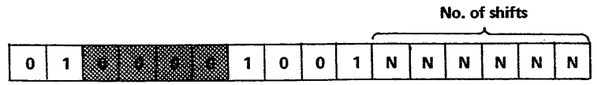
NOTE: MISSING SIGNALS CAN BE FOUND IN LLS ENTRY ANALYSIS

Instruction: Long Arithmetic Left Shift (LLS)

OP Code: 0411N **Type:** SH, 1 + n/2 cycles

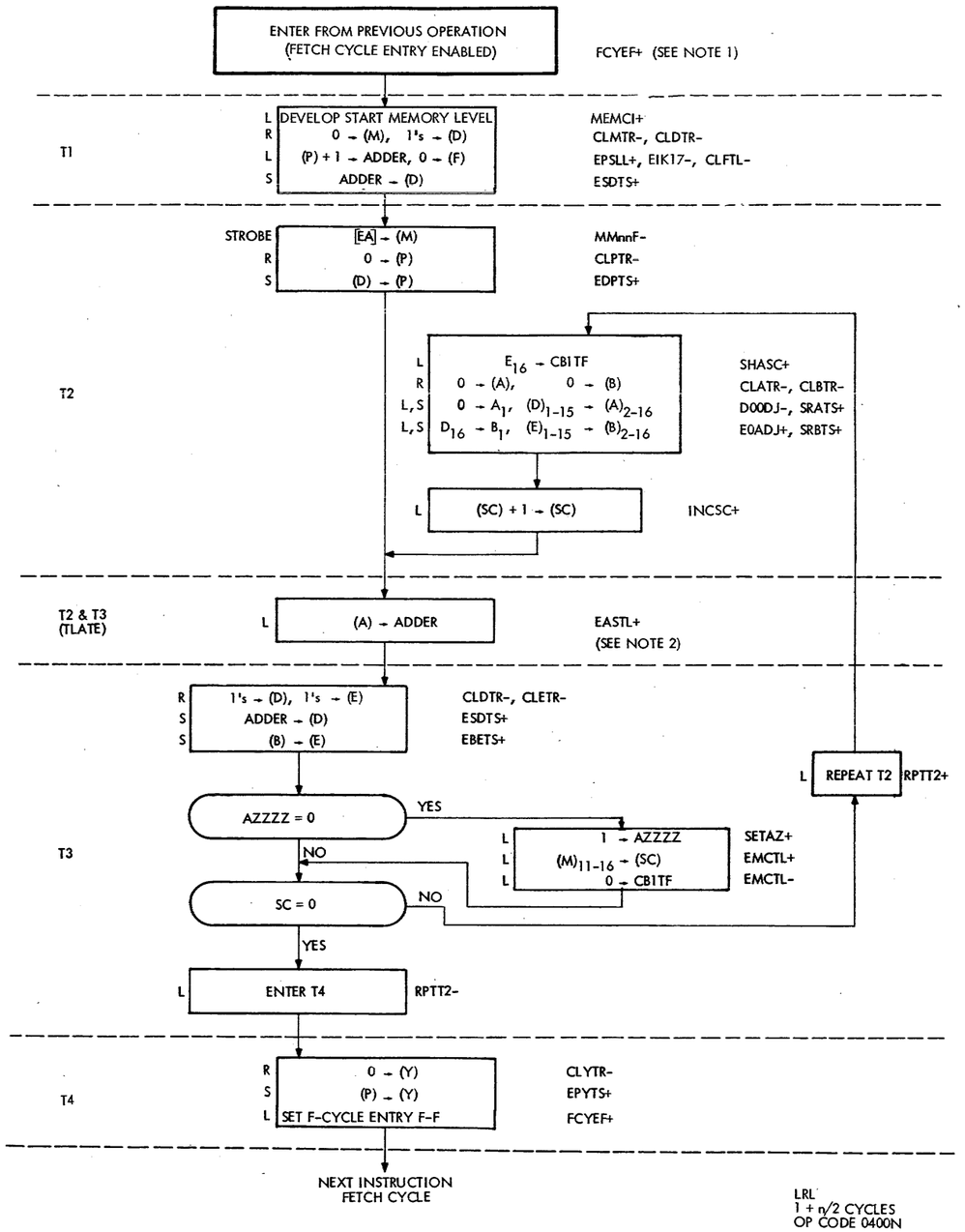
Description: n = no. of shifts





Execution Time (μs): 1.6 + 0.8n

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
					Common Entry (See Common Entry for Shift Instructions, Page 2-46)			
SHASC+	120—P7	F	TL2	L	(SHAOP+)(SCZRO−)	120—L7	122—D11/D12 123—F4 124—C1/D3	Shift A register and shift counter not equal to ZERO
CLATR−	122—K8	F	TL2	R	(SHASC+)(TL2FF+)(M07FF+)(MCRST+)	122—C12	101—116—L6	Clear A register
CLBTR−	123—M6	F	TL2	R	(SHASC+)(TL2FF+)(M07FF+)(M08FF−)(MCRST+)	123—F4/L6	101—116—L2	Clear B register
D17DJ+	130—G4	F	TL2	L	(M08FF−)(M10FF+)(E02FF+)	130—C5	116—J5	Left shift end effect
SLATS+	122—P11	F	TL2	S	(SHASC+)(TL2FF+)(M07FF+)(MCSET+)	122—C11	101—116—J5	Shift left A register
E0CDJ+	130—E8	F	TL2	L	(ACYLF−)(M10FF+)(E01FF−)	130—C8	101—J1	Set E1 into B1
SLBTS+	123—P4	F	TL2	S	(SHASC+)(TL2FF+)(M07FF+)(M08FF−)(MCSET+)	123—F4/L4	101—116—J1	Shift left B register
E0DDJ+	130—D12	F	TL2	L	(M09FF+)(E01FF+)	130—A12	116—J1	Set B16
D1 ≠ D2	124—E7	F	TL2	L	See inputs to gate CB1TF	124—E7	124—P2	Set CB1TF with SHASC+
					Common Exit (See Common Exit for Shift Instructions, Page 2-59)			



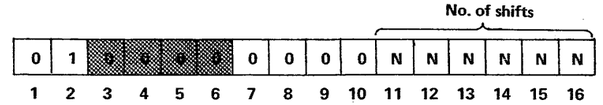
NOTES: 1. THIS INSTRUCTION IDENTICAL TO LRR EXCEPT FOR STATE OF D00DJ

2. MISSING SIGNALS CAN BE BE FOUND IN LRL ENTRY ANALYSIS

Instruction: Long Right Logical Shift (LRL)

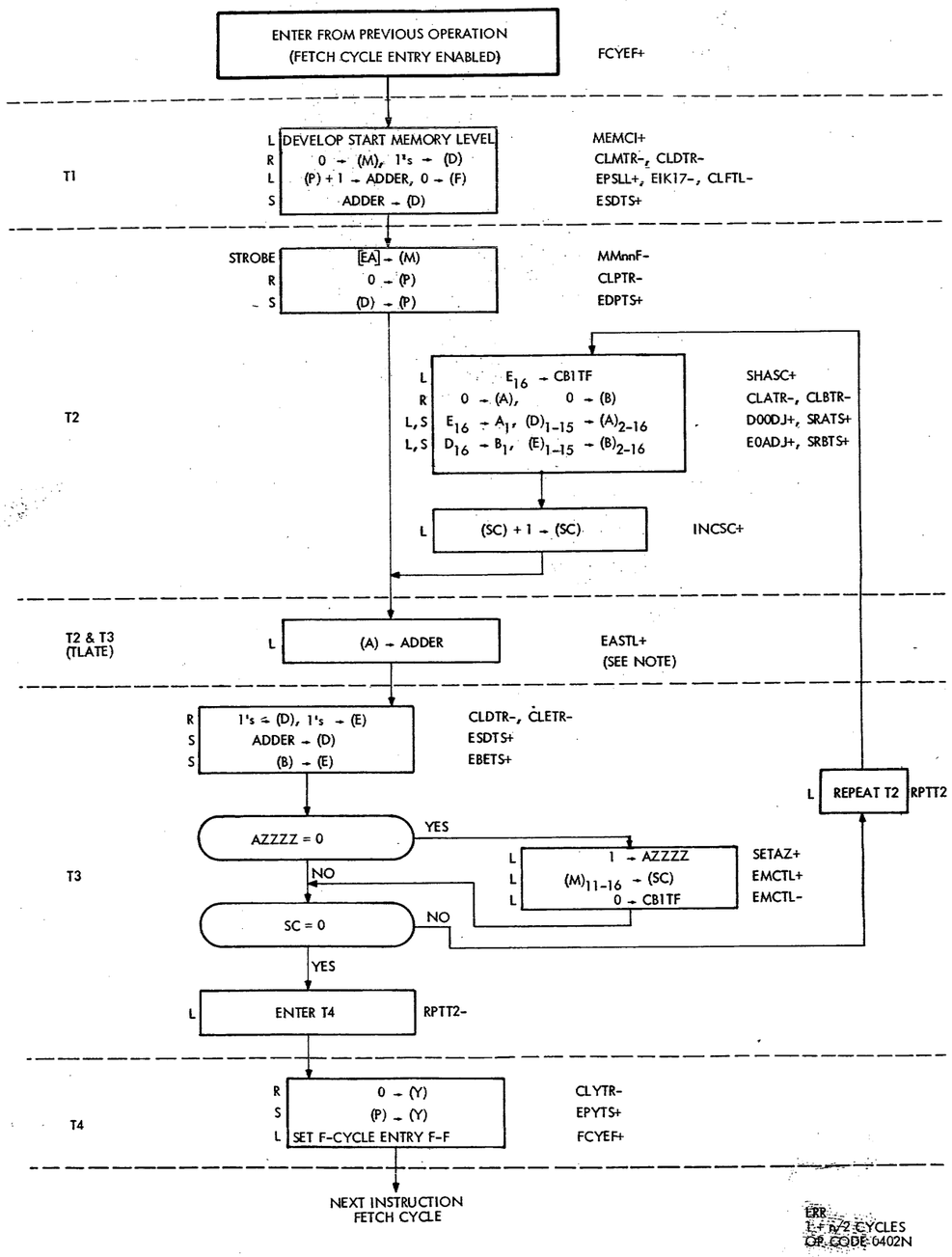
OP Code: 0400N **Type:** SH, 1 + n/2 cycles
n = no. of shifts

Description: 0→ 1 A 16 → 1 B 16 → C



Execution Time (μs): 1.6 + 0.8n

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
					Common Entry (See Common Entry for Shift Instructions, Page 2-46)			
SHASC+	120–P7	F	TL2	L	(SHAOP+)(SCZRO–)	120–L7	122–D11/D12 123–E4 124–D1/D3	Shift A register and shift counter not equal to ZERO
CB1TF	124–P1	F	TL2	S	(TL2FF+)(SHASC+)(M07FF–)(M08FF–)(E16FF+)(MCSET+)	124–D5	124–P2	Set E16 into CB1TF
MFG2E–	122–D12	F	TL2	L	(SHASC+)(TL2FF+)(M07FF–)	122–C12	124–G1	Clear CB1TF
CLATR–	122–K8	F	TL2	R	(SHASC+)(TL2FF+)(M07FF–)(MCRST+)	122–C11/J8	101–116–L6	Clear A register
CLBTR–	123–M6	F	TL2	R	(SHASC+)(TL2FF+)(M07FF–)(M08FF–)(MCRST+)	123–F6/L6	101–116–L2	Clear B register
D00DJ–	130–D1	F	TL2	L	(M10FF–)(M09FF–)	130–A2	101–J6	Clear A register bit 1 with SRATS+
SRATS+	122–P12	F	TL2	S	(SHASC+)(TL2FF+)(M07FF–)(MCSET)	122–C12	101–116–J6	Shift right A register
E0ADJ+	130–E10	F	TL2	L	(M10FF–)D16FF–)	130–C11	101–J2	Set D16 into B1
SRBTS+	123–P8	F	TL2	S	(SHASC+)(TL2FF+)(M07FF–)(M08FF–)(MCSET+)	123–F6/L8	101–116–J2	Shift right B register
					Common Exit (See Common Exit for Shift Instructions, Page 2-59)			



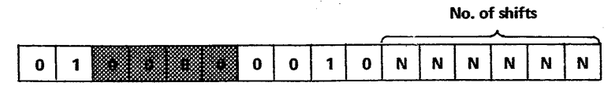
NOTES: 1. THIS INSTRUCTION IDENTICAL TO LRL EXCEPT FOR STATE OF D00DJ

2. MISSING SIGNALS CAN BE FOUND IN LRR ENTRY ANALYSIS

Instruction: Long Right Rotate (LRR)

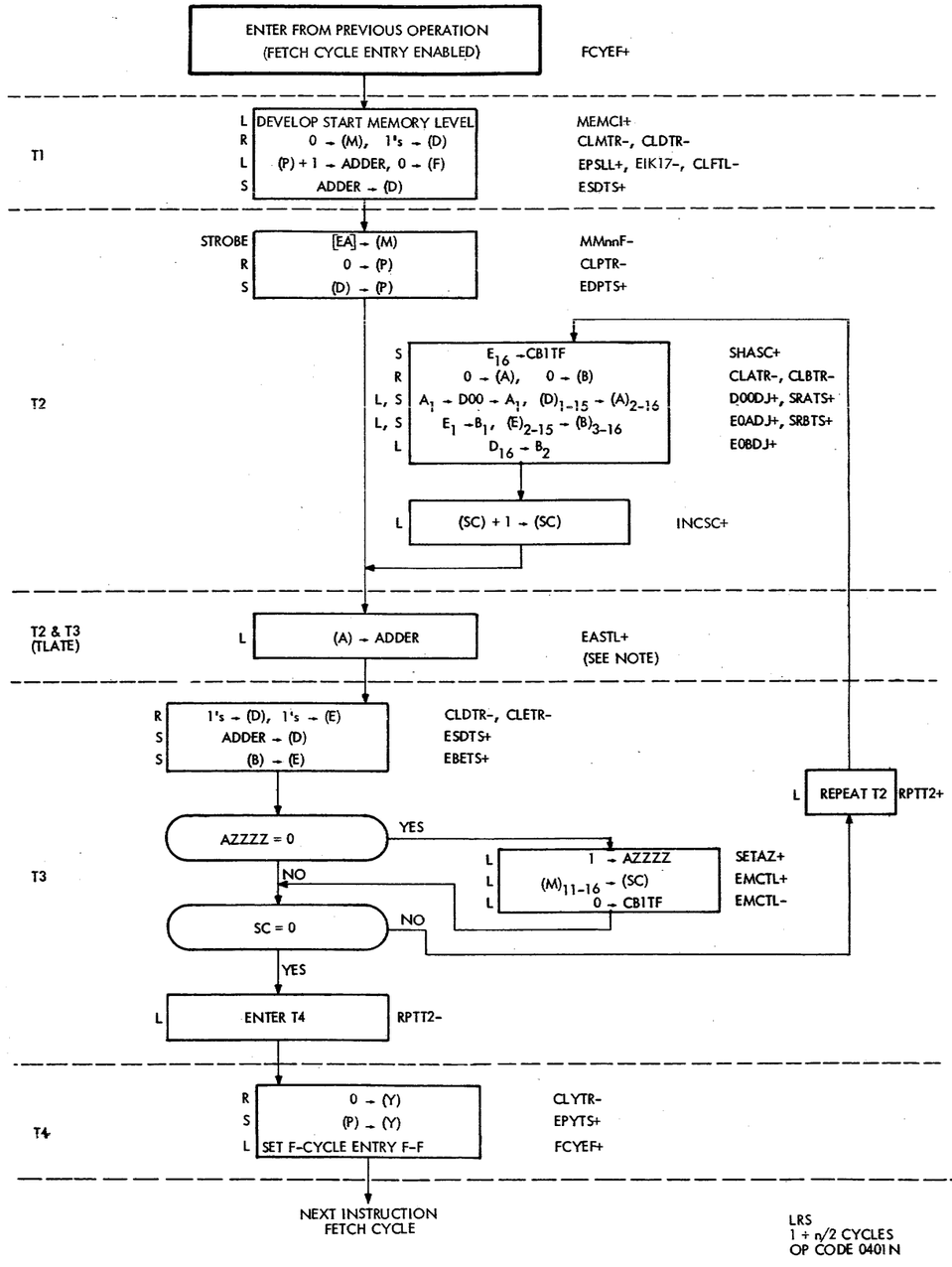
OP Code: 0402N **Type:** SH, 1 + n/2 cycles
n = no. of shifts

Description: 1 A 16 → 1 B 16 → C



Execution Time (μs): 1.6 + 0.8n

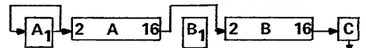
Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
					Common Entry (See Common Entry for Shift Instructions, Page 2-46)			
SHASC+	120–P7	F	TL2	L	(SHAOP+)(SCZRO–)	120–L7	122–D11/D12 123–E4 124–D1/D3	Shift A register and shift counter not equal to ZERO
CB1TF	124–P1	F	TL2	S	(TL2FF+)(SHASC+)(M07FF–)(M08FF–)(E16FF–)(MCSET+)	124–D5	124–P2	Set E16 into CB1TF
CLATR–	122–K8	F	TL2	R	(SHASC+)(TL2FF+)(M07FF–)(MCRST+)	122–C11/J8	101–116–L6	Clear A register
CLBTR–	123–M6	F	TL2	R	(SHASC+)(TL2FF+)(M07FF–)(M08FF–)(MCRST+)	123–F6/L6	101–116–L2	Clear B register
D00DJ+	130–D1	F	TL2	L	(SHAOP+)(M08FF–)(M09FF+)(E16FF+)	130–A3	101–J6	Set E16 into A1 with SRATS+
SRATS+	122–P12	F	TL2	S	(SHASC+)(TL2FF+)(M07FF–)(MCSET+)	122–C12	101–116–J6	Shift right A register
MFG2E–	122–D12	F	TL2	L	(SHASC+)(TL2FF+)(M07FF–)	122–C12	124–G1	Clear CB1TF
E0ADJ+	130–E10	F	TL2	L	(M10FF–)(D16FF–)	130–C11	101–J2	Set D16 into B1
SRBTS+	123–P8	F	TL2	S	(SHASC+)(TL2FF+)(M07FF–)(M08FF–)(MCSET+)	123–F6/L8	101–116–J2	Shift right B register
					Common Exit (See Common Exit for Shift Instructions, Page 2-59)			

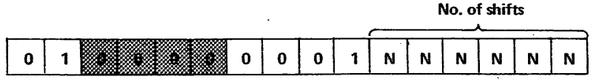


NOTE: MISSING SIGNALS CAN BE FOUND IN LRS ENTRY ANALYSIS

Instruction: Long Arithmetic Right Shift (LRS)

OP Code: 0401N **Type:** SH, 1 + n/2 cycles
n = no. of shifts

Description: 



Execution Time (μs): 1.6 + 0.8n

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
					Common Entry (See Common Entry for Shift Instructions, Page 2-46)			
SHASC+	120—P7	F	TL2	L	(SHAOP+)(SCZRO-)	120—L7	122—D11/D12 123—E4 124—D1/D3	Shift A register and shift counter not equal to ZERO
CB1TF	124—P1	F	TL2	S	(TL2FF+)(SHASC+)(M07FF-)(M08FF-)(E16FF+)(MCSET+)	124—D5	124—P2	Set E16 into CB1TF
CLATR-	122—K8	F	TL2	R	(SHASC+)(TL2FF+)(M07FF-)(MCRST+)	122—C11/J8	101—116—L6	Clear A register
CLBTR-	123—M6	F	TL2	R	(SHASC+)(TL2FF+)(M07FF-)(M08FF-)(MCRST+)	123—F6/L6	101—116—L2	Clear B register
D00DJ+	130—D1	F	TL2	L	(M10FF+)(D00FF+)	130—A1	101—J6	Maintain sign bit
D00FF+	130—K8	F	TL2	S	(ESDTS+)(R01PA+)(G01DJ-)	130—F6	130—A1	Extension of D register
R01PA+	101—D7	F	TL2	L	(HOLDJ-)	101—C7	101—D7	Adder network OR gate
G01DJ-	101—C5	F	TL2	L	(EASTL+)(A01FF+)	101—A4	101—C5	Adder network OR gate
SRATS+	122—P12	F	TL2	S	(SHASC+)(TL2FF+)(M07FF-)(MCSET+)	122—C12/J12	101—116—J6	Shift right A register
MFG2E-	122—D12	F	TL2	L	(SHASC+)(TL2FF+)(M07FF-)	122—C12	124—G1	Clear CB1TF
E0ADJ+	130—E10	F	TL2	L	(M10FF+)(E01FF-)	130—C11	101—J2	Set E1 into B1
E0BDJ+	130—H1	F	TL2	L	(M10FF+)(D16FF-)	130—F1	102—J2	Set D16 into B2
SRBTS+	123—P8	F	TL2	S	(SHASC+)(TL2FF+)(M07FF-)(M08FF-)(MCSET+)	123—F6/L8	101—116—J2	Shift right B register

Common shift instruction exit

Instruction:

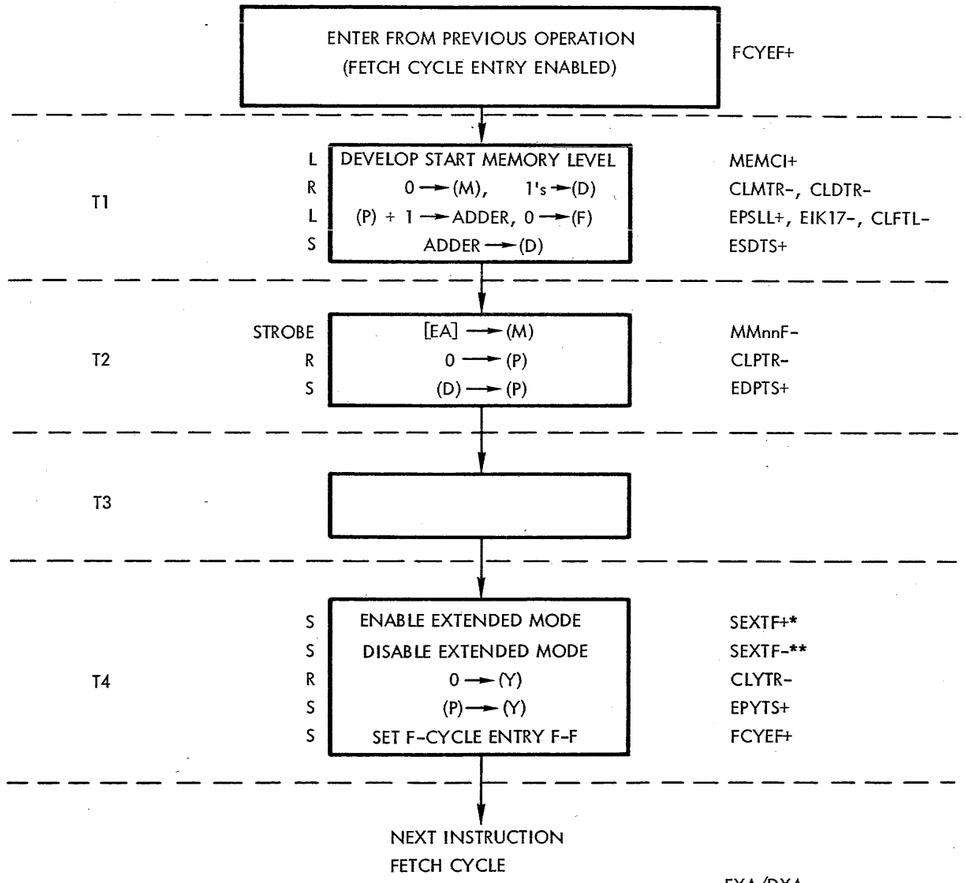
Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
INCSC+	126–P5	F	TL2	L	(FCYEF+)(TL2FF+)*	126–L5	121–A4	Increment shift counter
CLYTR–	129–P3	F	TL4	R	(ACYNX–)(TL4FF+)(MCRST+)	129–H3/ N3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(OPGJS–)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–) (IGACY+)	126–F12/ J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle

*Repeat T3 and T2 as required and enter T4.

See Page 2-46 for Common Shift Instruction Entry.

TABLE 2-1.
GENERATING OPGJS+ FOR SPECIFIC SKIP INSTRUCTIONS

Instruction	Op Code	Conditions for SKGRP+	Origin
Skip If C Set (SSC)	101001	(CB1TF+)(M16FF+)(MEMAC–) (SKGRP+)(M07FF+)	129–A10/H10
Skip If C reset (SRC)	100001	[(CB1TF+)(M16FF+)]–(MEMAC–) (SKGRP+)(M07FF–)	129–A10/H11
Skip If A_{16} = 1 (SLN)	101100	(A16FF+)(M10FF+)(MEMAC–) (SKGRP+)(M07FF+)	129–A4/H10
Skip If A_{16} = 0 (SLZ)	100100	[(A16FF+)(M10FF+)]–(MEMAC–) (M07FF–)	129–A4/H11
Skip If A Minus (SMI)	101400	(A01FF+)(M08FF+)(MEMAC–) (SKGRP+)(M07FF+)	129–A12/H10
Skip If A Plus (SPL)	100400	[(A01FF+)(M08FF+)]–(MEMAC–) (M07FF–)	129–A12/H11
Skip If A Not Zero (SNZ)	101040	(AZERO–)(M11FF+)(MEMAC–) (SKGRP+)(M07FF+)	129–B9/H10
Skip If A Zero (SZE)	100040	[(AZERO–)(M11FF+)] – (MEMAC–) (M07FF–)	129–B9/H11
Skip If Sense Switch 1 is Set (SS1)	101020	(SENS1+)(M12FF+)(MEMAC–) (SKGRP+)(M07FF+)	129–B5/H10
Skip If Sense Switch 1 is Reset (SR1)	100020	[(SENS1+)(M12FF+)]–(MEMAC–) M07FF–)	129–B5/H11
Skip If Sense Switch 2 is Set (SS2)	101010	(SENS2+)(M13FF+)(MEMAC–) (SKGRP+)(M07FF+)	129–B6/H10
Skip If Sense Switch 2 is Reset (SR2)	100010	[(SENS2+)(M13FF+)]–(MEMAC–) (M07FF–)	129–B6/H11
Skip If Sense Switch 3 is Set (SS3)	101004	(SENS3+)(M14FF+)(MEMAC–) (SKGRP+)(M07FF+)	129–B7/H10
Skip If Sense Switch 3 is Reset (SR3)	100004	[(SENS3+)(M14FF+)]–(MEMAC–) (M07FF–)	129–B7/H11
Skip If Sense Switch 4 is Set (SS4)	101002	(SENS4+)(M15FF+)(MEMAC–) (SKGRP+)(M07FF+)	129–B8/H10
Skip If Sense Switch 4 is Reset (SR4)	100002	[(SENS4+)(M15FF+)]–(MEMAC–) (M07FF–)	129–B8/H11
Skip If Any Sense Switch Set (SSS)	101036	(SENS1+)(M12FF+)V(SENS2+) (M13FF+) V(SENS3+)(M14FF+) V(SENS4+)(M15FF+)∧(MEMAC–) (SKGRP+)(M07FF+)	129–B6/B7/B8/ H10
Skip If Any Sense Switch Reset (SSR)	100036	[(SENS1+)(M12FF+)V(SENS2+) (M13FF+)V(SENS3+)–(M14FF+) V(SENS4+)(M15FF+)]∧(MEMAC–) (SKGRP+)(M07FF–)	129–B6/B7/B8/ H11
Unconditional Skip (SKP)	100000	(M08FF–) through (M16FF–) (MEMAC–) (SKGRP+) (M07FF–)	129–A3 through A11/H11
Skip If Memory Parity Error (SPS)	101200	(MPEFF–) (M09FF+) (MEMAC–) (SKGRP+) (M07FF+)	129–A1/A2/H10
Skip If No Memory Parity Error (SPN)	100200	(MPEFF–) (M09FF+) (MEMAC–) (SKGRP+) (M07FF–)	129–A1/A2/H11

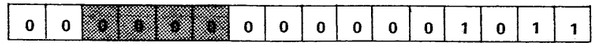


*APPLICABLE ONLY FOR EXA INSTRUCTION
WHEN COMPUTER IS EQUIPPED WITH
MEMORY EXPANSION OPTION

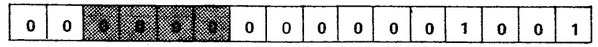
**APPLICABLE ONLY FOR DXA INSTRUCTION
WHEN COMPUTER IS EQUIPPED WITH
MEMORY EXPANSION OPTION

EXA/DXA
1 CYCLE
OP CODES 000013/000011

Instruction: Enable Extended Addressing (EXA)
Disable Extended Addressing (DXA)



Op Code: 000013 (EXA)
000011 (DXA)
Type G, 1 cycle

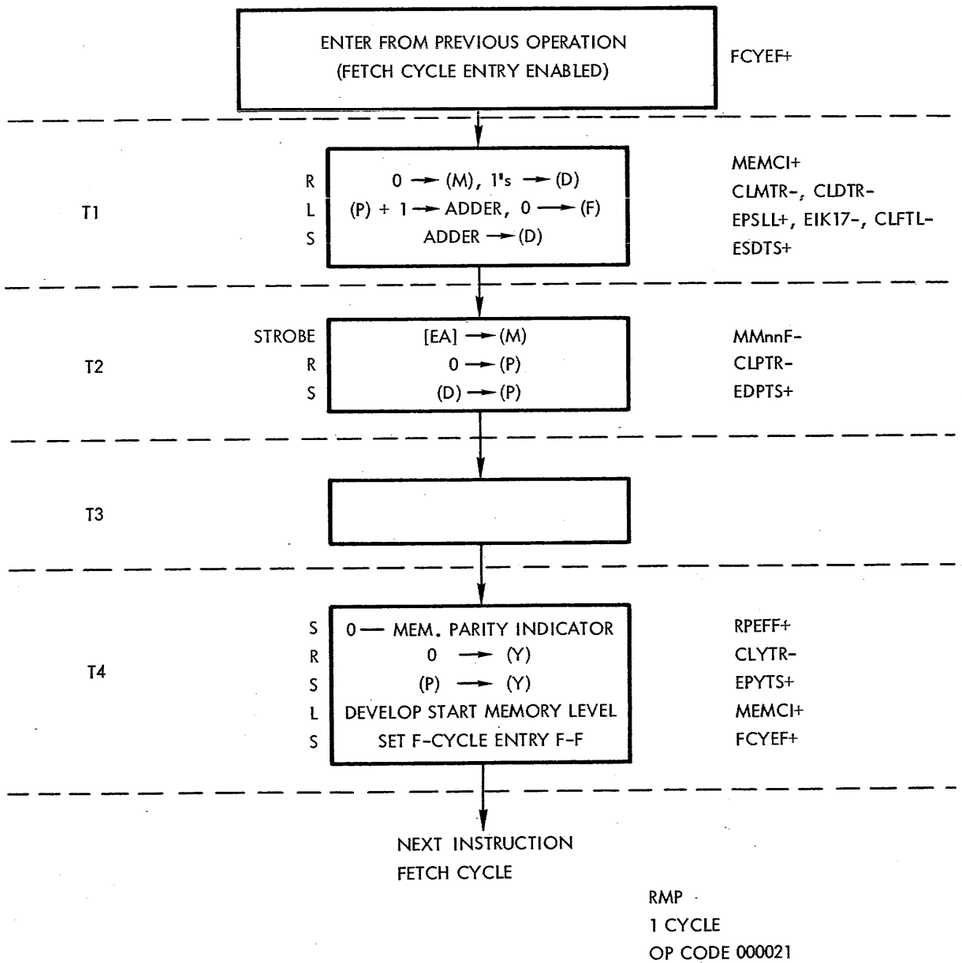


Description: EXA places computer in extend mode.
DXA restores computer to normal mode.

Execution Time (μs): 1.6

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
EPSLL+	128–K4	F	TLATE–	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P-register to adder
EIK17–	127–D5	F	TLATE–	L	(TLATE+)	127–K6	116–F7–F9	Force carry to adder
CLFTL–	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F-register Clear shift counter Clear AZZZZ flip-flop
CLMTR–	128–D9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M-register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF+)(TL1FF+)(MCRST+)	125–A6	101–116–F11	Clear D-register to ONEs
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF+)(TL1FF+)(MCSET+)	125–A5	101–116–F5/F9	Enable adder sum to D-register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M-register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZR0+)(MEMAC–)(MCRST+)	129–E7/L10	101–116–L12	Clear P-register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF+)(SCZR0+)(MEMAC–)(MCSET+)	129–E7/L10	101–116–J11	Enable D-register to P-register
SEXTF+*	136–G2	F	TL4	S	(GEN0B+)(TL4FF+)(M13FF+)(M15FF+)(MCSET+)	136–B3/D4	136–H2 136–M2	Enable set EXTMD flip-flop at next TL1 Enable set PMIND flip-flop
SEXTF–**	136–G2	F	TL4	S	(GEN0B+)(TL4FF+)(M13FF+)(M15FF+)(MCSET+)	136–B3/D4	136–H2 136–M2	Enable reset EXTMD flip-flop when next JMP is executed Enable reset PMIND flip-flop
CLYTR–	129–P3	F	TL4	R	(SCZR0+)(TL4FF+)(MCRST+)	129–E2	101–116–N12	Clear Y-register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)	129–E4	101–116–K11	Enable P-register to Y-register
MEMC1+	126–K12	F	TL1	L	(TL1FF+)(SPM0D–)(IGACY–)	126–F12	150–A2	Enable start memory cycle
COXXX+	150–D2	F	TL1	L	(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle

*Applicable for EXA instruction only
**Applicable for DXA instruction only



RMP
1 CYCLE
OP CODE 000021

Instruction: Reset Memory Parity Error (RMP)

OP Code: 000021 **Type:** G, 1 cycle

Description: Resets memory parity indicator

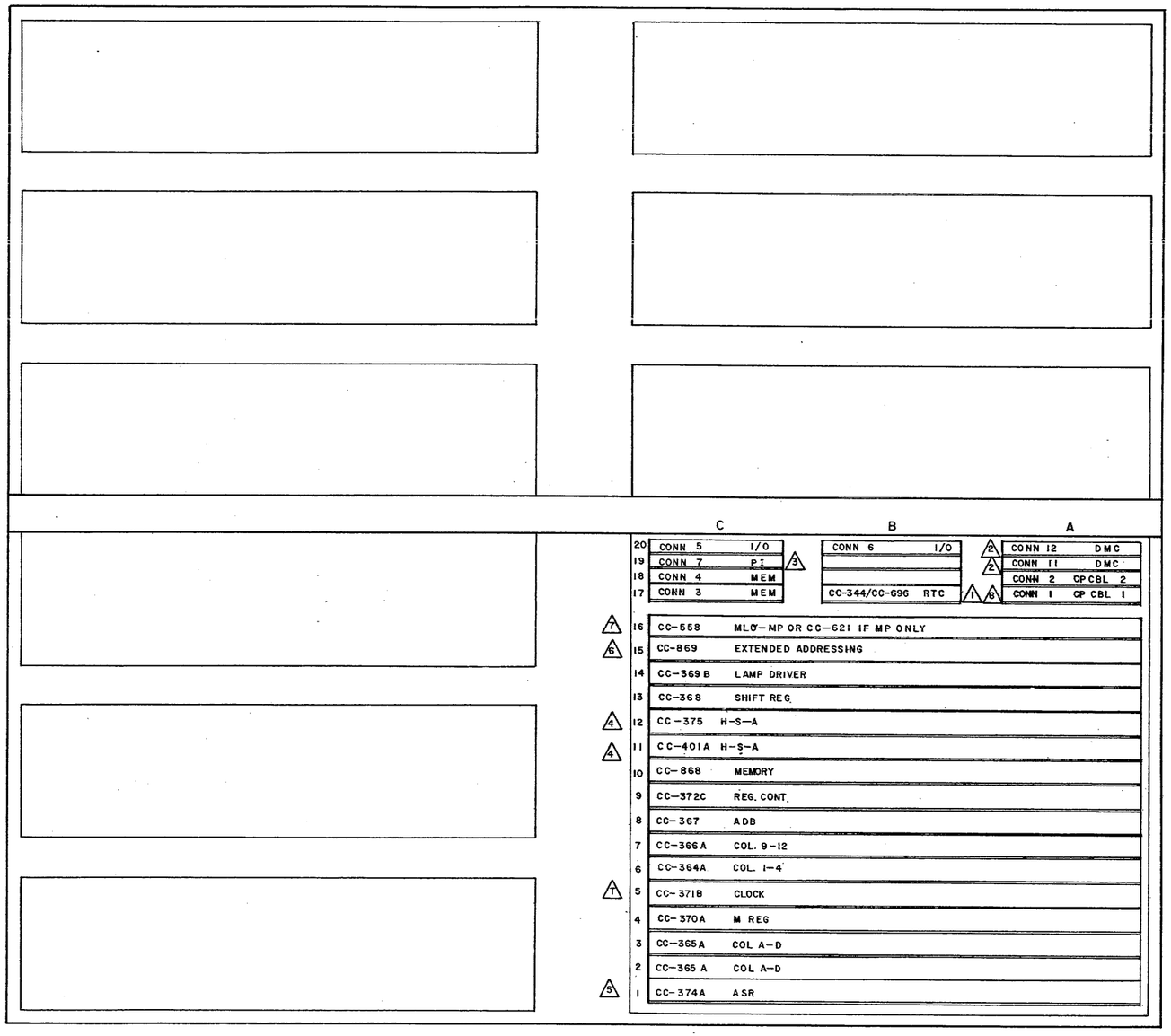
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Execution Time (μs): 1.6

Signal	Origin	Cyc	Tim	Clk	Signal Component	Origin	Destination	Operation
EPSLL+	128–K4	F	$\overline{\text{TLATE}}$	L	(FCYEF+)(TLATE–)	128–G3	101–116–A9	Enable P register to adder
EIK17–	127–P5	F	$\overline{\text{TLATE}}$	L	(TLATE–)	127–K6	116–F7-F9	Force carry to adder
CLMTR–	128–P9	F	TL1	R	(MCRST+)(HOLDM–)(TL1FF+)	128–P9	101–116–L9	Clear M register
CLDTR–	125–K5	F	TL1	R	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F11	Clear D register to ONEs
CLFTL	125–K8	F	TL1	L	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	120–A1 121–A5 125–D8	Clear F register Clear shift counter Clear AZZZZ FF
ESDTS+	125–M4	F	TL1	S	(ICYEF–)(ACYEF–)(TL1FF+)	125–A6	101–116–F5-F9	Enable adder sum to D register
MMnnF–	142				(SWnn±)(STRB–)	80.04	101–116–H8	Memory data set into M register
CLPTR–	129–M10	F	TL2	R	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCRST+)	129–E7/L10	101–116–L12	Clear P register
EDPTS+	129–P9	F	TL2	S	(FCYEF+)(TL2FF+)(SCZRO+)(MEMAC–)(MCSET+)	129–E7/L10	101–116–J11	Enable D register to P register
RPEFF+	133–E4	F	TL4	S	(GENOB+)(M12FF+)(TL4FF+)(MCSET+)	133–D4	133–G4	Reset memory parity error flip-flop
CLYTR–	129–P3	F	TL4	R	(SCZRO+)(TL4FF+)(MCRST+)	129–E1/H3	101–116–N12	Clear Y register
EPYTS+	129–P4	F	TL4	S	(PISEX–)(EOINS+)(TL4FF+)(OPGJS–)(MCSET+)	129–D4	101–116–L10	Enable P register to Y register
MEMCI+	126–K12	F	TL1	L	(TL1FF+)(SPMOD–); (IGACY+)	126–F12/J12	150–A2	Enable memory cycle
COXXX+	150–D2	F	TL1	L	(MCSET+)(MEMCI+)(MBSYX–)	150–A2	150–D2	Start memory cycle

SECTION IV
TYPE 316-0110 LOGIC BLOCK DIAGRAMS

This section contains all logic block diagrams for the Type 316-0110 central processor. These diagrams are tabulated in the contents at the front of this manual.



NOTES:

1. 702: REAL TIME CLOCK J-0012 CC-344
2. D.M.C. CABLE LOCATIONS
3. PRIORITY INTERRUPT CABLE LOCATION
4. 703: HSA
5. 704: ASR
6. EXTENDED ADDRESSING OPTION
7. MEM LOCKOUT AND MEM PARITY OPTION
8. 708 REAL TIME CLOCK J-1200CC-696

REV.	REVISIONS	CHK.
A	DATA BY ENG	

P70032793 | PARTS LIST

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. P BELBUSTI	DATE 8/22/72
ENG. M OLSEN	8/22/72
APP.	
PROJECT NO. 6014	

TITLE
H-316-0110
MF PAC COMP/ALLOC

SIZE	DWG NO.	REV.
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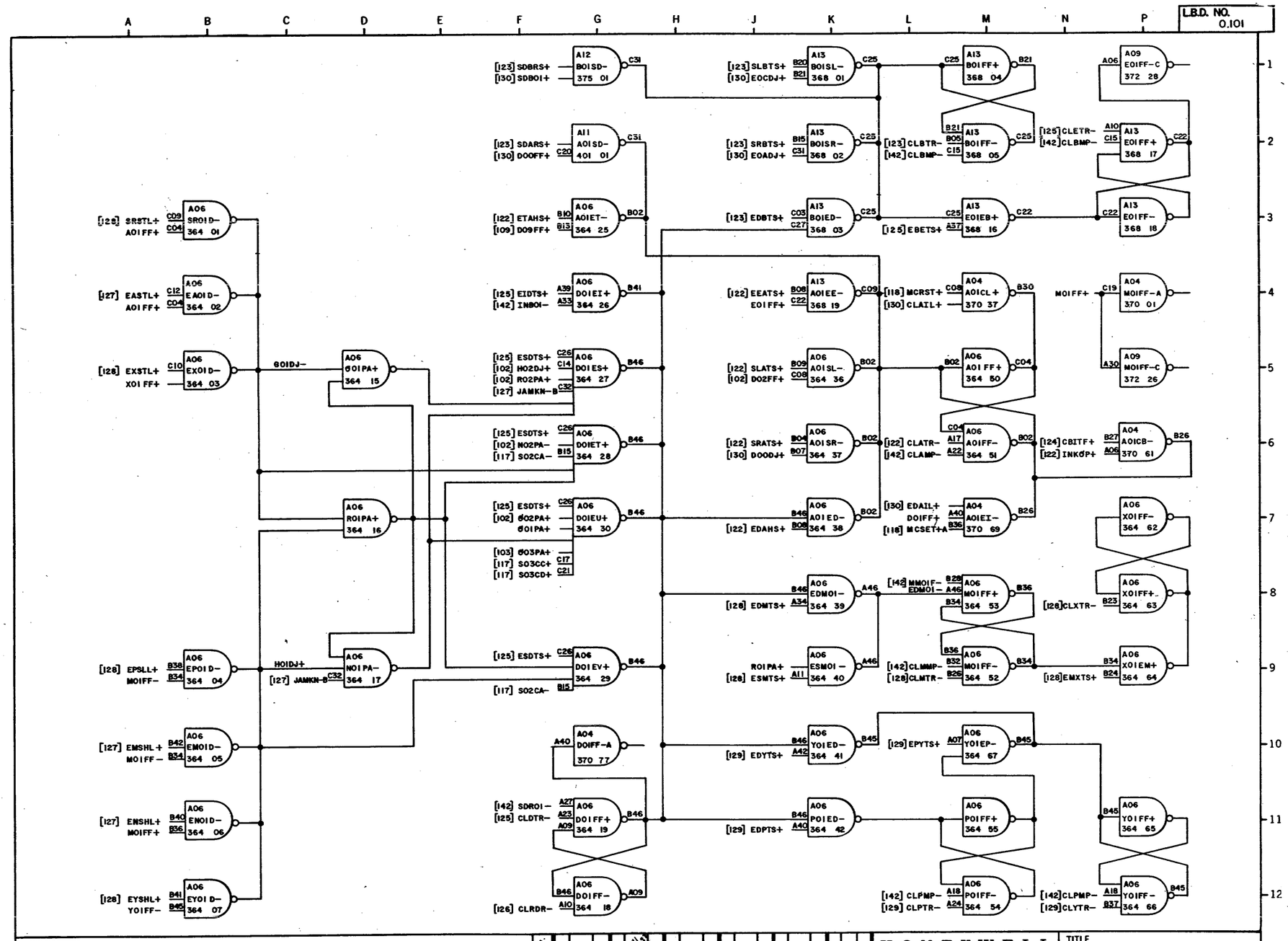
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A06 EX0ID- 364 03
A06 E0IPA+ 364 15
A06 R0IPA+ 364 16
A06 N0IPA- 364 17
A06 EP0ID- 364 04
A06 EM0ID- 364 05
A06 EN0ID- 364 06
A06 EY0ID- 364 07
A06 ET0ID- 364 25
A06 D0IEI+ 364 26
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A06 D0IET+ 364 28
A06 D0IEU+ 364 30
A06 D0IEV+ 364 29
A04 D0IFF-A 370 77
A06 D0IFF+ 364 19
A06 D0IFF- 364 18
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A13 B0ISR- 368 02
A13 E0IED- 368 03
A13 A0IEE- 368 19
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A06 EDM0I- 364 39
A06 ESM0I- 364 40
A06 Y0IED- 364 41
A06 P0IED- 364 42
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A13 B0IFF- 368 05
A13 E0IEB+ 368 16
A04 A0ICL+ 370 37
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A06 M0IFF- 364 52
A06 Y0IEP- 364 67
A06 P0IFF+ 364 55
A06 P0IFF- 364 54
A09 E0IFF-C 372 28
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A13 E0IFF- 368 18
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A09 M0IFF-C 372 26
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A06 Y0IFF+ 364 65
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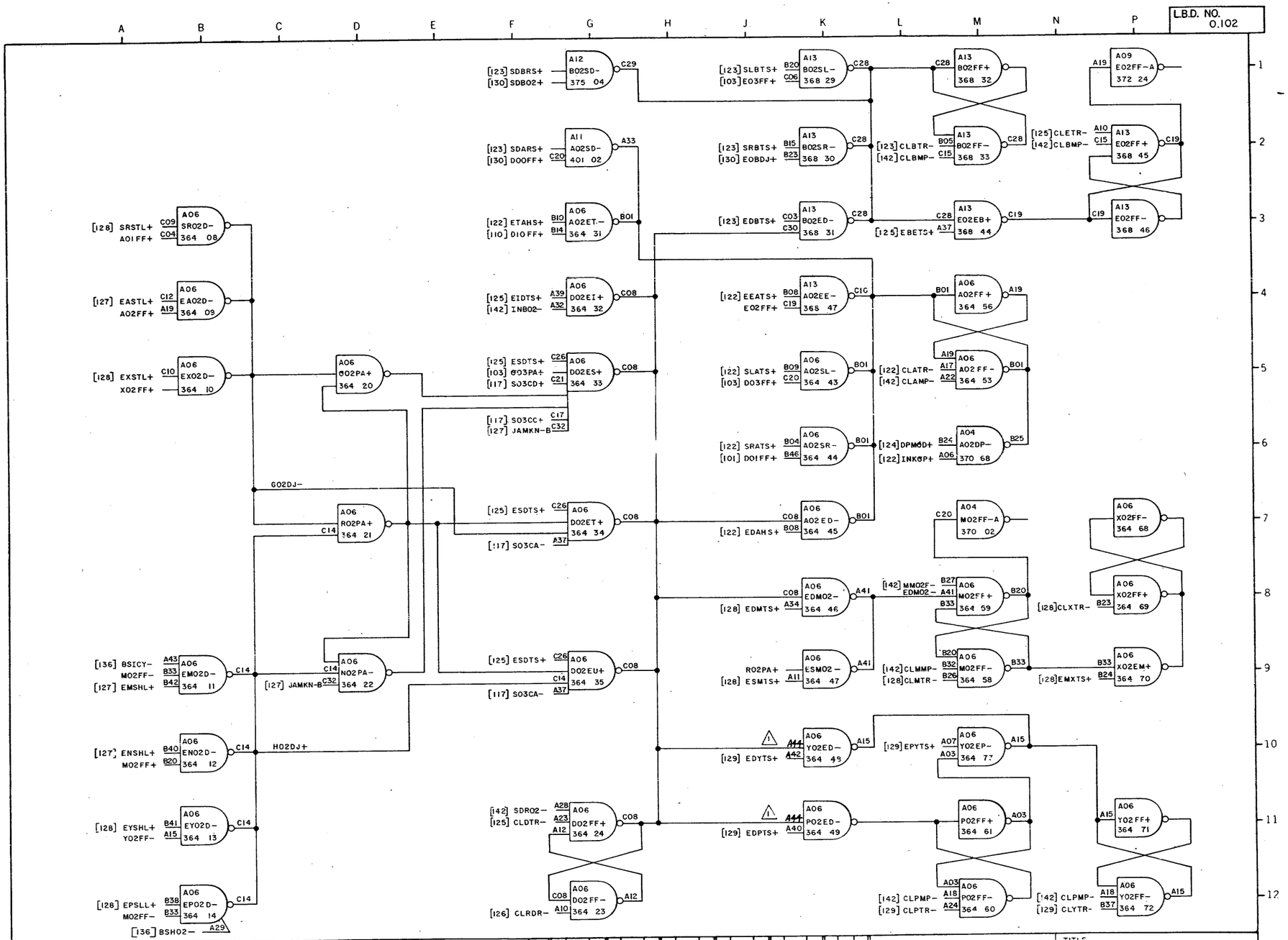
G0IDJ-
H0IDJ+ [127] JAMKN-B
NOTES:
REVISIONS
REV.
CHK.
S.R. 34-3585
ECO 7748
EXT CHANGES SEE ECO T.A.
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.
DR. D. HAMEL DATE 11-26-68
ENG. K. IZBICKI 11-26-68
APP. 7-2-69
PROJECT NO. 55202
TITLE
H-316
COLUMN No. 1
SIZE C
DWG NO. 70024485
REV. B

L.B.D. NO. 0.102



NOTES:

⚠1 DELETE D02FF+ AND ADD BSD02+ WITH EXT. ADD OPTION

△

△

△

REV.	REVISIONS	CHK
A	ORIG BY ENG	

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COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. JIM NICKERSON	DATE 2-16-73	
ENG. M. OLSEN		
APP.	2-16-73	
PROJECT NO. 6014		

TITLE
H-316-0110
COLUMN No. 2

SIZE C | DWG NO. 70033044 | REV. A

L.B.D. NO. 0.103

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A06 A03ET- 364 98 — [122] ETAHS+ [111] D11FF+ — B10 B11 — B03
A06 EA03D- 364 75 — [127] EASTL+ A03FF+ — C12 C13
A06 D03EI+ 364 99 — [125] EIDTS+ [142] IN803- — A39 A31 — C20
A06 EX03D- 364 76 — [128] EXSTL+ X03FF+ — C10
A06 803PA+ 364 88 — C11 C32
A06 D03ES+ 364 A0 — [125] ESDTS+ [117] S03CC+ [117] S03CD+ — C26 C17 C21 — C20
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G03DJ-
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A06 N03PA- 364 90 — [127] JAMKN-B — C32 — C11
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H03DJ+
A06 EP03D- 364 79 — [128] EPSLL+ P03FF- — B38 C01 — C22
A06 D03FF+ 364 92 — [142] SDR03- [125] CLDTR- — A25 A23 A13 — C20
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A13 B03SR- 368 58 — [123] SRBTS+ [102] E02FF+ — B15 C19 — C11
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A06 A03EE- 368 75 — [122] EEATS+ E03FF+ — B08 C06 — B46
A06 A03SL- 364 A8 — [122] SLATS+ [104] D04FF+ — B09 C25 — B03
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A06 EDM03- 364 B1 — [128] EDMTS+ — A34 — C20 — A45
A06 ESM03- 364 B2 — [128] ESMTS+ — A11 — R03PA+ — A45
A06 Y03ED- 364 B3 — [129] EDYTS+ — A42 — C20 — C02
A06 P03ED- 364 B4 — [129] EDPTS+ — A40 — C20 — C01

A13 B03FF+ 368 60 — C11
A13 B03FF- 368 61 — [123] CLBTR- [142] CLBMP- — B05 C15 — C11
A13 E03FB+ 368 72 — [125] EBETS+ — A37 — C11 — C06
A06 A03FF+ 364 C2 — B03 — C13
A06 A03FF- 364 C3 — C13 A17 A22 — B03
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[136] PMIND+ [122] INK6P+ — A05 A06 — A06 — B03
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A06 Y03FF+ 364 D7 — C02
A06 Y03FF- 364 D8 — [142] CLPMP- [129] CLYTR- — A18 A24 — C02
A06 X03FF- 364 D4
A06 X03FF+ 364 D5 — [128] CLXTR- — B23
A06 X03EM+ 364 D6 — [128] EMXTS+ — B24

NOTES:
1. THIS PT MUST BE GND. WITH NO EXT. ADD OPTION.

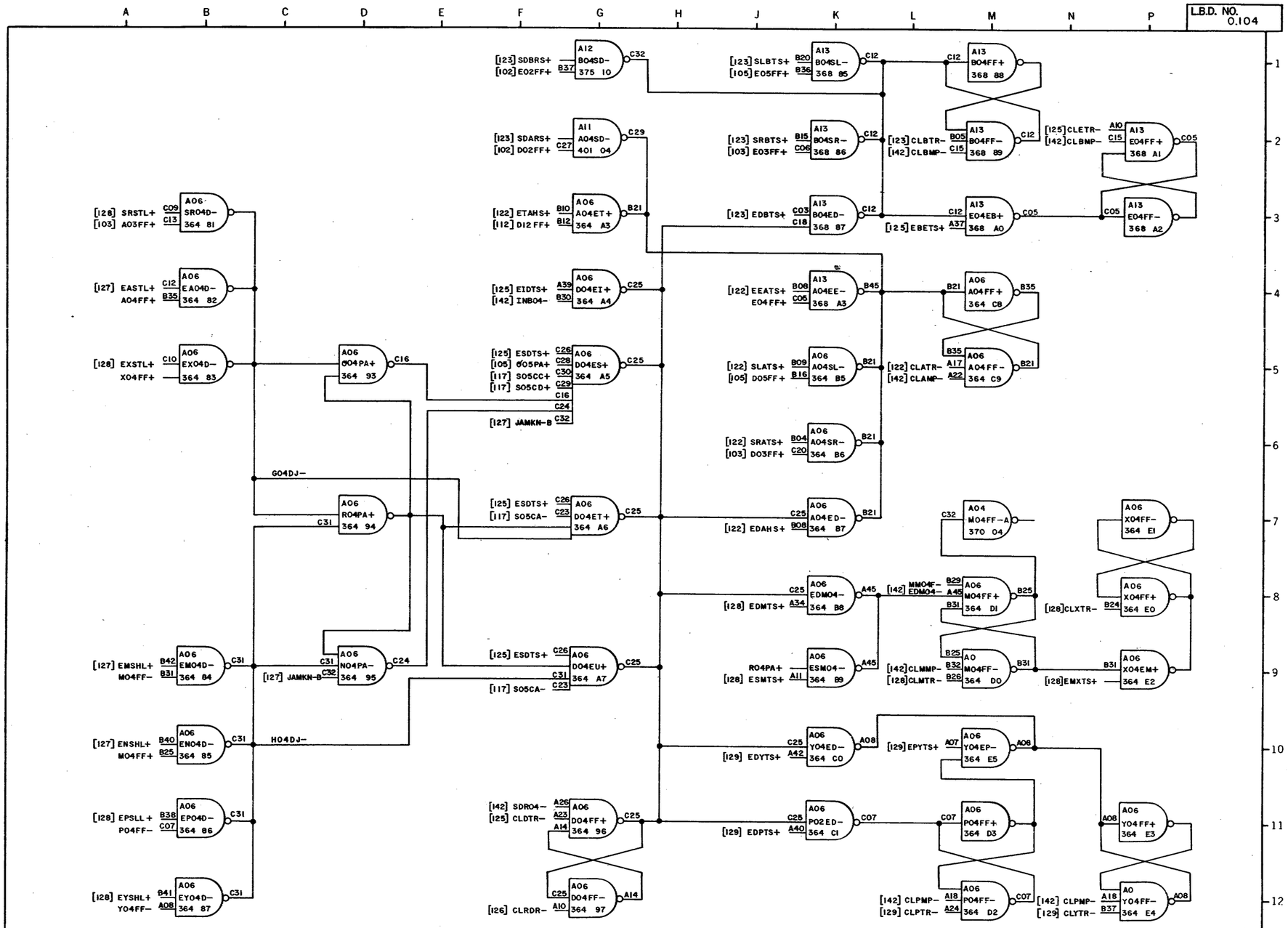
REVISIONS — REV. A — S.R. 54-3585 — ECO 7748 — REV. B — EXT. CHANGES SEE ECO T.A. 11/11/68 — CHK.

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. D. HAMEL	DATE 11-26-68	
ENG. K. IZBICKI	11-26-68	
APP.	12-6-68	
PROJECT NO. 55202		

TITLE: H-316 COLUMN No. 3

SIZE C — DWG NO. 70024487 — REV. B



NOTES:

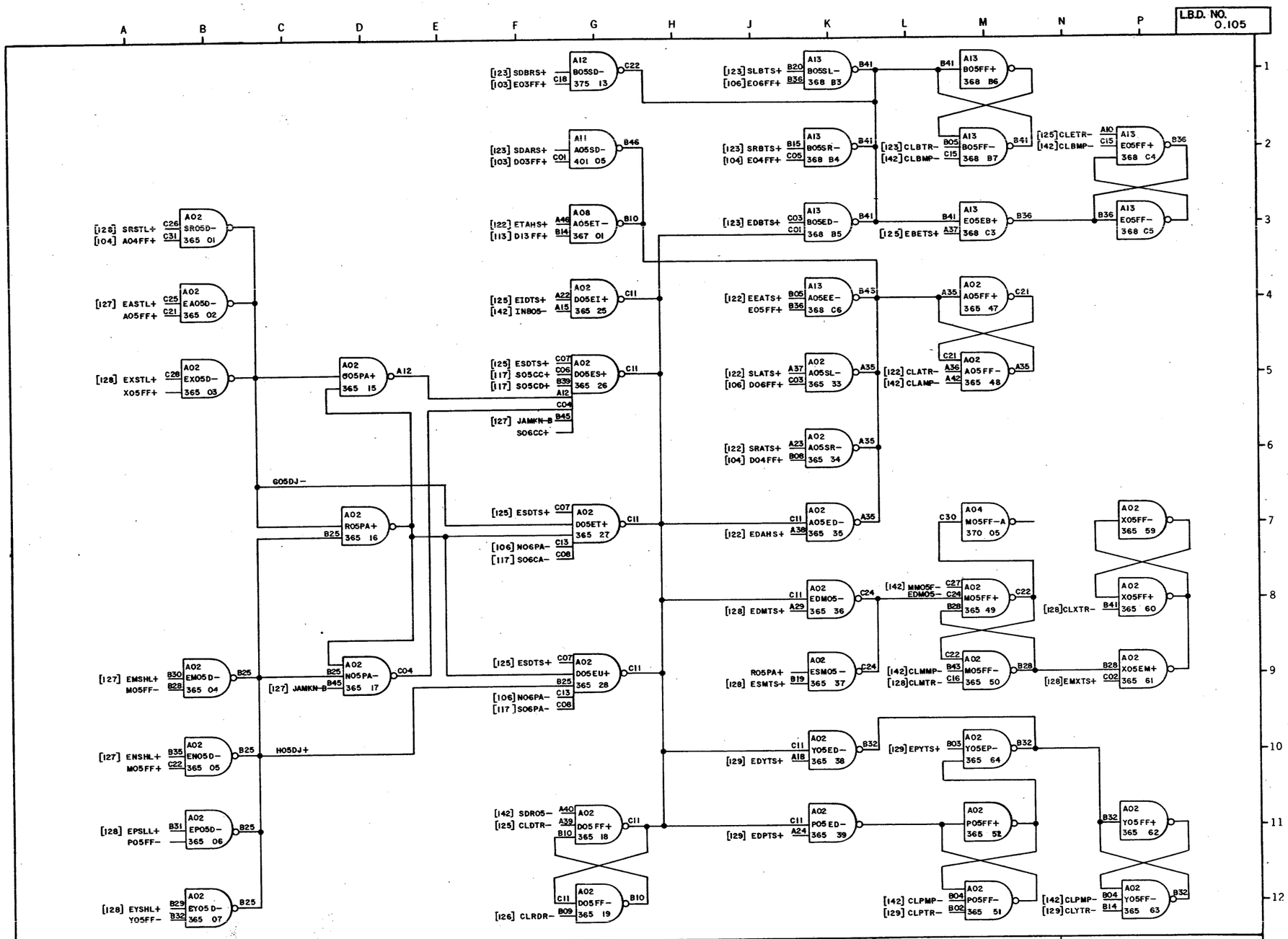
REVISIONS			
REV.	A	B	C
CHK.			
#	S.R. 54-3585	ECO 7748 EXT CHANGES SEE ECO T.K. 11/70	ECO 8302 EXT. CHGS SEE ECO 5/11/70 A.K.

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. D. HAMEL	DATE 11-26-68
ENG. K. IZBICKI	11-26-68
APP.	12-2-68
PROJECT NO. 55202	

TITLE
H-316
COLUMN No. 4

SIZE C | DWG NO. 70024488 | REV.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A11 A05SD- 401 05
A08 A05ET- 367 01
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A02 D05ES+ 365 26
A02 G05PA+ 365 15
A02 D05ET+ 365 27
A02 N05PA- 365 17
A02 D05EU+ 365 28
A02 D05FF+ 365 18
A02 D05FF- 365 19
A13 B05SL- 368 B3
A13 B05SR- 368 B4
A13 B05SD- 368 B5
A13 A05EE- 368 C6
A02 A05SL- 365 33
A02 A05SR- 365 34
A02 A05ED- 365 35
A02 EDM05- 365 36
A02 ESM05- 365 37
A02 Y05ED- 365 38
A02 P05ED- 365 39
A13 B05FF+ 368 B6
A13 B05FF- 368 B7
A13 E05EB+ 368 C3
A02 A05FF+ 365 47
A02 A05FF- 365 48
A04 M05FF-A 370 05
A02 M05FF+ 365 49
A02 M05FF- 365 50
A02 P05FF+ 365 52
A02 P05FF- 365 51
A13 E05FF+ 368 C4
A13 E05FF- 368 C5
A02 X05FF- 365 59
A02 X05FF+ 365 60
A02 X05EM+ 365 61
A02 Y05FF+ 365 62
A02 Y05FF- 365 63
A02 SR05D- 365 01
A02 EA05D- 365 02
A02 EX05D- 365 03
A02 EM05D- 365 04
A02 EM05D- 365 05
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A02 N05PA- 365 17
A02 H05PA+ 365 18
A02 Y05EP- 365 64
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[125] ESDTS+ [117] S05CC+ [117] S05CD+
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[125] ESDTS+
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[129] EDPTS+
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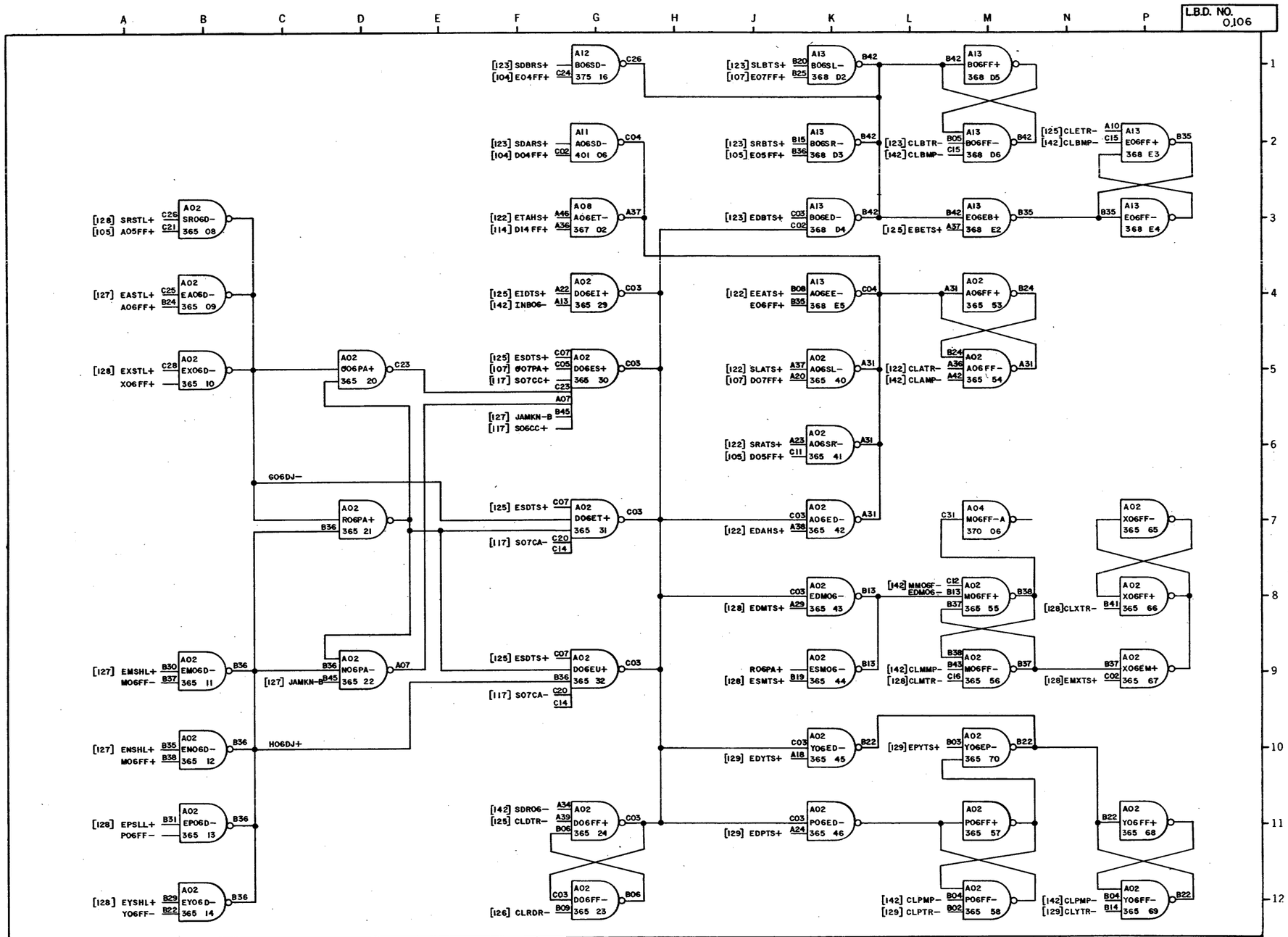
G05DJ-
H05DJ+
[127] JAMKN-B
NOTES:
REVISIONS
REV.
CHK.
S.R. 54-3585
ECO 7748
EXT. CHANGES SEE ECO T.A.
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass
DR. D. HAMEL DATE 11-26-68
ENG. K. IZBICKI 11-26-68
APP. 7-2-69
PROJECT NO. 55202
TITLE
H-316
COLUMN No. 5
SIZE C
DWG NO. 70024489
REV. B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A11 A06SD- 401 06
A08 A06ET- 367 02
A02 D06EI+ 365 29
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A02 D06ET+ 365 31
A02 D06EU+ 365 32
A02 D06FF+ 365 24
A02 D06FF- 365 23
A02 S06PA+ 365 20
A02 R06PA+ 365 21
A02 N06PA- 365 22
A02 SR06D- 365 08
A02 EA06D- 365 09
A02 EX06D- 365 10
A02 EM06D- 365 11
A02 EN06D- 365 12
A02 EP06D- 365 13
A02 EY06D- 365 14
A13 B06SL- 368 D2
A13 B06SR- 368 D3
A13 B06ED- 368 D4
A13 A06EE- 368 E5
A02 A06SL- 365 40
A02 A06SR- 365 41
A02 A06ED- 365 42
A02 EDM06- 365 43
A02 ESM06- 365 44
A02 Y06ED- 365 45
A02 P06ED- 365 46
A13 B06FF+ 368 D5
A13 B06FF- 368 D6
A13 E06EB+ 368 E2
A02 A06FF+ 365 53
A02 A06FF- 365 54
A02 M06FF+ 365 55
A02 M06FF- 365 56
A02 Y06EP- 365 70
A02 P06FF+ 365 57
A02 P06FF- 365 58
A13 E06FF+ 368 E3
A13 E06FF- 368 E4
A04 M06FF-A 370 06
A02 X06FF- 365 65
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A02 X06EM+ 365 67
A02 Y06FF+ 365 68
A02 Y06FF- 365 69
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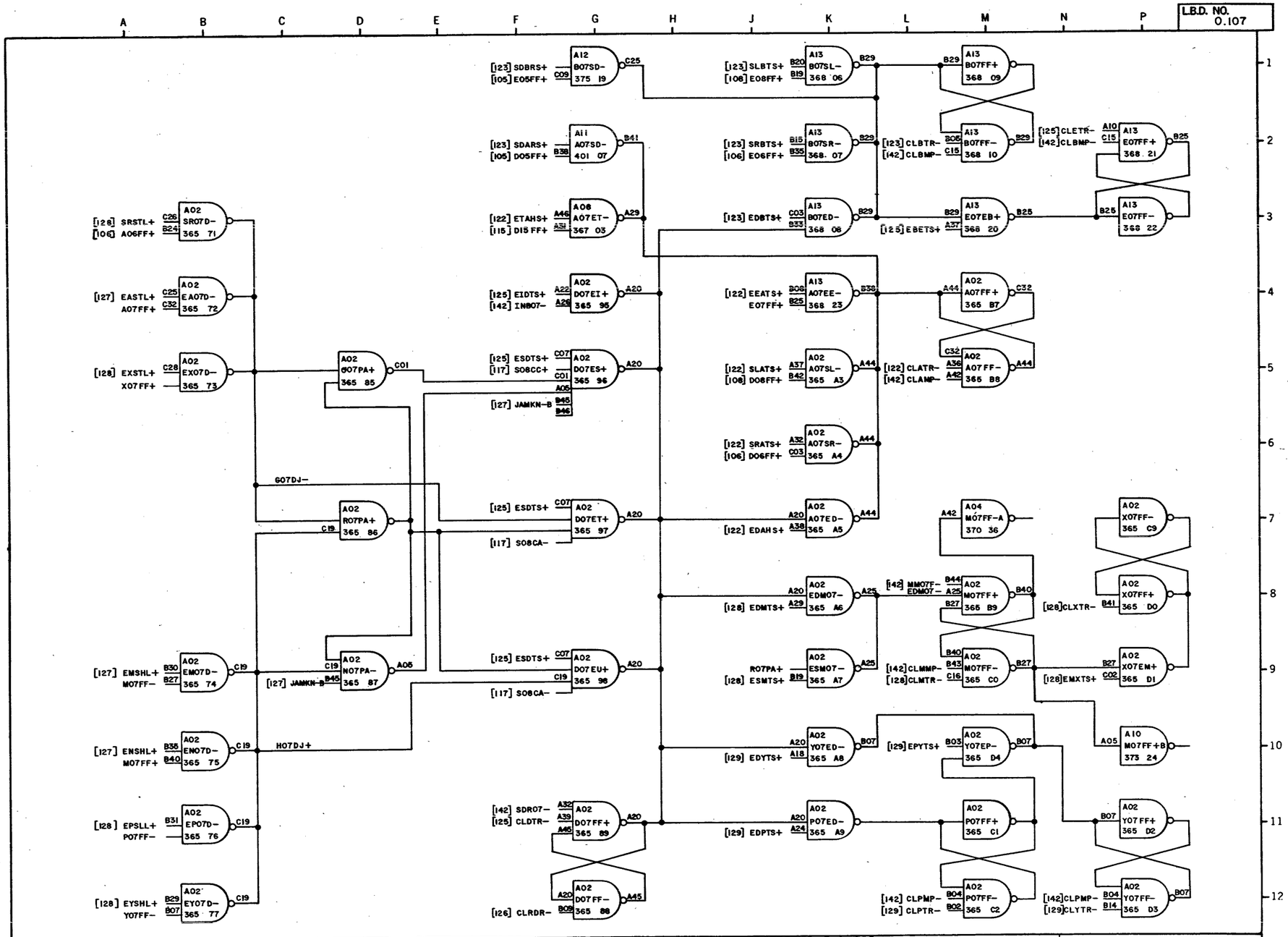
G06DJ-
H06DJ+
NOTES:
REVISIONS
REV. A
S.R. 54-385
ECO 7748
REV. B
EXT CHANGE 11/1/68 SEE ECO I.A.
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.
DR. D. HAMEL DATE 11-26-68
ENG. K. IZBICKI 11-26-68
APP. 7-2-69
PROJECT NO. 55202
TITLE
H-316
COLUMN No. 6
SIZE C
DWG NO. 7024490
REV. B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A13 B07SL- 368 06
A13 B07FF+ 368 09
Ai1 A07SD- 401 07
A13 B07SR- 368. 07
A13 B07FF- 368 10
A13 E07FF+ 368. 21
A08 A07ET- 367 03
A13 B07ED- 368 08
A13 E07EB+ 368 20
A13 E07FF- 368 22
A02 SR07D- 365 71
A02 D07EI+ 365 95
A02 A07EE- 368 23
A02 A07FF+ 365 87
A02 EA07D- 365 72
A02 EX07D- 365 73
A02 G07PA+ 365 85
A02 D07ES+ 365 96
A02 A07SL- 365 A3
A02 A07FF- 365 B8
A02 D07ET+ 365 97
A02 A07SR- 365 A4
A02 R07PA+ 365 86
A02 A07ED- 365 A5
A04 M07FF-A 370 36
A02 X07FF- 365 C9
A02 EDM07- 365 A6
A02 M07FF+ 365 B9
A02 X07FF+ 365 D0
A02 N07PA- 365 87
A02 D07EU+ 365 98
A02 ESM07- 365 A7
A02 M07FF- 365 C0
A02 X07EM+ 365 D1
A02 EM07D- 365 74
A02 Y07ED- 365 A8
A02 Y07EP- 365 D4
A10 M07FF+8 373 24
A02 D07FF+ 365 89
A02 P07ED- 365 A9
A02 P07FF+ 365 C1
A02 Y07FF+ 365 D2
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[142] CLAMP-
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X07FF+
G07DJ-
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R07PA+
[125] ESDTS+
[117] S08CA-
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EDM07-
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M07FF-
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[117] S08CA-
R07PA+
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H07DJ+
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Y07FF-
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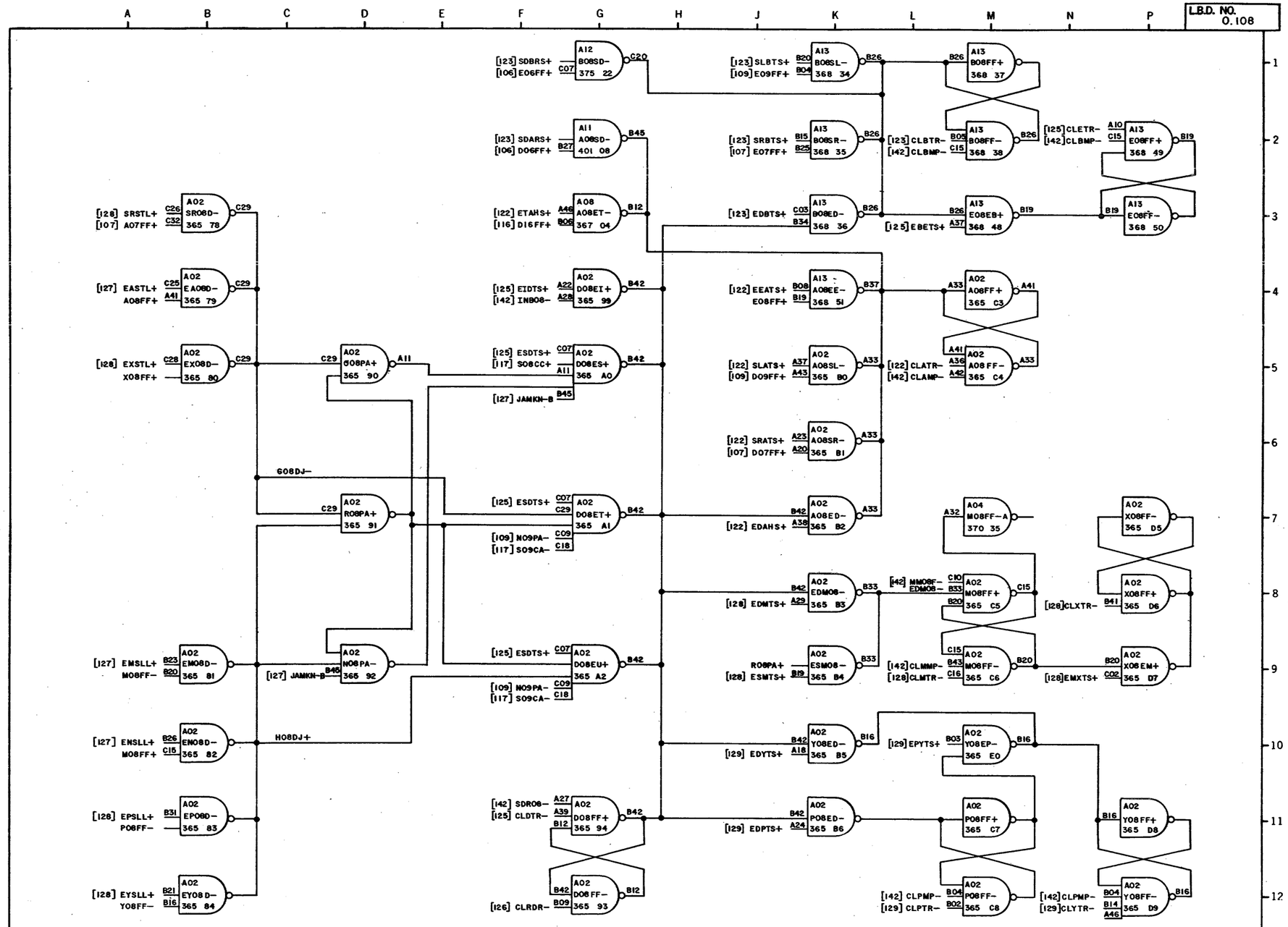
NOTES:
REVISIONS
REV.
CHK.
S.R. 54-3565
ECO 7748
EXT. CHANGES SEE ECO T.A.
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass
DR. D. HAMEL
DATE 11-26-68
ENG. K. IZBICKI
11-26-68
APP.
7-2-69
PROJECT NO. 55202
TITLE
H-316
COLUMN No. 7
SIZE C
DWG NO. 10024491
REV. L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A02 EY08D- 365 84
A02 608PA+ 365 90
A02 R08PA+ 365 91
A02 N08PA- 365 92
A11 A08SD- 401 08
A08 A08ET- 367 04
A02 D08EI+ 365 98
A02 D08ES+ 365 A0
A02 D08ET+ 365 A1
A02 D08EU+ 365 A2
A02 D08FF+ 365 94
A02 D08FF- 365 93
A12 B08SD- 375 22
A13 B08SL- 368 34
A13 B08SR- 368 35
A13 B08ED- 368 36
A13 A08EE- 368 51
A02 A08SL- 365 B0
A02 A08SR- 365 B1
A02 A08ED- 365 B2
A02 EDM08- 365 B3
A02 ESM08- 365 B4
A02 Y08ED- 365 B5
A02 P08ED- 365 B6
A13 B08FF+ 368 37
A13 B08FF- 368 38
A13 E08EB+ 368 48
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A02 M08FF+ 365 C5
A02 M08FF- 365 C6
A02 P08FF+ 365 C7
A02 P08FF- 365 C8
A02 Y08EP- 365 E0
A13 E08FF+ 368 49
A13 E08FF- 368 50
A04 M08FF-A 370 35
A02 X08FF+ 365 D5
A02 X08FF- 365 D6
A02 X08EM+ 365 D7
A02 Y08FF+ 365 D8
A02 Y08FF- 365 D9
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R08PA+ [128] ESMTS+
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608DJ-
H08DJ+
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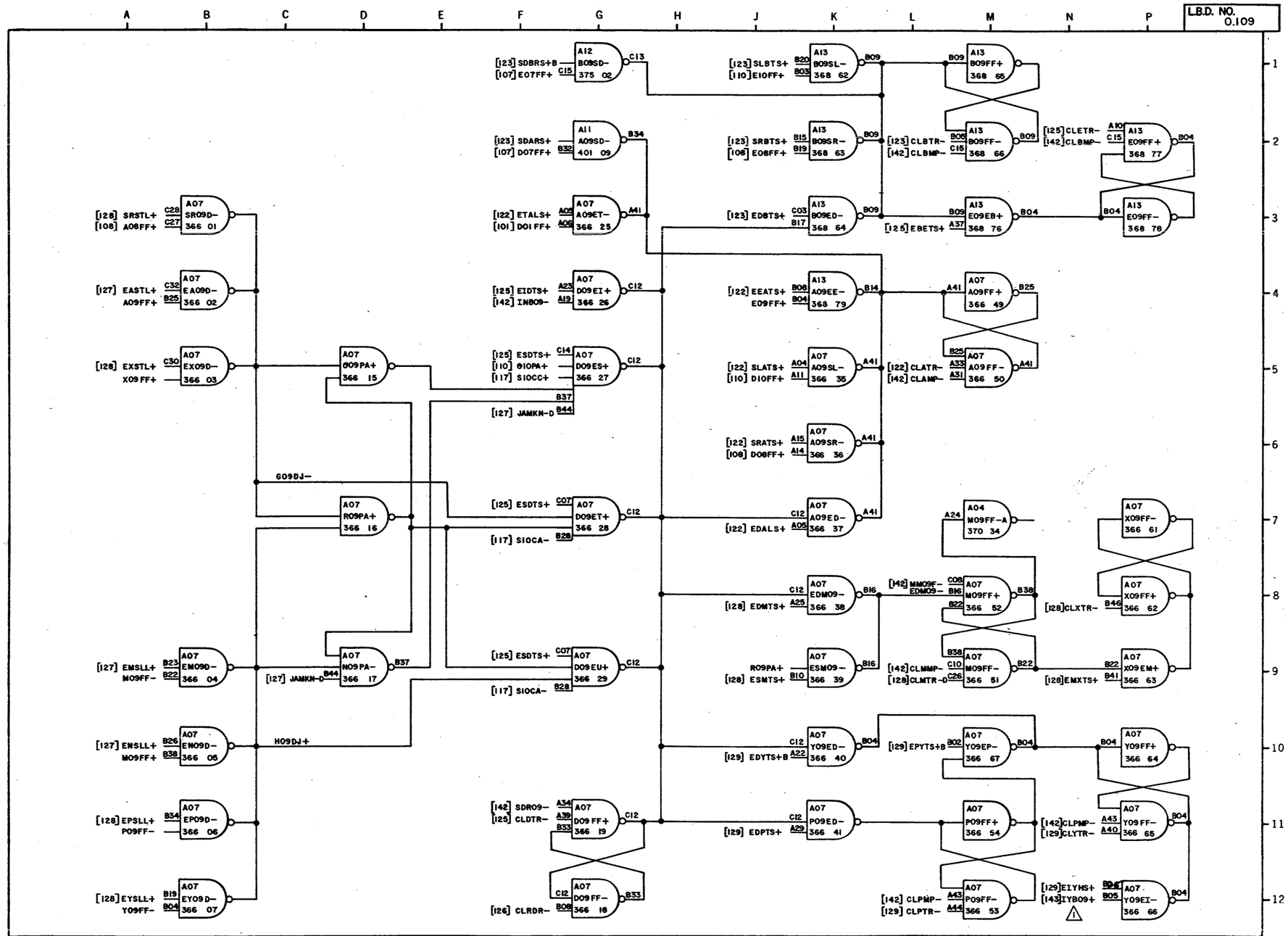
NOTES:
REVISIONS
S.R. 54-3585
ECO 7748
EXT. CHANGES SEE ECO FT.
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass
DR. D. HAMEL DATE 11-26-68
ENG. K. IZBICKI 11-26-68
APP. 12-2-69
PROJECT NO. 55202
TITLE
H-316
COLUMN No. 8
SIZE C
DWG NO. 7002 4492
REV. B



NOTES:

1. THIS PT. IS GND. WITH NO DMC OPTION

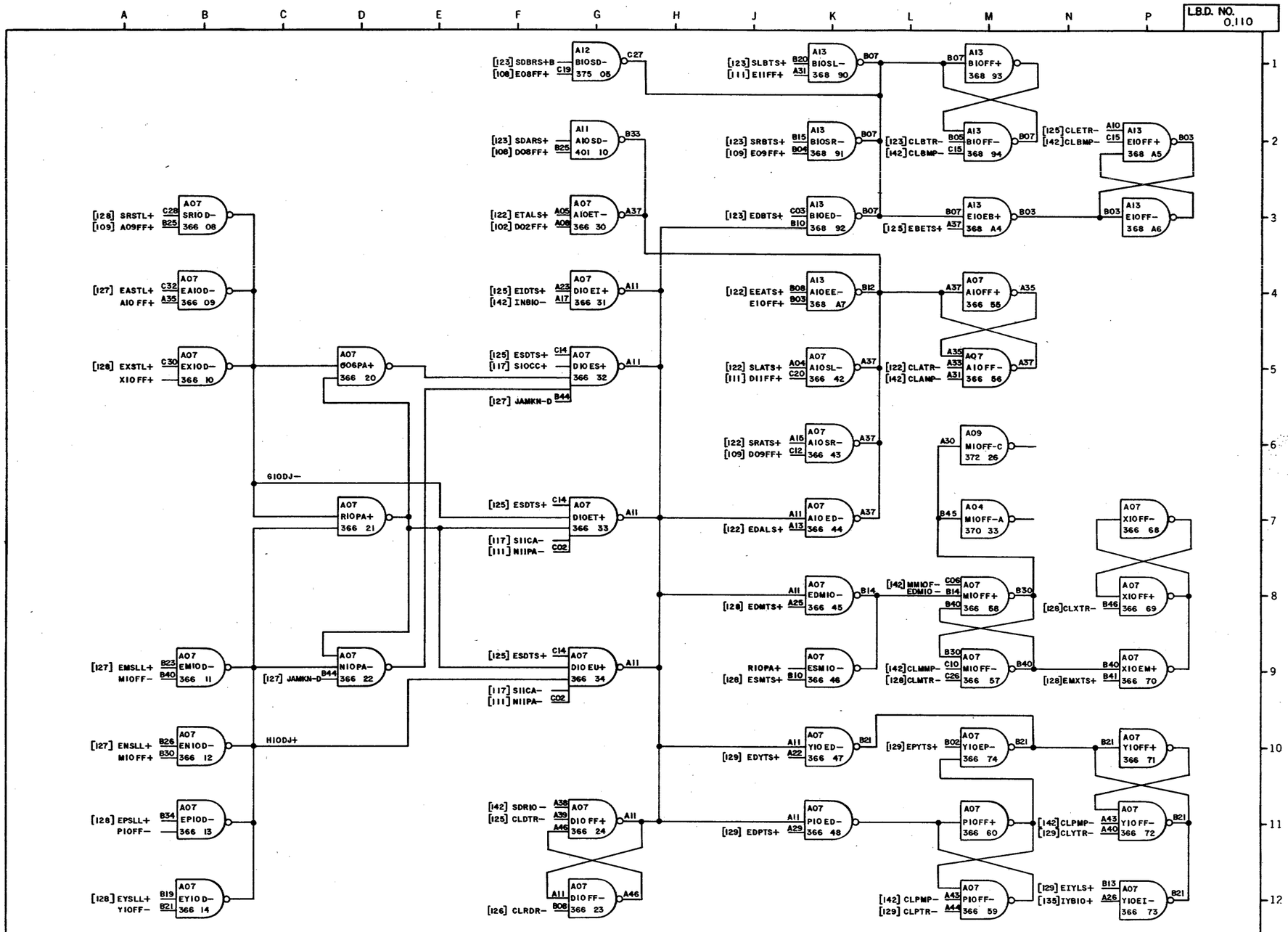
REV.	REVISIONS	C+K	
A	S.R. 54-3565		
B	ECO 7728 EXT. CHANGES SEE ECO T.A.		

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. D. HAMEL	DATE 11-26-68
ENG. K. IZBICKI	11-26-68
APP.	12-2-69
PROJECT NO. 58202	

TITLE
H-316
COLUMN No. 9

SIZE C | DWG NO. C70024493 | REV. B



NOTES:

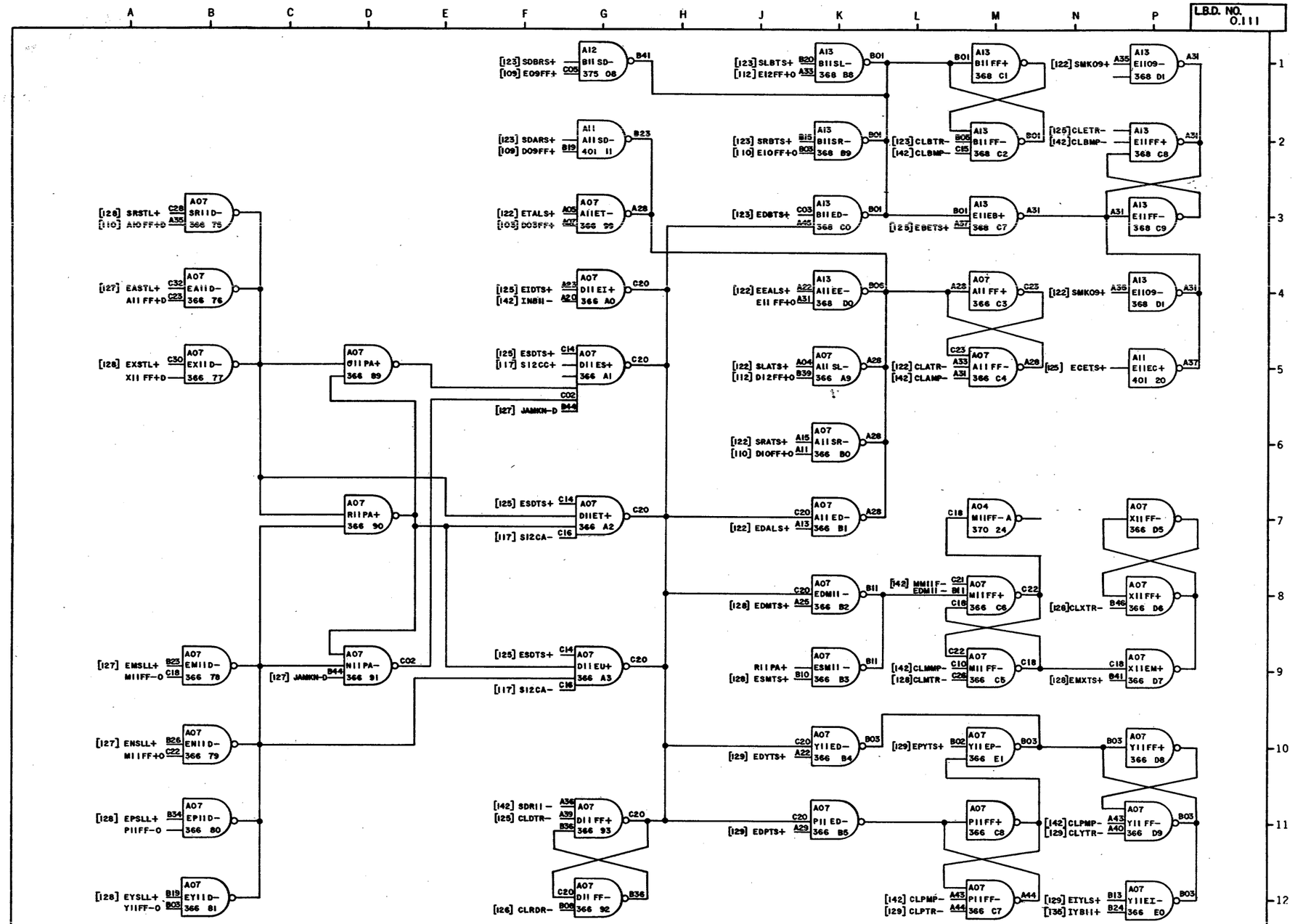
REV.	REVISIONS	CHK.
A	S.R. 54-3585	
B	ECO 7748 EXT CHANGES SEE ECO T.A.	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. D. HAMEL	DATE 11-26-68	
ENG. K. IZBICKI	11-26-68	
APP.	12-2-69	
PROJECT NO. 55202		

TITLE
H-316
COLUMN No. 10

SIZE C | DWG NO. 7002494 | REV. B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[127] ENSLL+ M11FF+0 B26 C22 A07 EN11D- 366 79
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[128] EYSLL+ Y11FF-0 B19 B03 A07 EY11D- 366 81
A07 S11PA+ 366 89
A07 R11PA+ 366 90
A07 N11PA- 366 91
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[126] CLRDR- B06 A07 D11 FF- 366 92 B36
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[129] EDYTS+ A22 A07 Y11ED- 366 B4 B03
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A07 P11FF+ 366 C8
A07 P11FF- 366 C7 A44
A04 M11FF-A 370 24 C18
A07 X11FF- 366 D5
A07 X11FF+ 366 D6
A07 X11EM+ 366 D7
A07 Y11FF+ 366 D8
A07 Y11 FF- 366 D9 B03
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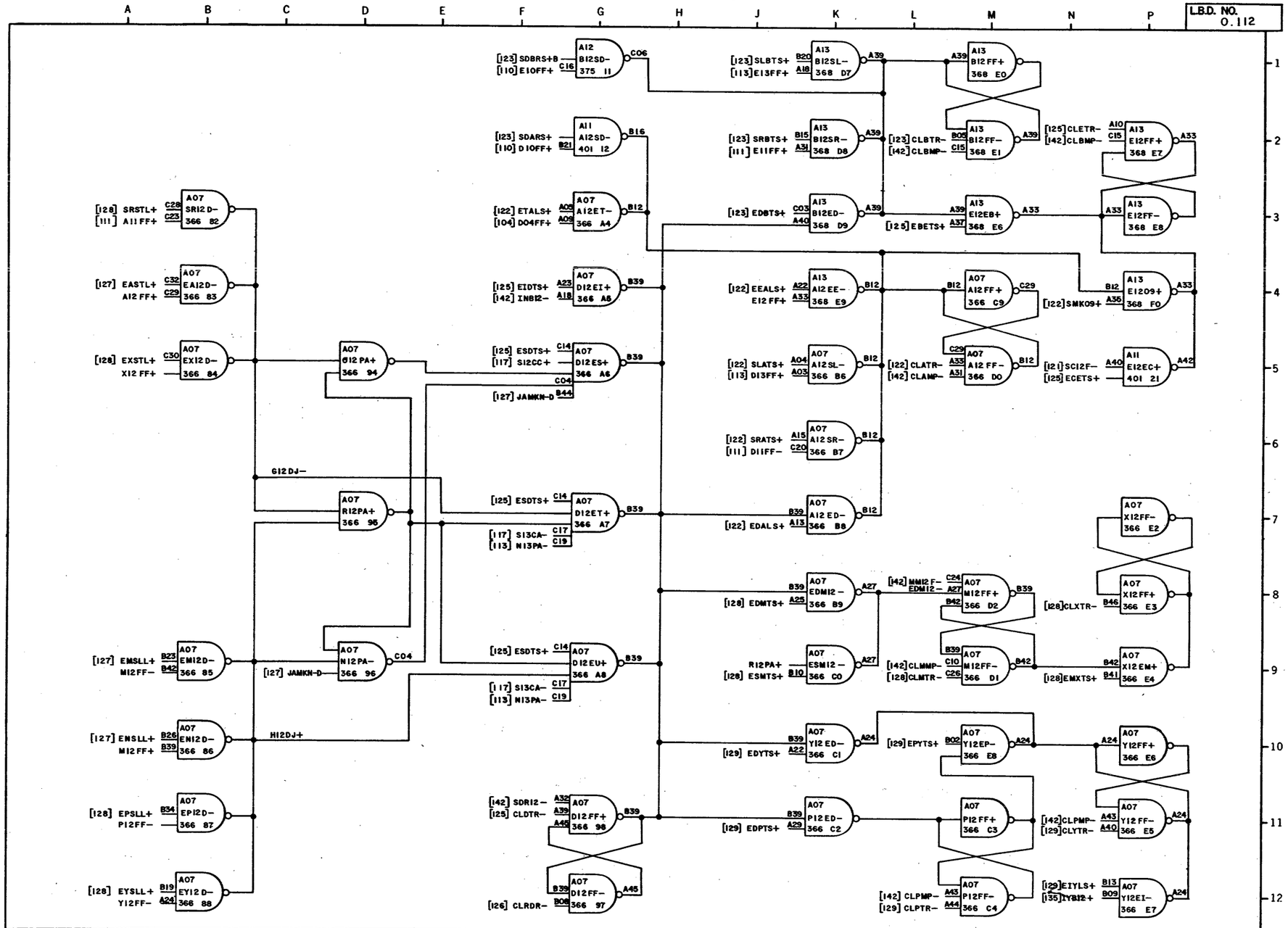
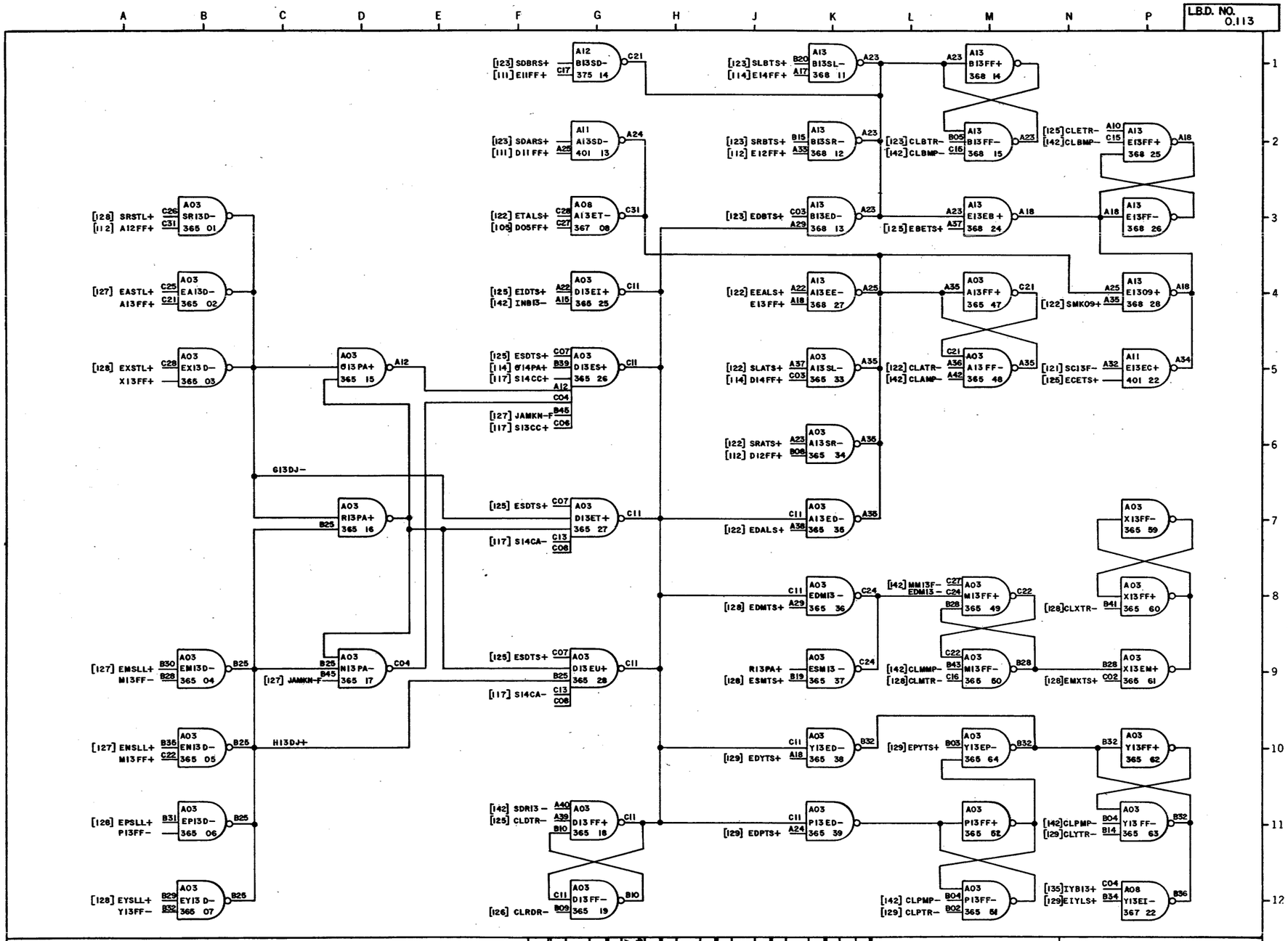
NOTES:
REVISIONS REV. A B CHK.
S.R. 54-3585
ECO 7748
EXT CHANGES SEE ECO T.A.
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass
DR. D. HAMEL DATE 11-26-68
ENG. K. IZBICKI 11-26-68
APP. 7-2-69
PROJECT NO. 55202
TITLE
H-316
COLUMN No. 11
SIZE DWG NO. REV.
C 7002 4495 B


L.B.D. NO. 0.112
A07 SR12D- 366 82
A07 EA12D- 366 83
A07 EX12D- 366 84
A07 EM12D- 366 85
A07 EN12D- 366 86
A07 EP12D- 366 87
A07 EY12D- 366 88
A07 612PA+ 366 94
A07 R12PA+ 366 95
A07 N12PA- 366 96
A07 D12FF- 366 97
A07 D12FF+ 366 98
A07 D12ET+ 366 A7
A07 D12EU+ 366 A8
A07 D12ES+ 366 A6
A07 D12EI+ 366 A5
A07 A12ET- 366 A4
A07 A12SR- 366 B7
A07 A12SL- 366 B6
A07 A12ED- 366 B8
A07 A12EE- 368 E9
A07 A12FF+ 366 C9
A07 A12FF- 366 DO
A07 P12ED- 366 C2
A07 P12FF+ 366 C3
A07 P12FF- 366 C4
A07 Y12ED- 366 C1
A07 Y12EP- 366 E8
A07 EDM12- 366 B9
A07 ESM12- 366 CO
A07 M12FF+ 366 D2
A07 M12FF- 366 D1
A07 X12FF- 366 E2
A07 X12FF+ 366 E3
A07 X12EM+ 366 E4
A07 Y12FF+ 366 E6
A07 Y12FF- 366 E5
A07 Y12EI- 366 E7
A11 A12SD- 401 12
A11 E12EC+ 401 21
A13 B12SL- 368 D7
A13 B12FF+ 368 EO
A13 B12SR- 368 D8
A13 B12FF- 368 E1
A13 B12ED- 368 D9
A13 E12EB+ 368 E6
A13 E12FF+ 368 E7
A13 E12FF- 368 E8
A13 E1209+ 368 FO
A13 E12EI- 368 E9
612DJ-
H12DJ+
NOTES:
REVISIONS
S.R. 54-3585
ECO 7748
EXT CHANGES SEE ECO A.T.
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass
DR. D. HAMEL
ENG. K. IZBICKI
APP.
PROJECT NO. 56202
DATE 11-26-68
11-26-68
9-2-69
TITLE
H-316
COLUMN No. 12
SIZE C
DWG NO. 70024496
REV. B

L.B.D. NO. 0.113



NOTES:

△
△
△
△

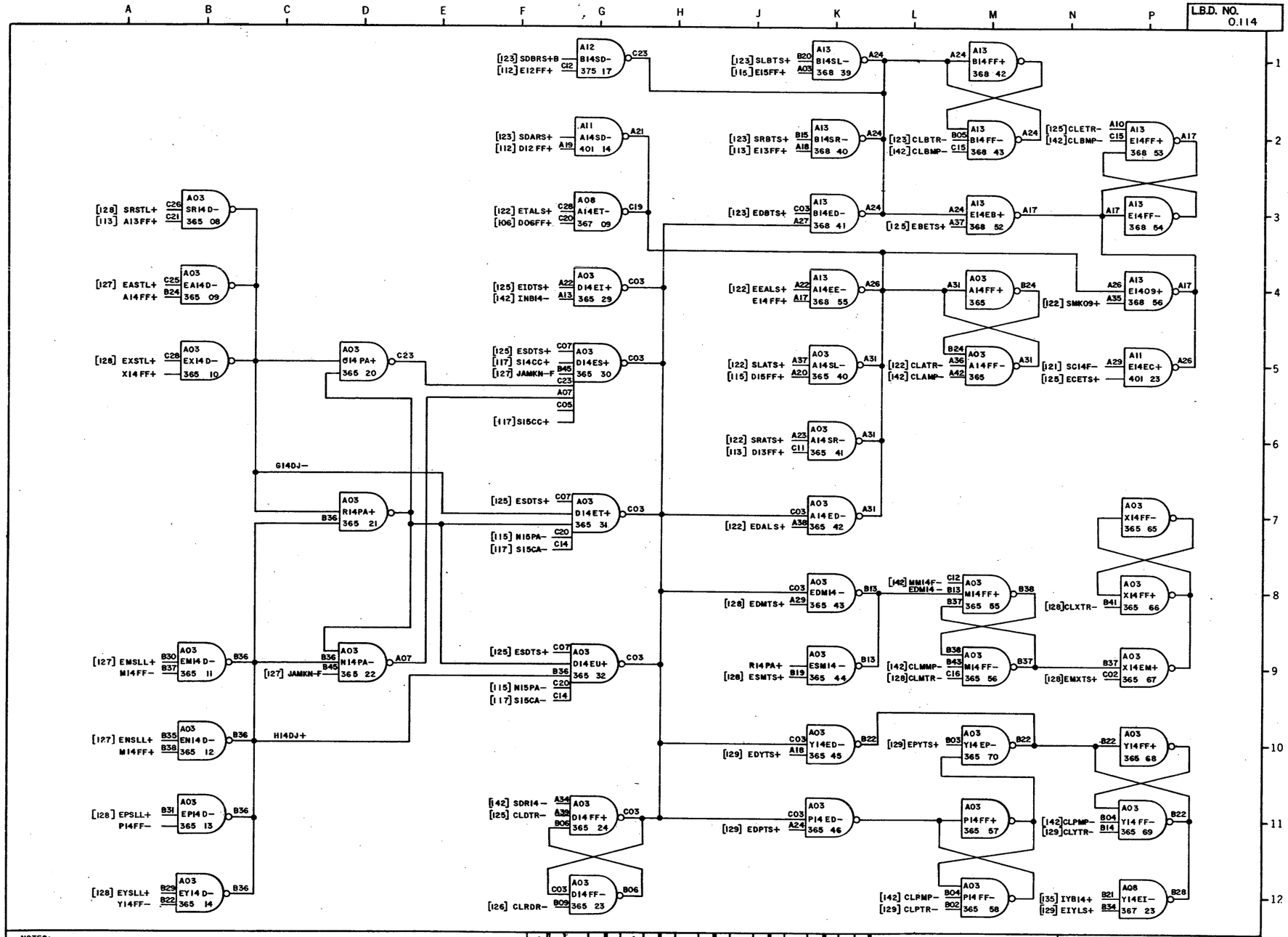
REV.	REVISIONS	CHK.
A	S.R. 54-3585	
B	ECO 7748 CHANGES I/W/O EXT SEE E.C.O. T.A.	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. D. HAMEL	DATE 11-26-68
ENG. K. IZBICKI	11-26-68
APP.	7-2-69
PROJECT NO. 55202	

TITLE
H-316
COLUMN No. 13

SIZE	DWG NO.	REV.
C	70024497	D



NOTES:

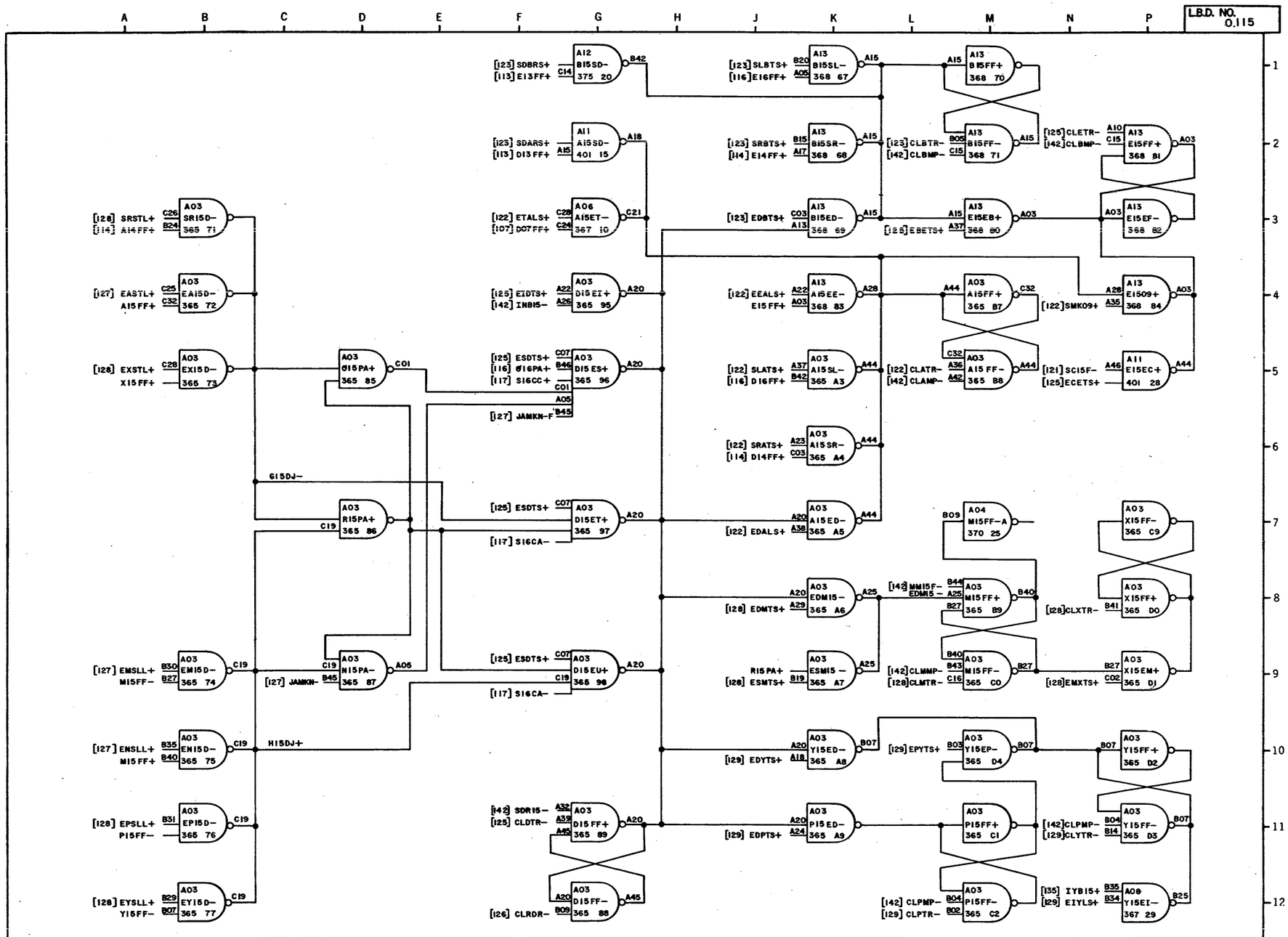
REVISIONS	REV.	
	A	S.R. 54-3585
	B	ECO 7748 EXT. CHANGES SEE ECO T.A. 1/19/68

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. D. HAMEL	DATE 11-26-68	
ENG. K. IZBICKI	11-26-68	
APP.	7-2-69	
PROJECT NO. 55202		

TITLE
H-316
COLUMN No. 14

SIZE	DWG NO.	REV.
C	70024498	B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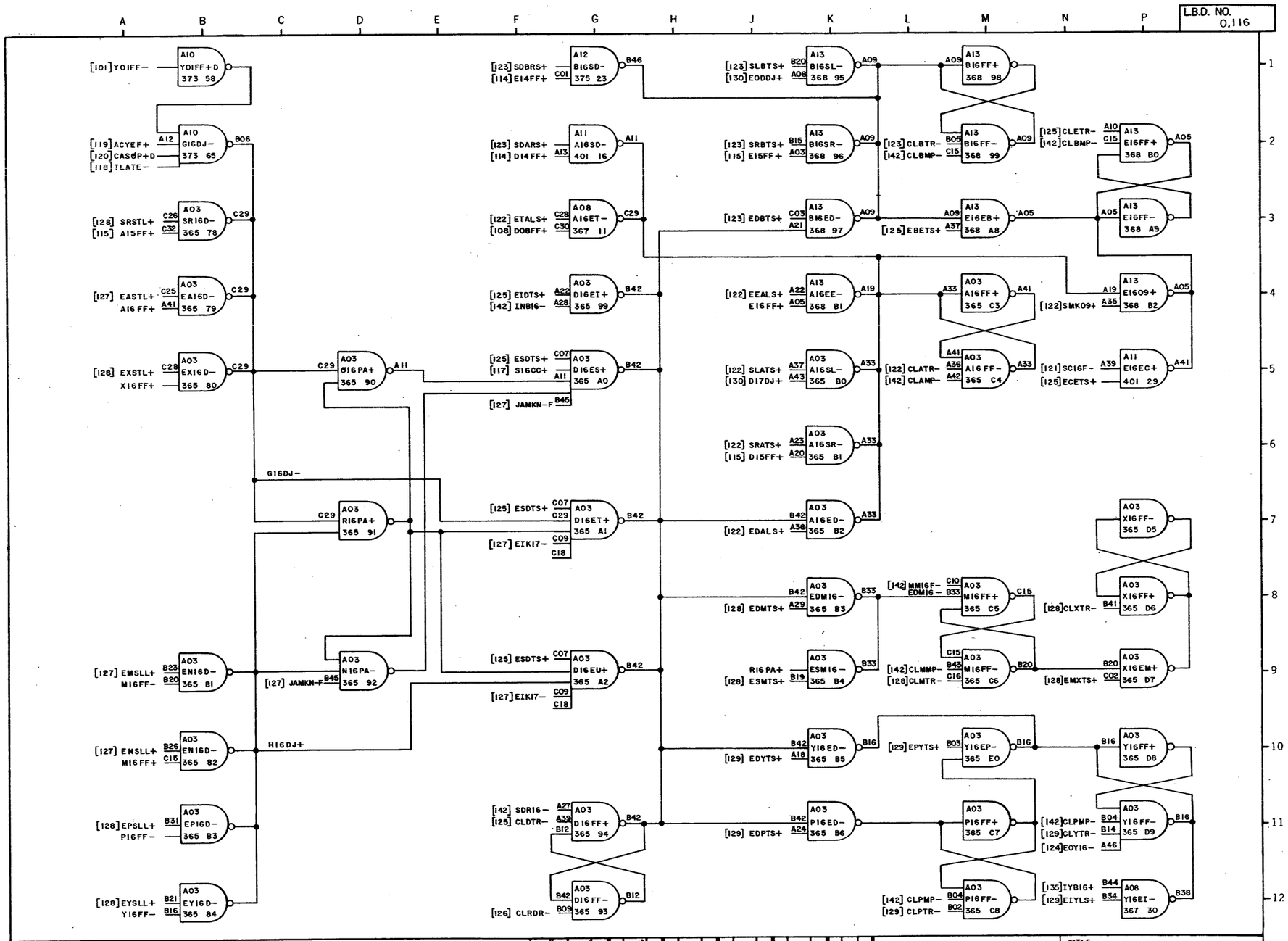
A12 B15SD- 375 20
A13 B15SL- 368 67
A13 B15FF+ 368 70
A11 A15SD- 401 15
A13 B15SR- 368 68
A13 B15FF- 368 71
A13 E15FF+ 368 81
A06 A15ET- 367 10
A13 B15ED- 368 69
A13 E15EB+ 368 80
A13 E15EF- 368 82
A03 SR15D- 365 71
A03 EA15D- 365 72
A03 EX15D- 365 73
A03 G15PA+ 365 85
A03 D15ES+ 365 96
A03 A15EE- 368 83
A03 A15FF+ 365 87
A13 E1509+ 368 84
A03 A15SL- 365 A3
A03 A15 FF- 365 88
A11 E15EC+ 401 28
A03 D15EI+ 365 96
A03 R15PA+ 365 86
A03 D15ET+ 365 97
A03 A15SR- 365 A4
A03 A15ED- 365 A5
A04 M15FF-A 370 25
A03 X15FF- 365 C9
A03 EM15D- 365 74
A03 N15PA- 365 87
A03 D15EU+ 365 98
A03 EN15D- 365 75
A03 EP15D- 365 76
A03 EY15D- 365 77
A03 D15FF+ 365 89
A03 D15FF- 365 88
A03 A15ED- 365 A6
A03 ES M15 - 365 A7
A03 Y15ED- 365 A8
A03 P15ED- 365 A9
A03 M15FF+ 365 B9
A03 M15FF- 365 C0
A03 X15FF+ 365 D0
A03 X15EM+ 365 D1
A03 Y15EP- 365 D4
A03 P15FF+ 365 C1
A03 P15FF- 365 C2
A03 Y15FF+ 365 D2
A03 Y15FF- 365 D3
A08 Y15EI- 367 29
[123] SDBRS+ [113] E13FF+
[123] SLBTS+ [116] E16FF+
[123] SDARS+ [113] D13FF+
[123] SRBTS+ [114] E14FF+
[123] CLBTR- [142] CLBMP-
[125] CLETR- [142] CLBMP-
[122] ETALS+ [107] D07FF+
[123] EDBTS+
[125] EBETS+
[128] SRSTL+ [114] A14FF+
[127] EASTL+ A15FF+
[128] EXSTL+ X15FF+
[125] EIDTS+ [142] INB15-
[122] EEALS+ E15FF+
[122] SMK09+
[125] ESDTS+ [116] G16PA+ [117] S16CC+
[122] SLATS+ [116] D16FF+
[122] CLATR- [142] CLAMP-
[121] SCI5F- [125] ECETS+
[127] JAMKN-F
[122] SRATS+ [114] D14FF+
G15DJ-
[125] ESDTS+ [117] S16CA-
[122] EDALS+
[142] MM15F- EDM15 -
[128] EDMTS+
[128] CLXTR-
R15PA+ [128] ESMTS+
[142] CLMMP- [128] CLMTR-
[128] EMXTS+
[127] EMSLL+ M15FF-
[127] JAMKN-
[117] S16CA-
[129] EPYTS+
[129] EDYTS+
[142] CLPMP- [129] CLYTR-
[127] ENSLL+ M15FF+
H15DJ+
[142] SDR15- [125] CLDTR-
[129] EDPTS+
[128] EPSLL+ P15FF-
[142] CLPMP- [129] CLPTR-
[135] IYB15+ [129] EIYLS+
[126] CLRDR-
[128] EYSLL+ Y15FF-
NOTES:
REVISIONS
REV.
CHK.
A
S.R. 54-3585
B
ECO 7748
EXT CANGES SEE ECO T.A.
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.
DR. D. HAMEL
DATE 11-26-68
ENG. K. IZBICKI
11-26-68
APP.
5-2-69
PROJECT NO. 55202
TITLE
H-316
COLUMN No. 15
SIZE C
DWG NO. 70024499
REV. B


L.B.D. NO. 0.116
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[119] AC YEF+
[120] CAS ØP+D
[118] TLATE-
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[128] SRSTL+
[115] A15FF+
A03 EA16D- 365 79
[127] EASTL+
A16FF+
A03 EX16D- 365 80
[128] EXSTL+
X16FF+
A03 DI6PA+ 365 90
A03 R16PA+ 365 91
A03 EN16D- 365 81
[127] EMSLL+
M16FF-
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[127] ENSLL+
M16FF+
A03 EP16D- 365 83
[128] EPSLL+
P16FF-
A03 EY16D- 365 84
[128] EYSLL+
Y16FF-
G16DJ-
H16DJ+
A03 N16PA- 365 92
[127] JAMKN-F
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[123] SDBRS+
[114] E14FF+
A11 A16SD- 401 16
[123] SDARS+
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A08 A16ET- 367 11
[122] ETALS+
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[125] EIDTS+
[142] INB16-
A03 DI6ES+ 365 A0
[125] ESDTS+
[117] S16CC+
[127] JAMKN-F
A03 DI6ET+ 365 A1
[125] ESDTS+
[127] EIKI7-
A03 DI6EU+ 365 A2
[125] ESDTS+
[127] EIKI7-
A03 D16FF+ 365 94
[142] SDR16-
[125] CLDTR-
A03 D16FF- 365 93
[126] CLRDR-
A13 B16SL- 368 95
[123] SLBTS+
[130] EODDJ+
A13 B16SR- 368 96
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A13 B16ED- 368 97
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[115] D15FF+
A03 A16ED- 365 B2
[122] EDALS+
A03 EDM16- 365 B3
[128] EDMTS+
A03 ESM16- 365 B4
R16PA+
[128] ESMTS+
A03 Y16ED- 365 B5
[129] EDYTS+
A03 P16ED- 365 B6
[129] EDPTS+
A13 B16FF+ 368 98
A13 B16FF- 368 99
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A13 E16E8+ 368 A8
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A03 A16FF+ 365 C3
A03 A16FF- 365 C4
[122] CLATR-
[142] CLAMP-
A03 M16FF+ 365 C5
[142] MM16F-
EDM16-
A03 M16FF- 365 C6
[142] CLMMP-
[126] CLMTR-
A03 Y16FF+ 365 C7
[129] EPYTS+
A03 P16FF- 365 C8
[142] CLPMP-
[129] CLPTR-
A13 E16FF+ 368 B0
[125] CLETR-
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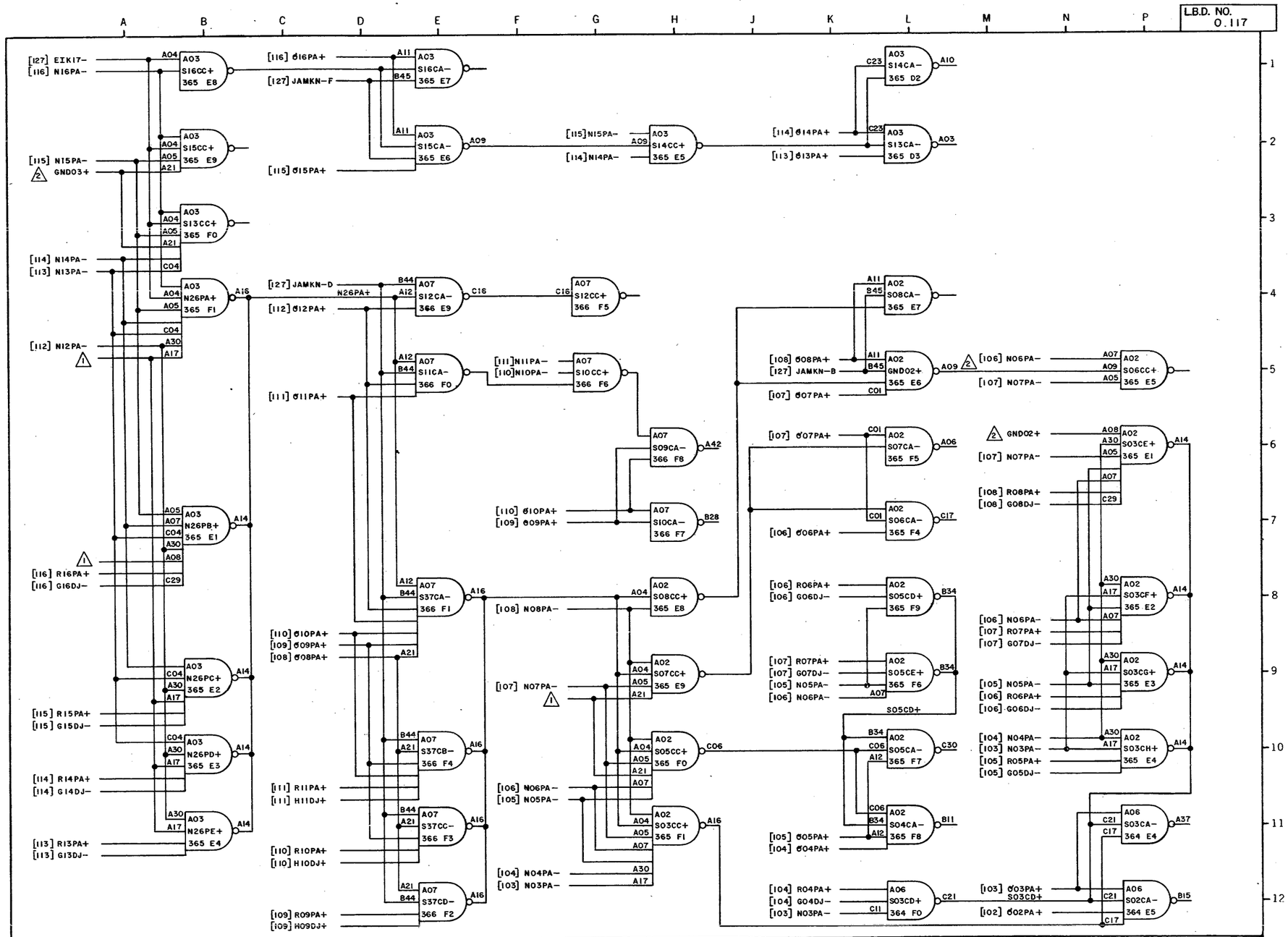
A13 E16FF- 368 A9
A13 E1609+ 368 B2
[122] SMK09+
A11 E16EC+ 401 29
[121] SC16F-
[125] ECETS+
A03 X16FF- 365 D5
A03 X16FF+ 365 D6
[128] CLXTR-
A03 X16EM+ 365 D7
[128] EMXTS+
A03 Y16FF- 365 D9
[142] CLPMP-
[129] CLYTR-
[124] EOY16-
A08 Y16EI- 367 30
[135] IYB16+
[129] EIYLS+
NOTES:
REVISIONS
REV. A
S.R. 54-3585
ECO 7748
B
EXT. CHANGES SEE ECO T.A.
CHK
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.
DR. D. HAMEL
DATE 11-26-68
ENG. K. IZBICKI
11-26-68
APP.
7-2-69
PROJECT NO. 55202
TITLE
H-316
COLUMN No. 16
SIZE C
DWG NO. 70024500
REV.

L.B.D. NO. 0.117



NOTES:

1. THESE PTS. ARE FLOATING. THIS IS DUE TO THE DOUBLE USAGE OF CC365
2. THESE PTS ARE TIED TO THEIR PAC GROUNDS. THIS IS DUE TO THE DOUBLE USAGE OF CC365.

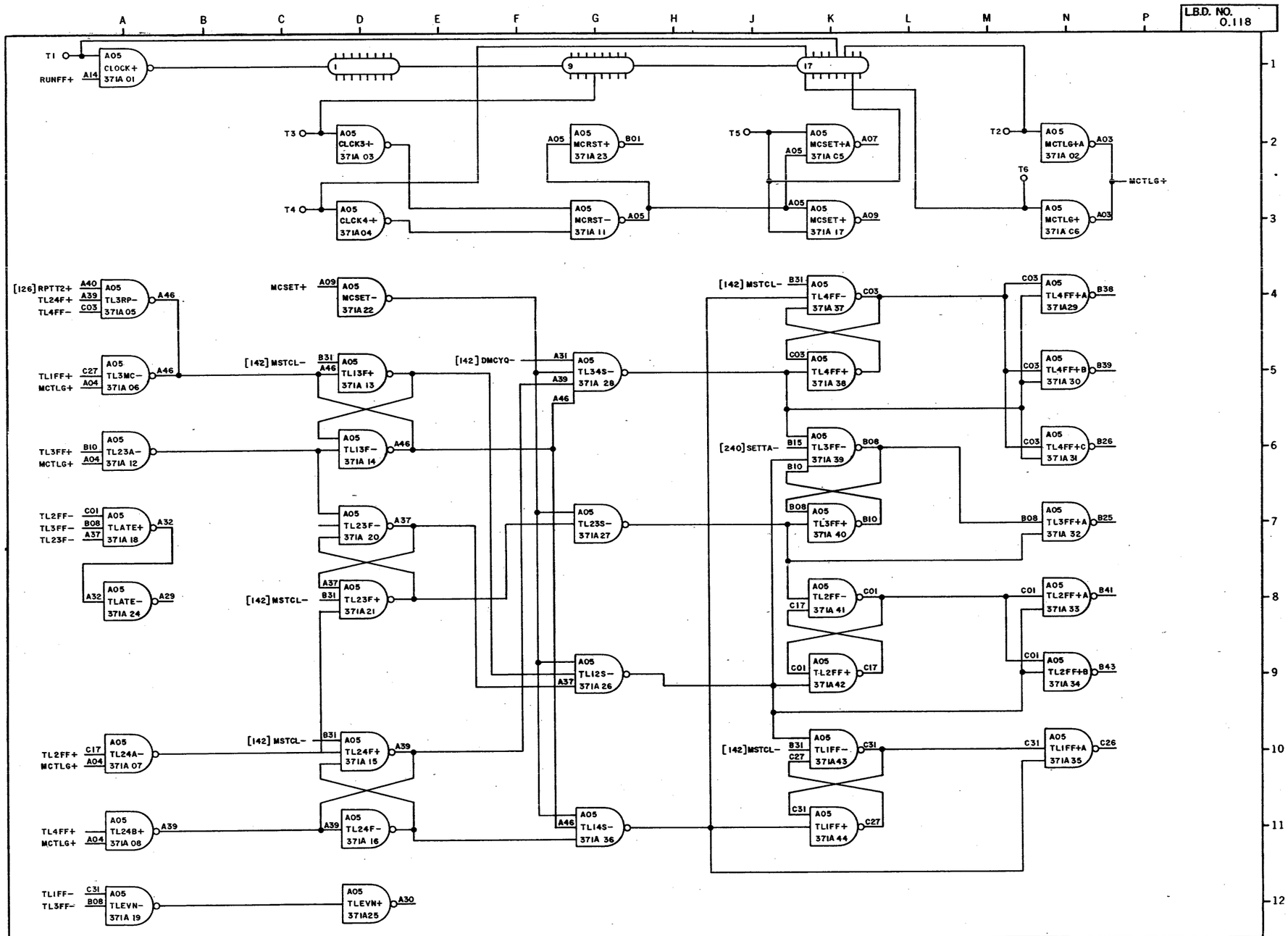
REV.	REVISIONS	
A	S.R. 54-3585	ECO 7748
B	EXT CHANGES SEE ECO T.A. 1/1/70	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR.	D. HAMEL	DATE 11-27-68
ENG.	K. IZBICKI	11-27-1968
APP.		4/1/69
PROJECT NO.	55202	

TITLE
H-316
CARRY NETWORK

SIZE C | D NO. 7002 4501 | REV. B



NOTES:

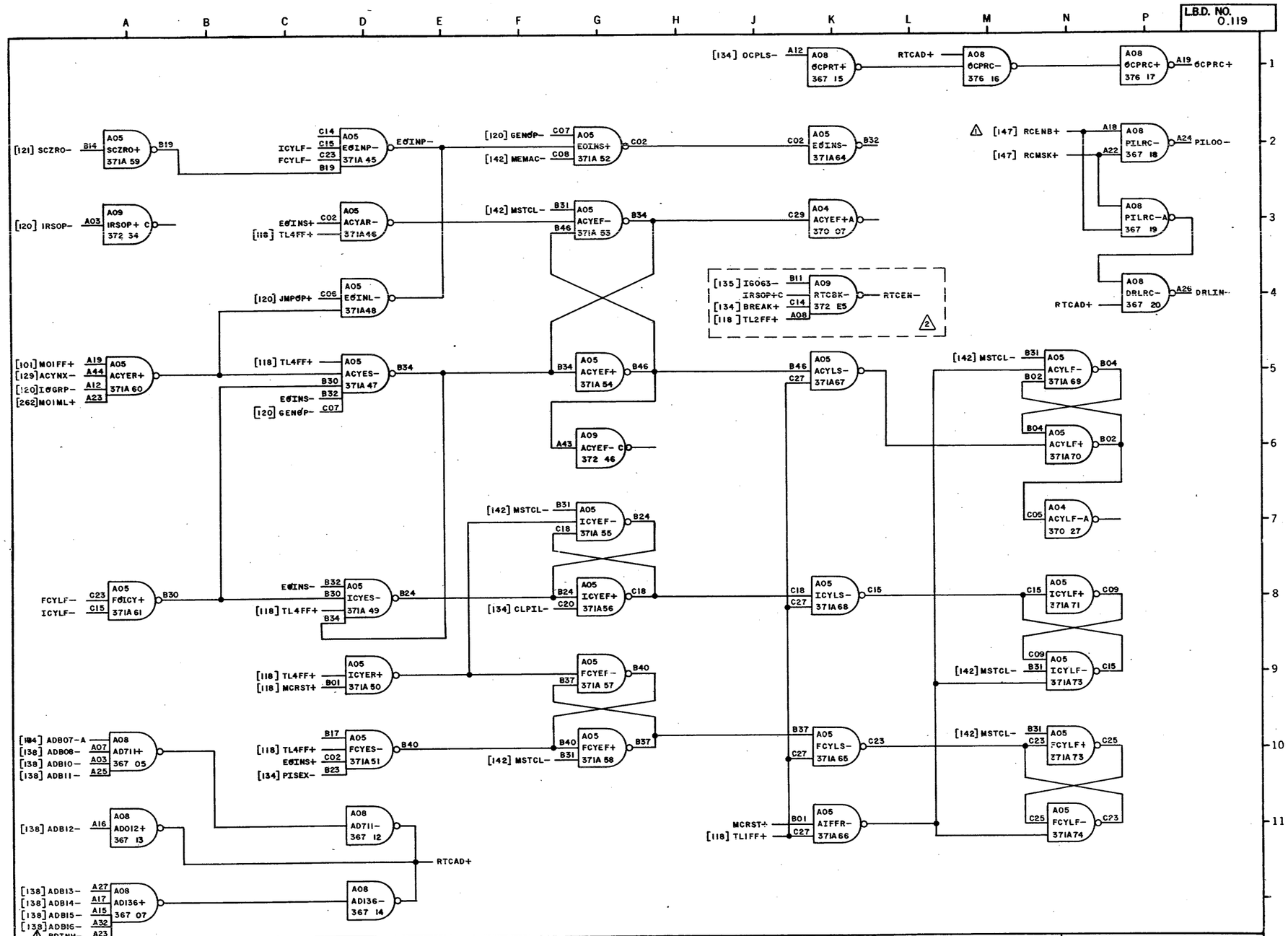
REVISIONS	REV.	
S.R. 54-3585	A	
ECO 7748 EXT CHANGES SEE ECO TA 7/66	B	
CHK.		

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. D. HAMEL	DATE	
ENG. K. IZBICKI	1-9-1969	
APP.	7-2-69	
PROJECT NO. 55202		

TITLE
H-316
TLG & CLOCK

SIZE	DWG NO.	REV.
C	70024502	B



NOTES:

1. REMOVE GROUND WHEN USING REAL TIME CLOCK
2. THIS GATE REPLACED BY RTCEN-A FROM DMC IF SDMC OR HSDMC IS INSTALLED

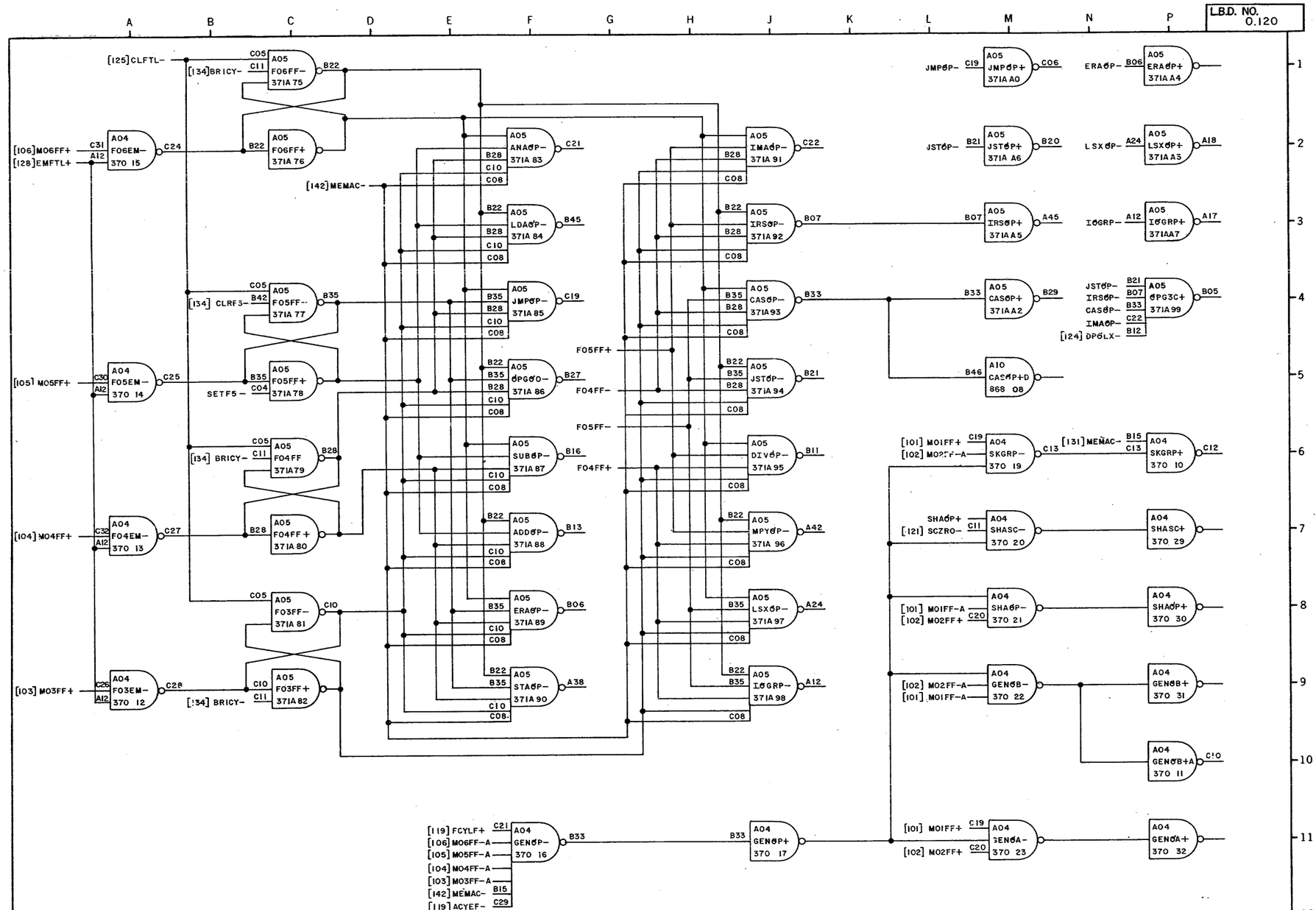
REV.	REVISIONS	CHK.
A	S.R. 54-3585	
B	ECO 7748 EXT CHANGES 11/67, SEE ECO T.A.	
C	ECO 8654 EXT. CHGS SEE ECO 8/14/70 A.K.	
D	ECO10228 SEE ECO 3/6/72 S.S.R.	
E	ECO 20649 ADDED [120] 4-2872 GENOP - R.S.	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. D. HAMEL	DATE 12-12-68	
ENG. K. IZBICKI	12-12-1968	
APP.	4-1-69	
PROJECT NO. 55202		

TITLE
H-316
PHASE REGISTER

SIZE C | DWG NO. 70024503 | REV. E



NOTES:

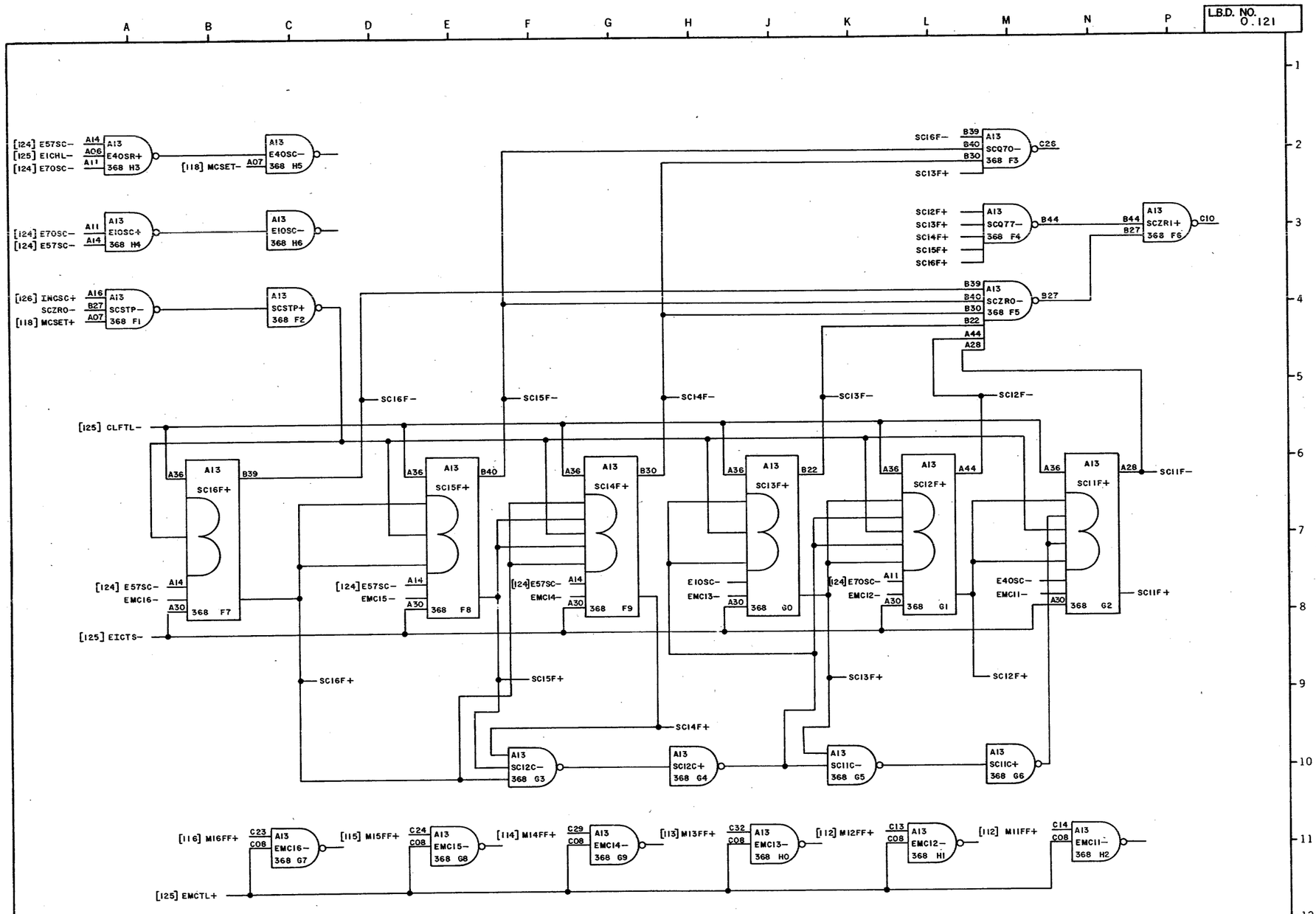
REV.	REVISIONS	CHK
A	DATA BY EWG	

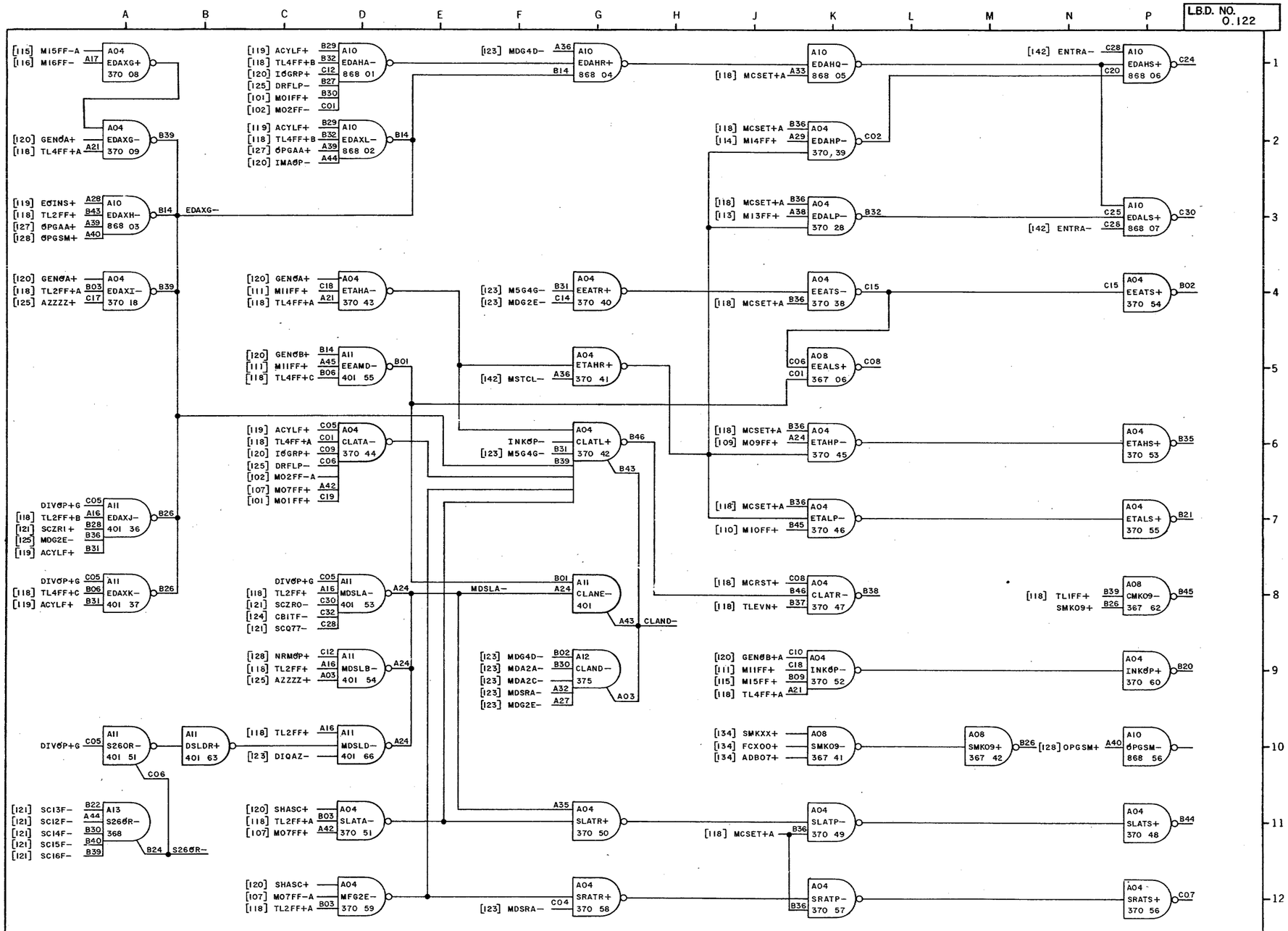
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. P. BELBUSTI	DATE 8/22/72
ENG. M. OLSEN	8/22/72
APP.	
PROJECT NO. 6014	

TITLE
H-316-0110
F REG & OP DECODE

SIZE	DWG NO.	REV.
C	70032801	A


L.B.D. NO. 0.121
[124] E57SC–
[125] E1CHL–
[124] E70SC–
A13 E40SR+ 368 H3
[118] MCSET–
A13 E40SC– 368 H5
[124] E70SC–
[124] E57SC–
A13 E10SC+ 368 H4
A13 E10SC– 368 H6
[126] INCSC+
SCZRO–
[118] MCSET+
A13 SCSTP– 368 F1
A13 SCSTP+ 368 F2
SC16F–
SC15F–
SC14F–
SC13F–
SC12F–
SC11F–
[125] CLFTL–
A13 SC16F+
A13 SC15F+
A13 SC14F+
A13 SC13F+
A13 SC12F+
A13 SC11F+
[124] E57SC– EMC16–
[124] E57SC– EMC15–
[124] E57SC– EMC14–
E10SC– EMC13–
[124] E70SC– EMC12–
E40SC– EMC11–
A30
368 F7
368 F8
368 F9
368 G0
368 G1
368 G2
SCI1F+
[125] EICTS–
SC16F+
SC15F+
SC13F+
SC12F+
SC14F+
A13 SC12C– 368 G3
A13 SC12C+ 368 G4
A13 SC11C– 368 G5
A13 SC11C+ 368 G6
SCI6F–
SCI3F+
A13 SCQ70– 368 F3
C26
SCI2F+
SCI3F+
SCI4F+
SCI5F+
SCI6F+
A13 SCQ77– 368 F4
B44
A13 SCZR1+ 368 F6
C10
B27
A13 SCZRO– 368 F5
[116] MI6FF+
[115] MI5FF+
[114] MI4FF+
[113] MI3FF+
[112] MI2FF+
[112] MI1FF+
A13 EMC16– 368 G7
A13 EMC15– 368 G8
A13 EMC14– 368 G9
A13 EMC13– 368 H0
A13 EMC12– 368 H1
A13 EMC11– 368 H2
[125] EMCTL+
NOTES:
REVISIONS
S.R. 54-3585
ECO 7748
EXT CHANGES 11/9/70
SEE ECO T.4,
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass
DR. D. HAMEL
ENG. K. IZBICKI 12-20-1968
APP.
PROJECT NO. 55202
TITLE
H-316
SHIFT COUNTER
SIZE C
DWG NO. 70024505
REV.


L.B.D. NO. 0.122
A B C D E F G H J K L M N P
1 2 3 4 5 6 7 8 9 10 11 12
[115] MI5FF-A
[116] MI6FF-
A04 EDAXG+ 370 08
[120] GENØA+
[118] TL4FF+A
A04 EDAXG- 370 09
[119] EØINS+
[118] TL2FF+
[127] ØPGAA+
[128] ØPGSM+
A10 EDAXH- 868 03
EDAXG-
[120] GENØA+
[118] TL2FF+A
[125] AZZZZ+
A04 EDAXI- 370 18
DIVØP+G
[118] TL2FF+B
[121] SCZRI+
[125] MDG2E-
[119] ACYLF+
A11 EDAXJ- 401 36
DIVØP+G
[118] TL4FF+C
[119] ACYLF+
A11 EDAXK- 401 37
[119] ACYLF+
[118] TL4FF+B
[120] IØGRP+
[125] DRFLP-
[101] MOIFF+
[102] MO2FF-
A10 EDAHA- 868 01
[119] ACYLF+
[118] TL4FF+B
[127] ØPGAA+
[120] IMAØP-
A10 EDAXL- 868 02
[120] GENØA+
[111] MIIFF+
[118] TL4FF+A
A04 ETAHA- 370 43
[120] GENØB+
[111] MIIFF+
[118] TL4FF+C
A11 EEAMD- 401 55
[119] ACYLF+
[118] TL4FF+A
[120] IØGRP+
[125] DRFLP-
[102] MO2FF-A
[107] MO7FF+
[101] MOIFF+
A04 CLATA- 370 44
DIVØP+G
[118] TL2FF+
[121] SCZRO-
[124] CBITF-
[121] SCQ77-
A11 MDSLA- 401 53
[128] NRMØP+
[118] TL2FF+
[125] AZZZZ+
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DIVØP+G
A11 S260R- 401 51
A11 DSLDR+ 401 63
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A11 MDSLD- 401 66
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A13 S26ØR- 368
S26ØR-
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[107] MO7FF+
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A04 MFG2E- 370 59
[123] M5G4D-
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A04 EEATR+ 370 40
[142] MSTCL-
A04 ETAHR+ 370 41
INKØP-
[123] M5G4G-
A04 CLATL+ 370 42
MDSLA-
A11 CLANE- 401
CLAND-
[123] MDG4D-
[123] MDA2A-
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[123] MDSRA-
[123] MDG2E-
A12 CLAND- 375
A35
A04 SLATR+ 370 50
[123] MDSRA-
A04 SRATR+ 370 58
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A10 EDAHQ- 868 05
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[114] MI4FF+
A04 EDAHP- 370, 39
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A04 EDALP- 370 28
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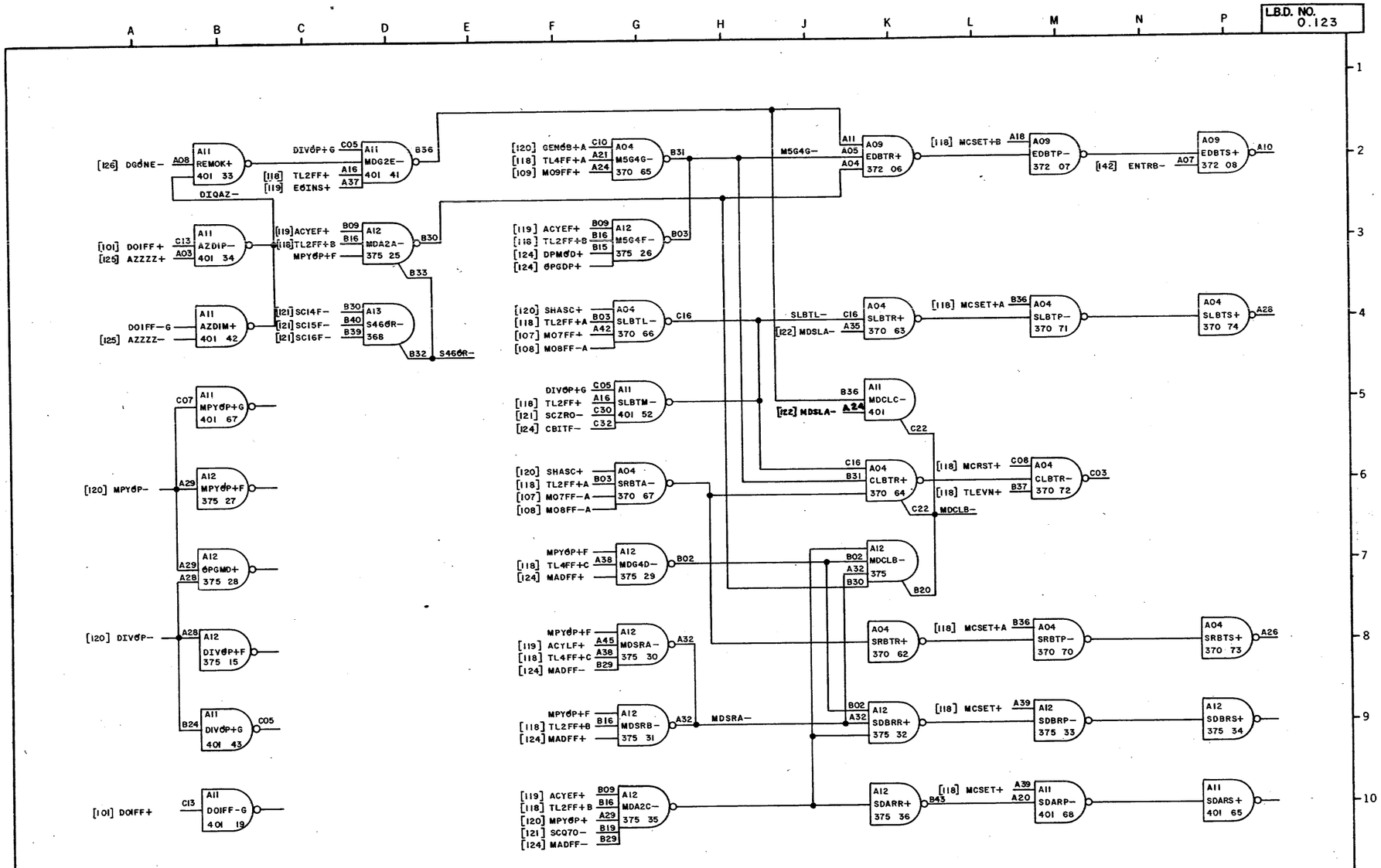
A04 EEATS- 370 38
C06
C01
A08 EEALS+ 367 06
[118] MCSET+A
[109] MO9FF+
A04 ETAHP- 370 45
[118] MCSET+A
[110] MIOFF+
A04 ETALP- 370 46
[118] MCRST+
[118] TLEVN+
A04 CLATR- 370 47
[118] MCSET+A
A04 SLATP- 370 49
[118] MCSET+A
[115] MI5FF+
[111] MIIFF+
[118] TL4FF+A
A04 INKØP- 370 52
[134] SMKXX+
[134] FCX00+
[134] ADB07+
A08 SMK09- 367 41
[142] ENTRA-
A10 EDAHS+ 868 06
[142] ENTRA-
A10 EDALS+ 868 07
C15
A04 EEATS+ 370 54
A04 ETAHS+ 370 53
A04 ETALS+ 370 55
[118] TLIFF+
SMK09+
A08 CMK09- 367 62
A04 SLATS+ 370 48
A04 SRATS+ 370 56
A04 INKØP+ 370 60
A08 SMK09+ 367 42
[128] ØPGSM+
A10 ØPGSM- 868 56
NOTES:
REVISIONS REV. CHK.
ORIG BY ENG
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.
DR. P. BELBUSTI DATE 8/22/72
ENG. M. OLSEN 8/22/72
APP.
PROJECT NO. 6014
TITLE
H-316-0110
CONTROL LOGIC A
SIZE C
DWG NO. 70032802
REV. A



NOTES:

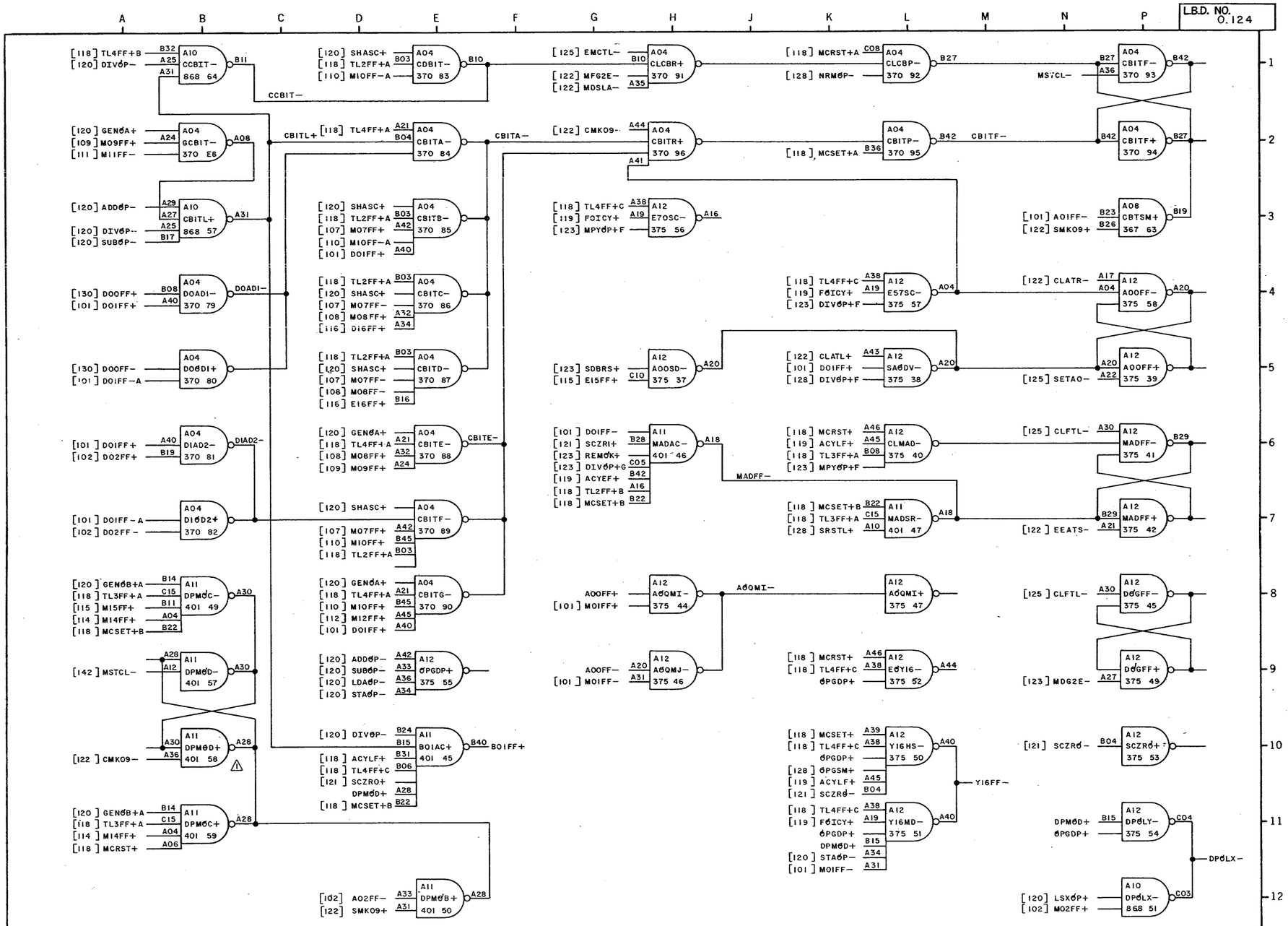
REV.	REVISIONS	CHK.
A	S.R. 54-3585	
B	ECO 7748 EXT CHANGES SEE ECO T.A.	
C	ECO 8654 EXT. CHGS SEE ECO 8/14/70 A.K.	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR.	D. HAMEL	DATE
ENG.	K. IZBICKI	12-26-1968
APP.		1-2-69
PROJECT NO.	55202	

TITLE
H-316
CONTROL LOGIC B

SIZE	DWG NO.	REV.
C	70024507	C



NOTES:

1. THIS PT. IS GND WITH NO HSA OPTION.

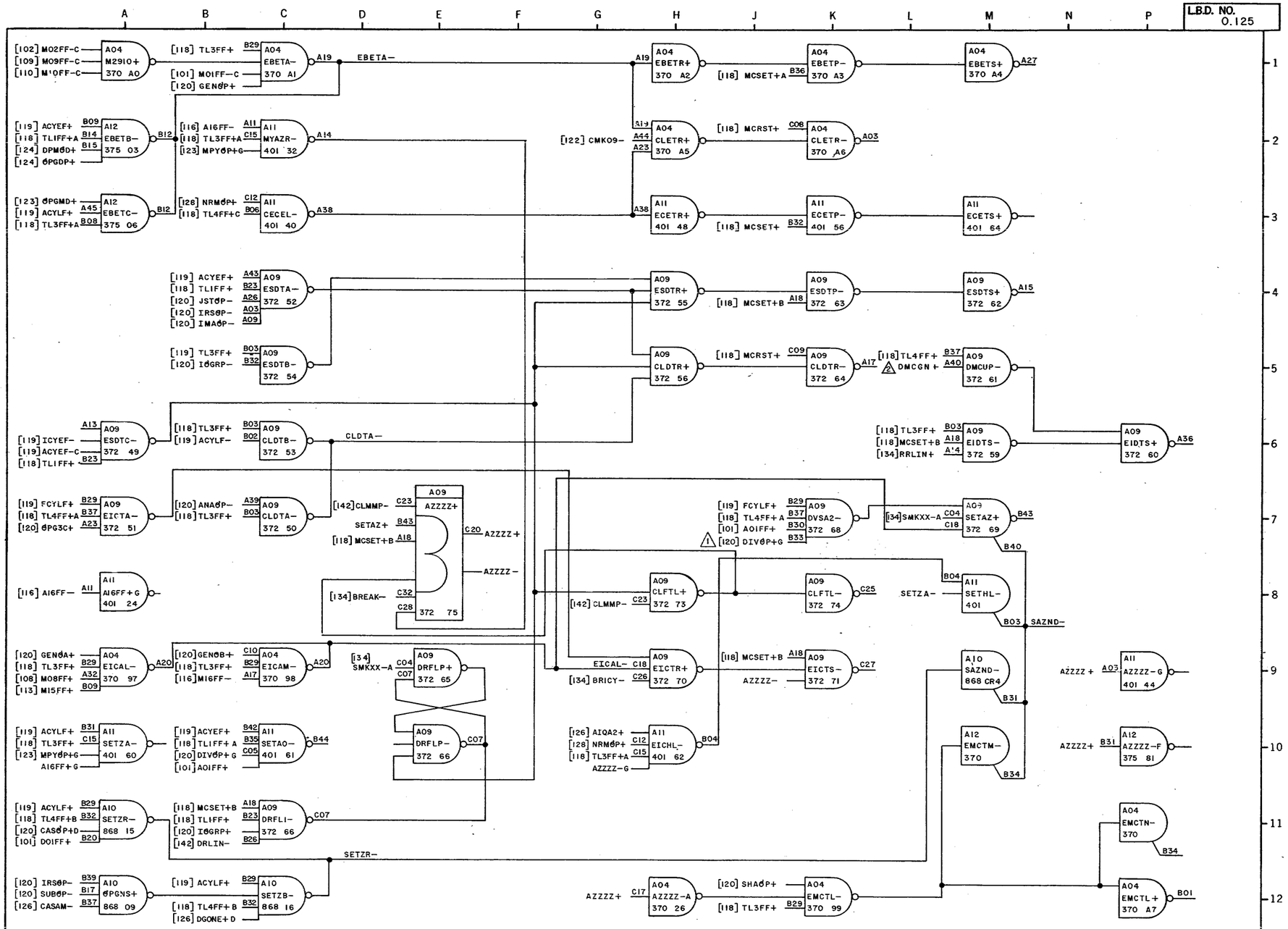
REV.	REVISIONS	CHK.
A	ORIG BY ENG	+

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. P BELBUSTI	DATE 8/22/72
ENG. M. OLSEN	8/22/72
APP.	
PROJECT NO. 6014	

TITLE
H-316-0110
CONTROL LOGIC C

SIZE	DWG NO.	REV.
C	70032803	A



NOTES:

1. THIS PT. MUST BE GND WITH NO HSA OPTION.
2. THIS PT. TIED TO GND.

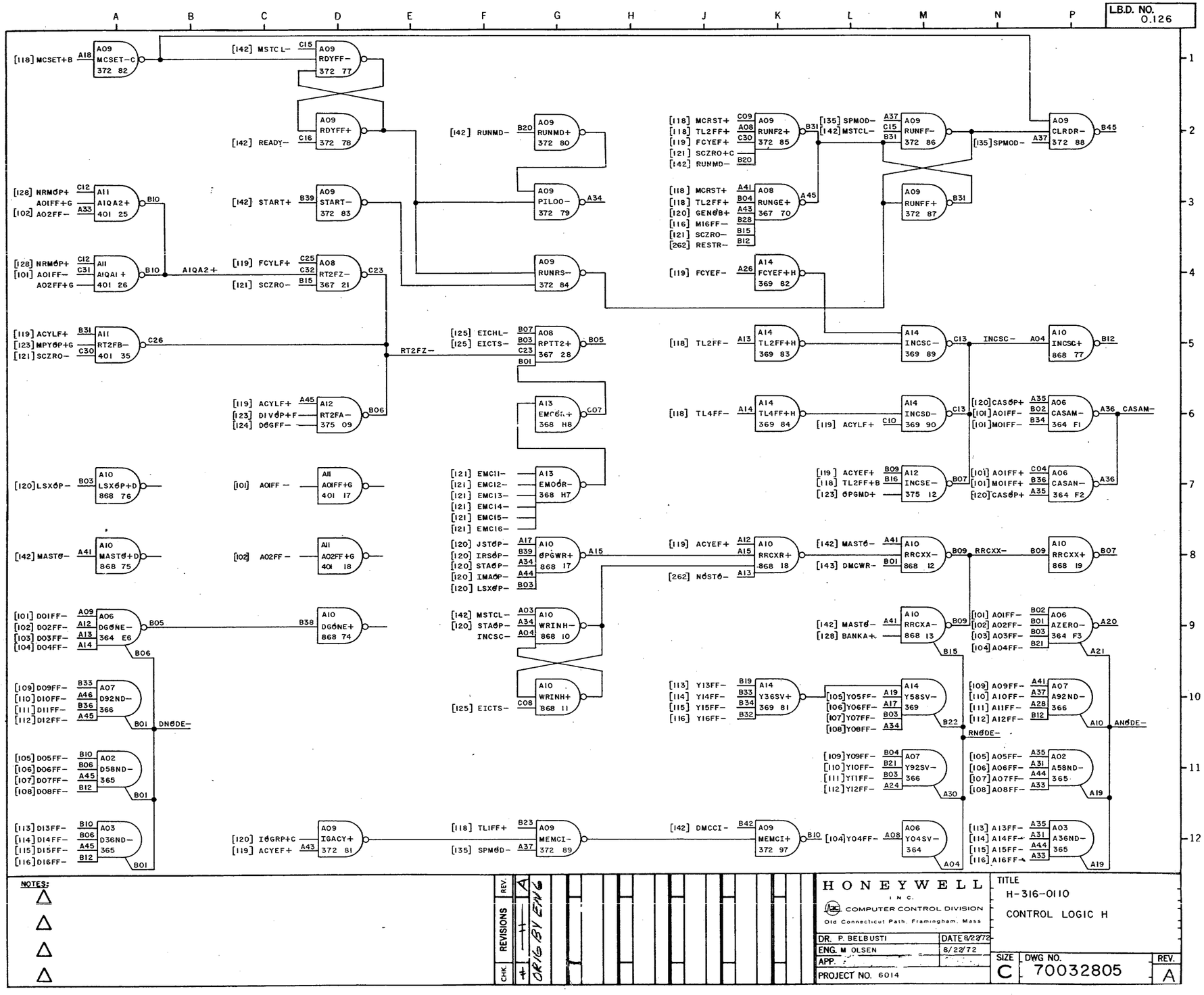
REV.	REVISIONS	CHK.
A	ORIG BY ENG	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass

DR. P. BELBUSTI	DATE 8/22/72	
ENG. M. OLSEN	8/22/72	
APP.		
PROJECT NO. 6014		

TITLE
H-316-0110
CONTROL LOGIC D/E

SIZE	DWG NO.	REV.
C	70032804	A



NOTES:

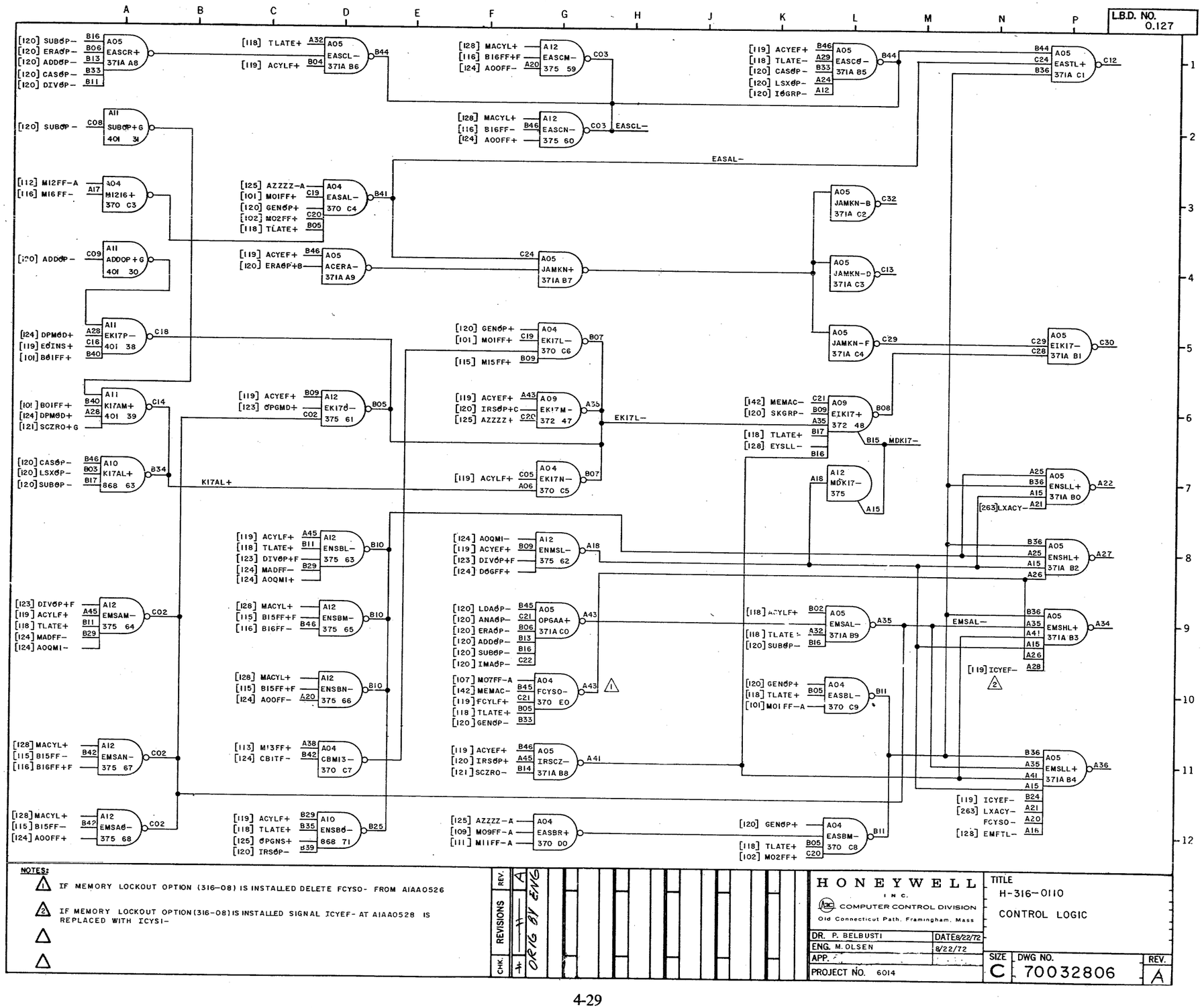
REVISIONS	REV.	
	A	ORIG ISY ENG
CHK.		

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. P. BELBUSTI	DATE 8/22/72
ENG. M. OLSEN	8/22/72
APP.	
PROJECT NO. 6014	

TITLE
H-316-0110
CONTROL LOGIC H

SIZE	DWG NO.	REV.
C	70032805	A



NOTES:

1. IF MEMORY LOCKOUT OPTION (316-08) IS INSTALLED DELETE FCYSO- FROM AIAA0526
2. IF MEMORY LOCKOUT OPTION (316-08) IS INSTALLED SIGNAL ICYEF- AT AIAA0528 IS REPLACED WITH ICYSI-

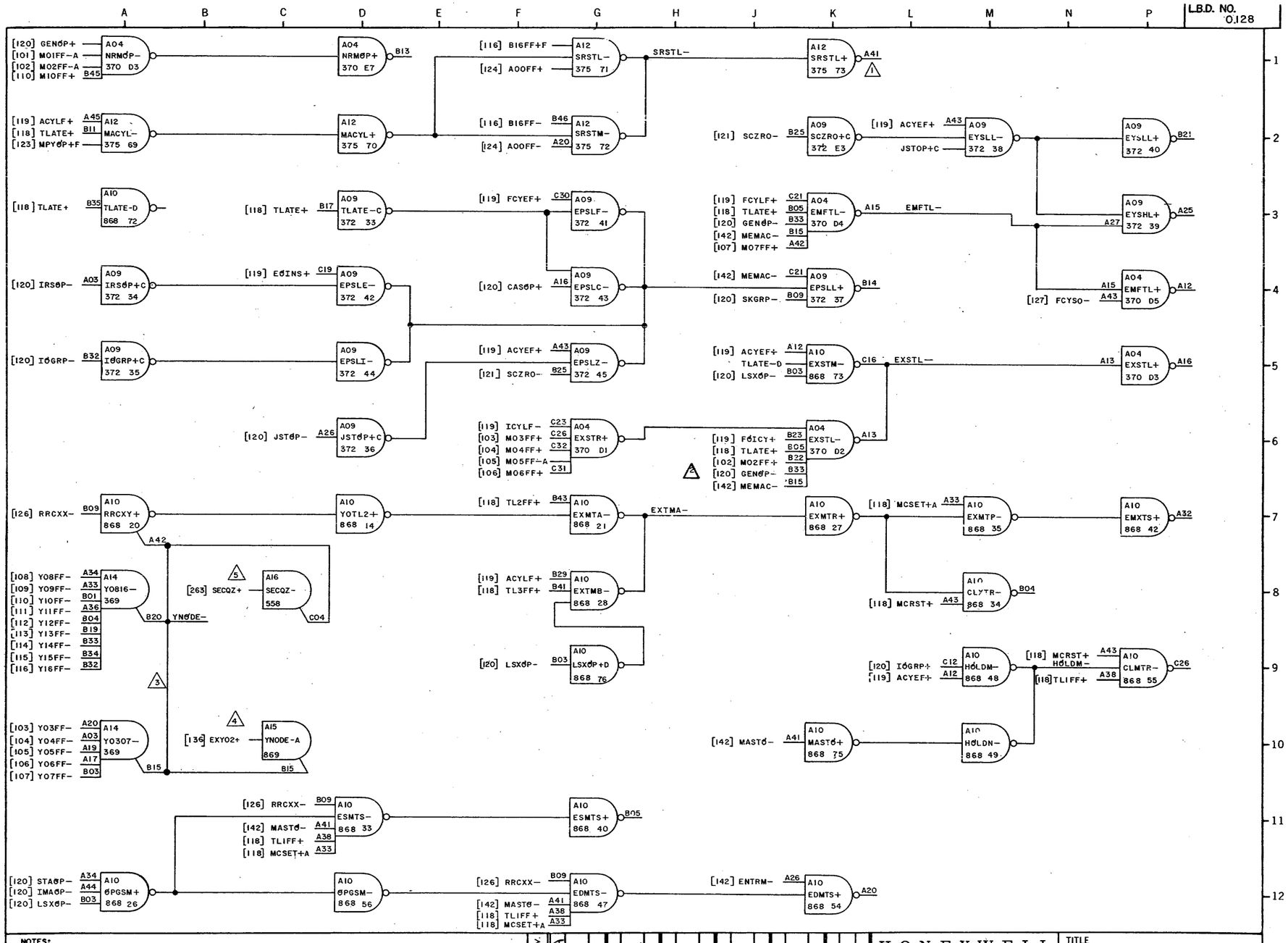
REVISIONS	REV.	
CHK.	A	ORIG BY ENG

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass

DR. P. BELBUSTI	DATE 8/22/72
ENG. M. OLSEN	8/22/72
APP.	
PROJECT NO. 6014	

TITLE
H-316-0110
CONTROL LOGIC

SIZE	DWG NO.	REV.
C	70032806	A



NOTES:

1. THIS PT IS TIED TO GND WITH NO HSA OPTION
2. DELETE M02FF + AND ADD M02DJ - WITH EXT ADD OPTION
3. DISCONNECT THIS WIRE IF MLO (316-08) IS INSTALLED
4. THIS GATE INCLUDED ONLY IF EXT ADD OPTION IS INSTALLED
5. THIS GATE INCLUDED ONLY IF MLO (316-08) IS INSTALLED.

REVISIONS

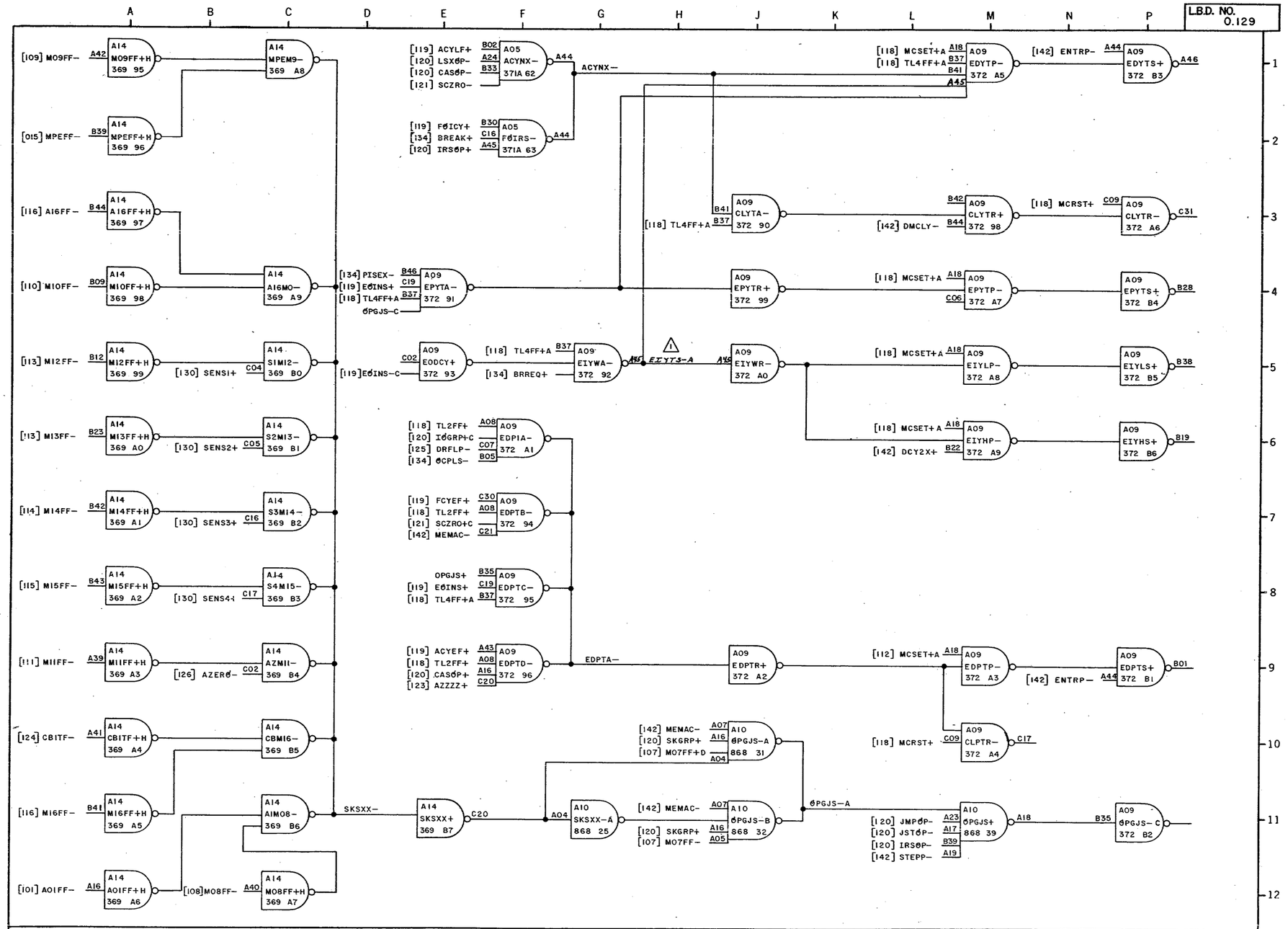
REV.		CHK.
A	4 — 11	ORIG BY FMS

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass

DR. P. BELBUSTI	DATE 8/22/72
ENG. M. OLSEN	8/22/72
APP.	
PROJECT NO. 6014	

TITLE
H-316-0110
CONTROL LOGIC MX

SIZE C | DWG NO. 70032807 | REV. A



NOTES:

1. THIS POINT DJ'D TO DMC OPTION. REFER TO LBD 142 CONN. A20 PIN 3
2.
3.
4.

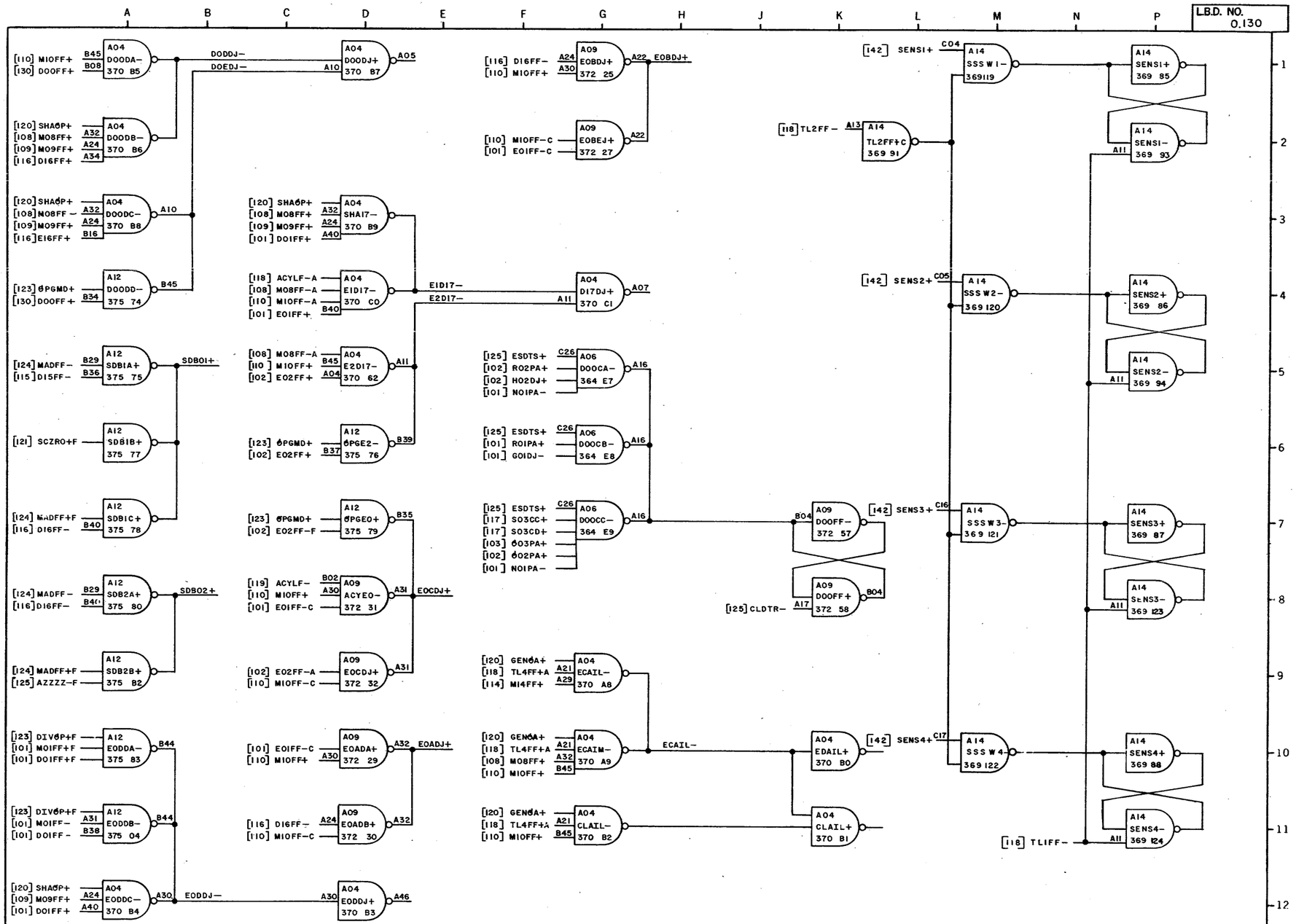
REV.	REVISIONS	CHK.
A	ORIG BY ENG	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. P. BELBUSTI	DATE 8/22/72
ENG. M. OLSEN	8/22/72
APP.	
PROJECT NO. 6014	

TITLE
H-316-0110
CONTROL LOGIC PY

SIZE C | DWG NO. 70032770 | REV. A



NOTES:

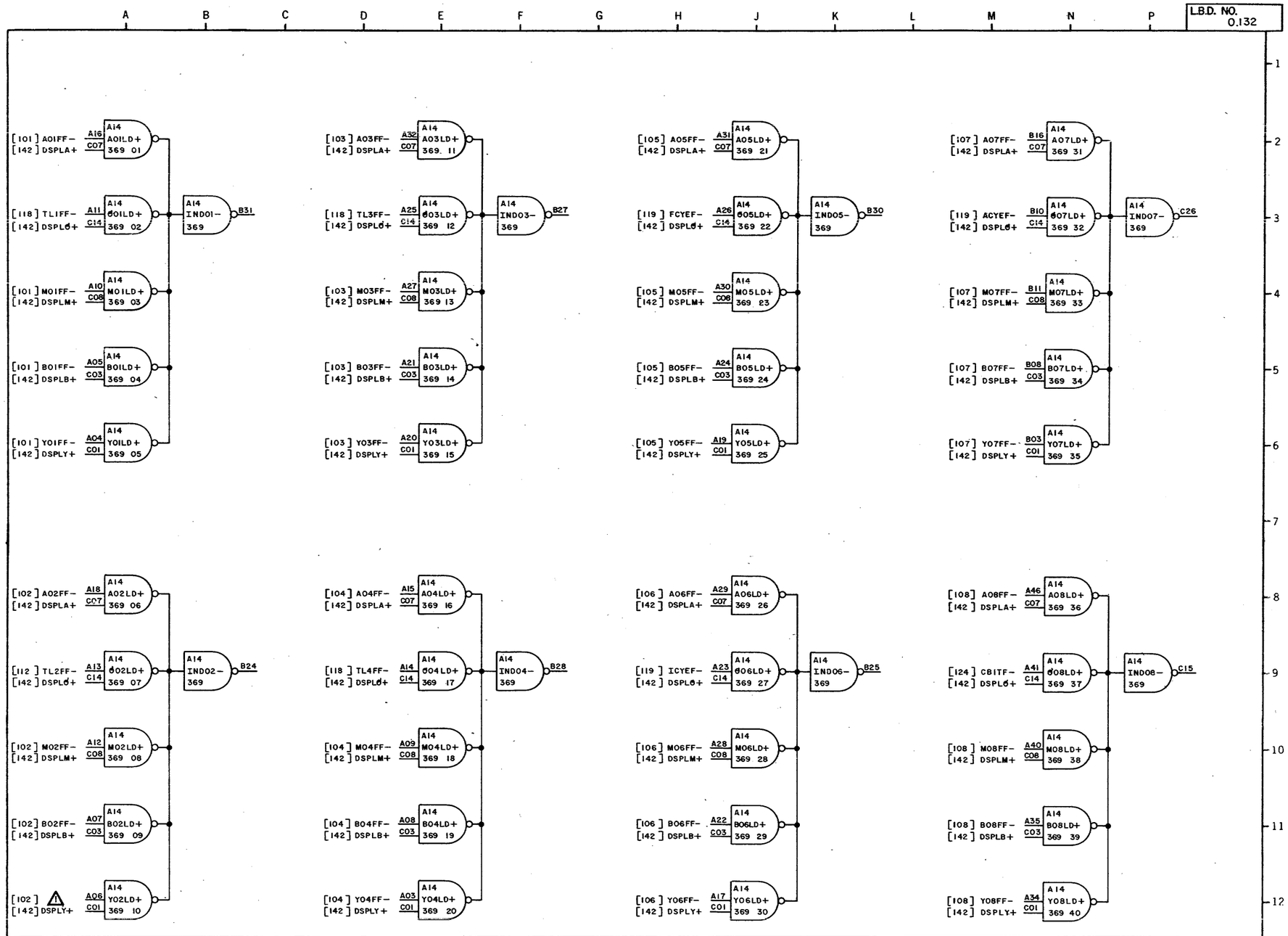
REV.	REVISIONS	CHK.
A	S.R. 54-3585	
B	ECO 7748 EXT. CHANGES SEE ECO T.A. 1/11/70	
C	ECO 10228 SEE ECO 3/6/72 S.S.R.	
D	ECO 20593 SEE ECO 9/27/72 T.L.B.	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR.	D. HAMEL	DATE
ENG.	K. IZBICKI	1-4-1969
APP.		2-2-69
PROJECT NO.	55202	

TITLE
H-316
CONTROL LOGIC PY

SIZE C | DWG NO. 70024514 | REV. D



NOTES:

⚠ ADD YO2FF- WITH EXT ADD OPTION

⚠

⚠

⚠

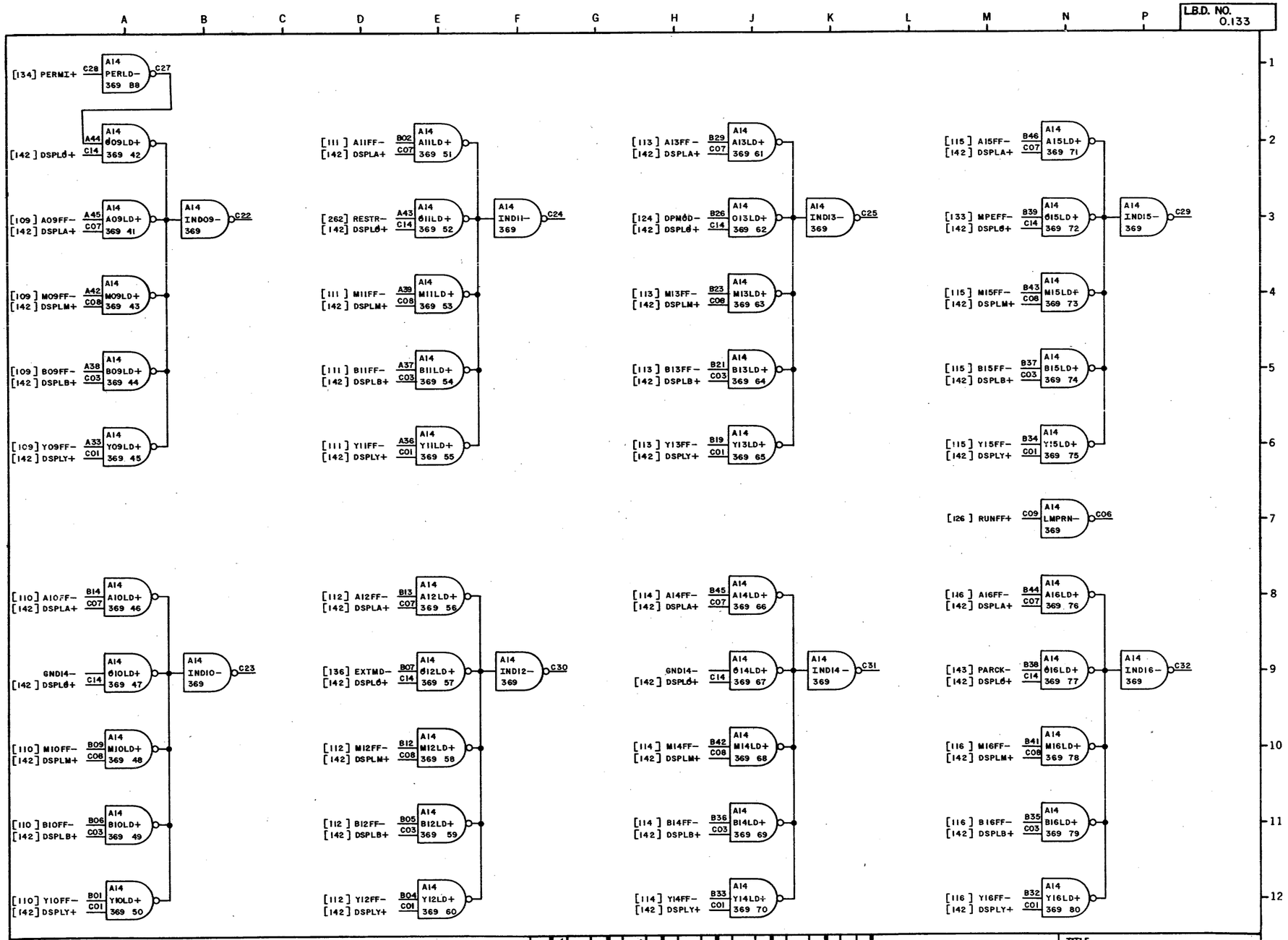
REVISIONS	REV.			
CHK.	44	—	1A	S.R. 54-3585
			B	ECO 7748 EXT CHANGES // W/ SEE ECO T.A.

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR.	D. HAMEL	DATE
ENG.	K. IZBICKI K.I.	1-7-1969
APP.	K. Izbicki	7-6-69
PROJECT NO.	55202	

TITLE
H-316
LAMP DRIVER 1-8

SIZE	DWG NO.	REV.
C	70024515	B



NOTES:

REV.	REVISIONS	CHK.
A	S.R. 54-3585 ECO 7748 EXT CHANGES SEE ECO T.A. 11/4/71	
B		

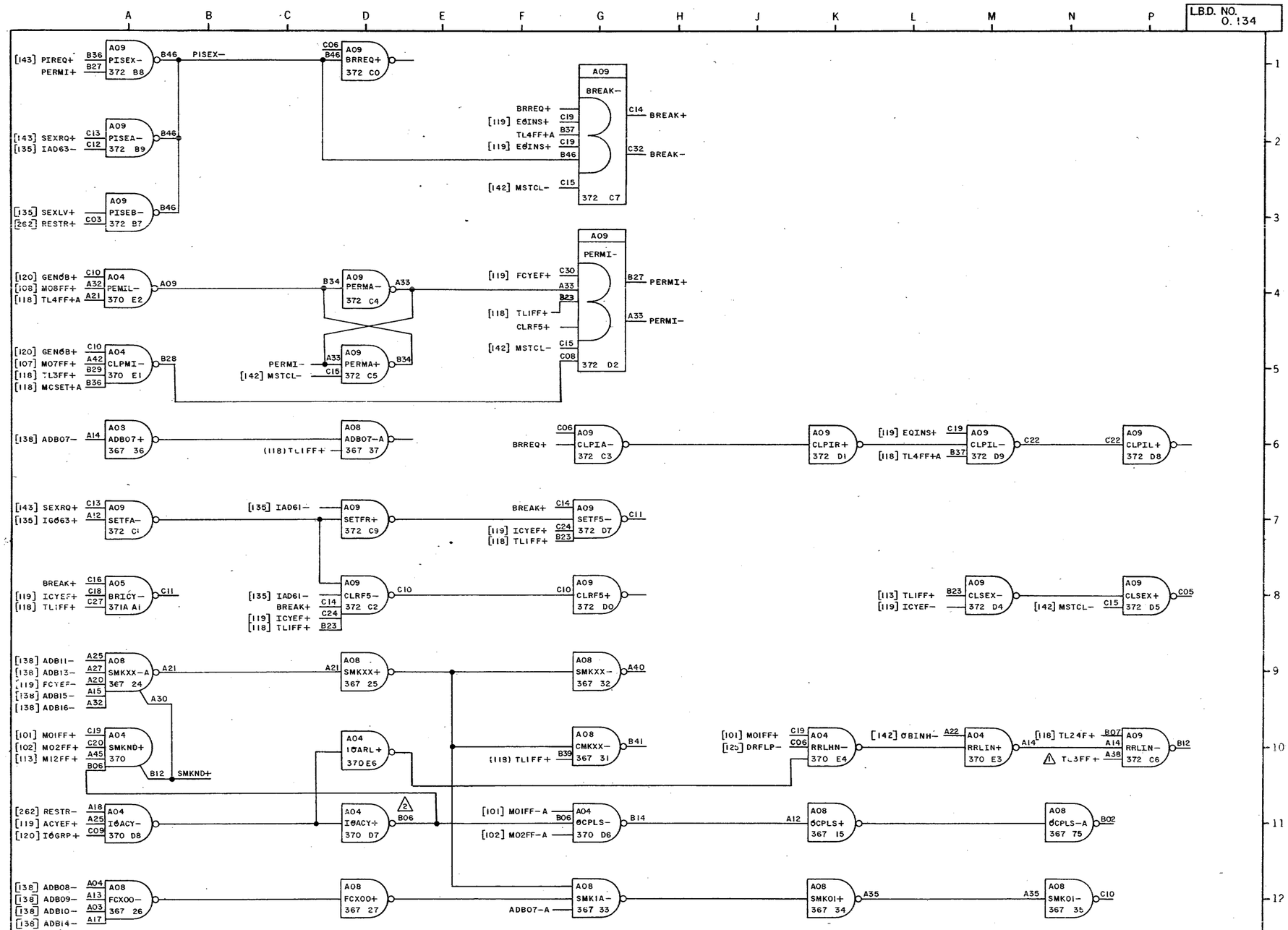
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. D. HAMEL	DATE	
ENG. K. IZBICKI	1-4-1969	
APP.	7-2-69	
PROJECT NO. 55202		

TITLE
H-316
LAMP DRIVER 9-16

SIZE	DWG NO.	REV.
C	70024516	B

L.B.D. NO. 0.133



NOTES:

1. WITH DMC OPTION REPLACE TL3FF + WITH DMFRL –
2. THIS POINT DJ'D WITH I0ACY+ TO DMC OPTION. REFER TO LBD 142 CONN. A20 PIN 08

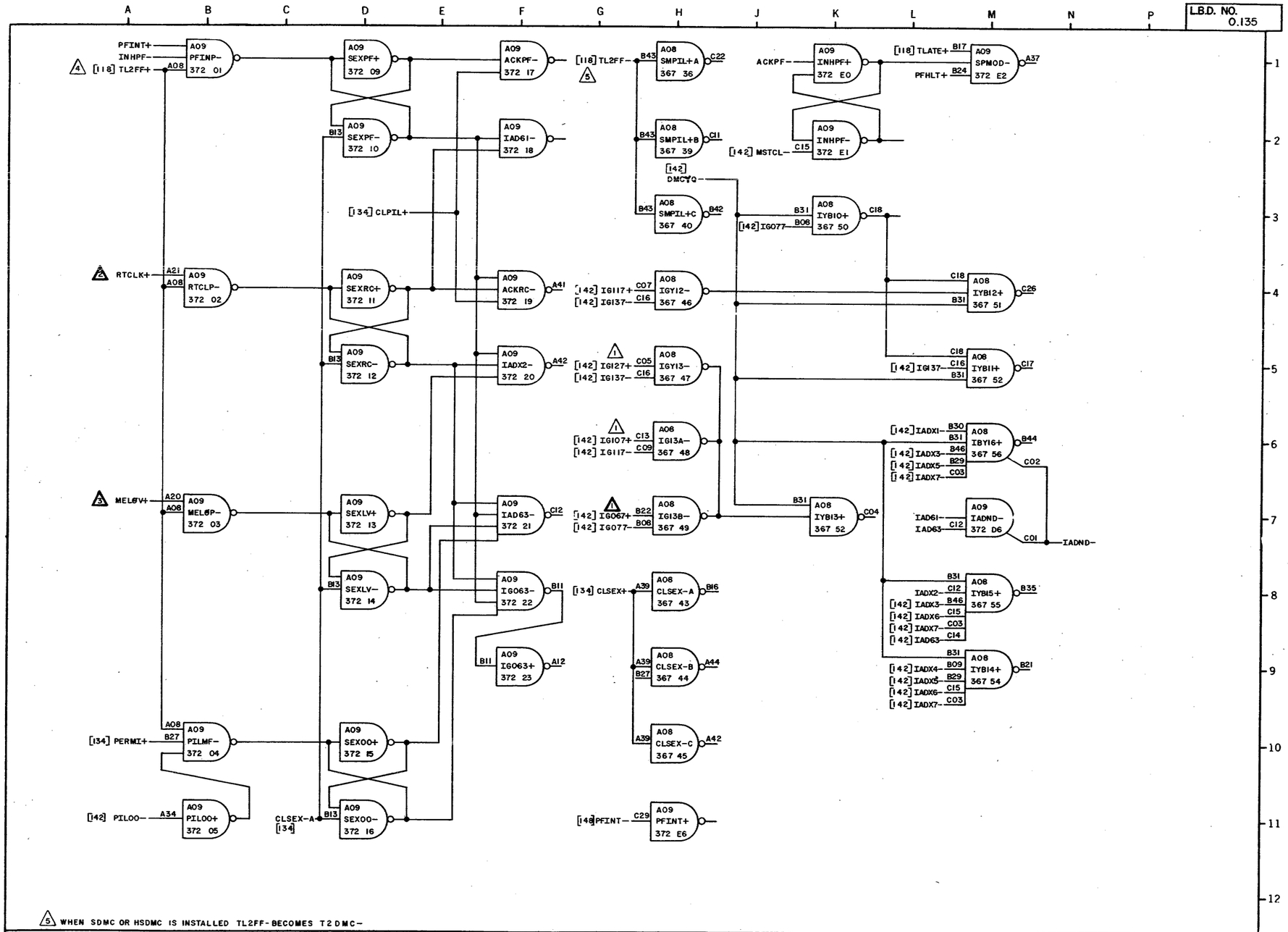
REV.	REVISIONS	CHK.
A	S.A. 54-3585	
G	ECO 20783 EXT CHGS SEE ECO T.L.B. 12/21/72	
	ECO EXT CHANGES SEE ECO	
D	ECO 8654 EXT CHGS SEE ECO A.K. 8/14/70	
E	ECO 9506 EXT CHANGES SEE ECO P.B. 8/17/71	
F	ECO 10228 SEE ECO S.S.R. 3/6/72	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. D. HAMEL	DATE	
ENG. K. IZBICKI	1-3-1969	
APP.		
PROJECT NO. 55202		

TITLE
H-316
CONTROL LOGIC I/O

SIZE C | DWG NO. 7002 4517 | REV.



5 WHEN SDMC OR HSDMC IS INSTALLED TL2FF- BECOMES T2DMC-

NOTES:
1. THIS PT IS GND WITH NO PI OPTION
2. THIS PT IS GND WITH NO RTC OPTION
3. THIS PT IS GND WITH NO M.L. OPTION
4. WHEN USING SDMC OR HSDMC TL2FF+ BECOMES T2DMC+

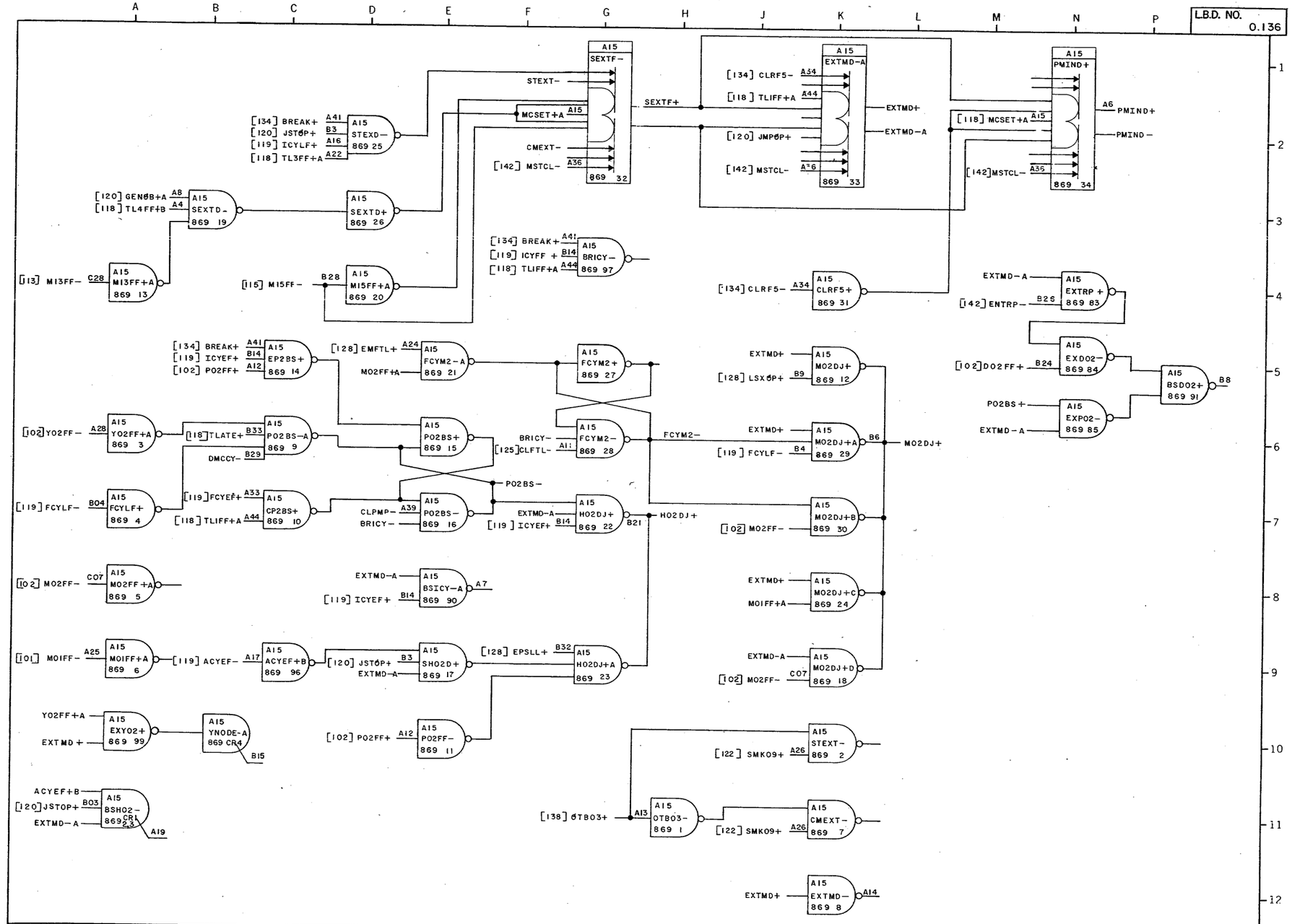
REVISIONS	REV.				
CHK.	A	B	C	D	
	S.R. 54-3585	ECO 7748 EXT. CHANGES SEE ECO T.A.	ECO 8654 EXT. CHGS SEE ECO A.K. 8/14/70	ECO 9365 EXT. CHGS SEE ECO S.S.R. 5/7/71	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR.	J.D.GILMARTIN	DATE
ENG.	K. IZBICKI	1-9-69
APP.		7-2-69
PROJECT NO.	55202	

TITLE
H-316
INTERRUPT ADDRESS
ENCODING

SIZE C | DWG NO. 70024518 | REV. D



NOTES:

REVISIONS	REV.	ORIG BY ENG
CHK	A	

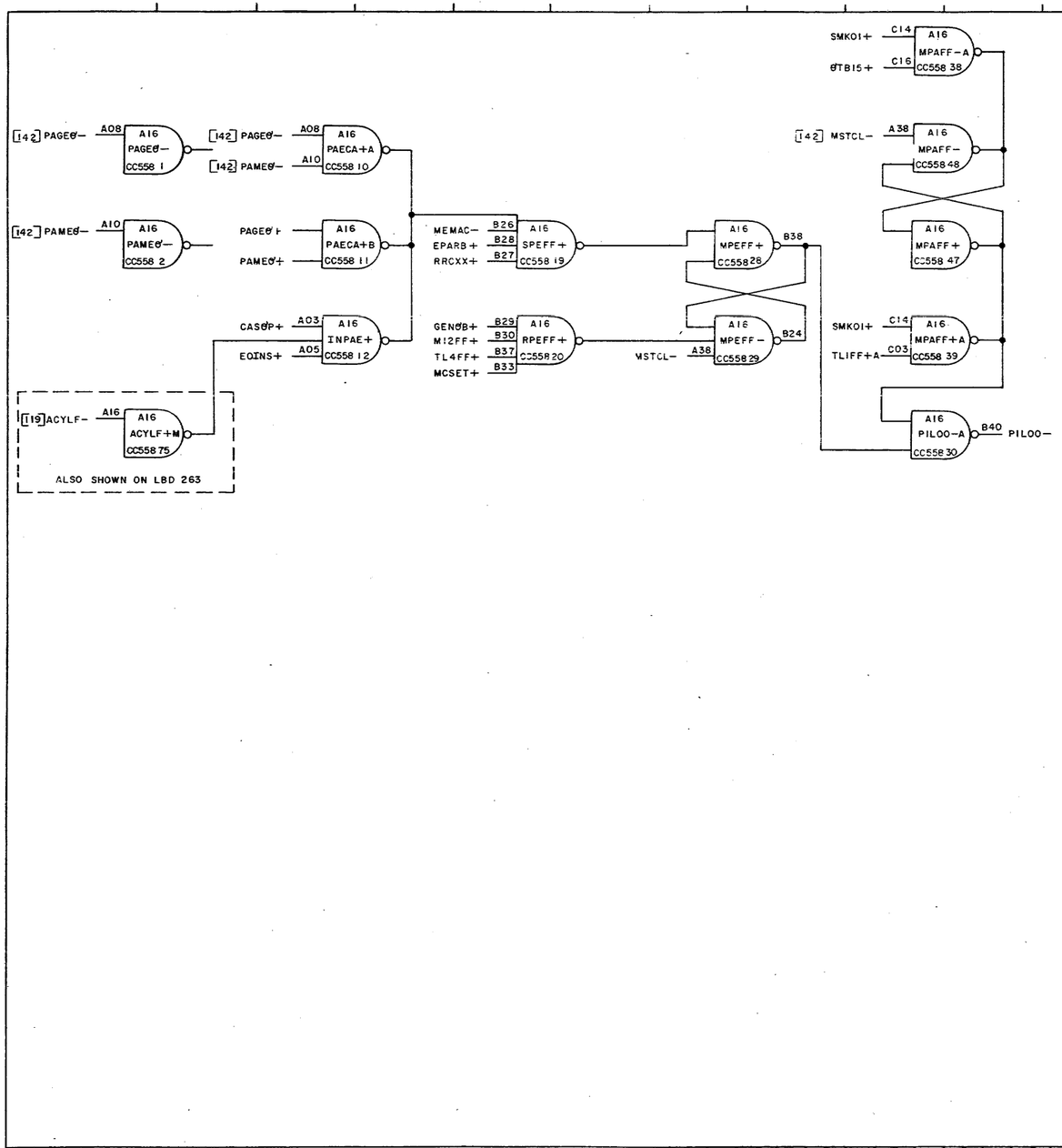
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass

DR. P. BELBUSTI	DATE 8/22/72
ENG. M OLSEN	8/22/72
APP.	
PROJECT NO. 6014	

TITLE
H-316-0611
MEMORY EXPANSION
CONTROL LOGIC

SIZE	DWG NO	REV.
C	70032796	A

L.B.D. NO. .137



NOTES:

1. WITHOUT MLO ALL GATES ON THIS LBD ARE ON THE CC621 PAC.

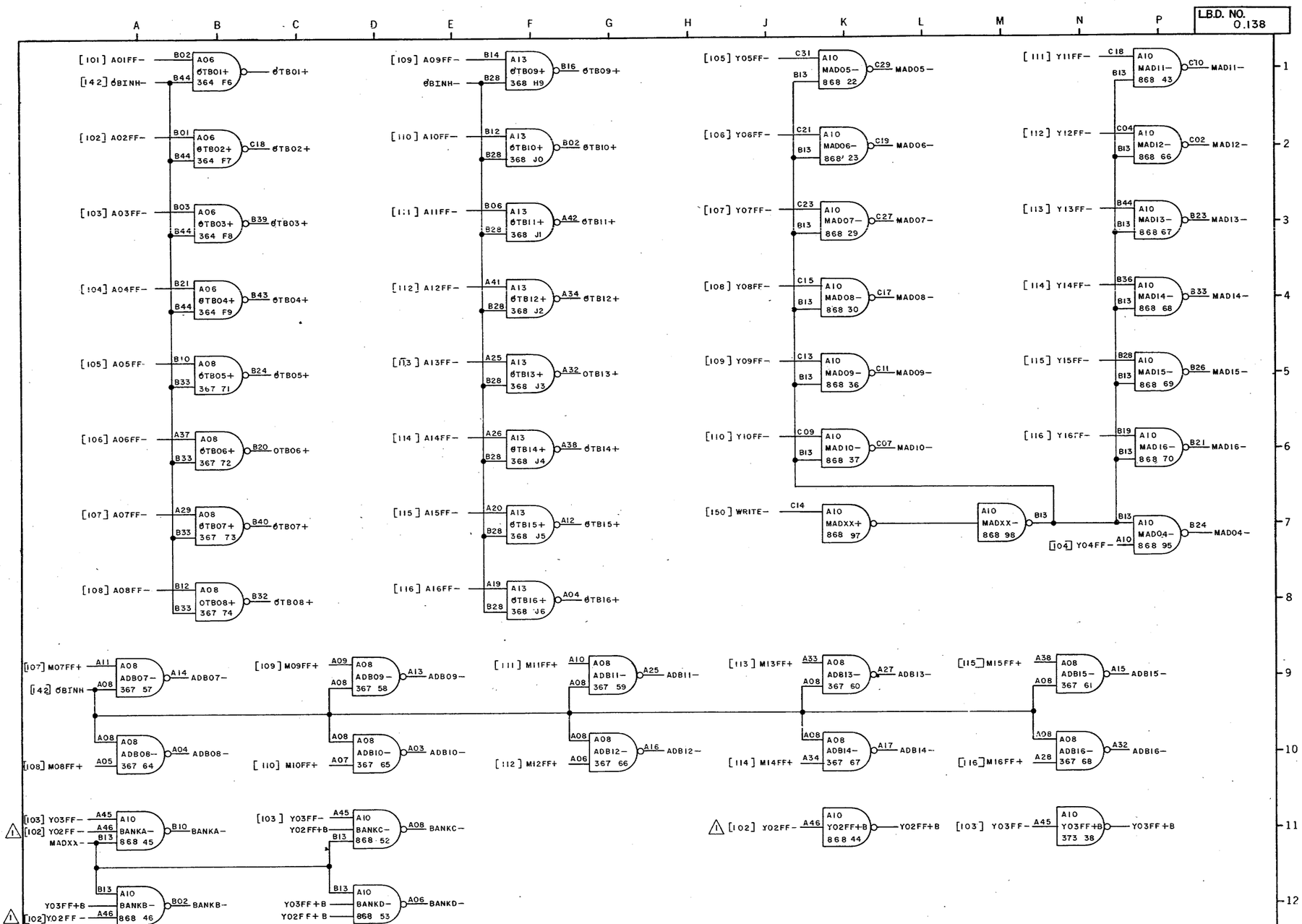
REV	REVISIONS	CHK
A	ORIG BY ENG	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path Framingham, Mass

DR P BELBUSTI	DAT 8/22/72
ENC. M. OLSEN	8/22/72
APP.	
PROJECT NO. 6014	

TITLE
H-316-0711
MEMORY PARITY LOGIC

SIZE	DWG NO.	REV.
C	70032798	A



NOTES:

1. ADD Y02FF-WITH EXT. ADD OPTION
2.
3.
4.

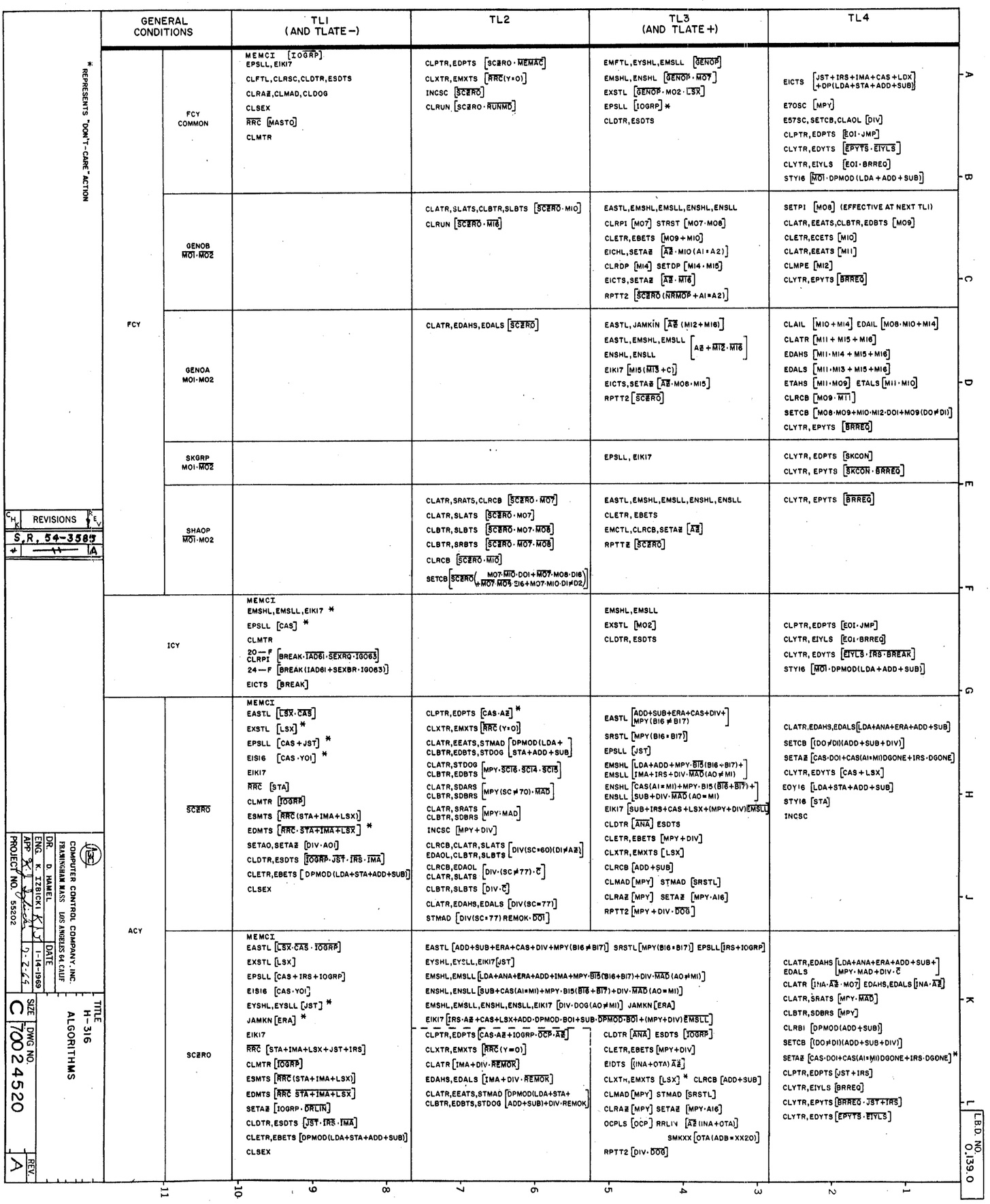
REV.	REVISIONS	CHK
A	ORIG BY ENG.	

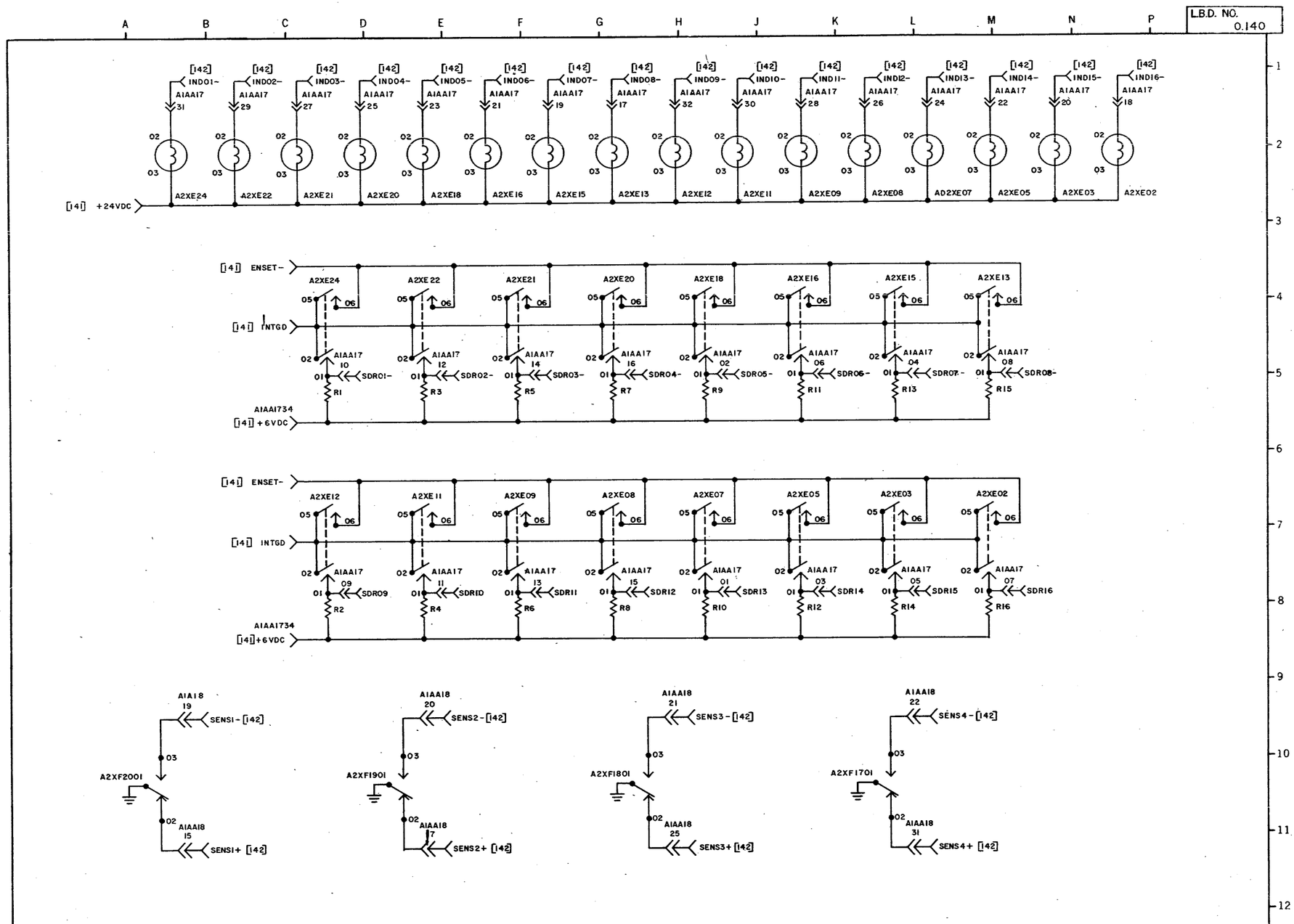
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path Framingham, Mass

DR. P. BELBUSTI	DATE 8/22/72	
ENG. M. OLSEN	8/22/72	
APP.		
PROJECT NO. 6014		

TITLE
H-316—0110
OUTPUT BUSES

SIZE	DWG NO.	REV.
C	70032794	A


GENERAL CONDITIONS
TL1 (AND TLATE−)
TL2
TL3 (AND TLATE+)
TL4
FCY
FCY COMMON
GENOB M01·M02
GENOA M01·M02
SKGRP M01·M02
SHAOP M01·M02
ICY
ACY
SCERO
SCERO
* REPRESENTS "DON'T-CARE" ACTION
REVISIONS
S,R, 54-3585
A
COMPUTER CONTROL COMPANY, INC.
FRAMINGHAM MASS. LOS ANGELES 64 CALIF.
DR. D. HAMEL 1-14-1969
ENG. K. ZABICKI
APP. 1-22-69
PROJECT NO. 55202
TITLE H-316 ALGORITHMS
SIZE C
DWG NO. 7002 4520
REV. A
LBD. NO. 0,139.0
4-40



NOTES:

1. ALL RESISTORS SHOWN ON THIS PAGE ARE ON CC079 CABLE PAC AIAA17

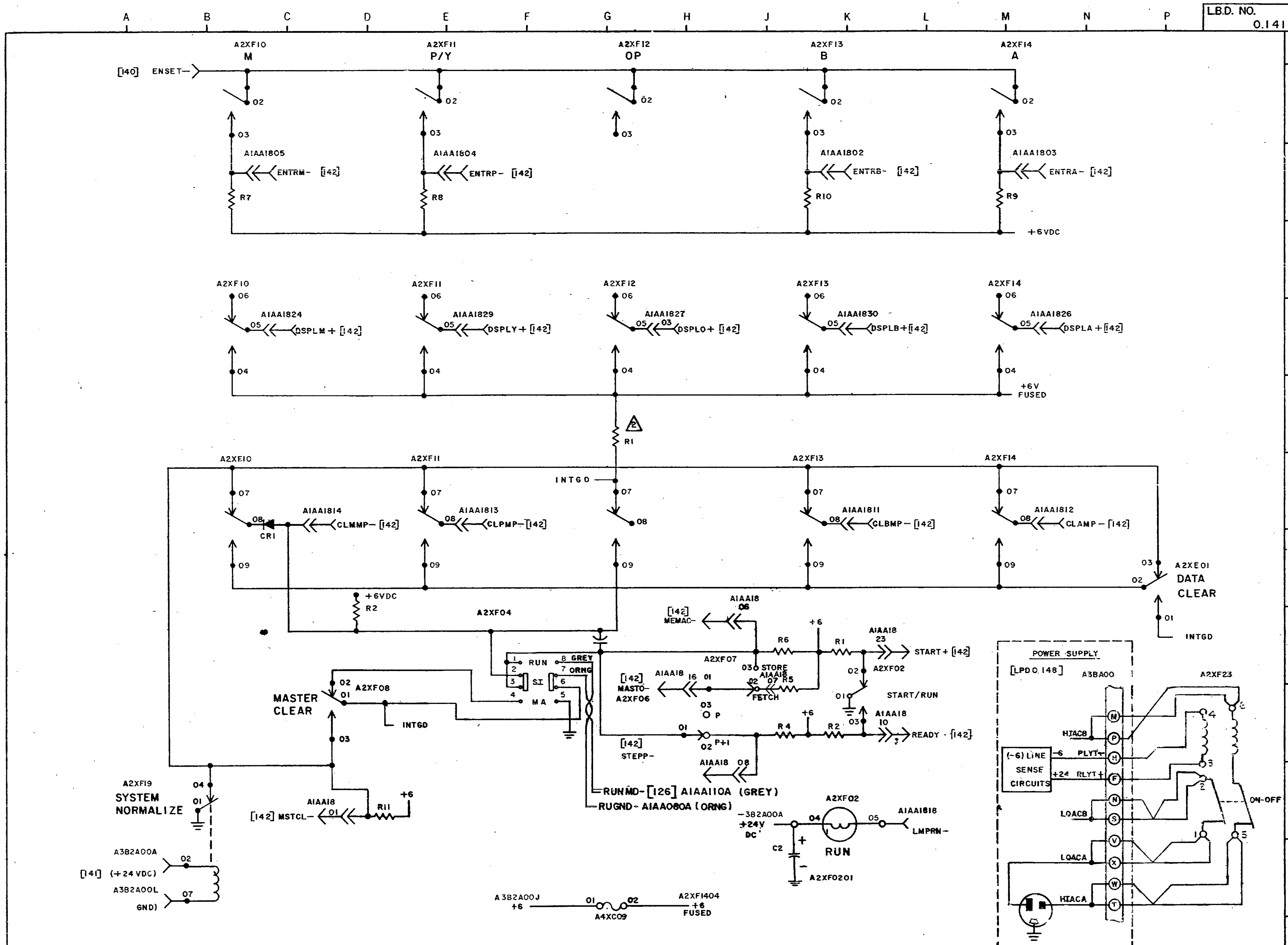
REVISIONS	REV.	
	A	SR-664-9335
	B	ECO 9848

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. A. KMICINSKI	DATE 8/4/70	
ENG.	8-7-70	
APP.	8-25-70	
PROJECT NO. 07201		

TITLE
H-316
CONTROL PANEL
316-0/00

SIZE C | DWG NO. 70030115 | REV. B | 140



NOTES:

1. RESISTORS SHOWN ON THIS PAGE ARE ON CC080 PAC A1AA18
2. THIS RESISTOR MOUNTED CONTROL PANEL

REV.	A	B	C	D	E
REVISIONS	SR 667-9535	ECO 9645	ECO 10228 3-8-72	ECO 30189 SEE ECO 73/5/03	ECO 30216 SEE ECO 73/8/10
CHK.		S.S.R.	S.S.R.	T.L.B.	C.M.F.

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

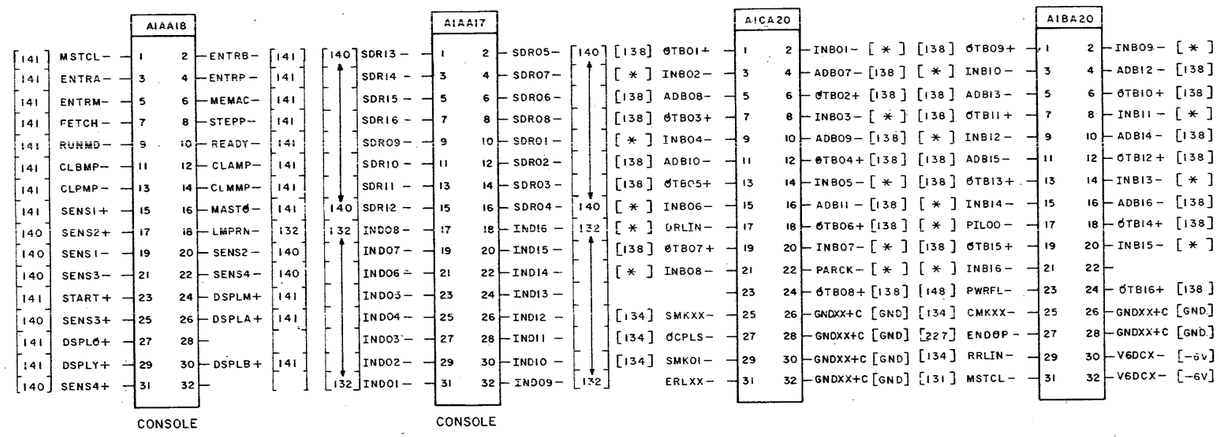
DR. A. KMICINSKI — DATE 8/4/70
ENG.
APP.
PROJECT NO. 07201

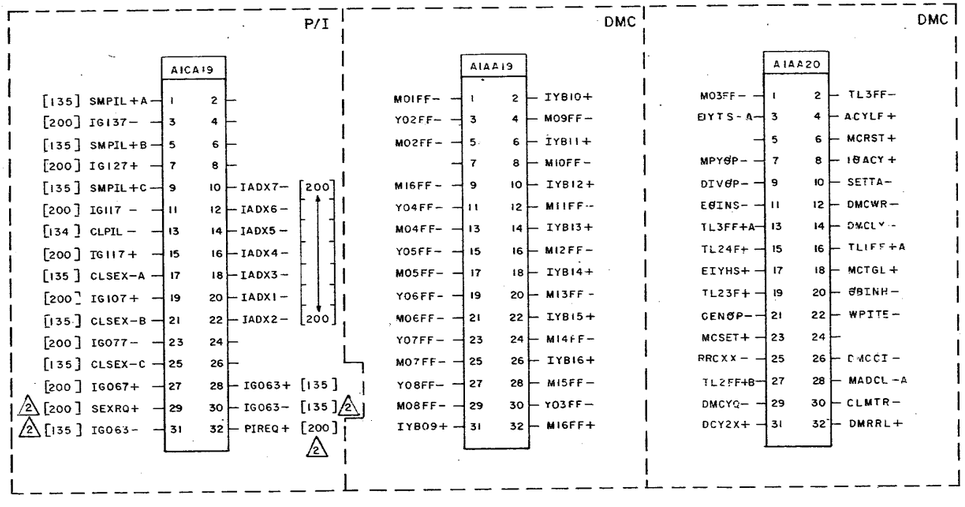
TITLE
H-316
CONTROL PANEL
SWITCHES
316-0/00

141

SIZE C — DWG NO. 70030116 — REV. E

L.B.D. NO. 0.142





NOTES:

1. * THESE SIGNALS ARRIVE BY BUS FROM I/O OPTIONS, DEPENDING ON SYSTEM CONFIGURATION.
2. WITH NO PI TIE SEXRQ÷ AND PIREQ+ TO IG063—

REV.	REVISIONS	CHK.
A	ORIG BY ENG	

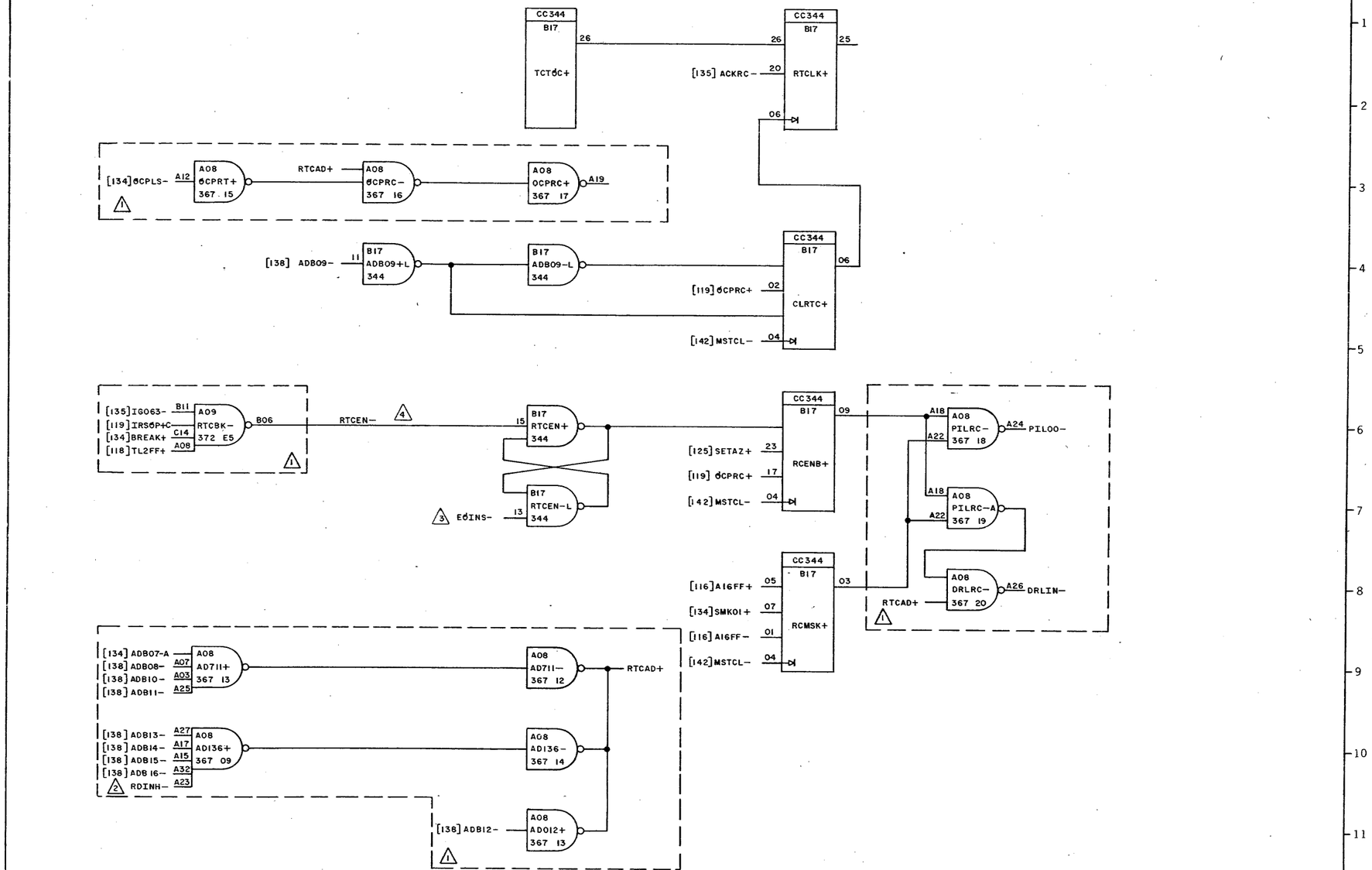
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. P BELBUSTI	DATE 8/22/72
ENG. M. OLSEN	8/22/72
APP.	
PROJECT NO. 6014	

TITLE
H-316-0110
CONSOLE AND I/O CONNECTORS

SIZE	DWG NO.	REV.
C	70032797	A

L.B.D. NO. 0.147



NOTES:

1. THESE CIRCUITS ARE ALSO SHOWN ON L.B.D. 0.119
2. REMOVE GND WHEN USING RTC
3. WHEN SDMC OR HSDMC IS INSTALLED EOINS– BECOMES RTCCL— FROM DMC
4. WHEN SDMC OR HSDMC IS INSTALLED RTCEN– BECOMES RTCEN–A FROM DMC

REV.	REVISIONS	CHK
A	[illegible]	
B	ECO 7748 EXT CHANGES SEE ECO T.A. 1/9/70	
C	ECO 8654 EXT. CHGS SEE ECO A.K. 8/14/70	
D	ECO 9365 EXT. CHGS SEE ECO S.S.R. 6/7/71	
E	ECO 10228 SEE ECO S.S.R. 3/6/72	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. D. HAMEL	DATE	
ENG. K. IZBICKI	2-27-69	
APP. [illegible]	4/10/69	
PROJECT NO. 55202		

TITLE
H-316-12
REAL TIME CLOCK

SIZE C | DWG NO. 70024524 | REV. E

L.B.D. NO. 0.148

A4XC07

MSTCL- 3 — SYSTEM NORMALIZE [141]

A3B2A

11 F — [141] RLYT-

12 H — [141] RLYT+

8, 9 A — +24 VDC

1, 2 D — COMMON

14 U — [141] LOFAN

15 R — [141] HIFAN

5 J — +6VDC

6 — +6VDC FUSED

18 M — [141] HIACB

4 —

7 —

19 N — [141] LOACB

S — [141] LOACB

[SEE LBD 141]

HIGH LINE

LOW LINE

CONTROL PANEL

ON-OFF

10 —

13 —

17 V — [141] LOACA

X — [141] LOACA

16 W — [141] HIACA

T — [141] HIACA

LOW LINE

HIGH LINE

+24 — (-6) LINE SENSE CIRCUITS — LINE SENSE WINDING

TO FANS

EXHAUST UNIT

A1A

A2A

A3A

A3B3B

A3B4B

A3B1B

115 VAC 10A 50/60 HZ INPUT

A3B2B

24VAC @ 1A

X — +6VDC

Y — COMMON

Z — -6VDC

POWER STATUS CIRCUITS

PWR STATUS CIRCUIT

COMMON — (PS) PWRFL- (FAULT SIGNAL TO OPTIONS) [143]

+24VDC

K1

CR4

330Ω ± 5%, 1/2W

+24VDC

6.2K ± 5%, 1/2W

CR1 CR2 CR3

Q1

820Ω ±5%, 1/2W

LINE FAULT SIGNAL [135] PFINT-

COMMON

TO LINE SENSE CIRCUIT

(B2A-J)

6.8K ±2% 1/4W

22MH

(B2A-D)

A5A

(B2A-A)

A4A

SERIES REGULATOR

A3B2C

X — S — +6VDC

H — +6VDC MEMORY

Y — E — BLK. 1 GND

D — 9 BLK GND

C — MEMORY GND.

Z — K — -6VDC MEMORY

P — WHT 3 -6VDC

M, N — TEMP SENSE ELEMENT (MEM. THERMISTOR)

B — +15.5 VDC @ 5A MEMORY

A — YEL. 4 +24VDC

RED 5, BLK 6 — TO ASR

[341] TYSIG-

AIXF01

BLUE 7 — LINE FAULT SIGNAL ([135] PFINT-)

8 BLUE — POWER STATUS (PWRFL-) [143] (PULLUP RESISTOR LOCATED ON 373 PAC A1AA1QU1)

AICA2Ø47

RED 2 — +6VDC

BLK. 1 — GND

9 BLK — GND

AIC A0924 C0924 B2023

(+B2023) from 30924-372 B1118 to C0401

NOTES:

1. CONNECTIONS NOT USED WITH FAST RECOVERY AUTO RESTART MODEL 316-1250

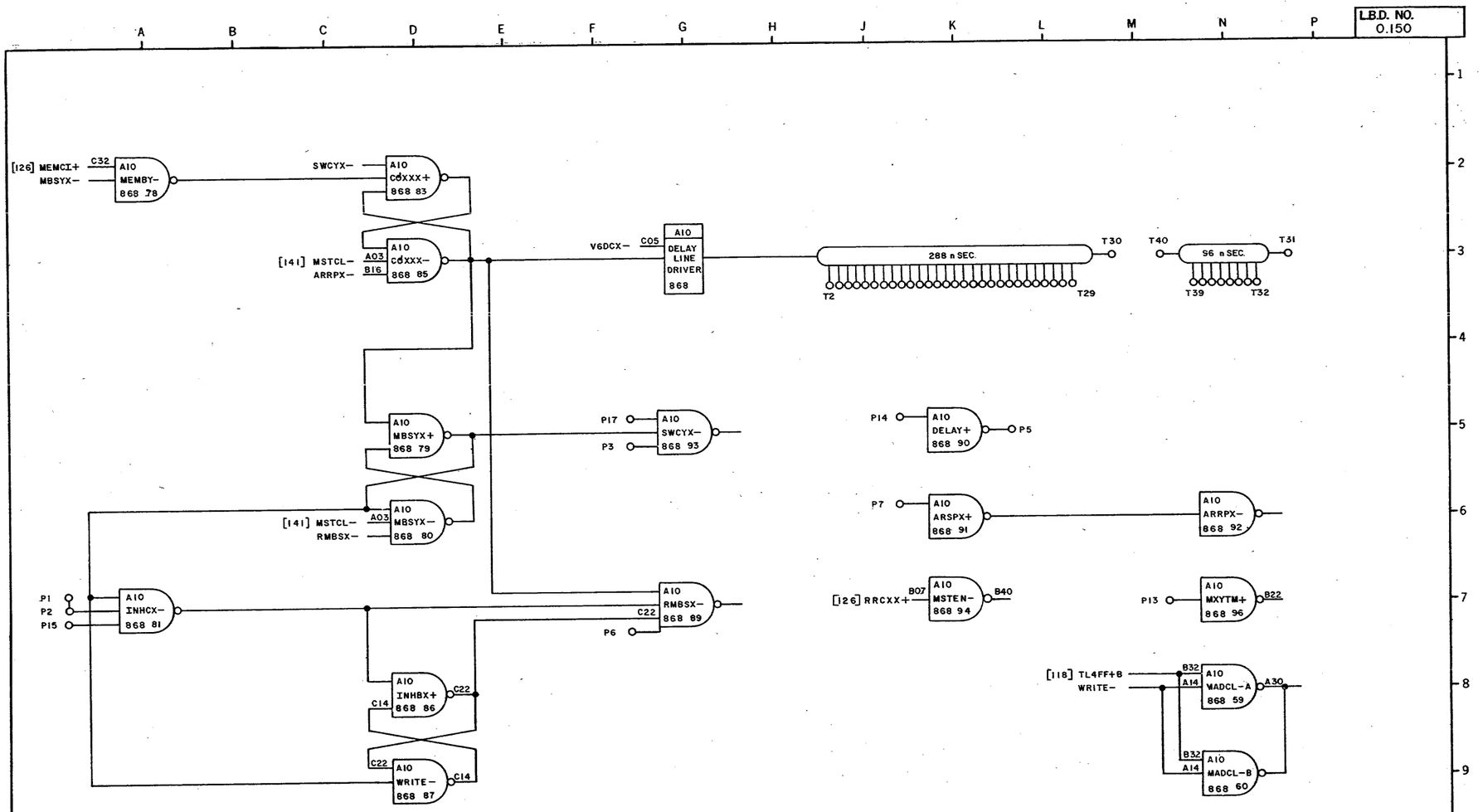
REV.	REVISIONS	CHK.
A	S.R. 54-3585	
B	ECO 7748 EXT. CHANGES SEE ECO TA.	
C	ECO 9086 EXT. CHGS SEE ECO S.S.R. 3/18/71	
D	ECO 9505 EXT CHGS SEE ECO P8 5/18/71	
E	ECO 10229 SEE ECO S.S.R. 3/29/72	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. [illegible]	DATE	
ENG. K. TZELICKI	1-8-1969	
APP.	7-2-69	
PROJECT NO. 55202		

TITLE
H-316
POWER SUPPLY & POWER DISTRIBUTION

SIZE C — DWG NO. 70024525 — REV. E



NOTES:

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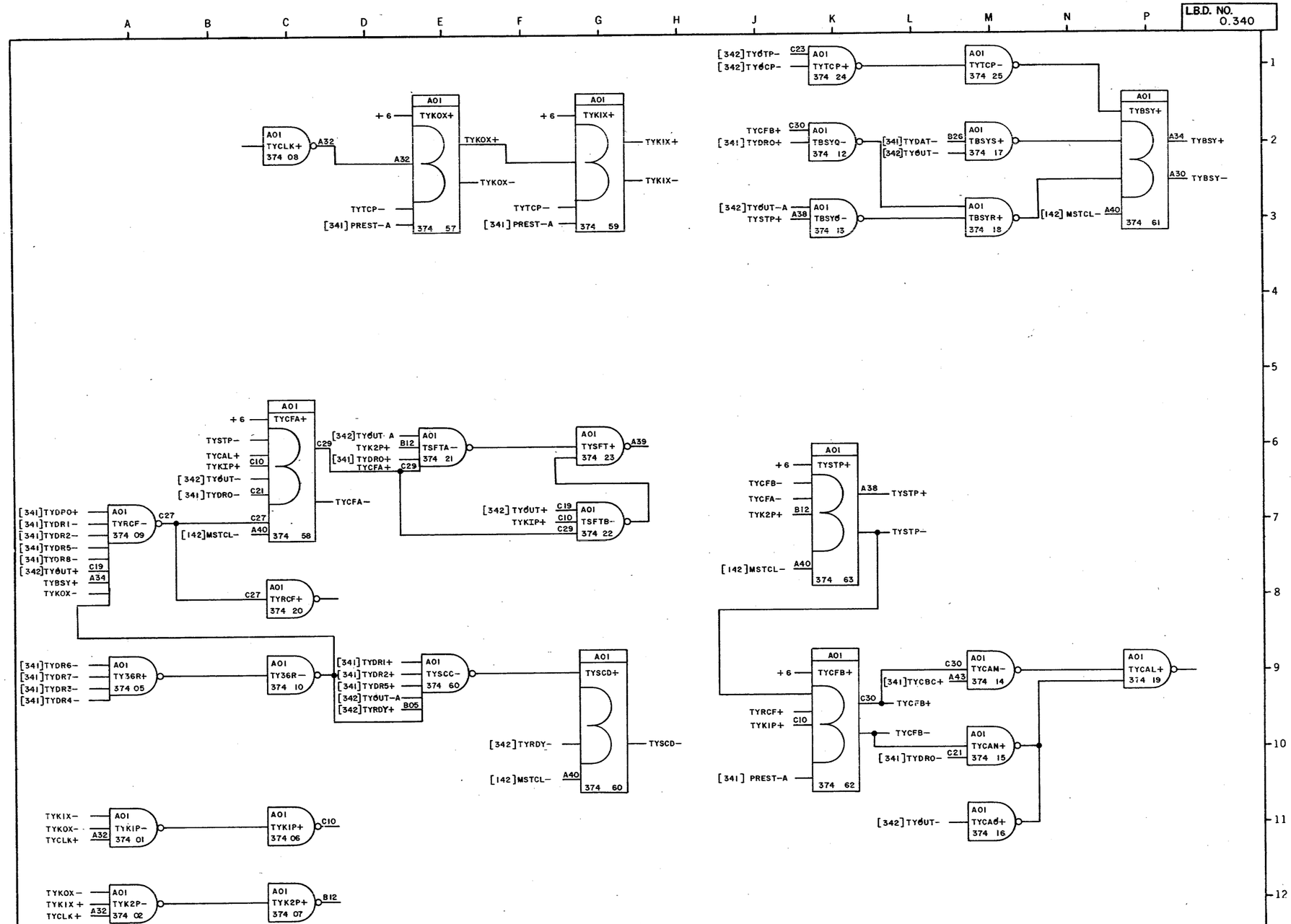
REVISIONS	REV.	
CHK.	A	ORIG BY ENG

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. P BELBUSTI	DATE 8/22/72
ENG. M. OLSEN	8/22/72
APP.	
PROJECT NO. 6014	

TITLE
H-316-0110
TIMING & CONTROL

SIZE	DWG NO.	REV.
C	70032795	A



NOTES:

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△

REVISIONS	REV.	
	A	S.R. 54-3585
CHK.		

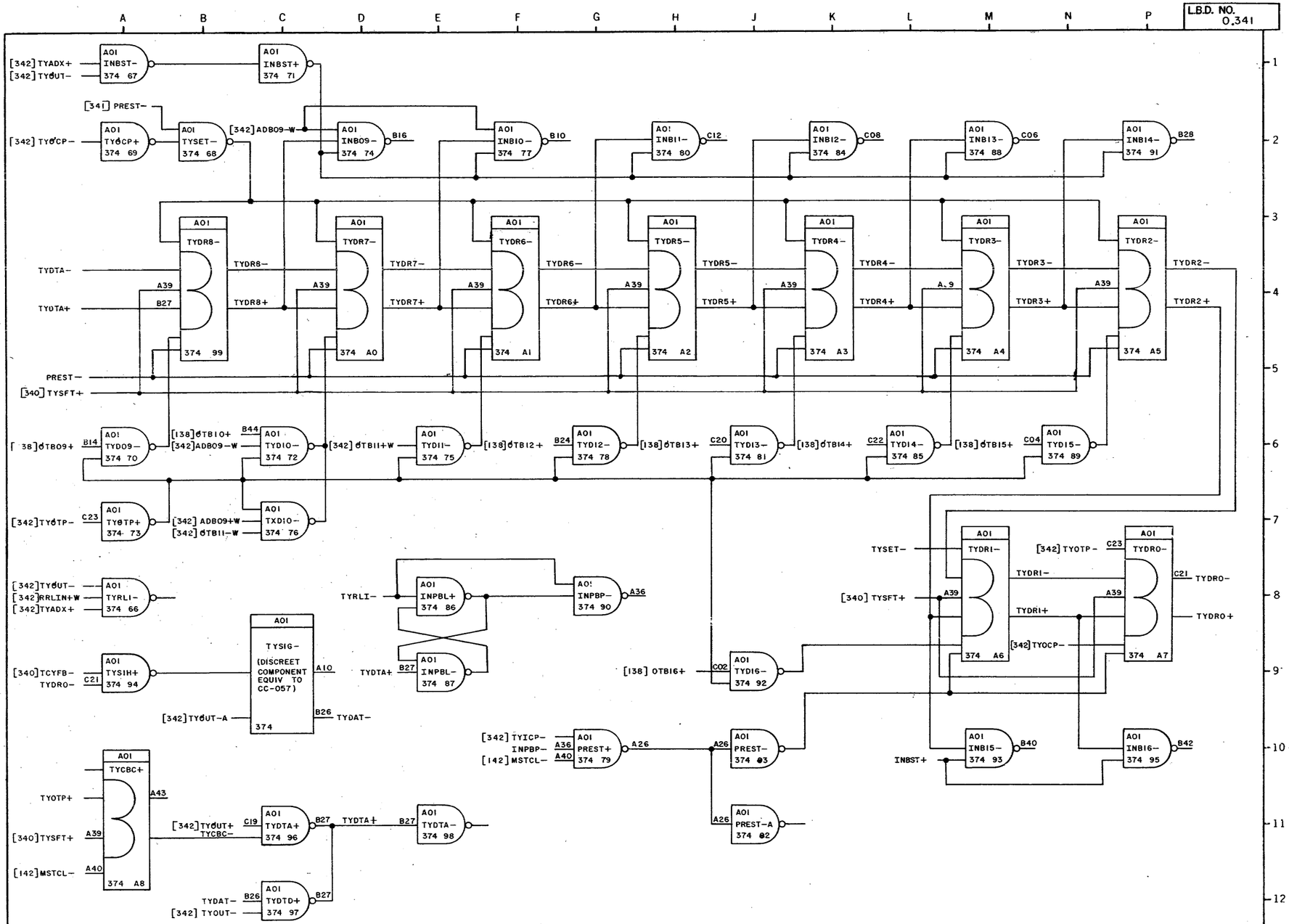
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass

		DATE
DR.	D. HAMEL	
ENG.	K. IZBICKI	1-9-1969
APP.		9/10/69
PROJECT NO.	53202	

TITLE
H-316
ASR 33/35
CONTROL

SIZE	DWG NO.	REV.
C	70024526	A

L.B.D. NO. 0,341



NOTES:

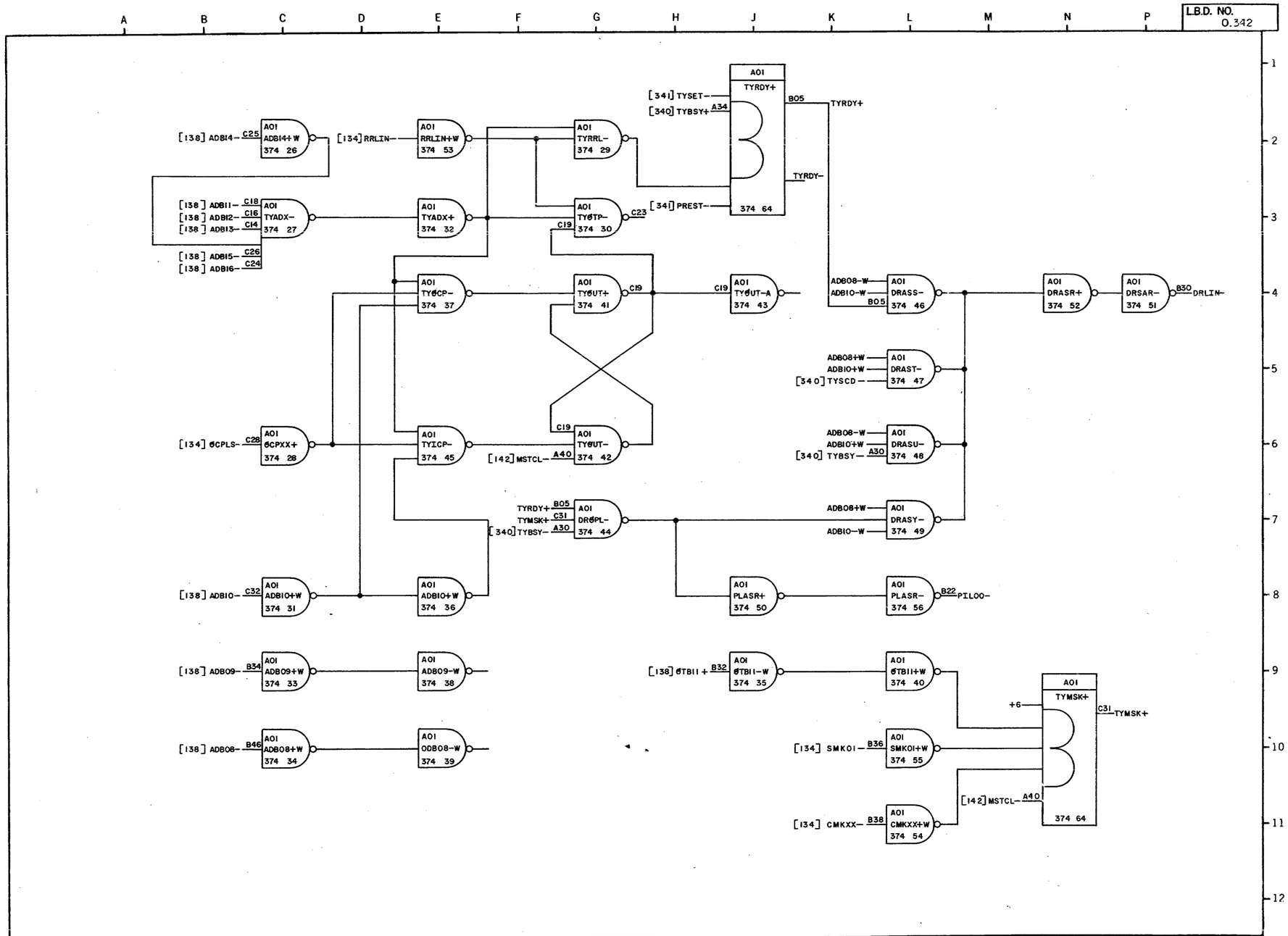
REV.	REVISIONS	CHK.
A	S.R. 54-3595	
B	ECO 7748 EXT CHANGES SEE ECO T.A. 1/19/17	
C	ECO 8302 EXT. CH05 SEE ECO 5/11/70 A.K.	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass

DR.	D. HAMEL	DATE
ENG.	K. IZBICKI	1-8-1969
APP.		1/10/69
PROJECT NO.	53202	

TITLE
H-316-56
BUFFER REGISTER
ASR 33/35

SIZE	DWG NO.	REV.
C	70024527	



NOTES:

REVISIONS	REV.	
	A	S.R. 54-3585

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

		DATE
DR.	J.D. GILMARTIN	
ENG.	K. IZBICKI	1-9-69
APP.	W. Phalen	4/10/69
PROJECT NO.	53202	

TITLE
H-316
ADDRESS & SKS
ASR 33/35

SIZE	DWG NO.	REV.
C	70024528	A

FIELD ENGINEERING MANUAL
USERS' REMARKS FORM

TITLE:

DOC. PART NO. _____
DATED _____

ERRORS NOTED:

Fold

Cut Along Line

SUGGESTIONS FOR IMPROVEMENT:

Fold

DATE _____

FROM: NAME _____
COMPANY _____ M/S _____
TITLE _____
ADDRESS _____
_____ ZIP _____

FIELD ENGINEERING MANUAL
USERS' REMARKS FORM

TITLE:

DOC. PART NO. _____
DATED _____

ERRORS NOTED:

Fold

Cut Along Line

SUGGESTIONS FOR IMPROVEMENT:

Fold

DATE _____

FROM: NAME _____
COMPANY _____ M/S _____
TITLE _____
ADDRESS _____
_____ ZIP _____

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