System 90 Manufacturing Diagnostic Specification

Table of Contents

1.0 OVERVIEW

The System 90 is a complex, highly advanced, Super-micro computer system. This new product will provide increased computing power and processing speed beyond current product capabilities.

This new product also provides a challange to design a system that is manufactureable, testable, and reliable. To that end, this document contains guidlines for development of manufacturing diagnostics.

2.0 REQUIREMENTS

2.1 MANUFACTURING DIAGNOSTICS

The Manfuacturing level diagnostics should be designed to troubleshoot and debug to the component level all functional blocks of a board. The diagnostic engineer may utilize any external test equipment commonly found in a production environment.

2.1.1 GOALS

The diagnostic must :

* support a user base of semi-skilled technical labor
* provide a user friendly interface
* provide a MTTR of not more than 1 hour per fault.
* require a minimal amount of test equipment:
* achieve 95 percent fault detection
* achieve 85 percent fault isolation
* provide error resolution to a component level where ever possible.

To accomplish these goals the following techniques are recommended:

Menu Driven Interface
Help Screens
Individual Test Selection (Go/NoGo)
Run all tests (Go/NoGo)
Loop on all tests (Extended testing)
Loop on Test (Intermitent failure detection)
Stop on Error (Breaks Loop on Error Detect)

The manufacturing diagnostic user environment is:

Test Station
1 Disk Drive (SCSI 170)(SMD 168)
UNIX 5.3 OS
1 Floppy (5.25 96TPI Dual Speed DSDD)
1 ARBITER
1 CSS/A1000 MOTHER BOARD
1 SPM
1 CPU (PM68020)
1 MM (8MB)
1 IOA
1 IOM
1 EDT (EDT/EDT-SCSI)
1 GCP (GCP/EGC/GC16)

Terminal
Oscillioscope 300Mhz
DVM

The manufacturing burn-in user environment is:

1 MPCS Host with download capabilities through the console of the target machine.
1 Terminal attatched to the Host

3.0 BOARD DIAGNOSTIC GUIDELINES

3.1 POWER UP DIAGNOSTICS

The power-up diagnostics should provide sufficeint fault detection to insure the ability of the board or peripheral to achieve a first level boot. If the board cannot initiate a first level boot, the error should be indicated on the console port of the SPM, the console port of the board (where provided), or the LED status registers.

3.2 MONITOR COMMANDS

3.2.1 SPM

3.2.1.1 BOOT LEVEL OPTIONS

System Boot

Device Boot
- disk
- tape
- floppy

System Reset
- soft reset
- hard reset

  The MPCS host at SBI requires the capability to reset the system under software control from the monitor. This is used several times in the Burn-In process to bring the machine to a known state.

- device reset
  - CSS board
  - IO Board
  - Disk
  - Tape

System Status
- Print System Config from NV RAM
- Edit System Config data in NV RAM
- Interogate System For Config data
- Update System Config data in NV RAM

System Test
- Debugger
- Interrupt Diapatcher Diag
- Interrupt Diapatcher Tests
- Floppy Based Diagnostics
- IO Debugger
- Memory Tests
- RWI Tests

Serial Down Load

Clock Source

Help Menus

3.2.1.2 SPM DEBUGGER

68202 CPU Cache Enable/Disable
Clock Source

Display Memory
Fill Memory
Modify memory
Move Memory
Compare Memory
Search Memory
Memory Simulation Mode
Initialize CSS
Reset CSS
Initialize Interrupt Dispatcher
Reset Arbiter Count
Increase Arbiter Count
Jump & Execute
Map Slot
Execute form main memory
Read/Set TOD Clock
Read Temp
Read Block
Write Block
Modify Bit Test
Set/Clear Bus Error Loop Flag
Set/Clear Bus Emulator Flag
Read Data From Device
    disk
    tape
    floppy

The MPCS host at SBI requires the capcbility to read one sector or block of data from each of the bootable devices to see if bootable media is present, and the device is functional.

3.2.1.3 SPM/IOM DEBUGGER

IOM Interrupt vector table W/R Loop
IOM Interrupt Test Loop
IOM Interrupt Counter Loop
IOM Response Overflow Test
IOM Command Overflow Test
IOM Data Error Test
IOM Down Link Parity Test
IOM Bus Grant Timeout Test
IOM Response Timeout Test
IOM Response-Source Mis-match Test
IOM Source Slot Error Test
IOM Memory write
IOM Memory read
IOM Memory Verify
IOM 8 Command Write Loop
IOM 16 Command Write Loop
IOM 4 Read Command Loop
IOM Error Register Test
Display IOM Memory Simulation Information
IOM registers W/R test
IOM/IOA Command register Test
IOM/IOA ICB Data Bus Test
IOM/IOA ICB Address Bus Test

3.2.1.4 SPM/IOA DEBUGGER

Reset IO System
IOA Register Test
IOA Command Register Read Loop
IOA ICB data strobe Test
IOA ICB data bus Test
IOA ICB Address bus Test
IOA ICB W/R Loop

IOA Interrupt Test
IOA DMA Test
IOA 4 Channel DMA Test
IOA Poll Slots
Show system config

3.2.1.5 SPM/MM DEBUGGER

Main Memory Test Loop
Main Memory Test 1 Loop
Main Memory Test 2 Loop
Main Memory Test 3 Loop
Main Memory Test 4 Loop
Main Memory Test 5 Loop
Main Memory Test 6 Loop
Main Memory Test 7 Loop
Main Memory Test 8 Loop
EDAC On/Off
EDAC Test
EDAC Test Loop
EDAC Checkbits Test
EDAC Pending Test
EDAC Interrupt Test Loop
EDAC 8,16,32 Byte Read Test
EDAC 8,16,32 Byte Read Test Loop

3.3 DOWNLOADABLE DIAGNOSTICS

At FCT , the station is powered up, and down many times per shift, and even several times while troubleshooting the same board. This form of diagnostics may not be desirable in this application.

4.0 SYSTEM DIAGNOSTICS GUIDELINES

4.0.1 DOWNLOADABLE DIAGNOSTICS

The downloadable diagnostics require an additional host to download tests to each of the target systems. The central host provides a means of diagnostic revsision control. The link to the target systems would be by serial RS232 link. The host would send the test down through one of its slave ports to the console port of the SPM of the target system.

The downloadable diagnostic modules should be kept small to reduce download time to 20-30 seconds. This is sufficient time to download approximately 26K of code and data. If this criteria cannot be met, the diagnostic should be moved to a higer transfer rate medium such as floppy or tape.

4.0.2 FLOPPY RESIDENT DIAGNOSTICS

The floppy resident diagnostics will consist of three basic modules. The first module is the boot loader, the second is the diagnostic executive, and the third is the diagnostic overlays.

The boot loader will initalize memory, and read in the diagnostic executive into local memory of the SPM board.

The executive will the post an appropriate signon message, and present a main menu. The user will then select an option from the menu, and the test overlay requested will be loaded into local memory directly above the executive. The executive will then enter the overlay, and execute the desired test. The executive will leave the overlay resident until a test on another overlay has been selected. The executive will provide for global test selection, so that several tests may be selected for execution even though the tests may reside in different overlays.

The test overlay will provide the executive with a jump table which contains entry points into the module. Upon completion of the test the overlay will return control and status to the executive.

4.0.3 TAPE RESIDENT DIAGNOSTICS

4.1 STANDALONE SINGLE TASKING DIAGNOSTICS

4.1.1 PERIPHERAL TESTS

4.1.1.1 DISK

4.1.1.1.1 SMD

- Unit Select
- Recal
- Format
- Write
- Read
- Seek
- Multi-Sector Write
- Multi-Sector Read
- Random Seek

4.1.1.1.2 SCSI

- Unit Select
- Request Sense
- Read Capacity
- Format
- Recal

Write
Read
Seek to Block
Multi-Sector Write
Multi-Sector Read

4.1.1.1.3 FLOPPY
Initialize Floppy
Floppy Test
Write Sector Loop
Read Sector Loop
Write/Read/Verify Sector Loop
Write/Read/Verify Floppy Loop
Report Status
Motor On/Off
Unit Select
Recal
Format Disk
Format Track
Write Sector
Read Sector
Seek
Multi-Sector Write
Multi-Sector Read
Random Seek

4.1.1.2 TAPE

4.1.1.2.1 STREAMING CARTRIDGE
Rewind
Write
Read
WriteFM
ReadFM
Append
Tension
Erase
Capacity

4.1.1.2.2 NINE TRACK
Rewind
Write
Read
WriteFM
ReadFM
Append
Cache

4.1.1.3 POWERSUPPLY
Load Performance Degradation
Noise Immunity
Surge Capacity
OV Protection
OI Protection
Thermal Protection

4.1.2 BOARD TESTS

4.1.2.1 RWI
SCC Tests
Internal Loop Back
External Loop Back
CIO Tests
register & Interrupt Test
Timer Test
Output Test

Read Ports Test
A/D Test
Voltage margining
Internal Tempature monitoring
Power On/Off

4.1.2.2 ARBITER

4.1.2.3 BACKPLANE

4.1.2.4 SPM

68202 CPU Cache Enable/Disable
Clock Source
Display Memory
Fill Memory
Modify memory
Move Memory
Compare Memory
Search Memory
Memory Simulation Mode
Initialize CSS
Reset CSS
Initialize Interrupt Dispatcher
Reset Arbiter Count
Increase Arbiter Count
Jump & Execute
Map Slot
Execute form main memory
Read/Set TOD Clock
Read Temp
Read Block
Write Block
Modify Bit Test
Set/Clear Bus Error Loop Flag
Set/Clear Bus Emulator Flag
Read Data From Device
- disk
- tape
- floppy

The MPCS host at SBI requires the capcbility to read one sector or block of data from each of the bootable devices to see if bootable media is present, and the device is functional.

NV RAM Integrity Test
Dispatcher Diagnostics
- Acknowledge Interrupt
- Display Dispatcher Memory
- Modify Dispatcher Memory
- Receive Interrupt Request
- Fill Queue with Interrupts
- Display Queue Status
- Reset
- Request CPU Service
- Read Board Id

Dispatcher Tests
- Self Test
- Non-directed Interrupts
- Directed Interrupt Test
- Directed Interrupt Test - Single CPU
- Non-directed and Directed Interrrupts Test
- Half Test - IOM to dispatcher
- Half Test - IOM to all slots
- IPCC Handshake

Forced Error Test
Poll Slots
Show Local Slot Enable/Disable Status

4.1.2.5 PM

Led Test
Diag Bag LED Loop Test
Cache as Ram Test
Bus Tags as Ram
Cache Tags as Ram
MMU Tags as Ram
TLB as Ram
Interrupts
Interrupts from Alien
Receive Buffer Test
Nak Status Test
Timeout Status Test
Bad I/O Status Test
Table Walk Error Status Test
Command Register Test
System Bus Parity Status Test
Read Permissions Test
Write Permissions Test
Execute Permissions Test
Page Fault Test
High Traffic Write Test
Write Accelerator Buffer Test
Receive Funnel Test
Cache Write Through Test
Cache Write Through Miss Test
Cache Data Fill Test
Cache Read-Miss Fill Test
Cache Fill W/O Scrub Test
Cache Fill W/ Scrub Test
Cache Write-Miss/Valid Bit Test
Cache Window(MPMS) Test
Cache RMW-Hit, Match Bit Test
Cache FIFO Test
Cache Fill (Scope Loop)
Cache Scrub Fill W/ Spy Test
Cache Slave Write Test

4.1.2.6 MM

Main Memory Test Loop
Main Memory Test 1 Loop
Main Memory Test 2 Loop
Main Memory Test 3 Loop
Main Memory Test 4 Loop
Main Memory Test 5 Loop
Main Memory Test 6 Loop
Main Memory Test 7 Loop
Main Memory Test 8 Loop
EDAC On/Off
EDAC Test
EDAC Test Loop
EDAC Checkbits Test
EDAC Pending Test
EDAC Interrupt Test Loop
EDAC 8,16,32 Byte Read Test
EDAC 8,16,32 Byte Read Test Loop
Address Test
Walking 1's

Walking 0's
Pattern Sensitivity Test

4.1.2.7 IOM

IOM Interrupt vector table W/R Loop
IOM Interrupt Test Loop
IOM Interrupt Counter Loop
IOM Response Overflow Test
IOM Command Overflow Test
IOM Data Error Test
IOM Down Link Parity Test
IOM Bus Grant Timeout Test
IOM Response Timeout Test
IOM Response-Source Mis-match Test
IOM Source Slot Error Test
IOM Memory write
IOM Memory read
IOM Memory Verify
IOM 8 Command Write Loop
IOM 16 Command Write Loop
IOM 4 Read Command Loop
IOM Error Register Test
Display IOM Memory Simulation Information
IOM registers W/R test
IOM/IOA Command register Test
IOM/IOA ICB Data Bus Test
IOM/IOA ICB Address Bus Test

4.1.2.8 IOA

Reset IO System
IOA Register Test
IOA Command Register Read Loop
IOA ICB data strobe Test
IOA ICB data bus Test
IOA ICB Address bus Test
IOA ICB W/R Loop
IOA Interrupt Test
IOA DMA Test
IOA 4 Channel DMA Test
IOA Poll Slots
Show system config

4.1.2.9 IOPM

4.2 STANDALONE MULTI TASKING DIAGNOSTICS

The Stand Alone Multi-tasking diagnostics will provide a means to troubleshoot system contention and timing errors. The kernal will load into the SPM and download drivers into each of the I/O Controllers.

Each I/O Controller will be responsible for testing each attached peripheral. The PM's will perform cache,mmu,spy, and memory tests. The SPM will provide status, and control through a menu driven interface at the console. The kernal on SPM will arbitrate system resources. The kernals on the I/O Controllers will make inter-processor requests to the SPM for memory allocation.

4.3 OS BASED DIAGNOSTICS

The current strategy is to use MST (Manufacturing System Test) as a multi-tasking diagnostic tool in the Unix environment.

5.0 SPECIFIC BOARD DIAGNOSTIC REQUIREMENTS

5.1 SPM

This board is the critical path for diagnostics in the S90 system. The diagnostics for the SPM must be designed to be durable, and thorough as possible.

5.2 PM

5.3 MM

5.4 IOM

5.5 IOA

5.6 IOPM

6.0 REMOTE DIAGNOSTIC CAPABILITIES

7.0 ONLINE DIAGNOSTICS

8.0 MILESTONES & SCHEDULE REQUIREMENTS

8.x FLOPPY BASED DIAGNOSTICS

The System 90 is scheduled for limited production in the second quarter of fiscal year 88/89. The floppy based system level diagnostics will be required at the end of the first quarter to develop an automated MPCS control program for manufacturing at SBI.