YAMAHA LSI

YMZ280B

PCMD8

8-Channel PCM/ADPCM Decoder

■ OVER VIEW

The YMZ280B is a PCM/ADPCM decoder for game machines that simultaneously plays back eight voices. Each voice data read from the external memory at the specified pitch is individually processed on the total level and panpot, and output in a 16-bit stereo data format. The voice data format can be selected from 4-bit ADPCM, 8-bit PCM and 16-bit PCM, according to the application. Maximum external memory address space of 16M bytes allows a large amount of voice data usage.

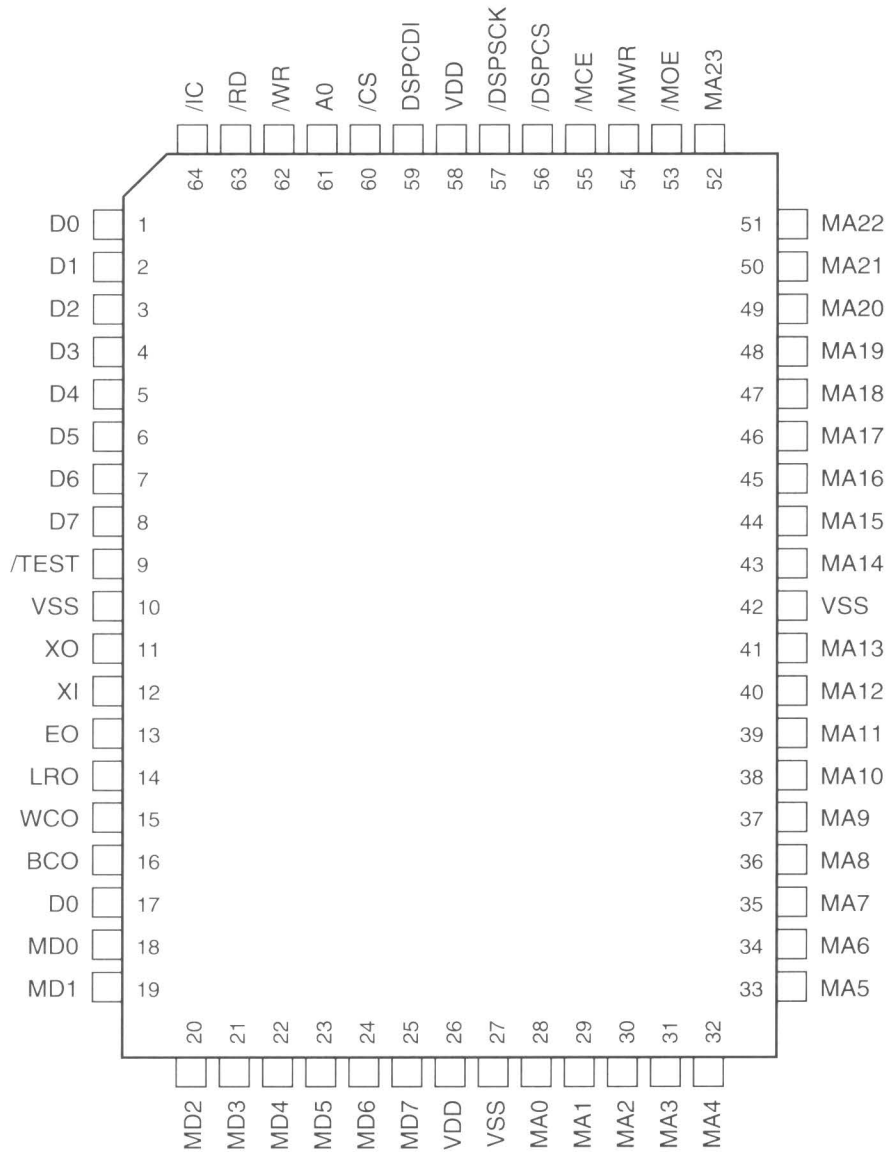
■ FEATURES

- Voice data stored in external memory can be played back simultaneously for up to eight voices.
- Voice data format can be selected from 4-bit ADPCM, 8-bit PCM and 16-bit PCM.
  The 4-bit ADPCM format is compatible with the YMZ263B (MMA).
- Control of voice data external memory
  Up to 16M bytes of ROM or SRAM (× 8 bits, access time 150ns max) can be connected.
  Continuous access is possible.
  Loop playback between selective addresses is possible.
- Voice data playback frequency control
  4-bit ADPCM ..... 0.172 to 44.1kHz in 256 steps
  8-bit PCM, 16-bit PCM ..... 0.172 to 88.2kHz in 512 steps
- 256 steps total level and 16 steps panpot can be set.
- Voice signal is output in stereo 16-bit 2's complement MSB-first format.
- YSS225 (EP) can be connected.
- +5V single power supply, silicon gate CMOS process
- 64-pin plastic QFP (YMZ280B-F)

YAMAHA CORPORATION

YMZ280B CATALOG
CATALOG No.: LSI-4MZ280B3
1996. 10

■ PIN OUT DIAGRAM



< 64pin QFP Top View >

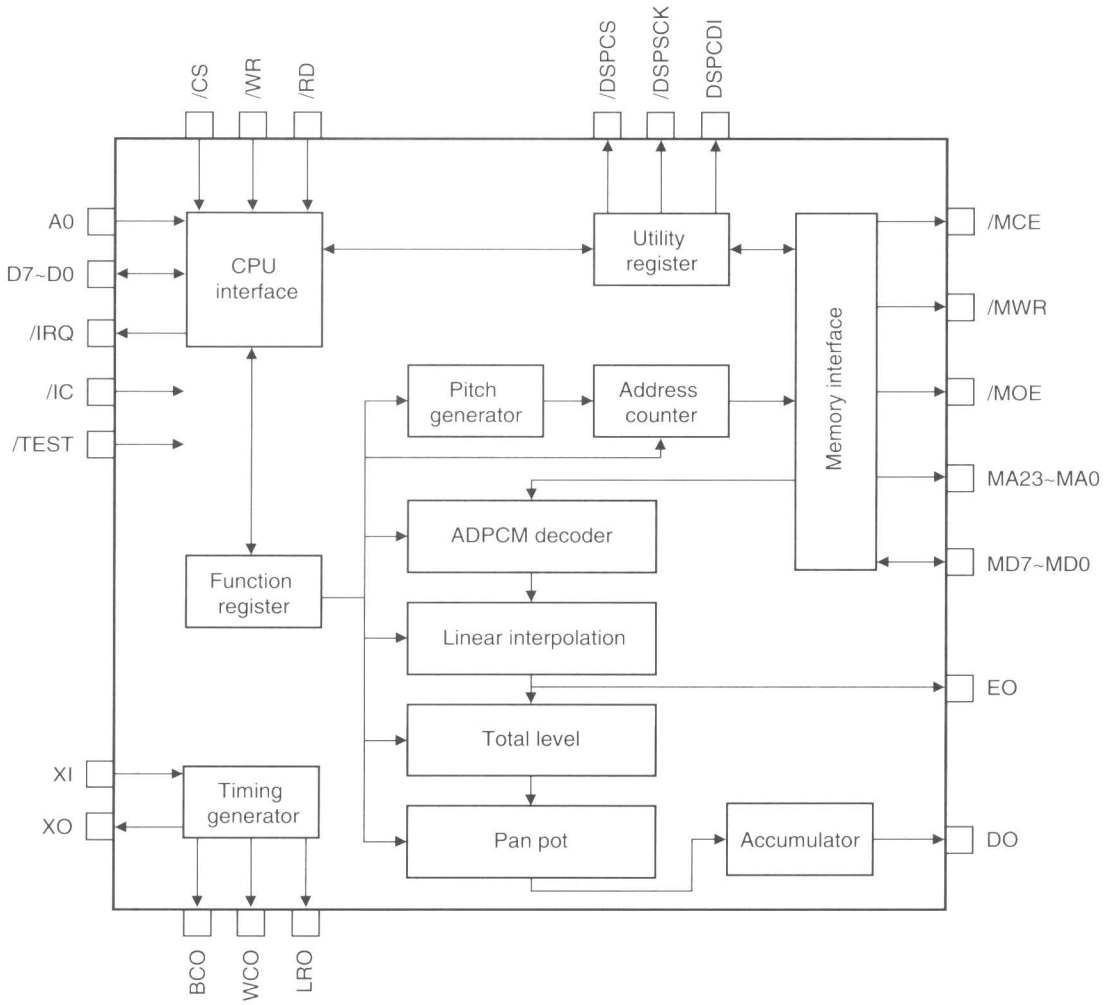
■ PIN DESCRIPTION

No.	Name	I/O	Function	
1	D0	I/O	CPU interface	data bus
2	D1	I/O		data bus
3	D2	I/O		data bus
4	D3	I/O		data bus
5	D4	I/O		data bus
6	D5	I/O		data bus
7	D6	I/O		data bus
8	D7	I/O		data bus
9	/TEST	I+	Test pin	
10	VSS	–	Ground	
11	XO	O	Crystal oscillator connecting pin	
12	XI	I	Crystal oscillator connecting pin or master clock input (16.9344MHz)	
13	EO	O	DSP voice data output	
14	LRO	O	LR clock output	
15	WCO	O	Word clock output	
16	BCO	O	Bit clock output	
17	DO	O	DAC voice data output	
18	MD0	I/O+	External memory	data bus
19	MD1	I/O+		data bus
20	MD2	I/O+		data bus
21	MD3	I/O+		data bus
22	MD4	I/O+		data bus
23	MD5	I/O+		data bus
24	MD6	I/O+		data bus
25	MD7	I/O+		data bus
26	VDD	–	+5V power supply	
27	VSS	–	Ground	
28	MA0	O+	External memory	address bus
29	MA1	O+		address bus
30	MA2	O+		address bus
31	MA3	O+		address bus
32	MA4	O+		address bus
33	MA5	O+		address bus
34	MA6	O+		address bus
35	MA7	O+		address bus
36	MA8	O+		address bus
37	MA9	O+		address bus
38	MA10	O+		address bus
39	MA11	O+		address bus
40	MA12	O+		address bus
41	MA13	O+		address bus

No.	Name	I/O	Function	
42	VSS	–	Ground	
43	MA14	O+	External memory	address bus
44	MA15	O+		address bus
45	MA16	O+		address bus
46	MA17	O+		address bus
47	MA18	O+		address bus
48	MA19	O+		address bus
49	MA20	O+		address bus
50	MA21	O+		address bus
51	MA22	O+		address bus
52	MA23	O+		address bus
53	/MOE	O+	External memory	control
54	/MWR	O+		control
55	/MCE	O+		control
56	/DSPCS	O	DSP interface	chip select output
57	/DSPSCK	O	DSP interface	clock output
58	VDD	–	+5V power supply	
59	DSPCDI,	O	DSP interface	control data output
	/IRQ	O	CPU interface	interrupt signal output
60	/CS	I+	CPU interface	chip select output
61	A0	I		address bus
62	/WR	I		write enable
63	/RD	I		read enable
64	/IC	I+	Initial clear	

Note) At initial clear, the MD7 to MD0, MA23 to MA0, /MCE, /MOE, and /MWR pins become high impedance.
+: Pin with built-in pull-up resistor.

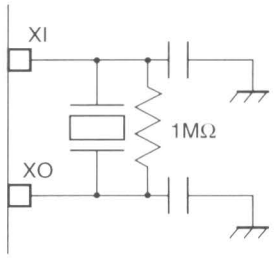
■ BLOCK DIAGRAM



■ FUNCTIONS

1. Clock oscillation XI, XO

Use the XI and XO pins to construct the clock oscillation circuit.
The oscillation frequency is 16.9344MHz.



2. Initial clear /IC

The internal registers and circuits are initialized by making the /IC pin "L" level.
After the power is turned on, initial clear is required.

3. CPU interface /CS, /WR, /RD/ A0, D7~D0

D0 to D7 are an 8-bit parallel data bus for interfacing with a CPU. The /CS, /WR, /RD, and A0 signals control the data bus.
These signals switch the data bus into the following modes:

/CS	/WR	/RD	A0	Function
L	L	H	L	Address write mode
L	L	H	H	Data write mode
L	H	L	L	External memory read mode
L	H	L	H	Status read mode
H	×	×	×	Inactive mode

Note) ×: don't care

(1) Address write mode
This mode specities register address, or external memory address. Output the specified address data on the data bus.

(2) Data write mode
This mode writes data to the address specified by the address write mode described above. Output the set data on the data bus. When accessing the same address, the address does not need to be specified again.

(3) External memory read mode
This mode reads data from the specified external memory address. The data is output on the data bus. The address is automatically incremented.

(4) Status read mode
This mode allows status information to be read. The status information is sent to the data bus.

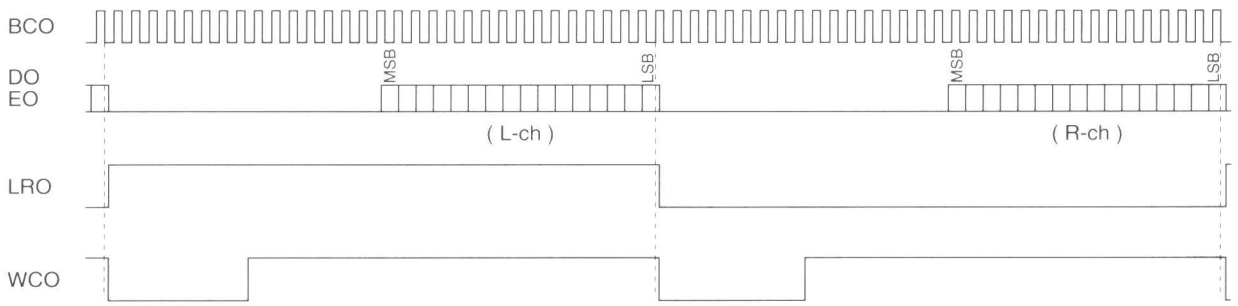
(5) Inactive mode
When the /CS pin is 'H', D0 to D7 become high impedance.

4. External memory interface /MCE, /MOE, /MWR/ MA23~MA0, MD7~MD0

The external memory control signals are output from the /MCE, /MOE, and /MWR pins and the address data is output from the MA23 to MA0 pins. Data is input and output at the MD7 to MD0 pins.
At initial clear, these pins become high impedance. In this case, the external memory is disconnected from the YMZ280B and memory can be accessed through other circuits.

5. Voice data output DO, EO, BCO, WCO, LRO

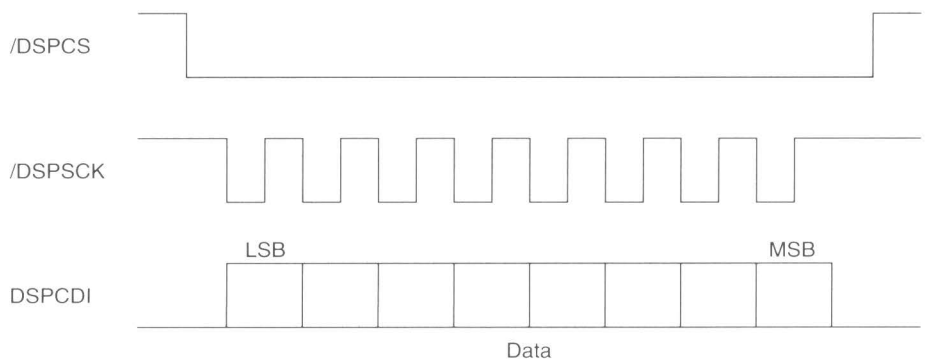
The YMZ280B carries out linear interpolation , total level, and panpot processing on the each channel voice data read from external memory at the specified pitch. The external memory voice data format can be selected from 4-bit ADPCM, 8-bit PCM, and 16-bit PCM. The stereo voice signal is output in 16-bit 2's complement MSB-first format.
The YSS225 (EP) can be connected to the YMZ280B. Two of the eight channels can be selected and output to the DSP.



Voice Data Output Format

6. DSP interface /DSPSCK, /DSPCS, DSPCDI

When DSP data is read to YMZ280B register $82, the serial control signals to the YAMAHA DSP are output from the /DSPSCK, /DSPCS, and DSPCDI pins as shown below.



DSP Interface Format

■ FUNCTION REGISTER

1. Register map

ADDRESS	CH	D7	D6	D5	D4	D3	D2	D1	D0
$00	CH0	Playback pitch							
		FN7	FN6	FN5	FN4	FN3	FN2	FN1	FN0
$01		Key on	Quantization mode		Loop				
		KON	MO1	MO0	LOOP				FN8
$02		Total level							
		TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
$03						Panpot			
						PAN3	PAN2	PAN1	PAN0
$04~07	CH1								
$08~0B	CH2								
$0C~0F	CH3								
$10~13	CH4								
$14~17	CH5								
$18~1B	CH6								
$1C~1F	CH7								
$20	CH0	Start address (H)							
		ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16
$21		Loop start address (H)							
		LS23	LS22	LS21	LS20	LS19	LS18	LS17	LS16
$22		Loop end address (H)							
		LE23	LE22	LE21	LE20	LE19	LE18	LE17	LE16
$23		End address (H)							
		EN23	EN22	EN21	EN20	EN19	EN18	EN17	EN16
$24~27	CH1								
$28~2B	CH2								
$2C~2F	CH3								
$30~33	CH4								
$34~37	CH5								
$38~3B	CH6								
$3C~3F	CH7								

ADDRESS	CH	D7	D6	D5	D4	D3	D2	D1	D0
$40	CH0	Start address (M)							
		ST15	ST14	ST13	ST12	ST11	ST10	ST09	ST08
$41		Loop start address (M)							
		LS15	LS14	LS13	LS12	LS11	LS10	LS09	LS08
$42		Loop end address (M)							
		LE15	LE14	LE13	LE12	LE11	LE10	LE09	LE08
$43		End address (M)							
		EN15	EN14	EN13	EN12	EN11	EN10	EN09	EN08
$44~47	CH1								
$48~4B	CH2								
$4C~4F	CH3								
$50~53	CH4								
$54~57	CH5								
$58~5B	CH6								
$5C~5F	CH7								
$60	CH0	Start address (L)							
		ST07	ST06	ST05	ST04	ST03	ST02	ST01	ST00
$61		Loop start address (L)							
		LS07	LS06	LS05	LS04	LS03	LS02	LS01	LS00
$62		Loop end address (L)							
		LE07	LE06	LE05	LE04	LE03	LE02	LE01	LE00
$63		End address (L)							
		EN07	EN06	EN05	EN04	EN03	EN02	EN01	EN00
$64~67	CH1								
$68~6B	CH2								
$6C~6F	CH3								
$70~73	CH4								
$74~77	CH5								
$78~7B	CH6								
$7C~7F	CH7								

2. Register functions

There is a function register for each channel.

Name	Function
FN8~FN0	Set the playback pitch. Resolution is 512 steps.
KON	Sets key on and key off. '1' = ON '0' = OFF
MO0, M01	Set the voice data quantization mode. MO1 MO0 0 0 = Ignore mode setting and set to same state as KON='0'. 0 1 = 4-bit ADPCM mode 1 0 = 8-bit linear PCM mode 1 1 = 16-bit linear PCM mode
LOOP	Enables loop playback. '0' = Disable '1' = Enable
TL7~TL0	Sets the total level. Resolution is 512 steps.
PAN3~PAN0	Set panpot. Resolution is 16 steps.
ST23~ST00	Set the start address.
LS23~LS00	Set the loop start address.
LE23~LE00	Set the loop end address.
EN23~EN00	Set the end address.

Note) All the register values become '0' by initial clear.
For start address, loop start address, loop end address, and end address, the absolute address of MA23 to MA0 is set by three bytes.
All the registers, except the loop start address during repetitive playback in the 4-bit ADPCM mode, can be rewritten at any time.

■ UTILITY REGISTER

1. Register map

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
$80	Lch enable	Lch - output channel No.			Rch enable	Rch - output channel No.		
	LENB	LCH2	LCH1	LCH0	RENB	RCH2	RCH1	RCH0
$81								DSP enable
								DSPE
$82	DSP data							
	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0
$84	RAM address (H)							
	MA23	MA22	MA21	MA20	MA19	MA18	MA17	MA16
$85	RAM address (M)							
	MA15	MA14	MA13	MA12	MA11	MA10	MA09	MA08
$86	RAM address (L)							
	MA07	MA06	MA05	MA04	MA03	MA02	MA01	MA00
$87	RAM data							
	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0
$E0	IRQ enable/mask							
	ENC7	ENC6	ENC5	ENC4	ENC3	ENC2	ENC1	ENC0
$FF	KON enable	Memory enable		IRQ enable			LSI TEST	
	KENB	MENB		IENB			TST2	TST1

2. Register functions

Name	Function
LCH2~LCH0	Select the channel which is output to DSP voice data output Lch.
RCH2~RCH0	Select the channel which is output to DSP voice data output Rch.
LENB	Enables the DSP voice data output Lch output. '0' = Enable '1' = Disable
RENB	Enables the DSP voice data output Rch output. '0' = Enable '1' = Disable
DSPE	Enables sending of control data to the DSP. '0' = Enable '1' = Disable
DSP7~DSP0	Set the control data to the DSP.
MA23~MA00	Set the external memory write/read address.
MD7~MD0	Set the write data at external memory. When data is set, the write address is incremented by one and the write operation is executed.
ENC7~ENC0	Set IRQ enable/mask for each channel. '0' = Mask '1' = Enable
KENB	Enables key on. '0' = Forcibly key off all channels. '1' = Accept key on of all channels.
IENB	Set /IRQ enable. '0' = Pin 59 becomes [DSPCDI] output. '1' = Pin 59 becomes [/IRQ] output.
MENB	Enables external memory. '0' = Make MA23~MA0, MD7~MD0, /MCE, /MWR, and /MOE pins high impedance. '1' = Normal state.
TST1,2	Used in LSI testing. Normally set to '0'.

Note) All the register values become '0' by initial clear.

■ STATUS REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
FLG7	FLG6	FLG5	FLG4	FLG3	FLG2	FLG1	FLG0

When a playback of the channel for which "1" is assigned to ENC7-ENCO of $FE reaches the end address (/IRQ pin="L" level), the status register (FLG7 is channel 7, and FLG0 is channel 0) for the relevant channel is set to "1". After the status register is read, the /IRQ pin turns to "High impedance" level and the status register set to "1" turns to "0".

■ ELECTRICAL CHARACTERISTICS

1. Absolute maximum ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.5~7.0	V
Input voltage	V_I	−0.5~V_{DD}+0.5	V
Output voltage	V_O	−0.5~V_{DD}+0.5	V
Operating temperature	T_{OP}	0~70	°C
Storage temperature	T_{stg}	−50~125	°C

2. Recommended operating conditions

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{DD}	4.75	5.0	5.25	V
Operating temperature	T_{OP}	0	25	70	°C

3. DC characteristics (Conditions: Ta=0~70°C, V_{DD}=5.0 ±0.25V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_I=0~5.0V, *1	−10		10	μA
Output leakage current	I_{LO}	V_I=0~5.0V, *2	−25		25	μA
Input voltage H level (1)	V_{IHC}	XI	3.5		V_{DD}	V
Input voltage L level (1)	V_{ILC}		−0.3		0.8	V
Input voltage H level (2)	V_{IH}		2.2		V_{DD}	V
Input voltage L level (2)	V_{IL}		−0.3		0.8	V
Output voltage H level	V_{OH}	I_{OH}=−80μA	4.0			V
Output voltage L level	V_{OL}	I_{OL}=4.0mA, *3			0.4	V
Power supply current	I_{DD}				20	mA
Pull-up resistor			30		300	kΩ

Notes) *1: Applied to all input pins, except the V_{DD}, V_{SS}, /TEST, XI, /CS, and /IC pins.

*2: Applied to all output pins.

*3: Applied to all output input/output and output pins.

4. AC characteristics (Conditions: Ta=0~70°C, V_{DD}=5.0 ±0.25V)

4-1 Clock

Item	Symbol	Figure	Min	Typ	Max	Unit
Master clock frequency	f_{MCLK}	Fig. 1	14.3	16.9344	19.2	MHz
Master clock cycle	t_C	Fig. 1	52.1	59.1	69.9	ns
Input clock rise time	t_{RC}	Fig. 1			10.0	ns
Input clock fall time	t_{FC}	Fig. 1			10.0	ns
Input clock duty	D		40	50	60	%

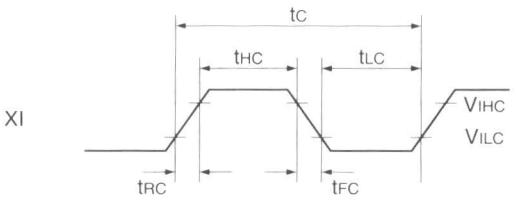


Fig. 1 Input Clock Timing

4-2 Reset

Item	Symbol	Figure	Min	Typ	Max	Unit
Reset pulse width	t_{RP}	Fig. 2	769 t_C			ns

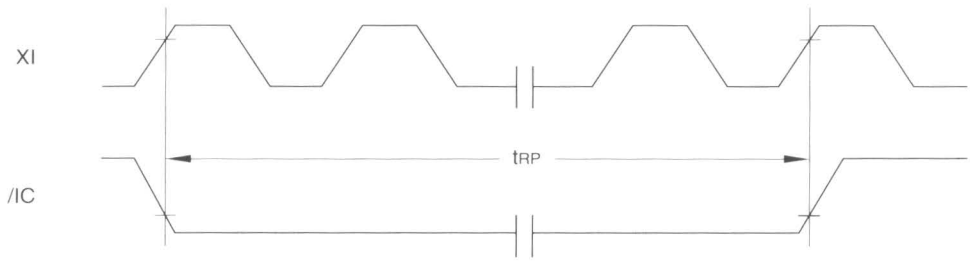


Fig. 2 Reset Timing

4-3 CPU interface

Item	Symbol	Figure	Min	Typ	Max	Unit
Address set-up time	t_{AS}	Fig. 3	10			ns
Address hold time	t_{AH}	Fig. 3	10			ns
Chip select write width	t_{CSW}	Fig. 3	100			ns
Write pulse width	t_{WW}	Fig. 3	100			ns
Write data set-up time	t_{WDS}	Fig. 3	20			ns
Write data hold time	t_{WDH}	Fig. 3	10			ns
Write command set-up time	t_{WCS}	Fig. 3	10			ns
Write command hold time	t_{WCH}	Fig. 3	10			ns
Chip select read width	t_{CSR}	Fig. 4	100			ns
Read pulse width	t_{RW}	Fig. 4	100			ns
Read command set-up time	t_{RCS}	Fig. 4	10			ns
Read command hold time	t_{RCH}	Fig. 4	10			ns
Read data access time	t_{ACC}	Fig. 4			100	ns
Read data hold time	t_{RDH}	Fig. 4	10			ns
Wait time after write	t_{WAW}	Fig. 5, *1	19tc			ns
		Fig. 6, *2	7tc			ns
		Fig. 6, *3	19tc			ns
		Fig. 6, *4	385tc			ns
		Fig. 6, *5	97tc			ns
		Fig. 6, *6	97tc			ns

Notes) Measurement conditions: Pins D0~D7 output capacitance=50 [pF]
Input level V_{IL}=0.4(V), V_{IH}=2.6(V)
Output judgment level V_{OL}=0.8(V), V_{OH}=2.2(V)

*1: Necessary wait time until voice data read after register address and data write.

*2: Necessary wait time up to next write operation after register address written.

*3: Necessary wait time up to next write operation after register data written.

*4: Necessary wait time up to next write operation after data written to register address $01H KON register.

*5: Necessary wait time up to next write operation after register address $82H DSP data register written.

*6: Necessary wait time until data written to register address $81H DSP enable register after register address $82H DSP data register written.

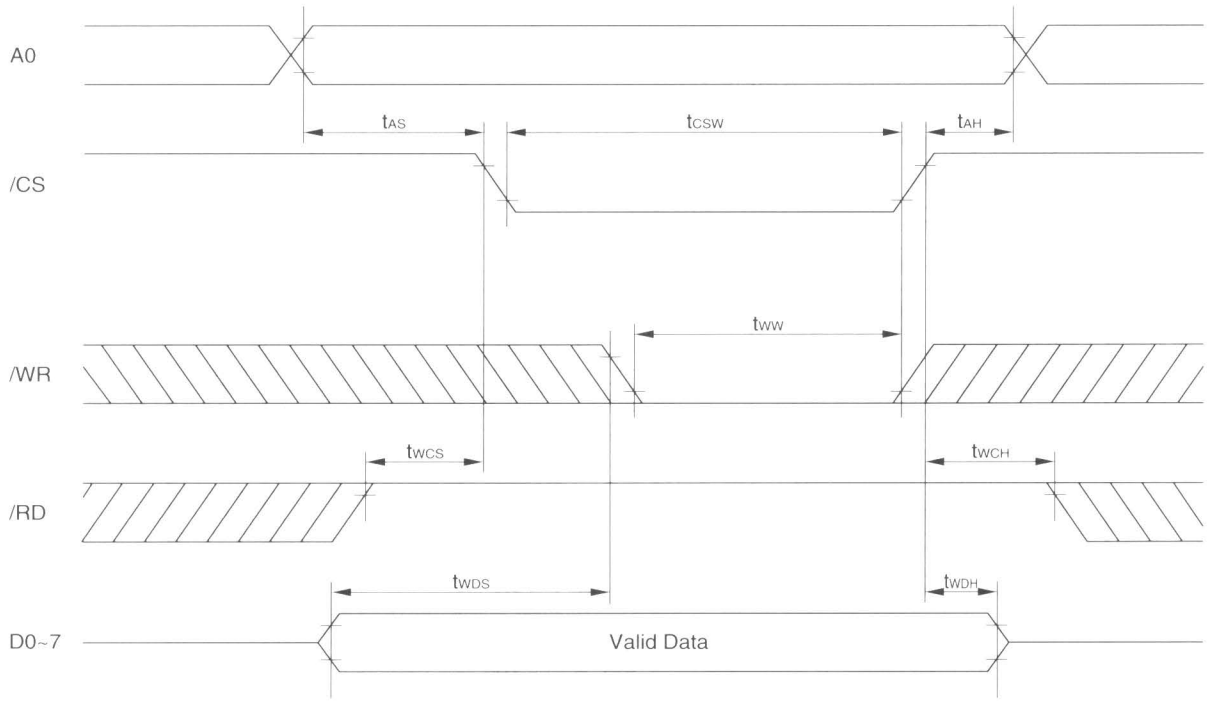


Fig. 3 CPU Interface Timing ①

Note) t_{WDS} is based on the falling-edge timing of /CS or /WR whichever is later.
t_{CSW}, t_{WW}, and t_{WDH} are based on the rising-edge of /CS or /WR whichever is faster.

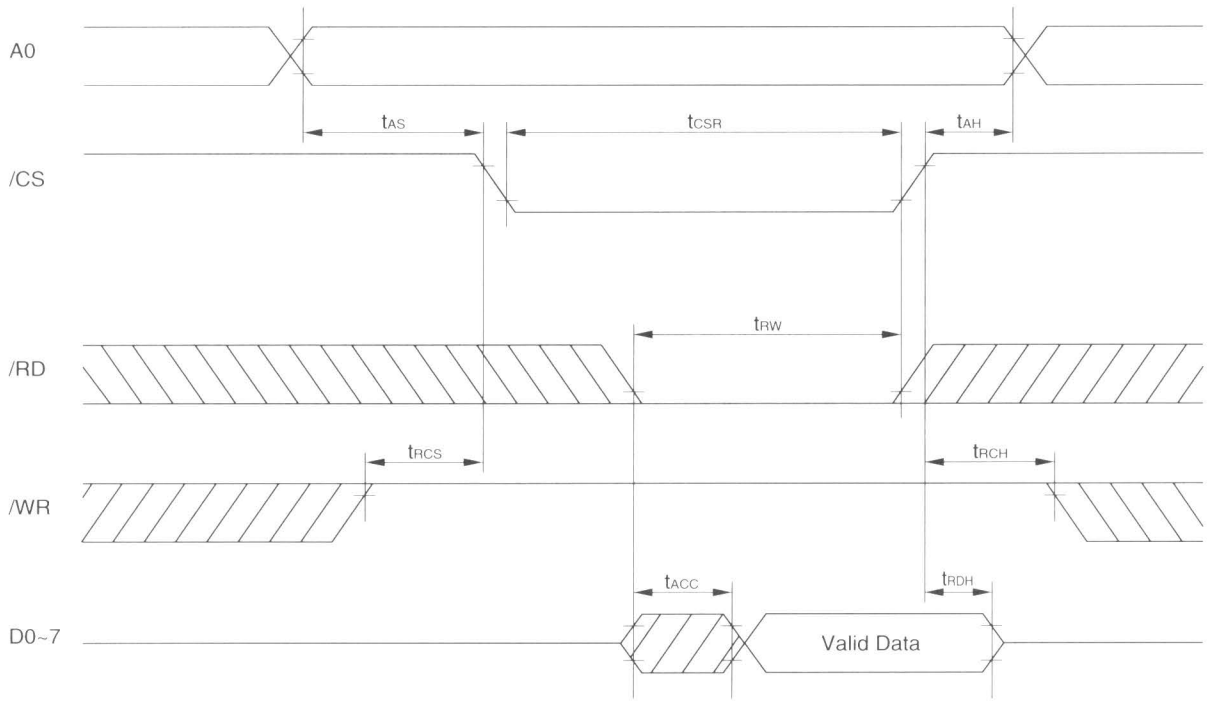


Fig. 4 CPU Interface Timing ②

Note) t_{ACC} is based on the falling-edge timing of /CS or /RD whichever is later.
t_{CSR}, t_{RW}, t_{RCH}, and t_{RDH} are based on the rising-edge of /CS or /RD whichever is faster.

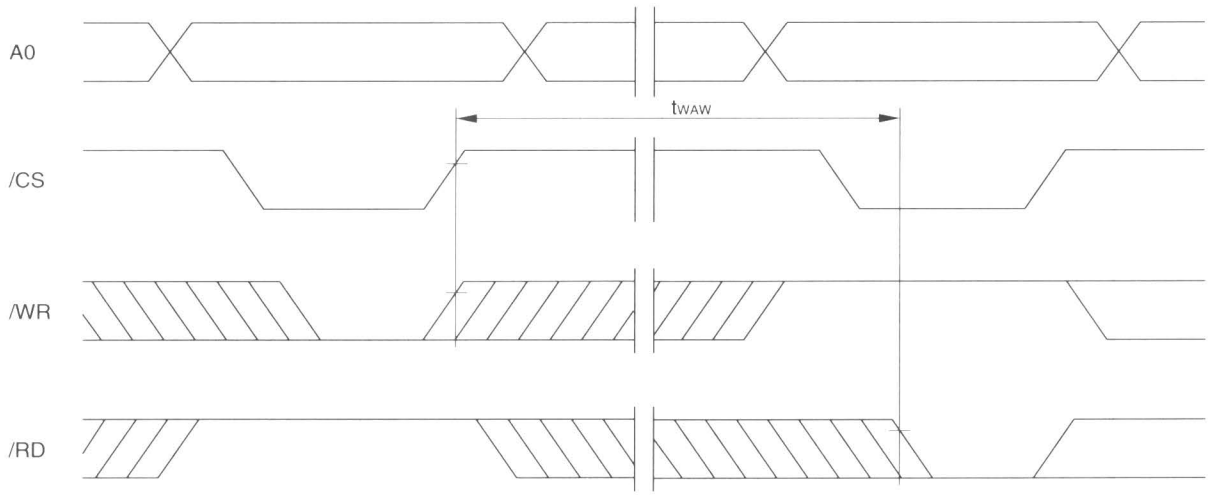


Fig. 5 CPU Interface Timing ③

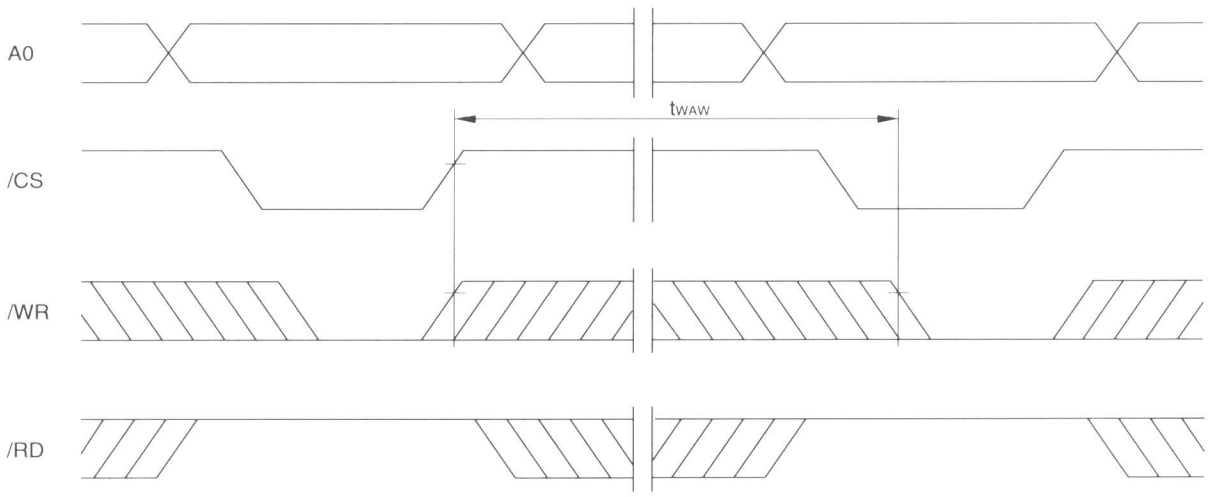


Fig. 6 CPU Interface Timing ④

4-4 External memory write

Item	Symbol	Figure	Min	Typ	Max	Unit
Memory write cycle time	t_{MWC}	Fig. 7		6tc		ns
/MCE pulse width	t_{MWCE}	Fig. 7		5tc		ns
/MCE precharge time	t_{MWP}	Fig. 7		tc		ns
/MOE set-up time	t_{WOSC}	Fig. 7		tc		ns
/MOE hold time	t_{WOHC}	Fig. 7		0tc		ns
Write command hold time	t_{MWCH}	Fig. 7		3tc		ns
Write command read time	t_{MWCR}	Fig. 7		4tc		ns
Memory write pulse width	t_{MW}	Fig. 7		2tc		ns
Memory address set-up time	t_{MAS}	Fig. 7		0.5tc		ns
Memory address hold time	t_{WAH}	Fig. 7		4.5tc		ns
Memory data set-up time	t_{WDSW}	Fig. 7		4tc		ns
	t_{WDSC}	Fig. 7		6tc		ns
Memory data hold time	t_{WDHW}	Fig. 7		2tc		ns
	t_{WDHC}	Fig. 7		0		ns

Note) Measurement conditions: Pins /MCE, /MOE, /MWR, MD0-MD7, MA0~MA23 output load capacitance C_L=50 [pF]
Input level V_{IL}=0.4(V), V_{IH}=2.6(V)
Output judgment level V_{OL}=0.8(V), V_{OH}=2.2(V)

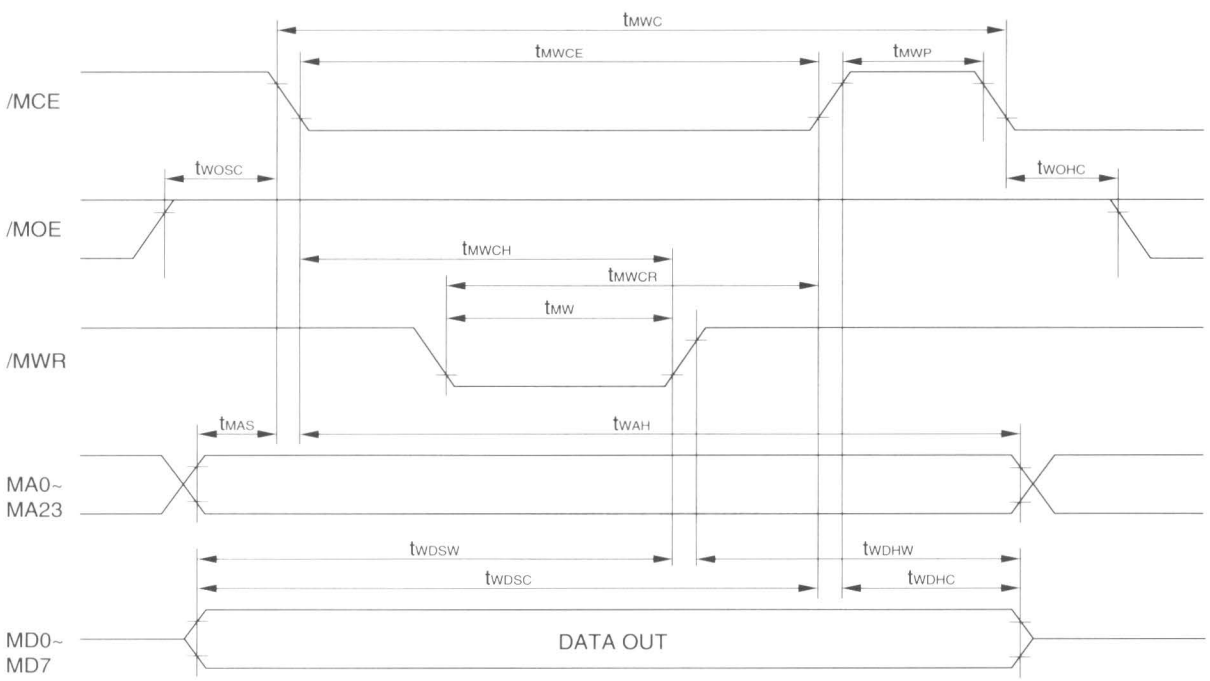


Fig. 7 External Memory Write Timing

4-5 External memory read

Item	Symbol	Figure	Min	Typ	Max	Unit
Memory read cycle time	t_{MRC}	Fig. 8		6tc		ns
/MCE pulse width	t_{MRCE}	Fig. 8		5tc		ns
/MCE precharge time	t_{MRP}	Fig. 8		tc		ns
/MOE pulse width	t_{MOEP}	Fig. 8		5tc		ns
/MOE set-up time	t_{MOEST}	Fig. 8		0		ns
/MOE hold time	t_{MOEHD}	Fig. 8		tc		ns
Read command set-up time	t_{MRCS}	Fig. 8		3tc		ns
Read command hold time	t_{MRCH}	Fig. 8		2tc		ns
Memory address set-up time	t_{MAS}	Fig. 8		0.5tc		ns
Memory address hold time	t_{MAH}	Fig. 8		4.5tc		ns
Memory data set-up time	t_{MDS}	Fig. 8	tc			ns
Memory data hold time	t_{MDH}	Fig. 8	0			ns

Note) Measurement conditions: Pins /MCE, /MOE, /MWR, MD0-MD7, MA0~MA23 output load capacitance C_L=50 [pF]
Input level V_{IL}=0.4(V), V_{IH}=2.6(V)
Output judgment level V_{OL}=0.8(V), V_{OH}=2.2(V)

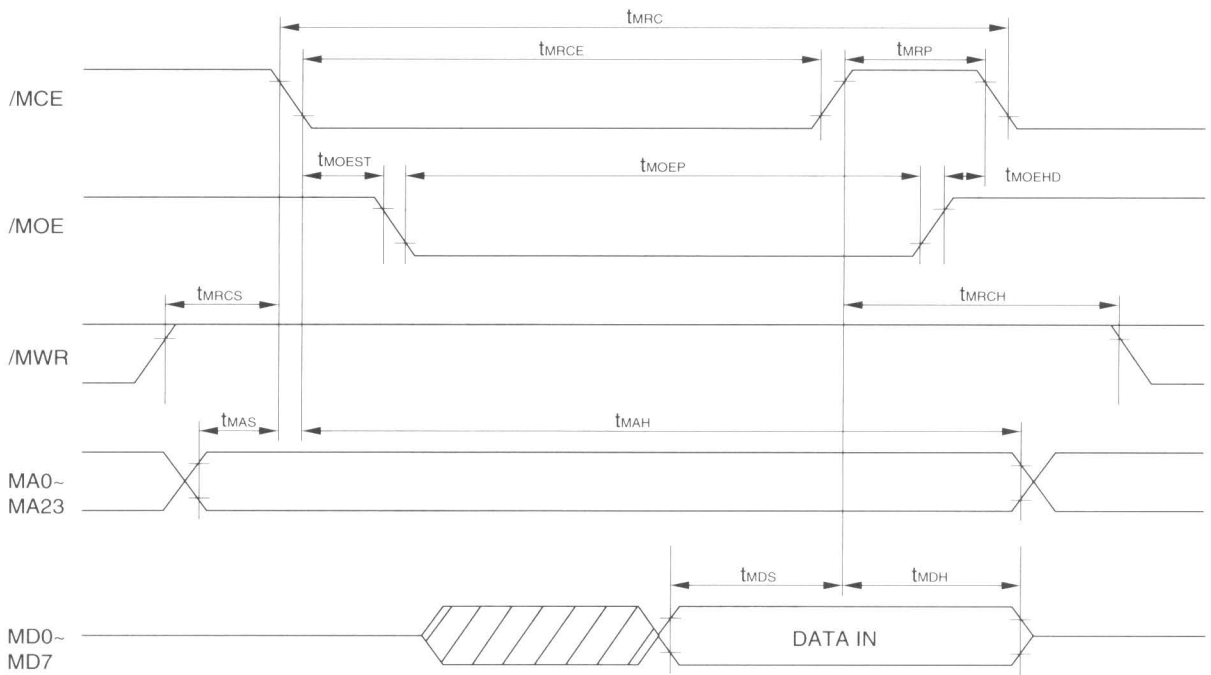


Fig. 8 External Memory Read Timing

4-6 Voice data output

Item	Symbol	Figure	Min	Typ	Max	Unit
BCO frequency	t_{BCO}	Fig. 9		$f_{MCLK}/6$		MHz
LRO frequency	t_{LRO}			$f_{MCLK}/384$		MHz
WCO frequency	t_{WCO}			$f_{MCLK}/192$		MHz
BCO duty	D_{BCO}			50		%
LRO duty	D_{LRO}			50		%
WCO duty	D_{WCO}			62.5		%
DO, EO set-up time	t_{DES}	Fig. 9		2tc		ns
DO, EO hold time	t_{DEH}	Fig. 9		4tc		ns
LRO set-up time	t_{LRS}	Fig. 9		2tc		ns
LRO hold time	t_{LRH}	Fig. 9		4tc		ns
WCO hold time	t_{WCH}	Fig. 9		4tc		ns
Rise time	t_{RD}	Fig. 9			30	ns
Fall time	t_{FD}	Fig. 9			30	ns

Note) Measurement conditions: Pins BCO, WCO, LRO, DO, EO output load capacitance C_{LDA}=50 [pF]
Input level V_{IL}=0.4(V), V_{IH}=2.6(V)
Output judgment level V_{OL}=0.8(V), V_{OH}=2.2(V)

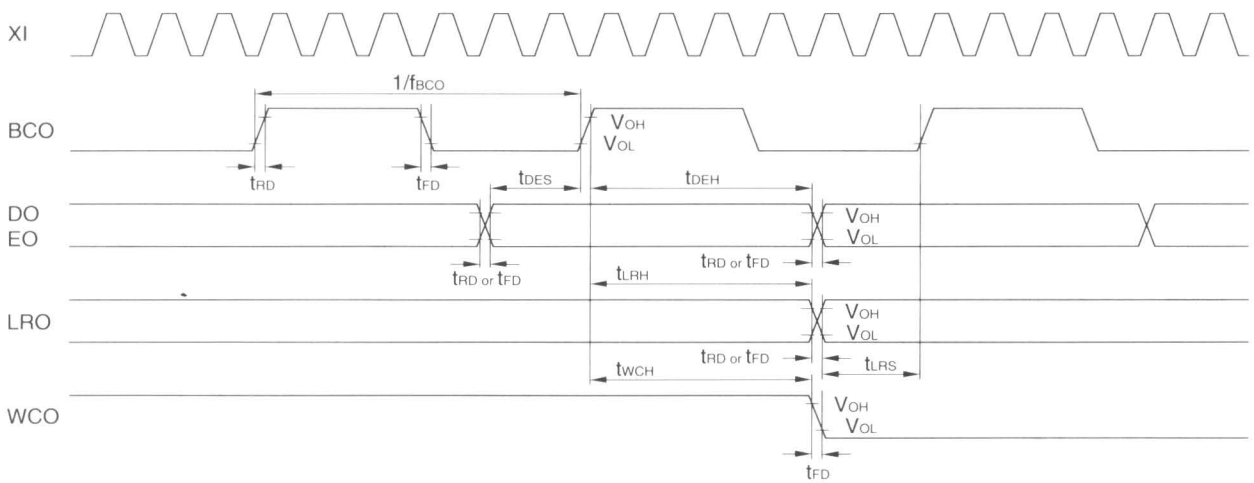


Fig. 9 Voice Data Output Timing

4-7 DSP interface

Item	Symbol	Figure	Min	Typ	Max	Unit
DSPCDI set-up time	t_{DSS}	Fig. 10	12tc			ns
DSPCDI hold time	t_{DSH}	Fig. 10	12tc			ns
DSPCDI output time	t_{DDO}	Fig. 10	192tc			ns
/DSPSCK fall delay time	t_{DCD}	Fig. 10	6tc			ns
/DSPCS rise delay time	t_{DCU}	Fig. 10	6tc			ns

Note) Measurement conditions: Pins DSPCDI, /DSPSCK, /DSPCS output load capacitance C_L=50 [pF]
Input level V_{IL}=0.4(V), V_{IH}=2.6(V)
Output judgment level V_{OL}=0.8(V), V_{OH}=2.2(V)

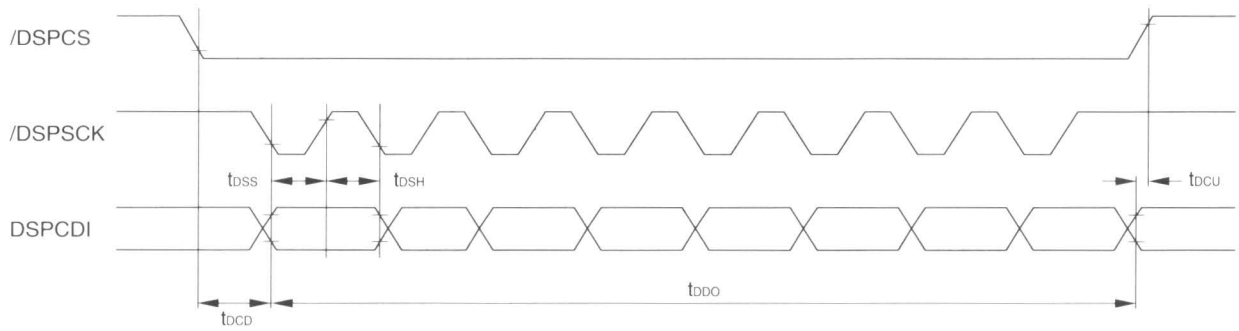
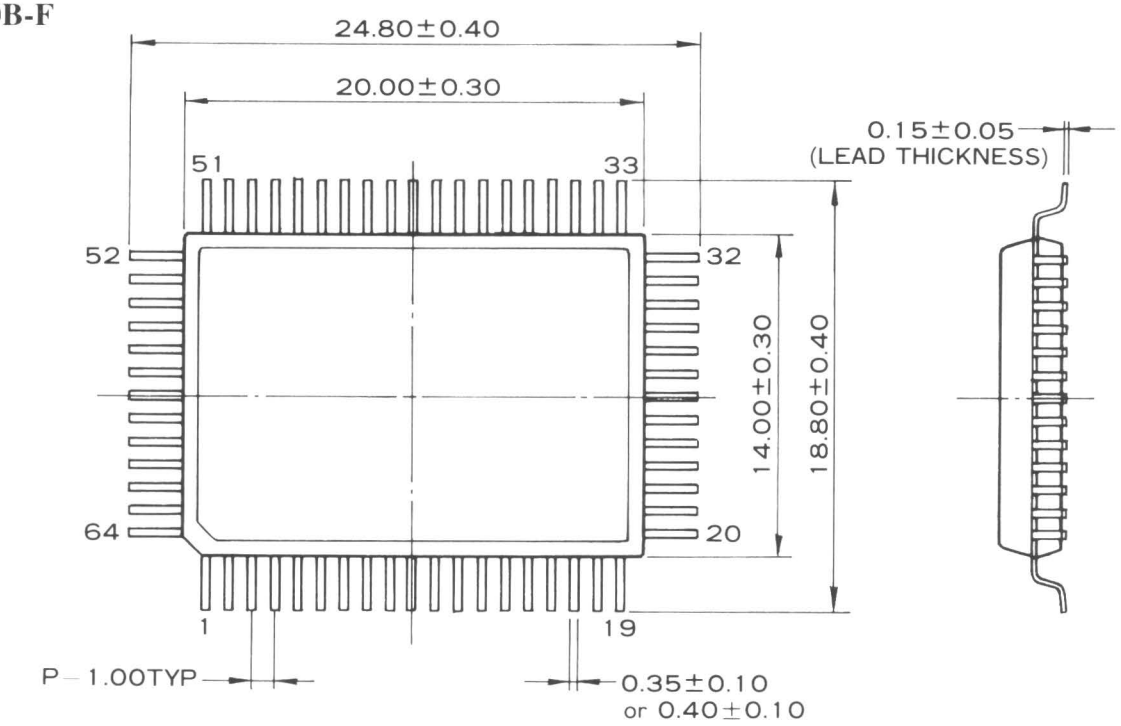
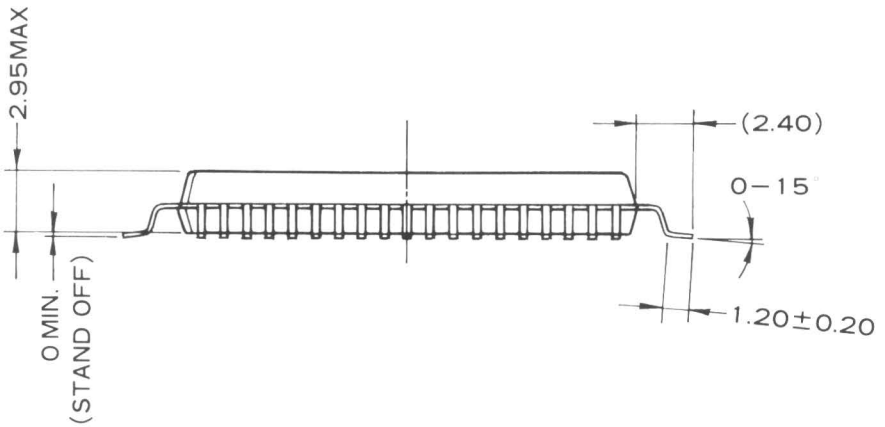


Fig. 10 DSP Interface Timing

■ EXTERNAL DIMENSION

YMZ280B-F





カッコ内の寸法値は参考値とする
モールド外形寸法はバリを含まない
単位(UNIT)：mm

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

Note : The LSIs for surface mount need especial consideration on storage and soldering conditions. For detailed information, please contact your nearest agent of yamaha.

4-7 DSP interface

Item	Symbol	Figure	Min	Typ	Max	Unit
DSPCDI set-up time	t_{DSS}	Fig. 10	12tc			ns
DSPCDI hold time	t_{DSH}	Fig. 10	12tc			ns
DSPCDI output time	t_{DDO}	Fig. 10	192tc			ns
/DSPSCK fall delay time	t_{DCD}	Fig. 10	6tc			ns
/DSPCS rise delay time	t_{DCU}	Fig. 10	6tc			ns

Note) Measurement conditions: Pins DSPCDI, /DSPSCK, /DSPCS output load capacitance C_L=50 [pF]
Input level V_{IL}=0.4(V), V_{IH}=2.6(V)
Output judgment level V_{OL}=0.8(V), V_{OH}=2.2(V)

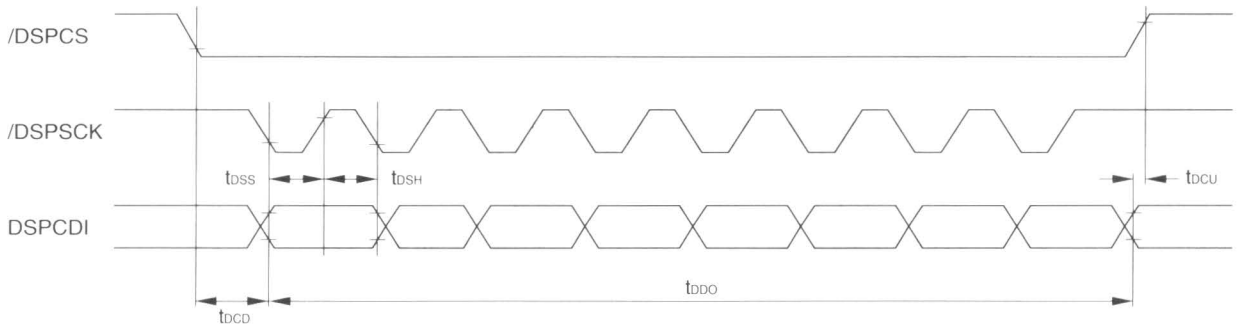


Fig. 10 DSP Interface Timing

■ MEMO

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