FE3031
AT Data Buffer

- ❑ 100 Pin PLCC
- ❑ PC AT* Data Bus Buffers
- ❑ Peripheral Data Bus Buffer
- ❑ Memory Data Bus Buffers
- ❑ Parity Generator/Checker
- ❑ 1.25 Micron CMOS Technology

The FE3031 is an IBM* AT data buffer and parity generator/checker in a 100-pin PLCC package that contains all of the data buffers necessary to implement an AT compatible computer. The FE3031 functions as a peripheral data bus buffer, memory data bus buffer, a parity/generator/checker, and PC/AT data bus buffer.

This document describes the pinouts, signals, timing and electrical specifications of the FE3031 AT Data Buffer IC. The FE3031 is part of the FE3600B AT Core Logic chip set for 16 MHz 80286 based AT computers.

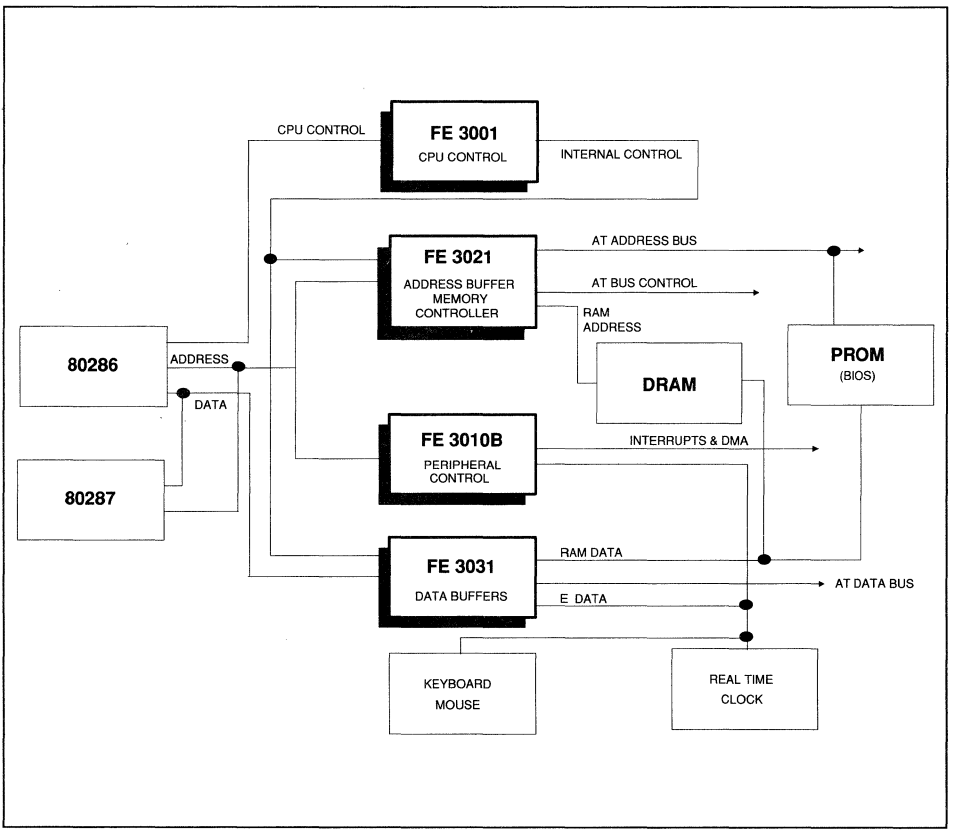


Figure 1. FE3600B Chip Set Functional Block Diagram

Additional References

*IBM * AT Technical Reference Manual*
Intel Microprocessor and Peripheral Handbook*

Disclaimer

Western Digital Corporation makes no representation or warranty of any kind with regard to the hardware and documentation herein described and especially disclaims any implied warranties of merchantability or fitness for any particular purpose. Further, Western Digital Corporation reserves the right to revise this hardware and associated documentation and to make changes from time to time in the content without obligation of Western Digital Corporation to notify any person of such revisions or changes.

Copyright

Western Digital Corporation reserves the right to make changes or improvements to the equipment, software, hardware, and documentation described herein at any time and without notice.

Table of Contents

List of Illustrations

List of Tables

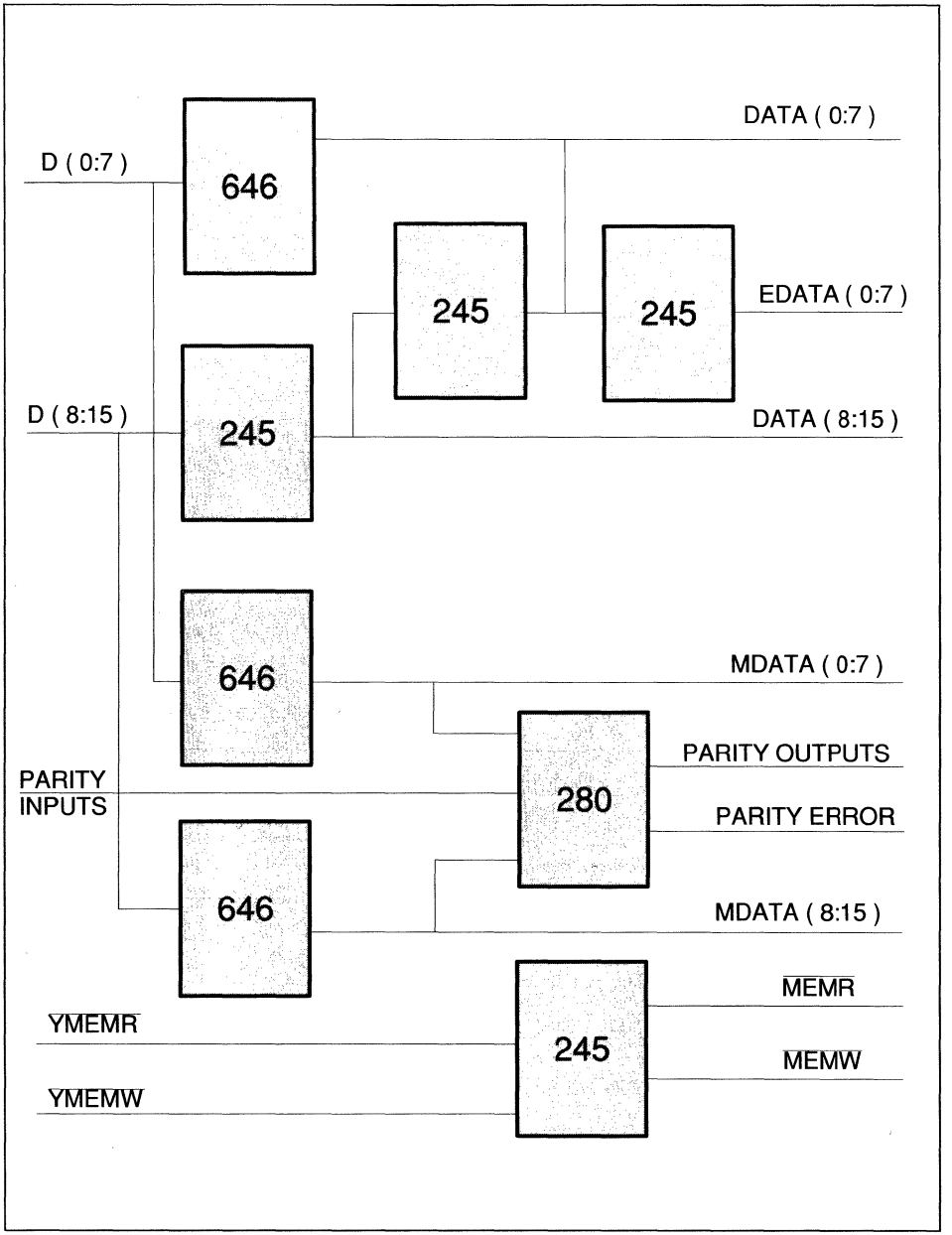


Figure 2. FE3031 Functional Block Diagram

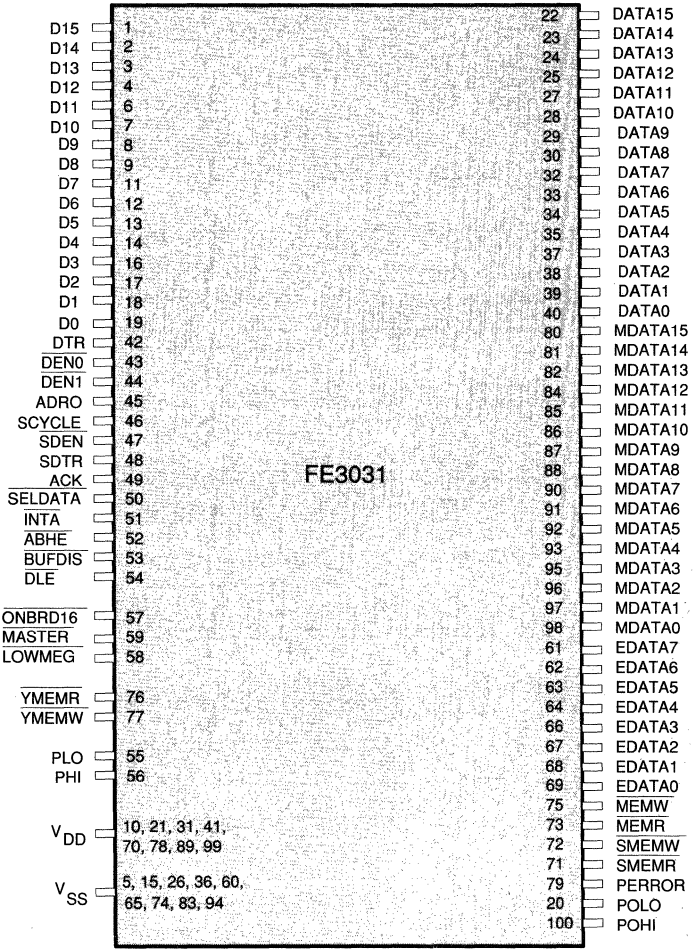


Figure 3. FE3031 Pin Assignments & Locations

1.0 SIGNAL DESCRIPTIONS

PIN#	SIGNAL	TYPE	DESCRIPTION
1-4 6-9 11-14 16-19	D(0:15)	I/O	80286 Local Data Bus
5,15 26,36 60,65 74,83 94	V_{SS}		Ground
10,21 31,41 70,78 89,99	V_{DD}		+5V V_{DD}
20	POLO	O	Low byte parity bit to the DRAMs
22-25 27-30 32-35 37-40	DATA (0:15)	I/O	PC/AT Data Bus
42	DTR	I	Data direction for DATA buffers
43	$\overline{\text{DEN0}}$	I	Low byte data enable to DATA buffers
44	$\overline{\text{DEN1}}$	I	High byte data enable to DATA buffers
45	ADR0	I	Address bit 0 for MDATA buffers and byte swap
46	SCYCLE	I	Latch low byte during byte swap read
47	$\overline{\text{SDEN}}$	I	Byte swap data buffer enable
48	SDTR	I	Byte swap data direction to swap buffer
49	ACK	I	DMA Acknowledge signal to the PC/AT bus
50	$\overline{\text{SELDATA}}$	I	EDATA bus enable
51	$\overline{\text{INTA}}$	I	Interrupt acknowledge
52	$\overline{\text{ABHE}}$	I	High byte enable for MDATA bus
53	$\overline{\text{BUFDIS}}$	I	Disable Buffers when low
54	$\overline{\text{DLE}}$	I	Latch MDATA bus during a read
55	PLO	I	Low byte parity bit from DRAMs
56	PHI	I	High byte parity bit from DRAMs
57	$\overline{\text{ONBRD16}}$	I	$\overline{\text{ONBRD}}$ indicates a local DRAM operation

Table 1. FE3031 Signal Descriptions

PIN	SIGNAL	TYPE	DESCRIPTION
58	LOWMEG	I	LOWMEG indicates access of low MB of memory
59	MASTER	I	Master on PC bus has control of the bus
61-64 66-69	EDATA (0:7)	I/O	Peripheral Data Bus for FE3001, FE3010B, RTC and Keyboard controller
71	SMEMR	O	Low 1 MB Memory Read to PC bus
72	SMEMW	O	Low 1 MB Memory Write to PC bus
73	MEMR	I/O	Memory read to/from AT bus
75	MEMW	I/O	Memory read to/from AT bus
76	YMEMR	I/O	Memory read to/from FE3001
77	YMEMW	I/O	Memory write to/from FE3001
79	PERROR	O	RAM parity error
80-82 84-88 90-93 95-98	MDATA (0:15)	I/O	Memory Data bus
100	POHI	O	High byte parity bit to the DRAMs

Table 1. FE3031 Signal Descriptions (Cont.)

2.0 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature (operating) =	0° to + 70°C
Storage Temperature =	- 40° to +125°C
Voltage on any pin to ground =	+7 V
Power Dissipation =	400 mW

3.0 DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{IL}	Input LOW Voltage		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V	
I_{OL}	LOW V Output Current[1]		4	mA	V_{OL} = 0.4 V
I_{OH}	HIGH V Output Current[1]		-4	mA	V_{OH} = 2.4 V
I_{OL}	LOW V Output Current[2]		6.4	mA	V_{OL} = 0.4 V
I_{OH}	HIGH V Output Current[2]		-6.4	mA	V_{OH} = 2.4 V
V_{DD}	Supply Voltage	4.75	5.25	V	

Notes:

1. Output currents are for D(0:15), EDATA(0:7), YMEMR, YMEMW, PERROR
2. Output currents are for DATA(0:15), MDATA(0:15), MEMR, MEMW, SMEMR, SMEMW, POLO, PHI

4.0 AC CHARACTERISTICS

SIGNAL PATH		PROP DLY (MAX)[1]	UNIT	NOTES
D(0:7) from	DATA (0:7)	22	ns	
	MDATA (0:7)	20	ns	
	ADR0	30	ns	
	$\overline{\text{BUFDIS}}$	30	ns	
	$\overline{\text{ONBRD16}}$	30	ns	1
	$\overline{\text{YMEMR}}$	30	ns	
	$\overline{\text{DEN0}}$	30	ns	
	DATA (8:15)	40	ns	
	EDATA (0:7)	40	ns	
D(8:15) from	DATA (8:15)	22	ns	
	MDATA (8:15)	20	ns	
	$\overline{\text{ABHE}}$	30	ns	
	$\overline{\text{BUFDIS}}$	30	ns	
	$\overline{\text{ONBRD16}}$	30	ns	1
	$\overline{\text{YMEMR}}$	30	ns	
	$\overline{\text{DEN1}}$	30	ns	
	DATA (0:7)	40	ns	
	EDATA (0:7)	40	ns	
DATA (0:7) from	D(0:7)	22	ns	
	D(8:15)	40	ns	
	DATA(8:15)	22	ns	
	EDATA(0:7)	22	ns	1, 2
	$\overline{\text{SDEN}}$	30	ns	
	$\overline{\text{DEN0}}$	30	ns	
	$\overline{\text{INTA}}$	30	ns	
	$\overline{\text{SELDATA}}$	30	ns	
DATA (8:15) from	D (8:15)	22	ns	
	DATA (0:7)	22	ns	1, 2
	$\overline{\text{DEN1}}$	30	ns	
EDATA (0:7) from	DATA(0:7)	36	ns	
	D(0:7)	36	ns	
	D (8:15)	36	ns	1
	$\overline{\text{INTA}}$	40	ns	
	$\overline{\text{SELDATA}}$	40	ns	
$\overline{\text{YMEMW}}$ from	$\overline{\text{MEMW}}$	33	ns	1
	$\overline{\text{MASTER}}$	40	ns	
$\overline{\text{YMEMR}}$ from	$\overline{\text{MEMR}}$	33	ns	1
	$\overline{\text{MASTER}}$	40	ns	

Table 2. AC Characteristics

Notes: 1. Prop delays are for 75pf load.
2. Add 8 ns for 200pf load.

SIGNAL PATH	PROP DLY (MAX) [1]	UNIT	NOTES
$\overline{\text{MEMW}}$ from $\overline{\text{YMEMW}}$	20	ns	
$\overline{\text{MASTER}}$	30	ns	1
$\overline{\text{ONBRD16}}$	30	ns	
$\overline{\text{MEMR}}$ from $\overline{\text{YMEMW}}$	20	ns	
$\overline{\text{MASTER}}$	30	ns	1
$\overline{\text{ONBRD16}}$	30	ns	
$\overline{\text{SMEMW}}$ from $\overline{\text{YMEMW}}$	20	ns	
$\overline{\text{MASTER}}$	30	ns	1
$\overline{\text{ONBRD16}}$	30	ns	
$\overline{\text{SMEMR}}$ from $\overline{\text{YMEMW}}$	20	ns	
$\overline{\text{MASTER}}$	30	ns	1
$\overline{\text{ONBRD16}}$	30	ns	
PERROR from MDATA(0:15)	40	ns	
PLO	40	ns	
PHI	40	ns	1
ADR0	40	ns	
$\overline{\text{ABHE}}$	40	ns	
POLO from D(0:7)	35	ns	1
POHI from D(8:15)	35	ns	1
MDATA (0:7) from D (0:7)	18	ns	
ADR0	30	ns	
$\overline{\text{ONBRD16}}$	30	ns	1
$\overline{\text{YMEMR}}$	30	ns	
$\overline{\text{DLE}}$	30	ns	
MDATA (8:15) from D (8:15)	18	ns	
$\overline{\text{ABHE}}$	30	ns	
$\overline{\text{ONBRD16}}$	30	ns	1
$\overline{\text{YMEMR}}$	30	ns	
$\overline{\text{DLE}}$	30	ns	

Table 2. AC Characteristics (Cont.)

Notes: 1. Prop delays are for 75pf load.
2. Add 8 ns for 200pf load.

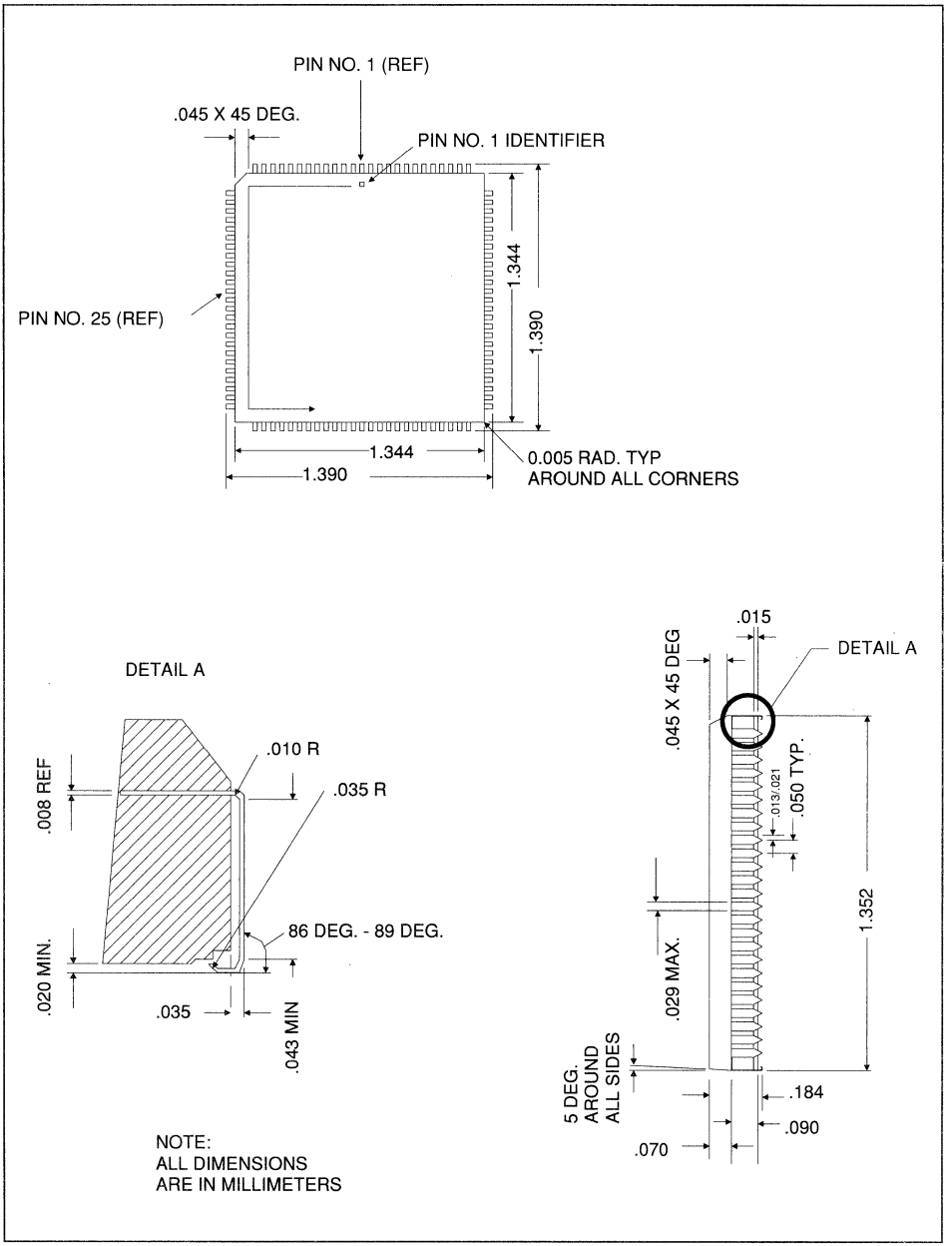


Figure 4. 100-Pin PLCC Packaging Diagram

5.0 PC/AT DATA BUS CYCLES

This description of the data bus cycles of the FE3600B PC AT expansion bus includes CPU, DMA, and MASTER cycles. The data portion of the PC AT expansion bus is a 16-bit wide bus divided into two bytes. In general, the low byte (DATA[0:7]) is accessed during cycles in which the address is even. The high byte (DATA[8:15]) is accessed when the address is odd. During 16-bit operations, both low and high bytes are accessed. There are several combinations of byte wide, word wide, even and odd addressing. Each of these combinations present a unique pattern of bus buffer enables and directions. These data buffer control states are described in this document.

NOTES:

* *Eight bit devices on the PC AT bus are always on the low byte (DATA[0:7]) of the expansion bus regardless of address. Sixteen bit devices use ADR0 and $\overline{EBHE}$ to distinguish between high and low byte transfers.*

* *In previous designs, the data buffers on the PC AT were inactive during DMA. This was due to the on-board DRAM being on the system bus. Now that the DRAM is on the 286 local bus the data buffers must be enabled and directed during DMA operations.*

* *A block diagram of the data bus hardware on the PC AT board is shown in Figure 4. It represents the equivalent 74LSXXX circuitry for the data buffers contained on the board. Signals used in this document are discussed in Table 3.*

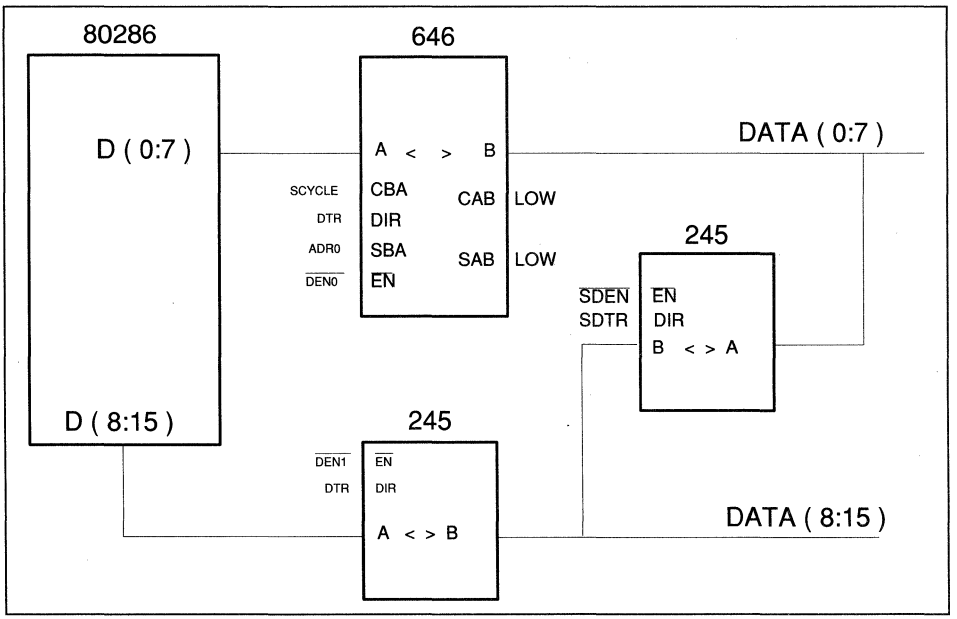


Figure 5. PC/AT Data Bus Architecture

'646				
$\overline{EN}$ $\overline{DEN0}$	DIR DTR	CBA SCYCLE	SBA ADR0	OPERATION
X	X	^	X	LATCH B DATA
0	0	X	0	A <------B (REAL TIME)
0	0	X	1	A <------B (LATCHED DATA)
0	1	X	X	A ------>B (REAL TIME)
1	X	X	X	BUFFERS DISABLED

'245	
DIR	OPERATION
0	A <---------- B
1	A ----------> B

COMMAND SIGNALS	DEFINITIONS
S0, S1	BUS CYCLE STATUS FROM 286
$\overline{MEMR}$	SYSTEM MEMORY READ
$\overline{MEMW}$	SYSTEM MEMORY WRITE
$\overline{IOR}$	SYSTEM I/O READ
$\overline{IOW}$	SYSTEM I/O WRITE
$\overline{NPCS}$	NUMERIC PROCESSOR CHIP SELECT
A0	ADDRESS BIT 0 FROM 286
$\overline{BHE}$	BUS HIGH ENABLE FROM 286
HLDA	HOLD ACKNOWLEDGE FROM 286
HLDA1	DMA HOLD ACKNOWLEDGE FROM DMA CONTROLLER
$\overline{PROMSL}$	BIOS DECODE FROM MEMORY/IO DECODER
$\overline{ONBRD}$	ON BOARD DRAM OR I/O DECODE
$\overline{IOCS16}$	16-BIT I/O DEVICE DECODE FROM EXPANSION BUS
$\overline{MEMCS16}$	16-BIT MEMORY DEVICE DECODE FROM EXPANSION BUS
$\overline{MASTER}$	BUS CONTROL SIGNAL FROM BUS MASTER
CONTROL SIGNALS	**DEFINITIONS**
DTR	DATA TRANSMIT/RECEIVE
$\overline{DEN0}$	LOW BYTE DATA ENABLE
$\overline{DEN1}$	HIGH BYTE DATA ENABLE
$\overline{SDEN}$	BYTE SWAP BUFFER ENABLE
SCYCLE	LOW BYTE DATA LATCH
SDTR	BYTE SWAP BUFFER TRANSMIT/RECEIVE
ADR0	SYSTEM ADDRESS BIT 0

Table 3. Signal Definitions

6.0 CPU CYCLES

The following cycles represent data cycles under CPU control for all devices excluding the on board DRAM and the 80287 Math Coprocessor. Since the 80287 and on-board DRAM are on the local bus, the data bus drivers for the expansion bus will be disabled. This is accomplished by setting $\overline{DEN0}$, $\overline{DEN1}$ and $\overline{SDEN}$ = 1 when $\overline{ONBRD}$ + /MNIO = 0 or $\overline{NPCS}$ = 0. Note that on-board I/O is indicated by $\overline{ONBRD}$ + MNIO = 0. On-board I/O devices are on the system bus.

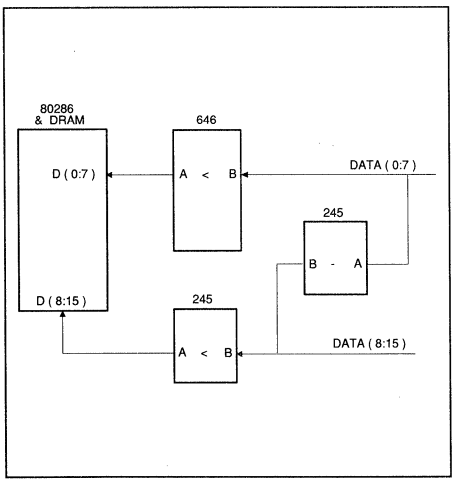
The following cycles are described in this section.

6.1 16-bit transfer, read from 16-bit device
6.2 16-bit transfer, write to 16-bit device
6.3 16-bit transfer, read from 8-bit device
6.4 16-bit transfer, write to 8-bit device
6.5 8-bit transfer, low byte read from 8 or 16-bit device
6.6 8-bit transfer, low byte write to 8 or 16-bit device
6.7 8-bit transfer, high byte read from 8-bit device
6.8 8-bit transfer, high byte write to 8-bit device
6.9 8-bit transfer, high byte read from 16-bit device
6.10 8-bit transfer, high byte write to 16-bit device

For all CPU cycles HLDA=0 and INTA- =1. In the following tables, $\overline{CS16}$ indicates that there is a 16-bit device on the expansion bus. The boolean equation for $\overline{CS16}$ is:

CS16 = $\overline{PROMCS * (IOCS16 + MNIO) * (MEMCS16 + /MNIO)}$

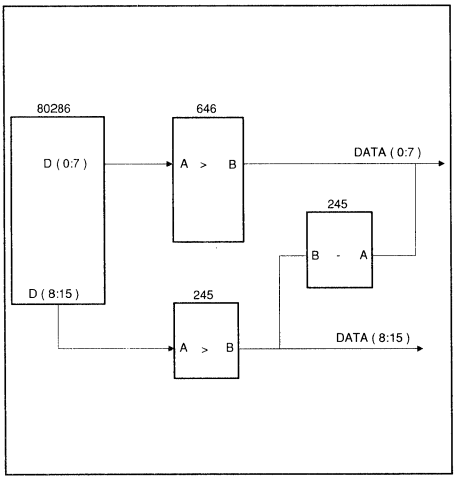
6.1 16-BIT READ FROM 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
$\overline{BHE}$	0
$\overline{CS16}$	0

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADRO	0

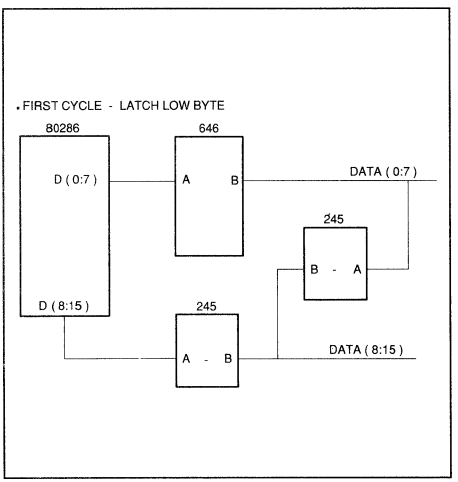
6.2 16-BIT WRITE TO 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	1
S0	0
A0	0
$\overline{BHE}$	0
$\overline{CS16}$	0

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADRO	0

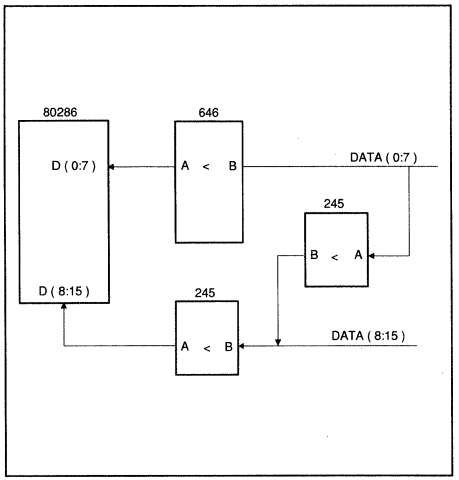
6.3 16-BIT READ FROM 8-BIT DEVICE



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
$\overline{BHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	X
$\overline{DEN0}$	X
$\overline{DEN1}$	X
$\overline{SDEN}$	1
SCYCLE	^
SDTR	X
ADR0	0

* *Second cycle - Enable latched low byte to 286 low byte and enable bus low byte to 286 high byte.*



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
$\overline{BHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	0
SCYCLE	X*
SDTR	1
ADR0	1

* SCYCLE must not change from low to high during the cycle.

6.4 16-BIT WRITE TO 8-BIT DEVICE

INPUT SIGNALS	STATE
S1	1
S0	0
A0	0
$\overline{BHE}$	0
$\overline{CS16}$	1

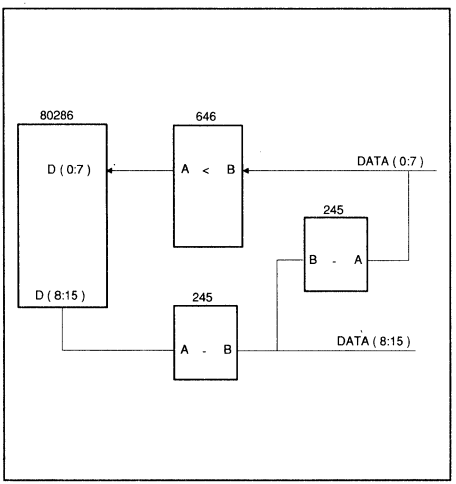
❑ FIRST CYCLE

- 8-bit, low byte write to 8-bit device or 16-bit device
- ADR0 is driven low during this cycle
- $\overline{EBHE}$ is driven high during this cycle

❑ SECOND CYCLE

- 8-bit, high byte write to 8-bit device
- ADR0 is driven high during this cycle
- $\overline{EBHE}$ is driven low during this cycle

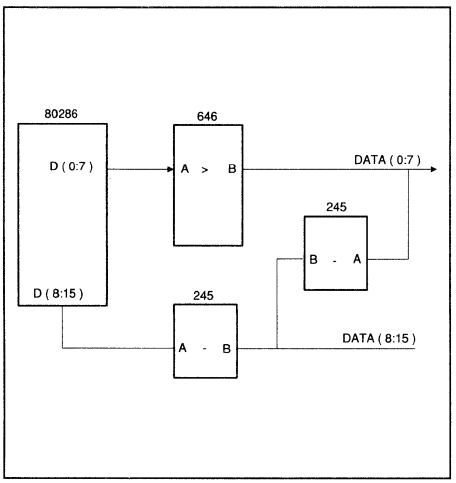
6.5 8-BIT, LOW BYTE READ FROM 8-BIT DEVICE OR 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
$\overline{BHE}$	1
$\overline{CS16}$	X

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	0
$\overline{DEN1}$	1
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADR0	0

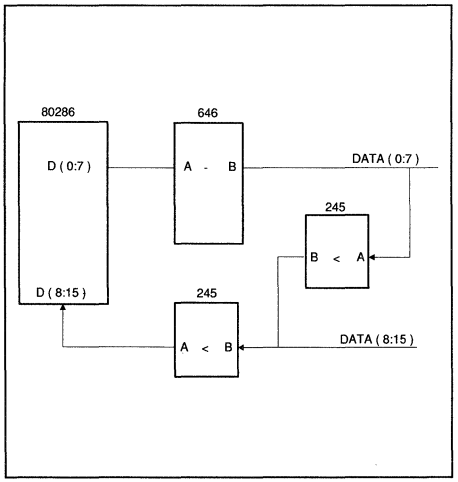
6.6 8-BIT, LOW BYTE WRITE TO 8-BIT DEVICE OR 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	1
A0	0
$\overline{BHE}$	1
$\overline{CS16}$	X

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN1}$	1
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADR0	0

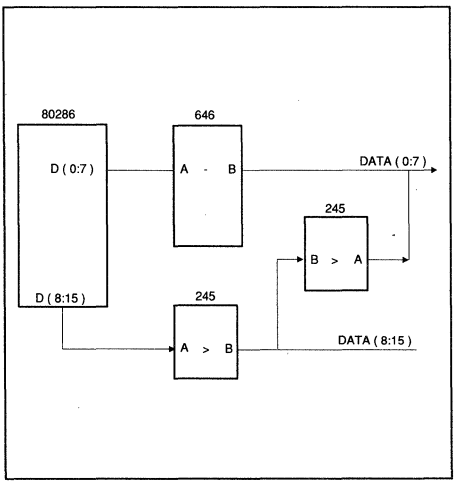
6.7 8-BIT, HIGH BYTE READ FROM 8-BIT DEVICE



INPUT SIGNALS	STATE
S1	0
S0	1
A0	1
$\overline{BHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	0
SCYCLE	X
SDTR	1
ADR0	1

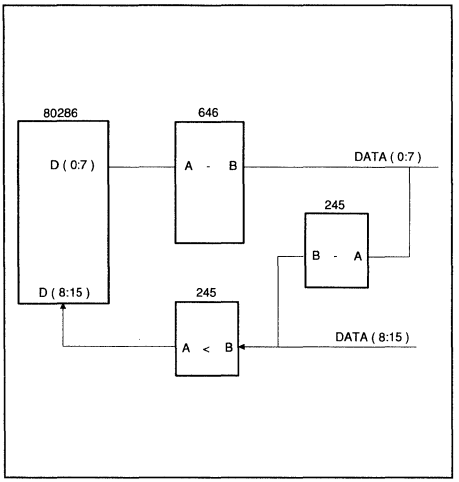
6.8 8-BIT, HIGH BYTE WRITE TO 8-BIT DEVICE



INPUT SIGNALS	STATE
S1	1
S0	0
A0	1
$\overline{BHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	0
SCYCLE	X
SDTR	0
ADR0	1

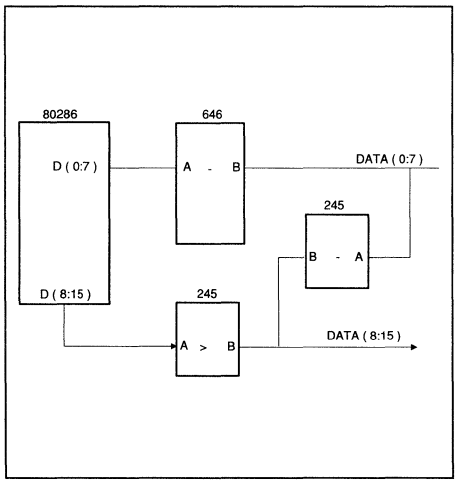
6.9 8-BIT, HIGH BYTE READ FROM 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	0
S0	1
A0	1
$\overline{BHE}$	0
$\overline{CS16}$	0

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADR0	1

6.10 8-BIT, HIGH BYTE WRITE TO 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	1
S0	0
A0	1
$\overline{BHE}$	0
$\overline{CS16}$	0

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADR0	1

7.0 DMA CYCLES

The following cycles represent data cycles under DMA control for all devices. DMA may be for on board DRAM ($\overline{ONBRD}$ =0) or system memory ($\overline{ONBRD}$ =1). Note that $\overline{ONBRD}$ decode for on-board I/O will be disabled during DMA.

The following DMA cycles are described in this section.

- ❑ For on board DRAM ($\overline{ONBRD}$ = 0)

7.1 8-bit DMA from even memory address to 8-bit I/O device.
7.2 8-bit DMA to even memory address from 8-bit I/O device.
7.3 8-bit DMA from odd memory address to 8-bit I/O device.
7.4 8-bit DMA to odd memory address from 8-bit I/O device.
7.5 16-bit DMA from memory to 16-bit I/O.
7.6 16-bit DMA to memory from 16-bit I/O.

- ❑ For system memory ($\overline{ONBRD}$ = 1)

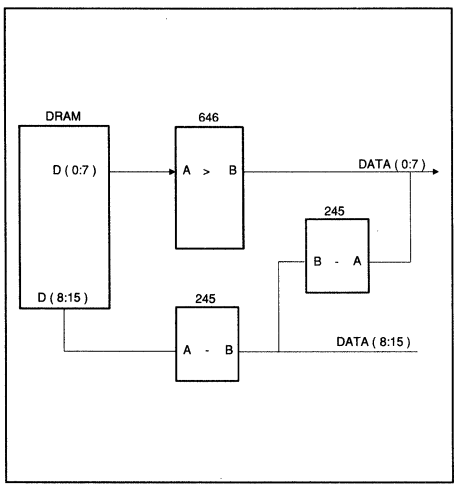
7.7 8-bit DMA from 16-bit memory, odd address to 8-bit I/O device.
7.8 8-bit DMA to 16-bit memory, odd address from 8-bit I/O device.

- ❑ For all other DMA cycles the data buffers are disabled.

7.9 All other DMA cycles.

For all DMA cycles HLDA=1, HLDA1=1 and $\overline{MASTER}$ =1.

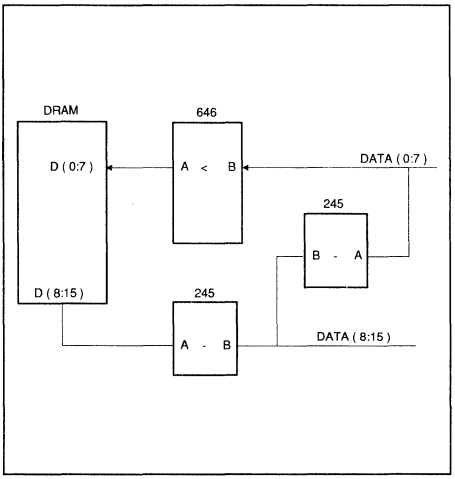
7.1 8-BIT DMA TRANSFER FROM EVEN MEMORY ADDRESS TO 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{DMAMR}$	0
$\overline{MEMW}$	1
$\overline{IOR}$	1
$\overline{IOW}$	0
ADR0	0
$\overline{EBHE}$	1

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	0
$\overline{DEN1}$	1
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X

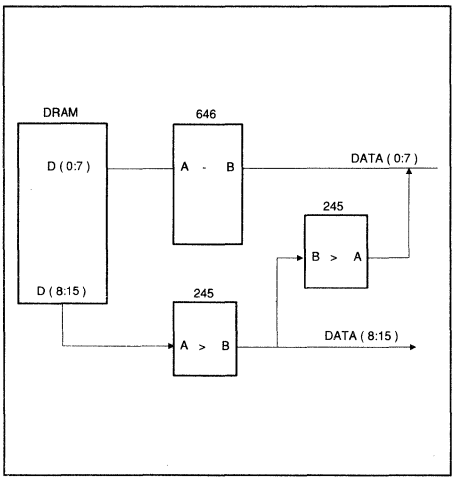
7.2 8-BIT DMA TRANSFER TO EVEN MEMORY ADDRESS FROM 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{\text{DMAMR}}$	1
$\overline{\text{MEMW}}$	0
$\overline{\text{IOR}}$	0
$\overline{\text{IOW}}$	1
ADR0	0
$\overline{\text{EBHE}}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{\text{DEN0}}$	0
$\overline{\text{DEN1}}$	1
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

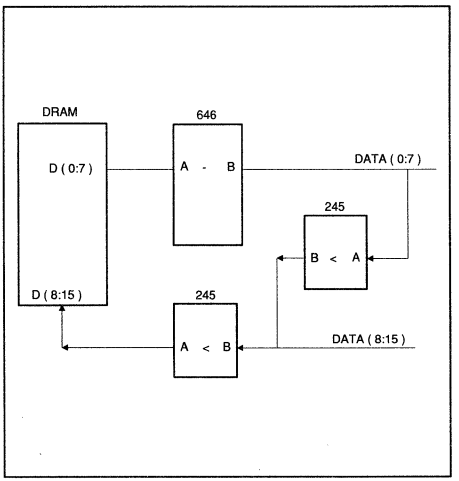
7.3 8-BIT DMA TRANSFER FROM ODD MEMORY ADDRESS TO 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{\text{DMAMR}}$	0
$\overline{\text{MEMW}}$	1
$\overline{\text{IOR}}$	1
$\overline{\text{IOW}}$	0
ADR0	1
$\overline{\text{EBHE}}$	0

CONTROL SIGNALS	STATE
DTR	1
$\overline{\text{DEN0}}$	1
$\overline{\text{DEN1}}$	0
$\overline{\text{SDEN}}$	0
SCYCLE	X
SDTR	0

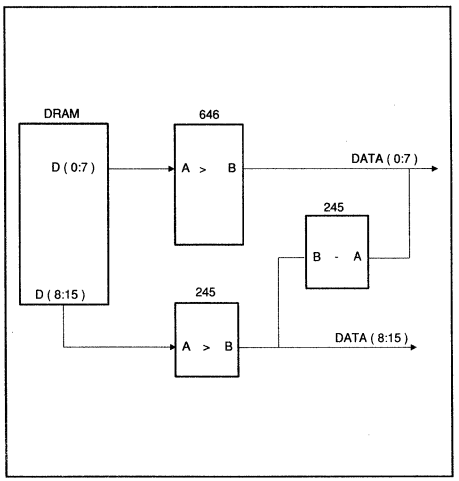
7.4 8-BIT DMA TRANSFER TO ODD MEMORY ADDRESS FROM 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{\text{DMAMR}}$	1
$\overline{\text{MEMW}}$	0
$\overline{\text{IOR}}$	0
$\overline{\text{IOW}}$	1
ADR0	1
$\overline{\text{EBHE}}$	0

CONTROL SIGNALS	STATE
DTR	0
$\overline{\text{DEN0}}$	1
$\overline{\text{DEN1}}$	0
$\overline{\text{SDEN}}$	0
SCYCLE	X
SDTR	1

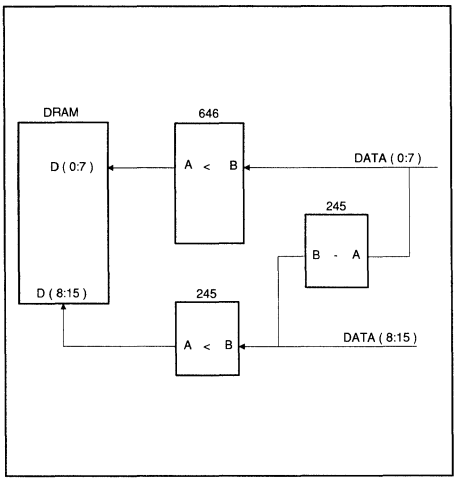
7.5 16-BIT DMA TRANSFER FROM MEMORY TO 16-BIT I/O



INPUT SIGNALS	STATE
$\overline{\text{DMAMR}}$	0
$\overline{\text{MEMW}}$	1
$\overline{\text{IOR}}$	1
$\overline{\text{IOW}}$	0
ADR0	0
$\overline{\text{EBHE}}$	0

CONTROL SIGNALS	STATE
DTR	1
$\overline{\text{DEN0}}$	0
$\overline{\text{DEN1}}$	0
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

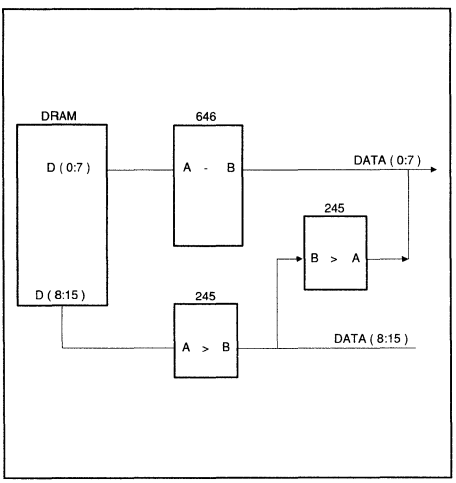
7.6 16-BIT DMA TRANSFER TO MEMORY FROM 16-BIT I/O



INPUT SIGNALS	STATE
$\overline{\text{DMAMR}}$	1
$\overline{\text{MEMW}}$	0
$\overline{\text{IOR}}$	0
$\overline{\text{IOW}}$	1
ADR0	0
$\overline{\text{EBHE}}$	0

CONTROL SIGNALS	STATE
DTR	0
$\overline{\text{DEN0}}$	0
$\overline{\text{DEN1}}$	0
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

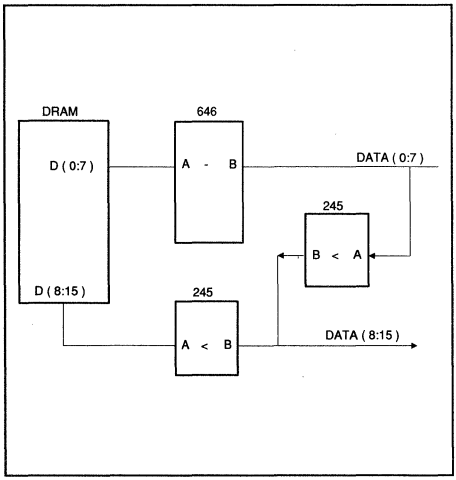
7.7 8-BIT DMA FROM 16-BIT MEMORY, ODD ADDRESS TO 8-BIT I/O DEVICE.



INPUT SIGNALS	STATE
$\overline{\text{DMAMR}}$	0
$\overline{\text{MEMW}}$	1
$\overline{\text{IOR}}$	1
$\overline{\text{IOW}}$	0
ADR0	1
$\overline{\text{EBHE}}$	0
$\overline{\text{MEMCS16}}$ * PROMSL	0

CONTROL SIGNALS	STATE
DTR	X
$\overline{\text{DEN0}}$	1
$\overline{\text{DEN1}}$	1
$\overline{\text{SDEN}}$	0
SCYCLE	X
SDTR	0

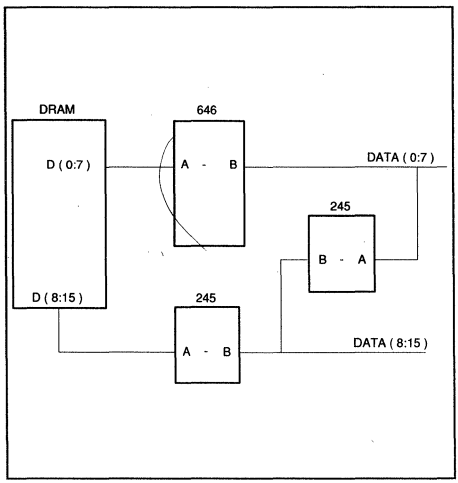
7.8 8-BIT DMA TO 16-BIT MEMORY, ODD ADDRESS FROM 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{\text{DMAMR}}$	1
$\overline{\text{MEMW}}$	0
$\overline{\text{IOR}}$	0
$\overline{\text{IOW}}$	1
ADR0	1
$\overline{\text{EBHE}}$	0
$\overline{\text{MEMCS16}}$ * $\overline{\text{PROMSL}}$	0

CONTROL SIGNALS	STATE
DTR	X
$\overline{\text{DEN0}}$	1
$\overline{\text{DEN1}}$	1
$\overline{\text{SDEN}}$	0
SCYCLE	X
SDTR	1

7.9 ALL OTHER DMA CYCLES (DATA BUFFERS DISABLED)



INPUT SIGNALS	STATE
DMAMR-	
MEMW-	
IOR-	
IOW-	
ADR0	
EBHE-	0

CONTROL SIGNALS	STATE
DTR	X
DEN0-	1
DEN1-	1
SDEN-	1
SCYCLE	X
SDTR	X

8.0 BUS MASTER CYCLES

The following cycles represent data cycles under the control of a bus master other than the 80286 or DMA controller. This condition is indicated by hold acknowledge active (HLDA=1) and bus master asserted ($\overline{\text{MASTER}}$ = 0). It is assumed that the bus master is always a 16-bit device. On-board DRAM and on-board I/O are distinguished by the memory or I/O read/write commands.

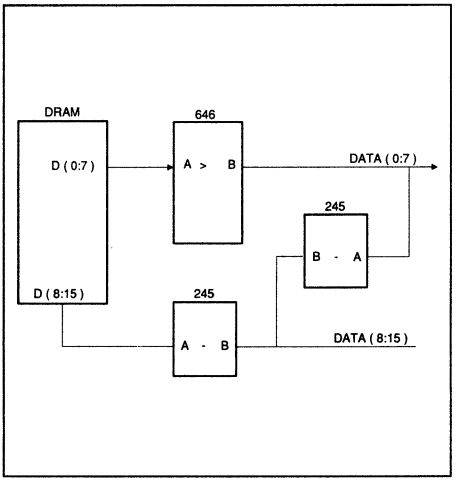
- For on-board DRAM

8.1 8-bit transfer low byte read from memory
8.2 8-bit transfer low byte write to memory
8.3 8-bit transfer high byte read from memory
8.4 8-bit transfer high byte write to memory
8.5 16-bit transfer read from memory
8.6 16-bit transfer write to memory

- For system memory and I/O

8.7 8-bit transfer high byte read from 8-bit system memory or I/O
8.8 8-bit transfer high byte write to 8-bit system memory or I/O

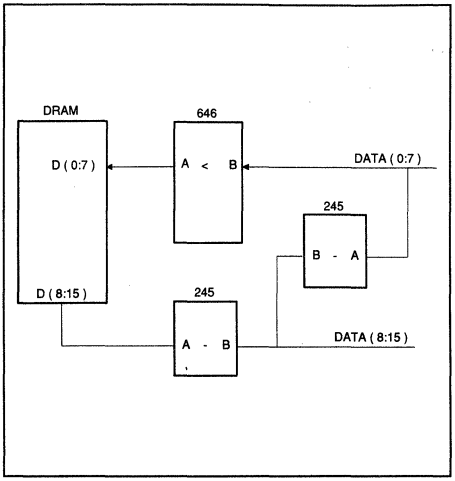
8.1 8- BIT LOW BYTE READ FROM MEMORY



INPUT SIGNALS	STATE
$\overline{\text{MEMR}}$	0
$\overline{\text{MEMW}}$	1
ADR0	0
$\overline{\text{EBHE}}$	1
$\overline{\text{CS16}}$	1

CONTROL SIGNALS	STATE
DTR	1
$\overline{\text{DEN0}}$	0
$\overline{\text{DEN1}}$	1
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

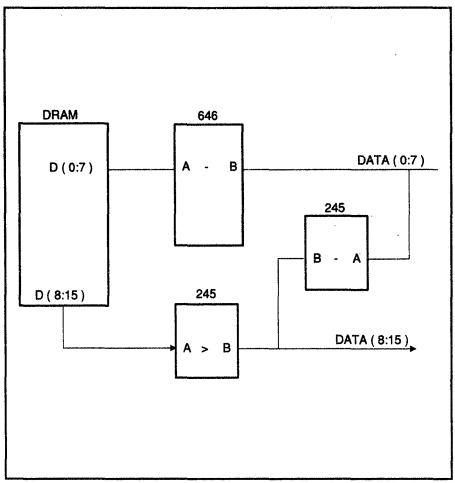
8.2 8-BIT LOW BYTE WRITE TO MEMORY



INPUT SIGNALS	STATE
$\overline{\text{MEMR}}$	1
$\overline{\text{MEMW}}$	0
ADR0	0
$\overline{\text{EBHE}}$	1
$\overline{\text{CS16}}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{\text{DEN0}}$	0
$\overline{\text{DEN1}}$	1
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

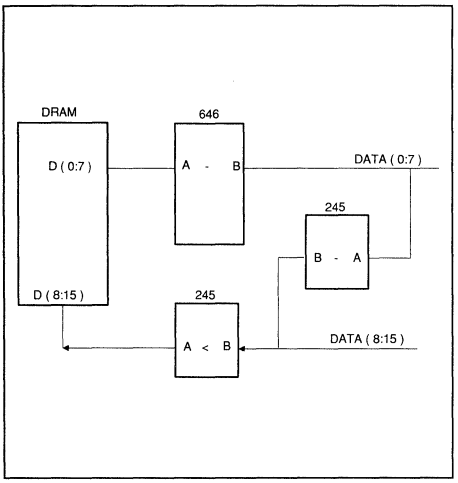
8.3 8-BIT HIGH BYTE READ FROM MEMORY



INPUT SIGNALS	STATE
$\overline{\text{MEMR}}$	0
$\overline{\text{MEMW}}$	1
ADR0	1
$\overline{\text{EBHE}}$	0
$\overline{\text{CS16}}$	1

CONTROL SIGNALS	STATE
DTR	1
$\overline{\text{DEN0}}$	1
$\overline{\text{DEN1}}$	0
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

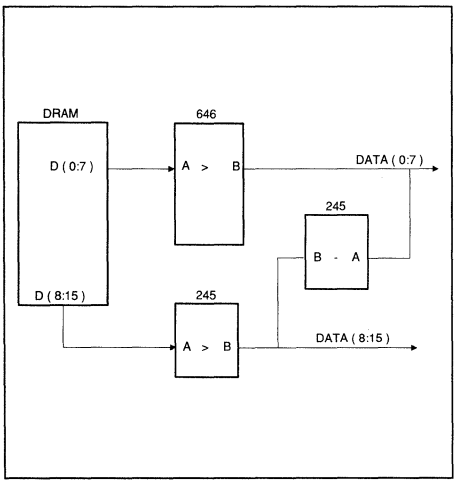
8.4 8-BIT HIGH BYTE WRITE TO MEMORY



INPUT SIGNALS	STATE
$\overline{\text{MEMR}}$	1
$\overline{\text{MEMW}}$	0
ADR0	1
$\overline{\text{EBHE}}$	0
$\overline{\text{CS16}}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{\text{DEN0}}$	1
$\overline{\text{DEN1}}$	0
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

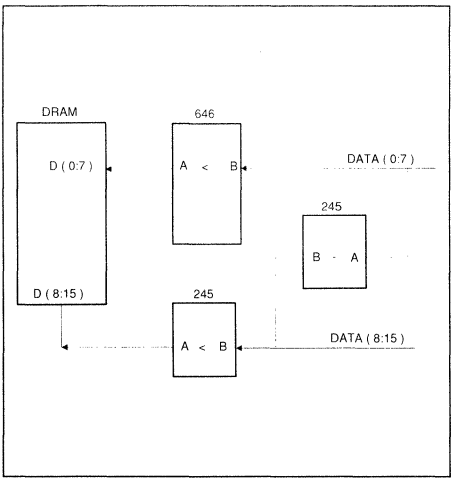
8.5 16-BIT READ FROM MEMORY



INPUT SIGNALS	STATE
$\overline{\text{MEMR}}$	0
$\overline{\text{MEMW}}$	1
ADR0	0
$\overline{\text{EBHE}}$	0
$\overline{\text{CS16}}$	1

CONTROL SIGNALS	STATE
DTR	1
$\overline{\text{DEN0}}$	0
$\overline{\text{DEN1}}$	0
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

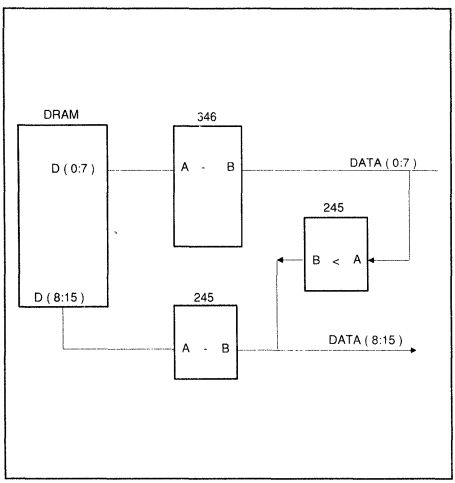
8.6 16-BIT WRITE TO MEMORY



INPUT SIGNALS	STATE
MEMR	1
MEMW	0
ADR0	0
EBHE	0
CS16	1

CONTROL SIGNALS	STATE
DTR	0
DEN0	0
DEN0	0
DEN1	0
SDEN	1
SCYCLE	X
SDTR	X

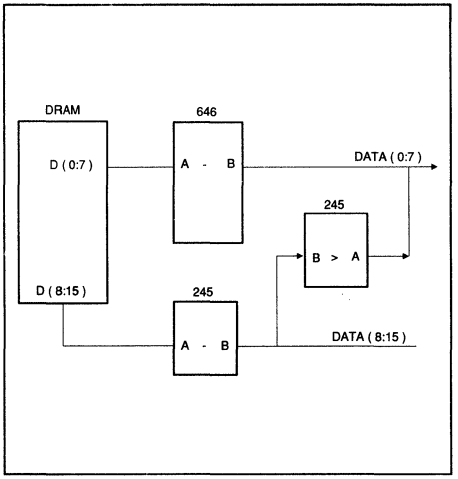
8.7 8-BIT HIGH BYTE READ FROM 8-BIT DEVICE



INPUT SIGNALS	STATE
MEMR * IOR	0
MEMW * IOW	1
ADR0	1
EBHE	0
CS16	1

CONTROL SIGNALS	STATE
DTR	X
DEN0	1
DEN1	1
SDEN	0
SCYCLE	X
SDTR	1

8.8 8-BIT HIGH BYTE WRITE TO 8-BIT DEVICE



INPUT SIGNALS	STATE
$\overline{MEMR}$ * $\overline{IOR}$	1
$\overline{MEMW}$ * $\overline{IOW}$	0
ADR0	1
$\overline{EBHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	X
$\overline{DEN0}$	1
$\overline{DEN1}$	1
$\overline{SDEN}$	0
SCYCLE	X
SDTR	0