VT82C686A
"Super South" South Bridge

PSIPC
PCI Super-I/O Integrated Peripheral Controller

PC98 COMPLIANT PCI-TO-ISA BRIDGE WITH INTEGRATED SUPER-I/O (FDC, LPT, COM1/2, AND IR), INTEGRATED SOUNDBLASTER/DIRECTSOUND AC97 AUDIO, ULTRADMA-33/66 MASTER MODE PCI-EIDE CONTROLLER, USB CONTROLLER, KEYBOARD CONTROLLER, RTC, DISTRIBUTED DMA, SERIAL IRQ, PLUG AND PLAY, ACPI, ENHANCED POWER MANAGEMENT, SMBUS, AND TEMPERATURE, VOLTAGE, AND FAN-SPEED MONITORING

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REVISION HISTORY

Document Release	Date	Revision	Initials
Revision 0.1	2/10/98	Initial release based on 82C596 “Mobile South” Data Sheet revision 0.3	DH
Revision 0.2	3/17/98	Updated features, overview, pins, regs; Added pin list, Sup-IO, HWM, audio	DH
Revision 0.3	4/20/98	Revised pinouts, fixed TC, changed reg defs, added regs in funcs 1, 3, & 4:	DH
Revision 0.4	4/29/98	Corrected TC, features, pin descriptions, f4/game port regs, removed timing	DH
Revision 0.5	5/27/98	Updated feature bullets, pinouts, registers in functions 0-4 and I/O	DH
Revision 0.6	5/29/98	Updated registers in functions 1, 3, and 4	DH
Revision 0.72	12/1/98	Added UltraDMA-66 capability to feature bullets Changed pinouts (primarily SA and USB pins) so changed name to 82C686A Removed PIRQ1, KBLOCK moved SLPBTN#, GPI4, SERIRQ, USBOC0-1# Changed IDE secondary data bus (SDD) multiplexing Moved KBCK, ROMCS#, USBCLK, & USBP0-1 ports to add USB ports 2-3 Added Status/Control I/O registers 14-17 (function 2) for new USB ports 2-3 Changed XOE# to SOE# (function changed as well as the name) Updated pin names & descriptions to match MVP4 design guide Updated register definitions to reflect the above pin changes Removed references to I/O APIC & changed register control bits to reserved Changed Super-I/O configuration RxF6[2] and RxF8[7-4] to reserved Changed FDC registers offset 2 bits 1-0 and offset 4 bits 2-3 (now reserved) Moved Super I/O ena/disa from bit 0 to 1& config ports from 398/9 to 3F0/1 Fixed errors in SMBus offsets D4-5, fixed PCI IRQ routing (f0 Rx55-57), added f0Rx4A[6],76[7], f1Rx71,79, f3Rx42[6], changed PMU Device ID	DH
Revision 0.8	12/7/98	Added Super-I/O config register bits RxF0[2], F6[4] Added Func0-Rx76[7-6] (bit-7 changed), Rx85[0,2-4] Added note to F0-Rx41[0], removed note from Rx4A[7] Func1-fixed Rx50[29], added Rx50[19, 3), added Rx54[3] Split Func 2 into two functions (2 = ports 0-1, 3 = ports 2-3), added Rx41[7] Moved Pwr Mgmt, SMBus, and HW Monitoring regs from func 3 to func 4 Pwr Mgmt Func4 added Rx41[6], 42[7], 54 Pwr Mgmt I/O added Rx4[15], 20[13], 22[13], 24[13], 45[3], removed 40 Moved audio codec registers to function 5	DH
Revision 0.9	12/9/98	Fixed USB (Function 2 and 3) Rx40[1] definition Updated function 5 (audio codec) regs & added function 6 (modem codec) Fix USB Rx41[2] definition reversed	DH
Revision 1.0	1/15/99	Corrected ROMCS# strapping polarity, feature bullet max EPROM support Corrected f0Rx8 Revision ID and f4Rx2 Device ID Fixed miscellaneous typographical errors in pin lists and pin descriptions	DH
Revision 1.1	4/15/99	Fixed typos in pinout diagram (PDD0-15 and RXD2) & fig 7 block diagram Moved pin option MCCS# from U5 to U8 and added SCIOUT# on U5 Removed GPO6 from V10 and added SUSST1# alternate function to GPO3 Added USBOC0-3#, APIC pin descriptions, Gameport/DRQ/DACK alt funcs Fixed HWM voltage sense pin descriptions, updated GPIO descriptions Added DMA ctrlr & timer shadow registers, modified int ctrlr shadow regs Modified ports 70 (CMOS Address RW), E6 (note), F6, F8 (2/4 drive option) Fixed register: f0Rx5C[2],74[7],75[3],77[0],81[3],85[4-2],88-89; f1Rx4[6-9],41[3,0],43[3-0]44[4,2,1], 50[26,18,10,2]; f2-3Rx41[5-7]; f4Rx4C[7-2],4D,50[6,2],54[3-2],90[31-16]; PMU I/O Rx4C; HWM I/O 13-17,27-28,35-38,42[2-1],44[2-1],49[3-0],4B defaults; f5Rx6[14-11,8],8,18,2C, 34; 42[6-5],48[4]; f5IORx2[3-2],22[3-2]; f6Rx6[14-11,8],9-B,41[3-0], 44[5-4]; f6IORx41[5-4],42[3-2],51[5-4], added IOBase2 Rx0-3 Updated electrical specs	DH

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- **Inter-operable with VIA and other Host-to-PCI Bridges**
  - Combine with VT82C598 for a complete Super-7 (66/75/83/100MHz) PCI / AGP / ISA system (Apollo MVP3)
  - Combine with VT82C501 for a complete Super-7 system with integrated 2D / 3D graphics (Apollo MVP4)
  - Combine with VT82C691 for a complete 66 / 100 MHz Socket-8 or Slot-1 PCI / ISA system (Apollo Pro)
  - Inter-operable with Intel or other Host-to-PCI bridges for a complete PC98 compliant PCI / AGP / ISA system
- **PCI to ISA Bridge**
  - Integrated ISA Bus Controller with integrated DMA, timer, and interrupt controller
  - Integrated Keyboard Controller with PS2 mouse support
  - Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
  - Integrated USB Controller with root hub and four function ports
  - Integrated UltraDMA-33/66 master mode EIDE controller with enhanced PCI bus commands
  - PCI-2.2 compliant with delay transaction and remote power management
  - Eight double-word line buffer between PCI and ISA bus
  - One level of PCI to ISA post-write buffer
  - Supports type F DMA transfers
  - Distributed DMA support for ISA legacy DMA across the PCI bus
  - Serial interrupt for docking and non-docking applications
  - Fast reset and Gate A20 operation
  - Edge trigger or level sensitive interrupt
  - Flash EPROM, 4Mb EPROM and combined BIOS support
  - Supports positive and subtractive decoding

- **UltraDMA-33 / 66 Master Mode PCI EIDE Controller**
  - Dual channel master mode PCI supporting four Enhanced IDE devices
  - Transfer rate up to 33MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-33 interface
  - Increased reliability using UltraDMA-66 transfer protocols
  - Thirty-two levels (doublewords) of prefetch and write buffers
  - Dual DMA engine for concurrent dual channel operation
  - Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 compliant
  - Full scatter gather capability
  - Support ATAPI compliant devices including DVD devices
  - Support PCI native and ATA compatibility modes
  - Complete software driver support
- **Integrated Super IO Controller**
  - Supports 2 serial ports, IR port, parallel port, and floppy disk controller functions
  - Two UARTs for Complete Serial Ports
    Programmable character lengths (5,6,7,8)
    Even, odd, stick or no parity bit generation and detection
    Programmable baud rate generator
    High speed baud rate (230Kbps, 460Kbps) support
    Independent transmit/receiver FIFOs
    Modem Control
    Plug and play with 96 base IO address and 12 IRQ options
  - One dedicated IR port
    Third serial port dedicated to IR function
    IR function either through the two complete serial ports or the third dedicated port
    Infrared-IrDA (HPSIR) and ASK (Amplitude Shift Keyed) IR
  - Multi-mode parallel port
    Standard mode, ECP and EPP support
    Plug and play with 192 base IO address, 12 IRQ and 4 DMA options
  - Floppy Disk Controller
    16 bytes of FIFO
    Data rates up to 1Mbps
    Perpendicular recording driver support
    Two FDDs with drive swap support
    Plug and play with 48 base IO address, 12 IRQ and 4 DMA options
- **SoundBlaster Pro Hardware and Direct Sound Ready AC97 Digital Audio Controller**
  - Dual full-duplex Direct Sound channels between system memory and AC97 link
  - PCI master interface with scatter / gather and bursting capability
  - 32 byte FIFO of each direct sound channel
  - Host based sample rate converter and mixer
  - Standard v1.0 or v2.0 AC97 Codec interface for single or cascaded AC97 Codec's from multiple vendors
  - Loopback capability for re-directing mixed audio streams into USB and 1394 speakers
  - Hardware SoundBlaster Pro for Windows DOS box and real-mode DOS legacy compatibility
  - Plug and play with 4 IRQ, 4 DMA, and 4 I/O space options for SoundBlaster Pro and MIDI hardware
  - Hardware assisted FM synthesis for legacy compatibility
  - Direct two game ports and one MIDI port interface
  - Complete software driver support for Windows-95, Windows-98 and Windows-NT

- **Voltage, Temperature, Fan Speed Monitor and Controller**
  - Five positive voltage (one internal), three temperature (one internal) and two fan-speed monitoring
  - Programmable control, status, monitor and alarm for flexible desktop management
  - External thermister or internal bandgap temperature sensing
  - Automatic clock throttling with integrated temperature sensing
  - Internal core VCC voltage sensing
  - Flexible external voltage sensing arrangement (any positive supply and battery)
- **Universal Serial Bus Controller**
  - USB v.1.1 and Intel Universal HCI v.1.1 compatible
  - Eighteen level (doublewords) data FIFO with full scatter and gather capability
  - Root hub and four function ports
  - Integrated physical layer transceivers with optional over-current detection status on USB inputs
  - Legacy keyboard and PS/2 mouse support
- **System Management Bus Interface**
  - Host interface for processor communications
  - Slave interface for external SMBus masters
- **Sophisticated PC98-Compatible Mobile Power Management**
  - Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management
  - ACPI v1.0 Compliant
  - APM v1.2 Compliant
  - CPU clock throttling and clock stop control for complete ACPI C0 to C3 state support
  - PCI bus clock run, Power Management Enable (PME) control, and PCI/CPU clock generator stop control
  - Supports multiple system suspend types: power-on suspends with flexible CPU/PCI bus reset options, suspend to DRAM, and suspend to disk (soft-off), all with hardware automatic wake-up
  - Multiple suspend power plane controls and suspend status indicators
  - One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer
  - Normal, doze, sleep, suspend and conserve modes
  - Global and local device power control
  - System event monitoring with two event classes
  - Primary and secondary interrupt differentiation for individual channels
  - Dedicated input pins for power and sleep buttons, external modem ring indicator, and notebook lid open/close for system wake-up
  - Up to 12 general purpose input ports and 23 output ports
  - Multiple internal and external SMI sources for flexible power management models
  - One programmable chip select and one microcontroller chip select
  - Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
  - Thermal alarm on either external or any combination of three internal temperature sensing circuits
  - Hot docking support
  - I/O pad leakage control
- **Plug and Play Controller**
  - PCI interrupts steerable to any interrupt channel
  - Steerable interrupts for integrated peripheral controllers: USB, floppy, serial, parallel, audio, soundblaster, MIDI
  - Steerable DMA channels for integrated floppy, parallel, and soundblaster pro controllers
  - One additional steerable interrupt channel for on-board plug and play devices
  - Microsoft Windows 98™, Windows NT™, Windows 95™ and plug and play BIOS compliant

- **Built-in NAND-tree pin scan test capability**
- **0.35um, 3.3V, low power CMOS process**
- **Single chip 27x27 mm, 352 pin BGA**

OVERVIEW

The VT82C686A PSIPC (PCI Super-I/O Integrated Peripheral Controller) is a high integration, high performance, power-efficient, and high compatibility device that supports Intel and non-Intel based processor to PCI bus bridge functionality to make a complete Microsoft PC98-compliant PCI/ISA system. In addition to complete ISA extension bus functionality, the VT82C686A includes standard intelligent peripheral controllers:

a) Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT82C686A also supports the UltraDMA-33 standard to allow reliable data transfer rates up to 33MB/sec throughput. The VT82C686A also supports the UltraDMA-66 standard. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-family compliant.

b) Universal Serial Bus controller that is USB v1.1 and Universal HCI v1.1 compliant. The VT82C686A includes the root hub with four function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

c) Keyboard controller with PS2 mouse support.

d) Real Time Clock with 256 byte extended CMOS. In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field, and other enhancements for compatibility with the ACPI standard.

e) Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.

f) Hardware monitoring subsystem for managing system / motherboard voltage levels, temperatures, and fan speeds

g) Full System Management Bus (SMBus) interface.

h) Two 16550-compatible serial I/O ports with infrared communications port option. A third serial port is available to be dedicated to the IR interface.

i) Integrated PCI-mastering dual full-duplex direct-sound AC97-link-compatible sound system. Hardware soundblaster-pro and hardware-assisted FM blocks are included for Windows DOS box and real-mode DOS compatibility. Loopback capability is also implemented for directing mixed audio streams into USB and 1394 speakers for high quality digital audio.

j) Two game ports and one MIDI port

k) ECP/EPP-capable parallel port

l) Standard floppy disk drive interface

m) Distributed DMA capability for support of ISA legacy DMA over the PCI bus. Serial IRQ is also supported for docking and non-docking applications.

n) Plug and Play controller that allows complete steerability of all PCI interrupts and internal interrupts / DMA channels to any interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and reconfigurability of on-board peripherals for Windows family compliance.

The VT82C686A also enhances the functionality of the standard ISA peripherals. The integrated interrupt controller supports both edge and level triggered interrupts channel by channel. The integrated DMA controller supports type F DMA in addition to standard ISA DMA modes. Compliant with the PCI-2.2 specification, the VT82C686A supports delayed transactions and remote power management so that slower ISA peripherals do not block the traffic of the PCI bus. Special circuitry is built in to allow concurrent operation without causing dead lock even in a PCI-to-PCI bridge environment. The chip also includes eight levels (doublewords) of line buffers from the PCI bus to the ISA bus to further enhance overall system performance.

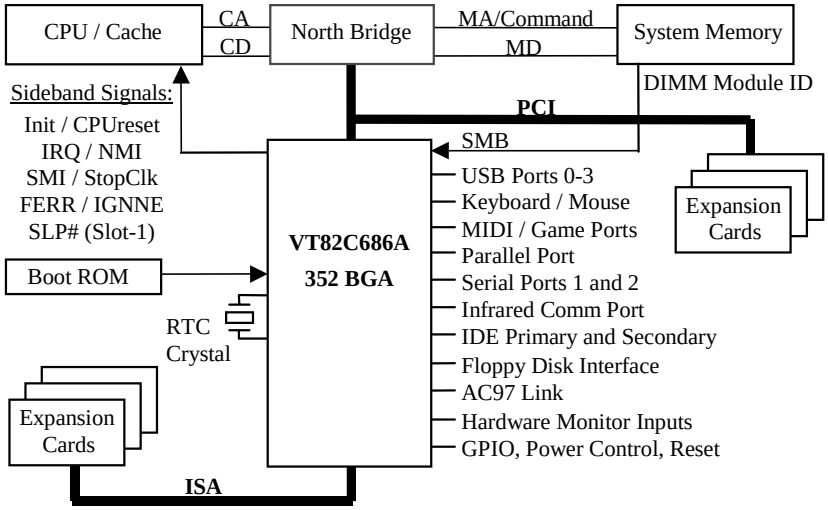

Figure 1. PC System Configuration Using the VT82C686A

PINOUTS

Pin Diagram

Figure 2. VT82C686A Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	SMEMR#	IOCHRDY	USBP0+	USBP2+	KBDT	WRTPRT#	WDATA#	DS1#	CTS2#	DCD2#	TXD1	DCD1#	PD7	PD2	ERR#	PIRQA#	AD31	AD28	AD26	AD25
B	SMEMW#	AEN	USBP0-	USBP2-	USBP3+	RDATA#	WGATE#	DS0#	DTR2#	RXD2	RTS1#	RXD1	ACK#	PD3	PD0	PCIRST#	PIRQD#	AD29	AD27	AD24
C	ROMCS#	IOW#	USBCLK	USBP1+	MSDT	DSKCHG#	HDSEL#	MTR1#	RI2#	DSR2#	CTS1#	DSR1#	BUSY	PD4	PINIT#	AUTOFD#	PIRQC#	AD30	C/BE3#	IDSEL
D	IOR#	DACK3#	DRQ3	USBP1-	MSCK	DRVEN1	INDEX#	DIR#	DRVEN0	TXD2	DTR1#	IRRX	PE	PD5	PD1	STROBE#	PIRQB#	AD23	AD22	AD21
E	DACK1#	DRQ1	RFSH#	OSC	KBCK	USBP3-	TRK00#	STEP#	MTR0#	RTS2#	RI1#	IRTX	SLCT	PD6	SLCTIN#	PCLK	AD20	AD19	AD18	AD17
F	MCS16#	SBHE#	IOCS16#	IOCHK#	IRQ7	**GND**	**VCC**	**GNDU**	**VCCU**	**VCC**	**GND**	**VCC**	**VCC**	**VCC**	**GND**	AD16	C/BE2#	FRM#	IRDY#	TRDY#
G	IRQ6SLPB	IRQ5	IRQ4	IRQ3	DACK2#	**GND**	**G7**	**8**	**9**	**10**	**11**	**12**	**13**	**G14**	**GND**	DEVSEL#	STOP#	SERR#	PAR	CBE1#
H	TC	BALE	DRQ2SIRQ	IRQ9	BCLK	**VCC**	**H**							**H**	**VCC**	AD15	AD14	AD13	AD12	AD11
J	RSTDRV	LA23	LA22	LA21	LA20	**VCC**	**J**		**GND**	**GND**	**GND**	**GND**		**J**	**VCC**	AD10	AD9	AD8	C/BE0#	AD7
K	SA19	SA18	IRQ10	IRQ11	IRQ15	**VCC**	**K**		**GND**	**GND**	**GND**	**GND**		**K**	**VCC**	AD6	AD5	AD4	AD3	AD2
L	IRQ14	DACK0#	DRQ0	DACK5#	SD8	**GND**	**L**		**GND**	**GND**	**GND**	**GND**		**L**	**GND**	AD1	AD0	PREQ#	PGNT#	PDCS1#
M	DRQ5	SD9	DACK6#	SD10	DRQ6	**VCC**	**M**		**GND**	**GND**	**GND**	**GND**		**M**	**VCC**	PDCS3#	PDA0	PDA2	PDA1	PDDACK#
N	SD11	DACK7#	SD12	DRQ7	SD13	**VCC**	**N**							**N**	**VCC**	PDRDY	PDIOR#	PDIOW#	PDDRQ	PDD15
P	SD14	SD15	SA17	SA16	SA15SDD15	**GND**	**P7**	**8**	**9**	**10**	**11**	**12**	**13**	**P14**	**GND**	PDD0	PDD14	PDD1	PDD13	PDD2
R	SA14SDD14	SA13SDD13	SA12SDD12	SA11SDD11	SA10SDD10	**GND**	**VCC**	**VCC**	**VCCS**	**VCCS**	**VCC**	**VCCH**	**GNDH**	**VCC**	**GND**	PDD12	PDD3	PDD11	PDD4	PDD10
T	SA9SDD9	SA8SDD8	SA7SDD7	SA6SDD6	XDIR	INIT	SLP#	GPO0	SMBDATA	SUSCLK	PME#	FAN1	**VREF**	GPIOA	SDD10JAB2	PDD5	PDD9	PDD6	PDD8	PDD7
U	SA5SDD5	SA4SDD4	SA3SDD3	MEMR#	SOE#	SMI#	NMI	GPIOD	SMBCLK	LID#	BATLOW#	FAN2	VSENS1	SDD7JBX	SDD5ACRS	SDD12JBB2	SDCS1#	SDCS3#	SDA0	SDA2
V	SA2SDD2	SA1SDD1	SD5	MEMW#	SPKR	RSMRST#	FERR#	CPURST#	SUSA#	SUST1#	RING#	PCISTP#	VSENS2	GPIOC	SDD9JAX	SDD3SYNC	SDD1SDI	SDA1	SDDACK#	SDRDY
W	SA0SDD0	SD2	SD4	SD7	RTCX2	PWRGD	STPCLK#	INTR	SUSB#	SMBALRT#	GPI1	PCKRUN#	TSENS1	VSENS3	SDD6JBY	SDD11JAB1	SDD13JBB1	SDD0BTCK	SDIOR#	SDIOW#
Y	SD0	SD1	SD3	SD6	RTCX1	**VBAT**	A20M#	IGNNE#	SUSC#	EXTSMI#	PWRBTN#	CPUSTP#	TSENS2	VSENS4	SDD8JAY	SDD4SDO	SDD2SDI2	SDD14MSO	SDD15MSI	SDDRQ

Note: Some of the pins above have alternate functions and alternate names. The table above contains only one name (usually the most often used function), but the pin lists and pin descriptions contain all names.

Pin Lists

Figure 3. VT82C686A Pin List (Numerical Order)

Pin		Pin Name	Pin		Pin Name	Pin		Pin Name	Pin		Pin Name	Pin		Pin Name
A01	O	SMEMR#	D12	IO	IRRX / GPO15	H19	IO	AD12	**N06**	**P**	**VCC**	U13	I	VSENS1 (2.0V)
A02	I	IOCHRDY	D13	I	PE	H20	IO	AD11	**N15**	**P**	**VCC**	U14	IO	SDD07 / JBX
A03	IO	USBP0+	D14	IO	PD5	J01	O	RSTDRV	N16	I	PDRDY	U15	IO	SDD05 / RST
A04	IO	USBP2+	D15	IO	PD1	J02	IO	LA23	N17	O	PDIOR#	U16	IO	SDD12 / JBB2
A05	IO	KBDT / KBRC	D16	IO	STROBE#	J03	IO	LA22	N18	O	PDIOW#	U17	O	SDCS1#
A06	I	WRTPRT#	D17	I	PIRQB#	J04	IO	LA21	N19	I	PDDRQ	U18	O	SDCS3#
A07	OD	WDATA#	D18	IO	AD23	J05	IO	LA20	N20	IO	PDD15	U19	O	SDA0
A08	OD	DS1#	D19	IO	AD22	**J06**	**P**	**VCC**	P01	IO	SD14	U20	O	SDA2
A09	I	CTS2#	D20	IO	AD21	**J09**	**P**	**GND**	P02	IO	SD15	V01	IO	SA02 / SDD2
A10	I	DCD2#	E01	O	DACK1#	**J10**	**P**	**GND**	P03	IO	SA17	V02	IO	SA01 / SDD1
A11	O	TXD1	E02	I	DRQ1	**J11**	**P**	**GND**	P04	IO	SA16	V03	IO	SD05 / KBIN4
A12	I	DCD1#	E03	IO	RFSH#	**J12**	**P**	**GND**	P05	IO	SA15 / SDD15	V04	IO	MEMW#
A13	IO	PD7	E04	I	OSC	**J15**	**P**	**VCC**	**P06**	**P**	**GND**	V05	IO	SPKR
A14	IO	PD2	E05	IO	KBCK/A20GATE	J16	IO	AD10	**P15**	**P**	**GND**	V06	I	RSMRST#
A15	I	ERROR#	E06	IO	USBP3-	J17	IO	AD09	P16	IO	PDD00	V07	I	FERR#
A16	I	PIRQA#	E07	I	TRK00#	J18	IO	AD08	P17	IO	PDD14	V08	OD	CPURST
A17	IO	AD31	E08	OD	STEP#	J19	IO	CBE0#	P18	IO	PDD01	V09	O	SUSA# / GPO1
A18	IO	AD28	E09	OD	MTR0#	J20	IO	AD07	P19	IO	PDD13	V10	O	SUSST1#
A19	IO	AD26	E10	O	RTS2#	K01	IO	SA19	P20	IO	PDD02	V11	I	RING# / GPI7
A20	IO	AD25	E11	I	RI1#	K02	IO	SA18	R01	IO	SA14 / SDD14	V12	O	PCISTP#/GPO5
B01	O	SMEMW#	E12	O	IRTX / GPO14	K03	I	IRO10	R02	IO	SA13 / SDD13	V13	I	VSENS2 (2.5V)
B02	O	AEN	E13	I	SLCT	K04	I	IRQ11	R03	IO	SA12 / SDD12	V14	IO	GPIOC(10)/CHAS
B03	IO	USBP0-	E14	IO	PD6	K05	I	IRQ15	R04	IO	SA11 / SDD11	V15	IO	SDD09 / JAX
B04	IO	USBP2-	E15	IO	SLCTIN#	**K06**	**P**	**VCC**	R05	IO	SA10 / SDD10	V16	IO	SDD03 / SYNC
B05	IO	USBP3+	E16	I	PCLK	**K09**	**P**	**GND**	**R06**	**P**	**GND**	V17	IO	SDD01 / SDI
B06	I	RDATA#	E17	IO	AD20	**K10**	**P**	**GND**	**R07**	**P**	**VCC**	V18	O	SDA1
B07	OD	WGATE#	E18	IO	AD19	**K11**	**P**	**GND**	**R08**	**P**	**VCC**	V19	O	SDDACK#
B08	OD	DS0#	E19	IO	AD18	**K12**	**P**	**GND**	**R09**	**P**	**VCCS**	V20	I	SDRDY
B09	O	DTR2#	E20	IO	AD17	**K15**	**P**	**VCC**	**R10**	**P**	**VCCS**	W01	IO	SA00 / SDD0
B10	I	RXD2	F01	I	MCS16#	K16	IO	AD06	**R11**	**P**	**VCC**	W02	IO	SD02
B11	O	RTS1#	F02	IO	SBHE#	K17	IO	AD05	**R12**	**P**	**VCCH**	W03	IO	SD04 / KBIN3
B12	I	RXD1	F03	I	IOCS16#	K18	IO	AD04	**R13**	**P**	**GNDH**	W04	IO	SD07 / KBIN6
B13	I	ACK#	F04	I	IOCHCK# / GPI0	K19	IO	AD03	**R14**	**P**	**VCC**	W05	O	RTCX2
B14	IO	PD3	F05	I	IRQ7	K20	IO	AD02	**R15**	**P**	**GND**	W06	I	PWRGD
B15	IO	PD0	**F06**	**P**	**GND**	L01	I	IRQ14	R16	IO	PDD12	W07	OD	STPCLK#
B16	O	PCIRST#	**F07**	**P**	**VCC**	L02	O	DACK0#	R17	IO	PDD03	W08	OD	INTR
B17	I	PIRQD#	**F08**	**P**	**GNDU**	L03	I	DRQ0	R18	IO	PDD11	W09	O	SUSB# / GPO2
B18	IO	AD29	**F09**	**P**	**VCCU**	L04	O	DACK5#	R19	IO	PDD04	W10	I	SMBALRT# / GPI6
B19	IO	AD27	**F10**	**P**	**VCC**	L05	IO	SD08	R20	IO	PDD10	W11	I	GPI1 / IRQ8#
B20	IO	AD24	**F11**	**P**	**GND**	**L06**	**P**	**GND**	T01	IO	SA09 / SDD9	W12	IO	PCKRUN#
C01	I	ROMCS#/KBCS#	**F12**	**P**	**VCC**	**L09**	**P**	**GND**	T02	IO	SA08 / SDD8	W13	I	TSENS1
C02	IO	IOW#	**F13**	**P**	**VCC**	**L10**	**P**	**GND**	T03	IO	SA07 / SDD7	W14	I	VSENS3 (5V)
C03	I	USBCLK	**F14**	**P**	**VCC**	**L11**	**P**	**GND**	T04	IO	SA06 / SDD6	W15	IO	SDD06 / JBY
C04	IO	USBP1+	**F15**	**P**	**GND**	**L12**	**P**	**GND**	T05	O	XDIR/GPO12/PCS0#	W16	IO	SDD11 / JAB1
C05	IO	MSDT / IRQ12	F16	IO	AD16	**L15**	**P**	**GND**	T06	OD	INIT	W17	IO	SDD13 / JBB1
C06	I	DSKCHG#	F17	IO	CBE2#	L16	IO	AD01	T07	OD	SLP# / GPO7	W18	IO	SDD00 / BTCK
C07	OD	HDSEL#	F18	IO	FRAME#	L17	IO	AD00	T08	O	GPO0	W19	O	SDIOR#
C08	OD	MTR1#	F19	IO	IRDY#	L18	O	PREQ#	T09	IO	SMBDATA	W20	O	SDIOW#
C09	I	RI2#	F20	IO	TRDY#	L19	I	PGNT#	T10	O	SUSCLK	Y01	IO	SD00
C10	I	DSR2#	G01	I	IRQ6/I4/SLPBTN#	L20	O	PDCS1#	T11	I	PME#/GPI5/THRM	Y02	IO	SD01
C11	I	CTS1#	G02	I	IRQ5	M01	I	DRQ5	T12	I	FAN1	Y03	IO	SD03
C12	I	DSR1#	G03	I	IRQ4	M02	IO	SD09	**T13**	**P**	**VREF**	Y04	IO	SD06 / KBIN5
C13	I	BUSY	G04	I	IRQ3	M03	O	DACK6#	T14	IO	GPIOA(8)/GPOWE#	Y05	I	RTCX1
C14	IO	PD4	G05	O	DACK2#/IOF/OC0#	M04	IO	SD10	T15	IO	SDD10 / JAB2	**Y06**	**P**	**VBAT**
C15	IO	PINIT#	**G06**	**P**	**GND**	M05	I	DRQ6	T16	IO	PDD05	Y07	OD	A20M#
C16	IO	AUTOFD#	**G15**	**P**	**GND**	**M06**	**P**	**VCC**	T17	IO	PDD09	Y08	OD	IGNNE#
C17	I	PIRQC#	G16	IO	DEVSEL#	**M09**	**P**	**GND**	T18	IO	PDD06	Y09	O	SUSC#
C18	IO	AD30	G17	IO	STOP#	**M10**	**P**	**GND**	T19	IO	PDD08	Y10	IOD	EXTSMI#
C19	IO	CBE3#	G18	I	SERR#	**M11**	**P**	**GND**	T20	IO	PDD07	Y11	I	PWRBTN#
C20	I	IDSEL	G19	IO	PAR	**M12**	**P**	**GND**	U01	IO	SA05 / SDD5	Y12	O	CPUSTP#/GPO4
D01	IO	IOR#	G20	IO	CBE1#	**M15**	**P**	**VCC**	U02	IO	SA04 / SDD4	Y13	I	TSENS2
D02	O	DACK3#	H01	O	TC	M16	O	PDCS3#	U03	IO	SA03 / SDD3	Y14	I	VSENS4 (12V)
D03	I	DRQ3	H02	O	BALE	M17	O	PDA0	U04	IO	MEMR#	Y15	IO	SDD08 / JAY
D04	IO	USBP1-	H03	I	DRQ2/IOE/OC1#/SQ	M18	O	PDA2	U05	O	SOE#/O13/SCIOUT#	Y16	IO	SDD04 / SDO
D05	IO	MSCK / IRQ1	H04	I	IRQ9	M19	O	PDA1	U06	OD	SMI#	Y17	IO	SDD02 /SDI2/GPO3
D06	OD	DRVEN1	H05	O	BCLK	M20	O	PDDACK#	U07	OD	NMI	Y18	IO	SDD14 / MSO
D07	I	INDEX#	**H06**	**P**	**VCC**	N01	IO	SD11	U08	IO	GPIOD(11) / MCCS#	Y19	IO	SDD15 / MSI
D08	OD	DIR#	**H15**	**P**	**VCC**	N02	O	DACK7#	U09	IO	SMBCLK	Y20	I	SDDRQ
D09	OD	DRVEN0	H16	IO	AD15	N03	IO	SD12	U10	I	LID / GPI3			
D10	O	TXD2	H17	IO	AD14	N04	I	DRQ7	U11	I	BATLOW#/GPI2			
D11	O	DTR1#	H18	IO	AD13	N05	IO	SD13	U12	IO	FAN2/GPIOB(9)			

Figure 4. VT82C686A Pin List (Alphabetical Order)

Pin		Pin Name	Pin		Pin Name	Pin		Pin Name	Pin		Pin Name	Pin		Pin Name
Y07	OD	A20M#	C12	I	DSR1#	J04	IO	LA21	Y05	I	RTCX1	E15	IO	SLCTIN#
B13	I	ACK#	C10	I	DSR2#	J03	IO	LA22	W05	O	RTCX2	T07	OD	SLP# / GPO7
L17	IO	AD00	D11	O	DTR1#	J02	IO	LA23	B11	O	RTS1#	W10	I	SMBALRT# / GPI6
L16	IO	AD01	B09	O	DTR2#	U10	I	LID / GPI3	E10	O	RTS2#	U09	IO	SMBCLK
K20	IO	AD02	A15	I	ERROR#	F01	I	MCS16#	B12	I	RXD1	T09	IO	SMBDATA
K19	IO	AD03	Y10	IOD	EXTSMI#	U04	IO	MEMR#	B10	I	RXD2	A01	O	SMEMR#
K18	IO	AD04	T12	I	FAN1	V04	IO	MEMW#	W01	IO	SA00 / SDD0	B01	O	SMEMW#
K17	IO	AD05	U12	IO	FAN2/GPIOB(9)	D05	IO	MSCK / IRQ1	V02	IO	SA01 / SDD1	U06	OD	SMI#
K16	IO	AD06	V07	I	FERR#	C05	IO	MSDT / IRQ12	V01	IO	SA02 / SDD2	U05	O	SOE#/O13/SCIOUT#
J20	IO	AD07	F18	IO	FRAME#	E09	OD	MTR0#	U03	IO	SA03 / SDD3	V05	IO	SPKR
J18	IO	AD08	**F06**	**P**	**GND**	C08	OD	MTR1#	U02	IO	SA04 / SDD4	E08	OD	STEP#
J17	IO	AD09	**F11**	**P**	**GND**	U07	OD	NMI	U01	IO	SA05 / SDD5	G17	IO	STOP#
J16	IO	AD10	**F15**	**P**	**GND**	E04	I	OSC	T04	IO	SA06 / SDD6	W07	OD	STPCLK#
H20	IO	AD11	**G06**	**P**	**GND**	G19	IO	PAR	T03	IO	SA07 / SDD7	D16	IO	STROBE#
H19	IO	AD12	**G15**	**P**	**GND**	W12	IO	PCKRUN#	T02	IO	SA08 / SDD8	V09	O	SUSA# / GPO1
H18	IO	AD13	**J09**	**P**	**GND**	E16	I	PCLK	T01	IO	SA09 / SDD9	W09	O	SUSB# / GPO2
H17	IO	AD14	**J10**	**P**	**GND**	B16	O	PCIRST#	R05	IO	SA10 / SDD10	Y09	O	SUSC#
H16	IO	AD15	**J11**	**P**	**GND**	V12	O	PCISTP#/GPO5	R04	IO	SA11 / SDD11	T10	O	SUSCLK
F16	IO	AD16	**J12**	**P**	**GND**	B15	IO	PD0	R03	IO	SA12 / SDD12	V10	O	SUSST1#
E20	IO	AD17	**K09**	**P**	**GND**	D15	IO	PD1	R02	IO	SA13 / SDD13	H01	O	TC
E19	IO	AD18	**K10**	**P**	**GND**	A14	IO	PD2	R01	IO	SA14 / SDD14	F20	IO	TRDY#
E18	IO	AD19	**K11**	**P**	**GND**	B14	IO	PD3	P05	IO	SA15 / SDD15	E07	I	TRK00#
E17	IO	AD20	**K12**	**P**	**GND**	C14	IO	PD4	P04	IO	SA16	W13	I	TSENS1
D20	IO	AD21	**L06**	**P**	**GND**	D14	IO	PD5	P03	IO	SA17	Y13	I	TSENS2
D19	IO	AD22	**L09**	**P**	**GND**	E14	IO	PD6	K02	IO	SA18	A11	O	TXD1
D18	IO	AD23	**L10**	**P**	**GND**	A13	IO	PD7	K01	IO	SA19	D10	O	TXD2
B20	IO	AD24	**L11**	**P**	**GND**	M17	O	PDA0	F02	IO	SBHE#	C03	I	USBCLK
A20	IO	AD25	**L12**	**P**	**GND**	M19	O	PDA1	Y01	IO	SD00	B03	IO	USBP0-
A19	IO	AD26	**L15**	**P**	**GND**	M18	O	PDA2	Y02	IO	SD01	A03	IO	USBP0+
B19	IO	AD27	**M09**	**P**	**GND**	L20	O	PDCS1#	W02	IO	SD02	D04	IO	USBP1-
A18	IO	AD28	**M10**	**P**	**GND**	M16	O	PDCS3#	Y03	IO	SD03	C04	IO	USBP1+
B18	IO	AD29	**M11**	**P**	**GND**	P16	IO	PDD00	W03	IO	SD04 / KBIN3	B04	IO	USBP2-
C18	IO	AD30	**M12**	**P**	**GND**	P18	IO	PDD01	V03	IO	SD05 / KBIN4	A04	IO	USBP2+
A17	IO	AD31	**P06**	**P**	**GND**	P20	IO	PDD02	Y04	IO	SD06 / KBIN5	E06	IO	USBP3-
B02	O	AEN	**P15**	**P**	**GND**	R17	IO	PDD03	W04	IO	SD07 / KBIN6	B05	IO	USBP3+
C16	IO	AUTOFD#	**R06**	**P**	**GND**	R19	IO	PDD04	L05	IO	SD08	**Y06**	**P**	**VBAT**
H02	O	BALE	**R15**	**P**	**GND**	T16	IO	PDD05	M02	IO	SD09	**F07**	**P**	**VCC**
U11	I	BATLOW#/GPI2	**R13**	**P**	**GNDH**	T18	IO	PDD06	M04	IO	SD10	**F10**	**P**	**VCC**
H05	O	BCLK	**F08**	**P**	**GNDU**	T20	IO	PDD07	N01	IO	SD11	**F12**	**P**	**VCC**
C13	I	BUSY	W11	I	GPI1 / IRQ8#	T19	IO	PDD08	N03	IO	SD12	**F13**	**P**	**VCC**
J19	IO	CBE0#	T14	IO	GPIOA(8)/GPOWE#	T17	IO	PDD09	N05	IO	SD13	**F14**	**P**	**VCC**
G20	IO	CBE1#	V14	IO	GPIOC(10)/CHAS	R20	IO	PDD10	P01	IO	SD14	**H06**	**P**	**VCC**
F17	IO	CBE2#	U08	IO	GPIOD(11)/MCCS#	R18	IO	PDD11	P02	IO	SD15	**H15**	**P**	**VCC**
C19	IO	CBE3#	T08	O	GPO0	R16	IO	PDD12	U19	O	SDA0	**J06**	**P**	**VCC**
V08	OD	CPURST	C07	OD	HDSEL#	P19	IO	PDD13	V18	O	SDA1	**J15**	**P**	**VCC**
Y12	O	CPUSTP#/GPO4	C20	I	IDSEL	P17	IO	PDD14	U20	O	SDA2	**K06**	**P**	**VCC**
C11	I	CTS1#	Y08	OD	IGNNE#	N20	IO	PDD15	U17	O	SDCS1#	**K15**	**P**	**VCC**
A09	I	CTS2#	D07	I	INDEX#	M20	O	PDDACK#	U18	O	SDCS3#	**M06**	**P**	**VCC**
L02	O	DACK0#	T06	OD	INIT	N19	I	PDDRQ	W18	IO	SDD00 / BTCK	**M15**	**P**	**VCC**
E01	O	DACK1#	W08	OD	INTR	N17	O	PDIOR#	V17	IO	SDD01 / SDI	**N06**	**P**	**VCC**
G05	O	DK2#/IOF/OC0#	F04	I	IOCHCK# / GPI0	N18	O	PDIOW#	Y17	IO	SDD02 / SDI2/O3	**N15**	**P**	**VCC**
D02	O	DACK3#	A02	I	IOCHRDY	N16	I	PDRDY	V16	IO	SDD03 / SYNC	**R07**	**P**	**VCC**
L04	O	DACK5#	F03	I	IOCS16#	D13	I	PE	Y16	IO	SDD04 / SDO	**R08**	**P**	**VCC**
M03	O	DACK6#	D01	IO	IOR#	L19	I	PGNT#	U15	IO	SDD05 / RST	**R11**	**P**	**VCC**
N02	O	DACK7#	C02	IO	IOW#	C15	IO	PINIT#	W15	IO	SDD06 / JBY	**R14**	**P**	**VCC**
A12	I	DCD1#	F19	IO	IRDY#	A16	I	PIRQA#	U14	IO	SDD07 / JBX	**R12**	**P**	**VCCH**
A10	I	DCD2#	G04	I	IRQ3	D17	I	PIRQB#	Y15	IO	SDD08 / JAY	**R09**	**P**	**VCCS**
G16	IO	DEVSEL#	G03	I	IRQ4	C17	I	PIRQC#	V15	IO	SDD09 / JAX	**R10**	**P**	**VCCS**
D08	OD	DIR#	G02	I	IRQ5	B17	I	PIRQD#	T15	IO	SDD10 / JAB2	**F09**	**P**	**VCCU**
L03	I	DRQ0	G01	I	IRQ6/I4/SLPBTN#	T11	I	PME#/GI5/THRM	W16	IO	SDD11 / JAB1	**T13**	**P**	**VREF**
E02	I	DRQ1	F05	I	IRQ7	L18	O	PREQ#	U16	IO	SDD12 / JBB2	U13	I	VSENS1 (2.0V)
H03	I	D2/IOE/OC1/SQ	H04	I	IRQ9	Y11	I	PWRBTN#	W17	IO	SDD13 / JBB1	V13	I	VSENS2 (2.2V)
D03	I	DRQ3	K03	I	IRQ10	W06	I	PWRGD	Y18	IO	SDD14 / MSO	W14	I	VSENS3 (5V)
M01	I	DRQ5	K04	I	IRQ11	B06	I	RDATA#	Y19	IO	SDD15 / MSI	Y14	I	VSENS4 (12V)
M05	I	DRQ6	L01	I	IRQ14	E03	IO	RFSH#	V19	O	SDDACK#	A07	OD	WDATA#
N04	I	DRQ7	K05	I	IRQ15	E11	I	RI1#	Y20	I	SDDRQ	B07	OD	WGATE#
D09	OD	DRVEN0	D12	IO	IRRX / GPO15	C09	I	RI2#	W19	O	SDIOR#	A06	I	WRTPRT#
D06	OD	DRVEN1	E12	O	IRTX / GPO14	V11	I	RING# / GPI7	W20	O	SDIOW#	T05	O	XDIR/GPO12/PCS0#
B08	OD	DS0#	E05	IO	KBCK / A20GATE	C01	O	ROMCS#/KBCS#	V20	I	SDRDY			
A08	OD	DS1#	A05	IO	KBDT / KBRC	V06	I	RSMRST#	G18	I	SERR#			
C06	I	DSKCHG#	J05	IO	LA20	J01	O	RSTDRV	E13	I	SLCT			

Pin Descriptions

Table 1. Pin Descriptions

PCI Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
AD[31:0]	(see pin list)	IO	**Address/Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
C/BE[3:0]#	C19, F17, G20, J19	IO	**Command/Byte Enable.** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
FRAME#	F18	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	F19	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	F20	IO	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	G17	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.
DEVSEL#	G16	IO	**Device Select.** The VT82C686A asserts this signal to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT82C686A-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
PAR	G19	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.
SERR#	G18	I	**System Error.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT82C686A can be programmed to generate an NMI to the CPU.
IDSEL	C20	I	**Initialization Device Select.** IDSEL is used as a chip select during configuration read and write cycles. Connect this pin to AD18 using a 100 Ω resistor.
PIRQA-D#	A16, D17, C17, B17	I	**PCI Interrupt Request**. These pins are typically connected to the PCI bus INTA#-INTD# pins as follows: PCI Slot 1: PIRQA# INTA#, PIRQB# INTB#, PIRQC# INTC#, PIRQD# INTD# PCI Slot 2: PIRQA# INTB#, PIRQB# INTC#, PIRQC# INTD#, PIRQD# INTA# PCI Slot 3: PIRQA# INTC#, PIRQB# INTD#, PIRQC# INTA#, PIRQD# INTB# PCI Slot 4: PIRQA# INTD#, PIRQB# INTA#, PIRQC# INTB#, PIRQD# INTC#
PREQ#	L18	O	**PCI Request.** This signal goes to the North Bridge to request the PCI bus.
PGNT#	L19	I	**PCI Grant.** This signal is driven by the North Bridge to grant PCI access to the VT82C686A.
PCLK	E16	I	**PCI Clock.** PCLK provides timing for all transactions on the PCI Bus.
PCKRUN#	W12	IO	**PCI Bus Clock Run.** This signal indicates whether the PCI clock is or will be stopped (high) or running (low). The VT82C686A drives this signal low when the PCI clock is running (default on reset) and releases it when it stops the PCI clock. External devices may assert this signal low to request that the PCI clock be restarted or prevent it from stopping. Connect this pin to ground using a 100 Ω resistor if the function is not used. Refer to the "PCI Mobile Design Guide" and the VIA "Apollo MVP4 Design Guide" for more details.

CPU Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
CPURST	V8	OD	**CPU Reset.** The VT82C686A asserts CPURST to reset the CPU during power-up.
INTR	W8	OD	**CPU Interrupt.** INTR is driven by the VT82C686A to signal the CPU that an interrupt request is pending and needs service.
NMI	U7	OD	**Non-Maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU. The VT82C686A generates an NMI when either SERR# or IOCHK# is asserted.
INIT	T6	OD	**Initialization.** The VT82C686A asserts INIT if it detects a shut-down special cycle on the PCI bus or if a soft reset is initiated by the register
STPCLK#	W7	OD	**Stop Clock.** STPCLK# is asserted by the VT82C686A to the CPU to throttle the processor clock.
SMI#	U6	OD	**System Management Interrupt.** SMI# is asserted by the VT82C686A to the CPU in response to different Power-Management events.
FERR#	V7	I	**Numerical Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active.
IGNNE#	Y8	OD	**Ignore Numeric Error.** This pin is connected to the "ignore error" pin on the CPU.
SLP# / GPO7	T7	OD	**Sleep** (Rx75[7] = 0). Used to put the CPU to sleep. Used with slot-1 CPUs only. Not currently used with socket-7 CPUs.
A20M#	Y7	OD	**A20 Mask.** Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit-1 (Fast_A20).

Note: Connect each of the above signals to 4.7K Ω pullup resistors to VCC3.

Advanced Programmable Interrupt Controller (APIC) Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
APICREQ# / GPI3 / LID	U10	I / I / I	**APIC Request.** Rx74[7] = 1. Asserted by external APIC synchronous to PCLK prior to sending an interrupt over the APIC serial bus. This signals the VT82C686A to flush its internal buffers.
APICACK# / GPO1 / SUSA#	V9	O / O / O	**APIC Acknowledge.** Rx74[7] = 1. Asserted by the VT82C686A to indicate that its internal buffers have been flushed (in response to APICREQ#). This indicates to the external APIC that the VT82C686A's internal buffers have been flushed and that it is OK for the APIC to send its interrupt.
APICCS# / GPO2 / SUSB#	W9	O / O / O	**APIC Chip Select.** Rx74[7] = 1. The VT82C686A drives this signal active to select an external APIC (if used). This occurs if the external APIC is enabled and a PCI cycle is detected within the programmed APIC address range.
SCIOUT# / GPO13 / SOE#	U5	O / O / O	**SCI Out.** Used to route the internally generated SCI and SMBus interrupts out of the South Bridge for connection to an external APIC (if used).

Universal Serial Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
USBP0+	A3	IO	**USB Port 0 Data +**
USBP0-	B3	IO	**USB Port 0 Data -**
USBP1+	C4	IO	**USB Port 1 Data +**
USBP1-	D4	IO	**USB Port 1 Data -**
USBP2+	A4	IO	**USB Port 2 Data +**
USBP2-	B4	IO	**USB Port 2 Data -**
USBP3+	B5	IO	**USB Port 3 Data +**
USBP3-	E6	IO	**USB Port 3 Data -**
USBCLK	C3	I	**USB Clock.** 48MHz clock input for the USB interface
USBOC0# / GPIOF / DACK2# **USBOC1# / GPIOE / DRQ2 / SERIRQ**	G5 H3	I / IO / O I / IO / I / I	**USB Port 0 Over Current Detect.** Port 0 is disabled if low. **USB Port 1 Over Current Detect.** Port 1 is disabled if this input is low. Direct inputs are provided for overcurrent protection for ports 0 and 1 which may be used if the alternate functions of these two pins are not required. If overcurrent protection is desired on all four ports (or it is desired to use the alternate functions of these two pins), an external buffer may be used to drive the state of USBOC[3-0]# onto SD[3-0] during ISA bus refresh cycles (i.e., while ISA bus RFSH# is low, so that RFSH# may be used as the buffer enable).
USBOC0# (SD2 & RFSH#)	(W2)	I	**USB Port 0 Over Current Detect**
USBOC1# (SD1 & RFSH#)	(Y2)	I	**USB Port 1 Over Current Detect**
USBOC2# (SD0 & RFSH#)	(Y1)	I	**USB Port 2 Over Current Detect**
USBOC3# (SD3 & RFSH#)	(Y3)	I	**USB Port 3 Over Current Detect**

System Management Bus (SMB) Interface (I^2C Bus)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
SMBCLK	U9	IO	**SMB / I^2C Clock.**
SMBDATA	T9	IO	**SMB / I^2C Data.**
SMBALRT# / GPI6	W10	I	**SMB Alert.** (System Management Bus I/O space Rx08[3] = 1) When the chip is enabled to allow it, assertion generates an IRQ or SMI interrupt or a power management resume event. The same pin is used as General Purpose Input 6 whose value is reflected in Rx48[6] of function 4 I/O space

UltraDMA-33 / 66 Enhanced IDE Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PDRDY / PDDMARDY / PDSTROBE	N16	I	EIDE Mode: **Primary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Primary Device DMA Ready**. Output flow control. The device may assert DDMARDY to pause output transfers **Primary Device Strobe**. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
SDRDY / SDDMARDY / SDSTROBE	V20	I	EIDE Mode: **Secondary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Secondary Device DMA Ready**. Output flow control. The device may assert DDMARDY to pause output transfers **Secondary Device Strobe**. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
PDIOR / PHDMARDY / PHSTROBE	N17	O	EIDE Mode: **Primary Device I/O Read.** Device read strobe UltraDMA Mode: **Primary Host DMA Ready**. Primary channel input flow control**.** The host may assert HDMARDY to pause input transfers **Primary Host Strobe**. Output data strobe (both edges). The host may stop HSTROBE to pause output data transfers
SDIOR / SHDMARDY / SHSTROBE	W19	O	EIDE Mode: **Secondary Device I/O Read.** Device read strobe UltraDMA Mode: **Secondary Host DMA Ready**. Input flow control. The host may assert HDMARDY to pause input transfers **Host Strobe B**. Output strobe (both edges). The host may stop HSTROBE to pause output data transfers
PDIOW# / PSTOP	N18	O	EIDE Mode: **Primary Device I/O Write.** Device write strobe UltraDMA Mode: **Primary Stop**. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
SDIOW# / SSTOP	W20	O	EIDE Mode: **Secondary Device I/O Write.** Device write strobe UltraDMA Mode: **Secondary Stop**. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
PDDRQ	N19	I	**Primary Device DMA Request.** Primary channel DMA request
SDDRQ	Y20	I	**Secondary Device DMA Request.** Secondary channel DMA request
PDDACK#	M20	O	**Primary Device DMA Acknowledge.** Primary channel DMA acknowledge
SDDACK#	V19	O	**Secondary Device DMA Acknowledge.** Secondary channel DMA acknowledge

UltraDMA-33 / 66 Enhanced IDE Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PDCS1#	L20	O	**Primary Master Chip Select.** This signal corresponds to CS1FX# on the primary IDE connector.
PDCS3#	M16	O	**Primary Slave Chip Select.** This signal corresponds to CS3FX# on the primary IDE connector.
SDCS1#	U17	O	**Secondary Master Chip Select.** This signal corresponds to CS17X# on the secondary IDE connector.
SDCS3#	U18	O	**Secondary Slave Chip Select.** This signal corresponds to CS37X# on the secondary IDE connector.
PDA[2-0]	M18, M19, M17	O	**Primary Disk Address.** PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
SDA[2-0]	U20, V18, U19	O	**Secondary Disk Address.** SDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
PDD[15-0]	N20, P17, P19, R16, R18, R20, T17, T19, T20, T18, T16, R19, R17, P20, P18, P16	IO	**Primary Disk Data**
SDD[15-0] / SA[15-0]	P5, R1-R5, T1-T4, U1-U3, V1, V2, W1	IO	**Secondary Disk Data** muxed with ISA Bus Address (Audio Enabled) **ISA Bus Address only** (Audio Disabled / Dedicated Secondary IDE Data) Note: Audio is enabled by strapping the SPKR pin high with 4.7K ohms and disabled by strapping the SPKR pin low with 4.7K ohms.
			Secondary Disk Data (SPKR strap = 0) **or** **AC-Link/Game Ports** (SPKR strap = 1)
SDD[15] / **MSI**,	Y19,	IO / I	**Secondary Disk Data 15 / Midi Serial In**
SDD[14] / **MSO**,	Y18,	IO / O	**Secondary Disk Data 14 / Midi Serial Out**
SDD[13] / **JBB1** / PDRQB,	W17,	IO / I	**Secondary Disk Data 13 / Game Port Joystick B Button 1**
SDD[12] / **JBB2** / PGNTB,	U16,	IO / I	**Secondary Disk Data 12 / Game Port Joystick B Button 2**
SDD[11] / **JAB1** / PDRQA,	W16,	IO / I	**Secondary Disk Data 11 / Game Port Joystick A Button 1**
SDD[10] / **JAB2** / PGNTA,	T15,	IO / I	**Secondary Disk Data 10 / Game Port Joystick A Button 2**
SDD[9] / **JAX** / GPO23,	V15,	IO / I	**Secondary Disk Data 9 / Game Port Joystick A X-axis**
SDD[8] / **JAY** / GPO22,	Y15,	IO / I	**Secondary Disk Data 8 / Game Port Joystick A Y-axis**
SDD[7] / **JBX** / GPI23,	U14,	IO / I	**Secondary Disk Data 7 / Game Port Joystick B X-axis**
SDD[6] / **JBY** / GPI22,	W15,	IO / I	**Secondary Disk Data 6 / Game Port Joystick B Y-axis**
SDD[5] / **ACRST**,	U15,	IO / O	**Secondary Disk Data 5 / AC97 Reset**
SDD[4] / **SDOUT**,	Y16,	IO / O	**Secondary Disk Data 4 / AC97 Serial Data Out**
SDD[3] / **SYNC**,	V16,	IO / O	**Secondary Disk Data 3 / AC97 Sync**
SDD[2] / **SDIN2**,	Y17,	IO / I	**Secondary Disk Data 2 / AC97 Serial Data In 2**
SDD[1] / **SDIN**,	V17,	IO / I	**Secondary Disk Data 1 / AC97 Serial Data In**
SDD[0] / **BITCLK**	W18	IO / I	**Secondary Disk Data 0 / AC97 Bit Clock**

MIDI Interface				
Signal Name	**Pin #**	**I/O**	**Signal Description**	
MSI / SDD[15]	Y19	I / IO	**MIDI Serial In**	/ Secondary Disk Data 15 (SPKR strap = 1)
MSO / SDD[14]	Y18	O / IO	**MIDI Serial Out**	/ Secondary Disk Data 14 (SPKR strap = 1)

AC97 Audio / Modem Interface				
Signal Name	**Pin #**	**I/O**	**Signal Description**	
ACRST / SDD[5]	U15	O / IO	**AC97 Reset**	/ Secondary Disk Data 5 (SPKR strap = 1)
SDOUT / SDD[4]	Y16	O / IO	**AC97 Serial Data Out**	/ Secondary Disk Data 4 (SPKR strap = 1)
SYNC / SDD[3]	V16	O / IO	**AC97 Sync**	/ Secondary Disk Data 3 (SPKR strap = 1)
SDIN2 / SDD[2]	Y17	I / IO	**AC97 Serial Data In 2**	/ Secondary Disk Data 2 (SPKR strap = 1)
SDIN / SDD[1]	V17	I / IO	**AC97 Serial Data In**	/ Secondary Disk Data 1 (SPKR strap = 1)
BITCLK / SDD[0]	W18	I / IO	**AC97 Bit Clock**	/ Secondary Disk Data 0 (SPKR strap = 1)

Game Port Interface				
Signal Name	**Pin #**	**I/O**	**Signal Description**	
JAB1 / SDD[11] / PDRQA	W16	I / IO / I	**Joystick A Button 1**	/ Secondary Disk Data 11 (SPKR strap = 1)
JAB2 / SDD[10] / PGNTA	T15	I / IO / O	**Joystick A Button 2**	/ Secondary Disk Data 10 (SPKR strap = 1)
JBB1 / SDD[13] / PDRQB	W17	I / IO / I	**Joystick B Button 1**	/ Secondary Disk Data 13 (SPKR strap = 1)
JBB2 / SDD[12] / PGNTB	U16	I / IO / O	**Joystick B Button 2**	/ Secondary Disk Data 12 (SPKR strap = 1)
JAX / SDD[9] / GPO23	V15	I / IO / O	**Joystick A X-axis**	/ Secondary Disk Data 9 (SPKR strap = 1)
JAY / SDD[8] / GPO22	Y15	I / IO / O	**Joystick A Y-axis**	/ Secondary Disk Data 8 (SPKR strap = 1)
JBX / SDD[7] / GPI23	U14	I / IO / I	**Joystick B X-axis**	/ Secondary Disk Data 7 (SPKR strap = 1)
JBY / SDD[6] / GPI22	W15	I / IO / I	**Joystick B Y-axis**	/ Secondary Disk Data 6 (SPKR strap = 1)

PDRQ / PGNT Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PDRQA / SDD[11] JAB1	W16	I / IO / I	
PGNTA / SDD[10] / JAB2	T15	O / IO / I	
PDRQB / SDD[13] / JBB1	W17	I / IO / I	
PGNTB / SDD[12] / JBB2	U16	O / IO / I	

Floppy Disk Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
DRVEN0	D9	OD	**Drive Enable 0.** Indicates the drive and media selected.
DRVEN1	D6	OD	**Drive Enable 1.** Indicates the drive and media selected.
MTR0#	E9	OD	**Motor Control 0.** Select motor on drive 0.
MTR1#	C8	OD	**Motor Control 1.** Select motor on drive 1
DS0#	B8	OD	**Drive Select 0.** Select drive 0.
DS1#	A8	OD	**Drive Select 1.** Select drive 1
DIR#	D8	OD	**Direction.** Direction of head movement (0 = inward motion, 1 = outward motion)
STEP#	E8	OD	**Step.** Low pulse for each track-to-track movement of the head.
INDEX#	D7	I	**Index.** Sense to detect that the head is positioned over the beginning of a track
HDSEL#	C7	OD	**Head Select.** Selects the side for R/W operations (0 = side 1, 1 = side 0)
TRK00#	E7	I	**Track 0.** Sense to detect that the head is positioned over track 0.
RDATA#	B6	I	**Read Data.** Raw serial bit stream from the drive for read operatrions.
WDATA#	A7	OD	**Write Data.** Encoded data to the drive for write operations.
WGATE#	B7	OD	**Write Gate.** Signal to the drive to enable current flow in the write head.
DSKCHG#	C6	I	**Disk Change.** Sense that the drive door is open or the diskette has been changed since the last drive selection.
WRTPRT#	A6	I	**Write Protect.** Sense for detection that the diskette is write protected (causes write commands to be ignored)

Parallel Port Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PINIT#	C15	IO	**Initialize.** Initialize printer. Output in standard mode, I/O in ECP/EPP mode.
STROBE#	D16	IO	**Strobe.** Output used to strobe data into the printer. I/O in ECP/EPP mode.
AUTOFD#	C16	IO	**Auto Feed.** Output used to cause the printer to automatically feed one line after each line is printed. I/O pin in ECP/EPP mode.
SLCTIN#	E15	IO	**Select In.** Output used to select the printer. I/O pin in ECP/EPP mode.
SLCT	E13	I	**Select.** Status output from the printer. High indicates that it is powered on.
ACK#	B13	I	**Acknowledge.** Status output from the printer. Low indicates that it has received the data and is ready to accept new data
ERROR#	A15	I	**Error.** Status output from the printer. Low indicates an error condition in the printer.
BUSY	C13	I	**Busy.** Status output from the printer. High indicates not ready to accept data.
PE	D13	I	**Paper End.** Status output from the printer. High indicates that it is out of paper.
PD[7:0]	A13, E14, D14, C14, B14, A14, D15, B15	IO	**Parallel Port Data.**

Serial Ports and Infrared Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
TXD1	A11	O	**Transmit Data 1.** Serial port 1 transmit data out.
TXD2	D10	O	**Transmit Data 2.** Serial port 2 transmit data out.
IRTX / GPO14	E12	O	**Infrared Transmit.** IR transmit data out (Rx76[5] = 0) selectable from serial port 1, 2, or 3. General Purpose Output 14 if Rx76[5] = 1
RXD1	B12	I	**Receive Data 1.** Serial port 1 receive data in.
RXD2	B10	I	**Receive Data 2.** Serial port 2 receive data in.
IRRX / GPO15	D12	IO	**Infrared Receive.** IR receive data in (Rx76[5] = 0) selectable to serial port 1, 2, or 3. General Purpose Output 15 if Rx76[5] = 1
RTS1#	B11	O	**Request To Send 1.** Indicator that serial output port 1 is ready to transmit data. Typically used as hardware handshake with CTS1# for low level flow control. Designed for direct input to external RS-232C driver.
RTS2##	E10	O	**Request To Send 2.** Indicator that serial output port 2 is ready to transmit data. Typically used as hardware handshake with CTS2# for low level flow control. Designed for direct input to external RS-232C driver.
CTS1#	C11	I	**Clear To Send 1.** Indicator to serial port 1 that external communications device is ready to receive data. Typically used as hardware handshake with RTS1# for low level flow control. Designed for input from external RS-232C receiver.
CTS2#	A9	I	**Clear To Send 2.** Indicator to serial port 2 that external communications device is ready to receive data. Typically used as hardware handshake with RTS2# for low level flow control. Designed for input from external RS-232C receiver.
DTR1#	D11	O	**Data Terminal Ready 1.** Serial port 1 indicator that port is powered, initialized, and ready. Typically used as hardware handshake with DSR1# for overall readiness to communicate. Designed for direct input to external RS-232C driver.
DTR2#	B9	O	**Data Terminal Ready 2.** Serial port 2 indicator that port is powered, initialized, and ready. Typically used as hardware handshake with DSR2# for overall readiness to communicate. Designed for direct input to external RS-232C driver.
DSR1#	C12	I	**Data Set Ready 1.** Indicator to serial port 1 that external serial communications device is powered, initialized, and ready. Typically used as hardware handshake with DTR1# for overall readiness to communicate. Designed for direct input from external RS-232C receiver.
DSR2#	C10	I	**Data Set Ready 2.** Indicator to serial port 2 that external serial communications device is powered, initialized, and ready. Typically used as hardware handshake with DTR2# for overall readiness to communicate. Designed for direct input from external RS-232C receiver.
DCD1#	A12	I	**Data Carrier Detect 1.** Indicator to serial port 1 that external modem is detecting a carrier signal (i.e., a communications channel is currently open). In direct connect environments, this input will typically be driven by DTR1# as part of the DTR/DSR handshake. Designed for direct input from external RS-232C receiver.
DCD2#	A10	I	**Data Carrier Detect 2.** Indicator to serial port 2 that external modem is detecting a carrier signal (i.e., a communications channel is currently open). In direct connect environments, this input will typically be driven by DTR2# as part of the DTR/DSR handshake. Designed for direct input from external RS-232C receiver.
RI1#	E11	I	**Ring Indicator 1.** Indicator to serial port 1 that external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel. Designed for direct input from external RS-232C receiver (whose input is typically not connected in direct connect environments).
RI2#	C9	I	**Ring Indicator 2.** Indicator to serial port 2 that external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel. Designed for direct input from external RS-232C receiver (whose input is typically not connected in direct connect environments).

ISA Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
SA[19:16], SA[15-0] / SDD[15-0]	K1, K2, P3, P4, P5, R1, R2, R3, R4, R5, T1, T2, T3, T4, U1, U2, U3, V1, V2, W1	IO IO	**System Address Bus**. SA[19-16] are connected to ISA bus SA[19-16] directly. SA[19-17] are also connected to LA[19-17] of the ISA bus. If the audio interface is disabled (SPKR pin strapped low), SA[15-0] are connected directly to ISA address bus pins SA[15-0] (the audio interface pins are used for the IDE secondary data bus). If the audio interface is enabled (SPKR pin strapped high), SA[15-0] are multiplexed with the IDE Secondary Data Bus. In this case, SA[15-0] may be connected to both SDD[15-0] and ISA bus SA[15-0]. However, if ISA address bus loading is a concern, 74F245 transceivers may be used to externally drive ISA address bus pins SA[15-0]. In this case, these pins would connect directly to the IDE secondary data bus and to the transceiver "A" pins and the ISA address bus would connect to the transceiver "B" pins. SOE# would be used to control the transceiver output enables and the ISA bus MASTER# signal would drive the transceiver direction controls.
LA[23:20]	J2, J3, J4, J5	IO	**System "Latched" Address Bus**: The LA[23:20] address lines are bi-directional. These address lines allow accesses to physical memory on the ISA bus up to 16Mbytes. LA[19-17] on the ISA bus are connected to SA[19-17] (see notes above).
SD[15:0]	P2, P1, N5, N3, N1, M4, M2, L5, W4, Y4, V3, W3, Y3, W2, Y2, Y1	IO	**System Data.** SD[15:0] provide the data path for devices residing on the ISA bus. X-Bus data signals XD[7:0] may be derived if needed from SD[7:0] using an external 74F245-type transceiver (see the XDIR pin description for transceiver connection details). SD7:4 are strap options for keyboard inputs 6:3 (see Function 0 Rx5A)
SBHE#	F2	IO	**System Byte High Enable.** SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles.
IOR#	D1	IO	**I/O Read.** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus.
IOW#	C2	IO	**I/O Write.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus.
MEMR#	U4	IO	**Memory Read.** MEMR# is the command to a memory slave that it may drive data onto the ISA data bus.
MEMW#	V4	IO	**Memory Write.** MEMW# is the command to a memory slave that it may latch data from the ISA data bus.
SMEMR#	A1	O	**Standard Memory Read.** SMEMR# is the command to a memory slave, under 1MB, which indicates that it may drive data onto the ISA data bus
SMEMW#	B1	O	**Standard Memory Write.** SMEMW# is the command to a memory slave, under 1MB, which indicates that it may latch data from the ISA data bus.
BALE	H2	O	**Bus Address Latch Enable.** BALE is an active high signal asserted by the VT82C686A to indicate that the address (SA[19:0], LA[23:17] and the SBHE# signal) is valid
IOCS16#	F3	I	**16-Bit I/O Chip Select.** This signal is driven by I/O devices on the ISA Bus to indicate that they support 16-bit I/O bus cycles.
MCS16#	F1	I	**Memory Chip Select 16.** ISA slaves that are 16-bit memory devices drive this line low to indicate they support 16-bit memory bus cycles.
IOCHCK# / GPI0	F4	I	**I/O Channel Check** (Rx74[0] = 1). When this signal is asserted, it indicates that a parity or an uncorrectable error has occurred for an I/O or memory device on the ISA Bus. The same pin may optionally be used as General Purpose Input 0.
IOCHRDY	A2	I	**I/O Channel Ready** (Rx74[0] = 1). This signal is normally high. Devices on the ISA Bus assert IOCHRDY low to indicate that additional time (wait states) is required to complete the cycle.

ISA Bus Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
RFSH#	E3	IO	**Refresh.** As an output RFSH# indicates when a refresh cycle is in progress. RFSH# is also driven by 16-bit ISA Bus masters to indicate a refresh cycle.
AEN	B2	O	**Address Enable.** AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles.
IRQ1 / MSCK	D5	I / IO	**Interrupt Request 1** (Rx5A[1] = 0)
IRQ3	G4	I	**Interrupt Request 3.**
IRQ4	G3	I	**Interrupt Request 4.**
IRQ5	G2	I	**Interrupt Request 5.**
IRQ6 / GPI4 / SLPBTN#	G1	I / I / I	**Interrupt Request 6.**
IRQ7	F5	I	**Interrupt Request 7.**
IRQ8# / GPI1	W11	I / I	**Interrupt Request 8** from ext RTC if int RTC disabled (Rx5A[2] = 0)
IRQ9	H4	I	**Interrupt Request 9.**
IRQ10	K3	I	**Interrupt Request 10.**
IRQ11	K4	I	**Interrupt Request 11.**
IRQ12 / MSDT	C5	I / IO	**Interrupt Request 12.** (Rx5A[1] = 0)
IRQ14	L1	I	**Interrupt Request 14.**
IRQ15	K5	I	**Interrupt Request 15.**
DRQ7 / GPI21, **DRQ6** / GPI20, **DRQ5** / GPI19, **DRQ3** / GPI18, **DRQ2** / GPI12 / SERIRQ / GPIOE / USBOC1#, **DRQ1** / GPI17, **DRQ0** / GPI16	N4, M5, M1, D3, H3, E2, L3	I / I I / I I / I I / I I / I / I / IO / I I / I I / I	**DMA Request.** Used to request DMA services from the internal DMA controller.
DACK7# / USBIRQB / GPO21, **DACK6#** / USBIRQA / GPO20, **DACK5#** / MC97IRQ / GPO19 / SERIRQ, **DACK3#** / AC97IRQ / GPO18, **DACK2#** / USBOC0# / GPIOF / GPI13, **DACK1#** / IDEIRQB / GPO17, **DACK0#** / IDEIRQA / GPO16	N2, M3, L4, D2, G5, E1, L2	O / O / O O / O / O O / O / O / I O / O / O O / I / IO / I O / O / O O / O / O	**Acknowledge.** Used by the internal DMA controller to indicate that a request for DMA service has been granted.
TC	H1	O	**Terminal Count.** Asserted to DMA slaves as a terminal count indicator.
SPKR / strap	V5	O / I	**Speaker Drive.** Output of internal timer/counter 2. Also functions as a **strap input** sampled at reset to determine the function of the Audio / Game interface pins: 0=Disable Audio / Game interface (pins used for IDE Secondary Data Bus SDD[15-0] and ISA SA[15-0] pins used for ISA bus only), 1=Enable Audio / Game interface (pins used for Audio/Game functions and SDD[15-0] are multiplexed with ISA SA[15-0]).
SOE# / SCIOUT# / GPO13	U5	O / O / O	**ISA Address (SA) Output Enable.** Asserted low when ISA address (SA) is valid (deasserted when SDD is valid) when SA and SDD are multiplexed on SA pins 15-0 (i.e., when SPKR is strapped low to enable the audio interface pins). SOE# is tied directly to the output enable of 74F245 transceivers that buffer IDE Secondary Bus data and ISA-address (see SA pins for more information).

Serial IRQ			
Signal Name	**Pin #**	**I/O**	**Signal Description**
SERIRQ / DRQ2 / GPIOE / USBOC1#	H3	I	**Serial IRQ** (Rx68[3] = 1 and Rx74[6] = 0 and Rx75[3] = 1)
SERIRQ / DACK5# / GPO19 / MC97IRQ	L4	I	**Serial IRQ** (Rx68[3] = 1 and Rx74[6] = 1)

Internal Keyboard Controller			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MSCK / IRQ1	D5	IO / I	**MultiFunction Pin** (Internal mouse controller enabled by Rx5A[1]) Rx5A[1]=1 **Mouse Clock.** From internal mouse controller. Rx5A[1]=0 **Interrupt Request 1**. Interrupt input 1.
MSDT / IRQ12	C5	IO / I	**MultiFunction Pin** (Internal mouse controller enabled by Rx5A[1]) Rx5A[1]=1 **Mouse Data.** From internal mouse controller. Rx5A[1]=0 **Interrupt Request 12**. Interrupt input 12.
KBCK / A20GATE	E5	IO / I	**MultiFunction Pin** (Internal keyboard controller enabled by Rx5A[0]) Rx5A[0]=1 **Keyboard Clock.** From internal keyboard controller Rx5A[0]=0 **Gate A20.** Input from external keyboard controller.
KBDT / KBRC	A5	IO / I	**MultiFunction Pin** (Internal keyboard controller enabled by Rx5A[0]) Rx5A[0]=1 **Keyboard Data.** From internal keyboard controller. Rx5A[0]=0 **Keyboard Reset.** From external keyboard controller (KBC) for CPURST# generation
KBCS# / ROMCS# / **strap**	C1	O / O / I	**Keyboard Chip Select** (Rx5A[0]=0). To external keyboard controller chip. **Power-Up Configuration Strap (Sampled At Reset)**: 4.7K to GND = Socket-7, 4.7K to VCC3 = Socket-370 / Slot-1
KBIN[6-3] / SD[7-4]	W4, Y4, V3, W3	I / IO	**Keyboard Inputs 6-3.** Sampled at reset on SD[7-4] and latched into Rx5A[7-4].

Chip Selects			
Signal Name	**Pin #**	**I/O**	**Signal Description**
ROMCS# / KBCS# / **strap**	C1	O / O / I	**ROM Chip Select** (Rx5A[0]=1). Chip Select to the BIOS ROM. **Power-Up Configuration Strap (Sampled At Reset)**: 4.7K to GND = Socket-7, 4.7K to VCC3 = Socket-370 / Slot-1
PCS0# / GPO12 / XDIR	T5	O / IO / IO	**Programmable Chip Select 0** (Rx76[1] = 1 and Rx76[4] = 1). Asserted during I/O cycles to programmable read or write ISA I/O port ranges. Addressed devices drive data to the SD pins (XDIR is disabled and the X-Bus is not implemented).
MCCS# / GPIOD / GPIO11	U8	O / IO / IO	**Microcontroller Chip Select** (Rx76[1] = 1 and Rx76[3] = 1). Asserted during read or write accesses to I/O ports 62h or 66h.

General Purpose Inputs			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GPI0 / IOCHCK#	F4	I	**General Purpose Input 0** (Rx74[0] = 0)
GPI1 / IRQ8#	W11	I	**General Purpose Input 1** (Rx5A[2] = 1)
GPI2 / BATLOW#	U11	I	**General Purpose Input 2**
GPI3 / LID / APICREQ#	U10	I	**General Purpose Input 3**
GPI4 / IRQ6 / SLPBTN#	G1	I	**General Purpose Input 4**
GPI5 / PME# / THRM	T11	I	**General Purpose Input 5** (Read pin state at function 4 Rx48[5])
GPI6 / SMBALRT#	W10	I	**General Purpose Input 6**
GPI7 / RING#	V11	I	**General Purpose Input 7**
GPI8 / GPO8 / GPIOA / GPOWE#	T14	I	**General Purpose Input 8** (Rx74[2] = 0)
GPI9 / GPO9 / GPIOB / FAN2 / DTEST	U12	I	**General Purpose Input 9** (Rx74[3] = 0)
GPI10 / GPO10 / GPIOC / CHAS / ATEST	V14	I	**General Purpose Input 10** (Rx74[4] = 0)
GPI11 / GPO11 / GPIOD	U8	I	**General Purpose Input 11** (Rx74[5] = 0)
GPI12 / GPO24 / GPIOE / DRQ2 / SERIRQ / USBOC1#	H3	I	**General Purpose Input 12** (Rx75[3] = 1 & 75[1]=0 & 68[3]=0)
GPI13 / GPO25 / GPIOF / DACK2# / USBOC0#	G5	I	**General Purpose Input 13** (Rx75[3] = 1 & 75[2]=0)
GPI16 / DRQ0 **(Rev H)**	L3	I	**General Purpose Input 16** (Rx77[7] = 1)
GPI17 / DRQ1 **(Rev H)**	E2	I	**General Purpose Input 17** (Rx77[7] = 1)
GPI18 / DRQ3 **(Rev H)**	D3	I	**General Purpose Input 18** (Rx77[7] = 1)
GPI19 / DRQ5 **(Rev H)**	M1	I	**General Purpose Input 19** (Rx77[7] = 1)
GPI20 / DRQ6 **(Rev H)**	M5	I	**General Purpose Input 20** (Rx77[7] = 1)
GPI21 / DRQ7 **(Rev H)**	N4	I	**General Purpose Input 21** (Rx77[7] = 1)
GPI22 / SDD6 **(Rev H)**	W15	I	**General Purpose Input 22** (Rx77[6] = 1, audio ena, game disa)
GPI23 / SDD7 **(Rev H)**	U14	I	**General Purpose Input 23** (Rx77[6] = 1, audio ena, game disa)
GPI[23-16] (SD[7-0] & RFSH#)	n/a	I	**General Purpose Inputs 16-23** (enabled on SD[7-0] by RFSH# active) (Rx77[7] = 0)

General Purpose Outputs			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GPO0 / SLOWCLK	T8	O	**General Purpose Output 0** (Function 4 Rx54[0] = 0 and Rx54[1] = 0)
GPO1 / SUSA#	V9	O	**General Purpose Output 1** (Rx74[7] = 0 and Function 4 Rx54[2] = 1)
GPO2 / SUSB#	W9	O	**General Purpose Output 2** (Rx74[7] = 0 and Function 4 Rx54[3] = 1)
GPO3 / SDD[2] / SDIN2 / SUSST1#	Y17	O	**General Purpose Output 3** (Function 4 Rx54[4] = 1)
GPO4 / CPUSTP#	Y12	O	**General Purpose Output 4** (Rx75[4] = 1)
GPO5 / PCISTP#	V12	O	**General Purpose Output 5** (Rx75[5] = 1)
GPO6 / SUSST1#	V10	O	**General Purpose Output 6** (Rx75[6] = 1)
GPO7 / SLP#	T7	O	**General Purpose Output 7** (Rx75[7] = 1)
GPO8 / GPI8 / GPIOA / GPOWE#	T14	O	**General Purpose Output 8** (Rx74[2] = 1 and Rx76[0] = 0)
GPO9 / GPI9 / GPIOB / FAN2	U12	O	**General Purpose Output 9** (Rx74[3] = 1)
GPO10 / GPI10 / GPIOC / CHAS	V14	O	**General Purpose Output 10** (Rx74[4] = 1 and Rx76[2] = 0)
GPO11 / GPI11 / GPIOD	U8	O	**General Purpose Output 11** (Rx74[5] = 1 and Rx76[3] = 0)
GPO12 / XDIR / PCS0#	T5	O	**General Purpose Output 12** (Rx76[1] = 1 and Rx76[4] = 0)
GPO13 / SOE# / SCIOUT#	U5	O	**General Purpose Output 13** (Rx77[0] = 1 and Rx74[7] = 0)
GPO14 / IRTX	E12	O	**General Purpose Output 14** (Rx76[5] = 1)
GPO15 / IRRX	D12	O	**General Purpose Output 15** (Rx76[5] = 1)
GPO16 / DACK0# (**Rev H**)	L2	O	**General Purpose Output 16** (Rx77[7] = 1 and Rx77[3] = 0)
GPO17 / DACK1# (**Rev H**)	E1	O	**General Purpose Output 17** (Rx77[7] = 1 and Rx77[3] = 0)
GPO18 / DACK3# (**Rev H**)	D2	O	**General Purpose Output 18** (Rx77[7] = 1 and Rx77[3] = 0)
GPO19 / DACK5# (**Rev H**)	L4	O	**General Purpose Output 19** (Rx77[7] = 1 and Rx77[3] = 0)
GPO20 / DACK6# (**Rev H**)	M3	O	**General Purpose Output 20** (Rx77[7] = 1 and Rx77[3] = 0)
GPO21 / DACK7# (**Rev H**)	N2	O	**General Purpose Output 21** (Rx77[7] = 1 and Rx77[3] = 0)
GPO22 / SDD8 (**Rev H**)	Y15	O	**General Purpose Output 22** (Rx77[6] = 1, audio enabled, game disabled)
GPO23 / SDD9 (**Rev H**)	V15	O	**General Purpose Output 23** (Rx77[6] = 1, audio enabled, game disabled)
GPO24/DRQ2/GPI12/IOE/SIRQ/OC1	H3	O	**General Purpose Output 24** (Rx75[3] = 1 & Rx75[1]=1 & Rx68[3]=0)
GPO25/DACK2#/GPI13/GPIOF/OC0	G5	O	**General Purpose Output 25** (Rx75[3] = 1 & Rx75[2]=1)
GPO[23-16] (latched from SD[7-0])	n/a	O	**General Purpose Output 23-16** (Rx74[7]=0) latched by GPOWE# rising
GPOWE# / GPIOA / GPI8 / GPO8	T14	O	**General Purpose Output Write Enable** (Rx74[2] = 1 and Rx76[0] = 1).

General Purpose I/Os			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GPIOA (GPIO8) / GPOWE#	T14	IO	**General Purpose I/O A / 8** (Rx76[0] = 0). GPOWE# if Rx76[0] = 1.
GPIOB (GPIO9) / FAN2 / DTEST	U12	IO	**General Purpose I/O B / 9**
GPIOC (GPIO10) / CHAS / ATEST	V14	IO	**General Purpose I/O C / 10** (Rx76[2] = 0)
GPIOD (GPIO11) / MCCS#	U8	IO	**General Purpose I/O D / 11**
GPIOE / GPI12 / USBOC1# / DRQ2 / SERIRQ	H3	IO	**General Purpose I/O E**
GPIOF / GPI13 / USBOC0# / DACK2#	G5	IO	**General Purpose I/O F**

Hardware Monitoring			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VSENS1	U13	I	**Voltage Sense 2.0V.** Monitor for CPU core voltage.
VSENS2	V13	I	**Voltage Sense 2.5V.** Monitor for North Bridge core voltage.
VSENS3	W14	I	**Voltage Sense 5V.**
VSENS4	Y14	I	**Voltage Sense 12V.** Connect +12V through a resistive voltage divider to insure 5V max to the input pin (see MVP4 Design Guide for details).
VREF	T13	P	**Voltage Reference for Thermal Sensing** (5V ±5%)
TSENS1	W13	I	**Temperature Sense 1.**
TSENS2	Y13	I	**Temperature Sense 2.**
FAN1	T12	I	**Fan Speed Monitor 1.** (3.3V only)
FAN2 / GPIOB/9 / DTEST	U12	I	**Fan Speed Monitor 2.**
CHAS / GPIOC/10 / ATEST	V14	I	**Chassis Intrusion Detect** (Rx76[2] = 1 and Rx74[4] = 1). Used for system security purposes.
DTEST / FAN2 / GPIOB/9 **ATEST** / CHAS / GPIOC/10	U12 V14	O O	**Hardware Monitor Digital Test Out** **Hardware Monitor Analog Test Out**

XD Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
XDIR / PCS0# / GPO12	T5	O	**X-Bus Data Direction.** (Rx76[1]=0) Asserted low for all I/O read cycles and for memory read cycles to the programmed BIOS address space. XDIR is tied directly to the direction control of a 74F245 transceiver that buffers the X-Bus data and ISA-Bus data. The transceiver output enable may be grounded. SD0-7 connect to the "A" side of the transceiver and XD0-7 connect to the "B" side. XDIR high indicates that SD0-7 drives XD0-7.

Power Management			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PME# / **THRM** / GPI5	T11	I	**MultiFunction Pin** **Power Management Event** (Rx74[1] = 0) (10K PU to VCCS if not used) **Thermal Alarm Monitor** (Rx74[1] = 1) General Purpose Input 5 (pin state may be read at Function 4 I/O Rx48[5])
PWRBTN#	Y11	I	**Power Button.** Used by the Power Management subsystem to monitor an external system on/off button or switch. The VT82C686A performs a 200us debounce of this input if Function 4 Rx40[5] is set to 1. (3.3V only)
SLPBTN# / IRQ6 / GPI4	G1	I / I / I	**Sleep Button.** Used by the Power Management subsystem to monitor an external system sleep button or switch. (Function 4 Rx40[6]=1) (10K PU to VCC if not used)
RSMRST#	V6	I	**Resume Reset.** Resets the internal logic connected to the VCCS power plane and also resets portions of the internal RTC logic.
EXTSMI#	Y10	IOD	**External System Management Interrupt.** When enabled to allow it, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. (10K PU to VCCS if not used) (3.3V only)
SMBALRT# / GPI6	W10	I	**SMB Alert** (System Management Bus I/O space Rx08[3] = 1). When the chip is enabled to allow it, assertion generates an IRQ or SMI or power management event. (10K PU to VCCS if not used)
LID / GPI3	U10	I	**Notebook Computer Display Lid Open / Closed Monitor.** Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high and/or high-to-low transitions to generate an SMI#. The VT82C686A performs a 200 usec debounce of this input if Function 4 Rx40[5] is set to 1. (10K PU to VCCS if not used)
RING# / GPI7	V11	I	**Ring Indicator.** May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. (10K PU to VCCS if not used)
BATLOW# / GPI2	U11	I	**Battery Low Indicator.** (10K PU to VCCS if not used) (3.3V only)
CPUSTP# / GPO4	Y12	O	**CPU Clock Stop** (Rx75[4] = 0). Signals the system clock generator to disable the CPU clock outputs. Not connected if not used.
PCISTP# / GPO5	V12	O	**PCI Clock Stop** (Rx75[5] = 0). Signals the system clock generator to disable the PCI clock outputs. Not connected if not used.
SLOWCLK / GPO0	T8		**Slow Clock** (Function 4 Rx54[0] = 1 or Rx54[1] = 1).
SUSA# / GPO1 / APICACK#	V9	O	**Suspend Plane A Control** (Rx74[7]=0 and Function 4 Rx54[2]=0). Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane. (10K PU to VCCS if not used)
SUSB# / GPO2 / APICCS#	W9	O	**Suspend Plane B Control** (Rx74[7]=0 and Function 4 Rx54[3]=0). Asserted during power management STR and STD suspend states. Used to control the secondary power plane. (10K PU to VCCS if not used)
SUSC#	Y9	O	**Suspend Plane C Control.** Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry.
SUSST1# / GPO6 **SUSST1#** / GPO3	V10 Y17	O O	**Suspend Status 1** (Rx75[6] = 0 for GPO6 and Func4 Rx54[4] = 0 for GPO3). Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend states. Connect 10K PU to VCCS.
SUSCLK	T10	O	**Suspend Clock.** 32.768 KHz output clock for use by the North Bridge (e.g., Apollo MVP3 or MVP4) for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes. Connect 10K PU to VCCS.

Resets and Clocks			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PWRGD	W6	I	**Power Good.** Connected to the PWRGOOD signal on the Power Supply.
PCIRST#	B16	O	**PCI Reset.** Active low reset signal for the PCI bus. The VT82C686A will assert this pin during power-up or from the control register.
RSTDRV	J1	O	**Reset Drive.** Reset signal to the ISA bus. Connect through an inverter to the chipset north bridge RESET# input and to PCI bus RESET#.
BCLK	H5	O	**Bus Clock.** ISA bus clock.
OSC	E4	I	**Oscillator.** 14.31818 MHz clock signal used by the internal Timer.
RTCX1	Y5	I	**RTC Crystal Input**: 32.768 KHz crystal or oscillator input. This input is used for the internal RTC and for power-well power management logic.
RTCX2	W5	O	**RTC Crystal Output**: 32.768 KHz crystal output

Power and Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCC	F7, F10, F12-F14, H6, H15, J6, J15, K6, K15, M6, M15, N6, N15, R7-R8, R11, R14	P	**Core Power.** 3.3V nominal (3.15V to 3.45V). This supply is turned on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high. This pin should be connected to the same voltage as the CPU I/O circuitry. Internally connected to hardware monitoring system voltage detection circuitry for 3.3V monitoring.
GND	F6, F11, F15, G6, G15, J9-J12, K9-K12, L6, L9-L12, L15, M9-M12, P6, P15, R6, R15	P	**Ground.** Connect to primary motherboard ground plane.
VCCS	R9-R10	P	**Suspend Power.** Always available unless the mechanical switch of the power supply is turned off. If the "soft-off" state is not implemented, then this pin can be connected to VCC. Signals powered by or referenced to this plane are: PWRGD, RSMRST#, PWRBTN#, SMBCLK, SMBDATA, SUSCLK, SUSA# / GPO1, SUSB# / GPO2, SUSC#, SUSST1# / GPO6, GPI1 / IRQ8#, GPI2 / BATLOW#, GPI3 / LID, GPI5 / PME#, GPI6 / SMBALRT#, GPI7 / RING#, GPO0
VBAT	Y6	P	**RTC Battery.** Battery input for internal RTC (RTCX1, RTCX2)
VREF	T13	P	**Voltage Reference** (5V ±5%). For thermal sensing and 5V input tolerance.
VCCH	R12	P	**Hardware Monitor Power.** Power for hardware monitoring subsystem (voltage monitoring, temperature monitoring, and fan speed monitoring). Connect to VCC through a ferrite bead.
GNDH	R13	P	**Hardware Monitor Ground.** Connect to GND through a ferrite bead.
VCCU	F9	P	**USB Differential Output Power.** Power for USB differential outputs (USBP0+, P0-, P1+, P1-, P2+, P2-, P3+, P3-). Connect to VCC through a ferrite bead.
GNDU	F8	P	**USB Differential Output Ground.** Connect to GND through a ferrite bead.

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the VT82C686A. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated

Table 2. System I/O Map

Port	Function	Actual Port Decoding
00-1F	Master DMA Controller	0000 0000 000x nnnn
20-3F	Master Interrupt Controller	0000 0000 001x xxxn
40-5F	Timer / Counter	0000 0000 010x xxnn
60-6F	Keyboard Controller	0000 0000 0110 xnxn
(60h)	KBC Data	0000 0000 0110 x0x0
(61h)	Misc Functions & Spkr Ctrl	0000 0000 0110 xxx1
(64h)	KBC Command / Status	0000 0000 0110 x1x0
70-77	RTC/CMOS/NMI-Disable	0000 0000 0111 0nnn
78-7F	-available for system use-	0000 0000 0111 1xxx
80	-reserved- (debug port)	0000 0000 1000 0000
81-8F	DMA Page Registers	0000 0000 1000 nnnn
90-91	-available for system use-	0000 0000 1001 000x
92	System Control	0000 0000 1001 0010
93-9F	-available for system use-	0000 0000 1001 nnnn
A0-BF	Slave Interrupt Controller	0000 0000 101x xxxn
C0-DF	Slave DMA Controller	0000 0000 110n nnnx
E0-FF	-available for system use-	0000 0000 111x xxxx
100-CF7	-available for system use*	
CF8-CFB	PCI Configuration Address	0000 1100 1111 10xx
CFC-CFF	PCI Configuration Data	0000 1100 1111 11xx
D00-FFFF	-available for system use-	

* On-Chip Super-I/O Functions – PC-Standard Port Addresses

200-20F	Game Port
2E8-2EF	COM4
2F8-2FF	COM2
378-37F	Parallel Port (Standard & EPP)
3E8-3EF	COM3
3F0-3F1	Configuration Index / Data
3F0-3F7	Floppy Controller
3F8-3FF	COM1
400-402	Parallel Port (ECP Extensions)

Table 3. Registers

Legacy I/O Registers

Port	Master DMA Controller Registers	Default	Acc
00	Channel 0 Base & Current Address		RW
01	Channel 0 Base & Current Count		RW
02	Channel 1 Base & Current Address		RW
03	Channel 1 Base & Current Count		RW
04	Channel 2 Base & Current Address		RW
05	Channel 2 Base & Current Count		RW
06	Channel 3 Base & Current Address		RW
07	Channel 3 Base & Current Count		RW
08	Status / Command		RW
09	Write Request		**WO**
0A	Write Single Mask		**WO**
0B	Write Mode		**WO**
0C	Clear Byte Pointer FF		**WO**
0D	Master Clear		**WO**
0E	Clear Mask		**WO**
0F	Read / Write Mask		RW

Port	Master Interrupt Controller Regs	Default	Acc
20	Master Interrupt Control	—	*
21	Master Interrupt Mask	—	*
20	Master Interrupt Control Shadow	—	**RW**
21	Master Interrupt Mask Shadow	—	**RW**

* RW if shadow registers are disabled

Port	Timer/Counter Registers	Default	Acc
40	Timer / Counter 0 Count		RW
41	Timer / Counter 1 Count		RW
42	Timer / Counter 2 Count		RW
43	Timer / Counter Control		**WO**

Port	Keyboard Controller Registers	Default	Acc
60	Keyboard Controller Data		RW
61	Misc Functions & Speaker Control		RW
64	Keyboard Ctrlr Command / Status		RW

Port	CMOS / RTC / NMI Registers	Default	Acc
70	CMOS Memory Address & NMI Disa		**WO**
71	CMOS Memory Data (128 bytes)		RW
72	CMOS Memory Address		RW
73	CMOS Memory Data (256 bytes)		RW
74	CMOS Memory Address		RW
75	CMOS Memory Data (256 bytes)		RW

NMI Disable is port 70h (CMOS Memory Address) bit-7.
RTC control occurs via specific CMOS data locations (0-0Dh).
Ports 72-73 may be used to access all 256 locations of CMOS.
Ports 74-75 may be used to access CMOS if the internal RTC is disabled.

Port	DMA Page Registers	Default	Acc
87	DMA Page - DMA Channel 0		RW
83	DMA Page - DMA Channel 1		RW
81	DMA Page - DMA Channel 2		RW
82	DMA Page - DMA Channel 3		RW
8F	DMA Page - DMA Channel 4		RW
8B	DMA Page - DMA Channel 5		RW
89	DMA Page - DMA Channel 6		RW
8A	DMA Page - DMA Channel 7		RW

Port	System Control Registers	Default	Acc
92	System Control		RW

Port	Slave Interrupt Controller Regs	Default	Acc
A0	Slave Interrupt Control	—	*
A1	Slave Interrupt Mask	—	*
A0	Slave Interrupt Control Shadow	—	**RW**
A1	Slave Interrupt Mask Shadow	—	**RW**

* RW accessible if shadow registers are disabled

Port	Slave DMA Controller Registers	Default	Acc
C0	Channel 0 Base & Current Address		RW
C2	Channel 0 Base & Current Count		RW
C4	Channel 1 Base & Current Address		RW
C6	Channel 1 Base & Current Count		RW
C8	Channel 2 Base & Current Address		RW
CA	Channel 2 Base & Current Count		RW
CC	Channel 3 Base & Current Address		RW
CE	Channel 3 Base & Current Count		RW
D0	Status / Command		RW
D2	Write Request		**WO**
D4	Write Single Mask		**WO**
D6	Write Mode		**WO**
D8	Clear Byte Pointer FF		**WO**
DA	Master Clear		**WO**
DC	Clear Mask		**WO**
DE	Read / Write Mask		RW

Super-I/O Configuration Registers (I/O Space)

Port	Super-I/O Configuration Registers	Default	Acc
3F0	Super-I/O Config Index (Rx85[1]=1)	00	RW
3F1	Super-I/O Config Data (Rx85[1]=1)	00	RW

Super-I/O Configuration Registers (Indexed via Port 3F0/1)

Offset	Super-I/O Control	Default	Acc
00-DF	-reserved-	00	RO
E0	Super-I/O Device ID	3C	**RW**
E1	Super-I/O Device Revision	00	**RW**
E2	Function Select	00	**RW**
E3	Floppy Ctrlr Base Addr (def = 3F0-7)	FC	**RW**
E4-E5	-reserved-	00	RO
E6	Parallel Port Base Addr (def = 378-F)	DE	**RW**
E7	Serial Port 1 Base Addr (def = 3F8-F)	FE	**RW**
E8	Serial Port 2 Base Addr (def = 2F8-F)	BE	**RW**
E9-ED	-reserved-	00	RO
EE	Serial Port Configuration	00	**RW**
EF	Power Down Control	00	**RW**
F0	Parallel Port Printer Control	00	**RW**
F1	Serial Port Control	00	**RW**
F2	Test Mode (Do Not Program)	00	**RW**
F3	-reserved-	00	RO
F4	Test Mode (Do Not Program) 2	00	**RW**
F5	-reserved-	00	RO
F6	Floppy Controller Configuration	00	**RW**
F7	-reserved-	00	RO
F8	Floppy Controller Drive Select	00	**RW**
F9-FB	-reserved-	00	RO
FC	General Purpose I/O	00	**RW**
FD-FF	-reserved-	00	RO

Super-I/O I/O Ports

Offset	Floppy Disk Controller (3F0-3F7)	Default	Acc
00	-reserved-	00	--
01	FDC Status A / B (Rx85[1]=0)	--	**RO**
02	FDC Command	--	RW
03	-reserved-	00	--
04	FDC Main Status	--	**RO**
04	FDC Data Rate Select	00	**WO**
05	FDC Data	--	RW
06	-reserved-	00	--
07	Diskchange Status	--	**RO**
07	FDC Configuration Control	00	**WO**

Offset	Parallel Port (378-37F typical)	Default	Acc
00	Parallel Port Data	--	RW
01	Parallel Port Status	--	**RO**
02	Parallel Port Control	E0	RW
03	EPP Address		RW
04	EPP Data Port 0		RW
05	EPP Data Port 1		RW
06	EPP Data Port 2		RW
07	EPP Data Port 3		RW
400h	ECP Data / Configuration A		RW
401h	ECP Configuration B		RW
402h	ECP Extended Control		RW

Offset	Serial Port 1 (COM1=3F8, 3=3E8)	Default	Acc
0	Transmit (Wr) / Receive (Rd) Buffer		RW
1	Interrupt Enable		RW
2	FIFO Control		**WO**
2	Interrupt Status		**RO**
3	UART Control		RW
4	Handshake Control		RW
5	UART Status		RW
6	Handshake Status		RW
7	Scratchpad		RW
9-8	Baud Rate Generator Divisor		RW
A-F	-undefined-		--

Offset	Serial Port 2 (COM2=2F8, 4=2E8)	Default	Acc
0	Transmit (Wr) / Receive (Rd) Buffer		RW
1	Interrupt Enable		RW
2	FIFO Control		**WO**
2	Interrupt Status		**RO**
3	UART Control		RW
4	Handshake Control		RW
5	UART Status		RW
6	Handshake Status		RW
7	Scratchpad		RW
9-8	Baud Rate Generator Divisor		RW
A-F	-undefined-		--

PCI Function 0 Registers - PCI-to-ISA Bridge

Configuration Space PCI-to-ISA Bridge Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	0686	RO
5-4	Command	0087	**RW**
7-6	Status	0200	**WC**
8	Revision ID	nn	RO
9	Programming Interface	00	RO
A	Sub Class Code	01	RO
B	Base Class Code	06	RO
C	-reserved- (cache line size)	00	—
D	-reserved- (latency timer)	00	—
E	Header Type	80	RO
F	Built In Self Test (BIST)	00	RO
10-27	-reserved- (base address registers)	00	—
28-2B	-reserved- (unassigned)	00	—
2F-2C	Subsystem ID Read	00	RO
30-33	-reserved- (expan. ROM base addr)	00	—
34-3B	-reserved- (unassigned)	00	—
3C	-reserved- (interrupt line)	00	—
3D	-reserved- (interrupt pin)	00	—
3E	-reserved- (min gnt)	00	—
3F	-reserved- (max lat)	00	—

Configuration Space PCI-to-ISA Bridge-Specific Registers

Offset	ISA Bus Control	Default	Acc
40	ISA Bus Control	00	RW
41	ISA Test Mode	00	RW
42	ISA Clock Control	00	RW
43	ROM Decode Control	00	RW
44	Keyboard Controller Control	00	RW
45	Type F DMA Control	00	RW
46	Miscellaneous Control 1	00	RW
47	Miscellaneous Control 2	00	RW
48	Miscellaneous Control 3	01	RW
49	-reserved-	00	—
4A	IDE Interrupt Routing	04	RW
4B	-reserved-	00	—
4C	DMA / Master Mem Access Control 1	00	RW
4D	DMA / Master Mem Access Control 2	00	RW
4F-4E	DMA / Master Mem Access Control 3	0300	RW

Offset	Plug and Play Control	Default	Acc
50	PnP DMA Request Control	2D	RW
51	PnP Routing for LPT / FDC IRQ	00	RW
52	PnP Routing for COM2 / COM1 IRQ	00	RW
53	-reserved-	00	—
54	PCI IRQ Edge / Level Select	00	RW
55	PnP Routing for PCI INTA	00	RW
56	PnP Routing for PCI INTB-C	00	RW
57	PnP Routing for PCI INTD	00	RW
58-59	-reserved-	00	—
5A	KBC / RTC Control	x4†	RW
5B	Internal RTC Test Mode	00	RW
5C	DMA Control	00	RW
5F-5D	-reserved-	00	—

† Bit 7-4 power-up default value depends on external strapping

Offset	Distributed DMA	Default	Acc
61-60	Channel 0 Base Address / Enable	0000	RW
63-62	Channel 1 Base Address / Enable	0000	RW
65-64	Channel 2 Base Address / Enable	0000	RW
67-66	Channel 3 Base Address / Enable	0000	RW
69-68	Serial IRQ Control	0000	RW
6B-6A	Channel 5 Base Address / Enable	0000	RW
6D-6C	Channel 6 Base Address / Enable	0000	RW
6F-6E	Channel 7 Base Address / Enable	0000	RW

Offset	Miscellaneous	Default	Acc
70	Subsystem ID Write	00	WO
71-73	-reserved-	00	—
74	GPIO Control 1	00	RW
75	GPIO Control 2	00	RW
76	GPIO Control 3	00	RW
77	GPIO Control 4	00	RW
79-78	Programmable Chip Select Control	0000 0000	RW
7A-7F	-reserved-	00	—
80	Programmable Chip Select Mask	00	RW
81	ISA Positive Decoding Control 1	00	RW
82	ISA Positive Decoding Control 2	00	RW
83	ISA Positive Decoding Control 3	00	RW
84	ISA Positive Decoding Control 4	00	RW
85	Extended Function Enable	00	RW
86-87	PnP IRQ/DRQ Test (do not program)	00	RW
88	PLL Test	00	RW
89	PLL Control	00	RW
8A-FF	-reserved-	00	—

PCI Function 1 Registers - IDE Controller

Configuration Space IDE Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	0571	RO
5-4	Command	0080	RO
7-6	Status	0280	**RW**
8	Revision ID	nn	RO
9	Programming Interface	85	**RW**
A	Sub Class Code	01	RO
B	Base Class Code	01	RO
C	-reserved- (cache line size)	00	—
D	Latency Timer	00	RW
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Base Address - Pri Data / Command	000001F0	RO
17-14	Base Address - Pri Control / Status	000003F4	RO
1B-18	Base Address - Sec Data / Command	00000170	RO
1F-1C	Base Address - Sec Control / Status	00000374	RO
23-20	Base Address - Bus Master Control	0000CC01	**RW**
24-2F	-reserved- (unassigned)	00	—
30-33	-reserved- (expan ROM base addr)	00	—
34-3B	-reserved- (unassigned)	00	—
3C	Interrupt Line	0E	RW
3D	Interrupt Pin	00	RO
3E	Minimum Grant	00	RO
3F	Maximum Latency	00	RO

Configuration Space IDE-Specific Registers

Offset	Configuration Space IDE Registers	Default	Acc
40	IDE Chip Enable	08	RW
41	IDE Configuration	02	RW
42	-reserved- (do not program)	09	**RW**
43	IDE FIFO Configuration	3A	RW
44	IDE Miscellaneous Control 1	68	RW
45	IDE Miscellaneous Control 2	03	RW
46	IDE Miscellaneous Control 3	C0	RW
4B-48	IDE Drive Timing Control	A8A8A8A8	RW
4C	IDE Address Setup Time	FF	RW
4D	-reserved- (do not program)	00	**RW**
4E	Sec Non-1F0 IDE Port Access Timing	FF	RW
4F	Pri Non-1F0 IDE Port Access Timing	FF	RW
53-50	UltraDMA Extended Timing Control	03030303	RW
54	UltraDMA FIFO Control	06	RW
55-5F	-reserved-	00	—
61-60	IDE Primary Sector Size	0200	RW
62-67	-reserved-	00	—
69-68	IDE Secondary Sector Size	0200	RW
69-6F	-reserved-	00	—
70	IDE Primary Status	00	RW
71	IDE Primary Interrupt Control	00	RW
72-73	-reserved-	00	—
74	IDE Primary Command 1	00	RW
75	IDE Primary Command 2	00	RW
76-77	-reserved-	00	—
78	IDE Secondary Status	00	RW
79	IDE Secondary Interrupt Control	00	RW
7A-7B	-reserved-	00	—
7C	IDE Secondary Command 1	00	RW
7D	IDE Secondary Command 2	00	RW
7E-7F	-reserved-	00	—
83-80	IDE Primary S/G Descriptor Address	0000 0000	RW
84-87	-reserved-	00	—
8B-88	IDE Secondary S/G Descriptor Addr	0000 0000	RW
8C-97	-reserved-	00	—
99-98	IDE Configuration I/O Space	0000	RW
9A-FF	-reserved-	00	—

I/O Registers - IDE Controller (SFF 8038 v1.0 Compliant

Offset	IDE I/O Registers	Default	Acc
0	Primary Channel Command	00	RW
1	-reserved-	00	—
2	Primary Channel Status	00	WC
3	-reserved-	00	—
4-7	Primary Channel PRD Table Addr	00	RW
8	Secondary Channel Command	00	RW
9	-reserved-	00	—
A	Secondary Channel Status	00	WC
B	-reserved-	00	—
C-F	Secondary Channel PRD Table Addr	00	RW

PCI Function 2 Registers - USB Controller Ports 0-1

Configuration Space USB Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	3038	RO
5-4	Command	0000	**RW**
7-6	Status	0200	**WC**
8	Revision ID	nn	RO
9	Programming Interface	00	RO
A	Sub Class Code	03	RO
B	Base Class Code	0C	RO
C	Cache Line Size	00	RO
D	Latency Timer	16	**RW**
E	Header Type	00	RO
F	BIST	00	RO
10-1F	-reserved-	00	—
23-20	USB I/O Register Base Address	00000301	**RW**
24-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	04	**RO**
3E-3F	-reserved-	00	—

Configuration Space USB-Specific Registers

Offset	USB Control	Default	Acc
40	USB Miscellaneous Control 1	00	**RW**
41	USB Miscellaneous Control 2	00	**RW**
42-43	-reserved-	00	RO
44-45	-reserved- (test, do not program)		**RW**
46-47	-reserved- (test)		RO
48-5F	-reserved-	00	—
60	USB Serial Bus Release Number	10	RO
61-BF	-reserved-	00	—
C1-C0	USB Legacy Support	2000	**RW**
C2-FF	-reserved-	00	—

I/O Registers - USB Controller

Offset	USB I/O Registers	Default	Acc
1-0	USB Command	0000	RW
3-2	USB Status	0000	**WC**
5-4	USB Interrupt Enable	0000	RW
7-6	Frame Number	0000	RW
B-8	Frame List Base Address	00000000	RW
C	Start Of Frame Modify	40	RW
11-10	Port 0 Status / Control	0080	**WC**
13-12	Port 1 Status / Control	0080	**WC**
14-1F	-reserved-	00	—

PCI Function 3 Registers - USB Controller Ports 2-3

Configuration Space USB Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	3038	RO
5-4	Command	0000	**RW**
7-6	Status	0200	**WC**
8	Revision ID	nn	RO
9	Programming Interface	00	RO
A	Sub Class Code	03	RO
B	Base Class Code	0C	RO
C	Cache Line Size	00	RO
D	Latency Timer	16	**RW**
E	Header Type	00	RO
F	BIST	00	RO
10-1F	-reserved-	00	—
23-20	USB I/O Register Base Address	00000301	**RW**
24-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	04	**RO**
3E-3F	-reserved-	00	—

Configuration Space USB-Specific Registers

Offset	USB Control	Default	Acc
40	USB Miscellaneous Control 1	00	**RW**
41	USB Miscellaneous Control 2	00	**RW**
42-43	-reserved-	00	RO
44-45	-reserved- (test only, do not program)		**RW**
46-47	-reserved- (test)		RO
48-5F	-reserved-	00	—
60	USB Serial Bus Release Number	10	RO
61-BF	-reserved-	00	—
C1-C0	USB Legacy Support	2000	**RW**
C2-FF	-reserved-	00	—

I/O Registers - USB Controller

Offset	USB I/O Registers	Default	Acc
1-0	USB Command	0000	RW
3-2	USB Status	0000	**WC**
5-4	USB Interrupt Enable	0000	RW
7-6	Frame Number	0000	RW
B-8	Frame List Base Address	00000000	RW
C	Start Of Frame Modify	40	RW
11-10	Port 2 Status / Control	0080	**WC**
13-12	Port 3 Status / Control	0080	**WC**
14-1F	-reserved-	00	—

PCI Function 4 Registers - Power Management

Configuration Space Power Management Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	3068	RO
5-4	Command	0000	RO
7-6	Status	0280	**WC**
8	Revision ID	nn	RO
9	Programming Interface	00†	RO
A	Sub Class Code	00†	RO
B	Base Class Code	00†	RO
C	Cache Line Size	00	RO
D	Latency Timer	00	RO
E	Header Type	00	RO
F	BIST	00	RO
10-3F	-reserved-	00	—

† The default values for these registers may be changed by writing to offsets 61-63h (see below).

Configuration Space Power Management Registers

Offset	Power Management	Default	Acc
40	General Configuration 0	00	RW
41	General Configuration 1	00	RW
42	ACPI Interrupt Select	00	RW
43	Internal Timer Read Test	—	**RO**
45-44	Primary Interrupt Channel	0000	RW
47-46	Secondary Interrupt Channel	0000	RW
4B-48	**Power Mgmt I/O Base (256 Bytes)**	0000 0001	RW
4C	Host Bus Power Management Control	00	RW
4D	Throttle / Clock Stop Control	00	RW
4E-4F	-reserved-	00	—
53-50	GP Timer Control	0000 0000	RW
54	Power Well Control	00	RW
55-60	-reserved-	00	—
61	Write value for Offset 9 (Prog Intfc)	00	**WO**
62	Write value for Offset A (Sub Class)	00	**WO**
63	Write value for Offset B (Base Class)	00	**WO**
64-7F	-reserved-	00	—

Configuration Space Hardware Monitor Registers

Offset	System Management Bus	Default	Acc
71-70	**Hardware Mon IO Base (128 Bytes)**	0001	RW
72-73	-reserved-	00	—
74	Hardware Monitor Control	00	**RW**
75-8F	-reserved-	00	—

Configuration Space SMBus Registers

Offset	System Management Bus	Default	Acc
93-90	**SMBus I/O Base (16 Bytes)**	0000 0001	RW
94-D1	-reserved-	00	—
D2	SMBus Host Configuration	00	RW
D3	SMBus Host Slave Command	00	RW
D4	SMBus Slave Address Shadow Port 1	00	RW
D5	SMBus Slave Address Shadow Port 2	00	RW
D6	SMBus Revision ID	nn	**RO**
D7-FF	-reserved-	00	—

I/O Space Power Management- Registers

Offset	Basic Control / Status Registers	Default	Acc
1-0	Power Management Status	0000	**WC**
3-2	Power Management Enable	0000	RW
5-4	Power Management Control	0000	RW
6-7	-reserved-	00	—
B-8	Power Management Timer	0000 0000	RW
C-F	-reserved-	00	—
Offset	**Processor Registers**	**Default**	**Acc**
13-10	Processor and PCI Bus Control	0000 0000	RW
14	Processor LVL2	00	**RO**
15	Processor LVL3	00	**RO**
16-1F	-reserved-	00	—
Offset	**General Purpose Registers**	**Default**	**Acc**
21-20	General Purpose Status	0000	**WC**
23-22	General Purpose SCI Enable	0000	RW
25-24	General Purpose SMI Enable	0000	RW
26-27	-reserved-	00	—
Offset	**Generic Registers**	**Default**	**Acc**
29-28	Global Status	0000	**WC**
2B-2A	Global Enable	0000	RW
2D-2C	Global Control	0010	RW
2E	-reserved-	00	—
2F	SMI Command	00	RW
33-30	Primary Activity Detect Status	0000 0000	**WC**
37-34	Primary Activity Detect Enable	0000 0000	RW
3B-38	GP Timer Reload Enable	0000 0000	RW
3C-3F	-reserved-	00	—
Offset	**General Purpose I/O Registers**	**Default**	**Acc**
40-43	-reserved-	00	—
44	External SMI Input Value	input	**RO**
45	IRQ Resume Status	00	**RO**
46-47	-reserved-	00	—
4B-48	GPI Port Input Value	input	**RO**
4F-4C	GPO Port Output Value	03FF FFFF	RW
50-FF	-reserved-	00	—

I/O Space System Management Bus Registers

Offset	System Management Bus	Default	Acc
0	SMBus Host Status	00	**WC**
1	SMBus Slave Status	00	RW
2	SMBus Host Control	00	RW
3	SMBus Host Command	00	RW
4	SMBus Host Address	00	RW
5	SMBus Host Data 0	00	RW
6	SMBus Host Data 1	00	RW
7	SMBus Block Data	00	RW
8	SMBus Slave Control	00	RW
9	SMBus Shadow Command	00	**RO**
A-B	SMBus Slave Event	0000	RW
C-D	SMBus Slave Data	0000	**RO**
E-F	-reserved-	00	—

I/O Space Hardware Monitor Registers

Offset	Hardware Monitor	Default	Acc
00-3F	Value RAM		
00-1C	-reserved-	00	—
1D	TSENS3 Hot Hi Limit	00	RW
1E	TSENS3 Hot Hysteresis Lo Lim	00	RW
1F	TSENS3 (Int) Temp Reading	00	RW
20	TSENS1 (W13) Temp Reading	00	RW
21	TSENS2 (Y13) Temp Reading	00	RW
22	VSENS1 (U13) Voltage Reading	00	RW
23	VSENS2 (V13) Voltage Reading	00	RW
24	Internal Core VCC Voltage Reading	00	RW
25	VSENS3 (W14) Voltage Reading	00	RW
26	VSENS4 (Y14) Voltage Reading	00	RW
27-28	-reserved-	00	—
29	FAN1 (T12) Count Reading	00	RW
2A	FAN2 (U12) Count Reading	00	RW
2B	VSENS1 Voltage High Limit	00	RW
2C	VSENS1 Voltage Low Limit	00	RW
2D	VSENS2 Voltage High Limit	00	RW
2E	VSENS2 Voltage Low Limit	00	RW
2F	Internal Core VCC High Limit	00	RW
30	Internal Core VCC Low Limit	00	RW
31	VSENS3 Voltage High Limit	00	RW
32	VSENS3 Voltage Low Limit	00	RW
33	VSENS4 Voltage High Limit	00	RW
34	VSENS4 Voltage Low Limit	00	RW
35-38	-reserved-	00	—
39	TSENS1 Hot High Limit	00	RW
3A	TSENS1 Hot Hysteresis Lo Lim	00	RW
3B	FAN1 Fan Count Limit	00	RW
3C	FAN2 Fan Count Limit	00	RW
3D	TSENS2 Hot High Limit	00	RW
3E	TSENS2 Hot Hysteresis Lo Lim	00	RW
3F	Stepping ID Number	00	RW
40	Hardware Monitor Configuration	**08**	RW
41	Hardware Monitor Interrupt Status 1	00	**RO**
42	Hardware Monitor Interrupt Status 2	00	**RO**
43	Hardware Monitor Interrupt Mask 1	00	RW
44	Hardware Monitor Interrupt Mask 2	00	RW
45-46	-reserved-	00	—
47	Hardware Monitor Fan Configuration	**50**	RW
48	-reserved-	00	—
49	HW Mon Temp Value Lo-Order Bits	00	RW
4A	-reserved-	00	—
4B	Temperature Interrupt Configuration	**15**	RW
4C-FF	-reserved-	00	—

PCI Function 5 & 6 Registers – AC97 / MC97 Codecs

Function 5 Configuration Space AC97 Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	3058	RO
5-4	Command	0000	**RW**
7-6	Status	0200	**WC**
8	Revision ID	nn	RO
9	Programming Interface	00	RO
A	Sub Class Code	01	RO
B	Base Class Code	04	RO
C	Cache Line Size	00	RO
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	BIST	00	RO
13-10	Base Address 0 - SGD Control/Status	0000 0001	**RW**
17-14	Base Address 1 – FM NMI Status	0000 0001	**RW**
1B-18	Base Address 2 (reserved)	0000 0000	—
1F-1C	Base Address 3 (reserved)	0000 0000	—
23-20	Base Address 4 (reserved)	0000 0000	—
27-24	Base Address 5 (reserved)	0000 0000	—
28-2F	-reserved-	00	—
33-30	Expansion ROM (reserved)	0000 0000	—
34-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	03	RO
3E-3F	-reserved-	00	—

Function 6 Configuration Space MC97 Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	3068	RO
5-4	Command	0000	**RW**
7-6	Status	0200	**WC**
8	Revision ID	nn	RO
9	Programming Interface	00	RO
A	Sub Class Code	80	RO
B	Base Class Code	07	RO
C	Cache Line Size	00	RO
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	BIST	00	RO
13-10	Base Address 0 - SGD Control/Status	0000 0001	**RW**
17-14	Base Address 1 – FM NMI Status	0000 0001	**RW**
1B-18	Base Address 2 (reserved)	0000 0000	—
1F-1C	Base Address 3 (reserved)	0000 0000	—
23-20	Base Address 4 (reserved)	0000 0000	—
27-24	Base Address 5 (reserved)	0000 0000	—
28-2F	-reserved-	00	—
33-30	Expansion ROM (reserved)	0000 0000	—
34-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	03	RO
3E-3F	-reserved-	00	—

Configuration Space Audio Codec-Specific Registers

Offset	Audio Codec Link Control	Default	Acc
40	AC-Link Interface Status	00	**RO**
41	AC-Link Interface Control	00	RW
42	Function Enable	00	RW
43	Plug and Play Control	1C	RW
44	MC97 Interface Control	00	**RO**
45-47	-reserved-	00	—
48	FM NMI Control	00	**RO**
49-FF	-reserved-	00	—

Note that these registers are the same as function 6 except for offset 44 (Read / Write in function 6)

Configuration Space Modem Codec-Specific Registers

Offset	Modem Codec Link Control	Default	Acc
40	AC-Link Interface Status	00	**RO**
41	AC-Link Interface Control	00	RW
42	Function Enable	00	RW
43	Plug and Play Control	1C	RW
44	MC97 Interface Control	00	RW
45-47	-reserved-	00	—
48	FM NMI Control	00	**RO**
49-FF	-reserved-	00	—

Note that these registers are the same as function 5 except for offset 44 (Read Only in function 5)

I/O Registers (I/O Base 0) – AC97 Scatter-Gather DMA

Offset	AC97 SGD I/O Registers	Default	Acc
0	SGD Read Channel Status	00	**WC**
1	SGD Read Channel Control	00	RW
2	SGD Type	00	RW
3	Reserved	00	—
7-4	SGD Read Chan Table Pointer Base SGD Read Channel Current Address	0000 0000	WR RD
B-8	Reserved (Test)	0000 0000	**RO**
F-C	SGD Read Chan Current Count	0000 0000	**RO**
10	SGD Write Channel Status	00	**WC**
11	SGD Write Channel Control	00	RW
12	SGD Type	00	RW
13	Reserved	00	—
17-14	SGD Write Chan Table Pointer Base SGD Write Channel Current Address	0000 0000	WR RD
1B-18	Reserved (Test)	0000 0000	**RO**
1F-1C	SGD Write Channel Current Count	0000 0000	**RO**
20	SGD FM Channel Status	00	**WC**
21	SGD FM Channel Control	00	RW
22	SGD FM Type	00	RW
23	Reserved	00	—
27-24	SGD FM Channel Table Pointer Base SGD FM Channel Current Address	0000 0000	WR RD
2B-28	Reserved (Test)	0000 0000	**RO**
2F-2C	SGD FM Channel Current Count	0000 0000	**RO**
30-3F	Reserved	00	—

The above registers are writable from **function 5 only**. They are Read / Only in **function 6**

I/O Registers (I/O Base 0) – MC97 Scatter-Gather DMA

Offset	MC97 SGD I/O Registers	Default	Acc
40	SGD Read Channel Status	00	**WC**
41	SGD Read Channel Control	00	RW
42	SGD Type	00	RW
43	Reserved	00	—
47-44	SGD Read Chan Table Pointer Base SGD Read Channel Current Address	0000 0000	WR RD
4B-48	Reserved (Test)	0000 0000	**RO**
4F-4C	SGD Read Chan Current Count	0000 0000	**RO**
50	SGD Write Channel Status	00	**WC**
51	SGD Write Channel Control	00	RW
52	SGD Type	00	RW
53	Reserved	00	—
57-54	SGD Write Chan Table Pointer Base SGD Write Channel Current Address	0000 0000	WR RD
5B-58	Reserved (Test)	0000 0000	**RO**
5F-5C	SGD Write Channel Current Count	0000 0000	**RO**
60-7F	Reserved	00	—

The above registers are writable from **function 6 only**. They are Read / Only in **function 5**

Offset	AC97 Controller I/O Registers	Default	Acc
83-80	AC97 Controller Command / Status	0000 0000	RW
87-84	SGD Status Shadow	0000 0000	**RO**

The above registers are writable from **both function 5 and function 6**.

Offset	AC97 Controller I/O Registers	Default	Acc
8B-88	Codec GPI Interrupt Status / GPIO	0000 0000	**WC**
8F-8C	Codec GPI Interrupt Enable	0000 0000	RW
90-FF	Reserved	00	—

The above registers are writable from **function 6 only**. They are Read / Only in **function 5**

I/O Registers (I/O Base 1) – FM NMI Status

Offset	FM NMI Status Registers	Default	Acc
0	FM NMI Status	00	**RO**
1	FM NMI Data	00	**RO**
2	FM NMI Index	00	**RO**
3	Reserved	00	—

The above registers are accessable through **function 5** only.

I/O Registers – SoundBlaster Pro

Offset	SB Pro Registers (220 or 240h typ)	Default	Acc
0	FM Left Channel Index / Status		RW
1	FM Left Channel Data		**WO**
2	FM Right Channel Index / Status		RW
3	FM Right Channel Data		**WO**
4	Mixer Index		**WO**
5	Mixer Data		RW
6	Sound Processor Reset		**WO**
7	-reserved-	00	--
8	FM Index / Status (Both Channels)		RW
9	FM Data (Both Channels)		**WO**
A	Sound Processor Data		**RO**
B	-reserved-	00	--
C	Sound Processor Command / Data Sound Processor Buffer Status		WR RD
D	-reserved-	00	--
E	Snd Processor Data Available Status		**RO**
F	-reserved-	00	--

Port	SB Pro Regs (same as offsets 8 & 9)	Default	Acc
388h	FM Index / Status		RW
389h	FM Data		**WO**

The above group of registers emulates the “FM”, “Mixer”, and “Sound Processor” functions of the SoundBlaster Pro.

I/O Registers – Game Port

Offset	Game Port (200-20F typical)	Default	Acc
0	-reserved-	00	--
1	Game Port Status		**RO**
1	Start One-Shot		**WO**
2-F	-reserved-	00	--

Register Descriptions

Configuration Space I/O

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address .....RW

31 Configuration Space Enable
- 0 Disabled .....default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved ..... always reads 0

23-16 PCI Bus Number
Used to choose a specific PCI bus in the system

15-11 Device Number
Used to choose a specific device in the system

10-8 Function Number
Used to choose a specific function if the selected device supports multiple functions

7-2 Register Number
Used to select a specific DWORD in the device's configuration space

1-0 Fixed ..... always reads 0

Port CFF-CFC - Configuration Data .....RW

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

Legacy I/O Ports

This group of registers includes the DMA Controllers, Interrupt Controllers, and Timer/Counters as well as a number of miscellaneous ports originally implemented using discrete logic on original PC/AT motherboards. All of the registers listed are integrated on-chip. These registers are implemented in a precise manner for backwards compatibility with previous generations of PC hardware. These registers are listed for information purposes only. Detailed descriptions of the actions and programming of these registers are included in numerous industry publications (duplication of that information here is beyond the scope of this document). All of these registers reside in I/O space.

Port 61 - Misc Functions & Speaker Control..... RW

7 Reserved .....always reads 0

6 IOCHCK# Active .....RO
This bit is set when the ISA bus IOCHCK# signal is asserted. Once set, this bit may be cleared by setting bit-3 of this register. Bit-3 should be cleared to enable recording of the next IOCHCK#. IOCHCK# generates NMI to the CPU if NMI is enabled.

5 Timer/Counter 2 Output.....RO
This bit reflects the output of Timer/Counter 2 without any synchronization.

4 Refresh Detected.....RO
This bit toggles on every rising edge of the ISA bus REFRESH# signal.

3 IOCHCK# Disable.....RW
- 0 Enable IOCHCK# assertions ..... default
- 1 Force IOCHCK# inactive and clear any "IOCHCK# Active" condition in bit-6

2 Reserved .....RW, default=0

1 Speaker Enable.....RW
- 0 Disable..... default
- 1 Enable Timer/Ctr 2 output to drive SPKR pin

0 Timer/Counter 2 Enable .....RW
- 0 Disable..... default
- 1 Enable Timer/Counter 2

Port 92h - System Control..... RW

7-6 Hard Disk Activity LED Status
- 0 Off ..... default
- 1-3 On

5-4 Reserved .....always reads 0

3 Power-On Password Bytes Inaccessable ..default=0

2 Reserved .....always reads 0

1 A20 Address Line Enable
- 0 A20 disabled / forced 0 (real mode) ..... default
- 1 A20 address line enabled

0 High Speed Reset
- 0 Normal
- 1 Briefly pulse system reset to switch from protected mode to real mode

Keyboard Controller Registers

The keyboard controller handles the keyboard and mouse interfaces. Two ports are used: port 60 and port 64. Reads from port 64 return a status byte. Writes to port 64h are command codes (see command code list following the register descriptions). Input and output data is transferred via port 60.

A "Control" register is also available. It is accessable by writing commands 20h / 60h to the command port (port 64h); The control byte is written by first sending 60h to the command port, then sending the control byte value. The control register may be read by sending a command of 20h to port 64h, waiting for "Output Buffer Full" status = 1, then reading the control byte value from port 60h.

Traditional (non-integrated) keyboard controllers have an "Input Port" and an "Output Port" with specific pins dedicated to certain functions and other pins available for general purpose I/O. Specific commands are provided to set these pins high and low. All outputs are "open-collector" so to allow input on one of these pins, the output value for that pin would be set high (non-driving) and the desired input value read on the input port. These ports are defined as follows:

Bit	Input Port	Lo Code	Hi Code
0	P10 - Keyboard Data In	B0	B8
1	P11 - Mouse Data In	B1	B9
2	P12 - Turbo Pin (PS/2 mode only)	B2	BA
3	P13 - user-defined	B3	BB
4	P14 - user-defined	B6	BE
5	P15 - user-defined	B7	BF
6	P16 - user-defined	–	–
7	P17 - undefined	–	–

Bit	Output Port	Lo Code	Hi Code
0	P20 - SYSRST (1=execute reset)	–	–
1	P21 - GATEA20 (1=A20 enabled)	–	–
2	P22 - Mouse Data Out	B4	BC
3	P23 - Mouse Clock Out	B5	BD
4	P24 - Keyboard OBF Interrupt (IRQ1)	–	–
5	P25 - Mouse OBF Interrupt (IRQ 12)	–	–
6	P26 - Keyboard Clock Out	–	–
7	P27 - Keyboard Data Out	–	–

Bit	Test Port	Lo Code	Hi Code
0	T0 - Keyboard Clock In	–	–
1	T1 - Mouse Clock In	–	–

Note: Command code C0h transfers input port data to the output buffer. Command code D0h copies output port values to the output buffer. Command code E0h transfers test input port data to the output buffer.

Port 60 - Keyboard Controller Input Buffer ..... WO

Only write to port 60h if port 64h bit-1 = 0 (1=full).

Port 60 - Keyboard Controller Output Buffer .....RO

Only read from port 60h if port 64h bit-0 = 1 (0=empty).

Port 64 - Keyboard / Mouse Status ..... RO

7 Parity Error
- 0 No parity error (odd parity received)..... default
- 1 Even parity occurred on last byte received from keyboard / mouse

6 General Receive / Transmit Timeout
- 0 No error ..... default
- 1 Error

5 Mouse Output Buffer Full
- 0 Mouse output buffer empty..... default
- 1 Mouse output buffer holds mouse data

4 Keylock Status
- 0 Locked
- 1 Free

3 Command / Data
- 0 Last write was data write ..... default
- 1 Last write was command write

2 System Flag
- 0 Power-On Default..... default
- 1 Self Test Successful

1 Input Buffer Full
- 0 Input Buffer Empty..... default
- 1 Input Buffer Full

0 Keyboard Output Buffer Full
- 0 Keyboard Output Buffer Empty..... default
- 1 Keyboard Output Buffer Full

KBC Control Register .....(R/W via Commands 20h/60h)

7 Reserved .....always reads 0

6 PC Compatibility
- 0 Disable scan conversion
- 1 Convert scan codes to PC format; convert 2-byte break sequences to 1-byte PC-compatible break codes ..... default

5 Mouse Disable
- 0 Enable Mouse Interface ..... default
- 1 Disable Mouse Interface

4 Keyboard Disable
- 0 Enable Keyboard Interface ..... default
- 1 Disable Keyboard Interface

3 Keyboard Lock Disable
- 0 Enable Keyboard Inhibit Function..... default
- 1 Disable Keyboard Inhibit Function

2 System Flag .....default=0

This bit may be read back as status register bit-2

1 Mouse Interrupt Enable
- 0 Disable mouse interrupts ..... default
- 1 Generate interrupt on IRQ12 when mouse data comes in output bufer

0 Keyboard Interrupt Enable
- 0 Disable Keyboard Interrupts..... default
- 1 Generate interrupt on IRQ1 when output buffer has been written.

Port 64 - Keyboard / Mouse Command..... WO

This port is used to send commands to the keyboard / mouse controller. The command codes recognized by the VT82C686A are listed n the table below.

Note: The VT82C686A Keyboard Controller is compatible with the VIA VT82C42 Industry-Standard Keyboard Controller except that due to its integrated nature, many of the input and output port pins are not available externally for use as general purpose I/O pins (even though P13-P16 are set on power-up as strapping options). In other words, many of the commands below are provided and "work", but otherwise perform no useful function (e.g., commands that set P12-P17 high or low). Also note that setting P10-11, P22-23, P26-27, and T0-1 high or low directly serves no useful purpose, since these bits are used to implement the keyboard and mouse ports and are directly controlled by keyboard controller logic.

Table 4. Keyboard Controller Command Codes

Code	Keyboard Command Code Description
20h	Read Control Byte (next byte is Control Byte)
21-3Fh	Read SRAM Data (next byte is Data Byte)
60h	Write Control Byte (next byte is Control Byte)
61-7Fh	Write SRAM Data (next byte is Data Byte)
9xh	Write low nibble (bits 0-3) to P10-P13
A1h	Output Keyboard Controller Version #
A4h	Test if Password is installed (always returns F1h to indicate not installed)
A7h	Disable Mouse Interface
A8h	Enable Mouse Interface
A9h	Mouse Interface Test (puts test results in port 60h) (value: 0=OK, 1=clk stuck low, 2=clk stuck high, 3=data stuck lo, 4=data stuck hi, FF=general error)
AAh	KBC self test (returns 55h if OK, FCh if not)
ABh	Keyboard Interface Test (see A9h Mouse Test)
ADh	Disable Keyboard Interface
AEh	Enable Keyboard Interface
AFh	Return Version #
B0h	Set P10 low
B1h	Set P11 low
B2h	Set P12 low
B3h	Set P13 low
B4h	Set P22 low
B5h	Set P23 low
B6h	Set P14 low
B7h	Set P15 low
B8h	Set P10 high
B9h	Set P11 high
BAh	Set P12 high
BBh	Set P13 high
BCh	Set P22 high
BDh	Set P23 high
BEh	Set P14 high
BFh	Set P15 high
C0h	Read input port (read P10-17 input data to the output buffer)
C1h	Poll input port low (read input data on P11-13 repeatably & put in bits 5-7 of status
C2h	Poll input port high (same except P15-17)
C8h	Unblock P22-23 (use before D1 to change active mode)
C9h	Reblock P22-23 (protection mechanism for D1)
CAh	Read mode (output KBC mode info to port 60 output buffer (bit-0=0 if ISA, 1 if PS/2)
D0h	Read Output Port (copy P10-17 output port values to port 60)
D1h	Write Output Port (data byte following is written to keyboard output port as if it came from keyboard)
D2h	Write Keyboard Output Buffer & clear status bit-5 (write following byte to keyboard)
D3h	Write Mouse Output Buffer & set status bit-5 (write following byte to mouse; put value in mouse input buffer so it appears to have come from the mouse)
D4h	Write Mouse (write following byte to mouse)
E0h	Read test inputs (T0-1 read to bits 0-1 of resp byte)
Exh	Set P23-P21 per command bits 3-1
Fxh	Pulse P23-P20 low for 6usec per command bits 3-0

All other codes not listed are undefined.

DMA Controller I/O Registers

Ports 00-0F - Master DMA Controller

Channels 0-3 of the Master DMA Controller control System DMA Channels 0-3. There are 16 Master DMA Controller registers:

I/O Address Bits 15-0	Register Name	
0000 0000 000x 0000	**Ch 0 Base / Current Address**	**RW**
0000 0000 000x 0001	**Ch 0 Base / Current Count**	**RW**
0000 0000 000x 0010	**Ch 1 Base / Current Address**	**RW**
0000 0000 000x 0011	**Ch 1 Base / Current Count**	**RW**
0000 0000 000x 0100	**Ch 2 Base / Current Address**	**RW**
0000 0000 000x 0101	**Ch 2 Base / Current Count**	**RW**
0000 0000 000x 0110	**Ch 3 Base / Current Address**	**RW**
0000 0000 000x 0111	**Ch 3 Base / Current Count**	**RW**
0000 0000 000x 1000	**Status / Command**	**RW**
0000 0000 000x 1001	**Write Request**	**WO**
0000 0000 000x 1010	**Write Single Mask**	**WO**
0000 0000 000x 1011	**Write Mode**	**WO**
0000 0000 000x 1100	**Clear Byte Pointer F/F**	**WO**
0000 0000 000x 1101	**Master Clear**	**WO**
0000 0000 000x 1110	**Clear Mask**	**WO**
0000 0000 000x 1111	**R/W All Mask Bits**	**RW**

Ports C0-DF - Slave DMA Controller

Channels 0-3 of the Slave DMA Controller control System DMA Channels 4-7. There are 16 Slave DMA Controller registers:

I/O Address Bits 15-0	Register Name	
0000 0000 1100 000x	**Ch 4 Base / Current Address**	**RW**
0000 0000 1100 001x	**Ch 4 Base / Current Count**	**RW**
0000 0000 1100 010x	**Ch 5 Base / Current Address**	**RW**
0000 0000 1100 011x	**Ch 5 Base / Current Count**	**RW**
0000 0000 1100 100x	**Ch 6 Base / Current Address**	**RW**
0000 0000 1100 101x	**Ch 6 Base / Current Count**	**RW**
0000 0000 1100 110x	**Ch 7 Base / Current Address**	**RW**
0000 0000 1100 111x	**Ch 7 Base / Current Count**	**RW**
0000 0000 1101 000x	**Status / Command**	**RW**
0000 0000 1101 001x	**Write Request**	**WO**
0000 0000 1101 010x	**Write Single Mask**	**WO**
0000 0000 1101 011x	**Write Mode**	**WO**
0000 0000 1101 100x	**Clear Byte Pointer F/F**	**WO**
0000 0000 1101 101x	**Master Clear**	**WO**
0000 0000 1101 110x	**Clear Mask**	**WO**
0000 0000 1101 111x	**Read/Write All Mask Bits**	**WO**

Note that not all bits of the address are decoded.

The Master and Slave DMA Controllers are compatible with the Intel 8237 DMA Controller chip. Detailed description of 8237 DMA controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Ports 80-8F - DMA Page Registers

There are eight DMA Page Registers, one for each DMA channel. These registers provide bits 16-23 of the 24-bit address for each DMA channel (bits 0-15 are stored in registers in the Master and Slave DMA Controllers). They are located at the following I/O Port addresses:

I/O Address Bits 15-0	Register Name	
0000 0000 1000 0111	**Channel 0 DMA Page (M-0).....**	**RW**
0000 0000 1000 0011	**Channel 1 DMA Page (M-1).....**	**RW**
0000 0000 1000 0001	**Channel 2 DMA Page (M-2).....**	**RW**
0000 0000 1000 0010	**Channel 3 DMA Page (M-3).....**	**RW**
0000 0000 1000 1111	**Channel 4 DMA Page (S-0) .....**	**RW**
0000 0000 1000 1011	**Channel 5 DMA Page (S-1) .....**	**RW**
0000 0000 1000 1001	**Channel 6 DMA Page (S-2) .....**	**RW**
0000 0000 1000 1010	**Channel 7 DMA Page (S-3) .....**	**RW**

DMA Controller Shadow Registers

The DMA Controller shadow registers are enabled by setting function 0 Rx77 bit 0. If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard DMA controller registers (writes are unchanged).

Port 0 –Channel 0 Base Address ..... RO
Port 1 –Channel 0 Byte Count..... RO
Port 2 –Channel 1 Base Address ..... RO
Port 3 –Channel 1 Byte Count..... RO
Port 4 –Channel 2 Base Address ..... RO
Port 5 –Channel 2 Byte Count..... RO
Port 6 –Channel 3 Base Address ..... RO
Port 7 –Channel 3 Byte Count..... RO

Port 8 –1st Read Channel 0-3 Command Register ..... RO
Port 8 –2nd Read Channel 0-3 Request Register..... RO
Port 8 –3rd Read Channel 0 Mode Register..... RO
Port 8 –4th Read Channel 1 Mode Register ..... RO
Port 8 –5th Read Channel 2 Mode Register ..... RO
Port 8 –6th Read Channel 3 Mode Register ..... RO

Port F –Channel 0-3 Read All Mask ..... RO

Port C4 –Channel 5 Base Address..... RO
Port C6 –Channel 5 Byte Count ..... RO
Port C8 –Channel 6 Base Address..... RO
Port CA –Channel 6 Byte Count ..... RO
Port CC –Channel 7 Base Address..... RO
Port CE –Channel 7 Byte Count ..... RO

Port D0 –1st Read Channel 4-7 Command Register..... RO
Port D0 –2nd Read Channel 4-7 Request Register..... RO
Port D0 –3rd Read Channel 4 Mode Register ..... RO
Port D0 –4th Read Channel 5 Mode Register ..... RO
Port D0 –5th Read Channel 6 Mode Register ..... RO
Port D0 –6th Read Channel 7 Mode Register ..... RO

Port DE –Channel 4-7 Read All Mask..... RO

Interrupt Controller Registers

Ports 20-21 - Master Interrupt Controller

The Master Interrupt Controller controls system interrupt channels 0-7. Two registers control the Master Interrupt Controller. They are:

I/O Address Bits 15-0	Register Name	
0000 0000 001x xxx0	**Master Interrupt Control**	**RW**
0000 0000 001x xxx1	**Master Interrupt Mask**	**RW**

Note that not all bits of the address are decoded.

The Master Interrupt Controller is compatible with the Intel 8259 Interrupt Controller chip. Detailed descriptions of 8259 Interrupt Controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Ports A0-A1 - Slave Interrupt Controller

The Slave Interrupt Controller controls system interrupt channels 8-15. The slave system interrupt controller also occupies two register locations:

I/O Address Bits 15-0	Register Name	
0000 0000 101x xxx0	**Slave Interrupt Control**	**RW**
0000 0000 101x xxx1	**Slave Interrupt Mask**	**RW**

Note that not all address bits are decoded.

The Slave Interrupt Controller is compatible with the Intel 8259 Interrupt Controller chip. Detailed descriptions of 8259 Interrupt Controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Interrupt Controller Shadow Registers

The following shadow registers are enabled by setting function 0 Rx47[4]. If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard interrupt controller registers (writes are unchanged).

Port 20 - Master Interrupt Control Shadow ..... RO
Port A0 - Slave Interrupt Control Shadow ..... RO

- **7 Reserved** ..... always reads 0
- **6 OCW3 bit 2 (POLL)**
- **5 OCW3 bit 0 (RIS)**
- **4 OCW3 bit 5 (SMM)**
- **3 OCW2 bit 7 (R)**
- **2 ICW4 bit 4 (SFNM)**
- **1 ICW4 bit 1 (AEOI)**
- **0 ICW1 bit 3 (LTIM)**

Port 21 - Master Interrupt Mask Shadow ..... RO
Port A1 - Slave Interrupt Mask Shadow ..... RO

- **7-5 Reserved** ..... always reads 0
- **4-0 T7-T3 of Interrupt Vector Address**

Timer / Counter Registers

Ports 40-43 - Timer / Counter Registers

There are 4 Timer / Counter registers:

I/O Address Bits 15-0	Register Name	
0000 0000 010x xx00	**Timer / Counter 0 Count**	**RW**
0000 0000 010x xx01	**Timer / Counter 1 Count**	**RW**
0000 0000 010x xx10	**Timer / Counter 2 Count**	**RW**
0000 0000 010x xx11	**Timer / Counter Cmd Mode**	**WO**

Note that not all bits of the address are decoded.

The Timer / Counters are compatible with the Intel 8254 Timer / Counter chip. Detailed descriptions of 8254 Timer / Counter operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Timer / Counter Shadow Registers

The following shadow registers are enabled for readback by setting function 0 Rx47[4]. If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard timer / counter registers (writes are unchanged).

Port 40 – Counter 0 Base Count Value (LSB 1st MSB 2nd)RO
Port 41 – Counter 1 Base Count Value (LSB 1st MSB 2nd)RO
Port 42 – Counter 2 Base Count Value (LSB 1st MSB 2nd)RO

CMOS / RTC Registers

Port 70 - CMOS Address.....RW

7 NMI Disable..... RW
- 0 Enable NMI Generation. NMI is asserted on encountering IOCHCK# on the ISA bus or SERR# on the PCI bus.
- 1 Disable NMI Generation .....default

6-0 CMOS Address (lower 128 bytes)..... RW

Port 71 - CMOS Data.....RW

7-0 CMOS Data (128 bytes)

Note: Ports 70-71 may be accessed if Rx5A bit-2 is set to one to select the internal RTC. If Rx5A bit-2 is set to zero, accesses to ports 70-71 will be directed to an external RTC.

Port 72 - CMOS Address.....RW

7-0 CMOS Address (256 bytes)..... RW

Port 73 - CMOS Data.....RW

7-0 CMOS Data (256 bytes)

Note: Ports 72-73 may be accessed if Rx5A bit-2 is set to one to select the internal RTC. If Rx5A bit-2 is set to zero, accesses to ports 72-73 will be directed to an external RTC.

Port 74 - CMOS Address.....RW

7-0 CMOS Address (256 bytes)..... RW

Port 75 - CMOS Data.....RW

7-0 CMOS Data (256 bytes)

Note: Ports 74-75 may be accessed only if Function 0 Rx5B bit-1 is set to one to enable the internal RTC SRAM and if Rx48 bit-3 (Port 74/75 Access Enable) is set to one to enable port 74/75 access.

Note: Ports 70-71 are compatible with PC industry-standards and may be used to access the lower 128 bytes of the 256-byte on-chip CMOS RAM. Ports 72-73 may be used to access the full extended 256-byte space. Ports 74-75 may be used to access the full on-chip extended 256-byte space in cases where the on-chip RTC is disabled.

Note: The system Real Time Clock (RTC) is part of the "CMOS" block. The RTC control registers are located at specific offsets in the CMOS data area (0-0Dh and 7D-7Fh). Detailed descriptions of CMOS / RTC operation and programming can be obtained from the VIA VT82887 Data Book or numerous other industry publications. For reference, the definition of the RTC register locations and bits are summarized in the following table:

Offset	Description		Binary Range	BCD Range
00	**Seconds**		00-3Bh	00-59h
01	**Seconds Alarm**		00-3Bh	00-59h
02	**Minutes**		00-3Bh	00-59h
03	**Minutes Alarm**		00-3Bh	00-59h
04	**Hours**	am 12hr:	01-1Ch	01-12h
		pm 12hr:	81-8Ch	81-92h
		24hr:	00-17h	00-23h
05	**Hours Alarm**	am 12hr:	01-1Ch	01-12h
		pm 12hr:	81-8Ch	81-92h
		24hr:	00-17h	00-23h
06	**Day of the Week**	Sun=1:	01-07h	01-07h
07	**Day of the Month**		01-1Fh	01-31h
08	**Month**		01-0Ch	01-12h
09	**Year**		00-63h	00-99h

0A Register A

7	**UIP**	Update In Progress
6-4	**DV2-0**	Divide (010=ena osc & keep time)
3-0	**RS3-0**	Rate Select for Periodic Interrupt

0B Register B

7	**SET**	Inhibit Update Transfers
6	**PIE**	Periodic Interrupt Enable
5	**AIE**	Alarm Interrupt Enable
4	**UIE**	Update Ended Interrupt Enable
3	**SQWE**	No function (read/write bit)
2	**DM**	Data Mode (0=BCD, 1=binary)
1	**24/12**	Hours Byte Format (0=12, 1=24)
0	**DSE**	Daylight Savings Enable

0C Register C

7	**IRQF**	Interrupt Request Flag
6	**PF**	Periodic Interrupt Flag
5	**AF**	Alarm Interrupt Flag
4	**UF**	Update Ended Flag
3-0	**0**	Unused (always read 0)

0D Register D

7	**VRT**	Reads 1 if VBAT voltage is OK
6-0	**0**	Unused (always read 0)

0E-7C Software-Defined Storage Registers (111 Bytes)

Offset	Extended Functions	Binary Range	BCD Range
7D	**Date Alarm**	01-1Fh	01-31h
7E	**Month Alarm**	01-0Ch	01-12h
7F	**Century Field**	13-14h	19-20h

80-FF Software-Defined Storage Registers (128 Bytes)

Table 5. CMOS Register Summary

Super-I/O Configuration Index Registers

Super-I/O configuration registers are accessed by performing I/O operations to/from an index / data pair of registers in system I/O space at port addresses 3F0h and 3F1h. The configuration registers accessed using this mechanism are used to configure the Super-I/O registers (parallel port, serial ports, IR port, and floppy controller).

Super-I/O Configuration Index / Data Registers

Port 3F0h – Super-I/O Configuration Index.....RW

7-0 Index value

Function 0 PCI configuration space register Rx85[1] must be set to 1 to enable access to the Super-I/O configuration registers.

Port 3F1h – Super-I/O Configuration Data.....RW

7-0 Data value

This register shares a port with the Floppy Status Port (which is read only). This port is accessible only when Rx85[1] is set to 1 (the floppy status port is accessed if Rx85[1] = 0).

Super-I/O Configuration Registers

These registers are accessed via the port 3F0/3F1 index / data register pair using the indicated index values below

Index E0 – Super-I/O Device ID.....RO

7-0 Super-I/O ID ..... default = 3Ch

Index E1 – Super-I/O Device Revision.....RO

7-0 Super-I/O Revision Code .....default = 0

Index E2 – Super-I/O Function Select .....RW

7-5 Reserved .....always reads 0

4 Floppy Controller Enable
- 0 Disable..... default
- 1 Enable

3 Serial Port 2 Enable
- 0 Disable..... default
- 1 Enable

2 Serial Port 1 Enable
- 0 Disable..... default
- 1 Enable

1-0 Parallel Port Mode / Enable
- 00 Unidirectional mode ..... default
- 01 ECP
- 10 EPP
- 11 Parallel Port Disabled

Index E3 – Floppy Controller I/O Base Address .....RW

7-2 I/O Address 9-4.....default = 0
1-0 Must be 0 .....default = 0

Index E6 – Parallel Port I/O Base Address .....RW

7-0 I/O Address 9-2.....default = 0

If EPP is not enabled, the parallel port can be set to 192 locations on 4-byte boundaries from 100h to 3FCh. If EPP is enabled, the parallel port can be set to 96 locations on 8-byte boundaries from 100h to 3F8h.

Index E7 – Serial Port 1 I/O Base Address.....RW

7-1 I/O Address 9-3.....default = 0
0 Must be 0 .....default = 0

Index E8 – Serial Port 2 I/O Base Address.....RW

7-1 I/O Address 9-3.....default = 0
0 Must be 0 .....default = 0

Index EE – Serial Port Configuration .....RW

7 Serial Port 2 High Speed Enable
- 0 Disable .....default
- 1 Enable

6 Serial Port 1 High Speed Enable
- 0 Disable .....default
- 1 Enable

5-3 Serial Port 2 Mode
- 000 Standard
- 001 IrDA (HIPSIR)
- 010 Amplitude shift keyed IR @ 500KHz
- 011 -reserved-
- 1xx -reserved-

2 Serial Port 2 Half Duplex
- 0 Disable .....default
- 1 Enable

1 Serial Port 2 TX Output Inversion
- 0 Disable .....default
- 1 Enable

0 Serial Port 2 RX Input Inversion
- 0 Disable .....default
- 1 Enable

Index EF – Power Down Control.....RW

7-6 Reserved ..... always reads 0

5 Clock Power Down
- 0 Normal operation .....default
- 1 Power Down

4 Parallel Port Power Down
- 0 Normal operation .....default
- 1 Power Down

3 Serial Port 2 Power Down
- 0 Normal operation .....default
- 1 Power Down

2 Serial Port 1 Power Down
- 0 Normal operation .....default
- 1 Power Down

1 FDC Power Down
- 0 Normal operation .....default
- 1 Power Down

0 All Power Down
- 0 Normal operation .....default
- 1 Power Down All

Index F0 – Parallel Port Printer Control..... RW

7 PIO Bit-5 Enable in PIO Mode
- 0 Disable..... default
- 1 Enable

6 EPP Direction by Register not by IOW
- 0 Disable..... default
- 1 Enable

5 EPP+ECP
- 0 Disable..... default
- 1 Enable

4 SPP Version
- 0 Version 1.9 ..... default
- 1 Not Version 1.9

3 Reserved .....always reads 0

2 IRQ Polarity

1-0 Reserved .....always reads 0

Index F1 – Serial Port Control ..... RW

7-6 Reserved .....always reads 0

5 IR Loop Back
- 0 Disable..... default
- 1 Enable

4 Serial Port 2 Power-Down State
- 0 Normal..... default
- 1 Tristate output in power down mode

3 Serial Port 1 Power-Down State
- 0 Normal..... default
- 1 Tristate output in power down mode

2-0 Reserved .....always reads 0

Index F2 – Test Mode (Do Not Program) ..... RW

Index F4 – Test Mode (Do Not Program) ..... RW

Index F6 – Floppy Controller Configuration.....RW

- **7-5 Reserved** ..... always reads 0
- **4 3-Mode FDD**
  - 0 Disable .....default
  - 1 Enable
- **3 Reserved** ..... always reads 0
- **2 Four Floppy Drive Option**
  - 0 Internal 2-Drive Decoder .....default
  - 1 External 4-Drive Decoder
- **1 FDC DMA Non-Burst**
  - 0 Burst .....default
  - 1 Non-Burst
- **0 FDC Swap**
  - 0 Disable .....default
  - 1 Enable

Index F8 – Floppy Drive Control ..... RW

- **7-6 Floppy Drive 3** (see table below)
- **5-4 Floppy Drive 2** (see table below)
- **3-2 Floppy Drive 1** (see table below)
- **1-0 Floppy Drive 0** (see table below)

	DRVEN1	DRVEN0
00	SENSEL	DRATE0
01	DRATE1	DRATE0
10	SENSEL#	DRATE0
11	DRATE1	DRATE0

Super-I/O I/O Ports

Floppy Disk Controller Registers

These registers are located at I/O ports which are offsets from "FDCBase" (index C3h of the Super-I/O configuration registers). FDCBase is typically set to allow these ports to be accessed at the standard floppy disk controller address range of 3F0-3F7h.

Port FDCBase+1 – FDC Status A .....RO

- **7 Interrupt Pending**
  - 0 Interrupt inactive
  - 1 Interrupt signal active
- **6 # of Drives**
  - 0 Two drives connected
  - 1 One drive connected
- **5 Step Pulse**
  - 0 Not transferred
  - 1 Transferred
- **4 Track 00**
  - 0 Head currently not at track 00
  - 1 Head currently at track 00
- **3 Head Selected**
  - 0 Head 0
  - 1 Head 1
- **2 Index Mark**
  - 0 Index mark detected
  - 1 Index mark not detected
- **1 Write Protection Status**
  - 0 Disk Write Protected
  - 1 Disk not write protected
- **0 Step Direction of Head**
  - 0 Outward (to smaller cylinder numbers)
  - 1 Inward (to higher cylinder numbers)

Port FDCBase+1 – FDC Status B .....RO

- **7-6 Unused** .....always read 1
- **5 Drive Selected**
  - 0 Other drive selected
  - 1 Drive 0 selected
- **4 Write Data**
  - 0 Data has been transmitted to drive
  - 1 No data written
- **3 Read Data**
  - 0 Data has been transmitted from drive
  - 1 No data read
- **2 Write Enable**
  - 0 Head can read data only
  - 1 Head activated for writing
- **1 Motor 1 Status**
  - 0 Motor is off
  - 1 Motor is on
- **0 Motor 0 Status**
  - 0 Motor is off
  - 1 Motor is on

Port FDCBase+2 – FDC Command ..... RW

- **7 Motor 3 (unused in VT82C686A: no MTR3# pin)**
- **6 Motor 2 (unused in VT82C686A: no MTR2# pin)**
- **5 Motor 1**
  - 0 Motor Off
  - 1 Motor On
- **4 Motor 0**
  - 0 Motor Off
  - 1 Motor On
- **3 DMA and IRQ Channels**
  - 0 Disabled
  - 1 Enabled
- **2 FDC Reset**
  - 0 Execute FDC Reset
  - 1 FDC Enabled
- **1-0 Drive Select**
  - 00 Select Drive 0
  - 01 Select Drive 1
  - 1x -reserved-

Port FDCBase+4 – FDC Main Status ..... RO

- **7 Main Request**
  - 0 Data register not ready
  - 1 Data register ready
- **6 Data Input / Output**
  - 0 CPU => FDC
  - 1 FDC => CPU
- **5 Non-DMA Mode**
  - 0 FDC in DMA mode
  - 1 FDC not in DMA mode
- **4 FDC Busy**
  - 0 FDC inactive
  - 1 FDC active
- **3-2 Reserved** .....always reads 0
- **1 Drive 1 Active**
  - 0 Drive inactive
  - 1 Drive performing a positioning change
- **0 Drive 0 Active**
  - 0 Drive inactive
  - 1 Drive performing a positioning change

Port FDCBase+4 – FDC Data Rate Select ..... WO

Port FDCBase+5 – FDC Data .....RW

Port FDCBase+7 – FDC Disk Change Status .....RO

7 Disk Change
- 0 Floppy not changed
- 1 Floppy changed since last instruction

6-3 Undefined .....always read 1

2-1 Data Rate
- 00 500 Kbit/sec (1.2MB 5” or 1.44 MB 3” drive)
- 01 300 Kbit/sec (360KB 5” drive)
- 10 250 Kbit/sec (720KB 3” drive)
- 11 1 Mbit/sec

0 High Density Rate
- 0 500 Kbit/sec or 1 Mbit/sec selected
- 1 250 Kbit/set or 300 Kbit/sec selected

Port FDCBase+7 – FDC Configuration Control.....WO

7-2 Undefined ..... always read 1

1-0 Data Rate
- 00 500 Kbit/sec (1.2MB 5” or 1.44 MB 3” drive)
- 01 300 Kbit/sec (360KB 5” drive)
- 10 250 Kbit/sec (720KB 3” drive)
- 11 1 Mbit/sec

Parallel Port Registers

These registers are located at I/O ports which are offsets from "LPTBase" (index C6h of the Super-I/O configuration registers). LPTBase is typically set to allow these ports to be accessed at the standard parallel port address range of 378-37Fh.

Port LPTBase+0 – Parallel Port Data .....RW

7-0 Parallel Port Data

Port LPTBase+1 – Parallel Port Status.....RO

7 BUSY#
- 0 Printer busy, offline, or error
- 1 Printer not busy

6 ACK#
- 0 Data transfer to printer complete
- 1 Data transfer to printer in progress

5 PE
- 0 Paper available
- 1 No paper available

4 SLCT
- 0 Printer offline
- 1 Printer online

3 ERROR#
- 0 Printer error
- 1 Printer OK

2-0 Reserved ..... always read 1 bits

Port LPTBase+2 – Parallel Port Control..... RW

7-5 Undefined ..... always read back 1

4 Hardware Interrupt
- 0 Disable..... default
- 1 Enable

3 Printer Select
- 0 Deselect printer..... default
- 1 Select printer

2 Printer Initialize
- 0 Initialize Printer ..... default
- 1 Allow printer to operate normally

1 Automatic Line Feed
- 0 Host handles line feeds ..... default
- 1 Printer does automatic line feeds

0 Strobe
- 0 No data transfer ..... default
- 1 Transfer data to printer

Port LPTBase+3 – Parallel Port EPP Address..... RW

Port LPTBase+4 – Parallel Port EPP Data Port 0..... RW

Port LPTBase+5 – Parallel Port EPP Data Port 1..... RW

Port LPTBase+6 – Parallel Port EPP Data Port 2..... RW

Port LPTBase+7 – Parallel Port EPP Data Port 3..... RW

Port LPTBase+400h – Parallel Port ECP Data / Cfg A RW

Port LPTBase+401h – Parallel Port ECP Config B..... RW

Port LPTBase+401h – Parallel Port ECP Extd Ctrl..... RW

Serial Port 1 Registers

These registers are located at I/O ports which are offsets from "COM1Base" (index C7h of the Super-I/O configuration registers). COM1Base is typically set to allow these ports to be accessed at the standard serial port 1 address range of 3F8-3FFh.

Port COM1Base+0 – Transmit / Receive Buffer .....RW

7-0 Serial Data

Port COM1Base+1 – Interrupt Enable .....RW

7-4 Undefined .....always read 0
3 Interrupt on Hnadshake Input State Change
2 Intr on Parity, Overrun, Framing Error or Break
1 Interrupt on Transmit Buffer Empty
0 Interrupt on Receive Data Ready

Port COM1Base+2 – Interrupt Status .....RO

7-3 Undefined .....always read 0
2-1 Interrupt ID (0=highest priority)
00 Priority 3 (Handshake Input Changed State)
01 Priority 2 (Transmit Buffer Empty)
10 Priority 1 (Data Received)
11 Priority 0 (Serialization Error or Break)
0 Interrupt Pending
0 Interrupt Pending
1 No Interrupt Pending

Port COM1Base+2 – FIFO Control ..... WO

Port COM1Base+3 – UART Control.....RW

7 Divisor Latch Access
0 Select transmit / receive registers
1 Select divisor latch
6 Break
0 Break condition off
1 Break condition on
5-3 Parity
000 None
001 Odd
011 Even
101 Mark
111 Space
2 Stop Bits
0 1
1 2
1-0 Data Bits
00 5
01 6
10 7
11 8

Port COM1Base+4 – Handshake Control ..... RW

7-5 Undefined ..... always read 0
4 Loopback Check
0 Normal operation
1 Loopback enabled
3 General Purpose Output 2 (unused in 82C686A)
2 General Purpose Output 1 (unused in 82C686A)
1 Request To Send
0 Disabled
1 Enabled
0 Data Terminal Ready
0 Disabled
1 Enabled

Port COM1Base+5 – UART Status..... RW

7 Undefined ..... always read 0
6 Transmitter Empty
0 1 byte in transmit hold or transmit shift register
1 0 bytes transmit hold and transmit shift regs
5 Transmit Buffer Empty
0 1 byte in transmit hold register
1 Transmit hold register empty
4 Break Detected
0 No break detected
1 Break detected
3 Framing Error Detected
0 No error
1 Error
2 Parity Error Detected
0 No error
1 Error
1 Overrun Error Detected
0 No error
1 Error
0 Received Data Ready
0 No received data available
1 Received data in receiver buffer register

Port COM1Base+6 – Handshake Status..... RW

7 DCD Status (1=Active, 0=Inactive)
6 RI Status (1=Active, 0=Inactive)
5 DSR Status (1=Active, 0=Inactive)
4 CTS Status (1=Active, 0=Inactive)
3 DCD Changed (1=Changed Since Last Read)
2 RI Changed (1=Changed Since Last Read)
1 DSR Changed (1=Changed Since Last Read)
0 CTS Changed (1=Changed Since Last Read)

Port COM1Base+7 – Scratchpad ..... RW

7 Scratchpad Data

Port COM1Base+9-8 – Baud Rate Generator Divisor .. RW

15-0 Divisor Value for Basud Rate Generator
Baud Rate = 115,200 / Divisor
(e.g., setting this register to 1 selects 115.2 Kbaud)

Serial Port 2 Registers

These registers are located at I/O ports which are offsets from "COM2Base" (index C8h of the Super-I/O configuration registers). COM2Base is typically set to allow these ports to be accessed at the standard serial port 2 address range of 2F8-2FFh.

Port COM1Base+0 – Transmit / Receive Buffer .....RW

7-0 Serial Data

Port COM1Base+1 – Interrupt Enable .....RW

7-4 Undefined .....always read 0
3 Interrupt on Hnadshake Input State Change
2 Intr on Parity, Overrun, Framing Error or Break
1 Interrupt on Transmit Buffer Empty
0 Interrupt on Receive Data Ready

Port COM1Base+2 – Interrupt Status .....RO

7-3 Undefined .....always read 0
2-1 Interrupt ID (0=highest priority)
00 Priority 3 (Handshake Input Changed State)
01 Priority 2 (Transmit Buffer Empty)
10 Priority 1 (Data Received)
11 Priority 0 (Serialization Error or Break)
0 Interrupt Pending
0 Interrupt Pending
1 No Interrupt Pending

Port COM1Base+2 – FIFO Control ..... WO

Port COM1Base+3 – UART Control.....RW

7 Divisor Latch Access
0 Select transmit / receive registers
1 Select divisor latch
6 Break
0 Break condition off
1 Break condition on
5-3 Parity
000 None
001 Odd
011 Even
101 Mark
111 Space
2 Stop Bits
0 1
1 2
1-0 Data Bits
00 5
01 6
10 7
11 8

Port COM1Base+4 – Handshake Control ..... RW

7-5 Undefined ..... always read 0
4 Loopback Check
0 Normal operation
1 Loopback enabled
3 General Purpose Output 2 (unused in 82C686A)
2 General Purpose Output 1 (unused in 82C686A)
1 Request To Send
0 Disabled
1 Enabled
0 Data Terminal Ready
0 Disabled
1 Enabled

Port COM1Base+5 – UART Status..... RW

7 Undefined ..... always read 0
6 Transmitter Empty
0 1 byte in transmit hold or transmit shift register
1 0 bytes transmit hold and transmit shift regs
5 Transmit Buffer Empty
0 1 byte in transmit hold register
1 Transmit hold register empty
4 Break Detected
0 No break detected
1 Break detected
3 Framing Error Detected
0 No error
1 Error
2 Parity Error Detected
0 No error
1 Error
1 Overrun Error Detected
0 No error
1 Error
0 Received Data Ready
0 No received data available
1 Received data in receiver buffer register

Port COM1Base+6 – Handshake Status..... RW

7 DCD Status (1=Active, 0=Inactive)
6 RI Status (1=Active, 0=Inactive)
5 DSR Status (1=Active, 0=Inactive)
4 CTS Status (1=Active, 0=Inactive)
3 DCD Changed (1=Changed Since Last Read)
2 RI Changed (1=Changed Since Last Read)
1 DSR Changed (1=Changed Since Last Read)
0 CTS Changed (1=Changed Since Last Read)

Port COM1Base+7 – Scratchpad ..... RW

7 Scratchpad Data

Port COM1Base+9-8 – Baud Rate Generator Divisor .. RW

15-0 Divisor Value for Basud Rate Generator
Baud Rate = 115,200 / Divisor
(e.g., setting this register to 1 selects 115.2 Kbaud)

SoundBlaster Pro Port Registers

These registers are located at offsets from "SBPBase" (defined in Rx43 of Audio Function 5 PCI configuration space). SBPBase is typically set to allow these ports to be accessed at the standard SoundBlaster Pro port address of 220h or 240h.

FM Registers

Port SBPBase+0 – FM Left Channel Index / Status.....RW

7-0 FM Right Channel Index / Status

Port SBPBase+1 – FM Left Channel Data..... WO

7-0 Right Channel FM Data

Port SBPBase+2 – FM Right Channel Index / Status ....RW

7-0 FM Right Channel Index / Status

Port SBPBase+3 – FM Right Channel Data ..... WO

7-0 Right Channel FM Data

Port 388h or SBPBase+8 – FM Index / Status.....RW

7-0 FM Index / Status (Both Channels)

Writing to this port programs both the left and right channels (the write programms port offsets 0 and 2 as well)

Port 389h or SBPBase+9 – FM Data ..... WO

7-0 FM Data (Both Channels)

Writing to this port programs both the left and right channels (the write programms port offsets 1 and 3 as well)

Mixer Registers

Port SBPBase+4 – Mixer Index..... WO

7-0 Mixer Index

Port SBPBase+5 – Mixer Data.....RW

7-0 Mixer Data

Sound Processor Registers

Port SBPBase+6 – Sound Processor Reset ..... WO

0 1 = Sound Processor Reset

Port SBPBase+A – Sound Processor Read Data .....RO

7-0 Sound Processor Read Data

Port SBPBase+C – Sound Processor Command / Data WO

7-0 Sound Processor Command / Write Data

Port SBPBase+C – Sound Processor Buffer Status.....RO

7 1 = Sound Processor Command / Data Port Busy

Port SBPBase+E – Sound Processor Data Avail Status..RO

7 1 = Sound Processor Data Available

Register Summary - FM

Index	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
01	Test							
02	Fast Counter (80 usec)							
03	Slow Counter (320 usec)							
04	IRQ	MFC	MSC				SSSC	SSFC
08	CSM	SEL						
20-35	AM	VIB	EGT	KSR	Multi			
40-55	KSL		Total Level (TL)					
60-75	Attack Rate (AR)				Decay Rate (DR)			
80-95	Sustain Level (SL)				Release Rate (RR)			
A0-A8	F-Number							
B0-B8			Key	Block			F-Number	
BD	Int AM VIB		Ryth	Bass	Snare	Tom	Cym	HiHat
C0-C8					Feedback			FM
E0-F5							WS	

MFC=Mask Fast Counter SSFC=Start / Stop Fast Counter
MSC=Mask Slow Counter SSSC=Start / Stop Slow Counter

Register Summary – Mixer

Index	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
00	Data Reset							
02	SP Volume L				SP Volume R			
0A						Mic Vol		
0C			Finp		TFIL	Select		
0E			Fout				ST	
22	General Volume				General Volume			
26	FM Volume L				FM Volume R			
28	CD Volume L				CD Volume R			
2E	Line Volume L				Line Volume R			

Finp = Input Filter
Fout = Output Filter
TFIL = Input Filter Type
ST = Stereo / Mono Mode
Select = Input Choices (0=Microphone, 1=CD, 3=Line)

Command Summary – Sound Processor (see next page)

Command Summary – Sound Processor

#	Type	Command
10	Play	8 bits directly
14	Play	8 bits via DMA
91	Play	High-speed 8 bits via DMA
16	Play	2-bit compressed via DMA
17	Play	2-bit compressed via DMA with reference
74	Play	4-bit compressed via DMA
75	Play	4-bit compressed via DMA with reference
76	Play	2.6-bit compressed via DMA
77	Play	2.6-bit compressed via DMA with reference
20	Record	Direct
24	Record	Via DMA
99	Record	High-speed 8 bits via DMA
D1	Speaker	Turn on speaker connection
D3	Speaker	Turn off speaker connection
D8	Speaker	Get speaker setting
40	Misc	Set sample rate
48	Misc	Set block length
80	Misc	Set silence block
D0	Misc	Stop DMA
D4	Misc	Continue DMA
E1	Misc	Get version
30	MIDI	Direct MIDI input
31	MIDI	MIDI input via interrupt
32	MIDI	Direct MIDI input with time stamp
33	MIDI	MIDI input via interrupt with time stamp
34	MIDI	Direct MIDI UART mode
35	MIDI	MIDI UART mode via interrupt
36	MIDI	Direct MIDI UART mode with time stamp
37	MIDI	MIDI UART mode via interrupt with time stamp
38	MIDI	Send MIDI code

Game Port Registers

These registers are fixed at the standard game port address of 201h.

I/O Port 201h – Game Port Status ..... RO

- **7 Joystick B Button 2 Status**
- **6 Joystick B Button 1 Status**
- **5 Joystick A Button 2 Status**
- **4 Joystick A Button 1 Status**
- **3 Joystick B One-Shot Status for Y-Potentiometer**
- **2 Joystick B One-Shot Status for X-Potentiometer**
- **1 Joystick A One-Shot Status for Y-Potentiometer**
- **0 Joystick A One-Shot Status for X-Potentiometer**

I/O Port 201h – Start One-Shot..... WO

7-0 (Value Written is Ignored)

Function 0 Registers - PCI to ISA Bridge

All registers are located in the function 0 PCI configuration space of the VT82C686A. These registers are accessed through PCI configuration mechanism #1 via I/O address CF8/CFC.

PCI Configuration Space Header

Offset 1-0 - Vendor ID = 1106h ..... RO

Offset 3-2 - Device ID = 0686h ..... RO

Offset 5-4 - Command ..... RW

- **15-8 Reserved** ..... always reads 0
- **7 Address / Data Stepping**
  - 0 Disable
  - 1 Enable ..... default
- **6-4 Reserved** ..... always reads 0
- **3 Special Cycle Enable** ..... Normally RW†, default = 0
- **2 Bus Master** ..... always reads 1
- **1 Memory Space** ..... Normally RO†, reads as 1
- **0 I/O Space** ..... Normally RO†, reads as 1

† If the test bit at offset 46 bit-4 is set, access to the above indicated bits is reversed: bit-3 above becomes read only (reading back 1) and bits 0-1 above become read / write (with a default of 1).

Offset 7-6 - Status ..... RWC

- **15 Detected Parity Error** ..... write one to clear
- **14 Signalled System Error** ..... always reads 0
- **13 Signalled Master Abort** ..... write one to clear
- **12 Received Target Abort** ..... write one to clear
- **11 Signalled Target Abort** ..... write one to clear
- **10-9 DEVSEL# Timing** ..... fixed at 01 (medium)
- **8 Data Parity Detected** ..... always reads 0
- **7 Fast Back-to-Back** ..... always reads 0
- **6-0 Reserved** ..... always reads 0

Offset 8 - Revision ID = nn ..... RO

- **7-0 Revision ID**
  - 0x VT82C686
  - 1x VT82C686A

Offset 9 - Program Interface = 00h ..... RO

Offset A - Sub Class Code = 01h ..... RO

Offset B - Class Code = 06h ..... RO

Offset E - Header Type = 80h ..... RO

- **7-0 Header Type Code** ..... 80h (Multifunction Device)

Offset F - BIST = 00h ..... RO

Offset 2F-2C - Subsystem ID ..... RO

Use offset 70-73 to change the value returned.

ISA Bus Control

Offset 40 - ISA Bus Control ..... RW

- **7 ISA Command Delay**
  - 0 Normal ..... default
  - 1 Extra
- **6 Extended ISA Bus Ready**
  - 0 Disable ..... default
  - 1 Enable
- **5 ISA Slave Wait States**
  - 0 4 Wait States ..... default
  - 1 5 Wait States
- **4 Chipset I/O Wait States**
  - 0 2 Wait States ..... default
  - 1 4 Wait States
- **3 I/O Recovery Time**
  - 0 Disable ..... default
  - 1 Enable
- **2 Extend-ALE**
  - 0 Disable ..... default
  - 1 Enable
- **1 ROM Wait States**
  - 0 1 Wait State ..... default
  - 1 0 Wait States
- **0 ROM Write**
  - 0 Disable ..... default
  - 1 Enable

Offset 41 - ISA Test Mode ..... RW

- **7 Bus Refresh Arbitration** (do not program) default=0
- **6 XRDY Test Mode** (do not program) ..... default=0
- **5 Port 92 Fast Reset**
  - 0 Disable ..... default
  - 1 Enable
- **4 A20G Emulation** (do not program) ..... default=0
- **3 Double DMA Clock**
  - 0 Disable (DMA Clock = ½ ISA Clock)... default
  - 1 Enable (DMA Clock = ISA Clock)
- **2 SHOLD Lock During INTA** (do not program) def=0
- **1 Refresh Request Test Mode** (do not program). def=0
- **0 ISA Refresh**
  - 0 Disable ..... default
  - 1 Enable

  This bit should be set to 1 for ISA compatibility.

Offset 42 - ISA Clock Control. .....RW

7 Latch IO16#
- 0 Enable (recommended setting) .....default
- 1 Disable

6 MCS16# Output
- 0 Disable .....default
- 1 Enable

5 Master Request Test Mode (do not program)
- 0 Disable .....default
- 1 Enable

4 Reserved (Do Not Program) ..... default = 0

3 ISA Clock (BCLK) Select Enable
- 0 BCLK = PCICLK/4.....default
- 1 BCLK selected per bits 2-0

2-0 ISA Bus Clock Select (if bit-3 = 1)
- 000 BCLK = PCICLK/3.....default
- 001 BCLK = PCICLK/2
- 010 BCLK = PCICLK/4
- 011 BCLK = PCICLK/6
- 100 BCLK = PCICLK/5
- 101 BCLK = PCICLK/10
- 110 BCLK = PCICLK/12
- 111 BCLK = OSC/2

Note: Procedure for ISA Clock switching:
1) Set bit 3 to 0; 2) Change value of bit 2-0; 3) Set bit 3 to 1

Offset 43 - ROM Decode Control..... RW

Setting these bits enables the indicated address range to be included in the ROMCS# decode:

7 FFFE0000h-FFFEFFFFh .....default=0
6 FFF80000h-FFFDFFFFh .....default=0
5 000E8000h-000EFFFFh .....default=0
4 000E0000h-000E7FFFh .....default=0
3 000D8000h-000DFFFFh .....default=0
2 000D0000h-000D7FFFh .....default=0
1 000C8000h-000CFFFFh .....default=0
0 000C0000h-000C7FFFh.....default=0

Offset 44 - Keyboard Controller Control ..... RW

7 KBC Timeout Test (do not program).....default = 0
6-4 Reserved (do not program).....default = 0
3 Mouse Lock Enable
- 0 Disable..... default
- 1 Enable

2-1 Reserved (do not program).....default = 0
0 Reserved (no function) .....default = 0

Offset 45 - Type F DMA Control ..... RW

7 ISA Master / DMA to PCI Line Buffer
- 0 Disable..... default
- 1 Enable

6 DMA type F Timing on Channel 7.....default=0
5 DMA type F Timing on Channel 6.....default=0
4 DMA type F Timing on Channel 5.....default=0
3 DMA type F Timing on Channel 3.....default=0
2 DMA type F Timing on Channel 2.....default=0
1 DMA type F Timing on Channel 1.....default=0
0 DMA type F Timing on Channel 0.....default=0

Offset 46 - Miscellaneous Control 1.....RW

7 PCI Master Write Wait States
- 0 0 Wait States .....default
- 1 1 Wait State

6 Gate INTR
- 0 Disable .....default
- 1 Enable

5 Flush Line Buffer for Int or DMA IOR Cycle
- 0 Disable .....default
- 1 Enable

4 Config Command Reg Rx04 Access (Test Only)
- 0 Normal: Bits 0-1=RO, Bit 3=RW.....default
- 1 Test Mode: Bits 0-1=RW, Bit-3=RO

3 Reserved (do not program)..... default = 0

2 Reserved (no function)..... default = 0

1 PCI Burst Read Interruptability
- 0 Allow burst reads to be interrupted by ISA master or DMA.....default
- 1 Don't allow PCI burst reads to be interrupted

0 Posted Memory Write Enable
- 0 Disable .....default
- 1 Enable

The Posted Memory Write function is automatically enabled when Delay Transaction (see Rx47 bit-6 below) is enabled, independent of the state of this bit.

Offset 47 - Miscellaneous Control 2 ..... RW

7 CPU Reset Source
- 0 Use CPURST as CPU Reset..... default
- 1 Use INIT as CPU Reset

6 PCI Delay Transaction Enable
- 0 Disable..... default
- 1 Enable

The "Posted Memory Write" function is automatically enabled when this bit is enabled, independent of the state of Rx46 bit-0.

5 EISA 4D0/4D1 Port Enable
- 0 Disable (ignore ports 4D0-1)..... default
- 1 Enable (ports 4D0-1 per EISA specification)

4 Interrupt Controller Shadow Register Enable
- 0 Disable..... default
- 1 Enable (for test purposes, enable readback of interrupt controller internal functions on I/O reads from ports 20-21, A0-A1, A8-A9, and C8-C9) (Contact VIA Test Engineering department)

3 Reserved (always program to 0).....default = 0

Note: Always mask this bit. This bit may read back as either 0 or 1 but must always be programmed with 0.

2 Write Delay Transaction Time-Out Timer
- 0 Disable..... default
- 1 Enable

1 Read Delay Transaction Time-Out Timer
- 0 Disable..... default
- 1 Enable

0 Software PCI Reset .....write 1 to generate PCI reset

Offset 48 - Miscellaneous Control 3.....RW

7-4 Reserved ..... always reads 0

3 Extra RTC Port 74/75 Enable
- 0 Disable .....default
- 1 Enable

2 Integrated USB Controller Disable
- 0 Enable.....default
- 1 Disable

1 Integrated IDE Controller Disable
- 0 Enable.....default
- 1 Disable

0 512K PCI Memory Decode
- 0 Use Rx4E[15-12] to select top of PCI memory
- 1 Use contents of Rx4E[15-12] plus 512K as top of PCI memory.....default

Offset 4A - IDE Interrupt Routing .....RW

7 Wait for PGNT Before Grant to ISA Master / DMA
- 0 Disable .....default
- 1 Enable

6 Bus Select for Access to I/O Devices Below 100h
- 0 Access ports 00-FFh via XD bus.....default
- 1 Access ports 00-FFh via SD bus (applies to external devices only; internal devices such as the mouse controller are not effected)

5-4 Reserved (do not program) ..... default = 0

3-2 IDE Second Channel IRQ Routing
- 00 IRQ14
- 01 IRQ15.....default
- 10 IRQ10
- 11 IRQ11

1-0 IDE Primary Channel IRQ Routing
- 00 IRQ14.....default
- 01 IRQ15
- 10 IRQ10
- 11 IRQ11

4C - ISA DMA/Master Memory Access Control 1 ..... RW

7-0 PCI Memory Hole Bottom Address
These bits correspond to HA[23:16] .....default=0

4D - ISA DMA/Master Memory Access Control 2 ..... RW

7-0 PCI Memory Hole Top Address (HA[23:16])
These bits correspond to HA[23:16] .....default=0

Note: Access to the memory defined in the PCI memory hole will not be forwarded to PCI. This function is disabled if the top address is less than or equal to the bottom address.

4F-4E - ISA DMA/Master Memory Access Control 3... RW

15-12 Top of PCI Memory for ISA DMA/Master accesses
- 0000 1M ..... default
- 0001 2M
- ... ...
- 1111 16M

Note: All ISA DMA / Masters that access addresses higher than the top of PCI memory will not be directed to the PCI bus.

11 Forward E0000-EFFFF Accesses to PCI.....def=0
10 Forward A0000-BFFFF Accesses to PCI .....def=0
9 Forward 80000-9FFFF Accesses to PCI .....def=1
8 Forward 00000-7FFF Accesses to PCI .....def=1
7 Forward DC000-DFFFF Accesses to PCI .....def=0
6 Forward D8000-DBFFF Accesses to PCI .....def=0
5 Forward D4000-D7FFF Accesses to PCI .....def=0
4 Forward D0000-D3FFF Accesses to PCI .....def=0
3 Forward CC000-CFFFF Accesses to PCI .....def=0
2 Forward C8000-CBFFF Accesses to PCI .....def=0
1 Forward C4000-C7FFF Accesses to PCI .....def=0
0 Forward C0000-C3FFF Accesses to PCI .....def=0

Plug and Play Control

Offset 50 – PNP DMA Request Control.....RW

7-4 Reserved ..... default = 0
3-2 PnP Routing for Parallel Port DRQ.....def = DRQ3
1-0 PnP Routing for Floppy DRQ.....def = DRQ2

DRQ Mapping: 00=DRQ0, 01=DRQ1, 10=DRQ2, 11=DRQ3

Offset 51 - PNP IRQ Routing 1.....RW

7-4 PnP Routing for Parallel Port IRQ (see PnP IRQ routing table)
3-0 PnP Routing for Floppy IRQ (see PnP IRQ routing table)

Offset 52 - PNP IRQ Routing 2.....RW

7-4 PnP Routing for Serial Port 2 IRQ (see PnP IRQ routing table)
3-0 PnP Routing for Serial Port 1 IRQ (see PnP IRQ routing table)

Offset 54 - PCI IRQ Edge / Level Select.....RW

7-4 Reserved ..... always reads 0
The following bits all default to "level" triggered (0)
3 PIRQA# Invert (edge) / Non-invert (level).....(1/0)
2 PIRQB# Invert (edge) / Non-invert (level).....(1/0)
1 PIRQC# Invert (edge) / Non-invert (level).....(1/0)
0 PIRQD# Invert (edge) / Non-invert (level).....(1/0)

Note: PIRQA-D# normally connect to PCI interrupt pins INTA-D# (see pin definitions for more information).

Offset 55 - PNP IRQ Routing 4.....RW

7-4 PIRQA# Routing (see PnP IRQ routing table)
3-0 Reserved ..... always reads 0

Offset 56 - PNP IRQ Routing 5.....RW

7-4 PIRQC# Routing (see PnP IRQ routing table)
3-0 PIRQB# Routing (see PnP IRQ routing table)

Offset 57 - PNP IRQ Routing 6.....RW

7-4 PIRQD# Routing (see PnP IRQ routing table)
3-0 Reserved ..... always reads 0

PnP IRQ Routing Table

0000 Disabled..... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 Reserved
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 Reserved
1110 IRQ14
1111 IRQ15

Offset 5A – KBC / RTC Control .....RW

Bits 7-4 of this register are latched from pins SD7-4 at power-up but are read/write accessible so may be changed after power-up to change the default strap setting:

- **7** **Keyboard RP16** ..... latched from SD7
- **6** **Keyboard RP15** ..... latched from SD6
- **5** **Keyboard RP14** ..... latched from SD5
- **4** **Keyboard RP13** ..... latched from SD4
- **3** **Audio Function Enable**
  ..... RO, strapped from SPKR pin V5
  - 0 Disable (SDD pins function as SDD)
  - 1 Enable (SDD pins function as Audio / Game)
- **2** **Internal RTC Enable**
  - 0 Disable
  - 1 Enable .....default
- **1** **Internal PS2 Mouse Enable**
  - 0 Disable .....default
  - 1 Enable
- **0** **Internal KBC Enable**
  - 0 Disable .....default
  - 1 Enable

Note: External strap option values may be set by connecting the indicated external pin to a 4.7K ohm pullup (for 1) or driving it low during reset with a 7407 TTL open collector buffer (for 0) as shown in the suggested circuit below:

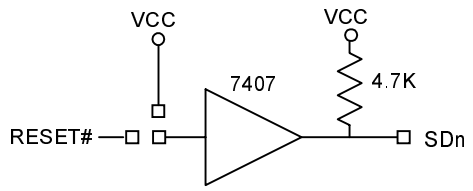

Figure 5. Strap Option Circuit

Offset 5B - Internal RTC Test Mode ..... RW

- **7-3** **Reserved** .....always reads 0
- **2** **RTC Reset Enable** (do not program) .....default=0
- **1** **RTC SRAM Access Enable**
  - 0 Disable..... default
  - 1 Enable

  This bit is set if the internal RTC is disabled but it is desired to still be able to access the internal RTC SRAM via ports 74-75. If the internal RTC is enabled, setting this bit does nothing (the internal RTC SRAM should be accessed at either ports 70/71 or 72/73.
- **0** **RTC Test Mode Enable** (do not program) .default=0

Offset 5C - DMA Control..... RW

- **7** **Reserved** .....always reads 0
- **6** **Passive Release**
  - 0 Disable..... default
  - 1 Enable
- **5** **Internal Passive Release**
  - 0 Disable..... default
  - 1 Enable
- **4** **Dummy PREQ**
  - 0 Disable..... default
  - 1 Enable
- **3** **Reserved** .....always reads 0
- **2** **APIC Connection**
  - 0 APIC on SD Bus..... default
  - 1 APIC on XD Bus
- **1** **Reserved (Do Not Program)** .....default = 0
- **0** **DMA Line Buffer Disable**
  - 0 DMA cycles can be to/from line buffer ..... def
  - 1 Disable DMA Line Buffer

Distributed DMA / Serial IRQ Control

Offset 61-60 - Distributed DMA Ch 0 Base / Enable.....RW

15-4 Channel 0 Base Address Bits 15-4 ..... default = 0

3 Channel 0 Enable

0 Disable .....default

1 Enable

2-0 Reserved ..... always reads 0

Offset 63-62 - Distributed DMA Ch 1 Base / Enable.....RW

15-4 Channel 1 Base Address Bits 15-4 ..... default = 0

3 Channel 1 Enable

0 Disable .....default

1 Enable

2-0 Reserved ..... always reads 0

Offset 65-64 - Distributed DMA Ch 2 Base / Enable.....RW

15-4 Channel 2 Base Address Bits 15-4 ..... default = 0

3 Channel 2 Enable

0 Disable .....default

1 Enable

2-0 Reserved ..... always reads 0

Offset 67-66 - Distributed DMA Ch 3 Base / Enable.....RW

15-4 Channel 3 Base Address Bits 15-4 ..... default = 0

3 Channel 3 Enable

0 Disable .....default

1 Enable

2-0 Reserved ..... always reads 0

Offset 69-68 – Serial IRQ Control .....RW

15-4 Reserved ..... always reads 0

3 Serial IRQ Enable

0 Disable .....default

1 Enable

2 Serial IRQ Mode

0 Continuous Mode .....default

1 Quiet Mode

1-0 Serial IRQ Start-Frame Width

00 4 PCI Clocks .....default

01 6 PCI Clocks

10 8 PCI Clocks

11 -reserved-

The frame size is fixed at 21 PCI clocks.

Offset 6B-6A - Distributed DMA Ch 5 Base / Enable.... RW

15-4 Channel 5 Base Address Bits 15-4.....default = 0

3 Channel 5 Enable

0 Disable..... default

1 Enable

2-0 Reserved .....always reads 0

Offset 6D-6C - Distributed DMA Ch 6 Base / Enable ... RW

15-4 Channel 6 Base Address Bits 15-4.....default = 0

3 Channel 6 Enable

0 Disable..... default

1 Enable

2-0 Reserved .....always reads 0

Offset 6F-6E - Distributed DMA Ch 7 Base / Enable .... RW

15-4 Channel 7 Base Address Bits 15-4.....default = 0

3 Channel 7 Enable

0 Disable..... default

1 Enable

2-0 Reserved .....always reads 0

Miscellaneous / General Purpose I/O

Offset 73-70 - Subsystem ID ..... WO

31-0 Subsystem ID / Vendor ID..... always reads 0
Contents may be read at offset 2C.

Offset 74 – GPIO Control 1.....RW

7 APIC Enable
0 Disable .....default
1 Enable

6 Reserved ..... always reads 0

5 GPIOD Direction (Pin U8)
0 Input .....default
1 Output

4 GPIOC Direction (Pin V14)
0 Input .....default
1 Output

3 GPIOB Direction (Pin U12)
0 Input .....default
1 Output

2 GPIOA Direction (Pin T14)
0 Input .....default
1 Output

1 THRM Enable (Pin T11)
0 PME# .....default
1 THRM
Note that pin T11 is also used as GPI5 whose value is reflected in Function 4 Rx48[5].

0 GPI0 / IOCHCK# Select
0 GPI0 .....default
1 IOCHCK#

Offset 75 – GPIO Control 2.....RW

7 GPO7 Enable (Pin T7)
0 Pin defined as SLP# .....default
1 Pin defined as GPO7

6 GPO6 Enable (Pin V10)
0 Pin defined as SUSST1# .....default
1 Pin defined as GPO6

5 GPO5 Enable (Pin V12)
0 Pin defined as PCISTP# .....default
1 Pin defined as GPO5

4 GPO4 Enable (Pin Y12)
0 Pin defined as CPUSTP# .....default
1 Pin defined as GPO4

3 FDC External IRQ / DRQ Interface
0 Enable.....default
1 Disable

2 GPO2 Enable (Pin W9)
0 Pin defined as SUSB# .....default
1 Pin defined as GPO2

1 GPO1 Enable (Pin V9)
0 Pin defined as SUSA# .....default
1 Pin defined as GPO1

0 Positive Decode
0 Subtractive Decode .....default
1 Positive Decode

Offset 76 – GPIO Control 3 ..... RW

7 Over-Current (OC) Input
0 Disable..... default
1 Enable

6 OC[3:0] From SD[3:0] By Scan
0 Disable..... default
1 Enable

5 GPO14 / GPO15 Enable (Pins E12 / D12)
0 Pins used for IRTX and IRRX..... default
1 Pins used for GPO14 and GPO15

4 PCS0# Enable (Pin T5)
Bit-1 = 0: pin is defined as XDIR (this bit is ignored)
Bit-1 = 1: pin is defined per this bit:
0 Pin is defined as GPO12..... defaul;t
1 Pin is defined as PCS0#

3 MCCS# Enable (Pin U5)
Bit-1 = 0: pin is defined as SOE# (this bit is ignored)
Bit-1 = 1: pin is defined per this bit:
0 Pin is defined as GPO13..... default
1 Pin is defined as MCCS#

2 CHAS Enable (Pin V14)
0 Pin is defined as GPIOC..... default
1 Pin is defined as CHAS

1 GPO12 / GPO13 Enable (Pins T5 / U5)
0 Pins are defined as XDIR and SOE# ..... default
1 Pins are defined per bits 3 and 4:
Bit-4 = 0: Pin T5 is defined as GPO12
Bit-4 = 1: Pin T5 is defined as PCS0#
Bit-3 = 0: Pin U5 is defined as GPO13
Bit-3 = 1: Pin U5 is defined as MCCS#

0 GPOWE# (GPO[23-16]) Enable (Pin T14)
0 Pin is defined as GPIOA..... default
1 Pin is defined as GPOWE# (Rx74[2] also must be set to 1)

Offset 77 – GPIO Control 4 Control..... RW

7-1 Reserved .....always reads 0

0 GPO13 Enable (Pin U5)
0 Pin defined as SOE#..... default
1 Pin defined as GPO13

Offset 79-78 – Programmable Chip Select Control ..... RW

15-0 PCS0# I/O Port Address [15-0]

Offset 80 – Programmable Chip Select Mask ..... RW

7-4 Reserved
3-0 PCS0# I/O Port Address Mask [3-0]

Offset 81 – ISA Positive Decoding Control 1 .....RW

7 On-Board I/O Port Positive Decoding
- 0 Disable .....default
- 1 Enable

6 Microsoft-Sound System I/O Port Positive Decoding
- 0 Disable .....default
- 1 Enable

5-4 Microsoft-Sound System I/O Decode Range
- 00 0530h-0537h .....default
- 01 0604h-060Bh
- 10 0E80-0E87h
- 11 0F40h-0F47h

3 APIC Positive Decoding
- 0 Disable .....default
- 1 Enable

2 BIOS ROM Positive Decoding
- 0 Disable .....default
- 1 Enable

1 Reserved ..... always reads 0

0 PCS0 Positive Decoding
- 0 Disable .....default
- 1 Enable

Offset 82 – ISA Positive Decoding Control 2 .....RW

7 FDC Positive Decoding
- 0 Disable .....default
- 1 Enable

6 LPT Positive Decoding
- 0 Disable .....default
- 1 Enable

5-4 LPT Decode Range
- 00 3BCh-3BFh, 7BCh-7BEh.....default
- 01 378h-37Fh, 778h-77Ah
- 10 278h-27Fh, 678h-67Ah
- 11 -reserved-

3 Game Port Positive Decoding
- 0 Disable .....default
- 1 Enable

2 MIDI Positive Decoding
- 0 Disable .....default
- 1 Enable

1-0 MIDI Decode Range
- 00 300h-303h .....default
- 01 310h-313h
- 10 320h-323h
- 11 330h-333h

Offset 83 – ISA Positive Decoding Control 3..... RW

7 COM Port B Positive Decoding
- 0 Disable..... default
- 1 Enable

6-4 COM-Port B Decode Range
- 000 3F8h-3FFh (COM1)..... default
- 001 2F8h-2FFh (COM2)
- 010 220h-227h
- 011 228h-22Fh
- 100 238h-23Fh
- 101 2E8h-2EFh (COM4)
- 110 338h-33Fh
- 111 3E8h-3EFh (COM3)

3 COM Port A Positive Decoding
- 0 Disable..... default
- 1 Enable

2-0 COM-Port A Decode Range
- 000 3F8h-3FFh (COM1)..... default
- 001 2F8h-2FFh (COM2)
- 010 220h-227h
- 011 228h-22Fh
- 100 238h-23Fh
- 101 2E8h-2EFh (COM4)
- 110 338h-33Fh
- 111 3E8h-3EFh (COM3)

Offset 84 – ISA Positive Decoding Control 4..... RW

7-4 Reserved .....always reads 0

3 FDC Decoding Range
- 0 Primary ..... default
- 1 Secondary

2 Sound Blaster Positive Decoding
- 0 Disable..... default
- 1 Enable

1-0 Sound Blaster Decode Range
- 00 220h-22Fh, 230h-233h ..... default
- 01 240h-24Fh, 250h-253h
- 10 260h-26Fh, 270h-273h
- 11 280h-28Fh, 290h-293h

Offset 85 – Extended Function Enable .....RW

7-5 Reserved ..... always reads 0

4 Function 3 USB Ports 2-3
- 0 Enable.....default
- 1 Disable

3 Function 6 Modem / Audio
- 0 Enable.....default
- 1 Disable

2 Function 5 Audio
- 0 Enable.....default
- 1 Disable

1 Super-I/O Configuration
- 0 Disable .....default
- 1 Enable

0 Super-I/O
- 0 Disable .....default
- 1 Enable

Offset 86 – PNP IRQ/DRQ Test 1 (Do Not Program) ... RW

Offset 87 – PNP IRQ/DRQ Test 2 (Do Not Program) ... RW

Offset 88 – PLL Test (Do Not Program)..... RW

Offset 89 – PLL Control..... RW

7-4 Reserved ..... always reads 0

3-2 PLL PCLK Input Delay Select

1-0 PLL CLK66 Feedback Delay Select

Function 1 Registers - Enhanced IDE Controller

This Enhanced IDE controller interface is fully compatible with the SFF 8038i v.1.0 specification. There are two sets of software accessible registers -- PCI configuration registers and Bus Master IDE I/O registers. The PCI configuration registers are located in the function 1 PCI configuration space of the VT82C686A. The Bus Master IDE I/O registers are defined in the SFF8038i v1.0 specification.

PCI Configuration Space Header

Offset 1-0 - Vendor ID (1106h=VIA).....RO

Offset 3-2 - Device ID (0571h=IDE Controller).....RO

Offset 5-4 - Command.....RW

- **15-10 Reserved** ..... always reads 0
- **9 Fast Back to Back Cycles** ..... default = 0 (disabled)
- **8 SERR# Enable**..... default = 0 (disabled)
- **7 Address Stepping** ..... **fixed at 1 (enabled)**
  A value of 1 provides additional address decode time to IDE devices.
- **6 Parity Error Response**..... default = 0 (disabled)
- **5 VGA Palette Snoop** .....fixed at 0 (disabled)
- **4 Memory Write & Invalidate** .....fixed at 0 (disabled)
- **3 Special Cycles** .....fixed at 0 (disabled)
- **2 Bus Master** ..... default = 0 (disabled)
  S/G operation can be issued only when the "Bus Master" bit is enabled.
- **1 Memory Space**.....fixed at 0 (disabled)
- **0 I/O Space** ..... default = 0 (disabled)
  When the "I/O Space" bit is disabled, the device will not respond to any I/O addresses for both compatible and native mode.

Offset 7-6 - Status.....RWC

- **15 Detected Parity Error**..... default=0
- **14 Signalled System Error**..... default=0
- **13 Received Master Abort**..... default=0
- **12 Received Target Abort** ..... default=0
- **11 Signalled Target Abort**.....Fixed at 0
- **10-9 DEVSEL# Timing** .....default = 01 (medium)
- **8 Data Parity Detected**..... default=0
- **7 Fast Back to Back** .....Fixed at 1
- **6-0 Reserved** ..... always reads 0

Offset 8 - Revision ID (06) .....RO

- **0-7 Revision Code for IDE Controller Logic Block**

Offset 9 - Programming Interface ..... RW

- **7 Master IDE Capability**..... fixed at 1 (Supported)
- **6-4 Reserved** .....always reads 0
- **3 Programmable Indicator - Secondary** ..... fixed at 1
  Supports both modes (may be set to either mode by writing bit-2)
- **2 Channel Operating Mode - Secondary**
  - 0 Compatibility Mode (fixed addressing)
  - 1 Native PCI Mode (flexible addressing) ..... def
- **1 Programmable Indicator - Primary**..... fixed at 1
  Supports both modes (may be set to either mode by writing bit-0)
- **0 Channel Operating Mode - Primary**
  - 0 Compatibility Mode (fixed addressing)
  - 1 Native PCI Mode (flexible addressing) ..... def

Compatibility Mode (fixed IRQs and I/O addresses):

Channel	Command Block Registers	Control Block Registers	IRQ
Pri	1F0-1F7	3F6	14
Sec	170-177	376	15

Native PCI Mode (registers are programmable in I/O space)

Channel	Command Block Registers	Control Block Registers
Pri	BA @offset 10h	BA @offset 14h
Sec	BA @offset 18h	BA @offset 1Ch

Command register blocks are 8 bytes of I/O space
Control registers are 4 bytes of I/O space (only byte 2 is used)

Offset A - Sub Class Code (01h=IDE Controller) ..... RO

Offset B - Base Class Code (01h=Mass Storage Ctrlr) ... RO

Offset C – Cache Line Size (00h).....RO

Offset D - Latency Timer (Default=0).....RW

Offset E - Header Type (00h).....RO

Offset F - BIST (00h).....RO

Offset 13-10 - Pri Data / Command Base Address.....RW

Specifies an 8 byte I/O address space.

31-16	**Reserved**	always read 0
15-3	**Port Address**	default=01F0h
2-0	**Fixed at 001b**	fixed

Offset 17-14 - Pri Control / Status Base Address.....RW

Specifies a 4 byte I/O address space of which only the third byte is active (i.e., 3F6h for the default base address of 3F4h).

31-16	**Reserved**	always read 0
15-2	**Port Address**	default=03F4h
1-0	**Fixed at 01b**	fixed

Offset 1B-18 - Sec Data / Command Base Address .....RW

Specifies an 8 byte I/O address space.

31-16	**Reserved**	always read 0
15-3	**Port Address**	default=0170h
2-0	**Fixed at 001b**	fixed

Offset 1F-1C - Sec Control / Status Base Address.....RW

Specifies a 4 byte I/O address space of which only the third byte is active (i.e., 376h for the default base address of 374h).

31-16	**Reserved**	always read 0
15-2	**Port Address**	default=0374h
1-0	**Fixed at 01b**	fixed

Offset 23-20 - Bus Master Control Regs Base Address..RW

Specifies a 16 byte I/O address space compliant with the **SFF-8038**i **rev 1.0** specification.

31-16	**Reserved**	always read 0
15-4	**Port Address**	default=CC0h
3-0	**Fixed at 0001b**	fixed

Offset 3C - Interrupt Line (0Eh) ..... RW

Offset 3D - Interrupt Pin (00h).....RO

7-0 Interrupt Routing Mode

00h Legacy mode interrupt routing..... default
01h Native mode interrupt routing

Offset 3E - Min Gnt (00h) .....RO

Offset 3F - Max Latency (00h).....RO

IDE-Controller-Specific Confiiguration Registers

Offset 40 - Chip Enable.....RW

- **7-4 Reserved** ..... always reads 0
- **3-2 Reserved (Do Not Program)**.....R/W, default = 0
- **1 Primary Channel Enable**..... default = 0 (disabled)
- **0 Secondary Channel Enable** .... default = 0 (disabled)

Offset 41 - IDE Configuration.....RW

- **7 Primary IDE Read Prefetch Buffer**
  - 0 Disable .....default
  - 1 Enable
- **6 Primary IDE Post Write Buffer**
  - 0 Disable .....default
  - 1 Enable
- **5 Secondary IDE Read Prefetch Buffer**
  - 0 Disable .....default
  - 1 Enable
- **4 Secondary IDE Post Write Buffer**
  - 0 Disable .....default
  - 1 Enable
- **3 SERR# Response**
  - 0 Disable .....default
  - 1 Enable
- **2 Reserved (Do Not Change)**..... default=1
- **1 Reserved (Do Not Change)**..... default=1
- **0 PERR# Response**
  - 0 Disable .....default
  - 1 Enable

Offset 42 - Reserved (Do Not Program) .....RW

Offset 43 - FIFO Configuration..... RW

- **7 Hold PCI Request Until DACK Release**
  - 0 Disabled..... default
  - 1 Enabled
- **6-4 FIFO Configuration Between the Two Channels**

	Primary	Secondary	
00x	32	0	..... default
010	24	8	
011	16	16	
100	16	16	
101	8	24	
11x	0	32	

- **3-2 Threshold for Primary Channel**
  - 00 0
  - 01 3/4
  - 10 1/2 ..... default
  - 11 1/4
- **1-0 Threshold for Secondary Channel**
  - 00 0
  - 01 3/4
  - 10 1/2 ..... default
  - 11 1/4

Offset 44 - Miscellaneous Control 1.....RW

7 Reserved ..... always reads 0

6 Master Read Cycle IRDY# Wait States
- 0 0 wait states
- 1 1 wait state.....default

5 Master Write Cycle IRDY# Wait States
- 0 0 wait states
- 1 1 wait state.....default

4 Reserved ..... always reads 0

3 Bus Master IDE Status Register Read Retry
Retry bus master IDE status register read when master write operation for DMA read is not complete
- 0 Disabled
- 1 Enabled.....default

2-1 Reserved ..... always reads 0

0 UltraDMA Host Must Wait for First Strobe Before Termination
- 0 Enabled.....default
- 1 Disabled

Offset 45 - Miscellaneous Control 2.....RW

7 Reserved ..... always reads 0

6 Interrupt Steering Swap
- 0 Don't swap channel interrupts.....default
- 1 Swap interrupts between the two channels

5-2 Reserved ..... always reads 0

1 Secondary Channel Threshold Enable
- 0 Disable (data transfer starts immediately if FIFO is not empty)
- 1 Enable (data transfer will not start until the FIFO is filled to the threshold set in bits 1-0 of Rx43) .....default

0 Primary Channel Threshold Enable
- 0 Disable (data transfer starts immediately if FIFO is not empty)
- 1 Enable (data transfer will not start until the FIFO is filled to the threshold set in bits 3-2 of Rx43) .....default

Offset 46 - Miscellaneous Control 3 ..... RW

7 Primary Channel Read DMA FIFO Flush
1 = Enable FIFO flush for read DMA when interrupt asserts primary channel. .....default=1 (enabled)

6 Secondary Channel Read DMA FIFO Flush
1 = Enable FIFO flush for Read DMA when interrupt asserts secondary channel. .....Default=1 (enabled)

5 Primary Channel End-of-Sector FIFO Flush
1 = Enable FIFO flush at the end of each sector for the primary channel. ..... Default=0 (disabled)

4 Secondary Channel End-of-Sector FIFO Flush
1 = Enable FIFO flush at the end of each sector for the secondary channel..... Default=0 (disabled)

3-2 Reserved .....always reads 0

1-0 Max DRDY Pulse Width
Maximum DRDY# pulse width after the cycle count. Command will deassert in spite of DRDY# status to avoid system ready hang.
- 00 No limitation..... default
- 01 64 PCI clocks
- 10 128 PCI clocks
- 11 192 PCI clocks

Offset 4B-48 - Drive Timing Control.....RW

The following fields define the Active Pulse Width and Recovery Time for the IDE DIOR# and DIOW# signals:

31-28 Primary Drive 0 Active Pulse Width..... def=1010b
27-24 Primary Drive 0 Recovery Time..... def=1000b
23-20 Primary Drive 1 Active Pulse Width..... def=1010b
19-16 Primary Drive 1 Recovery Time..... def=1000b
15-12 Secondary Drive 0 Active Pulse Width .. def=1010b
11-8 Secondary Drive 0 Recovery Time ..... def=1000b
7-4 Secondary Drive 1 Active Pulse Width .. def=1010b
3-0 Secondary Drive 1 Recovery Time ..... def=1000b

The actual value for each field is the encoded value in the field plus one and indicates the number of PCI clocks.

Offset 4C - Address Setup Time.....RW

7-6 Primary Drive 0 Address Setup Time
5-4 Primary Drive 1 Address Setup Time
3-2 Secondary Drive 0 Address Setup Time
1-0 Secondary Drive 1 Address Setup Time

For each field above:
00 1T
01 2T
10 3T
11 4T .....default

Offset 4E - Secondary Non-1F0 Port Access Timing.....RW

7-4 DIOR#/DIOW# Active Pulse Width..... def=1111b
3-0 DIOR#/DIOW# Recovery Time..... def=1111b

The actual value for each field is the encoded value in the field plus one and indicates the number of PCI clocks.

Offset 4F - Primary Non-1F0 Port Access Timing` .....RW

7-4 DIOR#/DIOW# Active Pulse Width..... def=1111b
3-0 DIOR#/DIOW# Recovery Time..... def=1111b

The actual value for each field is the encoded value in the field plus one and indicates the number of PCI clocks.

Offset 53-50 - UltraDMA Extended Timing Control..... RW

31 Pri Drive 0 UltraDMA-Mode Enable Method
0 Enable by using “Set Feature” command..... def
1 Enable by setting bit-30 of this register
30 Pri Drive 0 UltraDMA-Mode Enable
0 Disable..... default
1 Enable UltraDMA-Mode Operation
29 Pri Drive 0 Transfer Mode
0 DMA or PIO Mode ..... default
1 UltraDMA Mode
28-27 Reserved .....always reads 0
26-24 Pri Drive 0 Cycle Time (T = 30nsec @33MHz)
000 2T
001 3T
010 4T
011 5T .....default (rev A-E)
100 6T
101 7T
110 8T
111 9T .....default (rev H)

23 Pri Drive 1 UltraDMA-Mode Enable Method
22 Pri Drive 1 UltraDMA-Mode Enable
21 Pri Drive 1 Transfer Mode
20 Reserved .....always reads 0
19 Pri Clock Source
0 33 MHz..... default
1 66 MHz
18-16 Pri Drive 1 Cycle Time

15 Sec Drive 0 UltraDMA-Mode Enable Method
14 Sec Drive 0 UltraDMA-Mode Enable
13 Sec Drive 0 Transfer Mode
12-11 Reserved .....always reads 0
10-8 Sec Drive 0 Cycle Time

7 Sec Drive 1 UltraDMA-Mode Enable Method
6 Sec Drive 1 UltraDMA-Mode Enable
5 Sec Drive 1 Transfer Mode
4 Reserved .....always reads 0
3 Sec Clock Source
0 33 MHz..... default
1 66 MHz
2-0 Sec Drive 1 Cycle Time

Each byte defines UltraDMA operation for the indicated drive. The bit definitions are the same within each byte.

Offset 54 – UltraDMA FIFO Control.....RW

7-4 Reserved (Do Not Program).....RW, default=0

3 Grant ISA While Sharing Bus with SA & IDE in IDLE State

0 Enable .....default

1 Disable

2 Change Drive to Clear All FIFO & Internal States

0 Disabled

1 Enabled .....default

1 Add Dummy FIFO Push After End of Transfer

0 Enabled

1 Disabled .....default

This bit is normally set to 0 for effective handling of transfer lengths that are not doubleword multiples

0 Complete DMA Cycle with Transfer Size Less Than FIFO Size

0 Enabled.....default

1 Disabled

Offset 61-60 - Primary Sector Size ..... RW

15-12 Reserved .....always reads 0

11-0 Number of Bytes Per Sector ...def=200h (512 bytes)

Offset 69-68 - Secondary Sector Size ..... RW

15-12 Reserved .....always reads 0

11-0 Number of Bytes Per Sector ...def=200h (512 bytes)

Offset 70 – Primary IDE Status .....RW

7 Interrupt Status
6 Prefetch Buffer Status
5 Post Write Buffer Status
4 DMA Read Prefetch Status
3 DMA Write Prefetch Status
2 S/G Operation Complete
1-0 Reserved ..... always reads 0

Offset 71 – Primary Interrupt Control.....RW

7-1 Reserved ..... always reads 0
0 Flush FIFO Before Generating IDE Interrupt
0 Desable.....default
1 Enable

Offset 74 – Primary IDE Command 1 .....RW

7 Reload Sector Size After Last Command Register Write
6-0 Reserved ..... always reads 0

Offset 75 – Primary IDE Command 2 .....RW

7 Set Controller to Perform PIO Mode Data Port Prefetch
6 Set Controller to Perform PIO Mode Data Port Buffer Write
5 Set Controller to Perform DMA Mode Read Pipeline Operation
4 Set Controller to Perform DMA Mode Write Pipeline Operation
3 Stop S/G Bus Master
2-0 Reserved ..... always reads 0

Offset 78 – Secondary IDE Status ..... RW

7 Interrupt Status
6 Prefetch Buffer Status
5 Post Write Buffer Status
4 DMA Read Prefetch Status
3 DMA Write Prefetch Status
2 S/G Operation Complete
1-0 Reserved .....always reads 0

Offset 79 - Secondary Interrupt Control ..... RW

7-1 Reserved .....always reads 0
0 Flush FIFO Before Generating IDE Interrupt
0 Desable ..... default
1 Enable

Offset 7C – Secondary IDE Command 1 ..... RW

7 Reload Sector Size After Last Command Register Write
6-0 Reserved .....always reads 0

Offset 7D – Secondary IDE Command 2 ..... RW

7 Set Controller to Perform PIO Mode Data Port Prefetch
6 Set Controller to Perform PIO Mode Data Port Buffer Write
5 Set Controller to Perform DMA Mode Read Pipeline Operation
4 Set Controller to Perform DMA Mode Write Pipeline Operation
3 Stop S/G Bus Master
2-0 Reserved .....always reads 0

Offset 83-80 – Primary S/G Descriptor Address .....RW

Offset 8B-88 – Secondary S/G Descriptor Address .....RW

Offset 99-98 – Configuration I/O Space .....RW

Specifies an 8-byte I/O space for index and data ports.

IDE I/O Registers

These registers are compliant with the SFF 8038I v1.0 standard. Refer to the SFF 8038I v1.0 specification for further details.

I/O Offset 0 - Primary Channel Command

I/O Offset 2 - Primary Channel Status

I/O Offset 4-7 - Primary Channel PRD Table Address

I/O Offset 8 - Secondary Channel Command

I/O Offset A - Secondary Channel Status

I/O Offset C-F - Secondary Channel PRD Table Address

Function 2 Registers - USB Controller Ports 0-1

This Universal Serial Bus host controller interface is fully compatible with UHCI specification v1.1. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the function 2 PCI configuration space of the VT82C686A. The USB I/O registers are defined in UHCI specification v1.1. The registers in this function control USB ports 0-1 (see function 3 for ports 2-3).

PCI Configuration Space Header

Offset 1-0 - Vendor ID ..... RO

0-7 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID ..... RO

0-7 Device ID (3038h = VT82C686A USB Controller)

Offset 5-4 - Command ..... RW

15-8 Reserved ..... always reads 0
7 Address Stepping ..... default=0 (disabled)
6 Reserved (parity error response) ..... fixed at 0
5 Reserved (VGA palette snoop) ..... fixed at 0
4 Memory Write and Invalidate . default=0 (disabled)
3 Reserved (special cycle monitoring) ..... fixed at 0
2 Bus Master ..... default=0 (disabled)
1 Memory Space ..... default=0 (disabled)
0 I/O Space ..... default=0 (disabled)

Offset 7-6 - Status ..... RWC

15 Reserved (detected parity error) ..... always reads 0
14 Signalled System Error ..... default=0
13 Received Master Abort ..... default=0
12 Received Target Abort ..... default=0
11 Signalled Target Abort ..... default=0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... default (fixed)
10 Slow
11 Reserved
8-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) ..... RO

7-0 Silicon Revision Code (0 indicates first silicon)

Offset 9 - Programming Interface (00h) ..... RO

Offset A - Sub Class Code (03h=USB Controller) ..... RO

Offset B - Base Class Code (0Ch=Serial Bus Controller) RO

Offset C – Cache Line Size (00h) ..... RO

Offset D - Latency Timer ..... RW

7-0 Timer Value ..... default = 16h

Offset E - Header Type (00h) ..... RO

Offset F - BIST (00h) ..... RO

Offset 23-20 - USB I/O Register Base Address ..... RW

31-16 Reserved ..... always reads 0
15-5 USB I/O Register Base Address. Port Address for the base of the 32-byte USB I/O Register block, corresponding to AD[15:5]
4-0 00001b

Offset 3C - Interrupt Line (00h) ..... RW

7-4 Reserved ..... always reads 0
3-0 USB Interrupt Routing ..... default = 16h
0000 Disabled ..... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 IRQ8
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 IRQ13
1110 IRQ14
1111 Disabled

Offset 3D - Interrupt Pin (04h) ..... RO

USB-Specific Configuration Registers

Offset 40 - Miscellaneous Control 1.....RW

7 PCI Memory Command Option
- 0 Support Memory-Read-Line, Memory-Read-Multiple, & Memory-Write-&-Invalidate.... def
- 1 Only support Mem Read, Mem Write Cmds

6 Babble Option
- 0 Automatically disable babbled port when EOF babble occurs.....default
- 1 Don't disable babbled port

5 PCI Parity Check Option
- 0 Disable PERR# generation.....default
- 1 Enable parity check and PERR# generation

4 Frame Interval Select
- 0 1 ms frame.....default
- 1 0.1 ms frame

3 USB Data Length Option
- 0 Support TD length up to 1280.....default
- 1 Support TD length up to 1023

2 USB Power Management
- 0 Disable USB power management.....default
- 1 Enable USB power management

1 DMA Option
- 0 8 DW burst access with better FIFO latency def
- 1 16 DW burst access (original performance)

0 PCI Wait States
- 0 Zero wait .....default
- 1 One wait

Offset 41 - Miscellaneous Control 2 ..... RW

7 USB 1.1 Improvement for EOP
- 0 Enable..... default
- 1 Disable

6 Patch Read / Resume Issue
- 0 Enable..... default
- 1 Disable

5 Patch 16 Bit-time EOP
- 0 Enable..... default
- 1 Disable

4 Hold PCI Request for Successive Accesses
- 0 Disable..... default
- 1 Enable

3 Frame Counter Test Mode
- 0 Disable..... default
- 1 Enable

2 Trap Option
- 0 Set trap 60/64 status bits only when trap 60/64 enable bits are set. ..... default
- 1 Set trap 60/64 status bits without checking enable bits

1 A20gate Pass Through Option
- 0 Pass through A20GATE command sequence defined in UHCI ..... default
- 1 Don't pass through Write I/O port 64 (ff)

0 USB IRQ Test Mode
- 0 Normal Operation..... default
- 1 Generate USB IRQ

Offset 60 - Serial Bus Release Number ..... RO

7-0 Release Number..... always reads 10h

Offset C1-C0 - Legacy Support ..... RO

15-0 UHCI v1.1 Compliant ..... always reads 2000h

USB I/O Registers

These registers are compliant with the UHCI v1.1 standard. Refer to the UHCI v1.1 specification for further details.

I/O Offset 1-0 - USB Command

I/O Offset 3-2 - USB Status

I/O Offset 5-4 - USB Interrupt Enable

I/O Offset 7-6 - Frame Number

I/O Offset B-8 - Frame List Base Address

I/O Offset 0C - Start Of Frame Modify

I/O Offset 11-10 - Port 0 Status / Control

I/O Offset 13-12 - Port 1 Status / Control

Function 3 Registers - USB Controller Ports 2-3

This Universal Serial Bus host controller interface is fully compatible with UHCI specification v1.1. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the function 3 PCI configuration space of the VT82C686A. The USB I/O registers are defined in UHCI specification v1.1. The registers in this function control USB ports 2-3 (see function 2 for ports 0-1).

PCI Configuration Space Header

Offset 1-0 - Vendor ID ..... RO

0-7 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID ..... RO

0-7 Device ID (3038h = VT82C686A USB Controller)

Offset 5-4 - Command ..... RW

15-8 Reserved ..... always reads 0
7 Address Stepping ..... default=0 (disabled)
6 Reserved (parity error response) ..... fixed at 0
5 Reserved (VGA palette snoop) ..... fixed at 0
4 Memory Write and Invalidate . default=0 (disabled)
3 Reserved (special cycle monitoring) ..... fixed at 0
2 Bus Master ..... default=0 (disabled)
1 Memory Space ..... default=0 (disabled)
0 I/O Space ..... default=0 (disabled)

Offset 7-6 - Status ..... RWC

15 Reserved (detected parity error)..... always reads 0
14 Signalled System Error ..... default=0
13 Received Master Abort ..... default=0
12 Received Target Abort ..... default=0
11 Signalled Target Abort ..... default=0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... default (fixed)
10 Slow
11 Reserved
8-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) ..... RO

7-0 Silicon Revision Code (0 indicates first silicon)

Offset 9 - Programming Interface (00h) ..... RO

Offset A - Sub Class Code (03h=USB Controller) ..... RO

Offset B - Base Class Code (0Ch=Serial Bus Controller) RO

Offset C – Cache Line Size (00h) ..... RO

Offset D - Latency Timer ..... RW

7-0 Timer Value ..... default = 16h

Offset E - Header Type (00h) ..... RO

Offset F - BIST (00h) ..... RO

Offset 23-20 - USB I/O Register Base Address ..... RW

31-16 Reserved ..... always reads 0
15-5 USB I/O Register Base Address. Port Address for the base of the 32-byte USB I/O Register block, corresponding to AD[15:5]
4-0 00001b

Offset 3C - Interrupt Line (00h) ..... RW

7-4 Reserved ..... always reads 0
3-0 USB Interrupt Routing ..... default = 16h
0000 Disabled ..... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 IRQ8
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 IRQ13
1110 IRQ14
1111 Disabled

Offset 3D - Interrupt Pin (04h) ..... RO

USB-Specific Configuration Registers

Offset 40 - Miscellaneous Control 1.....RW

7 PCI Memory Command Option
- 0 Support Memory-Read-Line, Memory-Read-Multiple, & Memory-Write-&-Invalidate.... def
- 1 Only support Mem Read, Mem Write Cmds

6 Babble Option
- 0 Automatically disable babbled port when EOF babble occurs.....default
- 1 Don't disable babbled port

5 PCI Parity Check Option
- 0 Disable PERR# generation.....default
- 1 Enable parity check and PERR# generation

4 Frame Interval Select
- 0 1 ms frame.....default
- 1 0.1 ms frame

3 USB Data Length Option
- 0 Support TD length up to 1280.....default
- 1 Support TD length up to 1023

2 USB Power Management
- 0 Disable USB power management.....default
- 1 Enable USB power management

1 DMA Option
- 0 8 DW burst access with better FIFO latency def
- 1 16 DW burst access (original performance)

0 PCI Wait States
- 0 Zero wait .....default
- 1 One wait

Offset 41 - Miscellaneous Control 2 ..... RW

7 USB 1.1 Improvement for EOP
- 0 Enable..... default
- 1 Disable

6 Patch Read / Resume Issue
- 0 Enable..... default
- 1 Disable

5 Patch 16 Bit-time EOP
- 0 Enable..... default
- 1 Disable

4 Hold PCI Request for Successive Accesses
- 0 Disable..... default
- 1 Enable

3 Frame Counter Test Mode
- 0 Disable..... default
- 1 Enable

2 Trap Option
- 0 Set trap 60/64 status bits only when trap 60/64 enable bits are set. ..... default
- 1 Set trap 60/64 status bits without checking enable bits

1 A20gate Pass Through Option
- 0 Pass through A20GATE command sequence defined in UHCI ..... default
- 1 Don't pass through Write I/O port 64 (ff)

0 USB IRQ Test Mode
- 0 Normal Operation..... default
- 1 Generate USB IRQ

Offset 60 - Serial Bus Release Number ..... RO

7-0 Release Number..... always reads 10h

Offset C1-C0 - Legacy Support ..... RO

15-0 UHCI v1.1 Compliant ..... always reads 2000h

USB I/O Registers

These registers are compliant with the UHCI v1.1 standard. Refer to the UHCI v1.1 specification for further details.

I/O Offset 1-0 - USB Command

I/O Offset 3-2 - USB Status

I/O Offset 5-4 - USB Interrupt Enable

I/O Offset 7-6 - Frame Number

I/O Offset B-8 - Frame List Base Address

I/O Offset 0C - Start Of Frame Modify

I/O Offset 11-10 - Port 0 Status / Control

I/O Offset 13-12 - Port 1 Status / Control

Function 4 Regs - Power Management, SMBus and HWM

This section describes the ACPI (Advanced Configuration and Power Interface) Power Management system of the VT82C686A which includes a System Management Bus (SMBus) interface controller and Hardware Monitoring (HWM) subsystem. The power management system of the VT82C686A supports both ACPI and legacy power management functions and is compatible with the APM v1.2 and ACPI v1.0 specifications.

PCI Configuration Space Header

Offset 1-0 - Vendor ID ..... RO

0-7 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID ..... RO

0-7 Device ID ..... (3057h = ACPI Power Mgmt)

Offset 5-4 - Command ..... RW

15-8 Reserved ..... always reads 0
7 Address Stepping ..... fixed at 0
6 Reserved (parity error response) ..... fixed at 0
5 Reserved (VGA palette snoop) ..... fixed at 0
4 Memory Write and Invalidate ..... fixed at 0
3 Reserved (special cycle monitoring) ..... fixed at 0
2 Bus Master ..... fixed at 0
1 Memory Space ..... fixed at 0
0 I/O Space ..... fixed at 0

Offset 7-6 - Status ..... RWC

15 Detected Parity Error ..... always reads 0
14 Signalled System Error ..... always reads 0
13 Received Master Abort ..... always reads 0
12 Received Target Abort ..... always reads 0
11 Signalled Target Abort ..... always reads 0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... default (fixed)
10 Slow
11 Reserved
8 Data Parity Detected ..... always reads 0
7 Fast Back to Back Capable ..... always reads 1
6-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) ..... RO

7-0 Silicon Revision Code

Offset 9 - Programming Interface (00h) ..... RO

The value returned by this register may be changed by writing the desired value to PCI Configuration Function 4 offset 61h.

Offset A - Sub Class Code (00h) ..... RO

The value returned by this register may be changed by writing the desired value to PCI Configuration Function 4 offset 62h.

Offset B - Base Class Code (00h) ..... RO

The value returned by this register may be changed by writing the desired value to PCI Configuration Function 4 offset 63h.

Offset 0D - Latency Timer ..... RW

7-0 Timer Value ..... default = 0

Offset 0E - Header Type (00h) ..... RO

Power Management-Specific PCI Configuration Registers

Offset 40 – General Configuration 0 .....RW

7 Thermal Alarm Source Select
- 0 From pin T11 (Function 0 Rx74[1] must be set to define the pin as THRM#).....default
- 1 From any of the three internal temperature sensing circuits (see Rx43 and Rx44 of Hardware Monitoring configuration space)

6 Sleep Button
- 0 Disable .....default
- 1 Sleep Button is on IRQ6 pin (pin G1)

5 Debounce LID and PWRBTN# Inputs for 200us
- 0 Disable .....default
- 1 Enable

4 Reserved ..... always reads 0

3 Microsoft Sound Monitor in Audio Access
- 0 Disable .....default
- 1 Enable

2 Game Port Monitor in Audio Access
- 0 Disable .....default
- 1 Enable

1 SoundBlaster Monitor in Audio Access
- 0 Disable .....default
- 1 Enable

0 MIDI Monitor in Audio Access
- 0 Disable .....default
- 1 Enable

Offset 41 - General Configuration 1..... RW

7 I/O Enable for ACPI I/O Base
- 0 Disable access to ACPI I/O block..... default
- 1 Allow access to Power Management I/O Register Block (see offset 4B-48 to set the base address for this register block). The definitions of the registers in the Power Management I/O Register Block are included later in this document, following the Power Management Subsystem overview.

6 ACPI Timer Reset
- 0 Normal Timer Operation ..... default
- 1 Reset Timer

5-4 PMU Timer Test Mode (Do Not Program) ....def = 0

3 ACPI Timer Count Select
- 0 24-bit Timer..... default
- 1 32-bit Timer

2 RTC Enable Signal Gated with PSON (SUSC#) in Soft-Off Mode
- 0 Disable..... default
- 1 Enable

1 Clock Throttling Clock Selection
- 0 32 usec (512 usec cycle time)..... default
- 1 1 msec (16 msec cycle time)

0 DEVSEL# Test Mode (Do Not Program).....def = 0

Offset 42 - ACPI Interrupt Select .....RW

7 ATX / AT Power Indicator.....RO
- 0 ATX
- 1 AT

6 SUSC# State..... RO

5 Reserved ..... always reads 0

4 SUSC# AC-Power-On Default Value ..... RO
This bit is written at RTC Index 0A bit-7.

3-0 SCI Interrupt Assignment
- 0000 Disabled .....default
- 0001 IRQ1
- 0010 Reserved
- 0011 IRQ3
- 0100 IRQ4
- 0101 IRQ5
- 0110 IRQ6
- 0111 IRQ7
- 1000 IRQ8
- 1001 IRQ9
- 1010 IRQ10
- 1011 IRQ11
- 1100 IRQ12
- 1101 IRQ13
- 1110 IRQ14
- 1111 IRQ15

Offset 43 – Internal Timer Read Test.....RO

7-0 Internal Timer Read Test

Offset 45-44 - Primary Interrupt Channel (0000h) ..... RW

15 1/0 = Ena/Disa IRQ15 as Primary Intrpt Channel
14 1/0 = Ena/Disa IRQ14 as Primary Intrpt Channel
13 1/0 = Ena/Disa IRQ13 as Primary Intrpt Channel
12 1/0 = Ena/Disa IRQ12 as Primary Intrpt Channel
11 1/0 = Ena/Disa IRQ11 as Primary Intrpt Channel
10 1/0 = Ena/Disa IRQ10 as Primary Intrpt Channel
9 1/0 = Ena/Disa IRQ9 as Primary Intrpt Channel
8 1/0 = Ena/Disa IRQ8 as Primary Intrpt Channel
7 1/0 = Ena/Disa IRQ7 as Primary Intrpt Channel
6 1/0 = Ena/Disa IRQ6 as Primary Intrpt Channel
5 1/0 = Ena/Disa IRQ5 as Primary Intrpt Channel
4 1/0 = Ena/Disa IRQ4 as Primary Intrpt Channel
3 1/0 = Ena/Disa IRQ3 as Primary Intrpt Channel
2 Reserved .....always reads 0
1 1/0 = Ena/Disa IRQ1 as Primary Intrpt Channel
0 1/0 = Ena/Disa IRQ0 as Primary Intrpt Channel

Offset 47-46 - Secondary Interrupt Channel (0000h).... RW

15 1/0 = Ena/Disa IRQ15 as Secondary Intr Channel
14 1/0 = Ena/Disa IRQ14 as Secondary Intr Channel
13 1/0 = Ena/Disa IRQ13 as Secondary Intr Channel
12 1/0 = Ena/Disa IRQ12 as Secondary Intr Channel
11 1/0 = Ena/Disa IRQ11 as Secondary Intr Channel
10 1/0 = Ena/Disa IRQ10 as Secondary Intr Channel
9 1/0 = Ena/Disa IRQ9 as Secondary Intr Channel
8 1/0 = Ena/Disa IRQ8 as Secondary Intr Channel
7 1/0 = Ena/Disa IRQ7 as Secondary Intr Channel
6 1/0 = Ena/Disa IRQ6 as Secondary Intr Channel
5 1/0 = Ena/Disa IRQ5 as Secondary Intr Channel
4 1/0 = Ena/Disa IRQ4 as Secondary Intr Channel
3 1/0 = Ena/Disa IRQ3 as Secondary Intr Channel
2 Reserved .....always reads 0
1 1/0 = Ena/Disa IRQ1 as Secondary Intr Channel
0 1/0 = Ena/Disa IRQ0 as Secondary Intr Channel

Offset 4B-48 – Power Management I/O Base .....RW

31-16 Reserved ..... always reads 0

15-7 Power Management I/O Register Base Address. Port Address for the base of the 128-byte Power Management I/O Register block, corresponding to AD[15:7]. The "I/O Space" bit at offset 41 bit-7 enables access to this register block. The definitions of the registers in the Power Management I/O Register Block are included later in this document, following the Power-Management-Specific PCI Configuration register descriptions and the Power Management Subsystem overview.

6-0 0000001b

Offset 4C – Host Bus Power Management Control.....RW

7-4 Thermal Duty Cycle (THM_DTY)

This 4-bit field determines the duty cycle of the STPCLK# signal when the THRM# pin is asserted low. The field is decoded as follows:

0000 Reserved.....default
0001 0-6.25%
0010 6.25-12.50%
0011 18.75-25.00%
0100 31.25-37.50%
0101 37.50-43.75%
0110 43.75-50.00%
0111 50.00-56.25%
1000 56.25-62.50%
1001 62.50-68.75%
1010 68.75-75.00%
1011 75.00-87.50%
1100 75.00-81.25%
1101 81.25-87.50%
1110 87.50-93.75%
1111 93.75-100%

3 THRM Enable

0 Disable .....default
1 Enable

2 Frame Input as Resume Event in C3

0 Disable .....default
1 Enable

1 Reserved ..... always reads 0

0 CPU Stop Grant Cycle Select

0 From Halt and Stop Grant Cycle .....default
1 From Stop Grant Cycle

This bit is combined with I/O space Rx2C[3] for controlling the start of STPCLK# assertion during system suspend mode:

Rx2C[3] Function 4 I/O Space	Rx4C[0] Function 4 Cfg Space	STPCLK# Assertion
0	x	Immediate
1	0	Wait for CPU Halt / Stop Grant cycle
1	1	Wait for CPU Stop Grant cycle

Offset 4D – Throttle / Clock Stop Control..... RW

7 Throttle Timer Reset.....def = 0

6-5 Throttle Timer

0x 4-Bit ..... default
10 3-Bit
11 2-Bit

4 Fast Clock (7.5us) as Throttle Timer Tick

0 Disable..... default
1 Enable

3 Reserved .....always reads 0

2 Internal Clock Stop for PCI Idle

0 Disable..... default
1 Enable

1 Internal Clock Stop During C3

0 Disable..... default
1 Enable

0 Internal Clock Stop During Suspend

0 Disable..... default
1 Enable

Offset 53-50 - GP Timer Control (0000 0000h) .....RW

31-30 Conserve Mode Timer Count Value
- 00 1/16 second .....default
- 01 1/8 second
- 10 1 second
- 11 1 minute

29 Conserve Mode Status
This bit reads 1 when in Conserve Mode

28 Conserve Mode Enable
- 0 Disable .....default
- 1 Enable

27-26 Secondary Event Timer Count Value
- 00 2 milliseconds.....default
- 01 64 milliseconds
- 10 ½ second
- 11 by EOI + 0.25 milliseconds

25 Secondary Event Occurred Status
This bit reads 1 to indicate that a secondary event has occurred (to resume the system from suspend) and the secondary event timer is counting down.

24 Secondary Event Timer Enable
- 0 Disable .....default
- 1 Enable

23-16 GP1 Timer Count Value (base defined by bits 5-4)
Write to load count value; Read to get current count

15-8 GP0 Timer Count Value (base defined by bits 1-0)
Write to load count value; Read to get current count

7 GP1 Timer Start
On setting this bit to 1, the GP1 timer loads the value defined by bits 23-16 of this register and starts counting down. The GP1 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP1 timer counts down to zero, then the GP1 Timer Timeout Status bit is set to one (bit-3 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP1 Timer Timeout Enable bit is set (bit-3 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

6 GP1 Timer Automatic Reload
- 0 GP1 Timer stops at 0 .....default
- 1 Reload GP1 timer automatically after counting down to 0

5-4 GP1 Timer Base
- 00 Disable .....default
- 01 1/4 msec
- 10 1 second
- 11 1 minute

3 GP0 Timer Start
On setting this bit to 1, the GP0 timer loads the value defined by bits 15-8 of this register and starts counting down. The GP0 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP0 timer counts down to zero, then the GP0 Timer Timeout Status bit is set to one (bit-2 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP0 Timer Timeout Enable bit is set (bit-2 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

2 GP0 Timer Automatic Reload
- 0 GP0 Timer stops at 0 ..... default
- 1 Reload GP0 timer automatically after counting down to 0

1-0 GP0 Timer Base
- 00 Disable..... default
- 01 1/16 second
- 10 1 second
- 11 1 minute

Offset 54 – Power Well Control ..... WO

7 Reserved ..... always reads 0

6 STR Power Well Output Gating
- 0 Disable .....default
- 1 Enable

5 SUSC# = 0 for STR
- 0 Disable .....default
- 1 Enable

4 SUSST1# / GPO3 Select
- 0 SUSST1#.....default
- 1 GPO3

3 GPO2 / SUSB# Select
- 0 SUSB#.....default
- 1 GPO2

Before chip rev C, these definitions were reversed

2 GPO1 / SUSA# Select
- 0 SUSA# .....default
- 1 GPO1

Before chip rev C, these definitions were reversed

1-0 GPO0 Output Selection
- 00 From GPO (ACPI Rx4C[0]).....default
- 01 1 Hz
- 10 4 Hz
- 11 16 Hz

Offset 61 – Program Interface Read Value ..... WO

7-0 Rx09 Read Value

The value returned by the register at offset 9h (Programming Interface) may be changed by writing the desired value to this location.

Offset 62 - Sub Class Read Value ..... WO

7-0 Rx0A Read Value

The value returned by the register at offset 0Ah (Sub Class Code) may be changed by writing the desired value to this location.

Offset 63 - Base Class Read Value..... WO

7-0 Rx0B Read Value

The value returned by the register at offset 0Bh (Base Class Code) may be changed by writing the desired value to this location.

Hardware-Monitor-Specific Configuration Registers

Offset 71-70 – Hardware Monitor I/O Base .....RW

15-7 **I/O Base (128-byte I/O space)** ..... default = 0
6-0 **Fixed** ..... always reads 0000001b

Offset 74 –Hardware Monitor Control .....RW

7-4 **Reserved** ..... always reads 0
3 **Hardware Monitoring Interrupt**
0 SMI .....default
1 SCI
2-1 **Reserved** ..... always reads 0
0 **Hardware Monitoring I/O Enable**
0 Disable hardware monitor functions.....default
1 Enable hardware monitor functions

System Management Bus-Specific Configuration Registers

Offset 93-90 – SMBus I/O Base ..... RW

31-16 **Reserved** .....always reads 0
15-4 **I/O Base (16-byte I/O space)**.....default = 00h
3-0 **Fixed** .....always reads 0001b

Offset D2 – SMBus Host Configuration ..... RW

7-4 **Reserved** .....always reads 0
3 **SMBus Interrupt Select**
0 SMI ..... default
1 SCI
2-1 **Reserved** .....always reads 0
0 **SMBus Host Controller Enable**
0 Disable SMB controller functions ..... default
1 Enable SMB controller functions

Offset D3 – SMBus Host Slave Command..... RW

7-0 **SMBus Host Slave Command Code**.....default=0

Offset D4 – SMBus Slave Address for Port 1..... RW

7-0 **SMBus Slave Address for Port 1**.....default=0
Bit-0 must be set to 0 for proper operation

Offset D5 – SMBus Slave Address for Port 2..... RW

7-0 **SMBus Slave Address for Port 2**.....default=0
Bit-0 must be set to 0 for proper operation

Offset D6 – SMBus Revision ID ..... RO

7-0 **SMBus Revision Code**

Power Management I/O-Space Registers

Basic Power Management Control and Status

I/O Offset 1-0 - Power Management Status .....RWC

The bits in this register are set only by hardware and can be reset by software by writing a one to the desired bit position.

15 **Wakeup Status** (WAK_STS) ..... default = 0
This bit is set when the system is in the suspend state and an enabled resume event occurs. Upon setting this bit, the system automatically transitions from the suspend state to the normal working state (from C3 to C0 for the processor).

14-11 **Reserved** ..... always reads 0

10 **RTC Status** (RTC_STS)..... default = 0
This bit is set when the RTC generates an alarm (on assertion of the RTC IRQ signal).

9 **Sleep Button Status** (SB_STS)..... default = 0
This bit is set when the sleep button (SLPBTN# / IRQ6) is pressed.

8 **Power Button Status** (PB_STS)..... default = 0
This bit is set when the PWRBTN# signal is asserted LOW. If the PWRBTN# signal is held LOW for more than four seconds, this bit is cleared, the PBOR_STS bit is set, and the system will transition into the soft off state.

7-6 **Reserved** ..... always reads 0

5 **Global Status** (GBL_STS)..... default = 0
This bit is set by hardware when BIOS_RLS is set (typically by an SMI routine to release control of the SCI/SMI lock). When this bit is cleared by software (by writing a one to this bit position) the BIOS_RLS bit is also cleared at the same time by hardware.

4 **Bus Master Status** (BM_STS) ..... default = 0
This bit is set when a system bus master requests the system bus. All PCI master, ISA master and ISA DMA devices are included.

3-1 **Reserved** ..... always reads 0

0 **ACPI Timer Carry Status** (TMR_STS).. default = 0
The bit is set when the 23rd (31st) bit of the 24 (32) bit ACPI power management timer changes.

I/O Offset 3-2 - Power Management Enable ..... RW

The bits in this register correspond to the bits in the Power Management Status Register at offset 1-0.

15 **Reserved** .....always reads 0

14-11 **Reserved** .....always reads 0

10 **RTC Enable** (RTC_EN).....default = 0
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI_EN bit) to be generated when the RTC_STS bit is set.

9 **Sleep Button Enable** (SB_EN) .....default = 0
This bit may be set to trigger either an SCI or SMI when the SB_STS bit is set.

8 **Power Button Enable** (PB_EN) .....default = 0
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI_EN bit) to be generated when the PB_STS bit is set.

7-6 **Reserved** .....always reads 0

5 **Global Enable** (GBL_EN).....default = 0
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI_EN bit) to be generated when the GBL_STS bit is set.

4 **Reserved** .....always reads 0

3-1 **Reserved** .....always reads 0

0 **ACPI Timer Enable** (TMR_EN) .....default = 0
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI_EN bit) to be generated when the TMR_STS bit is set.

I/O Offset 5-4 - Power Management Control .....RW

15 Soft Resume

14 Reserved ..... always reads 0

13 Sleep Enable (SLP_EN)..... always reads 0
This is a write-only bit; reads from this bit always return zero. Writing a one to this bit causes the system to sequence into the sleep (suspend) state defined by the SLP_TYP field.

12-10 Sleep Type (SLP_TYP)
- 000 Normal On
- 001 Suspend to RAM (STR)
- 010 Suspend to Disk (STD) (also called Soft Off). The VCC power plane is turned off while the VCCS and VBAT planes remain on.
- 011 Reserved
- 100 Power On Suspend without Reset
- 101 Power On Suspend with CPU Reset
- 110 Power On Suspend with CPU/PCI Reset
- 111 Reserved

In any sleep state, there is minimal interface between powered and non-powered planes so that the effort for hardware design may be well managed.

9-3 Reserved ..... always reads 0

2 Global Release (GBL_RLS) ..... **WO**, default = 0
This bit is set by ACPI software to indicate the release of the SCI / SMI lock. Upon setting of this bit, the hardware automatically sets the BIOS_STS bit. The bit is cleared by hardware when the BIOS_STS bit is cleared by software. Note that the setting of this bit will cause an SMI to be generated if the BIOS_EN bit is set (bit-5 of the Global Enable register at offset 2Ah).

1 Bus Master Reload (BMS_RLD)..... default = 0
- 0 Bus master requests are ignored by power management logic
- 1 Bus master requests transition the processor from the C3 state to the C0 state

0 SCI Enable (SCI_EN)..... default = 0
Selects the power management event to generate either an SCI or SMI:
- 0 Generate SMI
- 1 Generate SCI

Note that certain power management events can be programmed individually to generate an SCI or SMI independent of the setting of this bit (refer to the General Purpose SCI Enable and General Purpose SMI Enable registers at offsets 22 and 24). Also, TMR_STS & GBL_STS always generate SCI and BIOS_STS always generates SMI.

I/O Offset 0B-08 - Power Management Timer ..... RW

31-24 Extended Timer Value (ETM_VAL)
This field reads back 0 if the 24-bit timer option is selected (Rx41 bit-3).

23-0 Timer Value (TMR_VAL)
This read-only field returns the running count of the power management timer. This is a 24/32-bit counter that runs off a 3.579545 MHz clock, and counts while in the S0 (working) system state. The timer is reset to an initial value of zero during a reset, and then continues counting until the 14.31818 MHz input to the chip is stopped. If the clock is restarted without a reset, then the counter will continue counting from where it stopped.

Processor Power Management Registers

I/O Offset 13-10 - Processor & PCI Bus Control.....RW

31-12 Reserved ..... always reads 0

11 PCI Stop (PCISTP# asserted) when PCKRUN# is Deasserted (PCI_STP)
- 0 Enable.....default
- 1 Disable

10 PCI Bus Clock Run Without Stop (PCI_RUN)
- 0 PCKRUN# will be de-activated after the PCI bus is idle for 26 clocks.....default
- 1 PCKRUN# is always asserted

9 Host Clock Stop Enable (HOST_STP)
- 0 STPCLK# will be asserted in the C3 state, but the CPU clock is not stopped .....default
- 1 CPU clock is stopped in the C3 state

8 Assert SLP# for LVL3 Read
- 0 Disable .....default
- 1 Enable

Used in Slot-1 systems only.

7-5 Reserved ..... always reads 0

4 Throttling Enable (THT_EN).
Setting this bit starts clock throttling (modulating the STPCLK# signal) regardless of the CPU state. The throttling duty cycle is determined by bits 3-0 of this register.

3-0 Throttling Duty Cycle (THT_DTY)
This 4-bit field determines the duty cycle of the STPCLK# signal when the system is in throttling mode (the "Throttling Enable" bit is set to one). The duty cycle indicates the percentage of time the STPCLK# signal is asserted while the Throttling Enable bit is set. The field is decoded as follows:

0000 Reserved
0001 0-6.25%
0010 6.25-12.50%
0011 18.75-25.00%
0100 31.25-37.50%
0101 37.50-43.75%
0110 43.75-50.00%
0111 50.00-56.25%
1000 56.25-62.50%
1001 62.50-68.75%
1010 68.75-75.00%
1011 75.00-87.50%
1100 75.00-81.25%
1101 81.25-87.50%
1110 87.50-93.75%
1111 93.75-100%

I/O Offset 14 - Processor Level 2 (P_LVL2)..... RO

7-0 Level 2 .....always reads 0
Reads from this register put the processor into the Stop Grant state (the VT82C686A asserts STPCLK# to suspend the processor). Wake up from Stop Grant state is by interrupt (INTR, SMI, and SCI).

Reads from this register return all zeros; writes to this register have no effect.

I/O Offset 15 - Processor Level 3 (P_LVL3)..... RO

7-0 Level 3 .....always reads 0
Reads from this register put the processor in the C3 clock state with the STPCLK# signal asserted. If Rx10[9] = 1 then the CPU clock is also stopped by asserting CPUSTP#. Wake up from the C3 state is by interrupt (INTR, SMI, and SCI).

Reads from this register return all zeros; writes to this register have no effect.

General Purpose Power Management Registers

I/O Offset 21-20 - General Purpose Status (GP_STS). RWC

15-14 Reserved ..... always reads 0

13 AC97 Wakeup Status (WAKE_STS)
Can be set only in suspend mode

12 Battery Low Status (BL_STS)
This bit is set when the BATLOW# input is asserted low.

11 Notebook Lid Status (LID_STS)
This bit is set when the LID input detects the edge selected by Rx2C bit-7 (0=rising, 1=falling).

10 Thermal Detect Status (THRM_STS)
This bit is set when the THRM input detects the edge selected by Rx2C bit-6 (0=rising, 1=falling).

9 USB Resume Status (USB_STS)
This bit is set when a USB peripheral generates a resume event.

8 Ring Status (RING_STS)
This bit is set when the RING# input is asserted low.

7 Reserved ..... always reads 0

6 GPI6 / EXTSMI6 Toggle Status (GPI6_STS)
This bit is set when the GPI6 pin is toggled.

5 PME# Toggle Status (PME_STS)
This bit is set when the PME# pin is toggled.

4 GPI4 / SLPBTN# Toggle Status (GPI4_STS)
This bit is set when the GPI4 pin is toggled.

3-2 Reserved ..... always reads 0

1 GPI1 Status (GPI1_STS)
This bit is set when the GPI1 pin is asserted low.

0 EXTSMI# Status (EXT_STS)
This bit is set when the EXTSMI# pin is asserted low.

Note that the above bits correspond one for one with the bits of the General Purpose SCI Enable and General Purpose SMI Enable registers at offsets 22 and 24: an SCI or SMI is generated if the corresponding bit of the General Purpose SCI or SMI Enable registers, respectively, is set to one.

The above bits are set by hardware only and can only be cleared by writing a one to the desired bit.

I/O Offset 23-22 - General Purpose SCI Enable ..... RW

15-14 Reserved ..... always reads 0

13 Enable SCI on setting of the WAKE_STS bit def=0

12 Enable SCI on setting of the BL_STS bit ..... def=0

11 Enable SCI on setting of the LID_STS bit ..... def=0

10 Enable SCI on setting of the THRM_STS bit def=0

9 Enable SCI on setting of the USB_STS bit .... def=0

8 Enable SCI on setting of the RING_STS bit . def=0

7 Reserved ..... always reads 0

6 Enable SCI on setting of the GPI6_STS bit.... def=0

5 Enable SCI on setting of the PME_STS bit.... def=0

4 Enable SCI on setting of the GPI4_STS bit.... def=0

3-2 Reserved ..... always reads 0

1 Enable SCI on setting of the GPI1_STS bit.... def=0

0 Enable SCI on setting of the EXT_STS bit .... def=0

These bits allow generation of an SCI using a separate set of conditions from those used for generating an SMI.

I/O Offset 25-24 - General Purpose SMI Enable ..... RW

15-14 Reserved ..... always reads 0

13 Enable SMI on setting of the WAKE_STS bit def=0

12 Enable SMI on setting of the BL_STS bit ..... def=0

11 Enable SMI on setting of the LID_STS bit .... def=0

10 Enable SMI on setting of the THRM_STS bit def=0

9 Enable SMI on setting of the USB_STS bit ... def=0

8 Enable SMI on setting of the RING_STS bit def=0

7 Reserved ..... always reads 0

6 Enable SMI on setting of the GPI6_STS bit... def=0

5 Enable SMI on setting of the PME_STS bit... def=0

4 Enable SMI on setting of the GPI4_STS bit... def=0

3-2 Reserved ..... always reads 0

1 Enable SMI on setting of the GPI1_STS bit... def=0

0 Enable SMI on setting of the EXT_STS bit.... def=0

These bits allow generation of an SMI using a separate set of conditions from those used for generating an SCI.

Generic Power Management Registers

I/O Offset 29-28 - Global Status.....RWC

15-9 Reserved ..... always reads 0

8 PCKRUN# Resume Status (PRRSM_STS).... def=0
This bit is set when PCI bus peripherals wake up the system by asserting PCKRUN#

7 Primary IRQ Resume Status (PIRSM_STS) . def=0
This bit is set at the occurrence of primary IRQs as defined in Rx45-44 of PCI configuration space

6 Software SMI Status (SW_SMI_STS)..... def=0
This bit is set when the SMI_CMD port (offset 2F) is written.

5 BIOS Status (BIOS_STS) ..... def=0
This bit is set when the GBL_RLS bit is set to one (typically by the ACPI software to release control of the SCI/SMI lock). When this bit is reset (by writing a one to this bit position) the GBL_RLS bit is reset at the same time by hardware.

4 Legacy USB Status (LEG_USB_STS) ..... def=0
This bit is set when a legacy USB event occurs.

3 GP1 Timer Time Out Status (GP1TO_STS).. def=0
This bit is set when the GP1 timer times out.

2 GP0 Timer Time Out Status (GP0TO_STS).. def=0
This bit is set when the GP0 timer times out.

1 Secondary Event Timer Time Out Status (STTO_STS) ..... def=0
This bit is set when the secondary event timer times out.

0 Primary Activity Status (PACT_STS)..... def=0
This bit is set at the occurrence of any enabled primary system activity (see the Primary Activity Detect Status register at offset 30h and the Primary Activity Detect Enable register at offset 34h). After checking this bit, software can check the status bits in the Primary Activity Detect Status register at offset 30h to identify the specific source of the primary event. Note that setting this bit can be enabled to reload the GP0 timer (see bit-0 of the GP Timer Reload Enable register at offset 38).

Note that SMI can be generated based on the setting of any of the above bits (see the offset 2Ah Global Enable register bit descriptions in the right hand column of this page).

The bits in this register are set by hardware only and can only be cleared by writing a one to the desired bit position.

I/O Offset 2B-2A - Global Enable ..... RW

15-9 Reserved ..... always reads 0

8 PCKRUN# Resume Enable (PRRSM_EN) .... def=0
This bit may be set to trigger an SMI to be generated when the PRRSM_STS bit is set.

7 Primary IRQ Resume Enable (PIRSM_EN).. def=0
This bit may be set to trigger an SMI to be generated when the PIRSM_STS bit is set.

6 SMI on Software SMI (SW_SMI_EN) ..... def=0
This bit may be set to trigger an SMI to be generated when the SW_SMI_STS bit is set.

5 SMI on BIOS Status (BIOS_EN) ..... def=0
This bit may be set to trigger an SMI to be generated when the BIOS_STS bit is set.

4 SMI on Legacy USB (LEG_USB_EN)..... def=0
This bit may be set to trigger an SMI to be generated when the LEG_USB_STS bit is set.

3 SMI on GP1 Timer Time Out (GP1TO_EN) . def=0
This bit may be set to trigger an SMI to be generated when the GP1TO_STS bit is set.

2 SMI on GP0 Timer Time Out (GP0TO_EN) . def=0
This bit may be set to trigger an SMI to be generated when the GP0TO_STS bit is set.

1 SMI on Secondary Event Timer Time Out (STTO_EN) ..... def=0
This bit may be set to trigger an SMI to be generated when the STTO_STS bit is set.

0 SMI on Primary Activity (PACT_EN) ..... def=0
This bit may be set to trigger an SMI to be generated when the PACT_STS bit is set.

I/O Offset 2D-2C - Global Control (GBL_CTL) .....RW

15-9 Reserved ..... always reads 0

8 SMI Active (INSMI)
- 0 SMI Inactive.....default
- 1 SMI Active. If the SMIIG bit is set, this bit needs to be written with a 1 to clear it before the next SMI can be generated.

7 LID Triggering Polarity
- 0 Rising Edge .....default
- 1 Falling Edge

6 THRM# Triggering Polarity
- 0 Rising Edge .....default
- 1 Falling Edge

5 Battery Low Resume Disable
- 0 Enable resume .....default
- 1 Disable resume from suspend when BATLOW# is asserted

4 SMI Lock (SMIIG)
- 0 Disable SMI Lock
- 1 Enable SMI Lock (SMI low to gate for the next SMI) .....default

3 Wait for Halt / Stop Grant Cycle for STPCLK# Assertion
- 0 Don't wait.....default
- 1 Wait

This bit works with Rx4C[7] of PCI configuration space to control the start of STPCLK# assertion.

2 Power Button Triggering Select
- 0 SCI/SMI generated by PWRBTN# rising edge .....default
- 1 SCI/SMI generated by PWRBTN# low level

Set to zero to avoid the situation where PB_STS is set to wake up the system then reset again by PBOR_STS to switch the system into the soft-off state.

1 BIOS Release (BIOS_RLS)

This bit is set by legacy software to indicate release of the SCI/SMI lock. Upon setting of this bit, hardware automatically sets the GBL_STS bit. This bit is cleared by hardware when the GBL_STS bit cleared by software.

Note that if the GBL_EN bit is set (bit-5 of the Power Management Enable register at offset 2), then setting this bit causes an SCI to be generated (because setting this bit causes the GBL_STS bit to be set).

0 SMI Enable (SMI_EN)
- 0 Disable all SMI generation.....default
- 1 Enable SMI generation

I/O Offset 2F - SMI Command (SMI_CMD) ..... RW

7-0 SMI Command

Writing to this port sets the SW_SMI_STS bit. Note that if the SW_SMI_EN bit is set (see bit-6 of the Global Enable register at offset 2Ah), then an SMI is generated.

I/O Offset 33-30 - Primary Activity Detect Status.....RWC

These bits correspond to the Primary Activity Detect Enable bits in offset 37-34. All bits default to 0, are set by hardware only, and may only be cleared by writing 1s to the desired bit.

31-11 Reserved .....always read 0

10 Audio Access Status ..... (AUD_STS)
Set if Audio is accessed via I/O port ??.

9 Keyboard Controller Access Status..... (KBC_STS)
Set if the KBC is accessed via I/O port 60h.

8 VGA Access Status..... (VGA_STS)
Set if the VGA port is accessed via I/O ports 3B0-3DFh or memory space A0000-BFFFFh.

7 Parallel Port Access Status..... (LPT_STS)
Set if the parallel port is accessed via I/O ports 278-27Fh or 378-37Fh (LPT2 or LPT1).

6 Serial Port B Access Status ..... (COMB_STS)
Set if the serial port is accessed via I/O ports 2F8-2FFh or 2E8-2Efh (COM2 and COM4 respectively).

5 Serial Port A Access Status ..... (COMA_STS)
Set if the serial port is accessed via I/O ports 3F8-3FFh or 3E8-3EFh (COM1 and COM3, respectively).

4 Floppy Access Status.....(FDC_STS)
Set if the floppy controller is accessed via I/O ports 3F0-3F5h or 3F7h.

3 Secondary IDE Access Status.....(SIDE_STS)
Set if the IDE controller is accessed via I/O ports 170-177h or 376h.

2 Primary IDE Access Status ..... (PIDE_STS)
Set if the IDE controller is accessed via I/O ports 1F0-1F7h or 3F6h.

1 Primary Interrupt Activity Status..... (PIRQ_STS)
Set on the occurrence of a primary interrupt (enabled via the "Primary Interrupt Channel" register at Function 4 PCI configuration register offset 44h).

0 PCI Master Access Status ..... (DRQ_STS)
Set on the occurrence of PCI master activity.

Note: The bits above correspond to the bits of the Primary Activity Detect Enable register at offset 34 (see right hand column of this page): if the corresponding bit is set in that register, setting of the above bits will cause the PACT_STS bit to be set (bit-0 of the Global Status register at offset 28). Setting of PACT_STS may be set up to enable a "Primary Activity Event": an SMI will be generated if PACT_EN is set (bit-0 of the Global Enable register at offset 2Ah) and/or the GP0 timer will be reloaded if the "GP0 Timer Reload on Primary Activity" bit is set (bit-0 of the GP Timer Reload Enable register at offset 38 on this page).
Note: Bits 2-9 above also correspond to bits of the GP Timer Reload Enable register (see offset 38 on next page): If bits are set in that register, setting a corresponding bit in this register will cause the GP1 timer to be reloaded.

I/O Offset 37-34 - Primary Activity Detect Enable..... RW

These bits correspond to the Primary Activity Detect Status bits in offset 33-30. Setting of any of these bits also sets the PACT_STS bit (bit-0 of offset 28) which causes the GP0 timer to be reloaded (if PACT_GP0_EN is set) or generates an SMI (if PACT_EN is set).

31-11 Reserved ..... always read 0

10 SMI on Audio Status ..... (KBC_EN)
0 Don't set PACT_STS if AUD_STS is set .... def
1 Set PACT_STS if AUD_STS is set

9 SMI on Keyboard Controller Status..... (KBC_EN)
0 Don't set PACT_STS if KBC_STS is set..... def
1 Set PACT_STS if KBC_STS is set

8 SMI on VGA Status..... (VGA_EN)
0 Don't set PACT_STS if VGA_STS is set .... def
1 Set PACT_STS if VGA_STS is set

7 SMI on Parallel Port Status..... (LPT_EN)
0 Don't set PACT_STS if LPT_STS is set..... def
1 Set PACT_STS if LPT_STS is set

6 SMI on Serial Port B Status .....(COMB_EN)
0 Don't set PACT_STS if COMB_STS is set. def
1 Set PACT_STS if COMB_STS is set

5 SMI on Serial Port A Status ..... (COMA_EN)
0 Don't set PACT_STS if COMA_STS is set. def
1 Set PACT_STS if COMA_STS is set

4 SMI on Floppy Status .....(FDC_EN)
0 Don't set PACT_STS if FDC_STS is set ..... def
1 Set PACT_STS if FDC_STS is set

3 SMI on Secondary IDE Status.....(SIDE_EN)
0 Don't set PACT_STS if SIDE_STS is set .... def
1 Set PACT_STS if SIDE_STS is set

2 SMI on PrimaryIDE Status .....(PIDE_EN)
0 Don't set PACT_STS if PIDE_STS is set .... def
1 Set PACT_STS if PIDE_STS is set

1 SMI on Primary INTR Status ..... (PIRQ_EN)
0 Don't set PACT_STS if PIRQ_STS is set.... def
1 Set PACT_STS if PIRQ_STS is set

0 SMI on PCI Master Status ..... (DRQ_EN)
0 Don't set PACT_STS if DRQ_STS is set .... def
1 Set PACT_STS if DRQ_STS is set

I/O Offset 3B-38 - GP Timer Reload Enable .....RW

All bits in this register default to 0 on power up.

31-8 Reserved .....always read 0

7 Enable GP1 Timer Reload on KBC Access
- 0 Normal GP1 Timer Operation
- 1 Setting of KBC_STS causes the GP1 timer to reload.

6 Enable GP1 Timer Reload on Serial Port Access
- 0 Normal GP1 Timer Operation
- 1 Setting of COMA_STS or COMB_STS causes the GP1 timer to reload.

5 Reserved .....always read 0

4 Enable GP1 Timer Reload on VGA Access
- 0 Normal GP1 Timer Operation
- 1 Setting of VGA_STS causes the GP1 timer to reload.

3 Enable GP1 Timer Reload on IDE/Floppy Access
- 0 Normal GP1 Timer Operation
- 1 Setting of FDC_STS, SIDE_STS, or PIDE_STS causes the GP1 timer to reload.

2-1 Reserved .....always read 0

0 Enable GP0 Timer Reload on Primary Activity
- 0 Normal GP0 Timer Operation
- 1 Setting of PACT_STS causes the GP0 timer to reload. Primary activities are enabled via the Primary Activity Detect Enable register (offset 37-34) with status recorded in the Primary Activity Detect Status register (offset 33-30).

General Purpose I/O Registers

I/O Offset 44 – External SMI Input Value (EXTSMI_VAL).....RO

Depending on the configuration, up to 8 external SCI/SMI ports are available as indicated below. The state of these inputs may be read in this register.

- **7 GPI7 Input Value (RING#)**
- **6 GPI6 Input Value (SMBALRT#)**
- **5 GPI5 Input Value (PME#)**
- **4 GPI4 Input Value (SLPBTN#)**
- **3 GPI3 Input Value (LID)**
- **2 GPI2 Input Value (BATLOW#)**
- **1 GPI1 Input Value**
- **0 EXTSMI# Input Value**

I/O Offset 45 – IRQ / Resume Status.....RW

- **7-4 Reserved** ..... always reads 0
- **3 FM SMI or Serial SMI Status**
- **2 Hardware Monitor IRQ Status**
- **1 SMBus IRQ Status**
- **0 SMBus Resume Status**

I/O Offset 4B-48 - GPI Port Input Value (GPI_VAL).... RO

- **31-24 Reserved** ..... always read 0
- **23-16 GPI[23-16] by Refresh Scan** ..... Read Only
- **15-12 Reserved** ..... always read 0
- **11-0 GPI[11-0] Input Value** ..... Read Only

I/O Offset 4F-4C - GPO Port Output Value (GPO_VAL)RW

Reads from this register return the last value written (held on chip)

- **31-26 Reserved** ..... always reads 0
- **25-0 GPO[25-0] Output Value**.....def = 3FFFFFFh

System Management Bus I/O-Space Registers

The base address for these registers is defined in Rx93-90 of the Function 4 PCI configuration registers. The System Management Bus I/O space is enabled for access by the system if RxD2[0] = 1.

I/O Offset 00 – SMBus Host Status.....RWC

7-5 Reserved ..... always reads 0

4 Failed Bus Transaction.....RWC
- 0 SMBus interrupt not caused by failed bus transaction .....default
- 1 SMBus interrupt caused by failed bus transaction. This bit may be set when the KILL bit (I/O Rx02[1]) is set and can be cleared by writing a 1 to this bit position.

3 Bus Collision.....RWC
- 0 SMBus interrupt not caused by transaction collision.....default
- 1 SMBus interrupt caused by transaction collision. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

2 Device Error.....RWC
- 0 SMBus interrupt not caused by generation of an SMBus transaction error.....default
- 1 SMBus interrupt caused by generation of an SMBus transaction error (illegal command field, unclaimed host-initiated cycle, or host device timeout). This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

1 SMBus Interrupt.....RWC
- 0 SMBus interrupt not caused by host command completion.....default
- 1 SMBus interrupt caused by host command completion. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

0 Host Busy .....RO
- 0 SMBus controller host interface is not processing a command .....default
- 1 SMBus host controller is busy processing a command. None of the other SMBus registers should be accessed if this bit is set.

I/O Offset 01h – SMBus Slave Status..... RWC

7-6 Reserved .....always reads 0

5 Alert Status ..... RWC
- 0 SMBus interrupt not caused by SMBALERT# signal ..... default
- 1 SMBus interrupt caused by SMBALERT# signal. This bit will be set only if the Alert Enable bit is set in the SMBus Slave Control Register at I/O Offset R08[3]. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

4 Shadow 2 Status..... RWC
- 0 SMBus interrupt not caused by address match to SMBus Shadow Address Port 2..... default
- 1 SMBus interrupt or resume event caused by slave cycle address match to SMBus Shadow Address Port 2. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

3 Shadow 1 Status..... RWC
- 0 SMBus interrupt not caused by address match to SMBus Shadow Address Port 1..... default
- 1 SMBus interrupt or resume event caused by slave cycle address match to SMBus Shadow Address Port 1. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

2 Slave Status ..... RWC
- 0 SMBus interrupt not caused by slave event match ..... default
- 1 SMBus interrupt or resume event caused by slave cycle event match of the SMBus Slave Command Register at PCI Function 4 Configuration Offset D3h (command match) and the SMBus Slave Event Register at SMBus Base + Offset 0Ah (data event match). This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

1 Reserved .....always reads 0

0 Slave Busy ..... RO
- 0 SMBus controller slave interface is not processing data ..... default
- 1 SMBus controller slave interface is busy receiving data. None of the other SMBus registers should be accessed if this bit is set.

I/O Offset 02h – SMBus Host Control.....RW

7 Reserved ..... always reads 0

6 Start ..... always reads 0

0 Writing 0 has no effect.....default

1 Start Execution of Command

Writing a 1 to this bit causes the SMBus controller host interface to initiate execution of the command programmed in the SMBus Command Protocol field (bits 4-2). All necessary registers should be programmed prior to writing a 1 to this bit. The Host Busy bit (SMBus Host Status Register bit-0) can be used to identify when the SMBus controller has completed command execution.

5 Reserved ..... always reads 0

4-2 SMBus Command Protocol

000 Quick Read or Write .....default

001 Byte Read or Write

010 Byte Data Read or Write

011 Word Data Read or Write

100 Reserved

101 Block Read or Write

110 Reserved

111 Reserved

1 Kill Transaction in Progress

0 Normal host controller operation .....default

1 Stop host transaction currently in progress.

Setting this bit also sets the FAILED status bit (Host Status bit-4) and asserts the interrupt selected by the SMB Interrupt Select bit (Function 4 SMBus Host Configuration Register RxD2[3]).

0 Interrupt Enable

0 Disable interrupt generation .....default

1 Enable generation of interrupts on completion of the current host transaction.

I/O Offset 03h – SMBus Host Command..... RW

7-0 SMBUS Host Command .....default = 0

This field contains the data transmitted in the command field of the SMBus host transaction.

I/O Offset 04h – SMBus Host Address..... RW

The contents of this register are transmitted in the address field of the SMBus host transaction.

7-1 SMBUS Address .....default = 0

This field contains the 7-bit address of the targeted slave device.

0 SMBUS Read or Write

0 Execute a WRITE command ..... default

1 Execute a READ command

I/O Offset 05h – SMBus Host Data 0 ..... RW

The contents of this register are transmitted in the Data 0 field of SMBus host transaction writes. On reads, Data 0 bytes are stored here.

7-0 SMBUS Data 0.....default = 0

For Block Write commands, this field is programmed with the block transfer count (a value between 1 and 32). Counts of 0 or greater than 32 are undefined. For Block Read commands, the count received from the SMBus device is stored here.

I/O Offset 06h – SMBus Host Data 1 ..... RW

The contents of this register are transmitted in the Data 1 field of SMBus host transaction writes. On reads, Data 1 bytes are stored here.

7-0 SMBUS Data 1.....default = 0

I/O Offset 07h – SMBus Block Data ..... RW

Reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array. It is reset to 0 by reads of the SMBus Host Control register (I/O Offset 2) and incremented automatically by each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0.

7-0 SMBUS Block Data .....default = 0

I/O Offset 08h – SMBus Slave Control.....RW

7-4 Reserved ..... always reads 0

3 SMBus Alert Enable

0 Disable .....default

1 Enable generation of an interrupt or resume event on the assertion of the SMBALERT# signal

2 SMBus Shadow Port 2 Enable

0 Disable .....default

1 Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 2 register (PCI function 4 configuration register RxD5).

1 SMBus Shadow Port 1 Enable

0 Disable .....default

1 Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 1 register (PCI function 4 configuration register RxD4).

0 SMBus Slave Enable

0 Disable .....default

1 Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus host controller slave port of 10h, a command field which matches the SMBus Slave Command register (PCI function 4 configuration register RxD3), and a match of one of the corresponding enabled events in the SMBus Slave Event Register (I/O Offset 0Ah).

I/O Offset 09h – SMBus Shadow Command ..... RO

This register is used to store command values for external SMBus master accesses to the host slave and slave shadow ports.

7-0 Shadow Command.....default = 0

This field contains the command value which was received during an external SMBus master access whose address field matched the host slave address (10h) or one of the slave shadow port addresses.

I/O Offset 0Ah – SMBus Slave Event ..... RW

This register is used to enable generation of interrupt or resume events for accesses to the host controller's slave port.

15-0 SMBus Slave Event .....default = 0

This field contains data bits used to compare against incoming data to the SMBus Slave Data Register (I/O Offset 0Ch). When a bit in this register is set and the corresponding bit the Slave Data register is also set, an interrupt or resume event will be generated if the command value matches the value in the SMBus Slave Command register and the access was to SMBus host address 10h.

I/O Offset 0Ch – SMBus Slave Data ..... RO

This register is used to store data values for external SMBus master accesses to the shadow ports or the SMBus host controller's slave port.

15-0 SMBus Slave Data.....default = 0

This field contains the data value which was transmitted during an external SMBus master access whose address field matched one of the slave shadow port addresses or the SMBus host controller slave port address of 10h.

Hardware Monitor I/O Space Registers

The I/O base address for access to the Hardware Monitor registers is defined in Rx71-70 of function 4 PCI configuration space. The hardware monitor I/O space is enabled for I/O access by the system if Rx74[0] = 1.

Offset 13 – Analog Data 15-8 .....RW

Offset 14 – Analog Data 7-0 .....RW

Offset 15 – Digital Data 7-0 .....RW

Offset 16 – Channel Counter.....RW

Offset 17 – Data Valid & Channel Indicators.....RW

Offset 1D – TSENS3 Hot Temperature High Limit .....RW

Offset 1E – TSENS3 Hot Temp Hysteresis Lo Limit.....RW

Offset 1F – TSENS3 Temperature Reading.....RW

Temperature sensor 3 is an internal bandgap-type sensor which has 10-bit resolution. The high order 8 bits are stored here and the low order 2 bits are stored in Rx49[7-6]. Only the high order 8 bits are used for comparison with the limit values in offsets 1D and 1E.

Offset 20 – TSENS1 Temperature Reading .....RW

Temperature sensor 1 is an external sensor input on pin W13 which has 10-bit resolution. The high order 8 bits are stored here and the low order 2 bits are stored in Rx4B[7-6]. Only the high order 8 bits are used for comparison with the limit values in offsets 39 and 3A.

Offset 21 – TSENS2 Temperature Reading .....RW

Temperature sensor 2 is an external sensor input on pin Y13 which has 10-bit resolution. The high order 8 bits are stored here and the low order 2 bits are stored in Rx49[5-4]. Only the high order 8 bits are used for comparison with the limit values in offsets 3D and 3E.

Offset 22 – VSENS1 (Pin U13) Voltage Reading (2.0V).RW

Offset 23 – VSENS2 (Pin V13) Voltage Reading (2.5V).RW

Offset 24 – Internal Core Voltage Reading (3.3V) .....RW

Offset 25 – VSENS3 (Pin W14) Voltage Reading (5V) ..RW

Offset 26 – VSENS4 (Pin Y14) Voltage Reading (12V)..RW

Offset 27 – VSENS4 (Pin Y14) Voltage Reading (12V)..RW

Offset 28 – Sense Voltage Reading (-12V).....RW

Offset 29 – Sense Voltage Reading (-5V).....RW

Offset 29 – FAN1 (Pin T12) Count Reading .....RW

Offset 2A – FAN2 (Pin U12) Count Reading .....RW

The above two locations store the number of counts of the internal clock per fan revolution.

Offset 2B – VSENS1 Voltage High Limit (CPU 2.0V)... RW

Offset 2C – VSENS1 Voltage Low Limit (CPU 2.0V) ... RW

Offset 2D – VSENS2 Voltage High Limit (NB 2.5V) ..... RW

Offset 2E – VSENS2 Voltage Low Limit (NB 2.5V) ..... RW

Offset 2F – Internal Core Voltage High Limit (3.3V).... RW

Offset 30 – Internal Core Voltage Low Limit (3.3V)..... RW

Offset 31 – VSENS3 Voltage High Limit (5V)..... RW

Offset 32 – VSENS3 Voltage Low Limit (5V) ..... RW

Offset 33 – VSENS4 Voltage High Limit (12V)..... RW

Offset 34 – VSENS4 Voltage Low Limit (12V) ..... RW

Offset 35 – Voltage Sense High Limit (-12V)..... RW

Offset 36 – Voltage Sense Low Limit (-12V) ..... RW

Offset 37 – Voltage Sense High Limit (-5V)..... RW

Offset 38 – Voltage Sense Low Limit (-5V) ..... RW

Offset 39 – TSENS1 Hot Temperature High Limit..... RW

Offset 3A – TSENS1Hot Temp Hysteresis Lo Limit..... RW

Offset 3B – FAN1 Fan Count Limit ..... RW

Offset 3C – FAN2 Fan Count Limit ..... RW

The above two locations store the number of counts of the internal clock per fan revolution for the low limit of the fan speed.

Offset 3D – TSENS2 Hot Temperature High Limit..... RW

Offset 3E – TSENS2 Hot Temp Hysteresis Lo Limit..... RW

Offset 3F – Stepping ID Number..... RW

Note: For high limits, comparisons are “greater than” comparisons. For low limits, comparisons are “less than or equal” comparisons.

One consequence of the above is that if high limits are set to all ones (FFh or 11111111b), interrupts are disabled for high limits (i.e., interrupts will only be generated for cases when voltages are equal to or below the low limits).

Offset 40 –Hardware Monitor Configuration .....RW

7 Initialization
- 0 Normal operation .....default
- 1 Restore power-up default values to this register, the interrupt status and mask registers, the FAN/RST#/OS# register, and the OS# Configuration / Temperature Resolution register. This bit automatically clears itself since the power-on default is 0.

6 Chassis Intrusion Reset
- 0 Normal operation .....default
- 1 Reset the Chassis Intrusion pin

5-4 Reserved (R/W)..... default = 0

3 Hardware Monitor Interrupt Clear
- 0 Normal operation
- 1 Clear the hardware monitor interrupt output (does not effect the contents of the interrupt status register). Normally set during interrupt service .....default

2 Reserved ..... always reads 0

1 Hardware Monitor Interrupt Enable
- 0 Disable hardware monitor interrupt output.. def
- 1 Enable hardware monitor interrupt output

0 Start
- 0 Place hardware monitor in standby mode.... def
- 1 Enable startup of hardware monitor logic. At startup, limit checking functions and scanning begins. All high and low limits should be set prior to turning on this bit. Note: the hardware monitor interrupt output will not be cleared if the user writes a zero to this bit after an interrupt has occurred (the hardware monitor interrupt clear bit must be used for this purpose).

Offset 41 –Hardware Monitor Interrupt Status 1.....RO

7 Fan 2 Error
- 0 No error.....default
- 1 Fan 2 count limit exceeded

6 Fan 1 Error
- 0 No error.....default
- 1 Fan 1 count limit exceeded

5 Reserved ..... always reads 0

4 TSENS1 Temperature Error
- 0 No error.....default
- 1 High or low hot temperature limit exceeded. The interrupt mode is determined by Temperature Resolution register Rx4B[1-0].

3 VSENS3 Voltage Error (5V)
- 0 No error.....default
- 1 High or low limit exceeded

2 Internal Core VCC Voltage Error (3.3V)
- 0 No error.....default
- 1 High or low limit exceeded

1 VSENS2 Voltage Error (2.5V NB Core Voltage)
- 0 No error.....default
- 1 High or low limit exceeded

0 VSENS1 Voltage Error (2.0V CPU Core Voltage)
- 0 No error.....default
- 1 High or low limit exceeded

Offset 42 –Hardware Monitor Interrupt Status 2.....RO

7 TSENS3 (Internal Bandgap) Temp Error
- 0 No error.....default
- 1 High or low hot temperature limit exceeded. Interrupt mode is determined by Rx4B[5-4].

6-5 Reserved ..... always reads 0

4 Chassis Error
- 0 No error.....default
- 1 Chassis Intrusion has gone high

3 TSENS2 Temperature Error
- 0 No error.....default
- 1 High or low hot temperature limit exceeded. Interrupt mode is determined by Rx4B[3-2].

2 Minus 5V Voltage Error (-5V)
- 0 No error.....default
- 1 High or low limit exceeded

1 Minus 12V Voltage Error (-12V)
- 0 No error.....default
- 1 High or low limit exceeded

0 VSENS4 Voltage Error (12V)
- 0 No error.....default
- 1 High or low limit exceeded

Note: When either status register is read, status conditions in that register are reset. In the case of voltage priority indications, if two or more voltages were out of limits, then another indication would automatically be generated if it was not handled during interrupt service. Errant voltages may be disabled in the control register until the operator has time to clear the errant condition or set the limit higher or lower.

Offset 43 –Hardware Monitor Interrupt Mask 1 ..... RW

7 Fan 2 Count Error Mask
- 0 Enable interrupt on error status bit set ..... def
- 1 Disable interrupt on error status bit set

6 Fan 1 Count Error Mask
- 0 Enable interrupt on error status bit set ..... def
- 1 Disable interrupt on error status bit set

5 TSENS1 Thermal Alarm Control Mask
- 0 Enable TSENS1 over-temp condition to control the thermal alarm (function 4 Rx40[7] automatic CPU clock throttling must be set)def
- 1 Disable

4 TSENS1 Temperature Error Mask
- 0 Enable interrupt on error status bit set ..... def
- 1 Disable interrupt on error status bit set

3 VSENS3 Voltage Error Mask (5V)
- 0 Enable interrupt on error status bit set ..... def
- 1 Disable interrupt on error status bit set

2 Internal Core VCC Voltage Error Mask (3.3V)
- 0 Enable interrupt on error status bit set ..... def
- 1 Disable interrupt on error status bit set

1 VSENS2 Voltage Error Mask (2.5V NB Core)
- 0 Enable interrupt on error status bit set ..... def
- 1 Disable interrupt on error status bit set

0 VSENS1 Voltage Error Mask (2.0V CPU Core)
- 0 Enable interrupt on error status bit set ..... def
- 1 Disable interrupt on error status bit set

Offset 44 –Hardware Monitor Interrupt Mask 2 ..... RW

7 TSENS3 Temperature Error Mask
- 0 Enable interrupt on error status bit set ..... def
- 1 Disable interrupt on error status bit set

6 TSENS3 Thermal Alarm Control Mask
- 0 Enable TSENS3 over-temp condition to control the thermal alarm (function 4 Rx40[7] automatic CPU clock throttling must be set) def
- 1 Disable

5 TSENS2 Thermal Alarm Control Mask
- 0 Enable TSENS2 over-temp condition to control the thermal alarm (function 4 Rx40[7] automatic CPU clock throttling must be set) def
- 1 Disable

4 Chassis Error Mask
- 0 Enable interrupt on error status bit set ..... def
- 1 Disable interrupt on error status bit set

3 TSENS2 Temperature Error Mask
- 0 Enable interrupt on error status bit set ..... def
- 1 Disable interrupt on error status bit set

2 Minus 5V Voltage Error Mask (-5V)
- 0 Enable interrupt on error status bit set ..... def
- 1 Disable interrupt on error status bit set

1 Minus 12V Voltage Error Mask (-12V)
- 0 Enable interrupt on error status bit set ..... def
- 1 Disable interrupt on error status bit set

0 VSENS4 Voltage Error Mask (12V)
- 0 Enable interrupt on error status bit set ..... def
- 1 Disable interrupt on error status bit set

Offset 47 –Hardware Monitor Fan Configuration.....RW

7-6 Fan 2 RPM Control
- 00 Divide by 1
- 01 Divide by 2 .....default
- 10 Divide by 4
- 11 Divide by 8

5-4 Fan 1 RPM Control
- 00 Divide by 1
- 01 Divide by 2 .....default
- 10 Divide by 4
- 11 Divide by 8

3-0 Reserved ..... always reads 0

Offset 49 –Hardware Monitor Temp Low Order Value RW

7-6 TSENS3 Value Low-Order Bits
Upper 8 bits are stored in offset 1Fh

5-4 TSENS2 Value Low-Order Bits
Upper 8 bits are stored in offset 21h

3 Over Temperature Active Low for PMU to Control Stop Clock
- 0 Disable .....default
- 1 Enable

2 Chassis Active Low Output 20 msec
- 0 Disable .....default
- 1 Enable

1 Interrupt Active High Output
- 0 Disable .....default
- 1 Enable

0 Reserved ..... always reads 0

Offset 4B –Temperature Interrupt Configuration ..... RW

7-6 TSENS1 Value Low-Order Bits .....def = 00
Upper 8 bits are stored in offset 20h

5-4 TSENS3 Hot Temp Interrupt Mode .....def = 01

3-2 TSENS2 Hot Temp Interrupt Mode .....def = 01

1-0 TSENS1 Hot Temp Interrupt Mode .....def = 01

The following applies to each of the above 3 fields
- 00 Default Interrupt Mode. An interrupt occurs if the temperature goes above the hot limit. The interrupt will be cleared once the status register is read, but will be generated again when the next conversion is completed. Interrupts will continue to be generated until the temperature goes below the hysteresis limit.
- 01 One-Time Interrupt Mode. An interrupt is generated if the temperrature goes above the hot limit. The interrupt will be cleared when the status register is read. Another interrupt will not be generated until the temperature first drops below the hysteresis limit.....default
- 10 Comparator mode. An interrupt occurs if the temperature goes above the hot limit. This interrupt remains active until the temperature goes below the hot limit (i.e., no hysteresis).
- 11 Default Interrupt Mode (same as 00)

Function 5 & 6 Registers - AC97 Audio & Modem Codecs

The codec interface is hardware compatible with AC97 and SoundBlaster Pro. There are two sets of software accessible registers: PCI configuration registers and I/O registers. The PCI configuration registers for the **Audio Codec** are located in the **function 5** PCI configuration space of the VT82C686A. The PCI configuration registers for the **Modem Codec** are located in the **function 6** PCI configuration space. The I/O registers are located in the system I/O space.

PCI Configuration Space Header – Function 5 Audio

Offset 1-0 - Vendor ID ..... RO

0-7 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID ..... RO

0-7 Device ID (3058h = 82C686A Audio Codec)

Offset 5-4 - Command ..... RW

15-10 Reserved ..... always reads 0
9 Fast Back-to-Back ..... fixed at 0
8 SERR# Enable ..... fixed at 0
7 Address Stepping ..... fixed at 0
6 Parity Error Response ..... fixed at 0
5 VGA Palette Snoop ..... fixed at 0
4 Memory Write and Invalidate ..... fixed at 0
3 Special Cycle Monitoring ..... fixed at 0
2 Bus Master ..... fixed at 0
1 Memory Space ..... fixed at 0
0 I/O Space ..... default=0 (disabled)

Offset 7-6 - Status ..... RWC

15 Detected Parity Error ..... always reads 0
14 Signalled System Error ..... default=0
13 Received Master Abort ..... fixed at 0
12 Received Target Abort ..... fixed at 0
11 Signalled Target Abort ..... fixed at 0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... fixed
10 Slow
11 Reserved
8 Data Parity Error ..... fixed at 0
7 Fast Back-to-Back Capable ..... fixed at 0
6-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) ..... **RO**

7-0 Silicon Revision Code
10h Revision A
11h Revision B
12h Revision C
13h Revision D
14h Revision E
20h Revision H

Offset 9 - Programming Interface (00h) ..... **RO**

Offset A - Sub Class Code (01h=Audio Device) ..... **RO**

Offset B - Base Class Code (04h=Multimedia Device) ..... **RO**

Offset D - Latency Timer (00h) ..... **RO**

Offset E - Header Type (00h) ..... **RO**

Offset F - BIST (00h) ..... **RO**

Offset 13-10 - Base Address 0 – SGD Control / Status .. RW

31-16 Reserved ..... always reads 0
15-8 Base Address ..... default = 00h
7-0 00000001b (256 bytes)

Offset 17-14 - Base Address 1 – FM NMI Status ..... RW

31-16 Reserved ..... always reads 0
15-2 Base Address ..... default = 0000h
1-0 01b (4 bytes)

Offset 1B-18 - Base Address 2 – MIDI Port (Rev H)..... RW

31-16 Reserved ..... always reads 0
15-2 Base Address ..... default = 0330h
1-0 01b (4 bytes)

Offset 2F-2C – Subsystem ID / Sub Vendor ID (Rev H) RO*

*This register is RW if function 5-6 Rx48[4] = 1

Offset 34 – Capture Pointer (Rev H) (Default = C0h) .... RO

Offset 3C - Interrupt Line ..... RW

7-4 Reserved ..... always reads 0
3-0 Audio Interrupt Routing
0000 Disabled ..... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 IRQ8
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 IRQ13
1110 IRQ14
1111 Disabled

Offset 3D - Interrupt Pin (03h) ..... **RO**

Offset 3E - Minimum Grant (00h) ..... **RO**

Offset 3F - Minimum Latency (00h) ..... **RO**

PCI Configuration Space Header – Function 6 Modem

Offset 1-0 - Vendor ID .....RO

0-7 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID.....RO

0-7 Device ID (3068h = 82C686A Modem Codec)

Offset 5-4 - Command.....RW

15-10 Reserved ..... always reads 0
9 Fast Back-to-Back.....fixed at 0
8 SERR# Enable.....fixed at 0
7 Address Stepping .....fixed at 0
6 Parity Error Response.....fixed at 0
5 VGA Palette Snoop .....fixed at 0
4 Memory Write and Invalidate .....fixed at 0
3 Special Cycle Monitoring .....fixed at 0
2 Bus Master .....fixed at 0
1 Memory Space.....fixed at 0
0 I/O Space ..... default=0 (disabled)

Offset 7-6 - Status.....RWC

15 Detected Parity Error..... always reads 0
14 Signalled System Error.....fixed at 0
13 Received Master Abort.....fixed at 0
12 Received Target Abort .....fixed at 0
11 Signalled Target Abort.....fixed at 0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... fixed
10 Slow
11 Reserved
8 Data Parity Error.....fixed at 0
7 Fast Back-to-Back Capable.....fixed at 0
6-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) .....RO

7-0 Silicon Revision Code (0 indicates first silicon)

Offset 9 - Programming Interface (00h) .....*RO

Offset A - Sub Class Code (80h).....*RO

Offset B - Base Class Code (07h).....*RO

*Registers 9-B are RW if function 5-6 Rx44[5] = 1

Offset D - Latency Timer (00h) .....RO

Offset E - Header Type (00h) .....RO

Offset F - BIST (00h).....RO

Offset 13-10 - Base Address 0 – SGD Control / Status .. RW

31-16 Reserved .....always reads 0
15-8 Base Address.....default = 00h
7-0 00000001b (256 bytes)

Offset 3C - Interrupt Line..... RW

7-4 Reserved .....always reads 0
3-0 Audio Interrupt Routing
0000 Disabled..... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 IRQ8
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 IRQ13
1110 IRQ14
1111 Disabled

Offset 3D - Interrupt Pin (03h).....RO

Offset 3E - Minimum Grant (00h).....RO

Offset 3F - Minimum Latency (00h).....RO

Function 5 & 6 Codec-Specific Configuration Registers

Offset 40 – AC97 Interface Status .....RO

7-3 Reserved ..... always reads 0

2 Secondary Codec Ready Status .....RO
- 0 Codec Not Ready
- 1 Codec Ready (AC97 ctrlr can access codec)

1 AC97 Codec Low-Power Status.....RO
- 0 AC97 Codec not in low-power mode
- 1 AC97 Codec in low-power mode

0 AC97 Codec Ready Status.....RO
- 0 Codec Not Ready
- 1 Codec Ready (AC97 ctrlr can access codec)

Offset 41 – AC Link Interface Control ..... RW

7 AC-Link Interface Enable (ENAC97)
- 0 Disable..... default
- 1 Enable

6 AC-Link Reset (ACRST#)
- 0 Assert AC-Link Reset..... default
- 1 De-assert AC-Link Reset

5 AC-Link Sync (RSYNCHI)
- 0 Release SYNC ..... default
- 1 Force SYNC High

4 AC-Link Serial Data Out
- 0 Release SDO..... default
- 1 Force SDO High

3 Variable-Sample-Rate On-Demand Mode
- 0 Disable..... default
- 1 Enable

Bit valid in function 5 only (reserved in function 6)

2 AC Link SGD Read Channel PCM Data Output
- 0 Disable..... default
- 1 Enable

Bit valid in function 5 only (reserved in function 6)

1 AC Link FM Channel PCM Data Out (SELFM)
- 0 Disable..... default
- 1 Enable

Bit valid in function 5 only (reserved in function 6)

0 AC Link SB PCM Data Output (SELSB)
- 0 Disable..... default
- 1 Enable

Bit valid in function 5 only (reserved in function 6)

Offset 42 – Function Enable .....RW (Function 5)
Offset 42 – Function Enable .....RO (Function 6)

7 Reserved ..... always reads 0

6 MIDI PnP (Rev H)
- 0 MIDI Port Address Selected by Rx43[3-2]. def
- 1 MIDI Port Address Selected by IOBase2

5 Function 5 Config Reg Rx2C Writable (Rev H)
- 0 F5Rx2C-2F RO .....default
- 1 F5Rx2C-2F RW

4 Gate SoundBlaster PCM When FIFO Empty
- 0 Disable .....default
- 1 Enable

3 Game Port Enable (ENGAME)
- 0 Disable .....default
- 1 Enable (200-207h)

2 FM Enable (ENFM)
- 0 Disable .....default
- 1 Enable (388-38B)

1 MIDI Enable (ENMIDI)
- 0 Disable .....default
- 1 Enable

0 SoundBlaster Enable (ENSB)
- 0 Disable .....default
- 1 Enable

Offset 43 – Plug and Play Control .....RW (Function 5)
Offset 43 – Plug and Play Control .....RO (Function 6)

7-6 SoundBlaster IRQ Select (SBIRQS[1:0])
- 00 IRQ5 .....default
- 01 IRQ7
- 10 IRQ9
- 11 IRQ10

5-4 SoundBlaster DRQ Select (SBDRQS[1:0])
- 00 DMA Channel 0
- 01 DMA Channel 1 .....default
- 10 DMA Channel 2
- 11 DMA Channel 3

3-2 MIDI Decode Select (MIDIBASE)
- 00 300-303h
- 01 310-313h
- 10 320-323h
- 11 330-333h .....default

1-0 SoundBlaster Decode Select (SBBASE)
- 00 220-22Fh .....default
- 01 240-24Fh
- 10 260-26Fh
- 11 280-28Fh

Offset 44 – MC97 Interface Control ..... RO (Function 5)
Offset 44 – MC97 Interface Control ..... RW (Function 6)

7 Function 5 AC-Link Interface Access
- 0 Disable..... default
- 1 Enable

6 Secondary Codec Support
- 0 Disable..... default
- 1 Enable

5 Function 6 Config Reg Rx9-B Writable (Rev H)
- 0 F6Rx9-B RO..... default
- 1 F6Rx9-B RW

4 Function 6 Config Reg 2Ch Writable (Rev H)
- 0 F6Rx2C-2F RO..... default
- 1 F6Rx2C-2F RW

3-0 Reserved .....always reads 0

Offset 48 – FM NMI Control..... RW (Function 5)
Offset 48 – FM NMI Control..... RO (Function 6)

7-6 Reserved .....always reads 0

5 Function 5 Config Reg Rx2C Writable (Rev H)
- 0 F5Rx2C-2F RO..... default
- 1 F5Rx2C-2F RW

4 Reserved .....always reads 0

2 FM IRQ Select (FMIRQS)
- 0 Route FM Trap interrupt to NMI..... default
- 1 Route FM Trap interrupt to IRQ

1 FM SGD Data for SoundBlaster Mixing
- 0 Disable..... default
- 1 Enable

0 FM Trap Interrupt (EN_FMI
- 0 Enable..... default
- 1 Disable

I/O Base 0 Registers –Audio/Modem Scatter/Gather DMA

Read / Write through function 5, R/O through function 6.

I/O Offset 0 – Audio SGD Read Channel Status .....RWC

- **7 SGD Active (0 = completed or terminated).....RO**
- **6 SGD Paused .....RO**
- **5-4 Reserved** ..... always reads 0
- **3 SGD Trigger Queued (will restart after EOL) ..RO**
- **2 SGD Stopped (write 1 to resume) .....RWC**
- **1 SGD EOL .....RWC**
- **0 SGD Flag .....RWC**

I/O Offset 1 – Audio SGD Read Channel Control.....RW

- **7 SGD Start .....WO (always reads 0)**
  - 0 No effect
  - 1 Start SGD read channel operation
- **6 SGD Terminate .....WO (always reads 0)**
  - 0 No effect
  - 1 Terminate SGD read channel operation
- **5-4 Reserved** .....always reads 0, writing 1 not allowed
- **3 SGD Pause**
  - 0 Release SGD read channel pause and resume the transfer from the paused line
  - 1 Pause SGD read channel operation (SGD read channel pointer stays at the current address)
- **2-0 Reserved** ..... always reads 0

I/O Offset 2 – Audio SGD Read Channel Type .....RW

- **7 Auto-Start SGD at EOL** (1=Enable) ..... default = 0
- **6 Reserved** ..... always reads 0
- **5 PCM 16-Bit Format**
  - 0 8-Bit Format.....default
  - 1 16-Bit Format
- **4 PCM Stereo Format**
  - 0 Mono Format.....default
  - 1 Stereo Format
- **3-2 Interrupt Select**
  - 00 Interrupt at PCI Read of Last Line .....default
  - 01 Interrupt at Last Sample Sent
  - 10 Interrupt at Less Than One Line to Send
  - 11 -reserved-
- **1 Interrupt on EOL @ End of Block** (1=Ena)... def=0
- **0 Interrupt on FLAG @ End-of-Blk** (1=Ena) ... def=0

I/O Offset 7-4 – Audio SGD R Ch Table Pointer Base...RW

- **31-0 SGD Table Pointer Base Address (even addr).....W**
  Current Pointer Address .....R

I/O Offset F-C – Audio SGD R Ch Current Count .....RO

- **31-24 Reserved** ..... always reads 0
- **23-0 Current SGD Read Channel Count**

SGD Table Format

63	62	61	60-56	55-32	31-0
EOL	FLAG	STOP	-reserved-	Base Count [23:0]	Base Address [31:0]

I/O Offset 10 – Audio SGD Write Channel Status.....RO

- **7 SGD Active (0 = completed or terminated) .....RO**
- **6 SGD Paused .....RO**
- **5-4 Reserved** .....always reads 0
- **3 SGD Trigger Queued (will restart after EOL)..RO**
- **2 SGD Stopped (write 1 to resume)..... RWC**
- **1 SGD EOL ..... RWC**
- **0 SGD Flag ..... RWC**

I/O Offset 11 – Audio SGD Write Channel Control..... RW

- **7 SGD Start .....WO (always reads 0)**
  - 0 No effect
  - 1 Start SGD write channel operation
- **6 SGD Terminate.....WO (always reads 0)**
  - 0 No effect
  - 1 Terminate SGD write channel operation
- **5-4 Reserved** .... always reads 0, writing 1 not allowed
- **3 SGD Pause**
  - 0 Release SGD write channel pause and resume the transfer from the paused line
  - 1 Pause SGD write channel operation (SGD write channel pointer stays at current address)
- **2-0 Reserved** .....always reads 0

I/O Offset 12 – Audio SGD Write Channel Type..... RW

- **7 Auto-Start SGD at EOL** (1=Enable).....default = 0
- **6 Reserved** .....always reads 0
- **5 PCM 16-Bit Format**
  - 0 8-Bit Format ..... default
  - 1 16-Bit Format
- **4 PCM Stereo Format**
  - 0 Mono Format ..... default
  - 1 Stereo Format
- **3-2 Reserved** .....always reads 0
- **1 Interrupt on EOL @ End of Block** (1=Ena) ...def=0
- **0 Interrupt on FLAG @ End-of-Blk** (1=Ena)....def=0

I/O Offset 17-14 – Audio SGD W Ch Table Pointer BaseRW

- **31-0 SGD Table Pointer Base Address (even addr) .... W**
  Current Pointer Address ..... R

I/O Offset 1F-1C – Audio SGD W Ch Current Count ... RO

- **31-24 Reserved** .....always reads 0
- **23-0 Current SGD Write Channel Count**

EOL End Of Link. 1 indicates this block is the last of the link. If the channel "Interrupt on EOL" bit is set, then an interrupt is generated at the end of the transfer.

FLAG Block Flag. If set, transfer pauses at the end of this block. If the channel "Interrupt on FLAG" bit is set, then an interrupt is generated at the end of this block.

STOP Block Stop. If set, transfer pauses at the end of this block. To resume the transfer, write 1 to Rx?0[2].

Read / Write through function 5, R/O through function 6.

The following set of registers is dedicated for FM:

I/O Offset 20 – FM SGD Read Channel Status .....RWC

- **7 SGD Active (0 = completed or terminated).....RO**
- **6 SGD Paused.....RO**
- **5-4 Reserved** ..... always reads 0
- **3 SGD Trigger Queued (will restart after EOL) ..RO**
- **2 SGD Stopped (write 1 to resume) .....RWC**
- **1 SGD EOL .....RWC**
- **0 SGD Flag .....RWC**

I/O Offset 21 – FM SGD Read Channel Control.....RW

- **7 SGD Start .....WO (always reads 0)**
  - 0 No effect
  - 1 Start SGD read channel operation
- **6 SGD Terminate .....WO (always reads 0)**
  - 0 No effect
  - 1 Terminate SGD read channel operation
- **5-4 Reserved** .....always reads 0, writing 1 not allowed
- **3 SGD Pause .....RW**
  - 0 Release SGD read channel pause and resume the transfer from the paused line
  - 1 Pause SGD read channel operation (SGD read channel pointer stays at the current address)
- **2-0 Reserved** ..... always reads 0

I/O Offset 22 – FM SGD Read Channel Type .....RW

- **7 Auto-Start SGD at EOL** (1=Enable) ..... default = 0
- **6-4 Reserved** ..... always reads 0
- **3-2 Interrupt Select**
  - 00 Interrupt at PCI Read of Last Line .....default
  - 01 Interrupt at Last Sample Sent
  - 10 Interrupt at Less Than One Line to Send
  - 11 -reserved-
- **1 Interrupt on EOL @ End of Block**
  - 0 Disable .....default
  - 1 Enable
- **0 Interrupt on FLAG @ End-of-Blk**
  - 0 Disable .....default
  - 1 Enable

I/O Offset 27-24 – FM SGD Rd Ch Table Pointer Base RW

- **31-0 SGD Table Pointer Base Address (even addr).....W**
  Current Pointer Address.....R

I/O Offset 2F-2C – FM SGD Rd Chan Current Count...RO

- **31-24 Reserved** ..... always reads 0
- **23-0 Current SGD FM Read Channel Count**

Read / Write through function 6, R/O through function 5.

I/O Offset 40 – Modem SGD Read Channel Status.....RWC

7 SGD Active (0 = completed or terminated).....RO
6 SGD Paused.....RO
5-4 Reserved ..... always reads 0
3 SGD Trigger Queued (will restart after EOL) ..RO
2 SGD Stopped (write 1 to resume) .....RWC
1 SGD EOL .....RWC
0 SGD Flag .....RWC

I/O Offset 41 – ModemSGD Read Channel Control .....RW

7 SGD Start .....WO (always reads 0)
0 No effect
1 Start SGD read channel operation
6 SGD Terminate .....WO (always reads 0)
0 No effect
1 Terminate SGD read channel operation
5-4 Test (Do Not Program).....always write 0
3 SGD Pause .....RW
0 Release SGD read channel pause and resume the transfer from the paused line
1 Pause SGD read channel operation (SGD read channel pointer stays at the current address)
2-0 Reserved ..... always reads 0

I/O Offset 42 – Modem SGD Read Channel Type.....RW

7 Auto-Start SGD at EOL (1=Enable) ..... default = 0
6-4 Reserved ..... always reads 0
3-2 Interrupt Select
00 Interrupt at PCI Read of Last Line .....default
01 Interrupt at Last Sample Sent
10 Interrupt at Less Than One Line to Send
11 -reserved-
1 Interrupt on EOL @ End of Block
0 Disable .....default
1 Enable
0 Interrupt on FLAG @ End-of-Blk
0 Disable .....default
1 Enable

I/O Offset 47-44 – Modem SGD R Ch Table Ptr Base...RW

31-0 SGD Table Pointer Base Address (even addr).....W
Current Pointer Address.....R

I/O Offset 4F-4C – Modem SGD R Ch Current Count ..RO

31-24 Reserved ..... always reads 0
23-0 Current SGD Read Channel Count

SGD Table Format

63	62	61	60-56	55-32	31-0
EOL	FLAG	STOP	-reserved-	Base Count [23:0]	Base Address [31:0]

I/O Offset 50 – ModemSGD Write Channel Status ..... RO

7 SGD Active (0 = completed or terminated) ..... RO
6 SGD Paused ..... RO
5-4 Reserved .....always reads 0
3 SGD Trigger Queued (will restart after EOL).. RO
2 SGD Stopped (write 1 to resume)..... RWC
1 SGD EOL ..... RWC
0 SGD Flag ..... RWC

I/O Offset 51 – Modem SGD Write Channel Control ... RW

7 SGD Start .....WO (always reads 0)
0 No effect
1 Start SGD write channel operation
6 SGD Terminate.....WO (always reads 0)
0 No effect
1 Terminate SGD write channel operation
5-4 Test (Do Not Program)..... always write 0
3 SGD Pause ..... RW
0 Release SGD write channel pause and resume the transfer from the paused line
1 Pause SGD write channel operation (SGD write channel pointer stays at current address)
2-0 Reserved .....always reads 0

I/O Offset 52 – Modem SGD Write Channel Type ..... RW

7 Auto-Start SGD at EOL (1=Enable).....default = 0
6-2 Reserved .....always reads 0
1 Interrupt on EOL @ End of Block (1=Ena) ...def=0
0 Interrupt on FLAG @ End-of-Blk (1=Ena)....def=0

I/O Offset 57-54 – Modem SGD W Ch Table Ptr Base . RW

31-0 SGD Table Pointer Base Address (even addr) .... W
Current Pointer Address ..... R

I/O Offset 5F-5C – Modem SGD W Ch Current Count. RO

31-24 Reserved .....always reads 0
23-0 Current SGD Write Channel Count

EOL End Of Link. 1 indicates this block is the last of the link. If the channel "Interrupt on EOL" bit is set, then an interrupt is generated at the end of the transfer.

FLAG Block Flag. If set, transfer pauses at the end of this block. If the channel "Interrupt on FLAG" bit is set, then an interrupt is generated at the end of this block.

STOP Block Stop. If set, transfer pauses at the end of this block. To resume the transfer, write 1 to Rx?0[2].

The audio / modem interface is compliant with AC97. Refer to the AC97 specification and AC97 Codec data sheets for further details.

Read / Write through both functions 5 and 6.

Offset 83-80 – AC97 Controller Command / Status .....RW

Read / Write through both functions 5 and 6.

31-30 Codec ID ..... RW
- 00 Select Primary Codec
- 01 Select Secondary Codec
- 1x -reserved-

29-28 Reserved ..... always reads 0

27 Secondary Codec Data / Status / Index Valid.RWC
- 0 Not Valid
- 1 Valid (OK to Read bits 0-23)

26 Reserved ..... always reads 0

25 Primary Codec Data / Status / Index Valid.....RWC
- 0 Not Valid
- 1 Valid (OK to Read bits 0-23)

24 AC97 Controller Busy ..... RO
- 0 Primary Codec is ready for a register access command
- 1 AC97 Controller is sending a command to the primary codec (commands are not accepted)

23 Codec Command Register Write Mode ..... RW
- 0 Select Codec command register write mode
- 1 Select Codec command register read mode

22-16 Codec Command Register Index [7:1] ..... RW

Index of the AC97 codec command register to access (in the attached codec). Data must be written before or at the same time as Index as writing to the index triggers the AC97 controller to access the addressed codec register over the AC-link interface.

15-0 Codec Command Register Data / Status ..... RW
- W Codec Command Register Data
- R Codec Status Register Data

Offset 87-84 – SGD Status Shadow ..... RO

Read / Only through both functions 5 and 6.

31-30 Reserved ..... always reads 0
29 Modem Write Chan SGD Active Shadow (Rx50[7])
28 Modem Read Chan SGD Active Shadow (Rx40[7])
27-26 Reserved ..... always reads 0
25 Modem Write Chan SGD STOP Shadow (Rx50[2])
24 Modem Read Chan SGD STOP Shadow. (Rx40[2])

23-22 Reserved ..... always reads 0
21 Modem Write Chan SGD EOL Shadow.. (Rx50[1])
20 Modem Read Chan SGD EOL Shadow... (Rx40[1])
19-18 Reserved ..... always reads 0
17 Modem Write Chan SGD FLAG Shadow (Rx50[0])
16 Modem Read Chan SGD FLAG Shadow (Rx40[0])

15 Reserved ..... always reads 0
14 FM Channel SGD Active Shadow..... (Rx20[7])
13 Audio Write Chan SGD Active Shadow.. (Rx10[7])
12 Audio Read Chan SGD Active Shadow... (Rx00[7])
11 Reserved ..... always reads 0
10 FM Channel SGD STOP Shadow ..... (Rx20[2])
9 Audio Write Chan SGD STOP Shadow .. (Rx10[2])
8 Audio Read Chan SGD STOP Shadow ... (Rx00[2])

7 Reserved ..... always reads 0
6 FM Channel SGD EOL Shadow ..... (Rx20[1])
5 Audio Write Chan SGD EOL Shadow .... (Rx10[1])
4 Audio Read Chan SGD EOL Shadow ..... (Rx00[1])
3 Reserved ..... always reads 0
2 FM Channel SGD FLAG Shadow..... (Rx20[0])
1 Audio Write Chan SGD FLAG Shadow.. (Rx10[0])
0 Audio Read Chan SGD FLAG Shadow... (Rx00[0])

Read / Only through function 5 and Read / Write through function 6:

Offset 8B-88 – Codec GPI Interrupt Status / GPIO ... RWC

31-16 GPI Interrupt Status ..... RWC
- R GPI[15-0] Interrupt Status
- W 1 to clear

15-0 Codec GPIO ..... RW
- R Reflect status of Codec GPI[15-0]
- W Triggers AC-Link slot-12 output to codec

Offset 8F-8C – Codec GPI Interrupt Enable ..... RW

31-16 Interrupt on GPI[15-0] Change of Status..... RW
- 0 Disable
- 1 Enable

15-0 Reserved ..... always reads 0

I/O Base 1 Registers –Audio FM NMI Status Registers

These registers are accessable through **function 5 only.**

I/O Offset 0 – FM NMI Status .....RO

7-2 Reserved ..... always reads 0

1-0 FM NMI Status

00 Undefined
01 OPL3 Bank 0
10 OPL3 Bank 1
11 Undefined

I/O Offset 1 – FM NMI Data.....RO

7-0 FM NMI Data

This register allows readback of the data written to the FM data port

I/O Offset 2 – FM NMI Index .....RO

7-0 FM NMI Index

This register allows readback of the data written to the FM index port

I/O Base 2 Registers –MIDI / Game Port (Rev H)

I/O Offset 1-0 – MIDI Base..... RW

15-0 MIDI Port Base Address.....default = 0330h

This register is functional only if Rx42[6] = 1

I/O Offset 3-2 – Game Port Base ..... RW

15-0 Game Port Base Address .....default = 0200h

FUNCTIONAL DESCRIPTIONS

Power Management

Power Management Subsystem Overview

The power management function of the VT82C686A is indicated in the following block diagram:

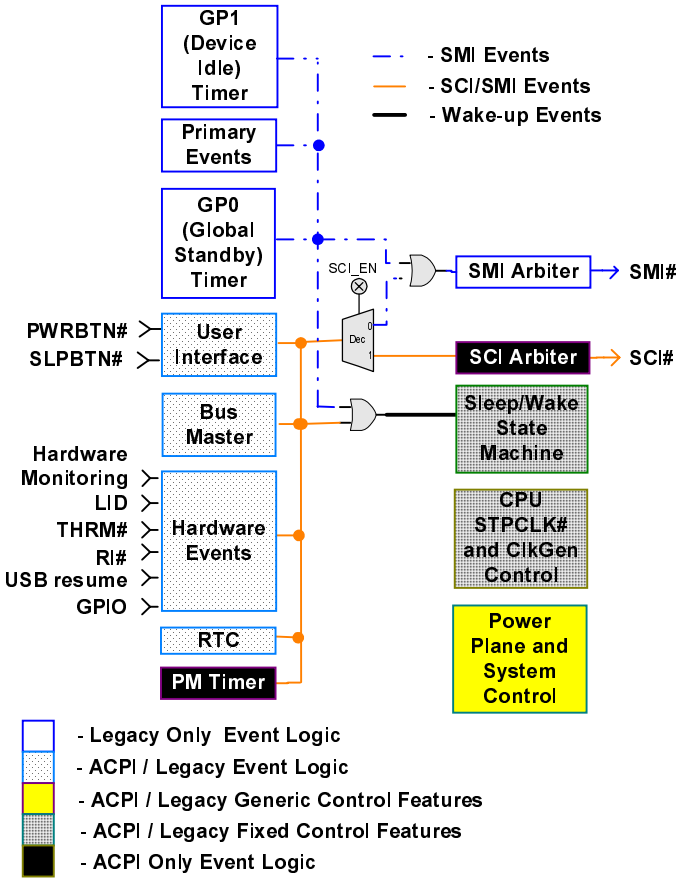

Figure 6. Power Management Subsystem Block Diagram

Refer to ACPI Specification v1.0 and APM specification v1.2 for additional information.

Processor Bus States

The VT82C686A supports the complete set of C0 to C3 processor states as specified in the Advanced Configuration and Power Interface (ACPI) specification (and defined in ACPI I/O space Registers 10-15):

C0: Normal Operation

C1: CPU Halt (controlled by software).

C2: Stop Clock. Entered when the P_LVL2 register is read. The STPCLK# signal is asserted to put the processor in the Stop Grant State. The CPUSTP# signal is not asserted so that host clocks remain running. To exit this state, the chip negates STPCLK#.

C3: Suspend. Entered when the P_LVL3 register is read. In addition to STPCLK# assertion as in the C2 state, the SUSST1# (suspend status 1) signal is asserted to tell the north bridge to switch to "Suspend DRAM Refresh" mode based on the 32KHz suspend clock (SUSCLK) provided by the VT82C686A. If the HOST_STP bit is enabled, then CPUSTP# is also asserted to stop clock generation and put the CPU into Stop Clock State. To exit this state, the chip negates CPUSTP# and allows time for the processor PLL to lock. Then the SUSST1# and STPCLK# signals are negated to resume to normal operation.

During normal operation, two mechanisms are provided to modulate CPU execution and control power consumption by throttling the duty cycle of STPCLK#:

a. Setting the THT_EN bit to 1, the duty cycle defined in THT_DTY (IO space Rx10) is used.

b. THRM# pin assertion enables automatic clock throttling with duty cycle pre-configured in THM_DTY (PCI configuration Rx4C).

System Suspend States and Power Plane Control

There are three power planes inside the VT82C686A. The first power plane (VCCS) is always on unless turned off by the mechanical switch. The second power plane (VCC) is controlled by chip output SUSC# (also called "PSON"). The third plane (VCCRTC) is powered by the combination of the VCCS and the external battery (VBAT) for the integrated real time clock. Most of the circuitry inside the VT82C686A is powered by VCC. The amount of logic powered by VCCS is very small; its main function is to control the supply of VCC and other power planes. VCCRTC is always on unless both the mechanical switch and VBAT are removed.

The VT82C686A supports multiple system suspend states by configuring the SLP_TYP field of ACPI I/O space register Rx4-5:

a) **POS (Power On Suspend):** Most devices in the system remain powered. The host bus is put into an equivalent of the C3 state. In particular, the CPU is put into the Stop Grant State or Stop Clock State depending on the setting of the HOST_STP bit. SUSST1# is asserted to tell the north bridge to switch to "Suspend DRAM Refresh" mode based on the 32KHz SUSCLK provided by the VT82C686A. As to the PCI bus, setting the PCLK_RUN bit to 0 enables the CLKRUN protocol defined in the PCI Mobile Design Guide. That is, the PCKRUN# pin will be de-activated after the PCI bus is idle for 26 clocks. Any PCI bus masters including the north bridge may resume PCI clock operation by pulling the PCKRUN# pin low. During the PCKRUN# de-activation period, the PCISTP# pin may be activated to disable the output of the PCI clock generator if the PCI_STP bit is enabled. When the system resumes from POS, the VT82C686A can optionally resume without resetting the system, can reset the processor only, or can reset the entire system. When no reset is performed, the chip only needs to wait for the clock synthesizer and processor PLL to lock before the system is resumed, which typically takes 20ms.

b) **STR (Suspend to RAM):** Power is removed from most of the system except the system DRAM. Power is supplied to the suspend refresh logic in the north bridge (VTT of VT82C598) and the suspend logic of the VT82C686A (VCCS). The VT82C686A provides a 32KHz suspend clock to the north bridge for it to use to continue DRAM refresh.

c) **STD (Suspend to Disk, also called Soft-off):** Power is removed from most of the system except the suspend logic of VT82C686A (VCCS).

d) **Mechanical Off:** This is not a suspend state. All power in the system is removed except the RTC battery.

The suspend state is entered by setting the SLP_EN bit to 1. Three power plane control signals (SUSA#, SUSB# and SUSC#) are provided to turn off more system power planes as the system moves to deeper power-down states, i.e., from normal operation to POS (only SUSA# asserted), to STR (both SUSA# and SUSB# asserted), and to STD (all three SUS# signals asserted). In particular, the assertion of SUSC# can be used to turn off the VCC supply to the VT82C686A.

One additional suspend status indicator (SUSST1#) is provided to inform the north bridge and the rest of the system of the processor and system suspend states. SUSST1# is asserted when the system enters the suspend state or the processor enters the C3 state. SUSST1# is connected to the north bridge to switch between normal and suspend-DRAM-refresh modes.

General Purpose I/O Ports

As ACPI compliant hardware, the VT82C686A includes PWRBTN#, SLPBTN#, and RI# pins to implement power button, sleep button, and ring indicator functionality, respectively. Furthermore, the VT82C686A offers many general-purpose I/O ports with the following capabilities:

- **I^2C/SMB Support**
- **Thermal Detect**
- **Notebook Lid Open/Close Detect**
- **Battery Low Detect**
- **Twelve General Purpose Input Ports** (multiplexed with other functions).
- **Nineteen General Purpose Output Ports** (1 dedicated and 18 multiplexed with other functions)
- **Four General Purpose Input / Output Ports** (multiplexed with other functions)

In addition, the VT82C686A provides an external dedicated SMI pin (EXTSMI#). The external SMI input can be programmed to trigger an SCI or SMI at both the rising and falling edges of the corresponding input signal. Software can check the status of the input pin and take appropriate actions.

Power Management Events

Three types of power management events are supported:

1) **ACPI-required Fixed Events** defined in the PM1a_STS and PM1a_EN registers. These events can trigger either SCI or SMI depending on the SCI_EN bit:
   - PWRBTN# Triggering
   - RTC Alarm
   - Sleep Button
   - ACPI Power Management Timer Carry (always SCI)
   - BIOS Release (always SCI)

2) **ACPI-aware General Purpose Function Events** defined in the GP_STS and GP_SCI_EN, and GP_SMI_EN registers. These events can trigger either SCI or SMI depending on the setting of individual SMI and SCI enable bits:
   - External SMI triggering
   - USB Resume
   - Ring Indicator (RI#)
   - Battery Low Detect (BATLOW#)
   - Notebook Lid Open/Close Detect (LID)
   - Thermal Detect (THRM#)

3) **Generic Global Events** defined in the GBL_STS and GBL_EN registers. These registers are mainly used for SMI:
   - PCI Bus Clock Run Resume
   - Primary Interrupt Occurance
   - GP0 and GP1 Timer Time Out
   - Secondary Event Timer Time Out
   - Occurrence of Primary Events (defined in register PACT_STS and PACT_EN)
   - Legacy USB accesses (keyboard and mouse)
   - Software SMI

System and Processor Resume Events

Depending on the system suspend state, different features can be enabled to resume the system. There are two classes of resume events:

a) VCCS-based events. Event logic resides in the VCCS plane and thus can resume the system from any suspend state. Such events include PWRBTN#, RI#, BATLOW#, LID, SMBus resume event, RTC alarm, EXTSMI#, and GP1 (EXTSMI1#).

b) VCC-Based Events. Event logic resides in the VCC plane and thus can only resume the system from the POS state. Such events include the ACPI PM timer, USB resume, and EXTSMIn#.

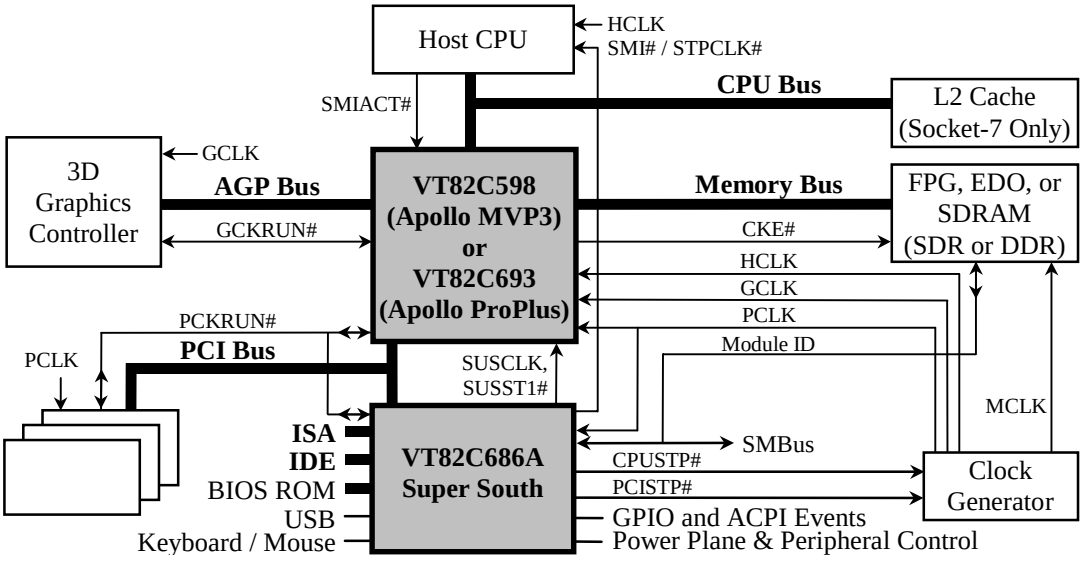

Figure 7. System Block Diagram Using the VT82C686A Super South Bridge

Legacy Power Management Timers

In addition to the ACPI power management timer, the VT82C686A includes the following four legacy power management timers:

GP0 Timer: general purpose timer with primary event

GP1 Timer: general purpose timer with peripheral event reload

Secondary Event Timer: to monitor secondary events

Conserve Mode Timer: Hardware-controlled return to standby

The normal sequence of operations for a general purpose timer (GP0 or GP1) is to

1) First program the time base and timer value of the initial count (register GP_TIM_CNT).
2) Then activate counting by setting the GP0_START or GP1_START bit to one: the timer will start with the initial count and count down towards 0.
3) When the timer counts down to zero, an SMI will be generated if enabled (GP0TO_EN and GP1TO_EN in the GBL_EN register) with status recorded (GP0TO_STS and GP1TO_STS in the GBL_STS register).
4) Each timer can also be programmed to reload the initial count and restart counting automatically after counting down to 0. This feature is not used in standard VIA BIOS.

The GP0 and GP1 timers can be used just as the general purpose timers described above. However, they can also be programmed to reload the initial count by system primary events or peripheral events thus used as primary event (global standby) timer and peripheral timer, respectively. The secondary event timer is solely used to monitor secondary events.

System Primary and Secondary Events

Primary system events are distinguished in the PRI_ACT_STS and PRI_ACT_EN registers:

Bit	Event	Trigger
7	**Keyboard Access**	I/O port 60h
6	**Serial Port Access**	I/O ports 3F8h-3FFh, 2F8h-2FFh, 3E8h-3EFh, or 2E8h-2EFh
5	**Parallel Port Access**	I/O ports 378h-37Fh or 278h-27Fh
4	**Video Access**	I/O ports 3B0h-3DFh or memory A/B segments
3	**IDE/Floppy Access**	I/O ports 1F0h-1F7h, 170h-177h, or 3F5h
2	**Reserved**	
1	**Primary Interrupts**	Each channel of the interrupt controller can be programmed to be a primary or secondary interrupt
0	**ISA Master/DMA Activity**	

Each category can be enabled as a primary event by setting the corresponding bit of the PRI_ACT_EN register to 1. If enabled, the occurrence of the primary event reloads the GP0 timer if the PACT_GP0_EN bit is also set to 1. The cause of the timer reload is recorded in the corresponding bit of PRI_ACT_STS register while the timer is reloaded. If no enabled primary event occurs during the count down, the GP0 timer will time out (count down to 0) and the system can be programmed (setting the GP0TO_EN bit in the GBL_EN register to one) to trigger an SMI to switch the system to a power down mode.

The VT82C686A distinguishes two kinds of interrupt requests as far as power management is concerned: the primary and secondary interrupts. Like other primary events, the occurrence of a primary interrupt demands that the system be restored to full processing capability. Secondary interrupts, however, are typically used for housekeeping tasks in the background unnoticeable to the user. The VT82C686A allows each channel of interrupt request to be declared as either primary, secondary, or ignorable in the PIRQ_CH and SIRQ_CH registers. Secondary interrupts are the only system secondary events defined in the VT82C686A.

Like primary events, primary interrupts can be made to reload the GP0 timer by setting the PIRQ_EN bit to 1. Secondary interrupts do not reload the GP0 timer. Therefore the GP0 timer will time out and the SMI routine can put the system into power down mode if no events other than secondary interrupts are happening periodically in the background.

Primary events can be programmed to trigger an SMI (setting of the PACT_EN bit). Typically, this SMI triggering is turned off during normal system operation to avoid degrading system performance. Triggering is turned on by the SMI routine before entering the power down mode so that the system may be returned to normal operation at the occurrence of primary events. At the same time, the GP0 timer is reloaded and the count down process is restarted.

Peripheral Events

Primary and secondary events define system events in general and the response is typically expressed in terms of system events. Individual peripheral events can also be monitored by the VT82C686A through the GP1 timer. The following four categories of peripheral events are distinguished (via register GP_RLD_EN):

Bit-7 **Keyboard Access**
Bit-6 **Serial Port Access**
Bit-4 **Video Access**
Bit-3 **IDE/Floppy Access**

The four categories are subsets of the primary events as defined in PRI_ACT_EN and the occurrence of these events can be checked through a common register PRI_ACT_STS. As a peripheral timer, GP1 can be used to monitor one (or more than one) of the above four device types by programming the corresponding bit to one and the other bits to zero. Time out of the GP1 timer indicates no activity of the corresponding device type and appropriate action can be taken as a result.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit	Comment
Storage temperature	-55	125	^{o}C	T_S
Operating temperature - Case	0	85	^{o}C	T_C
Operating temperature - Ambient	0	70	^{o}C	T_A
Reference Voltage	0	5.5	Volts	V_{REF}
Core Voltage	0	3.6	Volts	V_{CC}
Suspend Voltage	-0.5	V_{CC} + 0.3	Volts	V_{SUS}
USB Voltage	-0.5	V_{CC} + 0.3	Volts	V_{USB}
Hardware Monitor Voltage	-0.5	V_{CC} + 0.3	Volts	V_{HWM}
Battery Voltage	-0.5	V_{CC} + 0.3	Volts	V_{BAT}
Input voltage (3.3V only inputs)	-0.5	V_{CC} + 0.3	Volts	FERR#, USBCLK, PWRBTN#, EXTSMI#, BATLOW#, FAN1, FAN2, SMBCLK, SMBDATA
Input voltage (5V tolerant inputs)	-0.5	V_{REF} + 0.5	Volts	All other inputs

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

T_A -0-70^{o}C, V_{REF}=5V ±5%, V_{CC}= V_{CCS}= V_{CCH}= V_{CCU}=3.3V ±0.3V, V_{BAT}=3.3V +0.3/-1.3V, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-0.5	0.8	V	
V_{IH}	Input high voltage	2.0	V_{CC}+0.3	V	
V_{OL}	Output low voltage	-	0.45	V	I_{OL} = 4.0mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH} = -1.0mA
I_{IL}	Input leakage current	-	±10	uA	$0 < V_{IN} < V_{CC}$
I_{OZ}	Tristate leakage current	-	±20	uA	$0.45 < V_{OUT} < V_{CC}$
I_{CC}	Power supply current	-	80	mA	

PACKAGE MECHANICAL SPECIFICATIONS

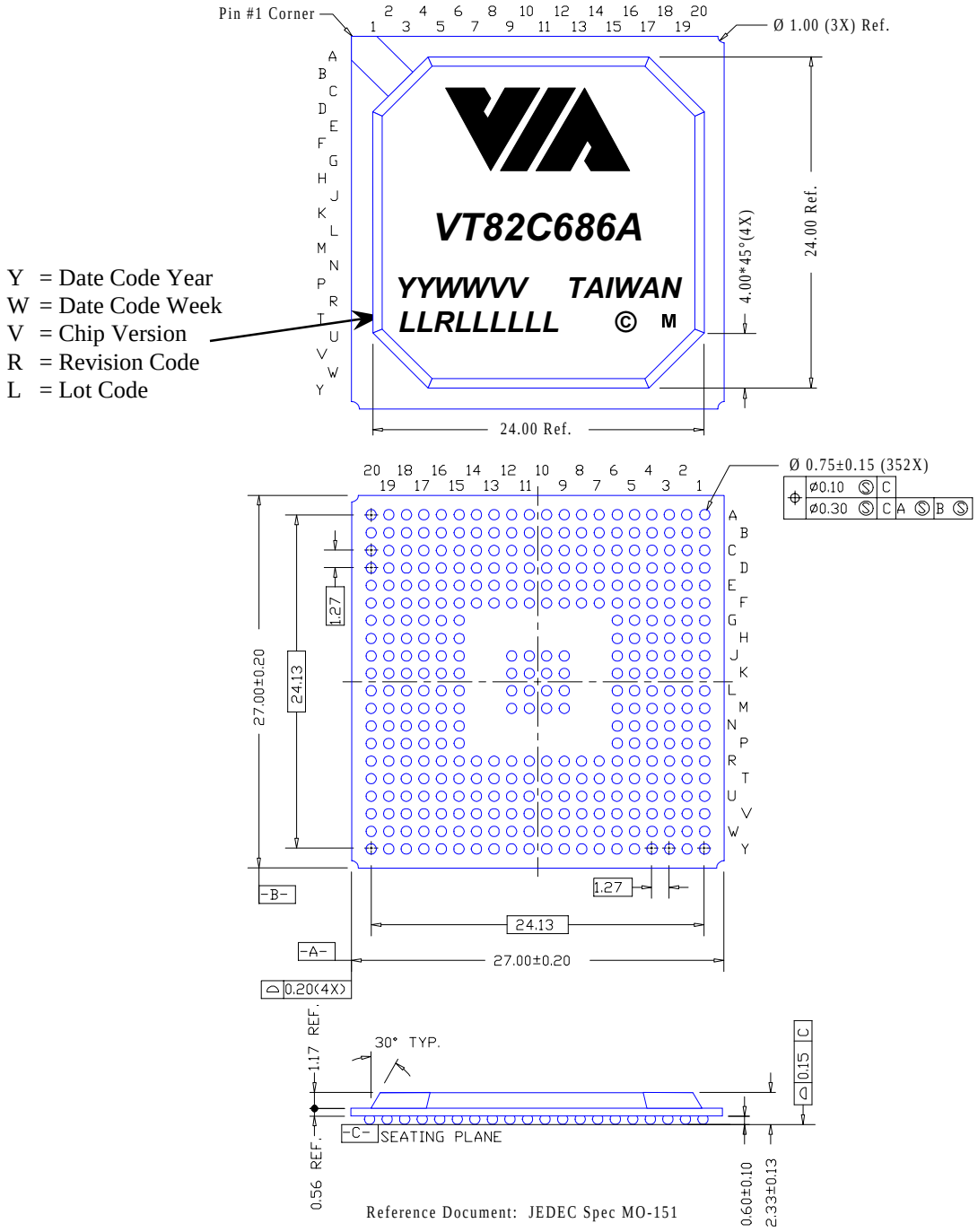

Figure 8. Mechanical Specifications – 352 Pin Ball Grid Array Package