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VIA VT82C505
Pentium/486 VL to PCI BRIDGE

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Features

* **VL to PCI Bridge**
  - Combined with VT82C486 or VT82C496G for 80486SX/DX/DX2/DX4 based PCI/VL/ISA Green-PC systems
  - Combined with VT82C530MV chip set for Pentium/P54C/M1 based PCI/VL/ISA Green-PC Systems

* **Sophisticated Bridging Capabilities**
  - Supports PCI master to PCI slave cycles
  - Supports PCI master to VL bus slave, system memory and ISA slave cycles
  - Supports VL master including CPU to PCI slave cycles
  - Supports ISA master to VL or PCI slave cycles
  - Supports multiple accelerated decoding schemes from VL master including CPU to PCI and ISA slaves
  - Supports CPUs with write-back level-one cache
  - Concurrent CPU and PCI operation
  - 4 level of CPU/VL to PCI post write buffers
  - Automatic detection of data streaming burst cycles from CPU/VL to PCI bus
  - 4 level of post write buffers from PCI master to VL slave, system memory and ISA slaves
  - 4 level of prefetch buffers from system memory for access by PCI masters
  - Bursting capability for both PCI and CPU/VL bus

* **Intelligent PCI Interface**
  - PCI 2.0 compliant
  - Synchronous or divide-by-two CPU clock
  - Hidden arbitration for up to four PCI masters
  - Supports PCI preemption and time-out function
  - Supports PCI master and slave initiated abort mechanism
  - Supports PCI lock function
  - Supports data parity generation for PCI master read cycles
  - Supports data parity checking for PCI master write cycles
  - Supports parity error and system error reporting on the PCI bus
  - Supports PCI configuration cycles
  - Interrupt steering and conversion to edge triggering for ISA compatibility

* **PCI Compliant IO Characteristics**

* **0.8um high speed and low power CMOS process**
* **160pin PQFP package**

Overview

The VT82C505 is a VL to PCI bus bridge that extends a currently matured and cost-effective VL/ISA chip set to a complete PCI/VL/ISA system. In particular, the VT82C505 can be combined with the VT82C486 or VT82C496G for a two chip Green PC ready PCI/VL/ISA system based on 80486SX/DX/DX2/DX4 or compatible processors (Figure 1). Similarly, the VT82C505 can be combined with the VT82C530MV chip set (VT82C535MV and VT82C531MV) for a Green PC ready PCI/VL/ISA system based on the Pentium/P54C/M1 superscalar processor (Figure 2). In all cases, the system management interface, power management unit, keyboard controller with PS2 mouse interface, clock stop mechanism and write-back level-one cache support are fully integrated into the chip set.

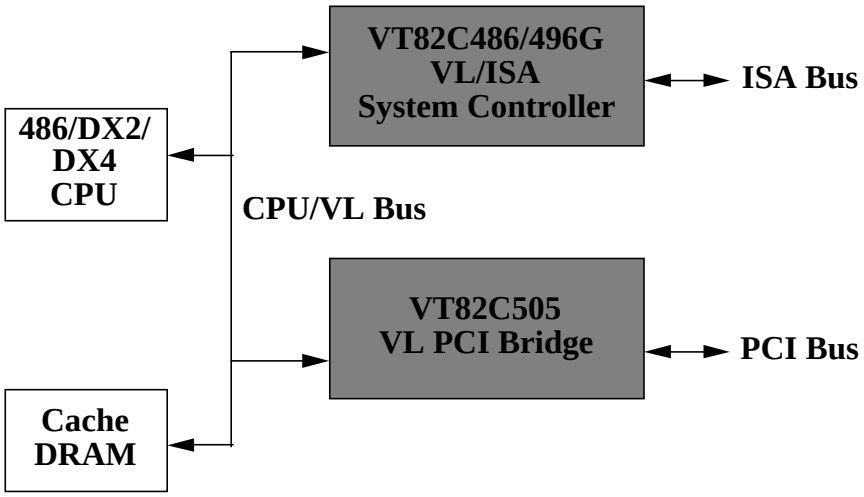


Figure 1. 80486 based PCI/VL/ISA System

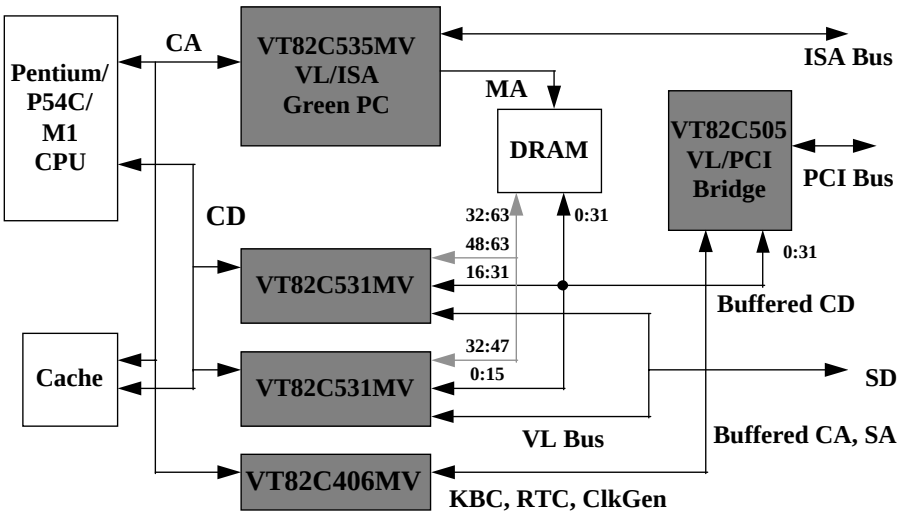


Figure 2. Pentium based PCI/VL/ISA System

The VT82C505 includes bi-directional VL to PCI bus conversion with prefetch and write buffer (FIFO) control. In addition, the interrupt steering and bus arbitration logic is also included in the chip for glueless interface with the companion VL/ISA chipset (VT82C486/496G/530MV). The functional block diagram for the VT82C505 is indicated in Figure 3.

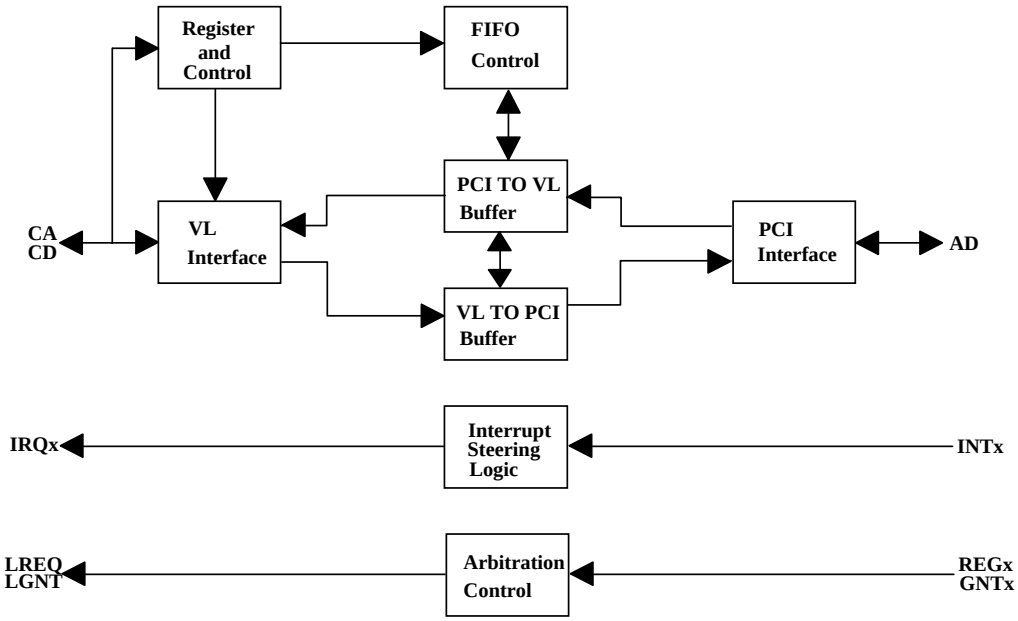


Figure 3. VT82C505 Functional Block Diagram

During a CPU or VL bus master cycle, the VT82C505 acts as a VL slave and PCI master if the cycle is decoded as a PCI cycle. The decoding is performed either by the DEVSEL# signaling of the PCI bus specification or through a number of accelerated schemes which are most effective when the PCI post write buffers are used. In addition to enabling concurrent CPU and PCI bus operation, the four level post write buffers also allow automatic detection of burst transactions from the CPU or VL bus masters to take advantage of the data streaming capability of the PCI bus.

During a PCI master cycle, the VT82C505 stands by if the cycle is decoded as a PCI slave cycle based on either the DEVSEL# signaling or the accelerated decoding schemes mentioned above. Otherwise, the VT82C505 acts as a PCI slave and VL master to access system memory, VL and ISA slaves through the VT82C486/496G/530MV system core logic. If the access hits a dirty line inside the CPU level one write-back cache, then the cycle will be held until the dirty line is written back to the system memory so that cache coherency may be maintained. Four level of post write buffers are provided to allow concurrent operation in the PCI and CPU/VL bus. Prefetch buffers are also included to allow early data retrieval from system memory to be accessed by the PCI masters. The VT82C505 also takes advantage of the bursting capability of the CPU/VL bus to further improve the bus throughput.

PCI 2.0 specification is supported by the VT82C505 for proper arbitration between PCI masters and proper transaction between PCI masters and slaves. In particular, the hidden arbitration scheme is implemented for up to four PCI masters in addition to the VT82C505 itself. The level sensitive interrupt signals from the PCI bus are steered and converted to edge triggering for ISA compatibility. Furthermore, the preemption, time-out, master and slave initiated abort and locking mechanism defined in the specification is supported for 100% compatibility in any PCI operating environment.

Functional Description

1. VT82C505 as a VL Slave and PCI Master

When the CPU (or an VL master) initiates a cycle, the VT82C505 acts as a VL slave and PCI master and determines the cycle type according to the following sequence:

1. If the cycle is an on-board memory access (cache or DRAM), then the VT82C505 stands by until the ready signal is returned by the companion VL/ISA chipset.
2. If the cycle accesses another VL device, then the VT82C505 stands by until the ready signal is returned by the VL device.
3. If the cycle accesses the internal register of the VT82C505 or other devices in the PCI bus, then the VT82C505 asserts LRDY# at the end of the cycle. The decoding is based on a combination of the "FRAME#-DEVSEL#" PCI bus protocol and a number of accelerated PCI and ISA decoding methods. Please refer to the sections of "PCI and ISA Cycle Decoding" and "Accelerated Decoding, Burst Detection and Write Buffers" for details.
4. Otherwise, the cycle is an ISA cycle and the companion VL/ISA chipset is responsible for handling the cycle until completion.

The VT82C505 needs to know whether a given memory cycle accesses the on-board memory. Several internal registers are provided for this purpose:

1. RX81h: records address 20 to 27 of the size of the on-board DRAM. For instance, RX81h records 04h if the on-board DRAM is 4MB. This register is programmed when BIOS detects the on-board DRAM type and size for the companion VL/ISA chipset.
2. RX30-32h: records if any 16KB in the C0000-FFFFFh area is shadowed in the DRAM (read and write cycles are programmed independently). Bit 2 of RX32h also indicates whether address range 15MB to 16MB maps to on-board DRAM or not.
3. RX33h: bit 2 and 3 record whether 256K/384K in the upper memory area (640KB-1MB) is relocated on top of the regular DRAM space.
4. RX5Bh: bit 3 records whether system management memory is turned on or not. If turned on, the available relocated memory is reduced from 256K/384K to 128K/256K, respectively. Bit 4 of RX5Bh indicates whether CPU address A0000-BFFFFh maps to on-board DRAM for direct system management memory access or not.

RX30-33h and RX5Bh are actually shadow registers for the companion VL/ISA chipset. The same registers are defined for both the VT82C505 and the companion VL/ISA chipset and are programmed at the same time when one IO write command is performed.

The VT82C505 samples LDEV# from another VL device at the same time as the companion VL/ISA chipset. The sampling time is either at the end of the first or second T2, depending on bit 6 of internal register RX83h.

2. PCI and ISA Cycle Decoding

The VT82C505 determines if a given cycle accesses its internal register, other PCI devices or ISA devices as follows:

1. If the cycle accesses the internal registers or is a PCI configuration cycle, then the cycle is decoded positively by the VT82C505 and LDEV# is asserted low by the end of the first T2. Refer to the section of "PCI Configuration and Internal Registers" for details.

2. If the cycle type and address fall within the accelerated PCI window, then the cycle is decoded positively by the VT82C505 and the LDEV# signal is asserted low by the end of the first T2. If the cycle is a write cycle and can be put into the post write buffer, then LRDY# is returned by the end of the second T2. The PCI windows need to be programmed before this positive decoding (or accelerated decoding) method can be applied. Refer to the section of "Accelerated Decoding, Burst Detection and Write Buffers" for more details.
3. The cycle is then checked to see if it is an accelerated ISA cycle by checking the content of RX92h. This register covers memory address range from A0000 to FFFFFh in either 32K or 64K increments. An accelerated ISA cycle is responded by asserting LDEV# low after the second T2 to activate the ISA cycle. Note that the latest time to recognize a local bus cycle is at the end of second T2. To work with the VT82C505, the option needs to be turned on in the companion VL/ISA chipset to interpret the activation of the LDEV# signal after the second T2 as an ISA command strobe.
4. If the cycle is neither an accelerated PCI nor an accelerated ISA cycle, then the VT82C505 asserts the FRAME# signal to the PCI bus to see if any device responds. If the DEVSEL# signal is responded by a device in the PCI bus, then the cycle is determined as a PCI cycle. Since the end of the second T2 is already passed, the LDEV# remains inactive. The TRDY# returned from the PCI slave can be either passed through or re-synchronized in the VT82C505 to the CPU/VL bus (bit 5 of RX83h).
5. If the DEVSEL# is not returned at a pre-determined time period, then the cycle is determined to be an ISA cycle. The LDEV# is asserted to activate the ISA cycle and the cycle is completed by the companion VL/ISA chipset.

3. Accelerated Decoding, Burst Detection and Write Buffers

The VT82C505 provides three PCI/VL memory windows, each of which is defined by three internal registers. For the first window,

- RX87h defines A<31:24> of the starting address of the memory window,
- RX88h defines A<23:16> of the starting address of the memory window, and
- RX89h defines the attributes and size of the memory window:
  bit 7: PCI device enable
  bit 6: write buffer enable
  bit 5: VL device enable
  bit 4-2: window size
  000: 64KB
  001: 128KB
  010: 256KB
  011: 512KB
  100: 1MB
  101: 2MB
  110: 4MB
  111: 8MB

Similarly, RX8A-8Ch and RX8D-8Fh define the second and the third memory windows, respectively. Each window can be used as a PCI window (if bit PCI device is enabled) or a VL window (if bit VL device is enabled). A PCI window is normally used in CPU cycles for fast decoding of PCI devices; a VL window is normally used in PCI master cycles for fast decoding of VL devices. The write buffer attribute is applicable for both PCI and VL windows.

For a CPU cycle, if the address falls within one of the PCI window, then the cycle is determined to be a PCI cycle. Additionally, if the cycle is a write cycle and the write buffer attribute is enabled, then

the cycle is pushed into the four-level write buffers and the LRDY# is returned at the end of the first or second T2 (bit 7 of RX83h). The CPU/VL bus and the PCI bus thus operate concurrently. Furthermore, if consecutive commands are of the same type accessing consecutive addresses, then the VT82C505 detects the bursting and generates the PCI commands in burst mode even though the original CPU commands are not bursted.

Other than the three memory windows, the VT82C505 also provides a dynamic acceleration method by remembering the high order address of the current PCI command. If the next CPU command falls within the same 1KB address space, then the cycle is automatically recognized as an PCI command even though the address may not fall within any of the three memory windows. This option can be enabled by setting bit 3 of RX82h to 1.

The mechanism of accelerated decoding, burst detection and write buffers improves the performance of CPU/VL to PCI transfers significantly.

4. VT82C505 as a PCI Slave and VL Master

When a PCI master obtains the ownership of the PCI bus and issues a command by asserting the FRAME# signal. The VT82C505 acts as a PCI slave and VL master and determines the cycle type according to the following sequence:

1. If the cycle is an on-board memory access, then the VT82C505 activates DEVSEL# to acknowledge acceptance of the PCI cycle. On behalf of the requesting PCI master, the VT82C505 obtains ownership of the CPU/VL bus and generates ADS# to access the memory through the companion VL/ISA chipset. The RTNRDY# signal from the CPU/VL bus may be either passed through or re-synchronized as TRDY# to the PCI bus (bit 4 of RX83h).
2. If the cycle falls within one the accelerated VL memory window, then the VT82C505 activates DEVSEL# to acknowledge acceptance of the PCI cycle. On behalf of the requesting PCI master, the VT82C505 obtains ownership of the CPU/VL bus and generates ADS# to access the local bus slave device.
3. If the cycle is detected as an accelerated ISA cycle, then the action is the same as item 1 above.
4. If none of the above accelerated decoding methods succeeds, then the VT82C505 monitors the PCI bus to see if any other PCI device signals DEVSEL# for acceptance of the cycle. If the answer is yes, then the VT82C505 stands by until completion of the cycle. Otherwise, the VT82C505 acts as a VL master to complete the transaction.

To speed up the transaction, four level of write buffers are provided for the PCI masters to access VL slaves, on-board memory and ISA slaves. Four level of prefetch buffers are also provided for look ahead access of VL slaves and on-board memory. Furthermore, bursting in the CPU/VL bus is performed if consecutive accesses allow such bursting to occur.

The VT82C505 supports CPUs with write-back level-one cache by connecting the WBACK# pin to the HITM# signal of the CPU directly. If the VL bus command generated by the VT82C505 on behalf of the PCI master hits an internal dirty line, the VT82C505 releases ownership of the CPU/VL bus until the dirty line inside the CPU is written back to the on-board memory.

5. PCI Bus Controller

In addition to being both a PCI slave and a PCI master device, the VT82C505 is also responsible for PCI bus master arbitration, error handling and interrupt steering. The PCI clock runs either synchronously with the CPU or at half the speed.

The VT82C505 supports hidden arbitration for up to four additional PCI masters. Two priority mechanisms are supported: 1. PCI master has priority, or 2. fairness between PCI masters and CPU/VL (bit 7 of RX85h). The arbitration can either be based on REQ# or FRAME# signals, i.e., the arbitration can be performed at the end of each REQ# or at the start of each FRAME# (bit 6 of RX85h).

Acted as a VL slave in CPU cycles, the VT82C505 may request the PCI bus ownership whether the accelerated decoding methods succeed or not. The REQ# and GNT# signal pair for the VT82C505 is built inside the chip to be arbitrated with the other PCI masters. Once granted, the VT82C505 acts as a PCI master on behalf of the CPU (or VL master) to access the PCI bus.

If a PCI master requests the bus ownership by asserting its REQ# signal to be arbitrated inside the VT82C505. The master is granted the control by activating the corresponding GNT#. As a PCI slave, the VT82C505 monitors the FRAME# signal to see if it is accessed by the active bus master.

Whether acted as a PCI master or slave, the VT82C505 follows the PCI-2.0 specification in handling master or slave initiated aborts, bus lock, time-out and preemption for complete compatibility.

The VT82C505 is also responsible for converting the level-sensitive PCI interrupts into the edge-triggered ISA interrupts. Any of the four PCI interrupts (INTA, B, C, D) can be steered to any of the six general purpose ISA interrupts (IRQ5, 9, 10, 11, 14, 15).

6. VL Bus Controller

The VT82C505 acts as both a VL master and slave. The main arbitration logic for the VL masters is built inside the companion VL/ISA chipset. Since the VT82C505 occupies one slot of the available

VL masters, it allows another VL master LREQ# and LGNT# pair to be arbitrated with the internal request before requesting the VL bus through the companion VL/ISA chipset.

The VT82C505 uses two different LDEV# signals: input LDEVI# is the combined LDEV# signal of all the other VL devices, and output LDEVO# is interpreted as LDEV# and ISA command strobe by the companion VL/ISA chipset as mentioned in the previous sections. Note that, due to critical timing consideration, LDEVO# does not reflect the LDEV# of the other VL devices and external combination is required.

The VT82C505 implements the complete VL-2.0p specification, including the WBACK# and the BLAST#/BRDY# burst transfer protocol.

7. PCI Configuration and Internal Registers

The VT82C505 supports the standard PCI configuration mechanism #1 and #2 (determined by bit 7 of internal register RX86h, defaulted as mechanism #1). Under mechanism #1, IO address CF8h is used as the configuration address port and CFCh as the configuration data port. Both ports are 32-bit wide. If the VT82C505 detects a full double word write at address CF8h, the chip latches the value into it. Any other types of accesses to this address are treated as a normal IO access. The format of the configuration address is as follows:

- bit 31 : configuration enable (this bit needs to be set to translate a configuration data access into a configuration cycle).
- bit 30-24 : reserved
- bit 23-16 : bus number (must be 0 to enable the configuration)
- bit 15-11 : device number (00000 access the VT82C505 internal registers, other values access other PCI devices)
- bit 10-8 : function number (don’t care for internal registers, but pass through to PCI bus for other PCI devices)

- bit 7-2 : register number
- bit 1-0 : always 00 (only type 0 format is supported)

The read or write command to the data port accesses any number of bytes (upto to four) in the configuration space.

Under mechanism #2, CPU IO read and write cycles to the C000-CFFFh address range are translated into PCI configuration read and write cycles, if configuration space enable register at address CF8h is enabled. The translation method carries the least significant 8 bits of the CPU address to the least significant 8 bits of the PCI address to select one of the 256 8-bit IO location in the PCI configuration space. Bits 8 to 11 of the CPU address are mapped to one of the 16 devices' IDSEL# input. These IDSEL# inputs of the PCI devices have to be hard-wired to one of the AD16-31 signals on the PCI bus. CA<11:8> being 0 accesses the internal configuration register of the VT82C505 and AD17-31 are available for other PCI devices.

The following configuration registers are defined in the VT82C505:

1. RX00-07h: Mandatory header field (or IDX00 and IDX04 based on the 32-bit IO port convention)

   - IDX00<15:0> - Vendor ID = 1106h (read only)
   - IDX00<31:16> - Device ID = 0505h (read only)
   - IDX04<15:0> - Command register
     bit 0: IO space = 1 (read only)
     bit 1: memory space = 1 (read only)
     bit 2: bus master = 1 (read only)
     bit 3: special cycle monitoring = 0 (read only)
     bit 4: memory write and invalid command = 0 (read only)
     bit 5: VGA palette snoop = 0 (read only)
     bit 6: parity error response (read/write, default=0)
     bit 7: address/data stepping = 0 (read only)
     bit 8: SERR# enable (read/write, default=0)
     bit 9: fast back-to-back cycle enable (read/write, default=0)
     bit 15-10: reserved
   - IDX04<31:16> - Status register (or IDX06<15:0>)
     bit 0-6: reserved
     bit 7: fast back-to-back: reserved
     bit 8: data parity detected: reserved
     bit 9-10: DEVSEL# timing: reserved
     bit 11: signaled target abort: reserved
     bit 12: received target abort (read only, write one to clear)
     bit 13: signaled master abort: reserved
     bit 14: signaled system error: reserved
     bit 15: detected parity error (write only, write one to clear)

2. RX80-9Fh: VT82C505 internal configuration registers.

   - RX80: dip-switch register
     bit 7 = 1/0: clock mode using PCLK=CCLK/PCLK=CCLK/2
     bit 6 = 1/0: synchronous clock mode/asynchronous clock mode
     bit 5 = 1/0: IRQ14, IRQ15/REQ#2, GNT#2 multi-function pin definition
     bit 4 = 1/0: BLAST#/HIADDR multi-function pin definition
     bit 3-0 = revision ID (read only)

The default of bit 7-4 depends on the power on condition of LREQ#, GNT#0, GNT#1 and GNT#3, respectively. To initialize a bit to 1, pull the corresponding signal pin high. Pulling the signal pin low initializes the corresponding bit to 0.

- RX81h: on-board memory size: <CA27-20> (default is 01h)

- RX82h: buffer control (default is 00h)
  bit 7 = 1/0: CPU/VL to PCI write buffer enable/disable
  bit 6 = 1/0: PCI to CPU/VL write buffer enable/disable
  bit 5: reserved
  bit 4 = 1/0: PCI accessing CPU/VL prefetch buffer enable/disable
  bit 3 = 1/0: PCI dynamic acceleration decoding enable/disable
  bit 2 : reserved
  bit 1 = 1/0: on-board memory burst write enable/disable
  bit 0 = 1/0: on-board memory burst read enable/disable

- RX83h: VL bus interface timing (default is 00h)
  bit 7 = 1/0: VL bus write 0 wait state/1 wait state
  bit 6 = 1/0: LDEV# sampling point at second T2/first T2
  bit 5 = 1/0: TRDY# to LRDY# using re-synchronization/bypass
  bit 4 = 1/0: RDYTRN# to TRDY# using re-synchronization/bypass
  bit 3 = 1/0: on-board memory detection point for PCI master at first data phase/address phase
  bit 2-1: reserved
  bit 0: must be 0

- RX84h: PCI interface timing (default is 03h)
  bit 7 = 1/0: slave mode lock function enable/disable
  bit 6 = 1/0: retry count at 64 times/16 times
  bit 5 = 1/0: retry deadlock error reporting enable/disable
  bit 4 = 1/0: retry status occurred/no occurred (write a 1 to reset)
  bit 3 = 1/0: CPU to PCI fast back to back enable/disable
  bit 2 = 1/0: fast FRAME# generation enable/disable
  bit 1-0 = 11/10/01/00: DEVSEL# decoding time subtractive/slow/medium/fast

- RX85h: PCI arbitration (default is 00h)
  bit 7 = 1/0: arbitration mechanism based on fairness between CPU and PCI/priority on PCI bus
  bit 6 = 1/0: arbitration mode using FRAME# based/REQ# based
  bit 5-4 = 11/10/01/00: CPU time slot at 32/16/8/4 PCI clock
  bit 3-0: PCI master bus time out
  0000: disable
  0001: 1x32PCI clock
  0010: 2x32PCI clock
  .....
  1111: 15x32PCI clock

- RX86h: configuration mechanism and misc. control (default is 00h)
  bit 7 = 1/0: configuration mechanism #2/#1
  bit 6 = 1/0: monitoring EOI for interrupt conversion enable/disable
  bit 5 = 1/0: PCI interrupt to ISA IRQ intelligent conversion enable/disable
  bit 4 = 1/0: must be 0
  bit 3 = 1/0: SERR# generation enable/disable
  bit 2 = 1/0: SERR# generation status (writing a 1 clears status)
  bit 1 = 1/0: PCI master BROKE timer enable/disable
  bit 0 = 1/0: LREQI#, LGNTO#/REQ#3, GNT#3 multi-function pin definition

- RX87h: PCI/VL memory window #1 base address A<31:24>
- RX88h: PCI/VL memory window #1 based address A<23:16>
- RX89h: PCI/VL memory window #1 attributes (default is 00h)
  bit 7: PCI device enable
  bit 6: write buffer enable
  bit 5: VL device enable
  bit 4-2: window size
    000: 64KB
    001: 128KB
    010: 256KB
    011: 512KB
    100: 1MB
    101: 2MB
    110: 4MB
    111: 8MB
- RX8Ah: PCI/VL memory window #2 base address A<31:24>
- RX8Bh: PCI/VL memory window #2 based address A<23:16>
- RX8Ch: PCI/VL memory window #2 attributes (default is 00h)
- RX8Dh: PCI/VL memory window #3 base address A<31:24>
- RX8Eh: PCI/VL memory window #3 based address A<23:16>
- RX8Fh: PCI/VL memory window #3 attributes (default is 00h)
- RX90h: INTD/INTC interrupt control (default is 00h)
  bit 7 = 1/0: INTD enable/disable
  bit 6-4: INTD to IRQ steering
    000: none
    001: IRQ5
    010: IRQ9
    011: IRQ10
    100: IRQ11
    101: IRQ14
    110: IRQ15
    111: reserved
  bit 3 = 1/0: INTC enable/disable
  bit 2-1: INTC to IRQ steering
- RX91h: INTB/INTA interrupt control (default is 00h)
  bit 7 = 1/0: INTB enable/disable
  bit 6-4: INTB to IRQ steering
  bit 3 = 1/0: INTA enable/disable
  bit 2-1: INTA to IRQ steering
- RX92h: accelerated ISA cycle (default is 00h)
  bit 7: A0000h to AFFFFh enable/disable
  bit 6: B0000h to BFFFFh enable/disable
  bit 5: C0000h to C7FFFh enable/disable
  bit 4: C8000h to CFFFFh enable/disable
  bit 3: D0000h to D7FFFh enable/disable
  bit 2: D8000h to DFFFFh enable/disable
  bit 1: E0000h to E7FFFh enable/disable

bit 0: E8000h to EFFFFh enable/disable
* F0000h to FFFFFh is always accelerated ISA cycle

- RX93h: misc. control (default is 40h)
  bit 7-6: HIADDR address
  00: CA26 above
  01: CA27 above
  10: CA28 above
  11: CA29 above
  bit 5 = 1/0: IOCHK#/NMI multi-function pin definition
  the pin is floating before RX93h is written.

- RX94h: accelerated PCI cycle (default is 00h)
  bit 7: A0000h to AFFFFh enable/disable
  bit 6: B0000h to BFFFFh enable/disable
  bit 5: C0000h to C7FFFh enable/disable
  bit 4: C8000h to CFFFFh enable/disable
  bit 3: D0000h to D7FFFh enable/disable
  bit 2: D8000h to DFFFFh enable/disable
  bit 1: E0000h to E7FFFh enable/disable
  bit 0: E8000h to EFFFFh enable/disable

RX80-9Fh can also be accessed through IO port A8h and A9h as the companion VL/ISA chipset. Each port, if accessed this way, is only eight bit wide. To access an internal register, write the index to the A8h address port, then read or write the data through the A9h data port. Note that registers RX00-7Fh are reserved for the companion VL/ISA chipset. Some of these registers are write-shadowed in the VT82C505 for consistent operation:

- RX04 (bit 4): LDEV# signal as LDEV#/ISA command strobe
- RX30-32h: BIOS shadow for C0000-FFFFFh
- RX33h (bit 3,2): 256K/384K relocation
- RX5Bh (bit 4,3): SMM memory usage
- RX5Eh (bit 7,5): write-back CPU mode

VT82C505 Signal Description

Signal Name	Pin Number	Type	Signal Description
CPU/VL Bus Interface			
CCLK	149	I	CPU/VL clock
ADS#	1	B	Address Strobe: The falling edge indicates the start of a CPU local bus cycle. Act as input during CPU or VL master cycles and as output during PCI master cycles.
MIO#	2	B	Memory/IO status. High indicates a memory cycle and low indicates an IO cycle. Act as input during CPU or VL master cycles and as output during PCI master cycles.
WR#	3	B	Write/read status. High indicates a write cycle and low indicates a read cycle. Act as input during CPU or VL master cycles and as output during PCI master cycles.
DC#	4	B	Data/code status. High indicates data transfer and low indicates control operation.
BE#0-3	6-9		CPU byte enable. Act as input during CPU and VL master cycles and as output during PCI master cycles.
CA2-31	24-29, 31-38, 62-69, 71-72, 74-79	B	CPU local bus address. Act as input during CPU and VL master cycles and as output during PCI master cycles.
CD0-31	17-19, 21-23, 39-44, 56-61, 80-85, 106-109, 111-114	B	CPU local data bus.
LDEVO#	115	O	VL bus access output. This signal is asserted by the end of the second T2 to indicate the CPU/VL cycle accesses an internal register or a PCI device. After the end of the second T2, the signal is asserted to initiate an ISA cycle.
LRDY#	105	O	Local bus ready output .
LDEVI#	104	I	The combined local bus access input from other VL devices.
LREQO#	116	O	VL bus ownership request to the companion VL/ISA chipset
LGNTI#	117	I	VL bus ownership grant from the companion VL/ISA chipset
BLAST#/ HIADDR	148	O	Multi-function pin: 1. RX80h bit 4 = 1 (GNT3# pin high at power on): burst last indicator for the CPU/VL bus 2. RX80h bit 4 = 0 (GNT3# pin low at power on): hi-address access indicator for the companion VL/ISA chipset.
BRDY#	96	I	burst ready input
WBACK#	1016	I	Input from the CPU (with write-back L1 cache) to inform the VT82C505 to release the VL bus so that the dirty line may be written back to the system memory. Connect to the HITM# output of the CPU.
EADS#	136	O	External ADS# to signal to snoop the CPU internal cache

RDYRTN#	103	I	Returned ready input from the CPU/VL bus
PCI Bus Interface			
PCLK	151	I	PCI bus clock output
FRAME#	46	B	Cycle frame. This pin acts as an output when the VT82C505 acts as an PCI master on behalf of the CPU and VL masters. This pin acts as an input when the VT82C505 acts as an PCI slave.
AD#0-31	47-49, 51-55, 86-89, 91-95, 122-126, 131-135, 154-158	B	Multiplexed PCI address and data
C/BE#0-3	11-14	B	Multiplexed PCI command and byte enable
IRDY#	160	B	Initiator ready.
TRDY#	137	B	Target ready.
STOP#	142	B	Stop signal.
DEVSEL#	141	B	Device select.
PAR	139	B	Data parity.
PERR#	138	B	Parity error.
SERR#	5	B	System error.
LOCK#	121	B	Lock signal.
REQ#0-1	129, 128	I	PCI bus request from other PCI masters.
GNT#0-1	118, 119	O	PCI bus grant to other PCI masters.
REQ#2/ IRQ14	102	B	Multi-function pin: 1. RX80h bit 5 = 0 (GNT#1 pin low at power on): PCI bus request 2. RX80h bit 5 = 1 (GNT#1 pin high at power on): ISA interrupt request 14
GNT#2/ IRQ15	147	O	Multi-function pin: 1. RX80h bit 5 = 0 (GNT#1 pin low at power on): PCI bus grant 2. RX80h bit 5 = 1 (GNT#1 pin high at power on): ISA interrupt request 15.
REQ#3/ LREQI#	159	I	Multi-function pin: 1. RX86h bit 0 = 0: PCI bus request from another PCI master. 2. RX86h bit 0 = 1: VL bus request from another VL master.
INTA#, INTB#, INTC#, INTD#	98, 99, 15, 16	I	Level-sensitive PCI interrupt signals to be steered to the edge-triggered ISA interrupt signals.
System Interface			
RESET#	152	I	active low reset input from the companion VL/ISA chipset.
LREQI#/ REQ#3	159	I	Multi-function pin: 1. RX86h bit 0 = 1: VL bus request from another VL master. 2. RX86h bit 0 = 0: PCI bus request from another PCI master.
LGNTO#/ GNT#3	120	O	Multi-function pin: 1. RX86h bit 0 = 1: VL bus grant to the requesting master. 2. RX86h bit 0 = 0: PCI bus grant to the requesting master.

IOCHK#/ NMI	97	O	IO channel check (bit 5 of RX93h = 0) or NMI (bit 5 of RX93h=1) to signify the parity or system error at the PCI bus.
IRQ5, 9, 10, 11	143-146	O	Edge-sensitive ISA interrupt requested signals steered from the level-sensitive PCI interrupt signals
IRQ14/ REQ#2	102	B	Multi-function pin: 1. RX80h bit 5 = 1 (GNT#1 pin high at power on): ISA interrupt request 14. 2. RX80h bit 5 = 0 (GNT#1 pin low at power on): PCI bus request
IRQ15/ GNT#2	147	O	Multi-function pin: 1. RX80h bit 5 = 1 (GNT#1 pin high at power on): ISA interrupt request 15. 2. RX80h bit 5 = 0 (GNT#1 pin low at power on): PCI bus grant
Power and Ground			
VDD	20, 45, 73, 100, 127, 153	I	power supply of 4.5 to 5.5V.
VSS	10, 30, 50, 70, 90, 110, 130, 140, 150,	I	the ground

VT82C505 Pin Out in Numerical Order

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	ADS#	41	CD8	81	CD19	121	LOCK#
2	MIO#	42	CD9	82	CD20	122	AD17
3	WR#	43	CD10	83	CD21	123	AD18
4	DC#	44	CD11	84	CD22	124	AD19
5	SERR#	45	VDD	85	CD23	125	AD20
6	BE#0	46	FRAME#	86	AD8	126	AD21
7	BE#1	47	AD0	87	AD9	127	VDD
8	BE#2	48	AD1	88	AD10	128	REQ#1
9	BE#3	49	AD2	89	AD11	129	REQ#0
10	VSS	50	VSS	90	VSS	130	VSS
11	C/BE#0	51	AD3	91	AD12	131	AD22
12	C/BE#1	52	AD4	92	AD13	132	AD23
13	C/BE#2	53	AD5	93	AD14	133	AD24
14	C/BE#3	54	AD6	94	AD15	134	AD25
15	INTC#	55	AD7	95	AD16	135	AD26
16	INTD#	56	CD12	96	BRDY#	136	EADS#
17	CD0	57	CD13	97	NMI	137	TRDY#
18	CD1	58	CD14	98	INTA#	138	PERR#
19	CD2	59	CD15	99	INTB#	139	PAR
20	VDD	60	CD16	100	VDD	140	VSS
21	CD3	61	CD17	101	WBACK#	141	DEVSEL#
22	CD4	62	CA16	102	IRQ14	142	STOP#
23	CD5	63	CA17	103	RDYRTN#	143	IRQ5
24	CA2	64	CA18	104	LDEVI#	144	IRQ9
25	CA3	65	CA19	105	LRDY#	145	IRQ10
26	CA4	66	CA20	106	CD24	146	IRQ11
27	CA5	67	CA21	107	CD25	147	IRQ15
28	CA6	68	CA22	108	CD26	148	BLAST#
29	CA7	69	CA23	109	CD27	149	CCLK
30	VSS	70	VSS	110	VSS	150	VSS
31	CA8	71	CA24	111	CD28	151	PCLK
32	CA9	72	CA25	112	CD29	152	RESET#
33	CA10	73	VDD	113	CD30	153	VDD
34	CA11	74	CA26	114	CD31	154	AD27
35	CA12	75	CA27	115	LDEVO#	155	AD28
36	CA13	76	CA28	116	LREQO#	156	AD29
37	CA14	77	CA29	117	LGNTI#	157	AD30
38	CA15	78	CA30	118	GNT#0	158	AD31
39	CD6	79	CA31	119	GNT#1	159	REQ#3
40	CD7	80	CD18	120	GNT#3	160	IRDY#

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	^{o}C
Storate temperature	-55	125	^{o}C
Input voltage	-0.5	5.5	V
Output voltage	-0.5	5.5	V

Note :
Stress above these listed cause permanent damage to device. Functional operation of this evice should be restricted to the conditions described under operating conditions.

DC Characteristics

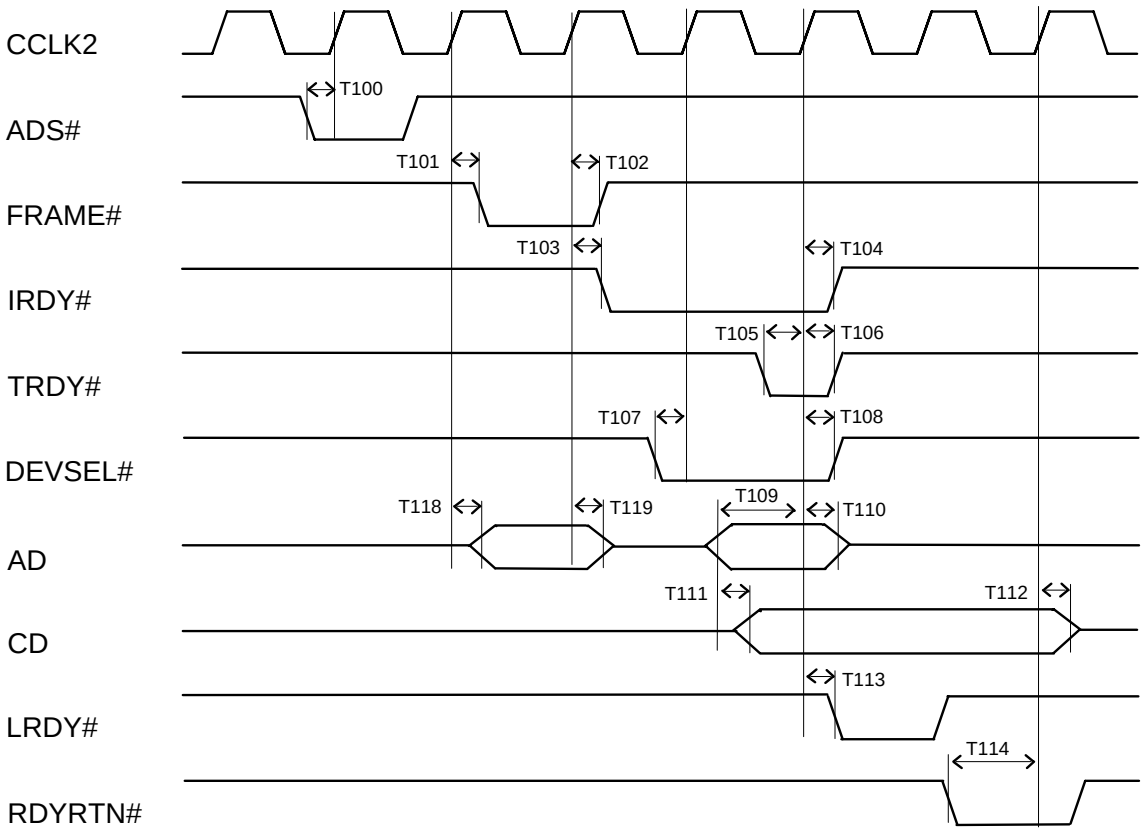
TA-0-70^{o}C, V_{DD}=5V+/-5%, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-.50	0.8	V	
V_{IH}	Imput high voltage	2.0	V_{DD}+0.5	V	
V_{OL}	Output low voltage	-	0.45	V	I_{OL}=4.0mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH}=-1.0mA
I_{IL}	Input leakage current	-	+/-10	uA	$0<V_{IN}<V_{DD}$
I_{OZ}	Tristate leakage current	-	+/-20	uA	$0.45<V_{OUT}<V_{DD}$
I_{CC}	Power supply current	-	80	mA	

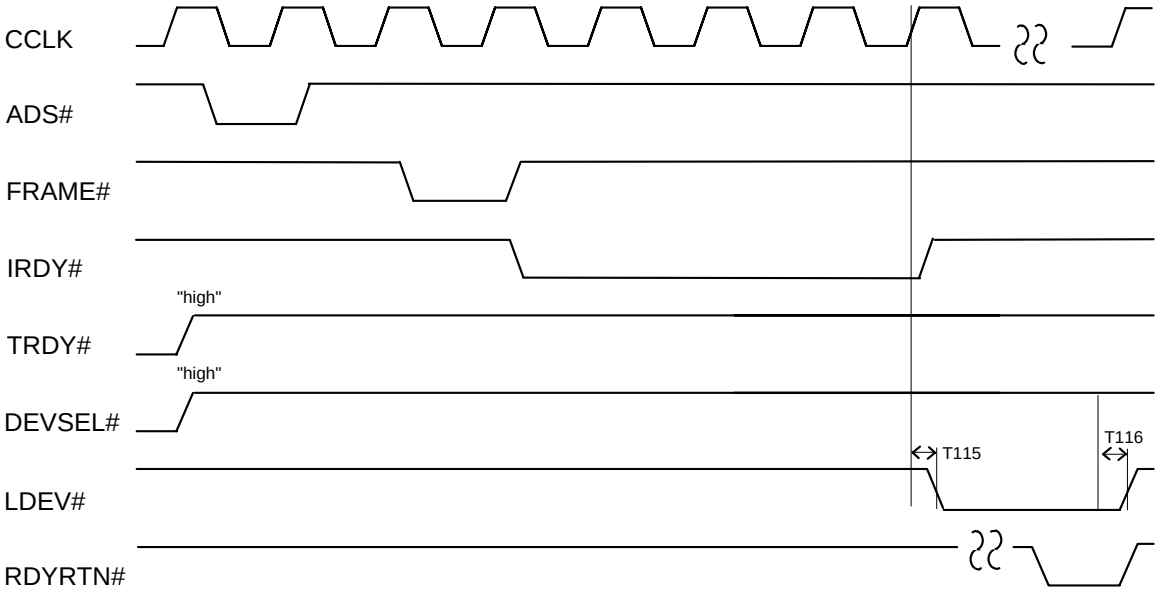
Symbol	Description	min(ns)	max(ns)
T100	ADS setup time to CCLK rising edge	5	
T101	FRAME# active delay from CCLK rising edge		13
T102	FRAME# inactive delay from CCLK rising edge	5	11
T103	IRDY# active delay from CCLK rising edge		13
T104	IRDY# inactive delay from CCLK rising edge	5	11
T105	TRDY# setup time to CCLK rising edge	4	
T106	TRDY# hold time from CCLK rising edge	1	
T107	DEVSEL# setup time to CCLK rising edge	5	
T108	DEVSEL# hold time from CCLK rising edge	1	
T109	AD setup time from CCLK rising edge	5	
T110	AD hold time from CCLK rising edge	2	
T111	AD to CD delay from CCLK rising edge	6	17
T112	CD float delay from CCLK risin edge	6	16
T113	LRDY# active delay from CCLK rising edge		15
T114	RDYRTN# setup time from CCLK rising edge	4	
T115	LDEV# valid delay from CCLK rising edge		14
T116	LDEV# invalid delay from CCLK rising edge	6	
T117	LDEVIN# setup time from CCLK rising edge	5	
T118	AD (address) valid delay from CCLK rising edge		14
T119	AD (address/data) float delay from CCLK rising edge		12
T120	AD (data) valid delay from CCLK rising edge		15
T121	LRDY# delay from TRDY#		12
T122	LRDY# valid delay (write buffered) from CCLK rising edge		18
T123	LDEV valid delay (write buffered) from CCLK rising edge		17

Symbol	Description	min(ns)	max(ns)
T200	ADS valid delay from CCLK rising edge		14
T201	ADS invalid delay from CCLK rising edge		13
T202	TRDY# valid delay from CCLK rising edge		14
T203	DEVSEL# valid delay from CCLK rising edge		13
T204	BRDY# setup time to CCLK rising edge	4	
T205	AD (address) setup time to rising edge	7	
T206	BLAST# valid delay from CCLK rising edge		13
T207	CD to AD delay from CCLK rising edge		17
T208	CD valid delay from CCLK rising edge		15
T209	CD float delay from CCLK rising edge		12

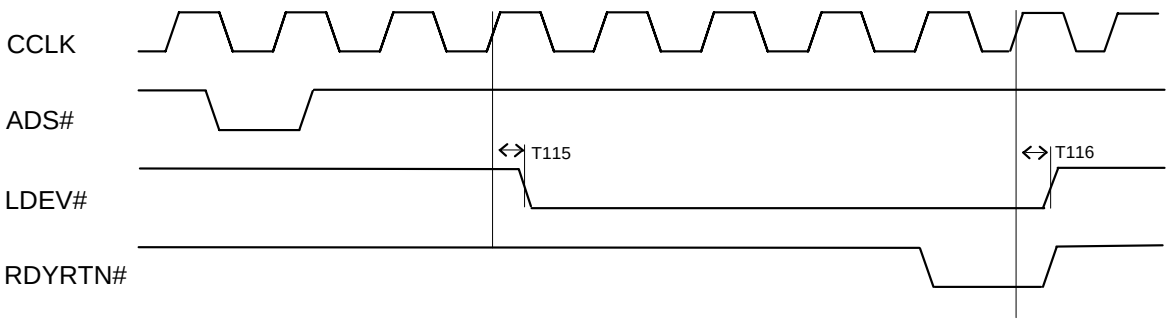
CPU Read PCI Slave



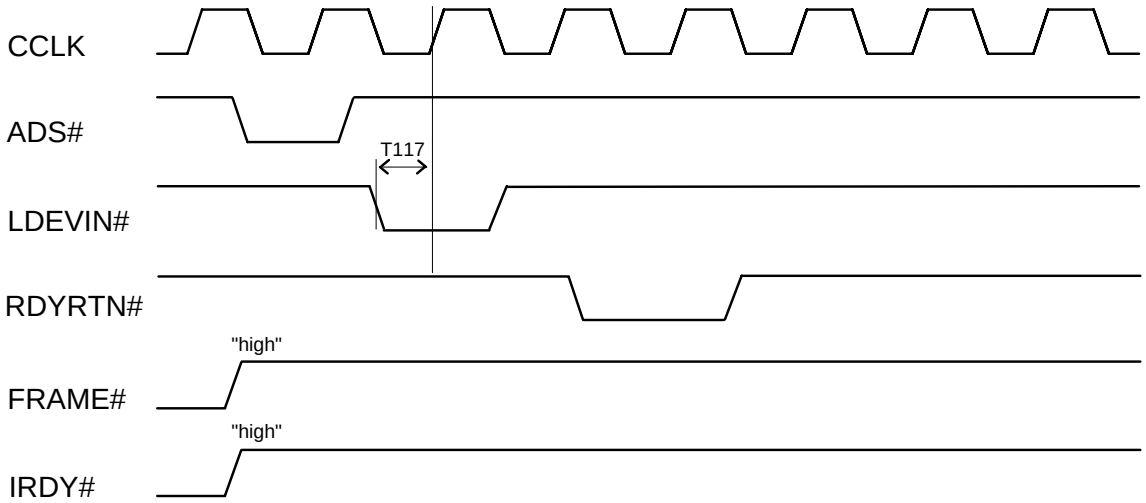
CPU Access ISA Bus
(PCI Bus Subtractive decoding)



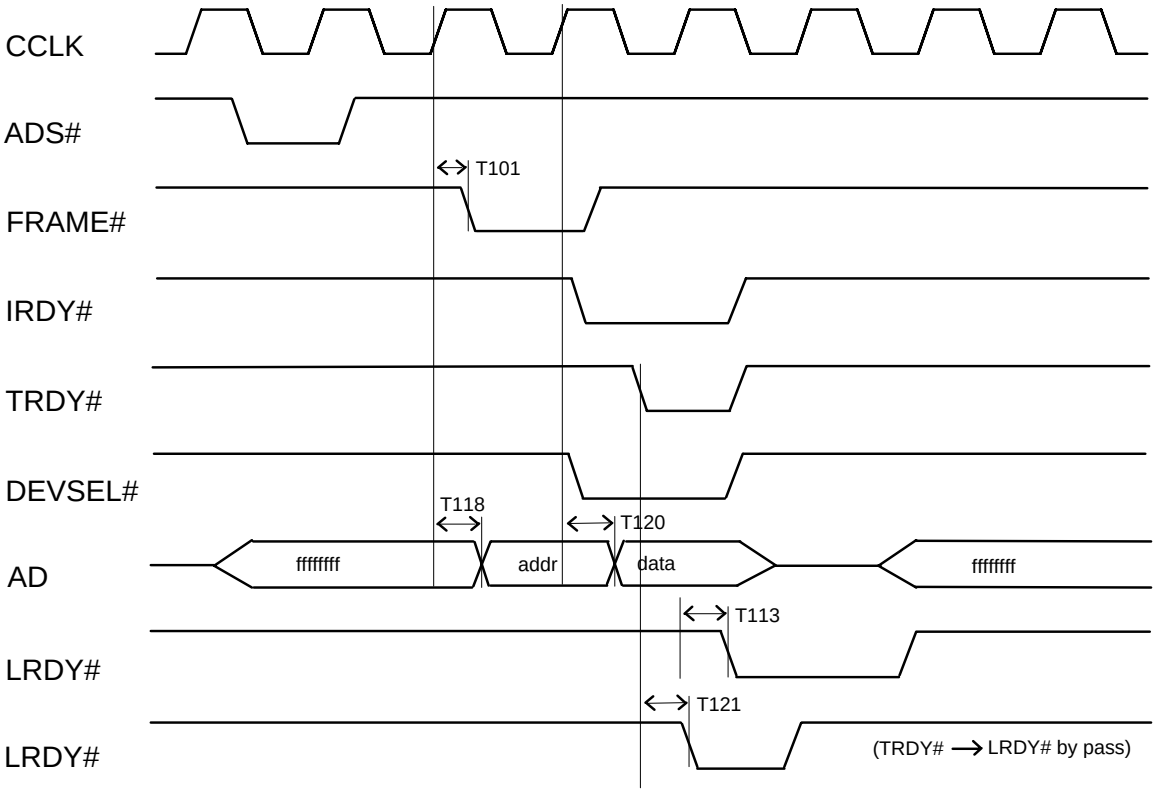
CPU Access ISA Bus (fast ISA)



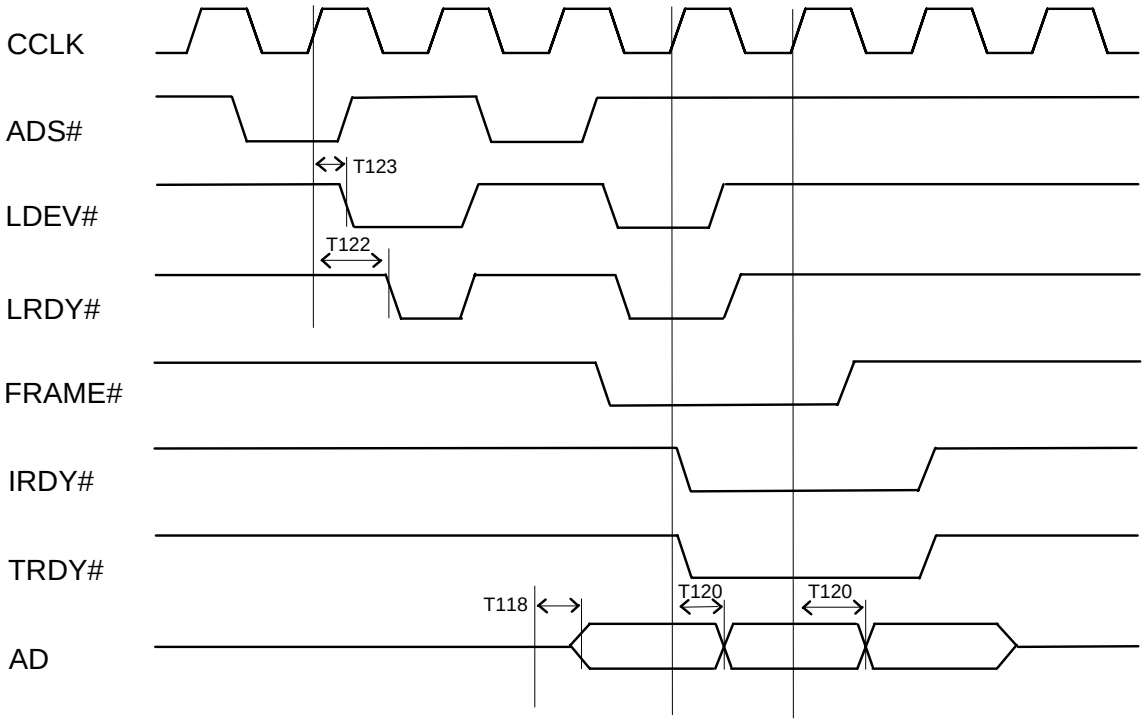
CPU Access VL Device



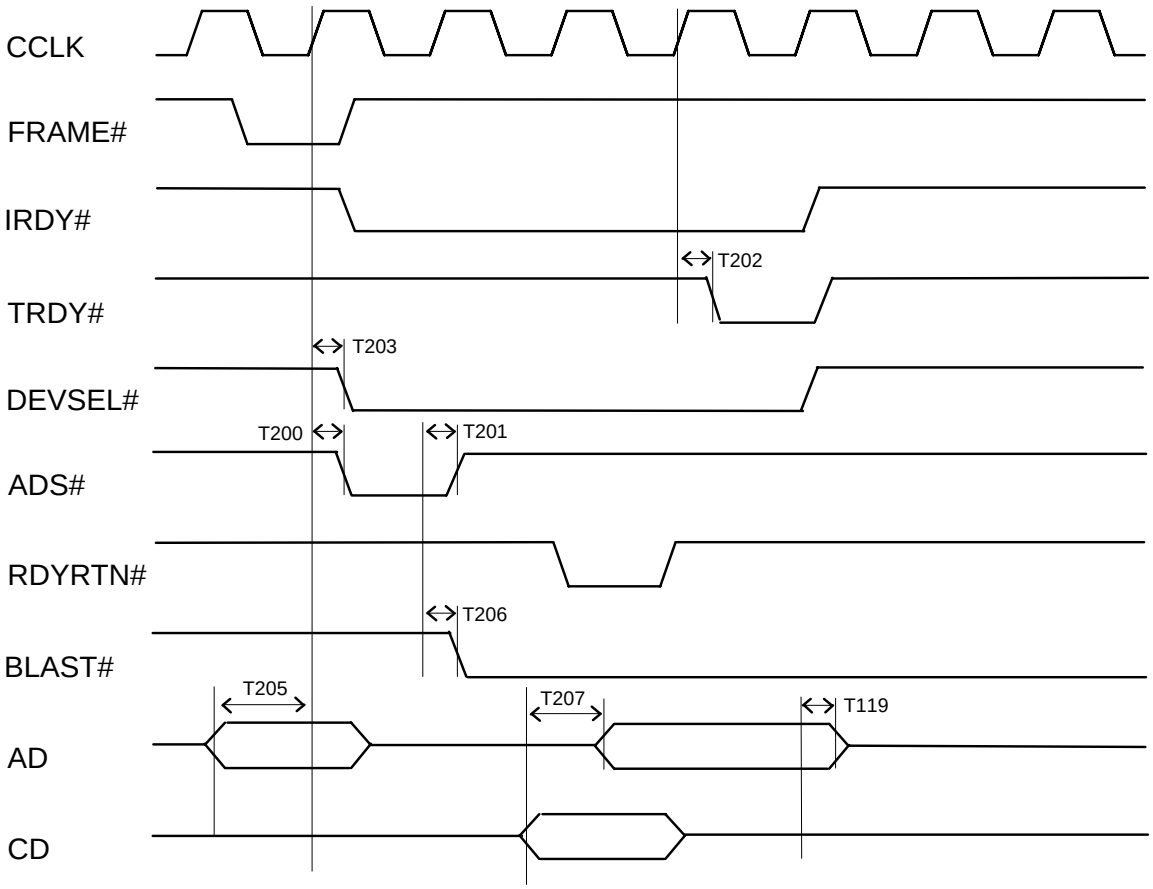
CPU Write PCI Slave (No Write Buffer)



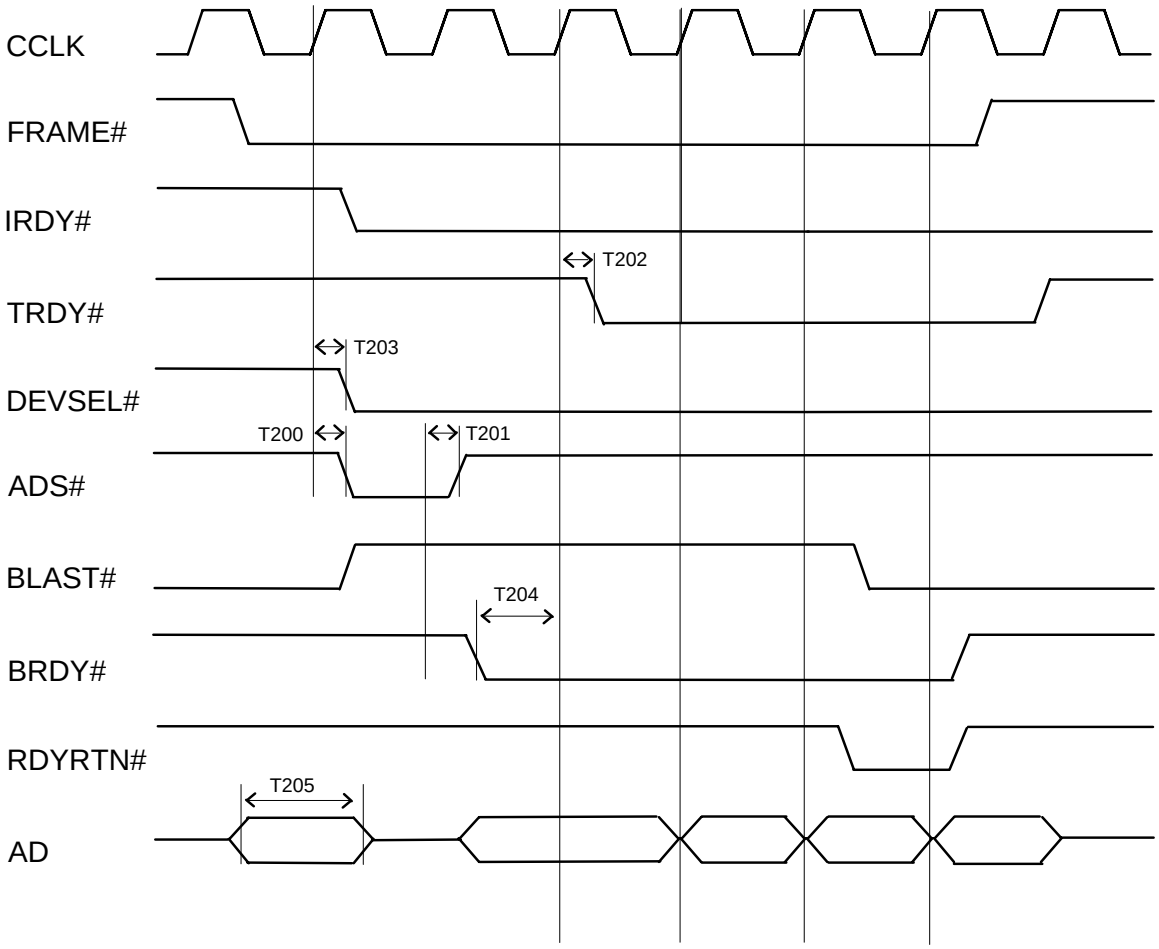
CPU Write PCI Slave
(Write Buffer + Burst Write on PCI Bus)



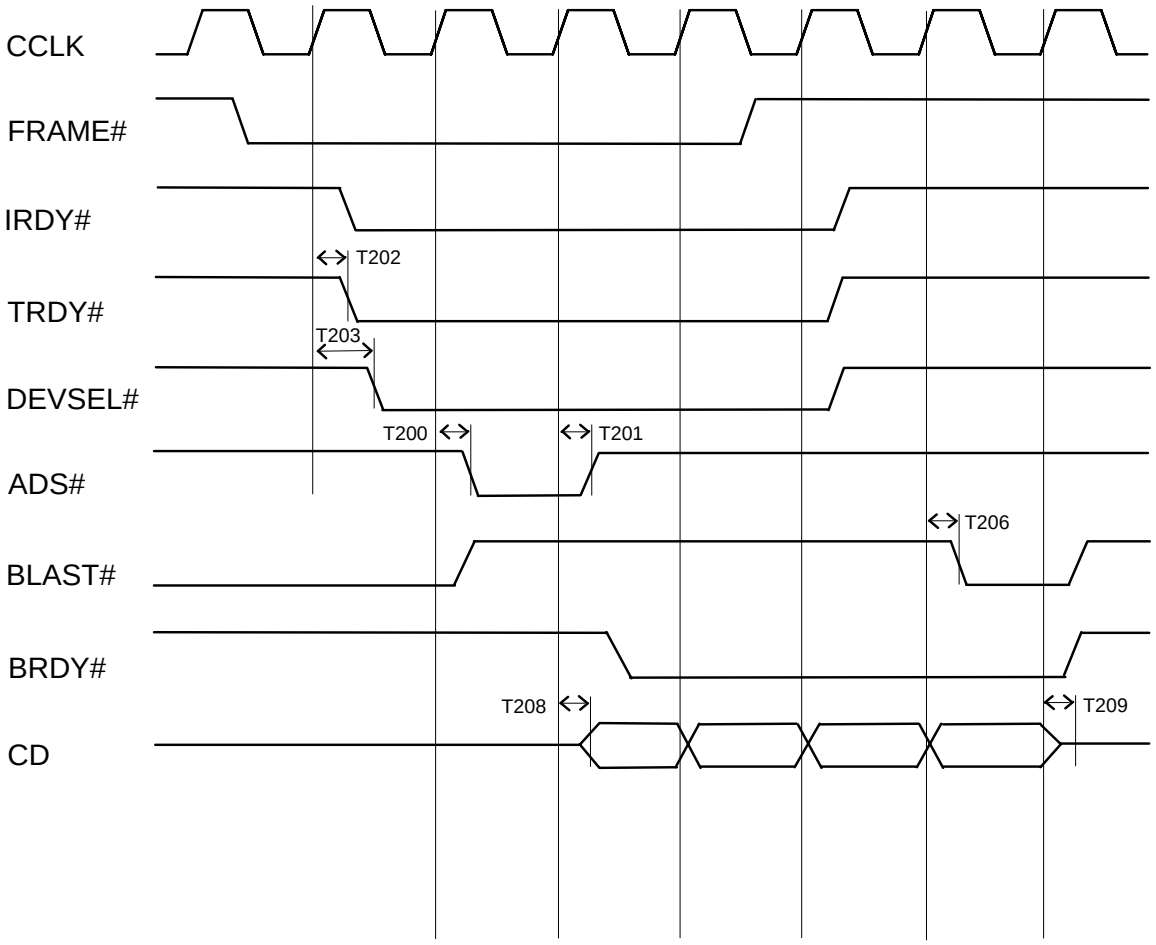
PCI Master Read Memory (Single Cycle)



PCI Master Read System Memory
(Prefetch Burst on both PCI and VL side)



PCI Master Write System Memory (Write-buffered and VL burst write)



160-Pin Plastic Flat Package