FlexSet™ PC/AT Single Chip Laptop LX

ADVANCE

FEATURES

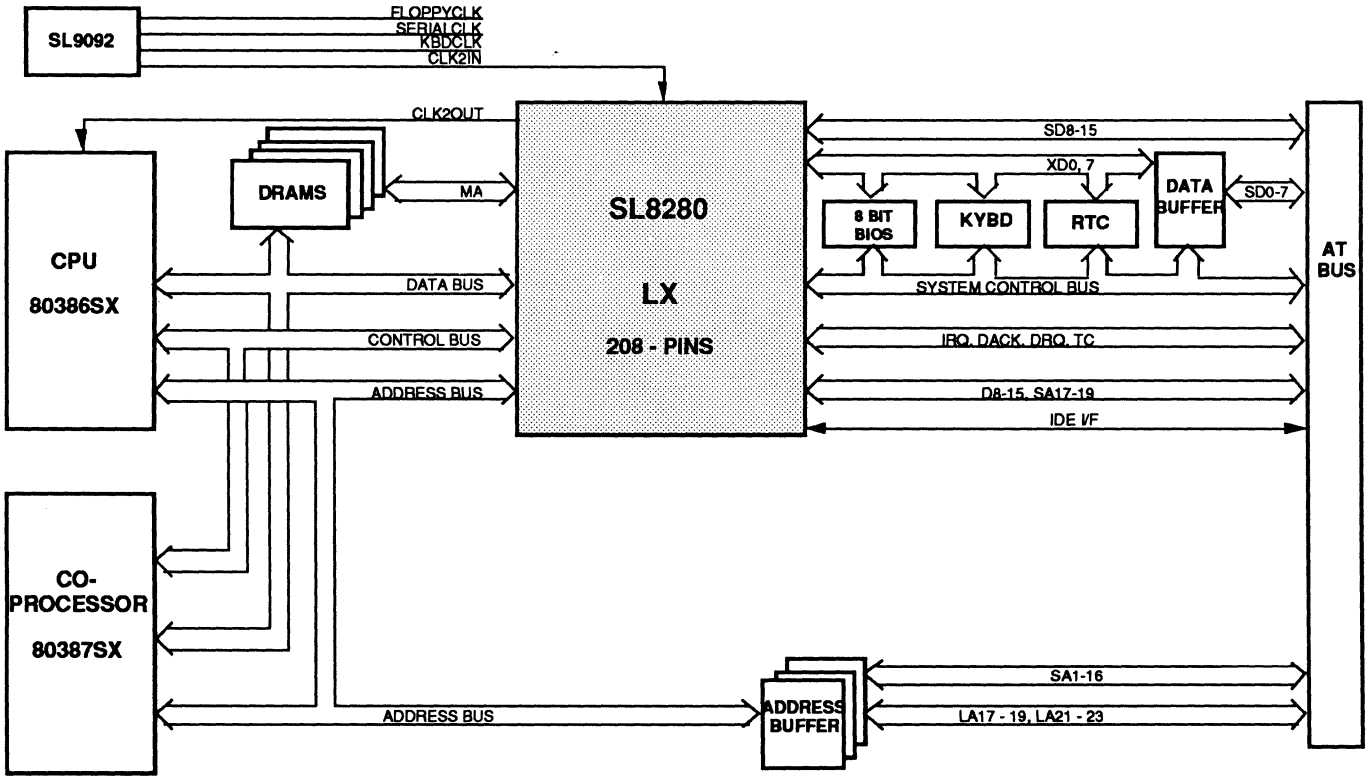
- Supports 80386SX based Laptop AT Designs.
- Glueless Interface for 387SX Co-processor.
- Supports Pipeline and Non-Pipeline Modes.
- Supports up to 20 MHz Designs.
- On Chip Advanced Page Mode Memory Control Unit (MCU).
- On Chip ISA Bus System Control Unit (SCU).
- On Chip Integrated Peripheral Control Unit (IPCU).
- On Chip Power Management Unit (PMU).
- Advanced Low Power 1.2 micron CMOS Technology.
- 208 Pin Plastic Flatpack.

May, 1991 (A)
4.050191

VIA Technologies, Inc. (408) 746-2200
860 East Arques Avenue
Sunnyvale, CA 94086

Overview

The SL8280 LX is a single chip around which a PC/AT compatible computer can be designed. It includes a Memory Control Unit, System Control Unit, Integrated Peripheral Control Unit, Power Management Unit, and incorporates a variety of programmable control features.



Laptop/Notebook Block Diagram

Memory Control Unit

The MCU offers advanced memory control functions and features needed to develop high performance PC/AT systems without using external TTL Logic. The MCU supports non-interleave and two-way page interleave mode for 80386SX based designs. Configuration registers can be used to enable or disable the Page interleave option. All memory banks which are interleaved use the same type of memory. Designers can enable the staggered RAS option during refresh, which minimizes power surge. Both pipeline and non-pipeline modes are supported by enabling or disabling the next address controls, and providing Ready at the correct time.

MCU Features:

- Page mode with 2 way interleave
- Supports 16 MB of on-board memory
- Shadow RAM with 16K granularity and 8 re-map options
- Programmable ROM chip select in 16K granularity
- Programmable ROM and RAM wait states
- Programmable RAS and CAS pre-charge
- Programmable memory partitioning to 0K in 128K resolution
- Can use 256K, 1M, or 4M DRAM's
- Staggered RAS refresh
- On chip parity generation and checking

System Control Unit

The SCU provides the AT System Control Logic. It generates all the major clocks for an AT compatible system design along with the command and control signals for both the system and peripheral busses. It interfaces with the CPU to determine the type of the bus cycle to execute, and generates the CPU READY signal. The SCU contains logic to make conversions between 16-bit and 8-bit data accesses. It also generates the control signals necessary for the 80387SX Numeric Processor.

The SCU controls all bus activity and provides arbitration between the CPU, DMA, External Master devices and the Refresh logic. It operates in four basic modes. First and most common, is the CPU mode. This mode is active any time CPUHLDA is LOW. The other modes can only be active when CPUHLDA is HIGH. These modes are DMA mode, External Master Mode, or Refresh Mode. If the inputs NAEN1 or NAEN2 are active, the SCU is in DMA mode and the command bus is driven from the Integrated Peripheral Control Unit (IPCU).

SCU Features:

- Synchronous and asynchronous ISA Bus support
- Programmable command delays
- Programmable memory and I/O wait states
- Fast gate A20 and Hot reset support
- Programmable BALE positioning
- Programmable READY positioning

Integrated Peripheral Control Unit

The Integrated Peripheral Control Unit (IPCU) is functionally compatible with VIA's Integrated Peripheral Controller SL9030 (and VTI's 82C100), and integrates two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 counter/timer and a 74LS612 equivalent along with support logic. It replaces all of the logic on the X bus of an AT-compatible design except the Keyboard Controller and Real Time Clock.

The IPCU consists of five major subsections. The chip select subsection is used to generate the chip select signals for each of the sub-cells within the IPCU.

The DMA subsection consists of two 8237 cells, two 8 bit latches to hold the middle range address bits during a DMA cycle and a 74LS612 equivalent cell to generate the upper range address bits during a DMA operation. The DMA subsection also has logic to force all DMA cycles to have one wait state inserted and additional logic to delay the leading edge of the MEMR signal for one DMA clock cycle. These functions are used to maintain AT-compatibility. The DMA subsection provides a total of seven external DMA channels. Four of these channels are used for 8 bit I/O adapters and the other three are used for 16 bit I/O adapters. All channels are capable of addressing all memory locations in a 16 megabyte address space.

The interrupt controller subsection consists of two 8259 cells cascaded together to accept 14 possible interrupt sources.

The counter/timer subsection contains a single 8254 cell. This cell has three internal counters. All of the counters are clocked at a 1.19 MHz rate. Gate inputs to counter 0 and 1 are always enabled (tied HIGH). Gate 2 is connected to the Q output of a flip-flop. The D input of this flip-flop is bit 0 of the X Data and is clocked by port B write decode. The output of Counter 0 is routed to the interrupt controller subsection to be used as interrupt request 0. The output from Counter 1 is routed to the hold request arbiter to initiate refresh cycles. Counter 2's output is available as an external pin.

The hold request arbiter and refresh subsection is used to arbitrate between a possible hold request from the DMA subsection or Counter 1 of the counter/timer subsection. This block of logic also controls the REFRESH output signal.

IPCU Features:

- Seven DMA channels
- 14 external Interrupt requests
- Three programmable timer counters
- 100% compatible with IBM AT I/O bus
- 74LS612 compatible memory mapping
- Quiet bus option for low power
- Support 16MB DMA address space

Power Management Unit

The on-chip Power Management Unit (PMU) supports three modes of operation, sleep mode, device auto power off and suspend/resume. As an option, slow refresh DRAM's can be used to further reduce power. In addition leads are provided to read AC power on and Low Battery Power status.

PMU Features:

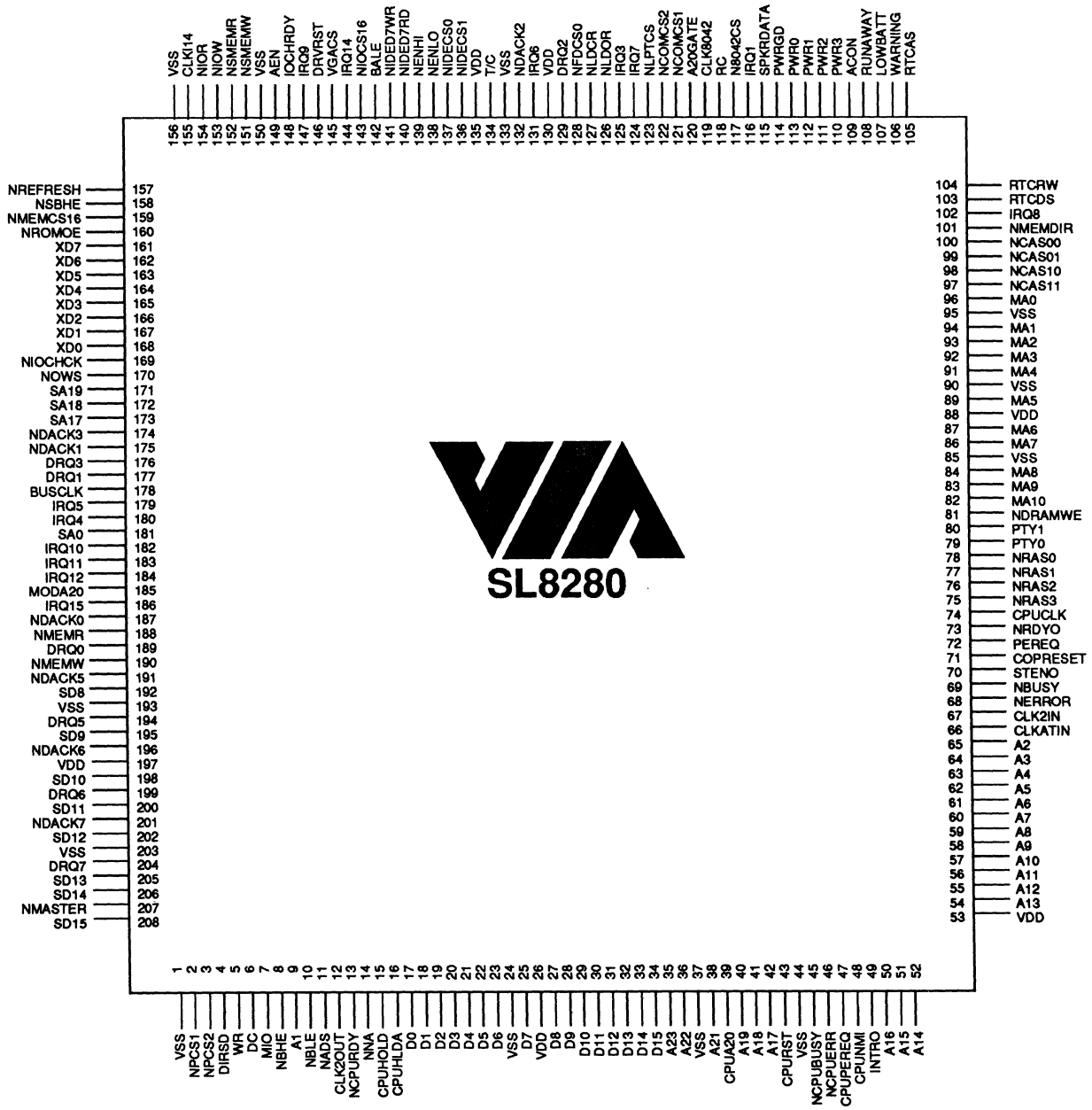
- Auto Power off when not in use
- Programmable peripheral power down option
- Supports sleep mode
- Supports suspend resume mode
- Supports slow refresh DRAM's
- Programmable quiet option for PC/AT I/O bus

Additional Features

These features allow the user to specify control logic states and addressing for I/O ports and to set up programmable chip selects. Register 25h controls I/O selections. Register 24h defines logic states for programmable chip selects (PCS), and registers 28h - 2Fh are used for addressing and address masking.

- Generates all address and data path controls
- On-chip byte swap logic and buffers
- Programmable peripheral chip select
- On-chip Port B and NMI logic
- Glueless I/F with Cirrus Logic VGA chipset
- Glueless I/F with FDC, serial/parallel chips

SL8280 PINOUT



LX Pin Descriptions

This section provides pin descriptions for the 208 pin SL8280. In some cases references are made to subunits within the chip which previously were individual IC's. These are also shown in the block diagram of the SL8280. Other signals may be referred to in later sections. These will be internal signals between blocks of the SL8280.

SYMBOL	PIN	TYPE	DESCRIPTION
			CPU I/F AND CLOCKS
CLK2IN	67	I	Input Clock used to generate CLK2 and clock internal state machine. It is twice the frequency of the CPU clock.
CLK2OUT	12	I/O	Clock 2 Output to CPU.
CLK8042	119	O	CLK8042 is CLKI14 divided by two. It is the keyboard controller clock.
CLKATIN	66	I	Asynchronous AT Clock Input. CLKATIN is twice the BUSCLK frequency, generated from the oscillator.
CLKI14	155	I	Clock In 14 MHz. 14 MHz being input from oscillator.
CPUA20	39	I/O	CPU Address Bus, bit 20. Output for ATbus MASTER accesses.
CPUCLK	74	O	Clock synchronized with 386SX internal clock. It is CLK2 divided by two.
CPUHLDA	16	I	CPU Hold Acknowledge. It is active HIGH when the bus is granted in response to hold request (HOLD). It is used to generate HLDA.
CPUHOLD	15	O	Hold is asserted HIGH whenever another bus master device like DMA or an external master wants to become a bus master. The signal goes to the CPU.
CPUNMI	48	O	NMI output connected to the CPU. It is active HIGH.

SL8280 PIN DESCRIPTIONS, CON'T

SYMBOL	PIN	TYPE	DESCRIPTION
CPUPEREQ	47	O	CPU Processor Extension Request. When active (HIGH) it indicates to CPU that NPX is ready for data transfer to/from its data FIFO. When FIFO is empty, this signal is negated. CPUPEREQ connects directly to the PEREQ pin on the CPU.
CPURST	43	O	This is the active HIGH CPU reset signal.
DC	6	I	CPU Status Signal. Differentiates between Data and Control instructions.
INTRO	49	O	CPU Interrupt out signal. Active HIGH, to be connected to CPU Interrupt input.
MIO	7	I	Memory Input/Output signal from the CPU. When HIGH, it indicates a memory cycle, when LOW, it indicates an I/O cycle.
NADS	11	I	Address Strobe is an active LOW input generated by the CPU. When asserted it indicates the start of a new cycle.
NBHE	8	I	Byte High Enable is an active LOW input signal which indicates the transfer of data on the high byte of the data bus. It is also asserted for 16-bit bus cycles. It is used to generate NENHI.
NBLE	10	I	Byte Low Enable is an active LOW input signal which indicates that the transfer of data is on the Low byte of the data bus. If is also asserted for 16 bit bus cycles.
NCPUBUSY	45	O	CPU Busy is an active LOW output to the CPU indicating that the NPX is busy executing a command. It connects to the CPU pin BUSY.

SL8280 PIN DESCRIPTIONS, CON'T

SYMBOL	PIN	TYPE	DESCRIPTION
NCPUERR	46	O	CPU Error is an active LOW output from the NPX to the CPU indicating that an unmasked error condition exists. NCPUERR connects to the ERROR input pin on the CPU.
NCPURDY	13	O	Ready is an active LOW output for the CPU.
NNA	14	O	CPU control input, Next Address. Asserted for address pipe-lining. Enables CPU to output address and status signals for the next Bus cycle during the current cycle.
WR	5	I	CPU status signal Write.
			NPX I/F
COPRESET	71	O	This output is latched RST387. It is connected to 80387SX coprocessor and it is active HIGH.
NBUSY	69	I	Numerical Coprocessor (NPX) Busy is an active LOW input indicating that NPX is currently executing a command. It is used to generate the busy signal to the CPU, NCPUBUSY.
NERROR	68	I	NPX Error is an active LOW input from 80X87. When asserted it indicates that a non-maskable exception has occurred during the current command cycle. It is used to generate NCPUERR.
NRDYO	73	I	Active LOW ready input from NPX.
PEREQ	72	I	NPX Peripheral Request is an active HIGH input from NPX. When asserted it causes CPUPEREQ to assert, indicating to the CPU that NPX is ready to transfer data to/from its data FIFO. When all data is written to or read from the data FIFO, PEREQ is negated.

SL8280 PIN DESCRIPTIONS, CON'T

SYMBOL	PIN	TYPE	DESCRIPTION
STENO	70	O	Status Enable is an active HIGH output. This pin serves as a chip select for the 80X87. When inactive, it forces the NPX outputs NBUSY, PEREQ, NERROR and NRDY into floating state.
			RAM I/F
MA0 - MA10	96,94-91, 89,87,86, 84-82	O	DRAM address bus.
NCAS00,01,10,11	100-97	O	Memory Column Address Strobe. Asserted LOW when either CPU or DMA master is accessing the memory. CAS for Bank 0 Byte 0, Bank 0 Byte 1, Bank 1 Byte 0 and Bank 1 Byte 1 respectively.
NDRAMWE	81	O	Memory Write is an active LOW input. It is asserted for local memory write cycles. It is used as /WE for DRAM.
NMEMDIR	101	O	Direction Select between D Bus and MD Bus. When LOW, direction is from MD Bus to D Bus (MEM Read). When HIGH, the direction is from D Bus to MD Bus (MEM Write).
NRAS0 - NRAS3	78-75	O	Row Address Strobes for Banks 0, 1, 2 and 3 for the on-board memory. Asserted LOW during CPU or DMA cycle master for memory access.
PTY0	79	I/O	Low Byte Parity.
PTY1	80	I/O	High Byte Parity.
			ROM I/F
NROMOE	160	I/O	This signal enables ROM output during ROM cycle. If the pin is sampled LOW at the trailing edge of reset then 8 bit ROM cycles are run and a byte conversion is initiated.

SL8280 PIN DESCRIPTIONS, CON'T

SYMBOL	PIN	TYPE	DESCRIPTION
			KBD I/F
A20GATE	120	I	CPUA20 is forced LOW when A20GATE is LOW and is transmitted as generated by CPU when A20GATE is HIGH.
IRQ1	116	I	Interrupt from keyboard connected to IRQ1 on the 8259 Interrupt Controller.
N8042CS	117	O	This active LOW signal is asserted to select the Keyboard Controller 8742 or 8042.
RC	118	I	External CPU Reset is an active LOW input. When asserted it resets the CPU by generating CPURST. It may come from a debounced switch.
			RTC I/F
IRQ8	102	I	RTC Interrupt Request, connected to IRQ8 of 8259.
RTCAS	105	O	Active HIGH Address strobe signal for RTC.
RTCDS	103	O	Active LOW Data strobe signal for RTC.
RTCRW	104	O	Active LOW Read/Write signal for RTC.
			POWER MANAGEMENT I/F
ACON	109	I	Active HIGH it indicates that the AC switch is ON.
LOWBATT	107	I	A LOW signal on this input indicates that the battery is getting weak and needs to be recharged.
PWR0-PWR3	113-110	O	These outputs control the power supply of different devices. When active (HIGH) it indicates that the power is ON.

SL8280 PIN DESCRIPTIONS, CON'T

SYMBOL	PIN	TYPE	DESCRIPTION
RUNAWAY	108	O	This output is generated if the CPU does not wake up after the sleep mode.
WARNING	106	O	This signal indicates low battery warning through either the speaker or LED.
			VGA I/F
A2-A19,A21-A23	65-54,52-50,42-40, 38,36,35	I/O	Address Bus.
AEN	149	O	DMA Address Enable. When LOW, enables data buffers between D Bus and SD Bus. It is HIGH during DMA cycles. It is used to drive SLOT AEN and the SL9025 Buffer Control.
D0 - D15	17-23,25, 27-34	I/O	Data Bus.
DRVRST	146	O	Device Reset is an active HIGH output. When asserted it resets the AT System. Directly drives the AT SLOT signal DRVRST.
IOCHRDY	148	I/O	I/O Channel Ready is an active HIGH input from the AT bus. When LOW it indicates a not ready condition and inserts wait states in AT I/O or AT memory cycles. It is used to generate NCPURDY. It is an output during NPX reset cycle.
NIOR	154	I/O	Input/Output Read is an active LOW bi-directional pin for the AT System bus. It is an output for CPU and DMA cycles and an input during an external master bus cycle.

SL8280 PIN DESCRIPTIONS, CON'T

SYMBOL	PIN	TYPE	DESCRIPTION
NIOW	153	I/O	Input/Output Write is an active LOW bi-directional pin for the AT System bus. It is an output during CPU and DMA cycles and an input during an external master bus cycle.
NMEMCS16	159	I	Memory Chip Select 16 is an active LOW input from the AT bus. When asserted, it indicates a 16 bit memory cycle. When HIGH it implies an 8-bit memory transfer. It is used to control NGAT1.
NREFRESH	157	I/O	The Refresh I/O signal will be pulled LOW by the IPCU whenever the 8254 counter 1 issues a CPUHRQ to the CPU and a hold acknowledge is received from the CPU. Refresh can also be used as an input if the refresh timing is to come from a source other than the 8254 channel 1 counter. Refresh is an open drain output capable of sinking 20 mA and requires an external pull-up resistor.
NSBHE	158	I/O	Byte High Enable is an active LOW bi-directional pin for the AT bus. It indicates the transfer of data on the high byte of the data bus. It is also asserted for 16-bit bus cycles. It is an output during CPU and DMA cycles and an input during an external master cycle.
NSMEMR	152	O	System Memory Read is an active LOW tri-state output for the AT bus. It is an output during CPU, DMA and refresh cycles. It goes to tri-state when more than 1 meg memory is accessed (protected mode).
NSMEMW	151	O	System Memory Write is an active LOW tri-state output for the AT bus. It is an output during CPU and DMA cycles. It goes tri-state when more than 1 meg memory is accessed (protected mode).
VGACS	145	O	Chip Select for VGA. Decodes 640K to 896K.

SL8280 PIN DESCRIPTIONS, CON'T

SYMBOL	PIN	TYPE	DESCRIPTION
			FD I/F
DRQ2	129	I	Input signal, DMA Request Bit 2 is an individual asynchronous request for DMA service connected to the 8237.
IRQ6	131	I	Interrupt Request bit 6 is an asynchronous interrupt request input to the 8259.
NDACK2	132	O	DMA Acknowledge Bit 2 output signal is an acknowledge signal for the corresponding DMA requests. The active polarity of this line is programmable and is set to active LOW on reset.
NFDCS0	128	O	Chip select for floppy 0.
NLDCR	127	O	Load Drive Control register for floppy drive.
NLDOR	126	O	Load Output register for floppy drive.
T/C	134	O	Terminal Count indicates that the terminal count of one of the DMA channels has been reached.
			SERIAL/PARALLEL PORT
IRQ3,4,7,9	125,180, 124,147	I	Interrupt Request from serial/parallel port.
NCOMCS1,2	121,122	O	Serial Port chipselect 1 and chipselect 2.
NLPTCS	123	O	Parallel Port Chip Select.
NPCS1,2	2,3	O	Low assert programmable chipselects 1 and 2.

SL8280 PIN DESCRIPTIONS, CON'T

SYMBOL	PIN	TYPE	DESCRIPTION
			IDE I/F
BALE	142	O	Buffered Address Latch Enable. Directly drives AT SLOT signal BALE.
IRQ14	144	I	Interrupt Request from HD connector interrupt 14 on chip Interrupt Controller 8259.
NIDECS0	137	O	Chip select 0 for IDE interface.
NIDECS1	136	O	Chip select 1 for IDE interface.
NIOCS16	143	I	Input/Output Chip select 16 is an active LOW input. It is asserted from AT bus by a 16-bit I/O device to indicate a 16-bit bus cycle. When HIGH it implies an 8-bit I/O transfer. It is used to control NGAT1.
SA0	181	I/O	System bus address bit 0 with HIGH drive I/O buffer.
			MISC. SIGNALS
PWRGD	114	I	Forcing PWRGD LOW generates a system reset (CPURST, DRVRST and NDRVRST). It is a schmidt trigger input and may be connected to a mechanical switch.
SPKRDATA	115	O	Active HIGH speaker data output. This is used to gate the timer tone signal to the speaker.
			AT BUS I/F
A1	9	I/O	Output when CPU is Master or during refresh cycle. Input for DMA and AT bus Master. To be connected to SA1 of AT bus.

SL8280 PIN DESCRIPTIONS, CON'T

SYMBOL	PIN	TYPE	DESCRIPTION
BUSCLK	178	O	System Bus Clock, can be 1/2 CPUCLK or 8MHz.
DIRSD	4	O	Direction control signal for system data bus drivers. HIGH enables D to SD transfer while LOW enables SD to D transfer.
DRQ0, 1, 3, 5, 6, 7	189,177, 176,194, 199,204	I	Input signals, DMA Request Bits 0, 1, 3, 5, 6 and 7, are the individual asynchronous requests for DMA service connected to the 8237. DRQ0 through DRQ3 supports transfers from 8 bit I/O adapters to/from 8 or 16 bit system memory. DRQ5 through DRQ7 support transfers from 16 bit I/O adapters to/from 16 bit system memory. DRQ4 is internally used to cascade the two DMA controllers together.
IRQ5, 10, 11, 12, 15	179,182-184,186	I	Interrupt Request bits 5, 10, 11, 12, and 15 are asynchronous interrupt request inputs to the 8259.
MODA20	185	I/O	CPU Address 20 gated with A20GATE.
NDACK0, 1, 3 NDACK5, 6, 7	187,175, 174,191, 196,201	O	DMA Acknowledge 0-3, 5-7 output signals are the acknowledge signals for the corresponding DMA requests. The active polarity of these lines is programmable and is set to active LOW on reset.
NENHI	139	O	Enable HIGH byte to the SL9020 Data Controller or D to SD buffers, is asserted LOW to enable HIGH byte data transfer between D8-D15 and SD8-SD15.
NENLO	138	O	Enable LOW byte to the SL9020 Data Controller or D to SD buffers, is asserted LOW to enable LOW byte data transfers between D0-D7 and SD0-SD7.
NIDED7RD	140	O	Active LOW IDE data7 Read.
NIDED7WR	141	O	Active LOW IDE data7 Write.

SL8280 PIN DESCRIPTIONS, CON'T

SYMBOL	PIN	TYPE	DESCRIPTION
NIOCHCK	169	I	This signal is asserted by the I/O devices to signal the CPU that an error has occurred on the channel.
NMASTER	207	I	External Master is an active LOW input from the AT bus. It indicates that an external master device is currently active.
NMEMR	188	I/O	Memory Read is an active LOW bi-directional signal. It is an output when CPU is reading peripheral or AT bus memory, or DMA is bus Master and during refresh cycle. It is an input to AT bus Master.
NMEMW	190	I/O	Memory Write is an active LOW bi-directional signal. It is an output when CPU is writing peripheral or AT bus memory, or DMA is bus Master and during refresh cycle. It is an input to AT bus Master.
N0WS	170	I	Zero Wait State is an active LOW input from the AT System bus. It causes termination of a bus cycle, at the cycle's phase 2 of the first T2.
SA17,18,19	173-171	O	System Address Bus bits 17, 18, 19.
SD8 - SD15	192,195, 198,200, 202,205, 206,208	I/O	SD Bus. 16 bit I/O channel data bus.
VDD	26,53,88,130, 135,197		+5V Power.
VSS	1,24,37,44,85, 90,95,133,150, 156,193,203		OV Ground.
XD0 - XD7	168-161	I/O	Peripheral Data Bus Bits 0-7. The eight least significant bits on the XD bus are bi-directional.

NOTES

NOTES