SiI 160
PanelLink® Digital Transmitter

April 2000

General Description

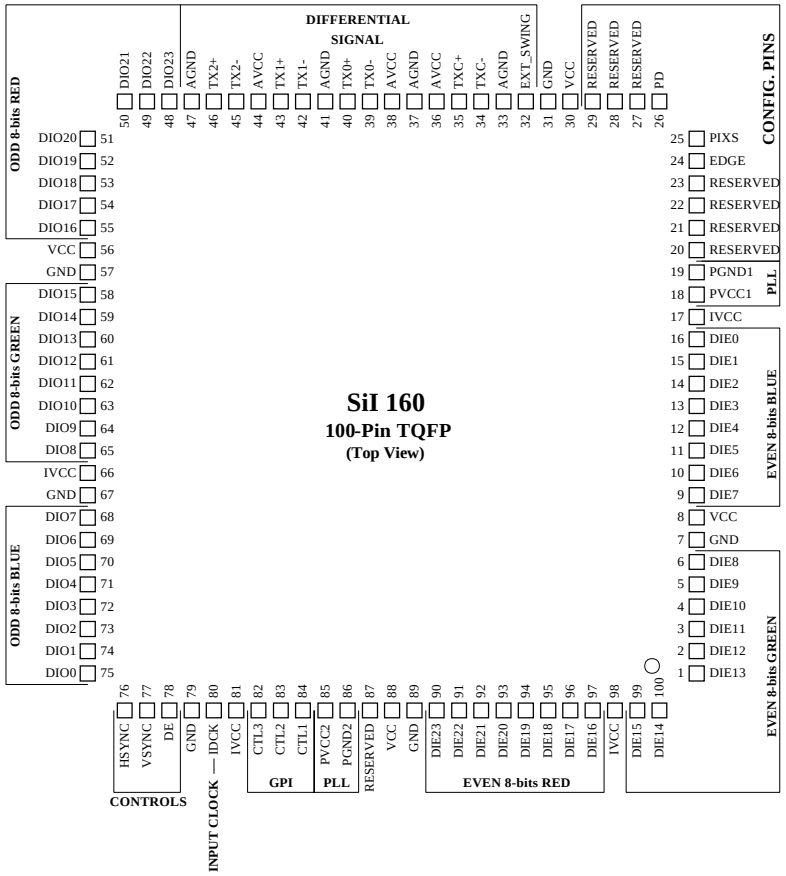
The SiI 160 transmitter uses PanelLink Digital technology to support displays ranging from VGA to UXGA resolutions (25-165 MHz). The SiI 160 transmitter supports up to true color panels (24 bit/pixel, 16.7M colors) in 1 or 2 pixels/clock mode, and also features an inter-pair skew tolerance up to 1 full input clock cycle. An advanced on-chip jitter filter is also added to extend tolerance to VGA clock jitter. Since all PanelLink products are designed on scaleable CMOS architecture to support future performance requirements while maintaining the same logical interface, system designers can be assured that the interface will be fixed through a number of technology and performance generations.

PanelLink Digital technology simplifies PC & display interface design by resolving many of the system level issues associated with high-speed digital design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

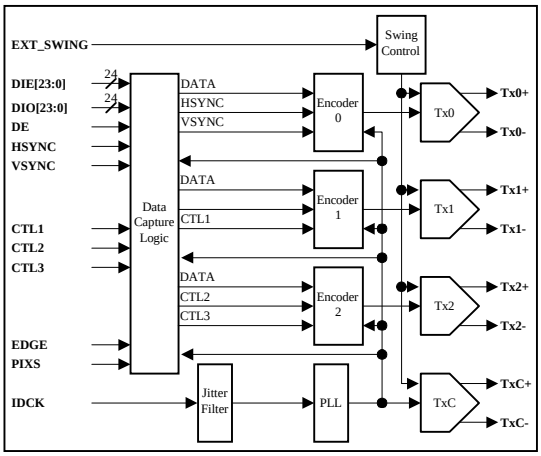
Features

- Scaleable Bandwidth: 25-165 MHz (VGA to UXGA)
- Low Power: 3.3V core operation
- High Skew Tolerance: 1 full input clock cycle (6ns at 165 MHz)
- Flexible panel interface: single or dual pixel in at up to 24-bits
- Sync Detect: for Plug & Display “Hot Plugging”
- Cable Distance Support: over 5m with twisted-pair, fiber-optics ready
- Compliant with DVI 1.0 (DVI is backwards compatible with VESA® P&D™ and DFP)

SiI 160 Pin Diagram



Functional Block Diagram



PanelLink® DIGITAL

Absolute Maximum Conditions

Note: Permanent device damage may occur if absolute maximum conditions are exceeded.
Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage 3.3V	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{CC}+ 0.3	V
V_O	Output Voltage	-0.3		V_{CC}+ 0.3	V
T_A	Ambient Temperature (with power applied)	-25		105	°C
T_{STG}	Storage Temperature	-40		125	°C
P_{PD}	Package Power Dissipation			1	W

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.00	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{P-P}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

DC Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
V_{CINL}	Input Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{CIPL}	Input Clamp Voltage[1]	I_{CL} = 18mA			IVCC + 0.8	V
V_{CONL}	Output Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{COPL}	Output Clamp Voltage[1]	I_{CL} = 18mA			OVCC + 0.8	V
I_{IL}	Input Leakage Current		-10		10	µA

Note: [1] Guaranteed by design.

DC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Voltage Single ended peak to peak amplitude	R_{LOAD} = 50 Ω R_{EXT_SWING} = 510 Ω	510	550	590	mV
V_{DOH}	Differential High-level Output Voltage[1]			AVCC		V
I_{DOS}	Differential Output Short Circuit Current[1]	V_{OUT} = 0 V			5	µA
I_{PD}	Power-down Current[2]				TBD	mA
I_{CCT}	Transmitter Supply Current	DCLK= 165 MHz, 1-pixel/clock mode, (DCLK= 112 MHz, 1-pixel/clock mode) R_{EXT_SWING} = 680Ω, IVCC = VCC, Typical Pattern[3]		70	95	mA
		DCLK= 165 MHz, 1-pixel/clock mode, (DCLK= 112 MHz, 1-pixel/clock mode) R_{EXT_SWING} = 680Ω, IVCC = VCC, Worse Case Pattern[4]		90	110	mA

Note: [1] Guaranteed by design.
[2] Assumes all inputs to the transmitter are not toggling.
[3] The Typical Pattern contains a gray scale area, checkerboard area, and text.
[4] Black and white checkerboard pattern, each checker is one pixel wide.

AC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{CIP}	IDCK Period, 1 Pixel/Clock		6.06		40	ns
F_{CIP}	IDCK Frequency, 1 Pixel/Clock		25		165	MHz
T_{CIP}	IDCK Period, 2 Pixels/Clock		12.3		80	ns
F_{CIP}	IDCK Frequency, 2 Pixels/Clock		12.5		81	MHz
T_{CIH}	IDCK High Time at 165MHz		2			ns
T_{CIL}	IDCK Low Time at 165MHz		2			ns
T_{IJIT}	Worst Case IDCK Clock Jitter[2,3]				2	ns
T_{SIDF}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Setup Time to IDCK falling edge	EDGE = 0	1.5			ns
T_{HIDF}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Hold Time from IDCK falling edge	EDGE = 0	1.5			ns
T_{SIDR}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Setup Time to IDCK rising edge[1]	EDGE = 1	1.5			ns
T_{HIDR}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Hold Time from IDCK rising edge[1]	EDGE = 1	1.5			ns
T_{DDF}	VSYNC, HSYNC, and CTL[3:1] Delay from DE falling edge[1]		T_{CIP}			ns
T_{DDR}	VSYNC, HSYNC, and CTL[3:1] Delay to DE rising edge[1]		T_{CIP}			ns
T_{HDE}	DE high time[1]				$8000T_{CIP}$	ns
T_{LDE}	DE low time[1]		$10T_{CIP}$			ns
S_{LHT}	Small Swing Low-to-High Transition Time	R_{LOAD} = 50Ω R_{EXT_SWING} = 510Ω	170	200	230	ns
S_{HLT}	Small Swing High-to-Low Transition Time	R_{LOAD} = 50Ω R_{EXT_SWING} = 510Ω	170	200	230	ns

Notes:
1. Guaranteed by design.
2. Jitter can be estimated by 1) triggering a digital scope at the rising of input clock and 2) measuring the peak to peak time spread of the rising edge of the input clock 1µs after the trigger.
3. Actual jitter tolerance may be higher depending on the frequency of the jitter.

Timing Diagrams

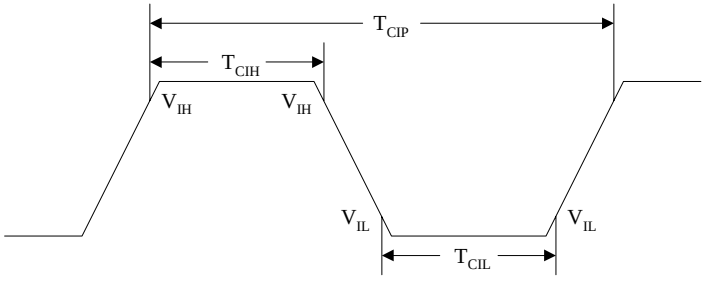


Figure 1. Clock Cycle/High/Low Times

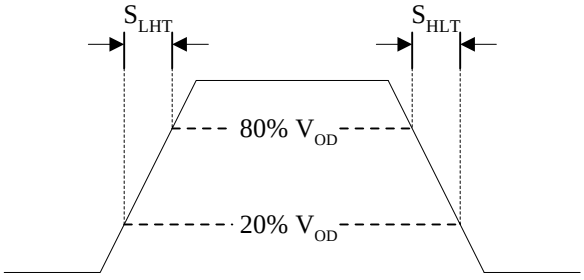


Figure 2. Small Swing Transition Times

Input Timing

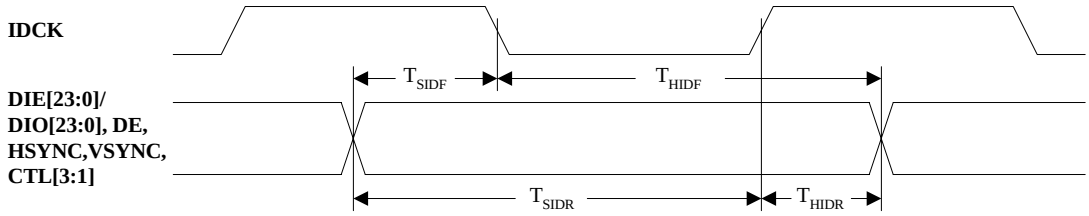


Figure 3. Input Data Setup/Hold Times to IDCK

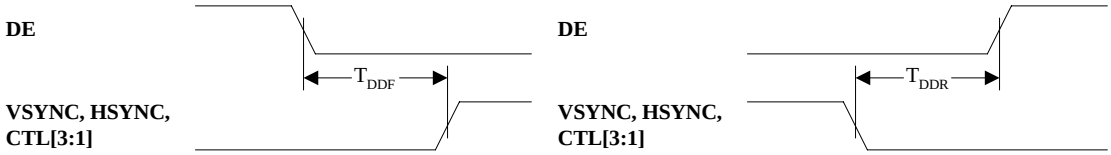


Figure 4. VSYNC, HSYNC, and CTL[3:1] Delay Times from DE

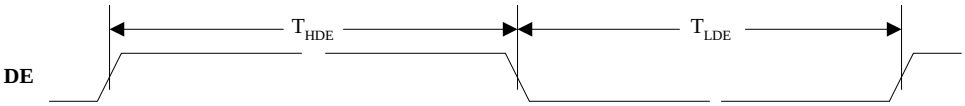


Figure 5. DE High/Low Times

Input Pin Description

Pin Name	Pin #	Type	Description
DIE23-DIE0	See SiI 160 Pin Diagram	In	Even Input Data[23:0] corresponds to 24-bit pixel data for 1-pixel/clock input mode or to the first 24-bit pixel data for 2-pixels/clock mode. Input data is synchronized to input data clock (IDCK). Data can be latched on the rising or the falling edge of IDCK depending on whether EDGE is high or low, respectively. Refer to the TFT and DSTN Signal Mapping application notes (SiI/AN-0008-A and SiI/AN-0007-A, respectively) which tabulate the relationship between the input data to the transmitter and output data from the receiver.
DIO23 – DIO0	See SiI 160 Pin Diagram	In	Input Odd Data[23:0] corresponds to the second 24-bit pixel data for 2-pixels/clock mode. In 1-pixel/clock mode, these inputs are a don't care. Recommendation is to tie them low for lower power consumption. Input data is synchronized to input data clock (IDCK). Data can be latched on the rising or the falling edge of IDCK depending on whether EDGE is high or low, respectively. Refer to the TFT and DSTN Signal Mapping application notes (SiI/AN-0008-A and SiI/AN-0007-A, respectively) which tabulate the relationship between the input data to the transmitter and output data from the receiver.
IDCK	80	In	Input Data Clock. Input data and control signals can be valid either on the falling or the rising edge of IDCK as selected by the EDGE pin.
DE	78	In	Input Data Enable. This signal qualifies the active data area. DE is always required by the transmitter and must be high during active display time and low during blanking time.
HSYNC	76	In	Horizontal Sync input control signal.
VSYNC	77	In	Vertical Sync input control signal.
CTL1	84	In	General input control signal 1.
CTL2	83	In	General input control signal 2.
CTL3	82	In	General input control signal 3.

Configuration Pin Description

Pin Name	Pin #	Type	Description
EDGE	24	In	Data/Control Latching Edge. A low level indicates that all input signals (DIE/DIO[23:0], HSYNC, VSYNC, DE, and CTL[3:1]) are latched on the falling edge of IDCK, while a high level (3.3V) indicates that all input signals are latched on the rising edge of IDCK.
PIXS	25	In	Pixel Select. A low level indicates one pixel (up to 24-bits) per clock mode using DIE[23:0]. A high level (3.3V) indicates two pixels (up to 48-bits) per clock mode using DIE[23:0] for the first pixel and DIO[23:0] for the second pixel.
RESERVED	27	In	This input must be tied high (3.3V), but we recommend that this pin have an option to tie it low.

Power Management Pin Description

Pin Name	Pin #	Type	Description
PD	26	In	Power Down (active low). A high level (3.3V) indicates normal operation and a low level (GND) indicates power down mode. During power down mode, all data (DIE/DIO[23:0]), data enable (DE), clock (IDCK) and control signals (HSYNC, VSYNC, CTL[3:1]), input buffers are disabled, all output buffers are tri-stated, and all internal circuitry is powered down.

Differential Signal Data Pin Description

Pin Name	Pin #	Type	Description
TX0+	40	Analog	TMDS Low Voltage Differential Signal output data pairs.
TX0-	39	Analog	
TX1+	43	Analog	
TX1-	42	Analog	
TX2+	46	Analog	
TX2-	45	Analog	
TXC+	35	Analog	TMDS Low Voltage Differential Signal output data pairs.
TXC-	34	Analog	
EXT_SWING	32	Analog	Voltage Swing Adjust. A resistor should tie this pin to AVCC. The amplitude of the voltage swing is determined by this resistance. For remote display applications, 400Ω is recommended. For notebook computers, 680Ω is recommended.

Reserved Pin Description

Pin Name	Pin #	Type	Description
RESERVED	20	In	Reserved for future use. Must be tied **HIGH** for normal operation.
RESERVED	21	In	Reserved for future use. Must be tied **LOW** for normal operation.
RESERVED	22	In	Reserved for future use. Must be tied **HIGH** for normal operation.
RESERVED	23	In	Reserved for future use. Must be tied **HIGH** for normal operation.
RESERVED	28	In	Reserved for future use. Must be tied **HIGH** for normal operation.
RESERVED	29	In	Reserved for future use. Must be tied **HIGH** for normal operation.
RESERVED	87	In	Reserved for future use. Must be tied **HIGH** for normal operation.

Power and Ground Pin Description

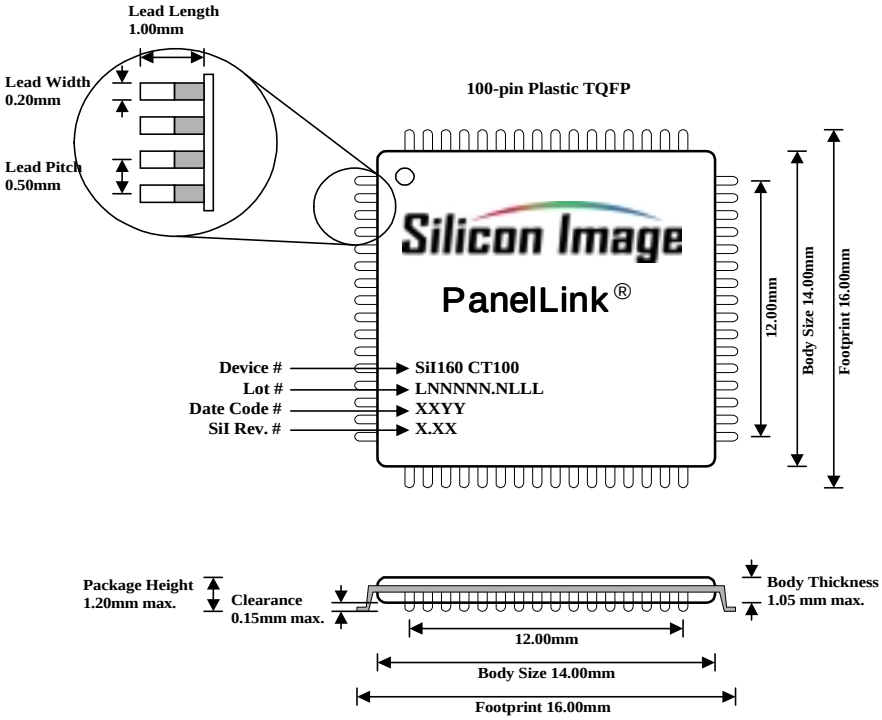
Pin Name	Pin #	Type	Description
VCC	8,30,56,88	Power	Digital Core VCC, must be set to 3.3V.
GND	7,31,57,67,79,89	Ground	Digital GND.
IVCC	17,66,81,98	Power	Input VCC, must be set to 3.3V.
AVCC	36,38,44	Power	Analog VCC, must be set to 3.3V.
AGND	33,37,41,47	Ground	Analog GND.
PVCC1	18	Power	PLL Analog VCC, must be set to 3.3V.
PVCC2	85	Power	PLL Analog VCC, must be set to 3.3V.
PGND1	19	Ground	PLL Analog GND. PGND1 **should not be directly connected to** PGND2 **before being connected to the GROUND plane. They should be connected individually to the GROUND plane.**
PGND2	86	Ground	PLL Analog GND. PGND1 **should not be directly connected to** PGND2 **before being connected to the GROUND plane. They should be connected individually to the GROUND plane.**

Application Information

To obtain the most updated Application Notes and other useful information for your design application, please visit the Silicon Image web site at ***www.siimage.com***, or contact your local Silicon Image sales office.

Package Dimensions

100-pin TQFP Package Dimensions



Ordering Information:

Part Number: SiI160CT100

Copyright Notice

Trademark Acknowledgment

Disclaimer

This document provides technical information for the user. Silicon Image, Inc. reserves the right to modify the information in this document as necessary. The customer should make sure that they have the most recent data sheet version. Silicon Image, Inc. holds no responsibility for any errors that may appear in this document. Customers should take appropriate action to ensure their use of the products does not infringe upon any patents. Silicon Image, Inc. respects valid patent rights of third parties and does not infringe upon or assist others to infringe upon such rights.

Silicon Image, Inc.
1060 E. Arques Avenue
Sunnyvale, CA 94086
USA

Tel: 408-616-4000
Fax: 408-830-9530
E-Mail: salessupport@siimage.com
Web: www.siimage.com
www.panellink.com