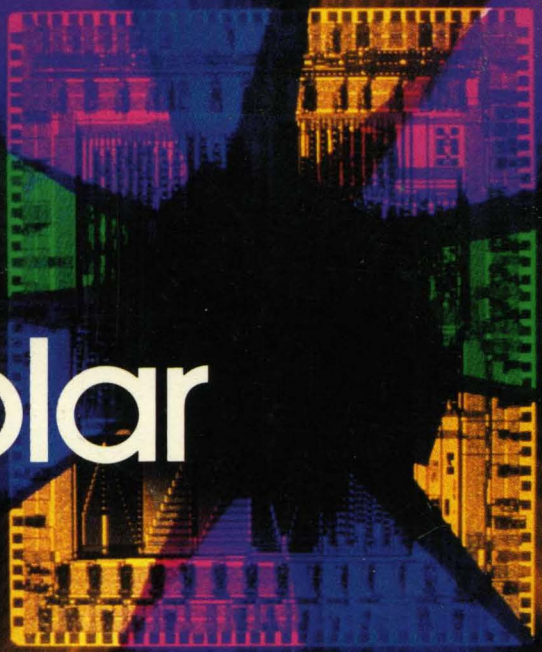
Signetics



Bipolar LSI Data Manual 1984

Bipolar LSI Data Manual
1984

Signetics

Signetics

PREFACE

The LSI Division of Signetics designs and manufactures a broad range of Bipolar products that includes both standard off-the-shelf devices as well as semicustom parts. Our standard product line is headed by a unique MicroController that is specifically designed for high-speed control applications. With peripherals that are presently available and those planned for the future, the MicroController provides a competitive edge in complex controller systems where speed, flexibility, reliability, and economy are prime considerations.

Semicustom products include gate arrays processed in one of four basic technologies — Integrated Schottky Logic (ISL), Composite Cell Logic (CCL), Emitter Coupled/Common Mode Logic (ECL/CML), and Complementary Metal Oxide Silicon (CMOS). These products provide the designer with various combinations of speed, packing densities, I/O capabilities, and power dissipation. All semicustom processes and tired-and-proven and Computer Aided Design (CAD) assures quick turnaround and error-free products.

All standard and semicustom products are processed, screened, and tested to the highest quality standards and, as indicated in the accompanying specifications, many of the parts are qualified for Military applications.

Signetics is continually developing new products to meet the changing needs of the world and the Marketing Department of the Bipolar LSI Division is continually searching for new and better ways of serving our customers — this manual being one of those ways. For further assistance, please call upon us or your nearest Signetics Sales Office.

Although every attempt has been made to ensure accuracy of the information contained herein, Signetics assumes no liability for errors. Suggestions for improvement in this document are always welcome.

PRODUCT DELETIONS

DELETIONS

8T35	PORT
8T33	PORT
8T39	PORT
8T31	PORT
8T32	PORT
8T36	PORT
8T42	4 – Input/4 – Output PORT

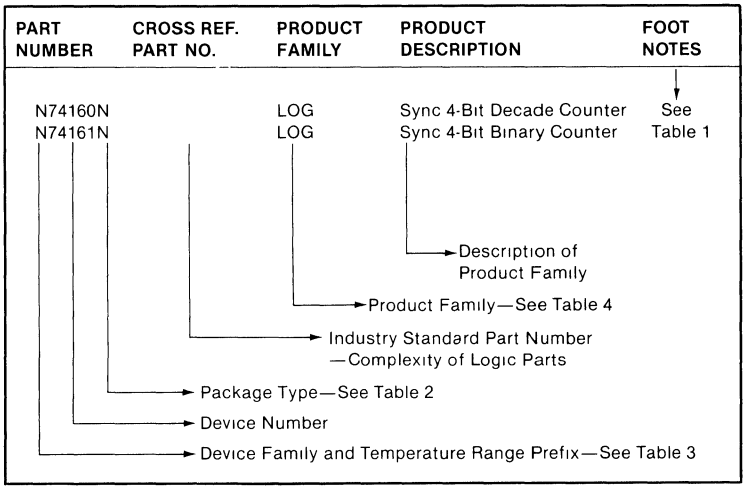
CONTENTS

CONTENTS

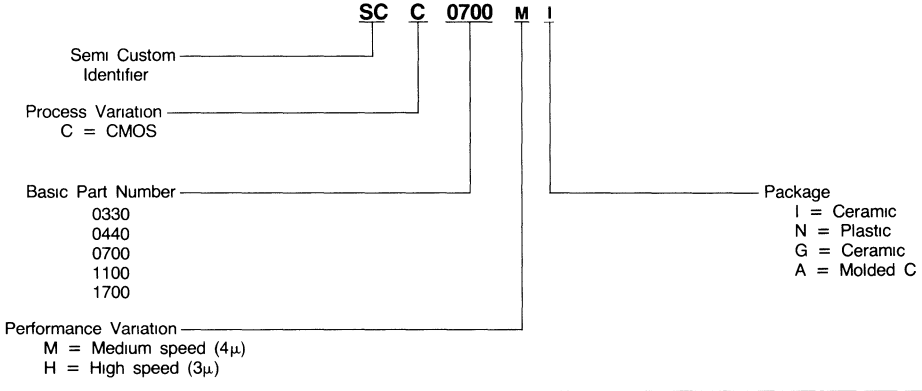
ORDERING INFORMATION

Package Styles

CK = Chip "S" visual and glassivation
D = Microminiature SO molded (epoxy)
EC = DMOS Products TO-46 header
EE = DMOS Products TO-72 header
F = Hermetic CERDIP
FE = Hermetic CERDIP - 8 lead
G = Chip carrier, leadless, type C
H = Hermetic metal header
I = Hermetic laminated DIP
N = DIP molded (epoxy)
P = DIP (ground pin) molded (epoxy)
Q = Hermetic laminated flat pack
R = Hermetic flat pack BeO base
U = Plastic power (single-in-line)
W = Hermetic flat pack - CERPAC
Y = Flat pack leads extended 4 sides



CMOS GATE ARRAY PART NUMBERING SYSTEM



ORDERING INFORMATION

ORDERING INFORMATION

The Signetics Military Products are available in a variety of different process levels and several different packages. The correct ordering code or part number for the devices is an alphanumeric sequence as explained below. Not all devices are available in all the packages. The ordering codes on the individual data sheets indicate the present or planned availability of the products. However, availability of specific part numbers can be obtained from your local sales office or franchised distributor.

Ordering Code

1) JM38510/07801BJB

- JB — LEAD FINISH
- J — PACKAGE TYPE
- B — CLASS "B"
- 07801 — SLASH SHEET NUMBER (BASIC DEVICE TYPE)
- JM38510/ — JAN QUALIFIED

2) JB54S181F

- F — PACKAGE TYPE
- 54S181 — BASIC DEVICE TYPE
- B — CLASS "B"
- J — JAN QUALIFIED

3) S54S181F883B

- B — LEVEL "B"
- 883 — MIL-STD-883
- F — PACKAGE TYPE
- 54S181 — BASIC DEVICE TYPE
- S — MILITARY TEMPERATURE RANGE (—55 TO 125°C)

4) RB54S181F

- F — PACKAGE TYPE
- 54S181 — BASIC DEVICE TYPE
- RB — MIL-STD-883, LEVEL "B"

NOTE
1) and 2) JAN qualified products
3) and 4) Non-JAN MIL-STD-883 products

For minimum quantity orders, contact your local Signetics sales representative.

PACKAGES AVAILABLE*

F = Ceramic DIP
I = Ceramic DIP
G = Ceramic Leadless Chip Carrier
W = Ceramic Flatpack

* See Package Outlines section for more information

For the latest military product information, please request a Military Products Guide from Publications Services, 408/746-2111.

ORDERING INFORMATION

BIPOLAR LSI ORDERING INFORMATION

3X300 I/O Peripheral Components

Various 8X300/8X305 MicroController I/O parts and bus expanders can be ordered with an address preprogrammed at the factory or unprogrammed to permit feild address assignment. Addresses in range indicated as STOCK in the table below may be ordered in any quantity. Addresses outside of the STOCK range but indicated as AVAILABLE require a minimum order of 250 pieces per line item per part type. To order, use the part number indicated in the table, substituting the desired address of xx or xxx when ordering preprogrammed parts.

PART NUMBER	ADDRESSES		ORDER NUMBER	
	AVAILABLE	STOCK	UNPROGRAMMED	PREPROGRAMMED
N8T32F	000-255	None	N8T32F	N8T32F-xxx
N8T32N	000-255	000-015	N8T32N	N8T32N-xxx
N8T36F	000-255	None	N8T36F	N8T36F-xxx
N8T36N	000-255	000-015	N8T36N	N8T36N-xxx
N8X372N	000-255	000-015	N8X372N	N8X372N-xxx
N8X374N	000-255	000-015	N8X374N	N8X374-xxx
N8X376N	000-255	000-015	N8X376N	N8X376N-xxx
N8X382N	000-255	000-015	N8X382N	N8X382N-xxx

MCCAP 8X300/8X305 CROSSASSEMBLER PROGRAM

MCCAP, the crossassembler program for the 8X300 and 8X305 Micro-Controllers, is supplied as a 9-track magnetic tape containing FORTRAN IV source code for the crossassembler program. For compatibility with various computer systems, the tape is available in various combinations of density and data encoding. To order, use the following part numbers.

NUMBER	DENSITY	ENCODING
8X300 AS1-1 SS	800	ASCII
8X300 AS1-2 SS	800	EBCDIC
8X300 AS1-3 SS	1600	ASCII
8X300 AS1-4 SS	1600	EBCDIC
8X300 AS2SS	SINGLE/ DOUBLE	FLOPPY DISK

PRODUCT STATUS DEFINITIONS

DEFINITION OF TERMS

Data Sheet Identification	Product Status	Definition
Preview	Formative or In Design	This data sheet contains the design specifications for product development Specifications may change in any manner without notice.
Advance Information	Sampling or Pre-Production	This data sheet contains advance information and specifications are subject to change without notice
Preliminary	First Production	This data sheet contains preliminary data and supplementary data will be published at a later date Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Section 1
Indices

NUMERICAL INDEX

STANDARD PRODUCTS

PRODUCT SUPPORT

SEMICUSTOM PRODUCTS

*The MCCAP Cross Assembler Manual is available on request.

BIPOLAR LSI CROSS REFERENCE GUIDE

BIPOLAR CROSS REFERENCE

Manufacture	AMD	FAIRCHILD	SIGNETICS

PACKAGE CROSS REFERENCES

Hermetic DIP	D	D, R	F-FE
Molded DIP	P	P	N
Mini-Molded DIP	T	T	NE
Metal Can	H	H	H
Small Outline (SO)	—	—	D

AMD	**SIGNETICS**
AM8X305	8X305
AM2960DC	N2960
AM2964B	N2964B

Fairchild	**SIGNETICS**
9401	N9401N
9403A	N9403N

Section 2
Quality and Reliability

SIGNETICS—PROGRESS IN QUALITY

INDUSTRY REQUIRES IMPROVED PRODUCT QUALITY

In recent years United States industry, and particularly those of you who buy integrated circuits, has increasingly demanded improved product quality. We at Signetics believe you have every right to expect quality products. If you buy components from a quality conscious manufacturer, the reward can be summed up in the words, lower cost of ownership.

Those of you who invest in costly test equipment and engineering to assure that incoming products meet your specifications have a special understanding of the cost of ownership. And your cost does not end there; you are also burdened with inflated inventories, lengthened lead times, and more rework.

Signetics Understands Customers' Needs

Signetics has long had an organization of quality professionals inside the operating units, coordinated by a corporate quality department. This organization provides leadership, feedback, and direction for achieving our high level of quality. Special programs are targeted on specific quality issues. For example, a program to reduce electrically defective units improved outgoing quality levels by an order of magnitude.

This graph shows how dramatically electrical, mechanical, and visual defects have been reduced across all product lines.

These improvements result from our emphasis on defect prevention which allows us to build quality into the product during manufacturing instead of relying on screening and sampling to remove defective parts.

The corresponding improvement in the estimated process quality (which measures the level of defective units produced during the manufacturing process prior to outgoing quality assurance) conclusively supports this fact.

You benefit from improved and more consistent product conformance at lower product cost.

In 1980 (see accompanying diagram) we recognized that in order to achieve outgoing levels on the order of 100 PPM (parts per million), down from an industry practice of 10,000 PPM, we needed to supplement our traditional quality programs with one that encompassed all activities and all levels of the company. Such unprecedented low defect levels could only be achieved by contributions from all employees, from the R and D laboratory to the shipping dock. In short, a program that would effect a total cultural change within Signetics in our attitude toward quality.

This new concept is based on the 14-step quality improvement program developed by Phil Crosby and outlined in his book Quality is Free.* The program focuses on defect prevention as the means of attaining improved quality.

Quality Pays Off for Our Customers

Signetics' dedicated programs in product quality improvement, supplemented by close working relationships with many of our customers, have improved outgoing product quality more than twenty-fold. Today many major customers no longer test Signetics circuits. Incoming product moves directly from the receiving dock to the production line, greatly accelerating throughput and reducing inventories. Additional customers have pared significantly the amount of sampling done on our products. Others are beginning to adopt these cost-saving practices.

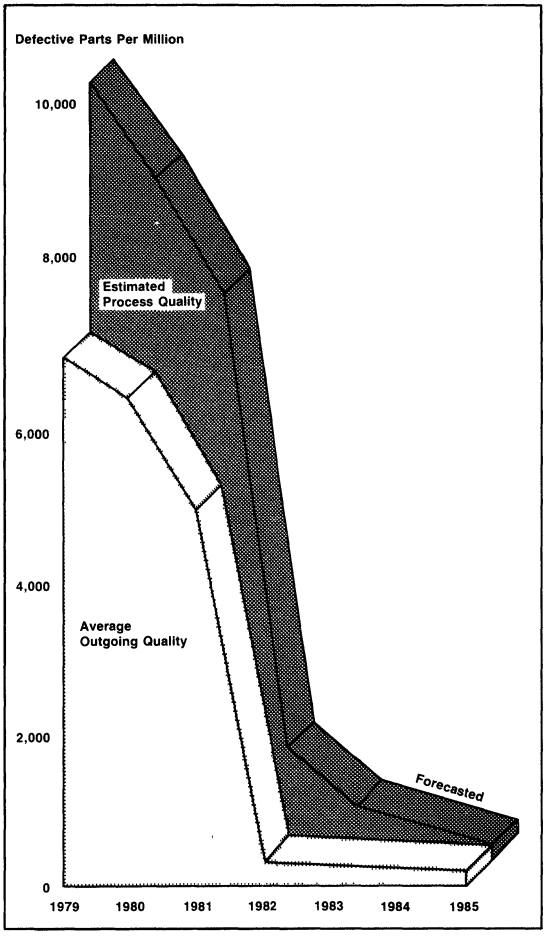


Figure 1. Reduction of Defects

We closely monitor the electrical, visual, and mechanical quality of all our products and review each return to find and correct the causes. Since 1981, over 90% of our customers report a significant improvement in our overall quality.

At Signetics, quality means more than working circuits. It means on-time delivery of the right quantity of the right product at the agreed upon price. Our quality improvement programs extend out from the traditional areas of product conformance into the administrative areas which affect order entry, scheduling, delivery, shipping, and invoicing.

SIGNETICS—PROGRESS IN QUALITY

Performance To Schedule

Signetics' attention to administrative quality has resulted in improved performance to schedule Doing it right the first time

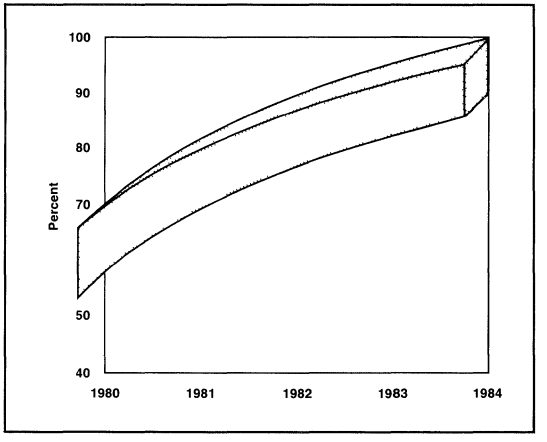


Figure 2. On Time Delivery

Signetics is Organized for Quality

Managing Cultural Change—
The "14-Step" Program
Quality College
Quality Improvement Teams
"Make Certain" Program
Corrective Action Teams
Error Cause Removal System

Engineering Quality
into the Product
SURE Program
Manufacturing Plant Product Monitoring
Qualification Programs
Vendor Certification Programs
Product Quality Program

Supporting
Quality Maintenance
Product Line
Quality and Reliability Assurance
Corporate Quality and Reliability
Failure Analysis Laboratories
Reliability Data Base
Statistical Quality Control

Ongoing Quality Programs at Signetics

The "14-Step" Quality Improvement Program, or "Do it Right the First Time"

The intent of this innovative program is to change the perception of Signetics' employees that somehow quality is solely a manufacturing issue where some level of defects is inevitable. This attitude has been replaced by one of acceptance of the fact that all errors and defects are preventable, a point of view shared by technical and administrative functions equally, and, we are sure, welcomed by our customers.

This program is company-wide and top down. It is personally led by President Charles Harwood who, with his staff, forms the corporate quality improvement team which implements corporate quality policy. Supporting the corporate quality improvement team are more than 40 quality improvement teams representing every unit in the company, each led by the unit manager.

Key components of the program are the Quality College, the "Make Certain" Program, Corrective Action Teams, and the Error Cause Removal System.

The core concepts of doing it right the first time are embodied in the four absolutes of quality:

1. **The definition of quality is conformance to requirements.**
2. **The system to achieve quality improvement is prevention.**
3. **The performance standard is zero defects.**
4. **The measurement system is the cost of quality.**

Quality College

Almost continuously in session, the Quality College is a prerequisite for all management and technical employees. The intensive two-day curriculum is built around the four "absolutes" of quality; colleges are conducted at company facilities throughout the world. More than 3000 employees have attended.

"Making Certain"—Administrative Quality Improvement

Signetics' experience has shown that the largest source of errors affecting product and service quality is found in paperwork and in other administrative functions. The "Make Certain" program focuses the attention of management and administrative personnel on error prevention, beginning with each employee's own actions.

This program promotes defect prevention in three ways: by educating employees as to the impact and cost of administrative errors, by changing attitudes from accepting occasional errors to one of accepting a personal work standard of zero defects, and by providing a formal mechanism for preventing errors.

Corrective Action Teams

Employees with the perspective, knowledge, and necessary skills are formed into ad hoc groups called Corrective Action Teams. These teams, the major force within the company for quality improvement, resolve administrative, technical, and manufacturing problems.

Error Cause Removal (ECR) System

The ECR System permits our employees to report to management any impediment to doing their job right the first time. Once

SIGNETICS—PROGRESS IN QUALITY

reported, management is obliged to respond promptly with a corrective program. Doing it right the first time in all company activities produces lower cost of ownership through product defect prevention and in all other ways meets our customers' expectations.

Product Quality Program

To reduce defects in outgoing products to nearly immeasurable levels, we created the Product Quality Program. This is managed by the Product Engineering Council, a task force composed of the top product engineering and test professionals in the company. This group:

1) Sets aggressive product quality improvement goals.
2) Provides corporate level visibility and focuses on problem areas.
3) Serves as a corporate resource for any group requiring assistance in quality improvement.
3) Serves as a corporate resource for any group requiring assistance in quality improvement.
4) Drives quality improvement projects.

As a result of this aggressive program, every major customer who reports back to us on product performance is reporting significant progress.

Standard Quality Programs

"SURE"—This acronym stands for Systematic Uniform Reliability Evaluation and is an on-going product evaluation first introduced in 1964. This activity provides our customers and us with an ongoing view of reliability performance of all generic families of Signetics' products.

Product Monitor—Each manufacturing facility monitors its generic product groups with short term stress tests, pressure pot and thermal shock. These tests are performed weekly, and performance trends are monitored to ensure that unwanted process deviations are spotted quickly and corrected before appearing in product received by our customers.

Qualification—Formal qualification procedures are required for all new or changed products, processes and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by the corporation and by the quality organizations of the product line that will operate the facility. After qualification, products manufactured by the new facility are subjected to highly-accelerated environmental stresses to ensure that the products can meet rigorous failure rate requirements. New or changed processes are qualified similarly.

Failure Analysis—This vital function is conducted by product line and plant failure analysis units coordinated through the corporate failure analysis group, a part of corporate reliability engineering. Our ten failure analysis groups will be expanded to 16 by the end of 1984 in our ongoing effort to accelerate and improve our understanding of product failure mechanisms.

Reliability Data Base—This computerized data base contains product reliability information collected from around the world. It is updated and published quarterly in "Signetics Product Reliability Summary."

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly procedures.

Vendor Certification Program—Our vendors are taking ownership of their own product quality by establishing improved process control and inspection systems. They subscribe to the zero defects philosophy. Progress has been excellent. Through intensive work with vendors, we have improved our lot acceptance rate on incoming materials as shown in the graph. Simultaneously, waivers of incoming material have been eliminated.

Material Waivers

1983–0 (Goal)
1982–2
1981–3
1980–134

Higher incoming quality material to us ensures higher outgoing quality products for you.

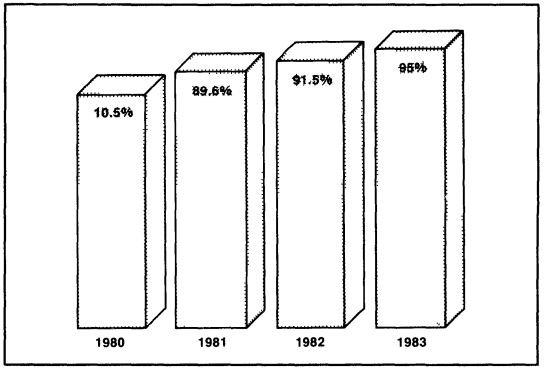


Figure 3. Lot Acceptance Rate from Signetics Vendors

QUALITY AND RELIABILITY ORGANIZATION

Quality and reliability specialists at the product line level are involved in all aspects of the product, from design through every step in the manufacturing process, and provide product assurance testing of outgoing product. A separate corporate level group provides direction and common facilities.

Quality and Reliability Function

- Manufacturing quality control
- Product assurance testing
- Laboratory facilities
  —failure analysis, chemical, metallurgy, thin film, oxides
- Environmental stress testing
- Quality and reliability engineering
- Customer liaison

SIGNETICS—PROGRESS IN QUALITY

Communicating With Each Other

For information on Signetics' quality programs or for any question concerning product quality, the field representative in your area will provide you with the quickest access to answers. Or, write on your letterhead directly to the Corporate Director of Quality at the corporate address shown on the back of this folder.

We are dedicated to preventing defects. When product problems do occur, we want to know about them so we can eliminate their causes. We are committed to zero defects. Here are some ways we can help each other:

- Provide us with one informed contact within your organization. This will establish continuity and build confidence levels.
- Periodic face-to-face exchanges of data and quality improvement ideas between your engineers and ours can help prevent problems before they occur.
- Test correlation data is very useful. Line pull information and field failure reports also help us improve product performance.
- Provide us with as much specific data on the problem as soon as possible to speed analysis and enable us to take corrective action.
- An advance sample of the devices in question can start us on the problem resolution before physical return of shipment.

This teamwork with you will allow us to achieve our mutual goal of improved product quality.

Quality Terms

Many terms and acronyms for quality have come into common use in conversation, in correspondence, and in the many reports on the subject in this quality conscious time. To help us all speak the same language, we hope the following glossary is useful to you.

AQL— Acceptable Quality Level—the maximum percent defective that, for the purpose of sampling inspection, can be considered satisfactory as a process average.

AOQ— Average Outgoing Quality—the average percent defective shipped (from accepted tests only) using rectifying inspection sampling. Rectifying is rescreening rejected lots and removing all defectives.

AOQL— Average Outgoing Quality Limit—the worst, or limit of, average quality of outgoing product including accepted lots and rejected lots that have been screened.

a— Producer's risk of a sampling plan—the probability that a "good" lot will be rejected by the sampling plan.

B— Consumer's risk of a sampling plan—the probability that a "bad" lot will be accepted by the sampling plan.

CAT— Corrective Action Teams—intra- and inter-department teams formed to solve problems.

Defect— Any nonconformance of the unit or product with a specified requirement.

Defective— A unit of product which contains one or more defects.

ECR— Error Cause Removal—a system allowing all employees to communicate problems that prevent them from performing their job correctly the first time.

EPQ— Estimated Process Quality—the measure of the performance of the product without rescreens. Expressed in percent or PPM.

Make Certain— An element of Signetics' Quality Program established for problem solving in administrative activities. Make Certain helps people "do it right the first time."

LAR— Lot Acceptance Rate—the number of lots accepted, divided by the total lots inspected, times 100.

LRR— Lot Rejection Rate—the number of lots rejected, divided by the total lots inspected, times 100.

LTPD— Lot Tolerance Percent Defective—the level of defectiveness that is unsatisfactory and should be rejected by the sampling plan.

PPM— Parts Per Million—a unit of measure of defects identified in a product or process expressed in defects per million units.

Quality— Conformance to requirements (specification).

SQC— Statistical Quality Control—a process control tool used to manage the manufacturing processes to ensure that they do not produce defects.

SUPR— Signetics Upgraded Product Reliability—a program offered on commercial products to provide customers with improved, reliable product.

SURE— Systematic and Uniform Reliability Evaluation—a program which consists of repetitive environmental stress management of all Signetics' generic product families.

URR— Unit Rejection Rate—the sum of all units rejected, divided by the total number of units which were inspected. Expressed in percent or PPM. Under certain conditions, the EPQ or AOQ may be the same as the URR.

ZD— Zero Defects—Signetics' quality performance standard.

SIGNETICS—PROGRESS IN QUALITY

ASSURING THE QUALITY OF LSI DIVISION PRODUCTS

Quality is built into the LSI Division product. Our in-process inspections have gone beyond testing to verify that the product will meet spec. Instead, all our inspection criteria meet the much tighter standard of assuring that the processes used to make our products are all in control. By the time the product reaches the end of our production line, our process average is 99 83/100% good. The final 100% testing sequence improves even this level to 99 93/100% (700 "ppm") before the product is shipped.

Figure 1 shows a brief summary of the process.

TABLE II—LSI QUALITY LEVELS

The following is a brief glimpse of our actual quality performance. The measure is SOQ. Please contact us for more complete information.

	PPM
Period 1, 1983	1500
Period 2, 1983	1200
Period 3, 1983	1124
Period 4, 1983	1410
Period 5, 1983	671
Period 6, 1983	658

TABLE III—LSI DIVISION RELIABILITY SUMMARY

For more complete data summaries, please ask for the latest LSI Division SURE III Test Program Report. The following capsule summary shows process averages for the first half of 1983.

	Failure Rate
Operating high temperature life test:	0.00%/1000 hrs.
Storage high temperature life test:	0.00%/1000 hrs.
Temperature/Humidity Bias Stress:	0.00%/1000 hrs.
Thermal Shock:	0.68%/100 cycles
Temperature Cycle:	0.00%/1000 cycles

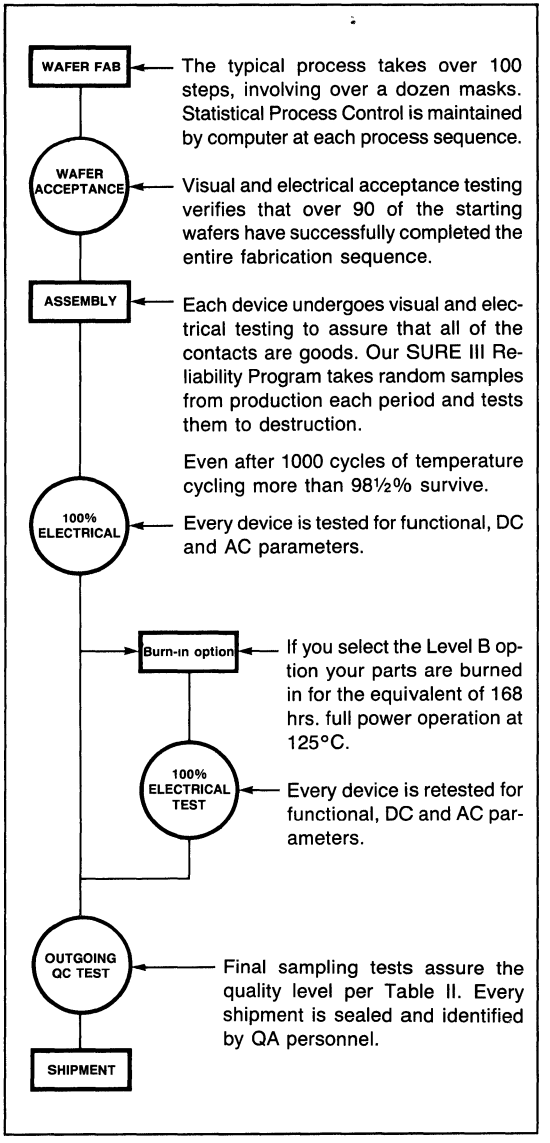


Figure 4. The LSI Process

NOTES

Section 3
8X300 Family

INDEX

BIPOLAR MICROPROCESSORS — 8X300 FAMILY

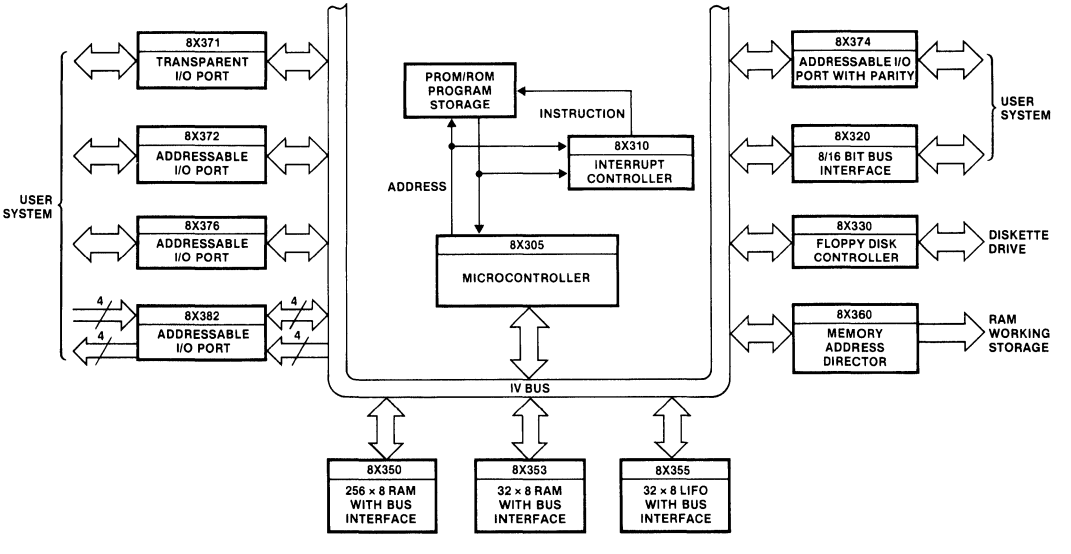
FEATURES

- Minimum Parts Count
- Bipolar Device Using Low Power Schottky Technology
- High Performance
- Source/Destination Architecture
- Design Flexibility
- After-Sales Support

USER BENEFITS

- Reduced Cost
- Extended Life of Product
- Full System Drive Without Buffering
- TTL Compatibility
- Proven Reliability
- Instruction Cycle Time of 200ns (8X305) or 250ns (8X300)
- Bit Addressability — Instruction Data Formats of 1-to-8 Bits Without Added Delay
- Efficient Use of Fixed Instruction Set
- Easy to Program
- Well-Suited for Control Applications
- Single-Chip Processor
- Full Complement of Support Devices
- Development System
- Training
- Complete Documentation
- Applications Support from Qualified Field Engineers

8X300 FAMILY



NOTES
1 The shaded devices are designed to take advantage of the improved performance of the 8X305
2 Refer to "Reference Table" on next page for a descriptive summary of each part in the 8X300 Family
3 The actual parts used in a specific system are selected based on the application requirements

PRODUCT LINE OVERVIEW

The Bipolar LSI Microprocessor product line is centered around two high-speed, Schottky-fabricated, MicroControllers and a large family of I/O devices, support ICs, and development support tools to expedite and simplify system design. No other microprocessor product line offers the advantages of the 8X300 Family in systems requiring intelligent control of high-speed data streams.

The MicroControllers themselves are capable of fetching, decoding, and executing each instruction in one machine cycle (250ns for the 8X300 and 200ns for the 8X305). A single instruction can read data from the bus, mask it, shift it, perform an ALU operation on it, rotate it, merge it, and return it to the bus. The architecture and instruction set of each processor are designed to provide high data throughput with both bit and byte oriented operations. The 8X305 offers more on-chip registers and significant data handling capability improvements over the original 8X300.

Because of its extremely high speed, the 8X300 family is able to perform through software many operations that would otherwise require additional hardware in the system. For example, using either MicroController, the 8X330 Floppy Disc Controller, and other support devices, a complete diskette drive controller can be built using only 10 Integrated Circuits. The resulting controller is programmable and capable of supporting multiple drive types and formats. Low parts counts typical of 8X300 Family designs result in reduced assembly and testing time, lower power consumption, and improved reliability.

The 8X300 Family is implemented using bipolar, Low-power Schottky technology to provide TTL speeds and drive capability without additional buffering. In addition, the family is compatible with most special-purpose devices often required in control applications. The excellent environmental characteristics of the technology make the 8X300 family ideal for military applications as well.

A complete complement of development support tools are offered to simplify design using the 8X300. A self-contained universal development system is available that supports full speed in-circuit emulation. Software tools are provided to enable use of mainframe or minicomputers to generate 8X300 software. Complete documentation is in place, including both data sheets and comprehensive reference manuals. In addition, evaluation and demonstration systems are available. To supplement these tools, Signetics employs a large, professional staff of applications engineers both in the field and at the factory to support your 8X300 design efforts.

8X300 FAMILY REFERENCE TABLE

PART NO.	PRODUCT DESCRIPTION	FUNCTION
8X300	MicroController	250ns processor for I/O and data control
8X305	MicroController	200ns processor for I/O and data control
8X310	Interrupt Controller	3 prioritzed interrupts with 4-level stack
8X320	Bus Interface Array	2-port RAM for 8/16-bit mailbox interfacing
8X330	Floppy Disk Controller	1Mb/sec data rate, programmable, supports ECC
8X350	Bipolar RAM	256 x 8 high-speed memory with bus interface
8X360	Memory Address Director	16-bit address controller for working storage
8X337	Transparent I/O Port	High-speed, 8-bit bidirectional, 3-state
8X372	Addressable I/O Port	High-speed, 8-bit bidirectional, synchronous, 3-state
8X376	Addressable I/O Port	High-speed, 8-bit bidirectional, asynchronous, 3-state
8X382	Addressable I/O Port	High-speed, 4-in/4-out, 3-state
8T31	Transparent I/O Port	8-bit bidirectional, 3-state
8T32	Addressable I/O Port	8-bit bidirectional, synchronous, 3-state
8T36	Addressable I/O Port	8-bit bidirectional, asynchronous, 3-state

MICROCONTROLLER 8X300

FEATURES

- **Fetch, Decode, and Execute a 16-bit instruction in a minimum of 250-nanoseconds (one machine cycle)**
- **Bit-oriented instruction set (addressable single-or-multiple bit subfields)**
- **Separate address, instruction, and I/O buses**
- **Source/destination architecture**
- **On-Chip oscillator and timing generation**
- **Eight 8-bit working registers**
- **TTL inputs and outputs**
- **BiPolar Low-Power Schottky technology**
- **3-State I/O bus**
- **Single +5V supply**

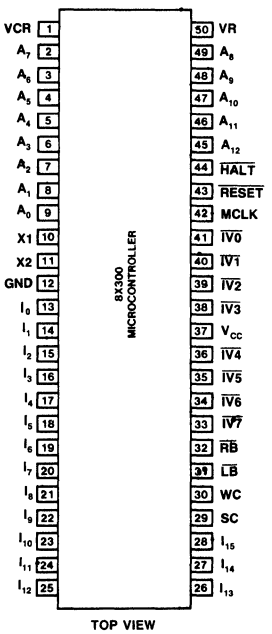
ARCHITECTURAL OVERVIEW

The Signetics 8X300 Microcontroller (Figure 1) is a high-speed bipolar microprocessor implemented with low-power Schottky technology. The 8X300 brings together all the qualities needed—SPEED, FLEXIBILITY, and ECONOMY—for systems design in the many areas that require reliable bit stream management. Consider!—5V operation, TTL bus compatibility, and an on-chip clock—the result, a system with fewer parts. Consider!—the inherent power of LSI logic (programmable Rotate, Mask, Shift, and Merge functions in the data-processing path) and the ability to Fetch, Decode, and Execute a 16-bit instruction in a minimum of 250-nanoseconds—the result, a system with superior bit handling capabilities. Consider!—the 250ns cycle time in conjunction with extended microcode—the result, the flexibility of bit-slice devices with the programming ease of MOS microprocessors. Now, consider the results!—a device tailored to bit-stream management in the areas of Industrial Control, Input/Output Control, and Data Communications.

The 8X300 uses three separate buses—one for 13-bit instruction addresses, one for 16-bit instructions, and a bidirectional 8-bit input/output data bus; except for the I/O bus, there are no time multiplexing of functions.

PIN CONFIGURATION

I PACKAGE



TOP VIEW

ORDER NUMBERS

N8X300I, S8X300-1, S8X300-2

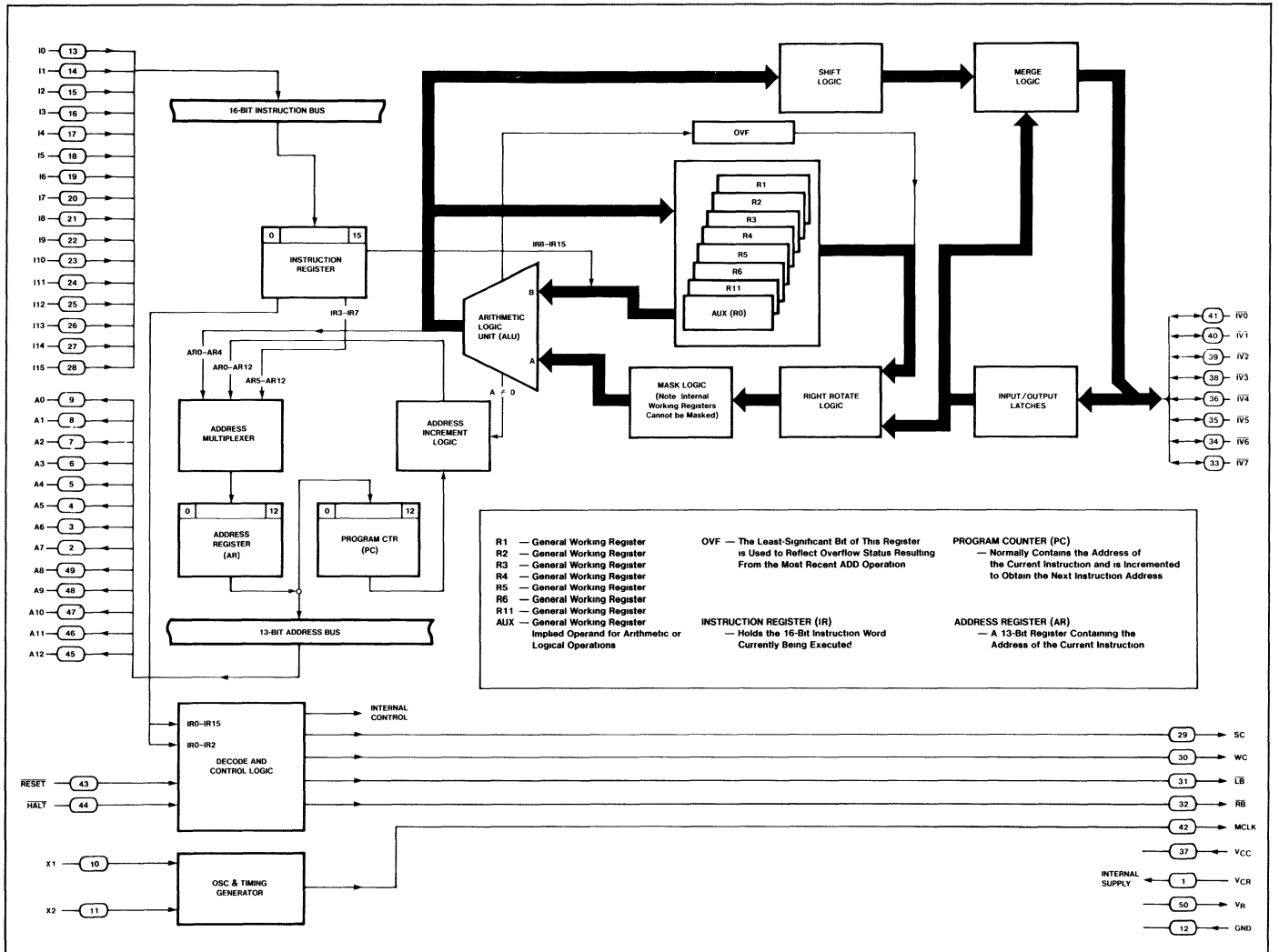
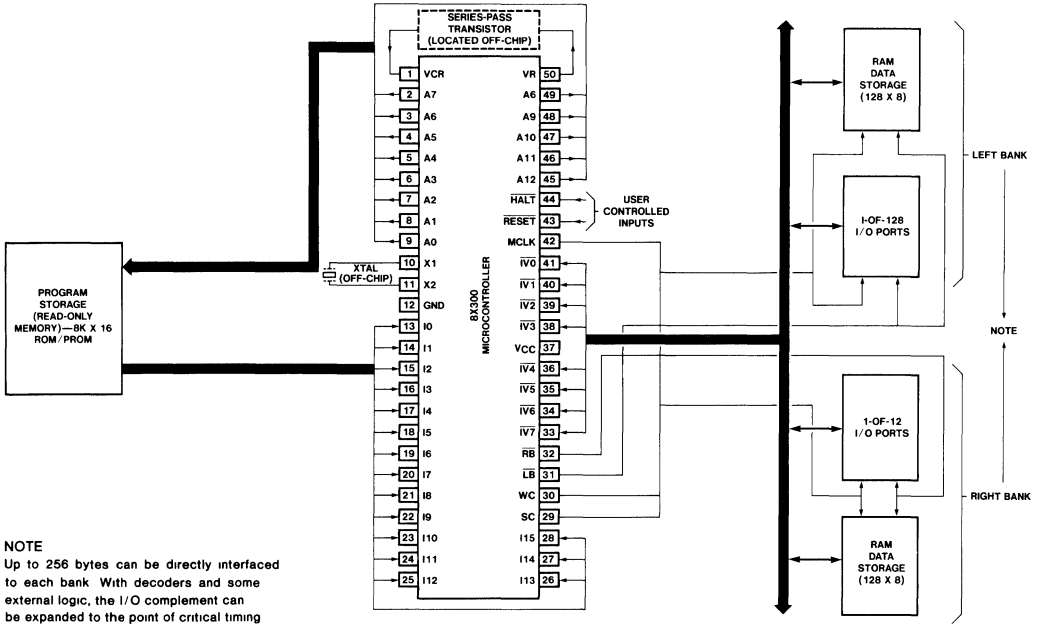


Figure 1. CPU Architecture and PIN Designations For 8X300 Microcontroller



PIN NO.	IDENTIFIER	NAME AND FUNCTION	ACTIVE STATE
2-9/45-49	A0-A12	**Program Address Lines:** These outputs permit direct addressing of up to 8192 words of program storage. A high voltage level equals a binary "1"; A12 is Least Significant Bit	High
13-28	I0-I15	**Instruction Lines:** These input lines receive 16-bit instructions from program storage. A high voltage level equals a binary "1"; I15 is Least Significant Bit.	High
33-36 38-41	$\overline{IV0}$-$\overline{IV7}$	**Input/Output Bus:** These bidirectional three-state lines communicate with up to 512 I/O devices (256 per bank). A low voltage level equals a binary "1"; $\overline{IV7}$ is Least Significant Bit	Low
10 & 11	X1 & X2	**Connections** for a capacitor, a series-resonant crystal, or an external clock source with complementary outputs. For precise frequency control, a crystal or external source is required.	—
42	MCLK	**Master Clock:** This output is used for clocking I/O devices and/or synchronization of external logic.	High
30	WC	**Write Command:** When signal is high (binary 1), data is being output on pins $\overline{IV0}$-$\overline{IV7}$ of I/O bus.	High
29	SC	**Select Command:** When signal is high (binary 1), an address is being output on pins $\overline{IV0}$-$\overline{IV7}$ of I/O bus	High
31	$\overline{LB}$	When the $\overline{LB}$ signal is low (binary 0), any one of up-to-256 I/O devices (or memory locations) in the left bank can be accessed. When the address of a particular device (or memory location) matches the address on the IV bus, that particular device (or memory location) is enabled and selected for input/output operations. All addresses on the left bank that do not match are deselected.	Low
32	$\overline{RB}$	When the $\overline{RB}$ signal is low (binary 0), any one of up-to-256 I/O devices (or memory locations) in the right bank can be accessed. When the address of a particular device (or memory location) matches the address on the I/O bus, that particular device (or memory location) is enabled and selected for input/output operations. All addresses on the right bank that do not match are deselected.	Low
43	$\overline{RESET}$	When reset input is low (binary 0), the microcontroller is initialized—sets Program Counter/Address to zero and inhibits MCLK output.	Low
44	$\overline{HALT}$	When halt input is low (binary 0), internal operation of microcontroller stops at the start of next instruction. The stop function does not inhibit MCLK or affect any internal registers.	Low
50	VR	Internally-generated reference output voltage for external series-pass transistor.	—
1	VCR	Regulated voltage input from series-pass transistor (2N5320 or equivalent).	—
12	GND	Circuit ground.	—
37	V_{CC}	Input connection for +5V power.	—

Figure 2. Typical 8X300 System with Pin Definitions

TYPICAL 8X300 SYSTEM HOOKUP

Although the system hookup shown in Figure 2 is of the simplest form, it provides a fundamental look at the 8X300 microcontroller and peripheral relationships. As indicated, program storage can be either ROM or PROM and, by using various addressing-methods/decoding-schemes, memory paging techniques can be easily implemented. Also, by proper bit assignment, some external interface logic and, under software control, the program memory can be used as a storage device for interrupt-service subroutines. The user interface ($\overline{IV0}$ through $\overline{IV7}$) is capable of addressing 256 Input/Output ports and, with the additional bank-select bit ($\overline{LB}$ and $\overline{RB}$), the number of addressable I/O ports is 512—the left bank and right bank each consisting of 256 ports. The I/O ports of each bank can be used in a variety of ways; one of these ways is shown in Figure 2. When $\overline{LB}$ is active low, the left bank can be enabled and, providing there is an address match, anyone of 128 I/O ports or anyone of 128 locations within the RAM memory can be accessed for input/output operations. When $\overline{RB}$ is active low, the same set of conditions are applicable to the right bank. With some sacrifice in speed, any given I/O port can be interfaced to a memory peripheral or other I/O device of the user.

PROGRAM STORAGE INTERFACE

As shown in Figure 2, program storage is connected to output address lines A0 through A12 (A12 = LSB) and input instruction lines I0 through I15. An address output on A0/A12 identifies one 16-bit instruction word in program storage. The instruction word is subsequently input on I0/I15 and defines the microcontroller operations which are to follow.

The Signetics 82S115 PROM or any TTL-compatible memory can be used for program storage. (Note. The worst-case access time depends upon the instruction cycle time, and also, the overall system configuration.)

I/O INTERFACE AND CONTROL

An 8-bit I/O data bus is used by the microcontroller to communicate with two fields of I/O devices. The complementary $\overline{LB}$ and $\overline{RB}$ signals identify which field of the I/O devices is enabled.

Both data and address information are output on the I/O bus. The SC (Select Command) and WC (Write Command) signals distinguish between data and address information as follows:

SC	WC	FUNCTION
High	Low	I/O address is being output on the I/O (IV) bus
Low	High	I/O data is being output on the I/O (IV) bus
Low	Low	Input data expected from selected I/O device
High	High	Invalid (not generated by 8X300)

DATA PROCESSING

From a data processing point of view, the 8X300 microcontroller chip (Figure 1) contains eight 8-bit working registers (R1 through R6, R11, AUXiliary), an arithmetic logic unit (ALU), an overflow register (OVF), rotate/shift/mask/merge logic, and a bidirectional 8-bit I/O bus. Internal 8-bit data paths connect the registers and I/O bus to the ALU inputs, and the ALU output to the registers and I/O bus. Inputs to the ALU are preceded by the data-rotate and data-mask logic and the ALU output is followed by the shift and merge logic. Any one or all of the logic functions can operate on 8-bits of data in a single instruction cycle. Data from the source register can be right-rotated (end around) before processing by the ALU; external data (I/O bus) can also be masked to isolate a portion of the 8-bit field. Since the ALU always processes 8-bits of data, bit positions not specified by the mask operation are filled with zeroes.

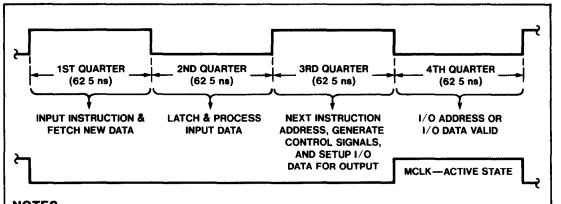
When less than 8-bits of data are specified as output to the I/O bus from the ALU, the data field (shifted and masked, as required) is merged with prior contents of the I/O latches to form the output data. Bit positions of the I/O data not affected by the logic operations are not modified. Depending upon whether an I/O peripheral or an internal register is specified in the instruction as the source of data, the I/O latches contain, respectively, I/O-bus source data or destination data. For instance, when an internal register is specified as a source of data and an I/O peripheral as the destination, data from the peripheral is read into the I/O latches at the start of the instruction cycle; processed data is then merged with contents of the I/O latches to form the I/O output data at the end of the instruction cycle. When an I/O peripheral is specified as both data source and destination, data from the source is used both as the input to the I/O latches and as data to be processed; the processed data is then merged with data from the I/O latches to form the previously-described I/O bus output. If the data source and destination are on opposite banks of the 8X300 bus, the destination data is written with a full 8-bits, since the prior contents were not stored in the I/O latches.

INSTRUCTION CYCLE

Each microcontroller operation is executed in a single instruction cycle. The instruction cycle is divided into quarters with each quarter cycle being as short as 62.5-nanoseconds. Figure 3 shows the general functions that occur during each quarter cycle; specifics regarding minimum/maximum timing and other critical values are described under "Design Parameters" in this data sheet. During the first quarter cycle, a new instruction from program storage is input on signal lines I0 through I15; simultaneously, new data is fetched via the input/output bus ($\overline{IV0}$ through $\overline{IV7}$). At the end of the first quarter cycle, the new instruction is latched in the instruction register and the new I/O data is present at the input of the chip but is not, as yet, latched by the IV latches.

In the second quarter cycle, the I/O data stabilizes and preliminary processing is completed; at the end of this quarter, the IV latches are closed and final processing can be accomplished. During the third quarter cycle, the address for the next instruction is output to the I/O (IV) bus, control signals are generated, and I/O data is setup for the output

phase. During the fourth quarter cycle, a master clock signal (MCLK) generated by the 8X300 is used to latch valid address or data into peripheral devices connected to the IV bus; MCLK is also used to synchronize any external logic with timing circuits of the 8X300. To summarize the action, the first half of the instruction cycle deals primarily with input functions and the second half is mostly concerned with output functions.



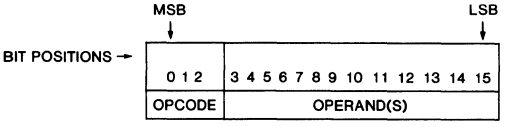
NOTES
1 New instruction must be accepted and latched at end of first quarter cycle
2 The I/O data latches are open for the first two quarter cycles, that is, for 125-nanoseconds
3 The address is output during third quarter cycle
4 I/O bus drivers are active (turned on) during third and fourth quarter cycles

Figure 3. Instruction Cycle and MCLK with: Crystal = 8MHz and Cycle Time = 250 ns

INSTRUCTION SET

General Format and Basic Operations

The 16-bit instruction word (I0 through 15) from program storage is input to the instruction register (Figure 1) and is subsequently decoded to implement the events to occur during the current instruction cycle. The instruction word is formatted as follows:



Rather than discrete instructions, the three operation code (OP CODE) bits specify eight instruction classes. Each instruction class is subject to a number of powerful variations; these variations are specified by the thirteen operand bits. General areas of control for the eight instruction classes are:

- Arithmetic and Logic Operations (ADD, AND, AND XOR)
- Movement of Data and Constants (MOVE and XMIT)
- Branch or Test (JMP, NZT, and XEC)

Basic operations for each of the eight instruction classes are as follows; a summary of the instruction set is provided in Table 1.

MOVE—data in source register or I/O-bus input is moved to destination register or I/O-bus output. Data can be shifted any number of places and/or masked to any length.

ADD—data in source register or I/O-but input is added to content of AUX (R0) register and the result is placed in the destination register or I/O-bus output. Data can be shifted and/or masked, as required.

Table 1. SUMMARY OF 8X300 INSTRUCTION SET

INSTRUC CLASS	OPCODE	FORMATS	DESCRIPTION	I/O CONT SIG	STATE OF CONTROL SIGNAL DURING INSTRUCTION CYCLE: INPUT PHASE (INSTRUCTION INPUT & DATA PROCESSING)	STATE OF CONTROL SIGNAL DURING INSTRUCTION CYCLE: OUTPUT PHASE (ADDRESS & I/O BUS)
MOVE	0	**F1: Register to Register** 0 1 2 | 3 4 5 6 7 | 8 9 10 | 11 12 13 14 15 OPCODE | S | R | D Invalid values of "S" 07_8, 17_8, 20_8-37_8 Invalid values of "D" 10_8, 20_8-37_8	(S) → D Move content of internal register specified by S-field to internal register specified by D-field Prior to the "MOVE" operation, right-rotate contents of internal source register by octal value (0 through 7) defined by the R-field	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L X X	H if "D" = 07_8, 17_8 L H if "D" = 17_8 L if "D" = 07_8
		F2: I/O Bus to Register 0 1 2 | 3 4 5 6 7 | 8 9 10 | 11 12 13 14 15 OPCODE | S | L | D Valid values of "S" 20_8-37_8 Invalid values of "D" 10_8, 20_8-37_8	Move right-rotated I/O bus (source) data specified by the S-field to internal register specified by the D-field The L-field specifies the length of source data starting from the LSB-position and, if less than 8-bits, the remaining bits are filled with zeroes	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L L if "S" = 20_8-27_8 H if "S" = 30_8-37_8	H if "D" = 07_8, 17_8 L H if "D" = 17_8 L if "D" = 07_8
		F2: Register to I/O Bus 0 1 2 3 | 4 5 6 7 | 8 9 10 | 11 12 13 14 15 OPCODE | S | L | D Invalid values of "S" 07_8, 17_8, 20_8, 37_8 Valid values of "D" 20_8-37_8	Move contents of internal register specified by the S-field to the I/O latches Before outputting on I/O bus, data is shifted as specified by the least significant octal digit of the D-field and the bits specified by the L-field are merged with the latched I/O data	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L L if "D" = 20_8-27_8 H if "D" = 30_8-37_8	L H L if "D" = 20_8-27_8 H if "D" = 30_8-37_8
		F2: I/O Bus to I/O Bus 0 1 2 | 3 4 5 6 7 | 8 9 10 | 11 12 13 14 15 OPCODE | S | L | D Valid values of "S" 20_8-37_8 Valid values of "D" 20_8-37_8	Move right rotated I/O-bus (source) data specified by the S-field to the I/O latches Before outputting on I/O bus, shift data as specified by the D-field, then merge source and latched I/O data as specified by the L (length) field	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L L if "D" = 20_8-27_8 H if "D" =30_8-37_8	L H L if "D" = 20_8-27_8 H if "D" = 30_8-37_8

Table 1. SUMMARY OF 8X300 INSTRUCTION SET (Continued)

INSTRUC CLASS	OPCODE	FORMATS	DESCRIPTION	I/O CONT SIG	STATE OF CONTROL SIGNAL DURING INSTRUCTION CYCLE: INPUT PHASE (INSTRUCTION INPUT & DATA PROCESSING)	STATE OF CONTROL SIGNAL DURING INSTRUCTION CYCLE: OUTPUT PHASE (ADDRESS & I/O BUS)
ADD	1	Same as MOVE instruction class	(S) plus (AUX) → D Same as MOVE instruction class except that contents of AUX (R0) register are ADDed to the source data If there is a "carry" from MSB, then OVF (overflow) = 1, otherwise OVF = 0	Same as MOVE instruction class		
AND	2	Same as MOVE instruction class	(S) ∧ (AUX) → D Same as MOVE instruction class except that contents of AUX (R0) register are ANDed with source data	Same as MOVE instruction class		
XOR	3	Same as MOVE instruction class	(S) ⊕ (AUX) → D Same as MOVE instruction class except that contents of AUX (R0) register are exclusively ORed with source data	Same as MOVE instruction class		
XEC	4	**F3: Register Immediate** 0 1 2 | 3 4 5 6 7 | 8 9 10 11 12 13 14 15 OPCODE | S | J Invalid values of "S": 07_8, 17_8, 20_8-37_8 Valid values of "J". 000_8-377_8	**Execute instruction at current page address offset by J (literal) + (S). Return to normal instruction flow unless a branch is encountered.** Execute instruction at an address determined by replacing the low-order 8-bits of the Program Counter with the following derived sum • Value of literal (J-field) plus • Contents of internal register specified by S-field The PC is not incremented and the overflow status (OVF) is not changed	SC = WC = $\overline{LB}$ =	L L X	L L X
		F4: I/O Bus Immediate 0 1 2 | 3 4 5 6 7 | 8 9 10 | 11 12 13 14 15 OPCODE | S | L | J Valid values of "S" 20_8-37_8 Valid values of "J": 00_8-37_8	Execute instruction at an address determined by replacing the low-order 5-bits of Program Counter with the following derived sum • 5-bit value of literal (J-field) plus • Value of rotated source data specified by S-field (The L-field specifies the length of source data starting from the LSB-position and, if less than 8-bits, the remaining bits are filled with zeros, the Program Counter is not incremented and the overflow status (OVF) is not changed)	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L L if "S" = 20_8-27_8 H if "S" = 30_8-37_8	L L X X
NZT	5	**F3: Register Immediate** 0 1 2 | 3 4 5 6 7 | 8 9 10 11 12 13 14 15 OPCODE | S | J Invalid values of "S" 07_8, 17_8, 20_8-37_8 Valid values of "J" 000_8-377_8	**If data specified by the S-field is not equal to zero, jump to current page address offset by value of J-field; otherwise, increment the Program Counter.** If contents of internal register specified by S-field is **non-zero**, transfer to address determined by replacing the low-order 8-bits of Program Counter with "J", otherwise, increment PC	SC = WC = $\overline{LB}$ =	L L X	L L X
		F4: I/O Bus Immediate 0 1 2 | 3 4 5 6 7 | 8 9 10 | 11 12 13 14 15 OPCODE | S | L | J Valid values of "S" 20_8-37_8 Valid values of "J" 00_8-37_8	If right-rotated I/O bus data is **non-zero**, transfer to address determined by replacing low-order 5-bits of Program Counter with "J", otherwise, increment PC (The L-field specifies the length of source I/O data starting from the LSB-position and, if less than 8-bits, the remaining bits are filled with zeroes)	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L L if "S" = 20_8-27_8 H if "S" = 30_8-37_8	L L X X
XMIT	6	**F3: Register Immediate** 0 1 2 | 3 4 5 6 7 | 8 9 10 11 12 13 14 15 OPCODE | D | J Invalid values of "D" 10_8, 20_8-37_8 Valid values of "J" 000_8-377_8	Transmit J → D Transmit and store 8-bit binary pattern in J-field to internal register specified by D-field	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L X X	H if D = 07_8 or 17_8 L H if D = 17_8 L if D = 07_8
		F4: I/O Bus Immediate 0 1 2 | 3 4 5 6 7 | 8 9 10 | 11 12 13 14 15 OPCODE | D | L | J Valid values of "D" 20_8-37_8 Valid values of "J" 00_8-37_8	Transmit binary pattern in J-field to I/O bus Before putting data on I/O bus, shift literal value "J" as specified by the D-field and merge bits specified by the L-field with existing I/O bus data If the L-field specifies more than 5-bits starting from the LSB-position, all remaining bits are set to zero	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L L if D = 20_8-27_8 H if D = 30_8-37_8	L H L if D = 20_8-27_8 H is D = 30_8-37_8
JMP	7	**F5: Address Immediate** 0 1 2 | 3 4 5 6 7 8 9 10 11 12 13 14 15 OPCODE | A Valid values of A 00000_8-17777_8	Jump to address in program storage specified by A-field, this address is loaded into the Address Register and the Program Counter	SC = WC = $\overline{LB}$ =	L L X	L L X

NOTES * $\overline{RB}$ is complement of $\overline{LB}$, X = Undefined

AND—data in source register or I/O-bus input is ANDed with content of AUX (R0) register and the result is placed in the destination register or I/O-bus output. Data can be shifted and/or masked, as required.

XOR—data in source register or I/O-bus input is exclusively ORed with contents of AUX (R0) register and the result is placed in the destination register or I/O-bus output. Data can be shifted and/or masked, as required.

XMIT—immediate data field of instruction word replaces data in destination register or I/O-bus output.

XEC—executes instruction at the program address which is formed by replacing the least significant bits of the last address with the sum of:

- Literal (J) field value of instruction plus,
- Value of data in source register or I/O-bus input.

NZT—least significant bits of program address are replaced by literal (J) field of instruction if the source register or I/O-bus is not equal to zero.

JMP—program address is replaced by address field of the instruction word.

Instruction Fields

As shown in Table 1, each instruction contains an operations code (OPCODE) field and from one-to-three operand fields. The operand fields are: Source (S), Destination (D), Rotate/Length (R/L), Literal (J), and Address (A). The OPCODE and operand fields are briefly described in the following paragraphs.

Operations Code Field: The three-bit OPCODE field specifies one of eight classes of 8X300 instructions; octal designations for this field and operands for each instruction class are shown in Table 1.

Source (S) and Destination (D) Fields: The five-bit (S) and (D) fields specify the source and destination of data for the operation defined by the OPCODE field. The AUXiliary (R0) register is an implied second operand for the ADD, AND, and XOR instructions, each of which require two source fields. That is, instructions of the form:

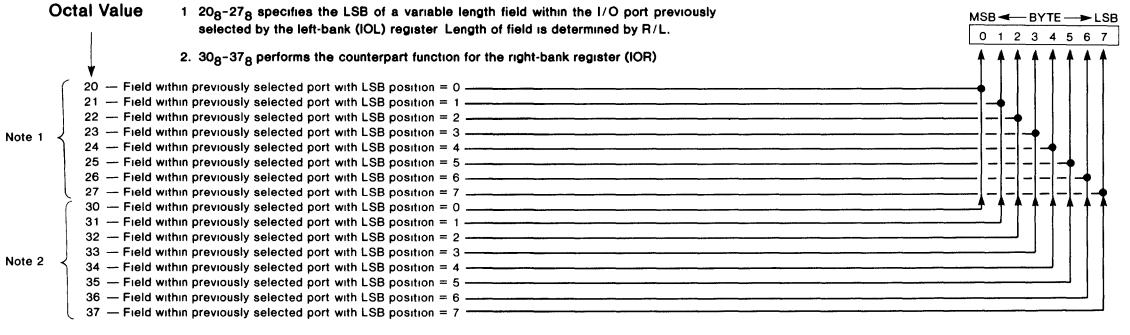
ADD X, Y

imply a third operand, say Z, located in the AUX (R0) register. Thus, the operation for the preceding expression is actually (X + Z), with the result stored in Y. The (S) and/or (D) fields can specify an internal 8X300 register or any one-to-eight bit I/O field; octal values for these registers and Source/Destination field assignments are provided in Table 2.

Table 2. OCTAL ADDRESSES OF 8X300 REGISTERS AND ADDRESS/BIT ASSIGNMENTS OF SOURCE/DESTINATION FIELDS

Octal Value	8X300 Register	Octal Value	8X300 Register
00	Auxiliary (R0)	10	OVF (Overflow Register)—used only as a source
01	R1	11	R11
02	R2	12	Unassigned
03	R3	13	Unassigned
04	R4	14	Unassigned
05	R5	15	Unassigned
06	R6	16	Unassigned
07	*IOL Register—Left Bank I/O Address Register; Used only as destination	17	*IOR Register—Right Bank I/O Address Register; Used only as destination

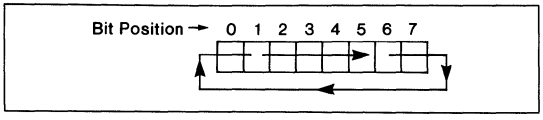
NOTE
*If IOL or IOR is specified as a source of data, the source data is all zeroes



Rotate (R) and Length (L) Field: The three-bit R/L field performs one of two functions, specifying either the field length (L) or a right-rotate (R). For a given instruction, the specified function depends upon the contents of the source (S) and destination (D) fields.

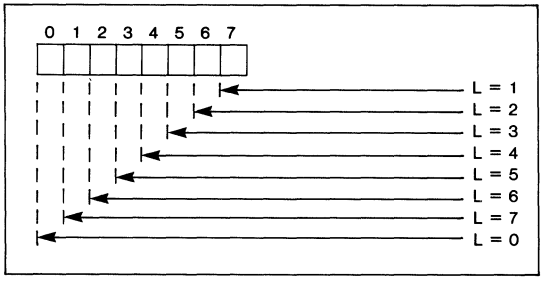
- When an internal register is specified by both the source and destination fields, the (R) field is invoked and it specifies a right-rotate of the data specified in the (S) field—see accompanying diagram. The source-register data (up to eight-bits) is right-rotated within one instruction cycle. (The right-rotate function is implemented on the bus and not in the source register.)

RIGHT-ROTATE FUNCTION



- When either or both of the source and destination fields specify a variable-length I/O data field, the (L) field specifies the length of the I/O data field—see accompanying diagram. If the source field specifies an I/O address (20_8-37_8) and the destination field specifies an internal register (00_8-06_8, 07_8, 11_8, or 17_8), the L-field specifies the length of source data; the source data is formed by right-rotating the I/O bus data according to the source address (Table 2) and then masking result as specified by L-field. If length is less than eight-bits, all remaining bits are set to zero prior to processing data in the ALU. If the source field specifies an internal register (00_8,-06_8, 10_8,or 11_8) and the destination field specifies I/O bus data (20_8-37_8), the L field specifies the length of the destination data. To form the destination data, the ALU output is left-shifted according to the destination address (Table 2) and then masked to the required length—see DATA LENGTH SPECIFICATION. The destination data is merged with data in the I/O latches to finalize the I/O bus data. Hence, a one-to-eight bit destination data field can be inserted into the existing eight-bit I/O port without modifying surrounding bits. If both the source and destination fields specify I/O bus data (20_8-37_8), the L-field specifies the length of both the source and destination data.

DATA LENGTH SPECIFICATION



To form the source data, the I/O bus data is right-rotated according to the source address (Table 2) and then masked to the required length—see preceding DATA LENGTH SPECIFICATION. If length is less than eight-bits, all remaining bits are set to zero before processing in the ALU. To form the destination data, the ALU output is left-shifted according to the destination address (Table 2) and masked to the required length specification. The destination data is then merged into the I/O bus data that was used to obtain the source; thus, if the source and destination addresses are on the same bank, the I/O bus data written to the destination register appears unmodified, except for bits changed during the shift-and-mask operations. If the source and destination addresses refer to different banks, the destination register is changed to contain the contents of the source register in those bit positions not affected by the destination data.

J-Field: The 5-bit or 8-bit (J) field is used to load a literal value (contained in the instruction) into a register, into a variable I/O data field, or to modify the low-order bits of the Program Counter. The bit-length of the (J) field is implied by the (S) field in the XEC, NZT, and XMIT instructions, based on the following considerations.

- When the source (S) field specifies an internal register, the literal value of the J-field is an 8-bit binary number.
- When the source (S) field specifies a variable I/O data field, the literal value of the J-field is a 5-bit binary number.

A-Field: The 13-bit (A) field is an address field which allows the 8X300 to directly address up 8192 locations in Program Storage memory.

INSTRUCTION SEQUENCE CONTROL

Formation of Instruction Address

The Address Register and Program Counter are used to generate addresses for accessing an instruction from program storage. The instruction address is formed in any one of four ways:

- For all except the JMP, XEC, and a "satisfied" NZT instruction, the Program Counter is incremented by one and placed in the Address Register.
- For the JMP instruction, the 13-bit A-field contained in the JMP instruction word replaces the contents of both the Address Register and Program Counter.
- For the XEC instruction, the Address Register is loaded with the high-order bits of the Program Counter modified as follows:
  XEC using I/O Bus Data: low order 5-bits of ALU output replaces counterpart bits in Address Register.
  XEC using Data from Internal Register: low order 8-bits of ALU output replaces counterpart bits in Address Register.
  The Program Counter is not modified for either of the above conditions.
- For a "satisfied" NZT instruction, the low order 5-bits (NZT source is I/O Bus Data) or low order 8/bits (NZT source is an Internal Register) of both the Address Register and Program Counter are loaded with the literal value specified by J-field of the instruction word.

Data Addressing

The source and/or destination addresses of the data to be operated upon are specified as part of the instruction word. As shown in Table 3, source/destination addresses are specified using a five-bit address (00_8 through 37_8). When the most significant octal digit is a 0 or 1, the source and/or destination address is an internal register; if the most significant digit is a 2 or 3, an I/O bus address is indicated—2 specifying a left-bank (LB) address and 3 specifying a right-bank (RB) address. The least significant octal digit (0 through 7) indicates either a specific internal register address or positioning information for the least significant bit when specifying I/O bus data. Referring to Table 1, the AUXiliary register (00) is the implied source of the second argument for the ADD, AND, and XOR operations. IOL (destination address 07_8) and IVR (destination address 17_8) provide a means of routing address information to I/O registers. With IOL or IOR specified as the destination address, the data is placed on the I/O bus during the output phase of the instruction cycle. Simultaneously, a select command (SC) is generated to inform all I/O devices that information on the I/O bus is to be considered as an I/O address. Since IOL and IOR are not harware registers, they should never be specified as a source address.

Control outputs $\overline{LB}$ and $\overline{RB}$ are used to partition I/O bus devices into two fields of 256 addresses. With LB in the active-low state and a source address of 20_8-27_8, the left bank of I/O devices are enabled during the input phase of the instruction cycle. With $\overline{RB}$ in the active-low state and a source address of 30_8-37_8, the right bank of devices are enabled. During the output phase, $\overline{RB}$ is low if the destination address is IOR (17_8) or 30_8-37_8; $\overline{LB}$ is low if the destination address is IOL (07_8) or 20_8-27_8. Each address field ($\overline{LB}$ and $\overline{RB}$) can have a different I/O device selected; thus, two devices can be directly accessed within one instruction cycle.

Table 3. SOURCE/DESTINATION ADDRESSES

SOURCE AND/OR DESTINATION FIELD (OCTAL)	SOURCE/DESTINATION
00	AUXiliary register (R0)
01-06	Working registers R1-R6, respectively
07	IOL Left-bank enable (Destination only)
10	Overflow status—OVF (Source only)
11	Working register R11
17	IOR Right-bank enable (Destination only)
2N (N = 0, 1, 2, 3 4, 5, 6, or 7)	If a source, I/O data is right-rotated (7 − N) bits and then masked as specified by the L-field. $\overline{LB}$ = low and $\overline{RB}$ = high generated during input phase. If a destination, I/O data is left-shift (7 − N) bits and merged (specified by L-field) with data contained in the I/O latches. $\overline{LB}$ = low and $\overline{RB}$ = high generated during output phase.
3N (N = 0, 1, 2, 3, 4, 5, 6, or 7)	If a source, I/O data is right-rotated (7 − N) bits and then masked as specified by the L-field. $\overline{LB}$ = high and $\overline{RB}$ = low generated during input phase. If a destination, I/O data is left-shifted (7 − N) bits and merged (specified by L-field) with data contained in the I/O latches. $\overline{LB}$ = high and $\overline{RB}$ = low generated during output phase.

DESIGN PARAMETERS

Hardware design of an 8X300-based system largely consists of the following operations:

- **Selecting and interfacing a Program Storage device—ROM, PROM, etc. (Pins 2 through 9 and 45 through 49 for 13-bit address interface; Pins 13 through 28 for 16-bit instruction interface.)**
- **Selecting and interfacing Input/Output devices—RAM, Multiplexers, I/O Ports, and other eight-bit addressable I/O devices. (Pins 33 through 36 and pins 38 through 41 for eight-bit I/O interface.)**
- **Choosing and implementing System Clock—Capacitor-Controlled, Crystal-Controlled, or Externally-Driven. (Pins 10 and 11 for System Clock interface.)**
- **Selection of 5-volt power supply and off-chip series-pass transistor.**
- **External logic, as required, to meet the control requirements of a particular application.**

All information required for easy implementation of these design requirements is provided under the following captions.

- **DC Characteristics**
- **AC Characteristics**
- **Timing Considerations**
- **Clock Considerations**
- **HALT/RESET Logic**
- **Voltage Regulator**

DC CHARACTERISTICS (Commercial Part) $4.75V \leq V_{CC} \leq 5.25V$, $0°C \leq T_A \leq 70°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT	COMMENTS
			Min	Typ	Max		
V_{CC}	Supply voltage		475	5.0	5.25	V	5V ± 5%; pin 37 only
V_{IH}	High level input voltage		0.6 2.0		2.0	V	X1 and X2 All other pins
V_{IL}	Low level input voltage				0.4 0.8	V	X1 and X2 All other pins
V_{OH}	High level output voltage	V_{CC} = min; I_{OH} = −3mA	2.4	3.0		V	
V_{OL}	Low level output voltage	V_{CC} = min; I_{OL} = 6mA V_{CC} = min; I_{OL} = 16mA		0.39 0.39	0.55 0.55	V	A0 through A12 All other outputs
V_{CR}	Regulator voltage	V_{CC} = 5V		3.1		V	From series-pass transistor
V_{IC}	Input clamp voltage	V_{CC} = min; I_{IN} = −10mA			−1.5	V	Crystal inputs X1 and X2 do not have internal clamp diodes.
I_{IH}	High-level input current	V_{CC} = max; V_{IH} = 0.6V V_{IH} = 4.5V		1	3.0 50	mA μA	X1 and X2 All other pins
I_{IL}	Low-level input current	V_{CC} = max; V_{IL} = 0.4V		 −0.13 −0.67 −0.23	−3 −0.2 −1.6 −0.4	mA	X1 and X2 $\overline{IV0}$-$\overline{IV7}$ I0-I15 $\overline{HALT}$ and $\overline{RESET}$
I_{OS}	Short circuit output current	V_{CC} = max; V_{CR} = V_{CRH} (Note: At any time, no more than one output should be connected to ground.)	−30		−140	mA	All output pins
I_{CC}	Supply current	V_{CC} = max; V_{CR} = V_{CRH}			160	mA	
I_{REG}	Regulator control	V_{CC} = 5.0V	−14		−21	mA	
I_{CR}	Regulator current	V_{CC} = max			230	mA	70°C
					265	mA	25°C
					290	mA	0°C

NOTES
1 Operating temperature ranges are guaranteed after thermal equilibrium has been reached
2 All voltages measured with respect to ground terminal

AC CHARACTERISTICS (Commercial Part)

CONDITIONS: V_{CC} = 5V (±5%), V_{IN} = 0V or 3V, $0°C \leq T_A \leq 70°C$
LOADING: (See test circuits)

PARAMETER (NOTE 1)		LIMITS (INSTRUCTION CYCLE TIME = 250 ns)			LIMITS (INSTRUCTION CYCLE TIME > 250 ns)			UNITS	COMMENTS
		Min	Typ	Max	Min	Typ	Max		
T_{PC}	Processor cycle time	250			250			ns	
T_{CP}	X1 clock period	125			125			ns	
T_{CH}	X1 clock high time	62			62			ns	
T_{CL}	X1 clock low time	62			62			ns	
T_{MCH}	MCLK high delay	31	42	52	31	42	52	ns	
T_{MCL}	MCLK low delay	31	42	52	31	42	52	ns	
T_W	MCLK pulse width	55	62	69	T_{4Q}−7	T_{4Q}		ns	Note 2
T_{AS}	X1 falling edge to address stable	50	63	80	50	63	80	ns	Note 7

AC CHARACTERISTICS (Commercial Part) (Continued) **CONDITIONS:** V_{CC} = 5V (±5%), V_{IN} = 0V or 3V, 0°C ≤ T_A ≤ 70°C
LOADING: (See test circuits)

PARAMETER (NOTE 1)		LIMITS (INSTRUCTION CYCLE TIME = 250 ns)			LIMITS (INSTRUCTION CYCLE TIME > 250 ns)			UNITS	COMMENTS
		Min	Typ	Max	Min	Typ	Max		
T_{MAS}	MCLK falling edge to address stable	130	143	160	$T_{1Q}+T_{2Q}$ +5	$T_{1Q}+T_{2Q}$ +18	$T_{1Q}+T_{2Q}$ +35	ns	Notes 2, 3, & 7
T_{IA}	Instruction to address			170			T_{2Q}+108	ns	Notes 2, 3, & 8
T_{IVA}	Input data to address			105			105	ns	Notes 3 & 9
T_{IS}	Instruction set-up time (X1 rising edge)	−7			−7			ns	Note 10
T_{MIS}	MCLK falling edge to instruction stable			20			T_{1Q}−42	ns	Notes 2, 4, & 10
T_{IH}	Instruction hold time (X1 rising edge)	45			45			ns	Note 11
T_{MIH}	Instruction hold time) (MCLK falling edge)	60			T_{1Q}−2			ns	Notes 2 & 11
T_{WH}	X1 falling edge to SC/WC rising edge	40	49	58	40	49	58	ns	
T_{MWH}	MCLK falling edge to SC/WC rising edge	125	130	135	$T_{1Q}+T_{2Q}$	$T_{1Q}+T_{2Q}$ +5	$T_{1Q}+T_{2Q}$ +10	ns ns	Note 2
T_{WL}	X1 falling edge to SC/WC falling edge	40	49	58	40	49	58	ns	
T_{MWL}	MCLK falling edge to SC/WC falling edge	5	7	15	5	7	15	ns	
T_{IBS}	X1 falling edge to $\overline{LB}/\overline{RB}$ (Input phase)	48	60	70	48	60	70	ns	
T_{MIBS}	MCLK falling edge to $\overline{LB}/\overline{RB}$ (Input phase)	7	17	25	7	17	25	ns	
T_{IIBS}	Instruction to $\overline{LB}/\overline{RB}$ (Input phase)		27	35		27	35	ns	
T_{OBS}	X1 falling edge to $\overline{LB}/\overline{RB}$ (Output phase)	48	60	70	48	60	70	ns	
T_{MOBS}	MCLK falling edge to $\overline{LB}/\overline{RB}$ (Output phase)	132	137	147	$T_{1Q}+T_{2Q}$ +7	$T_{1Q}+T_{2Q}$ +12	$T_{1Q}+T_{2Q}$ +22	ns	Note 2
T_{IDS}	Input data set-up time (X1 falling edge)	25	16		25	16		ns	
T_{MIDS}	MCLK falling edge to input data stable		65	55		$T_{1Q}+T_{2Q}$ −60	$T_{1Q}+T_{2Q}$ −70	ns	Notes 2 & 5
T_{IDH}	Input data hold time (X1 falling edge)	40	30		40	30		ns	
T_{MDIH}	Input data hold time (MCLK falling edge)	125	112		$T_{1Q}+T_{2Q}$	$T_{1Q}+T_{2Q}$ −13		ns	Note 2
T_{ODH}	Output data hold time (X1 falling edge)	55	65	75	55	65	75	ns	
T_{MODH}	Output data hold time (MCLK falling edge)	11	20	25	11	20	25	ns	
T_{ODS}	Output data stable (X1 falling edge)	74	84	94	74	84	94	ns	Notes 12, 14, & 15
T_{MODS}	Output data stable (MCLK falling edge)	150	160	170	$T_{1Q}+T_{2Q}$ +25	$T_{1Q}+T_{2Q}$ +35	$T_{1Q}+T_{2Q}$ +45	ns	Notes 2, 12, 14, & 15

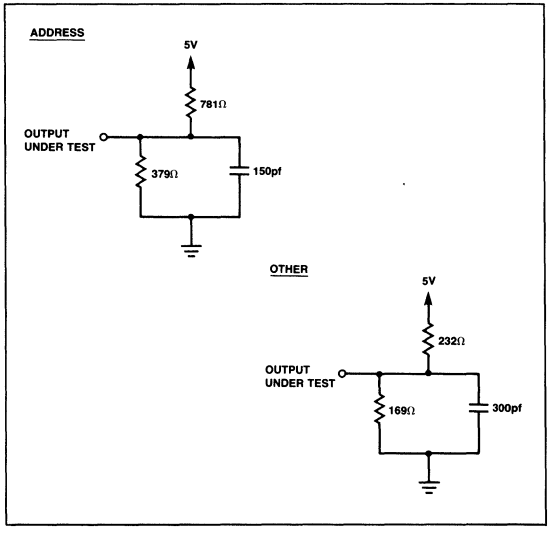
AC CHARACTERISTICS (Commercial Part) (Continued)

CONDITIONS: V_{CC} = 5V (±5%), V_{IN} = 0V or 3V, 0°C ≤ T_A ≤ 70°C
LOADING: (See test circuits)

PARAMETER (NOTE 1)		LIMITS (INSTRUCTION CYCLE TIME = 250 ns)			LIMITS (INSTRUCTION CYCLE TIME > 250 ns)			UNITS	COMMENTS
		Min	Typ	Max	Min	Typ	Max		
T_{DD}	Input data to output data	104	120	136	104	120	136	ns	Notes 13 & 15
T_{HS}	$\overline{HALT}$ set-up time (X1 rising edge)	0			0			ns	
T_{MHS}	MCLK falling edge to $\overline{HALT}$ falling edge			18			$T_{1Q}-44$	ns	Notes 2 & 6
T_{HH}	$\overline{HALT}$ hold time (X1 rising edge)	32			32			ns	
T_{MHH}	$\overline{HALT}$ hold time (MCLK falling edge)	50			$T_{1Q}-12$			ns	Note 2
T_{ACC}	Program storage access time			80				ns	
T_{IO}	I/O port output enable time ($\overline{LB}/\overline{RB}$ to valid IV data input)			30				ns	

NOTES:
1. X1 and X2 inputs are driven by an external pulse generator with an amplitude of 1.5 volts; all timing parameters are measured at this voltage level.
2. Respectively, T_{1Q}, T_{2Q}, T_{3Q}, and T_{4Q} represent time intervals for the first, second, third, and fourth quarter cycles.
3. Capacitive loading for the address bus is 150 picofarads.
4. Same as TIS but referenced to falling edge of MCLK.
5. Same as TIDS but referenced to falling edge of MCLK.
6. Same as THS but referenced to falling edge of MCLK
7. TAS is obtained by forcing a valid instruction and an I/O bus input to occur earlier than the specified minimum set-up time; the TAS parameter then represents the earliest time that the address bus is valid
8. TIA is obtained by forcing a valid instruction input to occur earlier than the minimum set-up time.
9. TIVA is obtained by forcing a valid I/O bus input to just meet the minimum set-up time.
10. TMIS represents the set-up time required by internal latches of the 8X300. In system applications, the instruction input may have to be valid before the worst-case set-up time in order for the system to respond with a valid I/O bus input that meets the I/O bus input set-up time (TIDS and TMIDS).
11. TIH represents the hold time required by internal latches of the 8X300 To generate proper LB/RB signals, the instruction must be held valid until the address bus changes.
12. TODS is obtained by forcing a valid I/O bus input to occur earlier than the I/O bus input set-up time (TIDS); this timing parameter represents the earliest time that the I/O output data can be valid.
13. TDD is obtained by forcing a valid I/O bus input to just meet the minimum I/O bus input set-up time; thus timing parameter represents the latest time that the I/O output data can be valid.
14. The minimum figure for these parameters represents the earliest time that I/O bus output drivers of the 8X300 will turn on.
15. For TIDS ≥ 35 ns, TODS or TMODS should be used to determine when the output data is stable.

TEST CIRCUITS



DC CHARACTERISTICS (Military Part)

S8X300-1 $-40°C \leq TC \leq 100°C$ $V_{CC} = 5V \pm 5\%$
S8X300-2 $-20°C \leq TC \leq 100°C$ $V_{CC} = 5V \pm 10\%$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IH}	High level input voltage X1, X2 All others		 0.6 2.0			 V V
V_{IL}	Low level input voltage X1, X2 All others				 0.4 0.8	 V V
V_{IC}	Input clamp voltage (Notes 1 & 5)	V_{CC} = min $I_I = -10mA$			-1.5	V
I_{IH}	High level input current X1, X2 All others	 V_{CC} = max V_{IH} = 0.6V V_{CC} = max V_{IH} = 4.5V			 3.0 0.05	 mA
I_{IL}	Low level input current X1, X2	 V_{CC} = max V_{IL} = 0.4V			 -3.0	 mA
	$\overline{IV0}$-$\overline{IV7}$	V_{CC} = max V_{IL} = 0.4V			-0.3	mA
	I0-I15	V_{CC} = max V_{IL} = 0.4V			-1.6	mA
	$\overline{HALT}$, $\overline{RESET}$	V_{CC} = max V_{IL} = 0.4V			-0.4	mA
V_{OL}	Low level output voltage A0-A12 All others	 V_{CC} = min I_L = 4.25mA V_{CC} = min I_{OL} = 16mA			 0.55 0.55	 V V
V_{OH}	High level output voltage	V_{CC} = min $I_{OH} = -3mA$	2.4			V
I_{OS}	Short circuit output current (Note 2)	V_{CC} = max	-30		-140	mA
I_{CC}	Supply current (Note 4)	V_{CC} = max			160	mA
I_{REG}	Regulator control	V_{CC} = 5.0V	-14		-21	mA
I_{CR}	Regulator current	V_{CC} = max			285	mA
I_{CR}	Regulator current	$TC \geq 25°C$ V_{CC} = max			330	mA
V_{CR}	Regulator voltage	$TC < 25°C$ (Note 3)		3.1		V

NOTES
1 Crystal inputs X1 and X2 do not have clamp diodes
2 Only one output may be grounded at a time
3 From series-passed transistor under the following conditions
VCC = Max, HALT = RESET = ADDRESS = IVX = 0 0V, all other pins open.
4 Pin 37 only
5 Test each input one at a time
6 All voltages are with respect to ground terminal
7 The operating temperature ranges are guaranteed after thermal equilibrium has been reached
8. Storage temperature $-65°C$ to $+150°C$

AC CHARACTERISTICS (Military Part)

CONDITIONS: S8X300-1—V_{CC} = 5V (±5%) -40°C ≤ T_C ≤ 100°C
S8X300-2—V_{CC} = 5V (±10%) -20°C ≤ T_C ≤ 100°C

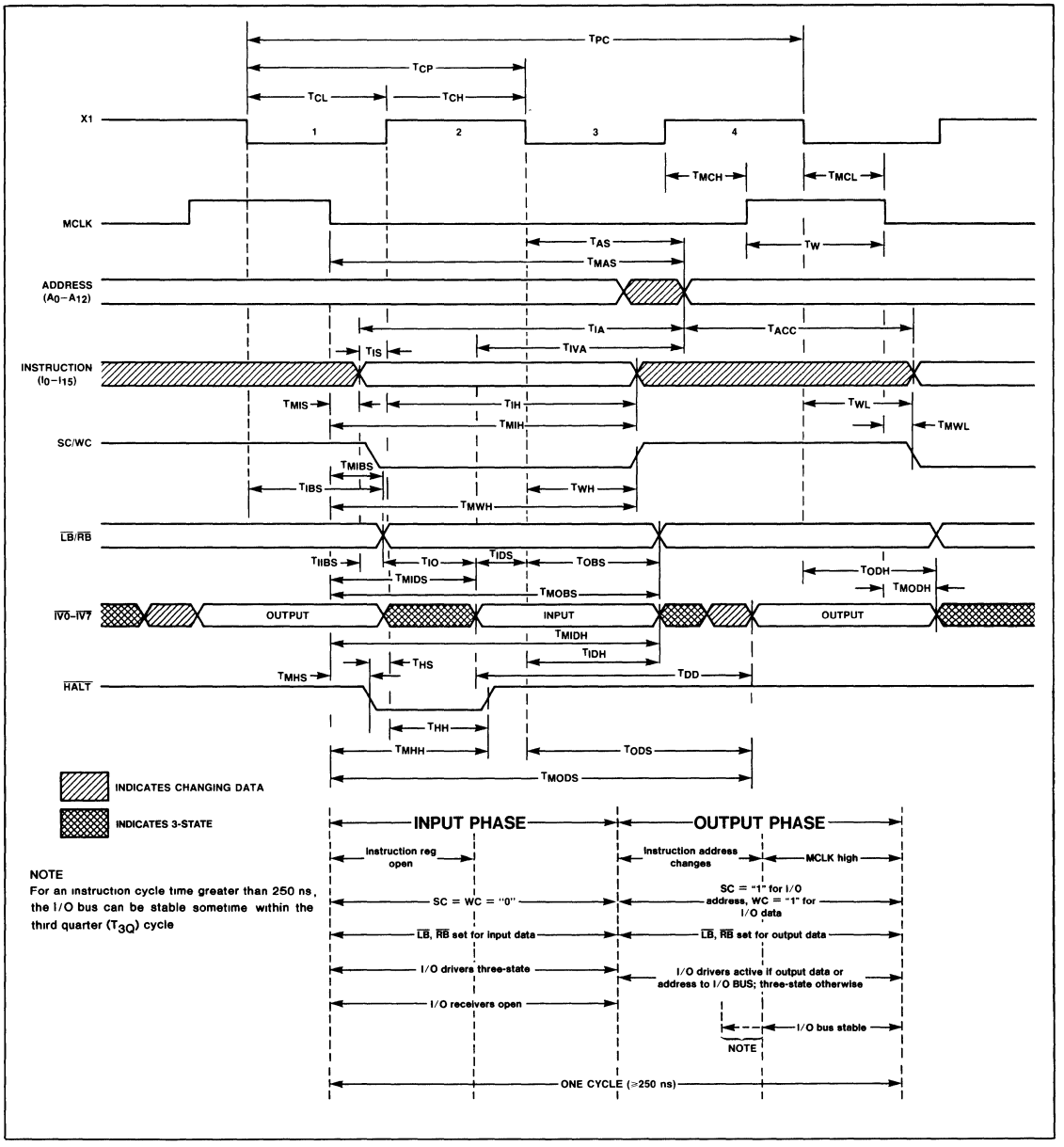
PARAMETER		TEST CONDITIONS (NOTES 1 & 2)	LIMITS			UNIT
			Min	Typ	Max	
Clock:						
T_{PC}	Processor cycle time		300			ns
T_{CP}	X1 clock period		150			ns
T_{CH}	X1 clock high time		62			ns
T_{CL}	X1 clock low time		62			ns
Controls:						
T_{HS}	$\overline{HALT}$ set-up time (X1 rising edge)		0			ns
T_{HH}	$\overline{HALT}$ hold time (X1 rising edge)		50			ns
Instructions:						
T_{AS}	X1 falling edge to address stable	CL = 100pF	35		92	ns
T_{IS}	Instruction set-up time (X1 rising edge)		0			ns
T_{IH}	Instruction hold time (X1 rising edge)		50			ns
T_{MCH}	MCLK high delay	X1 = 2.0V	20		55	ns
T_{MCL}	MCLK low delay	X1 = 2.0V	20		55	ns
T_{WH}	X1 falling edge to SC/$\overline{WC}$ rising edge				80	ns
T_{WL}	X1 falling edge to SC/$\overline{WC}$ falling edge				80	ns
T_{IIBS}	Instruction to $\overline{LB}$/$\overline{RB}$ (input phase)				52	ns
T_{IBS}	X1 falling edge to $\overline{LB}$/$\overline{RB}$ (input phase)		24			ns
T_{OBS}	X1 falling edge to $\overline{LB}$/$\overline{RB}$ (output phase)				90	ns
T_{IDS}	Input data set-up time (X1 falling edge)		36			ns
T_{IDH}	Input data hold time (X1 falling edge)		50			ns
T_{ODS}	Output data stable (X1 falling edge)				125	ns
T_{ODH}	Output data hold time (X1 falling edge)		35		85	ns
T_{ACC}	Instruction access time	Provided by worst case timing	80			ns
T_{IO}	Data I/O access time	Provided by worst case timing	40			ns

NOTES.
1 Operating temperature ranges are guaranteed after thermal equilibrium has been reached.
2 Unless otherwise noted CL = 300 pF, VIN = 3V

TIMING CONSIDERATIONS (Commercial Part)

As shown in the "AC CHARACTERISTICS" table for this part, the minimum instruction cycle time is 25 ns, whereas, the maximum is determined by the on-chip oscillator frequency and can be any value the user chooses. With an instruction cycle time of 250 ns, the part can be characterized in terms of absolute values; these are shown in the first "LIMITS" column of the table. When the instruction cycle time is greater than 250 ns, certain parameters are cycle-time dependent; thus, these parameters are specified in terms of the four quarter cycles (T_{1Q}, T_{2Q}, T_{3Q}, and T_{4Q}) that make up one instruction cycle—see 8X300 TIMING DIAGRAM. As the time interval for each instruction cycle increases (becomes greater than 250 ns), the delay for all parameters that are cycle-time dependent is likewise increased. In some cases, these delays have a significant impact on timing relationships and other areas of systems design; subsequent paragraphs describe these timing parameters and reliable methods of calculation.

8X300 TIMING DIAGRAM



NOTE
For an instruction cycle time greater than 250 ns, the I/O bus can be stable sometime within the third quarter (T_{3Q}) cycle

Timing parameters for the 8X300 are normally measured with reference to X1 or MCLK; those referenced to MCLK are prefaced with an "M" in the mnemonic—TMAS, TMIH, and so on. To determine the timing relationship between a particular signal, say "A" and MCLK, the user should, at all times, use the value specified in the table—DO NOT calculate the value by adding or subtracting two or more parameters that are referenced to X1. When deriving timing relationships between two signals (A to B, etc.) by adding or subtracting the parameter values, the user must consistently use the same parameter reference—MCLK or X1.

System determinants for the instruction cycle time are:

- Propagation delays within the 8X300
- Access time of Program Storage
- Enable time of the I/O port

Normally, the instruction cycle time is constrained by one or more of the following conditions:

Condition 1—Instruction or MCLK to $\overline{LB}/\overline{RB}$ (input phase) plus I/O port access time (TIO) $\leq$ IV data set-up time (Figure 4a).

Condition 2—Program storage access time (TACC) plus instruction to $\overline{LB}/\overline{RB}$ (input phase) plus I/O port access time (TIO) plus IV data (input phase) to address $\leq$ instruction time (Figure 4b).

Condition 3—Program storage access time plus instruction to address $\leq$ instruction cycle time (Figure 4c).

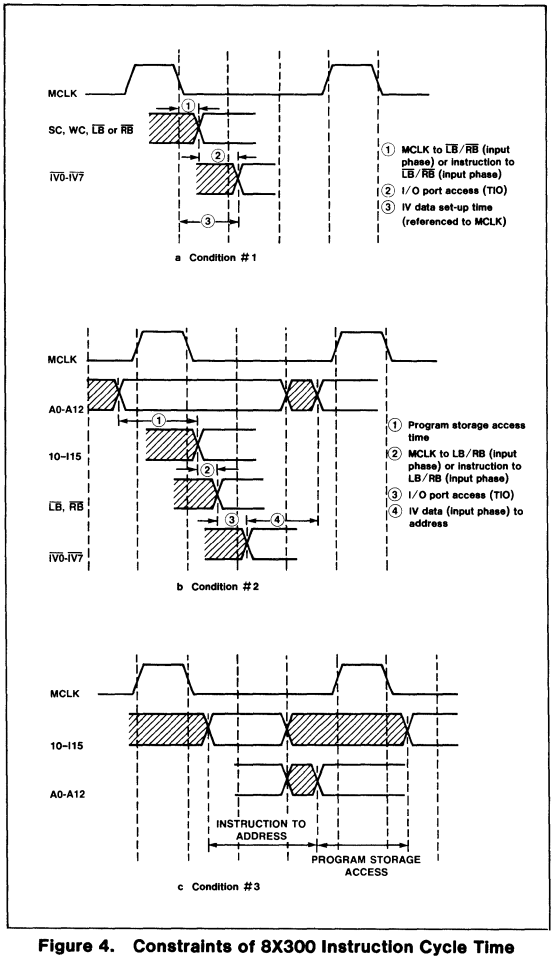


Figure 4. Constraints of 8X300 Instruction Cycle Time

From condition #1 and with an instruction cycle time of 250 ns, the I/O port access time (TIO) can be calculated as follows:

$$TMIBS + TIO \leq TMIDS$$
transposing, $TIO \leq TMIDS - TMIBS$
substituting, $TIO \leq 55ns - 25ns$
result, $TIO \leq 30\ ns$

Using 30 ns for TIO, the constraint imposed by condition #1 can also be used to calculate the minimum cycle time:

$$TMIBS + TIO \leq TMIDS$$
thus, $25ns + 30ns \leq T_{1Q} + T_{2Q} - 70$
$25ns + 30ns \leq \frac{1}{2}$ cycle $- 70$ therefore, the worst-case instruction cycle time is 250 ns. With subject parameters referenced to X1, the same calculations are valid:

$$TIBS + TIO + TIDS \leq \frac{1}{2}\text{ cycle}$$
thus, $70ns + 30ns + 25ns \leq \frac{1}{2}$ cycle therefore, the worst-case instruction cycle time is again 250 ns. From condition #2 and with an instruction cycle time of 250 ns, the program storage access time can be calculated:

$$TACC + TIIBS + TIO + TIVA \leq 250ns$$
transposing, $TACC \leq 250ns - TIIBS - TIO - TIVA$
substituting, $TACC \leq 250ns - 35ns - 30ns - 105ns$
thus, $TACC \leq 80ns$ hence, for an instruction cycle time of 250 ns, a program storage access time of 80 ns is implied. The constraint imposed by condition #3 can be used to verify the maximum program storage access time:

$$TIA + TACC \leq \text{Instruction Cycle}$$
thus, $TACC \leq 250ns - 170ns$
and, $TACC \leq 80ns$, confirming that a program storage access time of 80 ns is satisfactory.

For an instruction cycle time of 250 ns and a program storage access time of 80 ns (Condition #2/Figure 4b), the instruction should be valid 10 ns before the falling edge of MCLK. This relationship can be derived by the following equation:

$$250ns - TMAS - TACC$$
$$= 250ns - 160ns - 80ns$$
$$= 10ns$$

It is important to note that, during the input phase, the beginning of a valid $\overline{LB}/\overline{RB}$ signal is determined by either the instruction to $\overline{LB}/\overline{RB}$ delay (TIIBS) or the delay from the falling edge of MCLK to $\overline{LB}/\overline{RB}$ (TMIBS). Assuming the instruction is valid 10 ns before the falling edge of MCLK and adding the instruction-to-LB/RB delay (TIIBS) = 30ns), the $\overline{LB}/\overline{RB}$ signal will be valid 25 ns after the falling edge of MCLK. With a fast program storage memory and with a valid instruction more than 10 ns before the falling edge of MCLK—the $\overline{LB}/\overline{RB}$ signal will, due to the TMIBS delay, still be valid 25 ns after the falling edge of MCLK. Using a worst-case instruction cycle time of 250 ns, the user cannot gain a speed advantage by selecting a memory with faster access time. Under the same conditions, a speed advantage cannot be obtained by using an I/O port with fast access time (TIO) because the address bus will be stable 80 ns (TAS) after the beginning of the third quarter cycle—no matter how early the IV data input is valid.

Internal Timing and Timing Relationships

All timing and timing-control signals of the 8X300 are generated by the oscillator and sequencer shown in Figure 5. The sequencer outputs direct and control all of the timing parameters specified in the TIMING DIAGRAM. Observe that each input quarter cycle bears a fixed relationship to X1 via the propagation delay.

General and interactive timing relationships pertaining to I/O signals of the 8X300 are shown in Figure 6. Example—in the input phase, the switching point of the $\overline{LB}/\overline{RB}$ signal is caused by the worst-case delay from the instruction to $\overline{LB}/\overline{RB}$ or from the beginning of the first internal quarter cycle to $\overline{LB}/\overline{RB}$; the two arrows pointing to the $\overline{LB}/\overline{RB}$ transition indicate this "either/or" dependency. This information coupled with tabular values and the TIMING DIAGRAM provides the user with the wherewithal to calculate any and all system timing parameters.

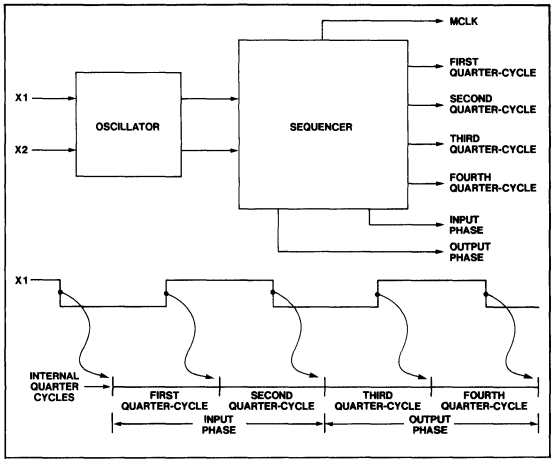


Figure 5. Timing and Timing Control Signals of the 8X300

CLOCK CONSIDERATIONS

The on-chip oscillator and timing-generation circuits of the 8X300 can be controlled by any one of the following methods:

Capacitor: if timing is not critical
Crystal: if precise timing is required
External Drive: if application requires that the 8X300 be synchronized with system clock

Capacitor Timing: A non-polarized ceramic or mica capacitor with a working voltage equal to or greater than 25-volts is recommended. The lead lengths of capacitor should be approximately the same and as short as possible; also, the timing circuits should not be in close proximity to external sources of noise. For various capacitor (C_X) values, the cycle time can be approximated as:

C_X (in pF)	APPROXIMATE CYCLE TIME
100	300 ns
200	500 ns
500	1.1 μs
1000	2.0 μs

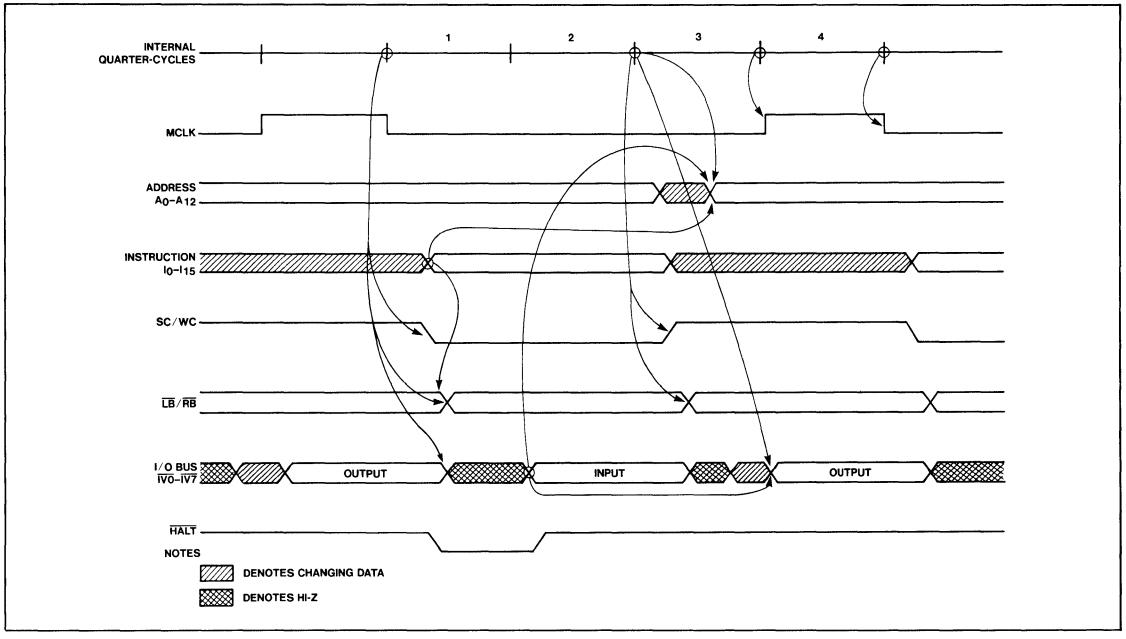


Figure 6. Timing Relationships of 8X300 I/O Signals

Crystal Timing: When a crystal is used, the on-chip oscillator operates at the resonant frequency (f_O) of the crystal; the series-resonant quartz crystal connects to the 8X300 via pins 10 (X1) and 11 (X2). The lead lengths of the crystal should be approximately equal and as short as possible; also, the timing circuits should not be in close proximity to external sources of noise. The crystal should be hermetically sealed (HC type can) and have the following electrical characteristics:
Type: Fundamental mode, series resonant
Impedance at Fundamental: 35-ohms maximum
Impedance at Harmonics and Spurs: 50-ohms minimum

The resonant frequency (f_O) of the crystal is related to the desired cycle time (T) by the equation $f_O = 2/T$; for a cycle time of 250 ns, f_O = 8MHz.

Using an External Clock: The 8X300 can be synchronized with an external clock by simply connecting appropriate drive circuits to the X1/X2 inputs. Figure 7 shows how the on-chip oscillator can be driven from the complementary outputs of a pulse generator. In applications where the microcontroller must be driven from a master clock, the X1/X2 lines can be interfaced to TTL logic as shown in Figure 8.

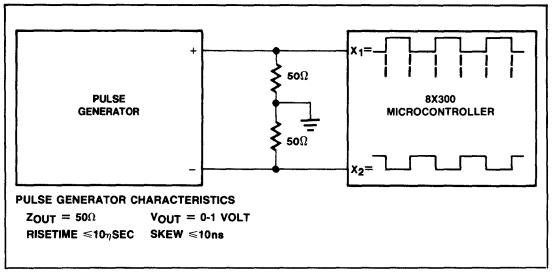


Figure 7. Clocking with a Pulse Generator

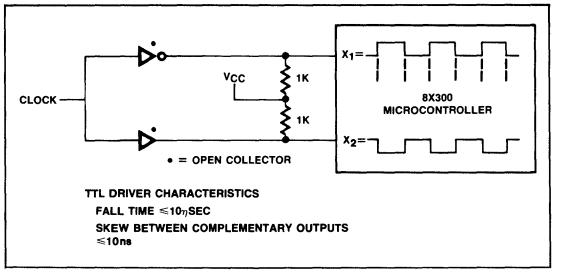


Figure 8. Clocking with TTL

RESET Logic

The $\overline{\text{RESET}}$ line (pin 43) can be driven from a high (inactive) state to a low (active) state at any time with respect to the system clock, that is, the reset function is asynchronous. To ensure proper operation, the $\overline{\text{RESET}}$ line should be held low (active) for one full instruction time. When the line is driven from a high state to an active-low state, several events occur—the precise instant of occurrence is basically a function of the propagation delay for that particular event. As shown in the acompanying $\overline{\text{RESET}}$ timing diagram, these events are:

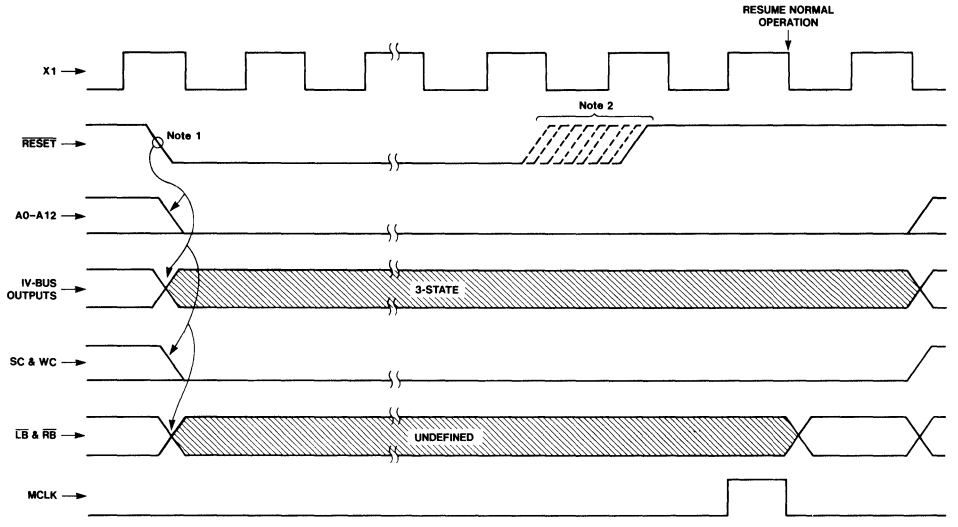
- **The Program Counter and Address Register are set to an all-zero configuration and remain in that state as long as the $\overline{\text{RESET}}$ line is low. Other than PC and AR, reset does not affect other internal registers.**
- **The input/output (IV) bus goes three-state and remains in that mode as long as the $\overline{\text{RESET}}$ line is low.**
- **The Select Command and Write Command signals are driven low and remain inactive as long as the $\overline{\text{RESET}}$ line is low.**
- **The Left Bank/Right Bank signals are undefined for the period in which the $\overline{\text{RESET}}$ line is low.**

During the time $\overline{\text{RESET}}$ is active-low, MCLK is inhibited; moreover, if the $\overline{\text{RESET}}$ line is driven low during the last two quarter cycles, MCLK can be shortened for that particular machine cycle. When $\overline{\text{RESET}}$ line is driven high (inactive)—one-quarter to one full instruction cycle later—MCLK appears just before normal operation is resumed. The $\overline{\text{RESET}}$/MCLK relationship is clearly shown by "B" in the timing diagram. As long as the $\overline{\text{RESET}}$ line is active-low, the $\overline{\text{HALT}}$ signal (described next) is not sampled by internal logic of the 8X300.

HALT Logic

The $\overline{\text{HALT}}$ signal is sampled via internal chip logic at the end of the first internal quarter of each instruction cycle. If, when sampled, the HALT signal is active-low, a halt is immediately executed and the current instruction cycle is terminated; however, the halt cycle does not inhibit MCLK nor does it affect any internal registers of the 8X300. As long as the $\overline{\text{HALT}}$ line is active-low, the SC and WC lines are low (inactive) and the input/output (IV) bus remains in the three-state mode of operation. The halt cycle continues until, when again sampled, the $\overline{\text{HALT}}$ line is found to be high; at this time, normal operation is resumed. Timing for the halt signal is shown in the accompanying diagram.

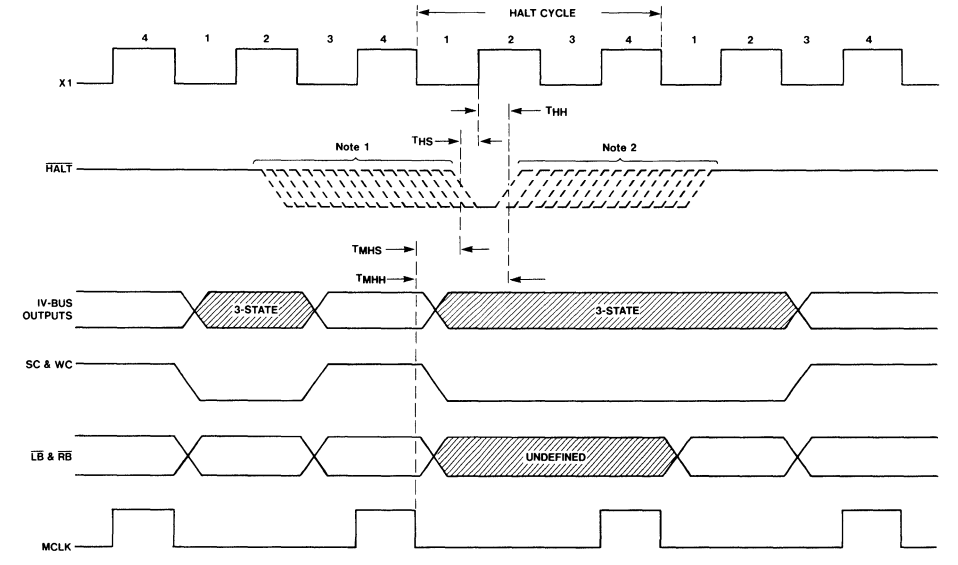
$\overline{\text{RESET}}$ TIMING DIAGRAM



NOTES

1. A High to Low transition of the $\overline{\text{RESET}}$ signal will force the Address Bus to an all-zero configuration.
2. The $\overline{\text{RESET}}$ signal can switch from Low to High at any point within this time interval and, in all cases, MCLK will occur at least one-quarter cycle time later as shown

$\overline{\text{HALT}}$ TIMING DIAGRAM



NOTES

1. The $\overline{\text{HALT}}$ signal can switch from High to Low at any time during this interval.
2. The $\overline{\text{HALT}}$ signal can switch from Low to High at any time during this interval

Timing Descriptions:

T_{HS}—set-up time from $\overline{\text{HALT}}$ to X1 (independent of instruction cycle time)

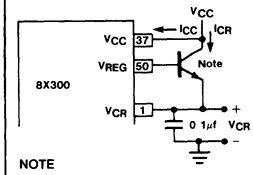
T_{HH}—hold time from X1 to $\overline{\text{HALT}}$ (independent of instruction cycle time)

T_{MHS}—set-up time from MCLK to $\overline{\text{HALT}}$ (dependent upon instruction cycle time)

T_{MHH}—hold time from MCLK to $\overline{\text{HALT}}$ (dependent upon instruction cycle time)

VOLTAGE REGULATOR

All internal logic of the 8X300 is powered by an on-chip voltage regulator that requires an external series-pass transistor. Electrical specifications for the off-chip power transistor and a typical hook-up are shown in the accompanying diagram. To minimize lead inductance, the transistor should be as close as possible to the 8X300 package and the emitter should be ac-grounded via a 0.1-microfarad ceramic capacitor.



PARAMETER	CONDITIONS	LIMITS
h_{fe}	V_{CE} = 2V, 100mA < I_C < 500mA	>50
BE_{ON}	V_{CE} = 5V, I_C = 500mA	<1V
V_{CESAT}	I_C = 500mA, I_B = 50mA	<0 5V
BV_{CEO}		>15V
f_t		>30MHz

NOTE
Typical approved parts—2N5320, 2N5337

FEATURES

- **Fetch, Decode, and Execute a 16-bit Instruction in a minimum of 200 nanoseconds (one machine cycle)**
- **Bit-oriented instruction set (addressable single-or-multiple bit subfields)**
- **Separate buses for instruction, instruction Address and Three-State I/O**
- **Thirteen 8-bit general-purpose working registers**
- **Source/destination architecture**
- **Bipolar low-power Schottky technology/TTL inputs and outputs**
- **On-chip oscillator and timing generation**
- **Single +5V supply**
- **0.9-in. 50-pin DIP**

PRODUCT DESCRIPTION

The Signetics 8X305 MicroController (Figure 1) is a high-speed bipolar microprocessor implemented with low-power Schottky technology. In a single chip, the 8X305 combines speed, flexibility, and a bit-oriented instruction set. These features and other basic characteristics of the chip combine to provide cost-effective solutions for a broad range of applications. The 8X305 is particularly useful in systems that require high-speed bit manipulations — sophisticated controllers, data communications, very fast interface control, and other applications of a similar nature.

The 8X305 can fetch, decode, and execute a 16-bit instruction word in a minimum of 200 nanoseconds. Within one instruction cycle, the 8-bit data-processing path can be programmed to rotate, mask, shift, and/or merge single or multiple bit subfields and, in addition, perform an ALU operation; in the same instruction, an external data field can be input, processed, and output to a specified destination — likewise, single or multiple bit data fields can be internally moved from a given source to a given destination. To summarize, fixed or variable-length data fields can be fetched, processed, operated on by the ALU, and moved to a different location — all in a timeframe of 200 nanoseconds. To interface with I/O and program memory, the 8X305 uses a 13-bit instruction address bus, a 16-bit instruction bus, an 8-bit bidirectional multiplexed I/O data/address bus and a 5-bit I/O control bus.

A wide selection of I/O devices, interface chips, and special-purpose parts are available for systems use. In most applications, the more powerful 8X305 is functionally interchangeable with its predecessor — the 8X300.

ASSOCIATED DOCUMENTATION

Other documents directly relating to *design* and *applications use* of the 8X305 MicroController are:

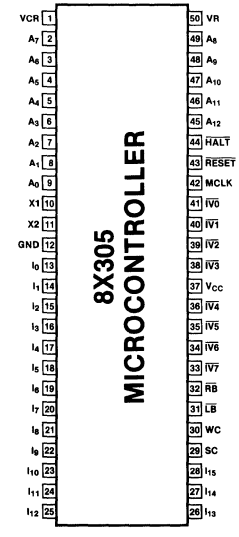
- Product Capabilities Manual
- 8X305 Users Manual

These documents and other current literature (Data Sheets, Product Bulletins, Applications Notes, etc.) are available at all Signetics Sales and Service Offices—see rear cover of this data sheet for the office in your locality.

3

PIN CONFIGURATION

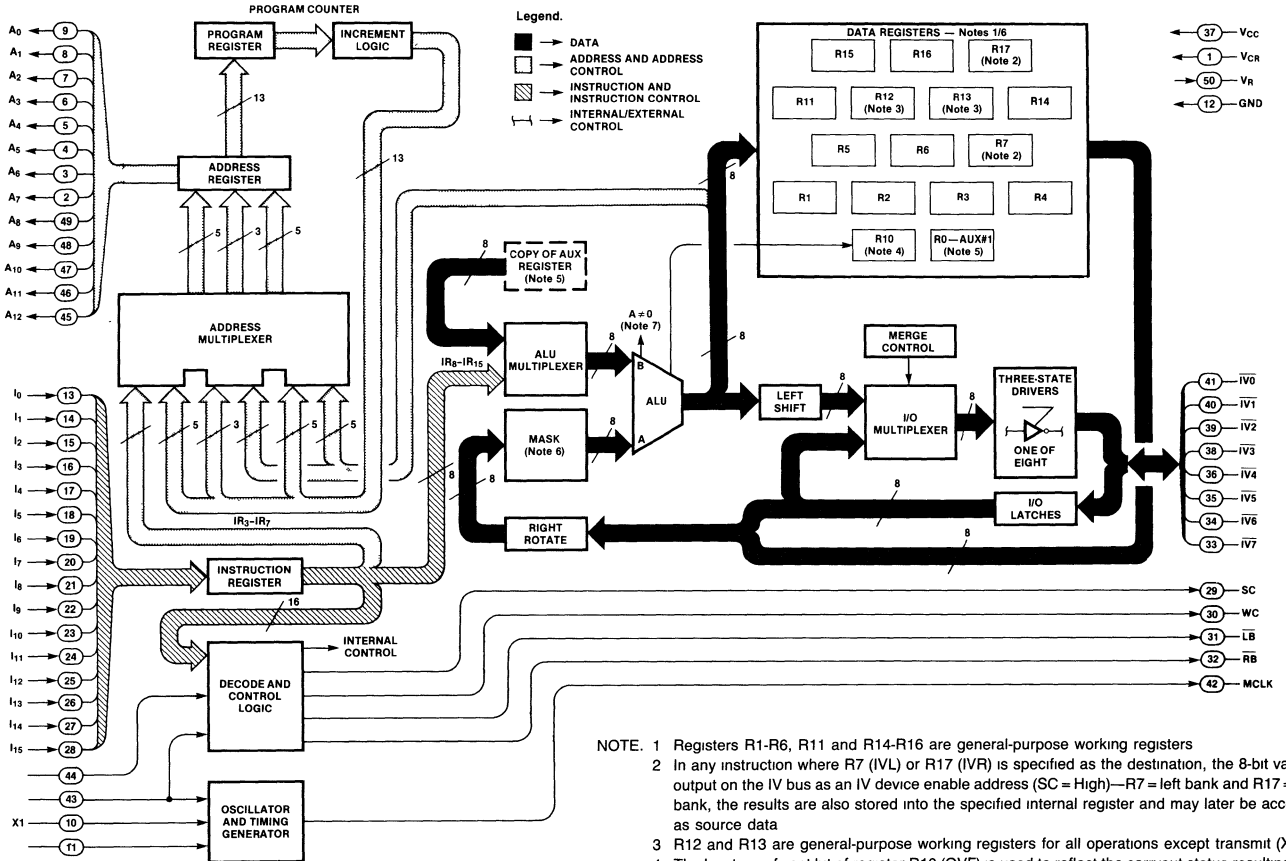
N, I PACKAGE



TOP VIEW

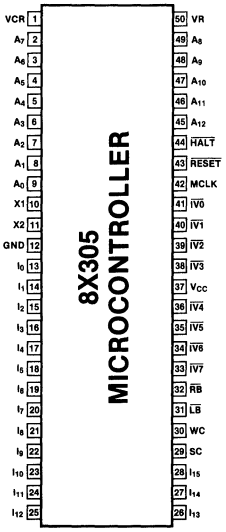
ORDER NUMBERS

8X305N, 8X305I
S8X305I/883B, S8X305I/883C



NOTE. 1 Registers R1-R6, R11 and R14-R16 are general-purpose working registers
2 In any instruction where R7 (IVL) or R17 (IVR) is specified as the destination, the 8-bit value is output on the IV bus as an IV device enable address (SC = High)—R7 = left bank and R17 = right bank, the results are also stored into the specified internal register and may later be accessed as source data
3 R12 and R13 are general-purpose working registers for all operations except transmit (XMIT)
4 The least significant bit of register R10 (OVF) is used to reflect the carryout status resulting from the most recent ADD operation
5 Auxiliary register R0 #1 is a general-purpose working register that holds the implied operand for Arithmetic and Logical operations; the content of this register is repeated in AUX #2 (shown dotted) The duplicate register is physically part of the ALU and is shown separate only for layout convenience
6 Internal working registers cannot be operated on by the MASK logic
7 During NZT instructions the ALU tests for all bits equal to "0" (Transfer if A≠0)—refer to BASIC OPERATIONS that follow

Figure 1. Architecture and Pin Designations for 8X305 MicroController



PIN NO.	IDENTIFIER	FUNCTION
1	VCR	Regulated voltage input from series-pass transistor (2N5320 or equivalent)
2-9, 45-49	$A_0 - A_{12}$	**Program Address Lines:** These active-high outputs permit direct addressing of up to 8192 words of program storage; A_{12} is least significant bit
10, 11	X1, X2	Timing generator connections for a capacitor, a series resonant crystal, or an external clock source with complementary outputs.
12	GND	Ground.
13-28	$I_0 - I_{15}$	**Instruction Lines:** These active-high input lines receive 16-bit instructions from program storage; I_{15} is least significant bit.
29	SC	**Select Command:** When high (binary 1), an address is being output on pins $\overline{IV0}$ through $\overline{IV7}$.
30	WC	**Write Command:** When high (binary 1), data is being output on pins $\overline{IV0}$ through $\overline{IV7}$
31	$\overline{LB}$	**Left Bank Control:** When low (binary 0), devices connected to the Left Bank are accessed (Note. *Typically, the $\overline{LB}$ signal is tied to the $\overline{ME}$ input pin of I/O peripherals).*
32	RB	**Right Bank Control:** When low (binary 0), devices connected to the Right Bank are accessed (Note *Typically, the $\overline{RB}$ signal is tied to the $\overline{ME}$ input pin of I/O peripherals).*
33-36, 38-41	$\overline{IV0}$-$\overline{IV7}$	**Interface Vector** (Input/Output Bus) — these bidirectional active-low three-state lines communicate data and/or addresses to I/O devices and memory locations A low voltage level equals a binary "1", $\overline{IV7}$ is Least Significant Bit.
37	V_{CC}	+5V power supply.
42	MCLK	**Master Clock:** This active-high output signal is used for clocking I/O devices and/or synchronization of external logic.
43	$\overline{RESET}$	When **$\overline{RESET}$** input is low (binary 0), the 8X305 is initialized — sets Program Counter/Address Register to zero and inhibits MCLK For the period of time $\overline{RESET}$ is low, the Left Bank/Right Bank ($\overline{LB}$/$\overline{RB}$) signals are forced high asynchronously.
44	$\overline{HALT}$	When **$\overline{HALT}$** input is low (binary 0), internal operation of the 8X305 stops at the start of next instruction; MCLK is not inhibited nor is any internal register affected; however, both the Left Bank/Right Bank ($\overline{LB}$/$\overline{RB}$) signals are synchronously driven high during the first quarter of the instruction cycle time and remain high during the time HALT is low
50	VR	Internally-generated reference output voltage for external series-pass regulator transistor

Figure 2. Designations and Descriptions for Pins of 8X305 MicroController.

FUNCTIONAL OPERATION

Typical System Configuration

Although the system hookup shown in Figure 3 is of the simplest form, it provides a fundamental look at the 8X305 MicroController and peripheral relationships. As indicated, the 8X305 can directly address up to 8K words of program storage — either ROM or PROM. The user interface ($\overline{IV0}$ through $\overline{IV7}$) is capable of uniquely addressing 256 Input/Output locations and, with additional bank bits ($\overline{LB}$, $\overline{RB}$), this number is expanded to 512 — each bank comprising 256 addressable locations. The addressable locations of each bank can be used in a variety of ways; a simple method of implementation is shown in Figure 3. When $\overline{LB}$ is active low, the left bank is enabled and any one of 256 locations within the RAM memory can be accessed for input/output operations. A similar set of "enable/access" conditions are applicable to the right bank when $\overline{RB}$ is active low.

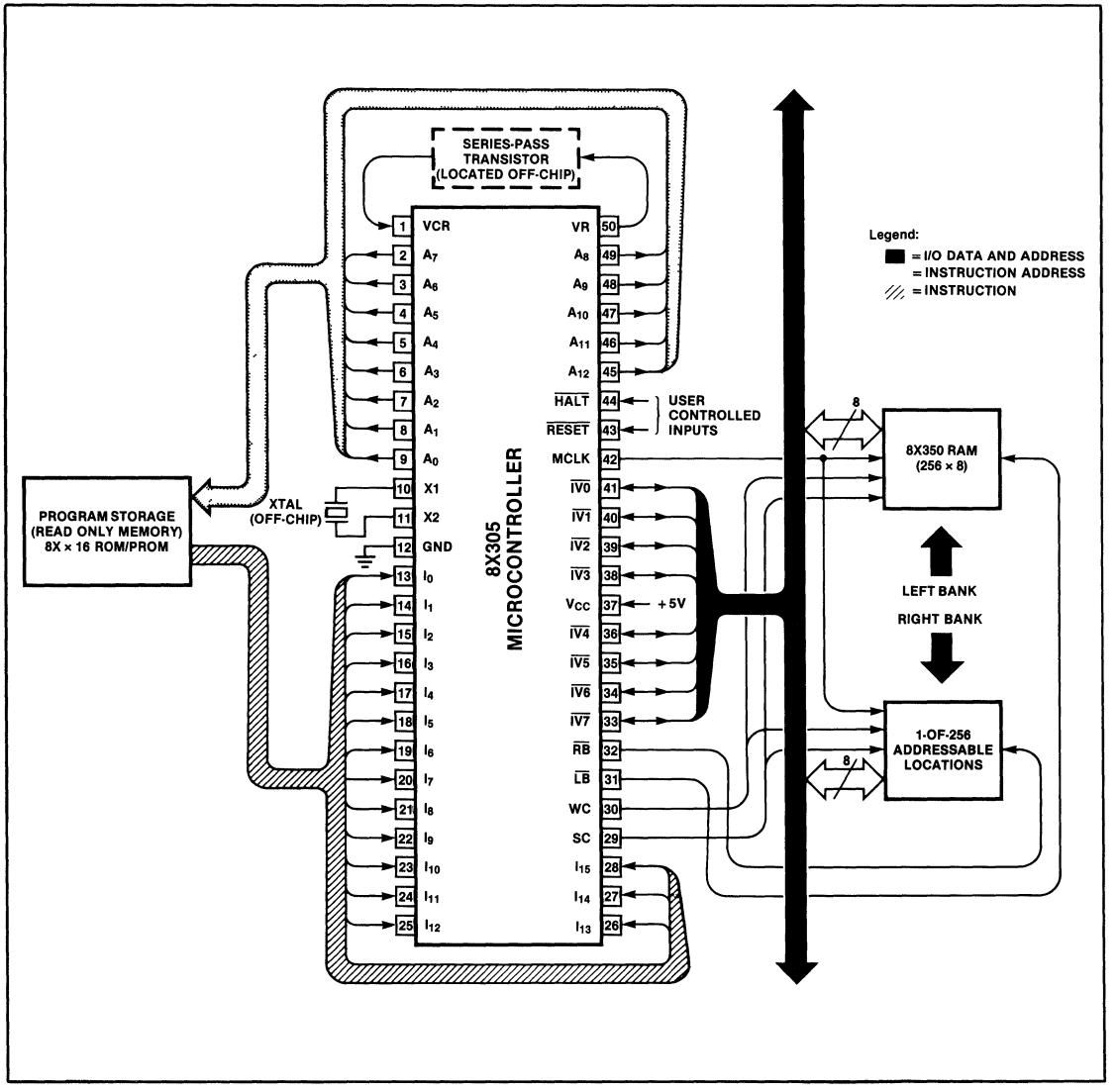


Figure 3. Typical 8X305 System Hookup

BASIC OPERATIONS OF 8X305

Refer to a later discussion of "Instruction Fields" for a detailed examination of all operand fields and subdivisions thereof—"S" (S_0, S_1), "D" (D_0, D_1), "R", "L", "J", and "A"

MOVE OPERATIONS

REGISTER-TO-REGISTER

SOURCE	DATA PROCESSING (PRE-ALU)	ALU	DATA PROCESSING (POST-ALU)	DESTINATION
R0-R17 as specified by "S" field of instruction	Right rotate as specified by "R" field of instruction	No operation	No operation	R0-R7, R11-R17 as specified by "D" field of instruction

REGISTER-TO-$\overline{IV}$ BUS

SOURCE	DATA PROCESSING (PRE-ALU)	ALU	DATA PROCESSING (POST-ALU)	DESTINATION
R0-R17 as specified by "S" field of instruction	No operation	No operation	Shift and merge as specified by "D_0" and "L" fields of instruction	Variable length field of $\overline{IV}$ bus—Left Bank ($\overline{LB}$) or Right Bank ($\overline{RB}$) as specified by "D_0" and "D_1" fields of instruction

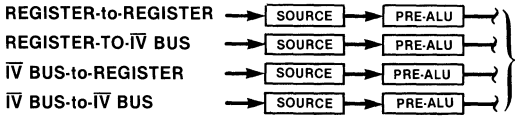
$\overline{IV}$ BUS-TO-REGISTER

SOURCE	DATA PROCESSING (PRE-ALU)	ALU	DATA PROCESSING (POST-ALU)	DESTINATION
Variable length field of $\overline{IV}$ bus—Left Bank ($\overline{LB}$) or Right Bank ($\overline{RB}$) as specified by "S_1" and "S_0" fields of instruction	Right rotate and mask as specified by "S_0" and "L" fields of instruction	No operation	No operation	R0-R7, R11-R17 as specified by "D" field of instruction

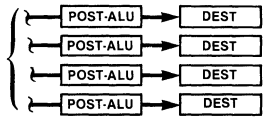
$\overline{IV}$ BUS-TO-$\overline{IV}$ BUS

SOURCE	DATA PROCESSING (PRE-ALU)	ALU	DATA PROCESSING (POST-ALU)	DESTINATION
Variable length field of $\overline{IV}$ bus—Left Bank ($\overline{LB}$) or Right Bank ($\overline{RB}$) as specified by "S_1" and "S_0" fields of instruction	Right rotate and mask as specified by "S_0" and "L" fields of instruction	No operation	Shift and merge as specified by "D_0" and "L" fields of instruction	Variable length field of $\overline{IV}$ bus—Left Bank ($\overline{LB}$) or Right Bank ($\overline{RB}$) as specified by "D_0" and "D_1" fields of instruction

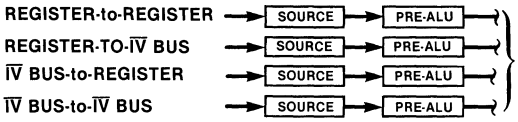
ADD OPERATIONS



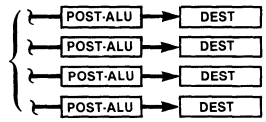
Same as MOVE operations, except source data is ADDed to contents of AUXiliary Register R0 via the ALU, if appropriate, Overflow Register R10 (OVF) is also set.



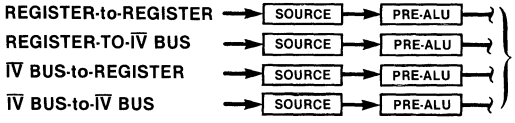
AND OPERATIONS



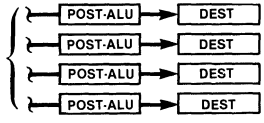
Same as MOVE operations, except source data is ANDed with contents of AUXiliary Register R0 via the ALU.



EXCLUSIVE OR (XOR) OPERATIONS



Same as MOVE operations, except source data is Exclusively ORed with contents of AUXiliary Register R0 via the ALU



EXECUTE (XEC) OPERATIONS

XEC, REGISTER

SOURCE	DATA PROCESSING (PRE-ALU)	ALU	DATA PROCESSING (POST-ALU)	DESTINATION
R0–R17 as specified by "S" field of instruction	No operation.	Add source data to 8-bit field specified by instruction literal ($0 \leq J \leq 377_8$)	No operation.	Replace 8 LSB of Address Register* with 8-bit sum from ALU *PGM CTR unchanged

XEC, $\overline{IV}$ BUS

SOURCE	DATA PROCESSING (PRE-ALU)	ALU	DATA PROCESSING (POST-ALU)	DESTINATION
Left or Right Bank of $\overline{IV}$ bus as specified by "S" field of instruction	Rotate and mask as specified by "S_0" and "L" fields of instruction	Add masked field of source data to 5-bit literal specified by "J" field of instruction ($0 \leq J \leq 37_8$)	No operation	Replace 5 LSB of Address Register* with 5-bit sum from ALU *PGM CTR unchanged

NON-ZERO TRANSFER (NZT) OPERATIONS

NZT, REGISTER

SOURCE	DATA PROCESSING (PRE-ALU)	ALU	DESTINATION
R0–R17 as specified by "S" field of instruction.	No operation	Test contents of source register for all zeroes	If S = 0, increment PC by 1, if S≠0, replace 8 LSB of AR and PC with literal specified by "J" field of instruction

NZT, $\overline{IV}$ BUS

SOURCE	DATA PROCESSING (PRE-ALU)	ALU	DESTINATION
Left or Right Bank of $\overline{IV}$ bus as specified by "S" field of instruction	Rotate and mask as specified by "S_0" and "L" fields of instruction	Test contents of masked field for all zeroes.	If S = 0, increment PC by 1, if S≠0, replace 5 LSB of AR and PC with literal specified by "J" field of instruction

TRANSMIT (XMIT) OPERATIONS

XMIT, REGISTER

SOURCE	DATA PROCESSING (PRE-ALU)	ALU	DATA PROCESSING (POST-ALU)	DESTINATION
$0 \leq J \leq 377_8$ – value specified by "J" field of instruction	No operation	No operation	No operation	R0–R7, R11, R14–R17 Load 8-bit integer specified by "J" field into register specified by "D" field

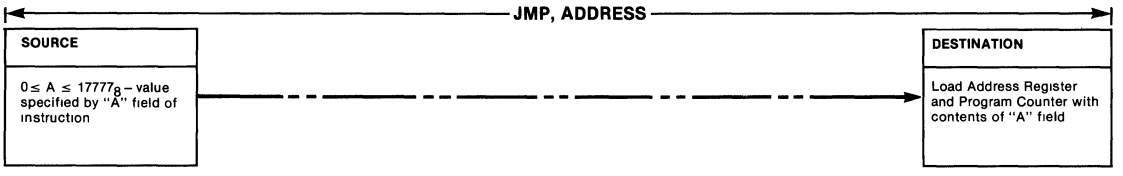
XMIT 8-BITS IMMEDIATE, $\overline{IV}$ BUS

SOURCE	DATA PROCESSING (PRE-ALU)	ALU	DATA PROCESSING (POST-ALU)	DESTINATION
$0 \leq J \leq 377_8$ – value specified by "J" field of instruction	No operation	No operation	No operation	Left (R12) or Right (R13) Bank of $\overline{IV}$ bus as specified by "D" field of instruction

XMIT VARIABLE-BIT FIELD IMMEDIATE $\overline{IV}$ BUS

SOURCE	DATA PROCESSING (PRE-ALU)	ALU	DATA PROCESSING (POST-ALU)	DESTINATION
$0 \leq J \leq 37_8$ – value specified by "J" field of instruction	No operation	No operation	Shift and merge source data as specified by "D_0" and "L" fields of instruction	Left or Right Bank of $\overline{IV}$ bus as specified by "D" field of instruction

JUMP (JMP) OPERATION



Program Storage Interface

As shown in Figure 3, program storage is connected to output address lines A_0 through A_{12} (A_{12} = LSB) and input instruction lines I_0 through I_{15}. An address output on A_0/A_{12} identifies one 16-bit instruction word in program storage. The instruction word is subsequently input on I_0/I_{15} and defines the MicroController operation which is to follow — one instruction word equals one completed operation. Any TTL-compatible memory can be used for program storage provided the worst-case access time is compatible with the instruction cycle time used for the application — see timing section for appropriate calculations.

I/O Interface and Control

An 8-bit bidirectional I/O bus, referred to as the Interface Vector ($\overline{IV}$) bus, provides a communication link between the MicroController and the two banks of I/O devices. The $\overline{LB}$ (Left Bank) and $\overline{RB}$ (Right Bank) control signals identify which bank is enabled; when both $\overline{LB}$ and $\overline{RB}$ are high (inactive), neither bank is enabled and the $\overline{IV}$ bus is inactive (three-state). A functional analysis of the Left and Right Bank signals is shown below:

$\overline{LB}$	$\overline{RB}$	FUNCTION
Low	Low	This state is not generated by the 8X305.
Low	High	Enable left bank devices.
High	Low	Enable right bank devices.
High	High	Disable all devices; $\overline{IV}$ bus is three-state.

Both data and I/O address information are multiplexed on the $\overline{IV}$ bus. The SC (Select Command) and WC (Write Command) signals distinguish between data and I/O address information as follows:

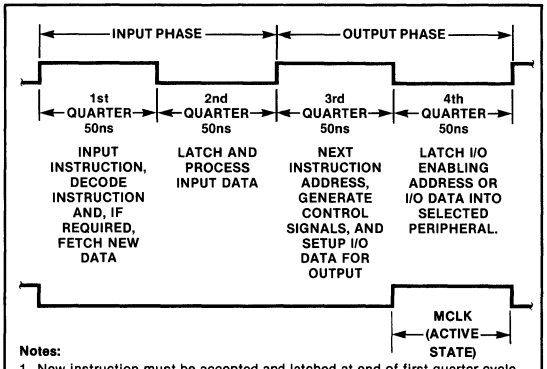
LB/RB	SC	WC	FUNCTION
High	Low	Low	The $\overline{IV}$ bus is three-state and not looking for input data.
Low	Low	Low	The $\overline{IV}$ bus is reading input data.
Low	Low	High	Data is being output.
Low	High	Low	Address is being output.
X	High	High	This condition is never generated.

Data Processing

Basically, the data processing path of the 8X305 consists of the Rotate/Mask logic, the Arithmetic Logic Unit (ALU), the Shift/ Merge functions, on-chip memory (sixteen 8-bit registers), and the bidirectional $\overline{IV}$ bus interface with its associated driver circuits and internal latches. The on-board memory and the $\overline{IV}$ bus are connected to both inputs and outputs of the ALU via internal 8-bit data paths — see Figure 1. Inputs to the ALU are preceded by right-rotate and data-mask functions; the ALU output is followed by the left-shift and merge operations. Depending on the desired operation, any one or all of the functions (Rotate/Mask/Shift/Merge) can operate on 8 bits of data in a single instruction cycle. For a summary of all data-processing capabilities, refer to BASIC OPERATIONS OF THE 8X305 described earlier in this data sheet.

Instruction Cycle

Each operation of the 8X305 is executed in a single instruction cycle. The instruction cycle is internally divided into four equal parts — each part being as short as 50 nanoseconds. Figure 4 shows the general functions that



Notes:
1 New instruction must be accepted and latched at end of first quarter cycle.
2 The I/O data latches are open for the first two quarter cycles, that is, for 100 nanoseconds.
3 The address changes during third quarter cycle
4 $\overline{IV}$ bus drivers are active (turned on) during third and fourth quarter cycles

Figure 4. Instruction Cycle and MCLK with: Crystal = 10MHz and Cycle Time = 200 nanoseconds.

occur during each quarter cycle; specifics regarding minimum/maximum timing and other critical values are described later in this data sheet. During the first quarter cycle, a new instruction from program storage is input via I_0–I_{15} and decoded. If an I/O operation is indicated, new data is fetched from a specified internal register or via the $\overline{IV}$ bus. At the end of the first quarter cycle, the new instruction is latched into the instruction register.

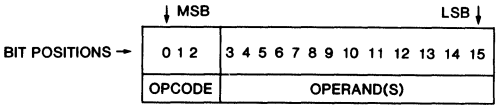
In the second quarter cycle, the I/O input data stabilizes and preliminary processing is completed; at the end of this quarter, the $\overline{IV}$ latches close and final processing can be accomplished, thus completing the input phase of the instruction cycle. During the third quarter cycle, the address for the next instruction is output to the instruction address bus, $\overline{IV}$ control signals are generated, and both data and destination are setup for the remainder of the output phase. During the fourth quarter cycle, a master clock signal (MCLK) generated by the 8X305 is used to latch either the I/O-enabling address or the I/O data into peripheral devices connected to the $\overline{IV}$ bus; MCLK can also be used to synchronize any external logic with timing circuits of the 8X305. To summarize the action, the first half of the instruction cycle deals primarily with input functions and the second half is mostly concerned with output functions.

INSTRUCTION SET

General Format and Operating Principles

The 16-bit instruction word (I_0 through I_{15}) from program storage is input to the instruction register (Figure 1) and is subsequently decoded to implement the events to occur during the current instruction cycle.

The general format for each instruction word is as follows:



The 3-bit operation code (OPCODE) define any one of eight classes of instructions; variations within each class are specified by the remaining thirteen operand bits. The eight instruction classes can be separated into two control areas — *data* and *program;* general functions within these areas are:

- Data Control —
  - ADD, AND, XOR } Arithmetic and Logic Operations
  - MOVE, XMIT } Movement of Data and Constants
- Program Control
  - XEC, NZT, JMP } Branch or Test

Instruction Fields

As shown in Table 1, each instruction word consists of an operation code (OPCODE) field and from one to three operand fields. The possible operand fields are: Source (S), Destination (D), Rotate/Length (R/L), Literal (J), and Address (A). The OPCODE and operand fields are described in the paragraphs that follow the table.

Table 1. FUNCTIONAL DESCRIPTION OF INSTRUCTION SET

INSTRUCTION WORD	DESCRIPTION	STATE OF CONTROL SIGNAL DURING INSTRUCTION CYCLE — SEE FIGURE 4		
		CONTROL SIGNAL	INPUT PHASE	OUTPUT PHASE
CLASS = **MOVE** OPCODE = **0** OPERATION = **(S) → D**				
Register-to-Register 0 1 2 | 3 4 5 6 7 | 8 9 10 | 11 12 13 14 15 OPCODE | S | R | D $S = 00_8$-17_8 $D = 00_8$-07_8, 11_8-17_8	Move content of internal register specified by S-field to internal register specified by D-field Prior to the "MOVE" operation, right-rotate contents of internal source register by octal value (0 through 7) defined by the R-field	SC	L	H if $D = 07_8$, 17_8
		WC	L	L
		$\overline{LB}$	H	L if $D = 07_8$
		$\overline{RB}$	H	L if $D = 17_8$
Register-to-$\overline{IV}$ Bus (Note) 0 1 2 | 3 4 5 6 7 | 8 9 10 | 11 12 13 14 15 OPCODE | S | L | D D_1 : D_0 $S = 00_8$-17_8 $D = 20_8$-37_8	Move contents of internal register specified by the S-field to the $\overline{IV}$ bus Before outputting on $\overline{IV}$ bus, data is shifted as specified by the least significant octal digit of the D-field and the bits specified by the L-field are merged with the latched I/O data	SC	L	L
		WC	L	H
		$\overline{LB}$	L if $D = 20_8$-27_8	L if $D = 20_8$-27_8
		$\overline{RB}$	L if $D = 30_8$-37_8	L if $D = 30_8$-37_8

Table 1. FUNCTIONAL DESCRIPTION OF INSTRUCTION SET (Continued)

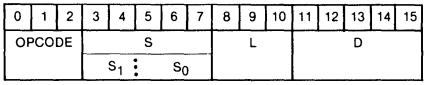
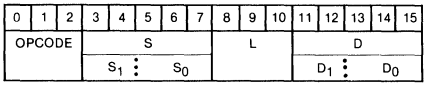
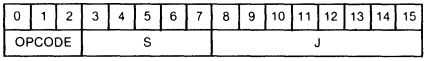
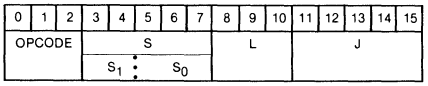
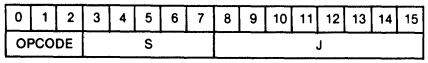
INSTRUCTION WORD	DESCRIPTION	STATE OF CONTROL SIGNAL DURING INSTRUCTION CYCLE — SEE FIGURE 3		
		CONTROL SIGNAL	INPUT PHASE	OUTPUT PHASE
CLASS = MOVE OPCODE = 0 OPERATION = (S) → D				
$\overline{IV}$ Bus-to-Register (Note)  $S = 20_8$-37_8 $D = 00_8$-07_8, 11_8-17_8	Move right-rotated $\overline{IV}$ bus (source) data specified by the S-field to internal register specified by the D-field The L-field specifies the length of source data starting from the LSB-position and, if less than 8 bits, the remaining bits are filled with zeros	SC	L	H if D = 07_8, 17_8
		WC	L	L
		$\overline{LB}$	L if S = 20_8-27_8	L if D = 07_8
		$\overline{RB}$	L if S = 30_8-37_8	L if D = 17_8
$\overline{IV}$ Bus-to-$\overline{IV}$ Bus (Note)  $S = 20_8$-37_8 $D = 20_8$-37_8	Move right-rotated $\overline{IV}$ bus (source) data specified by the S-field to the I/O latches Before outputting on $\overline{IV}$ bus, shift data as specified by the D-field, then merge source and latched I/O data as specified by the L (length) field	SC	L	L
		WC	L	H
		$\overline{LB}$	L if S = 20_8-27_8	L if D = 20_8-27_8
		$\overline{RB}$	L if S = 30_8-37_8	L if D = 30_8-37_8
CLASS = ADD OPCODE = 1 OPERATION = (S) + (AUX) → D				
Same as MOVE instruction class	Same as MOVE instruction class except that contents of AUX (R0) register are ADDed to the source data If there is a "carry" from MSB, then R10 (OVF) = 1 (overflow), otherwise OVF = 0	Same as MOVE instruction class		
CLASS = AND OPCODE = 2 OPERATION = (S) ∧ (AUX) → D				
Same as MOVE instruction class	Same as MOVE instruction class except that contents of AUX (R0) register are ANDed with source data	Same as MOVE instruction class		
CLASS = XOR OPCODE = 3 OPERATION = (S) ⊕ (AUX) → D				
Same as MOVE instruction class	Same as MOVE instruction class except that contents of AUX (R0) register are Exclusively ORed with source data	Same as MOVE instruction class		
CLASS = XEC OPCODE = 4 OPERATION = Refer to Description				
Register Immediate  $S = 00_8$-17_8 $J = 000_8$-377_8	Execute instruction at current page address offset by J (literal) + (S) Return to normal instruction flow unless a branch is encountered Execute instruction at an address determined by replacing the low-order 8 bits of the Address Register with the following derived sum Value of literal (J-field) plus contents of internal register specified by S-field The PC is not incremented and the overflow status (OVF) is not changed	SC	L	L
		WC	L	L
		$\overline{LB}$	H	H
		$\overline{RB}$	H	H
$\overline{IV}$ Bus Immediate (Note)  $S = 20_8$-37_8 $J = 00_8$-37_8	Execute instruction at an address determined by replacing the low-order 5 bits of Address Register with the following derived sum 5-bit value of literal (J-field) plus value of rotated source data specified by S-field The L-field specifies the length of source data starting from the LSB position and, if less than 8 bits, the remaining bits are filled with zeros, the Program Counter is not incremented and the overflow status (OVF) is not changed	SC	L	L
		WC	L	L
		$\overline{LB}$	L if S = 20_8-27_8	H
		$\overline{RB}$	L if S = 30_8-37_8	H
CLASS = NZT OPCODE = 5 OPERATION = Refer to Description				
Register Immediate  $S = 00_8$-17_8 $J = 000_8$-377_8	If data specified by the S-field is not equal to zero, jump to current page address offset by value of J-field, otherwise, increment the Program Counter If contents of internal register specified by S-field is non-zero, transfer to address determined by replacing the low-order 8 bits of Address Register and Program Counter with "J", otherwise, increment PC	SC	L	L
		WC	L	L
		$\overline{LB}$	H	H
		$\overline{RB}$	H	H

Table 1. FUNCTIONAL DESCRIPTION OF INSTRUCTION SET (Concluded)

INSTRUCTION WORD	DESCRIPTION	STATE OF CONTROL SIGNAL DURING INSTRUCTION CYCLE — SEE FIGURE 3		
		CONTROL SIGNAL	INPUT PHASE	OUTPUT PHASE
CLASS = NZT OPCODE = 5 OPERATION = Refer to Description				
$\overline{IV}$ Bus Immediate (Note) 0 1 2 | 3 4 5 6 7 | 8 9 10 | 11 12 13 14 15 OPCODE | S | L | J S_1 ⋮ S_0 $S = 20_8$-37_8 $J = 00_8$-37_8	If right-rotated and masked IV bus is non-zero, transfer to address determined by replacing low-order 5 bits of Address Register and Program Counter with "J", otherwise, increment PC (The L-field specifies the length of source I/O data starting from the LSB-position and, if less than 8 bits, the remaining bits are filled with zeros)	SC	L	L
		WC	L	L
		$\overline{LB}$	L if $S = 20_8$-27_8	H
		$\overline{RB}$	L if $S = 30_8$-37_8	H
CLASS = XMIT OPCODE = 6 OPERATION = J → D				
XMIT, Register 0 1 2 | 3 4 5 6 7 | 8 9 10 | 11 12 13 14 15 OPCODE | D | J $D = 00_8$-06_8, 11_8, 14_8-16_8 $J = 000_8$-377_8	Store 8-bit value specified by "J" into register specified by "D"	SC	L	L
		WC	L	L
		$\overline{LB}$	H	H
		$\overline{RB}$	H	H
XMIT, $\overline{IV}$ Bus Address 0 1 2 | 3 4 5 6 7 | 8 9 10 | 11 12 13 14 15 OPCODE | D | J $D = 07_8$, 17_8 $J = 000_8$-377_8	Enable I/O device on the bank specified by "D", whose address is the 8-bit integer specified by "J". Address "J" is stored in register "D"	SC	L	H
		WC	L	L
		$\overline{LB}$	H	L if $D = 07_8$
		$\overline{RB}$	H	L if $D = 17_8$
XMIT 8 Bits Immediate, $\overline{IV}$ Bus (Note) 0 1 2 | 3 4 5 6 7 | 8 9 10 | 11 12 13 14 15 OPCODE | D | J $D = 12_8$-13_8 $J = 000_8$-377_8	Store value of 8-bit integer in the previously enabled I/O port, at the bank destination ($\overline{LB}$ or $\overline{RB}$) specified by "D" Contents of R12 or R13 remain unchanged	SC	L	L
		WC	L	H
		$\overline{LB}$	H	L if $D = 12_8$
		$\overline{RB}$	H	L if $D = 13_8$
XMIT Variable Bit Field Immediate, $\overline{IV}$ Bus (Note) 0 1 2 | 3 4 5 6 7 | 8 9 10 | 11 12 13 14 15 OPCODE | D | L | J D_1 ⋮ D_0 $D = 20_8$-37_8 $J = 00_8$-37_8	Transmit Least Significant "L" bits of "J" field to "L-bit" field of $\overline{IV}$ bus specified by "D", if "L" is greated than 5 bits, the MSB bits of destination field is filled with zeros	SC	L	L
		WC	L	H
		$\overline{LB}$	L if $D = 20_8$-27_8	L if $D = 20_8$-27_8
		$\overline{RB}$	L if $D = 30_8$-37_8	L if $D = 30_8$-37_8
CLASS = JMP OPCODE = 7 OPERATION = Refer to Description				
Address Immediate 0 1 2 | 3 4 5 6 7 | 8 9 10 | 11 12 13 14 15 OPCODE | A $A = 00000_8$-17777_8	Jump to address in program storage specified by A-field; this address is loaded into the Address Register and the Program Counter	SC	L	L
		WC	L	L
		$\overline{LB}$	H	H
		$\overline{RB}$	H	H

Note.
S_0 specifies the LSB of rotated input data field
S_1 specifies the bank of $\overline{IV}$ bus from which source data will be input
D_0 specifies bit position in I/O device with which LSB of processed data will be aligned and
D_1 specifies the bank of $\overline{IV}$ bus which will be the destination

Operations Code Field. The 3-bit OPCODE field specifies one of eight classes of 8X305 instructions; octal designations for this field and operands for each instruction class are shown in the preceding table.

Source (S) and Destination (D) Fields. The 5-bit "S" and "D" fields specify the source and destination, respectively, for whatever operation is defined by the OPeration CODE. The "S" and/or "D" fields can specify an internal 8X305 register or any one-to-eight bit field within an I/O device; octal values and source/destination field assignments for all internal registers are shown in Table 2.

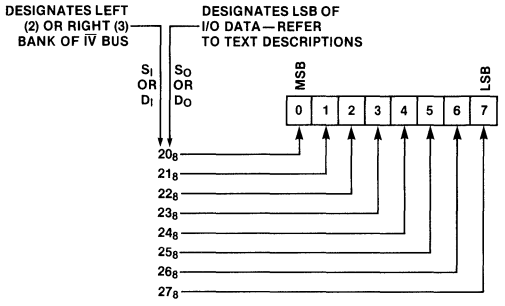
Table 2. OCTAL ADDRESSES AND SOURCE/DESTINATION FIELDS FOR 8X305 REGISTERS

ADDRESS	REGISTER DESIGNATION	SOURCE	DESTI-NATION	ADDRESS	REGISTER DESIGNATION	SOURCE	DESTI-NATION
00_8	R0 (AUX)—General purpose register	X	X	10_8	R10 (OVF—Overflow register)	X	
01_8	R1—General purpose register	X	X	11_8	R11—General purpose register	X	X
02_8	R2—General purpose register	X	X	12_8	R12—General purpose register (Note)	X	X
03_8	R3—General purpose register	X	X	13_8	R13—General purpose register (Note)	X	X
04_8	R4—General purpose register	X	X	14_8	R14—General purpose register	X	X
05_8	R5—General purpose register	X	X	15_8	R15—General purpose register	X	X
06_8	R6—General purpose register	X	X	16_8	R16—General purpose register	X	X
07_8	R7—Special purpose register (refer to next paragraph)	X	X	17_8	R17—Special purpose register (refer to next paragraph)	X	X

Note
R12 and R13 function as general purpose working registers for all operations except transmit (XMIT). During a transmit instruction where R12 or R13 is the destination, the 8-bit "J" field is immediately transferred to the $\overline{IV}$ bus, for this operation, the contents of the designated register remain unchanged

In instructions where $R7_8$ (IVL) or $R17_8$ (IVR) is specified as the destination, the 8-bit value is output on the $\overline{IV}$ bus as an I/O device address or memory location; register R7 selects the Left Bank and register R17 selects the Right Bank. The results are also stored into the specified internal register ($R7_8$ or $R17_8$) and may later be accessed as source data. When the $\overline{IV}$ bus is specified as a source and/or destination, the "S" and "D" fields are split into two parts, that is,

- Source (S) = S_1, S_0 and Destination (D) = D_1, D_0 where,
  S_0 specifies the LSB of rotated input data field
  S_1 specifies the bank of $\overline{IV}$ bus from which source data will be input
  D_0 specifies bit position in I/O device with which LSB of processed data will be aligned and
  D_1 specifies the bank of $\overline{IV}$ bus which will be the destination

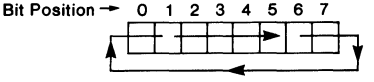


Notes
1 The field length of 0-to-8 bits is specified by the "L" field
2 For the Right Bank, 30_8-37_8 perform equivalent I/O functions

Rotate (R) and Length (L) Field. The 3-bit R/L field performs one of two functions, specifying either the field length (L) for I/O operations or a right-rotate (R) for internal operations. For a given instruction, the specified function depends upon the contents of the Source (S) and Destination (D) fields.

When an internal register is specified by both the source and destination fields, the "R" field is invoked and it specifies a right-rotate of the data specified in the "S" field — see accompanying diagram. The source-register data (up to 8 bits) is right-rotated during the "input phase" of the instruction cycle (Figure 4) and this function is always performed prior to any ALU operation. (*Note: The right-rotate function is implemented on the bus and not in the source register.*)

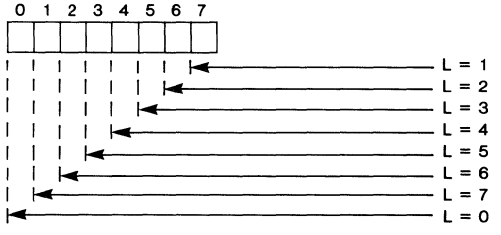
RIGHT-ROTATE FUNCTION



When either or both of the source and destination fields specify a variable-length I/O data field, the "L" field specifies the length of the I/O data field — see following diagram. If the source field specifies an $\overline{IV}$ address (20_8-37_8) and the destination field specifies an internal register (00_8-07_8, 11_8-17_8), the "L" field specifies the length of source data; the source data is formed by right-rotating the $\overline{IV}$ bus data according to the source address and then masking result as specified by the "L" field. If length is less than 8 bits, all remaining bits are set to zero prior to processing data in the ALU. If the source field

specifies an internal register (00_8–17_8) and the destination field specifies $\overline{IV}$ bus data (20_8–37_8), the "L" field specifies the length of the destination data. To form the destination data, the ALU output is left-shifted according to the destination address and then masked to the required length — see $\overline{IV}$ DATA LENGTH SPECIFICATION. The destination data is merged with data in the I/O latches to finalize the $\overline{IV}$ bus data. Hence, a one-to-eight bit destination data field can be inserted into the existing 8-bit I/O port without modifying surrounding bits. If both the source and destination fields specify $\overline{IV}$ bus data (20_8–37_8), the "L" field specifies the length of both the source and destination data.

$\overline{IV}$ DATA LENGTH SPECIFICATION
(No Rotate Function Specified)



To form the source data, the $\overline{IV}$ bus input data is right-rotated according to the source address and then masked to the required length—see $\overline{IV}$ DATA LENGTH SPECIFICATION. If length is less than 8 bits, all remaining bits are set to zero before processing in the ALU. To form the destination data, the ALU output is left-shifted according to the destination address and masked to the required length specification. The destination data is then merged into the $\overline{IV}$ bus data that was used to obtain the source; thus, if the source and destination addresses are on the same bank, the $\overline{IV}$ bus data written to the destination I/O Port appears unmodified, except for bits changed during the shift-and-mask operations. If the source and destination addresses refer to different banks, the destination I/O Port is changed to contain the contents of the source I/O Port in those bit positions not affected by the destination data.

J Field. The 5-bit or 8-bit "J" field is used to load a literal value (contained in the instruction) into a register, into a variable I/O data field, or to modify the low-order bits of the Program Counter. The bit length of the "J" field is implied by the "S" and "L" fields in the XEC, NZT, and XMIT instructions, based on the following conditions:

- When the Source (S) field specifies an internal register, the literal value of the "J" field is an 8-bit binary number.
- When the Source (S) field specifies a variable I/O data field, the literal value of the "J" field is a 5-bit binary number.

A Field. The 13-bit "A" field is an address field which allows the 8X305 to directly branch to any of the 8192 locations in Program Storage memory.

Formation of Instruction Address

The Address Register and Program Counter are used to generate addresses for accessing an instruction from program storage. The instruction address is formed in one of the following ways:

- For all except the JMP, XEC, and a "satisfied" NZT instruction, the Program Counter is incremented by one and placed in the Address Register.
- For the JMP instruction, the 13-bit "A" field contained in the JMP instruction word replaces the contents of both the Address Register and the Program Counter.
- For the XEC instruction, the Address Register is loaded with bits from the Program Counter modified as follows:

  XEC using $\overline{IV}$ Bus Data — low-order 5 bits of ALU output replaces counterpart bits in Address Register

  XEC using Data from Internal Register — low-order 8 bits of ALU output replaces counterpart bits in Address Register

  The Program Counter is not modified for either of the above conditions.
- For a "satisfied" NZT instruction, the low-order 5 bits (NZT source is $\overline{IV}$ bus data) or low-order 8 bits (NZT source is an internal register) of both the Address Register and Program Counter are loaded with the literal value specified by the "J" field of instruction word.

Data Addressing

The source and/or destination addresses of the data to be operated upon are specified as part of the instruction word. As shown earlier, source/destination addresses are specified using a 5-bit code (00_8–37_8). When the most significant octal digit is a "0" or "1", the source and/or destination address is an internal register; if the most significant digit is a 2 or 3, an $\overline{IV}$ bus operation is indicated — 2 specifying a Left-Bank ($\overline{LB}$) operation and 3 specifying a Right-Bank ($\overline{RB}$) operation. The least significant octal digit (0 through 7) indicates either a specific internal register address or positioning information for the least significant bit when specifying $\overline{IV}$ bus data. Referring to Table 1, AUXiliary register R0 (00_8) is the implied source

of the second argument for the ADD, AND, and XOR operations. IVL register R7 and IVR register R17 (destination addresses 07_8 and 17_8, respectively) provide a means of routing enabling address information to I/O peripherals. With IVL or IVR specified as the destination address, data is placed on the $\overline{IV}$ bus during the output phase of the instruction cycle; simultaneously, a Select Command (SC) is generated to inform all I/O devices that information on the $\overline{IV}$ bus is to be considered as an I/O address. Since the contents of IVL and IVR are preserved, either register may later be accessed as a source of data.

Control outputs $\overline{LB}$ and $\overline{RB}$ are used to partition I/O bus devices into two fields of 256 addresses. With $\overline{LB}$ in the active-low state and a source address of 20_8–27_8, the left bank of I/O devices are enabled during the input phase of the instruction cycle. With $\overline{RB}$ in the active-low state and a source address of 30_8–37_8, the right bank of devices are enabled. During the output phase, $\overline{LB}$ is low if the destination address is 07_8 or 20_8–27_8, whereas $\overline{RB}$ is low if the destination address is 17_8 or 30_8–37_8. Each address field ($\overline{LB}$ and $\overline{RB}$) can have a different I/O device selected, that is, data can be transferred from a device in one bank to a device in the other in one instruction cycle.

3

DESIGN PARAMETERS

Hardware design of an 8X305-based system largely consists of the following operations:

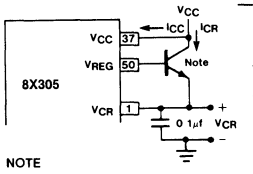
- Selecting and interfacing a Program Storage device — ROM, PROM, etc.
- Selecting and interfacing input/output devices — RAM, Ports, and other 8-bit addressable I/O devices.
- Choosing and implementing System Clock — Capacitor-Controlled, Crystal-Controlled, or Externally-Driven.
- Selection of an off-chip series-pass transistor.

All information required for easy implementation of these design requirements is provided under the following captions:

- Ordering Information
- Voltage Regulator
- DC Characteristics
- AC Characteristics
- Timing Considerations
- Clock Considerations
- $\overline{HALT}/\overline{RESET}$ Logic

VOLTAGE REGULATOR

All internal logic of the 8X305 is powered by an on-chip voltage regulator that requires an external series-pass transistor. Electrical specifications for the off-chip power transistor and a typical hook-up are shown in the accompanying diagram. To minimize lead inductance, the transistor should be as close as possible to the 8X305 package and the emitter should be ac-grounded via a 0.1 microfarad ceramic capacitor.



NOTE
Typical approved parts—2N5320, 2N5337

PARAMETER	CONDITIONS	LIMITS
h_{fe}	V_{CE} = 2V; 100mA < I_C < 500mA	> 50
VBE_{ON}	V_{CE} = 5V; I_C = 500mA	< 1V
V_{CESAT}	I_C = 500mA; I_B = 50mA	< 0.5V
BV_{CEO}		> 15V
f_t		> 30MHz

DC CHARACTERISTICS (Commercial Part) $4.75V \leq V_{CC} \leq 5.25V$, $0°C \leq T_A \leq 70°C$

ABSOLUTE MAXIMUM RATINGS

Storage Temperature (T_{STG}) ratings are from -65 to $+150°C$

PIN	DESCRIPTION	RATING	UNIT	PIN	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V	All other pins	Logic input voltage	5.5	V
X1, X2	Crystal input voltage	2.0	V				

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT	COMMENTS
V_{CC}	Supply voltage		4.75	5.0	5.25	V	
V_{IH}	High level input voltage		0.6 2.0		2.0 5.5	V	X1 and X2 All other pins
V_{IL}	Low level input voltage				0.4 0.8	V	X1 and X2 All other pins
V_{OH}	High level output voltage	V_{CC} = min; $I_{OH} = -3mA$	2.4			V	
V_{OL}	Low level output voltage	V_{CC} = min; $I_{OL} = 6mA$ V_{CC} = min; $I_{OL} = 16mA$			0.55 0.55	V	A_0 through A_{12} All other outputs
V_{CR}	Regulator voltage	$V_{CC} = 5V$		3.1 2.9		V	$T_A = 0°C$ $T_A = 70°C$
V_{IC}	Input clamp voltage	V_{CC} = min; $I_{IN} = -10mA$			−1.5	V	Crystal inputs X1 and X2 do not have internal clamp diodes
I_{IH}	High level input current	V_{CC} = max; $V_{IH} = 0.6V$ $V_{IH} = 4.5V$			4.0 50	mA μA	X1 and X2 All other pins
I_{IL}	Low-level input current	V_{CC} = max; $V_{IL} = 0.4V$			−3 −0.2 −1.6 −0.4	mA	X1 and X2 $\overline{IV0}$–$\overline{IV7}$ I0–I15 $\overline{HALT}$ and $\overline{RESET}$
I_{OS}	Short circuit output current	V_{CC} = max; (Note: At any time, no more than one output should be connected to ground.)	−30		−140	mA	All output pins
I_{CC}	Supply current	V_{CC} = max			180 195	mA	$T_A = 70°C$ $T_A = 0°C$
I_{REG}	Regulator control	$V_{CC} = 5.0V$	−10		−25	mA	Max available base drive for series-pass transistor
I_{CR}	Regulator current	V_{CC} = max			200 230	mA	$T_A = 70°C$ $T_A = 0°C$

Notes.
1 Operating temperature ranges are guaranteed after thermal equilibrium has been reached
2 All voltages measured with respect to ground terminal

AC CHARACTERISTICS (Commercial Part) CONDITIONS: $4.75V \leq V_{CC} \leq 5.25V$; $0°C \leq T_A \leq 70°C$

LOADING: (See test circuits)

PARAMETER (Note 1)		LIMITS (INSTRUCTION CYCLE TIME = 200ns) Min	Typ	Max	LIMITS (INSTRUCTION CYCLE TIME > 200ns) Min	Typ	Max	UNITS	COMMENTS
T_{PC}	Processor cycle time	200			200			ns	
T_{CP}	X1 clock period	100			100			ns	
T_{CH}	X1 clock high time	50			50			ns	
T_{CL}	X1 clock low time	50			50			ns	
T_{MCL}	MCLK low delay	15		40	15		40	ns	
T_W	MCLK pulse width	40		60	$T_{4Q} - 10$		$T_{4Q} + 10$	ns	Note 2
T_{MODO}	Output driver turn on time MCLK falling edge	125		145	$T_{1Q} + T_{2Q} + 25$		$T_{1Q} + T_{2Q} + 45$	ns	Note 9

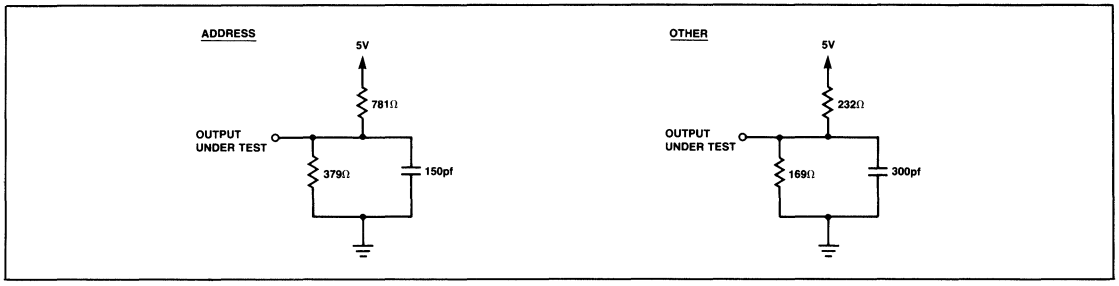
AC CHARACTERISTICS (Commercial Part) (Continued)

CONDITIONS: $4.75V \le V_{CC} \le 5.25V$; $0°C \le T_A \le 70°C$
LOADING: (See test circuits)

PARAMETER (Note 1)		LIMITS (INSTRUCTION CYCLE TIME = 200ns)			LIMITS (INSTRUCTION) CYCLE TIME > 200ns)			UNITS	COMMENTS
		Min	Typ	Max	Min	Typ	Max		
T_{DI}	Output driver turn-on time (SC/WC rising edge)	20			20			ns	Note 10
T_{DD}	Input data to output data	85		105	85		105	ns	
T_{MHS}	MCLK falling edge to $\overline{HALT}$ falling edge			30			$T_{1Q} - 20$	ns	Note 2
T_{MHH}	$\overline{HALT}$ hold time (MCLK falling edge)	65			$T_{1Q} + 15$			ns	Note 2
T_{ACC}	Program storage access time			60				ns	
T_{IO}	I/O port output enable time ($\overline{LR}/\overline{RB}$ to valide $\overline{IV}$ data input)			30				ns	
T_{MAS}	MCLK falling edge to address stable			140			$T_{1Q} + T_{2Q} + 40$	ns	Notes 2, 3 & 4
T_{IA}	Instruction to address			140			$T_{2Q} + 90$	ns	Notes 2, 3 & 5
T_{IVA}	Input data to address			85			85	ns	Notes 3 & 6
T_{MIS}	MCLK falling edge to instruction stable			30			$T_{1Q} - 20$	ns	Notes 2 & 10
T_{MIH}	Instruction hold time (MCLK falling edge)	55			$T_{1Q} + 5$			ns	Notes 2 & 8
T_{MWH}	MCLK falling edge to SC/WC rising edge	105		125	$T_{1Q} + T_{2Q} + 5$		$T_{1Q} + T_{2Q} + 25$	ns	Note 2
T_{MWL}	MCLK falling edge to SC/WC falling edge	5		15	5		15	ns	
T_{MIBS}	MCLK falling edge to $\overline{LB}/\overline{RB}$ (Input phase)	10		25	10		25	ns	
T_{IIBS}	Instruction to $\overline{LB}/\overline{RB}$ (Input phase)			25			25	ns	
T_{MOBS}	MCLK falling edge to $\overline{LB}/\overline{RB}$ (Output phase)	115		145	$T_{1Q} + T_{2Q} + 15$		$T_{1Q} + T_{2Q} + 45$	ns	Note 2
T_{MIDS}	MCLK falling edge to input data stable			55			$T_{1Q} + T_{2Q} - 45$	ns	Note 2
T_{MIDH}	Input data hold time (MCLK falling edge)	115			$T_{1Q} + T_{2Q} + 15$			ns	Note 2
T_{MODH}	Output data hold time (MCLK falling edge)	11			11			ns	
T_{MODS}	Output data stable (MCLK falling edge)	130		150	$T_{1Q} + T_{2Q} + 30$		$T_{1Q} + T_{2Q} + 50$	ns	Note 2

NOTES
1. X1 and X2 inputs are driven by an external pulse generator with an amplitude of 1 5 volts, all timing parameters are measured at this voltage level
2. Respectively, T_{1Q}, T_{2Q}, T_{3Q}, and T_{4Q} represent time intervals for the first, second, third, and fourth quarter cycles
3. Capacitive loading for the address bus is 150 picofarads
4. T_{MAS} is obtained by forcing a valid instruction and an I/O bus input to occur earlier than the specified minimum set up time
5. T_{IA} is obtained by forcing a valid instruction input to occur earlier than the minimum set up time
6. T_{IVA} is obtained by forcing a valid I/O bus input to meet the minium set up time
7. T_{MIS} represents the setup time required by internal latches of the 8X305 In system applications, the instruction input may have to be valid before the worst-case set up time in order for the system to respond with a valid I/O bus input that meets the I/O bus input set up time (T_{IDS} and T_{MIDS})
8. T_{MIH} represents the hold time required by internal latches of the 8X305 To generate proper $\overline{LB}/\overline{RB}$ signals, the instruction must be held valid until the address bus changes
9. The minimum figure for these parameters represents the earliest time that I/O bus output drivers of the 8X305 will turn on
10. This parameter represents the latest time that the output drivers of the input device should be turned off

TEST CIRCUITS



ABSOLUTE MAXIMUM RATINGS

Storage Temperature (T_{STG}) ratings are from −65 to +150°C

PIN	DESCRIPTION	RATING	UNIT	PIN	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V	All other pins	Logic input pins	5.5	V
X1, X2	Crystal input voltage	2.0	V				

DC CHARACTERISTICS (Military Part)

$4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_C \leq +125°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT	COMMENTS
			Min	Typ	Max		
V_{CC}	Supply voltage		4.5	5.0	5.5	V	
V_{IH}	High level input voltage		0.6 2.0		2.0	V	X1 and X2 All other pins
V_{IL}	Low level input voltage				0.4 0.8	V	X1 and X2 All other pins
V_{OH}	High level output voltage	V_{CC} = min; I_{OH} = −3mA	2.4			V	
V_{OL}	Low level output voltage	V_{CC} = min; I_{OL} = 6mA V_{CC} = min; I_{OL} = 16mA			0.55 0.55	V	A_0 through A_{12} All other outputs
V_{CR}	Regulator voltage	V_{CC} = 5V		3.5 3.1 2.6		V	T_C = −55°C T_C = 0°C T_C = 125°C
V_{IC}	Input clamp voltage	V_{CC} = min; I_{IN} = −10mA			−1.5	V	Crystal inputs X1 and X2 do not have internal clamp diodes.
I_{IH}	High level input current	V_{CC} = max; V_{IH} = 0.6V V_{IH} = 4.5V			4.0 50	mA μA	X1 and X2 All other pins
I_{IL}	Low-level input current	V_{CC} = max; V_{IL} = 0.4V			−3 −0.3 −1.6 −0.4	mA	X1 and X2 $\overline{IV0}$–$\overline{IV7}$ I0–I15 $\overline{HALT}$ and $\overline{RESET}$
I_{OS}	Short circuit output current	V_{CC} = max; (Note: At any time, no more than one output should be connected to ground.)	−30		−140	mA	All output pins
I_{CC}	Supply current	V_{CC} = max			175 205	mA	T_C = 125°C T_C = −55°C
I_{REG}	Regulator control	V_{CC} = 5.0V	−10		−25	mA	Max available base drive for series-pass transistor
I_{CR}	Regulator current	V_{CC} = max			180 260	mA	T_C = 125°C T_C = −55°C

NOTES
1. Operating temperature ranges are guaranteed after thermal equilibrium has been reached.
2. All voltages measured with respect to ground terminal.

AC CHARACTERISTICS (Military Part)

CONDITIONS: $4.5V \leq V_{CC} \leq 5.5V$; $-55°C \leq T_C \leq 125°C$
LOADING: (See test circuits)

PARAMETER (Note 1)		LIMITS (INSTRUCTION CYCLE TIME = 250ns)			LIMITS (INSTRUCTION) CYCLE TIME > 250ns)			UNITS	COMMENTS
		Min	Typ	Max	Min	Typ	Max		
T_{PC}	Processor cycle time	250			250			ns	
T_{CP}	X1 clock period	125			125			ns	
T_{CH}	X1 clock high time	62			62			ns	
T_{CL}	X1 clock low time	62			62			ns	
T_{MCL}	MCLK low delay	15		40	15		40	ns	
T_W	MCLK pulse width	47		72	$T_{4Q} - 15$		$T_{4Q} + 10$	ns	Note 2
T_{MODO}	Output driver turn-on time (MCLK falling edge)	145		175	$T_{1Q} + T_{2Q} + 20$		$T_{1Q} + T_{2Q} + 50$	ns	Note 9
T_{DI}	Output driver turn-on time (SC/WC rising edge)	20			20			ns	Note 10
T_{DD}	Input data to output data	80		115	80		115	ns	
T_{MHS}	MCLK falling edge to $\overline{HALT}$ falling edge			40			$T_{1Q} - 22$	ns	Note 2
T_{MHH}	$\overline{HALT}$ hold time (MCLK falling edge)	80			$T_{1Q} + 18$			ns	Note 2
T_{ACC}	Program storage access time			90				ns	
T_{IO}	I/O port output enable time ($\overline{LB}/\overline{RB}$ to valid $\overline{IV}$ data input)			40				ns	
T_{MAS}	MCLK falling edge to address stable			160			$T_{1Q} + T_{2Q} + 35$	ns	Notes 2, 3 & 4
T_{IA}	Instruction to address			160			$T_{2Q} + 98$	ns	Notes 2, 3 & 5
T_{IVA}	Input data to address			90			90	ns	Notes 3 & 6
T_{MIS}	MCLK falling edge to instruction stable			40			$T_{1Q} - 22$	ns	Notes 2 & 10
T_{MIH}	Instruction hold time (MCLK falling edge)	70			$T_{1Q} + 8$			ns	Notes 2 & 8
T_{MWH}	MCLK falling edge to SC/WC rising edge	127		154	$T_{1Q} + T_{2Q} + 2$		$T_{1Q} + T_{2Q} + 29$	ns	Note 2
T_{MWL}	MCLK falling edge to SC/WC falling edge	5		25	5		25	ns	
T_{MIBS}	MCLK falling edge to $\overline{LB}/\overline{RB}$ (Input phase)	10		35	10		35	ns	
T_{IIBS}	Instruction to $\overline{LB}/\overline{RB}$ (Input phase)			30			30	ns	
T_{MOBS}	MCLK falling edge to $\overline{LB}/\overline{RB}$ (Output phase)	140		170	$T_{1Q} + T_{2Q} + 15$		$T_{1Q} + T_{2Q} + 45$	ns	Note 2
T_{MIDS}	MCLK faling edge to input data stable			75			$T_{1Q} + T_{2Q} - 50$	ns	Note 2
T_{MIDH}	Input data hold time (MCLK falling edge)	140			$T_{1Q} + T_{2Q} + 15$			ns	Note 2
T_{MODH}	Output data hold time (MCLK falling edge)	11			11			ns	
T_{MODS}	Output data stable (MCLK falling edge)	150		180	$T_{1Q} + T_{2Q} + 25$		$T_{1Q} + T_{2Q} + 55$	ns	Note 2

NOTES
1. X1 and X2 inputs are driven by an external pulse generator with an amplitude of 1.5 volts, all timing parameters are measured at this voltage level.
2. Respectively, T_{1Q}, T_{2Q}, T_{3Q}, and T_{4Q} represent time intervals for the first, second, third, and fourth quarter cycles.
3. Capacitive loading for the address bus is 150 picofarads.
4. T_{MAS} is obtained by forcing a valid instruction and an I/O bus input to occur earlier than the specified minimum set up time.
5. T_{IA} is obtained by forcing a valid instruction input to occur earlier than the minimum set up time.
6. T_{IVA} is obtained by forcing a valid I/O bus input to meet the minium set up time
7. T_{MIS} represents the setup time required by internal latches of the 8X305. In system applications, the instruction input may have to be valid before the worst-case set up time in order for the system to respond with a valid I/O bus input that meets the I/O bus input set up time (T_{IDS} and T_{MIDS})
8. T_{MIH} represents the hold time required by internal latches of the 8X305. To generate proper $\overline{LB}/\overline{RB}$ signals, the instruction must be held valid until the address bus changes
9. The minimum figure for these parameters represents the earliest time that I/O bus output drivers of the 8X305 will turn on.
10. This parameter represents the latest time that the output drivers of the input device should be turned off.

TIMING CONSIDERATIONS (Commercial Part)

As shown in the AC CHARACTERISTICS table for the commercial part, the minimum instruction cycle time is 200 nanoseconds; whereas, the maximum is determined by the on-chip oscillator frequency and can be any value the user chooses. With an instruction cycle time of 200 nanoseconds, the part can be characterized in terms of absolute values; these are shown in the first "LIMITS" column of the table. When the instruction cycle time is greater than 200 nanoseconds, certain parameters are cycle-time dependent; thus, these parameters are specified in terms of the four quarter cycles (T_{1Q}, T_{2Q}, T_{3Q}, and T_{4Q}) that make up one instruction cycle — see 8X305 TIMING DIAGRAM. As the time interval for each instruction cycle increases (becomes greater than 200 nanoseconds), the delay for all parameters that are cycle-time dependent is likewise increased. In some cases, these delays have a significant impact on timing relationships and other areas of systems design; subsequent paragraphs describe these timing parameters and reliable methods of calculation.

Timing parameters for the 8X305 are normally measured with reference to MCLK.

System determinants for the instruction cycle time are:

- Propagation delays within the 8X305
- Access time of Program Storage
- Enable time of the I/O port

Normally, the instruction cycle time is constrained by one or more of the following conditions:

Condition 1 — Instruction or MCLK to $\overline{LB}/\overline{RB}$ (input phase) plus I/O port access time (TIO) ≤ $\overline{IV}$ data set up time (Figure 5a).

Condition 2 — Program storage access time (TACC) plus instruction to $\overline{LB}/\overline{RB}$ (input phase) plus I/O port access time (TIO) plus $\overline{IV}$ data (input phase) to address ≤ instruction cycle time (Figure 5b).

Condition 3 — Program storage access time plus instruction to address ≤ instruction cycle time (Figure 5c).

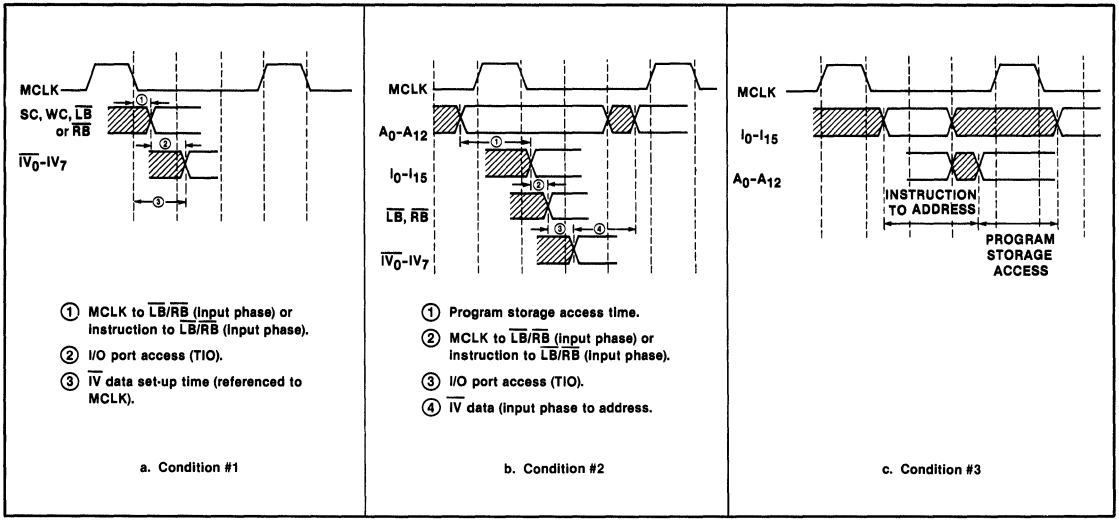
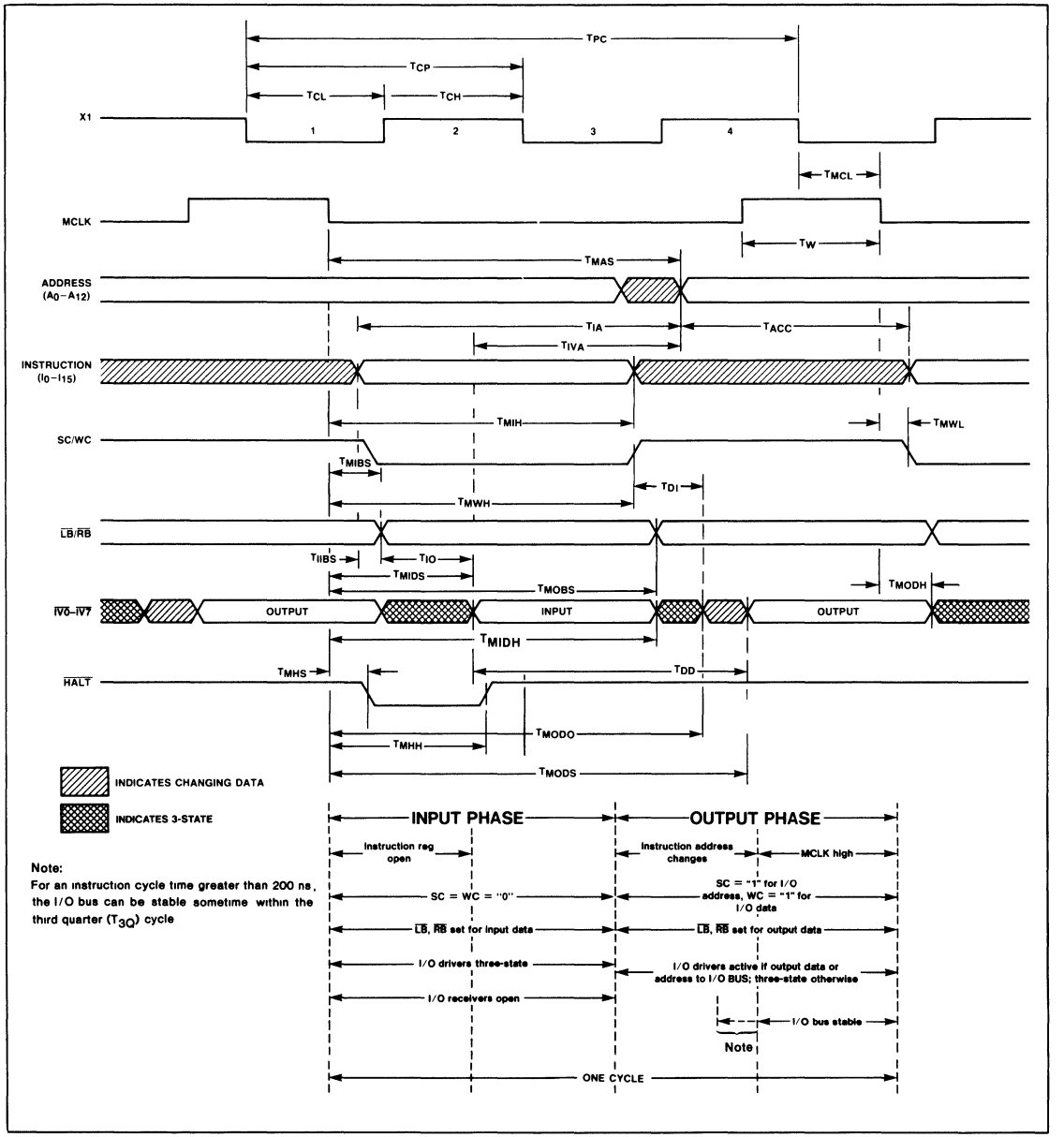


Figure 5. Constraints of 8X305 Instruction Cycle Time

8X305 TIMING DIAGRAM



Note:
For an instruction cycle time greater than 200 ns, the I/O bus can be stable sometime within the third quarter (T_{3Q}) cycle

From condition #1 and with an instruction cycle time of 200ns, the I/O port access time (TIO) can be calculated as follows:

$$TMIBS + TIO \leq TMIDS$$
transposing, $TIO \leq TMIDS = TMIBS$
substituting, $TIO \leq 55ns - 25ns$
result, $TIO \leq 30ns$

Using 30ns for TIO, the constraint imposed by condition #1 can also be used to calculate the minimum cycle time:

$$TMIBS + TIO \leq TMIDS$$
thus, $25ns + 30ns \leq T_{1Q} + T_{2Q} - 45$
$25ns + 30ns \leq 1/2$ cycle $- 45$ therefore,

the worst-case instruction cycle time is 200ns. With subject parameters referenced to X1, the same calculations are valid:

$$TIBS + TIO + TIDS \leq 1/2 \text{ cycle}$$
thus, $45ns + 30ns + 25ns \leq 1/2$ cycle therefore,

the worst-case instruction cycle time is again 200ns. From condition #2 and with an instruction cycle time of 200ns, the program storage access time can be calculated:

$$TACC + TIIBS + TIO + TIVA \leq 200ns$$
transposing, $TACC \leq 200ns - TIIBS - TIO - TIVA$
substituting, $TACC \leq 200ns - 25ns - 30ns - 85ns$
thus, $TACC \leq 60ns$ hence, for an instruction cycle time of 200ns, a program storage access time of 60ns is implied. The constraint imposed by condition #3 can be used to verify the maximum program storage access time:

$$TIA + TACC \leq \text{Instruction Cycle}$$
thus, $TACC \leq 200ns - 140ns$
and, $TACC \leq 60ns$, confirming that a program storage access time of 60ns is satisfactory.

For an instruction cycle time of 200ns and a program storage access time of 60ns (Condition #2/Figure 5b), the instruction should be valid at the falling edge of MCLK. This relationship can be derived by the following equation:

$$200ns - TMAS - TACC$$
$$= 200ns - 140ns - 60ns$$
$$= 0ns$$

It is important to note that, during the input phase, the beginning of a valid $\overline{LB}/\overline{RB}$ signal is determined by either the instruction to $\overline{LB}/\overline{RB}$ delay (TIIBS) or the delay from the falling edge of MCLK to $\overline{LB}/\overline{RB}$ (TMIBS). Assuming the instruction is valid at the falling edge of MCLK and adding the instruction-to-$\overline{LB}/\overline{RB}$ delay (TIIBS = 25ns), the $\overline{LB}/\overline{RB}$ signal will be valid 25ns after the falling edge of MCLK. With a fast program storage memory and with a valid instruction before the falling edge of MCLK — the $\overline{LB}/\overline{RB}$ signal will, due to the TMIBS delay, still be valid 25ns after the falling edge of MCLK. Using a worst-case instruction cycle time of 200ns, the user cannot gain a speed advantage by selecting a memory with faster access time. Under the same conditions, a speed advantage cannot be obtained by using an I/O port with fast access time (TIO) because the address bus will be stable 55ns (TAS) after the beginning of the third quarter cycle — no matter how early the $\overline{IV}$ data input is valid.

CLOCK CONSIDERATIONS

The on-chip oscillator and timing-generation circuits of the 8X305 can be controlled by any one of the following methods:

Capacitor — if timing is not critical
Crystal — if precise timing is required
External Drive — if application requires that the 8X305 be driven from a system clock

Capacitor Timing. A non-polarized ceramic or mica capacitor with a working voltage equal to or greater than 25 volts is recommended. The lead lengths of capacitor should be approximately the same and as short as possible; also, the timing circuits should not be in close proximity to external sources of noise. For various capacitor (C_X) values, the cycle time can be approximated as:

C_X (in pF)	APPROXIMATE CYCLE TIME
100	300ns
200	500ns
500	1.1μs
1000	2.0μs

Crystal Timing. When a crystal is used, the on-chip oscillator operates at the resonant frequency (f_o) of the crystal; the series-resonant quartz crystal connects to the 8X305 via pins 10 (X1) and 11 (X2). The lead lengths of the crystal should be approximately equal and as short as possible; also, the timing circuits should not be in close proximity to external sources of noise. The crystal should be hermetically sealed (HC type can) and have the following electrical characteristics:

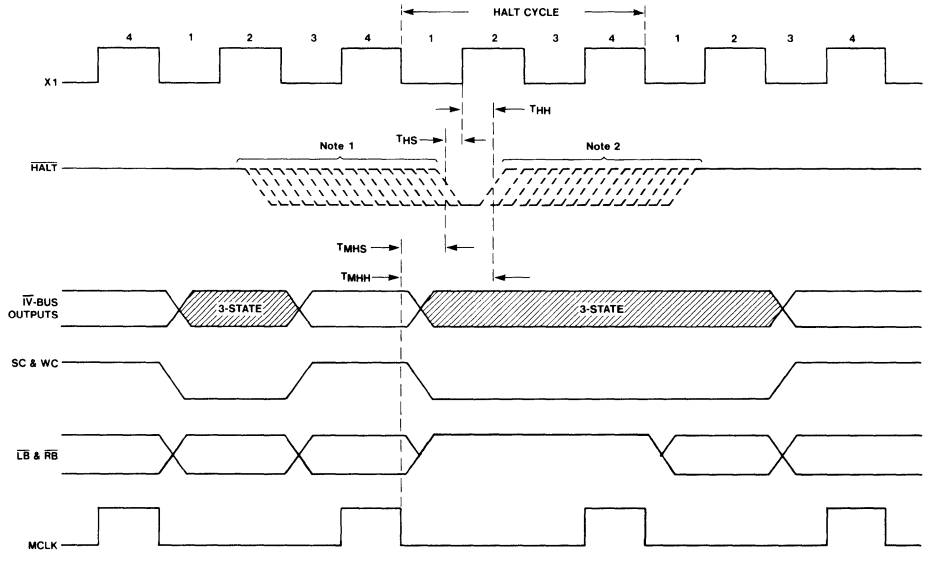
Type — Fundamental mode, series resonant
Impedance at Fundamental — 35 ohms maximum
Impedance at Harmonics and Spurs — 50 ohms minimum

The resonant frequency (f_o) of the crystal is related to the desired cycle time (T) by the equation: $f_o = 2/T$; thus, for a cycle time of 200 nanoseconds, $f_o = 10MHz$.

$\overline{HALT}$ Logic

The $\overline{HALT}$ signal is sampled via internal chip logic at the end of the first internal quarter of each instruction cycle. If, when sampled, the $\overline{HALT}$ signal is active-low, a halt is immediately executed and the current instruction cycle is terminated; however, the halt cycle does not inhibit MCLK nor does it affect any internal registers of the 8X305. As long as the $\overline{HALT}$ line is active-low, the SC and WC lines are low (inactive), the Left Bank ($\overline{LB}$)/Right Bank ($\overline{RB}$) signals are high (inactive), and the $\overline{IV}$ bus remains in the three-state mode of operation. Normal operation resumes at the next cycle in which $\overline{HALT}$ is high when sampled — see $\overline{HALT}$ TIMING DIAGRAM.

HALT TIMING DIAGRAM



Notes.

1. The $\overline{HALT}$ signal can switch from High to Low at any time during this interval.
2. The $\overline{HALT}$ signal can switch from Low to High at any time during this interval

Timing Descriptions.

T_{HS}—set-up time from $\overline{HALT}$ to X1 (independent of instruction cycle time)

T_{HH}—hold time from X1 to $\overline{HALT}$ (independent of instruction cycle time)

T_{MHS}—set-up time from MCLK to $\overline{HALT}$ (dependent upon instruction cycle time)

T_{MHH}—hold time from MCLK to $\overline{HALT}$ (dependent upon instruction cycle time)

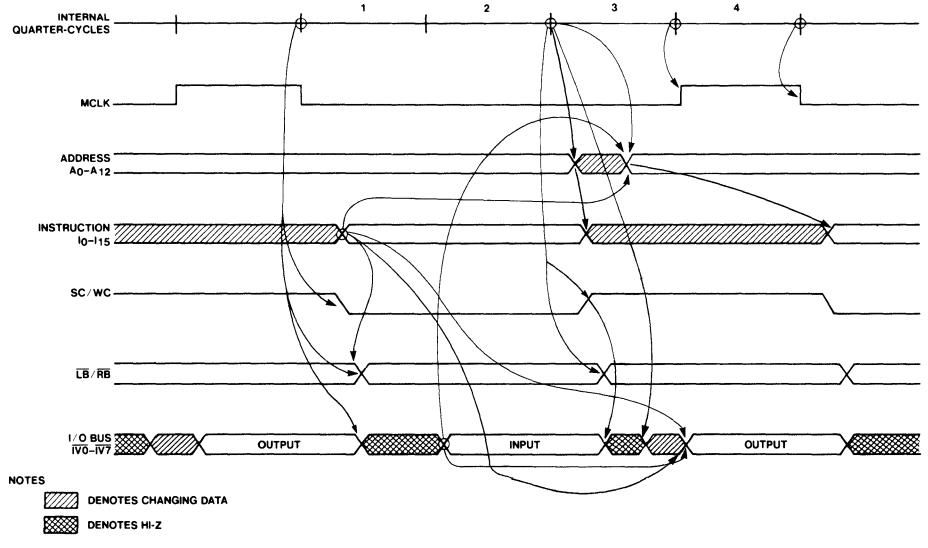


Figure 7. Timing Relationships of 8X305 I/O Signals

Using an External Clock. The 8X305 can be synchronized with an external clock by simply connecting appropriate drive circuits to the X1/X2 inputs. Figure 8 shows how the on-chip oscillator can be driven from the complementary outputs of a pulse generator. In applications where the MicroController must be driven from a master clock, the X1/X2 lines can be interfaced to TTL logic as shown in Figure 9.

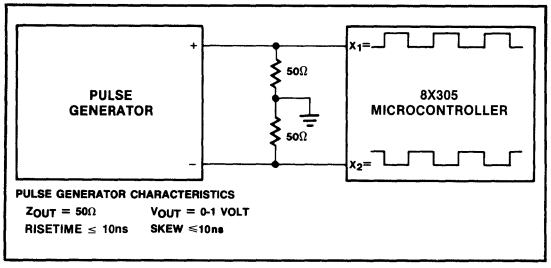


Figure 8. Clocking with a Pulse Generator

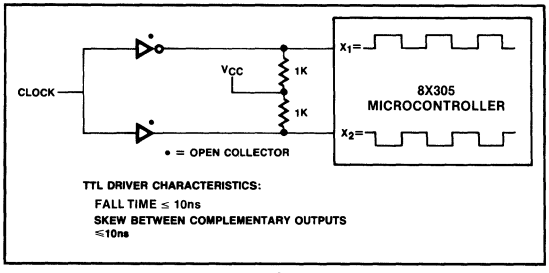


Figure 9. Clocking with TTL

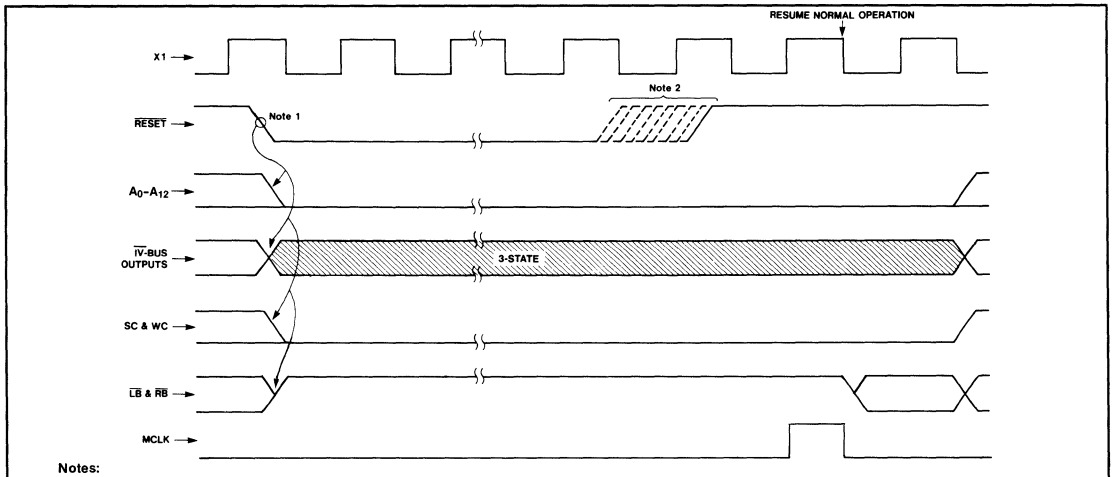
RESET Logic

RESET (pin 43) can be driven from a high (inactive) state to a low (active) state at any time with respect to the system clock, that is, the reset function is asynchronous. To ensure proper operation, RESET must be held low (active) for one full instruction time. When the line is driven from a high state to an active-low state, several events occur — the precise instant of occurrence is basically a function of the propagation delay for that particular event. As shown in the RESET TIMING DIAGRAM, these events are:

- The Program Counter and Address Register are set to address zero and remain in that state as long as the RESET line is low. Other than PC and AR, RESET does not affect other internal registers.
- The input/output (IV) bus goes three-state and remains in that condition as long as the RESET line is low.
- The Select Command and Write Command signals are driven low and remain low as long as the RESET line is low.
- The Left Bank/Right Bank (LB/RB) signals are forced high asynchronously for the period in which the RESET line is low.

During the time RESET is active-low, MCLK is inhibited; moreover, if the RESET line is driven low during the last two quarter cycles, MCLK may be shortened for that particular machine cycle. When RESET line is driven high (inactive)—one quarter to one full instruction cycle later, MCLK appears just before normal operation is resumed. The RESET/MCLK relationship is clearly shown by "B" in the timing diagram. As long as the RESET line is active-low, the HALT signal (described next) is not sampled by internal logic of the 8X305.

RESET TIMING DIAGRAM



Notes:
1 A High to Low transition of the RESET signal will force the Address Bus to an all-zero configuration
2 The RESET signal can switch from Low to High at any point within this time interval and, in all cases, MCLK will occur at least one-quarter cycle time later as shown

8-BIT LATCHED BIDIRECTIONAL I/O PORT 8T31

FEATURES

- **Dual bidirectional ports**
- **Independent port operation (User-port priority for data entry)**
- **User data input synchronous**
- **At power-up, User-port outputs are high and Microprocessor-port outputs are high-Z**
- **Three-state TTL outputs for high-drive capabilities**
- **Directly compatible with 8X300 Microcontroller**
- **Single +5V supply**

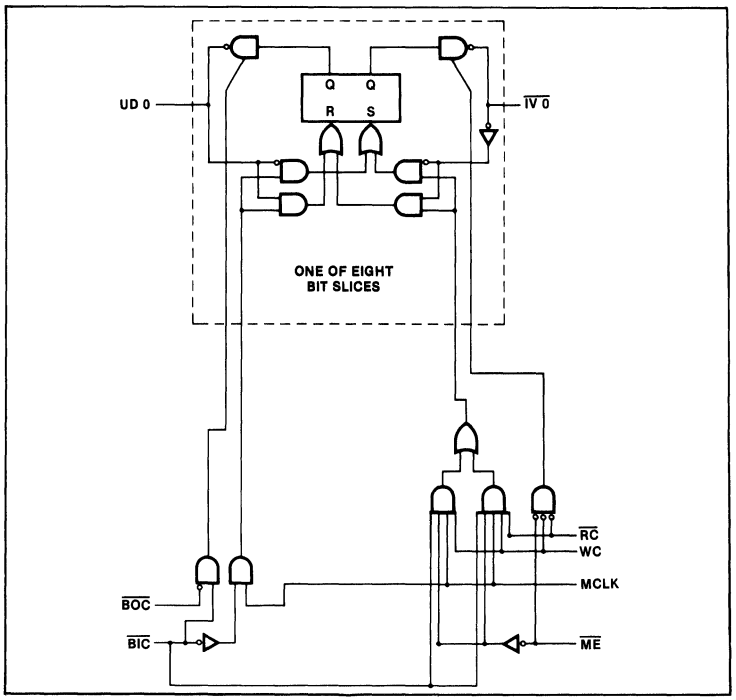
PRODUCT DESCRIPTION

The 8T31 is an 8-bit bidirectional data register designed to function as Input/Output interface elements in microprocessor systems.

Each part contains eight clocked data latches that are accessible from either a *microprocessor* port or a *user* port. Separate I/O control is provided for each port. The two ports operate independently, except that when both are attempting to input data into the data latches, the User port (UD0-UD7) has priority. The master enable (ME) signal enables or disables the microprocessor bus regardless of the state of the other inputs but has no effect on the user bus.

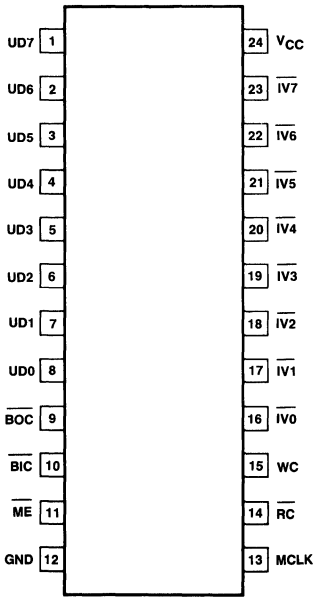
A unique feature of these parts is their ability to start up in a predetermined state. If the clock is maintained at a level of less than 0.8 volts until the power supply reaches 3.5 volts, all bits of the user port will wakeup at a "logic 1" level and those of the microprocessor port will wakeup in the high-impedance state

LOGIC DIAGRAM



PIN CONFIGURATION

N PACKAGE



TOP VIEW

ORDER NUMBERS

N8T31N, N8X31N

8-BIT LATCHED BIDIRECTIONAL I/O PORT 8T31

PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-8	UD0-UD7	User Data I/O Lines. Bidirectional data lines to communicate with user's equipment	Acitve high three-state
16-23	$\overline{IV0}$-$\overline{IV7}$	Microprocessor Bus. Bidirectional data lines to communicate with controlling digital system.	Active low three-state
10	$\overline{BIC}$:	Input Control. User input to control writing into the I/O Port from the user data lines.	Active low
9	$\overline{BOC}$.	Output Control. User input to control reading from the I/O Port onto the user data lines.	Active low
11	$\overline{ME}$:	Master Enable. System input to enable or disable all other system inputs and outputs. It has no effect on user inputs and outputs.	Active low
15	WC:	Write Command. When WC is high, stores contents of $\overline{IV0}$-$\overline{IV7}$ as data.	Active high
14	$\overline{RC}$	Read Command. When RC is low, data is presented on $\overline{IV0}$-$\overline{IV7}$.	Active low
13	MCLK	Master Clock. Input to strobe data into the latches. See function tables for details	Active high
24	V_{CC}	5V power connection.	
12	GND:	Ground	

Table 1. USER PORT CONTROL FUNCTION

$\overline{BIC}$	$\overline{BOC}$	MCLK	USER DATA BUS FUNCTION
H	L	X	Output Data
L	X	H	Input Data
H	H	X	Inactive

H = High Level L = Low Level X = Don't care

Table 2. MICROPROCESSOR PORT CONTROL FUNCTION

$\overline{ME}$	$\overline{RC}$	WC	MCLK	$\overline{BIC}$	MICROPROCESSOR BUS FUNCTION
L	L	L	X	X	Output Data
L	X	H	H	H	Input Data
X	H	L	X	X	Inactive
X	X	H	X	L	Inactive
H	X	X	X	X	Inactive

USER DATA BUS CONTROL

The activity of the user data bus is controlled by the $\overline{BIC}$ and $\overline{BOC}$ inputs as shown in Table 1.

The user data input is a synchronous function with MCLK. A low level on the $\overline{BIC}$ input allows data on the user data bus to be written into the data latches only if MCLK is at a high level. A low level on the BIC input allows data on the user data bus to be latched regardless of the level of the MCLK input.

To avoid conflicts at the data latches, input from the microprocessor port is inhibited when BIC is at a low level. Under all other conditions the 2 ports operate independently.

MICROPROCESSOR BUS CONTROL

As is shown in Table 2, the activity of the microprocessor port is controlled by the $\overline{ME}$, RC, WC and $\overline{BIC}$ inputs, as well as the state of an internal status latch. $\overline{BIC}$ is included to show user port priority over the microprocessor port for data input.

BUS OPERATION

Data written into the 8T31 from one port will appear inverted when read from the other port. Data written into the 8T31 from one port will not be inverted when read from the same port.

8-BIT LATCHED BIDIRECTIONAL I/O PORT 8T31

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V \pm 5\%$, $0°C \leq T_A \leq 70°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Input voltage:						V
V_{IH}	High		2.0			
V_{IL}	Low				.8	
V_{IC}	Clamp	I_I = 5mA			-1	
Output voltage:		V_{CC} = 4.75V				V
V_{OH}	High		2.4			
V_{OL}	Low				.55	
Input current[1]:		V_{CC} = 5.25V				μA
I_{IH}	High	V_{IH} = 5.25V		<10	100	
I_{IL}	Low	V_{IL} = .5V		-350	-550	
Output current[2]:						mA
I_{OS}	Short circuit	V_{CC} = 4.75V				
	UD bus		10			
	IV bus		20			
I_{CC}	VCC supply current	V_{CC} = 5.25V		100	150	mA

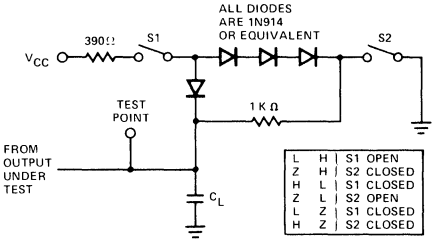
NOTES

1 The input current includes the three-state/open collector leakage current of the output driver on the data lines

2 Only one output may be shorted at a time

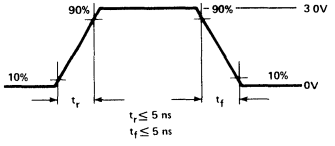
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT FOR THREE-STATE OUTPUTS

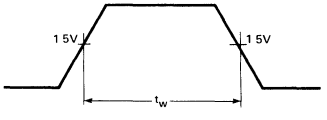


NOTE C_L includes fixture capacitance

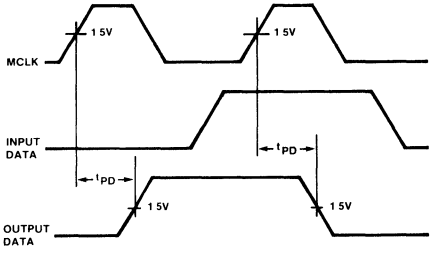
INPUT WAVEFORM



CLOCK PULSE WIDTH



DATA DELAY TIMES
Clock Referenced



8-BIT LATCHED BIDIRECTIONAL I/O PORT 8T31

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 5\%$

PARAMETERS		INPUT	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
		UD X			25	38	ns
t_{PD}	User data relay[1]	MCLK	C_L = 50pF		45	61	ns
t_{OE}	User output enable	$\overline{BOC}$	C_L = 50pF	18	26	47	ns
		$\overline{BIC}$		18	28	35	ns
t_{OD}	User output disable	BOC	C_L = 50pF	16	23	33	ns
		$\overline{IV\ X}$			38	53	ns
t_{PD}	μP data delay[1]	MCLK	C_L = 50pF		48	61	ns
		$\overline{ME}$					
t_{OE}	μP output enable	$\overline{RC}$	C_L = 50pF	14	19	25	ns
		WC					
		$\overline{ME}$					
t_{OD}	μP output disable	$\overline{RC}$	C_L = 50pF	13	17	32	ns
		WC					
t_W	Minimum pulse width	MCLK		40			ns
		$\overline{UD\ X}$[3]		15			
		$\overline{BIC}$		25			
		$\overline{IV\ X}$		55			
t_{SETUP}	Minimum setup time[2]	$\overline{ME}$		30			ns
		$\overline{RC}$		30			
		WC		30			
		$\overline{UD\ X}$[3]		25			
		$\overline{BIC}$		10			
		$\overline{IV\ X}$		10			
t_{HOLD}	Minimum hold time[2]	$\overline{ME}$		5			ns
		$\overline{RC}$		5			
		WC		5			

NOTES

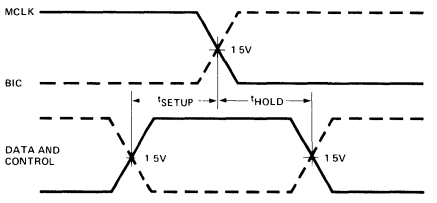
1 Data delays referenced to the clock are valid only if the input data is stable at the arrival of the clock and the hold time requirement is met

2 Set up and hold times given are for "normal" operation $\overline{BIC}$ setup and hold times are for a user write operation $\overline{RC}$ setup and hold times are for an I/O Port select operation $\overline{ME}$ and WC setup and hold times are for a microprocessor bus write operation

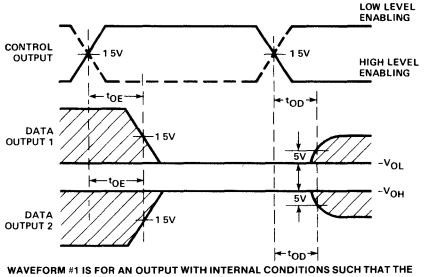
3 Times are referenced to MCLK

VOLTAGE WAVEFORMS

SETUP AND HOLD TIMES



OUTPUT ENABLE AND DISABLE TIMES
(Three-State Outputs)



WAVEFORM #1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW WHEN THE THREE-STATE DRIVER IS ENABLED WAVEFORM #2 IS FOR THE OPPOSITE CONDITION

8-BIT LATCHED ADDRESSABLE BIDIRECTIONAL I/O PORT 8T32/8T36

FEATURES

- **Independent port operation (user-port priority for data entry)**
- **User data input available as synchronous (8T32) or as asynchronous (8T36)**
- **User data bus available with three-state (8T32, 8T36)**
- **At power-up, user-port outputs are high and microprocessor-port outputs are high-z; status latch (from address compare) is also cleared at power-up**
- **Three-state TTL outputs for high-drive capabilities**
- **Directly compatible with 8X300 microcontroller**
- **Single +5V supply**

PRODUCT IDENTITY

8T32— Three-state, field-programmable (addresses 0-255), synchronous user port.

8T36—Three-state, field-programmable (addresses 0-255), asynchronous user port

PRODUCT DESCRIPTION

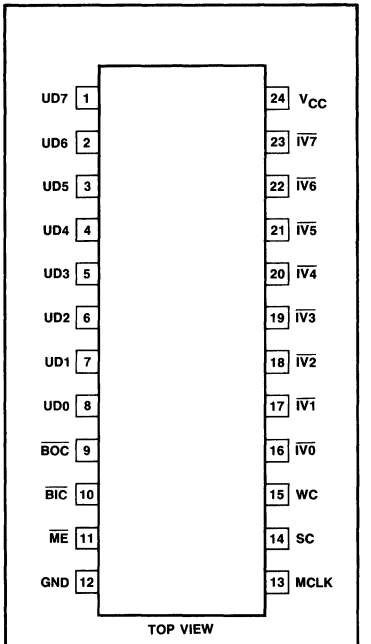
8T32/8T36. Each of these I/O Bytes is an addressable and bi-directional register designed for use as an interface element in any system with TTL-compatible buses. (*Note.* Since these I/O Bytes are frequently used with the 8X300 Microcontroller and its associated Interface Vector bus, the 8T32-8T36 family of parts are commonly called IV Bytes.) Each I/O Byte contains eight identical data latches (Bits 0 through 7); the latches are accessed from either of two 8-bit ports—one port connecting to the microprocessor (8X300) and the other port connecting to the user device.

Separate controls are provided for each port and the two ports operate independently, except when both attempt to input data at the same time; in this case, the user port bus has priority.

The address of each I/O Byte is field-programmable and the microprocessor port is accessed when a valid address is received; the user port is accessible at all times. A selected Byte is automatically deselected when the address of another I/O Byte is sensed on the address/data bus. A Master Enable (ME) input is available for use as a ninth address bit, allowing direct access to 512 I/O Bytes without address decoding.

A unique feature of these parts is their ability to start up in a predetermined state. If the clock is maintained at a level of less than 0.8 volts until the power supply reaches 3.5 volts, all bits of the user port will wakeup at a "logic 1" level and those of the microprocessor port will wakeup in the high-impedance state.

PIN CONFIGURATION



TOP VIEW

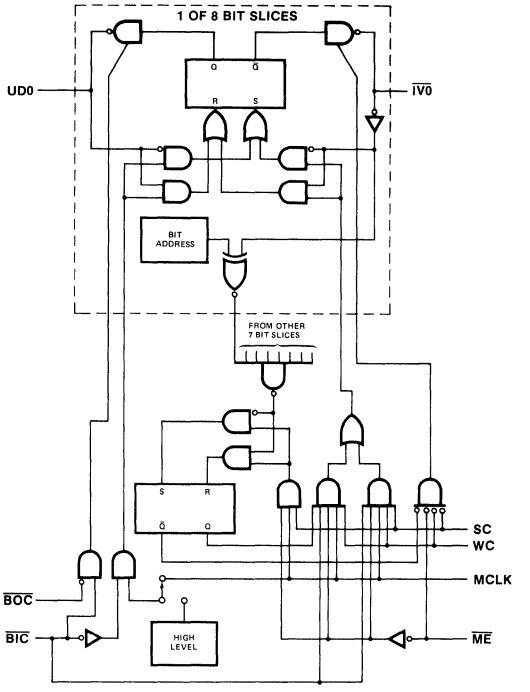
ORDER NUMBERS

CONTACT LOCAL SALES REPRESENATIVE

A stock of 8T32s and 8T36s with addresses "1" through "10" are maintained in inventory; with a longer lead time, a small quantity of address "11" through "50" are also available.

8-BIT LATCHED ADDRESSABLE BIDIRECTIONAL I/O PORT 8T32/8T36

TYPICAL BLOCK DIAGRAM



*Switch indicates synchronous/asynchronous user write option Switch shown for synchronous version

8-BIT LATCHED ADDRESSABLE BIDIRECTIONAL I/O PORT 8T32/8T36

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-8	UD0-UD7	User Data I/O Lines Bidirectional data lines to communicate with user's equipment Either tri-state or open collector outputs are available	Active high
16-23	$\overline{IV0}$-$\overline{IV7}$	Microprocessor Bus Bidirectional data lines to communicate with controlling digital system (microprocessor)	Active low three-state
10	$\overline{BIC}$	Input Control User input to control writing into the I/O Port from the user data lines	Active low
9	$\overline{BOC}$	Output Control User input to control reading from the I/O Port onto the user data lines	Active low
11	$\overline{ME}$	Master Enable System input to enable or disable all other system inputs and outputs It has no effect on user inputs and outputs	Active low
15	WC	Write Command. When WC is high and SC is low, I/O Port, if selected, stores contents of $\overline{IV0}$-$\overline{IV7}$ as data.	Active high
14	SC	Select Command. When SC is high and WC is low, data on $\overline{IV0}$-$\overline{IV7}$ is interpreted as an address I/O Port selects itself if its address is identical to μP bus data; it de-selects itself otherwise	Active high
13	MCLK	Master Clock Input to strobe data into the latches See function tables for details	Active high
24	VCC	5V power connection	
12	GND	Ground	

Table 1. USER PORT CONTROL FUNCTION

$\overline{BIC}$	$\overline{BOC}$	MCLK	USER DATA BUS FUNCTION	
			8T32	8T36
H	L	X	Output Data	Output Data
L	X	H	Input Data	Input Data
L	X	L	Inactive	Input Data
H	H	X	Inactive	Inactive

H = High Level L = Low Level X = Don't care

Table 2. MICROPROCESSOR PORT CONTROL FUNCTION

$\overline{ME}$	SC	WC	MCLK	$\overline{BIC}$	STATUS LATCH	I/O PORT FUNCTION
L	L	L	X	X	SET	Output Data
L	L	H	H	H	SET	Input Data
L	H	L	H	X	X	Input Address
L	H	H	H	L	X	Input Address
L	H	H	H	H	X	Input Data and Address
L	X	H	L	X	X	Inactive
L	H	X	L	X	X	Inactive
L	L	H	H	L	X	Inactive
L	L	X	X	X	Not Set	Inactive
H	X	X	X	X	X	Inactive

USER DATA BUS

The activity of the user data bus is controlled by the $\overline{BIC}$ and $\overline{BOC}$ inputs as shown in Table 1.

For the 8T32, user data input is a synchronous function with MCLK. A low level on the $\overline{BIC}$ input allows data on the user data bus to be written into the data latches only if MCLK is at a high level. For the 8T36, user data input is an asynchronous function. A low level on the $\overline{BIC}$ input allows data on the user data bus to be latched regardless of the level of the MCLK input Note that when the 8T36, is used with the 8X300 Microcontroller, care must be taken to insure that the Microprocessor bus is stable when it is being read by the 8X300 Microcontroller.

To avoid conflicts at the Data Latches, input from the Microprocessor Port is inhibited when $\overline{BIC}$ is at a low level. Under all other conditions the two ports operate independently

MICROPROCESSOR BUS CONTROL

As is shown in Table 2, the activity of the microprocessor port is controlled by the $\overline{ME}$, SC, WC, and $\overline{BIC}$ inputs, as well as the state of an internal status latch. $\overline{BIC}$ is included to show user port priority over the microprocessor port for data input.

Each I/O Port's status latch stores the result of the most recent I/O Port select; it is set when the I/O Port's internal address matches the Microprocessor Bus. It is cleared when an address that differs from the internal address is presented on the Microprocessor Bus.

In normal operation, the state of the status latch acts like a master enable; the microprocessor port can transfer data only when the status latch is set.

When SC and WC are both high, data on the Microprocessor Bus is accepted as data, whether or not the I/O Port was selected. The data is also interpreted as an address. The I/O Port sets its select status if its address matches the data read when SC and WC were both high; it resets its select status otherwise.

BUS OPERATION

Data written into the I/O Port from one port will appear inverted when read from the other port. Data written into the I/O Port from one port will not be inverted when read from the same port.

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 5\%$

PARAMETER	INPUT	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
t_{PD} User data delay (Note 1)	UD X	C_L = 50pF		25	38	ns
	MCLK*			45	61	
	$\overline{BIC}$†			40	55	
t_{OE} User output enable	$\overline{BOC}$	C_L = 50pF	18	26	47	ns
t_{OD} User output disable	$\overline{BIC}$	C_L = 50pF	18	28	35	ns
	$\overline{BOC}$		16	23	33	
t_{PD} µP data delay (Note 1)	$\overline{IV}$ X	C_L = 50pF		38	53	ns
	MCLK			48	61	
t_{OE} µP output enable	$\overline{ME}$	C_L = 50pF	14	19	25	ns
	SC					
	WC					
t_{OD} µP output disable	$\overline{ME}$	C_L = 50pF	13	17	32	ns
	SC					
	WC					
t_W Minimum pulse width	MCLK		40			ns
	$\overline{BIC}$†		35			
t_{SETUP} Minimum setup time	UD X□	(Note 2)	15			ns
	$\overline{BIC}$*		25			
	$\overline{IV}$ X		55			
	$\overline{ME}$		30			
	SC		30			
	WC		30			
t_{HOLD} Minimum hold time	UD X□	(Note 2)	25			ns
	$\overline{BIC}$*		10			
	$\overline{IV}$ X		10			
	$\overline{ME}$		5			
	SC		5			
	WC		5			

• Applies for 8T32.
† Applies for 8T36.
□ Times are referenced to MCLK for 8T32, and are referenced to BIC for 8T36.

NOTES:

1. Data delays referenced to the clock are valid only if the input data is stable at the arrival of the clock and the hold time requirement is met.
2. Set up and hold times given are for "normal" operation. $\overline{BIC}$ setup and hold times are for a user write operation. SC setup and hold times are for I/O Port select operation. $\overline{ME}$ setup and hold times are for both IV write and select operations.

3

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 5\%$

PARAMETER		TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		5 5	V
V_{IL}	Low-level input voltage		-1 0		8	V
V_{CL}	Input clamp voltage	$I_I = -5mA$			-1.0	V
I_{IH}	High-level input current[1]	$V_{CC} = 5\ 25V$ $V_{IH} = 5.25V$		<10	100	μA
I_{IL}	Low level input current[1]	$V_{CC} = 5.25V$ $V_{IL} = .5V$		-350	-550	μA
V_{OL}	Low-level output voltage	$V_{CC} = 4\ 75V$ $I_{OL} = 16mA$			.55	V
V_{OH}	High-level output voltage	$V_{CC} = 4.75V$ $I_{OH} = -3.2mA$	2.4			V
I_{OS}	Short-circuit output current[2] UD bus IV bus	 $V_{CC} = 4.75V$ $V_{CC} = 4.75V$	 10 20			 mA mA
I_{CC}	Supply current	$V_{CC} = 5.25V$		100	150	mA

NOTES

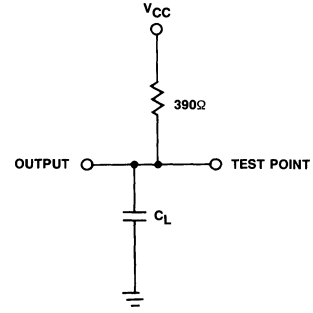
1 The input current includes the Three-state/Open Collector leakage current of the output driver on the data lines
2 Only one output may be shorted at a time
3 These limits do not apply during address programming

Absolute Maximum Ratings:

Supply voltage[3] 7V

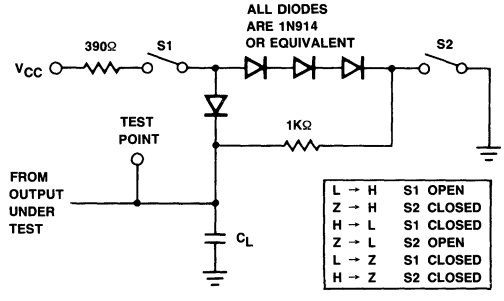
Input voltage[3] 5 5V

TEST LOAD CIRCUIT (OPEN COLLECTOR OUTPUTS)



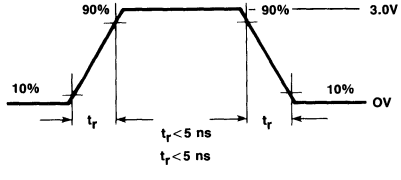
NOTE: C_L includes fixture capacitance.

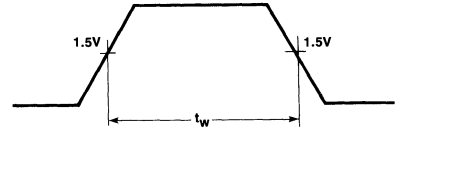
TEST LOAD CIRCUIT (THREE-STATE OUTPUTS)



NOTE: C_L includes fixture capacitance.

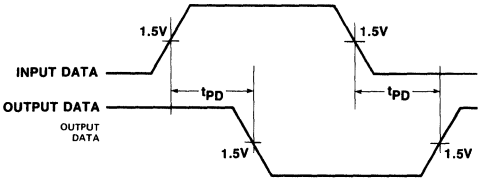
VOLTAGE WAVEFORMS



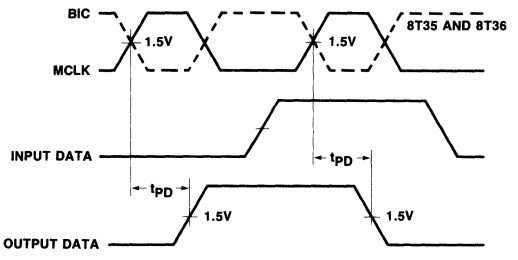


VOLTAGE WAVEFORMS (Cont'd)

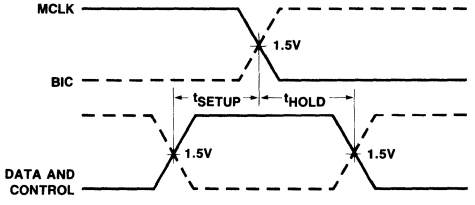
DATA DELAY TIMES
Input Data Reference



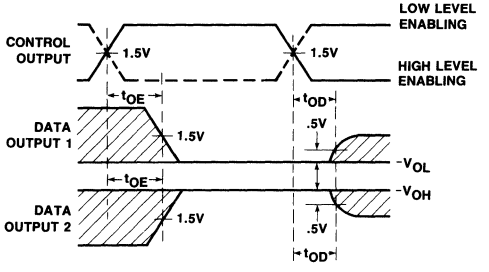
DATA DELAY TIMES
Clock Referenced



SETUP AND HOLD TIMES



OUTPUT ENABLE AND DISABLE TIMES
(Three-State Outputs)



Waveform #1 is for an output with internal conditions such that the output is Low when the three-state driver is enabled Waveform #2 is for the opposite condition

8-BIT LATCHED ADDRESSABLE BIDIRECTIONAL I/O PORT 8T32/8T36

ADDRESS PROGRAMMING

The I/O Port is manufactured such that an address of all high levels (>2V) on the Microprocessor Bus inputs matches the Port's internal address. To program a bit so a low-level input (<0.8V) matches, the following procedure should be used:

1. Set all control inputs to their inactive state ($\overline{BIC}$ = $\overline{BOC}$ = $\overline{ME}$ = V_{CC}, SC = WC = MCLK = GND). Leave all Microprocessor Bus I/O pins open.
2. Raise V_{CC} to 7.75V ± .25V.
3. After V_{CC} has stabilized, apply a single programming pulse to the user data bus bit where a low-level match is desired. The voltage should be limited to 18V; the current should be limited 75mA. Apply the pulse as shown in Figure 1.
4. Return V_{CC} to 0V. (Note 1).
5. Repeat this procedure for each bit where a low-level match is desired.
6. Verify that the proper address is programmed by setting the Port's status latch ($\overline{IV0}$-$\overline{IV7}$ = desired address, $\overline{ME}$ = WC = L, SC = MCLK = H). If the proper address has been programmed, data presented at the μP bus will appear inverted on the user bus outputs. (Use normal V_{CC} and input voltage for verification.)

After the desired address has been programmed, a second procedure must be followed to isolate the address circuitry. The procedure is:

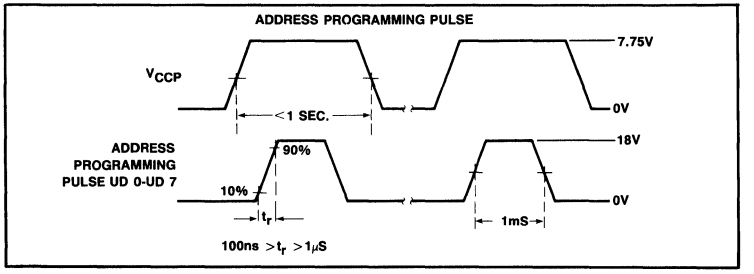


Figure 1

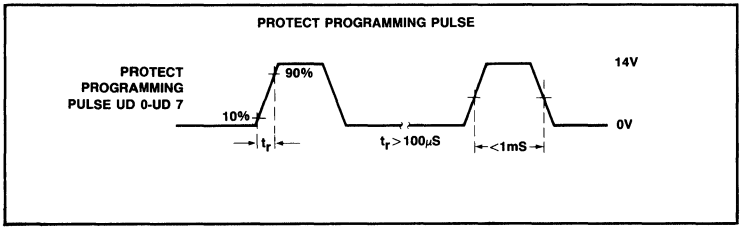


Figure 2

1. Set V_{CC} and all control inputs to 0V. (V_{CC} = $\overline{BIC}$ = $\overline{BOC}$ = $\overline{ME}$ = SC = WC = MCLK = 0V). Leave all Microprocessor Bus I/O pins open.
2. Apply a protect programming pulse to every user data bus pin, one at a time. The voltage should be limited to 14V; the current should be limited to 150mA. Apply the pulse as shown in Figure 2.
3. Verify that the address circuitry is isolated by applying 7V to each user data bus pin and measuring less than 1mA of input current. The conditions should be the same as in step 1 above. The rise time on the verification voltage must be slower than 100μs.

PROGRAMMING SPECIFICATIONS[1]

PARAMETER		TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
V_{CCP}	Programming supply voltage					
	Address		7.5		8.0	V
	Protect			0		V
I_{CCP}	Programming supply current	V_{CCP} = 8.0V			250	mA
	Max time V_{CCP}>5.25V				1.0	s
	Programming voltage					
	Address		17.5		18.5	V
	Protect		13.5		14.0	V
	Programming current					
	Address				75	mA
	Protect				150	mA
	Programming pulse rise time					
	Address		.1		1	μs
	Protect		100			μs
	Programming pulse width		.5		1	ms

NOTE

1. If all programming can be done in less than 1 second, V_{CC} may remain at 7.75V for the entire programming cycle.

8-BIT LATCHED ADDRESSABLE BIDIRECTIONAL I/O PORT 8T32/8T36

APPLICATIONS

Figure 3 shows some of the various ways to use the I/O Port in a system. By controlling the $\overline{BIC}$ and $\overline{BOC}$ lines, the device may be used for the input and output of data, control, and status signals. I/O Port 1 functions bidirectionally for data transfer and I/O Port 2 provides a similar function for discrete status and control lines. I/O Ports 3 and 4 serve as dedicated output and input ports, respectively.

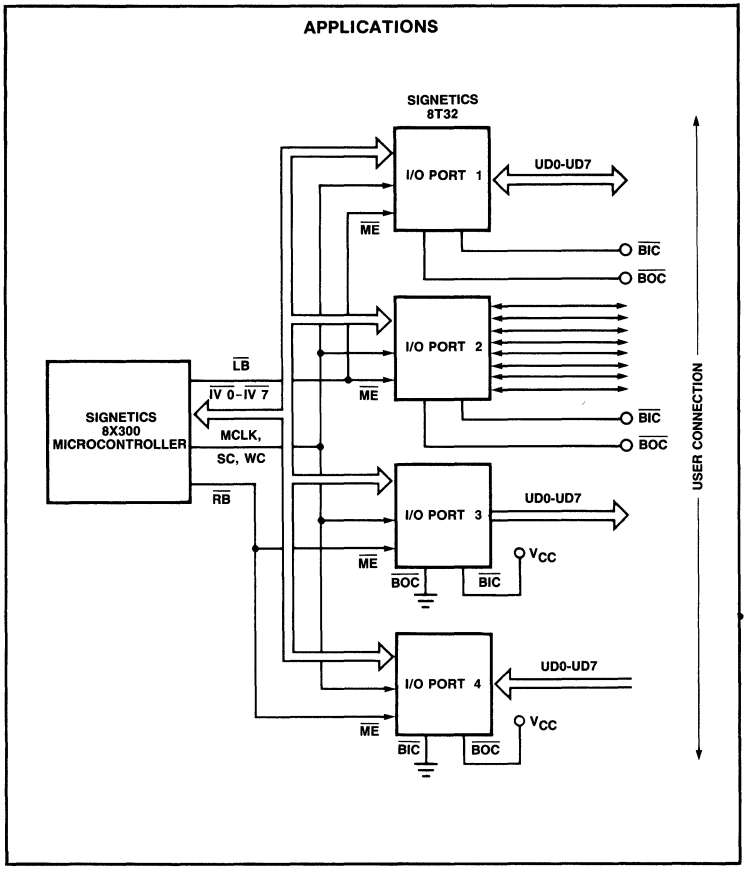


Figure 3

8-BIT LATCHED BIDIRECTIONAL I/O PORT — 8X371

FEATURES

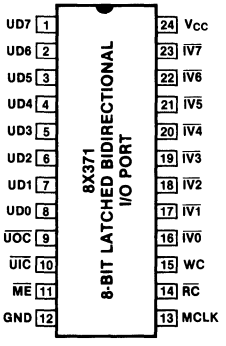
- **Two bidirectional 8-bit busses**
- **Independent bus operation (user-bus priority for data entry)**
- **User data input synchronous with respect to MCLK**
- **Three-state TTL outputs with high-drive capabilities**
- **Power-up to predetermined logic state**
- **Directly compatible with 8X305 (or 8X300) MicroControllers**
- **Single +5V supply**
- **0.4 inch 24-pin DIP**

PRODUCT DESCRIPTION

The 8X371 I/O Port is a bidirectional device designed for use as an interface element in systems that use TTL-compatible busses. Typically, the 8X371 is used with the 8X305 MicroController and its associated Interface Vector ($\overline{IV}$) bus; however, it can also be used with the 8X300 MicroController or an equivalent microprocessor. The 8X371 is functionally the same and pin-for-pin compatible with the older 8T31/8X31 but features improved performance and increased drive current. As shown in the logic diagram of Figure 1, the 8X371 consists of eight identical data latches—bits 0 through 7. The latches are accessed from either of two 8-bit busses—the MicroController ($\overline{IV}$ bus) and the user data (UD bus). Separate controls are provided for each bus and both busses operate independently, except when both attempt to input data at the same time; in such situations, the user bus always has priority. A Master Enable ($\overline{ME}$) input is available for additional control over the $\overline{IV}$ bus. The data latches are transparent, in that, while either bus is enabled for input, all input-data transitions are propagated to the other bus, if enabled for output.

8X371 PACKAGE and PIN DESIGNATIONS

N, I PACKAGE



TOP VIEW

ORDER NUMBERS

N8X371N, N8X371I
S8X371I/883B, S8X371I/883C

PIN. NO.	IDENTIFIER	FUNCTION
1-8	UD7-UD0	Three-state, bidirectional User Data (UD) bus, UD0 and corresponds to $\overline{IV0}$
9	$\overline{UOC}$	User Output Control—active low input to enable data output to UD0-UD7
10	$\overline{UIC}$	User Input Control—active low input to enable data input from UD0-UD7
11	$\overline{ME}$	Master Enable—active low input to enable the $\overline{IV}$ bus for data input, or data output, UD-bus operations are unaffected
12	GND	Ground
13	MCLK	Master Clock—active high input (from MicroController used to strobe data into data latches from the $\overline{IV}$ and UD buses
14	$\overline{RC}$	Read Control—active low input to enable data output to $\overline{IV0}$-$\overline{IV7}$
15	WC	Write Command—active high input (from MicroController) to enable the writing of data into the data latches from the $\overline{IV}$ bus (provided $\overline{UIC}$ is not low)
16-23	$\overline{IV0}$-$\overline{IV7}$	Interface Vector (Input/Output Bus)—three-state, bidirectional, MicroController data bus, $\overline{IV0}$ corresponds to UD0
24	V_{CC}	+5V power supply

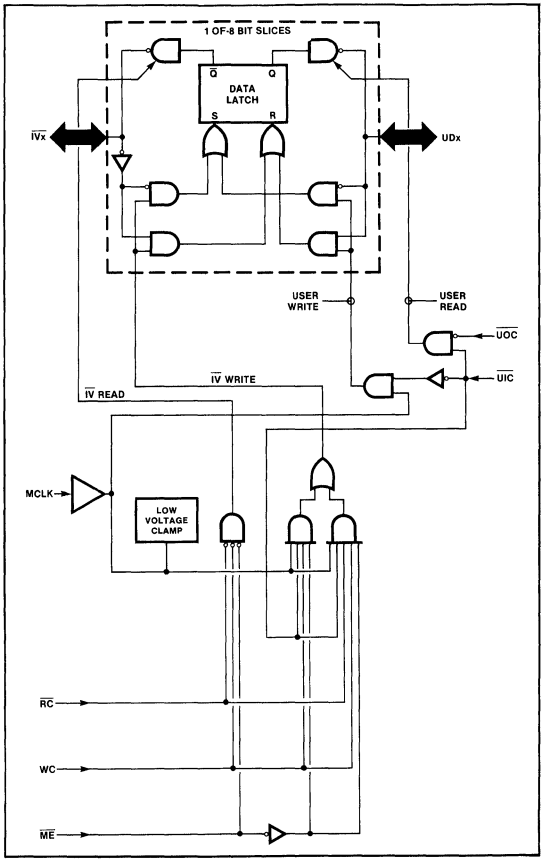


Figure 1. Logic Diagram for 8X371 I/O Port

8-BIT LATCHED BIDIRECTIONAL I/O PORT 8X371

FUNCTIONAL OPERATION

UD Bus Control

As shown in Table 1, the User Data (UD) bus interface is controlled by the $\overline{UIC}$ and $\overline{UOC}$ inputs. Data input to the UD bus is synchronous with MCLK, that is, with $\overline{UIC}$ low, information is written into the data latches only when MCLK is high. Output drivers on the UD bus are enabled when $\overline{UOC}$ is low and $\overline{UIC}$ is high.

Table 1. INPUT/OUTPUT CONTROL OF UD BUS

$\overline{UIC}$	$\overline{UOC}$	MCLK	FUNCTION OF UD BUS
H	L	X	Output data
L	X	H	Input data
L	X	L	Inactive
H	H	X	Inactive

X = don't care

$\overline{IV}$ Bus Control

Input/output control of the $\overline{IV}$ bus is shown in Table 2; this bus is controlled by $\overline{RC}$, WC, $\overline{ME}$, and MCLK. The $\overline{IV}$ bus is enabled for output (MicroController read operation) when $\overline{ME}$, $\overline{RC}$, and WC are all low. Data is written into the data latches from the $\overline{IV}$ bus when $\overline{ME}$ is low and both WC and MCLK are high. To avoid data-input conflicts, inputs from the $\overline{IV}$ bus are inhibited when $\overline{UIC}$ is low; under all other conditions, the $\overline{IV}$ and UD busses operate independently. The MicroController Left Bank ($\overline{LB}$) and Right Bank ($\overline{RB}$) outputs can control the $\overline{ME}$ inputs for two banks of I/O devices, thus acting as a ninth address bit. If more than one I/O Port (including the addressable parts—8X372, 8X376, 8X382, etc.) are to be connected to the same bank ($\overline{LB}$ or $\overline{RB}$) of the MicroController, selection of each 8X371 must be accomplished with external control logic to avoid bus conflicts.

Table 2. INPUT/OUTPUT CONTROL OF IV BUS

$\overline{ME}$	$\overline{RC}$	WC	MCLK	$\overline{UIC}$	FUNCTION OF $\overline{IV}$ BUS
L	L	L	X	X	Output Data
L	X	H	H	H	Input Data
L	H	L	X	X	Inactive
L	X	H	X	L	Inactive
L	X	H	L	H	Inactive
H	X	X	X	X	Inactive

Bus Logic Levels

Data written into the I/O port from either bus will appear inverted when read from the other bus. Data written into either bus will not be inverted when read from the same bus. (Note. *A logic "1" in MicroController software corresponds to a high level on the UD bus even though the $\overline{IV}$ bus is inverted.*) The 8X382 wakes up in the unselected state with all data bits latched at the "logic 1" level (UD bus outputs high if enabled).

DC ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5 5	Vdc
T_{STG}	Storage temperature range	-65 to +150	°C

COMMERCIAL 4 75V ≤ V_{CC} ≤ 5 25V, 0°C ≤ T_A ≤ 70°C
MILITARY. 4 5V ≤ V_{CC} ≤ 5 5V, -55°C ≤ T_C ≤ 125°C

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4 75	5	5 25	4 5	5	5 5	V
V_{IH}	High Level Input Voltage		2 0			2 0			V
V_{IL}	Low Level Input Voltage				0 8			0.8	V
V_{CL}	Input Clamp Voltage	V_{CC}=Min, I_I=-10mA			-1 5			-1.5	V
I_{IH}	High Level Input Current[1]	V_{CC}=Max, V_{IH}=2 7V		5	100		5	100	μA
I_{IL}	Low Level Input Current[1]	V_{CC}=Max, V_{IL}<0 5V		-350	-550		-350	-550	μA
V_{OL}	Low Level Output Voltage $\overline{IV}$ Bus ($\overline{IV0}$-$\overline{IV7}$)	V_{CC}=Min, I_{OL}= 16mA			0 55			0 55	V
	User Bus (UD4-UD7)	V_{CC}=Min, I_{OL}=24mA			0 55			0 55	V
V_{OH}	High Level Output Voltage	V_{CC}=Min, I_{OH}=-3.2mA	2 4			2 4			V
I_{OS}	Short Circuit Output Current[3] $\overline{IV}$ Bus ($\overline{IV0}$-$\overline{IV7}$)	V_{CC}=Max	-20			-20			mA
	UD Bus (UD4-UD7)	V_{CC}=Max	-10			-10			mA
I_{CC}	Supply Current	V_{CC}=Max, $\overline{ME}$=$\overline{UOC}$=V_{CC}		90	150		90	150	mA

Notes
1 The input current includes the Three-state leakage current of the output driver on the data lines
2 Only one output may be shorted at a time

AC ELECTRICAL CHARACTERISTICS (Cont'd)

COMMERCIAL: $4.75 \le V_{CC} \le 5.25V$, $0°C \le T_A \le 70°C$

MILITARY: $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_C \le 125°C$

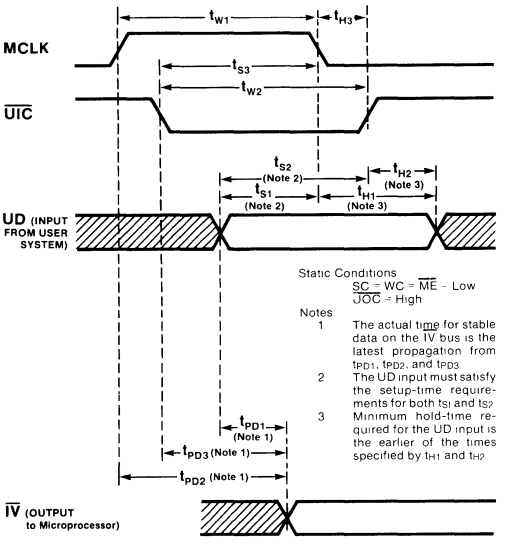
LOADING. See TEST LOADING CIRCUITS

PARAMETER	REFERENCES		TEST CONDITIONS	LIMITS (Commercial)			LIMITS (Military)			UNIT
	FROM	TO		Min	Typ	Max	Min	Typ	Max	
Pulse Widths:										
t_{W1} Clock High	↑MCLK	↓MCLK		35			35			ns
t_{W2} User Input Control	↓$\overline{UIC}$	↑$\overline{UIC}$	MCLK = High	35			35			ns
Propagation Delays:										
t_{PD1} UD Propagation Delay	UD	$\overline{IV}$	MCLK = High $\overline{RC}$ = WC = $\overline{ME}$ = $\overline{UCI}$ = Low			30			30	ns
t_{PD2} UD Clock Delay	↑MCLK	$\overline{IV}$	UD = Stable; $\overline{RC}$ = WC = $\overline{ME}$ = $\overline{UIC}$ = Low			50			50	ns
t_{PD3} UD Input Delay	↓$\overline{UIC}$	$\overline{IV}$	UD = Stable; MCLK = High $\overline{RC}$ = WC = $\overline{ME}$ = Low			50			50	ns
t_{PD4} $\overline{IV}$ Data Propagation Delay	$\overline{IV}$	UD	MCLK = WC = $\overline{UIC}$ = High; $\overline{ME}$ = $\overline{UOC}$ = $\overline{RC}$ = Low			45			45	ns
t_{PD5} $\overline{IV}$ Data Clock Delay	↑MCLK	UD	WC = $\overline{UIC}$ = High; $\overline{IV}$ = Stable $\overline{ME}$ = $\overline{UOC}$ = $\overline{RC}$ = Low			55			55	ns
Output Enable Timing:										
t_{OE1} UD Output Enable	↓UOC	UD	$\overline{UIC}$ = High			30			30	ns
t_{OE2} UD Input Recovey	↑$\overline{UIC}$	UD	$\overline{UOC}$ = Low			30			30	ns
t_{OE3} $\overline{IV}$ Data Master Enable	↓$\overline{ME}$	$\overline{IV}$	WC = $\overline{RC}$ = Low			22			25	ns
t_{OE4} $\overline{IV}$ Data Read Enable	↓$\overline{RC}$	$\overline{IV}$	WC = $\overline{ME}$ = Low			25			25	ns
t_{OE5} $\overline{IV}$ Data Write Recovery	↓WC	$\overline{IV}$	$\overline{RC}$ = $\overline{ME}$ = Low			25			25	ns
Output Disable Timing:										
t_{OD1} UD Output Disable	↑$\overline{UOC}$	UD	$\overline{UIC}$ = High			25			25	ns
t_{OD2} UD Input Override	↓$\overline{UIC}$	UD	$\overline{UOC}$ = Low			30			30	ns
t_{OD3}[1] $\overline{IV}$ Data Master Disable	↑$\overline{ME}$	$\overline{IV}$	WC = $\overline{RC}$ = Low			20			20	ns
t_{OD4}[1] $\overline{IV}$ Data Read Disable	↑$\overline{RC}$	$\overline{IV}$	WC = $\overline{ME}$ = Low			20			20	ns
t_{OD5} $\overline{IV}$ Data Write Override	↑WC	$\overline{IV}$	$\overline{RC}$ = $\overline{ME}$ = Low			20			20	ns
Setup Time:										
t_{S1} UD Clock Setup Time	UD	↓MCLK	$\overline{UIC}$ = Low	15			15			ns
t_{S2} UD Setup Time	UD	↑UIC	MCLK = High	15			15			ns
t_{S3} User Input Control Setup Time	↓$\overline{UIC}$	↓MCLK		25			25			ns
t_{S4} $\overline{IV}$ Data Setup Time	$\overline{IV}$	↓MCLK	WC = $\overline{UIC}$ = High; $\overline{ME}$ = Low	35			35			ns
t_{S5}[2] $\overline{IV}$ Master Enable Setup Time	↓$\overline{ME}$	↓MCLK	WC = $\overline{UIC}$ = High	30			30			ns
t_{S6} $\overline{IV}$ Write Control Setup Time	↑WC	↓MCLK	$\overline{ME}$ = Low; $\overline{UIC}$ = High	30			30			ns

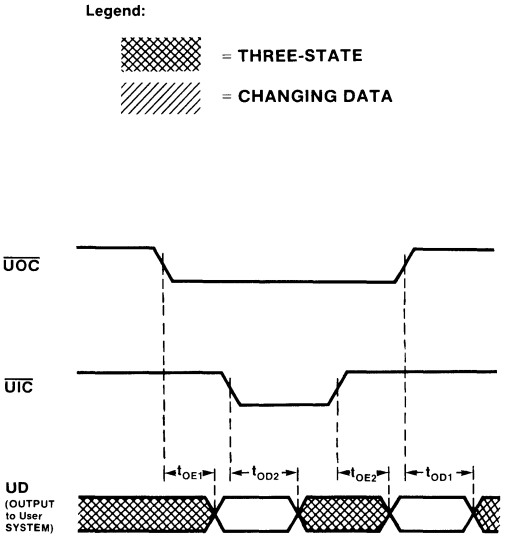
AC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER	REFERENCES		TEST CONDITIONS	LIMITS (Commercial)			LIMITS (Military)			UNIT
	FROM	TO		Min	Typ	Max	Min	Typ	Max	
Hold Times:										
t_{H1} UD Clock Hold Time	↓MCLK	UD	$\overline{UIC}$ = Low	15			15			ns
t_{H2} UD Control Hold Time	↑$\overline{UIC}$	UD	MCLK = High	15			15			ns
t_{H3} User Input Control Hold Time	↓MCLK	↑UIC		0			0			ns
t_{H4} $\overline{IV}$ Data Hold Time	↓MCLK	$\overline{IV}$	WC = $\overline{UIC}$ = High; $\overline{ME}$ = Low	5			5			ns
t_{H5}[2] $\overline{IV}$ Master Enable Hold Time	↓MCLK	↑$\overline{ME}$	WE = $\overline{UIC}$ = High	0			0			ns
t_{H6} $\overline{IV}$ Write Control Hold Time	↓MCLK	↓WC	$\overline{ME}$ = Low; = $\overline{UIC}$ = High	0			0			ns

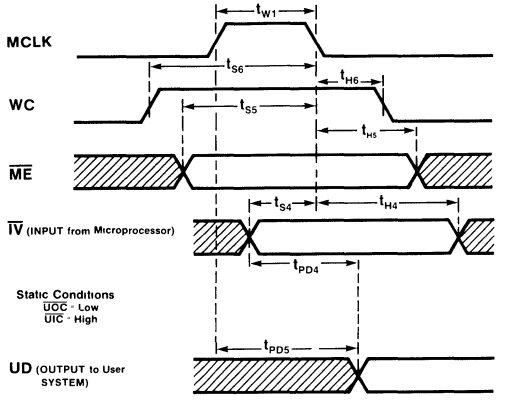
Notes:
1 These parameters are measured with a capacitive loading of 50 *pf* and represent the output driver turn-off time
2. If $\overline{ME}$ is to be high (inactive), it must be setup before the rising edge and held after the falling edge of MCLK to avoid unintended writing into or selection of the I/O port



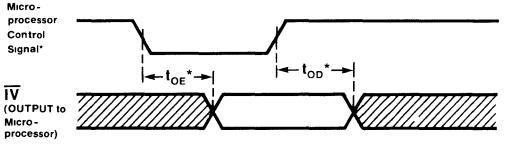
a. User Data Input Timing



b. User Data Output Timing



c. MicroController Write Cycle Timing



*PARAMETER KEY

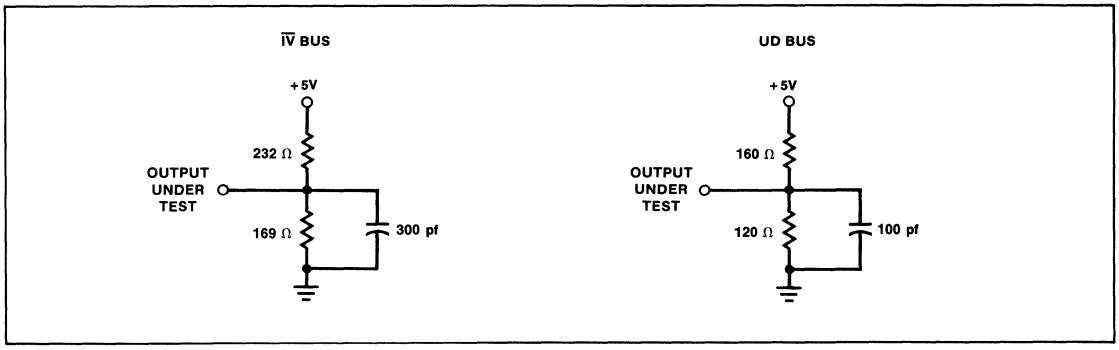
MICROPROCESSOR CONTROL SIGNAL	AC TIMING PARAMETERS	STATIC CONDITIONS
ME	t_{OE3} t_{OD3}	SC = WC = LOW
RC	t_{OE4} t_{OD4}	SC = ME = LOW
SC	t_{OE5} t_{OD5}	RC = ME = LOW

d. MicroController Select Cycle Timing

Figure 2. Timing Diagram

8-BIT LATCHED BIDIRECTIONAL I/O PORT 8X371

TEST LOADING CIRCUITS



8-BIT LATCHED BIDIRECTIONAL I/O PORT 8X371

APPLICATIONS

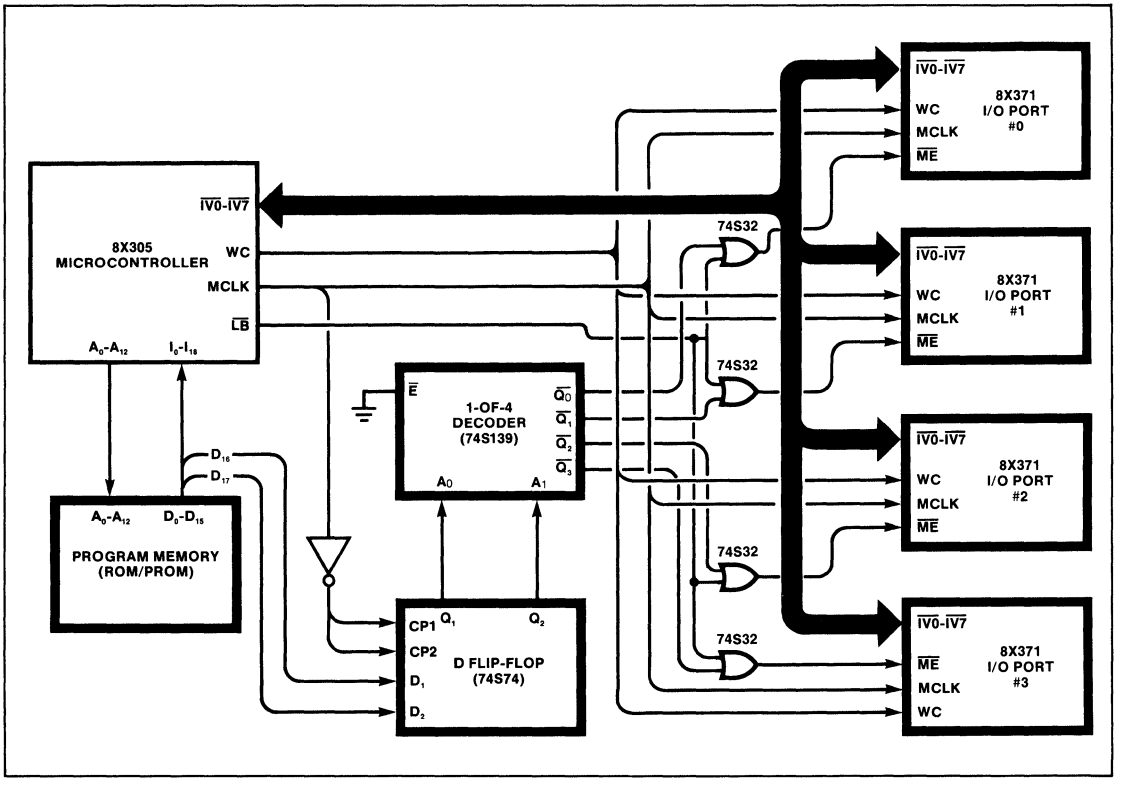
In some applications, performance of a MicroController system can be enhanced by using the 8X371 I/O Port instead of an addressable 8X372 port. Using a technique referred to as Extended Microcode or Fast $\overline{IV}$ Select, the address select cycles which normally precede a read or write operation when using an 8X372 can be eliminated by use of the 8X371.

This technique is often used in bit slice microprocessor designs and involves widening the program memory beyond the normal 16-bit requirement of the MicroController. The extra bits are used as enable signals for the 8X371 ports. Thus, the 8X371 is enabled during the instruction cycle in which it is required for input/output operations. Since the software overhead of separate address select cycles is eliminated, the overall system performance is improved.

As shown in the accompanying diagram, the program memory is extended by two bit positions (D_{16} and D_{17}), permitting any one of four 8X371 ports to be enabled during those instructions that perform input/output operations. Because of timing considerations, latches must be used to hold the Extended Microcode through the end of the instruction cycle. A decoder is used to obtain four enable signals from the two extra bits. The decoder outputs are ORed with the $\overline{LB}$ output of the 8X305; thus, all four I/O ports are placed on the Left Bank of the $\overline{IV}$ bus.

3

I/O PORT SELECTION USING EXTENDED MICROCODE



ADDRESSABLE/BIDIRECTIONAL I/O PORTS 8X372/8X376

FEATURES

- **Two bidirectional 8-bit busses**
- **Independent bus operation (user-bus priority for data entry)**
- **User data input synchronous (8X372) or asynchronous (8X376) with respect to MCLK**
- **Programmed MicroController port address**
- **Three-state TTL outputs with high-drive capabilities**
- **Power-up to predetermined logic state**
- **Directly compatible with 8X305 or 8X300 MicroControllers**
- **Single +5V supply**
- **0.4 inch 24-pin DIP**

PRODUCT IDENTITY

8X372—Synchronous, three-state, bidirectional I/O port with programmed address.
8X376—Asynchronous, three-state, bidirectional I/O port with programmed address.

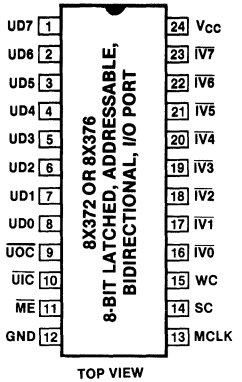
PRODUCT DESCRIPTION

Each of these I/O ports is an addressable device designed for use as a bidirectional interface element in systems that use TTL-compatible busses. Typically, these I/O ports are used with the 8X305 MicroController and its associated Interface Vector ($\overline{IV}$) bus; however, either port can also be used with the 8X300 MicroController or an equivalent microprocessor. The 8X372 and 8X376 are funtionally the same and pin-for-pin compatible with their respective counterparts, the 8T32/8X32 and 8T36/8X36, however, the new parts feature better performance, increased drive current, and improved programming procedures.

As shown in the logic diagram of Figure 1, each I/O port consists of eight identical data latches—bits 0 through 7. These latches are accessed through either of two 8-bit busses—one connecting to the MicroController ($\overline{IV}$ bus) and the other to the user system (UD bus). Separate controls are provided for each bus and both busses operate independently, except when both attempt to input data at the same time In such situations, the user bus always has priority. The data latches are transparent, in that, while either bus is enabled for input, all transitions in input data are propagated to the other bus, if enabled for output.

Both the 8X372 and 8X376 are available with preprogrammed addresses (0_{10} through 255_{10}), either device can be field-programmed over the same address range. Input/output operations can begin once the I/O port is selected and appropriate control signals are generated. Port selection is implemented by putting the I/O port address (0_{10}-255_{10}) on the $\overline{IV}$ bus; once selected, the I/O port remains selected until a different "port address" is put on the bus. Thus, software overhead is minimized. Data is accessible on the UD bus at all times. A Master Enable ($\overline{ME}$) input, which is typically connected to the Left Bank ($\overline{LB}$) or Right Bank ($\overline{RB}$) output of the MicroController, provides the capability of organizing the $\overline{IV}$ bus into two separate and independent banks of I/O devices.

N, I PACKAGE



TOP VIEW

ORDER NUMBERS

N8X372N or N8X376N
N8X372I or N8X376I
S8X372I/883B or S8X372I/883C
S8X376I/883B or S8X376I/883C

PIN. NO.	IDENTIFIER	FUNCTION
1-8	UD7-UD0	Three-state, bidirectional User Data (UD) bus, UD0 corresponds to $\overline{IV0}$
9	$\overline{UOC}$	User Output Control—active low input to enable data output to UD0-UD7
10	$\overline{UIC}$	User Input Control—active low input to enable data input from UD0-UD7
11	$\overline{ME}$	Master Enable—active low input to enable the $\overline{IV}$ bus for data input, data output, or $\overline{IV}$ address selection/deselection. UD-bus operations are unaffected
12	GND	Ground
13	MCLK	Master Clock—active high input from MicroController used to strobe data into data latches from the $\overline{IV}$ bus and, for the synchronous 8X372, from the UD bus. MCLK also synchronizes $\overline{IV}$ address selection
14	SC	Select Command—active high input from MicroController to enable $\overline{IV}$ address input from the $\overline{IV}$ bus for device selection
15	WC	Write Command—active high input from MicroController to enable the writing of data into the data latches from the $\overline{IV}$ bus, provided $\overline{UIC}$ is not low
16-23	$\overline{IV0}$-$\overline{IV7}$	Interface Vector Input/Output Bus —three-state, bidirectional MicroController data bus. $\overline{IV0}$ corresponds to UD0
24	V_{CC}	+5V power supply

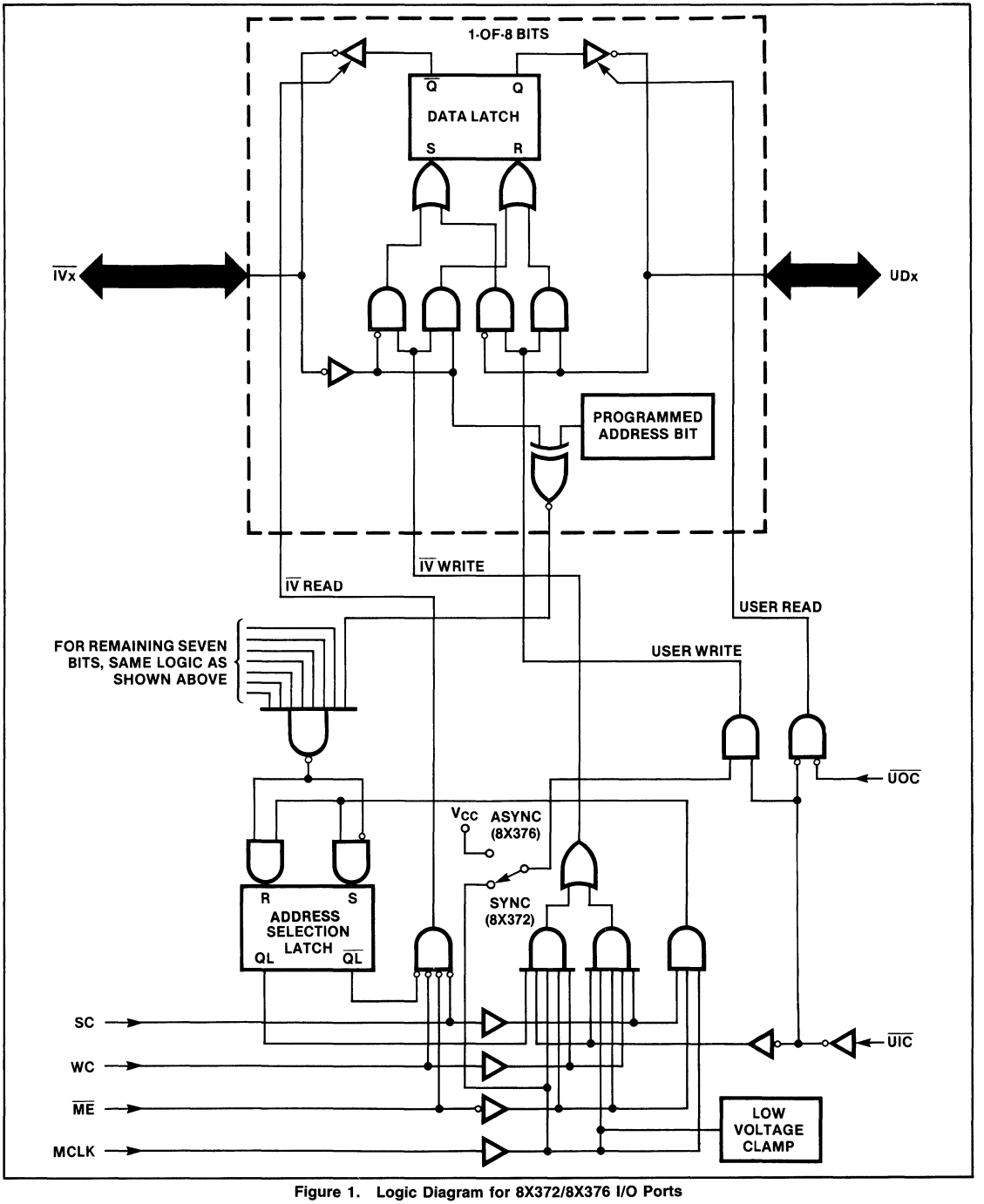


Figure 1. Logic Diagram for 8X372/8X376 I/O Ports

FUNCTIONAL OPERATION

UD Bus Control

As shown in Table 1, the User Data (UD) bus interface is controlled by the $\overline{UIC}$ and $\overline{UOC}$ inputs. For the 8X372, data input from the UD bus is written synchronously with MCLK, that is, with $\overline{UIC}$ low, information is written into the data latches only when MCLK is high. In the case of the 8X376, data input is asynchronous, in that, with $\overline{UIC}$ low, data is latched in without regard to the level of MCLK (Note *To avoid the possibility of processor error when using the asynchronous 8X376, the $\overline{IV}$ bus should not be read during the time the data latches are changing due to user input.*) Output drivers on the UD bus are enabled when UOC is low and $\overline{UIC}$ is high

Table 1. INPUT/OUTPUT CONTROL OF UD BUS

$\overline{UIC}$	$\overline{UOC}$	MCLK	FUNCTION OF UD BUS	
			8X372	8X376
H	L	X	Output data	Output data
L	X	H	Input data	Input data
L	X	L	Inactive	Input data
H	H	X	Inactive	Inactive

X = don't care

$\overline{IV}$ Bus Control

Input/output control of the $\overline{IV}$ bus is shown in Table 2; this bus is controlled by SC, WC, $\overline{ME}$, MCLK and the current state of the internal address selection latch. AS shown in Table 2, $\overline{UIC}$ is required to indicate priority of the UD bus for data input operations. The selection latch in the I/O port stores the result of the most recent $\overline{IV}$ address selection. The latch is set when the internally preprogrammed address of the port matches the address on the $\overline{IV}$ bus during an address-selection operation (SC = MCLK = High/WC = Low). The latch is cleared when the two 8-bit address patterns are in disagreement. The $\overline{IV}$ bus can transfer data only when the selection latch is set. As shown in the APPLICATION DIAGRAM, the MicroController Left Bank ($\overline{LB}$) and Right Bank ($\overline{RB}$) outputs can control the $\overline{ME}$ inputs for two banks of I/O devices, thus, acting as a ninth address bit.

Table 2. INPUT/OUTPUT CONTROL OF IV BUS

$\overline{ME}$	SC	WC	MCLK	$\overline{UIC}$	SELECTION LATCH	FUNCTION OF $\overline{IV}$ BUS
L	L	L	X	X	Set	Output Data
L	L	H	H	H	Set	Input Data
L	H	L	H	X	X	Input Address*
L	H	H	H	H	X	Input data and address*
L	H	H	H	L	X	Input Address*
L	X	H	L	X	X	Inactive
L	H	X	L	X	X	Inactive
L	L	H	H	L	X	Inactive
L	L	X	X	X	Not Set	Inactive
H	X	X	X	X	X	Inactive

X = don't care

* Selection latch is updated

Data is written into the data latches of a selected device from the $\overline{IV}$ bus when WC, MCLK, and $\overline{UIC}$ are all high and $\overline{ME}$ is low. To prevent data-input conflicts, inputs from the $\overline{IV}$ bus are inhibited when $\overline{UIC}$ is low; under all other conditions, the $\overline{IV}$ and UD busses operate independently Output drivers on the $\overline{IV}$ bus of a selected device are enabled when $\overline{ME}$, WC, and SC are all low and the address selection latch is set. With SC and WC both high (shaded entry of Table 2), the bit pattern present on $\overline{IV0}$-$\overline{IV7}$ is interpreted as both input data and $\overline{IV}$ address. Provided $\overline{UIC}$ is high, the data is latched into the data latches whether or not the I/O port has been previously selected. If the preprogrammed address of the I/O port matches the bit pattern on $\overline{IV0}$-$\overline{IV7}$ when SC and WC are both high, the selection latch is set; otherwise, it is reset. (Note *The MicroController never drives both SC and WC high at the same time.*)

Bus Logic Levels

Data written into the I/O port from either bus will appear inverted when read from the other bus. Data written into either bus will not be inverted when read from the same bus. (Note. *A logic "1" in MicroController software corresponds to a high level on the UD bus even though the $\overline{IV}$ bus is inverted.*) Both the 8X372 and 8X376 wakeup with the address selection latch in the unselected state and all data bits latched at the "logic 1" level (UD bus outputs high if enabled).

ADDRESS PROGRAMMING AND ADDRESS PROTECT

Programming Procedures

Both 8X372 and 8X376 can be programmed to respond to any address within a range of 0_{10} through 255_{10}. In an unprogrammed state, low level ($\leq$0.8V) inputs on all $\overline{IV}$ bus lines (address 255_{10}) will select the device. To program a given address bit to match a high level ($\geq$2.0V) input on the corresponding $\overline{IV}$ pin (a logical "0" to the MicroController), the counterpart UD-bus pin must be pulsed according to Table 3 and the following procedures:

Step 1: Set all control inputs to the inactive state—$\overline{UIC}$ = $\overline{UOC}$ = $\overline{ME}$ = V_{CC} and SC = WC = MCLK = GND; leave the UD and $\overline{IV}$ bus pins open.

Step 2: Increase V_{CC} to V_{CCP}.

Step 3: After V_{CC} has stabilized, apply a single programming pulse (Figure 2) to the user-bus bit that corresponds to the desired high-level $\overline{IV}$ address bit. The I/O port is programmed from the user bus (UD0-UD7) for addressing from the MicroController bus ($\overline{IV0}$-$\overline{IV7}$).

Step 4: Return V_{CC} to 0-volts. (Note. *If the programming of all address bits is completed in less than 1-second, V_{CC} can remain at 9.0-volts for the required interval of time.*)

Step 5: Step 1 through 3 are applicable to the programming of each address bit that requires a high-level $\overline{IV}$ match.

Table 3. PROGRAMMING SPECIFICATIONS

PARAMETERS	LIMITS			UNITS
	Min	Typ	Max	
V_{CCP} — Programming supply voltage				
Address	8.75	9.0	9.25	V
Protect		0		V
Maximum time V_{CCP} >5 25V			1 0	Sec
Programming voltage				
Address	8 75	9 0	9 25	V
Protect	8.75		9.25	V
Programming current				
Address			5	mA
Protect			50	mA
t_r — Programming pulse rise time				
Address	10		100	μS
Protect	10		100	μS
t_ω — Programming pulse width	0 5		1 0	mS

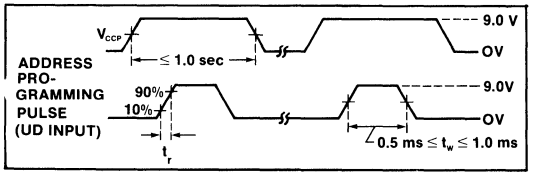


Figure 2. Address Programming Pulse

Step 6: To verify that the address is properly programmed, return V_{CC} to +5V, set $\overline{IV0}$-$\overline{IV7}$ to the desired (inverted) binary address pattern, set $\overline{ME}$ = WC = Low and SC = MCLK = High. If there are no programming errors, subsequent data written from $\overline{IV0}$-$\overline{IV7}$ (WC = High) will appear inverted on UD0-UD7.

Address Protect

After programming the I/O Port, steps should be taken to isolate the address circuits and make these circuits permanently immune to further change.

Step 1: Set V_{CC} and all control inputs to 0-volts (V_{CC} = $\overline{UIC}$ = $\overline{UOC}$ = $\overline{ME}$ = SC = WC = MCLK = 0V); $\overline{IV0}$-$\overline{IV7}$ = open circuit.

Step 2: Taking one pin at a time, apply a protect programming pulse (Figure 3) to each user-bus bit (UD0-UD7)—refer to Table 3 for min/max specifications pertaining to voltage and current.

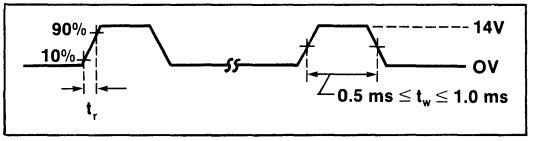


Figure 3. Protect Programming Pulse

Step 3: Verify that the address circuits for each bit is isolated by applying 9-volts, in turn, to each user-bus pin (UD0-UD7) and measuring less than 200 microamperes of input current. (Note. *Setup conditions are the same as those in Step 1.*)

DC ELECTRICAL CHARACTERISTICS

COMMERCIAL 4 75V ≤ V_{CC} ≤ 5.25V, 0°C ≤ T_A ≤ 70°C
MILITARY 4.5V ≤ V_{CC} ≤ 5 5V, -55°C ≤ T_C ≤ 125°C

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage[3]	+7	Vdc
V_{IN}	Input voltage[3]	+5 5	Vdc
T_{STG}	Storage temperature range	-65 to +150	°C

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.75	5	5 25	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2 0			2 0			V
V_{IL}	Low Level Input Voltage				0.8			0 8	V
V_{CL}	Input Clamp Voltage	V_{CC} = Min; I_I = -10mA			-1.5			-1.5	V
I_{IH}	High Level Input Current[1]	V_{CC} = Max; V_{IH} = 2.7V		5.0	100		5.0	100	μA
I_{IL}	Low Level Input Current[1]	V_{CC} = Max, V_{IL} = 0.5V		-350	-550		-350	-550	μA
V_{OL}	Low Level Output Voltage $\overline{IV}$ Bus ($\overline{IV0}$-$\overline{IV7}$)	V_{CC} = Min, I_{OL} = 16mA			0 55		0.55	V	
	User Bus (UD0-UD7)	V_{CC} = Min, I_{OL} = 24mA			0 55			0.55	V
V_{OH}	High Level Output Voltage	V_{CC} = Min; I_{OH} = -3.2mA	2 4			2.4			V
I_{OS}	Short Circuit Output Current[2] $\overline{IV}$ Bus ($\overline{IV0}$-$\overline{IV7}$)	V_{CC} = Max	-20			-20			mA
	UD Bus (UD0-UD7)	V_{CC} = Max	-10			-10			mA
I_{CC}	Supply Current	V_{CC} = Max, $\overline{ME}$ = $\overline{UOC}$ = V_{CC}		90	150		90	150	mA

NOTES:
1. The input current includes the Three-state leakage current of the output driver on the data lines.
2. Only one output may be shorted at a time.
3 These limits do not apply during address programming.

AC ELECTRICAL CHARACTERISTICS

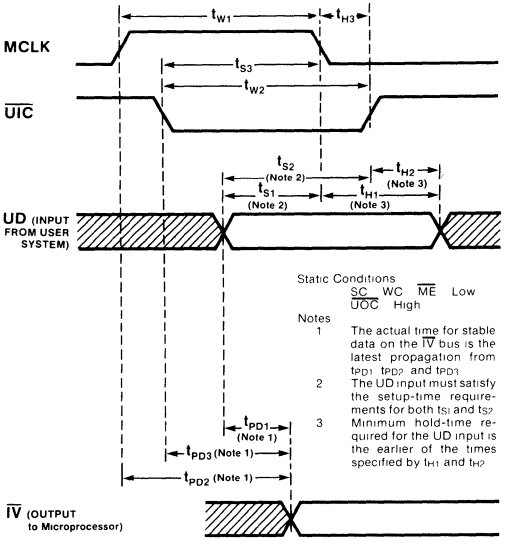
COMMERCIAL: 4.75V ≤ V_{CC} ≤ 5.25V, 0°C ≤ T_A ≤ 70°C
MILITARY: 4.5V ≤ V_{CC} ≤ 5.5V, -55°C = T_C ≤ 125°C
LOADING: See TEST LOADING CIRCUITS

PARAMETER	REFERENCES[1] FROM	REFERENCES[1] TO	TEST CONDITIONS	LIMITS (COMMERCIAL) Min	Typ	Max	LIMITS (MILITARY) Min	Typ	Max	UNIT
Pulse Widths:										
t_{W1} Clock High	↑MCLK	↓MCLK		35			35			ns
t_{W2} User Input Control	↓$\overline{UIC}$	↑$\overline{UIC}$	MCLK = High	35			35			ns
Propagation Delays:										
t_{PD1} UD Propagation Delay	UD	$\overline{IV}$	MCLK = High SC = WC = $\overline{ME}$ = $\overline{UIC}$ = Low			30			30	ns
t_{PD2} UD Clock Delay (8X732 only)	↑MCLK	$\overline{IV}$	UD = Stable, SC = WC = $\overline{ME}$ = $\overline{UIC}$ = Low			50			50	ns
t_{PD3} UD Input Delay	↓$\overline{UIC}$	$\overline{IV}$	UD = Stable, MCLK = High; SC = WC = $\overline{ME}$ = Low			50			50	ns
t_{PD4} $\overline{IV}$ Data Propagation Delay	$\overline{IV}$	UD	MCLK = WC = $\overline{UIC}$ = High, $\overline{ME}$ = $\overline{UOC}$ = SC = Low			45			45	ns
t_{PD5} $\overline{IV}$ Data Clock Delay	↑MCLK	UD	WC = $\overline{UIC}$ = High; $\overline{IV}$ = Stable, $\overline{ME}$ = $\overline{UOC}$ = SC = Low			55			55	ns
Output Enable Timing:										
t_{OE1} UD Output Enable	↓$\overline{UOC}$	UD	$\overline{UIC}$ = High			30			30	ns
t_{OE2} UD Input Recovery	↑$\overline{UIC}$	UD	$\overline{UOC}$ = Low			30			30	ns
t_{OE3} $\overline{IV}$ Data Master Enable	↓$\overline{ME}$	$\overline{IV}$	WC = SC = Low			22			25	ns
t_{OE5} $\overline{IV}$ Data Write Recovery	↓WC	$\overline{IV}$	SC = $\overline{ME}$ = Low			25			25	ns
t_{OE6} $\overline{IV}$ Data Select Recovery	↓SC	$\overline{IV}$	SC = $\overline{ME}$ = Low			25			25	ns
Output Disable Timing:										
t_{OD1} UD Output Disable	↑$\overline{UOC}$	UD	$\overline{UIC}$ = High			25			25	ns
t_{OD2} UD Input Override	↓$\overline{UIC}$	UD	$\overline{UOC}$ = Low			30			30	ns
t_{OD3}[2] $\overline{IV}$ Data Master Disable	↑$\overline{ME}$	$\overline{IV}$	WC = SC = Low			20			20	ns
t_{OD4}[2] $\overline{IV}$ Data Write Override	↑WC	$\overline{IV}$	SC = $\overline{ME}$ = Low			20			20	ns
t_{OD5}[2] $\overline{IV}$ Data Select Override	↑SC	$\overline{IV}$	WC = $\overline{ME}$ = Low			20			20	ns
Setup Times:										
t_{S1} UD Clock Setup Time (8X372 only)	UD	↓MCLK	$\overline{UIC}$ = Low	15			15			ns
t_{S2} UD Control Setup Time	UD	↑$\overline{UIC}$	MCLK = High	15			15			ns
t_{S3} User Input Control Setup Time (8X372 only)	↓$\overline{UIC}$	↓MCLK		25			25			ns
t_{S4} $\overline{IV}$ Data Setup Time	$\overline{IV}$	↓MCLK	WC = High or SC = High, $\overline{ME}$ = Low, $\overline{UIC}$ = High	35			35			ns
t_{S5}[3] $\overline{IV}$ Master Enable Setup Time	↓ME	↓MCLK	WC = High or SC = High, $\overline{UIC}$ = High	30			30			ns
t_{S6} $\overline{IV}$ Write Control Setup Time	↑WC	↓MCLK	SC = $\overline{ME}$ = Low, $\overline{UIC}$ = High	30			30			ns

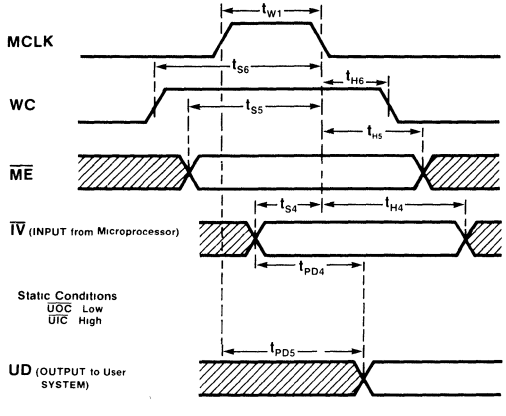
AC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER	REFERENCES FROM	REFERENCES TO	TEST CONDITIONS	LIMITS (COMMERCIAL) Min	Typ	Max	LIMITS (MILITARY) Min	Typ	Max	UNIT
t_{S7} $\overline{IV}$ Select Control Setup Time	↑SC	↓MCLK	WC = $\overline{ME}$ = Low	30			30			ns
Hold Times:										
t_{H1} UD Clock Hold Time (8X372 only)	↓MCLK	UD	$\overline{UIC}$ = Low	15			15			ns
t_{H2} UD Control Hold Time	↑$\overline{UIC}$	UD	MCLK = High	15			15			ns
t_{H3} User Input Control Hold Time (8X372 only)	↓MCLK	↑$\overline{UIC}$		0			0			ns
t_{H4} $\overline{IV}$ Data Hold Time	↓MCLK	$\overline{IV}$	WC = High or SC = High; $\overline{ME}$ = Low, $\overline{UIC}$ = High	5			5			ns
t_{H5}[3] $\overline{IV}$ Master Enable Hold Time	↓MCLK	↑$\overline{ME}$	WC = High or SC = High, $\overline{UIC}$ = High	0			0			ns
t_{H6} $\overline{IV}$ Write Control Hold Time	↓MCLK	↓WC	SC = $\overline{ME}$ = Low, $\overline{UIC}$ = High	0			0			ns
t_{H7} $\overline{IV}$ Select Control Hold Time	↓MCLK	↓SC	WC = $\overline{ME}$ = Low	0			0			ns

Notes
1 All measurements to the $\overline{IV}$ bus assumes the address selection latch is set
2 These parameters are measured with a capacitive loading of 50pf and represent the output driver turn-off time
3 If $\overline{ME}$ is to be high (inactive), it must be setup before the rising edge and held after the falling edge of MCLK to avoid unintended writing into or selection of the I/O port.



a. User Data Input Timing

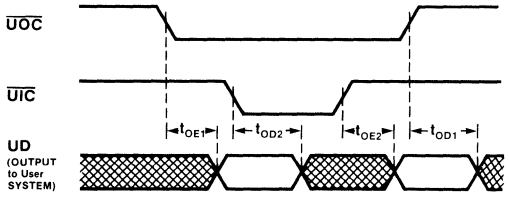


c. MicroController Write Cycle Timing

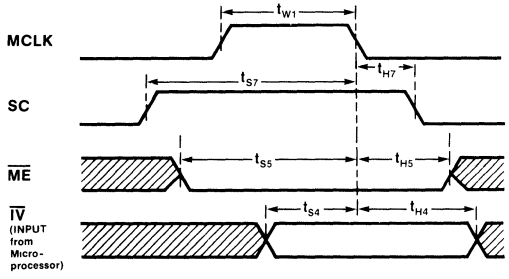
Legend:

= THREE-STATE

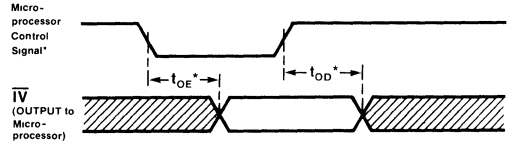
= CHANGING DATA



b. User Data Output Enable



d. MicroController Seclect Cycle Timing



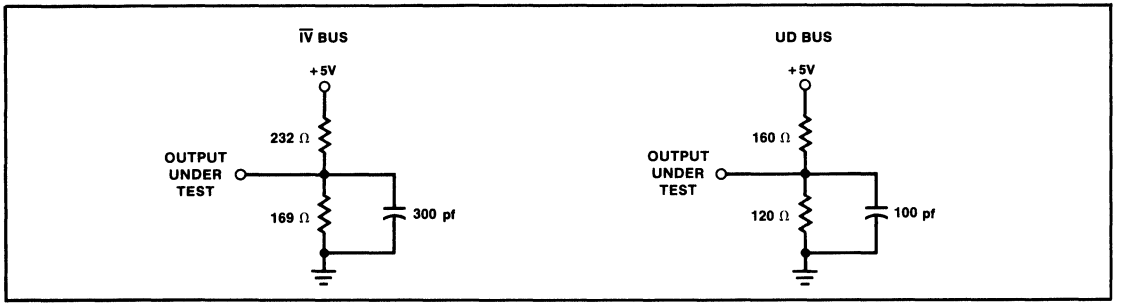
*PARAMETER KEY

MICROPROCESSOR CONTROL SIGNAL	AC TIMING PARAMETERS	STATIC CONDITIONS
ME	t_{OE3} t_{OD3}	SC = WC = LOW
WC	t_{OE5} t_{OD5}	SC = ME = LOW
SC	t_{OE6} t_{OD6}	WC = ME = LOW

e. MicroController Output Enable Timing

Figure 2. Timing Diagram

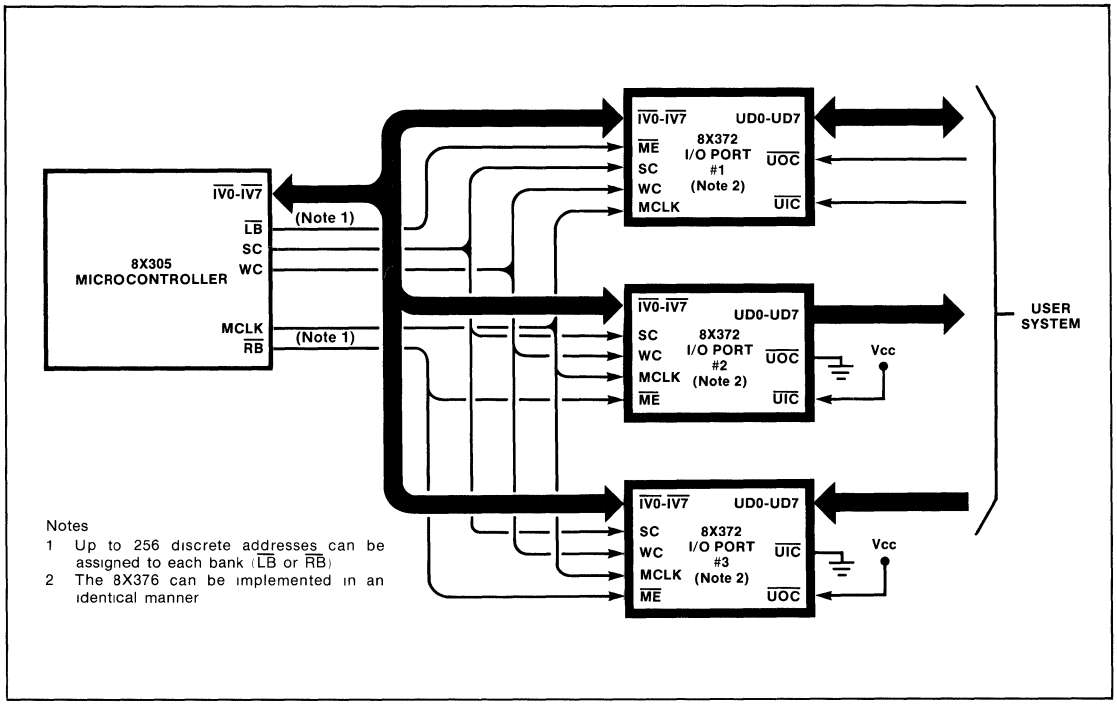
TEST LOADING CIRCUITS



ADDRESSABLE/BIDIRECTIONAL I/O PORTS 8X372/8X376

APPLICATIONS

One way of using I/O Ports in a microprocessor-based system is shown in the following application diagram; there are many other ways of implementing I/O functions with these parts, both singly and in combination. By proper control of the $\overline{UIC}$ and $\overline{UOC}$ lines, the user can implement bidirectional data transfers, exercise system control, and/or read system status. In the concept shown here, I/O Port #1 is setup for bidirectional data transfers and I/O Ports #2 and #3, respectively, serve as dedicated output and input devices.



ADDRESSABLE/BIDIRECTIONAL I/O PORT WITH PARITY 8X374

FEATURES

- **Two bidirectional 8-bit busses**
- **Independent bus operation (user bus priority for data entry)**
- **Parity generate/check logic with:**
  Odd/Even parity select
  Strobed error flag output
- **Synchronous data input**
- **Programmable MicroController port address**
- **Three-state TTL outputs (for all except parity error flag)**
- **High drive capabilities**
- **Power-up to predetermined state**
- **Directly compatible with 8X305 MicroController**
- **Single +5V supply**
- **0.6 inch, 28-pin DIP**

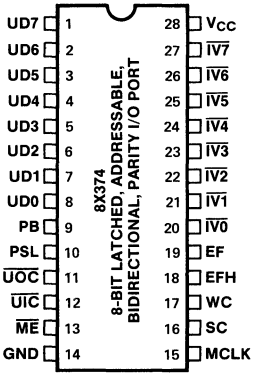
PRODUCT DESCRIPTION

The Signetics 8X374 is an addressable 8-bit I/O Port that features on-chip parity generate/check logic. The 8X374 port is designed for applications that require an 8-bit bidirectional interface element with parity-generate and parity-check capabilities. Typically, the 8X374 is used with the 8X305 MicroController and its associated Interface Vector (IV) bus.

As shown in the logic diagram of Figure 1, the 8X374 consists of eight identical latches, bits 0 through 7. These latches are accessed through either of two 8-bit busses, one connecting to the MicroController (IV bus) and the other to the user system (UD bus). Separate controls are provided for each bus and both busses operate independently, except when both attempt to input data at the same time. In such situations, the user bus always has priority. The data latches are transparent, in that, while either bus is enabled for input, all transitions in input data are propagated to the other bus, if enabled for output. The data latch in Figure 1 is common to both busses, that is, data traveling from the IV bus to the UD bus, or vice-versa, is latched and applied to the parity generate/check logic. The parity-bit latch is interfaced to the UD bus and latches the parity bit. The user can implement the parity features of the chip by simply selecting odd or even parity via the Parity SeLect (PSL) input pin. When data is output to the UD bus, a parity bit is generated and appended to each byte of data; for incoming data, parity is checked and the result is transmitted to an error-flag latch. The status of the latch (0 = no parity error/1 = parity error) is reflected by the Error Flag (EF) output pin. Operation of the error-flag latch is controlled by the Error Flag Hold (EFH) signal. With EFH low, the operation is transparent; when high the contents of the latch are frozen to avoid false errors while data latches are changing.

8X374 PACKAGE AND PIN DESIGNATIONS

N,F PACKAGE



TOP VIEW

ORDER NUMBERS

N8X374N, N8X374F
S8X374F/883B, S8X374F/883C

Pin No.	Identifier	Function
1-8	UD7-UD0	Three-state bidirectional User Data (UD) bus; UD0 corresponds to $\overline{IV0}$.
9	PB	User port Parity Bit I/O pin.
10	PSL	Parity SeLect input control; even parity = 1 and odd parity = 0.
11	$\overline{UOC}$	User Output Control — active low input to enable data output from UD0-UD7.
12	$\overline{UIC}$	User Input Control — active low input to enable data input from UD0-UD7.
13	$\overline{ME}$	Master Enable — active low input to enable the IV bus for data input, data output, or IV address selection/deselection; UD-bus operations are unaffected.
14	GND	Ground
15	MCLK	Master Clock — active high input from MicroController used to strobe data into the data latches; MCLK also synchronizes IV address selection.
16	SC	Select Command — active high input from MicroController to enable IV address input from the IV bus for device selection.
17	WC	Write Command — active high input from MicroController to enable the writing of data into the data latches from the IV bus, provided $\overline{UIC}$ is not low.
18	EFH	Error Flag Hold signal to control error-flag latch. When low, latch operation is transparent; when high, contents of latch are frozen.
19	EF	Error Flag output; no parity error = 0 parity error = 1.
20-27	$\overline{IV0}$-$\overline{IV7}$	Interface Vector (Input/Output Bus), three-state, bidirectional, MicroController data bus; $\overline{IV0}$ corresponds to UD0.
28	VCC	+5V power supply.

ADDRESSABLE/BIDIRECTIONAL I/O PORT WITH PARITY 8X374

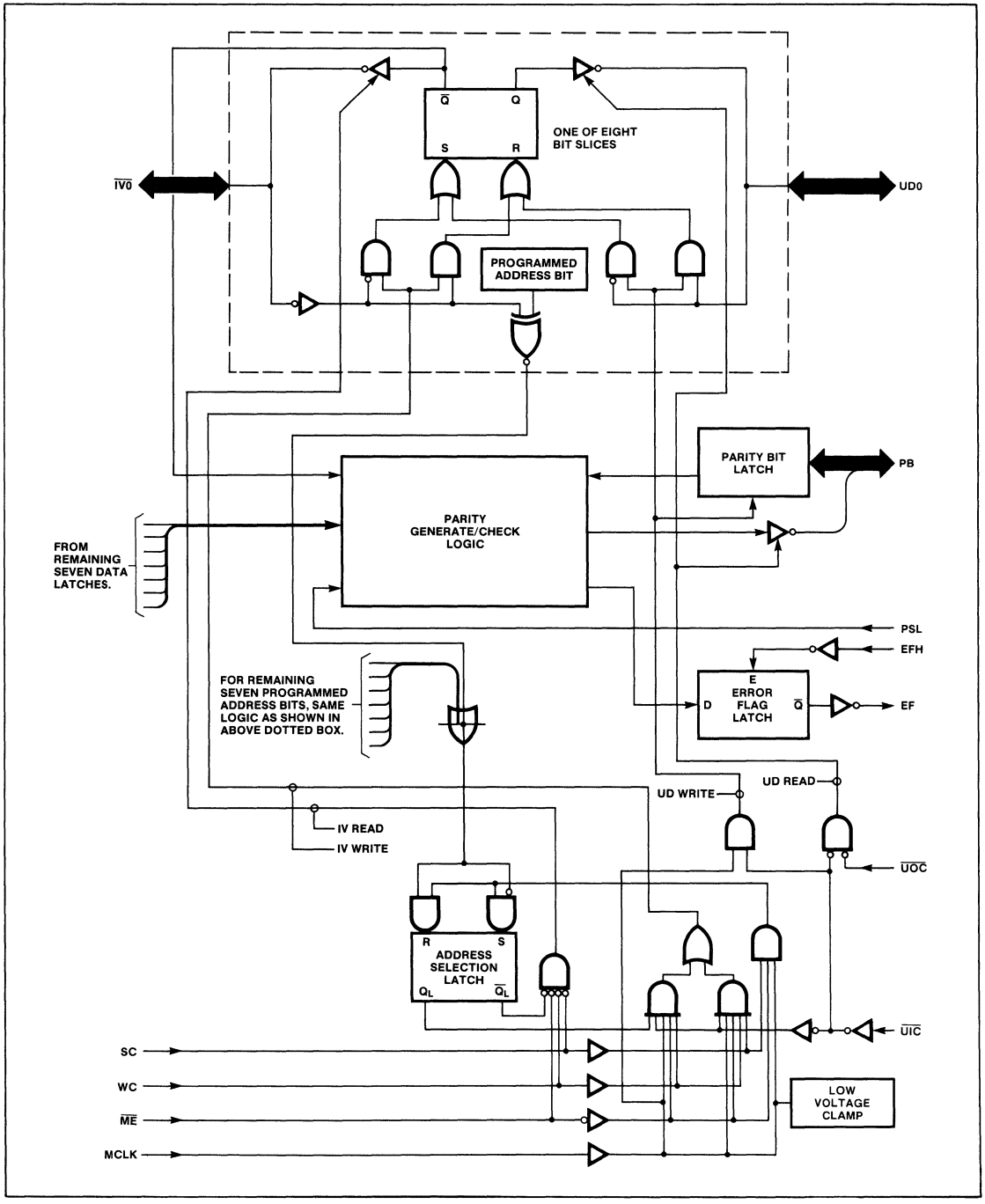


Figure 1. Logic Diagram for 8X374 I/O Port

The 8X374 is available with either preprogrammed addresses (0_{10} to 255_{10}) or unprogrammed; the device can be field-programmed over the same address range as the preprogrammed port. Input/Output operations to the MicroController bus can begin once the 8X374 enabling address has been selected and appropriate control signals from the IV bus are generated. Port selection is implemented by putting the 8X374 address (0_{10} to 255_{10}) on the IV bus. Once selected, the I/O port remains selected until a different port address is put on the bus.

With appropriate control inputs, data is accessible on the UD bus at all times. A Master Enable (ME) input, which is typically connected to the Left Bank (LB) or Right Bank (RB) output of the MicroController, provides the capability of organizing the IV bus into two separate and independent banks of I/O devices.

FUNCTIONAL OPERATION

UD Bus Control

As shown in Table 1, the User Data (UD) bus and parity-bit interface are controlled by the UIC and UOC inputs. Data from the UD bus is written synchronously with MCLK, that is with UIC low, information is written into the data latches only when MCLK is high. Output drivers on the UD bus are enabled when UOC is low and UIC is high.

Table 1. INPUT/OUTPUT CONTROL OF UD BUS

			Function of UD Bus	
UIC	UOC	MCLK	8-Bit Data Bus	Parity Bit
H	L	X	Output data	Output parity
L	X	H	Input data	Input parity
L	X	L	Inactive	Inactive
H	H	X	Inactive	Inactive

X = Don't Care

IV Bus Control

Input/Output control of the IV bus is shown in Table 2; this bus is controlled by SC, WC, ME, MCLK and the current state of the internal address selection latch. As shown in Table 2, UIC is required to indicate priority of the UD bus for data input operations. The selection latch in the I/O port stores the result of the most recent IV address selection. The latch is set when the internally preprogrammed address of the port matches the address on the IV bus during an address-selection operation (SC = MCLK = High; ME = WC = Low). The latch is cleared when the two 8-bit address patterns are in disagreement. The IV bus can transfer data only when the selection latch is set. As shown in the APPLICATION DIAGRAM, the 8X305 Left Bank (LB) and Right Bank (RB) outputs can control the ME inputs for two banks of I/O devices, thus, acting as a ninth address bit.

Table 2. INPUT/OUTPUT CONTROL OF IV BUS

ME	SC	WC	MCLK	UIC	Selection Latch	Function of IV Bus
L	L	L	X	X	Set	Output Data
L	L	H	H	H	Set	Input Data
L	H	L	H	X	X	Input Address*
L	X	H	L	X	X	Inactive
L	H	X	L	X	X	Inactive
L	L	H	H	L	X	Inactive
L	L	X	X	X	Not Set	Inactive
H	X	X	X	X	X	Inactive

X = Don't Care *Selection latch is updated.

Data is written into the data latches of a selected device from the IV bus when WC, MCLK and UIC are all high and ME is low. To prevent data-input conflicts, inputs from the IV bus are inhibited when UIC is low, under all other conditions, the IV and UD busses operate independently. Output drivers on the IV bus of a selected device are enabled when ME, WC, and SC are all low and the address selection latch is set.

Parity Generate/Check Logic

The Parity Bit (PB) pin provides both parity-generate and parity-check capabilities according to user data bus controls. With UIC low (active), a parity check is performed on the input data stream; with UOC low (active) and UIC high, the 8X374 generates the parity-bit for the output data stream. The user can select odd or even parity via the Parity SeLect (PSL) input control, 1 = even parity and 0 = odd parity. As data and parity are input to the data latches and the parity-bit latch from the UD bus and PB line (Figure 1), parity errors (if any) are continuously detected by the parity-check logic. Parity error status enters the error flag latch (if enabled) and appears at the EF output pin. The error latch can be strobed by the Error Flag Hold (EFH) control to latch in valid error status; otherwise, the error flag is transparent to the user. (Note: If the sytem uses less than eight data bits, keeping zeros in unused data latches preserves proper parity operation.)

Bus Logic Levels

Data written into the I/O port from either bus will appear inverted when read from the other bus. Data written into either bus will not be inverted when read from the same bus. (Note: A logic "1" in MicroController software corresponds to a high level on the UD bus even though the IV bus

is inverted.) The 8X374 wakes up with the address selection latch in the unselected state, all data bits latched at the "logic 1" level (UD bus outputs high if enabled), and the EF output high.

ADDRESS PROGRAMMING AND ADDRESS PROTECT

Programming Procedures

The 8X374 can be programmed to respond to any address within a range of 0_{10} through 255_{10}. In an unprogrammed state, low level (≤ 0.8 V) inputs on all IV bus lines (address 255_{10}) will select the device. To program a given address bit to match a high level (≥ 2.0 V) input on the corresponding IV pin (a logical "0" to the MicroController), the counterpart UD-bus pin must be pulsed according to Table 3 and the following procedures:

Step 1: Set all control inputs to the inactive state, UIC = UOC = ME = V_{CC} and SC = WC = MCLK = 0 V; leave the UD and IV bus pins open.

Table 3. PROGRAMMING SPECIFICATIONS

Parameters	Limits Min.	Typ.	Max.	Units
V_{CCP} — Programming supply voltage:				
Address	8.75	9.0	9.25	V
Protect		0		V
Maximum Time V_{CC} > 5.25 V			1.0	sec
Programming voltage:				
Address	8.75	9.0	9.25	V
Protect	8 75		9.25	V
Programming current:				
Address			5	mA
Protect			50	mA
t_r — Programming pulse rise time:				
Address	10		100	μs
Protect	10		100	μs
t_W — Programming pulse width	0.5		1.0	ms

Step 2: Increase V_{CC} to V_{CCP}.

Step 3: After V_{CC} has stabilized, apply a single programming pulse (Figure 2) to the user-bus bit that corresponds to the desired high-level IV address bit. The I/O port is programmed from the user bus (UD0-UD7) for addressing from the MicroController bus (IV0-IV7).

Step 4: Return V_{CC} to 0 volts. (Note: If the programming of all address bits is completed in less than one second, V_{CC} can remain at V_{CCP} for the required interval of time.)

Step 5: Step 1 through Step 3 are applicable to the programming of each address bit that requires a high-level IV match.

Step 6: To verify that the address is properly programmed, return V_{CC} to +5 V and set IV0-IV7 to the desired address pattern (inverted). Set ME = WC = Low and SC = MCLK = High to select the programmed I/O port. With ME = SC = Low and WC = MCLK = High, write an 8-bit pattern to the port. If there are no programming errors, the transmitted data pattern will appear inverted at UD0-UD7 of selected port.

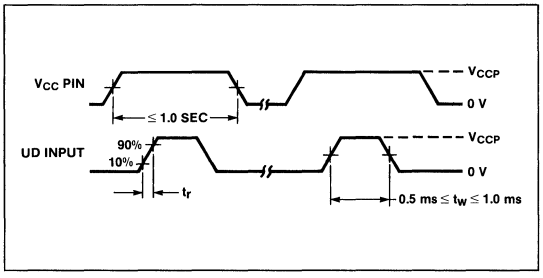


Figure 2. Address Programming Pulse

ADDRESS PROTECT

After programming the I/O Port, optional steps can be taken to isolate the fuse circuits and to make these circuits permanently immune to further change.

Step 1: Set V_{CC} and all control inputs to 0 volts, V_{CC} = UIC = UOC = ME = SC = WC = MCLK = 0V, IV0-IV7 = open circuit.

Step 2: Taking one pin at a time, apply a protect programming pulse (Figure 3) to each user-bus bit (UD0-UD7). Refer to Table 3 for min/max specifications pertaining to voltage and current.

Step 3: Verify that the address circuits for each bit are isolated by applying V_{CCP}, in turn, to each user-bus pin (UD0-UD7) and measuring less than 200 microamperes of input current. (Note: Setup conditions are the same as those in Step 1.)

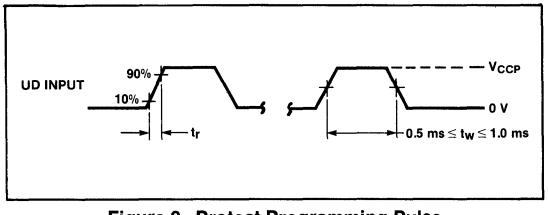


Figure 3. Protect Programming Pulse

ABSOLUTE MAXIMUM RATINGS

	Parameter	Rating	Unit
V_{CC}	Power supply voltage[3]	+7	V DC
V_{IN}	Input voltage[3]	+5.5	V DC
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

COMMERCIAL: V_{CC} = 5 V (±5%); $T_A \geq 0°C$
$T_A \leq 70°C$
MILITARY: V_{CC} = 5 V (±10%); $T_A \geq -55°C$
$T_C \leq 125°C$

Parameter		Test Conditions	Limits (Commercial)			Limits (Military)			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
V_{CL}	Input Clamp Voltage	V_{CC} = Min; I_I = -10 mA			-1.5			-1.5	V
I_{IH}	High Level Input Current[1]	V_{CC} = Max; V_{IH} = 2.7 V		5.0	100		5.0	250	μA
I_{IL}	Low Level Input Current[1]	V_{CC} = Max; V_{IL} = 0.5 V		-350	-550		-350	-550	μA
V_{OL}	Low Level Output Voltage $\overline{IV}$ Bus ($\overline{IV0}$-$\overline{IV7}$)	V_{CC} = Min; I_{OL} = 16 mA			0.55			0.55	V
	User Bus (UD0-UD7) and PB	V_{CC} = Min; I_{OL} = 24 mA			0.55			0.55	V
	EF	V_{CC} = Min; I_{OL} = 8 mA			0.55			0.55	V
V_{OH}	High Level Output Voltage EF	V_{CC} = Min; I_{OH} = -1 mA	2.4			2.4			V
	Others	V_{CC} = Min; I_{OH} = -3.2 mA	2.4			2.4			V
I_{OS}	Short Circuit Output Current[2] $\overline{IV}$ Bus ($\overline{IV0}$-$\overline{IV7}$)	V_{CC} = Max	-20			-20			mA
	UD Bus (UD0-UD7)	V_{CC} = Max	-10			-10			mA
I_{CC}	Supply Current	V_{CC} = Max; $\overline{ME}$ = $\overline{UOC}$ = V_{CC}		90	150		90	160	mA

Notes:
1. The input current includes the high-Z leakage current of the output drivers ($\overline{IV0}$-$\overline{IV7}$, UD0-UD7) on the data lines.
2. Only one output may be shorted at a time for testing purposes.
3. These limits do not apply during address programming.

AC ELECTRICAL CHARACTERISTICS

COMMERCIAL: V_{CC} = 5 V (±5%); $T_A \geq 0°C$, $T_A \leq 70°C$
MILITARY: V_{CC} = 5 V (±10%); $T_A \geq -55°C$, $T_C \leq 125°C$
LOADING: See TEST LOADING CIRCUITS

Parameter		References From	References To	Test Conditions[1]	Limits (Commercial) Min	Typ	Max	Limits (Military) Min	Typ	Max	Unit
Pulse Widths:											
t_{W1}	Clock High	↓MCLK	↓MCLK		35			35			ns
t_{W2}	User Input Control	↓$\overline{UIC}$	↑$\overline{UIC}$	MCLK = High	35			35			ns
Propagation Delays:											
t_{PD1}	UD Propagation Delay	UD	$\overline{IV}$	MCLK = High SC = WC = $\overline{ME}$ = $\overline{UIC}$ = Low			40			40	ns
t_{PD2}	UD Clock Delay	↑MCLK	$\overline{IV}$	UD = Stable; SC = WC = $\overline{ME}$ = $\overline{UIC}$ = Low			50			50	ns
t_{PD3}	UD Input Delay	↓$\overline{UIC}$	$\overline{IV}$	UD = Stable; MCLK = High; SC = WC = $\overline{ME}$ = Low			50			50	ns
t_{PD4}	$\overline{IV}$ Data Propagation Delay	$\overline{IV}$	UD	MCLK = WC = $\overline{UIC}$ = High; $\overline{ME}$ = $\overline{UOC}$ = SC = Low			45			45	ns
t_{PD5}	$\overline{IV}$ Data Clock Delay	↑MCLK	UD	WC = $\overline{UIC}$ = High; $\overline{IV}$ = Stable, $\overline{ME}$ = $\overline{UOC}$ = SC = Low			55			55	ns
t_{PD6}	Error Flag Propagation Delay	UD, PB	EF	MCLK = High; $\overline{UIC}$ = EFH = Low			55			55	ns
t_{PD7}	Parity Generate Propagation Delay	$\overline{IV}$	PB	MCLK = WC = $\overline{UIC}$ = High; $\overline{UOC}$ = $\overline{ME}$ = Low			55			55	ns
t_{PD8}	Error Flag Strobe Delay[3]	↓EFH	EF				20			20	ns
Output Enable Timing:											
t_{OE1}	UD Output Enable	↓$\overline{UOC}$	UD, PB	$\overline{UIC}$ = High			30			30	ns
t_{OE2}	UD Input Recovery	↑$\overline{UIC}$	UD, PB	$\overline{UOC}$ = Low			30			30	ns
t_{OE3}	$\overline{IV}$ Data Master Enable	↓$\overline{ME}$	$\overline{IV}$	WC = SC = Low			22			25	ns
t_{OE4}	$\overline{IV}$ Data Write Recovery	↓WC	$\overline{IV}$	SC = $\overline{ME}$ = Low			25			25	ns
t_{OE5}	$\overline{IV}$ Data Select Recovery	↓SC	$\overline{IV}$	SC = $\overline{ME}$ = Low			25			25	ns

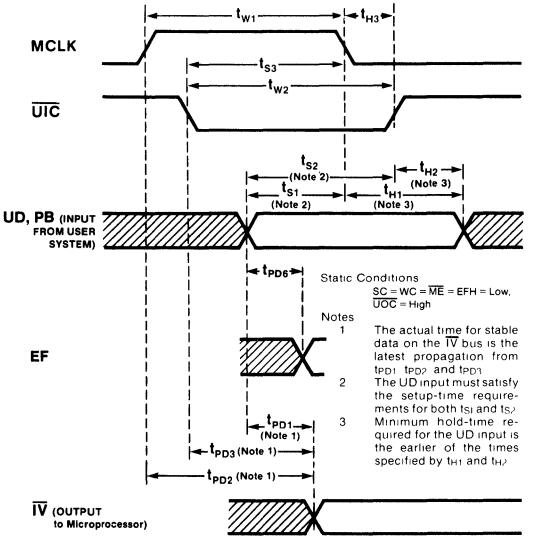
AC ELECTRICAL CHARACTERISTICS (Continued)

Parameter	References		Test Conditions[1]	Limits (Commercial)			Limits (Military)			Unit
	From	To		Min	Typ	Max	Min	Typ	Max	
Output Disable Timing:										
t_{OD1} UD Output Disable	↓$\overline{UOC}$	UD, PB	$\overline{UIC}$ = High			25			25	ns
t_{OD2} UD Input Override	↓$\overline{UIC}$	UD, PB	$\overline{UOC}$ = Low			30			30	ns
t_{OD3} $\overline{IV}$ Data Master Disable	↓$\overline{ME}$	$\overline{IV}$	WC = SC = Low			20			20	ns
t_{OD4} $\overline{IV}$ Data Write Override	↓WC	$\overline{IV}$	SC = $\overline{ME}$ = Low			20			20	ns
t_{OD5} $\overline{IV}$ Data Select Override	↓SC	$\overline{IV}$	WC = $\overline{ME}$ = Low			20			20	ns
Setup Times:										
t_{S1} UD Clock Setup Time	UD, PB	↑MCLK	$\overline{UIC}$ = Low	15			15			ns
t_{S2} UD Control Setup Time	UD, PB	↓$\overline{UIC}$	MCLK = High	15			15			ns
t_{S3} User Input Control Setup Time	↓$\overline{UIC}$	↑MCLK		25			25			ns
t_{S4} $\overline{IV}$ Data Setup Time	$\overline{IV}$	↑MCLK	WC = High or SC = High; $\overline{ME}$ = Low; $\overline{UIC}$ = High	35			35			ns
t_{S5}[2] $\overline{IV}$ Master Enable Setup Time	↑$\overline{ME}$	↑MCLK	WC = High or SC = High, $\overline{UIC}$ = High	30			30			ns
t_{S6} $\overline{IV}$ Write Control Setup Time	↑WC	↑MCLK	SC = $\overline{ME}$ = Low; $\overline{UIC}$ = High	30			30			ns
t_{S7} $\overline{IV}$ Select Control Setup Time	↑SC	↑MCLK	WC = $\overline{ME}$ = Low	30			30			ns
Hold Times:										
t_{H1} UD Clock Hold Time	↑MCLK	UD, PB	$\overline{UIC}$ = Low	15			15			ns
t_{H2} UD Control Hold Time	↓$\overline{UIC}$	UD, PB	MCLK = High	15			15			ns
t_{H3} User Input Control Hold Time	↑MCLK	↓$\overline{UIC}$		0			0			ns
t_{H4} $\overline{IV}$ Data Hold Time	↑MCLK	$\overline{IV}$	WC = High or SC = High, $\overline{ME}$ = Low, $\overline{UIC}$ = High	5			5			ns
t_{H5}[2] $\overline{IV}$ Master Enable Hold Time	↑MCLK	↑$\overline{ME}$	WC = High or SC = High; $\overline{UIC}$ = High	0			0			ns
t_{H6} $\overline{IV}$ Write Control Hold Time	↑MCLK	↑WC	SC = $\overline{ME}$ = Low; $\overline{UIC}$ = High	0			0			ns
t_{H7} $\overline{IV}$ Select Control Hold Time	↑MCLK	↑SC	WC = $\overline{ME}$ = Low	0			0			ns

Notes:
1 All measurements to the $\overline{IV}$ bus assumes the address selection latch is set
2 If $\overline{ME}$ is to be high (inactive), it must be setup before the rising edge and held after the falling edge of MCLK to avoid unintended writing into or selection of the I/O port.
3 Parameters are measured by holding $\overline{UIC}$ = High and MCLK = Low and changing the state of the PSL input before each EFH pulse.

TIMING DIAGRAMS

USER DATA INPUT TIMING



Static Conditions
$\overline{SC}$ = WC = $\overline{ME}$ = EFH = Low,
$\overline{UOC}$ = High

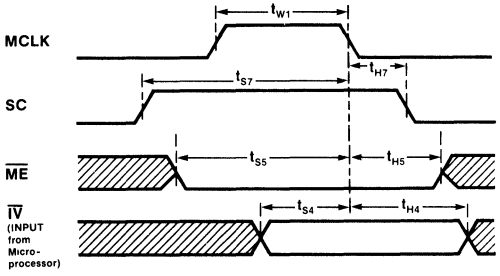
Notes
1. The actual time for stable data on the $\overline{IV}$ bus is the latest propagation from t_{PD1}, t_{PD2} and t_{PD3}.
2. The UD input must satisfy the setup-time requirements for both t_{S1} and t_{S2}.
3. Minimum hold-time required for the UD input is the earlier of the times specified by t_{H1} and t_{H2}.

Legend:

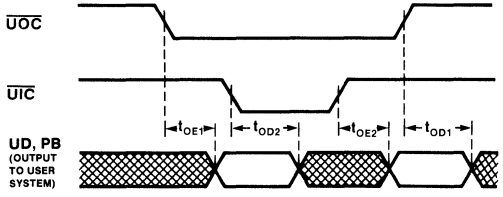
= HIGH-Z STATE

= CHANGING DATA

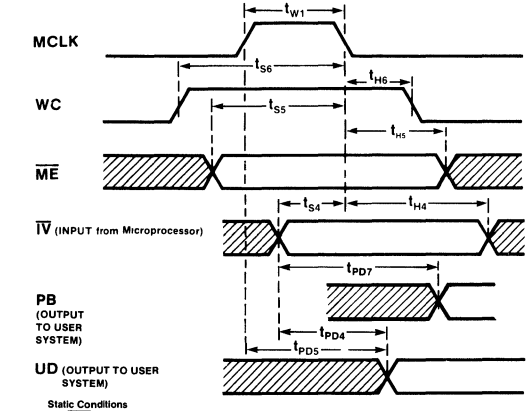
MICROCONTROLLER SELECT CYCLE TIMING



USER DATA OUTPUT ENABLE TIMING

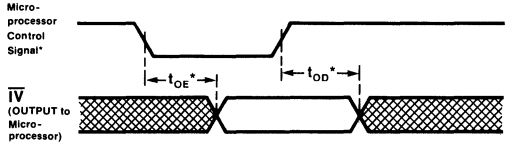


MICROCONTROLLER WRITE CYCLE TIMING



Static Conditions
$\overline{UOC}$ = Low
$\overline{UIC}$ = High

MICROCONTROLLER OUTPUT ENABLE TIMING

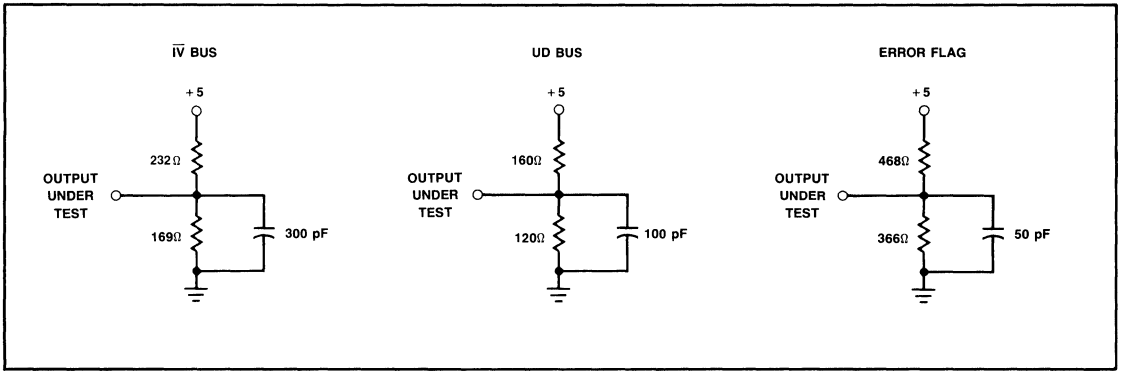


*PARAMETER KEY

MICROPROCESSOR CONTROL SIGNAL	AC TIMING PARAMETERS	STATIC CONDITIONS
$\overline{ME}$	t_{OE3} t_{OD3}	SC = WC = LOW
WC	t_{OE5} t_{OD5}	SC = $\overline{ME}$ = LOW
SC	t_{OE6} t_{OD6}	WC = $\overline{ME}$ = LOW

ADDRESSABLE/BIDIRECTIONAL I/O PORT WITH PARITY 8X374

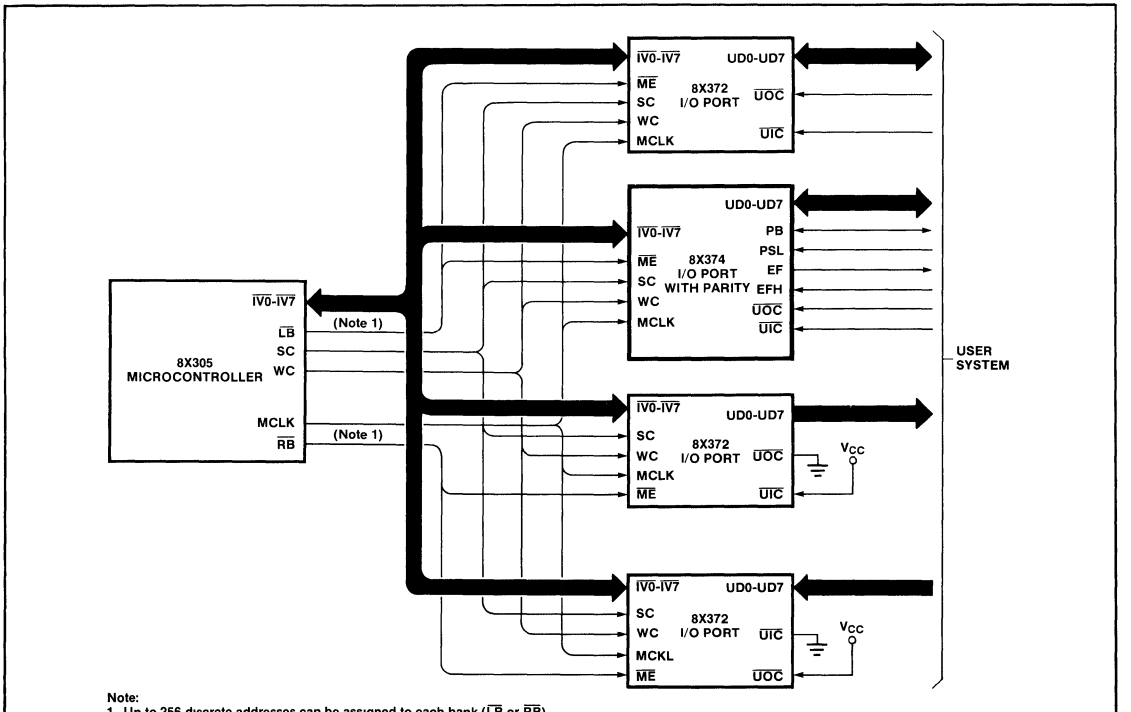
TEST LOADING CIRCUITS



APPLICATIONS

As shown in the following diagram, the 8X374 can be used with other I/O ports to provide a complete range of input/output functions By proper control of the UIC and UOC lines, the user can perform bidirectional data transfers, exercise system control, read system status and, by using the 8X374, implement a bidirectional parity-controlled data stream To use the parity capabilities, the user need only select even or odd parity (PSL = 1 or 0) and connect the PB pin to the system parity bit The EFH and EF pins can be wired according to system requirements

APPLICATIONS DIAGRAM



Note:
1. Up to 256 discrete addresses can be assigned to each bank ($\overline{LB}$ or $\overline{RB}$).

4-INPUT/4-OUTPUT ADDRESSABLE I/O PORT — 8X382

FEATURES

- **Bidirectional 8-bit MicroController ($\overline{IV}$) bus**
- **User bus—four input bits and four output bits**
- **Independent bus operation**
- **Synchronous user data input**
- **Programmed MicroController port address**
- **Three-state TTL outputs with high-drive capabilities**
- **Power-up to predetermined logic state**
- **Directly compatible with 8X305 or 8X300 MicroControllers**
- **Single +5V supply**
- **0.4 inch 24-pin DIP**

PRODUCT DESCRIPTION

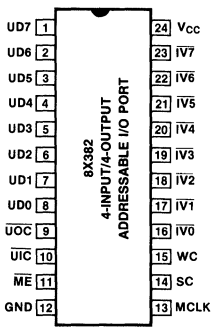
The 8X382 I/O Port is an addressable, three-state device designed for use as an interface element in systems that use TTL-compatible busses. Typically, the 8X382 is used with the 8X305 MicroController and its associated Interface Vector ($\overline{IV}$) bus; however, it can also be used with the 8X300 MicroController or an equivalent microprocessor. The 8X382 is functionally the same and pin-for-pin compatible with the older 8X42; however, the new port features better performance, increased drive current, and improved programming procedures.

As shown in the logic diagram of Figure 1, the I/O port consists of eight data latches—bits 0 through 7. These latches are accessed through either of two busses—an 8-bit bidirectional $\overline{IV}$ bus connected to the MicroController and a User Data (UD) bus consisting of four dedicated inputs (bits UD0 through UD3) and four dedicated outputs (bits UD4 through UD7). All eight bits may be read from or four data bits ($\overline{IV4}$-$\overline{IV7}$) can be written into via the $\overline{IV}$ bus; eight bits of I/O address can be written from the $\overline{IV}$ bus. Separate controls are provided for each bus and both busses operate independently. The I/O data latches are transparent, in that, when either bus is enabled for input, all transitions in input data are propagated to the other bus, if that bus in enabled for output.

The 8X382 is available with preprogrammed addresses (0_{10} through 255_{10}); it can also be field-programmed over the same address range. Input/output operations can begin once the I/O port is selected and appropriate control signals are generated. Port selection is implemented by putting the I/O port address (0_{10}-255_{10}) on the $\overline{IV}$ bus; once selected, the I/O port remains selected until a different "port address" is put on the bus. Thus, software overhead is minimized. Data is accessible on the UD bus at all times. A Master Enable ($\overline{ME}$) input, which is typically connected to the Left Bank ($\overline{LB}$) or Right Bank ($\overline{RB}$) output of the MicroController, provides the capability of organizing the $\overline{IV}$ bus into two separate and independent banks of I/O devices.

8X382 PACKAGE and PIN DESIGNATIONS

N, I PACKAGE



TOP VIEW

ORDER NUMBERS

N8X382N, N8X382I
S8X382I/883B, 8X382I/883C

PIN NO.	IDENTIFIER	FUNCTION
1-4	UD7-UD4	Three-state, dedicated output lines for user data, UD7 corresponds to $\overline{IV7}$
5-8	UD3-UD0	Dedicated input lines for user data, UD0 corresponds to $\overline{IV0}$
9	$\overline{UOC}$	User Output Control—active low input to enable data output to UD4-UD7
10	$\overline{UIC}$	User Input Control—active low input to enable data input to UD0-UD3
11	$\overline{ME}$	Master Enable—active low input to enable the $\overline{IV}$ bus for data input, data output, or $\overline{IV}$ address selection/deselection, UD-bus operations are unaffected
12	GND	Ground
13	MCLK	Master Clock—active high input (from MicroController) used to strobe data into data latches from the $\overline{IV}$ bus and bits UD0-UD3 of the UD bus, MCLK also synchronizes $\overline{IV}$ address selection
14	SC	Select Command—active high input (from MicroController) to enable $\overline{IV}$ address input from the $\overline{IV}$ bus for device selection
15	WC	Write Command—active high (from MicroController) to enable the writing of data into the data latches from the $\overline{IV}$ bus, provided $\overline{UIC}$ is not low
16-23	$\overline{IV0}$-$\overline{IV7}$	Interface Vector (Input/Output Bus)—three-state, bidirectional, data bus, $\overline{IV0}$ corresponds to UD0
24	V_{CC}	Supply Voltage

4-INPUT/4-OUTPUT ADDRESSABLE I/O PORT 8X382

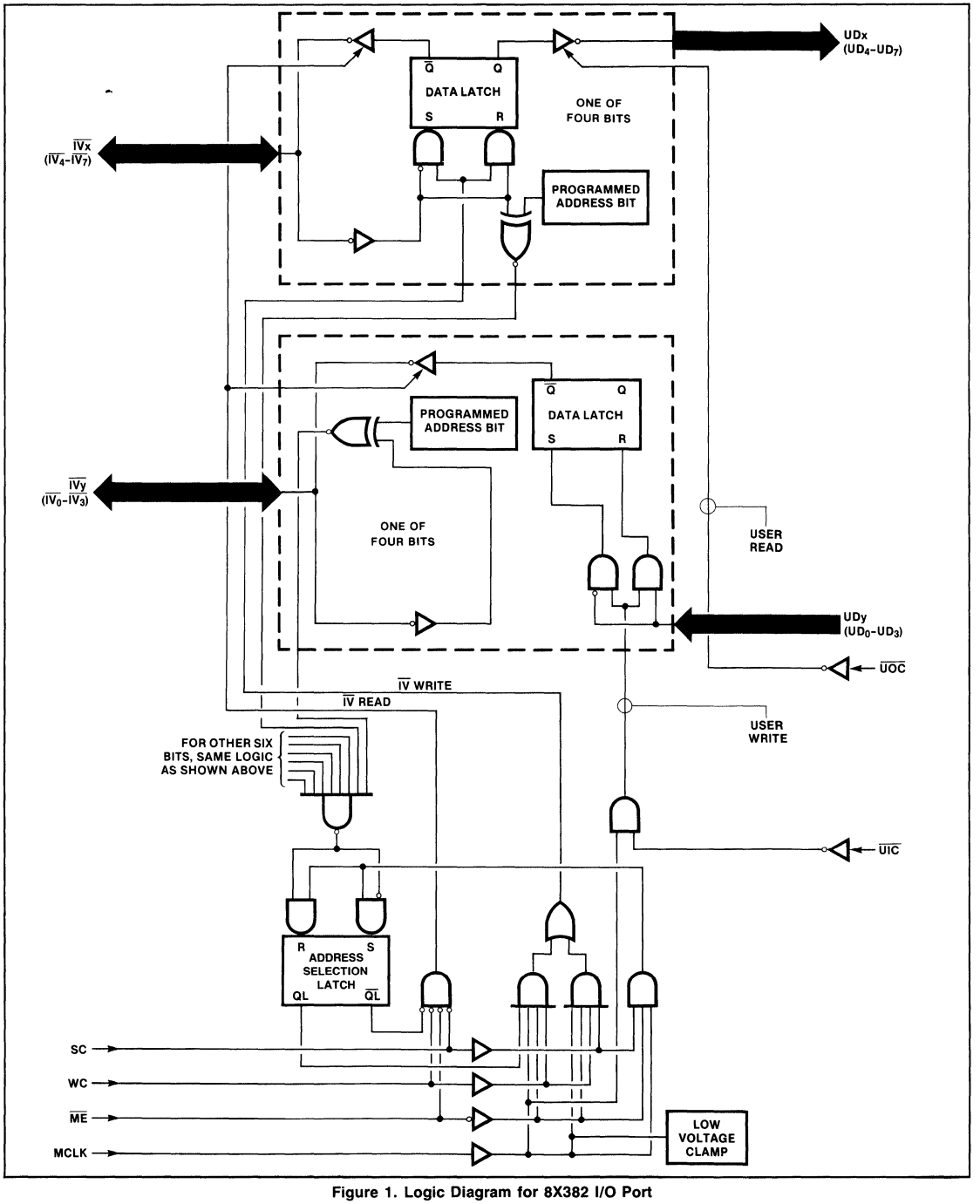


Figure 1. Logic Diagram for 8X382 I/O Port

FUNCTIONAL OPERATION

UD Bus Control

As shown in Table 1, the User Data-bus interface is controlled by the $\overline{UIC}$ and $\overline{UOC}$ inputs. Data input to UD0-UD3 is synchronous with MCLK, that is, with $\overline{UIC}$ low, information is written into the data latches only when MCLK is high. The output drivers of UD4-UD7 bus are enabled when $\overline{UOC}$ is low

Table 1. INPUT/OUTPUT CONTROL OF UD BUS

$\overline{UIC}$	$\overline{UOC}$	MCLK	FUNCTION OF UD BUS	
			UD0-UD3	UD4-UD7
H	L	X	Inactive	Output Data
L	X	H	Input Data	Inactive
L	X	L	Inactive	Inactive
H	H	X	Inactive	Inactive

X = don't care

$\overline{IV}$ Bus Control

Input/output control of the $\overline{IV}$ bus is shown in Table 2; this bus is controlled by SC, WC, $\overline{ME}$, MCLK and the current state of an internal address selection latch. The address selection latch in the I/O port stores the result of the most recent $\overline{IV}$ address selection. The latch is set when the internally preprogrammed address of the port matches the address on the $\overline{IV}$ bus during an address-selection operation (SC=MCLK=High/WC=Low). The latch is cleared when the two 8-bit address patterns are in disagreement. The $\overline{IV}$ bus can transfer data only when the selection latch is set. The MicroController Left Bank ($\overline{LB}$) and Right Bank ($\overline{RB}$) outputs can control the $\overline{ME}$ inputs for two banks of I/O devices, thus, acting as ninth address bit.

Data is written into the data latches of a selected device from the $\overline{IV}$ bus when WC = MCLK = High and $\overline{ME}$ = Low. Output drivers on the $\overline{IV}$ bus of the device with the address latch set are enabled with $\overline{ME}$, WC, and SC low. With SC and WC both high (shaded entry of Table 2), the bit pattern present on $\overline{IV0}$-$\overline{IV7}$ is interpreted as both input data ($\overline{IV4}$-$\overline{IV7}$ only) and $\overline{IV}$ address. The data in $\overline{IV4}$-$\overline{IV7}$ is latched in whether or not the I/O port has been previously selected. If the preprogrammed address of the I/O port matches the bit pattern on $\overline{IV0}$-$\overline{IV7}$ when SC and WC are both high, the selection latch is set; otherwise, it is reset. (Note. *The MicroController never drives both SC and WC high at the same time.*)

Table 2. INPUT/OUTPUT CONTROL OF IV BUS

$\overline{ME}$	SC	WC	MCLK	SEL LATCH	FUNCTION OF $\overline{IV}$ BUS
L	L	L	X	Set	Output Data
L	L	H	H	Set	Input Data ($\overline{IV4}$-$\overline{IV7}$ only)
L	H	L	H	X	Input Address*
L	H	H	H	X	Input Data ($\overline{IV4}$-$\overline{IV7}$ only) and address*
L	X	H	L	X	Inactive
L	H	X	L	X	Inactive
L	L	X	X	Not set	Inactive
H	X	X	X	X	Inactive

X = don't care * Selection latch is updated

Bus Logic Levels

Data written into the I/O port from either bus will appear inverted when read from the other bus. Data written into either bus will not be inverted when read from the same bus. (Note. *A logic "1" in MicroController software corresponds to a high level on the UD bus even though the IV bus is inverted).* The 8X382 wakes up in the unselected state with all data bits latched at the "logic 1" level (UD bus outputs high if enabled).

ADDRESS PROGRAMMING AND ADDRESS PROTECT

Programming Procedures

The 8X382 can be programmed to respond to any address within a range of 0_{10} through 255_{10}. In an unprogrammed state, low level (≤0.8V) inputs on all $\overline{IV}$ bus lines (address 255_{10}) will select the device. To program a given address bit to match a high level (≥2.0V) input on the corresponding $\overline{IV}$ pin (a logical "0" to the MicroController), the counterpart UD-bus pin must be pulsed according to Table 3 and the following procedures:

Step 1: Set all control inputs to the inactive state—$\overline{UIC}$ = $\overline{UOC}$ = $\overline{ME}$ = V_{CC} and SC = WC = MCLK = GND; leave the UD and $\overline{IV}$ bus pins open.

Step 2: Increase V_{CC} to V_{CCP}.

Step 3: After V_{CC} has stabilized, apply a single programming pulse (Figure 2) to the user-bus bit that corresponds to the desired high-level $\overline{IV}$ address bit. The I/O port is programmed from the user bus (UD0-UD7) for addressing from the MicroController bus ($\overline{IV0}$-$\overline{IV7}$).

Table 3. PROGRAMMING SPECIFICATIONS

PARAMETERS	LIMITS			UNITS
	Min	Typ	Max	
V_{CCP} — Programming supply voltage·				
Address	8.75	9.0	9 25	V
Protect		0		V
Maximum time V_{CCP} >5.25V			1 0	Sec
Programming voltage:				
Address	8.75	9 0	9 25	V
Protect	8.75		9.25	V
Programming current:				
Address			5	mA
Protect			50	mA
t_r — Programming pulse rise time·				
Address	10		100	μS
Protect	10		100	μS
tω — Programming pulse width	0.5		1.0	mS

Step 4: Return V_{CC} to 0-volts. (Note. *If the programming of all address bits is completed in less than 1-second, V_{CC} can remain at 9.0-volts for the required interval of time.*)

Step 5: Steps 1 through 3 are applicable to the programming of each address bit that requires a high-level $\overline{IV}$ match.

Step 6: To verify that the address is properly programmed, return V_{CC} to +5V, set $\overline{IV0}$-$\overline{IV7}$ to the desired (inverted) binary address pattern, set $\overline{ME}$ = WC = Low and SC = MCLK = High. If there are no programming errors, subsequent data written from $\overline{IV4}$-$\overline{IV7}$ (WC = High) will appear inverted on UD4-UD7.

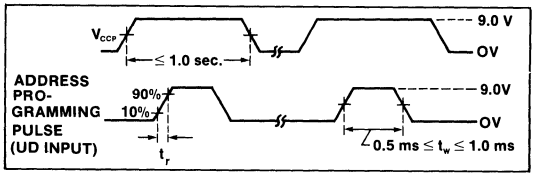


Figure 2. Address Programming Pulse

Address Protect

After programming the I/O Port, steps should be taken to isolate the address circuits and make these circuits permanently immune to further change.

Step 1: Set V_{CC} and all control inputs to 0-volts (V_{CC} = $\overline{UIC}$ = $\overline{UOC}$ = $\overline{ME}$ = SC = WC = MCLK = GND = 0.0V); $\overline{IV0}$-$\overline{IV7}$ = open circuit.

Step 2: Taking one pin at a time, apply a protect programming pulse (Figure 3) to each user-bus bit (UD0-UD7)—refer to Table 3 for min/max specifications pertaining to voltage and current.

Step 3: Verify that the address circuits for each bit is isolated by applying 9-volts, in turn, to each user-bus pin (UD0-UD7) and measuring less than 200 microamperes of input current. (Note. *Setup conditions are the same as those in Step 1.*)

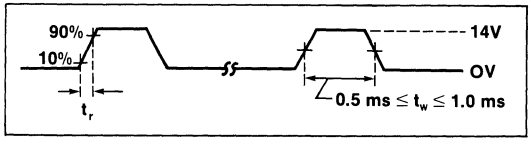


Figure 3. Protect Programming Pulse

DC ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage[3]	+7	Vdc
V_{IN}	Input voltage[3]	+5 5	Vdc
T_{STG}	Storage temperature range	-65 to +150	°C

COMMERCIAL. 4.75V ≤ V_{CC} ≤ 5.25V, 0°C ≤ T_A ≤ 70°C
MILITARY· 4 5V ≤ V_{CC} ≤ 5.5V, -55°C ≤ T_C ≤ 125°C

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4 75	5	5.25	4 5	5	5.5	V
V_{IH}	High Level Input Voltage		2 0			2 0			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
V_{CL}	Input Clamp Voltage	V_{CC} = Min, I_I = -10mA			-1.5			-1.5	V
I_{IH}	High Level Input Current[1]	V_{CC} = Max, V_{IH} = 2 7V		5 0	100		5.0	100	µA
I_{IL}	Low Level Input Current[1]	V_{CC} = Max, V_{IL} = 0.5V		-350	-550		-350	-550	µA
I_{OZH}	High-Z State Output Current—High Level[4]	V_{CC} = Max, V_{OH} = 2 5V			100			100	µA
I_{OZL}	High-Z State Output Current—Low Level[4]	V_{CC} = Max, V_{OL} = 0.5V			-100			-100	µA
V_{OL}	Low Level Output Voltage $\overline{IV}$ Bus ($\overline{IV0}$-$\overline{IV7}$)	V_{CC} = Min; I_{OL} = 16mA			0.55			0.55	V
	User Bus (UD4-UD7)	V_{CC} = Min, I_{OL} = 24mA			0.55			0.55	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = -3.2mA	2 4			2 4			V
I_{OS}	Short Circuit Output Current[2] $\overline{IV}$ Bus ($\overline{IV0}$-$\overline{IV7}$)	V_{CC} = Max	-20			-20			mA
	UD Bus (UD4-UD7)	V_{CC} = Max	-10			-10			mA
I_{CC}	Supply Current	V_{CC} = Max, $\overline{ME}$ = $\overline{UOC}$ = V_{CC}		90	150		90	150	mA

Notes
1 The input current includes the Three-state leakage current of the output driver on the data lines
2 Only one output may be shorted at a time
3 These limits do not apply during address programming
4 Applies only to pins UD4-UD7

AC ELECTRICAL CHARACTERISTICS

COMMERCIAL: $4.75V \leq V_{CC} \leq 5.25V$, $0°C \leq T_A \leq 70°C$

MILITARY: $4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_C \leq 125°C$

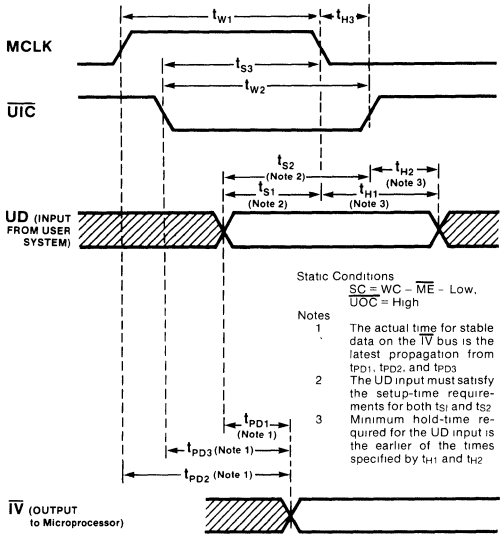
LOADING: See TEST LOADING CIRCUITS

PARAMETER	REFERENCES[1] FROM	REFERENCES[1] TO	TEST CONDITIONS	LIMITS (COMMERCIAL) Min	Typ	Max	LIMITS (MILITARY) Min	Typ	Max	UNIT
Pulse Widths:										
t_{W1} Clock High	↑MCLK	↓MCLK		35			35			ns
t_{W2} User Input Control	↓$\overline{UIC}$	↑$\overline{UIC}$	MCLK = High	35			35			ns
Propagation Delays:										
t_{PD1} UD Propagation Delay	UD_{0-3}	$\overline{IV}_{0-3}$	MCLK = High SC = WC = $\overline{ME}$ = $\overline{UIC}$ = Low			30			30	ns
t_{PD2} UD Clock Delay	↑MCLK	$\overline{IV}_{0-3}$	UD_{0-3} = Stable, MCLK = High; SC = WC = $\overline{ME}$ = $\overline{UIC}$ = Low			50			50	ns
t_{PD3} UD Input Delay	↓$\overline{UIC}$	$\overline{IV}_{0-3}$	UD_{0-3} = Stable; MCLK = High, SC = WC = $\overline{ME}$ = Low			50			50	ns
t_{PD4} $\overline{IV}$ Data Propagation Delay	$\overline{IV}_{4-7}$	UD_{4-7}	MCLK = WC = High; $\overline{ME}$ = $\overline{UOC}$ = SC = Low			45			45	ns
t_{PD5} $\overline{IV}$ Data Clock Delay	↑MCLK	UD_{4-7}	$\overline{IV}_{4-7}$ = Stable, WC = High; $\overline{ME}$ = $\overline{UOC}$ = SC = Low			55			55	ns
Output Enable Timing:										
t_{OE1} UD Output Enable	↓$\overline{UOC}$	UD_{4-7}				30			30	ns
t_{OE3} $\overline{IV}$ Data Master Enable	↓$\overline{ME}$	$\overline{IV}$	WC = SC = Low			22			25	ns
t_{OE5} $\overline{IV}$ Data Write Recovery	↓WC	$\overline{IV}$	SC = $\overline{ME}$ = Low			25			25	ns
t_{OE6} $\overline{IV}$ Data Select Recovery	↓SC	$\overline{IV}$	WC = $\overline{ME}$ = Low			25			25	ns
Output Disable Timing:										
t_{OD1} UD Output Disable	↑$\overline{UOC}$	UD_{4-7}				25			25	ns
t_{OD3}[2] $\overline{IV}$ Data Master Disable	↑$\overline{ME}$	$\overline{IV}$	WC = SC = Low			25			25	ns
t_{OD5}[2] $\overline{IV}$ Data Write Override	↑WC	$\overline{IV}$	SC = $\overline{ME}$ = Low			20			20	ns
t_{OD6}[2] $\overline{IV}$ Data Select Override	↑SC	$\overline{IV}$	WC = $\overline{ME}$ = Low			20			20	ns
Setup Times:										
t_{S1} UD Clock Setup Time	UD_{0-3}	↓MCLK	$\overline{UIC}$ = Low	15			15			ns
t_{S2} UD Control Setup Time	UD_{0-3}	↑$\overline{UIC}$	MCLK = High	15			15			ns
t_{S3} User Input Control Setup Time	↓$\overline{UIC}$	↓MCLK		25			25			ns
t_{S4} $\overline{IV}$ Data Setup Time	$\overline{IV}$	↓MCLK	WC = High or SC = High; $\overline{ME}$ = Low,	35			35			ns
t_{S5}[3] $\overline{IV}$ Master Enable Setup Time	↓$\overline{ME}$	↓MCLK	WC = High or SC = High	30			30			ns
t_{S6} $\overline{IV}$ Write Control Setup Time	↑WC	↓MCLK	SC = $\overline{ME}$ = Low;	30			30			ns
t_{S7} $\overline{IV}$ Select Control Setup Time	↑SC	↓MCLK	WC = $\overline{ME}$ = Low	30			30			ns

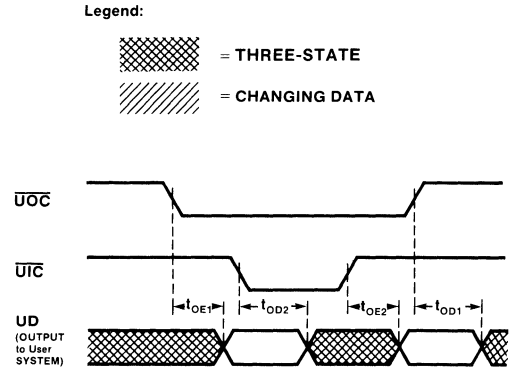
AC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER	REFERENCES FROM	REFERENCES TO	TEST CONDITIONS	LIMITS (COMMERCIAL) Min	Typ	Max	LIMITS (MILITARY) Min	Typ	Max	UNIT
Hold Times:										
t_{H1} UD Clock Hold Time	↓MCLK	UD	$\overline{UIC}$ = Low	15			15			ns
t_{H2} UD Control Hold Time	↑$\overline{UIC}$	UD	MCLK = High	15			15			ns
t_{H3} User Input Control Hold Time	↓MCLK	↑$\overline{UIC}$		0			0			ns
t_{H4} Data Hold Time	↓MCLK	$\overline{IV}$	WC = High or SC = High, $\overline{ME}$ = Low	5			5			ns
t_{H5}[3] Master Enable Hold Time	↓MCLK	↑$\overline{ME}$	WC = High or SC = High;	0			0			ns
t_{H6} $\overline{IV}$ Write Control Hold Time	↑MCLK	↓WC	SC = $\overline{ME}$ = Low	0			0			ns
t_{H7} $\overline{IV}$ Select Control Hold Time	↑MCLK	↓SC	WC = $\overline{ME}$ = Low	0			0			ns

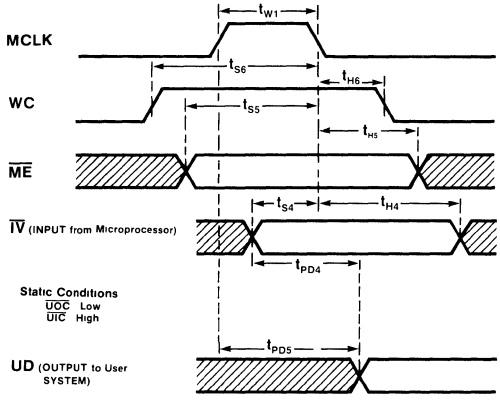
Notes:
1 All measurements to the $\overline{IV}$ bus assumes the address selection latch is set
2 These parameters are measured with a capacitive loading of 50 ρf and represent the output driver turn-off time.
3 If $\overline{ME}$ is to be high (inactive), it must be setup before the rising edge and held after the falling edge of MCLK to avoid unintended writing into or selection of the I/O port



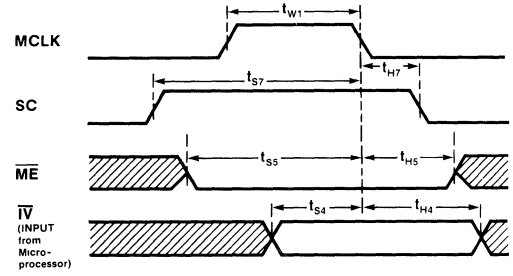
a. User Data Input Timing



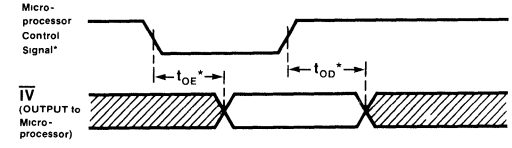
b. User Data Output Timing



c. MicroController Write Cycle Timing



d. MicroController Select Cycle Timing



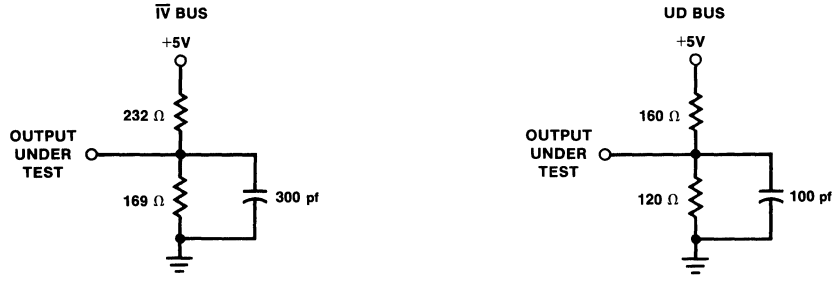
*PARAMETER KEY

MICROPROCESSOR CONTROL SIGNAL	AC TIMING PARAMETERS	STATIC CONDITIONS
ME	t_{OE3} t_{OD3}	SC = WC = LOW
WC	t_{OE5} t_{OD5}	SC = ME = LOW
SC	t_{OE6} t_{OD6}	WC = ME = LOW

e. MicroController Output Enable Timing

Figure 4. Timing Diagrams

TEST LOADING CIRCUITS



4-INPUT/4-OUTPUT ADDRESSABLE I/O PORT 8X382

APPLICATIONS

When compared to other MicroController ports in the 8X370 series, the 8X382 has some unique features that provide real design advantages in certain applications. Connection of the I/O port to the MicroController is simple and straightforward in that like pin names are tied together. The system designer must also decide on which bank of the MicroController to place the 8X382 and then connect the $\overline{ME}$ pin of the port to either the $\overline{LB}$ (Left Bank) or $\overline{RB}$ (Right Bank) of the MicroController.

The 8X382 is unique because it can be used for both dedicated input and output operations. In the system shown below, the user interface requires nine (9) dedicated inputs and eleven (11) dedicated outputs. Observe that by using an 8X382, the problem is solved by three devices, whereas, four 8X372 ports are required for the same solution.

Another important use of the 8X382 is in implementing a handshake interface. Since both input and output bits reside in the same port, I/O operations can be performed without port re-addressing. Users may also find the 8X382 an advantage in the layout of Printed Circuit boards, since random control/status signals can be grouped within the same device position.

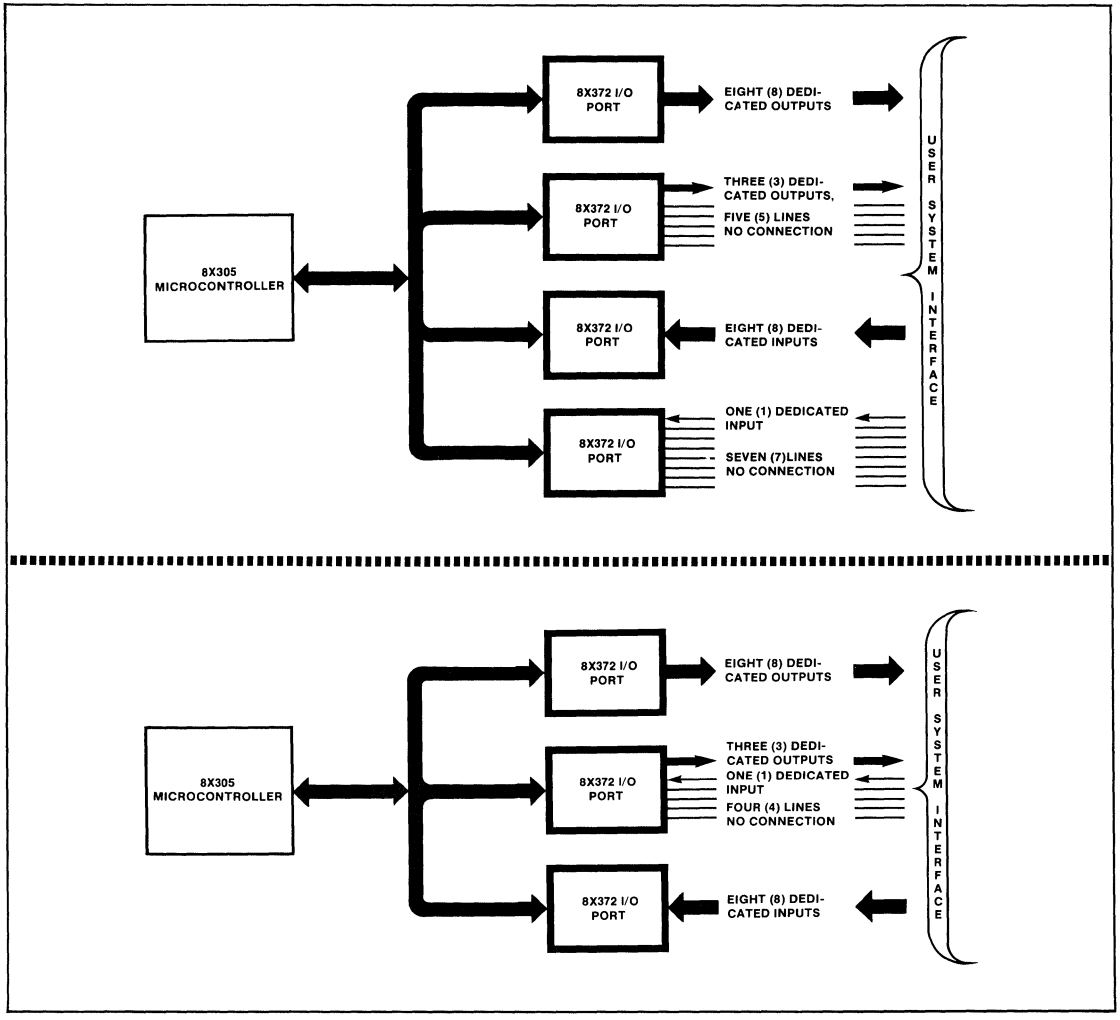


Figure 5. Logic Diagram for 8X382 I/O Port

INTERRUPT CONTROL COPROCESSOR 8X310

FEATURES

- **Three prioritized interrupts**
- **Subroutine handling capabilities**
- **4-level LIFO stack for return address storage**
- **Interrupt masking by software and hardware**
- **Stack full flag**
- **Directly compatible with 8X305 MicroController**
- **Bipolar ISL (Integrated Schottky Logic) and low-power Schottky technology**
- **Single +5 volt power supply**
- **0.6 inch, 40-pin DIP**

PRODUCT DESCRIPTION

The Signetics 8X310 Interrupt Control Coprocessor (ICC) supports the 8X305 MicroController in systems that are interrupt driven and those that require subroutine handling capabilities.

As shown in Figure 1, the ICC provides three prioritized interrupt request lines, INT 0 (highest priority), INT 1 and INT 2. A low-to-high transition applied to any of these input lines latches in an interrupt request which may be serviced when sampled by the ICC once each instruction cycle of the MicroController. When an interrupt request is serviced, the ICC forces the MicroController to jump to one of three fixed locations in program memory; instruction addresses 4, 5, and 6 correspond to INT 0, INT 1 and INT 2. At each of these addresses, the user programs a JMP instruction to another address where the user's interrupt service routine begins.

During interrupt servicing, the ICC also stores the proper return address into a four deep, Last-In-First-Out (LIFO) stack. At the conclusion of the interrupt service routine, the user program instructs the ICC to return to the main program at the location previously stored in the stack. The return operation is implemented by coding a special RETURN instruction which is decoded directly off the instruction bus by the ICC. There are five such special instructions relating to interrupt and subroutine handling functions performed by the ICC. These instruction codes are all treated as non-operational instructions (NOPs) by the MicroController.

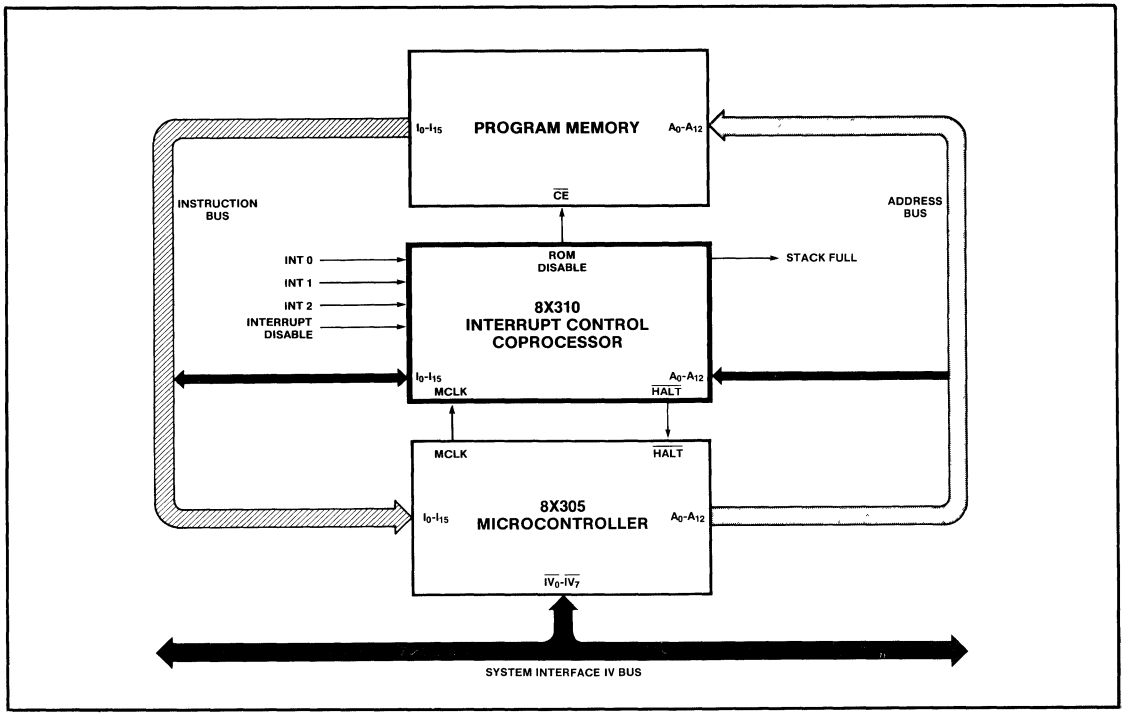


Figure 1. Typical System Connections Using ICC

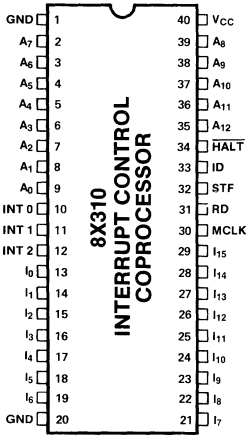
An internal one-bit mask is used to inhibit interrupt servicing. Whenever the mask is set, the ICC does not respond to any pending interrupt requests; however, any requests remain latched for future servicing. The mask can be set and cleared either by the user program or automatically during certain ICC functions. The special instructions SET MASK and CLEAR MASK are provided for user control. The Interrupt Disable input also inhibits interrupt request servicing.

The ICC provides a facility for implementing subroutines in the user program. A special PUSH instruction directs the ICC to store the return address into the stack in a manner similar to interrupt servicing. The jump to the subroutine, however, is performed by the user program. Subroutines may be nested (called from within other subroutines) depending on remaining vacancies in the four deep stack.

In general, the ICC adds some useful and very flexible facilities to the 8X305-based system. It offers both hardware and software capabilities that can improve efficiency and decrease program size. These features, from both a chip and system aspect, are described in subsequent paragraphs.

8X310 PACKAGE AND PIN DESIGNATIONS

N, I PACKAGE



TOP VIEW

ORDER NUMBERS

N8X310N, N8X310I
S8X310I/883B, S8X310I/883C

Pin No.	Identifier	Function
1, 20	GND	Ground. (Note: The printed circuit board should not use the ICC as a bridge for external ground.)
2-9, 35-39	A_7-A_0, A_{12}-A_8	Program address input lines from MicroController. Active high. A_0 is MSB.
10-12	INT 0-INT 2	Interrupt request input pins. INT 0 has the highest priority and INT 2 the lowest — Edge-triggered on a low-to-high transition.
13-19, 21-29	I_0-I_6, I_7-I_{15}	Bidirectional instruction bus; I_0 is MSB. When acting as an input, the ICC decodes the instruction flow (binary pattern on I_0-I_{15}) between program storage and the MicroController. During an interrupt or return cycle, the ICC outputs a JMP instruction to the MicroController via these lines —refer to FUNCTIONAL OPERATION of ICC.
30	MCLK	Master CLocK — active high input from 8X305 MicroController used for a timing reference and system synchronization.
31	RD	ROM (or PROM) Disable — active high output used to disable normal program storage so that the ICC can force an instruction to the MicroController.
32	STF	STack Full — active high output. When the LIFO stack is full, STF goes high and remains high until at least one register in the 4-level stack is empty.
33	ID	Interrupt Disable — active high. When this input pin is driven high, servicing of all interrupt requests is suspended.
34	$\overline{\text{HALT}}$	Active low output. Suspends all processing operations of the MicroController during period when the source of instruction data is changing between the ICC and program storage.
40	V_{CC}	+5 volt power supply.

FUNCTIONAL OPERATION

Basic Functions

The ICC performs the three general functions indicated below.

Function 1: Provides a means for the 8X305 MicroController to respond to interrupt requests by diverting the program flow of the 8X305 MicroController to the proper interrupt service routine or, in the case of a subroutine, the ICC stores the return address in the 4-level LIFO stack (Figure 2).

Function 2: Returns the user to the proper point in the main program for both interrupt and subroutine activities.

Function 3: Provides both automatic and programmed masking capabilities.

Interrupt Requests and Priority Considerations

An interrupt is requested when any one of the ICC input pins INT 0, INT 1, or INT 2 undergoes a low-to-high transition; this request is temporarily stored in an internal edge-triggered latch that corresponds to the affected interrupt input. The interrupt request latches are part of the Priority and Mask Logic shown in Figure 2. Unless masked or otherwise disabled, the ICC samples these latches once each instruction cycle. Any or all of the latches may be set when sampled by the ICC; however, only the interrupt of highest priority will be serviced — the remaining interrupts will be held in queue. Thus, if INT 0, INT 1 and INT 2 simultaneously compete for service, INT 0 is the first to be serviced followed, in order, by INT 1 and INT 2; likewise, if INT 1 and INT 2 compete for service, INT 1, being of higher priority will be serviced first. The CLEAR INTERRUPT instruction resets all interrupt request latches without affecting an interrupt service routine that is already in progress.

The highest priority interrupt request will be serviced when sampled by the ICC provided interrupts in general are not inhibited and a previous interrupt of equal or higher priority is not currently being serviced. The general masking of interrupts is discussed later. To determine priorities, the ICC keeps track of any interrupt that is serviced until the corresponding service routine returns. A subsequent interrupt request may interrupt a service routine in progress only if it is of a higher priority than that of the current interrupt being serviced. If, for example, INT 1 is requested and serviced, then before its service routine finishes, a request on INT 0 can be serviced as a second level interruption. However, a request on INT 2 or a second request on INT 1 must wait until the original INT 1 service routine returns. The interrupt service routine that was interrupted will resume execution at the point of interruption when the higher priority service routine returns (i.e. in the same manner as when returning to the main program).

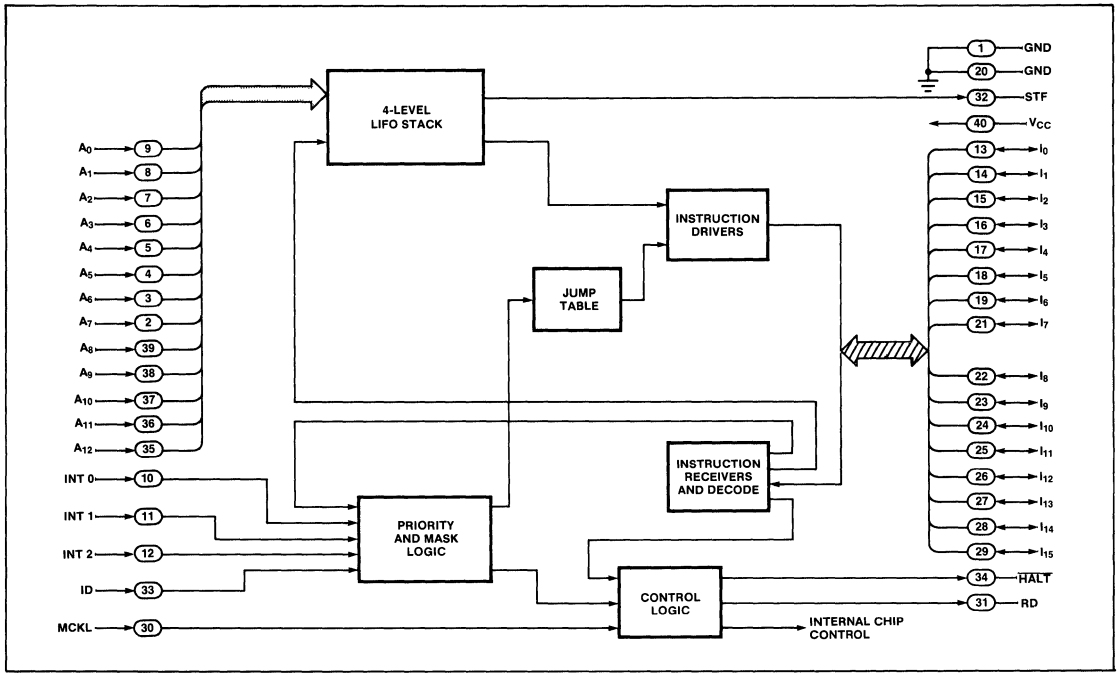


Figure 2. 8X310 Interrupt/Control Coprocessor — Functional Block Diagram

Interrupt Servicing

Interrupts are sampled only at the conclusion of an instruction cycle while the next instruction is being fetched from Program Memory.

When an interrupt request is serviced, the following general steps are performed:

- Address of the instruction that would normally be executed next is pushed into the 4-level LIFO Stack (Figure 2) for subsequent return to the main program.
- The ICC disables program storage and forces a JMP instruction onto the Instruction bus of the 8X305 MicroController. (Note: Because of timing considerations, the HALT signal is driven low to suspend operation of the MicroController for one instruction cycle; this permits the source of instruction data to change from program storage to the ICC without conflict.) The JMP instruction from the ICC transfers the MicroController to one of the three fixed program locations shown below. In each of these addresses, the user will normally store a JMP instruction to the interrupt service routine for that particular interrupt. Details of these operations are described later.

INT 0 ..... Address 4
INT 1 ..... Address 5
INT 2 ..... Address 6

Return from Interrupt Service Routine

Upon completion of the interrupt service routine, the user codes the special RETURN instruction. When executed, the ICC performs the following steps

- The return address is popped from the LIFO stack.
- The ICC disables program storage and forces a JMP instruction onto the MicroController instruction bus with the return address from the stack. (The HALT signal is driven low for one instruction cycle.)
- The JMP instruction from the ICC transfers the MicroController to the instruction that was about to execute at the time the interrupt was taken

A typical structure for a user program which handles interrupts is shown in the following example:

Address		Instruction	Comment
0		(any)	First instruction executed after system reset
•		•	
•		•	
3		JMP MAIN	Jump around interrupt vector locations.
4		JMP SERV0	Service INT 0 interrupt.
5		JMP SERV1	Service INT 1 interrupt.
6		JMP SERV2	Service INT 2 interrupt.
7	MAIN	(any)	Continue main program.
•		•	
•		•	
	SERV0	(any)	Begin INT 0 service routine.
•		•	
•		•	
		MAIN R6,R6	ICC RETURN instruction. End INT 0 service routine (resume main program execution).
	SERV1	(any)	Begin INT 1 service routine.
•		•	
•		•	
		MOVE R6,R6	RETURN from INT 1 service routine.
	SERV2	(any)	Begin INT 2 service routine.
•		•	
•		•	
		MOVE R6,R6	RETURN from INT 2 service routine.

Instruction Set

The five instructions shown in Table 1 allow the user to efficiently manage both the interrupt and subroutine capabilities of the ICC in an 8X310/8X305-based system. When an ICC instruction appears in the program, it is interpreted as a NOP by the 8X305 but is captured and decoded by the ICC to perform the desired function. The capture-and-decode functions of the chip are automatic. Assembly and object codes for each ICC instruction are shown in Table 1.

Table 1. INSTRUCTION SET FOR ICC

Instruction	Instruction Codes		8X305 Operation	Description of ICC Operation
	Assembler	Binary		
		I_0 = MSB ↓ I_{15} = LSB ↓		
SET MASK	MOVE R5,R5	000 00101 000 00101	NOP	When executed, sets interrupt mask, thus inhibiting all interrupt servicing.
CLEAR MASK	MOVE R4,R4	000 00100 000 00100	NOP	When executed, clears interrupt mask for all interrupts
RETURN	MOVE R6,R6	000 00110 000 00110	NOP	When executed returns program to address at top of LIFO stack.
PUSH	MOVE R3,R3	000 00011 000 00011	NOP	Pushes "address + 2" onto stack if PUSH is programmed on odd address in program memory and "address + 1" if PUSH is programmed on even address.
CLEAR INTERRUPT	MOVE R2,R2	000 00010 000 00010	NOP	Clears all interrupt requests; an interrupt service routine that is in progress is unaffected.

Interrupt Masking Operations

Certain operations performed by the ICC and also some system considerations require that program execution not be interrupted for a specified interval of time. The servicing of interrupts by the ICC can be inhibited in a number of ways. Any time interrupts are inhibited, the ICC ignores any latched interrupt requests. However, the interrupt request latches are not cleared so that any previously pending requests remain latched. Also, during an interval when interrupt servicing is inhibited, any new interrupt signals received will get latched. As soon as interrupt servicing is enabled, any latched requests can be serviced on a priority basis.

The primary means of inhibiting interrupt servicing is the internal one-bit mask (latch). This mask can be set (to inhibit interrupts) or cleared under control of the user program using the special ICC instructions SET MASK and CLEAR MASK — See Table 1. With these instructions, segments of the user program can be isolated so as to proceed without interruptions. Frequently, uninterruptable segments are needed at the very beginning of the user program (initialization routine) and at the beginning of, or throughout an interrupt service routine. To facilitate this, the ICC automatically sets the mask whenever the MicroController executes address zero (typically resulting from a system reset) and whenever the ICC services an interrupt. The ICC also automatically clears the mask after performing a RETURN operation from an interrupt service routine; a RETURN from a subroutine does not affect the status of the interrupt mask.

The Interrupt Disable (ID) input pin may also be used to inhibit interrupt servicing. Interrupt servicing remains disabled as long as a high level is applied to the input. The ID input has no effect, however, on the status of the internal interrupt mask.

To ensure proper program flow, the ICC suspends interrupt servicing momentarily during certain situations. During the cycle in which the MicroController encounters an XEC (Execute) instruction an interrupt will not be serviced. This is because the XEC causes the MicroController to issue an address of an instruction to be executed out of the sequence of normal program flow. This would not be a valid address.

Interrupts are also suspended during execution of a PUSH or RETURN instruction and the instruction immediately following. This ensures proper operation of the LIFO stack. In addition, no interrupts are latched or serviced and no special ICC instructions are decoded at address zero which resets the ICC.

Subroutine Calling

The ICC provides for subroutine calling by storing the proper return address into the LIFO stack under control of the user program. Two instructions are required to implement a subroutine call — a PUSH instruction executed by the ICC and a JMP to the subroutine executed by the MicroController. The PUSH instruction is normally programmed at an odd-numbered address in program memory immediately followed by the JMP. When the PUSH instruction is executed, the ICC finds the address of the next instruction (JMP to subroutine) on the MicroController's address bus. internally changes the least-significant bit to one (effectively adds one to the address) and stores this into the stack. Program execution proceeds normally and the MicroController makes the jump to the beginning of the subroutine. The subroutine may be located at any convenient place in program memory.

Upon completion of the subroutine, the user codes the RETURN instruction in the same manner as for an interrupt service routine. At that point, the ICC forces the MicroController to resume execution of the main program at the instruction immediately following the JMP-to-subroutine instruction.

The code for a typical subroutine call-and-return is shown in the following example.

Address	Instruction	Comment
X (any odd-numbered address)	MOVE R3,R3	PUSH instruction initiates subroutine call by causing ICC to push the address X+2 onto the stack. (The PUSH instruction is interpreted as a NOP by the MicroController.)
X+1 (even)	JMP SUBR	The MicroController JMPs to the beginning of the subroutine.
X+2 (odd)	(any instruction)	Main program execution resumes here after RETURN from subroutine.
•	•	
•	•	
•	•	
SUBR (any address)	(any instruction)	Execution of subroutine starts here.
•	•	
•	•	
•	•	
(any address)	MOVE R6,R6	RETURN instruction causes ICC to transfer program back to X+2.

Stack Operation

The LIFO stack holds up to four 13-bit program addresses which allows the ICC to return from a subroutine or interrupt service routine. When all four stack locations are filled, the STack Full (STF) output pin is driven high and remains high until a RETURN (or reset) operation occurs. If an additional interrupt is serviced or subroutine called while the stack is full, the stack will overflow and the oldest return address will be overwritten and lost. That is, the stack retains the four most recent entries. After an overflow, the status of the STF output is not valid (until a reset operation occurs).

To prevent an interrupt from overflowing the stack, the user can connect the STF output directly to the Interrupt Disable (ID) input of the ICC. Then, even if the internal mask and priorities permit interrupt servicing, the interrupt request must still wait for the most recent service routine or subroutine to return.

Because subroutine calling is controlled explicitly by the user software, the user can always ensure that subroutine nesting alone could not overflow the stack. However, care must be taken whenever calling a subroutine from within an interrupt service routine since the number of remaining stack locations may vary at the time the interrupt is taken. If, for example, three stack locations are already filled (STF is low) at the time an interrupt is serviced, then a subroutine call executed within the interrupt service routine would cause the stack to overflow and the earliest return address to be lost.

As mentioned earlier, whenever a RETURN operation is performed from an interrupt service routine, the internal interrupt mask is automatically cleared. A RETURN from a

subroutine, however, does not affect the status of the mask. To accomplish this, a flag bit is added to each of the four stack locations which records whether each address pushed into the stack is caused by an interrupt or a subroutine call. This flag is read during a RETURN operation to determine whether or not the interrupt mask is cleared. This allows interrupt servicing and subroutine calls to be intermixed in any order.

Initialization

The ICC decodes address zero as a reset command to perform certain initialization functions. (Zero is the first address generated after the MicroController is reset.) Specifically, the Instruction-bus drivers are placed in a high-impedance state, HALT output is set high, RD output is set low, and all interrupt request latches are cleared. The interrupt mask is set so that any initialization routine by the user will not be interrupted until a CLEAR MASK instruction (MOVE R4,R4) is executed. The LIFO stack is reset to an empty state and the STF output is set low.

SYSTEM TIMING RELATIONSHIPS

Interrupt Servicing

Interrupt servicing begins at the end of a MicroController instruction cycle when the 8X305's MCLK signal goes from low-to-high. Starting from this point, processing of the interrupt proceeds as follows:

From the rising edge of MCLK 1:

- Interrupt mask is set to inhibit other interrupts.
- HALT output is driven low to stop internal operation of the 8X305 MicroController for one instruction cycle; MCLK is unaffected. ROM Disable (RD) output is driven high to disable program memory.

From the falling edge of MCLK 1:

- Takes address of next instruction from address bus and pushes it onto the top of stack to be used as the return address to the main program.

From the rising edge of MCLK 2:

- The ICC forces a JMP onto the instruction bus to one of three fixed vector addresses:

INT 0	Address 4
INT 1	Address 5
INT 2	Address 6

- Releases HALT (high) which allows the MicroController to complete the JMP to the above specified vector location in program memory.

From the rising edge of MCLK 3:

- Instruction-bus drivers of the ICC are disabled.
- ROM Disable (RD) pin is cleared (low) enabling the program memory which resumes control of the Instruction bus.

Return Operation

When the interrupt service routine or subroutine is completed, the RETURN instruction initiates the following sequence of events:

From the rising edge of MCLK 1:

- Interrupts are temporarily inhibited through third MCLK cycle.
- HALT output is driven low to stop MicroController for one instruction cycle.
- RD output is set high to disable program memory.

From the rising edge of MCLK 2:

- HALT output is driven high (cleared).
- A JMP instruction to address stored at top of LIFO stack is forced onto the Instruction bus by the ICC. (The stack is popped.)

From the rising edge of MCLK 3:

- Instruction-bus drivers of the ICC are disabled.
- RD is cleared enabling the program memory.
- If returning from an interrupt service routine (condition recorded in extra stack bit) the interrupt mask is cleared; otherwise the mask remains unaffected.

Once the preceding return actions are completed, the 8X305 MicroController will resume execution of the instruction at the return address.

APPLICATION HINTS

- When programming an interrupt service routine or subroutine, certain system operations typically need to be considered. In many interrupt-driven systems, a handshake signal is required to acknowledge the servicing of an interrupt request. The acknowledge signal may be transmitted by the interrupt service routine using a standard I/O port from the 8X300 Family.
- If the user wants to allow a higher priority interrupt request to interrupt a service routine, then the CLEAR MASK instruction should be programmed (perhaps after completing any critical operations)
- For both service routines and subroutines, the user may need to save the contents of some or all of the working registers of the MicroController so that operation of the main program is not upset. Registers may be written out to a working storage RAM such as 8X350 near the beginning of the routine, and restored from RAM just before returning to the main program.
- Certain subroutine calling techniques may be used to increase the efficiency of the user program As shown in the following examples, a subroutine can automatically be repeated two, three or four times, if desired, without programming a loop.

SUBROUTINE AUTOMATICALLY EXECUTES TWICE

Address		Instruction	
X (even)	SUBR2	MOVE R3,R3	Push X+1 onto stack
X+1 (odd)		(start of subroutine)	
•		•	
•		•	
		MOVE R6,R6	RETURN — First time jumps to X+1, second time jumps back to main program

SUBROUTINE AUTOMATICALLY EXECUTES THREE TIMES

X (odd)	SUBR3	MOVE R3,R3	Push X+2 onto stack
X+1 (even)		MOVE R3,R3	Push X+2 onto stack
X+2 (odd)		(start of subroutine)	
•		•	
•		•	

SUBROUTINE AUTOMATICALLY EXECUTES FOUR TIMES

X (even)	SUBR4	MOVE R3,R3	Push X+1 onto stack
X+1 (odd)		MOVE R3,R3	Push X+3 onto stack
X+2 (even)		NOP	
X+3 (odd)		(start of subroutine)	
•		•	
•		•	

- In a manner similar to the MicroController multi-way branch technique, one of several subroutines can be selected according to an index value.

SUBROUTINE CALL SELECTED BY VALUE IN R1

Address		Instruction	
X (odd)		MOVE R3,R3	Push X+2 onto stack
X+1 (even)		XEC TABLE (R1)	Execute JMP at TABLE + (R1)
X+2 (odd)		(any)	Subroutine returns here
•		•	
•		•	
(any)	TABLE	JMP SUB0	Call SUB0 if R1 = 0
		JMP SUB1	Call SUB1 if R1 = 1.
		•	
		•	

DC ELECTRICAL CHARACTERISTICS

COMMERCIAL: V_{CC} = 5.0 V (±5%); 0° C ≤ T_A ≤ 70° C
MILITARY: V_{CC} = 5.0 V (±10%); T_A ≥ -55° C
T_C ≤ 125° C

ABSOLUTE MAXIMUM RATINGS

Parameter		Rating	Unit	Parameter		Rating	Unit
V_{CC}	Power supply voltage	+7	V DC	V_O	Off-state output voltage	+5.5	V DC
V_{IN}	Input voltage	+5.5	V DC	T_{STG}	Storage temperature range	−65 to +150	°C

Parameter		Test Conditions	Limits (Commercial) Min	Typ	Max	Limits (Military) Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min.; I_{OH} = −1.0 mA	2.4			2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min. COMMERCIAL: I_{OL} = 8 mA			0.55				V
		MILITARY: I_{OL} = 4.25 mA						0.55	
V_{CL}	Input Clamp-Diode Voltage	V_{CC} = Min; I_{CL} = −10 mA			−1.5			−1.5	V
I_{IH}	High Level Input Current	V_{CC} = Max; V_{IH} = 2.7 V			100			100	μA
I_{IL}	Low Level Input Current	V_{CC} = Max; V_{IL} = 0.4 V			−550			−700	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max; V_O = 0 V	−15		−80	−15		−80	mA
I_{CC}	Supply Current	V_{CC} = Max; I_0-I_{15} = High-Z							mA
		T_A = 0° C[2]			200				
		T_A = 70° C			185				
		T_A = −55° C[2]						230	
		T_C = 125° C						170	

AC ELECTRICAL CHARACTERISTICS

LOADING: See TEST LOADING CIRCUITS

COMMERCIAL: V_{CC} = 5.0 V (±5%); 0° C ≤ T_A ≤ 70° C
MILITARY: V_{CC} = 5.0 V (±10%); T_A ≥ -55° C
T_C ≤ 125° C

Parameter		References From	To	Test Conditions	Limits (Commercial) Min	Typ	Max	Limits (Military) Min	Typ	Max	Unit
Pulse Widths:											
t_{WIH}	Interrupt High	↑INT_i	↓INT_i		30			30			ns
t_{WIL}	Interrupt Low	↓INT_i	↑INT_i		35			35			ns
t_{WMH}	MCLK High	↑MCLK	↓MCLK	For all Functions	40			47			ns
Propagation Delays:											
t_{PRH}	RD High	↑MCLK	↑RD	Interrupt or Return			70			75	ns
t_{PRL}	RD Low	↑MCLK	↓RD	Interrupt or Return			15			17	ns
t_{PHL}	HALT Low	↑MCLK	↓HALT	Interrupt or Return			70			87	ns
t_{PHH}	HALT High	↑MCLK	↑HALT	Interrupt or Return			65			75	ns
t_{PSH}	Stack Full High	↓MCLK	↑STF	Interrupt or Subroutine Call			105			105	ns
t_{PSL}	Stack Full Low	↓MCLK	↓STF	Return or Reset			110			115	ns

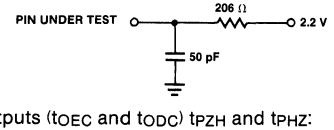
AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter		References From	References To	Test Conditions	Limits (Commercial) Min	Typ	Max	Limits (Military) Min	Typ	Max	Unit
Setup Times:											
t_{SIH}	Interrupt Input Setup[3]	↑INT_i	↑MCLK		35			35			ns
t_{SA}	Address Setup	A_0-A_{13}	↑MCLK	Interrupt, Subroutine Call, or Reset	0			0			ns
t_{SC}	Instruction Setup[5]	I_{0-15}	↓MCLK	All Commands	Note 5			Note 5			ns
t_{SD}	Interrupt Disable Setup[3]	ID	↑MCLK		30			30			ns
Hold and Reset Recovery Times:											
t_{HIL}	Interrupt Low Input Hold[3]	↑MCLK	↑INT_i		15			15			ns
t_{HA}	Address Hold	↓MCLK	A_{0-13}	Subroutine Call or Reset	75			90			ns
t_{HC}	Instruction Hold	↓MCLK	I_{0-15}	All Commands	55			55			ns
t_{HD}	Interrupt Disable Hold[3]	↑MCLK	ID		25			25			ns
t_{RI}	Interrupt Reset Recovery[4]	↓MCLK	↑INT_i	Reset or Cancel Command	70			70			ns
Output Enable/Disable Delays:											
t_{OEC}	Instruction Output Enable	↑MCLK	I_{0-15}	Interrupt or Return			70			87	ns
t_{ODC}	Instruction Output Disable	↑MCLK	I_{0-15}	Interrupt or Return			40			47	ns

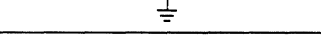
Notes:
1. All electrical characteristics are guaranteed after power is applied and thermal equilibrium has been reached.
2. The 200 and 230 milliampere values are worst case over the entire temperature range for the Commercial and Military parts, respectively.
3. Parameters t_{SIH}, t_{HIL}, T_{SD}, and t_{HD} are used only to determine whether an interrupt request will be serviced during the current or a subsequent instruction cycle. The INT_i and ID inputs are asynchronous and transitions on either input may safely occur at any time with respect to MCLK. A low-to-high transition on INT_i occurring after t_{SIH} and before t_{HIL} means only that it cannot be determined for sure whether or not the interrupt request will be honored during the current instruction cycle. Similarly, transitions on ID between t_{SD} and t_{HD} make it uncertain as to whether or not masking applies during the current instruction cycle.
4. When clearing interrupt requests (including a reset operation), any new low-to-high transitions appearing at the INT_i inputs that occur before t_{RI} risk being cleared and therefore ignored; however, any transition after t_{RI} is certain to be latched.
5. COMMERCIAL: t_{SC} (minimum) = 15 ns — t_{PRL} (actual).
   MILITARY: t_{SC} (minimum) = 17 ns — t_{PRL} (actual).
   (The required instruction enable time for the program memory depends on the sum of the t_{PRL} and t_{SC}.)

TEST SETUPS

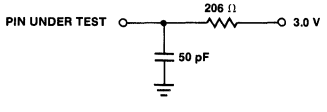
RD, STF, and $\overline{HALT}$ Outputs —



I_0-I_{15} Outputs (t_{OEC} and t_{ODC}) t_{PZH} and t_{PHZ}:



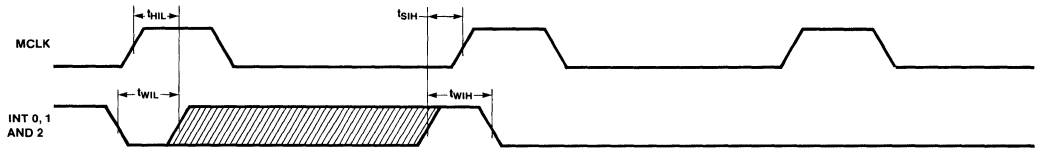
t_{PZL} and t_{PLZ}:



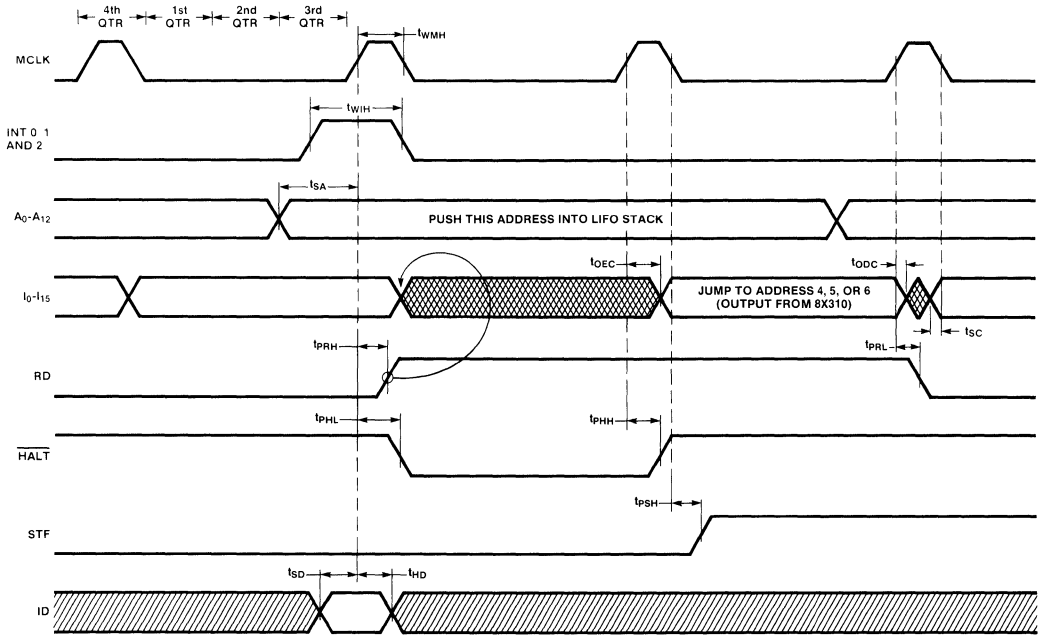
Notes:
1. V_{MEAS} = 1.5 V for all input signals and RD, STF, and HALT outputs.
2. For I_0-I_{15} (t_{OEC}): V_{MEAS} = 1.5 V
   For I_0-I_{15} (t_{ODC}): V_{MEAS} (t_{PLZ}) = V_{OL} + 0.5 V
   V_{MEAS} (t_{PHZ}) = V_{OH} − 0.5 V

TIMING DIAGRAMS

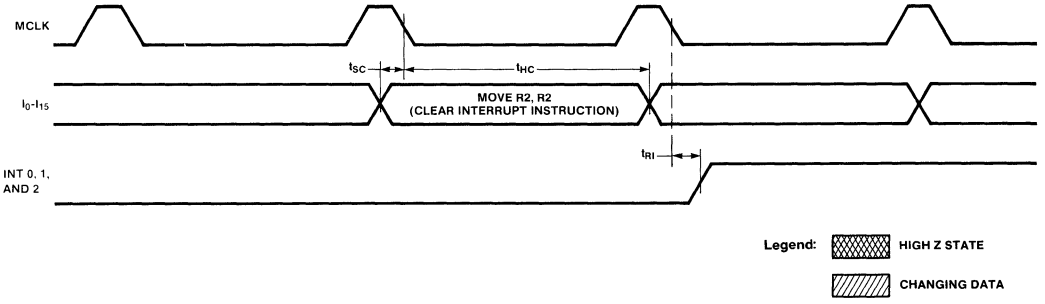
INTERRUPT REQUEST TIMING:



INTERRUPT SERVICE TIMING:

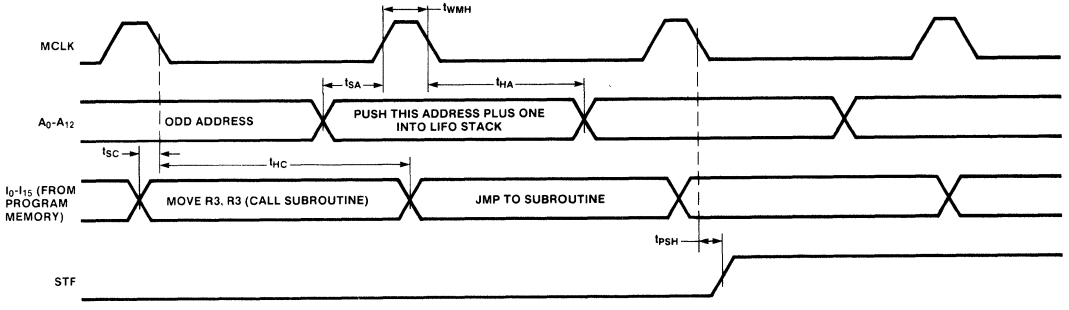


CLEAR INTERRUPT INSTRUCTION TIMING:

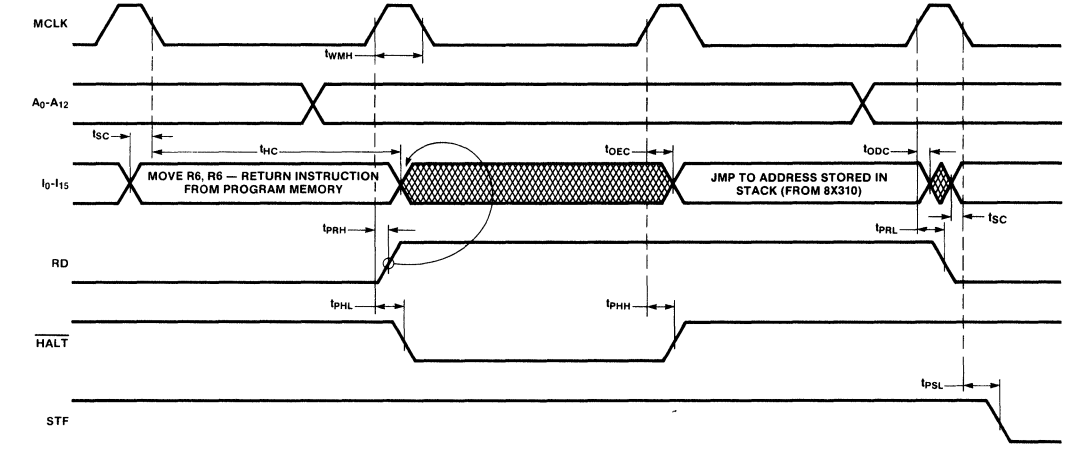


TIMING DIAGRAMS (Continued)

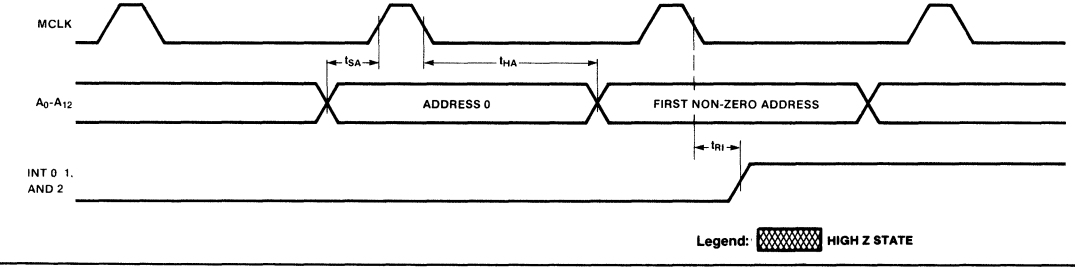
CALL SUBROUTINE TIMING:



RETURN TIMING (FROM INTERRUPT OR SUBROUTINE):



RESET TIMING:



BUS INTERFACE REGISTER ARRAY 8X320

FEATURES

- **16-byte/2-port interface**
- **8- or 16-bit primary port (Host) interface (User selectable)**
- **8-bit secondary port interface**
- **Two 8-bit flag registers (handshake control)**
- **DMA or programmed I/O operation**
- **Two three-state bidirectional ports**
- **Secondary port is bus compatible with 8X305**
- **Single 5V supply**
- **40-pin package**

ARCHITECTURAL OVERVIEW

The Signetics 8X320 Bus Interface Register Array (Figure 1) is a dual-port RAM memory designed for use between a host processor and a peripheral processor. Specifically, the register array provides a convenient and economical interface between the 8X305 (or 8X300) Microcontroller (secondary port) and User's Host System (primary port); the host can be almost any bus-oriented device—another processor, a minicomputer, or a mainframe computer. The host has 8-bit (byte) or 16-bit (word) access to the primary port; data can be read-from or written-into any memory location as determined by the primary-port address and control lines. The secondary port (8X305 bus) consists of eight input/output lines and four bus control lines. To implement the secondary-port interface, an 8-bit memory location is addressed during one machine cycle and, during another cycle, data is read or written under control of the secondary (8X305) processor. Both primary and secondary ports feature three-state outputs and both ports are bidirectional.

Besides the convenience and economy of a two-port memory, the array also provides simple handshake control via two 8-bit flag registers, logic to facilitate DMA transfers, and a write-protect feature for the primary port in both byte and word modes of operation.

BLOCK DIAGRAM

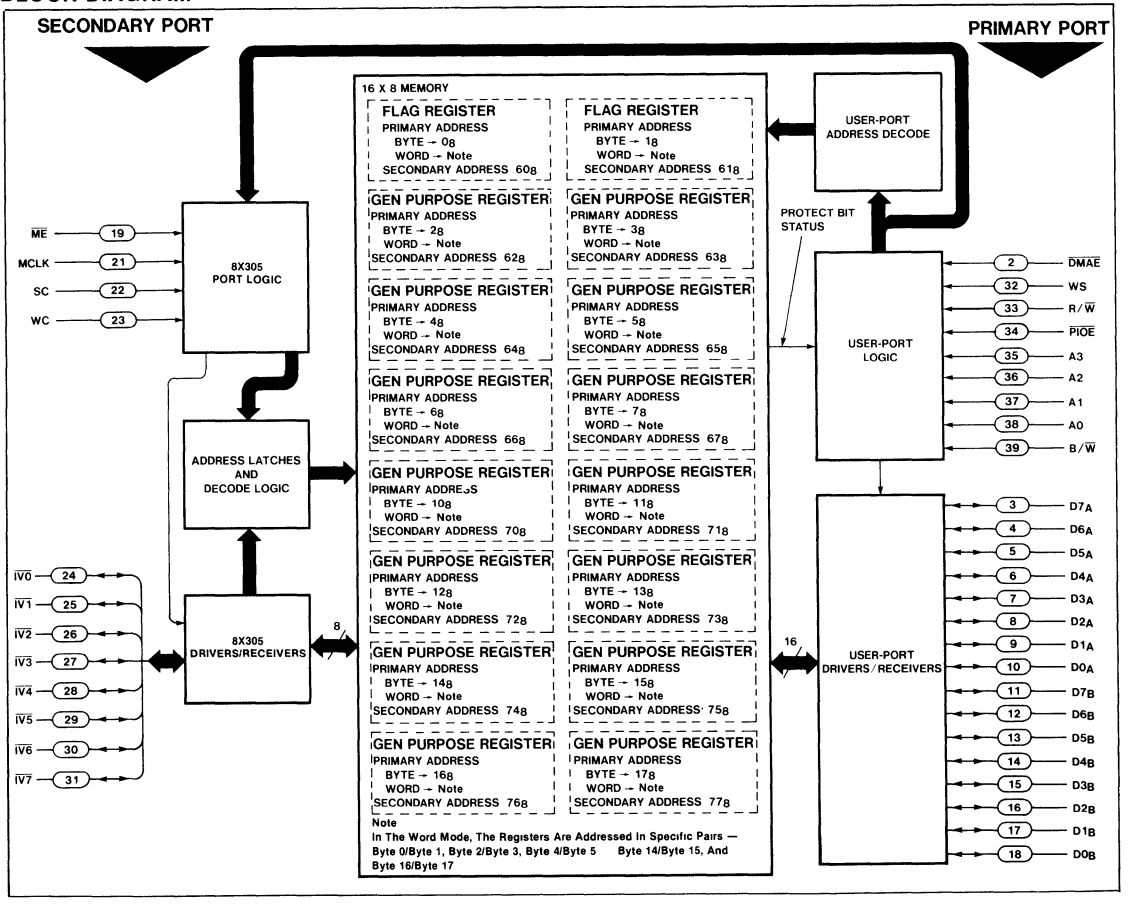
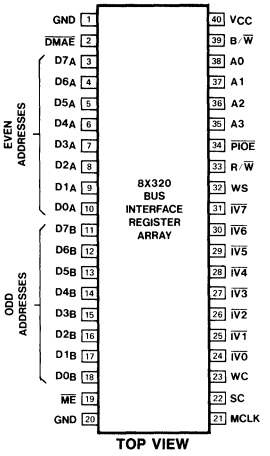


Figure 1. Block Diagram of 8X320 Bus Interface Register Array

BUS INTERFACE REGISTER ARRAY 8X320

N, I PACKAGE



TOP VIEW

ORDER NUMBERS

N8X320N, N8X320I

PIN NO.	PARAMETER		FUNCTION
1, 20	GND	Ground	Circuit ground.
2	$\overline{DMAE}$	Direct Memory Access Enable	Enables primary port to facilitate DMA transfers; does not affect secondary port.
3-18	$D0_A$-$D7_A$/ $D0_B$-$D7_B$	Primary Data Port	Sixteen 3-state lines used for data transfers to-and-from the primary data port; most significant bit is $D0_B$ and least significant bit is $D7_A$.
19	$\overline{ME}$	Master Enable	Enables secondary port when active low ($\overline{ME}$).
21	MCLK	Master Clock	When MCLK is high, and 8X320 is enabled ($\overline{ME}$ = Low), a register location may be either selected or written-into under control of SC and WC.
22	SC	Select Command	With SC high, WC low, MCLK high and $\overline{ME}$ low, data on $\overline{IV0}$ through $\overline{IV7}$ is interpreted as an address. If any one of the 16 register addresses (60_B-77_B) matches that on the I/O (IV) bus, that particular register is selected and remains selected until another address on the same bank (i.e. $\overline{ME}$ = low) is output on the I/O bus—at which time, the old register is deselected and a new register may or may not be selected.
23	WC	Write Command	With WC high, SC low, MCLK high, and $\overline{ME}$ low, the selected register stores contents of $\overline{IV0}$-$\overline{IV7}$ as data.
24-31	$\overline{IV0}$-$\overline{IV7}$	Secondary Data Port	Eight 3-state lines used to transfer data or I/O address to-and-from the secondary data port; most significant bit is $\overline{IV0}$ and least significant bit is $\overline{IV7}$.
32	WS	Write Strobe	When active high, data appearing at the primary port ($D0_A$-$D7_A$/$D0_B$-$D7_B$) is stored in the register array if the primary port is in the *write* mode.
33	R/$\overline{W}$	Read/Write Control	When this signal is high, primary port is in *read* mode; when signal is low, primary port is in *write* mode.
34	$\overline{PIOE}$	Programmed I/O Enable	When active low, primary port operates in programmed input/output mode with register to be read-from or written-into selected by A0-A3.
35-38	A0-A3	Primary Port Address Select	Selects register or register-pair that primary port is to read-from or write-into. Most significant bit is A3; least significant bit is A0.
39	B/$\overline{W}$	Byte/Word	When signal is high, the primary port operates in the byte (8-bit) mode; when signal is low, the primary port operates in the word (16-bit) mode.
40	V_{CC}	Power	+5 volts.

All barred symbols ($\overline{DMAE}$, etc) denote signals that are asserted (or active) when low (logical 0), signals that are not barred are asserted in the high state (logical 1)

OPERATING CHARACTERISTICS

Memory Organization

Memory and address correlation for the 16-register array is shown in Figure 2. From the primary port, the sixteen 8-bit registers can be addressed in either (8-bit) or word (16-bit) format; in the word mode, the registers are addressed in pairs—$0_8/1_8$, $2_8/3_8$, $4_8/5_8$, . . . $14_8/15_8$, and $16_8/17_8$. From the secondary port, all registers are addressed in byte format—60_8 through 77_8. The memory consists of two 8-bit flag registers and fourteen 8-bit general-purpose registers. The flag registers facilitate information transfers between the two ports and, in addition, they protect certain registers from being written into from the primary port.

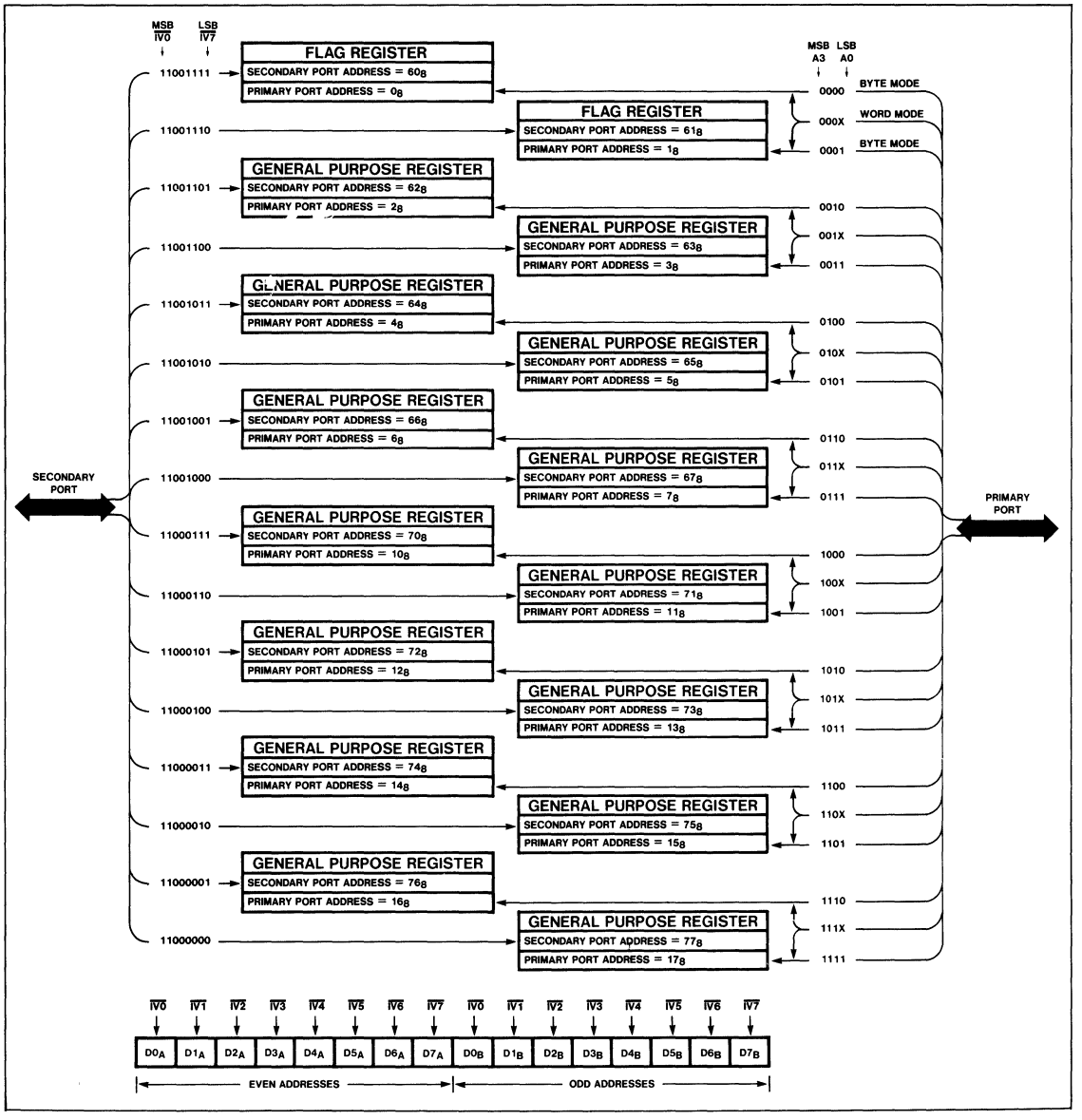


Figure 2. Memory and Address Organization for the 8X320

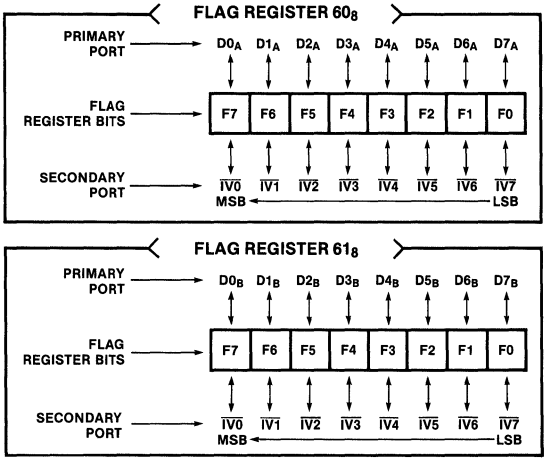
In either byte or word mode, the write-protect logic, implemented by bits F0 and F1 of register 60_8, inhibits the primary port from writing into addresses 16_8 and 17_8, respectively. Both write-protect bits (F0 and F1) can be read or written from the secondary port; the bits are read-only from the primary port.

As shown in Table 1, flag bits F2 through F7 of 60_8 and F0 through F7 of 61_8 are controlled by the fourteen general-purpose registers. When any one of these registers is written into by either port, the corresponding flag bit for that register is automatically set by internal logic of the 8x320. When information is read from any register, the corresponding flag bit must be reset by user software. Except for the write-protect bits, all other flag bits can be read or reset from the primary or the secondary port. Table 2 shows the relationship between bits of the flag registers and bits of the primary and secondary ports.

Table 1. CONTROL OF THE TWO FLAG REGISTERS

Flag Registers	60_8 (0_8)	F2 F3 F4 F5 F6 F7
	61_8 (1_8)	F0 F1 F2 F3 F4 F5 F6 F7
Octal Address of Controlling Byte	Primary	2 3 4 5 6 7 10 11 12 13 14 15 16 17
	Secondary	62 63 64 65 66 67 70 71 72 73 74 75 76 77

Table 2. RELATIONSHIP BETWEEN FLAG REGISTER BITS AND THOSE OF PRIMARY AND SECONDARY PORTS



FUNCTION AND CONTROL OF PRIMARY PORT

The primary port provides an 8-bit (byte) or 16-bit (word) interface between the 16-byte memory and the user's host system. If the host is an 8-bit system (or 16-bit system operating in Byte mode), the sixteen bidirectional I/O lines must be tied together ($D0_A$ to $D0_B$, $D1_A$ to $D1_B$, . . . and $D7_A$ to $D7_B$); when data is input or output on $D0_A$ through $D7_A$, the remaining eight lines ($D0_B$ through $D7_B$) are high-Z and vice-versa.

Other than the Byte/$\overline{\text{Word}}$ control line, specific operating characteristics of the primary port are controlled by two signals—$\overline{\text{PIOE}}$ (Programmed I/O Enable) and $\overline{\text{DMAE}}$ (Direct Memory Access Enable). When $\overline{\text{PIOE}}$ is active (low) and $\overline{\text{DMAE}}$ is inactive (high), the primary port operates in the programmed I/O mode—refer to Table 3; in this mode of operation, the register to be read-from or written-into is determined by four address lines (A0 through A3) and the Byte/$\overline{\text{Word}}$ control line—see Figure 2 and Table 4. In the DMA mode of operation, A1, A2, and A3 are not used; data is read-from or written-into preassigned registers: bytes 16_8 (76_8) and 17_8 (77_8) for the byte mode of operation and bytes 14_8 (74_8)/15_8 (75_8) and 16_8 (76_8)/17_8 (77_8) for the word mode of operation. In both cases, switching between bytes 16_8 and 17_8 in the byte mode and 14_8/15_8 and 16_8/17_8 in the word mode is controlled by A0 (the least significant address bit). Refer to Table 5.

Table 3. MODE CONTROL OF PRIMARY PORT

MODE	$\overline{\text{PIOE}}$	$\overline{\text{DMAE}}$
Disabled (output)	1	1
Programmed I/O	0	1
DMA	X	0

X = Don't Care

Table 4 defines programmed I/O operation of the primary port in terms of read/$\overline{\text{write}}$ functions and Byte/$\overline{\text{Word}}$ control. In the byte mode, data is read-from or written-into the even addresses (0_8, 2_8, 4_8, 6_8, 10_8, 12_8, 14_8, and 16_8) via data lines $D0_A$ through $D7_A$; data is read-from or written-into odd addresses (1_8, 3_8, 5_8, 7_8, 11_8, 13_8, 15_8, and 17_8) via data lines $D0_B$ through $D7_B$. When A0 is low (logical 0), even addresses are selected and when A0 is high (logical 1), odd addresses are selected; thus, A0 is the LSB of a 4-bit address. In the word mode, the state of A0 is irrelevant, since both the odd and even bytes are, simultaneously, read-from or written-into; thus, a register pair is selected by a 3-bit address, A1 being the LSB.

In the DMA mode of operation with $\overline{\text{DMAE}}$ set to 0 and other conditions satisfied, data is directly transferred to-or-from specified memory locations under control of Byte/$\overline{\text{Word}}$, R/$\overline{\text{W}}$, and A0. The state of the Byte/$\overline{\text{Word}}$ control line determines whether the data word is 8 bits or 16 bits. The A0 address line correlates eight of

Table 4. PRIMARY PORT OPERATING IN PROGRAMMED I/O MODE

MODE	B/$\overline{\text{W}}$	A0	$D0_A$-$D7_A$ (Even Addresses)	$D0_B$-$D7_B$ (Odd Addresses)
Read	0 (Word)	X	Stored Data	Stored Data
Read	1 (Byte)	0	Stored Data	HI-Z
Read	1 (Byte)	1	HI-Z	Stored Data
Write	0 (Word)	X	Write	Write
Write	1 (Byte)	0	Write	No Change
Write	1 (Byte)	1	No Change	Write

X = Don't Care

the sixteen data lines ($D0_A$-$D7_A$ or $D0_B$-$D7_B$) with the proper byte/word location. Thus, in the word mode, the exchange of data between the memory and the primary port occurs via $D0_A$-$D7_A$ for bytes 14_8 and 16_8 and via $D0_B$-$D7_B$ for bytes 15_8 and 17_8. The byte mode of operation is similar, except that the unused eight lines are three-stated.

FUNCTION AND CONTROL OF SECONDARY PORT

The secondary port provides an 8-bit interface between the sixteen memory registers and the 8X305 (or other processor). As shown in Table 6, the secondary-port interface is controlled by five input signals and a status latch. The status latch is set when SC is high (MCLK high/$\overline{ME}$ low) and a valid memory address (60_8-77_8) is presented to the 8X320 via the secondary data port ($\overline{IV0}$-$\overline{IV7}$). The latch is cleared by internal logic when an invalid memory address is presented at the secondary port. In all read/write operations from the secondary port, the status latch acts like a master enable; data can be transferred only if the status latch is set.

Table 5. DMA OPERATION OF THE PRIMARY PORT

MODE	BYTE/WORD	A0	$D0_A$-$D7_A$	$D0_B$-$D7_B$
Read	0 (Word)	0	Data stored in byte 14_8	Data stored in byte 15_8
Read	0 (Word)	1	Data stored in byte 16_8	Data stored in byte 17_8
Read	1 (Byte)	0	Data stored in byte 16_8	HI-Z
Read	1 (Byte)	1	HI-Z	Data stored in byte 17_8
Write	0 (Word)	0	Write to byte 14_8	Write to byte 15_8
Write	0 (Word)	1	Write to byte 16_8	Write to byte 17_8
Write	1 (Byte)	0	Write to byte 16_8	HI-Z
Write	1 (Byte)	1	HI-Z	Write to byte 17_8

Table 6. FUNCTIONAL CONTROL OF SECONDARY PORT

$\overline{ME}$	SC[1]	WC[1]	MCLK	R/$\overline{W}$	STATUS LATCH	FUNCTION OF SECONDARY BUS
L	L	L	X	X	Set	Output data from 8X320 memory to 8X305
L	L	H	H	H	Set	Data from 8X305 is input and written-into a previously-selected memory location of the 8X320 (Note 2).
L	L	H	H	L	Set	With the primary port in the write mode (R/$\overline{W}$ = 0), the secondary port is overridden and cannot write to the same register addressed by the primary port; however, the register addressed by the primary port can be read and any other register can be read-from or written-into from the secondary port (Note 2).
L	H	L	H	X	X	Data transmitted to the secondary port via the $\overline{IV}$ bus is interpreted as an address; if address is within range of 60_8-77_8 the memory status latch is subsequently set.
L	L	H	L	X	X	Inactive
L	H	L	L	X	X	Inactive
L	L	X	X	X	Not Set	Inactive
H	X	X	X	X	X	Inactive

Notes:
1. The SC and WC lines should never both be high at the same time, the 8X305 processor never generates this condition
2. During read or write operations, the same register can be simultaneously addressed from either port. For any write operation by both ports on the same register, the primary port has priority, other than this, the 8X320 does not indicate error conditions or resolve conflicts
3. X = Don't Care.

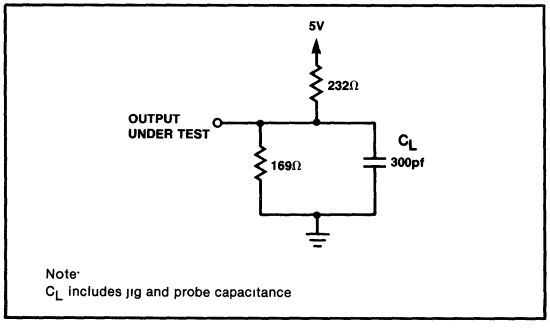
BUS INTERFACE REGISTER ARRAY 8X320

DC CHARACTERISTICS $0°C \leq T_A \leq 70°C$; $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1, 2]	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
$V_{IN\ (L)}$	Low level input voltage				0.80	V
$V_{IN\ (H)}$	High level input voltage		2.0			V
V_{OL}	Low level output voltage	V_{CC} = 4.75V; I_{OL} = 16mA			0.55	V
V_{OH}	High level output voltage	V_{CC} = 4.75V; I_{OH} = −3mA	2.40			V
V_{CL}	Input clamp voltage	I_I = −5mA			−1.00	V
I_{CC}	Supply current	V_{CC} = 5.25V (Both ports high-Z)			270	mA
I_{OS}	Short circuit output current[3]	V_{CC} = 4.75V	−20		−100	mA
$I_{IN\ (L)}$	WC, MCLK, SC, & $\overline{ME}$	V_{CC} = 5.25V; V_{IL} = 0.50V			−1.0	mA
$I_{IN\ (L)}$	B/$\overline{W}$	V_{CC} = 5.25V; V_{IL} = 0.50V			−1.6	mA
$I_{IN\ (L)}$	A0-A3	V_{CC} = 5.25V; V_{IL} = 0.50V			−1.0	mA
$I_{IN\ (L)}$	$\overline{DMAE}$	V_{CC} = 5.25V; V_{IL} = 0.5V			−800	μA
$I_{IN\ (L)}$	WS, $\overline{PIOE}$, & R/$\overline{W}$	V_{CC} = 5.25V; V_{IL} = 0.5V			−400	μA
$I_{IN\ (L)}$	$\overline{IV0}$-$\overline{IV7}$	V_{CC} = 5.25V; V_{IL} = 0.5V			−400 each line	μA
$I_{IN\ (L)}$	$D0_A$-$D7_A$/$D0_B$-$D7_B$	V_{CC} = 5.25V; V_{IL} = 0.5V			−400 each line	μA
$I_{IN\ (H)}$	WC, SC, MCLK, & $\overline{ME}$	V_{CC} = 5.25V; V_{IH} = 5.25V			100	μA
$I_{IN\ (H)}$	B/$\overline{W}$	V_{CC} = 5.25V; V_{IH} = 5.25V			240	μA
$I_{IN\ (H)}$	A0	V_{CC} = 5.25V; V_{IH} = 5.25V			120	μA
$I_{IN\ (H)}$	A1-A3	V_{CC} = 5.25V; V_{IH} = 5.25V			60	μA
$I_{IN\ (H)}$	$\overline{DMAE}$	V_{CC} = 5.25V; V_{IH} = 5.25V			120	μA
$I_{IN\ (H)}$	WS, $\overline{PIOE}$, & R/$\overline{W}$	V_{CC} = 5.25V; V_{IH} = 5.25V			60	μA
$I_{IN\ (H)}$	$\overline{IV0}$-$\overline{IV7}$ and $D0_A$-$D7_A$/$D0_B$-$D7_B$	V_{CC} = 5.25V; V_{IH} = 5.25V			100	μA

Notes
1 Operating temperature ranges are guaranteed after terminal equilibrium has been reached
2 All voltages are measured with respect to ground terminal
3 Short only one output at a time

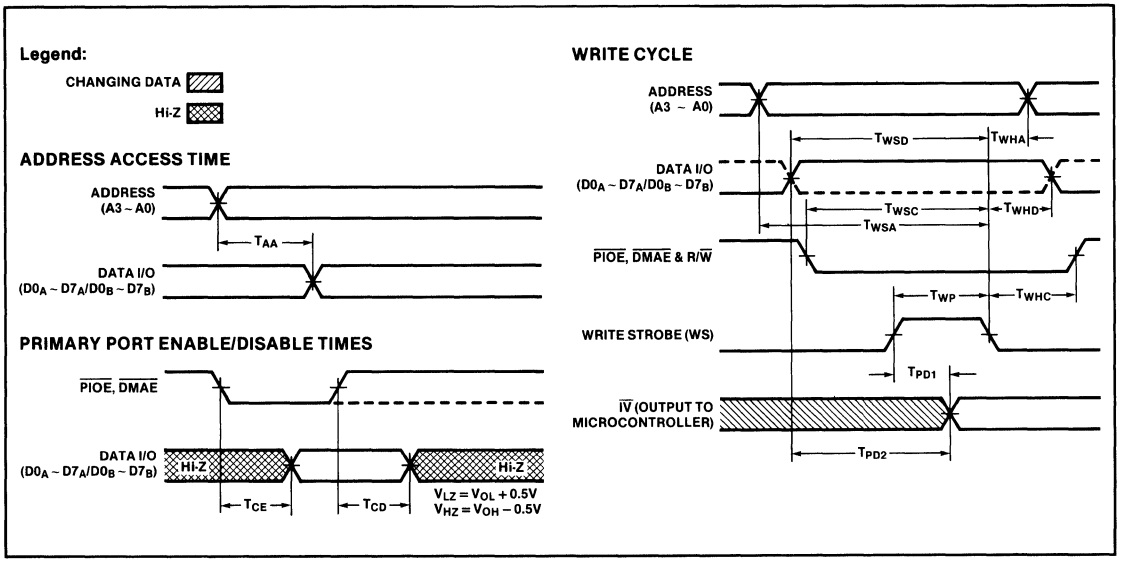
TEST CIRCUIT



Note:
C_L includes jig and probe capacitance

AC CHARACTERISTICS OF PRIMARY PORT

$0°C \leq T_A \leq 70°C$; $4.75V \leq V_{CC} \leq 5.25V$
Loading: See Test Circuit



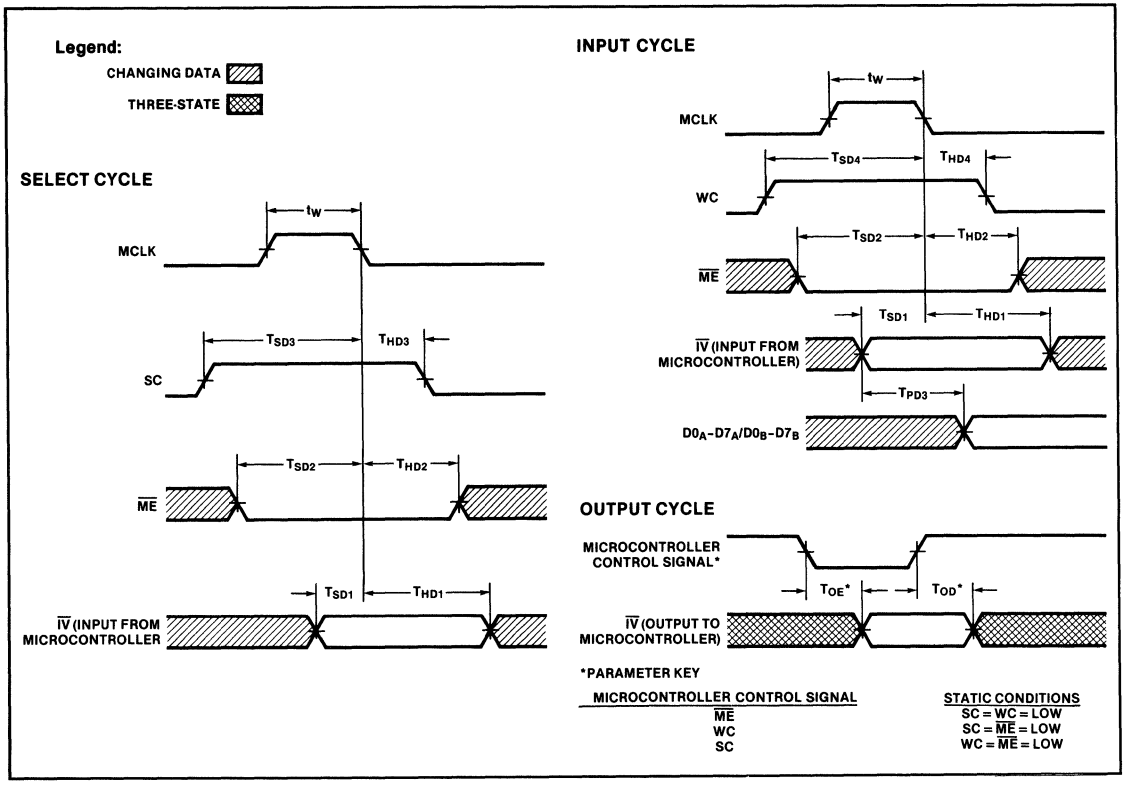
PARAMETER		FROM	TO	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
T_{AA}	Address Access Time	A3-A0	$D0_A$-$D7_A$/$D0_B$-$D7_B$			45	ns
T_{CE}	Primary port enable time	↓PIOE ↓DMAE	$D0_A$-$D7_A$/$D0_B$-$D7_B$			30	ns
T_{CD}	Primary port disable time	↑PIOE ↑DMAE	$D0_A$-$D7_A$/$D0_B$-$D7_B$			35	ns
T_{WSA}	Address setup time	A3-A0	↓WS	40			ns
T_{WHA}	Address hold time	↓WS	A3-A0	0			ns
T_{WSD}	Primary port data setup time	$D0_A$-$D7_A$/$D0_B$-$D7_B$	↓WS	30			ns
T_{WHD}	Primary port data hold time	↓WS	$D0_A$-$D7_A$/$D0_B$-$D7_B$	0			ns
T_{WSC}	Write mode control setup time	PIOE DMAE R/W	↓WS ↓WS ↓WS	30 40 30			ns ns ns
T_{WHC}	Write mode control hold time	↓WS	PIOE DMAE R/W	10 10 10			ns ns ns
T_{WP}	Write strobe pulse width			25			ns
T_{PD1}[1]	Primary port data delay	$D0_A$-$D7_A$/$D0_B$-$D7_B$	IV0-IV7			75	ns
T_{PD2}[2]	Primary port data delay from WS	↑WS	IV0-IV7			75	ns

Notes:
1 Measurement with Write Strobe set High and the control signals of the secondary port set for output data from the same register
2 Measurement with primary port data stable and control signals of secondary port set for output data from the same register.

BUS INTERFACE REGISTER ARRAY 8X320

AC CHARACTERISTICS OF SECONDARY PORT

$0°C \leq T_A \leq 70°C$, $4.75V \leq V_{CC} \leq 5.25V$
Loading: See Test Circuit



	PARAMETER	FROM	TO	LIMITS			UNIT
				Min	Typ	Max	
t_W	MCLK pulse width			30			ns
T_{SD1}	Data setup time	$\overline{IV0}$-$\overline{IV7}$	↓MCLK	35			ns
T_{SD2}	$\overline{ME}$ setup time	$\overline{ME}$	↓MCLK	30			ns
T_{SD3}	SC setup time	SC	↓MCLK	30			ns
T_{SD4}	WC setup time	WC	↓MCLK	30			ns
T_{HD1}	Data hold time	↓MCLK	$\overline{IV0}$-$\overline{IV7}$	0			ns
T_{HD2}	$\overline{ME}$ hold time	↓MCLK	$\overline{ME}$	0			ns
T_{HD3}	SC hold time	↓MCLK	SC	0			ns
T_{HD4}	WC hold time	↓MCLK	WC	0			ns
T_{PD3} (Note)	$\overline{IV}$ propagation delay	$\overline{IV}$	$D0_A$-$D7_A$/$D0_B$-$D7_B$			45	ns
T_{OE}	Output enable	$\overline{ME}$, SC, or WC	$\overline{IV0}$-$\overline{IV7}$			30	ns
T_{OD}	Output disable	$\overline{ME}$, SC, or WC	$\overline{IV0}$-$\overline{IV7}$			20	ns

Note:
Measured with MCLK = High and control signals of the primary port set for output data from the same register

FLOPPY DISK FORMATTER/CONTROLLER 8X330

FEATURES

- **Single or double density encoding/decoding**
- **On-chip data separator**
- **Programmable:**
  - **FM, MFM, and M²FM encoding/decoding**
  - **Preamble Polarity**
  - **Data transfer rate**
  - **Address mark encoding/decoding**
  - **Sector length**
  - **Output port (7-bits disk command)**
  - **Input port (5-bits disk status)**
- **Write Precompensation with on/off control**
- **On-chip phase lock loop**
- **CRC generator with software-controlled error correction capabilities**
- **40-pin package**
- **+5 volt operation**

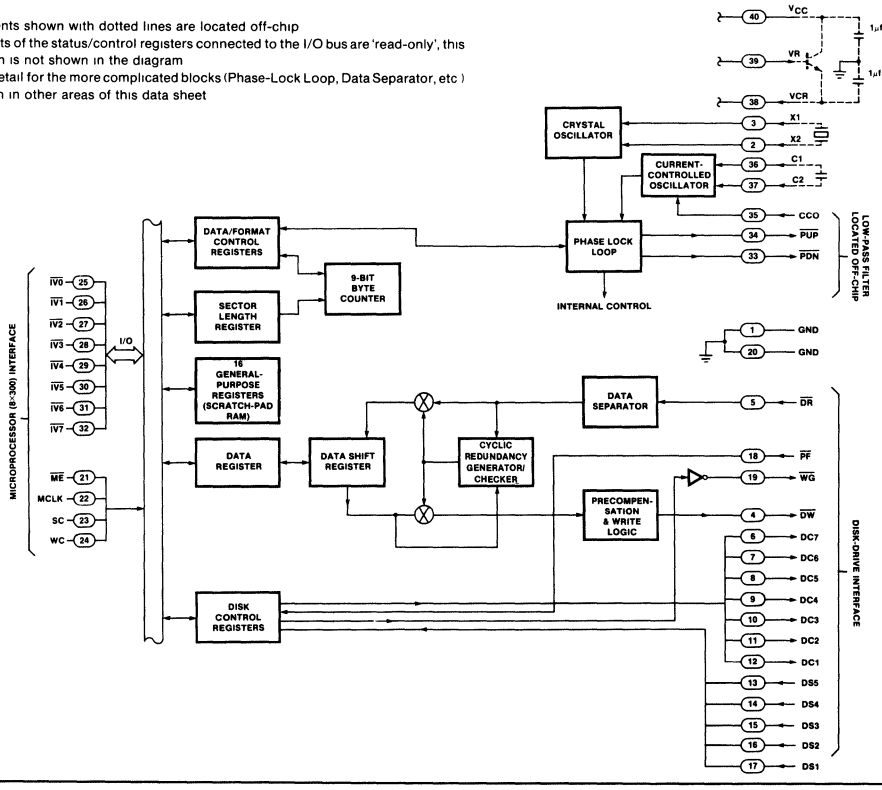
PRODUCT DESCRIPTION

The Signetics 8X330 Floppy Disk Formatter/Controller is a monolithic peripheral device of the 8X300 Family. The chip uses Bipolar-Schottky/I²L-Technology and some very unique features to provide 8X330 customers with a competitive edge in both simple and complicated disk-controller designs. The competitive advantage is measurable in terms of "systems parts count", "error correction capabilities", and "overall design concepts" that are applications oriented. Except for a crystal, a capacitor, an external transistor acting as a series-pass element for the on-chip voltage regulator, an active low-pass filter, and an optional off-chip voltage controlled oscillator (refer to Features and Option), the 8X330 contains all processing circuits and the required control logic to encode/decode double-density (MFM/M²FM) and single-density (FM) codes. Even the data-separation and write-precompensation logic are located on the chip; in addition, 16-bytes of scratch-pad RAM are provided for storage of various control/status parameters.

OPTION: External Voltage Controlled Oscillator (VCO). For critical applications, window margins can be improved by as much as 6% with the use of an external VCO.

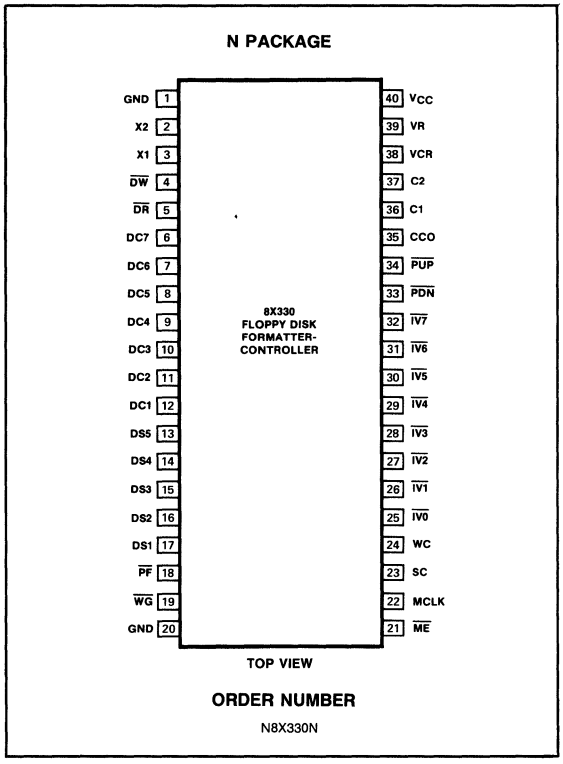
BLOCK DIAGRAM

NOTES
1 Components shown with dotted lines are located off-chip
2 Certain bits of the status/control registers connected to the I/O bus are 'read-only', this distinction is not shown in the diagram
3 Greater detail for the more complicated blocks (Phase-Lock Loop, Data Separator, etc) are shown in other areas of this data sheet



FLOPPY DISK FORMATTER/CONTROLLER 8X330

8X330 PACKAGE/PIN DESIGNATIONS



ORDER NUMBER

N8X330N

PIN NO.	MNEMONIC & DEFINITION		FUNCTION
1, 20	GND	Ground	Circuit ground
2, 3	X1, X2	Crystal inputs	Inputs from a crystal that determines frequency of an on-chip crystal oscillator
4	$\overline{DW}$	Data write	A series of negative-going pulses transmitted to the disk drive The data write signal produces pulses (with precompensation, if required) for data and clock in accordance with the applicable encoding rules (FM, MFM or M²FM)
5	$\overline{DR}$	Data read	Negative-going pulses transmitted from the disk drive to a Schmitt-trigger input of the 8X330, these pulses represent encoded data and clock from the disk media
6-12	DC1-DC7	Disk commands	Seven outputs from the 8X330 that allow general-purpose control, of one or more disk drives
13-17	DS1-DS5	Disk status	Five general-purpose Schmitt-trigger inputs from the disk drive (or drives) that provide status information for the 8X300
18	$\overline{PF}$	Power fail	Schmitt-trigger input from external logic that is active (low) when the "user-sensed" power supply voltage drops below a predetermined value
19	$\overline{WG}$	Write gate	When active (low), this 40-milliampere open-collector output enables writing to the disk media When $\overline{PF}$ is low, the write gate is inhibited during periods of power supply uncertainty
21	$\overline{ME}$	Master enable	When this input signal is active (low), the 8X330 can be accessed and enabled by the 8X300 (Refer to the $\overline{LB}$ and $\overline{RB}$ pinout discriptions of the 8X300 for further detail)
22	MCLK	Master clock	When active high and with $\overline{ME}$ in the active-low state, this input signal provides a means whereby the I/O output from the 8X300 is interpreted as an enabling address (provided there is an address match) or as input data (if one of the 8X330 registers has already been selected)
23	SC	Select command	When this signal is active (high), the information output on pins $\overline{IV0}$-$\overline{IV7}$ of the 8X300 is interpreted as an address input by the 8X330
24	WC	Write command	When this signal is active (high), the information output on pins $\overline{IV0}$-$\overline{IV7}$ of the 8X300 is interpreted as input data by the 8X330
25-32	$\overline{IV0}$-$\overline{IV7}$	Input/output lines	Eight three-state input/output lines that provide bidirectional data transfers between the 8X300 and the enabled I/O device, $\overline{IV7}$ is the *Least Significant Bit.*
33	$\overline{PDN}$	Pump down output	Open-collector output of on-chip phase detector which indicates (by a negative-going, quantized, pulse-width modulated signal) that internal CCO frequency is too high
34	$\overline{PUP}$	Pump up output	Open-collector output of on-chip phase detector which indicates (by a negative-going, quantized, pulse-width modulated signal) that internal CCO frequency is too low.
35	CCO	Frequency Control Input for Current-Controlled Oscillator	Variable input current from external low-pass filter that controls the frequency of the oscillator
36-37	C1, C2	Capacitor input terminals	Inputs for capacitor that determines center frequency of the current-controlled oscillator
38	VCR	Regulated supply voltage	DC voltage input from emitter of external series-pass transistor, this voltage powers internal logic of chip
39	VR	Reference voltage	Reference voltage output to base of series-pass transistor, this reference controls VCR
40	V_{CC}	Supply voltage	+5 volt power

SYSTEM INTERFACE

A typical floppy disk controller using an 8X300 microcontroller and the 8X330 is shown in Figure 2. The non-shaded portion of this particular configuration can service the command, status, and input/output requirements of two double-sided disk drives and, under software supervision, the system can read/write single-density (FM) or double-density (MFM/M2FM) codes. Interface requirements are simple—on one hand, consisting of the 8X300 microcontroller and, on the other, the two disk drives. All 8X330 control and data registers directly linked to the microprocessor interface (Figure 1) are addressable and appear to the 8X300 as simple I/O ports; a 13-bit address bus and a 16-bit instruction bus provide communications between the 8X300 and up to 8K of microprogram storage.

The disk-drive interface consists of seven (7) output control lines (DC1-DC7), five (5) input status lines (DS1-DS5), a write gate ($\overline{WG}$), a data- write output ($\overline{DW}$), and a data-read input ($\overline{DR}$). The twelve command/status lines are not dedicated; thus, the user can assign system functions to best suit a given application. As shown in Figure 2, all control lines except $\overline{WG}$ are buffered to accommodate a reasonable distance between the controller and the disk media; the Write Gate, being a 40-milliampere output, requires no buffering.

As shown by the shaded part of Figure 2, the control and status lines can be expanded with peripheral hardware—the 8T32 (in this example) being only one method of implementation. Using this particular technique, one I/O port is totally dedicated to output control, whereas, the other port is totally dedicated to input status. With additional hardware and supporting software, the disk-drive system can be expanded without limit; however, from a point of being practical, five or six drives is sufficient for most applications. By using the programmable features of the 8X330, the user can emphasize and prioritize those system parameters that are most important—economics, reliability and/or speed.

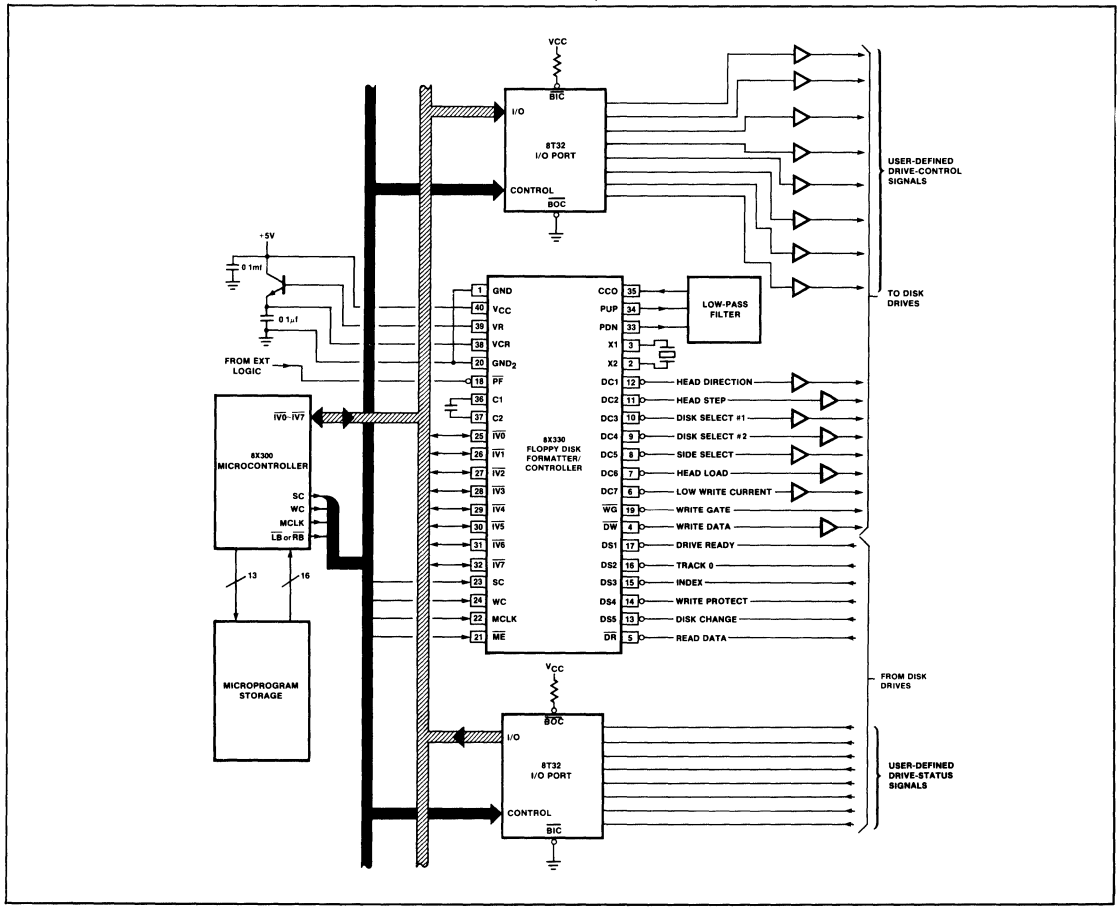


Figure 2. Typical Interface Using an 8X300 Microcontroller

FUNCTIONAL OPERATION

As shown in Figure 2, the interface between the 8X300 and 8X330 consists of twelve (12) lines—$\overline{IV0}$-$\overline{IV7}$, SC, WC, MCLK, and $\overline{ME}$; the Master Enable ($\overline{ME}$) input (pin 21) is driven from either the $\overline{LB}$ (Left Bank) or $\overline{RB}$ (Right Bank) output of the 8X300. An expanded view of this interface is shown in Figure 3 and, as indicated, the 8X330 appears as a number of addressable registers (110_8-127_8 and 132_8-137_8) under input/output control of the 8X300. These registers are used for general-purpose storage, data-transfer operations, disk commands, disk status, and various control functions. Design-oriented information for these registers and other data-processing/logic functions of the 8X330 are described in the paragraphs that follow; in all of these registers, bit 0 is the Most Significant Bit (MSB).

NOTE
When power is first applied to the 8X330, the Disk Command lines (DC1-DC7), the Write Gate ($\overline{WG}$) output, and contents of Command/Status Register #2 (CSR #2) are set to 1 (high). The wakeup state of all other bits is undefined

General-Purpose Register File

This general-purpose (scratch pad) memory is directly accessible by the 8X300 and is used to store system variables such as track address, sector address and other necessary parameters. The sixteen 8-bit registers (110_8-127_8) provide sufficient on-chip memory to accommodate a minimum of two disk drives; the maximum number of drives that this non-dedicated memory file can support depends on several factors—system configuration, reliability requirements, economic constraints, and so on. Because of the on-chip file, all other system memory can be dedicated to the purpose of handling data to-and-from the disk media.

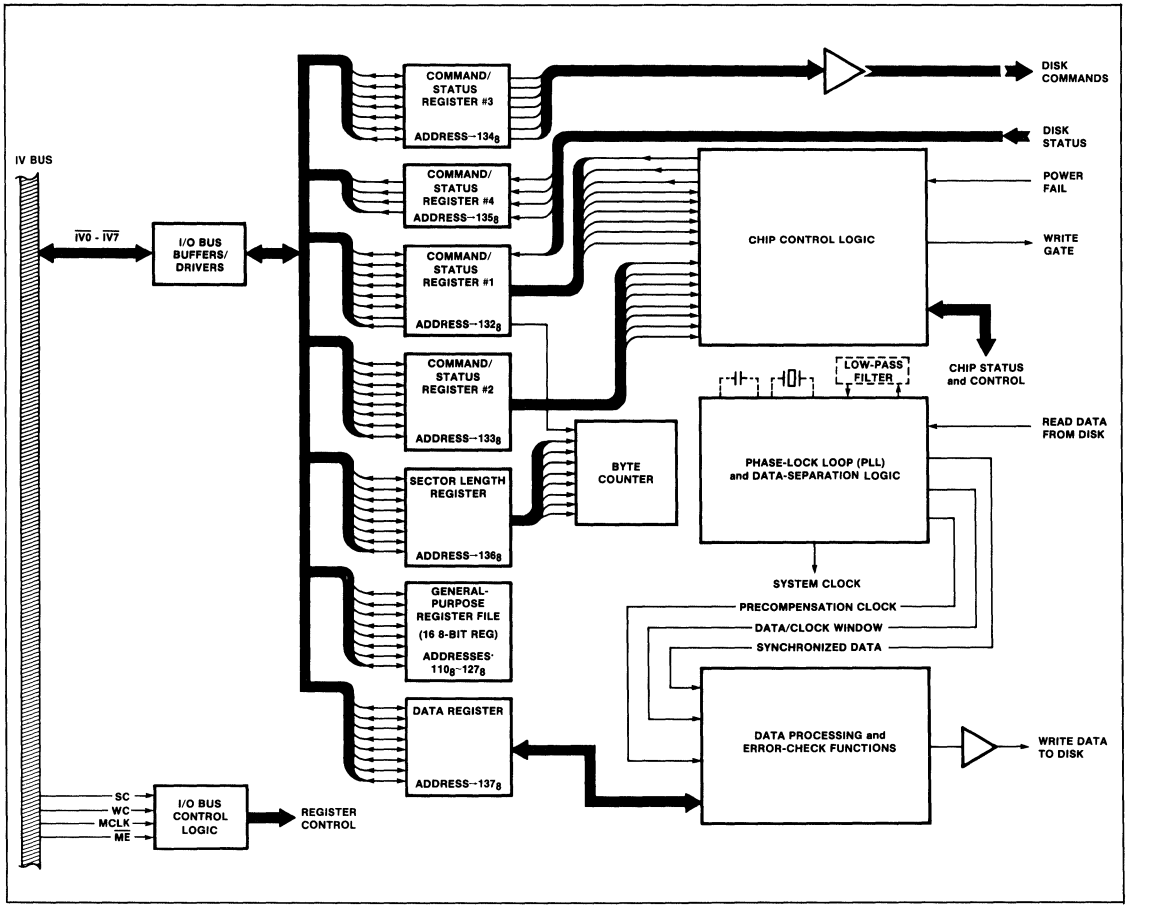


Figure 3. An Expanded View of the 8X330/8X300 Interface

Command/Status Register #1 (CSR 1/Address 132_8)

The disk status (read) or disk-command (write) contents of this register are interpreted as follows; unless otherwise indicated, all bits of CSR 1 are read/write from the I/O bus.

Bit 0 (Write Gate Enable)
Enables write gate output ($\overline{WG}$/pin 19) to disk drive(s)—the write gate ($\overline{WG}$) cannot be enabled unless the PF input pin (18) is high. When the WGE bit is set to 0, the $\overline{WG}$ ouput pin is low (enabled); when WGE is set to 1, the $\overline{WG}$ output is high (disabled). If the PF input goes low while the $\overline{WG}$ output is low, the $\overline{WG}$ output will go high and the Write Gate Enable bit is reset to 1.

Bit 1 (CRC Enable)
When set to 1, permits internal CRC register to compute remainders on the data stream in either read or write modes of operation. When set to 0, the CRC register becomes the source of data. A change in the CRC Enable bit does not become effective until the "next BYTRA flag appears" following the command bit change—refer to description of CSR 1/Bit 6.

Bit 2 (Data Register Control)
When set to 0, contents of data register consists of interleaved data-and-clock bits; starting from the MSB ($\overline{IV0}$) position, register contents are: Clock 1, Data 1, Clock 2, Data 2, Clock 3, Data 3, Clock 4, and Data 4. When writing an address mark, the appropriate data/clock pattern is loaded into the data register by the 8X300. Since each byte of data from the processor becomes an interleaved pattern (4-bits of data and 4-bits of clock) in the 8X330 data register, two bytes from the processor are required to write each full byte of address mark to the drive—eight bit cells with each cell containing a possible data and/or clock transition, or a total of 16 bit positions. When writing address marks, the normal on-chip clock insertion circuitry of the 8X330 is inhibited; thus, the user is free to define any clock/data pattern for the address mark.

When reading address marks, the data register is loaded with data and clock representing four bit cells from the disk media. The information in the data register can then be compared with the expected address mark by the 8X300 on a nibble-by-nibble basis. When the DRC bit is set to 1, the data register contains separated data (no clocks). A state change in this bit does not become effective until the "next BYTRA flag appears" following the state-change command.

Bit 3 (Sync Enable)
The Sync Enable bit allows the on-chip data separator to obtain bit and byte synchronization; this bit also controls initialization of the CRC Register. With the 8X330 in Read mode and with Bit 3 set to 0, bit synchronization occurs. The Preamble field is assumed to be all "zeroes" or all "ones" as determined by the Preamble Select bit (CSR 2/Bit 4).

When the proper number of preamble bytes, as determined by the disk-control program, have been found, the Sync Enable bit should be changed, under program direction, to a 1. This puts the 8X330 in the Address-Mark search mode. Accordingly, all bits of the CRC Register are preset to 1, the BYte TRAnsfer flag is inhibited, and the 8X330 examines the data stream for an Address Mark. The Address Mark is detected by observing the data and clock bits to find a change in the normal Preamble pattern. Byte synchronization is achieved by assuming that the change occurred in the bit cell determined by two Bit Select bits (CSR 2/Bits 2 and 3).

When the pattern change is found indicating the start of an Address Mark, the 8X330 starts CRC computation and synchronizes BYTRA to the byte boundaries. Note that the 8X330 presumes an Address Mark by finding a change in the preamble pattern; however, it is up to the 8X300 to read the Address Mark and to establish its validity or non-validity

In write mode, setting the Sync Enable bit to 0 presets all bits of the CRC Register to 1. Setting the Sync Enable bit to 1 allows CRC computation to begin at the next byte boundary.

Bit 4 (Load Counter)
When set to 1, transfers 8-bits of data from Sector Length register and 1-bit (MSB) of data from Byte Counter (refer to next description) to 9-bit Byte Counter. Loading of the 9-bit Byte Counter is effective one bit-cell time after the Load Counter bit is set to 1. In both the read and write modes of operation, the Byte Counter is incremented by BYTRA. The Load Counter bit is self-clearing and always returns a 0 when read.

NOTE
The Load Counter bit must be set one or more instruction cycles *after* setting the Byte Counter MSB, that is, bits 4 and 5 of CSR 1 cannot be set during th same instruction cycle

Bit 5 (Byte Counter MSB)
This bit is used to set and monitor the state of the ninth (MSB) bit in the Byte Counter; reading this bit always returns the current state of MSB in the Byte Counter. The MSB of the Byte Counter is set to the value of CSR 1/Bit 5 when the Load Counter bit (CSR 1/Bit 4) is asserted—refer to preceding description.

NOTE
The Byte Counter MSB must be set one or more instruction cycles *before* the Load Counter bits—bits 4 and 5 of CSR 1 cannot be set during the same instruction cycle

Bit 6 (BYTRA)
During a disk read operation, the BYte TRAnsfer flag is automatically set to 0 when 8-bits of information are transferred from the Data Shift Register to the Data Register —see Figure 1. During a disk write operation, BYTRA is automatically set to 0 when 8-bits are transferred from the Data Register to the Data Shift Register. BYTRA (a read-

only bit) is reset to a 1 when the Data Register (address 137_8) is selected by the user's program. During read/write operations, the 1-to-0 transition of the BYTRA flag increments the Byte Counter to keep count of bytes read or bytes written. All read-only bits of the 8X330 are designed to remain stable during the monitor period; thus, to read a status change of BYTRA, Disk-Status bit, the Byte Counter MSB, or other read-only bit requires a two-instruction loop similar to:

```
TEST    SEL   CSR 1
        NZT   BYTRA,   TEST
```

Bit 7 (Disk Status 1)
Reflects state (0 or 1) of input DS1 (pin 17); this is a user-definable read-only bit.

NOTE
A high input on any one of the Disk Status lines of the 8X330 is read by the 8X300 program as a logical 1 and a low input on the status lines is read as a logical 0

Command/Status Register #2 (CSR 2/Address 133_8)

The disk status (read) or disk-command (write) contents of this register are interpreted as follows:

Bit 0 (Precompensation Enable)
This command bit determines whether or not precompensation is applied to the data stream being written onto the disk. When set to 0, precompensation is inhibited. When set to 1 and with double-density encoding, write precompensation is applied to the following data/clock bit patterns:

Precomp Time	Data/Clock Pattern (in Data Shift Reg)			Bit Being Written	Bits Already Written to Disk		
2T (Late)	0	1	**0**	1	0	0	0
2T (Late)	0	1	**0**	1	0	0	1
2T (Early)	1	0	**0**	1	0	1	0
2T (Early)	0	0	**0**	1	0	1	0

where, $T = \frac{1}{\text{crystal frequency}}$ if bit 7 of CSR 2 ($1/2F$) = 1

$T = \frac{2}{\text{crystal frequency}}$ if bit 7 of CSR 2 ($1/2F$) = 0

Bit 1 (Read Mode)
When set to 0, the 8X330 reads data from the disk and transfers it to the Data Register; when set to 1, data from the Data Register is transferred to the disk, provided the Write Gate Enable bit (CSR1/Bit 0) is set to 1. With WGE set to 0 and the Read Mode bit set to 1, the current-controlled oscillator is forced to lock onto the crystal oscillator; this technique is used during a data-read operation to ensure rapid acquisition of the disk data.

Bits 2,3 (Bit Selects 1 and 0)
Together with the Sync Enable (CSR 1/Bit 3), these two bits allow the user to establish byte boundaries for the data stream; this is done in the following way. After bit synchronization is established, and the preamble pattern is verified, the 8X330 looks for a change in the normal preamble pattern. As shown in the following truth table, Bit Select 1 (Bit 2) and Bit Select 0 (Bit 3) identifies the bit cell within the first nibble of the first Address-Mark byte in which the first deviation from the normal preamble is expected. BYTRA is always referenced to bit cell 0.

BS 0	BS 1	Bit Cell
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4 (Preamble Select)
This bit is used only for bit sychronization—refer to CSR 1/Bit 3. With Bit 1 of CSR 2 set to 0 (Read Mode) and the Preamble Select bit set to 0, the preamble field is assumed to be all zeroes; with the Preamble Select it set to 1, the preamble field is assumed to be all ones. In either case, preamble validity is determined by the 8X300.

Bits 5,6 (E1 and E2)
Together, E1 and E2 select the encoding scheme used to write data on the disk—refer to truth table that follows.

E1	E2	Encoding Scheme
1	X	FM
0	0	MFM
0	1	M²FM

x = don't care

Bit 7 (1/2F)
This bit allows the data transfer rate to be changed without modification of the frequency-selective components in the data-separation logic; thus, differences in data transfer rates between standard-and-mini floppies can be accommodated via software—no component or other hardware changes. Assuming an 8 MHz crystal and with the 1/2F bit set to 1, the data transfer rate is 250K-bits per second in the single-density (FM) mode and 500K-bits per second in the double-density (MFM/M²FM) mode. When set to 0, the transfer rates are halved—125K-bits and 250K-bits, respectively. When using frequencies other than 8 MHz, the data transfer rate is determined as follows:

Bit 7 ($1/2F$)	Single-Density (FM)	Double-Density (MFM/M²FM)
0	$\frac{\text{xtal freq}}{64}$	$\frac{\text{xtal freq}}{32}$
1	$\frac{\text{xtal freq}}{32}$	$\frac{\text{xtal freq}}{16}$

Command/Status Register #3 (CSR 3/Address 134_8)

This register contains seven bits (Bit 0 through Bit 6) which determines the state of the disk-command outputs; writing to Bit 7 has no effect and reading Bit 7 always returns a zero. When a logical "1" is specified by the 8X300 program for a given disk-command line, a high will appear at the output of the 8X330 for that particular command line. Each bit and the output pin it controls are summarized below.

Bit (CSR 3)	Control Function	Pkg Pin No.
0	DC1 Output	12
1	DC2 Output	11
2	DC3 Output	10
3	DC4 Output	9
4	DC5 Output	8
5	DC6 Output	7
6	DC7 Output	6

Command/Status Register #4 (CSR 4/Address 135_8)

This register contains four bits (Bit 0 through Bit 3) which reflect the state of the disk-status inputs to the 8X330; reading all other bits (4 through 7) always returns a zero. These read-only bits and the reflected status they represent are as follows; the information specified by notation for Bit 7/CSR 1 is applicable to these input lines.

Bit (CSR 4)	Control Function	Pkg Pin No.
0	DS2 Input	16
1	DS3 Input	15
2	DS4 Input	14
3	DS5 Input	13

Sector Length Register—Address 136_8

This register contains the load value for the lower eight (LSBs) bits of the Byte Counter Data is transferred from the Sector Length Register to the Byte Counter under control of Load Counter Bit in CSR 1. When the contents of this register are transferred to another location via a read or write commands, the original holding of data is not lost; thus, if the same data is to be used more than once, a repetitive read or write can be implemented without reloading the register.

Data Register—Address 137_8

Together with the Data Shift Register, the Data Register is used for bidirectional transfer of data between the 8X330 and the I/O bus. All transfers to-and-from this register are made in conjunction with Bit 6 (BYTRA—Byte Transfer Flag) of CSR 1. When the Data Register Control bit (CSR 1/Bit 2) is set to 0, the content of this register is interleaved with four bits of data and four bits of clock. When data is transferred from the Data Register to the Data Shift Register, the original content of the Data Register is not lost.

Phase Lock Loop (PLL) and Data Separation Logic

An expanded view of the phase-lock loop and the data-separation logic is shown in Figure 4. Basically, the PLL consists of two counters, a phase detector, and a feedback loop containing a low-pass filter (off-chip) that controls a phase-locked oscillator (CCO). In simplified form, the data-separation logic consists of data flip-flops (pulse synchronizer) and other circuits required to separate data and clock transitions. In the read mode, the output of the phase-locked oscillator (CCO) is applied to the clock inputs of counter #1, counter #2, and the pulse synchronization circuits. Essentially, the frequencies of the two counters are identical (phase relationships may or may not be identical); to maintain proper frequencies and to continuously correct for any phase deviations, the following actions occur.

Preset values which represent, respectively, nominal midpoints of the clock and data windows are present at counter #2 and, when an output appears at the pulse synchronizer, these preset values are entered. The count sequence for both counters is from "0 to F"; hence, the phase difference between Carry 1 (counter #1) and Carry 2 (counter #2) actually corresponds to any phase deviation between the CCO and the synchronized data from the disk. The phase detector measures the phase difference between the two carry inputs and produces a series of quantized pulses whose widths are proportional to the phase error at the end of each counting cycle. After integration by the low-pass filter, a current proportional to the phase error is applied to the current-controlled oscillator. Accordingly, the CCO is driven in a direction (pump-up or pump-down) to correct any phase difference between the synchronized disk data and the feedback-controlled clock. Phase detector characteristics for both single-and-double density formats are shown in Figures 5 and 6.

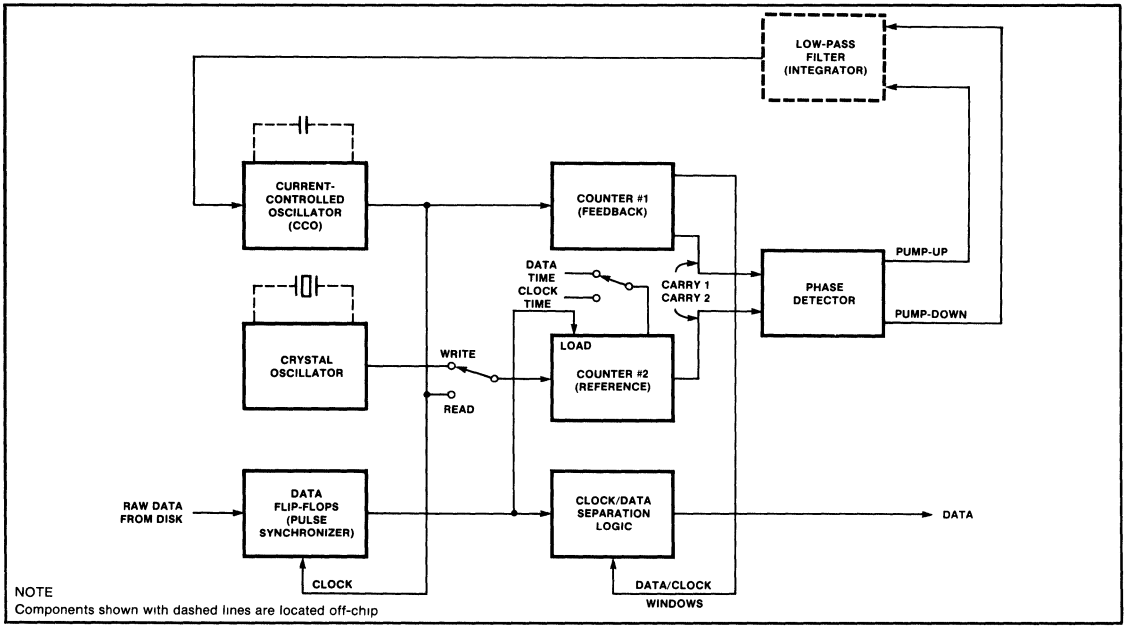


Figure 4. Simplified Block of Phase-Lock Loop

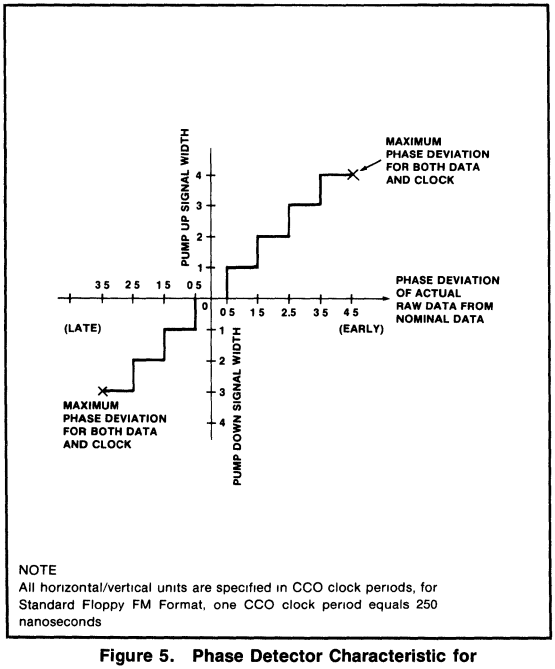


Figure 5. Phase Detector Characteristic for Single-Density (FM) Format

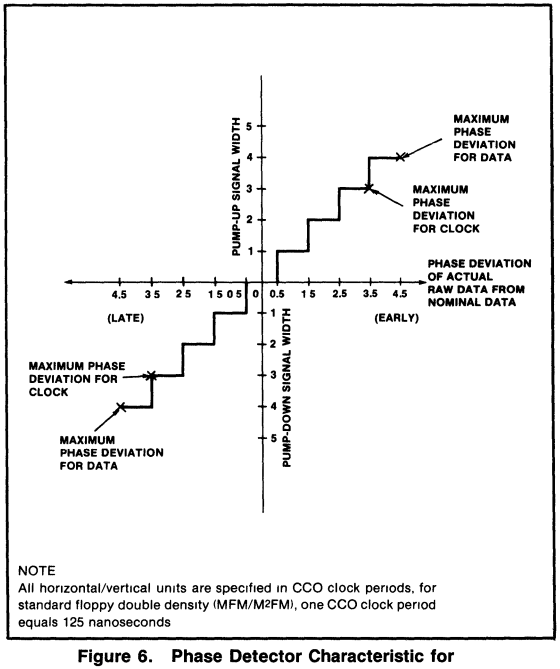


Figure 6. Phase Detector Characteristic for Double-Density (MFM/M²FM) Format

Data Processing and Error-Check Functions

These functions of the 8X330 are summarized in Figures 7 and 8. The read/write operations are software-controlled by previously-described bits of command/status registers CSR1 and CSR2. For the sake of simplicity, control lines and much of the control logic associated with the data processing and error-check functions are omitted in the read/write diagrams.

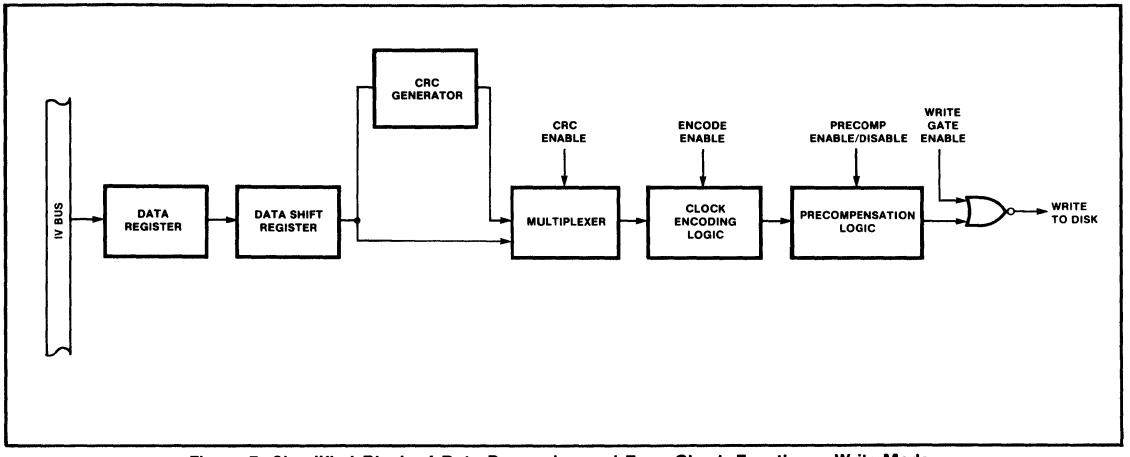


Figure 7. Simplified Block of Data Processing and Error Check Functions—Write Mode

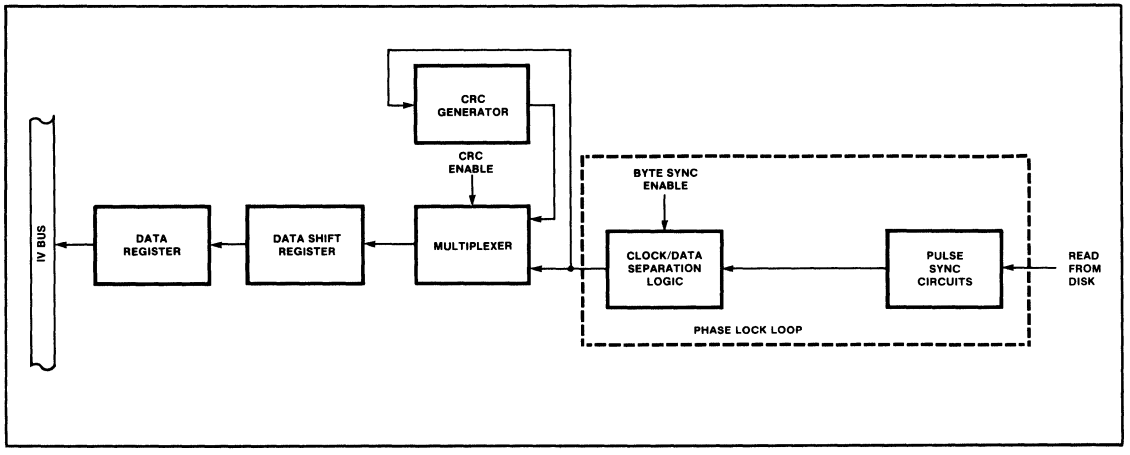


Figure 8. Simplified Block of Data Processing and Error Check Functions—Read Mode

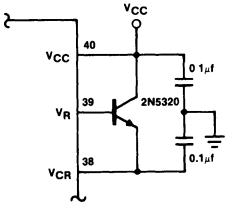
DC CHARACTERISTICS V_{CC} = 5V (±5%), T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	LIMITS			UNITS	COMMENTS
			Min	Typ	Max		
V_{IH}	High level input voltage		2.0		V_{CC}	V	For all inputs except X1, X2, C1, C2, CCO, and V_{CR}
V_{IL}	Low level input voltage		−1.0		0.8	V	
V_{CC}	Supply voltage		4.75	5.0	5.25	V	5V (±5%)
V_{CR}	Regulator voltage	V_{CC} = 5V		3.1		V	From series-pass transistor
V_{CL}	Input clamp voltage	V_{CC} = Min I_{IN} = −5mA	−1.0			V	Inputs X1, X2, C1, C2, and CC0 do not have internal clamp diodes.
V_{OH}	High level output voltage	V_{CC} = Min; I_{OH} = −0.4mA	2.7			V	DC1 through DC7 (Pins 6-12) & $\overline{DW}$ (Pin 4)
		V_{CC} = Min; I_{OH} = −3mA	2.4			V	$\overline{IV0}$-$\overline{IV7}$ (Pins 25-32)
V_{OL}	Low level output voltage	V_{CC} = Min; I_{OL} = 8mA			0.5	V	DC1 through DC7 (Pins 6-12); $\overline{PUP}$, $\overline{PDN}$ (Pins 33, 34); $\overline{DW}$ (Pin 4)
		V_{CC} = Min; I_{OL} = 16mA			0.55	V	$\overline{IV0}$-$\overline{IV7}$ (Pins 25-32)
		V_{CC} = Min; I_{OL} = 40mA			0.55	V	$\overline{WG}$ (Pin 19)
I_{CEX}	Open-collector leakage current with output set to 1.	V_{CC} = Min; V_{OUT} = V_{CC}			100	μA	$\overline{WG}$ (Pin 19); $\overline{PUP}$ (Pin 34); $\overline{PDN}$ (Pin 33)
I_{IH}	High level input current	V_{CC} = Max; V_{IN} = 2.7V			20	μA	DS1-DS5 (Pins 13-17); $\overline{PF}$ (Pin 18); $\overline{DR}$ (Pin 5)
					40	μA	$\overline{ME}$ (Pin 21); MCLK (Pin 22); SC (Pin 23); WC (Pin 24)
		V_{CC} = Max; V_{IN} = 5.25V; CCO (Pin 35) input current = 0mA			4	mA	With C1 (Pin 36) under test, C2 (Pin 37) is open and, vice-versa.
		V_{CC} = Max; V_{IN} = 5.25V CCO (Pin 35) input current = 1mA			2	mA	
		V_{CC} = Max; V_{IN} = 0.6V			4	mA	With X2 (Pin 2) under test, X1 (Pin 3) is open and, vice-versa.
		V_{CC} = Max; V_{IN} = 4.5V			50	μA	$\overline{IV0}$ - $\overline{IV7}$ (pins 25-32)
V_{CCO}	Input voltage for current-controlled oscillator	V_{CC} = 5V; T_A = 25°C CCO input current (Pin 35) = 300 μA		750		mV	

DC CHARACTERISTICS (Cont'd) V_{CC} = 5V (±5%), T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	LIMITS			UNITS	COMMENTS
			Min	Typ	Max		
I_{IL}	Low level input current	V_{CC} = Max; V_{IN} = 0.4V			−400	µA	DS1-DS5 (Pins 13-17); $\overline{PF}$ (Pin 18); $\overline{DR}$ (Pin 5)
					−800	µA	$\overline{ME}$ (Pin 21); MCLK (pin 22); SC (Pin 23); WC (Pin 24)
					−4	mA	X1 (Pin 2), X2 (Pin 3), with X1 under test, X2 is open and, vice-versa.
		V_{CC} = Max V_{IN} = 0.5V			−550	µA	$\overline{IV0}$-$\overline{IV7}$ (Pins 25-32)
I_{OS}	Output short-circuit current	V_{CC} = Max; Output = "1"; V_{OUT} = "0".	−15		−100	mA	DC1-DC7 (Pins 6-12) & $\overline{DW}$ (Pin 4)
		(NOTE At any time, no more than one output should be connected to ground)	−30		−140	mA	$\overline{IV0}$-$\overline{IV7}$ (Pins 25-32)
I_{CC}	(Pin 40)	V_{CC} = Max			200	mA	
I_{CR}		V_{CC} = Max			250	mA	
I_{REG}	(Pin 39)	V_{CC} = 5V; V_{CR} = 0V & V_R = 2V	−16		− 27	mA	

NOTES
1 Operating temperature ranges are guaranteed after thermal equilibrium has been reached
2 All voltages measured with respect to ground terminal
3 Unless otherwise specified, each test requires that V_{CR} be supplied through a series-pass transistor as shown in the accompanying drawing



AC CHARACTERISTICS V_{CC} = 5V (±5%), T_A = 0°C to 70°C

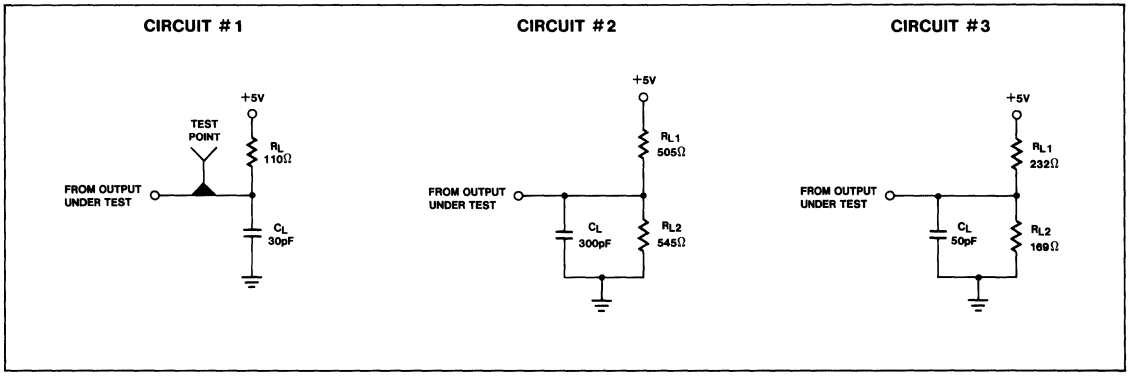
MNEMONIC	REFERENCE	INPUT	OUTPUT	Min	Typ	Max	COMMENTS
t_{PD}		$\overline{PF}$ ↓	$\overline{WG}$ ↑			60ns	Refer to Note 3 and Test Loading Circuit #1.
t_{PD}		MCLK ↑	$\overline{WG}$ ↑			100ns	
t_{PD}		MCLK ↑	$\overline{WG}$ ↓			100ns	
t_{PD}		MCLK ↑	DC1-7 ↑			70ns	Refer to Note 3 and Test Loading Circuit #2.
t_{PD}		MCLK ↑	DC1-7 ↓			70ns	
t_{pw}		$\overline{PF}$ ↓↑		50ns			
t_{pw}		$\overline{DR}$ ↓↑		50ns			
t_{pw}			$\overline{DW}$ ↓↑				Note 1
t_{SETUP}	SC ↓	Input on DS1-5		55ns			Note 2
t_{SETUP}	WC ↓	Input on DS1-5		55ns			Note 2
t_{SETUP}	$\overline{ME}$ ↓	Input on DS1-5		55ns			Note 2
t_{HOLD}	SC ↓	Input on DS1-5		0ns			Note 2
t_{HOLD}	WC ↓	Input on DS1-5		0ns			Note 2
t_{HOLD}	$\overline{ME}$ ↓	Input on DS1-5		0ns			Note 2
t_{OE}—$\overline{ME}$, SC & WC		$\overline{ME}$ ↓ SC ↓ WC ↓	I/O bus			25ns	Refer to Test Loading Circuit #3.
t_{OD}—$\overline{ME}$, SC & WC		$\overline{ME}$ ↑ SC ↑ WC ↑	I/O bus (three-state)			30ns	
t_w (MCLK pulse width)		MCLK ↓↑		45ns			
t_{SD} (data setup time)	$\overline{MCLK}$ ↓	I/O bus		50ns			
t_{SD} ($\overline{ME}$ setup time)	$\overline{MCLK}$ ↓	$\overline{ME}$		45ns			
t_{SD} (SC setup time)	$\overline{MCLK}$ ↓	SC		45ns			
t_{SD} (WC setup time)	$\overline{MCLK}$ ↓	WC		45ns			
t_{HD} (data hold time)	$\overline{MCLK}$ ↓	I/O bus		0ns			

AC CHARACTERISTICS (Cont'd) V_{CC} = 5V (±5%), T_A = 0°C to 70°C

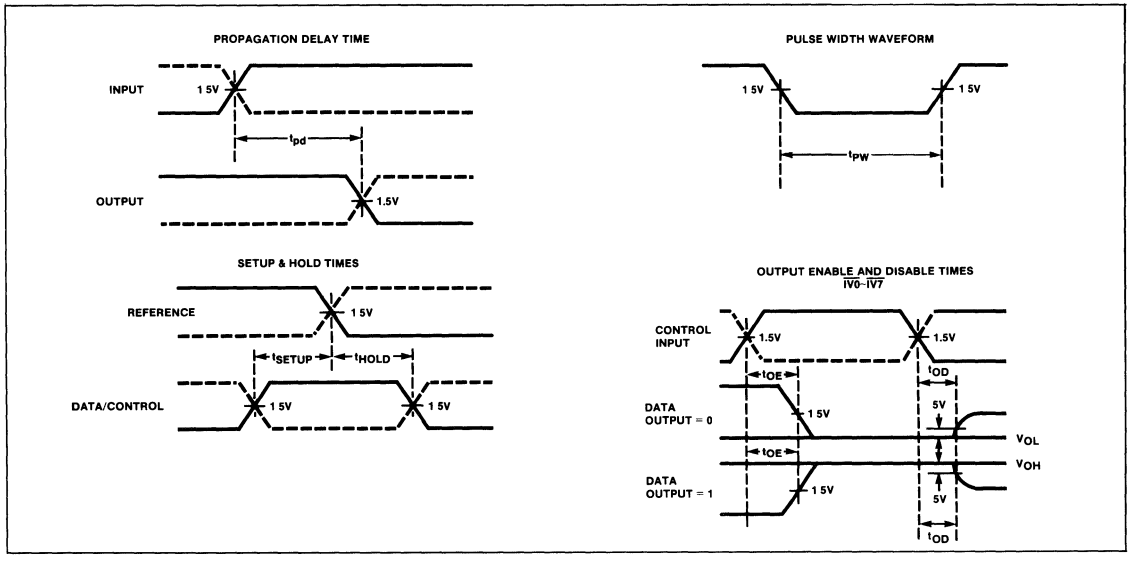
MNEMONIC	REFERENCE	INPUT	OUTPUT	Min	Typ	Max	COMMENTS
t_{HD} ($\overline{ME}$ hold time)	MCLK	$\overline{ME}$		0ns			
t_{HD} (SC hold time)	MCLK	SC		0ns			
t_{HD} (WC hold time)	MCLK	WC		0ns			

NOTES
1 Write pulse width = $2/F_{XTAL}$, that is, for 8MHz crystal, t_{pw} = 250nsec (typical)
2 Changes on DS1-5 are not stored in read mode ($\overline{ME}$ = 0, SC = 0, and WC = 0)
3 During the period when MCLK is high, measurement is made with $\overline{ME}$ = Low, SC = Low, and WC = High

TEST LOADING CIRCUIT



TIMING DIAGRAM



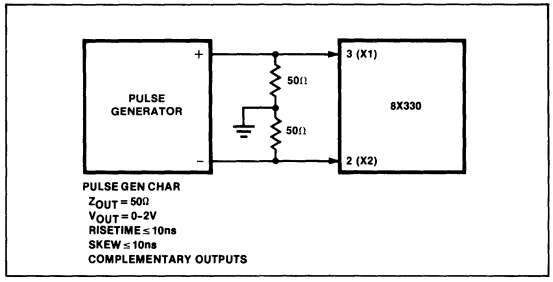
CLOCK REQUIREMENTS

Crystal Oscillator. The on-chip crystal oscillator circuit is designed for operation using an external series-resonant quartz crystal; alternately the crystal oscillator can be driven with complementary outputs of a pulse generator or interfaced to a master clock source via TTL logic—see accompanying circuits. When a crystal is used, the on-chip oscillator operates at the resonant frequency (f.) of the crystal; the crystal connects to the 8X330 via pins 3 (X1) and 2 (X2). The lead lengths of the crystal should be approximately equal and as short as possible; also, avoid close proximity to all potential noise sources. The crystal should be hermetically sealed (HC type can) and have the following electrical characteristics:

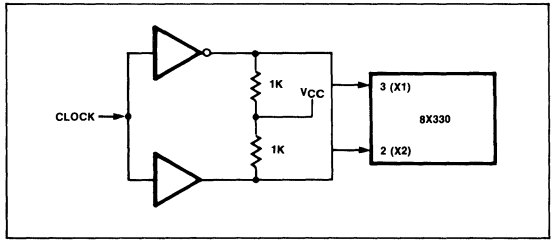
Type: Fundamental mode, series resonant
Impedance at Fundamental: 35-ohms maximum
Impedance at Harmonics and Spurs: 50-ohms minimum

When the crystal oscillator is externally-driven, typical waveforms are as follows:

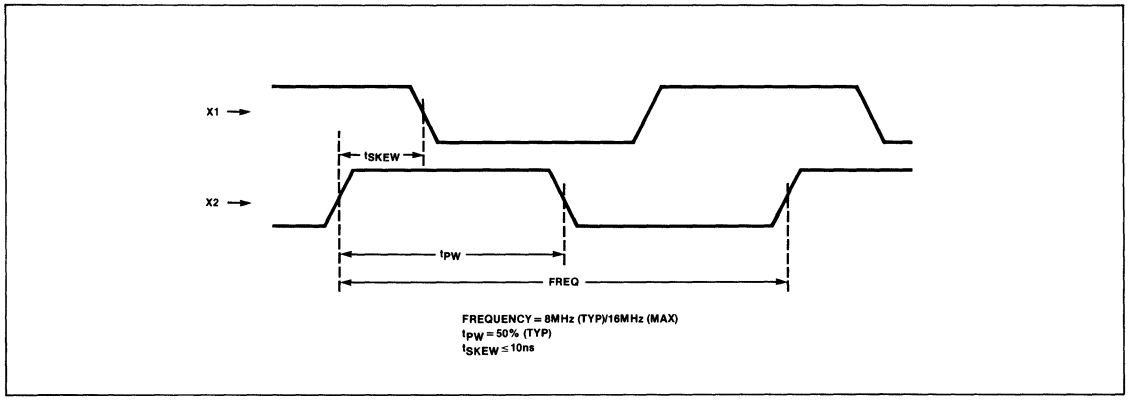
CLOCKING XTAL OSC WITH PULSE GEN



CLOCKING XTAL OSC WITH OPEN-COLLECTOR TTL

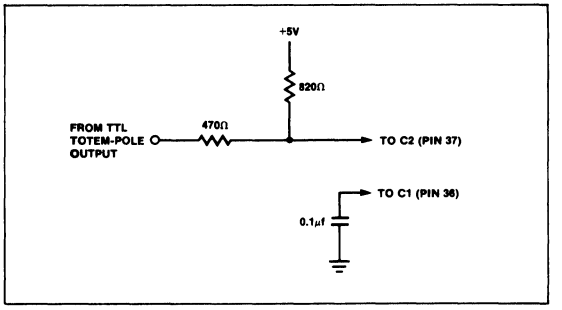


TYPICAL WAVE FORM

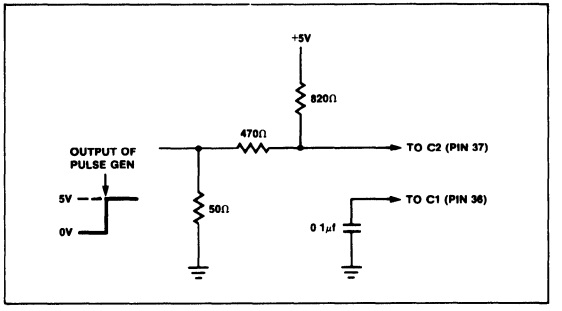


Current-Controlled Oscillator (CCO).
A non-polarized ceramic or mica capacitor is recommended for the current-controlled oscillator. The capacitor connects to the 8X330 via pins 37 (C2) and 36 (C1); lead lengths of the capacitor should be approximately the same and as short as possible. When the input current to the CCO is near zero (maximum frequency), the capacitor value should be chosen so that the high-limit rest frequency of the oscillator does not exceed 24 MHz. If the rest frequency is higher than 24 MHz, synchronization of the CCO with the crystal oscillator just prior to the read operation, may be impeded. The curves in Figure 9 (current-versus-frequency) and Figure 8 (capacitance-versus-frequency) show how these design parameters affect operation of the CCO over a temperature range of 0° C to 70° C. A suitable test circuit for verification/validation of the current-controlled oscillator is also shown in Figure 10. Like the crystal oscillator, the CCO can be driven with the TTL output of a pulse generator or interfaced to a master clock via TTL logic—see accompanying diagrams.

CLOCKING WITH OPEN-COLLECTOR TTL



CLOCKING WITH PULSE GENERATOR



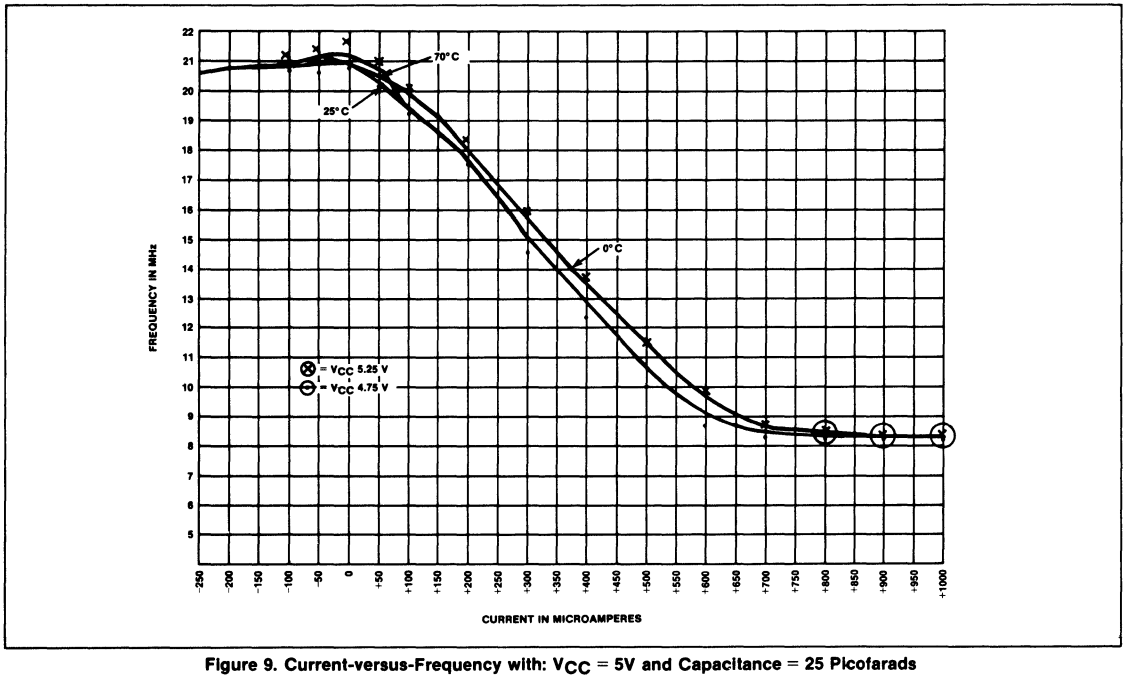


Figure 9. Current-versus-Frequency with: V_{CC} = 5V and Capacitance = 25 Picofarads

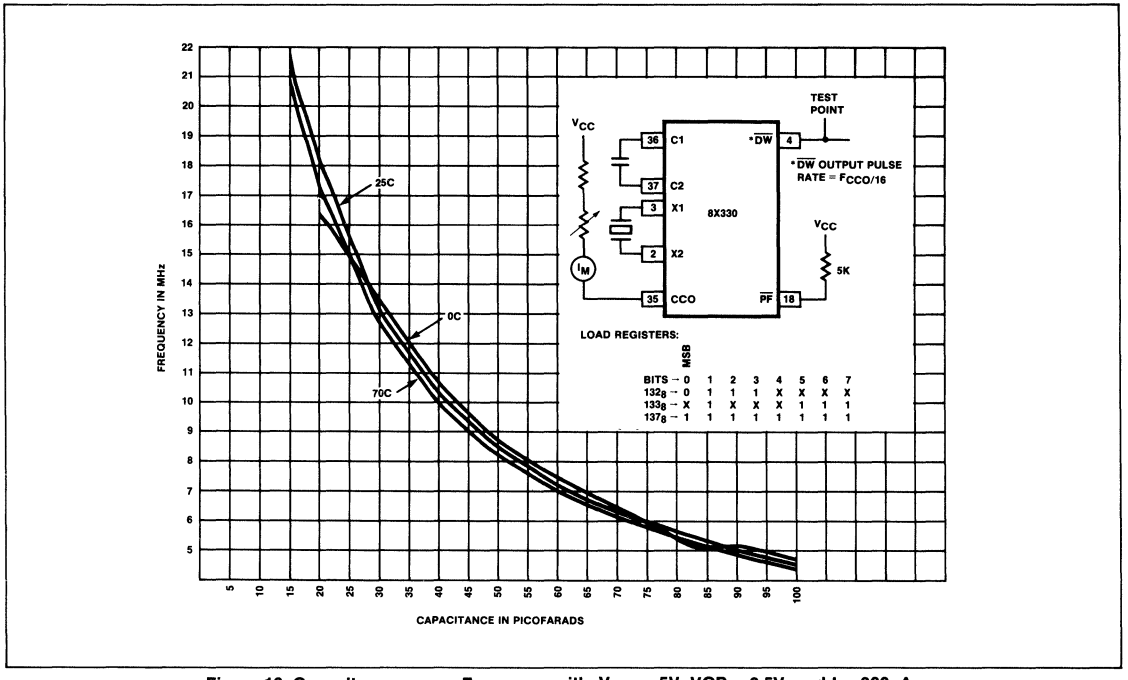


Figure 10. Capacitance-versus-Frequency with: V_{CC} = 5V, VCR = 2.5V, and I = 300μA

VOLTAGE REGULATOR

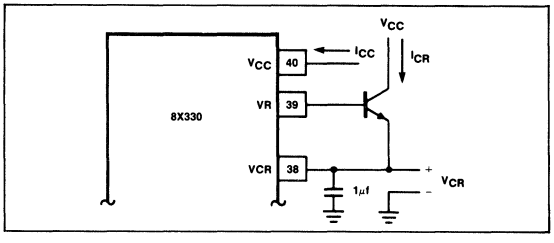
All internal logic of the 8X330 is powered by an on-chip voltage regulator that requires an external series-pass transistor. Electrical specifications for the off-chip power transistor and a typical hook-up are shown in accompanying diagrams. To minimize lead inductance, the transistor should be as close as possible to the 8X330 package and the emitter should be ac-grounded via a 0.1-microfarad capacitor.

ELECTRICAL SPECIFICATIONS

*PARAMETER	CONDITIONS	LIMITS
h_{fe}	V_{CE} = 2V	>50
V_{BEON}	V_{CE} = 5V/I_C = 500mA	<1V
V_{CESAT}	I_C = 500 mA/I_B = 50 mA	<0.5V
BV_{CEO}		>8V
f_t		>30 MHz

*Medium power NPN silicon (0°<T_A<70°C) recommended parts 2N5320, 2N5337

TYPICAL HOOK-UP



MEMORY ADDRESS DIRECTOR 8X360

FEATURES

- **Address control for working storage**
- **16-bit addressing capability**
- **Byte and word addressing support**
- **Automatic increment and decrement**
- **11 Address and word-count registers**
- **Reduces number of 8X305 instructions required**

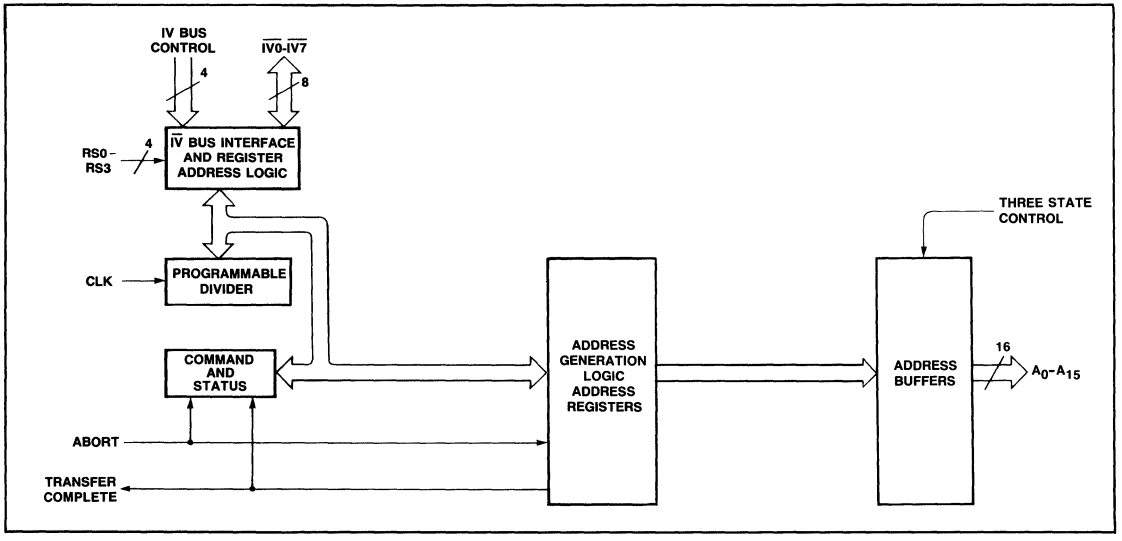
PRODUCT DESCRIPTION

The 8X360 Memory Address Director (MAD) is a high-performance member of the 8X300 Family that generates sequential memory addresses to facilitate the transfer of data to and from memory. The MAD provides a highly-efficient and cost-effective solution for DMA and other applications requiring large working-storage memories and high-speed data transfers. Once initialized with such information as starting address, ending address, byte count, address increment, address decrement, etc., the 8X360 performs all bookkeeping chores automatically and all address-management software is off-loaded from the processor. The 8X360 can be addressed by conventional means or by extended microcode; system status is available to the user via I/O pins.

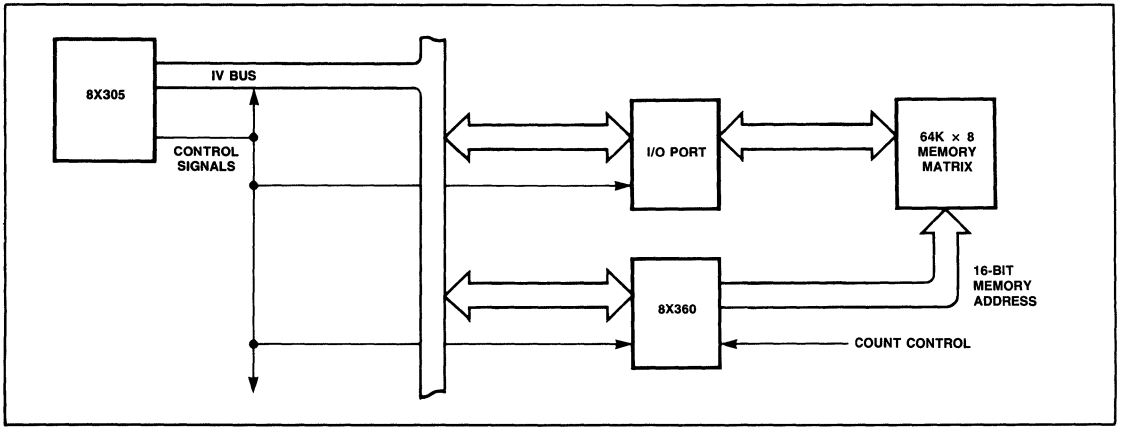
ORDERING INFORMATION

N8X360N, N8X360I, S8X360I

BLOCK DIAGRAM OF 8X360



8X360 APPLICATIONS



2048-BIT BIPOLAR RAM (256 × 8) 8X350 (T.S.)

FEATURES

- **On-chip address latches**
- **3-state outputs**
- **Schottky clamped TTL**
- **Internal control logic for 8X300 system**
- **Directly interfaces with the 8X300 bipolar microprocessor with no external logic**
- **May be used on left or right bank**

APPLICATIONS

- **8X300 or 8X305 working storage**

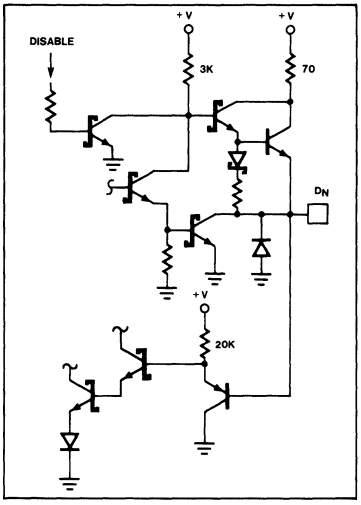
DESCRIPTION

The 8X350 bipolar RAM is designed principally as a working storage element in an 8X300 based system. Internal circuitry is provided for direct use in 8X300 applications. When used with the 8X300, the RAM address and data buses are tied together and connected to the IV bus of the system.

The data inputs and outputs share a common I/O bus with 3-state outputs.

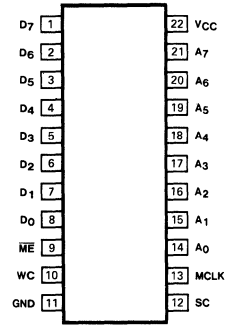
The 8X350 is available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N8X350-F, and for the miltiary temperature range (−55°C to +125°C) specify S8X350-F.

TYPICAL I/O STRUCTURE



PIN CONFIGURATION

F PACKAGE



TOP VIEW

F = Cerdip

ORDER NUMBERS

8X350N, 8X350F
S8X350F/883B

ABSOLUTE MAXIMUM RATINGS

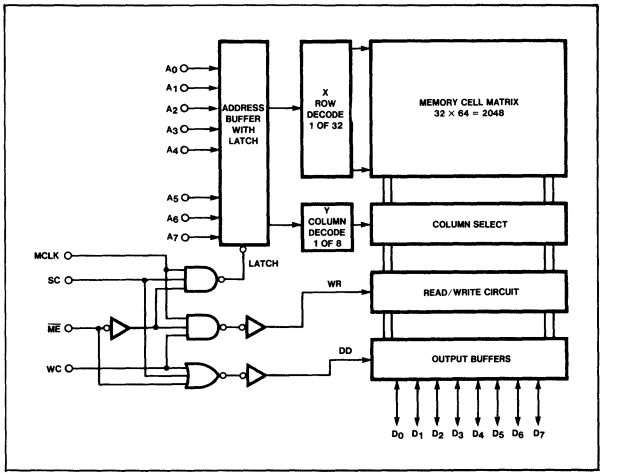
PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High	+5.5	
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	Commercial	0 to +75	
	Military	−55 to +125	
T_{STG}	Storage	−65 to +150	

TRUTH TABLE

Note X = Don't care

MODE	$\overline{ME}$	SC	WC	MCLK	BUSSED DATA/ADDRESS LINES
Hold address Disable data out	1	X	X	X	High Z data out
Input new address	0	1	0	1	Address High Z
Hold address Disable data out	0	1	0	0	High Z data out
Hold address Write data	0	0	1	1	Data in
Hold address Disable data out	0	0	1	0	High Z data out
Hold address Read data	0	0	0	X	Data out
Undefined state[12]	0	1	1	1	—
Hold address[12] Disable data out	0	1	1	0	High Z data out

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS[2]

N8X350: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S8X350: $-55°C \leq T_A \leq +125°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	N8X350			S8X350			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			.85			.80	
V_{IH}	High[1]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = −12mA			−1.2			−1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,4]	I_{OL} = 9.6mA			0.5			.5	
V_{OH}	High[1,5]	I_{OH} = −2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			−100			−150	
I_{IH}	High	V_{IN} = 5.5V			25			50	
	Output current								μA
$I_{O(OFF)}$	High Z state	$\overline{ME}$ = High, V_{OUT} = 5.5 V			40			60	μA
		$\overline{ME}$ = High, V_{OUT} = 0.5 V			−100			−100	
I_{OS}	Short circuit[3,6]	SC = WC, $\overline{ME}$ = Low, V_{OUT} = 0V, Stored High	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max			185			200	mA
	Capacitance	$\overline{ME}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS[2,9]

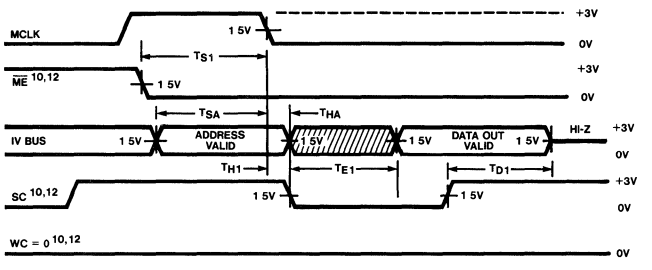
N8X350: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$ $R_1 = 470Ω$, $R_2 = 1kΩ$, $C_L = 30pF$
S8X350: $-55°C \leq T_A \leq +125°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TO	FROM	N8X350			S8X350			UNIT
				Min	Typ	Max	Min	Typ	Max	
	Enable time									ns
T_{E1}	Output	Data out	SC−			35			40	
T_{E2}	Output	Data out	$\overline{ME}$−			35			40	
	Disable time									ns
T_{D1}	Output	Data out	SC+			35			40	
T_{D2}	Output	Data out	$\overline{ME}$+			35			40	
	Pulse width									ns
T_W	Master clock[8]			40			50			
	Setup and hold time									ns
T_{SA}	Setup time	MCLK−	Address	30			40			
T_{HA}	Hold time	Address	MCLK−	5			10			
T_{SD}	Setup time	MCLK−	Data in	35			45			
T_{HD}	Hold time	Data in	MCLK−	5			10			
T_{S3}	Setup time	MCLK−	$\overline{ME}$−	40			50			
T_{H3}	Hold time	$\overline{ME}$+	MCLK−	5			5			
T_{S1}	Setup time	MCLK−	$\overline{ME}$−	30			40			
T_{H2}	Hold time	$\overline{ME}$−	MCLK−	5			5			
T_{S2}	Setup time	$\overline{ME}$−	SC−,WC−	0			5			
T_{H1}	Hold time	SC−	MCLK−	5			5			
T_{H4}	Hold time	WC−	MCLK−	5			5			

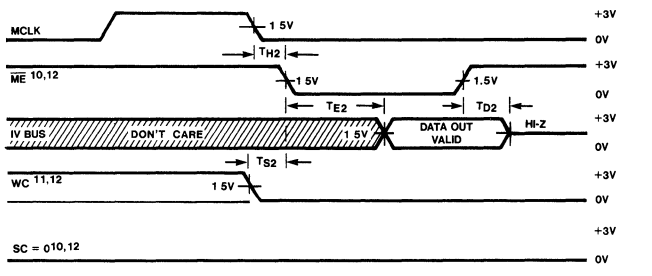
Notes on following page

TIMING DIAGRAMS

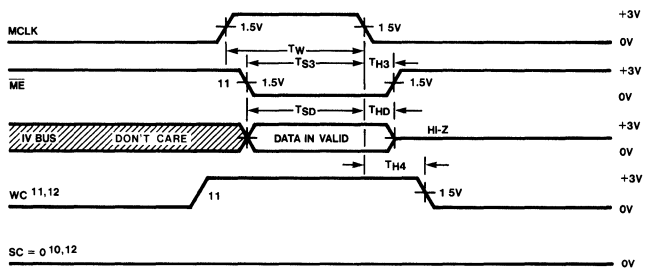
TRANSPARENT ADDRESS READ CYCLE



LATCHED ADDRESS READ CYCLE



LATCHED ADDRESS WRITE CYCLE



NOTES

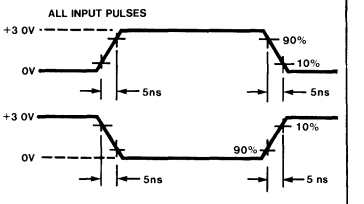
1. All voltage values are with respect to network ground terminal
2. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up
   Typical thermal resistance values of the package at maximum temperature are
   Θ_{JA} junction to ambient at 400fpm air flow - 50°C/watt
   Θ_{JA} junction to ambient - still air - 90°C/watt
   Θ_{JA} junction to case - 20°C/watt
3. Test each pin one at a time
4. Measured with a logic low stored Output sink current is supplied through a resistor to V_{CC}
5. Measured with a logic high stored
6. Duration of the short circuit should not exceed 1 second
7. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4 5V and the output open
8. Minimum required to guarantee a Write into the slowest bit
9. Applied to the 8X300 based system with the data and address pins tied to the IV Bus
10. SC + $\overline{ME}$ = 1 to avoid bus conflict
11. WC + $\overline{ME}$ = 1 to avoid bus conflict
12. The SC and WC outputs from the 8X300 are never at 1 simultaneously

TIMING DEFINITIONS

T_{S1}	Required delay between beginning of Master Enable low and falling edge of Master Clock.
T_{SA}	Required delay between beginning of valid address and falling edge of Master Clock.
T_{HA}	Required delay between falling edge of Master Clock and end of valid Address.
T_{H1}	Required delay between falling edge of Master Clock and when Select Command becomes low.
T_{E1}	Delay between beginning of Select Command low and beginning of valid data output on the IV Bus.
T_{D1}	Delay between when select Command becomes high and end of valid data output on the IV Bus.
T_{H2}	Required delay between falling edge of Master Clock and when Master Enable becomes low.
T_{E2}	Delay between when Master Enable becomes low and beginning of valid data output on the IV Bus.
T_{D2}	Delay between when Master Enable becomes high and end of valid data output on the IV Bus.
T_{S2}	Required delay between when Select Command or Write Command becomes low and when Master Enable becomes low.
T_W	Minimum width of the Master Clock pulse.
T_{S3}	Required delay between when Master Enable becomes low and falling edge of Master Clock.
T_{H3}	Required delay between falling edge of Master Clock and when Master Enable becomes high.
T_{SD}	Required delay between beginning of valid data input on the IV Bus and falling edge of Master Clock.
T_{HD}	Required delay between falling edge of Master Clock and end of valid data input on the IV Bus.
T_{H4}	Required delay between falling edge of Master Clock and when Write Command becomes low.

VOLTAGE WAVEFORM

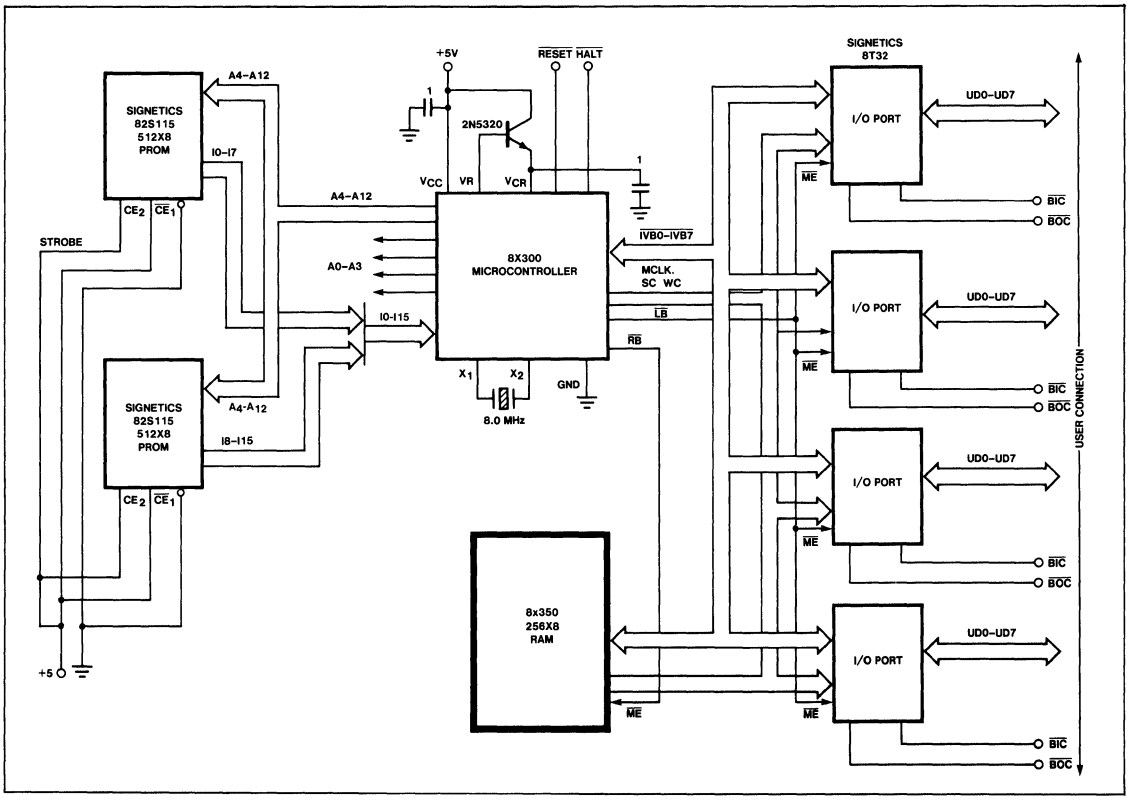
INPUT PULSES



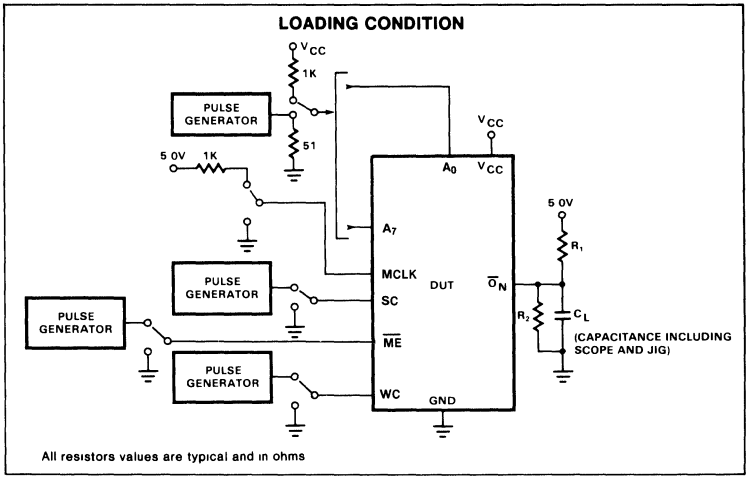
Measurements All circuit delays are measured at the +1 5V level of inputs and output

2048-BIT BIPOLAR RAM (256×8) 8X350 (T.S.)

TYPICAL 8X350 APPLICATION



TEST LOAD CIRCUIT



BIPOLAR RAM (32x8) 8X353

FEATURES

- **32 bytes of storage**
- **Dedicated port address**
- **Fast select feature for use with extended microcode**
- **On chip address decoding**
- **Separate address input pins**
- **Single 5 volt power supply**
- **0.3 inch, slim line package**

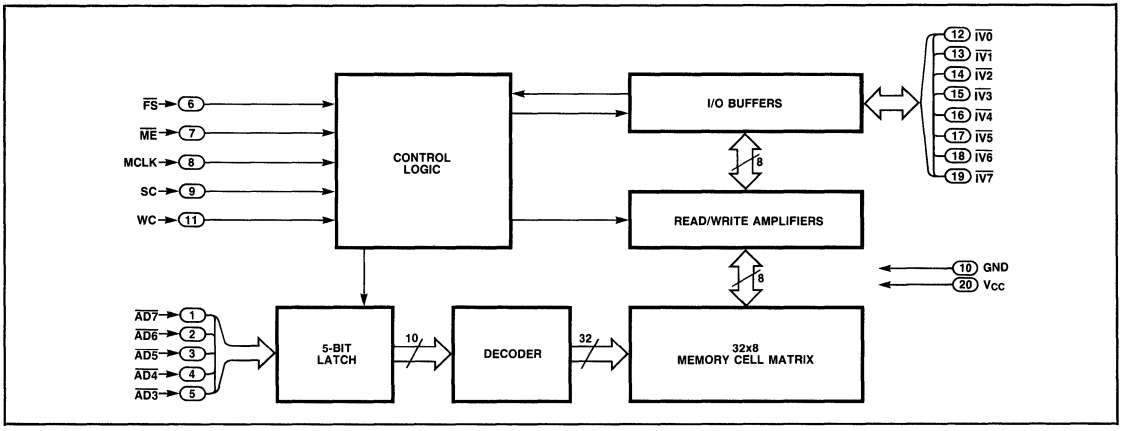
PRODUCT DESCRIPTION

The 8X353 is a 32-byte RAM designed principally as a working storage element in 8X305-based systems. The 8X353 is ideal for applications requiring a relatively small amount of data storage and maximum I/O flexibility. Since the 8X353 takes up 32 of 256 locations on a controller bank, this device allows single-cycle, bank to bank data transfer and other implementations in which the user does not wish to dedicate an entire I/O bank to data storage. Contributing to the versatility of the 8X353 is a fast select feature which allows the chip to be selected externally of the $\overline{IV}$ bus. A block diagram and summary of operation is shown below.

ORDERING INFORMATION

Contact Local Sales Representative

BLOCK DIAGRAM



SUMMARY OF OPERATION

INPUT						RESULTING OUTPUT				
$\overline{ME}$	SC	WC	MCLK	$\overline{FS}$	SELECT LATCH	$\overline{IV}$ BUS	ADDRESS BUS	DATA	ADDRESS LATCH	SELECT LATCH
H	X	X	X	H	X	Ignore	Ignore	Keep	Keep	Keep
H	X	X	H	L	X	Ignore	Input	Keep	Update	Keep
H	X	X	L	L	X	Ignore	Ignore	Keep	Keep	Keep
L	L	L	L	L	X	Output	Ignore	Keep	Keep	Keep
L	L	L	L	H	L	Ignore	Ignore	Keep	Keep	Keep
L	L	L	L	H	H	Output	Ignore	Keep	Keep	Keep
L	X	L	H	L	X	Ignore	Input	Keep	Update	Keep
L	L	H	L	X	X	Ignore	Ignore	Keep	Keep	Keep
L	L	H	H	L	X	Input	Ignore	Update	Keep	Keep
L	L	H	H	H	L	Ignore	Ignore	Keep	Keep	Keep
L	L	H	H	H	H	Input	Ignore	Update	Keep	Keep
L	H	L	L	X	X	Ignore	Ignore	Keep	Keep	Keep
L	H	L	H	X	X	Input (Address)	Input	Keep	Update	Update*
X	H	H	X	X	X	Not Defined				

Notes:
Depending on IV bus data X = don't care

LIFO STACK MEMORY (32x8) 8X355

FEATURES

- **32 bytes of storage**
- **Cascadable LIFO operation**
- **Dedicated port address**
- **Fast select feature for use with extended microcode**
- **Three state TTL outputs**
- **Single 5 volt power supply**
- **0.3 inch, slim line package**

PRODUCT DESCRIPTION

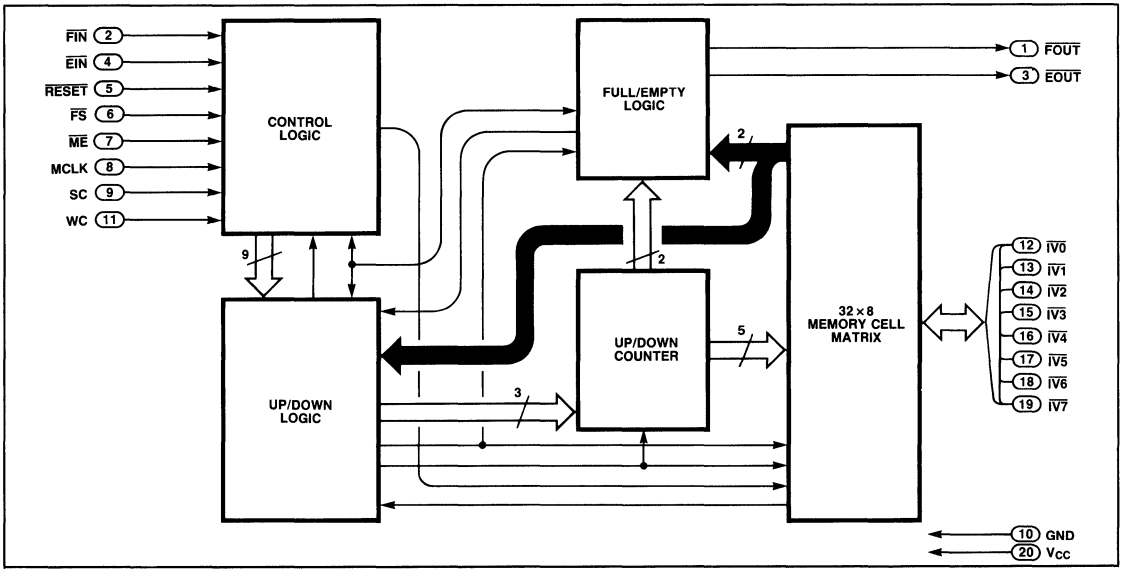
The 8X355 is a Last In/First Out stack memory designed to be compatible with 8X305-based systems. In addition to a 32-byte storage capacity, the 8X355 contains the necessary logic to allow cascaded operation.

The LIFO stack may be addressed using either conventional 8X305 techniques, i.e., $\overline{IV}$ bus select, or, in systems where extremely high performance is required, extended microcode can be implemented. A single enabling address is employed so that once enabled, a stack of 8X355s can accept an uninterrupted stream of data. By omitting the need for address select cycles prior to each data access, the LIFO stack delivers a much higher performance than conventional memories; this feature is particularly valuable for saving internal registers during interrupt servicing.

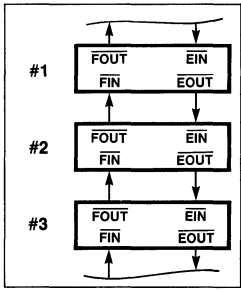
ORDERING INFORMATION

Contact Local Sales Representative

BLOCK DIAGRAM



TYPICAL CASCADED CONFIGURATION



INPUT				RESULTING OUTPUT				COMMENTS
$\overline{EIN}$	$\overline{FIN}$	$\overline{EOUT}$	$\overline{FOUT}$	$\overline{EOUT}$	$\overline{FOUT}$	PUSH	POP	
X	X	L	L	Not possible				Empty and full status
L	L	L	H	Update	H	Yes	No	Top of data stack at top of #1
L	L	H	L	H	Update	No	Yes	Top of data stack at top of #2
L	L	H	H	Update	Update	Yes	Yes	Top of data stack within #2
X	H	X	X	L	H	No	No	Top of data stack below #2
H	L	X	H	Not defined				Top of data stack moves from bottom to top
H	L	H	L	H	L	No	No	Top of data stack above #2

Notes.
Status signals and Push/Pop operations reference stack chip #2
X = don't care

NOTES

NOTES

NOTES

Section 4
Product Support

INDEX

4

SUPPORT FACILITIES

The 8X300 Family is strongly supported with Development Systems, Support Software, Applications, Training and Documentation Together, this support provides the user with a powerful set of tools to evaluate, design, debug, and implement a simple or complex system.

DEVELOPMENT SYSTEMS

EZ-PRO (Manufactured by American Automation)
- Universal Development System
- Relocating macroassembler
- Full speed in-circuit emulator/debugger
- Maximum memory support

8X305 ICEPACK (Manufactured by Sigen Corp.)
- Full speed in-circuit emulator/debugger
- RS-232 interface to CP/M or Intellec
- 4K word memory/8-bit extended microcode
- Low cost

Signetics 8X305 Prototyping System
- Single board module
- RS-232 interface
- Resident monitor
- 256 to 4096 words of Writable Control Storage
- Minimum cost

SOFTWARE

MCCAP CrossAssembler
- Full function macroassembler
  - Free format source code
  - Symbolic address assignment
  - Nested macro support
  - Cross-reference table
  - Supports extended microcode
- Multiple output formats
- Available in two versions
  - FORTRAN source code
  - Intellec/ISIS object code

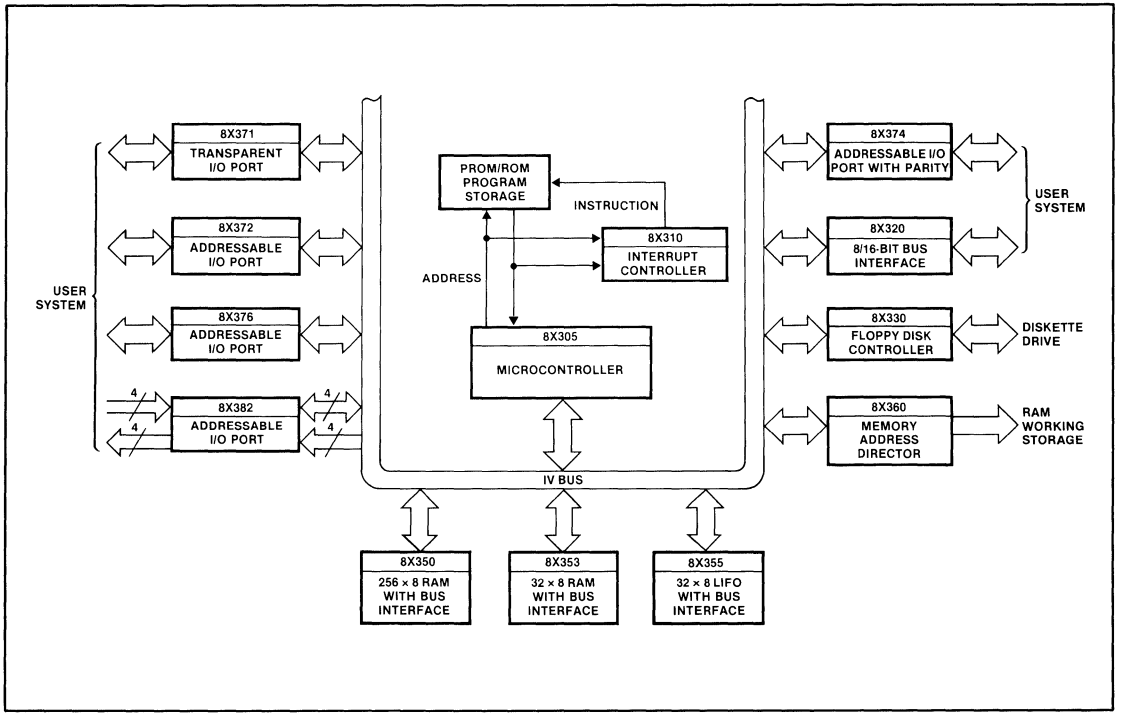
APPLICATIONS SUPPORT

Field applications engineers
Product applications engineers
Application notes
- Floppy disk controller
- ECC
- Hard disk controller
- Local network interfacing

TRAINING AND DOCUMENTATION

- Videocassette training course
- Designer's seminar
- 8X305 User's Manual
- 8X300 Family Product Capabilities Manual
- MCCAP Programming Manual
- Full complement of Data Sheets

4



8X305 Prototyping System

This document provides the information required to understand, set up and operate the 8X305 Prototyping System It is recommended that the user become thoroughly familiar with the 8X305 MicroController and the high speed peripherals that support the device For this purpose, the following documents are recommended

- 8X305 Users Manual — comprehensive functional detail, interface characteristics, hardware and software design data, and systems information for the 8X305 MicroController
- 8X300 Family Product Capabilities Manual — overview of the 8X300 Family of parts, including application information on the 8X305 MicroController and its support devices.
- MCCAP Manual — complete description of the powerful MicroController Cross-Assembler Program for the 8X300 and 8X305
- Data Sheets — electrical and functional characteristics for each member of the 8X300 Family and related parts.
  - — 8X305 MicroController
  - — 8X310 Interrupt Control Coprocessor
  - — 8X320 Bus Interface Register Array
  - — 8X330 Floppy Disk Formatter/Controller
  - — 8X338 Local Area Network Controller
  - — 8X350 256 Byte Bipolar RAM
  - — 8X360 Memory Address Director
  - — 8X371 Latched 8-bit Bidirectional I/O Port
  - — 8X372/8X376 Addressable 8-bit Bidirectional I/O Port
  - — 8X374 Addressable 8-bit Bidirectional I/O Port with Parity
  - — 8X382 Addressable 4-IN/4-OUT I/O Port
  - — 8X60 FIFO RAM Controller

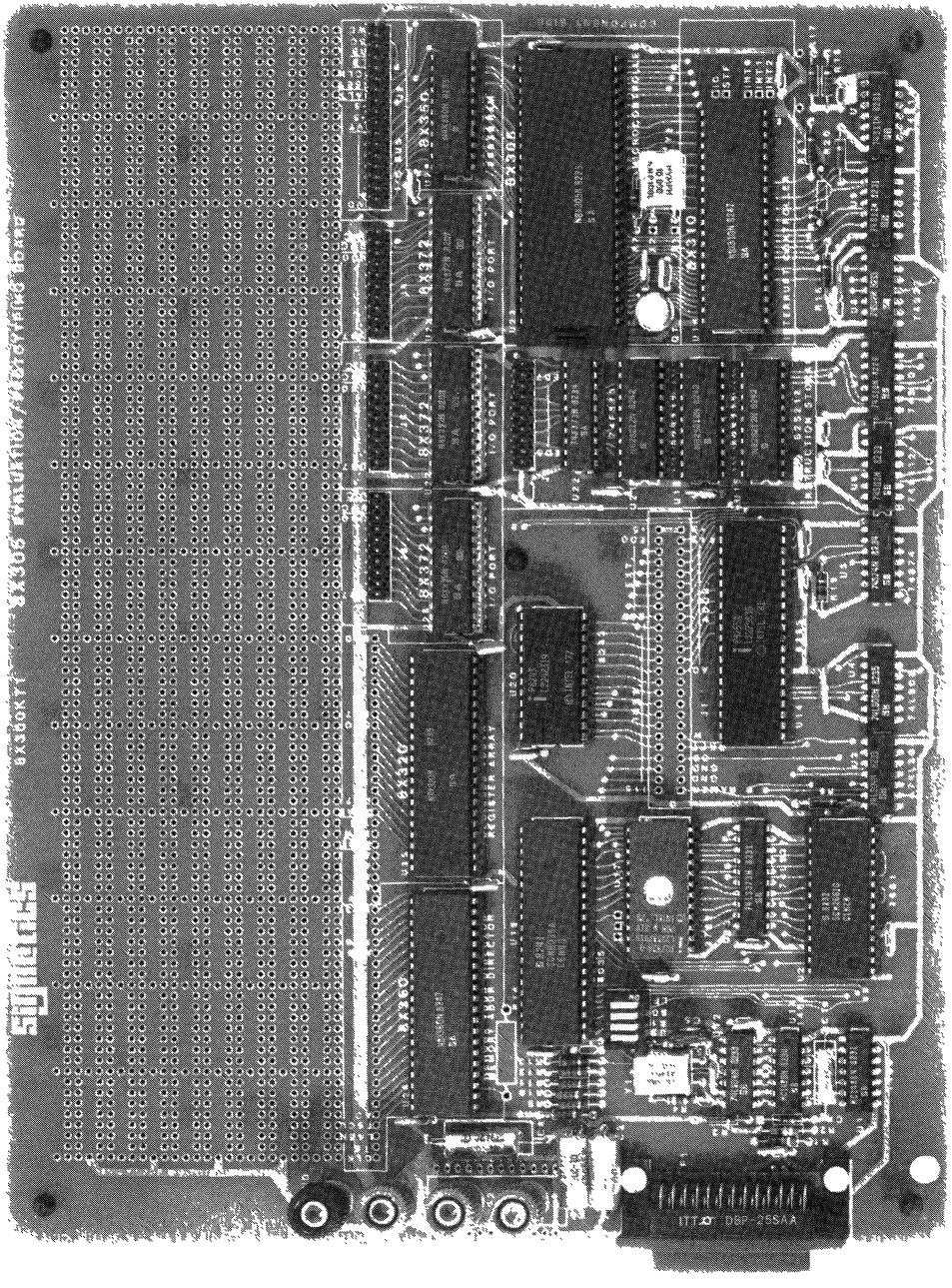


Figure 1-1. 8X305 Prototyping System

1.1 SYSTEM DESCRIPTION

The 8X305 Prototyping System is a powerful design support tool that aids the engineer in the evaluation, design, and prototyping of systems based on the Signetics 8X305 MicroController and its family of support devices. Its advanced features permit the development of both 8X305 firmware and application circuitry. The prototyping systems capabilities are adequate to serve as a complete development system for simple systems and provide a low-cost tool for evaluating portions of more complex designs.

1.2 ARCHITECTURAL OVERVIEW

As shown in Figure 1-1, the 8X305 Prototyping System consists of a single printed circuit board that includes an 8X305 MicroController and various 8X305 Family peripheral devices. The 8X305's microprogram resides in Writeable Control Storage (WCS). A Monitor Processor controls operation of the 8X305 by loading the WCS, activating the Run/ Step logic, and directly placing instructions onto the 8X305's Instruction bus. The Monitor Processor also controls the User Interface, which is through a standard RS-232 connector. The remainder of the board is occupied by power connections and a large wire-wrap area for prototyping of user-developed circuits. A complete discussion of the operation and interrelationship of these functions is contained in later chapters.

1.2.1 USER INTERFACE

The User Interface of the 8X305 Prototyping System is accomplished through a standard RS-232 connector. Data rates from 110 to 19,200 baud are switch selected by the user. The monitor program contained in the system controls all user communication, which is accomplished interactively through a straightforward and user-friendly syntax. While the operation of the system requires only a low-cost "dumb" terminal, it can be connected to a host computer to support more advanced developments. Commands are included to support up and down loading of programs in such applications.

1.2.2 MONITOR PROCESSOR AND RUN/STEP LOGIC

Operation of the system is controlled by the Monitor Processor, which is implemented using an 8035 Microprocessor. The Monitor Processor is responsible for the following functions:

- User interaction
- Loading Writeable Control Storage
- Loading and reading 8X305 registers and I/O devices
- Control of Run/Step logic

Programming for the Monitor Processor is supplied by Signetics and is contained in a PROM.

1.2.3 WRITEABLE CONTROL STORAGE

8X305 MicroController programs are executed from a Writeable Control Storage (WCS) that is contained on the board. The prototyping system is supplied with 256 words of instruction memory. An expansion module is available to support address space requirements of up to 4096 words. The WCS is sufficiently fast to permit full speed operation of the 8X305.

Writeable Control Storage words are 25 bits wide to support advanced microprogramming requirements. Sixteen of these bits contain actual 8X305 instructions. Eight of the remaining bits are used to support "Extended Microcode" designs as described in the 8X305 Users Manual. The 25th bit, transparent to the user, is set by the Monitor Processor to control breakpoints.

Since the three-bus architecture of the 8X305 does not permit the MicroController to modify its own program memory, the WCS is loaded by the Monitor Processor.

1.2.4 8X305 MICROCONTROLLER AND PERIPHERALS

An 8X305 MicroController and various 8X300 Family peripheral devices are included in the prototyping system.

The Instruction and Program Address busses of the 8X305 are connected to Writeable Control Storage (WCS) as well as an 8X310 Interrupt Control Coprocessor (ICC). The interrupt and status pins of the 8X310 are available to the user for use in prototyping real-time or other interrupt driven systems.

The 8X305's IV bus is connected to the following 8X300 Family peripheral devices:

(1) 8X320 Bus Interface Register Array
(1) 8X350 256 Byte Bipolar RAM
(1) 8X360 Memory Address Director
(3) 8X372 Addressable 8-bit Bidirectional I/O Ports

IV bus data and control signal connections are also available to the user to permit attachment of other devices or user developed logic. User interface connections to the 8X320, 8X360, and 8X372's are available adjacent to the wire-wrap area to permit prototyping of various 8X305 based designs.

4

2.1 POWER CONNECTIONS

CAUTION

Power connections must be properly made; otherwise, component damage will result.

Power connections to the Prototyping System are made through four binding posts located on the left hand edge of the board These are labeled GROUND, +5, —12, and +12 Without options or user circuitry in the wire-wrap area, the current drawn from each power source is as follows·

+5 VDC — less than 2 5 amperes
+12 VDC — less than 20 milliamperes
—12 VDC — less than 20 milliamperes

Additional current must be supplied for any options or user circuitry added to the board. At the user's option, a DC-to-DC converter (converts +5 VDC to ±12 VDC) can be installed in the space allotted to the —12 VDC and +12 VDC binding posts. Refer to the parts list in Appendix B for the manufacturer and part number of the recommended device

2.2 RS-232 INTERFACE

An RS-232 connector is provided in the lower left-hand corner of the system for interconnection to the user's CRT terminal, and is connected as shown in Table 2-1

Table 2-1 RS-232 CONNECTOR

Pin No.	Signal	Description
1	GND	Ground
2	TXD	Transmit Data(in)
3	RXD	Receive Data(out)
4	RTS	Request to Send(in)
5	CTS	Clear to Send(out)
6	DSR	Data Set Ready(out)
7	GND	Ground
8	CAD	Carrier Detect(out)

RS-232 specifications call for data communications equipment (DCE), such as this system, to be connected to data terminal equipment (DTE), such as the user's CRT terminal When connecting this system to another DCE, such as a host computer, be sure to interchange TXD (pin 2) with RXD (pin 3), and RTS (pin 4) with CTS (pin 5). This can be done on the cable or it can be accomplished logically by using a Null Modem Due to the variety of interpretations of RS-232, some terminals may not immediately work with the Prototyping System. If difficulties are encountered, first reduce the connections to three signals TXD, RXD, and GND Then if necessary, interchange TXD and RXD signals

2.3 BAUD RATE SELECTION

Any of the eight baud rates listed in Table 2-2 may be selected by proper setting of switches B2, B1 and B0 located near the RS-232 connector

Table 2-2 BAUD RATE

B2	B1	B0	Baud Rate
0	0	0	19200
0	0	1	9600
0	1	0	4800
0	1	1	2400
1	0	0	1200
1	0	1	600
1	1	0	300
1	1	1	110

(0 = Switch off, 1 = Switch on)

For hard-copy printing terminals, an optional line-feed feature may be selected to avoid over-strike of characters after a backspace on error. This feature is selected by setting the LF switch located next to switch B0 to the ON position

2.4 EXTERNAL OSCILLATOR CONNECTIONS

CAUTION

To prevent possible damage to the crystal, never apply an external oscillator signal to X1 or X2 input with crystal Y2 connected to the circuit.

The Prototyping System is supplied with a 10 MHz crystal, therefore it operates the 8X305 MicroController at its full rated speed of 200 nanoseconds per instruction. The crystal may be changed by the user to any frequency from 4 MHz to 10 MHz Alternatively, an external oscillator may be connected to the X1 and X2 inputs of the 8X305, as described in the 8X305 Users Manual The external oscillator may operate at any frequency between 0 2 MHz and 10 MHz Note that the 8X305 is capable of running at frequencies lower than 0 2 MHz, but the Prototyping System's Monitor Processor expects the 8X305 to be finished executing an instruction within 10 microseconds, thereby imposing a lower limit of 0 2 MHz Tie points for X1 and X2 are located next to crystal Y2 and the 8X305 Be sure to disconnect crystal Y2 before connecting the external oscillator inputs to X1 and X2

2.5 INHIBIT JUMPER FOR 8X310 ROM DISABLE

The 8X310 Interrupt Control Coprocessor connects to the Instruction and Address buses of the 8X305 It accomplishes interrupt and subroutine control by disabling the control storage that contains the 8X305's microprogram and placing specific JMP instructions onto the instruction bus To permit the Prototyping System to operate either with or without an 8X310 in the circuit, a jumper is incorporated into the ROM Disable (RD) circuitry

When the 8X310 Interrupt Control Coprocessor is physically present in location U16, the ROM Disable Inhibit Jumper located at R14 next to the 8X310 must not be present so that the 8X310 can disable WCS and avoid bus contention problems When the 8X310 is not present, this jumper must be connected to the board at location R14 to permanently enable the Writeable Control Store RAMs

3.1 POWER UP AND DIAGNOSTICS

When power is applied to the Prototyping System, resident diagnostic programs are executed to test the Micro-Controller and Writeable Control Store (WCS) The following message is then printed

8X305 PROTOTYPING SYSTEM

REV n

SYSTEM CHECK ON

*

where "n" equals the current revision level

If the Prototyping System is functioning improperly, either "MEMORY ERROR" or "8X305 ERROR" messages will be printed Then the "prompt" character (*) will be printed and the user may examine WCS memory or 8X305 functions to diagnose the problem

3.2 MONITOR PROGRAM

With the printing of the "prompt" character (*), system control passes to the monitor program The user may then enter any of the ten monitor commands

I **INPUT 8X305 instructions into memory:**
Accepts a starting WCS memory address and then permits the entering of an 8X305 instruction in mnemonic form and an extension instruction in octal notation

n **Register examine/change, where "n" = register number:**
Displays the register number and its contents and allows a new value to be substituted

(R0 may be accessed by its alternate name AUX by entering "A" or, R10 may be accessed by its alternate name OVF by entering "0")

G **GO execute user's 8X305 program:**
Accepts a starting memory address and executes at full speed until a breakpoint or keyboard entry is reached. Then the contents of the registers and the next executable instruction are displayed, and single stepping can proceed

S **STEP, single step user's program:**
Accepts a starting memory address and displays the contents of the registers and the instruction at that memory address The instruction is executed by hitting the space bar; and successive instructions by successively hitting the space bar

M **MEMORY and breakpoint examine/change:**
Accepts a starting WCS memory address and then displays the contents of that location in mnemonic form and indicates a possible breakpoint by an exclamation point A breakpoint at this location may be set by typing an exclamation point or cleared by typing a backspace A new 8X305 instruction and extension instruction is then entered by typing an I, as with the INPUT command.

L **LB, left-bank examine/change:**
Accepts a bank address (or the currently enabled address, if a blank is entered) and displays the contents of that left-bank address (0-377 octal) A new value may be entered to substitute for the original content

R **RB, right-bank examine/change:**
Operates the same as the LB command except action is upon the right-bank.

D **DUMP memory contents to terminal:**
Accepts a starting WCS memory address and an ending address, and then dumps the memory contents from the start address to the end address onto the RS-232 port in ASCII HEX QUOTE format as described in Section 3 6

F **FILL memory contents from terminal:**
Accepts a starting WCS memory address and fills memory in ASCII HEX QUOTE format as described in Section 3 6

X **XCODE, temporarily set extended microcode latch:**
Accepts a new extension code value to be temporarily set in the extended microcode latch for control of user circuitry The content of the extended microcode section of WCS is not changed by this command

Although the user need only enter a single letter command, the monitor will respond by typing the whole command name as indicated in capitals above

Any of the commands may be aborted before completion by typing an ASCII "control-C" character While entering any number (sequence of octal digits), corrections may be made by entering a backspace character and then entering the correct number

3.3 COMMAND SYNTAX DIAGRAMS

System commands and monitor responses are defined in the syntax diagrams in Figure 3-1a, b and c.

3.4 SAMPLE USAGE

The sample program in Figure 3-3 is shown to give the user an idea of a typical session and includes most commands used by the Prototyping System A short program is input to WCS via the terminal Keyboard that continually increments R6 of the 8X305 and writes each new (incremented) value to location 133 of the 8X350 on the Right-Bank of the IV Bus and to I/O Port 001 on the Left-Bank Since extended microcode is not needed in this example, none was entered as indicated by "/000"

3.5 BREAKPOINTS

Breakpoints are designed to halt the 8X305 just prior to the execution of an instruction on which a breakpoint has been specified If the GO command is issued to start at an address that has a breakpoint set, the system will not stop on that address immediately If the 8X305 should access that address again then a breakpoint stop will occur

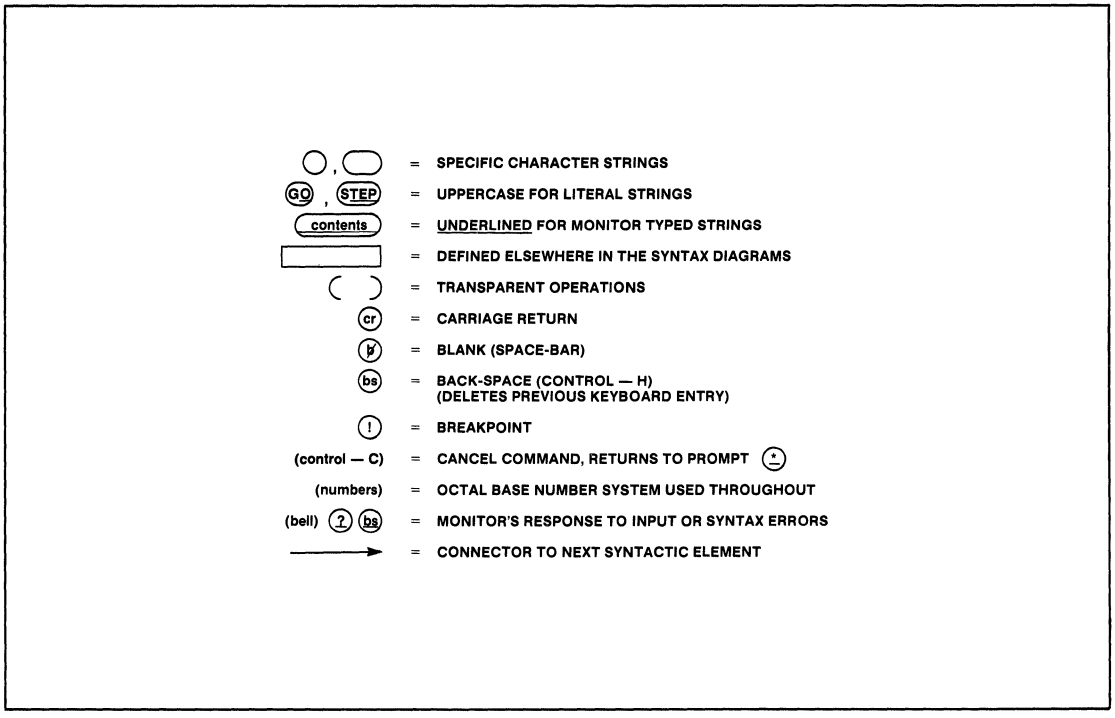


Figure 3-1a. Syntax Definitions

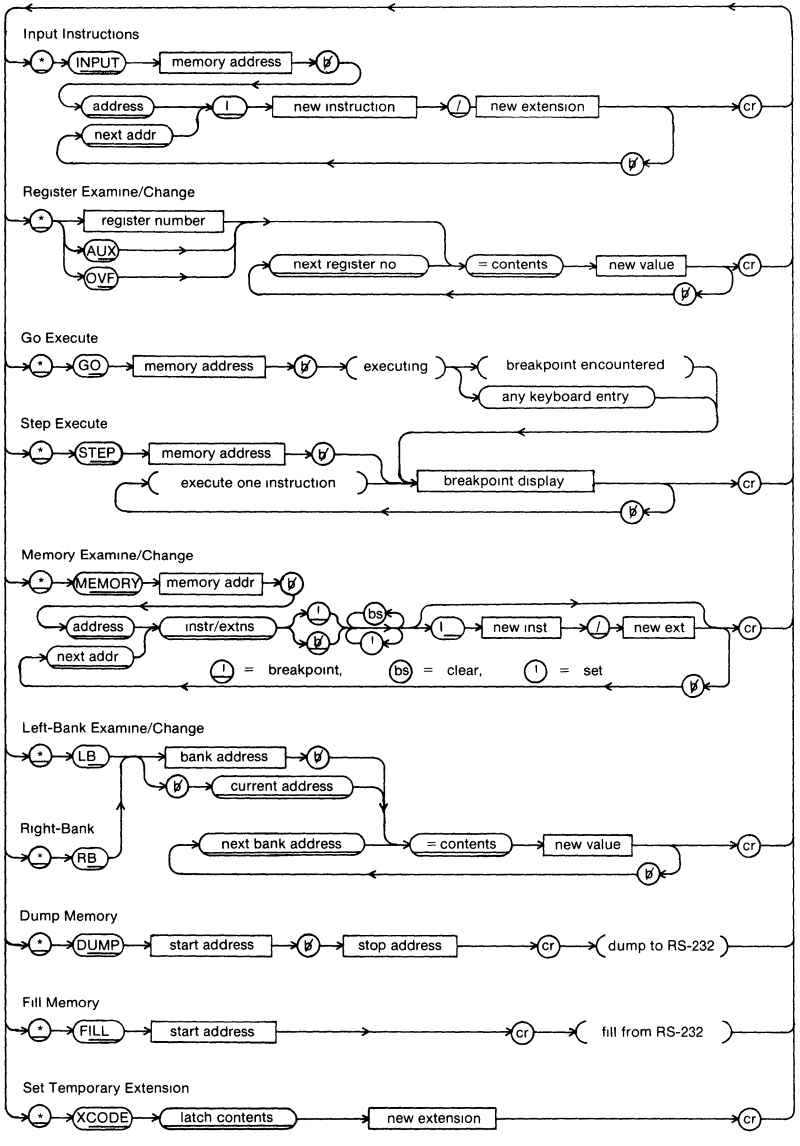
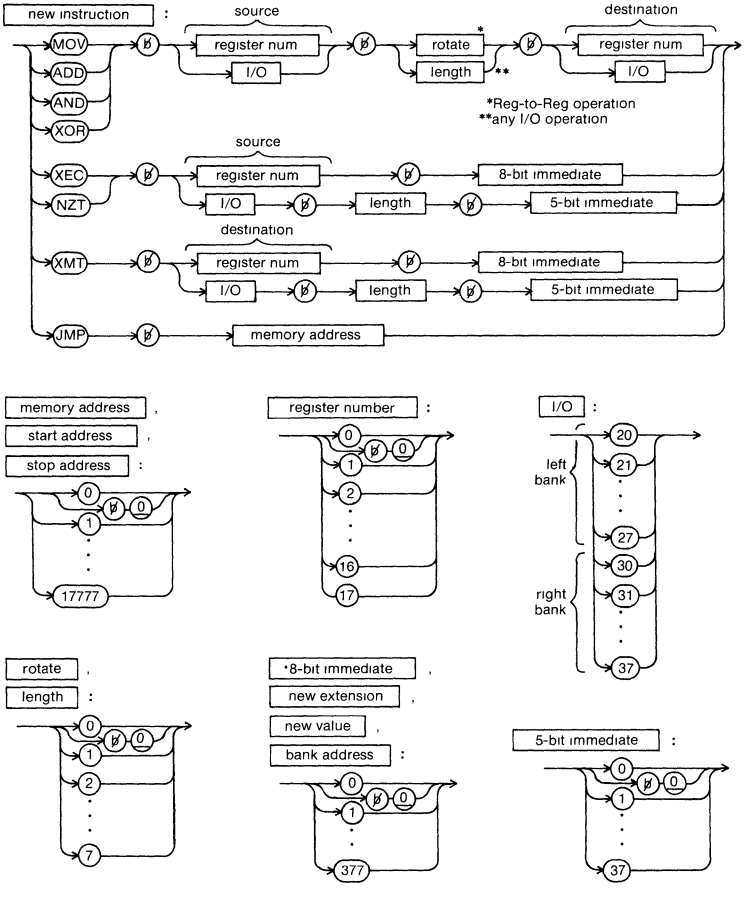


Figure 3-1b. Syntax Flow



breakpoint display (typical):

AUX	R1	R2	R3	R4	R5	R6	R7	OVF	R11	R12	R13	R14	R15	R16	R17
377	000	017	037	000	000	001	222	000	000	000	360	300	000	000	000

00013 — MOV 02 4 37 /244

note — First two lines are column headers, printed each breakpoint or each 20 single steps
— Third line is register contents
— Fourth line is breakpoint, address — instruction/extension
This is the next instruction to be executed in single step

Figure 3-1c. Syntax Flow

```
*
* DUMP 00000 00014
DUMPING HIGH BYTES
(STX)
00'C0'24'B9'C0'AC'68'74'01'10'70'11'F1'
(ETX)
DUMPING LOW BYTES
(STX)
00'00'08'BF'10'FF'FF'96'06'FF'7D'40'D7'
(ETX)
DUMPING EXT BYTES
(STX)
00'00'00'00'00'50'00'00'00'00'00'00'00'
(ETX)
*
*
```

Figure 3-2. Example of ASCII HEX QUOTE Format

3.6 ASCII HEX QUOTE FORMAT

Memory contents to and from the terminal during the DUMP and FILL commands are in an object code format commonly supported by PROM programming hardware known as "ASCII HEX QUOTE" format. Each block of eight-bit wide data is preceeded by an STX (ASCII Start of Text) character. Then each 8-bit byte is represented by 2 ASCII HEX characters (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F) followed by a single quote ('). As many bytes as necessary may be transmitted until an ETX (ASCII End of Text) character terminates the block. Three such blocks are transmitted for any specified memory range. high byte of 8X305 instruction, low byte of 8X305 instruction, and extended microcode byte Figure 3-2 shows an example of ASCII HEX QUOTE format.

3.7 XEC (EXECUTE) INSTRUCTIONS

When stepping through a user program and an 8X305 XEC instruction is encountered, the system will display an "XR" after the next instruction to indicate an XEC range of address

Note that stepping must start on or before an XEC instruction for the program flow to be correct If while running a program, a breakpoint or stop occurs on an instruction that is the target of an XEC instruction, an "XR" will not be displayed and program flow will not be correct if single stepping is then begun.

It is valid to nest any number of XEC instructions Single stepping will work properly provided that the user start on or before the first XEC instruction.

3.8 8X310 INTERRUPT CONTROL COPROCESSOR CONSIDERATIONS

Certain 8X305 "NOP" instructions have specific meanings to the 8X310 as indicated in the data sheet When using an 8X310 in the system, the user must start running or stepping from an instruction that is not an 8X310 instruction It is valid, however, to start running and encounter a breakpoint or stop on an 8X310 instruction and then continue single stepping the program.

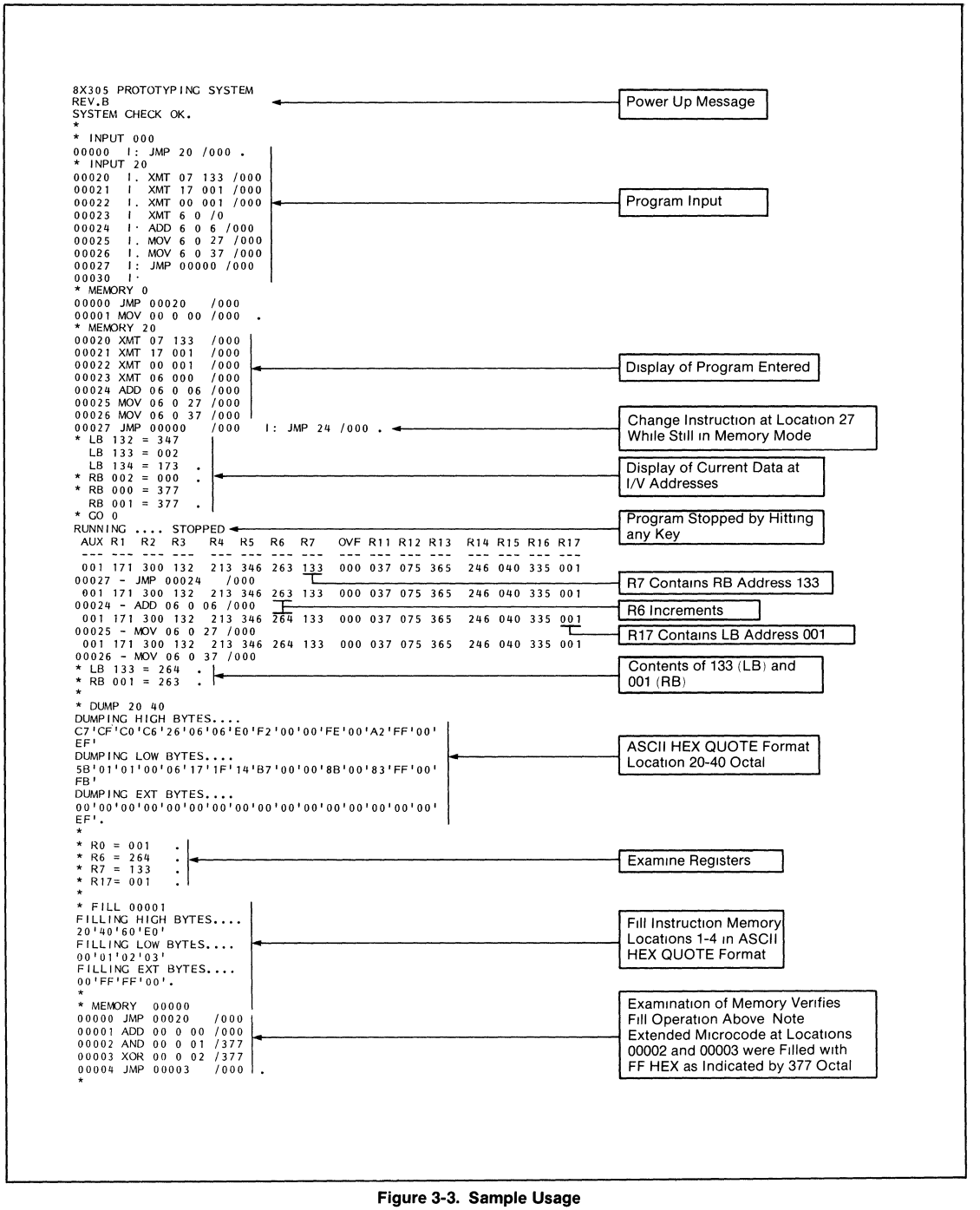


Figure 3-3. Sample Usage

4.1 WIRE-WRAP AREA

The wire-wrap area located at the top of the board provides 26 square inches for user prototyping. This space accommodates standard IC widths from 0.3 to 0.9 inches and also provides power and ground connections.

4.2 IV BUS CONNECTIONS

The IV bus is the major communications link between the 8X305 MicroController and its family of peripherals. The bus is logically partitioned into two banks, referred to as the Left-Bank and Right-Bank. In the Prototyping System the 8X350 Working Storage RAM is connected to the Left-Bank, and the 8X320 Register Array, 8X360 Memory Address Director, and 8X372 I/O Ports are connected to the Right-Bank. All IV bus signals are present at connector J2 as shown in Table 4-1.

Table 4-1 IV BUS CONNECTOR J2

Pin No.	Signal	Description
1	$\overline{IV0}$	BUS (MSB)
3	$\overline{IV1}$	BUS
5	$\overline{IV2}$	BUS
7	$\overline{IV3}$	BUS
9	$\overline{IV4}$	BUS
11	$\overline{IV5}$	BUS
13	$\overline{IV6}$	BUS
15	$\overline{IV7}$	BUS(LSB)
17	V_{CC}	+5 V
19	V_{CC}	+5 V
21	$\overline{HALT}$	Halt
23	$\overline{RESET}$	Reset
25	MCLK	Clock
27	$\overline{LB}$	Left-Bank
29	$\overline{RB}$	Right-Bank
31	SC	Select Control
33	WC	Write Control
(All even pins)	GND	Ground

4.3 I/O PORTS

These 8X372 I/O ports have been provided on the Right-Bank of the IV bus for latching of input or output data. The ports are programmed for addresses 000, 001 and 002 and all signals are available at connectors J4, J5 and J6 respectively. Signals on these connectors are described in Table 4-2. Note that I/O port compatibility allows the user to substitute an 8X376 or 8X382 for any one of the 8X372 I/O ports. (One 8X371 non-addressable I/O port may be substituted, but ONLY if all other components on that bank are removed.)

Table 4-2 I/O PORT CONNECTORS J4, J5, AND J6

Pin No.	Signal	Description
2	UD7	User Data (LSB)
4	UD6	User Data
6	UD5	User Data
8	UD4	User Data
10	UD3	User Data
12	UD2	User Data
14	UD1	User Data
16	UD0	User Data (MSB)
18	$\overline{UOC}$	Output Control
20	UIC	Input Control
(All odd pins)	GND	Ground

4.4 EXTENDED MICROCODE CAPABILITY

"Extended Microcode" is a technique commonly used in 8X305 MicroController based designs to optimize performance. It is implemented by designing program memory to be wider than the 16-bit instruction word required for the 8X305. The additional bits are referred to as the extension and can be used for fast I/O selection or other system control and status monitoring purposes.

The Prototyping System uses a 24-bit instruction word, thus providing facilities for 8 bits of extended microcode. These bits are accessible to the user at connector J3 as shown in Table 4-3.

Table 4-3 EXTENDED MICROCODE BITS AT CONNECTOR J3

Pin No.	Signal	Description
1		No Connection
3	ED0	Extended Microcode (MSB)
5	ED1	Extended Microcode
7	ED2	Extended Microcode
9	ED3	Extended Microcode
11	ED4	Extended Microcode
13	ED5	Extended Microcode
15	ED6	Extended Microcode
17	ED7	Extended Microcode (LSB)
19		No Connection
(All even pins)	GND	Ground

Table 4-4 8X320 SIGNAL CONNECTIONS

Signal	Description
B/$\overline{W}$	Byte/Word Control
A0	Primary Port Address (LSB)
A1	Primary Port Address
A2	Primary Port Address
A3	Primary Port Address (MSB)
$\overline{PIOE}$	Programmed I/O Enable
R/$\overline{W}$	Read/Write Control
WS	Write Strobe
$\overline{DMAE}$	Direct Mem. Access Enable
D7A	Primary Data Port (LSB)
D6A	Primary Data Port
D5A	Primary Data Port
D4A	Primary Data Port
D3A	Primary Data Port
D2A	Primary Data Port
D1A	Primary Data Port
D0A	Primary Data Port
D7B	Primary Data Port
D6B	Primary Data Port
D5B	Primary Data Port
D4B	Primary Data Port
D3B	Primary Data Port
D2B	Primary Data Port
D1B	Primary Data Port
D0B	Primary Data Port (MSB)

4.5 8X310 CONNECTIONS

The 8X310 is connected to the 8X305 MicroController and the Writeable Control Store RAM to provide interrupt and subroutine capability. Five additional signals are provided for user interface as described in the 8X310 data sheet. These signals are accessible at tie points just to the right of the 8X310 chip:

STF	Stack Full Status
ID	Interrupt Disable Control
INT0	Interrupt 0 Input
INT1	Interrupt 1 Input
INT2	Interrupt 2 Input

4.6 8X320 CONNECTIONS

An 8X320 Bus Interface Register Array has ben provided on the IV Bus as a Right-Bank I/O device for interfacing to the user's system. The primary data, status and command signals are accessible at tie points located between the 8X320 and the wire-wrap area. A list of these signals is provided in Table 4-4.

4.7 8X360 CONNECTIONS

The 8X360 Memory Address Director has been incorporated into the Prototyping System design to facilitate implementation of a DMA channel. It is connected to the IV Bus as a Right-Bank I/O device. Interconnection to the signals listed in Table 4-5 can be made at the tie points located between the 8X360 and the wire-wrap area.

In applications using extended microcode to enable I/O devices care must be taken to avoid IV Bus contention with 8X300 Family peripheral devices enabled through the more commonly used address — select cycle. Refer to the 8X305 Users Manual for more information on extended microcode operations.

4.8 MEMORY EXPANSION

The Prototyping System is provided with 256 24-bit words of Writeable Control Storage; 16 bits for 8X305 instructions and 8 bits for extended microcode. The depth of Control Storage can be increased by the connection of an expansion module to connector J1, as shown in Table 4-6. A 4096 word Writeable Control Storage Expansion Module is available from Signetics (Part Number 8X300KT2SK). A schematic for this expansion module is provided in Appendix D.

Table 4-5 8X360 SIGNAL CONNECTIONS

Signal	Description
CLK	Clock Input
TC	Terminal Count Status
LABN	Loop Abort Control
TSCL	Tri-state Control
A0	Address Output (LSB)
A1	Address Output
A2	Address Output
A3	Address Output
A4	Address Output
A5	Address Output
A6	Address Output
A7	Address Output
A8	Address Output
A9	Address Output
A10	Address Output
A11	Address Output
A12	Address Output
A13	Address Output
A14	Address Output
A15	Address Output (MSB)
RS0	Register Select (LSB)
RS1	Register Select
RS2	Register Select
RS3	Register Select (MSB)

Table 4-6 MEMORY EXPANSION CONNECTOR J1

Pin No.	Signal	Description
1	RAMEN	Disables on-board RAM
3	GND	Ground
5	GND	Ground
7	OD	Output Disable
9	BKPT	Breakpoint
11	$\overline{W}$	Write
13	—	No Connection
15	—	No Connection
17	—	No Connection
19	—	No Connection
21	CE1	Chip Enable
23	A0	8X305 Address (MSB)
25	A1	8X305 Address
27	A2	8X305 Address
29	A3	8X305 Address
31	A4	8X305 Address
33	A5	8X305 Address
35	A6	8X305 Address
37	A7	8X305 Address
39	A8	8X305 Address
41	A9	8X305 Address
43	A10	8X305 Address
45	A11	8X305 Address
47	A12	8X305 Address (LSB)
49	V_{CC}	+5 V

Pin No.	Signal	Description
2	I15	8X305 Instruction (LSB)
4	I14	8X305 Instruction
6	I13	8X305 Instruction
8	I12	8X305 Instruction
10	I11	8X305 Instruction
12	I10	8X305 Instruction
14	I9	8X305 Instruction
16	I8	8X305 Instruction
18	I7	8X305 Instruction
20	I6	8X305 Instruction
22	I5	8X305 Instruction
24	I4	8X305 Instruction
26	I3	8X305 Instruction
28	I2	8X305 Instruction
30	I1	8X305 Instruction
32	I0	8X305 Instruction (MSB)
34	E7	Extended Microcode (LSB)
36	E6	Extended Microcode
38	E5	Extended Microcode
40	E4	Extended Microcode
42	E3	Extended Microcode
44	E2	Extended Microcode
46	E1	Extended Microcode
48	E0	Extended Microcode (MSB)
50	V_{CC}	+5 V

As can be noted with the aid of the block diagram in Figure 5-1, the 8X305 prototyping system board contains circuits which may be categorized as follows:

1. Monitor Processor
2. 8X305 MicroController and Family
3. Writeable Control Store
4. Run/Step Logic

5.1 FUNCTIONS OF THE MONITOR PROCESSOR

The Monitor Processor, an 8035 microprocessor and peripherals, controls all the commands and operations described in Chapter 3. The Monitor Processor handles all communication with the terminal as well as reading and writing the 8X305's program storage, registers, and I/O port contents.

The 8X305 can execute instructions from Writeable Control Storage or an instruction that is latched into the 8243 by the Monitor Processor. Typically the instruction in the 8243 will store or read an 8X305's register contents, I/O Port contents, or set the address in the 8X305 Program Counter.

The 8243 is also used to read and write the contents of Writeable Control Store. Since the 8X305 does not have an address bus that can be three-stated and because a buffer would increase the memory access time, to read a specific memory location a JMP is "forced" upon the 8X305 by way of the 8243 to set the address lines.

The Monitor Processor reads the register contents of the 8X305 by forcing an XEC Rn, 000, where Rn is the desired register. This causes the register contents to be placed on the lower eight address lines of the 8X305 where it may be read by the Monitor Processor and sent out on the RS-232 interface. To store a value into the 8X305, the Monitor Processor will force a XMT Rn, XXX, where XXX is the desired register contents. (For R12 and R13, this will be accomplished by a XMT followed by a MOV.)

5.2 8X305 FAMILY

With the following two exceptions the 8X305 MicroController and its supporting peripherals connect to the prototyping system in a conventional manner:

1. Rather than a direct tie to the MCLK output of the 8X305, the MCLK input to the 8X310 Interrupt Control Coprocessor is gated. The gating circuits are required to implement correct single-step operation of the system.
2. The $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ inputs to the 8X305 are gated. Connected in this manner, the $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ signals will only affect the MicroController in the run mode. User circuits requiring either or both of these inputs should pick up the signals via the IV Bus connector J2.

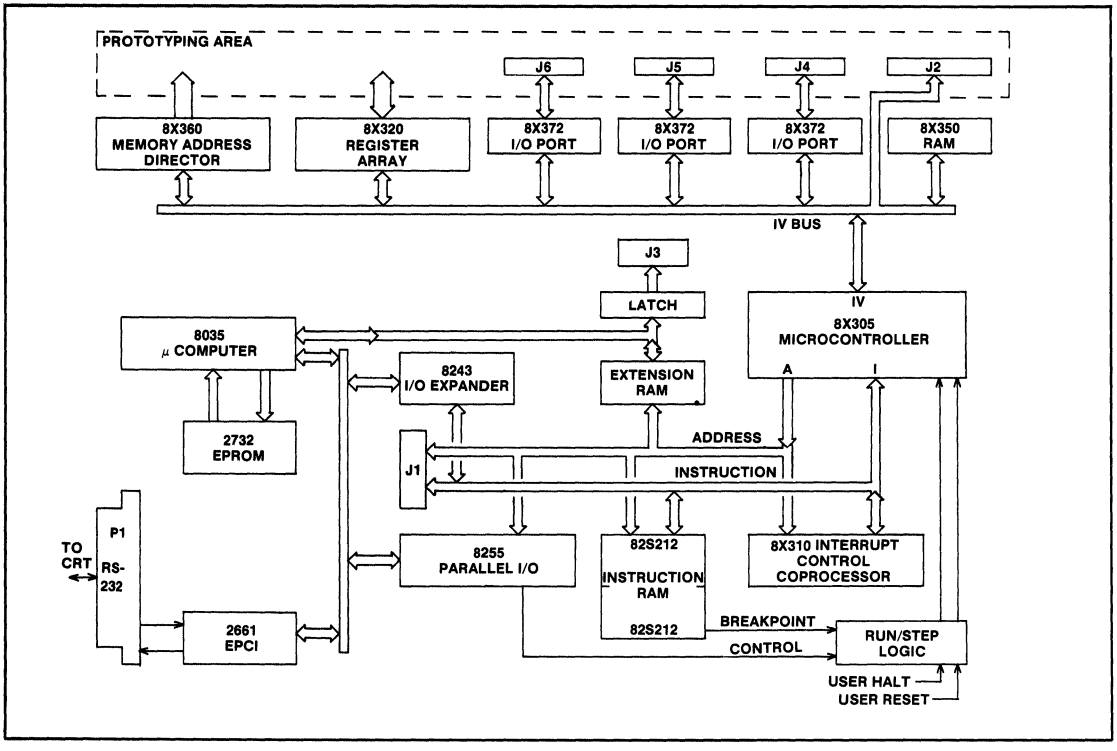


Figure 5-1. Detailed Block Diagram

5.3 WRITEABLE CONTROL STORAGE

Instead of the usual PROM or ROM instruction storage found in a typical 8X305 based system, a Writeable Control Store (WCS) has been implemented with high speed RAM to facilitate programming via the RS-232 terminal. The RAM memory provides 256 x 16 bits for 8X305 instruction storage, 256 x 8 bits for extended microcode, and 256 x 1 bit for breakpoints. If extended microcode is not desired the RAM chip at U21 may be removed and references to the extension will be removed from the display. Any one or all memory address locations may contain a breakpoint.

Note that no page decoding is provided on the board, so the 256 words of instructions will be repeated every 256 addresses throughout the entire 8K memory range of the 8X305.

The memory may be expanded up to the full 8K directly addressable by the 8X305. A 4K word Writeable Control Storage Expansion Module is available from Signetics (Part Number 8X300KT2SK). When the additional memory is installed in J1, the RAM enable (RAMEN) signal is grounded to disable the on-board 256-word memory, and the Monitor Processor is signaled to provide the correct write cycle at J1 for the added RAM. See Figure 5-2 for the differences:

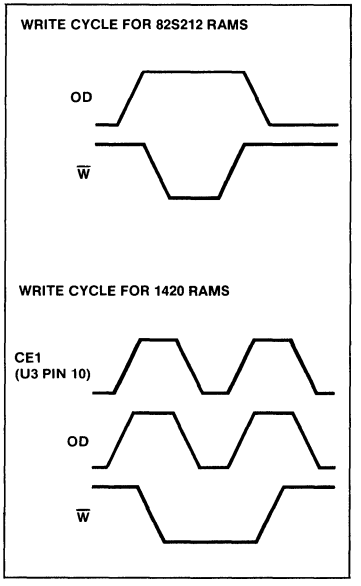


Figure 5-2. Write Cycle Variations

5.4 RUN STEP LOGIC

The Run-Step logic consists of components U5, U6, U7, U9 and U10 on the schematic in Appendix A. These circuits provide the control logic required to allow the 8X305 to execute instructions at full speed or in a single step mode of operation. This is easily accomplished since all instructions are executed within one machine cycle, the time from the falling edge of MCLK to the next falling edge of MCLK. The $\overline{HALT}$ input is sampled by the 8X305 sometime after the falling edge of MCLK. If it is low, the address lines of the MicroController are held stable; the current instruction is executed after the $\overline{HALT}$ input goes high (inactive). During the time that the $\overline{HALT}$ input is low (active), the MCLK output is unaffected. Inputs to the Run-Step logic are labeled RUN/$\overline{WAIT}$, STEP, BKPT and MCLK; the output is labeled $\overline{HALT}$ and connected directly to the $\overline{HALT}$ input of the 8X305 MicroController.

Two of the inputs, RUN/$\overline{WAIT}$ and STEP, are controlled by the Monitor Processor. The BKPT input connects to the extra bit in WCS that is used for breakpoints. The MCLK input comes directly from the MCLK output of the 8X305.

During single stepping the RUN/$\overline{WAIT}$ line is low and a pulse on the STEP line causes the 8X305 to execute only the current instruction. This is because the $\overline{HALT}$ line will go high for just one machine cycle. Entering the run mode the RUN/$\overline{WAIT}$ line is high and a pulse on the STEP line causes the 8X305 to begin executing instructions from the current address at full speed. The $\overline{HALT}$ input will go high and remain so until the RUN/$\overline{WAIT}$ line is brought low or until a breakpoint is encountered.

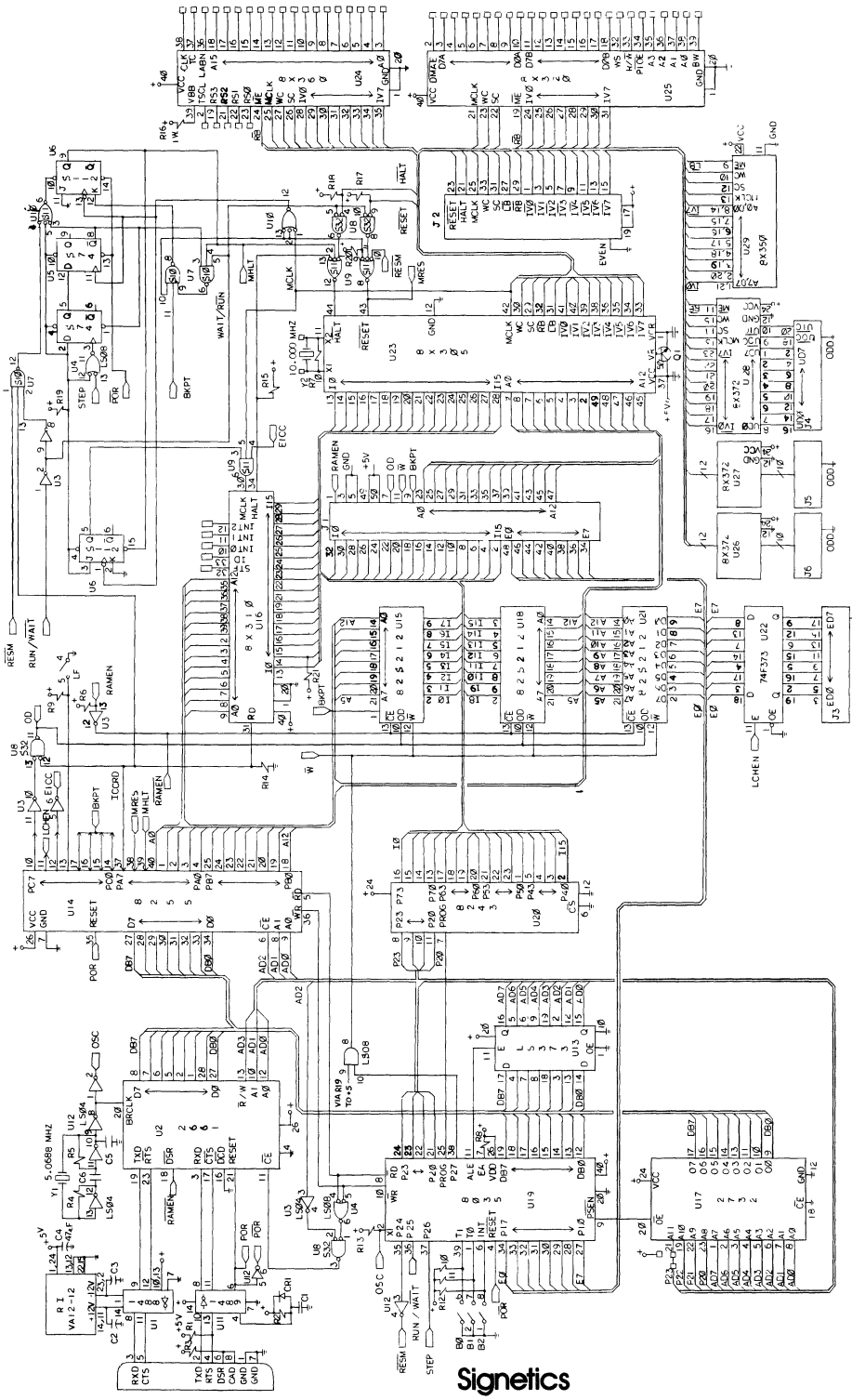
Appendices

A. 8X300KT1SK Prototyping System Schematic

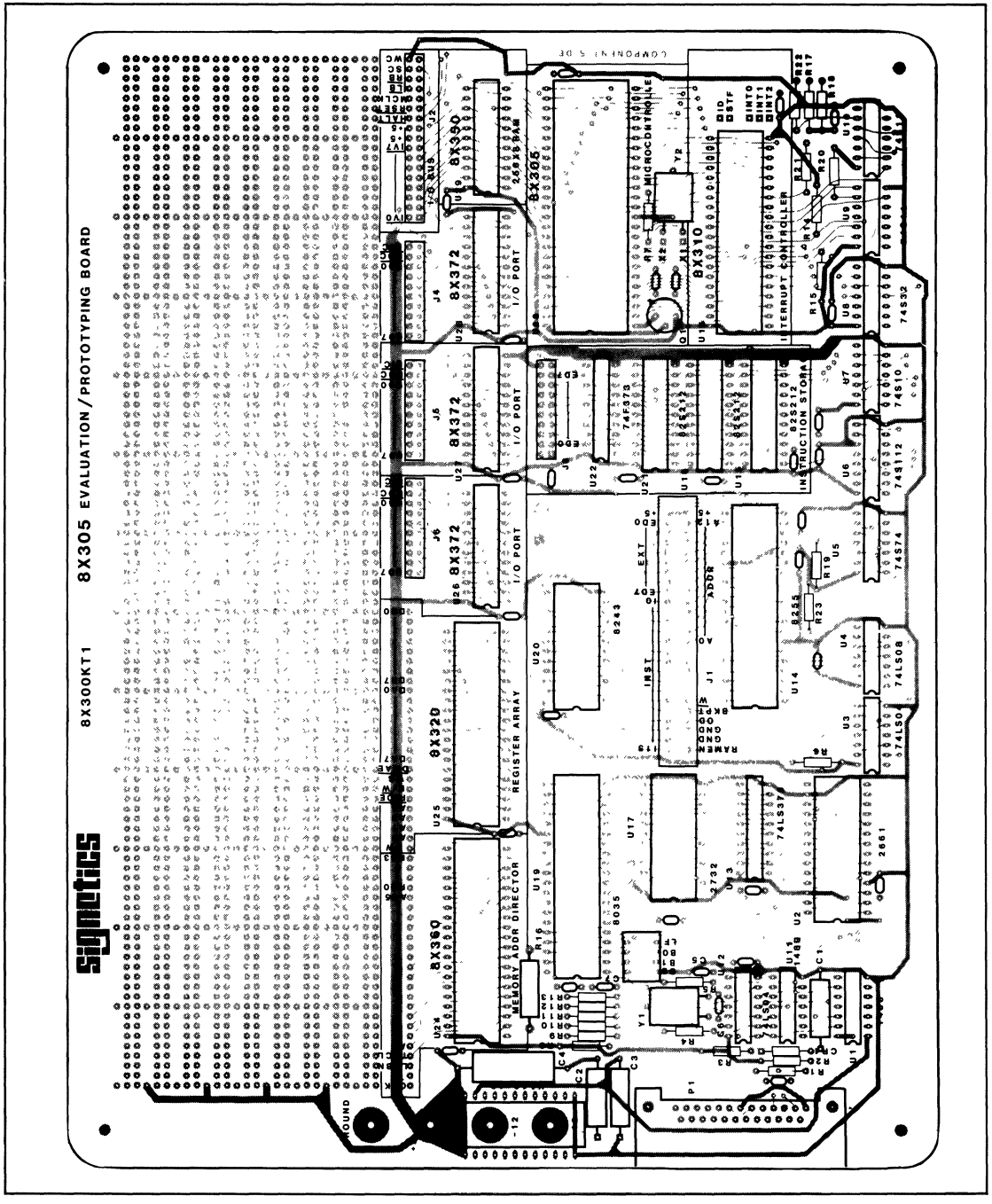
B. 8X300KT1SK PCB Layout and Parts Placement

C. Parts List

D. Memory Expansion Assembly Schematic



Appendix A. 8X300KT1SK Prototyping System Schematic



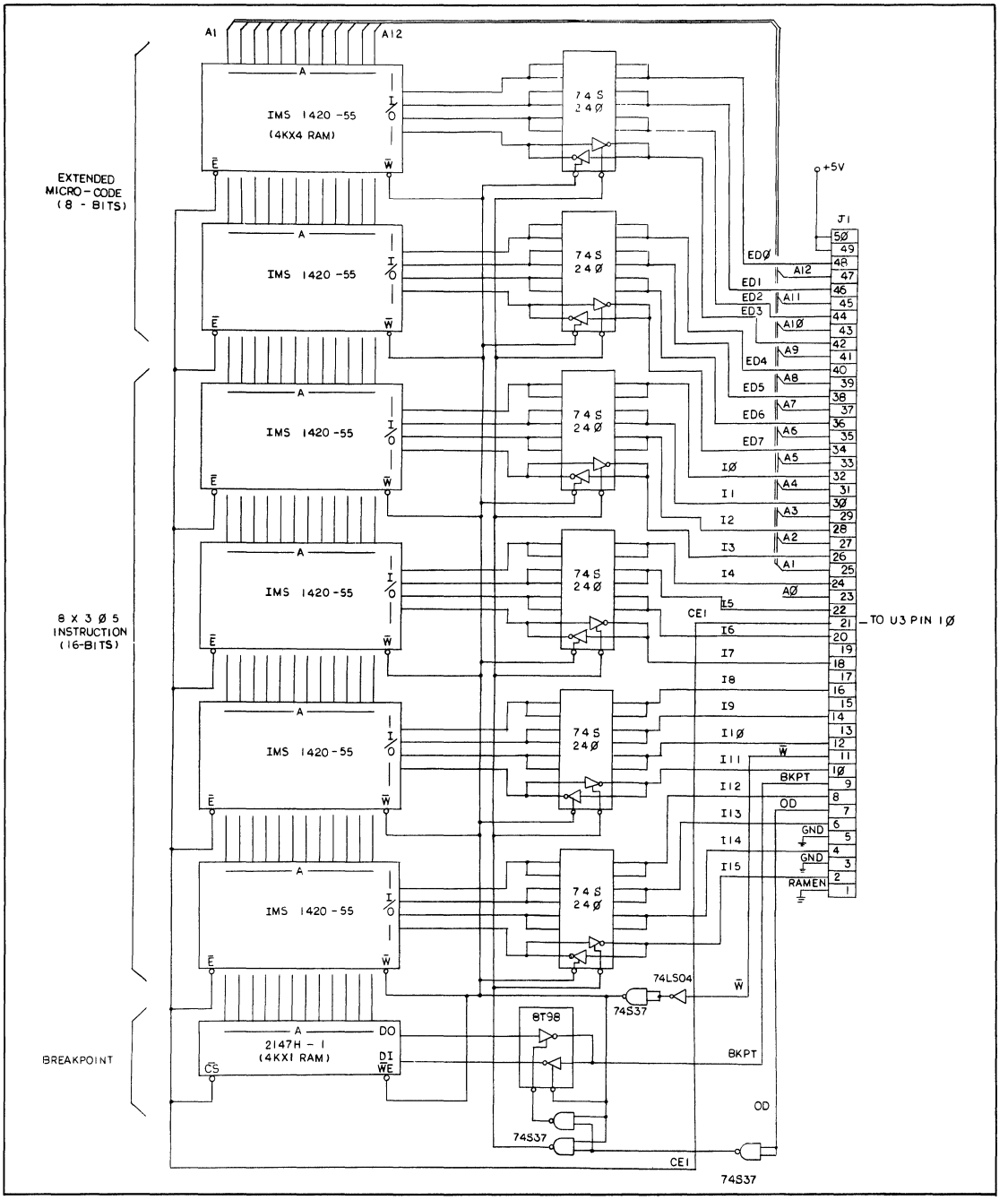
Appendix B. 8X300KT1SK PCB Layout and Parts Placement

Item No.	Manufacturer	Part Number	Description	Designator	Qty.
1	Signetics	MC1488N	Quad Line Driver	U1	1
2	Signetics	SCN2661CC1N28	EPCI	U2	1
3	Signetics	N74LS04N	Hex Inverter	U3, U12	2
4	Signetics	N74LS08N	Quad AND Gate	U4	1
5	Signetics	N74S74N	Dual D-Flip-Flop	U5	1
6	Signetics	N74S112N	Dual J-K Flip-Flop	U6	1
7	Signetics	N74S10N	Triple NAND Gate	U7	1
8	Signetics	N74S32N	Quad OR Gate	U8	1
9	Signetics	N74S11N	Triple AND Gate	U9, U10	2
10	Signetics	MC1489N	Quad Line Receiver	U11	1
11	Signetics	N74LS373N	Octal Latch	U13	1
12	Intel	P8255A	PPI	U14	1
13	Signetics	82S212N	256 x 9 RAM	U15, U18, U21	3
14	Signetics	N8X310N	Interrupt Control Coprocessor	U16	1
15	Intel	2732A-4	4096 x 8 EPROM	U17	1
16	Signetics	SCN8035AC6N40	8-Bit Microcomputer	U19	1
17	Intel	P8243	Input/Output Expander	U20	1
18	Signetics	N74F373N	Octal Latch	U22	1
19	Signetics	8X305I/N	MicroController	U23	1
20	Signetics	N8X360N	Memory Address Director	U24	1
21	Signetics	N8X320N	Register Array	U25	1
22	Signetics	N8X372-000N	I/O Port	U26	1
23	Signetics	N8X372-001N	I/O Port	U27	1
24	Signetics	N8X372-002N	I/O Port	U28	1
25	Signetics	N8X350N	256 x 8 RAM	U29	1
26	ITT CANNON	DBP-25SAA	RS-232 Connector	P1	1
27	TRW CINCH	252-25-30-360	Edge Connector, 50 Pin	J1	
28	Spectra-Strip	800-579	Header, 34 Pin	J2	1
29	Spectra-Strip	800-586	Header, 20 Pin	J3, J4, J5, J6	4

Appendix C. Parts List

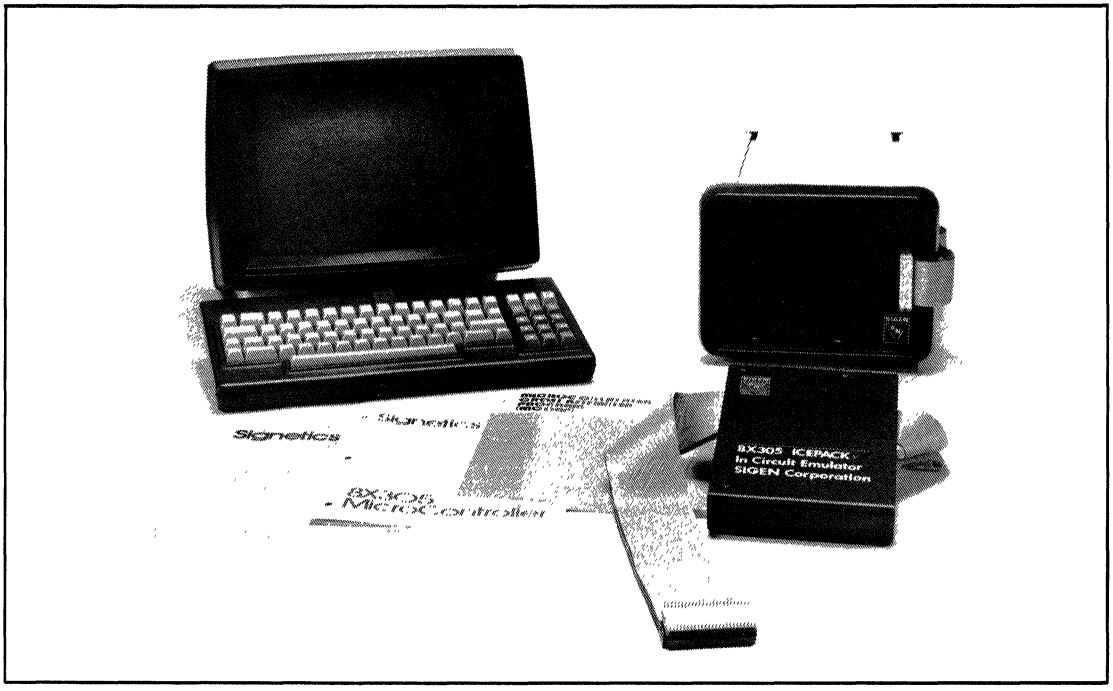
Item No	Manufacturer	Part Number	Description	Designator	Qty.
30	Reliability	VA12-12	DC-DC Converter		
31	Saronix	NMP051L	Crystal, 5 688 MHz	Y1	1
32	Saronix	NMP100L	Crystal, 10 000 MHz	Y2	1
33		2N5320	Transistor	Q1	1
34	ALCO	DSS-4	Switch, Mini-dip	B2, B1, B0, LF	1
35	Smith	230	Binding Post		4
36		1N914	Diode	CR1	1
37			CAP, 0 1 μF		28
38			CAP, 47 μF, 20 V	C2, C3, C4	3
39			CAP, 47 μF, 6 V	C1	1
40			CAP, 47 pF	C5	1
41			CAP, 0 1 μF	C6	1
42			RES, 1K, 1/4 W	R19	1
43			RES, 10K, 1/4 W	R1, R2, R3	3
44			RES, 390, 1/4 W	R4, R5	2
45			RES, 2 2K, 1/4 W	R6-R13, R15, R17, R18, R20, R21	13
46			RES, 18, 1 W	R16	1
47	H H Smith	2501	Bolt, Nylon 4 — 40 x 3/8"	P1	2
48	H H Smith	2554	HEX Nut, Nylon 4 — 40	P1	2
49	BURNDY	DILBQ50P-101	Socket, 50 Pin	U23	1
50	T I	C844002	Socket, 40 Pin	U14, U16, U19, U24, U25	5
51	T I	C842802	Socket, 0 6" 28 Pin	U2	1
52	T I	C842402	Socket, 0.6" 24 Pin	U17, U20	2
53	EMC	17424-01-445	Socket, 0 4" 24 Pin	U26, U27, U28	3
54	T I	C842202	Socket, 0 4" 22 Pin	U15, U18, U21, U29	4
55	T I	C842002	Socket, 0 3" 20 Pin	U22	1
56	Signetics	PCB-82001	P C Board		1
57	H H Smith	2450	Rubber Bumper		5

Appendix C. Parts List (continued)



Appendix D. Memory Expansion Assembly Schematic

ICEPACK 8X305



FEATURES

- Diagnostic Monitor for controlled program execution, 32 breakpoints, register, memory and I/O port examination/change, download/upload memory
- In-line assembler/disassembler for fast debugging of 8X305 code in symbolic assembly language
- System trace memory for 128 addresses, 12 bites each
- On-board emulation memory of 4096 x 24 bits
- Supports all other 8X305 family devices
- Supports microcoded designs using expanded instruction widths
- Power-on diagnostics
- Emulator and software runs with other CP/M* or ISIS* based systems

COMPLETE HARDWARE/SOFTWARE DEVELOPMENT SYSTEM INCLUDING:

- 8X305 Emulator module
- CP/M 2.2 System — Z80A, 64K RAM, dual minifloppies with 1.6 Mbytes storage
- Screen oriented editor for easy program development
- Cross Assembler supporting Signetics standard format mnemonics
- IBM P.C. version available

FASTER PRODUCT DEVELOPMENT

Demanding control applications based on the low cost, high performance Signetics 8X305 bipolar microcontroller can now be developed and implemented quickly and economically with the SIGEN 8X305 ICEPACK.

ICEPACK is a powerful, high performance development and in-circuit emulation system for use with the 8X305 series microcontroller product family. Designed for CP/M compatibility, ICEPACK provides a cost-effective means of rapid product development without the costly dedicated resources previously required.

---

*CP/M is a trademark of Digital Research Corp.
*ISIS is a trademark of Intel Corporation.

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PERFORMANCE YOU NEED

ICEPACK provides both the hardware performance and software tools needed for efficient 8X305 product development throughout a broad range of applications. Designed specifically by SIGEN for the development of 8X305 based products, ICEPACK performance has been proven throughout a variety of products. Its capabilities are especially useful in real time control applications.

The ICEPACK Emulator module simply plugs into the prototype system 8X305 socket through a flat ribbon cable. The ICEPACK's superior noise immunity eliminates typical problems associated with circuit interfacing. The ICEPACK Emulator hardware features high speed electronics supporting clock operation up to 10 MHz. Rugged packaging assures long life and reliable operation.

ICEPACK software includes:

- Powerful screen oriented Editor for easy program devlopment.
- Full featured Cross Assembler supporting standard Signetics mnemonics.
- Powerful diagnostic Monitor enabling controlled program execution including single stepping, breakpoint setting, memory and register examination an modification.
- In-line assembler/disassembler for easy assembly language and debug and patching.

FITS YOUR REQUIREMENTS

ICEPACK is available ready to use as a system, or ready to interface to your floppy based CP/M system. Either way, you get the same powerful ICEPACK System capabilities. The ICEPACK System includes a Z80A based, 64K RAM, dual floppy system, ICEPACK Emulator, interface adapter, CP/M 2.2 and all ICEPACK software and manuals. The ICEPACK Subsystem includes Emulator, parallel interface adapter, interface cables, ICEPACK software, and user manuals.

TECHNICAL SPECIFICATIONS

Power Requirements: 115/230VAC, 100 W

Physical	(CP/M System)	(Emulator)
Height	7.5 inches 190mm	1 inch 25mm
Width	9.5 inches 241mm	6 inches 152mm
Depth	14.5 inches 368mm	8 inches 204mm
Weight	13.0 pounds 5.9 kg	1 pound .45 kg

Environmental

Operating Temperature: 0°C to +40°C
Storage: −40°C to +85°C

Cables

(Target System)

— 100 wire flat cable, 18 inches long
— 20 wire flat cable, 18 inches long

(CP/M System)

— 37 wire flat cable, 5 feet long

Enclosure

(Emulator)

— Anodized brushed aluminum

(CP/M System)

— High impact plastic with internal shielding

DEVELOPMENT DATA I/O PORT PROGRAMMER 8X300/8X305

Hardware Features

- Real time in-circuit emulation to 10 MHz without wait states.
- 8K words of 35ns RAM, 16 or 32-bit words.
- Memory mapping in 1K word increments.
- Compatible with 8X310 Interrupt Control Chip.
- Trace capability includes 128 cycles of address, IV bus, RB, LB, WC, SC, and 3 selectable points in target system. Both input and output phases are traced in each cycle.
- Downloading and Uploading capability provided.
- I/O Port Programmer for 8X372, 8X376, 8X382.

Software Features

- Relocating macroassembler compatible with Signetics MCCAP.
- Linking editor permits linking separately-assembled modules to form one load module.
- Debugger program controls single stepping, stopping on a specified address, printing trace information, disasembling, program patching, changing register contents and memory management. Symbolic debug capability is provided.
- Command file capability provided in the Asembler, Linking Editor, and Debugger program.
- PROM formatting program available. Slices 16 and 32-bit words into 4 or 8-bit groups.

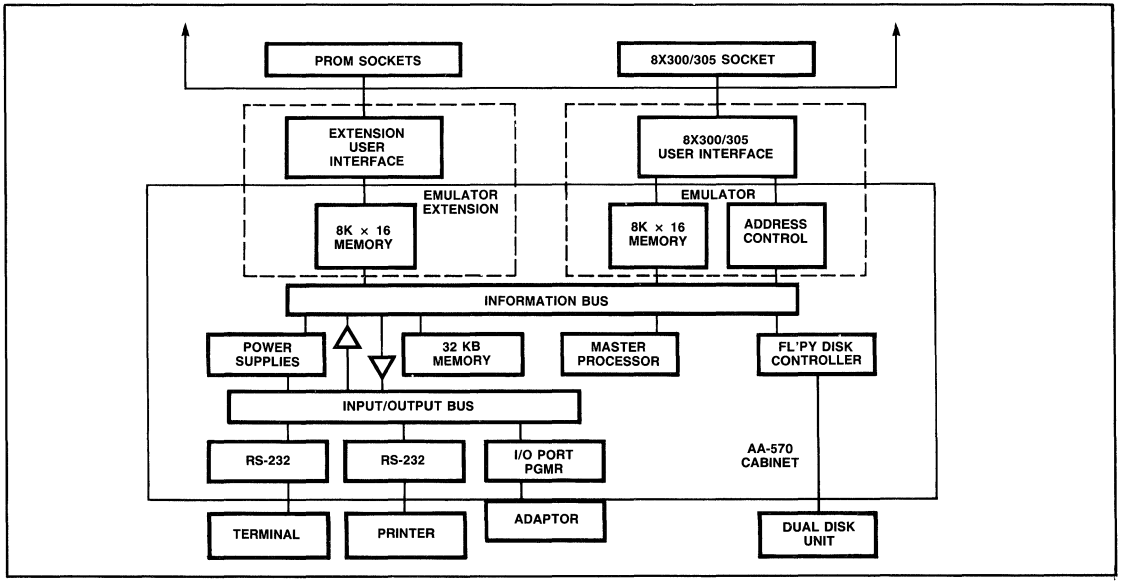
BLOCK DIAGRAM

The block diagram shows how the 8X300/305 support devices are incorporated in an EZ-PRO system. Devices unique to the 8X300/305 includes the AA-572-8X35 In-Circuit Emulator, the AA-572-8X35-M Emulator Extension and the AA-574-8X37 I/O Port Programmer. The Emulator Extension provides an extra sixteen bits of word length over the basic sixteen bits required for the 8X300/305 processor and may or may not be required in a particular development. Note that the emulator consists of three printed circuit board assemblies and the extension, two.

The Address Control assembly incorporates trace memory and logic for memory mapping, stopping, and single stepping as well as circuitry required to communicate with the User Interface and Master Processor. Each Emulator Memory assembly is equipped with 8K 16-bit words of 35 ns memory as well as interface circuitry. This memory is loaded and unloaded under control of the Master Processor and is accessed by addresses generated by the 8X300/305.

The 8X300/305 User Interface has the processor mounted on it along with cable termination networks, cable drivers, some logic and test points. Test points are provided for the three points which may be traced in the target system, connection to the 8X310 Interrupt Control Chip and oscilloscope sync.

TARGET SYSTEM



BLOCK DIAGRAM OF EZ-PRO CONFIGURED TO SUPPORT 8X300/305 DEVELOPMENT WITH 32-BIT WORK LENGTH

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The Extension User Interface is equipped with six DIP sockets and cables which permit connection into PROM sockets located in the target system. Four of the sockets are 18 pin (for 4-bit wide PROMs) and two are 24 pin (for 8-bit wide PROMs). Either set of sockets and cables may be used. Pin outs are compatible with Signetics 82S137, 185, 181, and 191 PROM types.

PROM programming is supported in two ways. Both require that PMFORM, the PROM formatting program, be utilized. After PMFORM has created files consisting of either 4-bit or 8-bit wide slices of the object program words, these files may be directed to a DATA I/O (or equivalent) PROM programmer connected to the RS232 printer port. Alternatively, with 8-bit wide slices, the AA-574-27XX EPROM Programmer may be utilized to write the files into 2716 or 2732 EPROMs. With appropriate off-line equipment, information in the EPROMs may be transferred into bipolar PROMs.

The I/O Port Programmer consists of a printed board assembly, an adaptor that fits into the ZIF socket located on the front of the AA-570 Basic Development Unit and a program. After checking to see that the 8X372/376,382 is properly oriented in the ZIF socket and fuses are unblown, the program permits the desired address to be programmed into the I/O port. Complete checking is then accomplished including validation of the address and transfer of information in both directions through the port.

EZ-PRO SYSTEM ELEMENTS FOR 8X300/305 SUPPORT

Model	Description
AA-570-200	Basic Development Unit
AA-59X	Dual Disk Unit
AA-572-8X35	In-Circuit Emulator for 8X300/305
AA-572-8X35-M	Emulator Extension
AA-562	Printer, RS232 Interface
AA-563	Video Terminal with Screen Editor
AA-553	PMFORM, PROM Formatter Program
AA-574-8X37	I/O Port Programmer
AA-574-27XX	EPROM Programmer for 2716 & 2732

Note that all required programs except PMFROM are supplied at no extra cost.

303A-8X PROGRAMMING TEST ADAPTER

The 303A-8X Programming Test Adapter is designed to program address fuses and activate protect fuses for Signetics' I/O Ports 8X372, 8X374, 8X376, and 8X382. Error messages are displayed if the programmed part is defective or if ambiguous addresses occur during the programming procedure. The test adapter operates in conjunction with the Data I/O Logic PAK 303A-V01 and various models of the Data I/O (System 19, 29A, and 100A). The Programming Test Adapter is quick and easy to use and most Signetics' Franchised Distributors provide on-site programming capabilities for customer parts.

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8X300 Family
Software Support

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5

MCCAP 8X300/8X305 CROSS ASSEMBLER PROGRAM

The MicroController Cross Assembler Program (MCCAP) has been developed to support the Signetics 8X300/8X305 MicroController. MCCAP provides many powerful features including macros, automatic subroutine handling, conditional assembly and extended instructions. These features significantly reduce the time required to compose and assemble MicroController programs. When combined with standard assembler features such as mnemonic op-codes and address labels, these extended features make MCCAP a powerful programming tool.

As input, MCCAP accepts source code written according to the rules presented in this manual. After assembling the source input, MCCAP produces an assembly listing and machine-readable object module.

MCCAP is written in ANSI standard FORTRAN IV and is available on the more popular timesharing services. MCCAP is also available as a fully supported product from Signetics for use on a user's in-house system.

MCCAP 8X300/8X305 CROSS ASSEMBLER PROGRAM

MCCAP, the crossassembler program for the 8X300 and 8X305 Micro-Controllers, is supplied as a 9-track magnetic tape containing FORTRAN IV source code for the crossassembler program. For compatibility with various computer systems, the tape is available in various combinations of density and data encoding. To order, use the following part numbers:

NUMBER	DENSITY	ENCODING
8X300 AS1-1SS	800 BPI	ASCII
8X300 AS1-2SS	800 BPI	EBCDIC
8X300 AS1-3SS	1600 BPI	ASCII
8X300 AS1-4SS	1600 BPI	EBCDIC

8X300/8X305 CROSS ASSEMBLER INSTALLATION GUIDE 8X300AS2SS

INTRODUCTION

The 8X300AS2 runs on an Intel Intellec™ Microcomputer Development System with 64K memory under the contorl of ISIS II operating system.

The 8X300AS2 is composed of a two-pass crossassembler program and a PROM formatter overlay. Both programs are written entirely in Intel 8080 Assembly language, and are assembled on the Intel 8080/8085 Macro Assembler version 4.0, linked and located to execute in overlay.

It assembles both 8X300 and 8X305 programs. Also needed is at least one single or double density disk drive with the PROM formatter overlay always residing in drive zero.

The 8X300AS2 software is contained on three diskettes. Disks 1 and 2 contain the Single Density version and disk 3 contains the Double Density version. Both versions will be shipped when ordered under this part number.

NOTES

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Section 6
Sequencers

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6

MICROPROGRAM CONTROL UNIT — S/N3001

N3001N, N3001I, S3001I

FEATURES

- **Schottky TTL process**
- **45ns cycle time (typ.)**
- **Direct addressing of standard bipolar PROM or ROM**
- **512 microinstruction addressability**
- **Advanced organization:**
  - **9-bit microprogram address register and bus organized to address memory by row and column**
  - **4-bit program latch**
  - **2-flag registers**
- **11 address control functions:**
  - **3 jump and test latch functions**
  - **16 way jump and test instructions**
- **8 flag control functions:**
  - **4 flag input functions**
  - **4 flag output functions**

DESCRIPTION

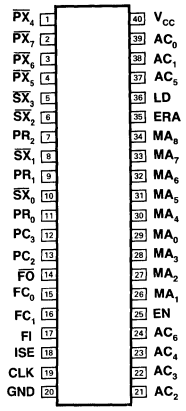
The SN3001 MCU is 1 element of a bipolar microcomputer set. When used with the SN3002, 54/74S182, ROM or PROM memory, a powerful microprogrammed computer can be implemented.

The 3001 MCU controls the fetch sequence of microinstructions from the microprogram memory. Functions performed by the 3001 include:

- Maintenance of microprogram address register
- Selection of next microinstruction address
- Decoding and testing of data supplied via several input buses
- Saving and testing of carry output data from the central processing (CP) array
- Control of carry/shift input data to the CP array
- Control of microprogram interrupts

PIN CONFIGURATION

I PACKAGE

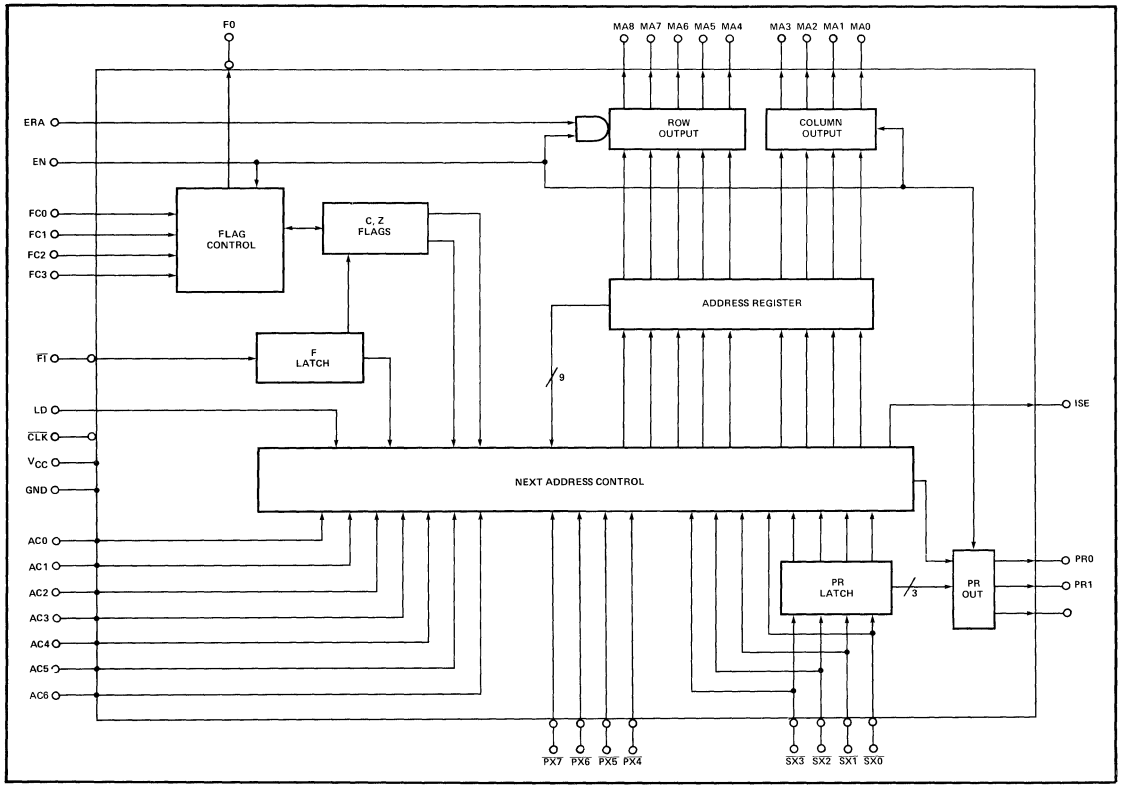


TOP VIEW

ORDER NUMBER

S/N3001

BLOCK DIAGRAM



MICROPROGRAM CONTROL UNIT S/N3001

PIN DESIGNATION

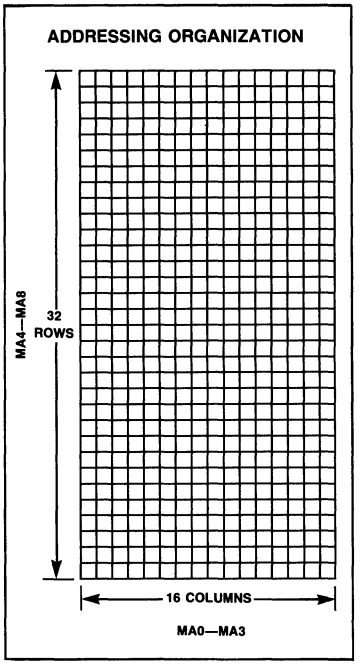
PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-4	$\overline{PX}_4$-$\overline{PX}_7$	Primary Instruction Bus Inputs Data on the primary instruction bus is tested by the JPX function to determine the next microprogram address.	Active low
5,6,8,10	$\overline{SX}_0$-$\overline{SX}_3$	Secondary Instruction Bus Inputs Data on the secondary instruction bus is synchronously loaded into the PR-latch while the data on the PX-bus is being tested (JPX). During a subsequent cycle, the contents of the PR-latch may be tested by the JPR, JLL, or JRL functions to determine the next microprogram address.	Active low
7,9,11	PR_0-PR_2	PR-Latch Outputs The PR-latch outputs (SX_0-SX_2) are synchronously enabled by the JCE function. They can be used to modify microinstructions at the outputs of the microprogram memory or to provide additional control lines.	Open Collector
12,13 15,16	FC_0-FC_3	Flag Logic Control Inputs The flat logic control inputs are used to cross-switch the flags (C and Z) with the flag logic input (FI) and the flag logic output (FO).	Active high
14	$\overline{FO}$	Flag Logic Output The outputs of the flags (C and Z) are multiplexed internally to form the common flag logic output. The output may also be forced to a logical 0 or logical 1.	Active low Three-state
17	$\overline{FI}$	Flag Logic Input The flag logic input is demultiplexed internally and applied to the inputs of the flags (C and Z). Note: The flag input data is saved in the F-latch when the clock input (CLK) is low.	Active low
18	ISE	Interrupt Strobe Enable Output The interrupt strobe enable output goes to logical 1 when one of the JZR functions are selected (see Functional Description). It can be used to provide the strobe signal required by interrupt circuits.	Active high
19	CLK	Clock Input	
20	GND	Ground	
21-24 37-39	AC_0-AC_6	Next Address Control Function Inputs All jump functions are selected by these control lines.	Active high
25	EN	Enable Input When in the high state, the enable input enables the microprogram address, PR-latch and flag outputs.	
26-29	MA_0-MA_3	Microprogram Column Address Outputs	Three-state
30-34	MA_4-MA_8	Microprogram Row Address Outputs	Three-state
35	ERA	Enable Row Address Input When in the low state, the enable row address input independently disables the microprogram row address outputs. It can be used to facilitate the implementation of priority interrupt systems.	Active high
36	LD	Microprogram Address Load Input When the active high state, the microprogram address load input inhibits all jump functions and synchronously loads the data on the instruction buses into the microprogram address register. However, it does not inhibit the operation of the PR-latch or the generation of the interrupt strobe enable.	Active high
40	V_{CC}	+5 Volt supply	

THEORY OF OPERATION

The MCU controls the sequence of microinstructions in the microprogram memory. The MCU simultaniously controls 2 flip-flops (C, Z) which are interactive with the carry-in and carry-out logic of an array of CPEs.

The functional control of the MCU provides both unconditional jumps to new memory locations and jumps which are dependent on the state of MCU flags or the state of the "PR" latch. Each intruction has a "jump set" associated with it. This "jump set" is the total group of memory locations which can be addressed by that instruction.

The MCU utilizes a two-dimensional addressing scheme in the microprogram memory. Microprogram memory is organized as 32 rows and 16 columns for a total of 512 words. Word length is variable according to application. Address is accomplished by a 9-bit address organized as a 5-bit row and 4-bit column address.



FUNCTIONAL DESCRIPTION

The following is a description of each of the eleven address control functions. The symbols shown below are used to specify row and colunm addresses.

MNEMONIC	FUNCTION
row_n	5-bit next row address where n is the decimal row address
col_n	4-bit next column address where n is the decimal column address.

Unconditional Address Control (Jump) Functions

The jump functions use the current microprogram address (i.e., the contents of the microprogram address register prior to the rising edge of the clock) and several bits from the address control inputs (AC0-AC6) to generate the next microprogram address.

Flag Conditional Address Control (Jump Test) Functions

The jump/test flag functions use the current microprogram address, the contents of the selected fag or latch, and several bits from the address control function to generate the next microprogram address.

JUMP FUNCTION TABLE

MNEMONIC	NAME AND FUNCTION
JCC	Jump in current column. AC_0-AC_4 are used to select 1 of 32 row addresses in the current column, specified by MA_0-MA_3, as the next address.
JZR	Jump to zero row. AC_0-AC_3 are used to select 1 of 16 column addresses in row_0, as the next address.
JCR	Jump in current row. AC_0-AC_3 are used to select 1 of 16 addresses in the current row, specified by MA_4-MA_8, as the next address.
JCE	Jump in current column/row group and enable PR-latch outputs. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7-MA_8, as the next row address. The current column is specified by MA_0-MA_3. The PR-latch outputs are asynchronously enabled.

JUMP/TEST FUNCTION TABLE

MNEMONIC	NAME AND FUNCTION
JFL	Jump/test F-latch. AC_0-AC_3 are used to select 1 of 16 row addresses in the current row group, specified by MA_8, as the next row address. If the current column group, specified by MA_3, is col_0-col_7, the F-latch is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8-col_{15}, the F-latch is used to select col_{10} or col_{11} as the next column address.
JCF	Jump/test C-flag, AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. If the current column group specified by MA_3 is col_0-col_7, the C-flag is used to selet col_2 or col_3 as the next column address. If MA_3 specifies column gorup col_8-col_{15}, the C-flag is used to select col_{10} or col_{11} as the next column address.
JZF	Jump/test Z-flag. Identical to the JCF function described above, except that the Z-flag, rather than the C-flag, is used to select the next column address.
JPR	Jump/test PR-latch. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. The 4 PR-latch bits are used to select 1 of 16 possible column addresses as the next column address.
JLL	Jump/test rightmost PR-latch bits. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_2 and PR_3 are used to select 1 of 4 column addresses in col_4 through col_7 as the next column address.
JRL	Jump/test rightmost PR-latch bits. AC_0 and AC_1 are used to select 1 of 4 high-order row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_0 and PR_1 are used to select 1 of 4 possible column addresses in col_{12} through col_{16} as the next column address.
JPX	Jump/test PX-bus and load PR-latch. AC_0 and AC_1 are used to select 1 of 4 row addresses in the current row group, specified by MA_6-MA_8, as the next row address. PX_4-PX_7 are used to select 1 of 16 possible column addresses as the next column address. SX_0-SX_3 data is locked in the PR-latch at the rising edge of the clock.

6

PX-Bus and PR-Latch Conditional Address Control (Jump/Test) Functions

The PX-bus jump/test function uses the data on the primary instruction bus (PX_4-PX_7), the current microprogram address control function to generate the next microprogram address. The PR-latch jump/test functions use the data in the PR-latch, the current microprogram address, and several selection bits from the address control function to generate the next microprogram address.

Flag Control Functions

The flag control functions of the MCU are selected by the 4 input lines designated FC_0-FC_3. Function code formats are given in "Flag Control Function summary".

The following is a detailed description of each of the 8 flag control functions.

Flag Input Control Functions

The flag input control functions select which flag or flags will be set to the current value of the flag input (FI) line.

Data on FI is stored in the F-latch when the clock is low. The content of the F-latch is loaded into the C and/or Z flag on the rising edge of the clock.

Flag Output Control Functions

The flag output control functions select the value to which the flag output (FO) line will be forced.

FLAG CONTROL FUNCTION

MNEMONIC	FUNCTION DESCRIPTION
SCZ	Set C-flag and Z-flag to FI The C-flag and the Z-flag are both set to the value of FI.
STZ	Set Z-flag to FI. The Z-flag is set to the value of FI. The C-flag is unaffected.
STC	Set C-flag to FI The C-flag is set to the value of FI The Z-flag is unaffected.
HCZ	Hold C-flag and Z-flag The values in the C-flag and Z-flag are unaffected.

FLAG OUTPUT CONTROL FUNCTION TABLE

MNEMONIC	FUNCTION DESCRIPTION
FF0	Force FO to 0 FO is forced to the value of logical 0.
FFC	Force FO to C. FO is forced to the value of the C-flag.
FFZ	Force FO to Z FO is forced to the value of the Z-flag.
FF1	Force FO to 1 FO is forced to the value of logical 1

FLAG CONTROL FUNCTION SUMMARY

TYPE	MNEMONIC	DESCRIPTION	FC_1	0
Flag Input	SCZ	Set C-flag and Z-flag to f	0	0
	STZ	Set Z-flag to f	0	0
	STC	Set C-flag to f	1	1
	HCZ	Hold C-flag and Z-flag	1	1

TYPE	MNEMONIC	DESCRIPTION	FC_3	2
Flag Output	FF0	Force FO to 0	0	0
	FFC	Force FO to C-flag	1	0
	FFZ	Force FO to Z-flag	0	1
	FF1	Force FO to 1	1	1

LOAD FUNCTION	NEXT ROW	NEXT COL
LD	MA_8 7 6 5 4	MA_3 2 1 0
0	See Address Control Function Summary	
1	0 X_3 X_2 X_1 X_0	X_7 X_6 X_5 X_4

NOTE
f = Contents of the F- latch xn = Data on PX- or SX-bus line n (active low)

ADDRESS CONTROL FUNCTION SUMMARY

MNEMONIC	DESCRIPTION	FUNCTION							NEXT ROW					NEXT COL			
		AC_6	5	4	3	2	1	0	MA_8	7	6	5	4	MA_3	2	1	0
JCC	Jump in current column	0	0	d_4	d_3	d_2	d_1	d_0	d_4	d_3	d_2	d_1	d_0	m_3	m_2	m_1	m_0
JZR	Jump to zero row	0	1	0	d_3	d_2	d_1	d_0	0	0	0	0	0	d_3	d_2	d_1	d_0
JCR	Jump in current row	0	1	1	d_3	d_2	d_1	d_0	m_8	m_7	m_6	m_5	m_4	d_3	d_2	d_1	d_0
JCE	Jump in column/enable	1	1	1	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	m_2	m_1	m_0
JFL	Jump/test F-latch	1	0	0	d_3	d_2	d_1	d_0	m_8	d_3	d_2	d_1	d_0	m_3	0	1	f
JCF	Jump/test C-flag	1	0	1	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	c
JZF	Jump/test Z-flag	1	0	1	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	Z
JPR	Jump/test PR-latch	1	1	0	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	p_3	p_2	p_1	p_0
JLL	Jump/test left PR bits	1	1	0	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	0	1	p_3	p_2
JRL	Jump/test right PR bits	1	1	1	1	1	d_1	d_0	m_8	m_7	1	d_1	d_0	1	1	p_1	p_0
JPX	Jump/test PX-bus	1	1	1	1	0	d_1	d_0	m_8	m_7	m_6	d_1	d_0	x_7	x_6	x_5	x_4

NOTE
dn = Data on address control line n
mn = Data in microprogram address register bit n
Pn = Data in PR-latch bit n
xn = Data on PX-bus line n (active low)
f,c,z = Contents of F-latch, C-flag, or Z-flag respectively

STROBE FUNCTIONS

The load function of the MCU is controlled by the input line designated LD. If the LD line is active high at the rising edge of the clock, the data on the primary and secondary instruction buses, PX_4-PX_7 and SX_0-SX_3, is loaded into the microprogram address register. PX_4-PX_7 are loaded into MA_4-MA_7. The high-order bit of the microprogram address register MA_8 is set to a logical 0. The bits from primary instruction bus select 1 of 16 possible column addresses. Likewise, the bits from the secondary instruction bus select 1 of the first 16 row addresses.

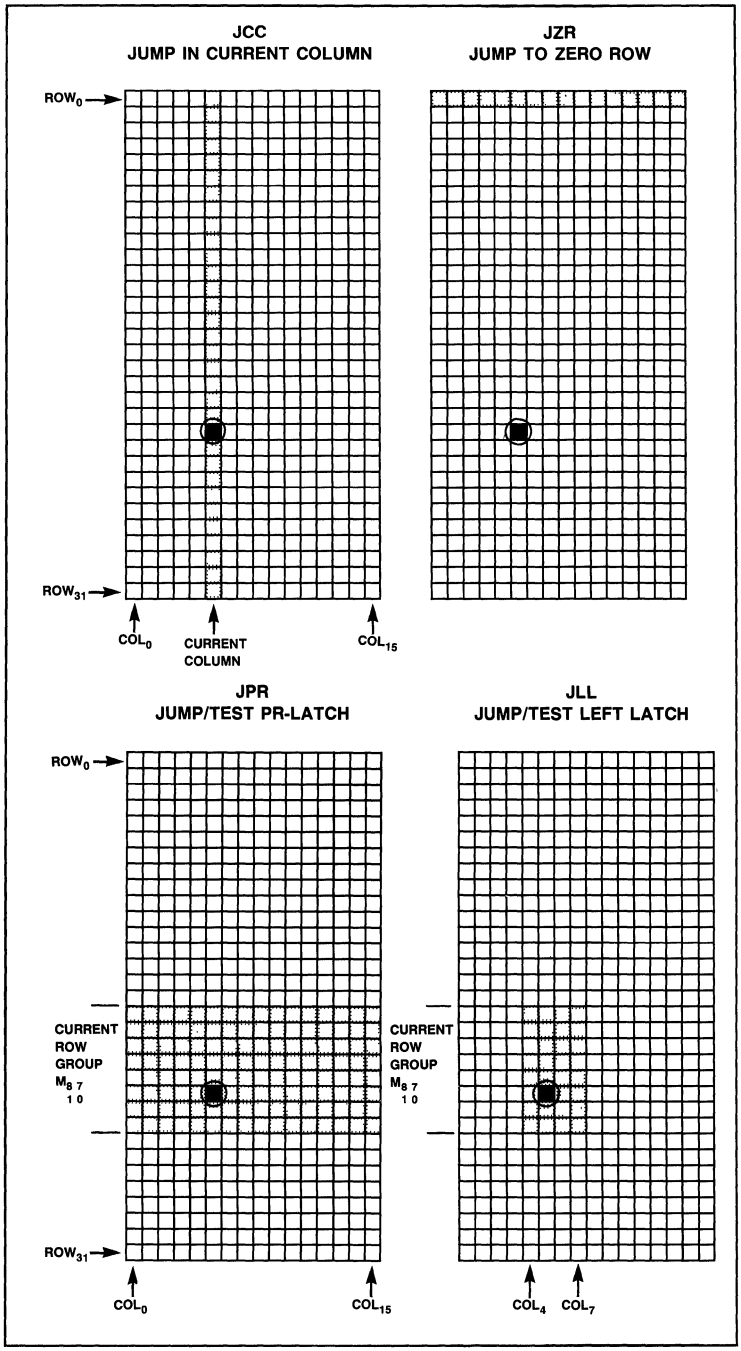
The MCU generates an interrupt strobe enable on the output line designated ISE. The line is placed in the active high state whenever a JZR to col_{15} is selected as the address control function. Generally, the start of a macroinstruction fetch sequence is situated at row_0 and col_{15} so the interrupt control may be enabled at the beginning of the fetch/execute cycle. The interrupt control responds to the interrupt by pulling the enable row address (ERA) input line low to override the selected next row address from the MCU. Then by gating an alternative next row address on to the row address lines of the microprogram memory, the microprogram may be forced to enter an interrupt handling routine. The alternative row address placed on the microprogram memory address lines does not alter the contents of the microprogram address register. Therefore, subsequent jump functions will utilize the row address in the register, and not the alternative row address, to determine the next microprogram addess.

Note, the load function always overrides the address control function on AC_0-AC_6. It does not, however, override the latch enable or load sub-functions of the JCE or JPX instruction, respectively. In addition, it does not inhibit the interrupt strobe enable or any of the flag control functions.

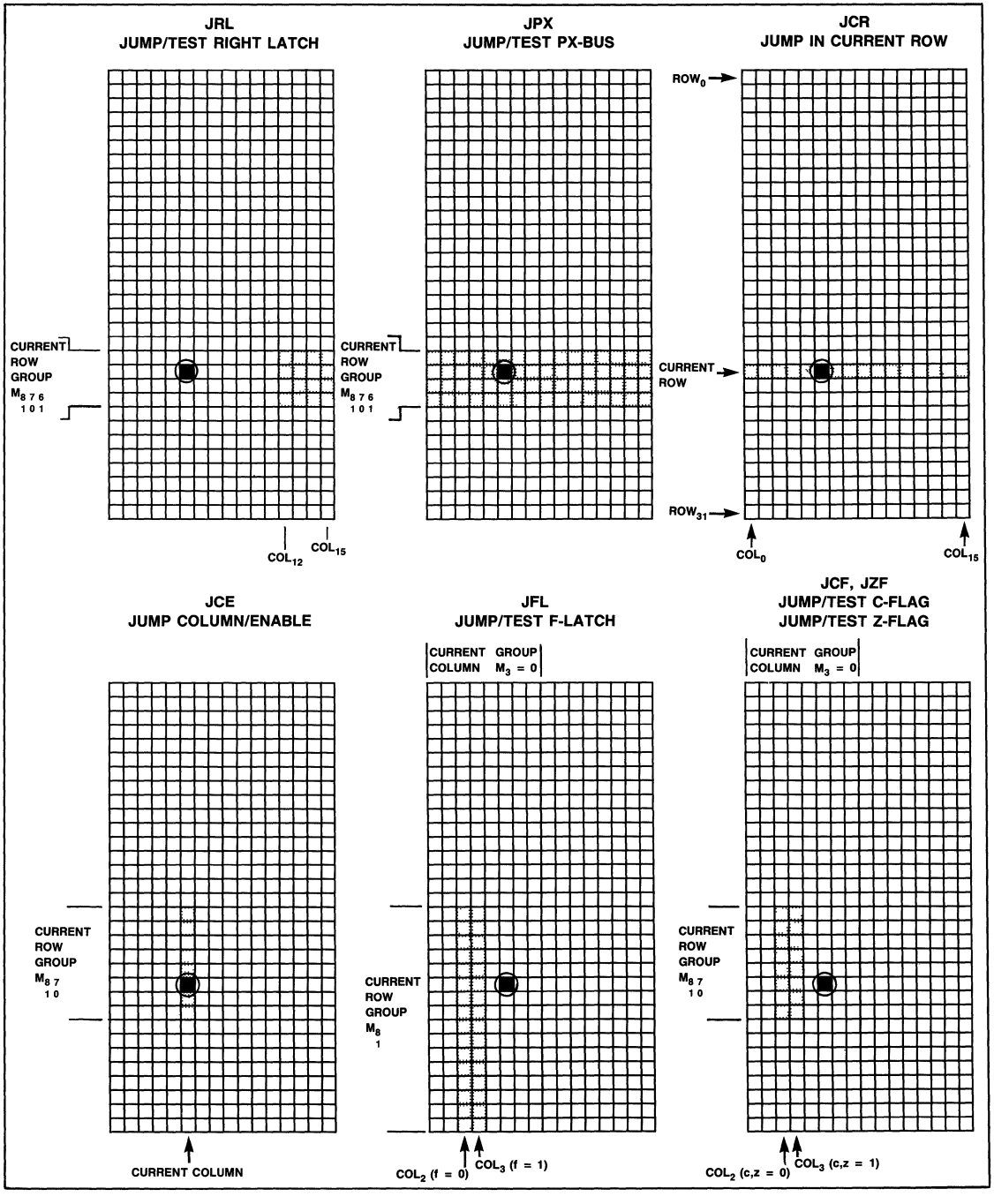
JUMP SET DIAGRAMS

The following 10 diagrams illustrate the jump set for each of the 11 jump and jump/test functions of the MCU. Location 341 indicated by the circled square, represents 1 current row (row_{21}) and current column (col_5) address. The dark boxes indicate the microprogram locations that may be selected by the particular function as the next address.

JUMP SET DIAGRAMS



JUMP SET DIAGRAMS (Continued)



AC ELECTRICAL CHARACTERISTICS

N3001 T_A = 0°C to +70°C, V_{CC} = 5.0V, ± 5%
S3001 T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

	PARAMETER	N3001			S3001			UNIT
		Min	Typ[1]	Max	Min	Typ[1]	Max	
t_{CY}	Cycle Time[2]	60	45		95	45		ns
t_{PW}	Clock Pulse Width	17	10		40	10		ns
	Control and Data Input Set-Up Times:							
t_{SF}	LD, AC_0-AC_6 (Set to "1"/"0")	20	3/14		20	3/14		ns
t_{SK}	FC_0, FC_1	7	5		10	5		ns
t_{SX}	PX_4-PX_7 (Set to "1"/"0")	28	4/13		35	4/13		ns
t_{SI}	FI (set to "1"/"0")	12	−6/0		15	−6/10		ns
t_{SX}	SX_0-SX_3	15	5		35	5		ns
	Control and Data Input Hold Times:							
t_{HF}	LD, AC_0-AC_6 (Hold to "1"/"0")	4	−3/−14		5	−3/−14		ns
t_{HK}	FC_0, FC_1	4	−5		10	−5		ns
t_{HX}	PX_4-PX_7 (Hold to "1"/"0")	0	−4/−13		25	−4/−13		ns
t_{HI}	FI (Hold to "1"/"0")	16	6.5/0		22	6.5/0		ns
t_{HX}	SX_0-SX_3	0	−5		25	−5		ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (mA_0-mA_8, FO) (tPHL/tPLH)		17/24	36	10	17/24	45	ns
t_{KO}	Propagation Delay from Control Inputs FC_2 and FC_3 to Flag Out (FO)		13	24		13	50	ns
t_{FO}	Propagation Delay from Control Inputs AC_0-AC_6 to Latch Outputs (PR_0-PR_2)		21	32		21	50	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (mA_0-mA_8, FO, PR_0-PR_2		17	26		17	35	ns
t_{FI}	Propagation Delay from Control Inputs AC_0-AC_6 to Interrupt Strobe Enable Output (ISE)		20	32		20	40	ns

NOTE
1. Typical values are for TA = 25°C and 5.0 supply voltage
2. S3001: tCY = tWP + tSF + tCO

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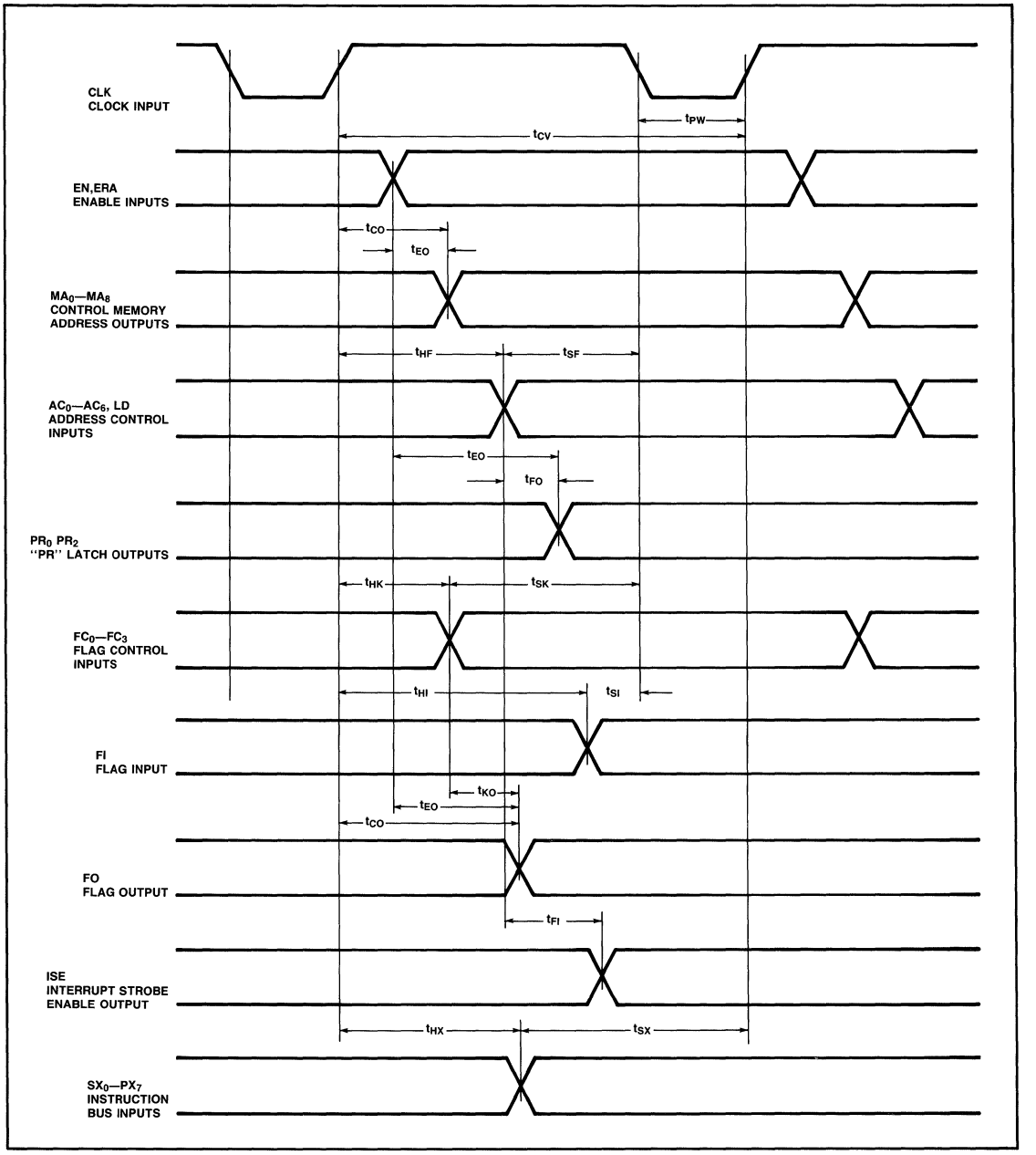
VOLTAGE WAVEFORMS



CENTRAL PROCESSING ELEMENT

S/N3002

FEATURES

- **45ns cycle time (typ)**
- **Easy expansion to multiple of 2 bits**
- **11 general purpose registers**
- **Full function accumulator**
- **Useful functions include:**
  - **2's complement arithmetic**
  - **Logical AND, OR, NOT, exclusive-NOR**
  - **Increment, decrement**
  - **Shift left/shift right**
  - **Bit testing and zero detection**
  - **Carry look-ahead generation**
  - **Masking via K-bus**
  - **Conditioned clocking allowing non-destructive testing of data in accumulator and scratchpad**
- **3 input buses**
- **2 output buses**
- **Control bus**

DESCRIPTION

The N3002 Central Processing Element (CPE) is one part of a bipolar microcomputer set. The N3002 is organized as a 2-bit slice and performs the logical and arithmetic functions required by microinstructions. A system with any number of bits in a data word can be implemented by using multiple N3002s, the N3001 microcomputer control unit, the N74S182 carry look-ahead unit and ROM or PROM memory

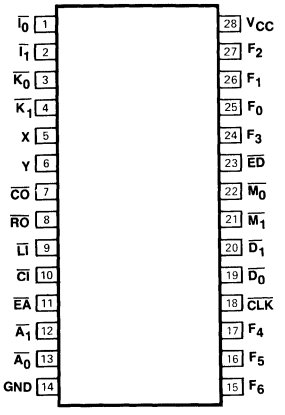
FUNCTION TRUTH TABLE

FUNCTION GROUP	F_6	F_5	F_4
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

REGISTER GROUP	REGISTER	F_3	F_2	F_1	F_0
I	R_0	0	0	0	0
	R_1	0	0	0	1
	R_2	0	0	1	0
	R_3	0	0	1	1
	R_4	0	1	0	0
	R_5	0	1	0	1
	R_6	0	1	1	0
	R_7	0	1	1	1
	R_8	1	0	0	0
	R_9	1	0	0	1
	T	1	1	0	0
	AC	1	1	0	1
II	T	1	0	1	0
	AC	1	0	1	1
III	T	1	1	1	0
	AC	1	1	1	1

PIN CONFIGURATION

I,XL PACKAGE

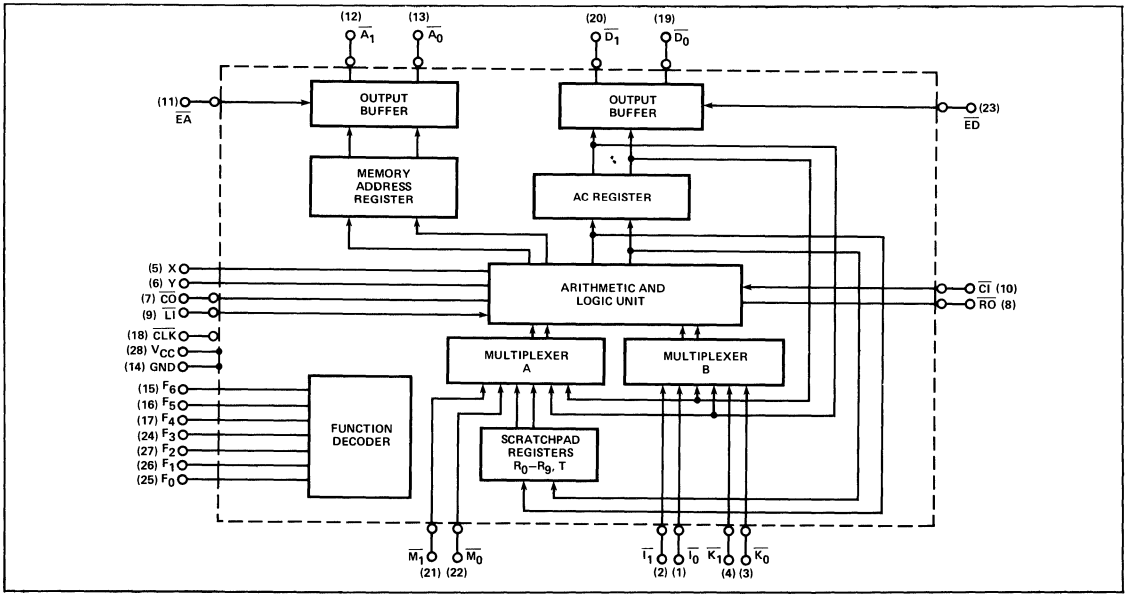


TOP VIEW

ORDER NUMBERS

S3002-I, N3002-I, XL

BLOCK DIAGRAM



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CENTRAL PROCESSING ELEMENT S/N3002

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1, 2	$I_0 - I_1$	External Bus Input The external bus inputs provide a separate input port for external input devices.	Active low
3, 4	$K_0 - K_1$	Mask Bus Inputs The mask bus inputs provide a separate input port from the microprogram memory, to allow mask or constant entry	Active low
5, 6	X, Y	Standard Carry Look-Ahead Cascade Outputs The cascade outputs allow high speed arithmetic operations to be performed when they are used in conjunction with the 74S182 Look-Ahead Carry Generator	Active high
7	CO	Ripple Carry Out The ripple carry output is only disabled during shift right operations.	Active low Three-state
8	RO	Shift Right Output The shift right output is only enabled during shift right operations.	Active low Three-state
9	LI	Shift Right Input	Active low
10	CI	Carry Input	Active low
11	EA	Memory Address Enable Input When in the low state, the memory address enable input enables the memory address outputs ($A_0 - A_1$).	Active low
12-13	$A_0 - A_1$	Memory Address Bus Outputs The memory address bus outputs are the buffered outputs of the memory address register (MAR).	Active low Three-state
14	GND	Ground	
14-17 24-27	$F_0 - F_6$	Micro-Function Bus Inputs The micro-function bus inputs control ALU function and register selection.	Active high
18	CLK	Clock Input	
19-20	$D_0 - D_1$	Memory Data Bus Outputs The memory data bus outputs are the buffered outputs of the full function accumulator register (AC).	Active low Three-state
21-22	$M_0 - M_1$	Memory Data Bus Inputs The memory data bus inputs provide a separate input port for memory data.	Active low
23	ED	Memory Data Enable Input When in the low state, the memory data enable input enables the memory data outputs ($D_0 - D_1$).	Active low
28	V_{CC}	+5 Volt Supply	

SYSTEM DESCRIPTION

Microfunction Decoder and K-Bus

Basic microfunctions are controlled by a 7-bit bus (F_0-F_6) which is organized into 2 groups. The higher 3 bits (F_4-F_6) are designated as F-Group and the lower 4 bits (F_0-F_3) are designated as the R-Group The F-Group specifies the type of operation to be performed and the R-Group specifies the registers involved.

The F-Bus instructs the microfunction decoder to:
- Select ALU functions to be performed
- Generate scratchpad register address
- Control A and B multiplexer

The resulting microfunction action can be:
- Data transfer
- Shift operations
- Increment and decrement
- Initialize stack
- Test for zero conditions
- 2's complement addition and subtraction
- Bit masking
- Maintain program counter

A and B Multiplexers

A and B multiplexers select the proper 2 operands to the ALU.

A multiplexer selects inputs from one of the following:
- M-bus (data from main memory)
- Scratchpad registers
- Accumulator

B multiplexer selects inputs from one of the following:
- I-bus (data from external I/O devices)
- Accumulator
- K-bus (literal or masking information from micro-program memory)

Scratchpad Registers

- Contains 11 registers (R_0-R_9, T)
- Scratchpad register outputs are multiplexed to the ALU via the A multiplexer
- Used to store intermediate results from arithmetic/logic operations
- Can be used as program counter

Arithmetic/Logic Unit (ALU)

The ALU performs the arithmetic and logic operations of the CPE.

Arithmetic operations are:
- 2's complement addition
- Incrementing
- Decrementing
- Shift left
- Shift right

Logical operations are:
- Transfer
- AND
- Inclusive-OR
- Exclusive-NOR
- Logic complement

ALU operation results are then stored in the accumulator and/or scratchpad registers. For easy expansion to larger arrays carry look-ahead outputs (X and Y) and cascading shift inputs (LI, RO) are provided.

Accumulator

- Stores results from ALU operations
- The output of accumulator is multiplexed into ALU via the A and B multiplexer as one of the operands

Input Buses

M-bus: Data bus from main memory

- Accepts 2 bits of data from main memory into CPE
- Is multiplexed into the ALU via the A multiplexer

I-bus: Data bus from input/output devices

Accepts 2 bits of data from external input/output devices into CPE

- Is multiplexed into the ALU via the B multiplexer

K-bus: A special feature of the N3002 CPE

- During arithmetic operations, the K-bus can be used to **mask** portions of the field being operated on
- Select or remove accumulator from operation by placing K-bus in all "1" or all "0" state respectively
- During non-arithmetic operation, the carry circuit can be used in conjunction with the K-bus for word-wise-OR operation for bit testing
- Supply literal or constant data to CPE

Output Buses

A-bus and Memory Address Register

- Main memory address is stored in the memory address register (MAR)
- Main memory is addressed via the A-bus
- MAR and A-bus may also be used to generate device address when executing I/O instructions
- A-bus has Tri-State outputs

D-bus: Data bus from CPE to main memory or to I/O devices

- Sends buffered accumulator outputs to main memory or the external I/O devices
- D-bus has Tri-State outputs

FUNCTION DESCRIPTION

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
0	I *	XX	—	$R_n + (AC\ K) + CI \rightarrow R_n, AC$	**Logically AND AC with K-bus.** Add the result to R_n and carry input (CI). Deposit the sum in AC and R_n.
		OO	ILR	$R_n + CI \rightarrow R, AC$	Conditionally increment R_n and load the result in AC. Used to load AC from R_n or to increment R_n and load a copy of the results in AC.
		11	ALR	$AC + R_n + CI \rightarrow R_n, AC$	Add AC and CI to R_n and load the result in AC. Used to add AC to a register. If R_n is AC, then AC is shifted left one bit position.
0	II	XX	—	$M + (AC\ K) + CI \rightarrow AT$	**Logically AND AC with the K-bus.** Add the result to CI and the M-bus. Deposit the sum in AC or T.
		OO	ACM	$M + CI \rightarrow AT$	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		11	AMA	$M + AM + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.
0	III	XX	—	$AT_L \vee (\overline{I_L \wedge K_L}) \rightarrow RO$ $LI \vee [(I_H \wedge K_H) \wedge AT_H] \rightarrow AT_H$ $[AT_L \wedge (I_L \wedge K_L)]$ $[AT_H \vee (I_H \wedge K_H)] \rightarrow AT_L$	None
		OO	SRA	$AT_L \rightarrow RO$ $AT_H \rightarrow AT_L$ $L_I \rightarrow AT_H$	Shift AC or T, as specified, right one bit position. Place the previous low order bit value on RO and fill the high order bit from the data on LI Used to shift or rotate AC or T right one bit.
1	I	XX	—	$K \vee R_n \rightarrow MAR$ $R_n + K + CI \rightarrow R_n$	**Logically OR R_n with the K-bus.** Deposit the result in MAR. Add the K-bus to R_n and CI. Deposit the result in R_n.
		OO	LMI	$R_n \rightarrow MAR m\ R_n + CI \rightarrow R_n$	Load MAR from R_n. Conditionally increment R_n. Used to maintain a macro-instruction program counter.
		11	DSM	$11 \rightarrow MAR, R_n - 1 + CI \rightarrow R_n$	Set MAR to all ones. Conditionally decrement R_n by one. Used to force MAR to its highest address and to decrement R_n.
1	II	XX	—	$KVM \rightarrow MAR$ $M + K + CI \rightarrow AT$	**Logically OR the M-bus with the K-bus.** Deposit the result in MAR. Add the K-bus to the M-bus and CI. Deposit the sum in AC or T.
		OO	LMM	$M \rightarrow MAR, M + CI \rightarrow AT$	Load MAR from the M-bus. Add CI to the M-bus. Deposit the result in AC or T. Used to load the address register with memory data for macro-instructions using indirect addressing.
		11	LDM	$11 \rightarrow MAR$ $M - 1 + CI \rightarrow AT$	Set MAR to all ones. Subtract one from the M-bus. Add CI to the difference and deposit the result in AC or T, as specified. Used to load decremented memory data in AC or T.

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FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
1	III	XX	—	$(\overline{AT} \vee K) + (AT \wedge K) + CI \rightarrow AT$	**Logically OR the K-bus with the complement of AC or T, as specified.** Add the result to the logical AND of specified register with the K-bus. Add the sum to CI. Deposit the result in the specified register.
		OO	CIA	$\overline{AT} + CI \rightarrow AT$	Add CI to the complement of AC or T, as specified. Deposit the result in the specified register. Used to form the 1's or 2's complement of AC or T.
		11	DCA	$\overline{AT} - 1 + CI \rightarrow AT$	Subtract one from AC or T, as specified. Add CI to the difference and deposit the sum in the specified register. Used to decrement AC or T.
2	I	XX	—	$(AC \wedge K) - 1 + CI \rightarrow R_n$	**Logically AND the K-bus with AC.** Subtract one from the result and add the difference to CI. Deposit the sum in R_n.
		OO	CSR	$CI - 1 \rightarrow R_n$ (See Note 1)	Subtract one from CI and deposit the difference in R_n. Used to conditionally clear or set R_n to all 0's or 1's, respecitively
		11	SDR	$AC - 1 + CI \rightarrow R_n$ (See Note 1)	Subtract one from AC and add the difference to CI. Deposit the sum in R_n. Used to store AC in R_n, or to store the decremented value of AC in R_n.
2	II	XX	—	$(AC \wedge K) - 1 + CI \rightarrow AT$ (See Note 1)	**Logically AND the K-bus with AC.** Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CSA	$CI - 1 \rightarrow AT$ (See Note 1)	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		11	SDA	$AC - 1 + CI \rightarrow AT$ (See Note 1)	Subtract one from AC and add the difference to CI. Deposit the sum in AC or T. Used to store AC in T, or decrement AC, or store the decremented value of AC in T.
2	III	XX	—	$(I \wedge K) - 1 + CI \rightarrow AT$ (See Note 1)	**Logically AND the data of the K-bus with the data on the I-bus.** Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CSA	$CI - 1 \rightarrow AT$	Subtract one from CI and deposit the difference in AC or T Used to conditionally clear or set AC or T
		11	LDI	$I - 1 + CI \rightarrow AT$	Subtract one from the data on the I-bus and add the difference to CI. Deposit the sum in AC or T, as specified Used to load input bus data or decremented input bus data in the specified register.
3	I	XX	—	$R_n + (AC \wedge K) + CI \rightarrow R_n$	**Logically AND AC with the K-bus.** Add R_n and CI to the result. Deposit the sum in R_n.
		OO	INR	$R_n + CI \rightarrow R_n$	Add CI to R_n and deposit the sum in R_n Used to increment R_n.
		11	ADR	$AC + R_n + CI \rightarrow R_n$	Add AC to R_n Add the result to CI and deposit the sum in R_n. Used to add the accumulator to a register or to add the incremented value of the accumulator to a register
3	II	XX	—	$M + (AC \wedge K) + CI \rightarrow AT$	**Logically AND AC with the K-bus.** Add the result to CI and the M-bus. Deposit the sum in AC or T.
		OO	ACM	$M + CI \rightarrow AT$	Add CI to M-bus Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		11	AMA	$M + AC + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register

NOTE
1. 2's complement arithmetic adds 111 11 to perform subtraction of 000 01

FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
3	III	XX	—	AT + (I ∧ K) + CI→AT	**Logically AND the K-bus with the I-bus.** Add CI and the contents of AC or T, as specified, to the result. Deposit the sum in the specified register.
		OO	INA	AT + CI→AT	Conditionally increment AC or T. Used to increment AC or T.
		11	AIA	I + AT + CI→AT	Add the I-bus to AC or T. Add CI to the result and deposit the sum in the specified register. Used to add input data or incremented input data to the specified register.
4	I	XX	—	CI ∨ (R_n ∧ AC ∧ K)→CO R_n ∧ (AC ∧ K)→R_n	**Logically AND the K-bus with AC.** Logically AND the result with the contents of R_n. Deposit the final result in R_n. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on the carry output (CO) line.
		OO	CLR	CI→CO, O→R_n	Clear R_n to all O's. Force CO to CI. Used to clear a register and force CO to CI.
		11	ANM	CI ∨ (R_n ∧ AC)→CO R_n ∧ AC→R_n	Logically AND AC with R_n. Deposit the result in R_n. Force CO to one if the result is non-zero. Used to AND the accumulator with a register and test for a zero result.
4	II	XX	—	CI ∨ (M ∧ AC ∧ K)→CO M ∧ (AC ∧ K)→AT	**Logically AND the K-bus with AC.** Logically AND the result with The M-bus. Deposit the final result in AC ot T. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on CO.
		OO	CLA	CI→CO, O→AT	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	ANM	CI ∨ (M ∧ AC)→CO M ∧ AC→AT	Logically AND the M-bus with AC. Deposit the result in AC or T. Force CO to one if the result is non-zero. Used to AND the M-bus data to the accumulator and test for a zero result.
4	III	XX	—	CI ∨ (AT ∧ 1 ∧ K)→CO AT ∧ (I ∧ K)→AT	**Logically AND the I-bus with the K-bus.** Logically AND the result with AC or T. Deposit the final result in the specified register. Logically OR CI with the word-wise OR of the final result. Place the value of the carry OR on CO.
		OO	CLA	CI→CO, O→AT	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	ANI	CI ∨ (AT ∧ I)→CO AT ∧ 1→AT	Logically AND the I-bus with AC or T, as specified. Deposit the result in the specified register. Force CO to one if the result is non-zero. Used to AND the I-bus to the accumulator and test for a zero result.
5	I	XX	—	CI ∨ (R_n ∧ K)→CO K ∧ R_n→R_n	**Logically AND the K-bus with R_n.** Deposit the result in R_n. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLR	CI→CO, O→R_n	Clear R_n to all O's. Force CO to CI. Used to clear a register and force CO to CI.
		11	TZR	CI ∨ R_n→CO R_n→R_n	Force CO to one if R_n is non-zero. Used to test a register for zero. Also used to AND K-bus data with a register for masking and, optionally, testing for a zero result.
5	II	XX	—	CI ∨ (M ∧ K)→CO K ∧ M→AT	**Logically AND the K-bus with the M-bus.** Deposit the result in AC or T, as specified. Logically OR CI with the work-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLA	CI→CO, O→AT	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	LTM	CI ∨ M→CO M→AT	Load AC or T, as specified, from the M-bus. Force CO to one if the result is non-zero. Used to load the specified register from memory and test for zero result. Also used to AND the K-bus with the M-bus for masking and, optionally, testing for a zero result.

FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
5	III	XX	—	$CI \vee (AT \wedge K) \rightarrow CO$ $K \wedge AT \rightarrow AT$	**Logically AND the K-bus with AC or T, as specified.** Deposit the result in the specified register. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLA	$CI \rightarrow CO$, $O \rightarrow AT$	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	TZA	$CI \vee AT \rightarrow CO$ $AT \rightarrow AT$	Force CO to one if AC or T, as specified, is non-zero. Used to test the specified register for zero. Also used to AND the K-bus to the specified register for masking and, optionally, testing for a zero result.
6	I	XX	—	$CI \vee (AC \wedge K) \rightarrow CO$ $R_n \vee (AC \wedge K) \rightarrow R_n$	**Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus.** Place the result of the carry OR on CO. Logically OR R_n with the logical AND of AC and the K-bus. Deposit the result in R_n.
		OO	NOP	$CI \rightarrow CO$, $R_n \rightarrow R_n$	Force CO to CI. Used as a null operation or to force CO to CI.
		11	ORR	$CI \vee AC \rightarrow CO$ $R_n \vee AC \rightarrow R_n$	Force CO to one if AC is non-zero. Logically OR AC with R_n. Deposit the result in R_n. Used to OR the accumulator to a register and, optionally, test the previous accumulator value for zero.
6	II	XX	—	$CI \vee (AC \wedge K) \rightarrow CO$ $M \vee (AC \wedge K) \rightarrow AT$	**Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus.** Place the carry OR on CO. Logically OR the M-bus, with the logical AND of AC and the K-bus. Deposit the final result in AC or T.
		OO	LMF	$CI \rightarrow CO$, $M \rightarrow AT$	Load AC or T, as specified, from the M-bus. Force CO to CI. Used to load the specified register with memory data and force CO to Ci.
		11	ORM	$CI \vee AC \rightarrow CO$ $M \vee AC \rightarrow AT$	Force CO to one if AC is non-zero. Logically OR the M-bus with AC. Deposit the result in AC or T, as specified. Used to OR M-bus with the AC and, optionally, test the previous value of AC for zero.
6	III	XX	—	$CI \vee (I \wedge K) \rightarrow CO$ $AT \vee (I \wedge I) \rightarrow AT$	**Logical OR CI with the word-wise OR of the logical AND of the I-bus and the K-bus.** Place the carry OR on CO. Logically AND the K-bus with the I-bus. Logically OR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	NOP	$CI \rightarrow CO$, $AT \rightarrow AT$	Force CO to CI. Used as a null operation or to force CO to CI.
		11	ORI	$CI \vee I \rightarrow CO$ $I \vee AT \rightarrow$	Force CO to one if the data on the I-bus is non-zero. Logically OR the I-bus to AC or T, as specified. Deposit the result in the specified register. Used to OR I-bus data with the specified register and, optionally, test the I-bus data for zero.
7	I	XX	—	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$ $R_n \bar{\oplus} (AC \wedge K) \rightarrow R_n$	**Logically OR CI with the word-wise OR of the logical AND of R_n and AC and the K-bus.** Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive-NOR the result with R_n. Deposit the final result in R_n.
		OO	CMR	$CI \rightarrow CO$, $R_n \rightarrow R_n$	Complement the contents of R_n. Force CO to CI.
		11	XNR	$CI \quad (R_n \vee AC) \rightarrow CO$ $R_n \bar{\oplus} AC \rightarrow R_n$	Force CO to one if the logical AND of AC and R_n is non-zero. Exclusive-NOR AC with R_n. Deposit the result in R_n. Used to exclusive-NOR the accumulator with a register.

FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
7	II	XX	—	CI ∨ (M ∧ AC ∧ K)→CO M ⊕̄ (AC ∧ K)→AT	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus and M-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive NOR the result with the M-bus. Deposit the final result in AC or T.
		OO	LCM	CI→CO, $\overline{M}$→AT	Load the complement of the M-bus into AC or T, as specified. Force CO to CI.
		11	XNM	CI (M ∧ AC)→CO M ⊕̄ AC→AT	Force CO to one if the logcal AND of AC and the M-bus is non-zero. Exclusive-NOR AC with the M-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR memory data with the accumulator.
7	III	XX	—	CI ∨ (AT ∧ I ∧ K)→CO AT⊕̄ (I ∧ K)→AT	Logically OR CI with the word-wise OR of the logical AND of the specified register and the I-bus and K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Exclusive-NOR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	CMA	CI→CO $\overline{AT}$→AT	Complement AC or T, as specified. Force CO to CI.
		11	XNI	CI ∨ (AT ∧ I)→CO I ⊕̄ AT→AT	Force CO to one if the logical AND of the specified register and the I-bus is non-zero. Exclusive-NOR AC with the I-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR input data with the accumulator.

FUNCTION DESCRIPTION KEY

SYMBOL	MEANING
I,K,M	Data on the I, K, and M buses, respectively
CI,LI	Data on the carry input and left input, respectively
CO,RO	Data on the carry output and right output, respectively
R_n	Contents of register n including T and AC (R-Group I)
AC	Contents of the accumulator
AT	Contents of AC or T, as specified
MAR	Contents of the memory address register
L,H	As subscripts, designate low and high ordr bit, respectively
+	2's complement addition
−	2's complement subtraction
∧	Logical AND
∨	Logical OR
⊕	Exclusive-NOR
→	Deposit into

6

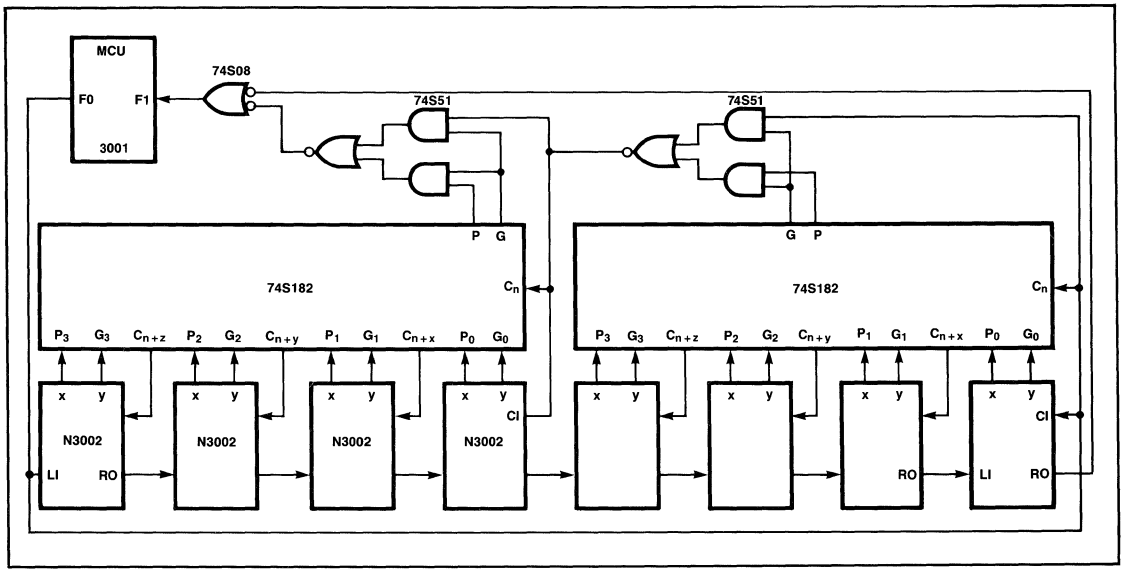
AC ELECTRICAL CHARACTERISTICS

N3001 = T_A = 0°C to +70°C, V_{CC} = 5V ± 5%
S3001 = T_A = −55°C to +125°C, V_{CC} = 5V ±10%

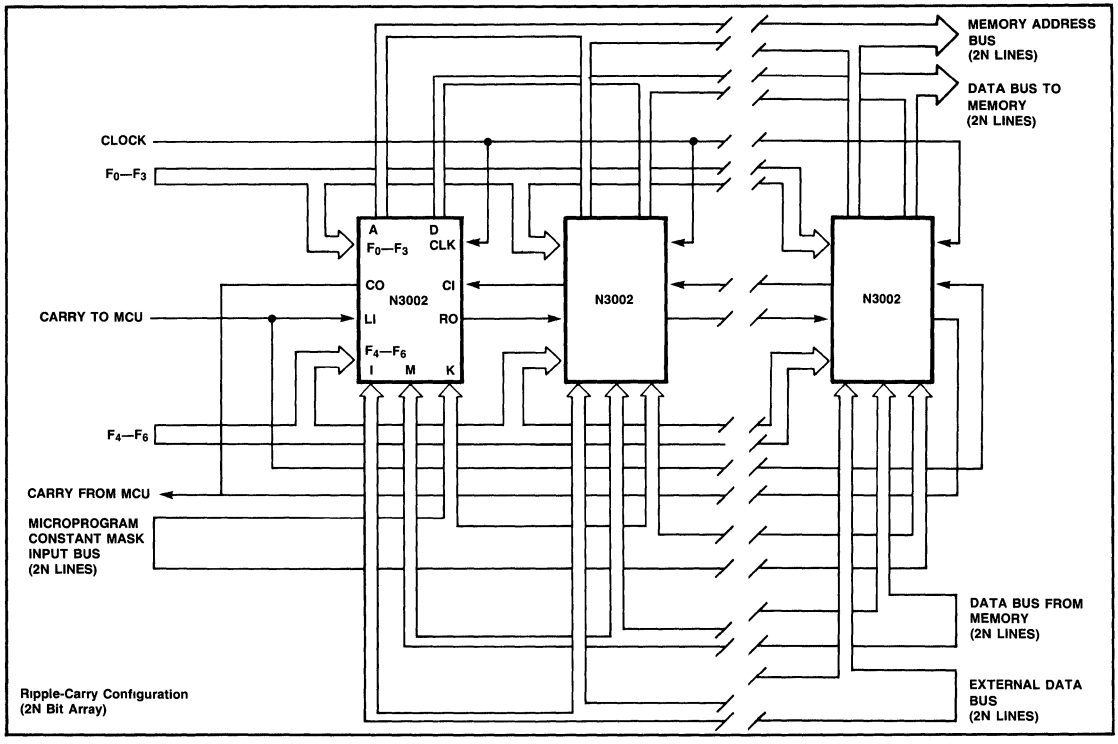
PARAMETER		N3002			S3002			UNIT
		Min	Typ*	Max	Min	Typ*	Max	
tCY	Clock Cycle Time	70	45		120	45		ns
tWP	Clock Pulse Width	17	10		42	10		ns
tFS	Function Input Set-Up Time (F_0 through F_6)	48	−23→35		70	−23→35		ns
Data Set-Up Time:								
tDS	I_0, I_1, M_0, M_1, K_0, K_1	40	12→29		60	12→29		ns
tSS	LI, CI	21	0→7		30	0→7		ns
Data and Function Hold Time:								
tFH	F_0 through F_6	4	0		5	0		ns
tDH	I_0, I_1, M_0, M_1, K_0, K_1	4	−28→−11		5	−28→−11		ns
tSH	LI, CI	12	−7→0		15	−7→0		ns
Propagation Delay to X, Y, RO from:								
tXF	Any Function Input		28	52		28	65	ns
tXD	Any Data Input		16→20	33		16→20	65	ns
tXT	Trailing Edge of CLK		33	48		33	75	ns
tXL	Leading Edge of CLK	13	18→40	70	13	18→40	90	ns
Propagation Delay to CO from:								
tCL	Leading Edge of CLK	16	24→44	70		24→44	90	ns
tCL	Trailing Edge of CLK		30→40	56		30→40	100	ns
tCF	Any Function Input		25→35	52		25→35	75	ns
tCD	Any Data Input		17→23	55		17→23	65	ns
tCC	CI (Ripple Carry)		9→13	20		9→13	30	ns
Propagation Delay to A_0, A_1, D_0, D_1 from:								
tDL	Leading Edge of CLK		17→25	40		17→25	75	ns
tDE	Enable Input ED, EA		10→12	20		10→12	35	ns

*NOTE
Typical values are for T_A = 25°C and typical supply voltage.

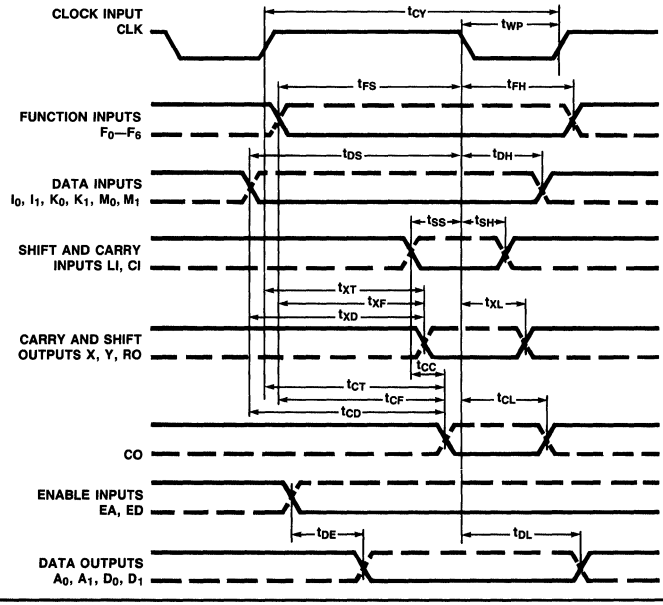
CARRY LOOK-AHEAD CONFIGURATION



TYPICAL CONFIGURATIONS



VOLTAGE WAVEFORMS



CONTROL STORE SEQUENCER 8X02A

FEATURES

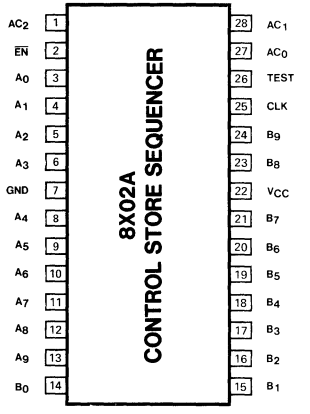
- **10-Bit Address Generator (1024 Microinstruction Addressability)**
- **Operating Frequency Exceeding 12 MHz**
- **Direct Branching Over Full Address Range**
- **Conditional Branching**
- **Subroutine Branching Capability**
- **4-Level Stack Register File**
- **Loop Control Facility Using Stack**
- **Three-State Address Outputs**

PRODUCT DESCRIPTION

The Signetics 8X02A Control Store Sequencer generates addresses to access instructions from a microprogram memory (control store). This high-speed device provides an efficient means of controlling the flow through a microprogram with a powerful set of sequencing functions. The 8X02A can directly address up to 1024 microinstructions; however, the total address space can be expanded by adding conventional paging techniques. Combined with memory, the 8X02A forms a powerful control section for CPU's, controllers, test equipment, and other microprogram-controlled systems.

8X02A PACKAGE AND PIN DESIGNATIONS

N PACKAGE



TOP VIEW

ORDER NUMBER

N8X02AN

PIN NO.	IDENTIFIER	FUNCTION
1, 28, 27	AC_2-AC_0	Inputs used to select any one of eight Address Control Functions—see Table 1.
2	$\overline{EN}$	Enable three-state address outputs (A_0-A_9); active-low input.
3-6, 8-13	A_0-A_9	Three-state address outputs used to specify microprogram address; (A_0 = LSB, A_9 = MSB).
7	GND	Ground.
14-21, 23, 24	B_0-B_9	Branch address inputs: (B_0 = LSB, B_9 = MSB).
22	V_{CC}	Supply voltage.
25	CLK	Clock input (positive edge used for all triggering).
26	TEST	Active-high condition input used to determine conditional skips, branches, subroutine calls, and loop termination.

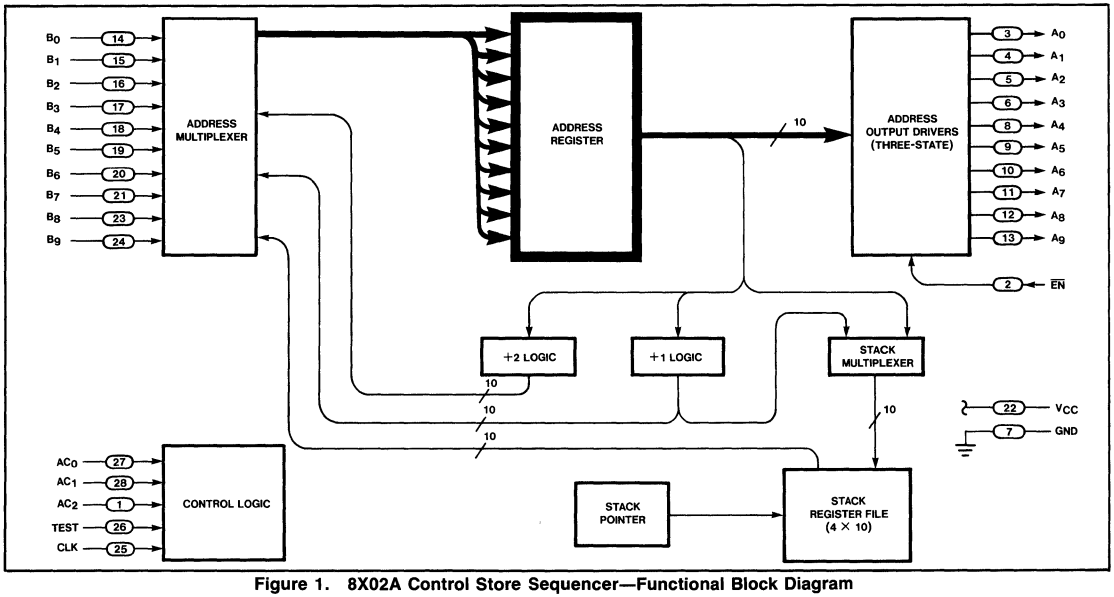


Figure 1. 8X02A Control Store Sequencer—Functional Block Diagram

FUNCTIONAL OPERATION

As shown in Figure 1, the data appearing on the address output pins (A_0-A_9) is the contents of the 10-bit Address Register. On the rising edge of the clock input pulse (CLK), a new address is latched into the Address Register. This new address is supplied via the Address Multiplexer which selects one of five sources:

- Branch Address Input (B_0-B_9)
- Current Address + 1
- Current Address + 2 (for the SKIP function)
- Stack Register File (most recent entry)
- All Zeroes (RESET)

The selection of the next address is determined by the "Address Control Function" specified by inputs AC_0-AC_2 and the TEST input. Table 1 defines the eight Address Control Functions.

The "Reset" (RST) Address Control Function unconditionally forces all Address Register bits to zero on the rising edge of CLK. Sequential microprogram flow is provided by the "Increment" (INC) function which unconditionally increments the Address Register by one for each clock cycle. The Address Register automatically wraps around from the highest address (all "1s") to the lowest address (all "0s").

As shown in Table 1, the TEST input is used to conditionally execute four of the eight Address Control Functions. If the TEST input is *low* (false), the Address Register is simply incremented by one—(for the BLT function, the Stack Pointer is also decremented). If the TEST input is *high* (true), the sequencer executes one of the following:

- Skip (TSK)—the Address Register is incremented by two.
- Branch (BRT)—the Address Register is loaded from the Branch Address Inputs.
- Branch-to-Subroutine (BSR).
- Branch-to-Loop (BLT).

The Stack Register File holds up to four 10-bit addresses and operates in the Last-In/First-Out (LIFO) mode. A Stack Pointer keeps track of the next register of the Stack File to be written into; the pointer is incremented after each "push" and decremented after each "pop"—see Table 1. When branching to a subroutine (BSR), the return address (current address + 1) is "pushed" onto the stack and the branch address input is loaded into the Address Register. To return from a subroutine, the "POP" function pops the return address off the stack and loads it into the Address Register.

The "Push-for-Looping" (PLP) function may be specified in the first instruction of a loop to "push" the current address onto the stack; the Address Register is incremented. A "Branch-to-Loop" (BLT) function placed at the end of the loop "pops" the stack and conditionally branches to the top-of-loop address, depending on the TEST input. If the test for repeating the loop is satisfied (TEST input *high*), the sequencer causes a branch back to the first instruction of the loop in which the top-of-loop address is "pushed" back onto the stack. If the test fails (TEST input *low*), the top-of-loop address is discarded, the stack pointer is decremented and the Address Register is incremented. A combination of subroutines and loops may be nested up to four levels deep.

In abnormal circumstances, the Stack Pointer will wraparound from the fourth to the first register of the Stack File and vice-versa. If the stack is full (four addresses currently stored), an additional "push" causes the first (oldest) entry to be overwritten—(the four most recent entries are always maintained). If the stack is empty, a "pop" will access the fourth register of the Stack File; however, the contents of this register may be unpredictable.

The three-state address outputs (A_0-A_9) are controlled by a common enable input ($\overline{EN}$). When the enable input is *high*, the output drivers are placed in the high-impedance state allowing alternative access to the microprogram memory. Other circuit functions are unaffected by $\overline{EN}$.

Note

To implement a RESET externally it is necessary to force all Address Control Inputs (AC_0-AC_2) to the *high* state until at least one rising edge of CLK has occurred. If the AC inputs are supplied directly from the microprogram memory, a RESET may be accomplished by disabling the memory outputs. Pullup resistors should be provided to achieve the required high voltage level.

Table 1. ADDRESS CONTROL FUNCTIONS

MNEMONIC AND DESCRIPTION	CONTROL LINES AC_2	AC_1	AC_0	TEST	NEXT ADDRESS	STACK OPERATION	STACK POINTER
TSK — Test and skip	0	0	0	0	Current address + 1	No change	No change
	0	0	0	1	Current address + 2	No change	No change
INC — Increment	0	0	1	X	Current address + 1	No change	No change
BLT — Branch to Loop if	0	1	0	0	Current address + 1	POP (Ignore data)	Decrement by 1
Test Condition is True	0	1	0	1	From stack register file	POP (Read)	Decrement by 1
POP — Pop stack (Return from subroutine)	0	1	1	X	From stack register file	POP (Read)	Decrement by 1
BSR — Branch to Subroutine if	1	0	0	0	Current address + 1	No change	No change
Test Condition is True	1	0	0	1	Branch address inputs B_0-B_9	PUSH (Write current address + 1)	Increment by 1
PLP — Push for Looping	1	0	1	X	Current address + 1	PUSH (Write current address)	Increment by 1
BRT — Branch if Test Condition	1	1	0	0	Current address + 1	No change	No change
is True	1	1	0	1	Branch address inputs B_0-B_9	No change	No change
RST — Reset Address to Zero	1	1	1	X	All zeroes	No change	No change

X = Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_O	Off-State output voltage	+5.5	Vdc
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

CONDITIONS:

Commercial—

V_{CC} = 5.0V (±5%)

$0°C \leq T_A \leq 70°C$

PARAMETER	DESCRIPTION	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP[1]	MAX	
V_{IH}	High Level Input Voltage	V_{CC} = Min	2			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min			0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min; I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min; I_{OH} = −2.6 mA	2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min; I_{OL} = 8 mA		0.42	0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC}= Max; V_I = 5.5V		1	100	µA
I_{IH}	High Level Input Current: AC_2-AC_0, TEST, CLK	V_{CC} = Max; V_{IH} = 2.7V		<0.1	40	µA
	B_9-B_0, $\overline{EN}$			<0.1	20	µA
I_{IL}	Low Level Input Current: AC_2-AC_0, TEST, CLK	V_{CC} = Max; V_{IL} = 0.4V		−24	−800	µA
	B_9-B_0, $\overline{EN}$			−12	−400	µA
I_{OS}	Short Circuit Output Current[2]	V_{CC} = Max	−15	−60	−100	mA
I_{OZH}	High-Z State Output Current—High Level	V_{CC} = Max; V_{OH} = 2.7V			20	µA
I_{OZL}	High-Z State Output Current—Low Level	V_{CC} = Max; V_{OL} = 0.4V			−20	µA
I_{CC}	Supply Current	V_{CC} = Max		170	250	mA

NOTES:

1 Typical limits are V_{CC} = 5.0V and T_A = 25°C

2 For purposes of testing, not more than one output should be shorted at a time

AC ELECTRICAL CHARACTERISTICS

CONDITIONS:

Commercial—
V_{CC} = 5.0V (±5%)
0°C ≤ T_A ≤ 70°C

Loading—
See TEST LOADING CIRCUIT

PARAMETERS[1]	REFERENCES FROM	REFERENCES TO	LIMITS[4] MIN	LIMITS[4] TYP[2]	LIMITS[4] MAX	UNITS
Pulse Width:						
t_{CW} — Clock cycle time	↑CLK	↑CLK	80			ns
t_{PWH} — Clock high	↑CLK	↓CLK	35	24		ns
t_{PWL} — Clock low	↓CLK	↑CLK	15	9		ns
Propagation Delay:						
t_{PLZ} — Low to High-Z	↑$\overline{EN}$	A_0-A_9		14	20	ns
t_{PHZ} — High to High-Z	↑$\overline{EN}$	A_0-A_9		35	42	ns
t_{PZL} — High-Z to Low	↓$\overline{EN}$	A_0-A_9		10	20	ns
t_{PZH} — High-Z to High	↓$\overline{EN}$	A_0-A_9		20	30	ns
t_{PHL} — High to Low	↑CLK	↓A_0-A_9		25	45	ns
t_{PLH} — Low to High	↑CLK	↑A_0-A_9		25	45	ns
t_{HA} — Address output hold time[3]	↑CLK	A_0-A_9	13			ns
Set-Up/Hold Times:						
t_{SF} — Function set-up time	AC_0-AC_2	↑CLK	20	18		ns
t_{SK} — Branch set-up time	B_0-B_9	↑CLK	15	7		ns
t_{SI} — Test set-up time	TEST	↑CLK	20	15		ns
t_{HF} — Function hold time	↑CLK	AC_0-AC_2	20	2		ns
t_{HK} — Branch hold time	↑CLK	B_0-B_9	15	9		ns
t_{HI} — Test hold time	↑CLK	TEST	12	−2		ns

NOTES

1. Parameter definitions are illustrated in the Timing Diagrams—See Figure 2
2. Typical limits are V_{CC} = 5.0V and T_A = 25°C.
3. t_{HA} is the minimum time the current address outputs remain stable before changing. This delay may be used to provide some of the hold times required for the AC, B, and TEST inputs, if these inputs are determined by the microprogram memory addressed by the 8X02A
4. This data supersedes the November, 1980 edition of this data sheet

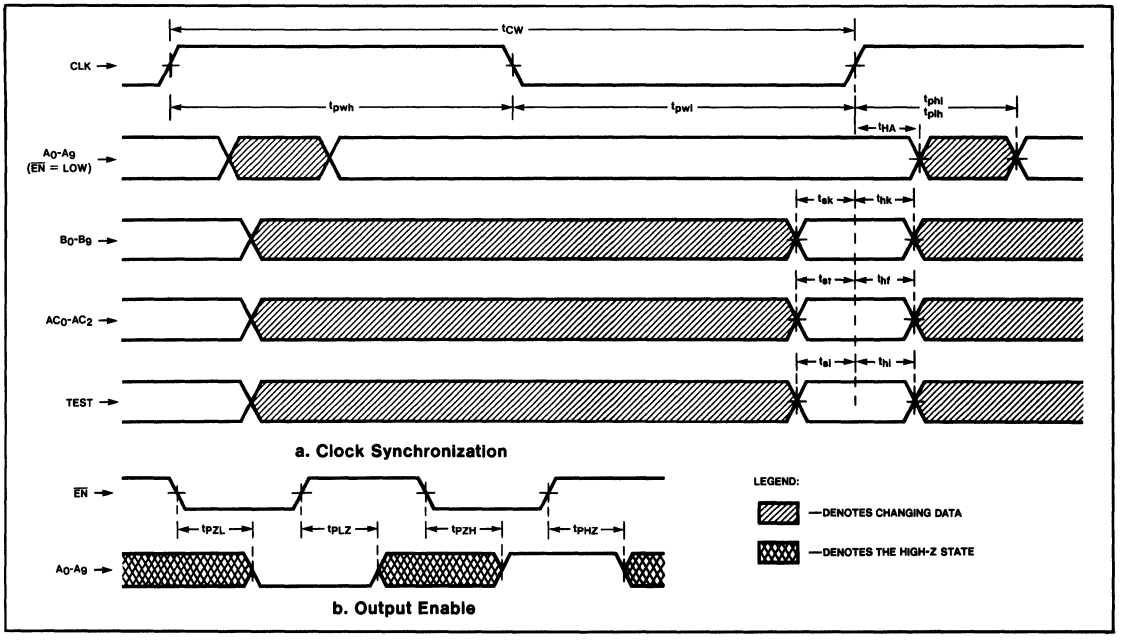
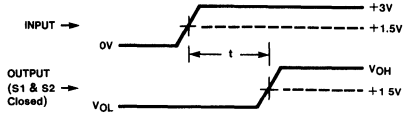


Figure 2. Timing Diagrams

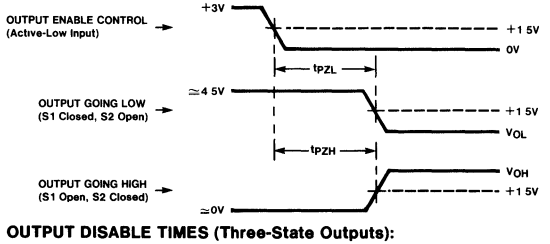
AC VOLTAGE WAVEFORMS and TEST LOADING

PROPAGATION DELAY (Typical Example):

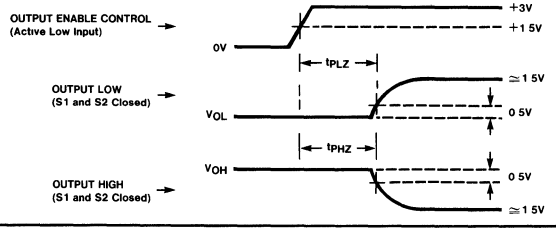


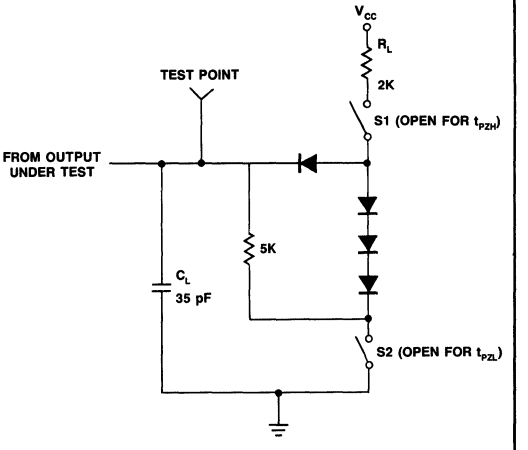
Pulse widths and setup/hold times are measured using the same reference points shown in the above waveforms

OUTPUT ENABLE TIMES (Three-State Outputs):



OUTPUT DISABLE TIMES (Three-State Outputs):





NOTES:
1. C_L includes probe and jig capacitance.
2. All diodes are 1N3064 or equivalent.
3. Switches S1 and S2 are both closed for all measurements except Output Enable times — See AC VOLTAGE WAVEFORMS.

6

APPLICATION

FUNCTIONAL DESCRIPTION

Figure 3 shows a typical configuration of an 8X02A-based control section in a CPU application. Microinstructions read from the memory are used to produce control signals for the CPU and to determine the next microinstruction via the 8X02A Address Control inputs (AC_0-AC_2). In the case of a conditional branch or skip, the status condition applied to the 8X02A TEST input is selected according to the microinstruction. In a branch-type microinstruction, a branch field typically supplies the 8X02A Branch Address inputs (B_0-B_9). (In non-branching instructions, this field may contain other CPU control information.) When a macroinstruction is presented to the CPU, the starting address of the microprogram routine which executes the macroinstruction is presented to the Branch Address inputs. Similar configurations may be used for other applications in which the Branch Address inputs are typically supplied directly from the microprogram memory.

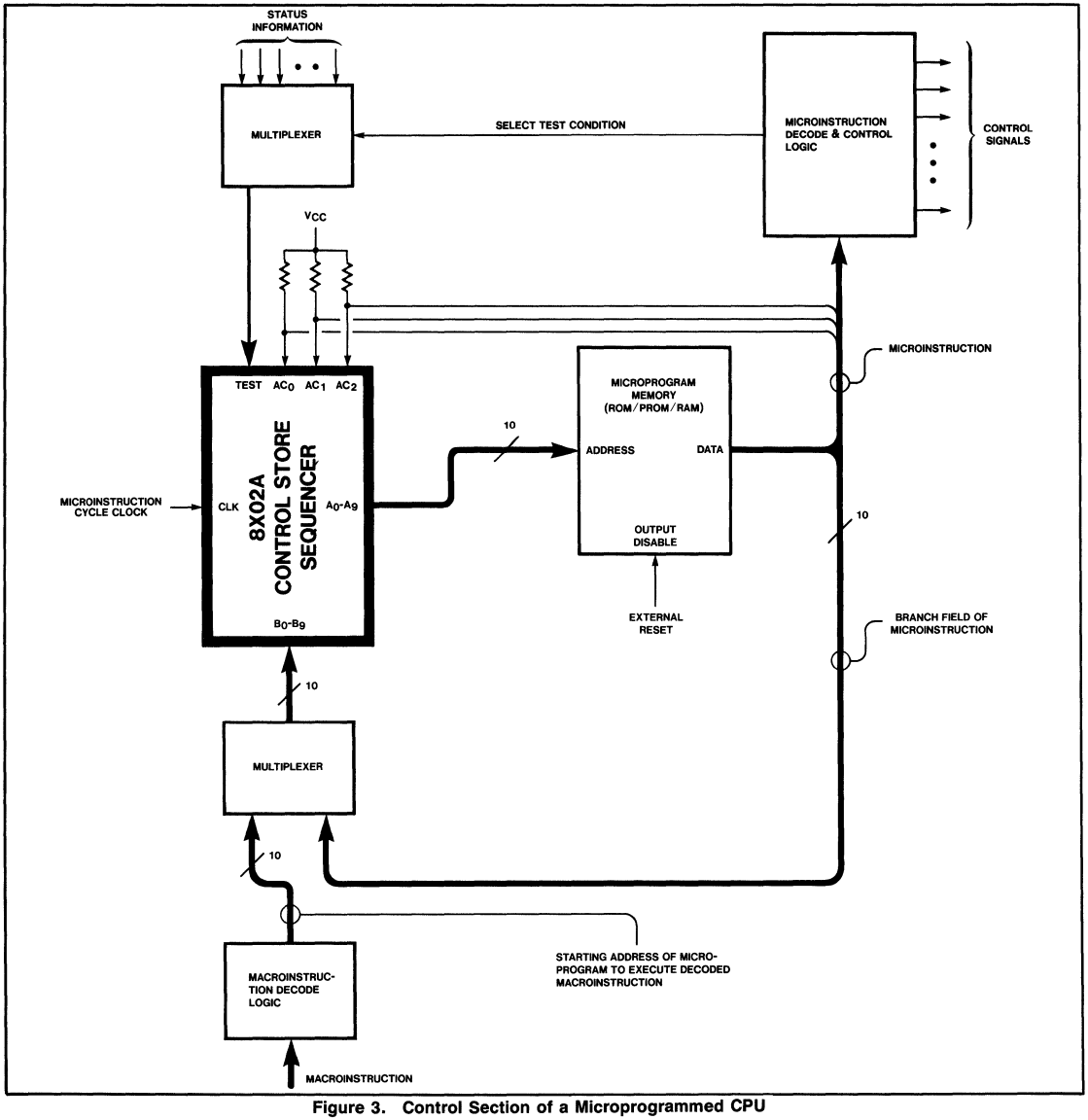


Figure 3. Control Section of a Microprogrammed CPU

NOTES

NOTES

Section 7
Special Purpose Circuits

INDEX

Section 7 — Special Purpose Circuits

CRC GENERATOR/CHECKER 8X01A/9401

PRELIMINARY

DESIGN FEATURES

- **TTL Inputs/outputs**
- **12MHz (Max) data rate**
- **Separate preset/reset controls**
- **SDLC specified pattern match (8X01A only)**
- **Automatic right justification**
- **Pin-for-pin compatibility and functionally identical with 8X01 (8X01A only)**
- **V_{CC} = 5V**
- **14-Pin DIP**

USE AND APPLICATION

- **Floppy and other disk systems**
- **Digital cassette and cartridge systems**
- **Data communication systems**

PRODUCT DESCRIPTION

The CRC Generator/Checker (8X01A or 9401) provides error-correction capabilities for digital systems that handle serial data. The two parts differ in that the 8X01A provides Synchronous Data Link Control (SDLC).

The serial data stream is divided by a selected polynomial; the remainder resulting from this algebraic process is transmitted at the end of the data stream as a Cyclic Redundancy Check Character (CRCC). At the receiving end, the same calculation is performed on the data. If the received message is error-free, the calculated remainder should satisfy a predetermined pattern. In most cases, the remainder is zero; however, where SDLC protocols (8X01A only) are used, the correct remainder is 1111000010111000 (X^0-X^{15}).

Eight polynomials are provided and any of these can be selected via a 3-bit control bus. Popular polynomials, such as CRC-16 and CCITT are implemented and the one selected can be programmed to start with all zeroes or all ones. Right justification for polynomials of degree less than 16 is automatic.

FUNCTIONAL OPERATION

8X01A and 9401

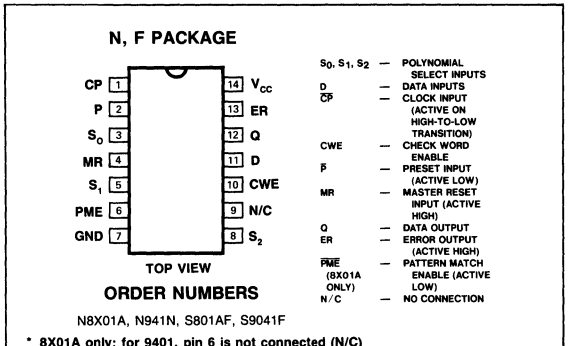
The CRC Generator/Checker circuit provides a means of detecting errors in a serial data communications environment. A binary message can be interpreted as a binary polynomial H(x). This polynomial can be divided by a generator polynomial P(x) such that H(x) = P(x) Q(x) + R(x) whereby Q(x) is the quotient and R(x) is the remainder. During transmission, the remainder is appended to the end of the message as check bits. For a given message, a unique remainder is generated. Hardware implementation of division is simply a feedback shift register with Exclusive-OR gating. Subtraction and addition in modulo 2 is implemented by the Exclusive-OR function. The number of shift register stages is equal to the degree of the divisor polynomial.

The accompanying truth table defines the polynomials implemented in the CRC circuit. Each polynomial can be selected via control inputs S_0, S_1 and S_2. To generate the check bits, the data stream is entered via the Data (D) input, using the high to low transition of the Clock ($\overline{CP}$) input. This data is gated with the most significant output (Q) of the shift register which, in turn, controls the exclusive OR gates. The Check Word Enable (CWE) must be held high while the data is being entered. After the last data bit is entered, the CWE is brought low and the check bits are shifted out of the register and appended to the data bits using external gating—see Check Word Generation diagram.

To check an incoming message for errors, both the data and check bits are entered through the "D" input with the CWE input held high. The 8X01A while not in the data path, monitors the message. After the last check bit is entered, in the 8X01A, the ERror output is made valid by a high-to-low transition of $\overline{CP}$. If no error is detected during the data transmission, all bits of the internal register are low and the ERror output is also low; if an error is detected, it is reflected by the bit pattern and the ERror output is high. The ERror output status remains valid until the next high-to-low transition of $\overline{CP}$ or until initialized by the preset ($\overline{P}$) or reset (MR) functions. The $\overline{PME}$ line must be high if the ERror output is used to indicate an all-zero result.

A high level applied to the Master Reset (MR) input asynchronously clears the shift register. A low level applied to the Preset (P) input asynchronously sets all bits to the appropriate state if the control-code inputs (S_0, S_1, and S_2) specify a 16-bit polynomial. In the

8X01A & 9401 PACKAGE/PIN DESIGNATOR

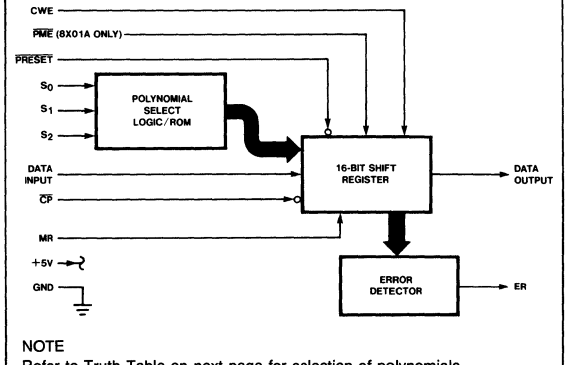


ORDER NUMBERS

N8X01A, N941N, S801AF, S9041F

* **8X01A only; for 9401, pin 6 is not connected (N/C)**

BLOCK DIAGRAM OF 8X01A & 9401



NOTE

Refer to Truth Table on next page for selection of polynomials.

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CRC GENERATOR/CHECKER 8X01A/9401

PRELIMINARY

FUNCTIONAL OPERATION (cont'd)

case of check polynomials that are 8-or-12 bits in length, only the most significant 8-or-12 bits of the shift register are set; all remaining bits are cleared.

8X01A ONLY

For data communications using the Synchronous Data Link Control (SDLC) protocol, the 8X01A is preset to an all-ones configuration before any accumulation is done; this applies to both transmitting and receiving modes of operation. Using SDLC, the check sum shifted out of the 8X01A must be inverted.

During the receiving mode, a special pattern of 1111000010111000 (X^0-X^{15}) is used in place of all-zeroes to check for a valid message. The Pattern Match Enable pin allows the user to select this option. If $\overline{PME}$ is low during the last bit time of the message, the ERror output is low providing the result matches the special pattern; if an error occurs, ER is high.

TRUTH TABLE

SELECT CODE			POLYNOMIAL	REMARKS
S_2	S_1	S_0		
L	L	L	$X^{16}+X^{15}+X^2+1$	CRC-16
L	L	H	$X^{16}+X^{14}+X+1$	CRC-16 REVERSE
L	H	L	$X^{16}+X^{15}+X^{13}+X^7+X^4+X^2+X^1+1$	
L	H	H	$X^{12}+X^{11}+X^3+X^2+X+1$	CRC-12
H	L	L	$X^8+X^7+X^5+X^4+X+1$	
H	L	H	X^8+1	LRC-8
H	H	L	$X^{16}+X^{12}+X^5+1$	CRC-CCITT
H	H	H	$X^{16}+X^{11}+X^4+1$	CRC-CCITT REVERSE

RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
$\overline{CP}$	Clock input	0		12	MHz

DC ELECTRICAL CHARACTERISTICS FOR 8X01A

PARAMETER	DESCRIPTION	TEST CONDITIONS[1]	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input high voltage		2.0			2 0			V
V_{IL}	Input low voltage				0.8			0.7	V
V_{IC}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = −18mA		−0.9	−1.5		−0.9	−1.5	V
V_{OH}	Output high voltage	V_{CC} = Min, I_{OH} = −400μA	2.7	3 4		2.4	3.4		V
V_{OL}	Output low voltage	V_{CC} = Min, I_{OL} = 4.0mA		0.35	0.4		0.35	0.4	V
		V_{CC} = Min, I_{OL} = 8.0mA		0 45	0.5		—	—	V
I_{IL}	Input low current	V_{CC} = Max, V_{IN} = 0.4V		−0.22	−0.36		−0.22	−0.36	mA
I_{IH}	Input high current	V_{CC} = Max, V_{IN} = 2.7V			20			20	μA
I_{IH}	Max input current	V_{CC} = Max, V_{IN} = 7V			0.1			0.1	mA
I_{OS}	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V[2]	−10		−42	−10		−42	mA
I_{CC}	Supply current	V_{CC} = Max, inputs open		60	110		60	110	mA

DC ELECTRICAL CHARACTERISTICS FOR 9401

PARAMETER	DESCRIPTION	TEST CONDITIONS[1]	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input high voltage	Guar. input high voltage	2.0			2.0			V
V_{IL}	Input low voltage	Guar. input low voltage			0 8			0.7	V
V_{IC}	Input clamp diode voltage	V_{CC} = Min I_{IN} = −18mA		−0.9	−1.5		−0.9	−1.5	V
V_{OH}	Output high voltage	V_{CC} = Min, I_{OH} = −400μA	2.4	3.4		2.4	3.4		V
V_{OL}	Output low voltage	V_{CC} = Min, I_{OL} = 4.0mA		0.35	0.4		0.35	0.4	V
		V_{CC} = Min, I_{OL} = 8.0mA		0 45	0.5		—	—	V
I_{IL}	Input low current	V_{CC} = Max, V_{IN} = 0.4V		−0.22	−0.36		−0.22	−0 36	mA
I_{IH}	Input high current	V_{CC} = Max, V_{IN} = 2.7V		1 0	40		1 0	40	μA
		V_{CC} = Max, V_{IN} = 5 5V			1.0			1.0	mA
I_{OS}	Output short circuit current[2]	V_{CC} = Max, V_{OUT} = 0V	−15		−100	−15		−100	mA
I_{CC}	Supply current	V_{CC} = Max, inputs open		70	110		70	110	mA

NOTES 1 Commercial—V_{CC}(min) = 4 75V, V_{CC}(max) = 5 25V Military—V_{CC}(min) = 4 50V, V_{CC}(max) = 5 50V 2 No more than one output should be shorted at a time

AC ELECTRICAL CHARACTERISTICS FOR 8X01A V_{CC} = 5V, T_A = +25°C

PARAMETER	DESCRIPTION	FROM	TO	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
					Min	Typ	Max	Min	Typ	Max	
f_{max}	Max clock freq				12			12			MHz
PULSE WIDTHS:											
t_W-$\overline{CP}$(L)	Clock low			See figure 2	35			35			ns
t_W-$\overline{P}$(L)	Preset low			See figure 3	35			35			ns
t_W-MR(H)	Master reset high			See figure 4	35			35			ns
SETUP/HOLD TIMES:											
t_S-D	Setup time	Data	Clock		55			55			ns
t_S-CWE	Setup time	CWE	Clock	See figure 5	55			55			ns
t_h-D & CWE	Hold time	Data & CWE	Clock		0			0			ns
PROPAGATION DELAY:											
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{PRESET}$	Data output	See figures 1, 2, & 3			55			55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	Master reset	Data output	See figure 4			55			55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{PRESET}$	Error output	See figure 3			55			55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	Master reset	Error output	See figure 4			55			55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{CP}$	Data output	See figure 2			55			55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{CP}$	Error output	See figure 2			55			55	ns
t_{REC}	Recovery time	Preset, MR	Clock	See fig. 3 & 4	35			35			ns

AC ELECTRICAL CHARACTERISTICS FOR 9401 V_{CC} = 5V, T_A = +25°C

PARAMETER	DESCRIPTION	FROM	TO	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
					Min	Typ	Max	Min	Typ	Max	
f_{max}	Max clock freq				12	20		12	20		MHz
PULSE WIDTHS:											
t_W-$\overline{CP}$(L)	Clock low			See figure 2	35			35			ns
t_W-$\overline{P}$(L)	Preset low			See figure 3	40	30		40	30		ns
t_W-MR(H)	Master reset high			See figure 4	35	25		35	25		ns
SETUP/HOLD TIMES:											
t_S-D	Setup time	Data	Clock		55	35		55	35		ns
t_S-CWE	Setup time	CWE	Clock	See figure 5	55	35		55	35		ns
t_h-D & CWE	Hold time	Data & CWE	Clock		0	−8		0	−8		ns
PROPAGATION DELAY:											
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{PRESET}$	Data output	See figures 1, 2, & 3		40	60		40	60	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	Master reset	Data output	See figure 4		30	55		30	55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{PRESET}$	Error output	See figure 3		40	60		40	60	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	Master reset	Error output	See figure 4		40	60		40	60	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{CP}$	Data output	See figure 2		30	55		30	55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{CP}$	Error output	See figure 2		40	60		40	60	ns
t_{REC}	Recovery time	Preset, MR	Clock	See fig. 3 & 4	35	25		35	25		ns

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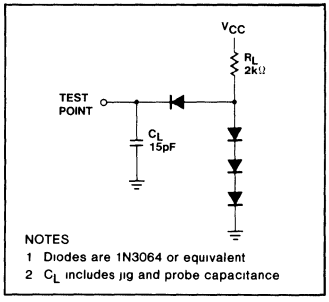
CRC GENERATOR/CHECKER 8X01A/9401

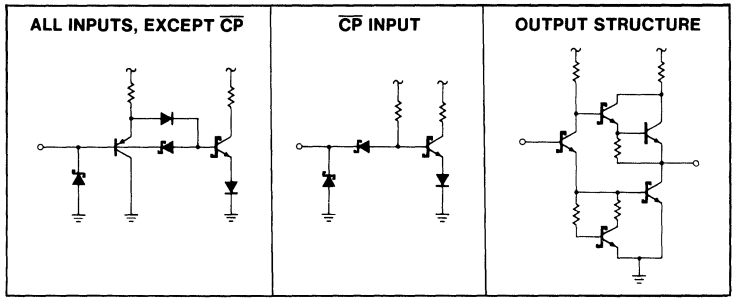
PRELIMINARY

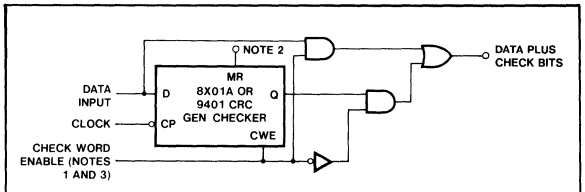
TEST CIRCUIT



NOTES
1 Diodes are 1N3064 or equivalent
2 C_L includes jig and probe capacitance

INPUT/OUTPUT STRUCTURES





NOTES
1 Check Word Enable is HIGH while data is being clocked, it is LOW during transmission of check bits
2 The 8X01A (or 9401) must be RESET or PRESET before each computation
3 CRC check bits are generated and appended to data bits

Figure 1. Check Word Generation

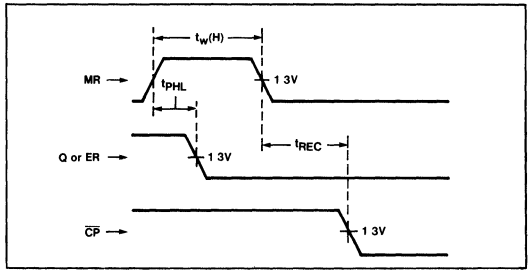


Figure 4. Propagation Delay—MR to Q and ER; Recovery Time—MR to $\overline{CP}$

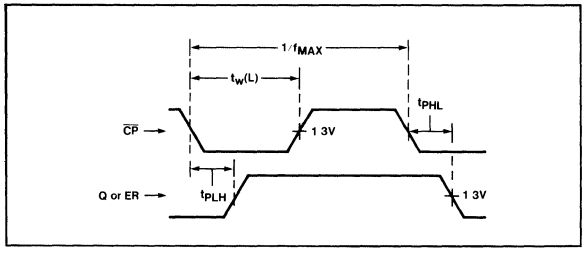


Figure 2. Propagation Delay—$\overline{CP}$ to Q and $\overline{CP}$ to ER

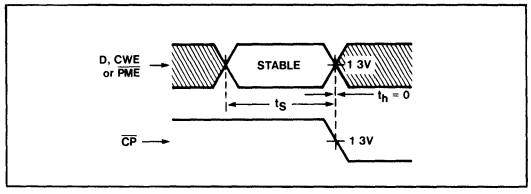


Figure 5. Setup and Hold Times—D to $\overline{CP}$, CWE to $\overline{CP}$, and $\overline{PME}$ to $\overline{CP}$

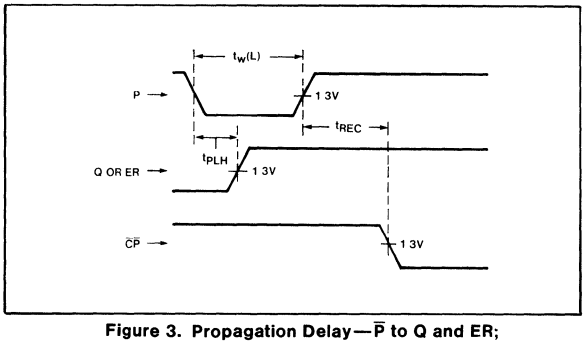


Figure 3. Propagation Delay—$\overline{P}$ to Q and ER; Recovery Time—$\overline{P}$ to $\overline{CP}$.

64-BIT FIFO BUFFER MEMORY (16×4) 9403

FEATURES

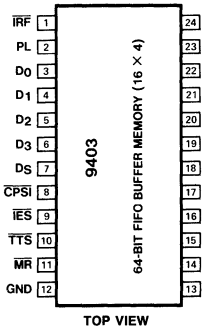
- **10MHz Serial or Parallel Data Rate**
- **Serial or Parallel Input and Output**
- **Expandable Without External Logic**
- **Three-State Outputs**
- **Fully TTL-Compatible**
- **Slim (0.4 in.) 24-Pin DIP**

PRODUCT DESCRIPTION

The 9403 is an expandable fall-through type First-In First-Out (FIFO) Buffer Memory that is optimized for high-speed disc/tape controllers and communication-buffer applications. In multiples of four, the device can be expanded to any number of bits and subsequently, to any number of words. Serial or parallel data can be asynchronously entered or retrieved which makes the 9403 *the* cost-effective solution for implementing buffer memories.

PIN DESIGNATIONS & DESCRIPTIONS

N PACKAGE



TOP VIEW

ORDER NUMBER

N9403N

MNEMONIC AND FUNCTION		DESCRIPTION
$\overline{IRF}$	= Input register full output	Low when input register is full
PL	= Parallel load input	High on PL enables D_0-D_3, not edge-triggered, 1's catching
D_0-D_3	= Parallel data input	—
D_S	= Serial data input	—
$\overline{CPSI}$	= Serial input clock	Edge-triggered and activates on falling edge
$\overline{IES}$	= Serial input enable	When low, serial input is enabled
$\overline{TTS}$	= Transfer to stack input	When low, initiates fall-through
$\overline{MR}$	= Master Reset	Active low
TOP	= Transfer out parallel input	When high and $\overline{TOS}$ is low, enables word transfer from stack to output register—not edge-triggered

MNEMONIC AND FUNCTION		DESCRIPTION
$\overline{TOS}$	= Transfer out serial input	When low and TOP is high, enables word transfer from stack to output register—not edge-triggered
$\overline{OES}$	= Serial output enable input	When low, enables serial output
$\overline{CPSO}$	= Serial output clock input	Edge-triggered and activates on falling edge
$\overline{EO}$	= Output enable	Active low
Q_0-Q_3	= Parallel data output	
Q_S	= Serial data output	
$\overline{ORE}$	= Output register empty output	When high, output register contains valid data
GND	= Ground	—
V_{CC}	= Supply voltage	+5 volts

FUNCTIONAL DESCRIPTION

As shown in Figure 1, the 9403 consists of three parts which operate asynchronously and are virtually independent. These parts are:

- **Input Register**—with serial and parallel data inputs and control signals that permit easy expansion and a handshake interface.
- **FIFO Stack**—4-bit wide, 14-word deep fall-through type with self-contained control logic.
- **Output Register**—with serial and parallel data outputs and control signals that permit easy expansion and a handshake interface.

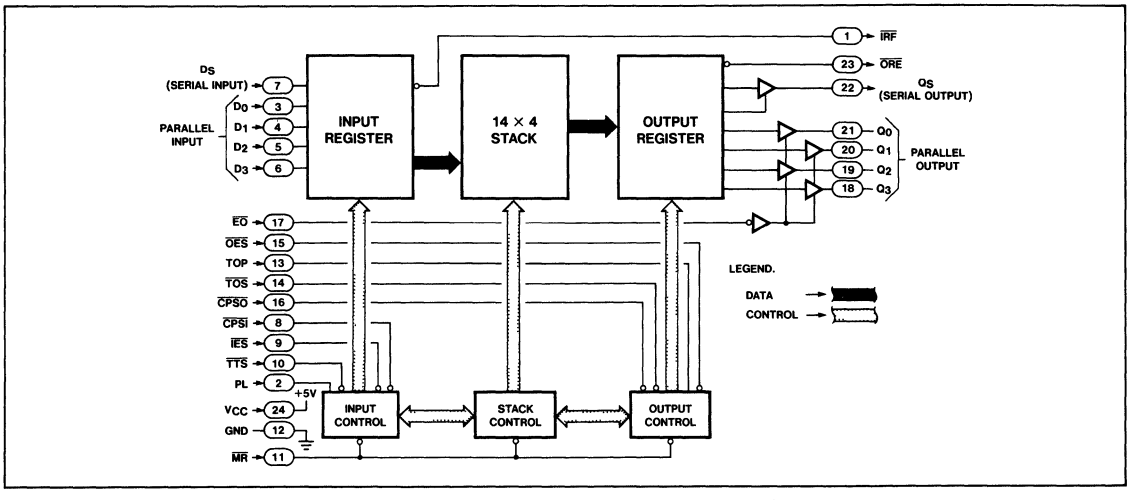


Figure 1. Simplified Block Diagram of 9403 Buffer Memory

INPUT REGISTER

Data can be entered serially or, using the parallel mode of operation, data is entered in 4-bit increments. In either case, the data is subsequently transferred to the fall-through stack; the functional equivalent of this register is shown in Figure 2. The Input Register Full ($\overline{IRF}$) status signal is internally generated by the Register Status (RS) flip-flop; when initialized, the $\overline{Q}$ ($\overline{IRF}$) output of this flip-flop is high.

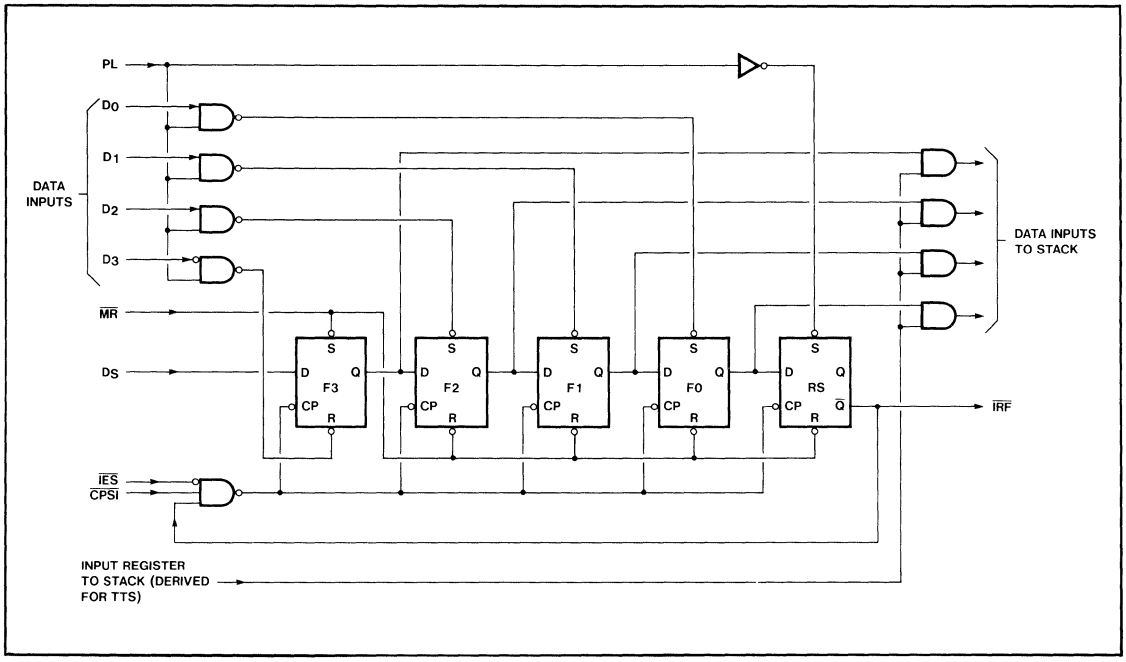


Figure 2. Functional Equivalent of Input Register

Serial Entry (Input Register)

Serial data is entered via the D_S input and is handled by a 5-bit shift register consisting of flip-flops F3, F2, F1, F0, and RS. With $\overline{IES}$ and PL both low, each high-to-low transition of the serial input clock ($\overline{CPSI}$) shifts the input data in domino order from F3 to F2 to F1 to F0. After the fourth clock transition, the four bits of serial data are aligned in F3 through F0 and RS is set, forcing $\overline{IRF}$ low and inhibiting $\overline{CPSI}$ until contents of the input register are transferred to the stack. Figure 3 shows how a serial train of 64-bits would appear in the 9403—four bits (B60-B63) in the input register, 56 bits (B4-B59) in the stack, and four bits (B0-B3) in the output register.

Parallel Entry (Input Register)

When PL is high and $\overline{CPSI}$ is low (Figure 2), flip-flops F0-F3 are loaded with data and $\overline{IRF}$ is forced low. This condition remains until current data is transferred to the stack. Once the data is transferred, $\overline{IRF}$ is driven high and new data can again be clocked into the input flip-flops. If parallel expansion is not being implemented, $\overline{IES}$ must be low to establish row mastership—refer to discussion of parallel expansion.

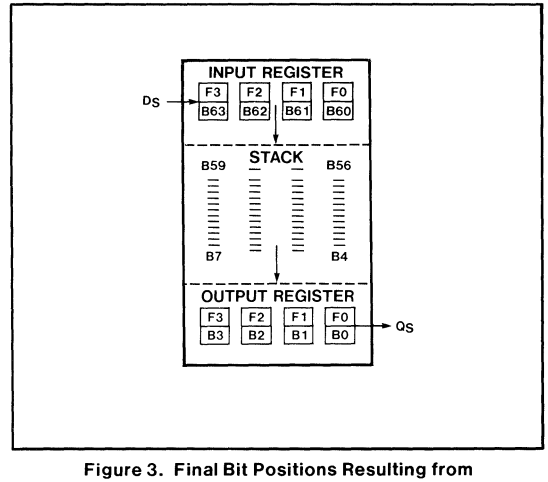


Figure 3. Final Bit Positions Resulting from a Serial Train of 64-Bits

STACK OPERATION

As shown in Figure 2, the outputs of F0-F3 are applied to the stack under control of a signal derived from $\overline{TTS}$. When $\overline{TTS}$ is low, an attempt to initiate a fall-through action is made If the top location of stack is empty, data is loaded and the input register is re-initialized provided PL is low. Note that initialization is postponed until PL is again low. Thus, automatic FIFO action is achieved by connecting the $\overline{TTS}$ input to the $\overline{IRF}$ output

OUTPUT REGISTER

This register receives and stores 4-bits of data from the bottom stack location and, on demand, outputs the data onto a three-state 4-bit parallel data bus or a three-state serial data bus. The Output Register Full ($\overline{ORE}$) status signal is internally-generated by the FX flip-flop, when data is transferred from the stack to the output register, $\overline{ORE}$ goes high The functional equivalent of the output register is shown in Figure 4

Retrieval of Serial Data

When the FIFO stack is empty and $\overline{MR}$ is driven low, the $\overline{ORE}$ output goes low to indicate that the output register is ready to accept new data from the stack After new data is entered and falls through to the bottom stack location, it is transferred to the output register provided $\overline{TOS}$ is low and TOP is high As a result of the data transfer, $\overline{ORE}$ goes high indicating valid data in the output register Subsequently, the $\overline{Q}_S$ output is automatically enabled and the first data bit is transmitted to the three-state serial data bus Henceforth, a serial shift of data occurs on each high-to-low transition of $\overline{CPSO}$. On the fourth transition, the register is emptied, $\overline{ORE}$ is forced low, and serial output $\overline{Q}_S$ is disabled To request a new word from the stack, the $\overline{TOS}$ input can be connected to the $\overline{ORE}$ output

The RS flip-flop (Figure 2) records the fact that data has been transferred to the stack; this flip-flop is not cleared until PL goes low. Therefore, if a particular data word is transferred to the stack and falls to the second location before PL goes low, the same word will not be re-transferred even though $\overline{IRF}$ and $\overline{TTS}$ are still low. Once data enters the stack, "fall-through" is automatic; a delay is necessary only when waiting for the next stack location to empty. In the 9403, as in most modern FIFO designs, the $\overline{MR}$ input initializes the stack control section and does not clear the data

Retrieval of Parallel Data

With the stack empty and $\overline{MR}$ in the active-low state, the $\overline{ORE}$ output goes low, signifying that the output register is also empty When new data is entered and has fallen through to bottom location of the stack, it is automatically transferred to the output register, provided the Transfer Out Parallel (TOP) input is high When the data is transferred from stack-to-register, $\overline{ORE}$ goes high and valid data appears at Q_0-Q_3 (Figure 4), provided the three-state buffers are enabled, that is, $\overline{EO}$ is active-low When TOP goes low, $\overline{ORE}$ is driven low which indicates that the data output cycle is complete; however, the original data remains latched in the flip-flops until the next word (if available) is transferred from the stack to the output register.

For parallel operation, $\overline{CPSO}$ must be low, whereas, $\overline{TOS}$ should be grounded for single-slice operation or connected to the appropriate $\overline{ORE}$ for expanded operation The TOP input is not edge-triggered, therefore, if it goes high before data is available from stack but data becomes available before it goes low, the data will be transferred to the output register However, internal control circuits prevent the same data from being transferred twice If TOP goes high and returns to low before data is available from the stack, $\overline{ORE}$ will remain low, indicating the absence of valid output data.

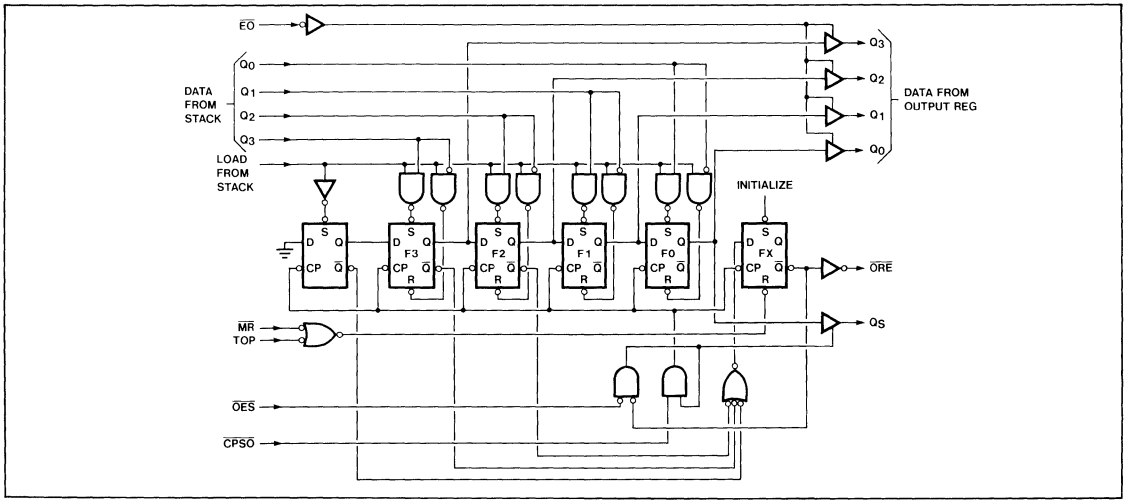


Figure 4. Functional Equivalent of Output Register

64-BIT FIFO BUFFER MEMORY (16×4) 9403

VERTICAL EXPANSION

In a vertical structure, the 9403 can be expanded to achieve greater word capacity without any external parts; a 46-word by 4-bit FIFO is shown in Figure 5. Using the same technique and similar connections, any FIFO of 15n+1 words (where *n* is the number of devices) can be constructed. Observe that word expansion does not sacrifice flexibility of the 9403 FIFO as regards serial/parallel input and output.

HORIZONTAL EXPANSION

The 9403 can be horizontally expanded to store long words in multiples of 4-bits, again without external logic. Connections required to form a 16-word by 12-bit FIFO are shown in Figure 6, using similar techniques, any 16-word by 4n-bit FIFO (where *n* is the number of devices) can be constructed.

For horizontal or bit expansion, it is good practice to connect, respectively, the $\overline{IRF}$ and $\overline{ORE}$ outputs of the right-most device (most significant device) to the $\overline{TTS}$ and $\overline{TOS}$ inputs of all devices to the left (least significant devices) to guarantee that no operation is initiated before each and every device is ready Word expansion does not affect the ability of the 9403 to handle serial/parallel inputs and outputs, however, the ripple form of expansion shown in Figure 6 does extract a penalty in speed of operation Whereas a single 9403 is guaranteed to operate at 10MHz, an array of four FIFOs connected as shown is guaranteed to operate at 4 3MHz

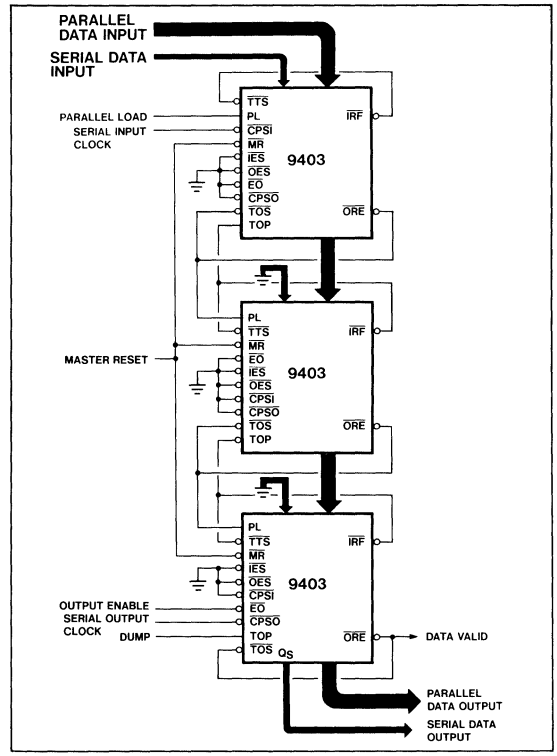


Figure 5. Word Expansion

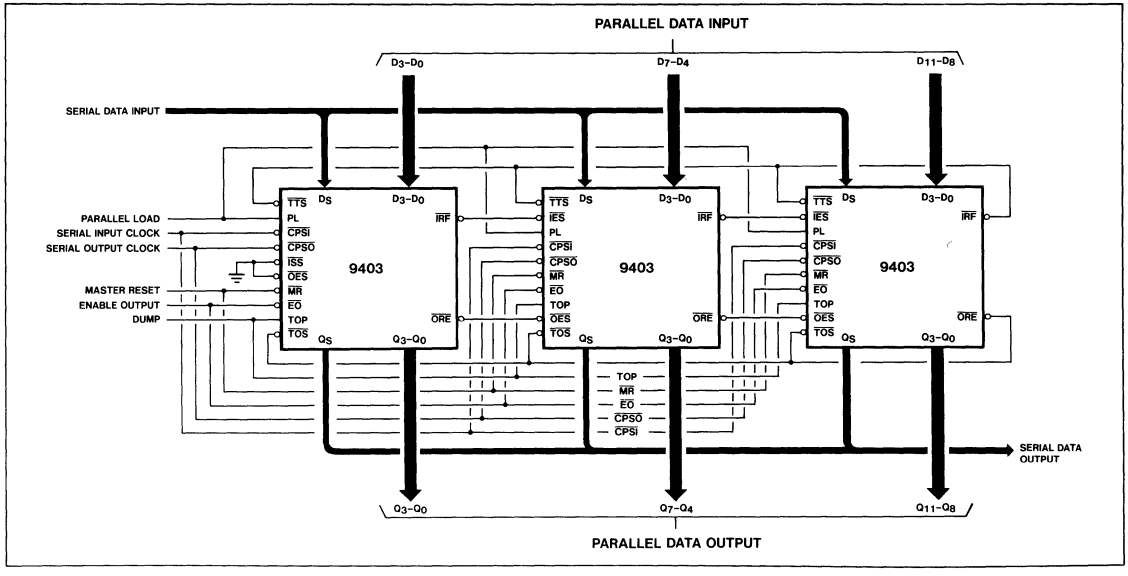


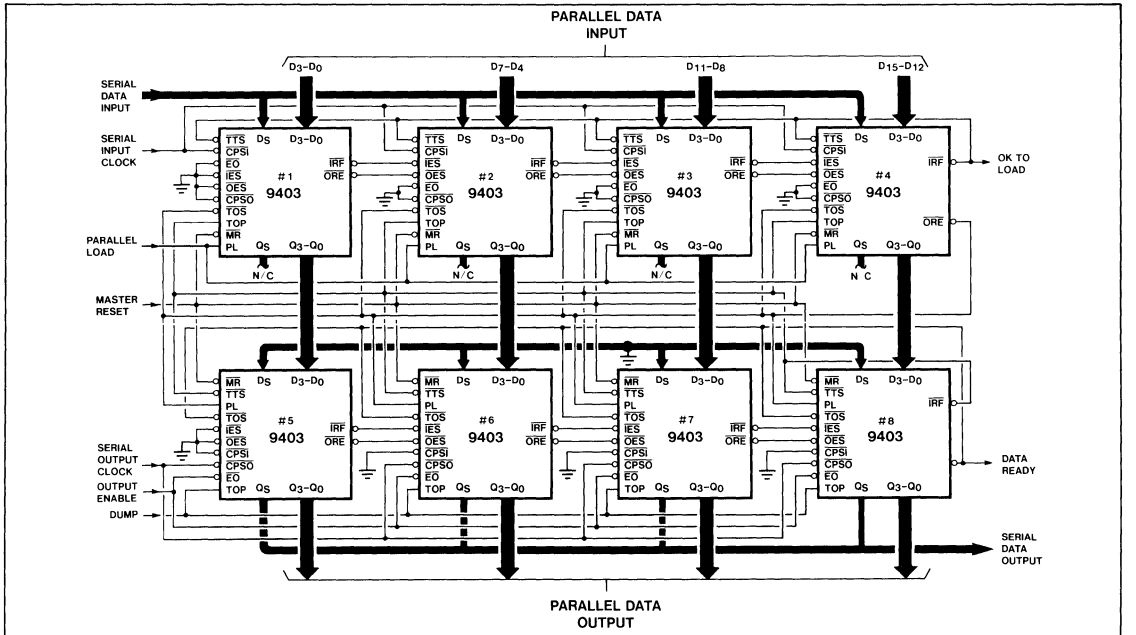
Figure 6. Bit Expansion

64-BIT FIFO BUFFER MEMORY (16×4) 9403

HORIZONTAL AND VERTICAL EXPANSION

In addition to bit-or-word expansion, the 9403 can be used to expand in both the horizontal and vertical directions; a 31-word by 16-bit FIFO is shown in Figure 7 Using the same or similar techniques, any FIFO of 15m+1 words by 4n-bits can be constructed, where *m* is the number of devices in a column and *n* is the number of devices in a row.

The chart appended to Figure 7 shows the final positions for a contiguous serial entry of 496 bits. Figures 8 and 9, respectively, show the timing relationships involved for data-entry and data-retrieval pertaining to the 31-word by 16-bit array



INPUT REGISTER	UNIT NUMBER & ORDER OF SERIAL BITS #1	#2	#3	#4	OUTPUT REGISTER	UNIT NUMBER & ORDER OF SERIAL BITS #5	#6	#7	#8
D_3	BIT 483	BIT 487	BIT 491	BIT 495	Q_3	BIT 3	BIT 7	BIT 11	BIT 15
D_2	↓ 482	↓ 486	↓ 490	↓ 494	Q_2	↓ 2	↓ 6	↓ 10	↓ 14
D_1	↓ 481	↓ 485	↓ 489	↓ 493	Q_1	↓ 1	↓ 5	↓ 9	↓ 13
D_0	↓ 480	↓ 484	↓ 488	↓ 492	Q_0	↓ 0	↓ 4	↓ 8	↓ 12

Figure 7. Horizontal and Vertical Expansion—31X16 FIFO

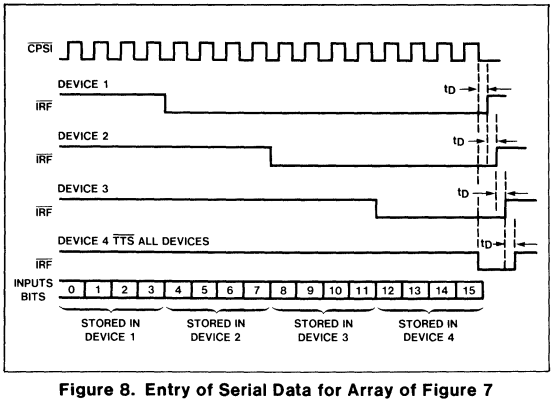


Figure 8. Entry of Serial Data for Array of Figure 7

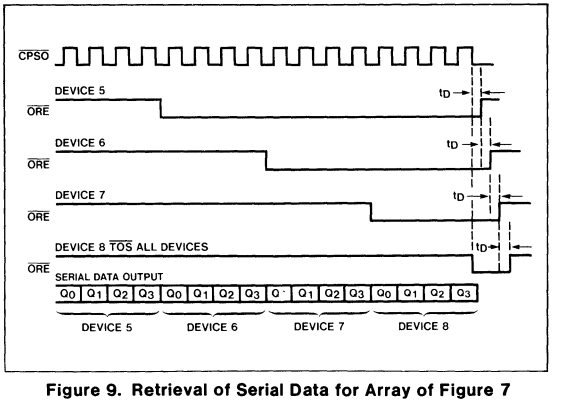


Figure 9. Retrieval of Serial Data for Array of Figure 7

INTERLOCKING CIRCUITS

Most conventional FIFO designs provide the status-signal counterparts of $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are used in arrays, variations in unit-to-unit operating speeds require the use of external gating to ensure that all devices have, in fact, completed the last operation. The 9403 incorporates simple but effective master/slave interlocking circuits to eliminate these gating requirements.

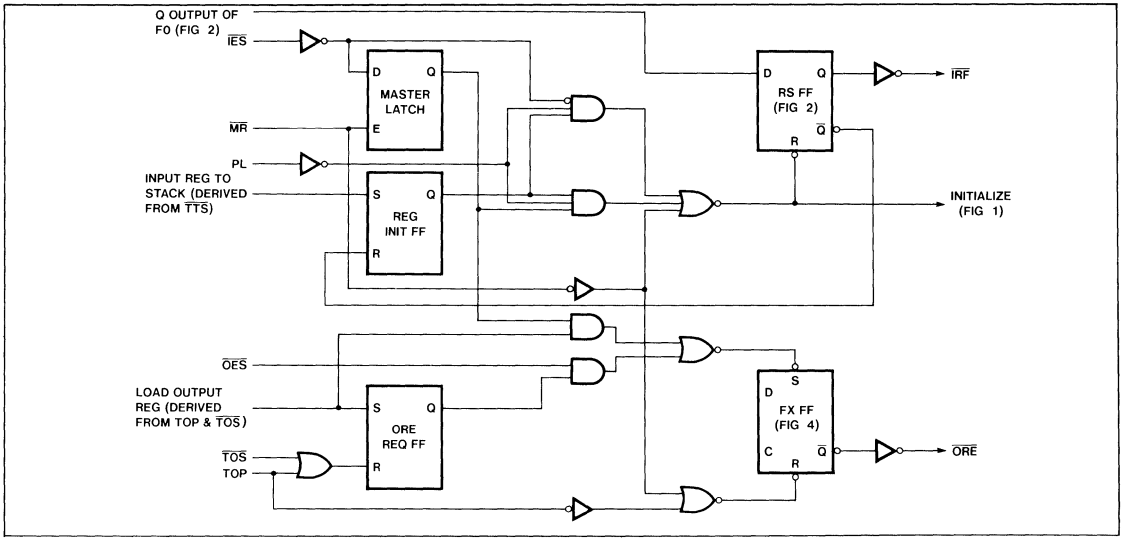


Figure 10. Functional Equivalent of Interlocking Circuits

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5 5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
T_A	Operating temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS Over operating temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ	Max	
V_{IH}	Input high voltage	Guaranteed input high voltage	2.0			V
V_{IL}	Input low voltage	Guaranteed input low voltage			0.8	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min, I_{IN} = −18mA		−0.9	−1.5	V
V_{OH}	Output high voltage, $\overline{ORE}$, $\overline{IRF}$	V_{CC} = Min, I_{OH} = −400μA	2 4	3.4		V
V_{OH}	Output high voltage, Q_0-Q_3, Q_S	I_{OH} = −5.7mA, V_{CC} = Min	2.4	3.1		V
V_{OL}	Output low voltage, Q_0-Q_3; Q_S	V_{CC} = Min, I_{OL} = 16mA		0.35	0.5	V
V_{OL}	Output low voltage, $\overline{ORE}$, $\overline{IRF}$	V_{CC} = Min, I_{OL} = 8.0mA		0.35	0.5	V
I_{OZH}	Output off current high, Q_0-Q_3, Q_S	V_{CC} = Max, V_{OUT} = 2.4V, V_E = 2V			100	μA
I_{OZL}	Output off current low, Q_0-Q_3, Q_S	V_{CC} = Max, V_{OUT} = 0.5V, V_E = 2V			−100	μA
I_{IH}	Input high current	V_{CC} = Max, V_{IN} = 2.7V		1.0	40	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
I_{IL}	Input low current, all except $\overline{OES}$ & $\overline{IES}$	V_{CC} = Max, V_{IN} = 0 4V			−0.36 −0.96	mA
I_{OS}	Output short circuit current, Q_0-Q_3, Q_S $\overline{ORE}$, $\overline{OES}$	V_{CC} = Max, V_{OUT} = 0, (Note 3)	−30		−130	mA
I_{CC}	Supply Current	V_{CC} Max, Inputs open		115	170	mA

NOTES
1 Operating temperature ranges are guaranteed after terminal equilibrium has been reached
2 All voltages measured with respect to ground terminal
3 No more than one output should be shorted at a time

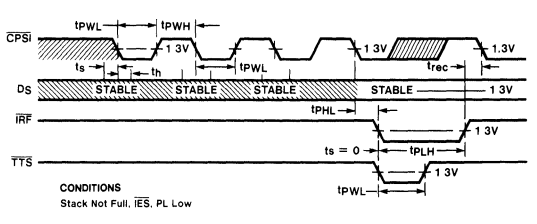
AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V, C_L = 15pF, T_A = 25° C

PARAMETER	FROM INPUT	TO OUTPUT	TEST CONDITIONS[1,2,3]	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
FALL-THROUGH TIME t_{DFT}	Positive going PL	Q_0-Q_3	$\overline{TTS}$ connected to $\overline{IRF}$, $\overline{TOS}$ connected to $\overline{ORE}$, $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ low, TOP high (f, Fig 11)		450	600	ns
PROPAGATION DELAY							ns
t_{PLH} Low-to-high t_{PHL} High-to-low	Negative going $\overline{TTS}$ Negative going $\overline{CPSI}$	$\overline{IRF}$ $\overline{IRF}$	Stack not full, PL low (a & b, Fig 11)		48 18	64 25	
t_{PLH} Low-to-high t_{PHL} High-to-low	Negative going $\overline{CPSO}$	Q_S	Serial output $\overline{OES}$ low, TOP high (c & d, Fig 11)		30 17	40 28	ns
t_{PHL} High-to-low	Negative going $\overline{CPSO}$	$\overline{ORE}$			32	42	ns
t_{PLH} Low-to-high t_{PHL} High-to-low	Positive going TOP	Q_0-Q_3	$\overline{EO}$, $\overline{CPSO}$ low (e, Fig 11)		40 31	56 45	ns
t_{PLH} Low-to-high t_{PHL} High-to-low	Positive going TOP Negative going TOP	$\overline{ORE}$ $\overline{ORE}$	Parallel output, $\overline{EO}$, $\overline{CPSO}$ low (e, Fig 11)		51 40	68 54	ns
t_{PLH} Low-to-high	Negative going $\overline{TOS}$	Positive going $\overline{ORE}$	Data in stack, TOP high, (c & d, Fig 11)		41	56	ns
t_{PHL} High-to-low	Positive going PL	Negative going $\overline{IRF}$	Stack not full (g & h, Fig 11)		20	33	ns
t_{PLH} Low-to-high t_{PLH} Low-to-high t_{PLH} Low-to-high	Negative going PL Positive going $\overline{OES}$ Positive going $\overline{IES}$	Positive going $\overline{IRF}$ $\overline{ORE}$ Positive going $\overline{IRF}$			33 26 31	46 44 40	ns
ENABLE DELAY t_{PZH} High t_{PZL} Low	$\overline{EO}$	Q_0-Q_3	Out of high impedance state		9	14 20	ns
t_{PZL} Low t_{PZH} High	Negative going $\overline{OES}$	Q_S			13	25 20	ns
DISABLE DELAY t_{PLZ} Low t_{PHZ} High	$\overline{EO}$	Q_0-Q_3	Into high impedance state		7	14	ns
t_{PLZ} Low t_{PHZ} High	Negative going $\overline{OES}$	Q_S			7	14	ns
APPEARANCE TIME t_{AP} Parallel t_{AS} Serial	$\overline{ORE}$ $\overline{ORE}$	Q_0-Q_3 Q_S	Time elapsed between $\overline{ORE}$ going high and valid data appearing at output, negative number indicates data available before $\overline{ORE}$ goes high		−12 6	−5 10	ns
PULSE WIDTH t_{PWL} $\overline{CPSI}$ low t_{PWH} $\overline{CPSI}$ high			Stack not full, PL low (a & b, Fig 11)	20 33	11 19		ns
t_{PWL} TOP low t_{PWH} TOP high			$\overline{CPSO}$ low, data available in stack (e, Fig 11)	30 26	17 13		ns
t_{PWL} $\overline{CPSO}$ low t_{PWH} $\overline{CPSO}$ high			TOP high, data in stack, (c & d, Fig 11)	30 32	16 18		ns
t_{PWH} PL high			Stack not full (g & h, Fig 11)	40	29		ns
t_{PWL} $\overline{TTS}$ low (serial or parallel mode)			Stack not full (a, b, g, & h, Fig 11)	20	9		ns
t_{PWL} $\overline{MR}$ low			(f, Fig 11)	25	13		ns
SETUP and HOLD TIME t_s Setup time t_h Hold time	D_S D_S	Negative $\overline{CPSI}$ CPSI	PL low (a & b, Fig 11)	28 0	17 −6		ns

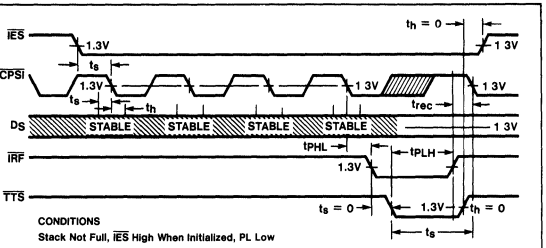
AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V, C_L = 15pF, T_A = 25° C (Cont'd)

PARAMETER		FROM	TO	TEST CONDITIONS[1,2,3]	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_s	Setup time	Parallel inputs	PL	Length of time parallel inputs must be applied prior to rising edge of PL	0	−22		ns
t_h	Hold time	Parallel inputs	PL	Length of time parallel inputs must remain applied after falling edge of PL	2			ns
t_s	Set up time (serial or parallel mode)	$\overline{TTS}$	$\overline{IRF}$	(a, b, g, & h, Fig 11)	0	−20		ns
t_s	Setup time	Negative going $\overline{ORE}$	Negative going $\overline{TOS}$	TOP high (c & d, Fig 11)	0	−24		ns
t_s t_s	Setup time Setup time	Negative going $\overline{IES}$ Negative $\overline{TTS}$	$\overline{CPSI}$ $\overline{CPSI}$	(b, Fig 11)	45 84	23 58		ns
RECOVERY TIME t_{rec}		$\overline{MR}$	Any input	(f, Fig 11)	15	5		ns

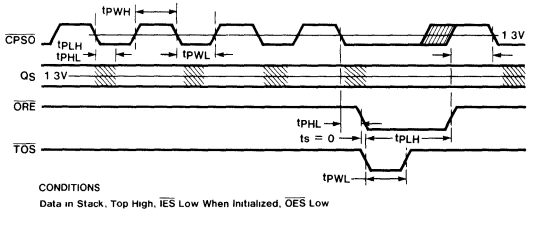
NOTES
1 Initialization requires a master reset to occur after power has been applied
2 $\overline{TTS}$ normally connected to $\overline{IRF}$
3 If stack is full, $\overline{IRF}$ will stay low



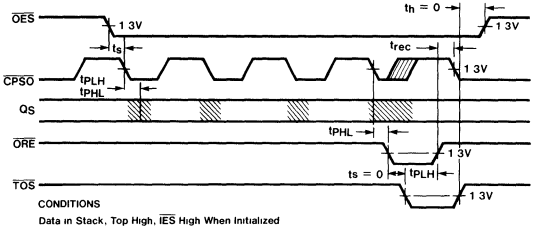
a. Serial Input, Unexpanded or Master Operation



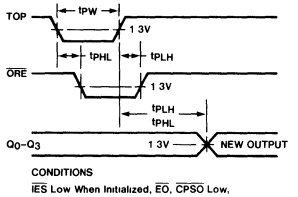
b. Serial Input, Expanded Slave Operation



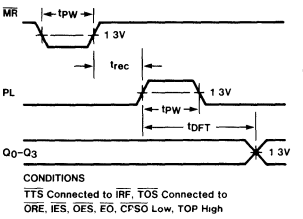
c. Serial Output, Unexpanded or Master Operation



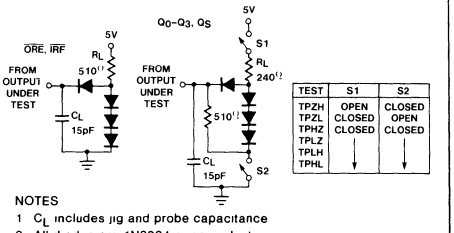
d. Serial Output, Slave Operation



e. Parallel Output, 4-Bit Word or Master/Slave Operation in Parallel Expansion

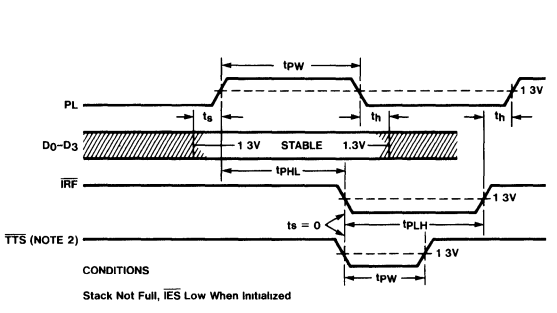


f. Fall-Through Time

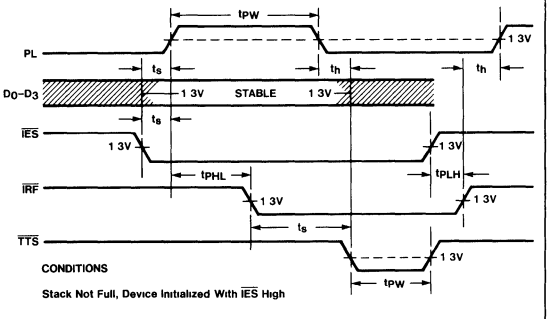


g. Test Circuit for Measurement of AC Parameters

Figure 11. 9403 Timing and Parameter-Measurement Information



h. Parallel Load Mode, 4-BIT Word (Unexpanded) or Master/Slave Operation in Parallel Expansion



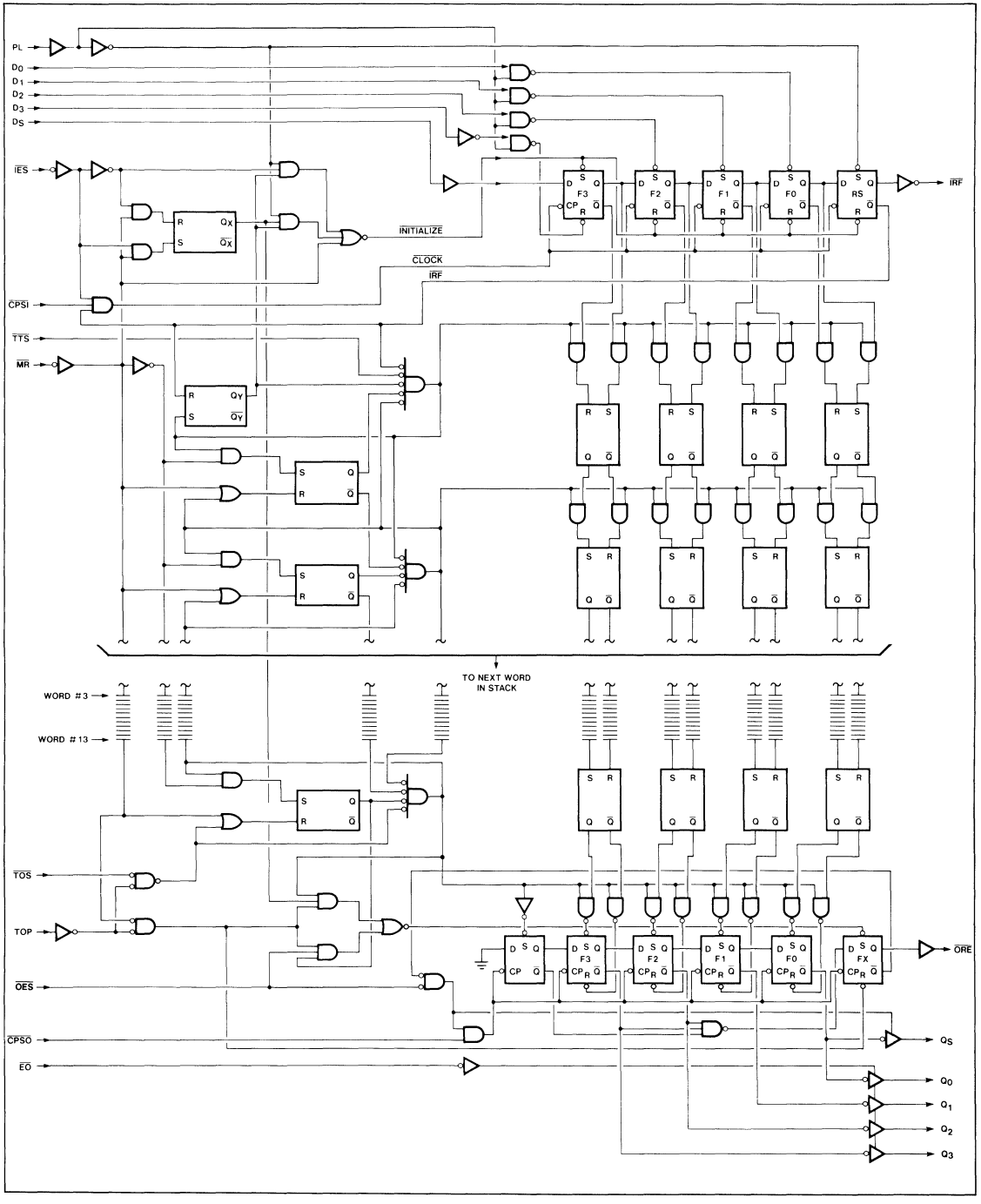
j. Parallel Load, Slave Mode

Figure 11. 9403 Timing and Parameter-Measurement Information (Cont'd)

7

64-BIT FIFO BUFFER MEMORY (16×4) 9403

LOGIC DIAGRAM



AUTODIRECTIONAL BUS TRANSCEIVER 8X41

DESIGN FEATURES

- **Intelligent bidirectional bus repeater with self-generating or external control**
- **Eight independent channels**
- **Open-collector outputs (meets DEC UNIBUS* specifications)**
- **TTL compatible**
- **High speed (30-nanoseconds max)**
- **Expandable to any number of bits**
- **High input impedance for every operating value of V_{CC}**
- **Low input current (less than 100-microamperes); high output current (up to 70-milliamperes)**
- **0.6 in. 24-pin DIP**
- **+5V supply**

USE AND APPLICATION

- **Minicomputers**
- **Microcomputers MOS/Bipolar**
- **Communications**
- **Signal buffer**
- **Bus fan-out extensions**
- **Distributed processing**
- **Bidirectional bus connector/isolator**

PRODUCT DESCRIPTION

The Signetics 8X41 Autodirectional Bus Transceiver is a general purpose asynchronous device ideal for system bus expansion applications. The 8X41 consists of eight data channels, each with one pair of terminals (A_I and B_I); each data channel can be operated independently.

The device requires no external controls since all intelligence is internally generated; thus, operation of the device is completely autonomous. The first logic low signal that occurs on one channel terminal (A_I or B_I) will be repeated on the corresponding terminal (B_I or A_I) of the same channel.

The 8X41 is designed for use in open-collector bus systems where high speed and low-current inputs/high-current outputs are required. In system configurations, the discrete capabilities of the bus transceiver can be expanded by parallel connection to service any number of bits. To provide reliable operation and integrity of data transfers, all channels are disabled by an on-chip power monitor whenever V_{CC} falls below approximately 4V.

FUNCTIONAL OPERATION

The 8X41 (Figure 1) consists of eight functionally independent yet logically identical channels. Each channel consists of two bus terminals (A_I and B_I); each terminal is internally connected to an open-collector driver and a high-impedance receiver. The monitoring state of each channel is defined when both terminals (A_I and B_I) are "high"; in this state, the internal logic of the 8X41 continually examines the A and B bus signals to determine signal direction—A_I to B_I or B_I to A_I. A low signal occurring at either of the two terminals causes the open-collector driver on the opposite terminal to follow suit; hence, the signal is repeated by the 8X41. For each channel, latches L1 and L2 determine signal direction. As shown in the truth table for these latches, there is no transmission of data when both signals are low, however, this condition should never occur during normal system operation.

The internal automatic direction control can be overridden by either or both of the common disable inputs—$\overline{DBA}$ and $\overline{DAB}$. When $\overline{DBA}$ is driven low ($\overline{DAB}$ = high), the B_I to A_I path is interrupted and the device becomes a unidirectional repeater in the A_I to B_I direction only. With these conditions reversed ($\overline{DAB}$ = low and $\overline{DBA}$ = high), the A_I to B_I path is interrupted and the chip functions as a unidirectional repeater in the B_I to A_I direction. When both control signals are low, data passage is inhibited in both directions. Refer to the I/O truth table for all possible input/output conditions.

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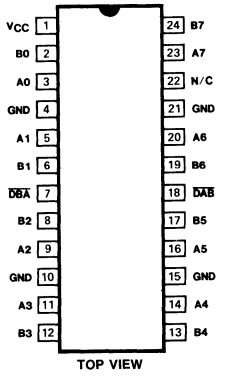
7

8X41 PACKAGE/PIN DESIGNATIONS

N PACKAGE



TOP VIEW

ORDER NUMBER

N8X41N

PIN NO.	IDENTIFIER	FUNCTION
1	V_{CC}	+5V power
3, 5, 9, 11, 14, 16, 20, and 23	A_0-A_7	A-bus input/output
2, 6, 8, 12, 13, 17, 19, and 24	B_0-B_7	B-bus input/output
4, 10, 15, and 21	GND	Circuit ground
7 & 18	$\overline{DBA}$ & $\overline{DAB}$	Input/output control
22	N/C	No connection

AUTODIRECTIONAL BUS TRANSCEIVER 8X41

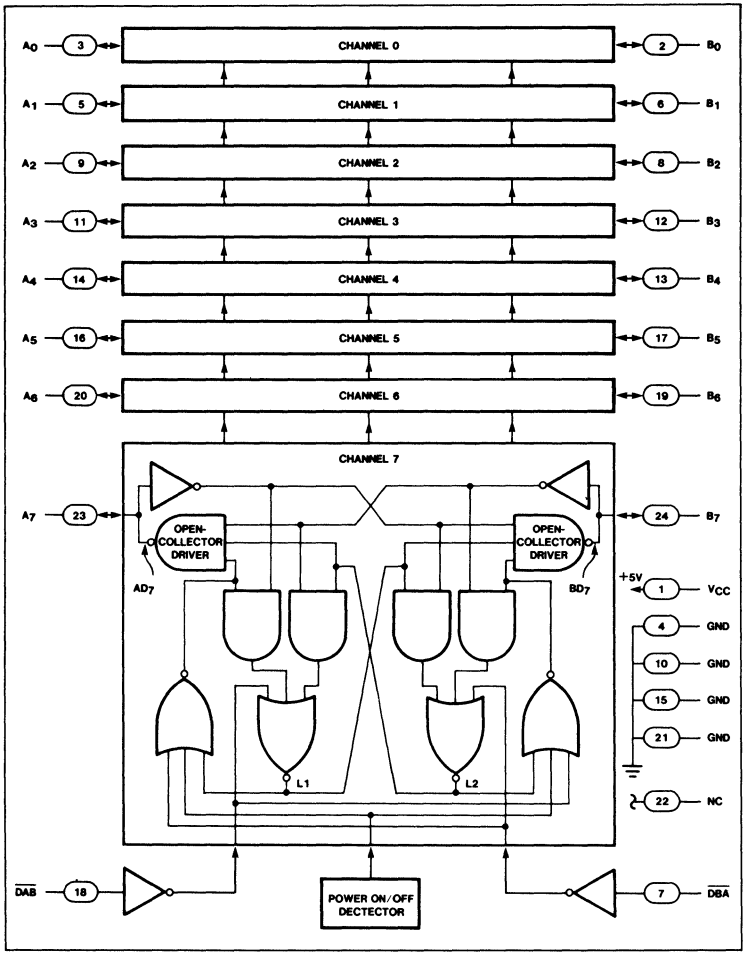


Figure 1. Logic Diagram of 8X41

$\overline{DBA}$	$\overline{DAB}$	FUNCTION
Ø	Ø	Data transmission inhibited
Ø	1	$A_i \rightarrow B_i$
1	Ø	$A_i \leftarrow B_i$
1	1	$A_i \rightarrow B_i$ $A_i \leftarrow B_i$

i = Channel 0, 1, 2, 3, 4, 5, 6, or 7
$A_i \rightarrow B_i$ = Data transmission from A_i to B_i
$A_i \leftarrow B_i$ = Data transmission from B_i to A_i

TRUTH TABLE FOR INTERNAL LATCHES

LATCHES		DIRECTION OF DATA
L1	L2	
1	1	Monitoring state
1	Ø	A_i to B_i
Ø	1	B_i to A_i
Ø	Ø	No transmission

INPUT/OUTPUT TRUTH TABLE

EXTERNAL CONTROLS		INPUT SIGNALS		OUTPUT DRIVER SIGNALS	
$\overline{DAB}$	$\overline{DBA}$	A_i	B_i	AD_i	BD_i
H	H	L	L	H	H
H	H	L	H	H	L
H	H	H	L	L	H
H	H	H	H	H	H
H	L	L	L	H	L
H	L	L	H	H	L
H	L	H	L	H	H
H	L	H	H	H	H
L	H	L	L	L	H
L	H	L	H	H	H
L	H	H	L	L	H
L	H	H	H	H	H
L	L	X	X	H	H

Notes
A_i = External signal
AD_i = Output A driver
B_i = External signal
BD_i = Output B driver
X = Don't care

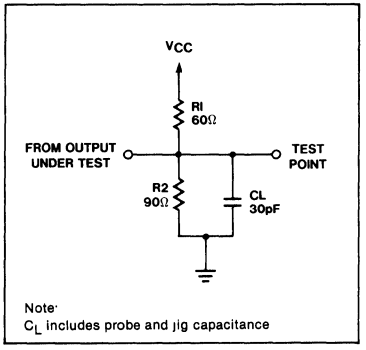
AUTODIRECTIONAL BUS TRANSCEIVER 8X41

DC CHARACTERISTICS $V_{CC} = 5V (\pm 5\%)$; $T_A = 0°C$ to $70°C$

PARAMETER	DESCRIPTION	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
V_{OL}	Bus output low voltage (driver ON)	I_{OL} = 70 mA; V_{CC} = Min			0.5	V
*V_B	Bus input threshold voltage (driver OFF)		1.3		1.7	V
V_{IH} ($\overline{DBA}$, $\overline{DAB}$ only)	High level input voltage		2.0			V
V_{IL} ($\overline{DBA}$, $\overline{DAB}$ only)	Low level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC} = Min; I_{IL} = −18mA			−1.5	V
V_{PD}	Power ON/OFF detector threshold voltage		3.7		4.35	V
I_{IH} ($\overline{DBA}$, $\overline{DAB}$ only)	High level input current	V_{CC} = Max; V_{IN} = 2.7V			20	μA
I_{IL} ($\overline{DBA}$, $\overline{DAB}$ only)	Low level input current	V_{CC} = Max; V_{IN} = 0.4V			−0.4	mA
I_I	Bus input current (driver OFF)	V_{CC} = Max; V_B = 2.5V*			100	μA
		V_{CC} = Max; V_B = 0V*			−20	μA
I_{OFF}	Bus leakage current (power OFF)	V_{CC} = 0V; V_B = 2.5V*			100	μA
I_{CC}	Supply current	V_{CC} = Max; A_0-A_7 = Low or B_0-B_7 = Low and $\overline{DBA}$ = $\overline{DAB}$ = High		145	180	mA

*$V_B = V_{BUS}$

LOAD CIRCUIT FOR OUTPUTS



Note:
C_L includes probe and jig capacitance

AC CHARACTERISTICS $V_{CC} = 5V (\pm 5\%)$; $T_A = 0°C$ to $70°C$

PARAMETER	DESCRIPTION	FROM	TO	TEST CONDITIONS	LIMITS			UNITS
					Min	Typ	Max	
t_{PLL}	Propagation delay	Low A_i Low B_i	Low BD_i Low AD_i	$\overline{DBA}$ = $\overline{DAB}$ = High			30	ns
t_{PHH}	Propagation delay	High A_i High B_i	High BD_i High AD_i	$\overline{DBA}$ = $\overline{DAB}$ = High			30	ns
t_{DHH}	Propagation delay	High A_i	High BD_i	$\overline{DBA}$ = Low; $\overline{DAB}$ = High			25	ns
		High B_i	High AD_i	$\overline{DAB}$ = Low; $\overline{DBA}$ = High			25	ns
t_{DLL}	Propagation delay	Low A_i	Low BD_i	$\overline{DBA}$ = Low; $\overline{DAB}$ = High			25	ns
		Low B_i	Low AD_i	$\overline{DAB}$ = Low; $\overline{DBA}$ = High			25	ns
t_{DEH}	Propagation delay	Low $\overline{DBA}$	High AD_i	$\overline{DAB}$ = Low; B_i = Low			30	ns
t_{DEL}	Propagation delay	High $\overline{DBA}$	Low AD_i	$\overline{DAB}$ = Low; B_i = Low			30	ns
t_{DEH}	Propagation delay	Low $\overline{DAB}$	High BD_i	$\overline{DBA}$ = Low; A_i = Low			30	ns
t_{DEL}	Propagation delay	High $\overline{DAB}$	Low BD_i	$\overline{DBA}$ = Low; A_i = Low			30	ns
t_r	Recovery time (see timing diagram)	—	—	$\overline{DBA}$ = $\overline{DAB}$ = High		20		ns

Notes A_i = External signal AD_i = Output A driver B_i = External signal BD_i = Output B driver

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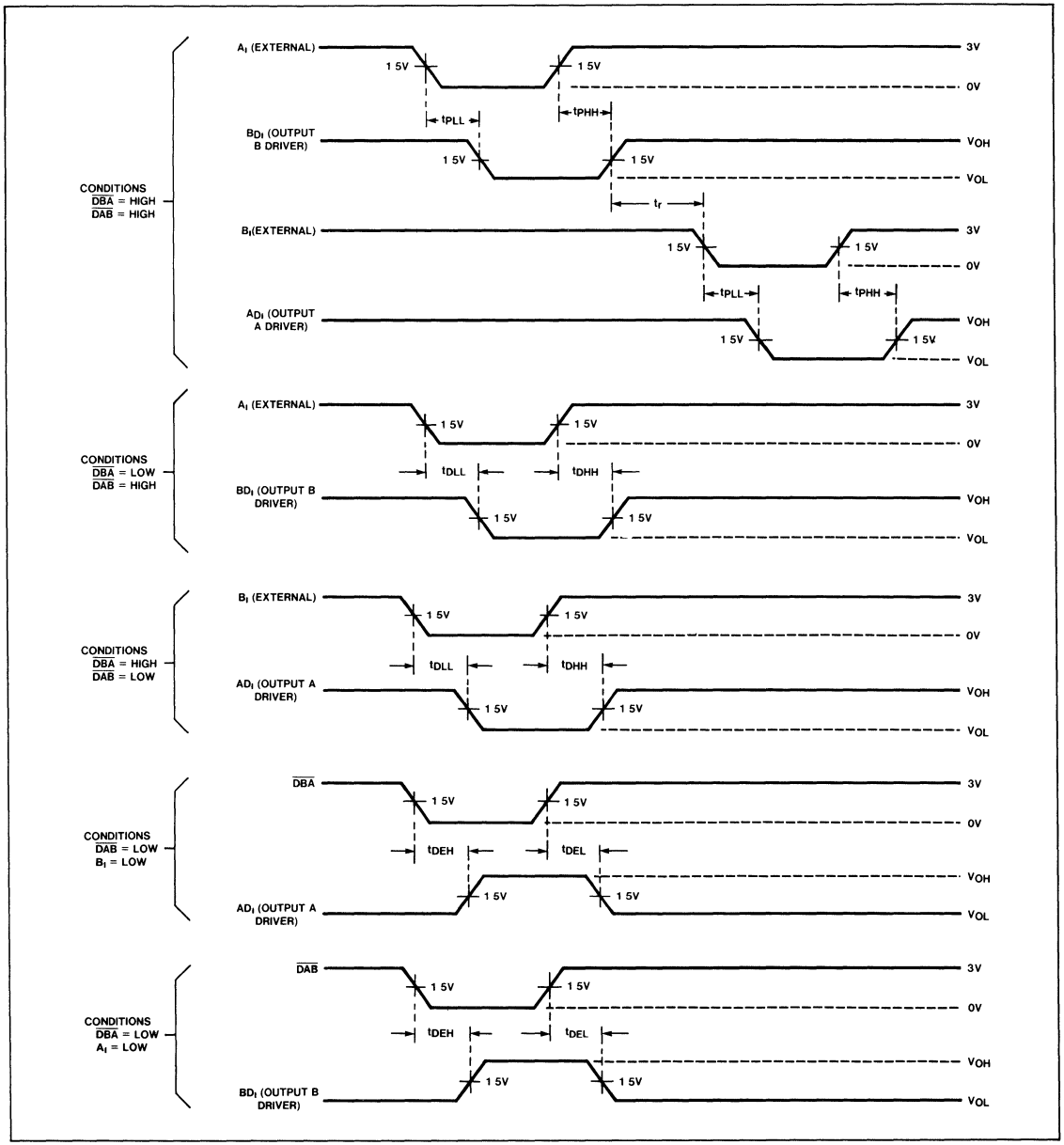
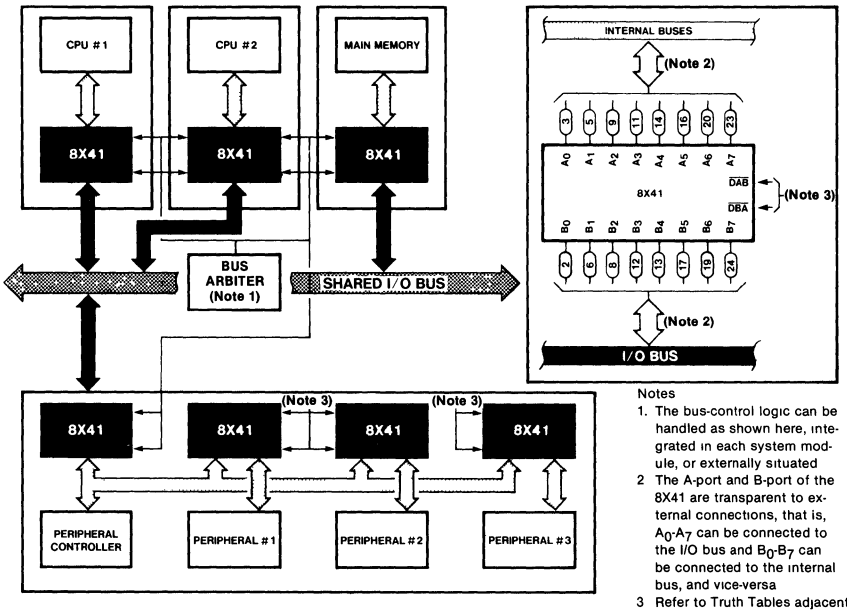
8X41 TIMING DIAGRAM



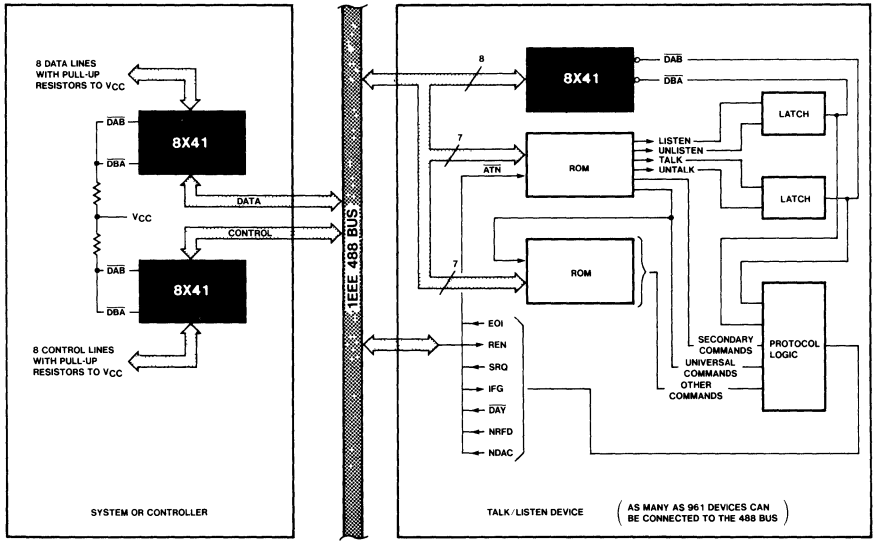
USING THE 8X41 IN A BUS-SHARED CONFIGURATION



Notes

1. The bus-control logic can be handled as shown here, integrated in each system module, or externally situated
2. The A-port and B-port of the 8X41 are transparent to external connections, that is, A_0-A_7 can be connected to the I/O bus and B_0-B_7 can be connected to the internal bus, and vice-versa
3. Refer to Truth Tables adjacent to Figure 1 for data control capabilities

INTERFACING 8X41 TO IEEE 488 BUS



FIFO RAM CONTROLLER (FRC) 8X60

DESIGN FEATURES

- **12-Bit FIFO Address Generator**
- **Data Rate Exceeding 8MHz**
- **Asynchronous Read/Write Operations**
- **Three-State Address Outputs**
- **User-Defined Word Width**
- **Specifically Designed for Use with High-Speed Bipolar RAMs (Adaptable for Use with MOS RAMs)**
- **TTL Input and Output**
- **16mA Address-Drive Capability**

USE AND APPLICATION

- **Interface Between Independently-Clocked Systems**
- **Buffer Memories for Disk and/or Tape**
- **Data Communication Concentrators**
- **CPU/Terminal Buffering**
- **DMA Applications**
- **CRT Terminals**

PRODUCT DESCRIPTION

The Signetics 8X60 FIFO RAM Controller (FRC) is an address and status generator designed to implement a high-speed/high-capacity First-In/First-Out (FIFO) stack utilizing standard off-the-shelf RAMs—see **APPLICATIONS** on the last page of this data sheet. The FRC can control up to 4096 words of buffer memory; intermediate buffer sizes can be selected—refer to the memory length table on the next page. Built-in arbitration logic handles read/write operations on a first-come/first-served basis.

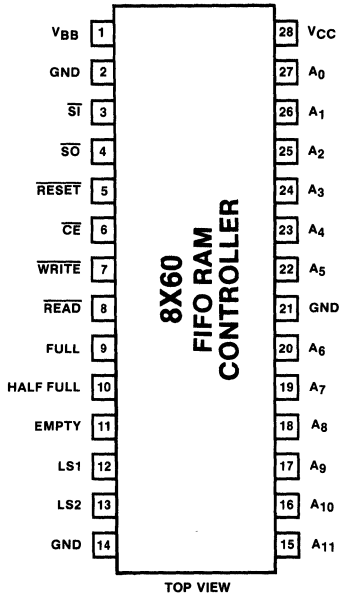
As shown in Figure 1, the FRC consists of:

- A 12-Bit Write Address Generation Counter (Counter #1) and a 12-Bit Read Address Generation Counter (Counter #2).
- A 12-Bit Up/Down Status Counter (Counter #3).
- Twelve Three-State Address Drivers.
- Control Logic.

The two address counters, #1 and #2, respectively, are used to generate write and read addresses; the outputs of these counters are multiplexed to the three-state address drivers. Counter #3 generates *full, empty,* and *half full* status.

PACKAGE AND PIN DESIGNATIONS

N, FQ PACKAGE



TOP VIEW

ORDER NUMBERS

N8X60N, RB8X60F

PIN NO.	IDENTIFIER	FUNCTION
1	V_{BB}	Supply voltage for internal circuits.
2, 14, 21	GND	Circuit ground.
3	$\overline{SI}$	Shift-In request for write cycle; active-low input
4	$\overline{SO}$	Shift-Out request for read cycle; active-low input.
5	$\overline{RESET}$	Active-low master reset input.
6	$\overline{CE}$	Active-low chip enable input
7	$\overline{WRITE}$	Write cycle address valid; active-low output
8	$\overline{READ}$	Read cycle address valid, active-low output
9	FULL	Memory full status output, also, override input capability. Active when *high*.
10	HALF FULL	Memory half-full status output, active-high
11	EMPTY	Memory empty status output; also, override input capability. Active when *high*
12	LS1	Least significant bit (LSB) of the memory length select input
13	LS2	Most significant bit (MSB) of the memory length select input
15–20 22–27	A_{11}–A_0	Three-state address outputs, A_0 = LSB
28	V_{CC}	Supply voltage.

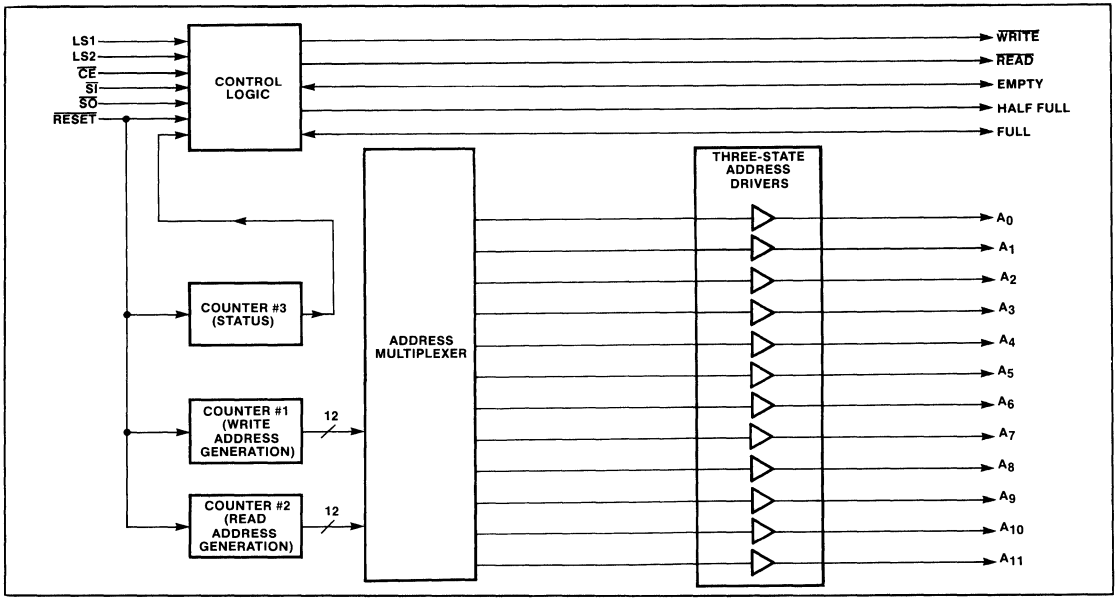


Figure 1. Functional Block Diagram of FIFO RAM Controller

FUNCTIONAL OPERATION

The FRC operates in either of two basic modes—*write* into the FIFO buffer memory or *read* from the FIFO buffer memory. These two operations are described in subsequent paragraphs and the complete sequence is summarized in Table 1. Typical Write/Read timing relationships, arbitration logic, and chip-enable control are shown in the **Timing Diagrams.**

FIFO BUFFER MEMORY—WRITE CYCLE

To perform a write operation, $\overline{SO}$ must be *high* and SI must be *low*. When these conditions exist and other control parameters (Table 1) are satisfied, the write address in Counter #1 (Figure 1) is output to the address bus via the multiplexer and $\overline{WRITE}$ output goes *low*. (*Note.* Normally, the $\overline{WRITE}$ output goes *low* after the address output becomes stable—refer to *WRITE CYCLE TIMING DIAGRAM*. The $\overline{WRITE}$ output may then act as a *write* or *chip* enable for the RAMs that are used to implement the memory.)

When the *write* cycle is ended ($\overline{SI}$ is forced high), the $\overline{WRITE}$ output goes *high*, the address output buffers return to a high-impedance state, Counter #1 (Write Address Generation) and Counter #3 (Status) are both incremented, and Counter #2 (Read Address Generation) remains unchanged.

FIFO BUFFER MEMORY—READ CYCLE

To perform a read operation, $\overline{SI}$ must be *high* and $\overline{SO}$ must be *low*. When these conditions exist and other control parameters (Table 1) are satisfied, the read address contained in Counter #2 (Figure 1) is output to the address bus and the $\overline{READ}$ output goes *low*.

When the *read* cycle is ended ($\overline{SO}$ is forced *high*), the $\overline{READ}$ output goes *high*, the output buffers return to a high-impedance state, Counter #2 (Read Address Generation) is incremented, Counter #3 (Status) is decremented, and Counter #1 (Write Address Generation) remains unchanged.

CONTROL LOGIC

To prevent the possibility of operational conflicts. $\overline{SI}$ and $\overline{SO}$ are treated on a first-come/first-served basis; these two input signals are controlled by internal arbitration logic—refer to the applicable **TIMING DIAGRAMS** and **AC CHARACTERISTICS** for functional and timing relationships. If one cycle is requested while the other cycle is in progress, the requested cycle will commence as soon as the current-cycle is complete (provided other control parameters are satisfied).

As shown in the accompanying diagram, the buffer length of the FIFO memory can be hardware-selected via the Length Select (LS1, LS2) inputs. When less than the maximum length is selected, the unused high-order bits of the address outputs are held in the high-impedance state.

MEMORY LENGTH

LS1	LS2	HALF LENGTH	FULL LENGTH
L	L	2048	4096
H	L	32	64
L	H	512	1024
H	H	128	256

Generation of the status output signals (HALF FULL, FULL and EMPTY) is a function of the Length Select (LS1, LS2) inputs and the current state of Status Counter #3. In general, the status outputs reflect the conditions that follow:

- **HALF FULL**—this status output signals goes *high* on the positive-going edge of $\overline{SI}$ if the MSB of the selected length of Counter #3 becomes a "1". The HALF FULL signal will go from *high-to-low* on the positive-going edge of $\overline{SO}$ when, after the *read* cycle, the selected length of Counter #3 changes from "100 . 00" to "011 . .11". For example, if the selected memory length is 256 words (FULL = 256), then HALF FULL = 128 words; hence, on the

positive-going edge of $\overline{SO}$ when Counter #3 reaches a count of 127, the HALF FULL output will go from *high*-to-*low*

- **FULL**—this signal serves both as a status output and as an override input The FULL signal goes *high* on the negative-going edge of $\overline{SI}$ if all bits of Counter #3 for selected length are equal to "1" The FULL output goes from *high*-to-*low* on the negative-going edge of $\overline{SO}$
- **EMPTY**—this signal also serves as a status output and as an override input On the negative-going edge of $\overline{SO}$, the EMPTY output is driven *high* if Status Counter #3 contains a value of "1", on the positive-going edge of $\overline{SO}$, the counter is decremented to "0" The EMPTY output goes from *high*-to-*low* on the negative-going edge of $\overline{SI}$

Once the FULL signal is *high*, further Write Cycle Requests ($\overline{SI}$ = low) are ignored; similarly, once the EMPTY signal is *high*, further Read Cycle requests ($\overline{SO}$ = low) are ignored. However, to accommodate diversified applications, the FULL and EMPTY outputs are open-collector with on-chip 4 7K passive pull-up resistors If either the FULL or EMPTY pins are forced *low* via external control, the corresponding *write* or *read* cycle may resume (provided the external FULL or EMPTY input is held *low* until the corresponding $\overline{WRITE}$ or $\overline{READ}$ output goes *low*) and the address/status counters will continue normal operation*—refer to Table 1

The user must force the $\overline{RESET}$ input *low* to initialize the chip (*Note.* If the $\overline{RESET}$ signal is driven *low* during a *write* or *read* cycle, the address output may have a short period of uncertainty before assuming a high-impedance state) The following actions occur when $\overline{RESET}$ is active

- All internal counters are set to "0"
- All address output lines are forced to the high-impedance state
- HALF FULL and FULL outputs are forced *low*
- $\overline{WRITE}$, $\overline{READ}$, and EMPTY outputs are forced high

When $\overline{CE}$ is *high*, the address output lines are forced to the high-impedance state, further *write* or *read* cycle requests are ignored, and all counters remain unchanged If $\overline{CE}$ switches from *low*-to-*high* during a *write* or *read* cycle, the cycle in progress is always completed before the disabled state is entered For details of these operations, refer to the timing information shown later in this data sheet

*Refer to **Note** on inside back cover

Table 1. Summary of Operation

INPUTS				INITIAL	RESULTING OUTPUTS			
$\overline{RESET}$	$\overline{CE}$	$\overline{SI}$	$\overline{SO}$	CONDITIONS	$\overline{WRITE}$	$\overline{READ}$	ADDRESS BUS	COMMENTS
L	X	X	X		H	H	Hi-Z	Reset all counters to 0
H	X	H	H		H	H	Hi-Z	No action
H	L	L	H	FULL = L	L	H	Write address from Ctr #1	Shift into FIFO stack (Write Cycle)
H	L	L	H	FULL = H	H	H	Hi-Z	Stack full (Write inhibited)
H	L	H	L	EMPTY = L	H	L	Read address from Ctr #2	Shift out of FIFO stack (Read Cycle)
H	L	H	L	EMPTY = H	H	H	Hi-Z	Stack empty (Read inhibited)
H	L	L	↓	Write cycle in progress	L	H	Write address from Ctr #1	Continue write cycle (until $\overline{SI}$ goes high)
H	L	↓	L	Read cycle in progress	H	L	Read address from Ctr #2	Continue read cycle (until $\overline{SO}$ goes high)
H	L	L	L	EMPTY = H	L	H	Write address from Ctr #1	Shift in (Read inhibited)
H	L	L	L	FULL = H	H	L	Read address from Ctr #2	Shift out (Write inhibited)
H	L	↑	H	Write cycle in progress	↑	H	Goes to Hi-Z	Increment write address counter #1 and status counter #3
H	L	H	↑	Read cycle in progress	H	↑	Goes to Hi-Z	Increment read address counter #2, decrement status counter #3
H	L	↑	L	Write cycle in progress (Note 1)	↑	↓	Changes to read address from Ctr #2	Increment write address counter #1 and status counter #3
H	L	L	↑	Read cycle in progress (Note 2)	↓	↑	Changes to write address from Ctr #1	Increment read address counter #2, decrement status counter #3
H	H	↓	H		H	H	Hi-Z	Chip disabled
H	H	H	↓		H	H	Hi-Z	Chip disabled
H	↑	L	X	FULL = L, write cycle begun (Note 1)	L	H	Write address from Ctr #1	Continue write cycle (until $\overline{SI}$ goes high)
H	↑	X	L	EMPTY = L, read cycle begun (Note 2)	H	L	Read address from Ctr #2	Continue read cycle (until $\overline{SO}$ goes high)
H	↓	L	L	FULL = L, EMPTY = L	—	—	—	This set of conditions should be avoided

NOTES
1 Write cycle will occur if either $\overline{SI}$ goes *low* before $\overline{SO}$ goes *low* or EMPTY = H when $\overline{SO}$ goes *low*
2 Read cycle will occur if either $\overline{SO}$ goes *low* before $\overline{SI}$ goes *low* or FULL = H when $\overline{SI}$ goes *low.*

ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{BB}	Supply Voltage for Internal Circuits	+4	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_O	Off-State Output Voltage	+5.5	Vdc
T_{STG}	Storage Temperature Range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

CONDITIONS: Commercial— $V_{CC} = 5.0V (\pm 5\%)$, $V_{BB} = 1.5V (\pm 5\%)$[1], $0°C \le T_A \le 70°C$
Military— $V_{CC} = 5.0V (\pm 10\%)$, $V_{BB} = 1.5V (\pm 10\%)$[1], $T_A \le -55°C$, $T_C \le 125°C$

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL) MIN	TYP[2]	MAX	LIMITS (MILITARY) MIN	TYP[2]	MAX	UNITS
V_{IH}	High level input voltage	Note 3	2.0			2.0			V
V_{IL}	Low level input voltage				0.8			0.8	V
V_{OH}	High level output voltage: All outputs except FULL and EMPTY	V_{CC} = Min; I_{OH} = −2.6mA	2.7	3.5		2.5	3.5		V
V_{OL}	Low level output voltage: Address Bus, $\overline{WRITE}$, $\overline{READ}$	V_{CC} = Min, I_{OL} = 16mA		0.38	0.5		0.38	0.5	V
	HALF FULL, FULL, and EMPTY	V_{CC} = Min; I_{OL} = 8mA		0.35	0.5		0.35	0.5	V
V_{CD}	Diode clamp voltage: All inputs except FULL and EMPTY	V_{CC} = Min; I_{CD} = −18mA	−1.5	−0.8		−1.5	−0.8		V
I_{IH}	High level input current: All inptus except FULL and EMPTY	V_{CC} = Max; V_{IH} = 2.7V		0.1	20		0.1	20	μA
	FULL and EMPTY	V_{CC} = Max; V_{IH} = 2.7V; Stack FULL or Stack EMPTY (Note 3)		−470	−750		−470	−900	μA
I_{IL}	Low level input current: All inputs except FULL and EMPTY	V_{CC} = Max; V_{IL} = 0.4V		−0.17	−0.4		−0.17	−0.4	mA
	FULL and EMPTY	V_{CC} = Max; V_{IL} = 0.4V; Stack FULL or Stack EMPTY		−1.12	−1.8		−1.12	−1.8	mA
I_{OH}	High level output current: FULL, EMPTY	V_{CC} = Min, V_{OH} = V_{CC} (min)		15	100		15	100	μA
I_{OZH}	High-Z output current (HIGH); Address Bus (Three-State)	V_{CC} = Max; V_{OUT} = 2.4V		0.9	20		0.9	20	μA
I_{OZL}	High-Z output current (LOW); Address Bus (Three-State)	V_{CC} = Max; V_{OUT} = 0.5V		−0.6	−20		−0.6	−20	μA
I_I	Input leakage current: All inputs except FULL and EMPTY	V_{CC} = Max; V_{IN} = 5.5V		0.03	0.1		0.03	0.1	mA
I_{OS}	Short-circuit output current: Address Bus and HALF FULL	V_{CC} = Max; V_{OH} = 0V	−15	−68	−100	−15	−68	−100	mA
	$\overline{WRITE}$, $\overline{READ}$	V_{CC} = Max; V_{OH} = 0V	−40	−73	−100	−40	−73	−100	mA
I_{CC}	Supply current from V_{CC}	V_{CC} = Max; Address Bus = High-Z, 0°C →		81	140	−55°C →		140	mA
		70°C →		81	110	125°C →		100	
I_{BB}	Supply current from V_{BB}	V_{BB} = Max, 0°C →		63	95	−55°C	63	100	mA
		70°C →		63	85	125°C	63	90	

NOTES
1. V_{BB} can be obtained from a regulated 1.5V supply, alternately, proper supply current (I_{BB}) can be obtained by connecting a 56-ohm (±5%, 0.5W) resistor in series with V_{CC} as shown later in the **APPLICATIONS** diagram
2. Typical limits are. V_{CC} = 5.0V, T_A = 25°C
3. Because of the internal pull-up resistor on the FULL and EMPTY pins, a negative current is required to force the required voltage
4. V_{OL} at I_{OL} = 4mA for Military part

CONDITIONS: Commercial— V_{CC} = 5.0V (±5%), V_{BB} = 1.5V (±5%), 0°C ≤ T_A ≤ 70°C; Military— V_{CC} = 5.0V (±10%), V_{BB} = 1.5V (÷10%), T_A ≤ −55°C, T_C ≤ 125°C; Loading— See TEST LOADING CIRCUITS

AC ELECTRICAL CHARACTERISTICS

PARAMETERS	REFERENCES FROM	REFERENCES TO	TEST CONDITIONS	LIMITS (Commercial) Min	Typ	Max	LIMITS (Military) Min	Typ	Max	UNITS
PULSE WIDTHS										
T_{LH} $\overline{SI}$ high	↑$\overline{SI}$	↓$\overline{SI}$	Stack approaching FULL (Note 1)	25	13		25	13		ns
T_{DH} $\overline{SO}$ high	↑$\overline{SO}$	↓$\overline{SO}$	Stack approaching EMPTY (Note 1)	30	16		30	16		ns
WRITE CYCLE TIMING										
T_{LA} Address stable delay	↓$\overline{SI}$	An	FULL = Low; $\overline{SO}$ = High		40	55		40	60	ns
T_{AW} Address lead time	An	↓$\overline{WRITE}$		3			0			ns
T_{LAW} $\overline{WRITE}$ output active delay	↓$\overline{SI}$	↓$\overline{WRITE}$	FULL = Low; $\overline{SO}$ = High	35	51	65	35	51	70	ns
T_{LW} $\overline{WRITE}$ output inactive dalay	↑$\overline{SI}$	↑$\overline{WRITE}$			3	10		3	10	ns
T_{WA} Address lag time	↑$\overline{WRITE}$	An		20	34		10	34		ns
T_{LT} Address output disable	↑$\overline{SI}$	An(Hi-Z)			37	60		37	60	ns
T_{LF} FULL status active delay	↓$\overline{SI}$	↑FULL	Stack approaching FULL; $\overline{SO}$ = High		39	65		39	70	ns
T_{LE} EMPTY status inactive delay	↓$\overline{SI}$	↓EMPTY	Stack = EMPTY		40	65		40	65	ns
T_{HFH} HALF-FULL status active delay	↑$\overline{SI}$	↑HALF FULL	Stack approaching HALF-FULL		30	45		30	50	ns
T_{DW} $\overline{WRITE}$ output active after read	↑$\overline{SO}$	↓$\overline{WRITE}$	Both $\overline{SI}$ & $\overline{READ}$ = Low		74	95		74	100	ns
READ CYCLE TIMING										
T_{DA} Address stable delay	↓$\overline{SO}$	An	EMPTY = Low; $\overline{SI}$ = High		40	55		40	60	ns
T_{AR} Address lead time	An	↓READ		−1			−5			ns
T_{DAR} $\overline{READ}$ output active delay	↓$\overline{SO}$	↓READ	EMPTY = Low; $\overline{SI}$ = High	30	48	65		35	70	ns
T_{DR} $\overline{READ}$ output inactive delay	↑$\overline{SO}$	↑$\overline{READ}$			5	10		5	10	ns
T_{RA} Address lag time	↑$\overline{READ}$	An		20	32		10	32		ns
T_{DT} Address output disable	↑$\overline{SO}$	An (Hi-Z)			37	60		37	60	ns
T_{DE} EMPTY status active delay	↓$\overline{SO}$	↑EMPTY	Stack approaching EMPTY; $\overline{SI}$ = High		38	50		38	50	ns
T_{DF} FULL status inactive delay	↓$\overline{SO}$	↓FULL	Stack = FULL		38	50		38	65	ns
T_{HFL} HALF-FULL status inactive delay	↑$\overline{SO}$	↓HALF FULL	Stack exactly HALF-FULL		54	75		54	85	ns
T_{LR} $\overline{READ}$ output active after wirte	↑$\overline{SI}$	↓$\overline{READ}$	Both $\overline{SO}$ & $\overline{WRITE}$ = Low		70	90		70	100	ns
CHIP ENABLE TIMING (WIRTE)										
T_{HEW} Chip enable hold time[2]	↓$\overline{SI}$	↑$\overline{CE}$	FULL = Low; $\overline{SO}$ = High	10	1		10	1		ns
T_{SEW} Chip disable setup time[3]	↑$\overline{CE}$	↓$\overline{SI}$	FULL = Low; $\overline{SO}$ = High	10	1		10	1		ns
T_{PEW} Chip enable delay time	↓$\overline{CE}$	↓$\overline{WRITE}$	FULL = Low; $\overline{SI}$ = Low; $\overline{SO}$ = High		69	95		69	110	ns
CHIP ENABLE TIMING (READ)										
T_{HER} Chip enable hold time[2]	↓$\overline{SO}$	↑$\overline{CE}$	EMPTY = Low; $\overline{SI}$ = High	10	1		10	1		ns
T_{SER} Chip disable setup time[3]	↑$\overline{CE}$	↓$\overline{SO}$	EMPTY = Low, $\overline{SI}$ = High	10	1		10	1		ns
T_{PER} Chip enable delay time	↓$\overline{CE}$	↓$\overline{READ}$	EMPTY = Low; $\overline{SO}$ = Low; $\overline{SI}$ = High		64	95		64	105	ns
RESET TIMING										
T_{RR} $\overline{RESET}$ recovery	↑$\overline{RESET}$	↓$\overline{WRITE}$	$\overline{SI}$ = Low		57	75		57	80	ns
T_{RL} $\overline{RESET}$ pulse width (low)	↓$\overline{RESET}$	↑$\overline{RESET}$		25	8		25	8		ns
FULL/EMPTY OVERRIDE TIMMING:										
T_{FW} Override Recovery for FULL	↓FULL	↓$\overline{WRITE}$	Stack = Full; $\overline{SI}$ = Low; $\overline{SO}$ = High		70	95		70	110	ns
T_{ER} Overrıde Recovery for EMPTY	↓EMPTY	↓$\overline{READ}$	Stack = EMPTY; $\overline{SO}$ = Low; $\overline{SI}$ = High		65	90		65	105	ns

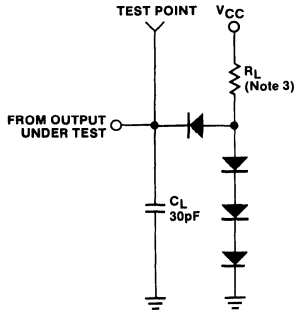
NOTES 1 Such that write/read request is inhibited after stack becomes full/empty

2 The earliest rising edge of $\overline{CE}$ such that the $\overline{WRITE}$ or $\overline{READ}$ output always occurs

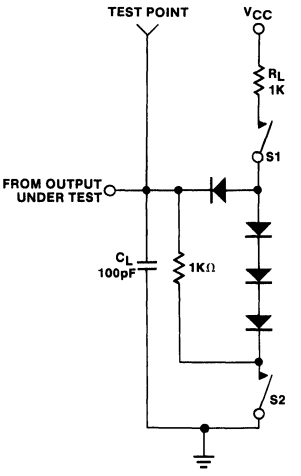
3 The latest rising edge of $\overline{CE}$ such that the $\overline{WRITE}$ or $\overline{READ}$ output never occurs

TEST LOADING CIRCUITS

APPLICABLE PINS: $\overline{WRITE}$ (7), $\overline{READ}$ (8), HALF FULL (10)

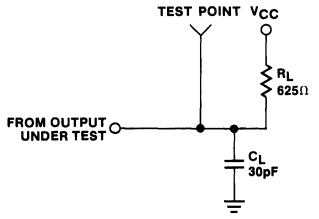


APPLICABLE PINS: A_n (15-20, 22-27)



OUTPUT STATE		SWITCH POSITION	
FROM	TO	S1	S2
Low	High	Closed	Closed
High	Low	Closed	Closed
High	HI-Z	Closed	Closed
Low	HI-Z	Closed	Closed
HI-Z	High	Open	Closed
HI-Z	Low	Closed	Open

APPLICABLE PINS: FULL (9) AND EMPTY (11)

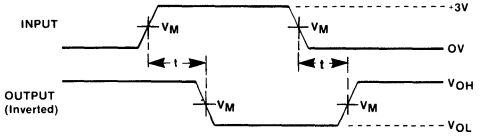


NOTES
1 In all cases C_L includes probe and jig capacitance
2 All diodes are 1N916, 1N3064, or equivalent
3 For $\overline{READ}$ and $\overline{WRITE}$ outputs, R_L = 280 ohms, for HALF FULL output, R_L = 2K ohms

7

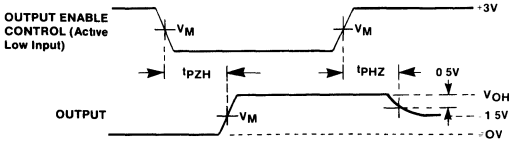
AC TEST WAVEFORMS

PROPAGATION DELAY
(Typical Example)

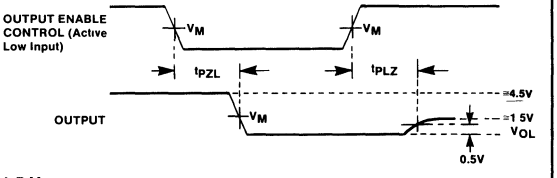


Note
Pulse widths and Setup/Hold times are measured using the same reference points as above waveform

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL

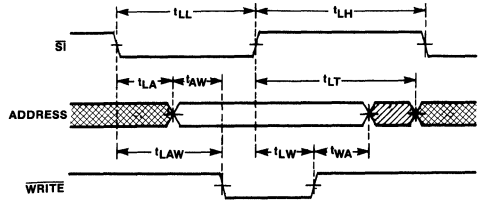


V_M = 1.5 V

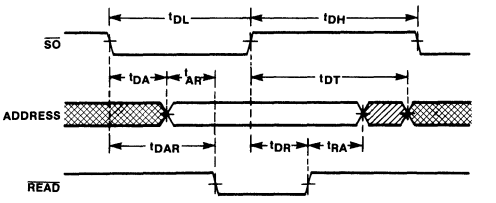
FIFO RAM CONTROLLER (FRC) 8X60

TIMING DIAGRAMS

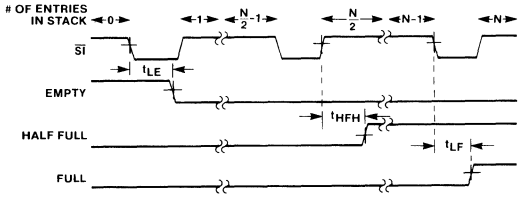
WRITE CYCLE TIMING



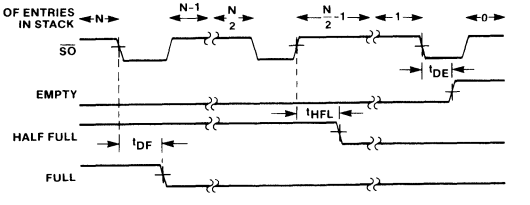
READ CYCLE TIMING



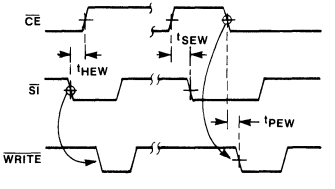
STATUS OUTPUT TIMING-WRITE



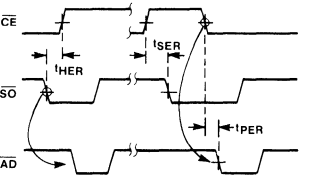
STATUS OUTPUT TIMING-READ



CHIP ENABLE TIMING WRITE*

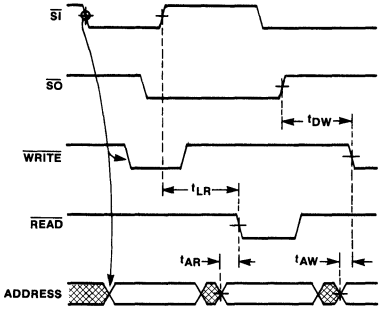


CHIP ENABLE TIMING READ*

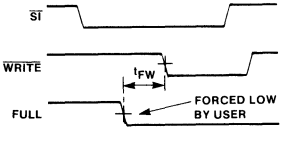


* The rising edge of $\overline{CE}$ should not occur within 10-nanoseconds before or after a falling edge of $\overline{SI}$ or $\overline{SO}$.

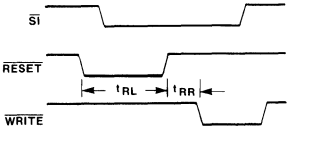
CHANGE OF CYCLE TIMING



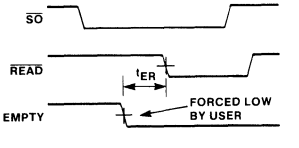
FULL OVERRIDE TIMING



RESET TIMING



EMPTY OVERRIDE TIMING



KEY

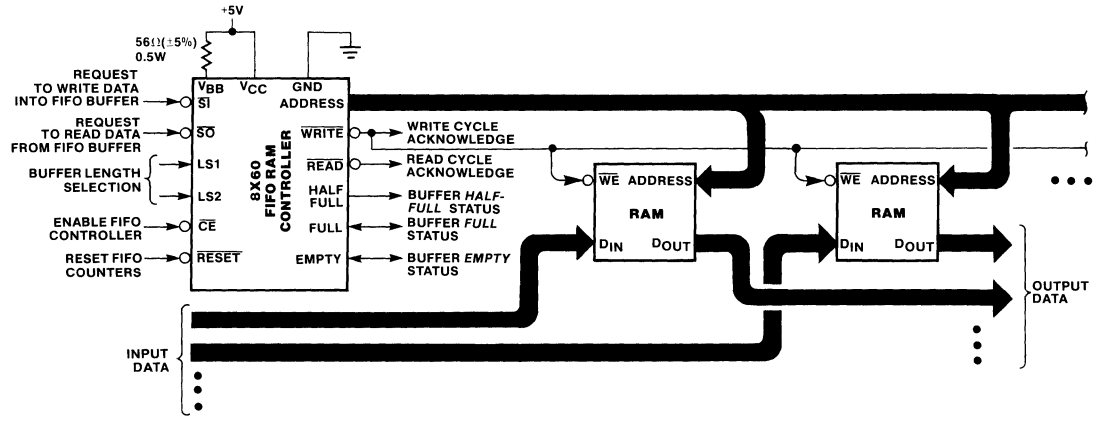
High-impedance state

Changing data

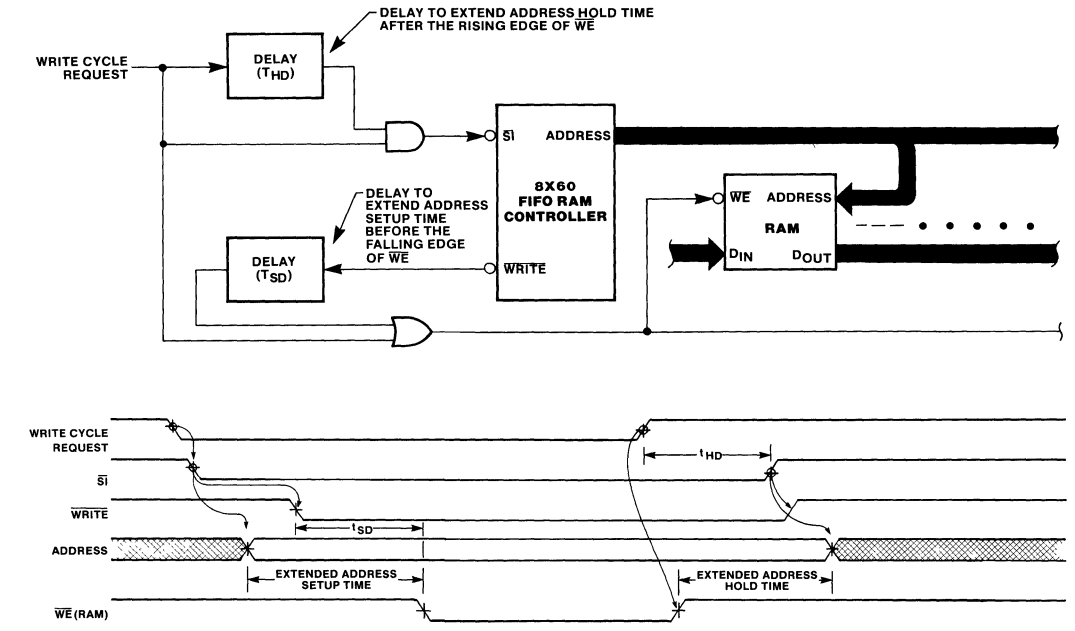
FIFO RAM CONTROLLER (FRC) 8X60

APPLICATIONS

IMPLEMENTATION OF A FIFO BUFFER USING THE 8X60 AND HIGH SPEED RAM



USING 8X60 WITH HIGH-DENSITY MOS RAMs



7

ERROR DETECTION and CORRECTION (EDC) UNIT 2960

FEATURES

- **Boosts Memory Reliability — Corrects all single-bit errors. Detects all double and some triple-bit errors. Reliability of dynamic RAM systems is increased more than 60-fold**
- **Very High Speed — Perfect for MOS microprocessor minicomputer and mainframe systems.**
  - **— Data in to error detect 32ns worst case**
  - **— Data in to corrected data out 65ns worst case**

  High performance systems can use the Signetics EDC in the check-only mode to avoid memory system slowdown
- **Replaces 25 to 50 MSI chips — All necessary features are built-in to the Signetics 2960 including diagnostics data in data out and check bit latches**
- **Handles Data Words From 8 to 64 Bits — The Signetics 2960 is cascadable: 1 EDC for 8 or 16 bits 2 for 32 bits 4 for 64 bits**
- **Easy Byte Operations — Separate byte enables on the data out latch simplifly the steps and cuts the time required for byte writes**
- **Built-in Diagnostics — The processor may completely exercise the EDC under software control to check for proper operation.**

PRODUCT DESCRIPTION

The Signetics 2960 Error Detection and Correction Unit (EDC) (Figure 1) contains the logic necessary to generate check bits on a 16-bit data field according to modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the EDC will correct any single bit error and will detect all double and some triple bit errors. For 16-bit words, 6 check bits are used. The 2960 can be expanded to operate 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome available on separate outputs for data logging.

The Signetics 2960 also features two diagnostic modes, in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions. The product is supplied in a 48 lead hermetic DIP package.

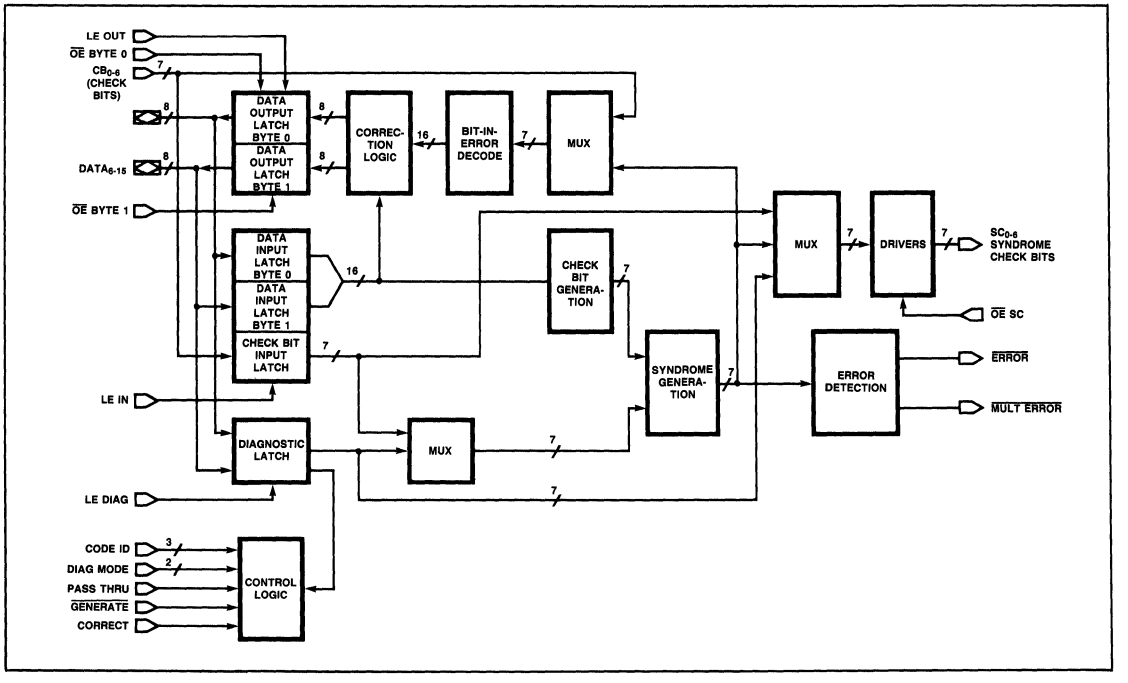


Figure 1. Block Diagram of 2960 Error Detection and Correction Unit

DYNAMIC MEMORY CONTROLLER 2964B

FEATURES

- **Operating Flexibility—controls 16K or 64K dynamic RAMSs**
- **8-Bit Refresh Counter—refresh address generation, clear input, and selectable terminal count (128 or 256) output**
- **Row Address Decoder—four active Row Address Select (RAS) outputs during refresh**
- **On-Chip Latches—dual 8-bit address latches and RAS decoder latches**
- **User-Selectable Refresh Modes—burst, distributed, or transparent**
- **3-port, 8-bit address multiplexer with Schottky speed**
- **Non-inverting address for RAS and CAS signal paths**

PRODUCT DESCRIPTION

The Signetics 2964 Dynamic Memory Controller (DMC) provides address multiplexing, refresh address generation, and Row/Column control for MOS dynamic memories of any data width. The eight bit address path is designed for 64K RAMs but can be used equally well with 16K RAMs. Sixteen address input latches and two row address select latches (for higher order address) allow the DMC to control up to 256K words of memory (with 64K RAMs) by using the internal row address decoder to select from one-of-four banks of RAMs.

FUNCTIONAL OPERATION

The Signetics 2964B Dynamic Memory Controller (Figure 1) replaces a dozen MSI devices by grouping several unique functions. Two 8-bit latches capture and hold the memory address. These latches and a clearable, 8-bit refresh counter feed into an 8-bit, 3-input, Schottky speed MUX, for output to the DRAM address lines.

The 2964B also includes a special RAS decoder and CAS buffer. Placing these functions on the same chip minimizes the time skew between output functions which would otherwise be separate MSI chips, and therefore, allows a faster memory cycle time by the amount of skew eliminated.

The RAS Decoder allows upper addresses to select one-of-four banks of DRAM by determining which bank receives a RAS input. During refresh ($\overline{RFSH}$ = LOW), the decoder mode is changed to four-of-four and all banks of memory receive a RAS input for refresh in response to a RASI active LOW input. CAS is inhibited during refresh.

Burst mode refresh is accomplished by holding RFSH low and toggling RASI.

A_{15} is a dual function input which controls the refresh counter's range. For 64K DRAMs, it is an address input. For 16K DRAMs, it can be pulled to + 12V through 1K to terminate the refresh count at 128 instead of 256.

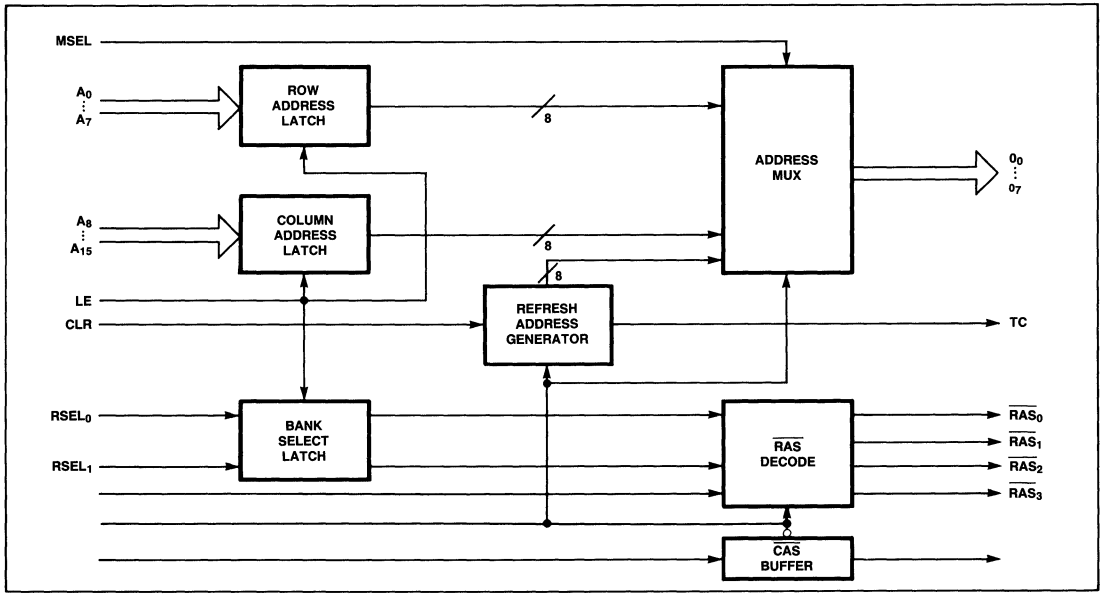


Figure 1. Block Diagram of 2964B Dynamic Memory Controller

NOTES

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Section 8
Semicustom Service

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8

THE COMPLETE SEMICUSTOM SOLUTION

To meet your semicustom needs Signetics has developed a comprehensive semicustom service that offers one-stop shopping with state-of-the-art technology. This service gives you a choice of silicon systems ranging from CMOS to T^2L and ECL, the widest range of semicustom products in the industry, with performance capable of meeting all your semicustom logic needs. All are supported with complete in-house capability for processing and fabrication, will full service CAD, which simplifies your design task and guarantees first-pass success for your semicustom program.

STATE-OF-THE-ART CAD

Signetics' CAD system encompasses the complete semicustom design process, from schematic input through auto place and route, design rule checking and test generation. This fully automated procedure speeds design and makes your job easy and guarantees that your semicustom chip is developed without error and on schedule. With Signetics' CAD you are using the most up-to-date semicustom design system available.

SCHEMATIC INPUT — FAST AND EASY

In designing a semicustom chip the first step is to enter your circuit into the computer. The most advanced method of circuit entry is Signetics schematic input system. This system only requires you to enter your schematic by use of a keyboard and mouse, which is fast and easy. The computer then automatically converts your schematic to a net list which is used for simulation and auto place and route.

For circuit entry Signetics gives you a choice of two schematic input systems, one with software originally developed by Future Net and one by Mentor. The Future Net system operates on a low cost IBM Personal Computer which you can use in your own shop or in a Signetics' sales office. The Mentor schematic input system operates on an Apollo computer which is available in one of Signetics' design centers. With either input system you will find the schematic entry step fast and easy.

COMPUTER SIMULATION — EASY AND SURE

Once your schematic has been entered, the next and final step is to simulate the logic using our TEGAS 5 Program. To do this you enter your test vectors then submit the job from your IBM PC to Signetics' computer via telephone link. If you are using one of our design centers the simulation can be performed on-site with the Apollo computer. Upon completion of simulation the computer returns to you the resulting output vectors to allow you to check your design. Computer simulation ensures that your circuit is functioning properly before Signetics manufactures your semicustom chip.

WHAT SIGNETICS DOES — MORE CAD

After completion of simulation your job is finished. Signetics takes over and completes the manufacture of your semicustom device, which involves the use of additional Signetics CAD. The effects of wire delay, if any, are compensated using our WIDGET program. Using your net list which was produced by the schematic input system, Signetics performs a comprehensive design rule check, then routes the chip automatically. Using your test vectors Signetics automatically produces a test tape for final testing using our SENGEN program. The routed chip is then masked and processed using our advanced semiconductor methodology.

In performing Signetics part of the task, a key step is auto place and route, and Signetics has placed a high emphasis on developing these programs. The MEDS program automatically routes at the gate level and is used for gate arrays and creation of macros. The CALMP program is used for more advanced structures, such as Signetics FLEXX™ Array. CALMP assembles macros and gates with automatically variable routing space for optimal packing of the chip. These and other similar programs allow Signetics to offer comprehensive use of auto-routing in all our semicustom products.

FULL IN-HOUSE CAPABILITY

As a full capability semiconductor supplier and in semicustom since 1975, Signetics has all the in-house support necessary for producing your semicustom chip. In addition to a full service CAD facility, Signetics has complete masking, wafer fabrication and processing, including military processing, for Source Control Drawing or MIL STD 883B parts production. This full capability ensures availability of parts and that your semicustom device will be processed according to your needs and on schedule.

A FULL CHOICE OF SILICON

With Signetics you can implement your semicustom requirement with silicon that is advanced in technology and architecture. In technology you have a choice of three levels of CMOS and five kinds of bipolar arrays with gate speed ranging from 8 nsec to 0.5 nsec and various output drive levels. In architecture these products are structured as gate arrays, masterslice, composite cell, and FLEXX™ arrays, with up to 5000 gates and 128 I/Os. These devices have been configured to encompass the complete range of semicustom applications to allow Signetics to meet your own specific needs.

CMOS GATE ARRAYS

Signetics CMOS gate arrays are oxide-isolated, silicon gate devices built on an epi substrate which virtually eliminates latch-up. Input/Output is compatible with CMOS or LSTTL logic. These are highly advanced CMOS gate arrays with a full selection of technology and architecture.

M-Series CMOS Gate Arrays Single layer metal, 330 to 1100 gates, up to 68 I/Os, with 8 nsec gate delay typical for a 2 output gate with 5V V_{DD}.

H-Series CMOS Gate Arrays Single layer metal, 330 to 1100 gates, up to 68 I/Os, with 4 nsec gate delay typical for a 2 output gate with 5V V_{DD}.

SH-Series CMOS Gate Arrays Dual layer metal, 1250 to 5000 gates, up to 128 I/Os, with 2 nsec gate delay typical for a 2 output gate with 5V V_{DD}.

BIPOLAR SEMICUSTOM DEVICES

Signetics bipolar semicustom devices are available with both junction isolation and oxide isolation, for T^2L and ECL applications. They are designed for high speed and high output drive.

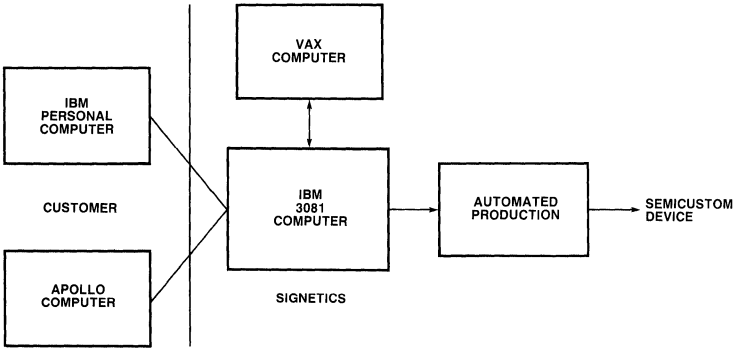
8AXXXX Series ISL Gate Arrays Dual layer metal junction isolated Integrated Schottky Logic for T^2L applications, 1200 to 2100 gates, up to 76 I/Os, with 4 nsec gate speed typical. Full military criteria.

Composite Cell Logic Three standard cell dual-layer metal libraries ranging from 3.5 nsec to 5 nsec typical gate delay. Up to 1000 actual gates, I/Os limited by package. Up to 80 mA output drive for T^2L applications. Full military criteria.

8HXXXX Series ISL Gate Arrays Dual layer metal, oxide isolated Integrated Schottky Logic for T^2L applications, 1600 to 3200 gates, up to 120 I/Os, with 1.5 nsec gate speed typical. Full military criteria.

FLEXX™ Array User-created or standard cells, dual-layer metal, variable routing space for optimal chip size, up to 2000 gates, I/Os limited by package. Oxide-isolated Integrated Schottky Logic for T^2L applications, 1.5 nsec gate delay typical. Full military criteria.

ACE Masterslice Array Oxide isolated CML for ECL 10 K, ECL 100 K and T^2L applications, 600 to 2200 gates, optional RAM on chip, up to 128 I/Os, 0.5 nsec gate delay, air cooled.



Signetics Computer Aided Design Facility used for design of semicustom devices. Provides remote access for schematic input and simulation. Signetics completes the design with design rule checking, automatic place and route, and automatic test tape generation before producing the semicustom device.

NOTES

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Section 9
Semicustom Products

INDEX

FEATURES

- **3-micron geometry (first metal)**
- **Internal gate delays as low as 300 picoseconds (average gate delay of 450 picoseconds)**
- **Expandable 80-cell MACRO library**
- **Mask-selectable rise/fall times for I/O interface cells**
- **Bidirectional and TTL interfaces**
- **10K/100K ECL compatibility**
- **Computer aided design (CAD) for layout, simulation, and testing**
- **Mature process (SUBILO P)**
- **Pin grid array packages for easy socket insertion**
- **25 and 50 ohm drive capability**

PRODUCT DESCRIPTION

The Signetics Advanced Customized ECL (ACE) family of products provides the user with a cost-effective technology, futuristic speeds, and other high-performance alternatives for the design of LSI-based systems. Basic cell designs are implemented with Emitter Coupled and Common Mode Logic (ECL/CML) to guarantee the very best compromise between speed, power, and interface capabilities—see Figure 1 and TECHNICAL SUMMARY that follows.

At present, the ACE product line is available with gate complements of 600, 900, 1320, 1400, and 2200; the 1320 array actually contains 1000 gates with an on-board 320-bit RAM. The 600/900-gate arrays, described in this data sheet, are well-suited for low-cost applications and for use in systems that do not require 25-ohm terminations. To meet the flexibility requirements, the rise-and-fall times for I/O cells of these arrays are mask-selectable and bidirectional and TTL interfaces are standard.

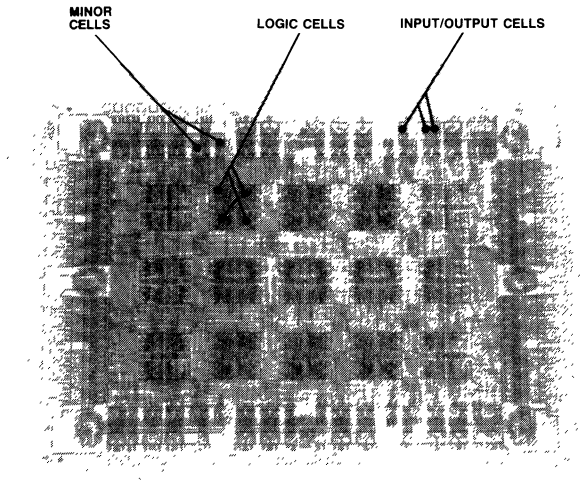
All ACE arrays are I/O compatible with the 10K/100K ECL logic family and all are fabricated with a very mature process; thus, even with 3-micron first-metal geometry, first pass success is a virtual certainty. The speed-power product for devices in the ACE family is in the neighborhood of 1 to 3 picojoules, permitting heat-sink cooling at ambient air temperatures. The ACE family and MACRO library is alternately sourced by a major supplier of semicustom devices.

To summarize, the designer, using ACE, is limited only by innovation and imagination:

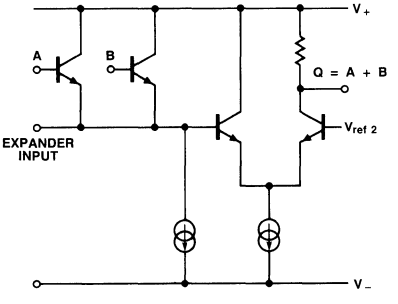
- ECL/CML Technology for SPEED and EFFICIENCY
- Mature process for PRODUCT CERTAINTY
- Computer aided design for QUICK DELIVERY
- Pin grid packages (socket insertion) for RELIABILITY
- Signetics for QUALITY

ORDERING INFORMATION

Contact Local Sales Representative



Typical ACE Array Showing Cell Locations



Typical ACE Cell

Figure 1. Chip Architecture and Typical Circuit

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TECHNICAL SUMMARY OF ACE FAMILY

PARAMETER	ACE 600	ACE 900	ACE 1320	ACE 1400	ACE 2200
Major cells	24	36	48	60	100
Input/output cells	28	28	96	96	128
Input cells	30	42	—	—	—
Worst case noise margin	24 - 45 mV		24 - 45 mV		
Junction temperature range	30 - 125°C		30 - 125°C		
Average prop delay (internal gate)	0.3 - 0.5 ns		0.3 - 0 5 ns		
	10K LEVEL	**100K LEVEL**	**10K LEVEL**	**100K LEVEL**	
Power supply	−5.25V ± 5%	−4.5V ± 5%	−5.25V ± 5%	−4.5V ± 5%	
Power consumption	2.1 - 2 7 mW	1 8 - 2.3 mW	4 6 - 6 3 mW	4 - 5 5 mW	

ACE PACKAGE TYPE AND THERMAL RESISTIVITY SELECTION

	PACKAGE	THERMAL RESISTIVITY (°C/W)		
		HEAT SINK	NO AIR FLOW	5 m/s AIR FLOW
ACE 600 & ACE 900	64 Pin	Yes	25	13
		No	50	25
ACE 1320, ACE 1400 & ACE 2200	144 Pin	Yes	12	6
		No	24	12

FEATURES

- **3-micron geometry (first metal)**
- **Internal gate delays as low as 300 picoseconds (average gate delay of 450 picoseconds)**
- **Expandable 80-cell MACRO library**
- **Mask-selectable rise/fall times for I/O interface cells**
- **Bidirectional and TTL interfaces**
- **10K/100K ECL compatibility**
- **Computer aided design (CAD) for layout, simulation, and testing**
- **Mature process (SUBILO P)**
- **Pin grid array packages for easy socket insertion**
- **25-ohm and 50-ohm load drive capability**

PRODUCT DESCRIPTION

The Signetics Advanced Customized ECL (ACE) family of products provides the user with a cost-effective technology, futuristic speeds, and other high-performance alternatives for the design of LSI-based systems. Basic cell designs are implemented with Emitter Coupled and Common Mode Logic (ECL/CML) to guarantee the very best compromise between speed, power, and interface capabilities—see Figure 1 and TECHNICAL SUMMARY that follows.

At present, the ACE product line is available with gate complements of 600, 900, 1320, 1400, and 2200; the 1320 array actually contains 1000 gates with an on-board 320-bit RAM.

The 1320/1400/2200 gate arrays, described in this data sheet, are particularly well suited for complex applications requiring relatively high gate counts and considerable design flexibility. To meet the flexibility requirements, the rise-and-fall times for I/C cells of these arrays are mask-selectable and bidirectional and TTL interfaces are standard.

All ACE arrays are I/O compatible with the 10K/100K ECL logic family and all are fabricated with a very mature process; thus, even with 3-micron first-metal geometry, first pass success is a virtual certainty. The speed-power product for devices in the ACE family is in the neighborhood of 1 to 3 picojoules, permitting heat-sink cooling at ambient air temperatures. The ACE family and MACRO library is alternately sourced by a major supplier of semicustom devices.

To summarize, the designer, using ACE, is limited only by innovation and imagination:

- ECL/CML Technology for SPEED and EFFICIENCY
- Mature process for PRODUCT CERTAINTY
- Computer aided design for QUICK DELIVERY
- Pin grid packages (socket insertion) for RELIABILITY
- Signetics for QUALITY

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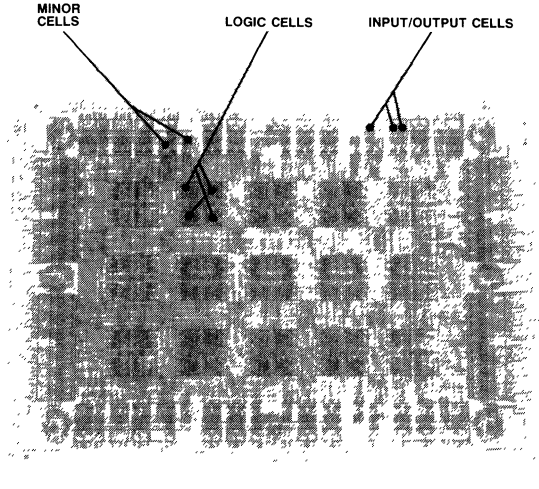
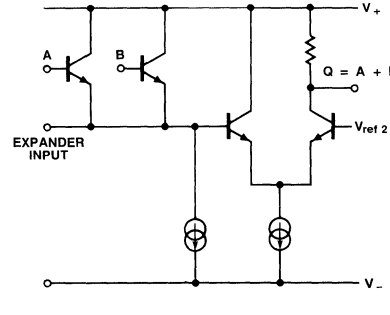


Typical ACE Array Showing Cell Locations



Typical ACE Cell

Figure 1. Chip Architecture and Typical Circuit

TECHNICAL SUMMARY OF ACE FAMILY

PARAMETER	ACE 600	ACE 900	ACE 1320	ACE 1400	ACE 2200
Major cells	24	36	48	60	100
Input/output cells	28	28	96	96	128
Input cells	30	42	—	—	—
Worst case noise margin	24 - 45 mV		24 - 45 mV		
Junction temperature range	30 - 125°C		30 - 125°C		
Average prop delay (internal gate)	0.3 - 0.5 ns		0 3 - 0.5 ns		
	10K LEVEL	**100K LEVEL**	**10K LEVEL**	**100K LEVEL**	
Power supply	−5.25V ± 5%	−4 5V ± 5%	−5.25V ± 5%	−4.5V ± 5%	
Power consumption	2 1 - 2.7 mW	1.8 - 2.3 mW	4.6 - 6.3 mW	4 - 5.5 mW	

ACE PACKAGE TYPE AND THERMAL RESISTIVITY SELECTION

	PACKAGE	THERMAL RESISTIVITY (°C/W)		
		HEAT SINK	NO AIR FLOW	5 m/s AIR FLOW
ACE 600 & ACE 900	64 Pin	Yes	25	13
		No	50	25
ACE 1320, ACE 1400 & ACE 2200	144 Pin	Yes	12	6
		No	24	12

COMPOSITE CELL LOGIC (CCL) SEMI-CUSTOM FAMILY

DESIGN FEATURES

- **Customer designed LSI**
- **Two cell libraries—EPL and ISL**
- **TTL compatible—each cell is functionally similar to the equivalent 7400 Logic Device**
- **Two-layer metal interconnects**
- **PNP or diode inputs**
- **Open-collector, active pullup, or three-state outputs**
- **80-milliampere sink-current capability for output cells**
- **Accommodate custom cell design**
- **Most standard packages available**
- **−55°C to +150°C junction temperature**
- **+5V (±10%) supply voltage; conditions permitting, on-chip derivation of V_{BB} (+1.5V)**

PRODUCT DESCRIPTION

Composite Cell Logic (CCL) provides a standard-cell approach to semi-custom bipolar logic. Besides the inherent advantages of LSI and proprietary design, CCL offers the designer a fast turnaround time, a high probability of first-pass success, and a die size that exactly meets all functional requirements of the logic. The CCL approach is particularly well suited to design applications where circuit complexities fall within a range of 100-to-1000 gates.

Figure 1 shows the CCL device together with two standard cells that might be used in the design process. At present, the available cells form two libraries—the Extended Performance Library (EPL) and the Integrated Schottky Library (ISL). Typically, the EPL cell (Figure 2) is used where speed is a critical factor—the speed of EPL cells is comparable to that of Schottky T^2L logic. *Note. Refer to table elsewhere in this data sheet for nominal figures pertaining to circuit propagation speeds of Schottky, Low-Power Schottky, T^2L, and Low-Power T^2L.* All EPL cells are input-expandable with no added delay, are highly immune to internal/external noise, and use active pullups to reduce sensitivity to lead capacitance and the effects of wire-ANDing.

The packing density of an ISL cell (Figure 3) is two to three times greater than that for EPL and the power required is only one-tenth ($1/10$) to one-twentieth ($1/20$) as great. The speed of ISL is slightly faster than that of Low-Power Schottky logic. For some circuits, the propagation speeds for ISL and EPL are nearly the same; for other circuits, there are appreciable differences. The speed-comparison table shown later in this data sheet provides a worthwhile guide for overall circuit design.

Output cells of both libraries can sink up to 80-milliamperes of current and both EPL and ISL cells use a 16-micron grid for easy conversion to "Automatic Place and Route" techniques—see Table 1 for a technical summary of both libraries.

Designing with CCL requires a cooperative effort between Signetics and the Customer. The contribution of each party and the overall development sequence are shown in Figure 4.

Table 1. TECHNICAL SUMMARY OF EPL AND ISL LIBRARIES

PARAMETER	EPL		ISL
Output structure	Active pullup		Open collector
Input structure	Schottky diode		Schottky diode
Worst-case noise margin	300mV (F.O. = 15)		70mV (F.O. = 15)
Junction temperature range	−55° to +155°C		−55° to +155°C
Power supply	+5V (±10%)		+1.5V (±10%)
	MEDIUM POWER	LOW POWER	
Max average speed (in ns)			
F.O. = 1 (T_J = 150°C)	4.5	5.5	6
F.O. = 6 (T_J = 150°C)	5.5	7.5	6 or 9*
Max average power (in mW):			
T_J = 150°C	5.6	2.6	0.3
Packing density gates/mm**	14 to 42		26 to 78

*Average speed of 6ns requires the use of a resistor pullup cell (optional).

**See Note 5 in Selection Guide regarding derivation of maximum values

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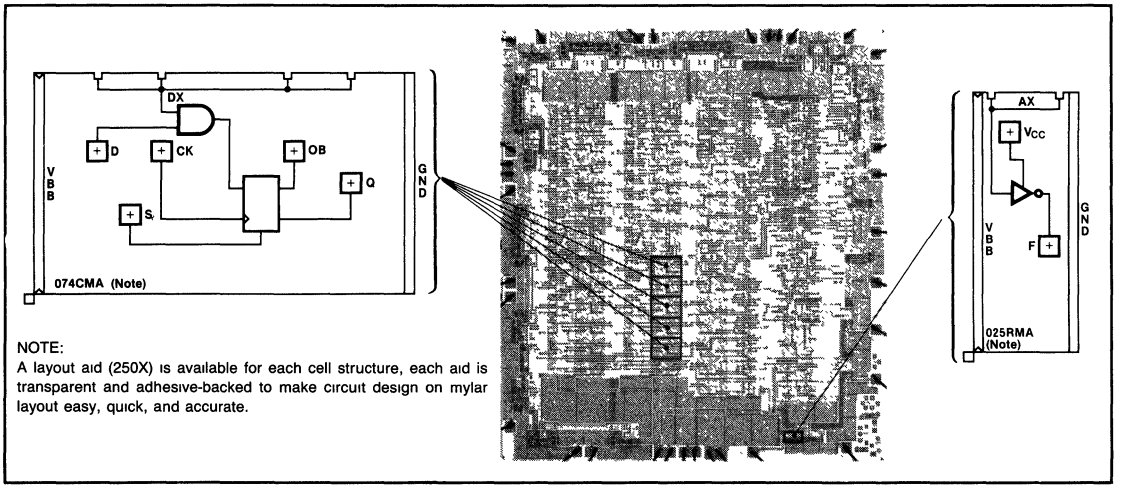
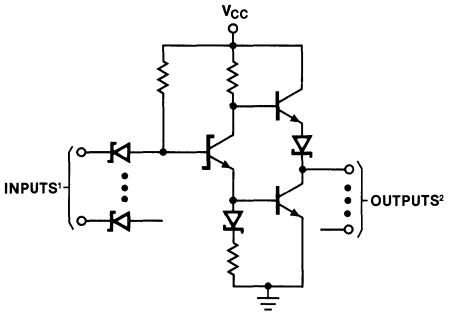


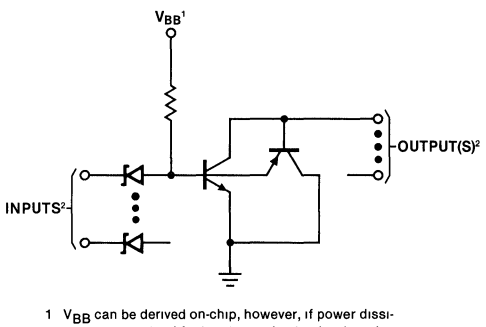
NOTE:
A layout aid (250X) is available for each cell structure, each aid is transparent and adhesive-backed to make circuit design on mylar layout easy, quick, and accurate.

Figure 1. Composite Cell Logic Showing Typical Cell Placement with the Use of Layout Aids.



1. Each input is driven by an active pullup, thus, the Fan-In is basically unrestricted
2. Outputs of standard cells are limited to a Fan-Out of 15; however, special-purpose clock buffer cells have Fan-Outs of up to 100

Figure 2. Typical EPL Cell.



1. V_{BB} can be derived on-chip, however, if power dissipation is a critical factor, it can also be developed off-chip
2. For standard cells, up to six inputs and/or outputs can be supported, special-purpose clock buffer cells may have up to 64 outputs

Figure 3. Typical ISL Cell.

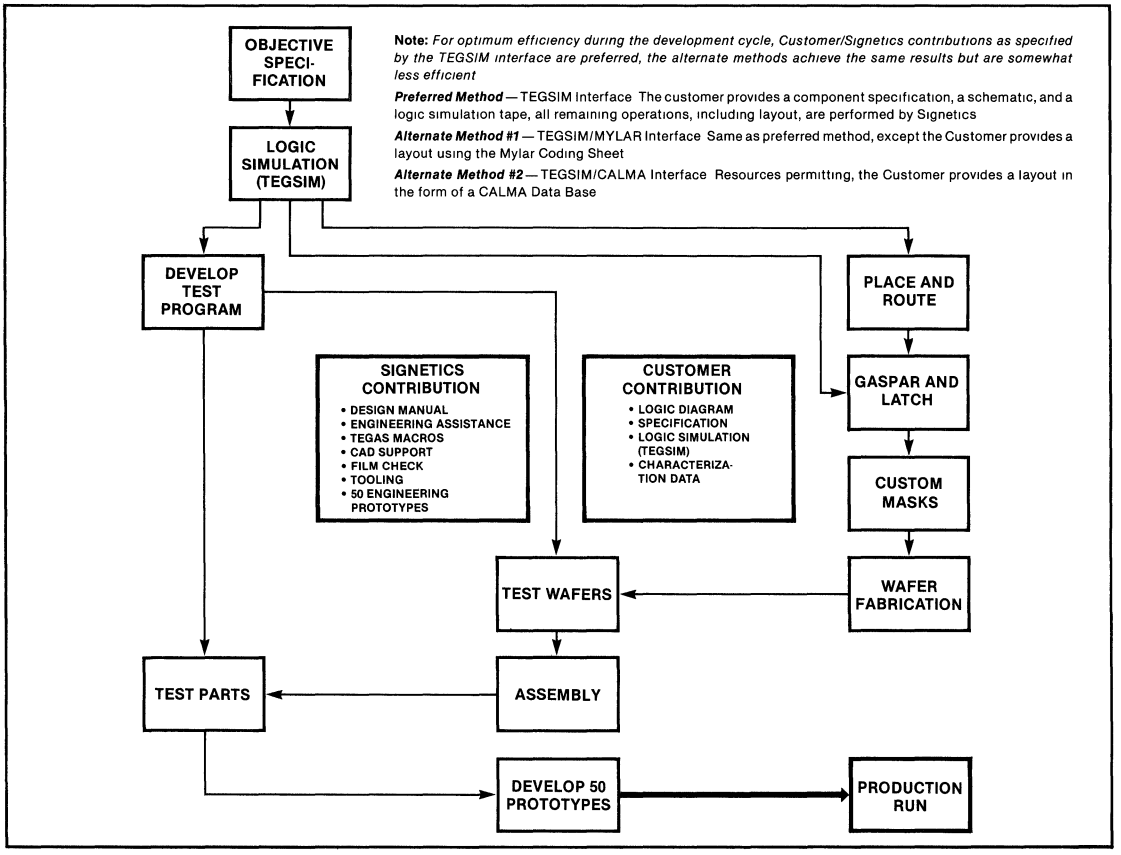


Figure 4. Development Sequence for CCL Logic Design

TYPICAL PERFORMANCE CHARACTERISTICS

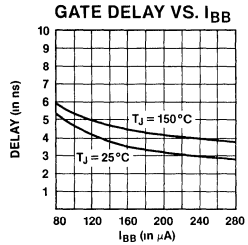
Note: *The information shown in Table 1 and that in the following pages is intended only as a design reference. To improve circuit performance, subject values may change. For guaranteed values, refer to the individual Cell Data Sheets in the CCL Design Manual.*

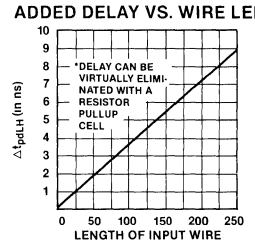
The overall performance of EPL cell structures is determined by the following parameters.

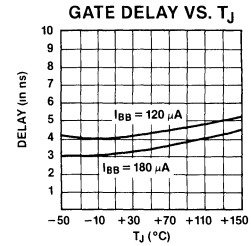
- Discrete gate delays
- Junction temperature (T_J)
- Gate current (I_{BB}) and gate voltage (V_{BB})

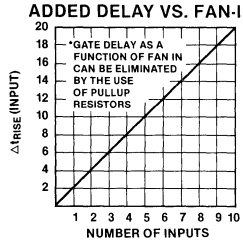
Gate delays are subject to several variables as shown in the accompanying graphs

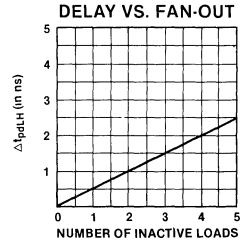
ISL LIBRARY

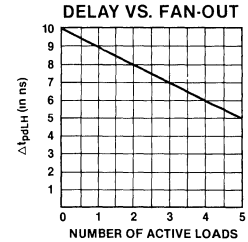




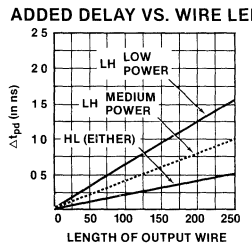


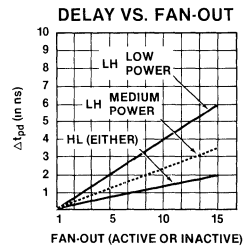


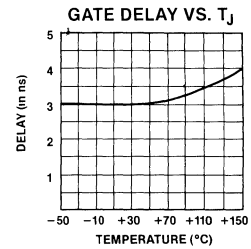




EPL LIBRARY







CALCULATION OF POWER DISSIPATION

At maximum junction temperature (T_J), the maximum power dissipation (P_d) for any given CCL configuration is determined by the following equation:

Maximum Power Dissipation $(P_d) = (T_J - T_A)/\theta_{Ja}$

where,

T_J = +150°C
T_A = Ambient temperature
P_d = Circuit power dissipation in watts
θ_{Ja} = Package thermal resistance in °C/W

thus,

$$P_d\,(ISL) = \frac{\text{total internal cells}}{(0.3\text{mW} \times \text{number of ISL gates used})} + \frac{\text{total I/O cells}}{\Sigma(I_{CC}\,\text{max})(V_{CC}\,\text{max})} + \frac{\text{total output cells}}{\Sigma(V_{OL}\,\text{max})(I_{OL}\,\text{max})}$$

$$P_d\,(EPL) = \frac{\text{internal + I/O cells}}{\Sigma(I_{CC}\,\text{max})\,(V_{CC}\,\text{max})} + \frac{\text{total output cells}}{\Sigma(V_{OL}\,\text{max})\,(I_{OL}\text{max})}$$

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Selection Guide and Design Limits for EPL Cells[1,2]

CELL IDENT	CELL DESCRIPTION	CELL AREA[3] (MIL^2)	I_{CC} MAX[4] (in mA)	t_{pdHL} MAX[4] (in ns)	t_{pdLH} MAX[4] (in ns)	FAN-OUT[5]
OR GATES						
ILX32	2-wide expandable OR, internal	55.55	1.40	7	12	15 UL
ILX52	2-wide expandable OR, internal	95.23	2.21	5	12	15 UL
IMX52	4-wide expandable OR, internal	95.23	4.75	4	8	15 UL
AND GATES						
ILX07	Expandable AND, internal	47.62	0.88	8	11	15 UL
IMX07	Expandable AND, internal	47.62	2.00	5	7	15 UL
RHX11	Expandable AND, input CLK driver	87.30	7.00	12	7	100 UL
RLX07	Expandable AND, input	47.62	0.97	8	13	15 UL
RLX11	Expandable AND, input CLK driver	71.42	1.85	7	7	40 UL
RMX07	Expandable AND, input	47.62	1.80	5	8	15 UL
RMX11	Expandable AND, input CLK driver	49.36	4.10	4	5	40 UL
TLX07	Expandable AND, output	63.49	1.50	12	9	8mA
TSX07	Expandable AND, output	87.30	8.30	9	8	24mA
NOR GATES (AND/OR Inverters)						
ILX02	2-wide expandable NOR, internal	47.62	1.06	5	8	15 UL
ILX24	4-wide expandable NOR, internal	95.23	1.90	3	7	15 UL
IMX02	2-wide expandable NOR, internal	47.62	2.50	4	5	15 UL
IMX24	4-wide expandable NOR, internal	95.23	4.40	4	4	15 UL
TLX24	4-wide expandable NOR, output	95.23	2.15	7	9	8mA
TSX24	4-wide expandable NOR, output	142.85	10.10	8	5	24mA
TZX02A	3-state, 2-wide expandable NOR gate (8mA/16mA)	83.33	10.10	8	5	24mA
NAND GATES						
ILX04	Expandable, internal	31.74	0.60	4	7	15 UL
IMX04	Expandable, internal	31.74	1.40	4	5	15 UL
RLX04	Expandable, input	47.62	0.60	3	10	15 UL
RHX37	Expandable, input CLK driver	95.23	6.50	4	4	100 UL
RLX37	Expandable, input, CLK driver	63.49	1.20	4	5	40 UL
RMX04	Expandable, input	47.62	1.14	4	5	15 UL
RMX37	Expandable, input, CLK driver	71.42	2.60	4	5	55 UL
THX04	Expandable, 40mA output	238.08	13.00	11	16	80mA
TLX03	Expandable, open-collector, output	31.74	1.18	11	19	8mA
TLX04	Expandable, 8mA output	63.49	1.20	8	6	8mA
TSX03	Expandable open-collector, 20mA output	55.55	7.30	11	8	24mA
TSX04	Expandable, 20mA output	87.30	7.30	8	4	24mA
ZLXQB	Non-expandable NAND, 8mA input	71.42	1.50	8	8	8mA
ZLX04	3-state expandable NAND, 8mA output	95.23	3.00	8	7	8mA
ZSX04	3-state expandable NAND, 20mA output	119.04	12.30	11	5	24mA
EXCLUSIVE OR/NOR GATES						
ILX26	2-wide expandable XNOR, internal	103.70	2.10	19	22	15 UL
ILX86	2-wide expandable XOR, internal	111.10	1.80	17	19	15 UL
IMX26	2-wide expandable XNOR, internal	103.17	4.40	13	13	15 UL
IMX86	2-wide expandable XOR, internal	95.23	3.80	11	13	15 UL
FLIP-FLOPS						
ILX74	Negative edge-triggered "D" flip-flop, internal	261.89	2.80	17	12	15 UL
ILX75	Gated "D" latch, internal	142.85	1.80	4	16	15 UL
ILX79	NAND latch, internal	79.36	0.88	4	8	15 UL
IMX74	Negative edge-triggered "D" flip-flop, internal	258.70	5.90	8	8	15 UL
IMX75	Gated "D" latch, internal	142.85	3.70	6	12	15 UL
IMX79	NAND latch, internal	79.36	2.00	4	5	15 UL

Selection Guide and Design Limits for EPL Cells[1,2] (Continued)

CELL IDENT	CELL DESCRIPTION	CELL AREA[3] (MIL^2)	I_{CC} MAX[4] (in mA)	t_{pdHL} MAX[4] (in ns)	t_{pdLH} MAX[4] (in ns)	FAN-OUT[5]
SCHMITT TRIGGER						
RMX14	Inverting, input	87.30	1.90	3	5	15 UL
HIGH-IMPEDANCE RECEIVER						
RH640	HI-Z Rcvr, input	119.04	5.20	14	11	15 UL
POWER-UP CLEAR						
POWER	Power-up/clear	166.66	7.80	—	—	15 UL
DIODE EXPANSION						
Twenty-six (26) diode expansion cells are available ranging in die size from 7 94 Mil^2 to 71 42 Mil^2						
DUMMY LOAD and/or PULLUPS						
Dummy loads or pull-up cells are not required for the EPL Library.						

Notes:
1. To improve performance and to meet changing needs, the EPL library is updated on a continuing basis via additions, deletions, and/or modifications, for the current status of any given cell, contact the nearest Signetics Sales Office
2. Custom EPL cells are available on a "qualification" basis
3. To convert Mil^2 to $Micron^2$, multiply Mil-value by 645.16
4. Design limits are based on standard modeling with similar circuits used in Signetics standard bipolar LSI products Actual simulation limits are maintained to be consistent with characterization updates for the CCL libraries.
5. A fan-out Unit Load (UL) corresponds to a load factor of approximately 220 microamperes.

Selection Guide and Design Limits for ISL Cells[1,2]

CELL IDENT	CELL DESCRIPTION	CELL AREA[3] (MIL^2)	I_{CC} MAX[4,5] (in mA)	I_{BB}[5,6] (in UL)	t_{pdHL}MAX[5,7] (in ns)	t_{pdLH} MAX[5,7] (in ns)	FAN-OUT[6]
MSI CELLS							
151ILA	8-to-1 multiplexer	371.46	N/A	15	Refer to individual Data Sheets in CCL Design Manual for these parameters		
161CLA	4-bit counter	TBD	N/A	60			
194ILA	4-bit left-right shift register	1317 4	N/A	40			
283ILA	4-bit adder	857 1	N/A	55			
934CLA	4-bit ALU	1650 7	N/A	30			
OR GATES							
20RIL	2-wide expandable OR, internal	31 7	N/A	3	14	12	6 UL
30RIL	3-wide expandable OR, internal	44 5	N/A	4	16	12	6 UL
40NIL	4-wide NOR/OR, internal	50.8	N/A	5	18	12	5 or 6 UL
40RIL	4-wide expandable OR, internal	50.8	N/A	5	18	12	6 UL
60RIL	6-wide expandable OR, internal	114 3	N/A	7	22	12	6 UL
AND GATES							
007IH	CLK buffer expandable AND, internal	63.5	1 8	N/A	19	18	64 UL
007IL	Expandable AND, internal	25 4	N/A	2	12	12	6 UL
007RH	CLK buffer expandable AND, input	57.1	1.8	N/A	19	18	64 UL
007RM	Expandable AND, input	63 5	1 2	N/A	7	9	15 UL
007TL	Expandable AND, output (8mA)	63.5	2.0	N/A	13	15	8mA
007TS	Expandable AND, output (20mA)	95 23	8 3	N/A	12	14	24mA
009IL	2-input expandable AND, internal	25 4	N/A	2	12	14	6 UL
015IL	3-input expandable AND, internal	31.7	N/A	2	12	16	6 UL

Selection Guide and Design Limits for ISL Cells[1,2] (Continued)

CELL IDENT	CELL DESCRIPTION	CELL AREA[3] (MIL^2)	I_{CC} MAX[4,5] (in mA)	I_{BB}[5,6] (in UL)	t_{pdHL} MAX[5,7] (in ns)	t_{pdLH} MAX[5,7] (in ns)	FAN-OUT[6]
NOR GATES (AND/OR INVERTERS)							
002TL	2-wide NOR, output (8mA)	63 5	2.0	N/A	13	9	8mA
002ZK	3-state 2-wide NOR, output (8/16mA)	133.3	3.9	N/A	20	10	16mA
027TL	3-wide NOR, output (8mA)	76 2	2 5	N/A	13	10	8mA
2NRCL	2-wide NOR, clock buffer driver	25.4	Note 8	Note 8	2	12	6 UL
2NRIH	2-wide expandable NOR, clock buffer	57 1	1 8	N/A	16	18	64 UL
2NRIL	2-wide expandable NOR, internal	25 4	N/A	2	2	12	6 UL
3NRIL	3-wide expandable NOR, internal	31 7	N/A	3	2	14	6 UL
40NIL	4-wide NOR/OR, internal	50 8	N/A	5	18	12	6 UL
4NRIL	4-wide expandable NOR, internal	44 4	N/A	4	2	16	6 UL
6NRIL	6-wide expandable NOR, internal	95 2	N/A	6	2	20	6 UL
NAND GATES							
003IL	2-input expandable, internal	19	N/A	1	4	10	6 UL
004IH	Clock buffer, expandable, internal	50 8	1 3	N/A	15	13	64 UL
004RH	Clock buffer, expandable, input	63 5	1 3	N/A	15	13	64 UL
004RM	Expandable, input	57 1	1 6	N/A	3	10	15 UL
004TB	Expandable, output (12mA/24mA)	76 2	3 4	N/A	17	7	24mA
004TL	Expandable, output (8mA)	57 1	1 5	N/A	13	7	8mA
004TS	Expandable, output (20mA)	76 2	7 3	N/A	14	6	24mA
004ZL	3-state expandable NAND (8mA)	69 84	2 4	N/A	14	8	8mA
005CL	Clock buffer driven, expandable, internal	19	Note 8	Note 8	2	10	6 UL
005IH	Expandable, internal, fan-out = 18	31.7	N/A	3	2	14	18 UL
005IL	Expandable, internal	19	N/A	1	2	10	6 UL
005IM	Expandable, internal, fan-out = 12	19	N/A	2	2	12	12 UL
005RM	Expandable, input	69 8	1 6	3	3	13	15 UL
005TB	Expandable, output (80mA) open collector	171 42	8 2	N/A	15	25	70mA
005TL	Expandable, output (8mA) open collector	31 7	3 3	N/A	13	17	8mA
012IL	3-input expandable, internal	25 4	N/A	1	6	10	6 UL
368ZL	3-state expandable NAND (12mA/24mA)	76 19	3 4	N/A	17	7	24mA
EXCLUSIVE OR/NOR GATES							
136IL	2-wide expandable XOR, internal	44 4	N/A	4	14	14	6 UL
266IL	2-wide expandable XOR, internal	38 1	N/A	3	12	12	6 UL
FLIP-FLOPS							
NRLIL	NOR latch, internal	57 1	N/A	4	2	14	5 UL
TOGCM	Clock buffer driven, toggle FF, internal	152 4	N/A	8	24	18	9 UL
074CL	Clock buffer driven "D", internal (fan-out = 6)	95 2	N/A	4	22	16	5 UL
074CM	Clock buffer driven "D", internal (fan-out = 12)	133 3	N/A	6	24	18	10 UL
074IL	Positive edge-triggered "D", internal	114 3	N/A	6	22	16	5 UL
075IL	Gated latch, internal	76.2	N/A	5	4	16	5 UL
279IL	NAND latch, internal	38 1	N/A	2	4	10	5 UL
POWER-UP CLEAR							
PWRRL	Power-Up/Clear	19	0 7	N/A	—	—	6 UL
DUMMY LOADS							
REFIL	Internal dummy load	12 7	N/A	1	—	—	—
REFIL	Output dummy load	19 0	0 26	N/A	—	—	—
DIODE EXPANSION							
Thirty-five (35) diode expansion cells are available ranging in die size from 6 35 Mil^2 to 19 05 Mil^2							

Notes:
1. To improve performance and to meet changing needs, the ISL library is updated on a continuing basis via additions, deletions, and/or modifications; for the current status of any given cell, contact the nearest Signetics Sales Office.
2. Custom ISL cells are available on a "qualification" basis.
3. To convert Mil^2 to Micron^2, multiply Mil-value by 645.16.
4. Maximum values of I_{CC} do not always occur at the same temperature for all ISL cells, thus I_{CC} should not be used for calculation of power dissipation for a discrete cell. The tabularized values can properly be used for worst-case power supply design.
5. Design limits are based on standard modeling with similar circuits used in Signetics standard bipolar LSI products. Actual simulation limits are maintained to be consistent with characterization updates for the CCL libraries.
6. A Unit Load (UL) for I_{BB} corresponds to a load factor of approximately 190 microamperes; a fan-out unit load corresponds to a load factor of approximately 220 microamperes.
7. The propagation-delay measurements were taken at 150°C with both fan-out and fan-in equal to 1.
8. The internal Clock Buffer ISL cells listed below are driven by any one of the special driver cells; to compute I_{CC} requirements, refer to appropriate data sheet(s) in CCL Design Manual.

Driven Cells		Driver Cells (Fan-Out = 64)	
Internal NOR	—C12NRCLA	Internal AND	—C1007IHA
Internal D Flip-Flop (Fan-Out = 5)	—C1074CLA	Input AND	—C1007RHA
Internal D Flip-Flop (Fan-Out = 10)	—C1074CMA	Input NOR	—C12NRIHA
Internal Toggle Flip-Flop	—CIT06CMA	Internal NAND	—C1004IHA
Internal NAND	—C1005CLA	Input NAND	—C1004RHA

Table 2. Comparison of CCL to 74S/74LS Functions

LOGIC FUNCTION	PARAMETERS[1,3,6]	LOGIC DEVICES		CCL (ISL CELLS)[2]	CCL (EPL CELLS)	
		74SXX	74LSXX		LOW POWER	MED. POWER
NAND (5400)	Power (in mW)	35.7	4.13	0.31	2.56	5.61
	t_{ON} (in ns)	5.0	15.0	2.00	3.00	3.00
	t_{OFF} (in ns)	4.5	15.00	10.00	6.00	3.00
AND (5408)	Power (in mW)	61.2	9.35	0	0	0
	t_{ON} (in ns)	7.5	20.00	0	0	0
	t_{OFF} (in ns)	7.0	15.00	2.00[4]	0	0
NOR (5402)	Power (in mW)	50.9	5.91	0.63	4.68	10.45
	t_{ON} (in ns)	5.5	15.00	2.00	3.00	3.00
	t_{OFF} (in ns)	5.5	15.00	12.00	7.00	3.00
OR (5432)	Power (in mW)	68.7	11.00	0.94	6.90	23.90
	t_{ON} (in ns)	7.00	22.00	14.00	4.00	3.00
	t_{OFF} (in ns)	7.00	22.00	12.00	8.00	5.00
EXCLUSIVE OR (5486)	Power (in mW)	103.00	13.75	1.25	9.24	19.00
	t_{ON} (in ns)	10.00	22.00	14.00	13.00	8.00
	t_{OFF} (in ns)	10.50	30.00	14.00	15.00	8.00
EXCLUSIVE NOR (54266)	Power (in mW)	N/A	17.90	0.94	10.70	22.00
	t_{ON} (in ns)	N/A	30.00	14.00	14.00	9.00
	t_{OFF} (in ns)	N/A	30.00	14.00	18.00	11.00
AND/OR INVERTERS (5451)	Power (in mW)	54.70	6.05	0.63	4.68	10.45
	t_{ON} (in ns)	5.50	20.00	2.00	3.00	3.00
	t_{OFF} (in ns)	5.50	20.00	12.00	7.00	3.00
D FLIP-FLOP (5474)	Power (in mW)	137.50	22.00	1.88	15.40	37.10
	t_{ON} (in ns)	13.50	40.00	22.00	12.00	8.00
	t_{OFF} (in ns)	6.00	25.00	18.00	11.00	8.00
	F_{max} (in MHz)	75.00	25.00	30.00	25.00[5]	50.00[5]

Notes:
1. Unless otherwise noted, all switching parameters (t_{ON} and t_{OFF}) are at 25°C/5V max.
2. Switching parameters for ISL cells are at 150°C max.
3. Power = $\frac{I_{CC_0} + I_{CC_1}}{2} \times V_{CC}$ max.
4. t_{OFF} is 2 ns for each input; t_{OFF} can be reduced to 0 ns with a pullup cell
5. F_{max} is at 150°C min.
6. ISL and CCL parameter values derived from design limits—refer to Note 4 under "Selection Guide and Design Limits for EPL Cells."

ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V
V_{BB}	ISL gate supply voltage	+7.0	V
E_{IN}	Input voltage, continuous	−0.5 to +5.5	V
I_{IN}	Input current, continuous	−30 to +1.0	mA
V_O	Voltage applied to open-collector output in off-state	−0.5 to +7.0	V
T_A	Ambient temperature, operating	−55 to +125	°C
T_{STG}	Storage temperature	−65 to +150	°C

AC AND DC ELECTRICAL CHARACTERISTICS

Conditions[1]: V_{CC} = 5.0V (±10%)
V_{BB} = 1.5V (±10%)
T_J = 0°C to +150°C

PARAMETER		TEST CONDITIONS[2]		DESIGN LIMITS[3] MIN	TYP	MAX	UNIT
EPL GATE (INTERNAL)							
$I_{CC/G}$	Power supply current per gate			0.18	0.29	0.47	mA
I_{LF}	Input load factor				1		UL
F_O	Fan-Out				15		
t_{pdAV}	Average gate propagation delay = $\frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = 1 EPL gate; Fan-out = 1 EPL gate			3	5.5	ns
t_{pdLH}	Propagation delay from low-to-high state	Fan-in = 1 EPL gate; Fan-out = 1 EPL gate			4	7	ns
t_{pdHL}	Propagation delay from high-to-low state				2	4	ns
ISL GATE (INTERNAL)							
$I_{BB/G}$	Power supply current per gate			110	150	190	μA
I_{LF}	Input load factor				1		UL
F_O	Fan-out				6		UL
t_{pdAV}	Average gate propagation delay = $\frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = 1 ISL gate; Fan-out = 1 ISL gate			3	6	ns
t_{pdLH}	Propagation delay from low-to-high state	Fan-in = 1 ISL gate; Fan-out = 1 ISL gate			5	10	ns
t_{pdHL}	Propagation delay from high-to-low state				1	2	ns
EPL/ISL INPUT CELLS							
V_{TH}	Input threshold voltage			0.8		2.0	V
V_{CD}	Input clamp diode voltage	I_{IN} = −18mA				−1.2	V
I_{IL}	Input low current	V_{IN} = 0.4V	PNP input			−20	mA
			Diode input			−400	
I_{IH}	Input high current	V_{IN} = 2.7V				20	μA
I_I	Maximum input high current	V_{IN} = 5.5V				100	
F_O	Fan-out (ISL library)	Standard cell				6	UL
		Clock buffer cell				64	
	Fan-out (EPL library)	Standard cell				15	
		Clock buffer cell				55	
		Clock buffer cell				100	

AC AND DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		TEST CONDITIONS[2]			DESIGN LIMITS[3] MIN	TYP	MAX	UNIT
EPL/ISL THREE-STATE OUTPUT BUFFERS								
I_{LF}	Input load factor	EPL					1 or 9	UL
		ISL					2 or 4	
V_{OL}	Output low voltage	Military: 4mA					400	mV
		Commercial: 8mA					500	
		Military: 12 mA					400	mV
		Commercial: 24 mA					500	
V_{OH}	Output high voltage	Military: $I_{OH} = -400\ \mu A$			2.5			V
		Commercial: $I_{OH} = -400\ \mu A$			2.7			
I_{OS}	Output short circuit current	$V_{OUT} = 0V$			−15		−100	mA
I_{OLZ}	Three-state off current (output low)	$V_{OUT} = 0.4V$					−20	μA
I_{OHZ}	Three-state off current (output high)	$V_{OUT} = 2.4V$					20	μA
EPL/ISL OPEN-COLLECTOR OUTPUT BUFFERS								
I_{LF}	Input load factor	EPL	8 mA output				1	UL
			20 mA output				3	
			80 mA output				5	
		ISL					2 or 4	
V_{OL}	Output low voltage	I_{OL}	8 mA output				500	mV
			20 mA				500	
			70 mA				500	
			80 mA				800	
I_{OH}	Output leakage current	V_{OUT}	80 mA Cells	2.75			60	μA
				5.5V			250	
			8/20 mA Cells	5.5V			100	
ACTIVE PULLUP OUTPUT BUFFER								
I_{LF}	Input load factor	EPL					1 or 3	UL
		ISL					2 or 4	
V_{OL}	Output low voltage	I_{OL} = 8 mA or 20 mA					500	mV
V_{OH}	Output high voltage	Military	$I_{OH} = -400\ \mu A$ or -1.0 mA		2.5			V
		Commercial	$I_{OH} = -400\ \mu A$ or -1.0 mA		2.7			
I_{OS}	Output short circuit current	$V_{OUT} = OV$	8 mA output		−15		−100	mA
			20 mA output		−40		−100	

Notes:
1. Maximum power dissipation is determined from individual cell data sheets; the figures are then summed to calculate total power for the chip. The total power must be less than the Maximum Power Dissipation (P_d) calculated earlier in this data sheet.
2. For test circuits and timing waveforms, refer to individual cell data sheets in the CCL Design Guide.
3. Design limits are based on standard modeling with similar circuits used in Signetics standard bipolar LSI products. Actual simulation limits are maintained to be consistent with characterization updates for the CCL libraries.

CMOS GATE ARRAYS (M-Series)

FEATURES

- **Customer programmable LSI**
- **330 to 1100 gate complexity**
- **Mature silicon gate technology with local oxidation**
- **Library of 60 pre-designed, fully characterized macrocells available**
- **Full CAD, including auto-place and auto-route, for quick error-free design**
- **Very low power consumption (e.g. standby power for SCC 0700 is 0.25mW)**
- **Excellent noise immunity**
- **Power supply range 3 to 15V**
- **Over 80% utilization typical**
- **Fully programmable I/O pins, each having a wide range of functions**
- **Input protection by series resistor and diode clamp to V_{SS}**
- **TTL outputs (buffers) drive up to four LSTTL loads**
- **−55°C to +125°C operating temperature**
- **Plastic and ceramic DIP, ceramic leadless chip carriers, and plastic leaded chip carriers available**

PRODUCT DESCRIPTION

The SCCXXXX gate array family offers the circuit designer the facility to create a semi-custom circuit with a unique set of CAD (Computer-Aided Design) tools in a well-established CMOS process.

Signetics M-Series CMOS Gate Arrays are single chip programmable devices that allow customization of user logic. Only metalization and contact are programmed in these mature CMOS devices. Thus, fast turnaround from logic to completed silicon is achieved.

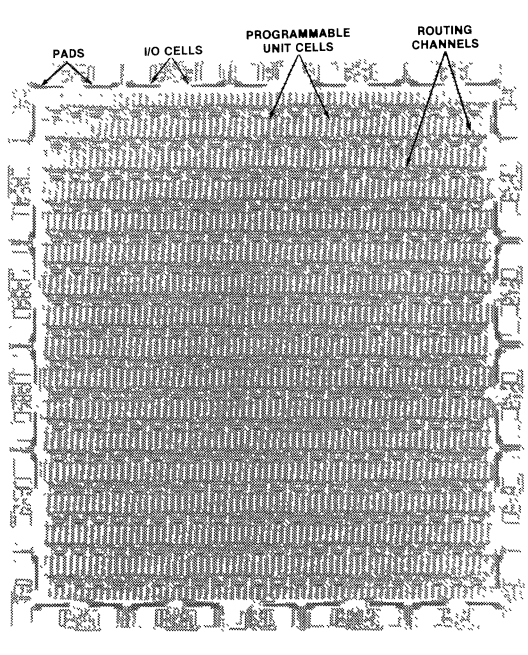
Each device in this family of low power gate arrays contains numerous identical, uncommitted unit cells (Figure 1) which are interconnected by two custom masks (metal and contact). Each unit cell contains four pairs of N and P transistors. Access to the transistors is from both the top and bottom of the cells and, additionally, there are two poly feed-throughs at each side of the cell. This homogenous cell design allows for excellent routing flexibility, and many designs result in better than 80% utilization of the gates available.

The M-Series Gate Arrays are built on a mature, state-of-the-art 4-micron Si-gate CMOS process incorporating an epi-substrate, which significantly reduces the potential for latch as compared with other bulk CMOS processes.

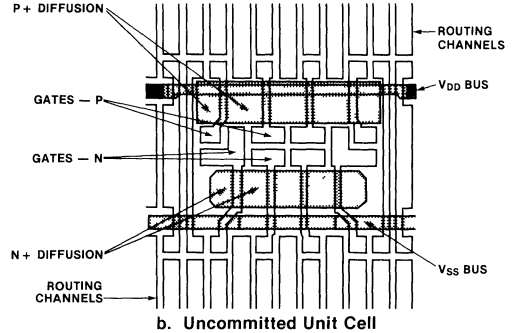
Computer Aided Design (CAD) is used throughout the design process to ensure accurate implementation of customer logic (see Figure 14 for typical process flow).

ORDERING INFORMATION

Contact Local Sales Representative



a. SCC0700 CMOS Gate Array



b. Uncommitted Unit Cell

	SCC0330	SCC0450	SCC0700	SCC1100
Gate equivalents (2 input)	330	448	704	1116
Unit cells	165	224	352	558
Rows	11	14	16	18
Unit cells per row	15	16	22	31
Pins (max)	40	28	40	68
I/O stages (max)	38	26	38	66
I/O options				
3 state I/O (max)	34	26	38	66
Direct or inverted inputs (max)	38	26	38	66
Drivers (max)	38	14	22	66
Buffers (max)	34	12	16	66
Schmitt Triggers (max)	34	8	10	66
Pin pull-up/pull down resistors (max)	34	26	34	66

c. Product Matrix

Figure 1. Internal Configuration and Functional Characteristics of M-Series CMOS Gate Arrays

ABSOLUTE MAXIMUM RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	− 0.5 to + 18V
Voltage on any input when pin pull up/down resistors are: Used Not used	 V_I V_I	 − 0.5 to V_{DD} + 0.5V − 0.5 to + 18V
DC current into any input or output	± 1	Max. 10mA
Power dissipation per output	P	Max. 100mW
Power dissipation per package For standard temperature range: − 40°C to + 85°C (plastic and ceramic DIP) For T_{amb} = − 40°C to + 60°C For T_{amb} = + 60°C to + 85°C	 P_{tot} P_{tot}	 Max 400mW Derate linearly by 8mW/K to 200mW
For extended temperature range: − 55°C to + 125°C (ceramic DIP) For T_{amb} = − 55°C to + 100°C For T_{amb} = + 100°C to + 125°C	 P_{tot} P_{tot}	 Max. 400mW Derate linearly by 8mW/K to 200mW
Storage temperature range	T_{stg}	− 65°C to + 150°C

DC ELECTRICAL CHARACTERISTICS V_{SS} = 0V, for all devices unless otherwise specified

SYMBOL AND PARAMETER	OPERATING TEMP (T_{amb})[1]	SUPPLY VOLTAGE	TEST CONDITIONS	TEMPERATURE RANGE[1]						UNIT
				T_{amb} = LOW		T_{amb} = 25°C		T_{amb} = HIGH		
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{DD} Quiescent device current	Standard	5	All valid input combinations, $V_I = V_{SS}$ or V_{DD}	—	50	—	50	—	375	µA
		10		—	100	—	100	—	750	
		15		—	200	—	200	—	1500	
	Extended	5		—	15	—	15	—	375	
		10		—	25	—	25	—	750	
		15		—	50	—	50	—	1500	
V_{OL} Output voltage Low	Both standard and extended ranges	5	$V_I = V_{SS}$ or V_{DD}, I_O < 1.0µA	—	0 05	—	0 05	—	0 05	V
		10		—	0 05	—	0 05	—	0 05	
		15		—	0 05	—	0 05	—	0 05	
V_{OH} Output voltage High		5		4 95	—	4 95	—	4 95	—	
		10		9 95	—	9 95	—	9 95	—	
		15		14 95	—	14 95	—	14 95	—	
V_{IL} Input voltage Low· INPI/INPB	Both standard and extended ranges	5	V_O = 0.5V or 4.5V; I_O < 1 0µA	—	1 5	—	1 5	—	1 5	
		10		—	3 0	—	3.0	—	3 0	
		15	V_O = 1 0V or 9 0V, I_O < 1 0µA	—	4.0	—	4 0	—	4 0	
V_{IH} Input voltage High: INPI/INPB		5		3 5	—	3 5	—	3 5	—	
		10	V_O = 1 5V or 13.5V, I_O < 1.0µA	7 0	—	7 0	—	7 0	—	
		15		11 0	—	11 0	—	11 0	—	
V_{IL} Input voltage Low INPA, INPD, INPS	Both standard and extended ranges	5	V_O = 0 5V or 4 5V, I_O < 1.0µA	—	1 0	—	1 0	—	1 0	
		10		—	2 0	—	2 0	—	2 0	
		15	V_O = 1 0V or 9.0V, I_O < 1 0µA	—	2.5	—	2 5	—	2 5	
V_{IH} Input voltage High: INPA, INPD, INPS		5		4.0	—	4 0	—	4 0	—	
		10	V_O = 1 5V or 13 5V; I_O < 1 0µA	8 0	—	8 0	—	8 0	—	
		15		12 5	—	12 5	—	12.5	—	

DC ELECTRICAL CHARACTERISTICS (Continued) V_{SS} = 0V; for all devices unless otherwise specified.

SYMBOL AND PARAMETER	OPERATING TEMP (T_{amb})[1]	SUPPLY VOLTAGE	TEST CONDITIONS	TEMPERATURE RANGE[1]						UNIT
				T_{amb} = LOW		T_{amb} = 25°C		T_{amb} = HIGH		
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{OL} Output (sink) current Low driver outputs	Standard	5	V_I = 0V or 5V; V_O = 0.4V	1.1	—	0.9	—	0.7	—	mA
		10		4.0	—	3.3	—	2.6	—	
		15		12.0	—	10.0	—	8.0	—	
	Extended	5		1.2	—	0.9	—	0.6	—	
		10		4.2	—	3.3	—	2.2	—	
		15	V_I = 0V or 10V; V_O = 0.5V	13.0	—	10.0	—	6.7	—	
I_{OL} Output (sink) current Low buffer outputs	Standard	5		2.2	—	1.8	—	1.4	—	
		10	V_I = 0V or 15V; V_O = 1.5V	8.0	—	6.6	—	5.6	—	
		15		24.0	—	20.0	—	16.0	—	
	Extended	5		2.4	—	1.8	—	1.2	—	
		10		8.4	—	6.6	—	4.4	—	
		15		26.0	—	20.0	—	13.4	—	
$-I_{OH}$ Output (source) current High	Standard	5	V_I = 0V or 5V; V_O = 4.6V	1.1	—	0.9	—	0.7	—	
		10		3.1	—	2.6	—	2.0	—	
		15	V_I = 0V or 10V; V_O = 9.5V	12.0	—	10.0	—	8.0	—	
	Extended	5		1.2	—	0.9	—	0.6	—	
		10		3.5		2.6		1.7		
		15	V_I = 0V or 15V; V_O = 13.5V	13.0	—	10.0	—	6.7	—	
$\pm I_{IN}$ Input leakage current	Standard	10	V_I = 0V or 10V	—	0.3	—	0.3	—	1.0	μA
		15		—	0.3	—	0.3	—	1.0	
	Extended	10	V_I = 0V or 15V	—	0.1	—	0.1	—	1.0	
		15		—	0.1	—	0.1	—	1.0	
I_{OZH} Three-state output and open N-channel output leakage current High	Standard	10	Output returned to V_{DD}	—	1.6	—	1.6	—	12.0	
		15		—	1.6	—	1.6	—	12.0	
	Extended	10		—	0.4	—	0.4	—	5.0	
		15		—	0.4	—	0.4	—	5.0	
$-I_{OZL}$ Three-state output and open P-channel output leakage current Low	Standard	10	Output returned to V_{SS}	—	1.6	—	1.6	—	12.0	
		15		—	1.6	—	1.6	—	12.0	
	Extended	10		—	0.4	—	0.4	—	5.0	
		15		—	0.4	—	0.4	—	5.0	
V_{TH} Upper threshold voltage	Standard	5	Internal Schmitt trigger	—	—	3.4 (Typical values)		—	—	V
		10		—	—	6.8 (Typical values)		—	—	
		15		—	—	10.2 (Typical values)		—	—	
V_{TL} Lower threshold voltage		5		—	—	2.2		—	—	
		10		—	—	3.0 (Typical values)		—	—	
		15		—	—	3.8		—	—	
V_H Hysteresis voltage input: INPS	—	5	—	—	—	0.2 (Typical values)		—	—	
		10		—	—	0.6 (Typical values)		—	—	
		15		—	—	0.8 (Typical values)		—	—	

NOTES.
1. T_{amb} Low: –40°C for standard temperature range; –55°C for extended temperature range. T_{amb} High: +85°C for standard temperature range; +125°C for extended temperature range.
2. Pin-connected pull-up and pull-down resistors are typically 7 to 78 K-ohms — see PERIPHERY
3. When pull-up or pull-down resistors are used, current limits for I_{DD} must be extrapolated

DC CHARACTERISTICS (Continued)

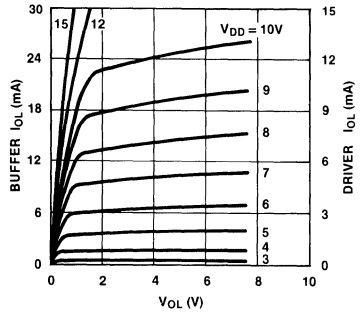


Figure 2. Minimum Output Current LOW as a Function of the Output Voltage LOW; Buffer and Driver Outputs

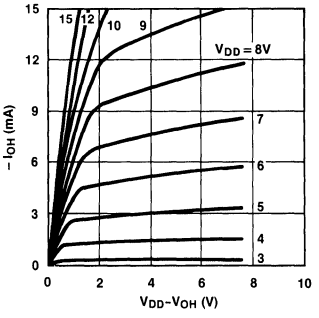


Figure 3. Minimum Output Current HIGH as a Function of the Supply Voltage Minus the Output Voltage HIGH

AC ELECTRICAL CHARACTERISTICS V_{SS} = 0V; T_{amb} = 25°C

SYMBOL AND PARAMETER		PWR SUP (V_{DD})	MIN	TYP	MAX	UNIT
f_{max}	Maximum toggle frequency flip-flop GT00 (no set/reset)	5	6	12	—	MHz
		10	12	24	—	MHz
		15	15	30	—	MHz
f_s	Maximum system frequency (may depend on number of gates in sequence)	5	3	6	—	MHz
		10	6	12	—	MHz
		15	9	18	—	MHz
t_p	Propagation delays for 2-input NAND gate with fanout of 2	5	—	8	16	ns
		10	—	3.2	6.4	ns
		15	—	2	4	ns

SYMBOL AND PARAMETER		PWR SUP (V_{DD})	MIN	TYP	MAX	UNIT
OUTPUT STAGE TRANSITION TIMES: Input transition ≤ 20ns, C_L = 50pF; V_{SS} = 0V, T_{amb} = 25°C						
t_{THL}	Driver outputs High-to-Low	5		60	120	ns
		10		30	60	ns
		15		20	40	ns
t_{THL}	Buffer outputs High-to-Low	5		30	60	ns
		10		15	30	ns
		15		10	20	ns
t_{TLH}	Buffer outputs Low-to-High	5		40	80	ns
		10		18	36	ns
		15		12	24	ns

9

GATE DELAYS

Nominal Propagation Delay

In Figures 6 through 12, examples are given of the nominal propagation delay times of several library cells, these being calculated from the delay figures given in the individual macro descriptions. These graphs are intended to provide quick-reference data to enable the designer to make an estimate of critical a.c. path without having built or simulated a network.

Accurate delay figures can only be obtained after incorporating the wiring length load automatically calculated by INGATE (i.e., the result of the automatic routing program). A maximum delay is obtained by multiplying the nominal value by 2.2.

GATE DELAYS (Continued)

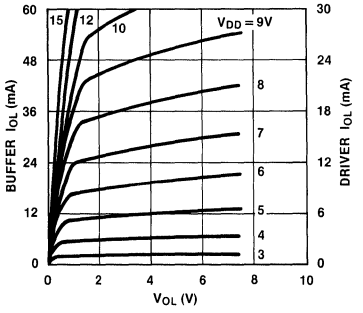


Figure 4. Typical Output Current LOW as a Function of the Output Voltage LOW; Buffer and Driver Outputs

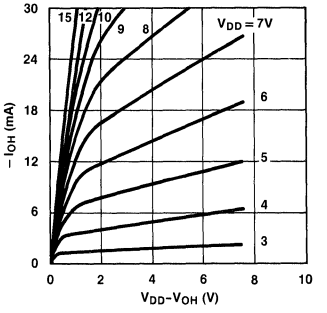


Figure 5. Typical Output Current HIGH as a Function of the Supply Voltage Minus the Output Voltage HIGH

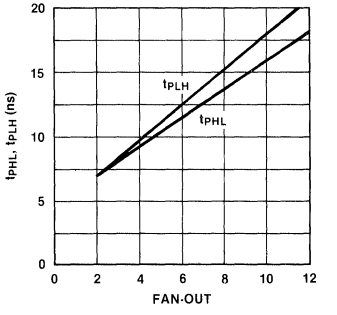


Figure 6. Nominal Propagation Delay as a Function of the Fan-Out; GIN1 (Single Inverter)

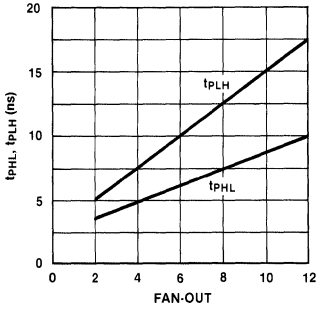


Figure 7. Nominal Propagation Delay as a Function of the Fan-Out; GNAND2 (2-Input NAND Gate)

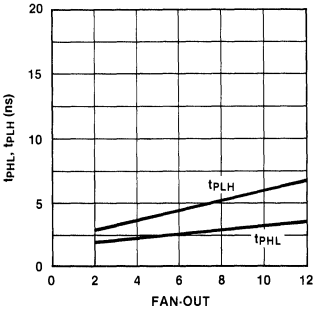


Figure 8. Nominal Propagation Delay as a Function of the Fan-Out; GIN4 (Quadruple Inverter)

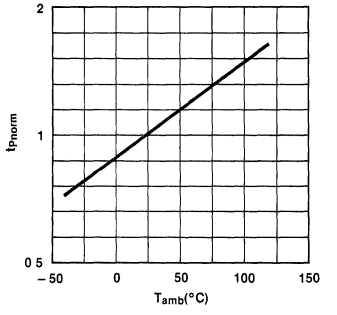


Figure 9. Normalized Propagation Delay (t_{Pnorm}) as a Function of the Ambient Temperature

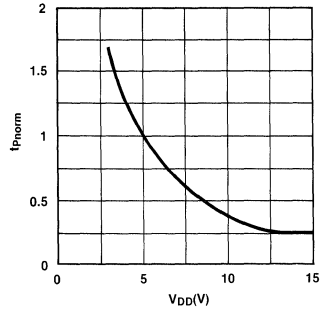


Figure 10. Normalized Propagation Delay (t_{Pnorm}) as a Function of the Supply Voltage

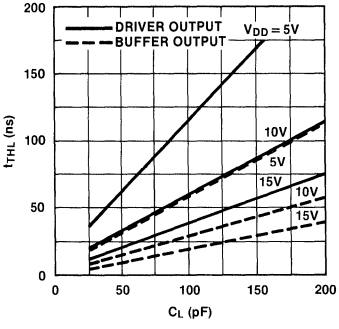


Figure 11. Output Transition Time (HIGH-to-LOW) as a Function of the Load Capacitance

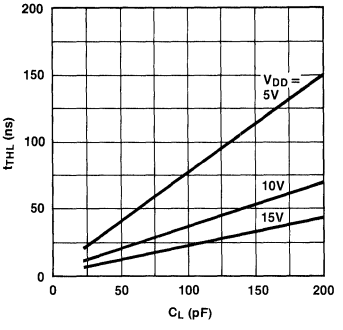
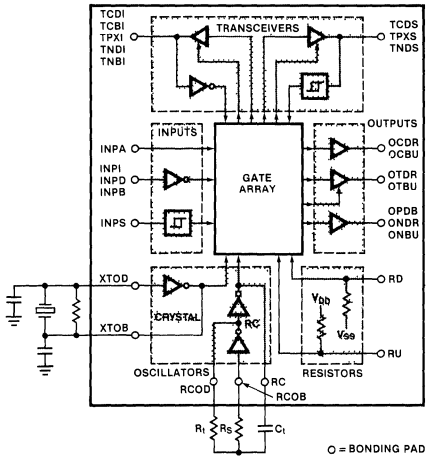


Figure 12. Output Transition Time (LOW-to-HIGH) as a Function of the Load Capacitance for Driver and Buffer Outputs

PERIPHERY

To provide a versatile interface, M-Series CMOS arrays have numerous I/O pads—see Figure 1a. These peripheral elements can be configured to match the input or output requirements of a wide variety of logic families. Accordingly, a bonding pad may have one of the following functions assigned to it:

- INPUT STAGE which includes an input protection circuit (series resistor and single diode clamp to V_{SS}). The recommended maximum load is 260 array gates, or 100 array gates for optimum speed performance. Because the input voltage is not clamped to V_{DD}, input voltages greater than the supply voltage is possible, thus allowing voltage level shifting.
- SCHMITT TRIGGER input stage for noise reduction, pulse shaping, or suppression of oscillation spikes associated with slow input clock transitions. The recommended maximum load is 10 array gates, or 5 for optimum speed performance.
- TRANSCEIVER input/output stage
- THREE-STATE output with driver or buffer performance capability for bussing applications
- COMPLEMENTARY OUTPUT with driver or buffer performance capability.
- OPEN DRAIN N- or P-transistor output
- PULL-UP/PULL-DOWN resistors (see Figure 2 for availability) may be added at various I/O stages. The values available are 5, 10, 15, 30, 60, 65, 70 and 75 Kohms.



TRANSCEIVERS WITH INVERTER INPUT	
TCDI	complementary driver output
TCBI	complementary buffer output
TPXI	open drain p-channel driver output
TNDI	open drain n-channel driver output
TNBI	open drain n-channel buffer output
TRANSCEIVER WITH SCHMITT TRIGGER INPUT	
TCDS	complementary driver output
TPXS	open drain p-channel driver output
TNDS	open drain n-channel driver output
INPUTS	
INPA	direct access to array
INPI	inverter
INPD	driver
INPB	buffer
INPS	Schmitt trigger
OUTPUTS	***FANOUT: DRIVER = 4 LSTTL LOADS @ 4.5V BUFFER = 6 LSTTL LOADS @ 4.5V***
OCDR	complementary driver
OCBU	complementary buffer
OTDR	3-state driver
OTBU	3-state buffer
OPDB	open drain p-channel driver
ONDR	open drain n-channel driver
ONBU	open drain n-channel buffer
OSCILLATORS	
XTOD	crystal oscillator with driver stage
XTOB	crystal oscillator with buffer stage
RCOD	RC oscillator with driver stage
RCOB	RC oscillator with buffer stage
RESISTORS	
RD	pull-down resistors
RU	pull-up resistors

Figure 13. The SCCXXXX I/O Cell Library

Table 1. THE SCCXXXX GATE ARRAY CELL LIBRARY

LIBRARY IDENT. CODE	LOGIC ELEMENT	FUNCTION	NUMBER OF UNITS	NUMBER OF EQUIV. GATES	REMARKS
Inverters/buffers					
GIN1	Inverter	A	¼	½	Max. 2 in one unit
GIN2	Array driver inverting	A	½	1	2 times GIN1
GIN3	Array driver inverting	A	¾	1 + ½	3 times GIN1
GIN4	Array driver inverting	A	1	2	4 times GIN1
GIN6	Array driver inverting	A	1 + ½	3	6 times GIN1
GIN8	Array driver inverting	A	2	4	8 times GIN1
GIN12	Array driver inverting	A	3	6	12 times GIN1
GB12	Array buffer non-inverting	A	1	2	2 times GIN1
GB13	Array buffer non-inverting	A	1	2	3 times GIN1
NAND/AND gates					
GNAND2	2-input NAND	$\overline{A1 \cdot A2}$	½	1	
GNAND3	3-input NAND	$\overline{A1 \cdot A2 \cdot A3}$	¾	1 + ½	
GNAND4	4-input NAND	$\overline{A1 \cdot A2 \cdot A3 \cdot A4}$	1	2	
GAND2	2-input AND	$A1 \cdot A2$	1	2	Output GIN2
GAND3	3-input AND	$A1 \cdot A2 \cdot A3$	1	2	
OR/NOR gates					
GNOR2	2-input NOR	$\overline{A1 + A2}$	½	1	
GNOR3	3-input NOR	$\overline{A1 + A2 + A3}$	¾	1 + ½	
GNOR4	4-input NOR	$\overline{A1 + A2 + A3 + A4}$	1	2	
GOR2	2-input OR	$A1 + A2$	1	2	Output GIN2
GOR3	3-input OR	$A1 + A2 + A3$	1	2	
Complex logic functions					
GF01	Complex function	$\overline{A1 + B1 \cdot B2}$	1	2	
GF02		$\overline{A1 + B1 \cdot B1 \cdot B3}$	1	2	
GF03		$\overline{A1 \cdot A2 + B1 \cdot B2}$	1	2	
GF06		$\overline{A1 + A2 + B1 \cdot B2}$	1	2	
GF15		$\overline{A1 + B1 \cdot (C1 + C2)}$	1	2	
GF51		$\overline{A1 \cdot (B1 + B2)}$	1	2	
GF52		$\overline{A1 \cdot (B1 + B2 + B3)}$	1	2	
GF53		$\overline{(A1 + A2) \cdot (B1 + B2)}$	1	2	
GF56		$\overline{A1 \cdot A2 \cdot (B1 + B2)}$	1	2	
GF65		$\overline{A1 \cdot (B1 + C1 \cdot C2)}$	1	2	
GXOR1	EXCLUSIVE-OR	$\overline{A \cdot B + \bar{A} \cdot \bar{B}}$	1	2	Unbuffered
GXNOR1	EXCLUSIVE-NOR	$A \cdot B + \bar{A} \cdot \bar{B}$	1	2	Unbuffered
GXOR2	EXCLUSIVE-OR	$A \cdot B + \bar{A} \cdot \bar{B}$	1	2	Buffered
GXNOR2	EXCLUSIVE-NOR	$A \cdot B + \bar{A} \cdot \bar{B}$	1	2	Buffered
GXOR3	EXCLUSIVE-OR	$A \cdot B + \bar{A} \cdot \bar{B}$	2	4	
Transmission gate latches					
GTL0	Strobed D-LATCH without SET and RESET		1	2	
GTLRP	Strobed D-LATCH with RESET		1 + ½	3	Positive triggered
GTLRN	Strobed D-LATCH with RESET		1 + ½	3	Negative triggered
GTLSP	Strobed D-LATCH with SET		1 + ½	3	Positive triggered
GTLSN	Strobed D-LATCH with SET		1 + ½	3	Negative triggered
GTL2	Strobed D-LATCH with SET and RESET		1 + ½	3	

Table 1. THE SCCXXXX GATE ARRAY CELL LIBRARY (Continued)

LIBRARY IDENT. CODE	LOGIC ELEMENT	FUNCTION	NUMBER OF UNITS	NUMBER OF EQUIV. GATES	REMARKS
Compound latches					
GGM0	MASTER module without SET and RESET		2	4	All positive triggered
GGMR	MASTER module with RESET		2	4	
GGMS	MASTER module with SET		2	4	
GGM2	MASTER module with SET and RESET		2	4	
GGS0	SLAVE module without SET and RESET		2	4	All negative triggered
GGSR	SLAVE module with RESET		2	4	
GGSS	SLAVE module with SET		2	4	
GGS2	SLAVE module with SET and RESET		2	4	
Transmission gate master-slave flip-flop (MD-D-FF)					
GT00	MS-D-FF without SET and RESET		2	4	
GTR0P	MS-D-FF with RESET on MASTER		2 + ½	5	Positive triggered
GTR0N	MS-D-FF with RESET on MASTER		2 + ½	5	Negative triggered
GTRRP	MS-D-FF with RESET on MASTER and SLAVE		3	6	Positive triggered
GTRRN	MS-D-FF with RESET on MASTER and SLAVE		3	6	Negative triggered
GTSSP	MS-D-FF with SET on MASTER and SLAVE		3	6	Positive triggered
GTSSN	MS-D-FF with SET on MASTER and SLAVE		3	6	Negative triggered
GT22	MS-D-FF with SET and RESET on MASTER and SLAVE		3	6	

DESIGNING A GATE ARRAY CHIP

The design of a gate array chip can be subdivided into several steps, which logically succeed each other, but can sometimes be performed in parallel. (See Figure 14.)

Logic Network Description

This transfers the user specification into a logic network description, using the gate array cells from the cell library.

The cell library contains several logic functions, ranging from simple logic gates (AND, NAND, etc.) to more complex flip-flop functions. For each cell, the logic function and timing are known. A macro-facility is available for user convenience.

SIMON — Logic Simulation

This step checks the logical behavior of the described network against the user specification. The well-proven logic simulator, SIMON, is used to simulate the response of the network on the user-supplied input stimuli. SIMON is an event-driven logic simulator with variable gate delay and uses five logic values (HIGH, LOW, UNKNOWN, etc.).

If the response of the simulated network does not comply with the user specification, the network has to be corrected and simulated again.

INGATE, Cell Placement and Routing

The INGATE step takes care of cell placement and automatic routing in accordance with the logic network description. The gate array cells used in the network have to be placed on the chip area in rows. The special construction of the cells results in very efficient use of the available chip area. The INGATE program calculates the wiring for the entire chip using only two mask steps (contacts and aluminum). User interaction is possible and useful for extremely dense circuits.

When large signal tracks occur on a chip, the capacitance of these can increase the fan-out driven by a gate output. This extra fan-out is computed in the INGATE program and can be fed back for use in the SIMON program to calculate the extra delay values that are necessary.

Mask-Making

The INGATE program interfaces directly with the CIRCUIT MASK program, which produces the control tapes for the mask generators for the two masks.

Testing

The logic simulator enables the fault coverage and efficiency of the user-supplied test sequences to be determined. The program interfaces with a test generation program that adds the d.c. parametric test and generates the control tapes to enable testing on any of the equipment used in the CAD program.

This equipment includes the following:

- Sentry VII
- Sentry 21

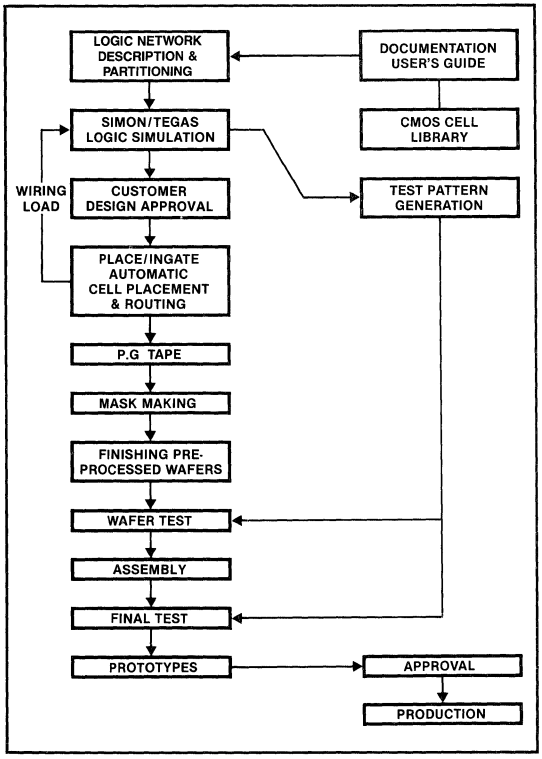


Figure 14. Development Flow

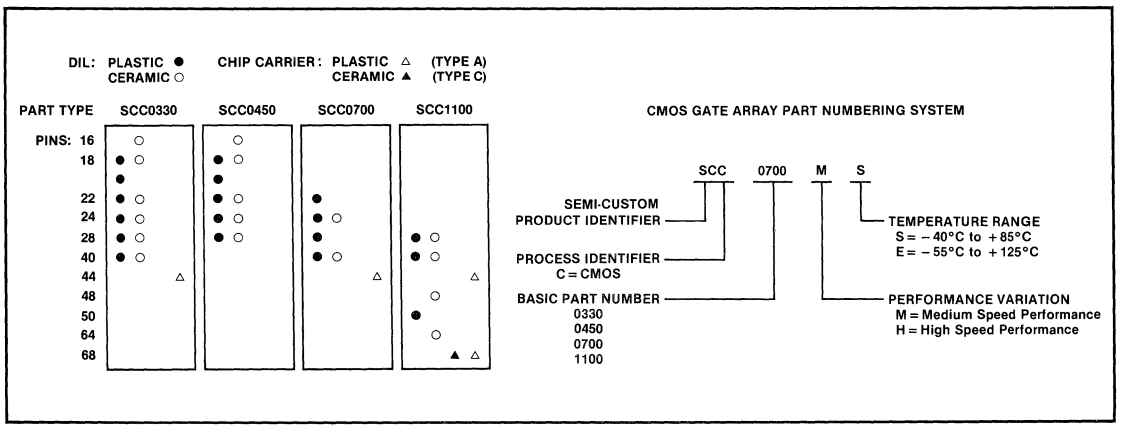
DESIGN PROCEDURE

Gate Count

The following step-by-step procedure is intended to guide the designer in determining the correct gate count.

- Simplify the logic circuit.
- Prepare a detailed logic drawing using only library cells provided in this data sheet.
- Expand all MSI functions to the level of gates and flip-flops (see e.g. the logic diagrams HE4000B family).
- Eliminate all unused functions and simplify the complex functions. Standard off-the-shelf products e.g. up/down counters, programmable counters and latches are often devices for considerable simplification.
- Partition the logic into several sections based on the pattern of interconnecting wiring. Circuits with numerous interconnections should be grouped together and interconnections between groups should be kept to a minimum.
- Examine the logic to see if complex functions can be used to reduce the gate count. Reduction can be achieved by using GF.. functions and eliminating unnecessary inversions.
- Rearrange the logic into the library cells. When fan-out is more than 10 to 15, add or use buffers to minimize delays.
- One "equivalent gate" is a 2-input device.
- A rough estimate count can quickly be made by using HE4000B family gate count table.
- Sequential logic is more desirable as extensive, random interconnection yields a lower utilization factor. In addition, regular LSI functions, such as memories, may lead to inefficient use of a gate array.

PACKAGING INFORMATION AND PART NUMBERING SYSTEM



GATE COUNT FOR HE400B FAMILY

A gate count is given below of 98 different devices that are described in the HE4000B CMOS Family Databook.

Only the gates to be implemented in the array area are given.

The connections to the 'outside world' are via the inputs or outputs located in the periphery area (among the bonding pads).

Preliminary list (use for indication only)

TYPE NUMBER	NUMBER OF EQUIV. GATES	TYPE NUMBER	NUMBER OF EQUIV. GATES
HEF4000B	4	HEF4502B	6
HEF4001UB	4	HEF4508B	12
HEF4002B	4	HEF4510B	82
HEF4006B	76	HEF4511B	49
HEF4007B	▲	HEF4512B	26
HEF4008B	45	HEF4514B	60
HEF4011UB	4	HEF4515B	60
HEF4012B	4	HEF4516B	82
HEF4013B	14	HEF4517B	552
HEF4014B	57	HEF4518B	58
HEF4015B	41	HEF4519B	27
HEF4017B	38	HEF4520B	54
HEF4018B	57	HEF4521B*	128
HEF4019B	8	HEF4522B	62
HEF4020B	70	HEF4526B	62
HEF4021B	73	HEF4527B	60
HEF4022B	31	HEF4528B	—
HEF4023B	6	HEF4531B	36
HEF4024B	35	HEF4532B	24
HEF4025B	6	HEF4534B	—
HEF4027B	22	HEF4539B	24
HEF4028B	23	HEF4541B**	100
HEF4029B	75	HEF4543B	65
HEF4030B	12	HEF4555B	16
HEF4031B	277	HEF4556B	16
HEF4035B	46	HEF4557B	360
HEF4040B	61	HEF4585B	40
HEF4041B	▲	HEF4724B	52
HEF4042B	11	HEF4731B; V	1064
HEF4043B	8	HEF4737B; V	—
HEF4044B	8	HEF40097B	▲
HEF4047B	—	HEF40098B	▲
HEF4049B	▲	HEF40106B	▲
HEF4050B	▲	HEF40160B	54
HEF4068B	6	HEF40161B	54
HEF4069UB	▲	HEF40162B	52
HEF4070B	12	HEF40163B	52
HEF4071B	8	HEF40174B	34
HEF4072B	6	HEF40175B	24
HEF4073B	6	HEF40192B	68
HEF4075B	6	HEF40193B	68
HEF4076B	30	HEF40194B	64
HEF4077B	12	HEF40195B	40
HEF4078B	6	HEF40240B	▲
HEF4081B	8	HEF40244B	▲
HEF4082B	4	HEF40245B	▲
HEF4085B	8	HEF40373B	16
HEF4086B	8	HEF40374B	32
HEF4093B	▲		
HEF4094B	54		

*Excluding V'_{DD} and V'_{SS}
**Excluding power-on reset
▲Located in the periphery

9

FEATURES

- 1.5 nsec typical gate delay
- Up to 2000 actual gates
- I/Os limited by package
- 250uW per gate
- Up to 48 mA output drive
- TTL Compatible
- Full CAD support
- Automatic schematic input
- Circuit simulation
- Automatic place and route
- Automatic macro generation
- Hard and soft macros
- Variable die size
- Plastic and ceramic chip carriers
- Standard DIPs

BENEFITS

- Fast, easy design
- Efficient use of silicon
- Proprietary LSI device
- High speed
- Replaces up to 100 SSI/MSI parts
- Reduces PCB area
- Saves manufacturing costs
- Reduces size, weight and power
- Improves system reliability

ORDERING INFORMATION

Contact Local Sales Representative

PRODUCT DESCRIPTION

The FLEXX™ array represents a major advance in semicustom technology which combines a new concept in architecture with the most advanced CAD available. With it you can create your proprietary semicustom LSI device quickly and easily, much like gate array or standard cell methodology, but with silicon utilization as efficient as standard LSI products designed by traditional handpacking methods. As a result of its superior design and silicon utilization efficiency the FLEXX™ Array is being used by Signetics to develop standard LSI products. The FLEXX™ Array is now available to Signetics customers as a semicustom development tool.

FLEXX™ Array Architecture

As shown in the figure, the FLEXX™ Array is composed of macros, which are rectangular assemblies of gates, with additional random gates included as required. The macros are variable in length and width for optimum routing efficiency, and the routing channel width is variable to accommodate only those traces required to route the chip. No unused gates are included. As a result of this architecture, the FLEXX™ Array is much more efficient in silicon utilization than a gate array or standard cell array, which means that the end device will have a smaller die and therefore a lower cost.

Multi-Level Software

To assembly the FLEXX™ Array Signetics uses multi-level automatic place and route software. The first level automatically generates the macros; it establishes the macro width and interconnects the gates within the macro. The second level places and interconnects the macros as well as individual gates; it varies the spacing between macros to accommodate the required interconnecting traces. This process is fully automatic and can be done quickly which speeds the development of your FLEXX™ Array.

Fully Automatic Design

To design a FLEXX™ Array the user enters the schematic and test vectors with a remote terminal then reviews the computer simulation of the circuit. In this procedure the user has the choice of using established ("hard") macros from Signetics computer library, modifying these macros or creating new ("soft") macros as required. Once the simulation is completed, Signetics takes over and routes the chip and procedures prototypes within ten weeks.

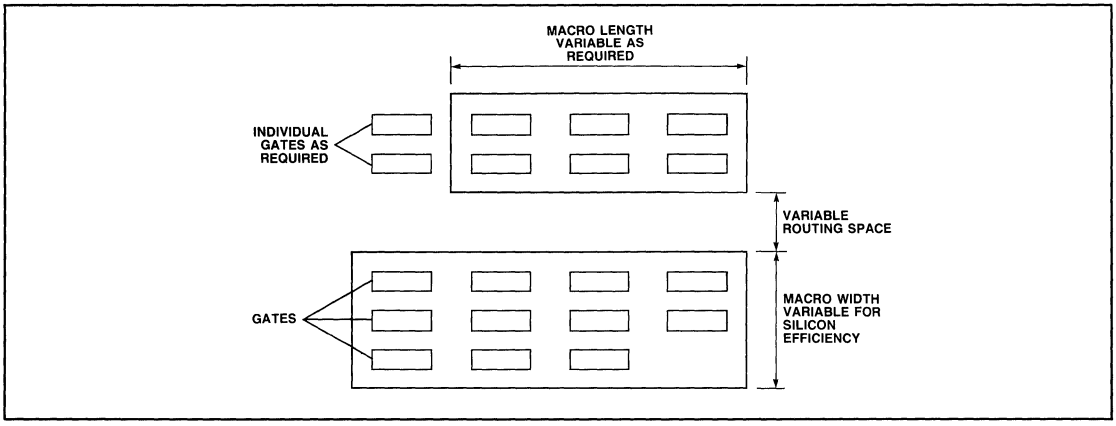
Silicon Technology — Performance

The FLEXX™ Array is a methodology for assembling a logic design on silicon; it is therefore largely independent of the particular silicon technology and can be used with CMOS and varieties of bipolar technology.

The first technology used to implement the FLEXX™ Array is oxide isolated ISL or Integrated Schottky Logic. ISL provides a superior speed power product with the speed of LSTTL at one-tenth the power. With oxide isolation, both the speed-power product and the gate delay of ISL are reduced by a factor of three, giving the FLEXX™ Array speed approaching ECL and power efficiency that allows large scale integration in a plastic package without special cooling.

With oxide-isolated ISL the gate used in the FLEXX™ Array has a typical delay time of 1.5 nsec. Output buffers are capable of driving up to 48 mA. The number of actual gates which can be placed on the FLEXX™ Array is limited to about 2000 by thermal constraints. The number of I/Os is limited only by package pin-out. Available packages currently include standard plastic and ceramic DIPs and a variety of chip carriers.

FLEXX™ ARRAY ARCHITECTURE



ISL GATE ARRAY 8A1200

FEATURES

- **Customer programmable LSI**
- **1144 ISL (NAND) gates**
- **Two-layer metal interconnection**
- **52 Schottky buffers**
- **36 I/O buffers**
- **LSTTL compatible**
- **Standard PNP inputs**
- **8mA output current sink**
- **−55°C to +125°C ambient temperature**
- **4ns gate speed (typical)**
- **Speed-power product—0.7 picojoules**
- **22, 28, 40, or 44-pin package**

PRODUCT DESCRIPTION

The 8A1200 Gate Array (Figure 1) is an uncommitted array of ISL gates (Figure 2), Schottky buffers (Figure 3) and LSTTL-compatible I/O cells (Figure 4). Thus, up to 1200 gates can be custom interconnected to provide the advantages of both Large Scale Integration (LSI) and proprietary design. The 8A1200 array is based on a technological subset of LSI called ISL (Integrated Schottky Logic). ISL combines the best features of low-power Schottky and I^2L Bipolar technologies.

Designing with the 8A1200 is easy and fast, requiring no more than conventional logic design, logic simulation, and custom coding of metal interconnections among preprocessed logic gates on the array—refer to Table 1 for a comparison of ISL and 74LS logic functions. The design techniques and the implementation processes are analogous to the design of a Printed Circuit Board.

Logic functions are defined by the user and are implemented by interconnecting 1144 ISL NAND gates, using two layers of metal routing Fifty-two Schottky buffers are provided to drive multi-load internal clock or enable signals. For external interface, up to 36 LSTTL I/O buffers can be specified. As shown in Figure 4, each I/O can be configured to implement any one of 11 different functions: inputs, input/output, totem-pole, open collector, and three-state.

ORDERING INFORMATION

Contact Local Sales Representative

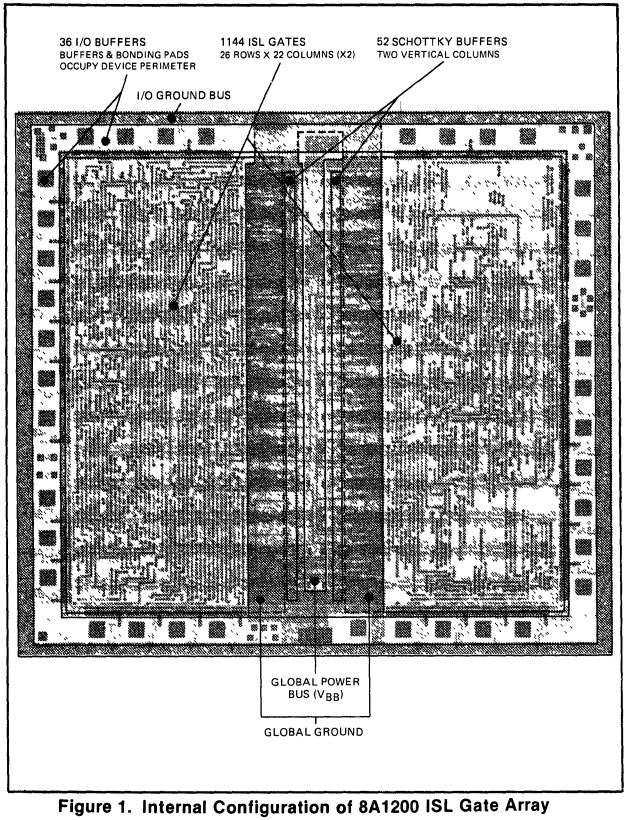


Figure 1. Internal Configuration of 8A1200 ISL Gate Array

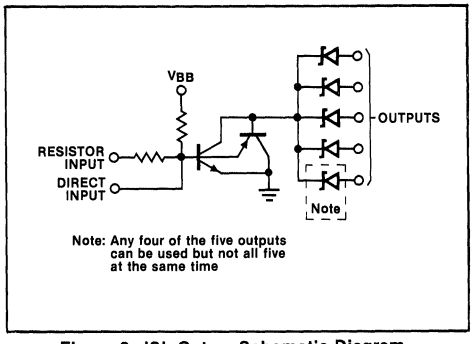


Figure 2. ISL Gate—Schematic Diagram

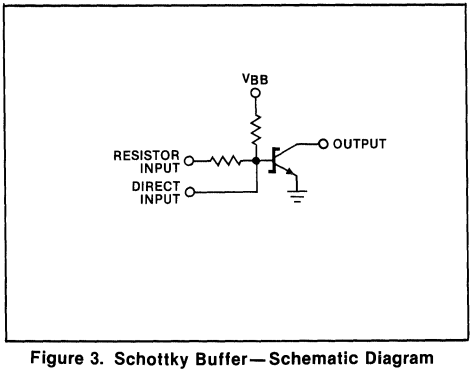


Figure 3. Schottky Buffer—Schematic Diagram

INPUT/OUTPUT CELLS

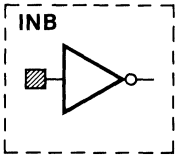
All signals within the array interface to external pins via I/O buffers located around the device perimeter A description plus the symbolic logic, and schematic representation for each I/O cell are shown in Figure 4

INPUT BUFFERS

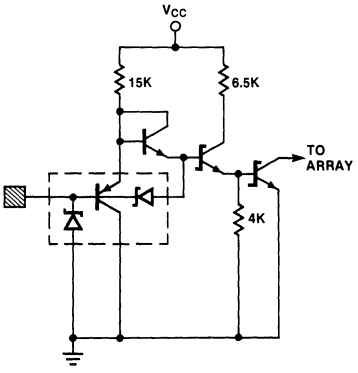
DESCRIPTION:

Low power Schottky input buffer with low current PNP input transistor.

SYMBOL & LOGIC:



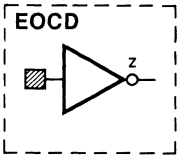
SCHEMATIC:



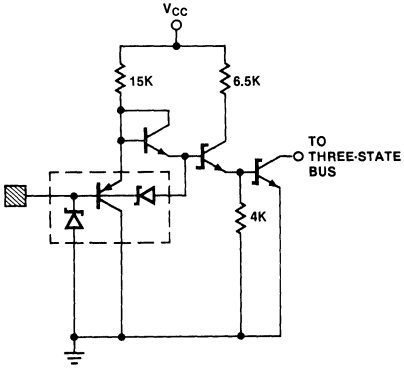
DESCRIPTION:

Input cell with output driver for driving the three-state enable of three-state output cells.

SYMBOL & LOGIC:



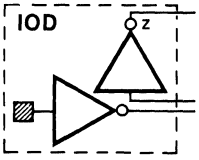
SCHEMATIC:



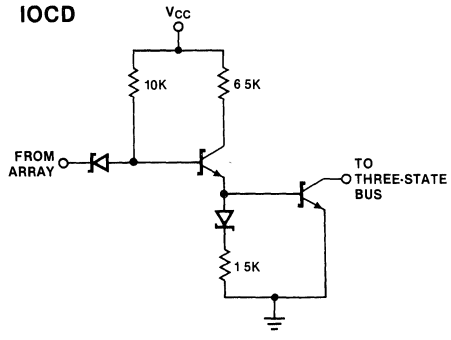
DESCRIPTION:

Input with three-state driver. This is a back-to-back configuration of an input buffer and and internal three-state driver (INB + IOCD).

SYMBOL & LOGIC:



SCHEMATICS:



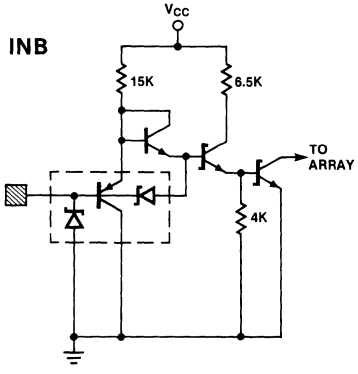


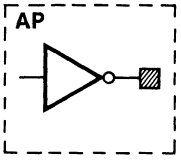
Figure 4. Description and Symbolic, Logic, and Schematic Representation of Eleven I/O Cells

OUTPUT BUFFERS

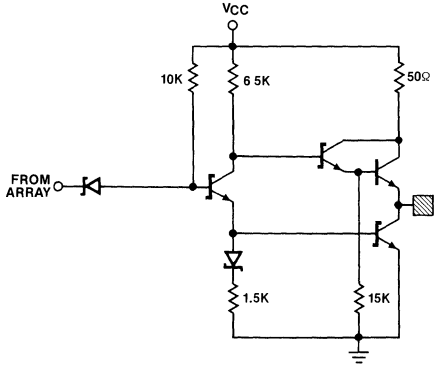
DESCRIPTION:

Standard low power Schottky output buffer with totem pole active pull-up.

SYMBOL & LOGIC:



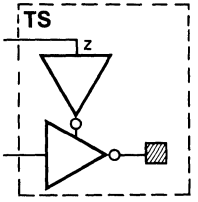
SCHEMATIC:



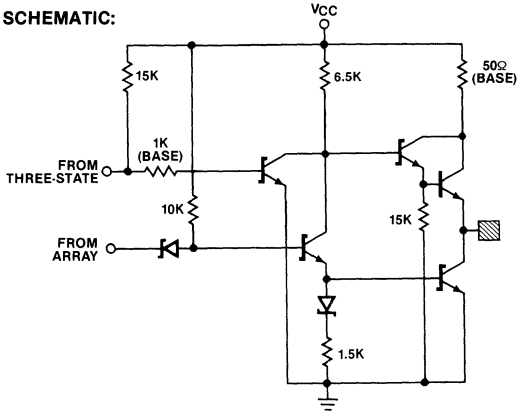
DESCRIPTION:

Standard three-state low power Schottky output.

SYMBOL & LOGIC:



SCHEMATIC:

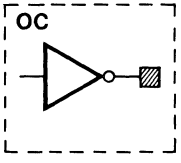


Preliminary

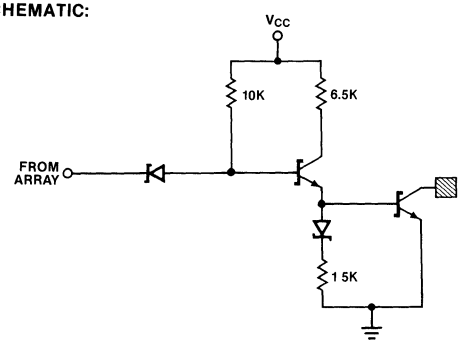
DESCRIPTION:

Low power Schottky output buffer with open-collector output.

SYMBOL & LOGIC:



SCHEMATIC:

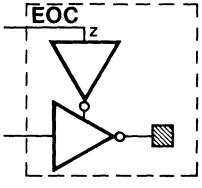


Preliminary

DESCRIPTION:

Low power Schottky output buffer with open-collector output. Enabled from a three-state enable signal.

SYMBOL & LOGIC:



SCHEMATIC:

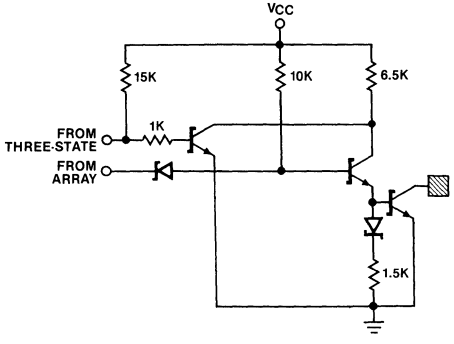


Figure 4. (continued) Description and Symbolic, Logic, and Schematic Representation of Eleven I/O Cells

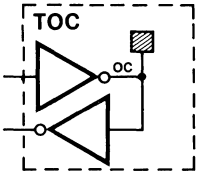
TRANSCEIVERS

Preliminary

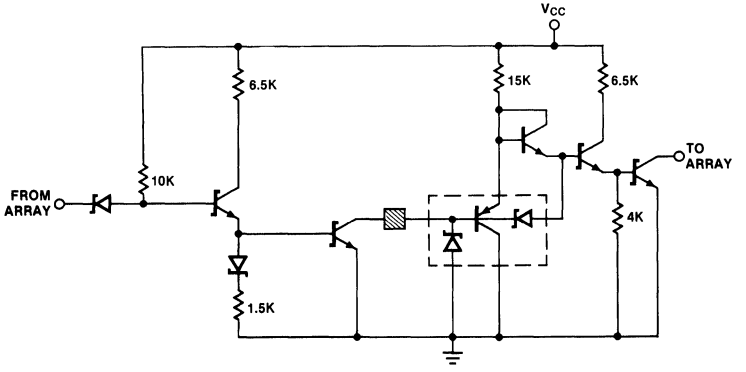
DESCRIPTION:

Open-collector transceiver. This is a back-to-back configuration of an input buffer and an open-collector output buffer (INB + OC).

SYMBOL & LOGIC:



SCHEMATIC:

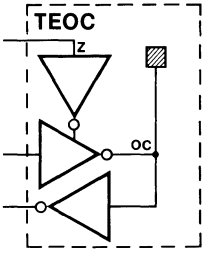


Preliminary

DESCRIPTION:

Enabled open-collector transceiver. This is a back-to-back configuration of an input buffer and an enabled open-collector output buffer (INB + EOC).

SYMBOL & LOGIC:



SCHEMATIC:

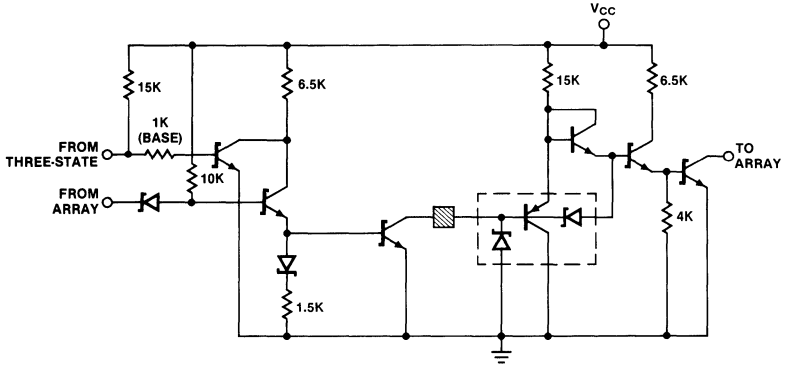


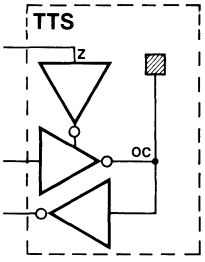
Figure 4. (continued) Description and Symbolic, Logic, and Schematic Representation of Eleven I/O Cells

TRANSCEIVERS (Continued)

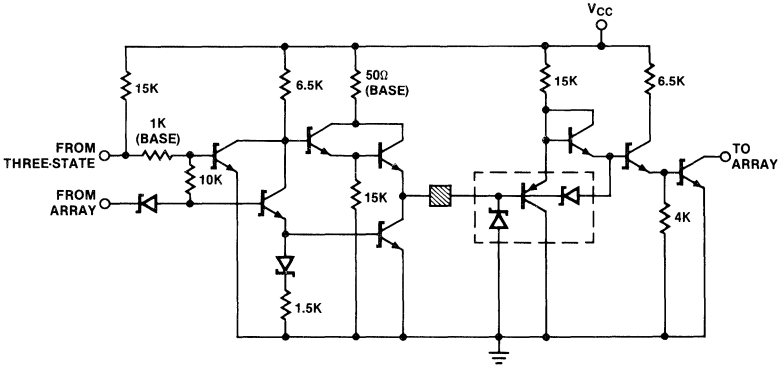
DESCRIPTION:

Three-state transceiver. This is a back-to-back configuration of an input buffer and a three-state output in one I/O cell (INB + TS).

SYMBOL & LOGIC:



SCHEMATIC:

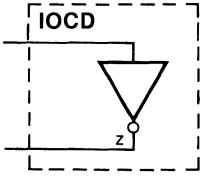


OTHER

DESCRIPTION:

Same as EOCD, except input is designed to interface with ISL gates. This cell is used internally and does not interface to an external pin.

SYMBOL & LOGIC:



SCHEMATIC:

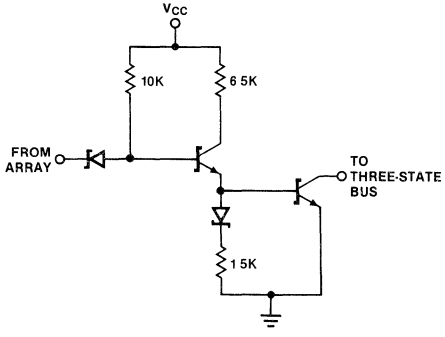


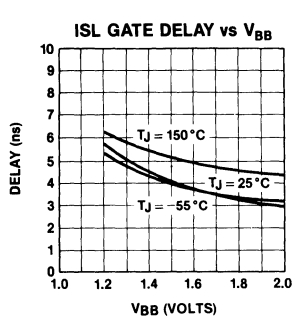
Figure 4. (continued) Description and Symbolic, Logic, and Schematic Representation of Eleven I/O Cells

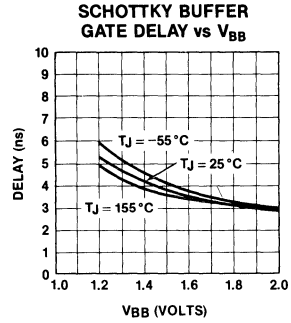
TYPICAL PERFORMANCE CHARACTERISTICS

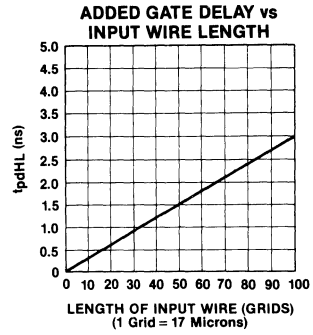
Overall performance of the gate array is determined by the following parameters:

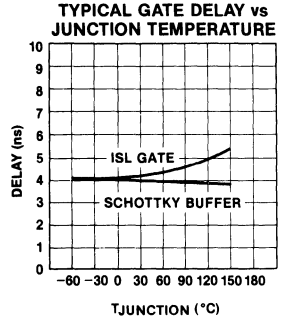
- Discrete gate delays
- Gate current (I_{BB}) and gate voltage (V_{BB})
- Junction Temperature (T_J)

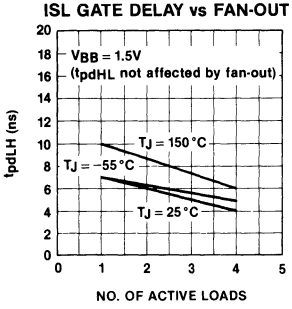
Gate delays are subject to several variables, any one of which can affect the overall circuit performance. An analysis of these variables is shown in the accompanying graphs.

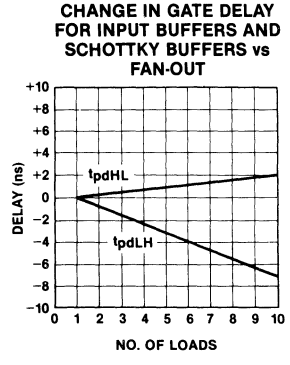


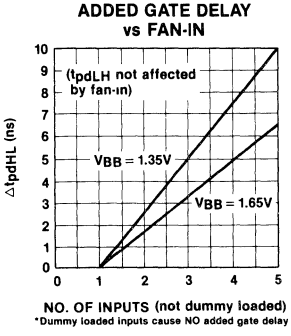












POWER DISSIPATION

For the purpose of package selection, the maximum power dissipation for any given implementation of the 8A1200 gate array is given by the following equation.

Maximum Power (in mW) = 0.25 mW x number of ISL
plus, 0.25 mW x number of Schottky buffers used
plus, 12 mW x number of TTS, TOC, and TEOC buffers
plus, 8 mW x number of AP, OC, EOC, TS and IOD buffers
plus, 5 mW x number of EOCD, INB, and IOCD buffers
plus, 0.5V x load current (in mA) of output buffers

NOTE:
Load Current = maximum I_{OL} for selected temperature range x the total number of output buffers and transceivers that cna simultaneously be at a low output state

Table 1. COMPARISON OF ISL WITH 74LS FUNCTIONS

LOGIC FUNCTION	PARAMETERS[3]	ISL[1]	74LS
NAND (7400)	Power (in mW)	0.30	2.00
	T_{ON} (in ns)	2.00	15.00
	T_{OFF} (in ns)	10.00	15.00
AND (7408)	Power (in mW)	0	11.00
	T_{ON} (in ns)	0	20.00
	T_{OFF} (in ns)	2^2	15.00
EXCLUSIVE OR (7486)	Power (in mW)	1.20	12.50
	T_{ON} (in ns)	18.00	22.00
	T_{OFF} (in ns)	24.00	30.00
EXCLUSIVE NOR (74266)	Power (in mW)	0.90	18.00
	T_{ON} (in ns)	15.00	30.00
	T_{OFF} (in ns)	16.00	30.00
D FLIP-FLOP (7474) $C \rightarrow \overline{Q}$	Power (in mW)	1.50	20.00
	T_{ON} (in ns)	28.00	40.00
	T_{OFF} (in ns)	28.00	40.00
D LATCH (7475) DATA $\rightarrow \overline{Q}$	Power (in mW)	1.20	30.00
	T_{ON} (in ns)	5.00	17.00
	T_{OFF} (in ns)	12.00	17.00
4-INPUT MUX (74153) DATA $\rightarrow \overline{Q}$	Power (in mW)	1.50	25.00
	T_{ON} (in ns)	7.00	26.00
	T_{OFF} (in ns)	16.00	26.00

Notes:
1. Power and delay times are given for 150°C MAX.
2. T_{OFF} is 2ns for each input; T_{OFF} can be reduced to 0ns with a pullup cell which uses 0.3 mW.
3. LS power dissipation is based on $V_{CC} \times I_{MAX}$.

AC AND DC ELECTRICAL CHARACTERISTICS

Conditions: Commercial—
$V_{CC} = 5.0V (\pm 5\%)$
$V_{BB} = 1.5V (\pm 10\%)$
$T_A^1 = 0°C$ to $70°C$

Military—
$V_{CC} = 5.0V (\pm 10\%)$
$V_{BB} = 1.5V (\pm 10\%)$
$T_A^1 = -55°C$ to $125°C$

ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V
V_{BB}	ISL gate supply voltage	+7.0	V
E_{IN}	Input voltage, continuous	−0.5 to +5.5	V
I_{IN}	Input current, continuous	−30 to +1.0	mA
V_O	Voltage applied to open-collector output in off-state	−0.5 to +7.0	V
T_A	Ambient temperature, operating	−55 to +125	°C
T_{STG}	Storage temperature	−65 to +150	°C

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL) MIN	TYP	MAX	LIMITS (MILITARY) MIN	TYP	MAX	UNITS
ISL GATE (Internal)									
I_{BB}/G	Power supply current per gate				190			190	μA
ILF	Input load factor				1			1	Unit load
FO	Fanout				4			4	Unit load
t_{pdAV}	Average gate propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = one (1) ISL gate or Schottky buffer Fan-out = one (1) ISL gate or Schottky buffer		4	6		4	6	ns
$t_{pdHL}2$	High-to-low propagation delay	Delay is inferred from circuit simulation		1	2		1	2	ns
$t_{pdLH}2$	Low-to-high propagation delay			7	10		7	10	ns
SCHOTTKY BUFFER (Internal)									
I_{BB}/G	Power supply current per gate				190			190	μA
ILF	Input load factor				1			1	Unit load
FO	Fanout				10			10	Unit load
t_{pdAV}	Average gate propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = one (1) ISL gate or Schottky buffer Fan-out = one (1) ISL gate or Schottky buffer		4	6		4	6	ns
$t_{pdHL}2$	High-to-low propagation delay	Delay is inferred from circuit simulation		1	2		1	2	ns
$t_{pdLH}2$	Low-to-high propagation delay			7	10		7	10	ns

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INTERNAL BUFFERS: IOD, IOCD (Internal)									
I_{CC}	IOCD power supply current	From array = high			1.38			1.50	mA
	IOD power supply current	V_{IN} = 3V, from array = high			2.53			2.75	mA
ILF	Input load factor					3			Unit load
FO	Fanout								
	To T.S. (I/O only)	(drives 3-state inputs only)				16		16	Inputs
	To Array (I/O only)	(drives internal gates)				10		10	Unit loads
t_{pdAV}	Average propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan in = one (1) ISL gate or Schottky buffer Fan out = one (1) from 3-state input of an output buffer			10	14	10	14	ns
INPUT BUFFERS: INB, EOCD, TEOC[3] (to array), IOD (to array), TOC (to array), TTS[3] (to array)									
I_{CC}	TOC, supply current	V_{IN} = 3V, from Array = L			1.76			1.90	mA
	INB, EOCD, supply current	V_{IN} = 3V			1.15			1.25	mA
	IOD, supply current	V_{IN} = 3V, from Array = H			2 53			2.75	mA
	TEOC, supply current	V_{IN} = 3V, from TS = H, from Array = L			3.11			3.35	mA
	TTS, supply current	From Array = L, from TS = H V_{IN} = 3V			3.11			3.35	mA
V_{TH}	Input threshold voltage		0.80		2.0	0.80		2.0	V
V_{CD}	Input clamp diode voltage	I_{IN} = − 18mA			− 1.5			− 1 5	V
I_{IL}	Input low current	V_{IN} = 0.4V			− 20			− 20	μA
I_{IH}	Input high current	V_{IN} = 2.7V			20			20	μA
I_I	Max input high current	V_{IN} = 5.5V, V_{CC} = Max			100			100	μA
FO	INB & IOD "to array" outputs				10			10	Unit load
	EOCD & IOD "to 3-state" outputs				16			16	Inputs
t_{pdLH}	Propagation delay, low-to-high F.O. = one (1) ISL load	See Figure 5a		5	8		5	8	ns
t_{pdHL}	Propagation delay, high-to-low F.O. = one (1) ISL load			2	4		2	4	ns
t_{pdLH}	Propagation delay, low-to-high F.O. = ten (10) ISL loads			3	4		3	4	ns
t_{pdHL}	Propagation delay, high-to-low F.O. = ten (10) ISL loads			4	5		4	5	ns
OUTPUT BUFFER: AP (Active Pullup)									
I_{CC}	Power supply current	From array = high			1.38			1.50	mA
ILF	Input load factor		3			3			Unit loads
V_{OL}	Output low voltage	I_{OL} = 8mA			500				mV
		I_{OL} = 4mA						400	mV
V_{OH}	Output high voltage	I_{OH} = − 400μA	2.7			2.5			V
I_{OS}	Output short circuit current	V_{OUT} = 0V	− 15		− 100	− 15		− 100	mA
t_{pdLH}	Propagation delay, low to high output	See Figure 5b		4	8		4	8	ns
t_{pdHL}	Propagation delay, high to low output			4	8		4	8	ns

ISL GATE ARRAY 8A1200

	PARAMETER	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OPEN COLLECTOR, OUTPUT BUFFERS: OC, TOC (from array), EOC, TEOC (from array)									Preliminary
I_{CC}	OC power supply current	From array = high			1.38			1.50	mA
	TOC power supply current	From array = low			1.76			1.90	mA
	EOC power supply current	From array = low, from T.S. = high			1.96			2.10	mA
	TEOC power supply current	From array = low, from T.S. = high			3.11			3.35	mA
ILF	Input load factor "from array"		3			3			Unit load
	Input load factor "from T.S."		3			3			Unit load
V_{OL}	Output low voltage	I_{OL} = 8mA comm			500				mV
		I_{OL} = 4mA						400	mV
I_{OH}	Output high current	V_{OUT} = 5.5V			20			20	μA
t_{pdLH}	Propagation delay low to high output	See Figure 5c		9	TBD		9	TBD	ns
t_{pdHL}	Propagation delay high to low output			8	TBD		8	TBD	ns
THREE-STATE OUTPUT BUFFERS: TS, TTS (from array)									
I_{CC}	TS power supply current	From T.S. = high From array = low			1.96			2.10	mA
	TTS power supply current	From array = low V_{IN} = 3V, from T.S. = high			3.11			3.35	mA
ILF	Input load factor, either input		3			3			Unit load
V_{OL}	Output low voltage	I_{OL} = 8mA			500				mV
		I_{OL} = 4mA						400	mV
V_{OH}	Output high voltage	I_{OH} = − 400μA	2.7			2.5			V
I_{OS}	Output short circuit current	V_{OUT} = 0V	− 15		− 100	− 15		− 100	mA
I_{OZL}	Three-state off current, output low	V_{OUT} = 0.4V			− 20			− 20	μA
I_{OZH}	Three-state off current, output high	V_{OUT} = 2.4V			20			20	μA
t_{pdLH}	Propagation delay, low to high output	See Figure 5d		4	9		4	9	ns
t_{pdHL}	Propagation delay, high to low output			6	10		6	10	ns
t_{pdZL}	Propagation delay, HI Z to low output			11	14		11	14	ns
t_{pdZH}	Propagation delay, HI Z to high output			10	13		10	13	ns
t_{pdLZ}	Propagation delay, low to HI Z output			6	12		6	12	ns
t_{pdHZ}	Propagation delay, high to HI Z output			7	7		7	7	ns

NOTES
1 Maximum power dissipation limit of circuit is determined by package selection
2 Guaranteed value is t_{pdAV}
3 For all input parameters on TEOC and TTS, the "form Three-State" input should be high

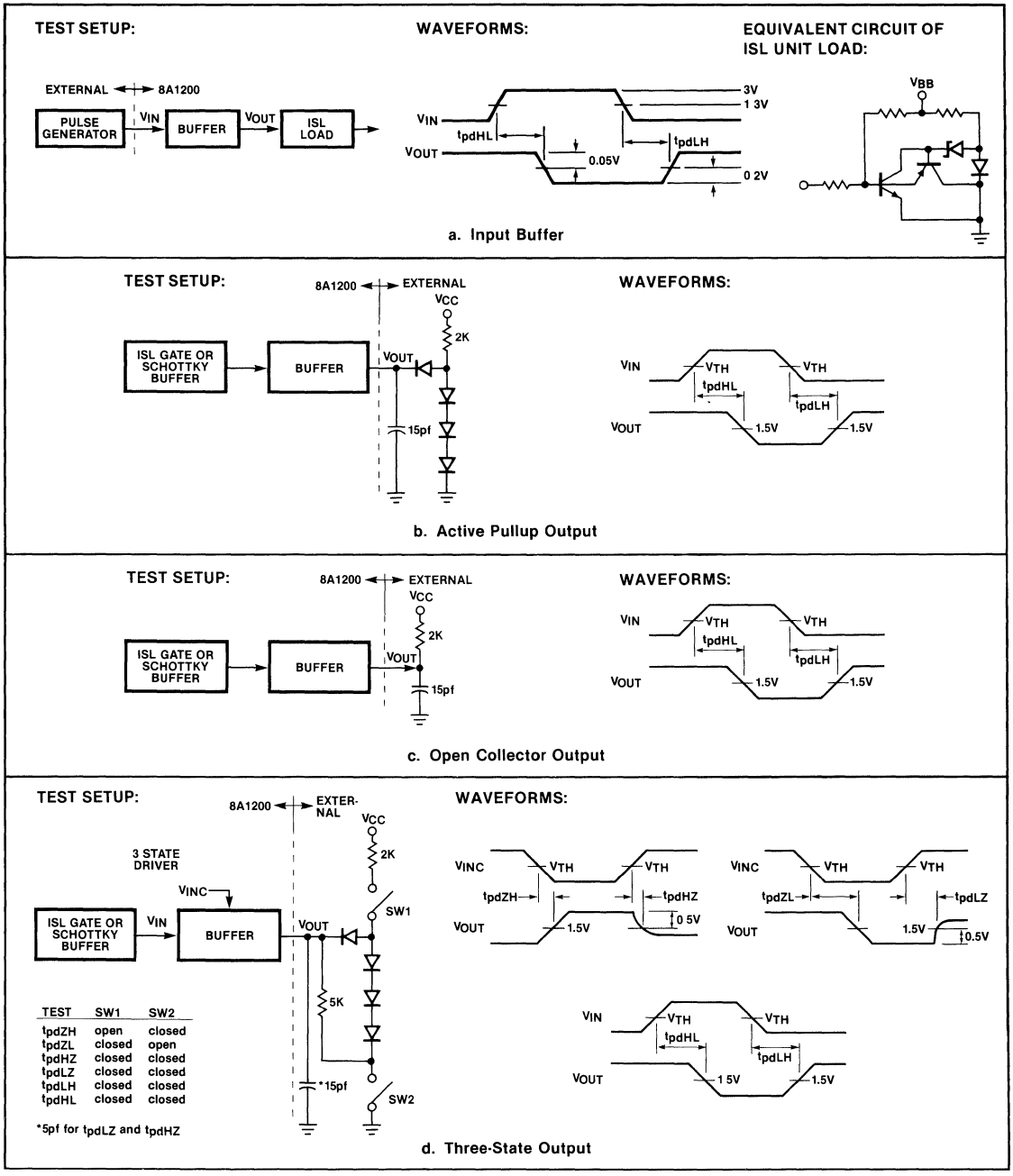


Figure 5. Test Circuits

FEATURES

- **Customer programmable LSI**
- **1144 ISL (NAND) gates**
- **Two-layer metal interconnection**
- **52 Schottky buffers**
- **60 I/O buffers**
- **LSTTL compatible**
- **Standard PNP inputs**
- **8mA output current sink**
- **−55°C to +125°C ambient temperature**
- **4ns gate speed (typical)**
- **Speed-power product—0.7 picojoules**
  68 pin package

PRODUCT DESCRIPTION

The 8A1260 Gate Array (Figure 1) is an uncommitted array of ISL gates (Figure 2), Schottky buffers (Figure 3) and LSTTL-compatible I/O cells (Figure 4). Thus, up to 1200 gates can be custom interconnected to provide the advantages of both Large Scale Integration (LSI) and proprietary design. The 8A1260 array is based on a technological subset of LSI called ISL (Integrated Schottky Logic). ISL combines the features of Schottky and the density of I^2L Bipolar technologies.

Designing with the 8A1260 is easy and fast, requiring no more than conventional logic design, logic simulation, and custom coding of metal interconnections among preprocessed logic gates on the array. Refer to Table 1 for a comparison of ISL and 74LS logic functions. The design techniques and the implementation processes are analogous to the design of a Printed Circuit Board.

Logic functions are defined by the user and are implemented by interconnecting 1144 ISL NAND gates, using two layers of metal routing. Fifty-two Schottky buffers are provided to drive multi-load internal clock or enable signals. For external interface, up to 60 LSTTL I/O buffers can be specified. Each I/O can be configured as 1-of-4 input buffers, 1-of-4 output buffers, or as a combination of one input buffer and one output buffer for a transceiver.

ORDERING INFORMATION

Contact Local Sales Representative

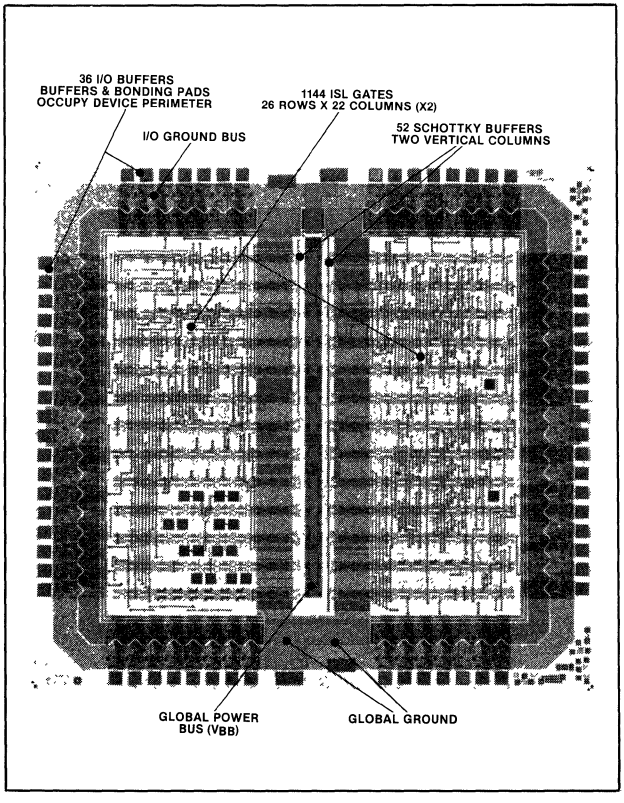


Figure 1. Internal Configuration of 8A1260

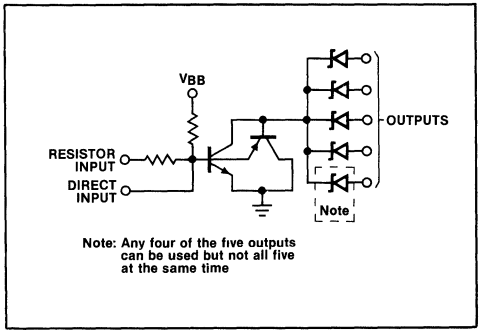


Figure 2. ISL Gate—Schematic Diagram

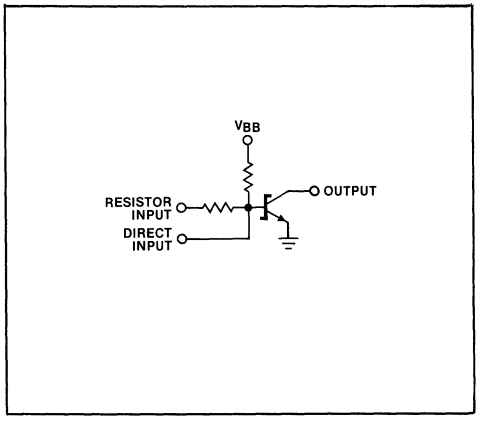


Figure 3. Schottky Buffer—Schematic Diagram

INPUT/OUTPUT CELLS

All signals within the array interface to external pins via I/O buffers located around the device perimeter

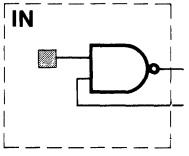
A description plus the symbolic, logic, and schematic representation for each I/O cell are shown in Figure 4

INPUT BUFFERS

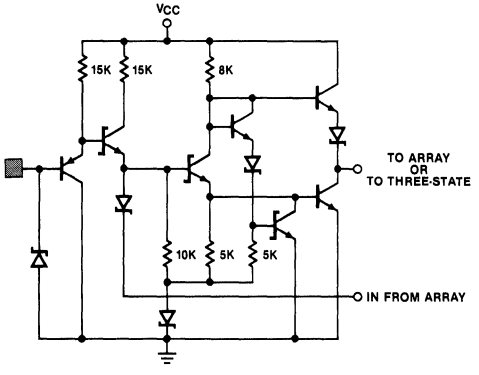
DESCRIPTION:

Low Power Schottky input buffer with internal feedback and direct output.

SYMBOL & LOGIC:



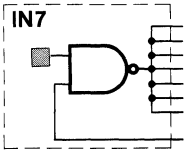
SCHEMATIC:



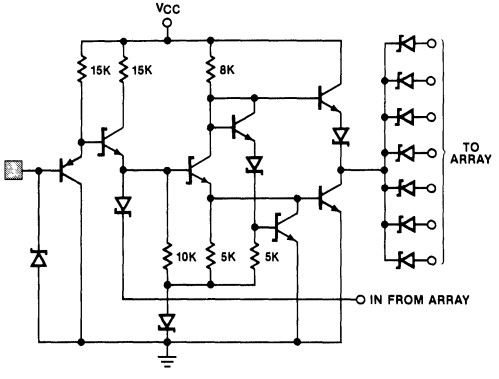
DESCRIPTION:

Low Power Schottky input buffer with internal feedback and diode output.

SYMBOL & LOGIC:



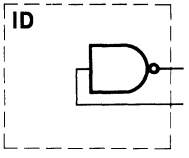
SCHEMATIC:



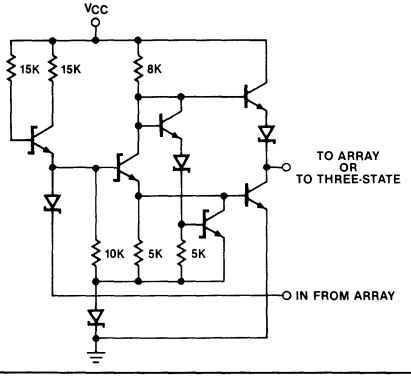
DESCRIPTION:

Internal driver with direct output.

SYMBOL & LOGIC:



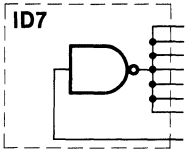
SCHEMATIC:



DESCRIPTION:

Internal driver with diode output.

SYMBOL & LOGIC:



SCHEMATIC:

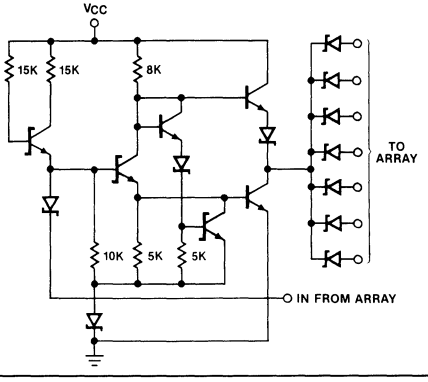


Figure 4. Description and Symbolic, Logic, and Schematic Representation of Eight I/O Cells

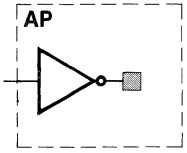
9

OUTPUT BUFFERS

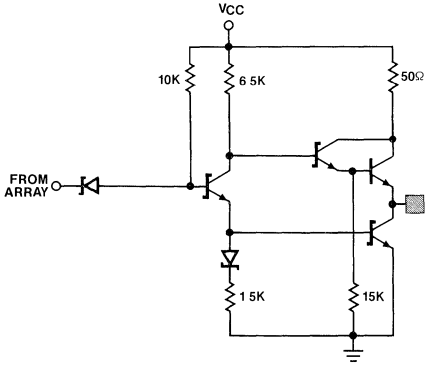
DESCRIPTION:

Low Power Schottky output buffer with totem pole active pullup.

SYMBOL & LOGIC:



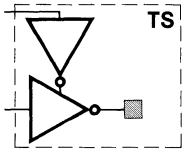
SCHEMATIC:



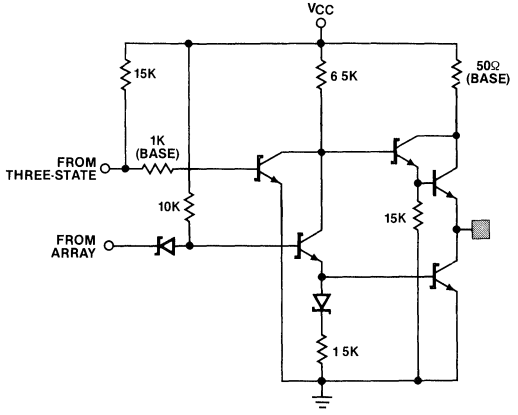
DESCRIPTION:

Low Power Schottky three-state output buffer.

SYMBOL & LOGIC:



SCHEMATIC:

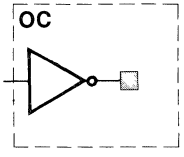


Preliminary

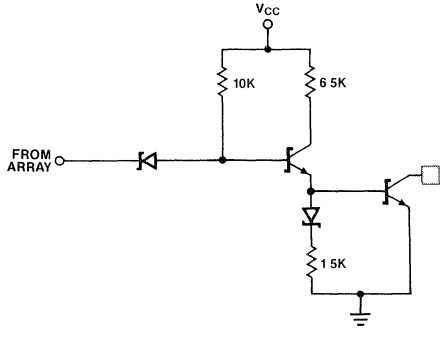
DESCRIPTION:

Low Power Schottky output buffer with open-collector output.

SYMBOL & LOGIC:



SCHEMATIC:

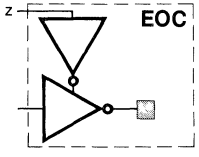


Preliminary

DESCRIPTION:

Low Power Schottky output buffer with open-collector output. Enabled from a three-state enable signal.

SYMBOL & LOGIC:



SCHEMATIC:

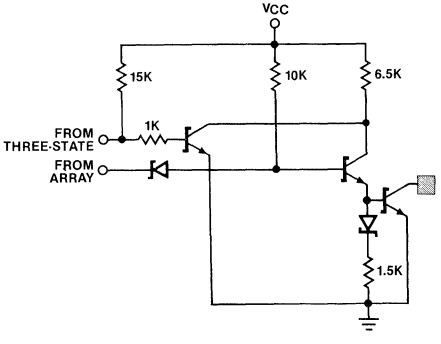


Figure 4. (continued) **Description and Symbolic, Logic, and Schematic Representation of Eight I/O Cells.**

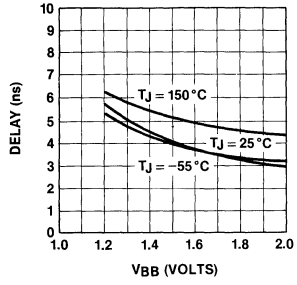
TYPICAL PERFORMANCE CHARACTERISTICS

Overall performance of the gate array is determined by the following parameters:

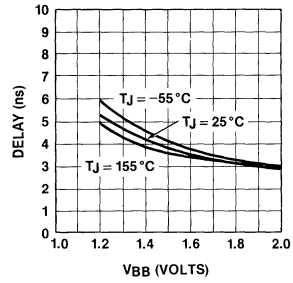
- Discrete gate delays
- Gate current (I_{BB}) and gate voltage (V_{BB})
- Junction Temperature (T_J)

Gate delays are subject to several variables, any one of which can affect the overall circuit performance. An analysis of these variables is shown in the accompanying graphs.

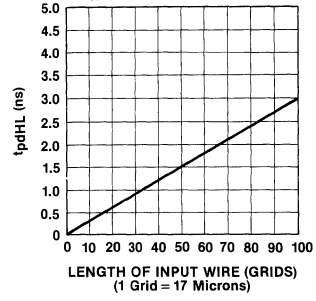
ISL GATE DELAY vs V_{BB}



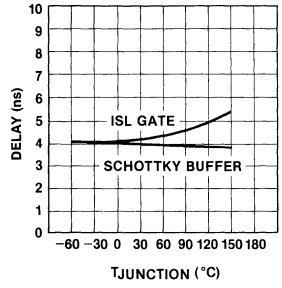
SCHOTTKY BUFFER GATE DELAY vs V_{BB}



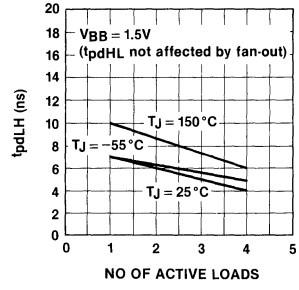
ADDED GATE DELAY vs INPUT WIRE LENGTH



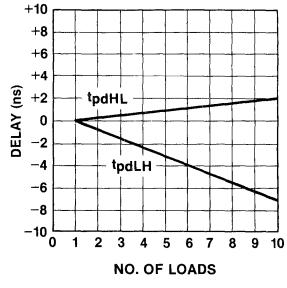
TYPICAL GATE DELAY vs JUNCTION TEMPERATURE



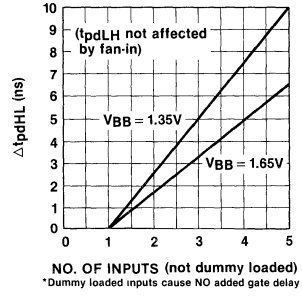
ISL GATE DELAY vs FAN-OUT



CHANGE IN GATE DELAY FOR INPUT BUFFERS AND SCHOTTKY BUFFERS vs FAN-OUT



ADDED GATE DELAY vs FAN-IN



POWER DISSIPATION

The maximum power dissipation for any given implementation of the 8A1260 gate array is given by the following equation.

Maximum Power (in mW) = 0.25 mW x number of ISL gates
plus, 0.25 mW x number of Schottky buffers used
plus, 8 mW x number of AP, OC, EOC, and TS
plus, 7 mW x number of IN, IN7, ID, and ID7
plus, 0.5V x load current (in mA) of output buffers

NOTE
Load Current = maximum I_{OL} for selected temperature range x the total number of output buffers and transceivers that can simutaneously be at low output state

Table 1. COMPARISON OF ISL WITH 74LS FUNCTIONS

LOGIC FUNCTION	PARAMETERS[3]	ISL[1]	74LS	LOGIC FUNCTION	PARAMETERS[3]	ISL[1]	74LS
NAND (7400)	Power (in mW) T_{ON} (in ns) T_{OFF} (in ns)	0.30 2.00 10.00	2.00 15.00 15.00	D FLIP-FLOP (7474) C Q	Power (in mW) T_{ON} (in ns) T_{OFF} (in ns)	1.50 28.00 28.00	20.00 40.00 40.00
AND (7408)	Power (in mW) T_{ON} (in ns) T_{OFF} (in ns)	0 0 2^2	11.00 20.00 15.00	D LATCH (7475) DATA Q	Power (in mW) T_{ON} (in ns) T_{OFF} (in ns)	1.20 5.00 12.00	30.00 17.00 17.00
EXCLUSIVE OR (7486)	Power (in mW) T_{ON} (in ns) T_{OFF} (in ns)	1.20 18.00 24.00	12.50 22.00 30.00	4-INPUT MUX (94153) DATA Q	Power (in mW) T_{ON} (in ns) T_{OFF} (in ns)	1.50 7.00 16.00	25.00 26.00 26.00
EXCLUSIVE NOR (74266)	Power (in mW) T_{ON} (in ns) T_{OFF} (in ns)	0.90 15.00 16.00	18.00 30.00 30.00	Notes 1 Power and delay times are given for 150°C max 2 T_{OFF} is 2 nanoseconds for each input, T_{OFF} can be reduced to 0 nanoseconds with a pullup call which uses 0 3 mW 3 LS power dissipation is based on $V_{CC} = I_{MAX}$			

AC AND DC ELECTRICAL CHARACTERISTICS

Conditions:

Commercial—
$V_{CC} = 5.0V (\pm 5\%)$
$V_{BB} = 1.5V (\pm 10\%)$
$T_A = 0°C$ to $70°C$

Military—
$V_{CC} = 5.0V (\pm 10\%)$
$V_{BB} = 1.5V (\pm 10\%)$
$T_A = -55°C$ to $125°C$

ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	RATING	UNIT	PARAMETER	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V	V_O	Voltage applied to open-collector output in off-state	−0.5 to +7.0	V
V_{BB}	ISL gate supply voltage	+7.0	V				
E_{IN}	Input voltage, continuous	−0.5 to +5.5	V	T_A	Ambient temperature, operating	−55 to +125	°C
I_{IN}	Input current, continuous	−30 to +1.0	mA	T_{STG}	Storage temperature	−65 to +150	°C

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ISL GATE (Internal)									
I_{BB}/G	Power supply current per gate				190			190	μA
ILF	Input load factor				1			1	Unit load
FO	Fan-out				4			4	Unit load
t_{pdAV}	Average gate propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = one (1) ISL gate or Schottky buffer Fan-out = one (1) ISL gate or Schottky buffer		4	6		4	6	ns
t_{pdHL}	High-to-low propagation delay	Delay is inferred from circuit simulation		1	2		1	2	ns
t_{pdLH}	Low-to-high propagation delay			7	10		7	10	ns

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SCHOTTKY BUFFER (Internal)									
I_{BB}/G	Power supply current per gate				190			190	μA
ILF	Input load factor				1			1	Unit load
FO	Fan-out				10			10	Unit load
t_{pdAV}	Average gate propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = one (1) ISL gate or Schottky buffer Fan-out = one (1) ISL gate or Schottky buffer		4	6		4	6	ns
t_{pdHL}	High-to-low propagation delay	Delay is inferred from circuit simulation		1	2		1	2	ns
t_{pdLH}	Low-to-high propagation delay			7	10		7	10	ns
INPUT BUFFERS: IN, IN7, ID, and ID7									
I_{CC}	Power supply current	V_{IN} = 3V(IN from Array = H)			1.30			1.40	mA
VTH	Input threshold voltage		0.80		2.0	0.80		2.0	V
VCD	Input clamp diode voltage	I_{IN} = −18mA			− 1.5			−1.5	V
I_{IL}	Input low current	V_{IN} = 0.4V			− 20			−20	μA
I_{IH}	Input high current	V_{IN} = 2.7V			20			20	μA
I_I	Max input high current	V_{IN} = 5.5V, V_{CC} = Max			100			100	μA
FO	INB & IOD "to array" outputs EOCD & IOD "to three-state" outputs				10 16			10 16	Unit load Unit load
t_{pdLH}	Propagation delay, low-to-high F.O. = one (1) ISL load	(See Fig. 5a)		5	8		5	8	ns
t_{pdHL}	Propagation delay, high-to-low F.O. = one (1) ISL load			2	4		2	4	ns
t_{pdLH}	Propagation delay, low-to-high F.O. = ten (10) ISL loads			3	4		3	4	ns
t_{pdHL}	Propagation delay, high-to-low F.O. = ten (10) ISL loads			4	5		4	5	ns
OUTPUT BUFFER: AP (Active Pullup)									
I_{CC}	Power supply current	From array = high			1.38			1.50	mA
ILF	Input load factor		3			3			Unit loads
V_{OL}	Output low voltage	I_{OL} = 8mA I_{OL} = 4mA			500			 400	mV mV
V_{OH}	Output high voltage	I_{OH} = −400μA	2.7			2.5			V
I_{OS}	Output short circut current	V_{OUT} = OV	− 15		− 100	−15		−100	mA

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT BUFFER: AP (Active Pullup) (continued)									
t_{pdLH}	Propagation delay, low-to-high output	(See Fig. 5b)		4	8		4	8	ns
t_{pdHL}	Propagation delay, high-to-low output			4	8		4	8	ns
OPEN COLLECTOR, OUTPUT BUFFERS: OC AND EOC (Preliminary)									
I_{CC}	OC power supply current	From array = high			1.38			1.50	mA
	EOC power supply current	From array = low, From T.S. = high			1.98			2.10	mA
ILF	Input load factor "from array"		3			3			Unit load
	Input load factor "from T.S."		3			3			Unit load
VOL	Output low voltage	I_{OL} = 8mA			500				mV
		I_{OL} = 4mA						400	mV
IOH	Output high current	V_{OUT} = 5.5V			20			20	μA
t_{pdLH}	Propagation delay, low-to-high output	(See Fig. 5c)		9	TBD		9	TBD	ns
t_{pdHL}	Propagation delay, high-to-low output			8	TBD		8	TBD	ns
THREE-STATE OUTPUT BUFFERS: TS									
I_{CC}	TS power supply current	From T.S. = high From array = low			1.98			2.10	mA
ILF	Input load factor, either input		3			3			Unit load
V_{OL}	Output low voltage	I_{OL} = 8mA			500				mV
		I_{OL} = 4mA						400	mV
V_{OH}	Output high voltage	I_{OH} = −400μA	2.7			2 5			V
I_{OS}	Output short circuit current	V_{OUT} = OV	− 15		− 100	−15		−100	mA
I_{OLZ}	Three-state off current, output low	V_{OUT} = 0.4V			− 20			−20	μA
I_{OHZ}	Three-state off current,	V_{OUT} = 2.4V			20			20	μA
t_{pdLH}	Propagation delay, low-to-high output (Note)	R_L = 2K		4	9		4	9	ns
t_{pdHL}	Propagation delay, high-to-low output (Note)	C_L = 15pf		6	10		6	10	ns
t_{pdZL}	Propagation delay, HI-Z to low output	(See Fig. 5d)		11	14		11	14	ns
t_{pdZH}	Propagation delay, HI-Z to high output			10	13		10	13	ns
t_{pdLZ}	Propagation delay, LOW to HI-Z output			6	12		6	12	ns
t_{pdHZ}	Propagation delay, high to HI-Z output			7	7		7	7	ns

NOTE Guaranteed value is $t_{ps(Ave)}$

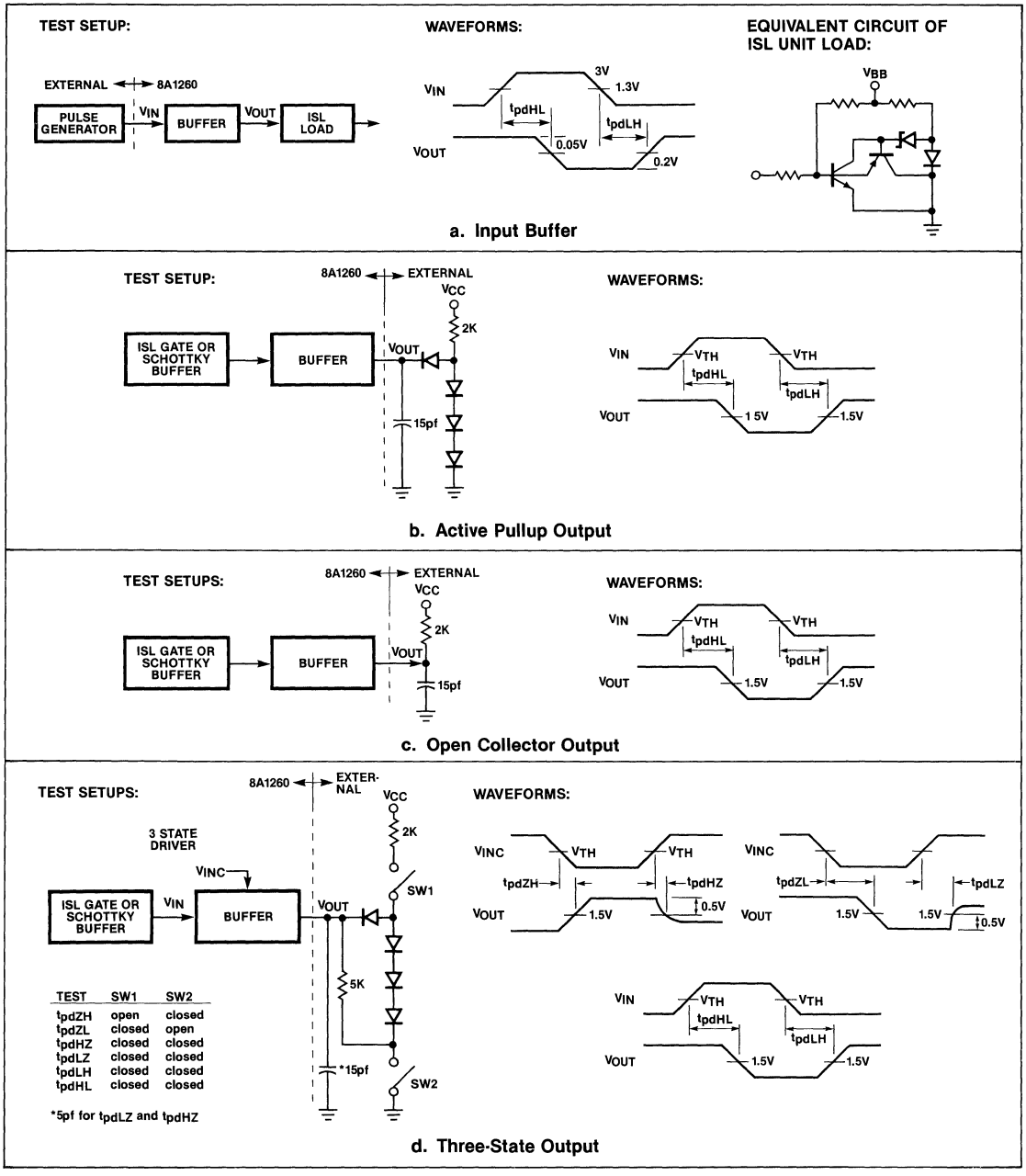


Figure 5. Test Circuits

ISL GATE ARRAY 8A1542

FEATURES

- **Customer programmable LSI**
- **1408 ISL (NAND) gates**
- **Two-layer metal interconnection**
- **64 Schottky buffers**
- **42 I/O buffers**
- **LSTTL compatible**
- **Standard PNP inputs**
- **8mA output current sink**
- **−55°C to +125°C ambient temperature**
- **4ns gate speed (typical)**
- **Speed-power product—0.7 picojoules**
- **28, 40, or 44-pin package**

PRODUCT DESCRIPTION

The 8A1542 Gate Array (Figure 1) is an uncommitted array of ISL gates (Figure 2), Schottky buffers (Figure 3) and LSTTL-compatible I/O cells (Figure 4). Thus, up to 1400 gates can be custom interconnected to provide the advantages of both Large Scale Integration (LSI) and proprietary design. The 8A1542 array is based on a technological subset of LSI called ISL (Integrated Schottky Logic). ISL combines the best features of low-power Schottky and I^2L Bipolar technologies.

Designing with the 8A1542 is easy and fast, requiring no more than conventional logic design, logic simulation, and custom coding of metal interconnections among preprocessed logic gates on the array—refer to Table 1 for a comparison of ISL and 74LS logic functions. The design techniques and the implementation processes are analogous to the design of a Printed Circuit Board.

Logic functions are defined by the user and are implemented by interconnecting 1408 ISL NAND gates, using two layers of metal routing. Sixty-four Schottky buffers are provided to drive multiload internal clock or enable signals. For external interface, up to 42 LSTTL I/O buffers can be specified. As shown in Figure 4, each I/O can be configured to implement any one of 11 different functions: inputs, input/output, totem-pole, open collector, and three-state.

ORDERING INFORMATION

Contact Local Sales Representative

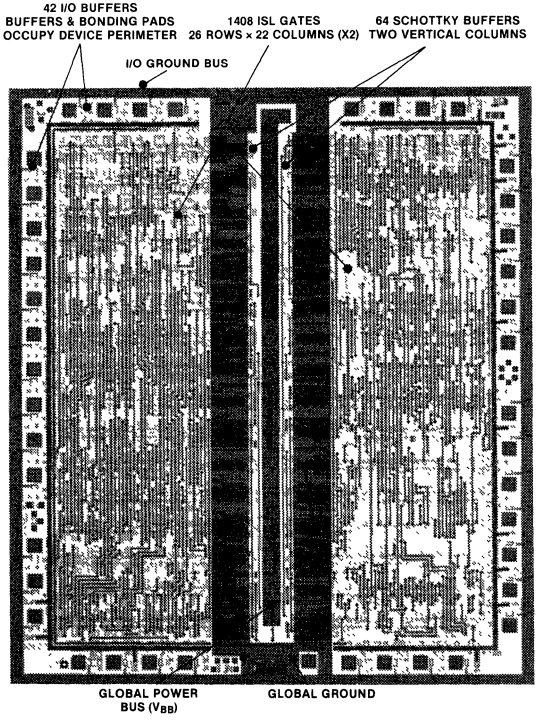


Figure 1. Internal Configuration of 8A1542 ISL Gate Array

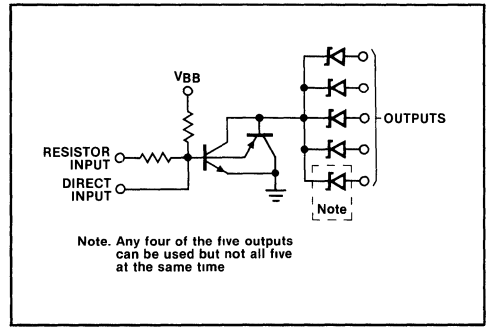


Figure 2. ISL Gate—Schematic Diagram

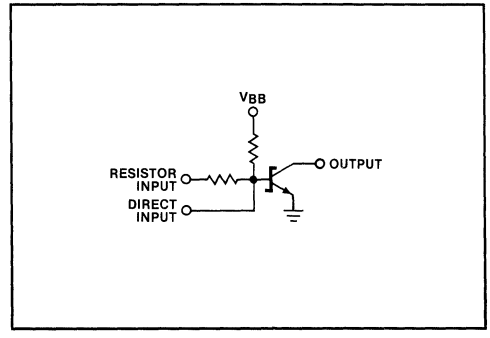


Figure 3. Schottky Buffer—Schematic Diagram

INPUT/OUTPUT CELLS

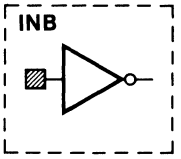
All signals within the array interface to external pins via I/O buffers located around the device perimeter. A description plus the symbolic logic, and schematic representation for each I/O cell are shown in Figure 4.

INPUT BUFFERS

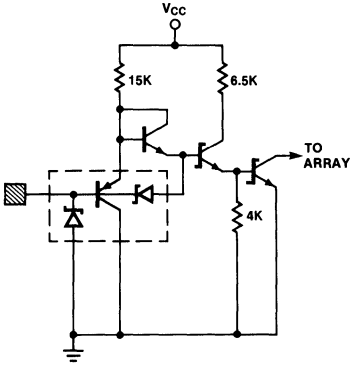
DESCRIPTION:

Low power Schottky input buffer with low current PNP input transistor.

SYMBOL & LOGIC:



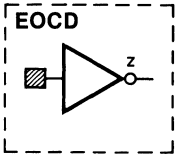
SCHEMATIC:



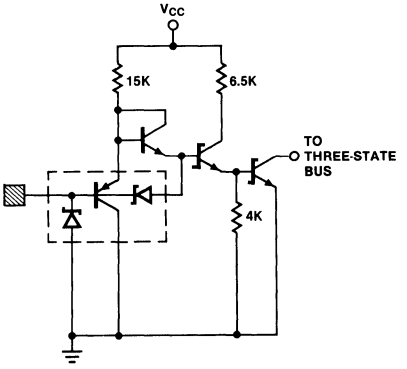
DESCRIPTION:

Input cell with output driver for driving the three-state enable of three-state output cells.

SYMBOL & LOGIC:



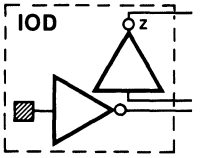
SCHEMATIC:



DESCRIPTION:

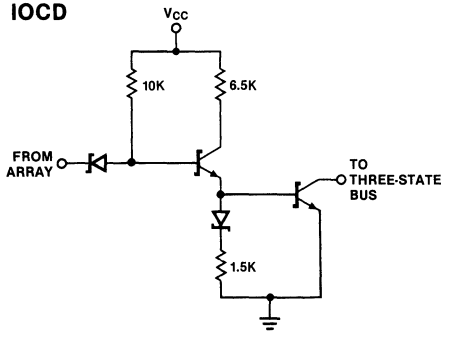
Input with three-state driver. This is a back-to-back configuration of an input buffer and and internal three-state driver (INB + IOCD).

SYMBOL & LOGIC:



SCHEMATICS:

IOCD



INB

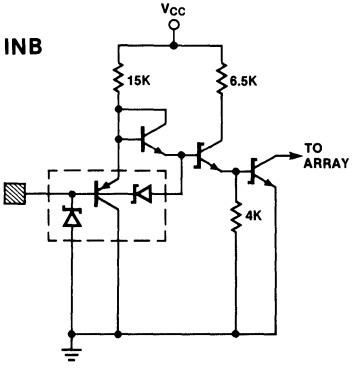


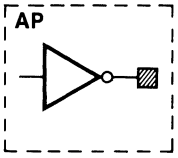
Figure 4. Description and Symbolic, Logic, and Schematic Representation of Eleven I/O Cells

OUTPUT BUFFERS

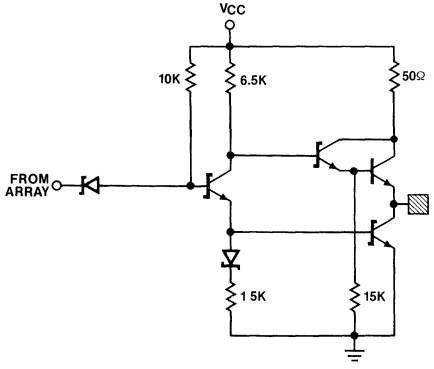
DESCRIPTION:

Standard low power Schottky output buffer with totem pole active pull-up.

SYMBOL & LOGIC:



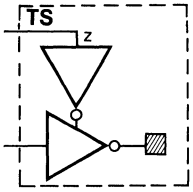
SCHEMATIC:



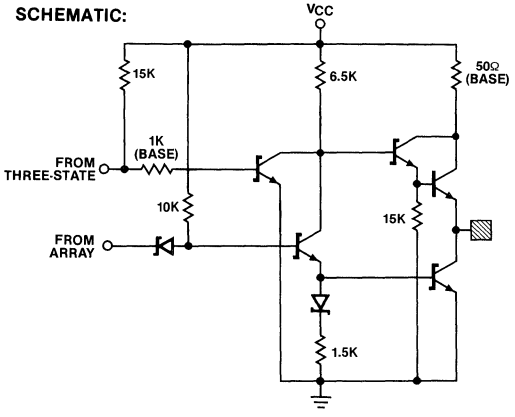
DESCRIPTION:

Standard three-state low power Schottky output.

SYMBOL & LOGIC:



SCHEMATIC:

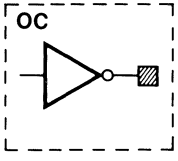


Preliminary

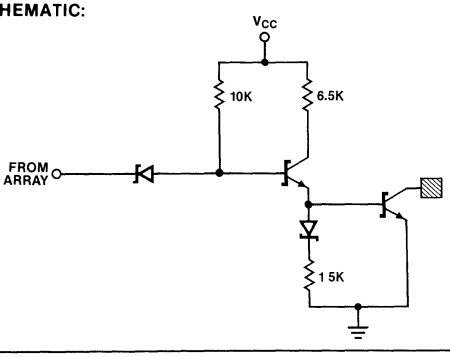
DESCRIPTION:

Low power Schottky output buffer with open-collector output.

SYMBOL & LOGIC:



SCHEMATIC:

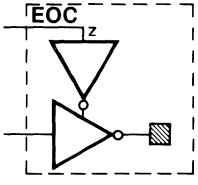


Preliminary

DESCRIPTION:

Low power Schottky output buffer with open-collector output. Enabled from a three-state enable signal.

SYMBOL & LOGIC:



SCHEMATIC:

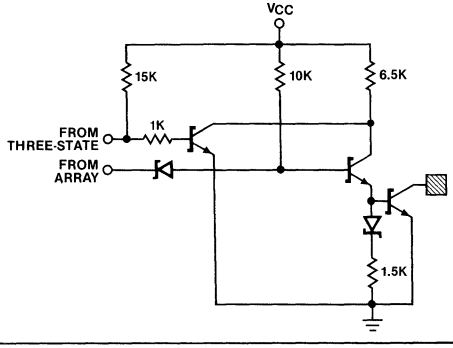


Figure 4. (continued) Description and Symbolic, Logic, and Schematic Representation of Eleven I/O Cells

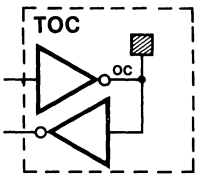
TRANSCEIVERS

Preliminary

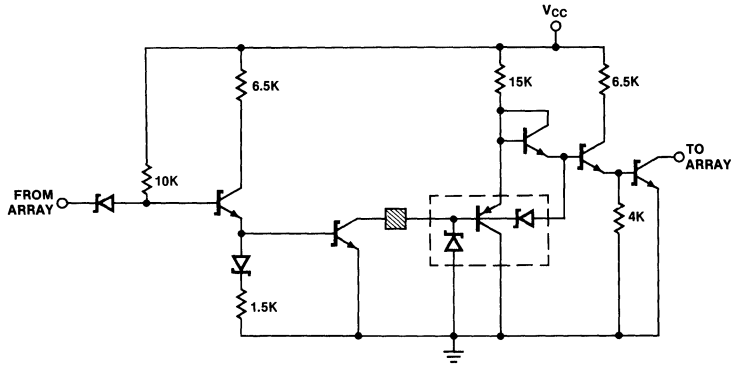
DESCRIPTION:

Open-collector transceiver. This is a back-to-back configuration of an input buffer and an open-collector output buffer (INB + OC).

SYMBOL & LOGIC:



SCHEMATIC:

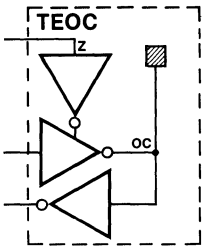


Preliminary

DESCRIPTION:

Enabled open-collector transceiver. This is a back-to-back configuration of an input buffer and an enabled open-collector output buffer (INB + EOC).

SYMBOL & LOGIC:



SCHEMATIC:

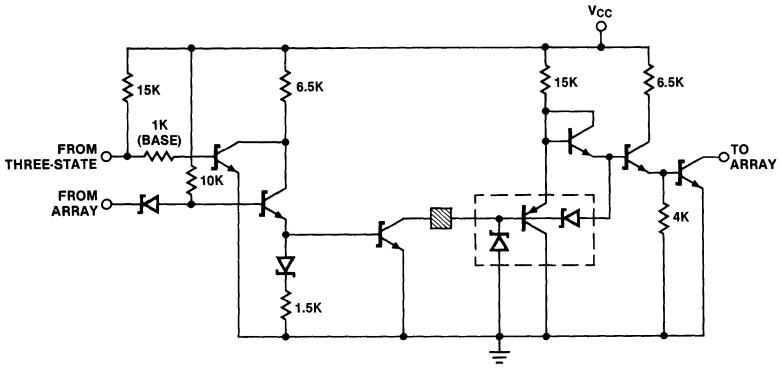


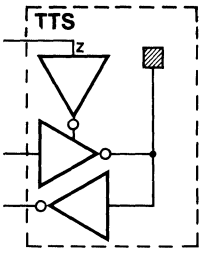
Figure 4. (continued) Description and Symbolic, Logic, and Schematic Representation of Eleven I/O Cells

TRANSCEIVERS (Continued)

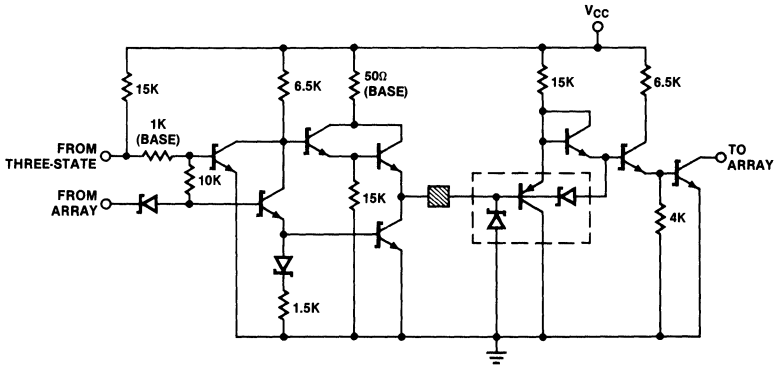
DESCRIPTION:

Three-state transceiver. This is a back-to-back configuration of an input buffer and a three-state output in one I/O cell (INB + TS).

SYMBOL & LOGIC:



SCHEMATIC:

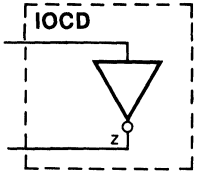


OTHER

DESCRIPTION:

Same as EOCD, except input is designed to interface with ISL gates. This cell is used internally and does not interface to an external pin.

SYMBOL & LOGIC:



SCHEMATIC:

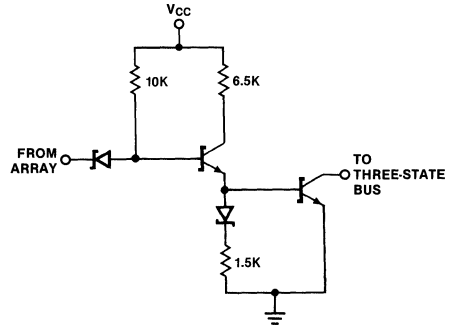


Figure 4. (continued) Description and Symbolic, Logic, and Schematic Representation of Eleven I/O Cells

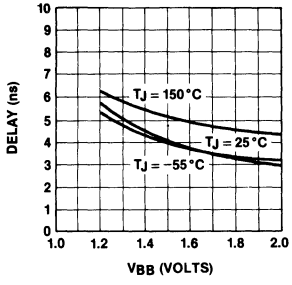
TYPICAL PERFORMANCE CHARACTERISTICS

Overall performance of the gate array is determined by the following parameters:

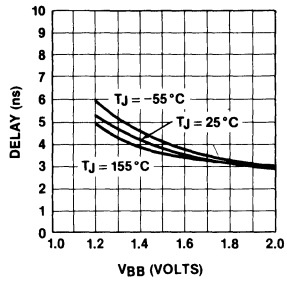
- Discrete gate delays
- Gate current (I_{BB}) and gate voltage (V_{BB})
- Junction Temperature (T_J)

Gate delays are subject to several variables, any one of which can affect the overall circuit performance. An analysis of these variables is shown in the accompanying graphs.

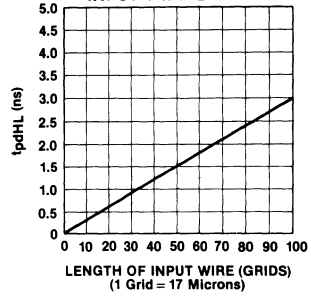
ISL GATE DELAY vs V_{BB}



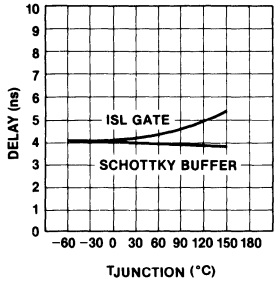
SCHOTTKY BUFFER GATE DELAY vs V_{BB}



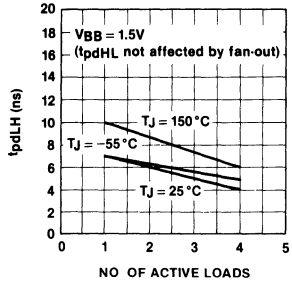
ADDED GATE DELAY vs INPUT WIRE LENGTH



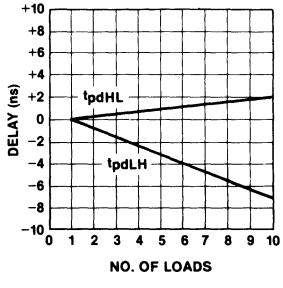
TYPICAL GATE DELAY vs JUNCTION TEMPERATURE



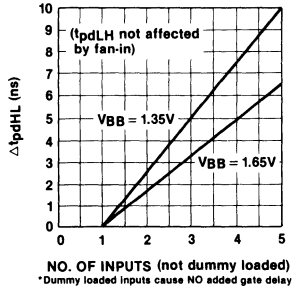
ISL GATE DELAY vs FAN-OUT



CHANGE IN GATE DELAY FOR INPUT BUFFERS AND SCHOTTKY BUFFERS vs FAN-OUT



ADDED GATE DELAY vs FAN-IN



POWER DISSIPATION

For the purpose of package selection, the maximum power dissipation for any given implementation of the 8A1542 gate array is given by the following equation.

Maximum Power (in mW) = 0.25 mW x number of ISL
plus, 0.25 mW x number of Schottky buffers used
plus, 12 mW x number of TTS, TOC, and TEOC buffers
plus, 8 mW x number of AP, OC, EOC, TS and IOD buffers
plus, 5 mW x number of EOCD, INB, and IOCD buffers
plus, 0.5V x load current (in mA) of output buffers

NOTE:
Load Current = maximum I_{OL} for selected temperature range x the total number of output buffers and transceivers that can simultaneously be at a low output state.

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Table 1. COMPARISON OF ISL WITH 74LS FUNCTIONS

LOGIC FUNCTION	PARAMETERS[3]	ISL[1]	74LS	LOGIC FUNCTION	PARAMETERS[3]	ISL[1]	74LS
NAND (7400)	Power (in mW)	0.30	2.00	D FLIP-FLOP (7474)	Power (in mW)	1.50	20.00
	T_{ON} (in ns)	2.00	15.00	C→$\overline{Q}$	T_{ON} (in ns)	28.00	40.00
	T_{OFF} (in ns)	10.00	15.00		T_{OFF} (in ns)	28.00	40.00
AND (7408)	Power (in mW)	0	11.00	D LATCH (7475)	Power (in mW)	1.20	30.00
	T_{ON} (in ns)	0	20.00	DATA→$\overline{Q}$	T_{ON} (in ns)	5.00	17.00
	T_{OFF} (in ns)	2[2]	15.00		T_{OFF} (in ns)	12.00	17.00
EXCLUSIVE OR (7486)	Power (in mW)	1.20	12 50	4-INPUT MUX (74153)	Power (in mW)	1.50	25.00
	T_{ON} (in ns)	18.00	22.00	DATA→$\overline{Q}$	T_{ON} (in ns)	7 00	26.00
	T_{OFF} (in ns)	24.00	30 00		T_{OFF} (in ns)	16.00	26.00
EXCLUSIVE NOR (74266)	Power (in mW)	0.90	18 00				
	T_{ON} (in ns)	15 00	30 00				
	T_{OFF} (in ns)	16 00	30 00				

Notes
1. Power and delay times are given for 150°C MAX
2. T_{OFF} is 2ns for each input, T_{OFF} can be reduced to 0ns with a pullup cell which uses 0.3 mW
3. LS power dissipation is based on $V_{CC} \times I_{MAX}$

AC AND DC ELECTRICAL CHARACTERISTICS

Conditions: Commercial—
$V_{CC} = 5.0V (\pm 5\%)$
$V_{BB} = 1.5V (\pm 10\%)$
T_A[1] = 0°C to 70°C

Military—
$V_{CC} = 5.0V (\pm 10\%)$
$V_{BB} = 1.5V (\pm 10\%)$
T_A[1] = −55°C to 125°C

ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	RATING	UNIT	PARAMETER	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage	+7 0	V	V_O	Voltage applied to open-collector output in off-state	−0 5 to +7.0	V
V_{BB}	ISL gate supply voltage	+7 0	V	T_A	Ambient temperature, operating	−55 to +125	°C
E_{IN}	Input voltage, continuous	−0 5 to +5.5	V				
I_{IN}	Input current, continuous	−30 to +1.0	mA	T_{STG}	Storage temperature	−65 to +150	°C

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ISL GATE (Internal)									
I_{BB}/G	Power supply current per gate				190			190	μA
ILF	Input load factor				1			1	Unit load
FO	Fanout				4			4	Unit load
t_{pdAV}	Average gate propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = one (1) ISL gate or Schottky buffer Fan-out = one (1) ISL gate or Schottky buffer		4	6		4	6	ns
$t_{pdHL}2$	High-to-low propagation delay	Delay is inferred from circuit simulation		1	2		1	2	ns
$t_{pdLH}2$	Low-to-high propagation delay			7	10		7	10	ns
SCHOTTKY BUFFER (Internal)									
I_{BB}/G	Power supply current per gate				190			190	μA
ILF	Input load factor				1			1	Unit load
FO	Fanout				10			10	Unit load
t_{pdAV}	Average gate propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = one (1) ISL gate or Schottky buffer Fan-out = one (1) ISL gate or Schottky buffer		4	6		4	6	ns
$t_{pdHL}2$	High-to-low propagation delay	Delay is inferred from circuit simulation		1	2		1	2	ns
$t_{pdLH}2$	Low-to-high propagation delay			7	10		7	10	ns

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INTERNAL BUFFERS: IOD, IOCD (Internal)									
I_{CC}	IOCD power supply current	From array = high			1.38			1.50	mA
	IOD power supply current	V_{IN} = 3V, from array = high			2 53			2.75	mA
ILF	Input load factor		3			3			Unit load
FO	Fanout								
	To T.S. (I/O only)	(drives 3-state inputs only)			16			16	Inputs
	To Array (I/O only)	(drives internal gates)			10			10	Unit loads
t_{pdAV}	Average propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan in = one (1) ISL gate or Schottky buffer Fan out = one (1) from 3-state input of an output buffer		10	14		10	14	ns
INPUT BUFFERS: INB, EOCD, TEOC[3] (to array), IOD (to array), TOC (to array), TTS[3] (to array)									
I_{CC}	TOC, supply current	V_{IN} = 3V, from Array = L			1.76			1.90	mA
	INB, EOCD, supply current	V_{IN} = 3V			1.15			1.25	mA
	IOD, supply current	V_{IN} = 3V, from Array = H			2.53			2.75	mA
	TEOC, supply current	V_{IN} = 3V, from TS = H, from Array = L			3.11			3.35	mA
	TTS, supply current	From Array = L, from TS = H V_{IN} = 3V			3 11			3.35	mA
V_{TH}	Input threshold voltage		0.8		2.0	0.80		2 0	V
V_{CD}	Input clamp diode voltage	I_{IN} = – 18mA			– 1 5			– 1.5	V
I_{IL}	Input low current	V_{IN} = 0.4V			– 20			– 20	µA
I_{IH}	Input high current	V_{IN} = 2.7V			20			20	µA
I_I	Max input high current	V_{IN} = 5 5V, V_{CC} = Max			100			100	µA
FO	INB & IOD "to array" outputs				10			10	Unit load
	EOCD & IOD "to 3-state" outputs				16			16	Inputs
t_{pdLH}	Propagation delay, low-to-high F O. = one (1) ISL load	See Figure 5a		5	8		5	8	ns
t_{pdHL}	Propagation delay, high-to-low F.O. = one (1) ISL load			2	4		2	4	ns
t_{pdLH}	Propagation delay, low-to-high F.O. = ten (10) ISL loads			3	4		3	4	ns
t_{pdHL}	Propagation delay, high-to-low F.O. = ten (10) ISL loads			4	5		4	5	ns
OUTPUT BUFFER: AP (Active Pullup)									
I_{CC}	Power supply current	From array = high			1.38			1.50	mA
ILF	Input load factor		3			3			Unit loads
V_{OL}	Output low voltage	I_{OL} = 8mA			500				mV
		I_{OL} = 4mA						400	mV
V_{OH}	Output high voltage	I_{OH} = – 400µA	2.7			2 5			V
I_{OS}	Output short circuit current	V_{OUT} = 0V	– 15		– 100	– 15		– 100	mA
t_{pdLH}	Propagation delay, low to high output	See Figure 5b		4	8		4	8	ns
t_{pdHL}	Propagation delay, high to low output			4	8		4	8	ns

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PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			Min	Typ	Max	Min	Typ	Max	
OPEN COLLECTOR, OUTPUT BUFFERS: OC, TOC (from array), EOC, TEOC (from array)									**Preliminary**
I_{CC}	OC power supply current	From array = high			1.38			1.50	mA
	TOC power supply current	From array = low			1.76			1.90	mA
	EOC power supply current	From array = low, from T.S. = high			1.96			2.10	mA
	TEOC power supply current	From array = low, from T.S. = high			3.11			3.35	mA
ILF	Input load factor "from array"		3			3			Unit load
	Input load factor "from T.S."		3			3			Unit load
V_{OL}	Output low voltage	I_{OL} = 8mA I_{OL} = 4mA			500			 400	mV mV
I_{OH}	Output high current	V_{OUT} = 5.5V			20			20	μA
t_{pdLH}	Propagation delay low to high output	See Figure 5c		9	TBD		9	TBD	ns
t_{pdHL}	Propagation delay high to low output			8	TBD		8	TBD	ns
THREE-STATE OUTPUT BUFFERS: TS, TTS (from array)									
I_{CC}	TS power supply current	From T.S. = high From array = low			1.96			2.10	mA
	TTS power supply current	From array = low V_{IN} = 3V, from T.S. = high			3.11			3.35	mA
ILF	Input load factor, either input		3			3			Unit load
V_{OL}	Output low voltage	I_{OL} = 8mA I_{OL} = 4mA			500			 400	mV mV
V_{OH}	Output high voltage	I_{OH} = −400μA	2.7			2.5			V
I_{OS}	Output short circuit current	V_{OUT} = 0V	−15		−100	−15		−100	mA
I_{OZL}	Three-state off current, output low	V_{OUT} = 0.4V			−20			−20	μA
I_{OZH}	Three-state off current, output high	V_{OUT} = 2.4V			20			20	μA
t_{pdLH}	Propagation delay, low to high output	See Figure 5d		4	9		4	9	ns
t_{pdHL}	Propagation delay, high to low output			6	10		6	10	ns
t_{pdZL}	Propagation delay, HI Z to low output			11	14		11	14	ns
t_{pdZH}	Propagation delay, HI Z to high output			10	13		10	13	ns
t_{pdLZ}	Propagation delay, low to HI Z output			6	12		6	12	ns
t_{pdHZ}	Propagation delay, high to HI Z output			7	7		7	7	ns

NOTES.
1 Maximum power dissipation limit of circuit is determined by package selection
2 Guaranteed value is t_{pdAV}.
3 For all input parameters on TEOC and TTS, the "from Three-State" input should be high.

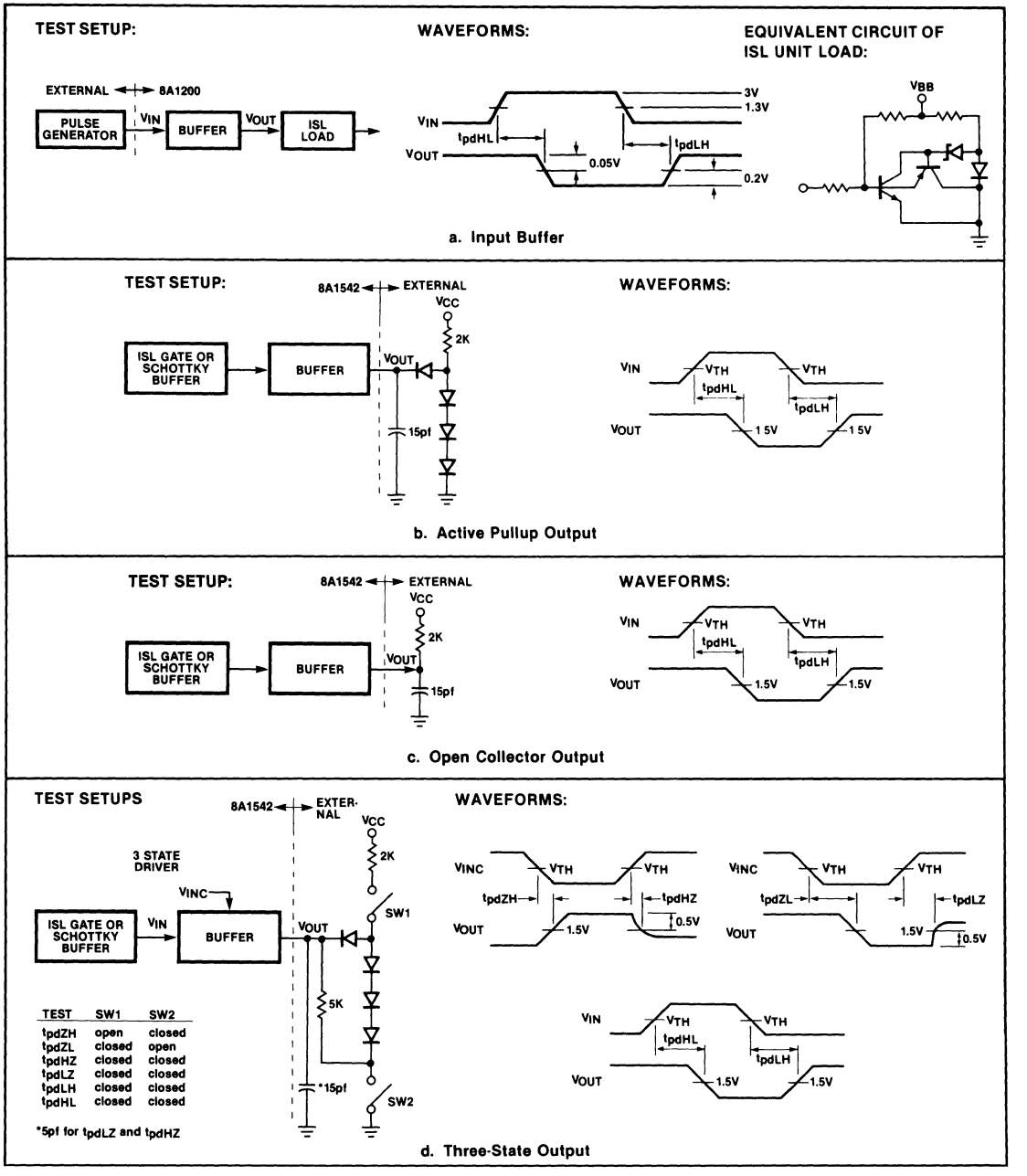

Figure 5. Test Circuits

ISL GATE ARRAY 8A1664

FEATURES

- **Customer programmable LSI**
- **1560 ISL (NAND) gates**
- **Two-layer metal interconnection**
- **60 Schottky buffers**
- **64 I/O buffers**
- **LS TTL compatible**
- **Standard PNP inputs**
- **8-, or 24-milliamperes output current sink**
- **−55°C to +125°C ambient temperature**
- **4-nanosecond gate speed (typical)**
- **Speed-power product — 0.7 picojoules**
- **68 pin package**

PRODUCT DESCRIPTION

The 8A1664 Gate Array (Figure 1) is an uncommitted array of ISL gates (Figure 2), Schottky Buffers (Figure 3), and the LSTTL compatible I/O cells. Thus, up to 1600 gates can be custom interconnected to provide the advantages of both Large Scale Integration (LSI) and proprietary design. The 8A1664 array is based on a technological subset of LSI called ISL (Integrated Schottky Logic). ISL combines the features of Schottky and the density of I^2L Bipolar technologies.

Designing with the 8A1664 is easy and fast, requiring no more than conventional logic design, logic simulation, and custom coding of metal interconnections among preprocessed logic gates on the array. The design techniques and the implementation processes are analogous to the design of a Printed Circuit Board.

Logic functions are defined by the user and are implemented by interconnecting 1560 ISL NAND gates, using two layers of metal routing. Sixty Schottky buffers are provided to drive multi-load internal clock or enable signals. For external interface, up to 64 LS TTL I/O buffers can be specified. Each 8-milliampere I/O site can be configured as 1-of-6 input/internal buffers or as 1-of-8 output buffers; each 24-milliampere I/O site can also be configured as 1-of-6 input/internal buffers but the output buffer configuration can be 1-of-12. For a transceiver, either I/O site can be connected in combinations of one input and one output buffer.

ORDERING INFORMATION

Contact Local Sales Representative

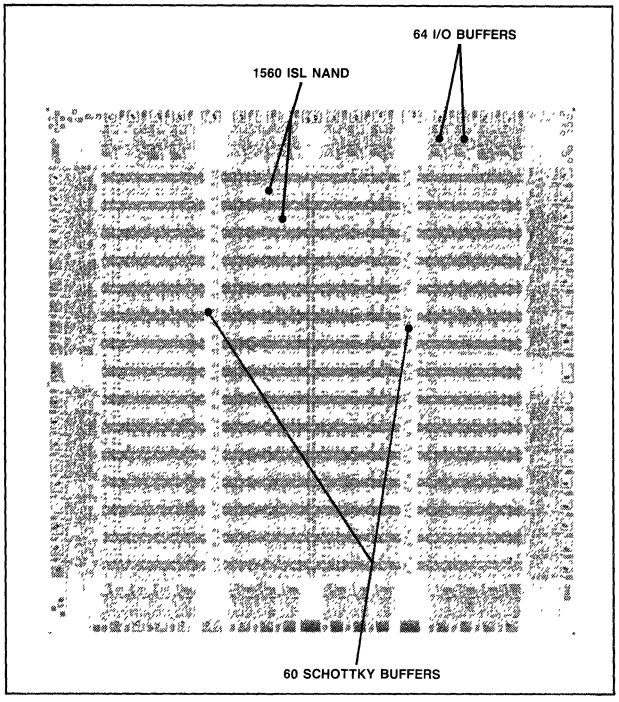

Figure 1. Internal Configuration of 8A1664

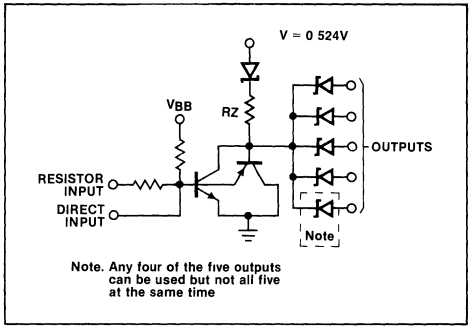

Figure 2. ISL Gate — Schematic Diagram

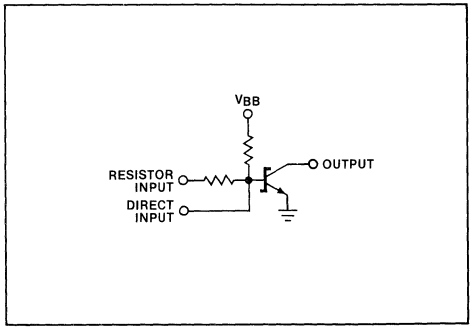

Figure 3. Schottky Buffer — Schematic Diagram

FEATURES

- **Customer programmable LSI**
- **1740 ISL (NAND) gates**
- **Two-layer metal interconnection**
- **60 Schottky buffers**
- **72 I/O buffers**
- **LS TTL compatible**
- **Standard PNP inputs**
- **8-, or 24-milliamperes output current sink**
- **−55°C to +125°C ambient temperature**
- **4-nanosecond gate speed (typical)**
- **Speed-power product — 0.7 picojoules**
- **40-, 44-, 50- or 68-pin packages**

PRODUCT DESCRIPTION

The 8A1864 Gate Array (Figure 1) is an uncommitted array of ISL gates (Figure 2). Schottky buffers (Figure 3) and LSTTL-compatible I/O cells. Thus, up to 1740 gates and 60 buffers can be interconnected to provide the advantages of both Large Scale Integration (LSI) and proprietary design. The 8A1864 array is based on a technological subset of LSI called ISL (integrated Schottky Logic). ISL combines the features of Schottky and the density of I^2L Bipolar technologies.

Designing with the 8A1864 is easy and fast, requiring no more than conventional logic design, logic simulation, and coding of metal interconnections between preprocessed logic gates on the array. The design techniques and the implementation processes are analogous to the design of a Printed Circuit Board.

Logic functions are defined by the user and are implemented by interconnecting up to 1740 ISL NAND gates, and up to 60 buffers, using two layers of metal routing. Sixty Schottky buffers are provided to drive multi-load internal clock or enable signals. For external interface, up to 64 LS TTL I/O buffers can be specified. Each 8-milliampere I/O site can be configured as 1-of-6 input/internal buffers or as 1-of-8 output buffers; each 24-milliampere I/O site can also be configured as 1-of-6 input/internal buffers but the output buffer configuration can be 1-of-12. For a transceiver, either I/O site can be connected in combinations of one input and one output buffer.

ORDERING INFORMATION

Contact Local Sales Representative

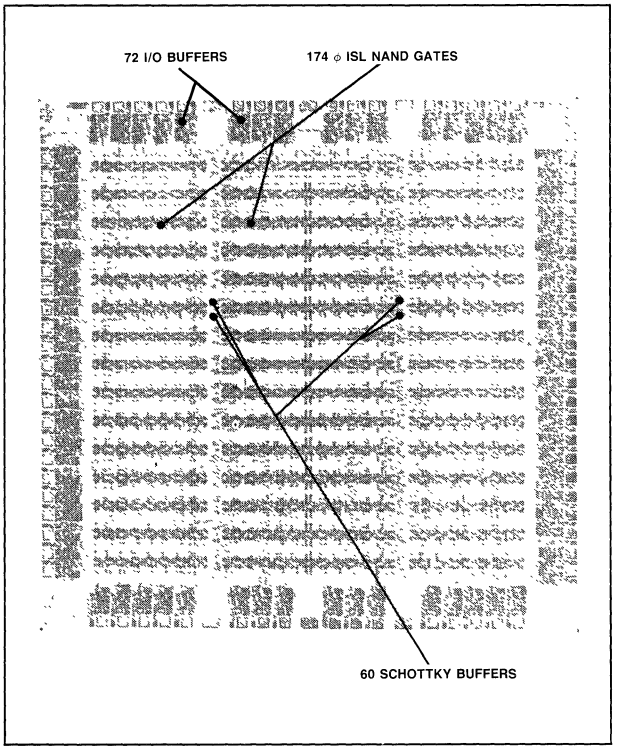

Figure 1. Internal Configuration of 8A1864

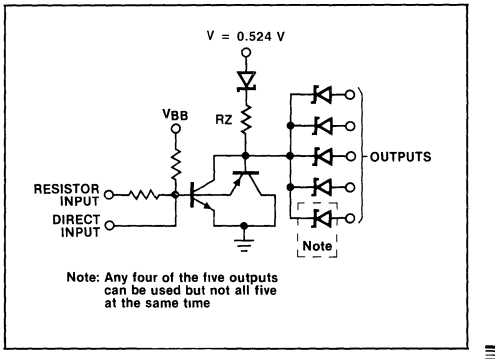

Figure 2. ISL Gate — Schematic Diagram

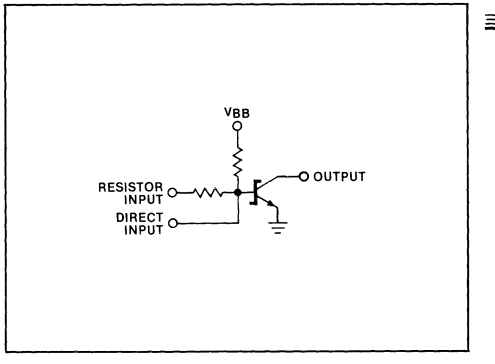

Figure 3. Schottky Buffer — Schematic Diagram

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ISL GATE ARRAY 8A2176

FEATURES

- **Customer programmable LSI**
- **2016 ISL (NAND) gates**
- **72 Schottky buffers**
- **76 I/O buffers**
- **LS TTL compatible**
- **Standard PNP inputs**
- **8 mA and 24 mA output current sink**
- **−55°C to +125°C ambient temperature**
- **4 ns gate speed (typical)**
- **Speed power product −0.7 picojoules**
- **28, 40, 68, or 84 pin package**

PRODUCT DESCRIPTION

The 8A2176 Gate Array (Figure 1) is an uncommitted array of ISL gates (Figure 2), Schottky buffers (Figure 3) and LSTTL-compatible I/O cells. Thus, up to 2016 gates can be custom interconnected to provide the advantages of both Large Scale Integration (LSI) and proprietary design. The 8A2176 76 array is based on a technological subset of LSI called ISL (Integrated Schottky Logic). ISL combines the features of Schottky and the density of I^2L Bipolar technologies.

Designing with the 8A2176 is easy and fast, requiring no more than conventional logic design, logic simulation, and custom coding of metal interconnections among preprocessed logic gates on the array. The design techniques and the implementation processes are analogous to the design of a Printed Circuit Board.

Logic functions are defined by the user and are implemented by interconnecting 2016 ISL NAND gates, using two layers of metal routing. Seventy-two Schottky buffers are provided to drive multi-load internal clock or enable signals. For external interface, up to 76 LSTTL I/O buffers can be specified.

Each 8-milliampere I/O site can be configured as 1-of-6 input/internal buffers or as 1-of-8 output buffers; each 24-milliampere I/O site can also be configured as 1-of-6 input/internal buffers but the output buffer configuration can be 1-of-12. For a transceiver, either I/O site can be connected in combinations of one input and one output buffer.

ORDERING INFORMATION

Contact Local Sales Representative

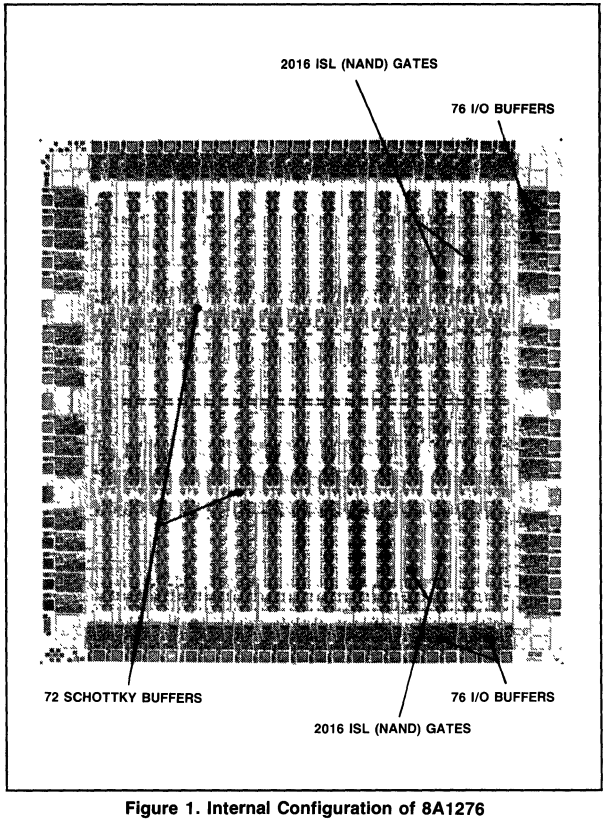


Figure 1. Internal Configuration of 8A1276

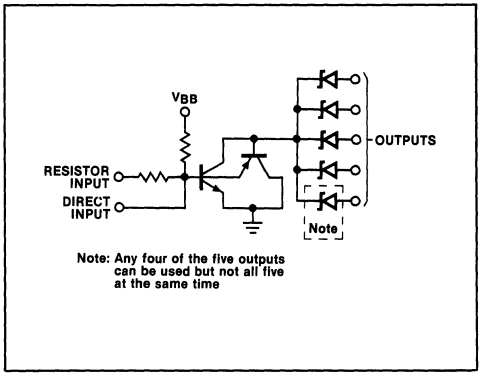


Figure 2. ISL Gate — Schematic Diagram

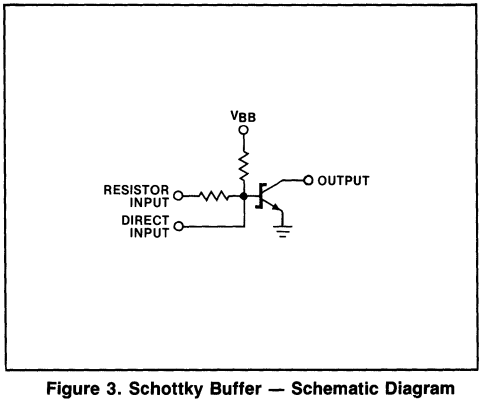


Figure 3. Schottky Buffer — Schematic Diagram

8A1200 EVALUATION CIRCUIT — CG1001

FEATURES

REPRESENTATIVE LOGIC FUNCTIONS:

- **8 to 1 Multiplexer (Figure 3)—similar to 74152.**
- **4-Bit Adder (Figure 4)—similar to 7483.**
- **4-Bit Universal Shift Register (Figure 5)—similar to 74194.**

SPECIAL TEST CIRCUITS.

- **D-flip flop wired as a toggle flip flop**
- **Demonstration of fanout effects on ISL gates**
- **Test of fanin and pattern sensitivity effects on ISL gates**
- **Ring oscillators which show the basic gate delays of ISL gates and Schottky buffers under various layout and logical conditions**

PRODUCT DESCRIPTION

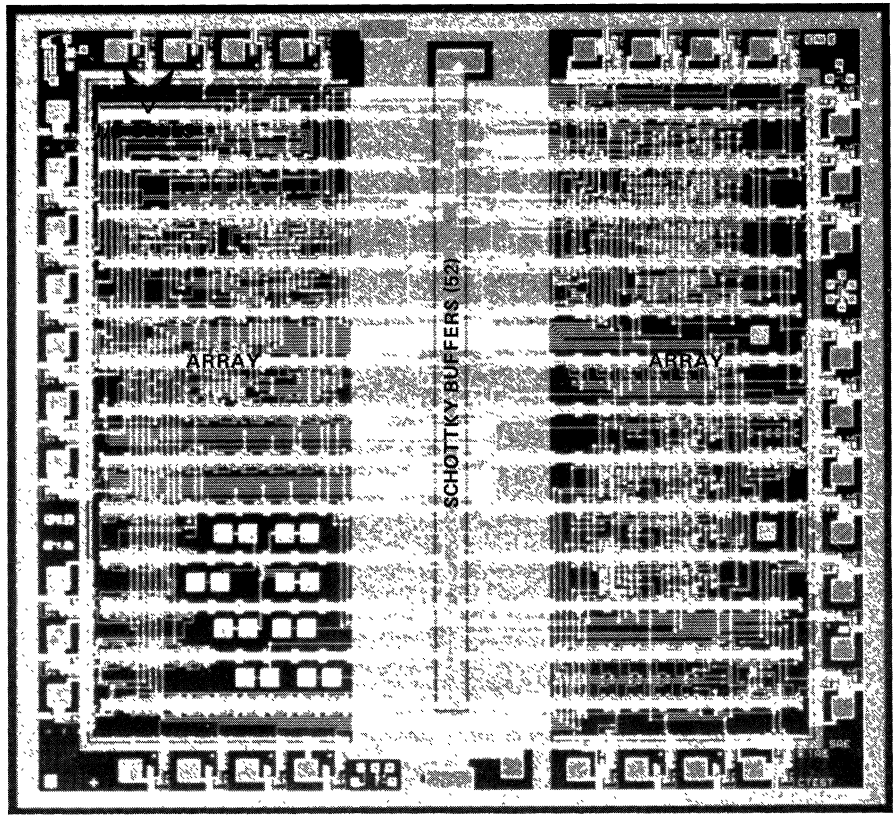
The 8A1200/CG1001 Evaluation Circuit is a committed array of ISL gates, Schottky buffers, and LSTTL I/O cells, providing the user with several logic functions that can be easily and economically implemented by the use of semi-custom LSI. Basically, the CG1001 provides a demonstration vehicle for characterizing design functions of the 8A1200 ISL Gate Array; the demonstration part contains logic functions that are representative of, and can be compared with, those of standard 7400-series parts.

Also, the CG1001 contains several test configurations that can be used in evaluating circuit performance under various logical, topological, and environmental conditions. A block diagram of the Gate Array Evaluation Circuit is shown in Figure 2 and logic representations of each discrete function are shown in Figures 3 through 6.

ORDERING INFORMATION

Contact Local Sales Representative

8A1200/CG1001 EVALUATION CIRCUIT



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8A1200 EVALUATION CIRCUIT CG1001

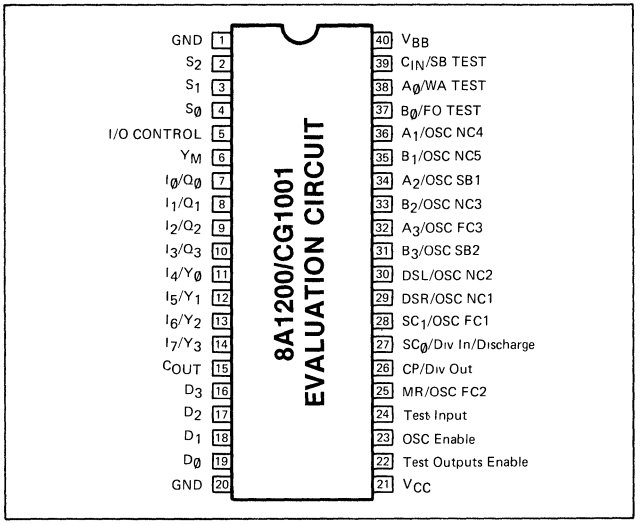

Figure 1. Package Configuration and Pin Designators of 8A1200/CG1001 Evaluation Circuit

Table 1. PIN DESCRIPTIONS OF EVALUATION CIRCUIT

Pin No.	Description	I/O Cell	Function
1	GND	——	Ground
2, 3, 4	$S_2, S_1, S_Ø$	INB	Multiplexer-select and test-select input
5	I/O control	EOCD	Three-state control for pins 7 through 15; H = output/L = input or three-state
6	Y_M	OC	Open-collector multiplexer output
7, 8, 9, 10	$Q_Ø, Q_1, Q_2, Q_3$ if pin 5 = *High*	TTS	Three-state shift register output
	$I_Ø, I_1, I_2, I_3$ if pin 5 = *Low*		Multiplexer inputs
11, 12, 13, 14	$Y_Ø, Y_1, Y_2, Y_3$ if pin 5 = *High*	TTS	Three-state adder sum
	I_4, I_5, I_6, I_7 if pin 5 = *Low*		Multiplexer inputs
15	C_{OUT}	TS	Three-state carry out from adder
16, 17, 18, 19	$D_3, D_2, D_1, D_Ø$	INB	Parallel data inputs for shift register
20	GND	——	Ground
21	V_{CC}	——	+5V supply
22	Test output enable	IOD	Three-state control for pins 25, 28, and 30 through 38, H = output/L = input
23	Osc enable	INB	Ring oscillator enable input
24	Test input	INB	Input for fan-out, Wired-AND, and Schottky buffer tests
25	$\overline{MR}$ if pin 22 = *Low*	TTS	Active-low input to reset shift register
	Osc FC2 if pin 22 = *High*		Far-collector ring oscillator #2 (output)
26	CP if pin 22 = *Low*	TTS	Input clock for shift register
	Div Out if pin 22 = *High*		Toggle flip-flop output
27	$SC_Ø$/Div In/Discharge	INB	Input for multiplexer, flip-flop, and wired-AND
28	SC_1 if pin 22 = *Low*	TEOC	Input for multiplexer select control W/$SC_Ø$
	Osc FC1 if pin 22 is *High*		Far-collector ring oscillator #1 (output)
29	DSR if pin 22 = *Low*	TOC	Shift right serial input
	Osc NC1 if pin 22 = *High*		Near-collector ring oscillator #1 (output)

Table 1. PIN DESCRIPTIONS OF EVALUATION CIRCUIT (Cont'd)

Pin No.	Description	I/O Cell	Function
30	DSL if pin 22 = *Low*	TTS	Shift left serial input
	Osc NC2 if pin 22 = *High*		Near-collector ring oscillator #2 (output)
31	B_3 if pin 22 = *Low*	TTS	Adder input
	Osc SB2 if pin 22 = *High*		Schottky buffer ring oscillator #2 (output)
32	A_3 if pin 22 = *Low*	TTS	Adder input
	Osc FC3 if pin 22 = *High*		Far-collector ring oscillator #2 (output)
33	B_2 if pin 22 = *Low*	TTS	Adder input
	Osc NC3 if pin 22 = *High*		Near-collector ring oscillator #3 (output)
34	A_2 if pin 22 = *Low*	TTS	Adder input
	Osc SB1 if pin 22 = *High*		Schottky buffer ring oscillator #2 (output)
35	B_1 if pin 22 = *Low*	TTS	Adder input
	Osc NC5 if pin 22 = *High*		Near-collector ring oscillator #5 (output)
36	A_1 if pin 22 = *Low*	TTS	Adder input
	Osc NC4 if pin 22 = *High*		Near-collector ring oscillator #4 (output)
37	$B_\emptyset$ if pin 22 = *Low*	TTS	Adder input
	$F_\emptyset$ test if pin 22 = *High*		Fan-out test output
38	$A_\emptyset$ if pin 22 = *Low*	TTS	Adder input
	WA test if pin 22 = *High*		Wired-AND test output
39	C_{IN} if pin 22 = *Low*	TTS	Adder carry input
	SB test if pin 22 = *High*		Schottky buffer test output
40	V_{BB}	—	1.5V bias for ISL cells

FUNCTION TABLES

8-TO-1 MULTIPLEXER

PIN 5 =L (INPUT)
PIN 22 = L (TEST OUTPUTS OFF)
PIN 23 = L (OSC OFF)

FUNCTION →	S_2	S_1	$S_\emptyset$	$I_\emptyset$	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Y_M
PIN NO. →	2	3	4	7	8	9	10	11	12	13	14	6
STATES →	L	L	L	L	X	X	X	X	X	X	X	L
	L	L	L	H	X	X	X	X	X	X	X	H
	L	L	H	X	L	X	X	X	X	X	X	L
	L	L	H	X	H	X	X	X	X	X	X	H
	L	H	L	X	X	L	X	X	X	X	X	L
	L	H	L	X	X	H	X	X	X	X	X	H
	L	H	H	X	X	X	L	X	X	X	X	L
	L	H	H	X	X	X	H	X	X	X	X	H
	H	L	L	X	X	X	X	L	X	X	X	L
	H	L	L	X	X	X	X	H	X	X	X	H
	H	L	H	X	X	X	X	X	L	X	X	L
	H	L	H	X	X	X	X	X	H	X	X	H
	H	H	L	X	X	X	X	X	X	L	X	L
	H	H	L	X	X	X	X	X	X	H	X	H
	H	H	H	X	X	X	X	X	X	X	L	L
	H	H	H	X	X	X	X	X	X	X	H	H

Legend

H = *High* voltage level

h = *High* voltage level one setup time prior to the *Low*-to-*High* clock transition

L = *Low* voltage level

ℓ = *Low* voltage level one setup time prior to the *Low*-to-*High* clock transition

$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the *Low*-to-*High* clock transition

↑ = *Low*-to-*High* clock transition

x = Don't care

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8A1200 EVALUATION CIRCUIT — CG1001

FUNCTION TABLES (cont'd)

4-BIT SHIFT REGISTER

PIN 5 = H (OUTPUT)
PIN 22 = L (TEST OUTPUTS OFF)
PIN 23 = L (OSC OFF)

FUNCTION →	CP	MR	$SO_\emptyset$	SC_1	D_{SR}	D_{SL}	$D_\emptyset$	D_1	D_2	D_3	$Q_\emptyset$	Q_1	Q_2	Q_3
PIN NO. →	26	25	27	28	29	30	19	18	17	16	7	8	9	10
LOAD →	X	L	X	X	X	X	X	X	X	X	L	L	L	L
HOLD →	X	H	ℓ	ℓ	X	X	X	X	X	X	$q_\emptyset$	q_1	q_2	q_3
SHIFT LEFT →	↑	H	ℓ	h	X	ℓ	X	X	X	X	q_1	q_2	q_3	L
	↑	H	ℓ	h	X	h	X	X	X	X	q_1	q_2	q_2	H
SHIFT RIGHT →	↑	H	h	ℓ	ℓ	X	X	X	X	X	L	$q_\emptyset$	q_1	q_2
	↑	H	h	ℓ	h	X	X	X	X	X	H	$q_\emptyset$	q_1	q_2
LOAD →	↑	H	h	h	X	X	$d_\emptyset$	d_1	d_2	d_3	$d_\emptyset$	d_1	d_2	d_3

4-BIT ADDER (TYPICAL FUNCTION)

PIN 5 = H (OUTPUT)
PIN 22 = L (TEST OUTPUTS OFF)
PIN 23 = L (OSC OFF)

FUNCTION →	B_3	A_3	B_2	A_2	B_1	A_1	$B_\emptyset$	$A_\emptyset$	C_{IN}	Y_3	Y_2	Y_1	$Y_\emptyset$	C_{OUT}
PIN NO. →	31	32	33	34	35	36	37	38	39	14	13	12	11	15
STATES →	H	H	L	L	L	H	H	L	L	L	L	H	H	H
	H	L	L	H	H	L	H	L	H	L	L	L	L	H
	L	H	H	L	H	L	L	L	H	H	H	H	H	L

DC ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current at V_{CC}	Pins 5 and 22 = L (OUTPUT ENABLES)		56	87		59	93	mA
I_{BB}	Supply current at V_{BB}			62	85		62	93	mA

NOTE. All other DC CHARACTERISTICS are specific to the I/O cells and can be found in the Data Sheet pertaining to the 8A1200 ISL Gate.

8A1200 EVALUATION CIRCUIT — CG1001

AC ELECTRICAL CHARACTERISTICS

PARAMETERS (Note 1)	REFERENCES FROM	REFERENCES TO	TEST CONDITIONS	LIMITS (COMMERCIAL) MIN	LIMITS (COMMERCIAL) TYP	LIMITS (COMMERCIAL) MAX	LIMITS (MILITARY) MIN	LIMITS (MILITARY) TYP	LIMITS (MILITARY) MAX	UNITS
Propagation delay of 8-to-1 Multiplexer										
t_{pdHL}	PINS 7-14	PIN 6	See test setup		40					ns
t_{pdLH}	PINS 7-14	PIN 6	below		55					ns

TEST SETUP FOR 8-TO-1 MULTIPLEXER

PIN 5 = L (INPUT)
PIN 22 = L (TEST OUTPUTS OFF)
PIN 23 = L (OSC OFF)

FUNCTION → / PIN NO. →	S_2 2	S_1 3	$S_\emptyset$ 4	$I_\emptyset$ 7	I_1 8	I_2 9	I_3 10	I_4 11	I_5 12	I_6 13	I_7 14	Y_M 6
STATES →	L	L	L	In	L	L	L	L	L	L	L	Out
	L	L	H	L	In	L	L	L	L	L	L	Out
	L	H	L	L	L	In	L	L	L	L	L	Out
	L	H	H	L	L	L	In	L	L	L	L	Out
	H	L	L	L	L	L	L	In	L	L	L	Out
	H	L	H	L	L	L	L	L	In	L	L	Out
	H	H	L	L	L	L	L	L	L	In	L	Out
	H	H	H	L	L	L	L	L	L	L	In	Out

PARAMETERS (Note 1)	REFERENCES FROM	REFERENCES TO	TEST CONDITIONS	LIMITS (COMMERCIAL) MIN	LIMITS (COMMERCIAL) TYP	LIMITS (COMMERCIAL) MAX	LIMITS (MILITARY) MIN	LIMITS (MILITARY) TYP	LIMITS (MILITARY) MAX	UNITS
Propagation delay of 4-Bit Adder										
t_{pdHL}	PIN 39	PIN 15			41					ns
t_{pdLH}			See test setup		40					ns
t_{pdHL}	PIN 39	PIN 11	below		42					ns
t_{pdLH}					35					ns
t_{pdHL}	PIN 32	PIN 15			40					ns
t_{pdLH}					35					ns

TEST SETUP FOR 4-BIT ADDER

PIN 5 = H (OUTPUT)
PIN 22 = L (TEST OUTPUTS OFF)
PIN 23 = L (OSC OFF)

FUNCTION → / PIN NO. →	B_3 31	A_3 32	B_2 33	A_2 34	B_1 35	A_1 36	$B_\emptyset$ 37	$A_\emptyset$ 38	C_{IN} 39	Y_3 14	Y_2 13	Y_1 12	$Y_\emptyset$ 11	C_{OUT} 15
STATES →	L	H	L	H	L	H	L	H	In	X	X	X	X	Out
	L	L	L	L	L	L	L	L	In	X	X	X	Out	X
	H	In	L	H	L	H	L	H	L	X	X	X	X	Out

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AC ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETERS (Note 1)	REFERENCES FROM	REFERENCES TO	TEST CONDITIONS	LIMITS (COMMERCIAL) MIN	LIMITS (COMMERCIAL) TYP	LIMITS (COMMERCIAL) MAX	LIMITS (MILITARY) MIN	LIMITS (MILITARY) TYP	LIMITS (MILITARY) MAX	UNITS
Propagation delay of Fan-In/Fan-Out tests										
t_{pdHL}	PIN 24	PIN 37	See test setup		37					ns
t_{pdLH}			"r" below		36					ns
t_{pdHL}			See test setups		38					ns
t_{pdLH}			"s" and "t" below		35					ns
t_{pdHL}			See test setups		37					ns
t_{pdLH}			"v" and "w" below		33					ns
t_{pdHL}	PIN 24	PIN 38	See test setup		744					ns
t_{pdLH}			"p" below		737					ns
t_{pdHL}			See test setup		39					ns
t_{pdLH}			"r" below		40					ns
t_{pdHL}			See test setups		40					ns
t_{pdLH}			"s" "t", and "u" below		40					ns
t_{pdHL}			See test setups		51					ns
t_{pdLH}			"v", "w", and "x" below		40					ns
t_{pdHL}	PIN 24	PIN 39	See test setup		35					ns
t_{pdLH}			"r" below		35					ns
t_{pdHL}			See test setup		34					ns
t_{pdLH}			"s" below		36					ns
t_{pdHL}			See test setup		28					ns
t_{pdLH}			"v" below		38					ns

TEST SETUPS FOR FAN-IN/FAN-OUT TESTS (See DELAY COMPARISONS)

PIN 5 = L (INPUT)
PIN 22 = H (TEST OUTPUTS ON)
PIN 23 = L (OSC OFF)

TEST SETUP	SELECTOR S_1 PIN 3	SELECTOR $S_\emptyset$ PIN 4	DISCHARGE (NOTE 2) PIN 27	LOAD PIN 2	TEST INPUT PIN 24	FAN-OUT TEST PIN 37	Wired-AND TEST PIN 38	SCHOTTKY BUFFER TEST PIN 39
p	L	L	L	L	In	–	Out	–
r	L	H	L	L	In	Out	Out	Out
s	H	L	L	L	In	Out	Out	Out
t	H	L	⌐¯_	H	In	Out	Out	–
u	H	L	⌐¯_	L	In	–	Out	–
v	H	H	L	L	In	Out	Out	Out
w	H	H	⌐¯_	H	In	Out	Out	–
x	H	H	⌐¯_	L	In	–	Out	–

AC ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETERS (Note 1)	REFERENCES FROM	REFERENCES TO	TEST CONDITIONS	LIMITS (COMMERCIAL) MIN	LIMITS (COMMERCIAL) TYP	LIMITS (COMMERCIAL) MAX	LIMITS (MILITARY) MIN	LIMITS (MILITARY) TYP	LIMITS (MILITARY) MAX	UNITS
Propagation delay of 4-Bit Shift Register			See test setup							
t_{pdHL}	PIN 26	PINS 7,8	below		34					ns
t_{pdLH}					34					ns
t_{pdHL}	PIN 26	PIN 9			37					ns
t_{pdLH}					34					ns
t_{pdHL}	PIN 26	PIN 10			33					ns
t_{pdLH}					33					ns
t_{pdHL}	PIN 25	PINS 7-10			33					ns

TEST SETUP FOR 4-BIT SHIFT REGISTER

PIN 5 = H (OUTPUT)
PIN 22 = L (TEST OUTPUTS OFF)
PIN 23 = L (OSC OFF)

FUNCTION (NOTES 3, 4, & 5) → / PIN NO. →	CP 26	$\overline{MR}$ 25	SC_0 27	SC_1 28	D_{ST} 29	D_{SL} 30	D_0 19	D_1 18	D_2 17	D_3 16	Q_0 7	Q_1 8	Q_2 9	Q_3 10
STATES →	In(↑)	H	H	H	X	X	D_{IN}	X	X	X	Out	X	X	X
	In(↑)	H	H	H	X	X	X	X	D_{IN}	X	X	X	Out	X
	In(↑)	H	H	H	X	X	X	X	X	D_{IN}	X	X	X	Out
	X	In	X	X	X	X	X	X	X	X	Out	Out	Out	Out

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AC ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETERS (Note 1)	REFERENCES FROM	REFERENCES TO	TEST CONDITIONS	LIMITS (COMMERCIAL) MIN	LIMITS (COMMERCIAL) TYP	LIMITS (COMMERCIAL) MAX	LIMITS (MILITARY) MIN	LIMITS (MILITARY) TYP	LIMITS (MILITARY) MAX	UNITS
Propagation delay for Divider.										
t_{pdHL}	PIN 27	PIN 26	See test setup		44					ns
t_{pdLH}			below		39					ns
Period of Ring Oscillator.										
tosc	–	PIN 25			108					ns
tosc	–	PIN 28			109					ns
tosc	–	PIN 29			107					ns
tosc	–	PIN 30			106					ns
tosc	–	PIN 31	See test setup below		101					ns
tosc	–	PIN 32			107					ns
tosc	–	PIN 33			86					ns
tosc	–	PIN 34			91					ns
tosc	–	PIN 35			147					ns
tosc	–	PIN 36			82					ns

TEST SETUP FOR DIVIDER/RING OSCILLATORS

PIN 23 = L (OSC OFF)

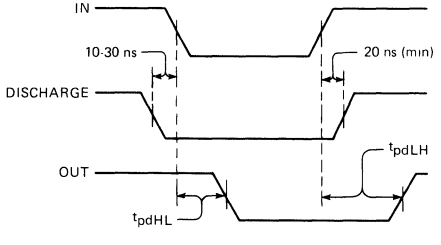
PIN 5 = L (INPUT)
PIN 22 = H (TEST OUTPUTS ON)
PIN 23 = H (OSC ON)

DIV IN PIN 27	DIV OUT PIN 26	OSC FC2 PIN 25	OSC FC1 PIN 28	OSC NC1 PIN 29	OSC NC2 PIN 30	OSC SB2 PIN 31	OSC FC3 PIN 32	OSC NC3 PIN 33	OSC SB1 PIN 34	OSC NC5 PIN 35	OSC NC4 PIN 36
In(↑)	Out	Oscillator Calculations. The ten 11-gate rings oscillate with a period (t_{osc}) equal to 22 gate delays. Average gate delay (t_{avg} = half pair delay) can be calculated as follows: $t_{avg} = \frac{t_{osc}}{22} = \frac{t_{pdLH} + t_{pdHL}}{2}$									

Notes.

1. Measure t_{pdLH} and t_{pdHL} from "In" to "Out" for each path.
2. Discharge input (pin 27) must meet both MIN and MAX times for setup and hold– see WAVEFORM 1.
3. For $Q_{\emptyset}$ and Q_1 outputs (pins 7 and 8), propagation delay is representative of the delay through an input buffer, a three-state output buffer with a fan-in of 1, and a standard ISL "D" flip-flop.
4. For the Q_2 output (pin 9), the propagation delay will differ from that of $Q_{\emptyset}$ and Q_1 by the Δ time delay caused by the additional fan-in of 4 on the three-state output buffer.
5. For the Q_3 output (pin 10), the propagation delay will differ from that of $Q_{\emptyset}$ and Q_1 by the Δ time delay caused by the additional fan-in of 2 on the three-state output buffer.

WAVEFORM 1: Discharge Input Timing



DELAY COMPARISONS

Wired-AND Test (Pin 38)

COMPARISON (Note 1)	DESCRIPTION
(r) - (s)	Effect of Δ fan-in of 4 on ISL gate delay, load capacitors precharged
(r) - (u)	Effect of Δ fan-in of 4 on ISL gate delay, load capacitors discharged
(s) - (v)	Effect of Δ fan-in of 5 on ISL gate delay, load capacitors precharged
(u) - (x)	Effect of Δ fan-in of 5 on ISL gate delay, load capacitors discharged
(r) - (v)	Effect of Δ fan-in of 9 on ISL gate delay, load capacitors precharged
(r) - (x)	Effect of Δ fan-in of 9 on ISL gate delay, load capacitors discharged
(t) - (u)	Effect of dummy loads, fan-in = 5
(w) - (x)	Effect of dummy loads, fan-in = 10
(s) - (u)	Effect of worst case pattern sensitivity, fan-in = 5
(v) - (x)	Effect of worst case pattern sensitivity, fan-in = 10
(p)	Delay of 142 ISL gates + input buffer + T.S. output buffer

DELAY COMPARISONS (cont'd)

Fan-Out Test (Pin 37)

COMPARISONS (Note 1)	DESCRIPTION (Note 2)
(r) - (s)	Effect of Δ fan-out of 1 active load on ISL gate delay
(s) - (v)	Effect of Δ fan-out of 2 active loads on ISL gate delay
(r) - (v)	Effect of Δ fan-out of 3 active loads on ISL gate delay
(s) - (t)	Effect of active to passive loading, fan-out = 2
(v) - (w)	Effect of active to passive loading, fan-out = 4

Schottky Buffer Test (Pin 39)

COMPARISONS (Note 1)	DESCRIPTION
(r) - (s)	Effect of resistor input to ISL gate
(s) - (v)	Effect of Δ fan-out of 9 on Schottky buffer delay

Notes:

1. Letters in parentheses refer to the TEST SETUPS FOR FAN-IN/FAN-OUT TESTS; actual numerical values are listed in the appropriate AC CHARACTERISTICS table.
2. "Active Load" means both AC and DC loading; "passive load" refers only to AC loading.

FUNCTIONS OF RING OSCILLATORS (Note)

DESIG/PIN NO.	DESCRIPTION
NC1/PIN 29	Near collector ring oscillator
FC1/PIN 28	Far collector ring oscillator
FC2/PIN 25	Far collector ring oscillator with near collectors present, but unconnected
FC3/PIN 32	Far collector ring oscillator with near collectors tied together and brought out to an internal probe pad
NC2/PIN 30	Near collector ring oscillator with far collectors all tied together and brought out to an internal probe pad
NC3/PIN 33	Near collector ring oscillator with far collectors each individually loaded with an ISL gate
NC4/PIN 36	Near collector ring oscillator with far collectors each individually pulled up to V_{bb} with separate resistors
NC5/PIN 35	Near collector ring oscillator loaded with metal capacitors
SB1/PIN 34	Schottky buffer ring oscillator using direct input gates
SB2/PIN 31	Schottky buffer ring oscillator using resistor input gates

NOTE:
Oscillator enable (pin 23) enables ring oscillators when high; when low, the oscillator is stopped to reduce power supply noise for other noise sensitive tests.

RING OSCILLATOR COMPARISONS

DESIGNATORS	DESCRIPTION
NC1-FC1	Comparison of near-collector to far-collector gate delays. The delta delay is typically less than 0.2 ns and is ignored.
FC1-FC2	Effect that floating collector has upon stored charge. This collector can act as a third parasitic PNP which can decrease gate delay. The delta delay is typically less than 0.3 nS and is ignored.
FC1-FC3	Effect of charge sharing between several gates. Common collector acts as a capacitive current source which can decrease gate delays. The delta delay is typically less than 0.2 nS and is ignored.
NC2-FC3	Comparison of effect of capacitive current source charging point. The delta delay between near collectors tied together and far collectors tied together is typically less than 0.3 nS and is ignored.
NC1-NC3	Effect of farout on average gate delay. The delta delay between loaded and unloaded gates is typically less than 1.0 nS. Since the speed up of a loaded gate is a function of the state of logic on the output of the gate, this speedup is normally ignored.
NC3-NC4	Effect of pullup on average gate delay. The delta delay between a gate which has a second collector connected to a gate input and one connected to a resistor to V_{BB} is typically 0.0 nS.
NC5-NC1	Effect of metal interconnect capacitors on average gate delay. The delta delay between a gate driving minimum length metal lines and one driving lines 123 grids long is typically 2.8 nS (.23 nS/grid). This delta must be accounted for in logic design (max spec = .035 nS/grid).
SB1-SB2	Effect of resistor inputs on average gate delay. The delta delay between gates with and without resistor inputs is typically less than 0.6 nS. This delay is due to the current limiting effect on gate delay. This delay is reflected in gate delay specs.
NC1	Osc period ÷ 22 = average ISL gate delay (F.O. = 1, F.I. = 1). This gate will typically be 4.5 nS.
SB1	Osc period ÷ 22 = average Schottky buffer gate delay (F.O. = 1, F.I. = 1). This gate delay will typically be 4.0 nS.

9

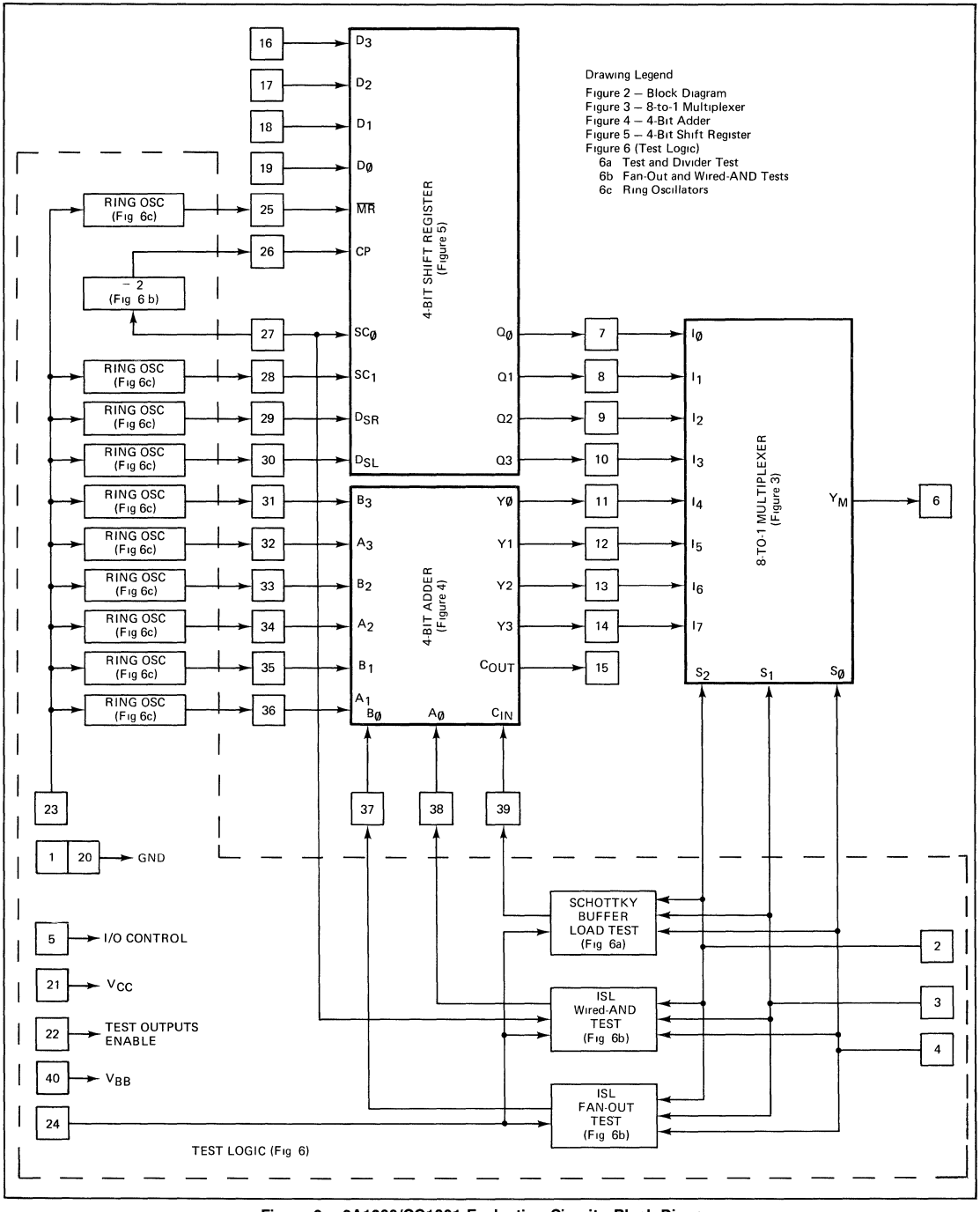


Figure 2. 8A1200/CG1001 Evaluation Circuit—Block Diagram

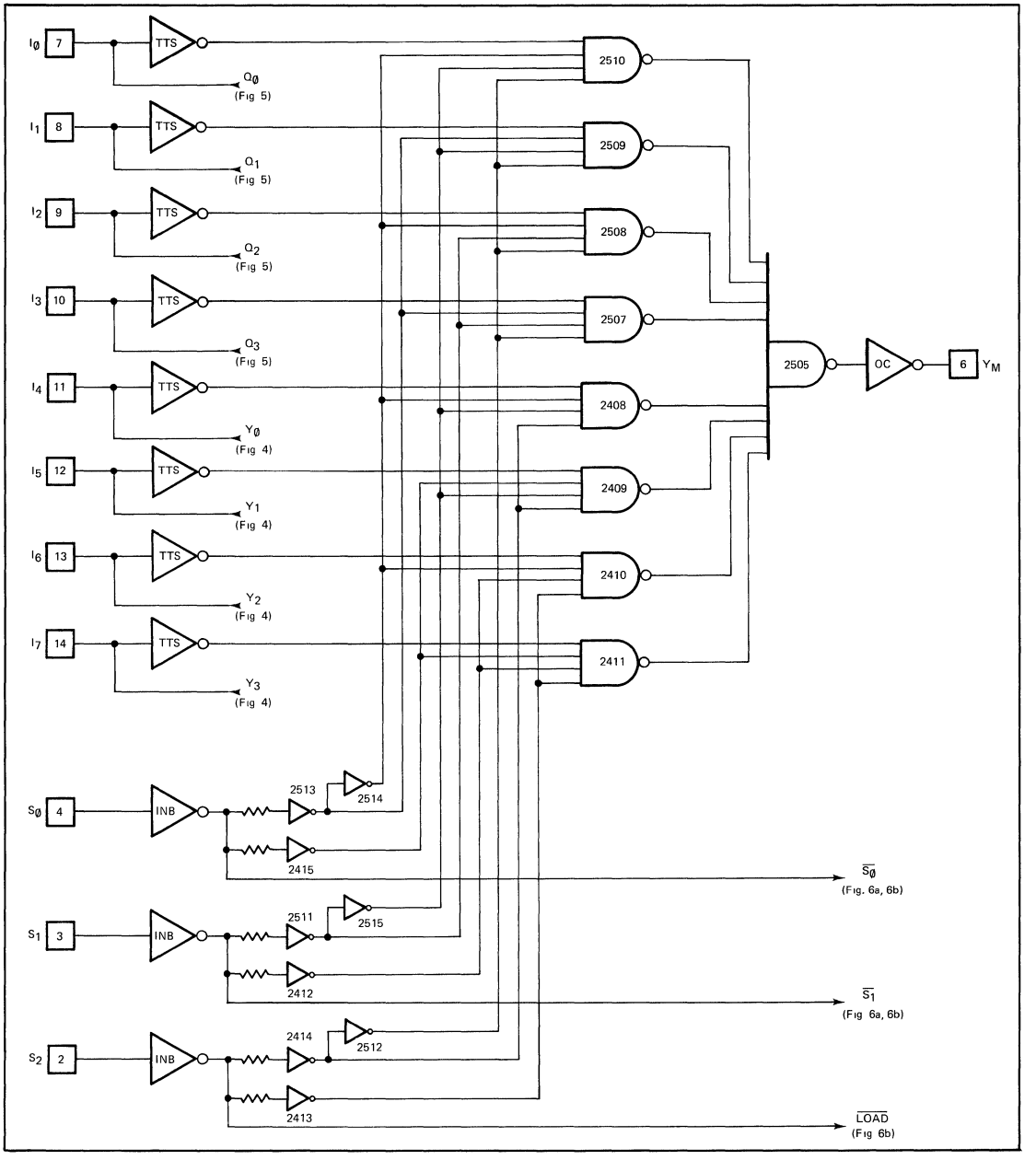


Figure 3. 8-to-1 Multiplexer

8A1200 EVALUATION CIRCUIT

CG1001

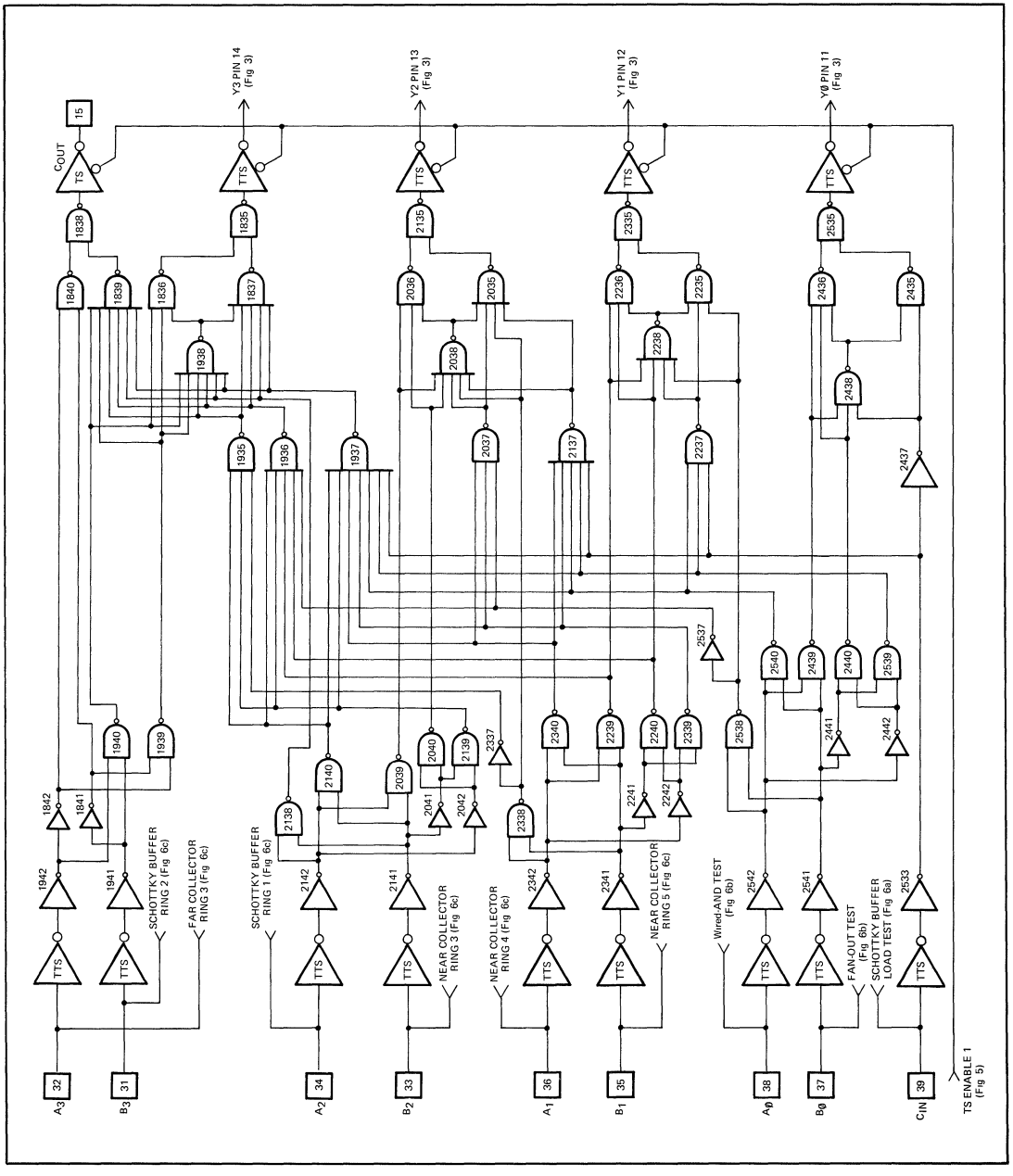


Figure 4. 4-Bit Adder

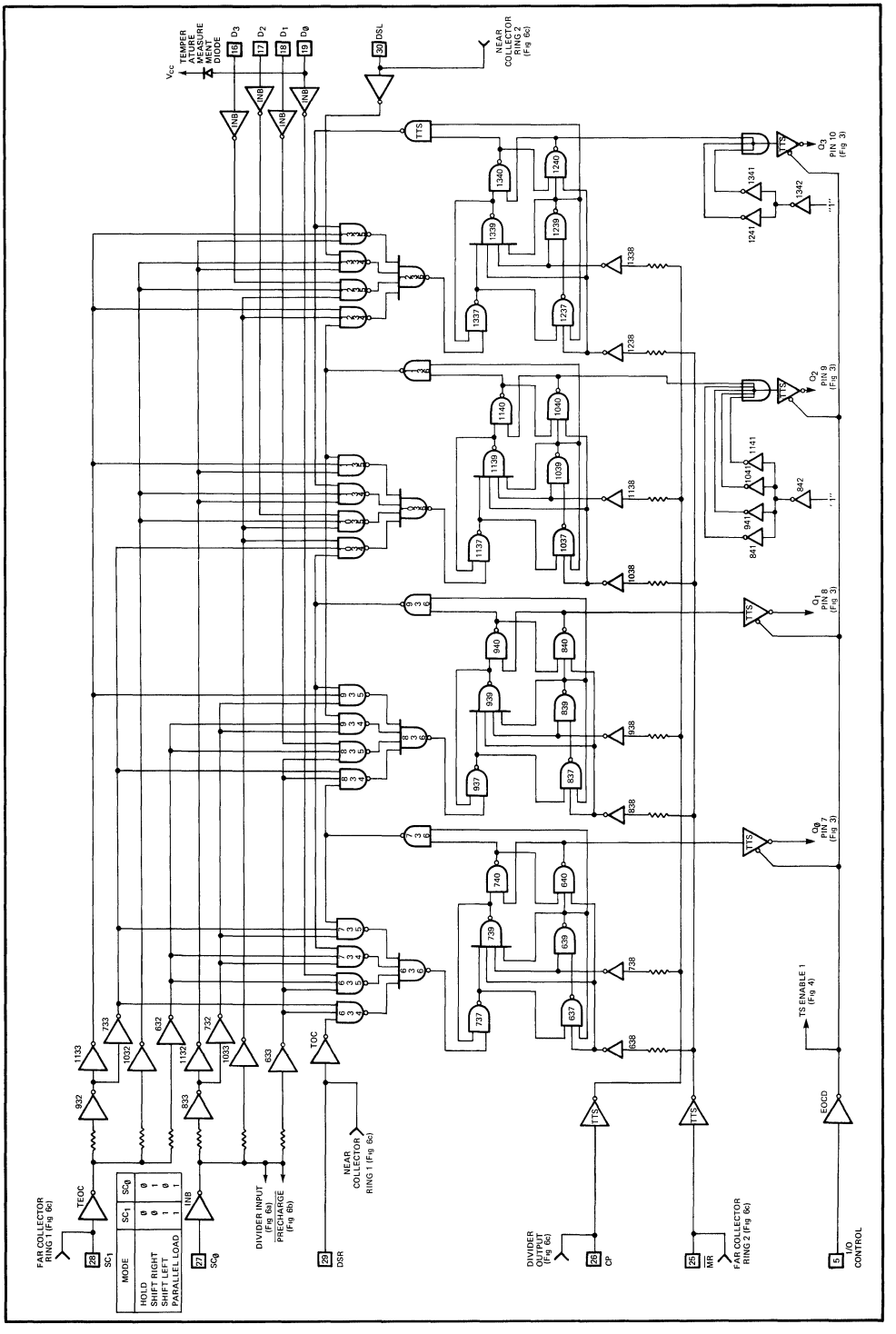


Figure 5. 4-Bit Shift Register

8A1200 EVALUATION CIRCUIT

CG1001

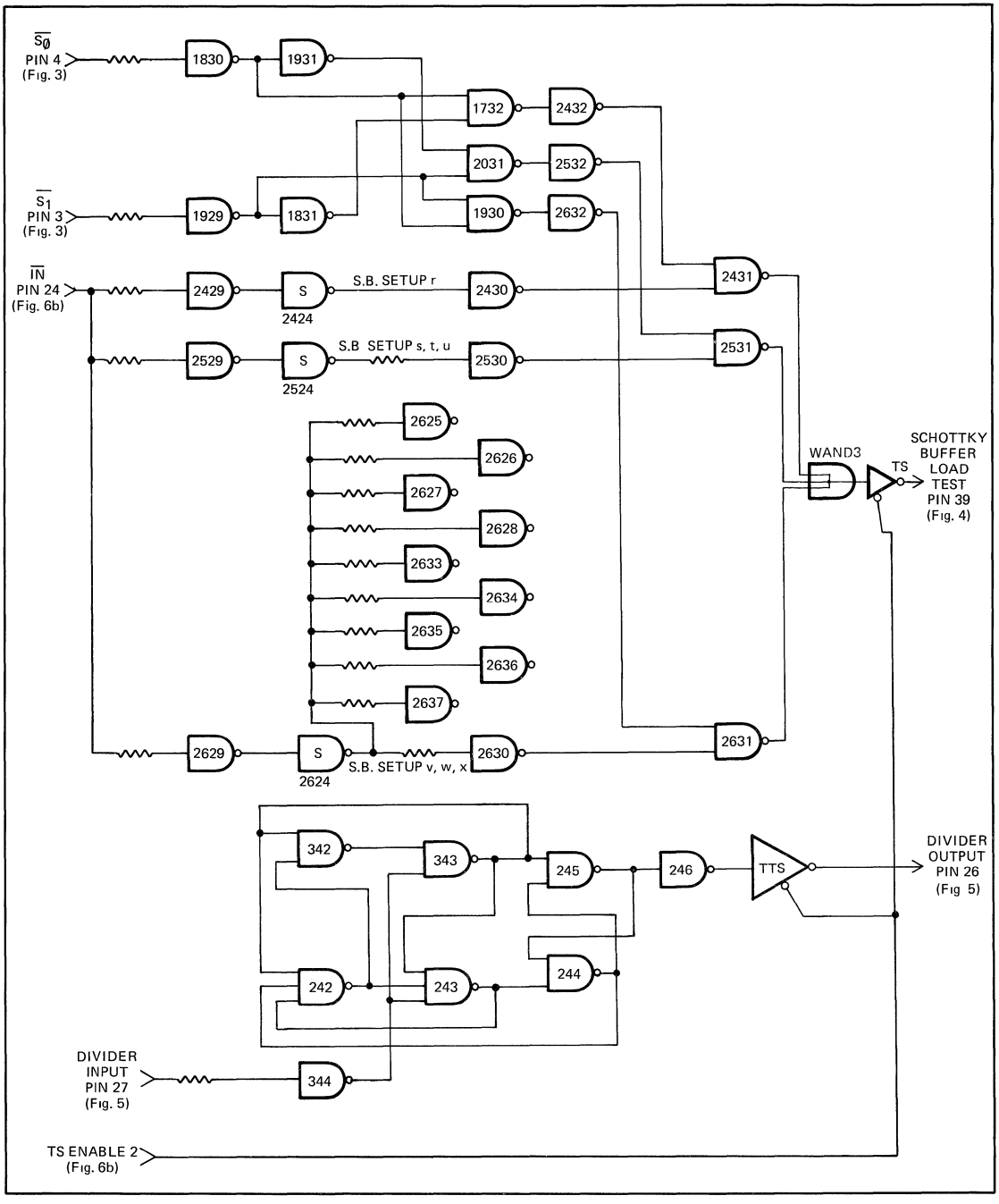


Figure 6a. Test Logic (Test and Divider Test)

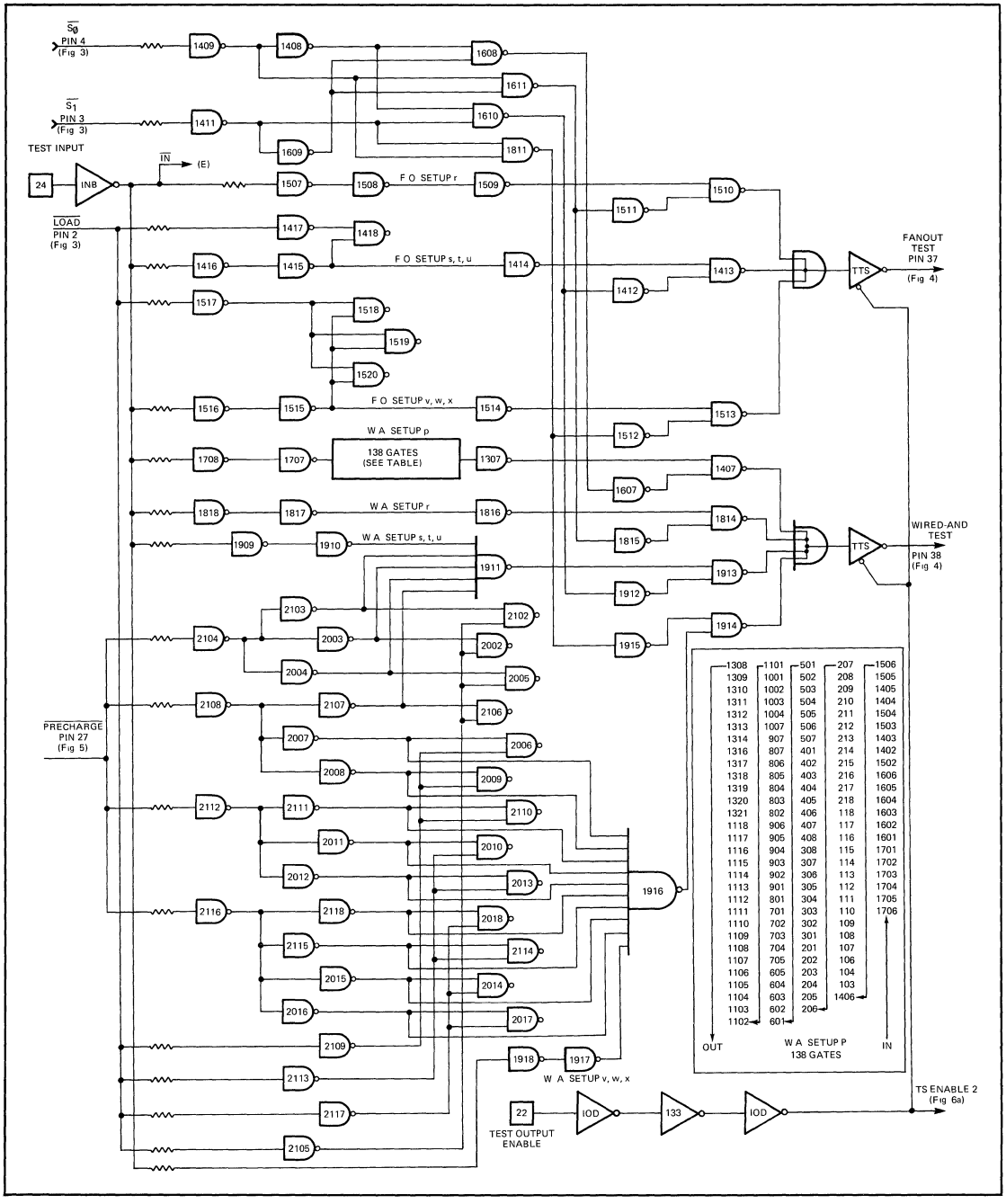
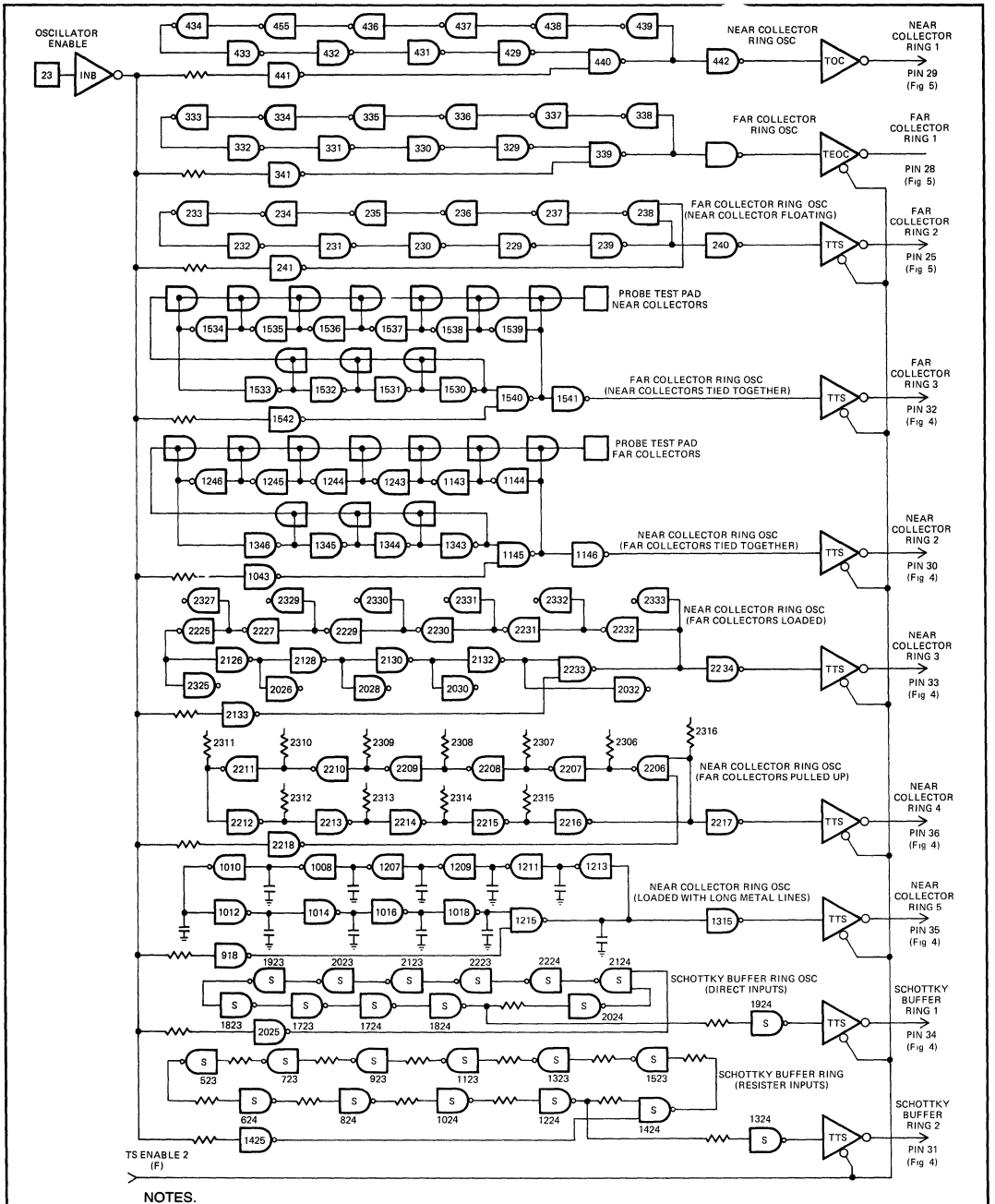


Figure 6b. Test Logic (Fan-Out and Wired-AND Tests)



NOTES.
1. Near collector is nearest to base
2. Far collector is farthest from base.
3. Floating indicates contact present without metal interconnection.

Figure 6c. Test Logic (Ring Oscillators)

NOTES

NOTES

Section 10
Military

INDEX

10

MILITARY PRODUCTS/ PROCESS LEVELS

The Signetics MIL-M-38510 and MIL-STD-883 Programs are organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. These programs are designed to provide our customers.

- Fully compliant 883/M5004 flows on all products.
- Standard processing flows to help minimize the need for custom specifications.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allow customers to buy products off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specifications.

The following explains the different processing options available. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 2 and 3.

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES					
	CERAMIC					
	8-PIN	14-PIN	16-PIN	18-PIN	20-PIN	24-PIN
PB	FE	—	—	—	—	—
CB	—	F	—	—	—	—
EB	—	—	F	—	—	—
JB	—	—	—	—	—	F
DB	—	W	—	—	—	—
FB	—	—	W	—	—	—
RB	—	—	—	—	F	—
VB	—	—	—	F	—	—

All products listed are also available in Die form.

Table 1 MILITARY PACKAGE AVAILABILITY

	JS	JB	RB
	JAN Qualified		883B
54	X	X	X
54LS	X	X	X
54S	X	X	X
82	—	—	X
8T	—	—	X
93XX	—	X	X
96XX	—	—	X
Analog	—	X	X
Bipolar Memory	—	X	X
Microprocessor	—	—	X

Table 2 MILITARY SUMMARY

JAN QUALIFIED (JS and JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M-38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL 38510)

Quality conformance inspection testing, per MIL-STD-883, Method 5005, is performed according to Mil-M-38510 as follows:

- Group A; each sublot. (Alternate Group A)
- Group B; one sublot for each package type every week. (Alternate Group B)
- Group C; one sublot for each microcircuit group every 13 weeks.
- Group D, one sublot for each package type every 26 weeks.

NOTE: This category of part conforms to Quality Level B ($\pi_Q = 1.0$) of MIL-HDBK-217D.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

By implementing this government standardization program, Signetics complies with the trend of reducing the numerous similar Source Control Drawings (SCD's). This standardized trend results in a *single* complete and comprehensive specification, a *single* product flow, and a *single* administrative effort—for both the aerospace community and for Signetics. Because the list of Signetics' qualified products will change periodically, you may wish to contact your nearest Signetics' Sales Office or refer to the *Products Qualified* under Military Specification from DESC for our current update.

JAN Class S products are quoted on a unit price basis only (similar to present Class B programs). There will be no lot charges for SEM inspection, electrical testing, or Group B or D quality conformance inspection. All additional charges are amortized in the unit price.

Package types currently qualified are:
1) Cerdip—ceramic dual-in-line
2) Cerpac—ceramic flat pack

Government Source Inspection (GSI) is a requirement of the JAN 38510 Class S specification. No alterations to this specification may be instituted Therefore, the only allowed customer source inspection option is at pre-ship (verification only).

Additional program data options (such as wafer lot acceptance, attributes, Group B, D, and others) are available upon request for a nominal fee.

MIL-STD-883, LEVEL B

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to MIL-STD-883 Method 5004, and is 100% electrically tested to Signetics data sheets.

Quality conformance inspection per MIL-STD-883, Method 5005, Group A, is performed on each sublot. Group A subgroup electrical parameters are those included in the detailed Signetics data book. Contact the factory for parametric subgroup assignments.

Generic quality conformance data per Method 5005, Groups B, C, and D, is generally available on popular device types and packages, but availability is not guaranteed. The factory must be consulted

prior to ordering generic data. When available, generic data is defined as follows:

- Group B: Performed once per package type every six weeks of seal.
- Group C: Performed once per microcircuit group every 52 weeks of seal.
- Group D: Performed once per package type every 52 weeks of seal.

Quality conformance endpoint electrical parameters for Groups C and D are the Group A subgroups 1, 2, and 3.

Copies of generic data, Groups A, B, C, and D, may be ordered by customers at a nominal charge.

NOTE: This category of part conforms of Quality Level B-2 ($\pi_Q = 6.5$) of MIL-HDBK-217D.

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 and MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS		
			JAN CLASS S	JAN QUALIFIED (B)	883
General Mil-M-38510 1. Pre-Certification A Product Assurance Program B Manufacturer's Certification	The Manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity.	—	X	X	N/A
2. Certification	Received after manufacturer has completed a successful DESC survey.	—	X	X	N/A
3 Device Qualification	Device qualification shall consist of subjecting the desired device to Groups A, B, C, and D of Method 5005.	—	X	X	N/A
4. Traceability	Traceability maintained back to wafer production lots.	—	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories.	—	X	X	N/A
Screening Per Method 5004 of Mil-Std-883					
6. Non-Destructive Bond Pull	2023	100%	×	N/A	N/A
7. Internal Visual (Precap)	2010, Cond. A or B	100%	A	B	B
8. Stabilization Bake	1008, Cond. C Min	100%	×	×	×
9. Temperature Cycling	1010, Cond. C; (10 cycles,–65 °C to + 150 °C)	100%	×	×	×
10. Constant Acceleration	2001 Cond. E; Y1 (30 kg in Y1 Plane)	100%	×	×	×
11. Visual Inspection	There is no test method for this screen; it is intended only for the removal of Catastrophic Failures defined as Missing Leads, Broken Packages or Lids Off.	100%	×	×	×
12. Seal (Hermeticity) A. Fine B. Gross	 1014 Cond. A or B; (5.0 x 10^{-8}CC/Sec) 1014 Cond. C.	 100% 100%	 × ×	 × ×	 × ×
13. Marking	Fungus inhibiting ink	100%	X	×	×
14. Particle Impart Noise Test	2020, Cond. A	100%	×	N/A	N/A
15. Radiographic	2012; two views	100%	×	N/A	N/A
16. Interim Electricals (Pre Burn-In)	Per applicable device specification	100%	×	Optional	Optional
17. Burn-In	1015, Cond. as specified (160 hrs. Min at 125 °C Min)	100%	240 hrs.	×	×

Table 3. REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 and MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS		
			JAN CLASS S	JAN QUALIFIED (B)	883
18 Final Electricals	Per applicable device specification	100%	100% Read & Record	Slash Sheet	Data Sheet
a Static Tests @25°C	Subgroup 1		×	×	×
b Static Tests @ +125°C	Subgroup 2		×	×	×
c Static Tests @ −55°C	Subgroup 3		×	×	×
d Dynamic Test @25°C	Subgroup 4 (for Linear Products only)		×	×	×
e Functional Test @25°C	Subgroup 7		×	×	×
f Switching Test @25°C	Subgroup 9		×	×	×
g Switching Test @ temperature	Subgroup 10, 11, (as applicable)		×	×	×
19. Percent Defective Allowable (PDA)	A PDA of 10% is a requirement applied against the static tests @25°C (A-1) This is controlled by the slash sheets for JAN products. For RB, 10% is standard.	10%	5%	×	×
20 External Visual	2009	100%	×	×	×
Quality Conformance Inspection per Method 5005 of Mil-Std 883	**ATTRIBUTE DATA ONLY**				
21 Group A	Electrical Tests — Final Electricals (#18 above) repeated on a sample basis (Subgroups 1 through 12 as specified) performed in line with final electricals.	Each sublot	×	×	×
22 Group B	Package functional and constructional related test (package dimensions; resistance to solvents; internal, visual, and mechanical bond strength; and solderability).	Each pkg type	Each sublot	Each week of seal	Generic
23 Group C	Die related tests (1,000 hour operating life, temperature cycling, and constant acceleration.	Each µcircuit group	N/A	Each 13 weeks of seal	Generic
24 Group D.	Package related tests (physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration, variable frequency, constant acceleration, and salt atmosphere).	Each pkg type	Each 26 weeks of seal	Each 26 weeks of seal	Generic

Table 3. REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS (Continued)

NOTES

Section 11
Package Information

INDEX

PACKAGE OUTLINES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip demensions are to centerline of leads.
3. Tolerances non-cumulative.
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120 mils square die in the smallest available cavity for hermetic packages. Allunits were solder mounted to P.C. boards, with standard stand-off, for measurement.

PLASTIC ONLY

5. Lead material: Allow 42 (Nickelltron Alloy) Olin 194 (Copper Alloy) or equivalents, solder dipped.
6. Body material: Plastic (Epoxy).
7. Rounded hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.
9. SO Packages-microminiature packages.

HERMETIC ONLY

10. Lead material
    a. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
    b. ASTM allow F-30 (Alloy 42) or equivalent—tin plated, gold plated or solder dipped.
    c. ASTM allow F-15 (KOVAR) or equivalent—gold plated.
11. Body Material
    a. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
    b. Ceramic with glass seal at leads.
    c. BeO ceramic with glass seal at leads.
    d. Ceramic with ASTM alloy F-30 or equivalent.
12. Lid Material
    a. Nickel or tin played nickel, wold seal.
    b. Ceramic, glass seal.
    c. ASTM alloy F-15 or equivalent, gold plated, alloy seal.
    d. BeO Ceramic with glass seal.
13. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
14. Recommended minimum offset before lead bend.
15. Maximum glass climb .010 inches.
16. Maximum glass climb or lid skew is .010 inches.
17. Typical four places.
18. Dimension also applies to seating plane.

STANDARD PRODUCTS:

PIN COUNT	PART NO.	PACKAGES	
		MILITARY	COMMERCIAL
14	9401		N
20	8X353 & 8X355		N
22	8X350	F	N, F
24	8X371,	I	I, N
	8X372	I	I, N
	8X376	I	I, N
	8X382	I	I, N
	8X41		N
	9403		N
28	8X374,	I	N
	8X60,	F	N, F
	8X02A,	I	I
	& 3002	I, F	I, F, N
40	8X310,	I	I, N
	8X320,	I	I, N
	8X330,		N
	8X360,	I	I, N
	& 3001	I	I, N
50	8X305	I	I, N

SEMICUSTOM PRODUCTS

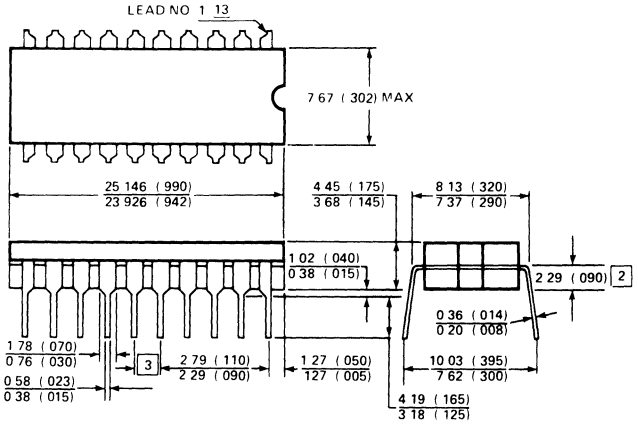
PART NO.	PIN CONFIG	PACKAGE TYPE
8A1200	22, 24, & 28	F
	24, 28, & 40	N
	40	I
8A1260	50	I, N
	44, 68	G
8A1542	40, 50	I, N
	44, 68	G
8A1664	50	I, N
	68	G, Y
8A1864	68	G, Y
8A2176	68	G, Y

Note For package detail on other semicustom products, refer to Data Sheet or your nearest Signetics Sales/Service Office

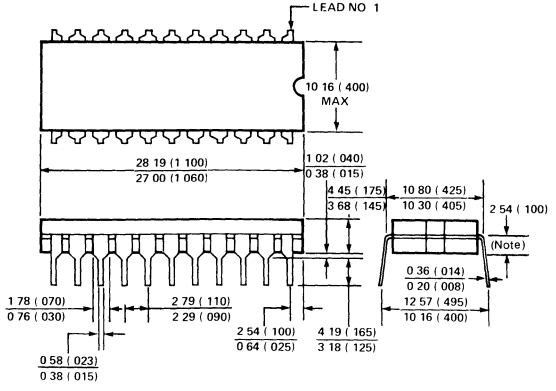
Legend: N = Plastic DIP
I = Ceramic DIP
F = CERDIP
G = Leadless Chip Carrier
Y = Leaded Chip Carrier

PACKAGE OUTLINES

F PACKAGE-CERAMIC
(20-PIN)



F-PACKAGE-HERMETIC
(22-PIN)



PACKAGE OUTLINES

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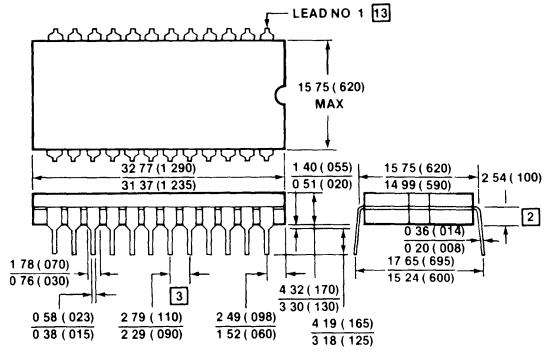
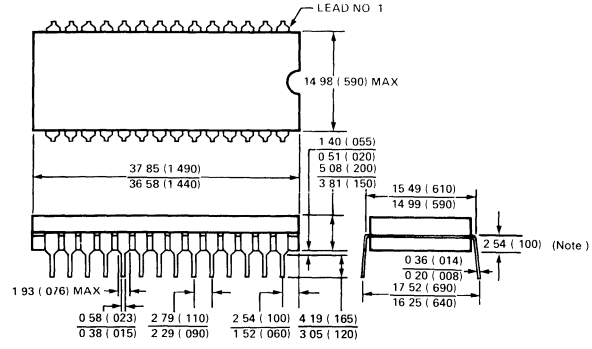


CONSTRUCTION NOTES 10b, 11b, 12b

F-PACKAGE-HERMETIC (28-PIN)



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PACKAGE OUTLINES

G PACKAGE-CHIP CARRIER
(44-PIN)

For current information
contact local sales offices

G PACKAGE-CHIP CARRIER
(68-PIN)

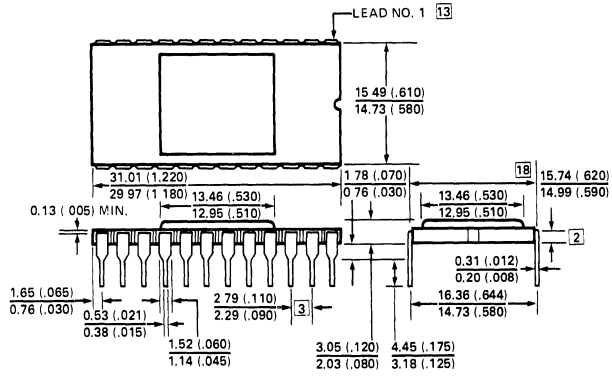
For current information
contact local sales offices

GC-PACKAGE-CHIP CARRIER
(84-PIN)

For current information
contact local sales offices

PACKAGE OUTLINES

I PACKAGE-HERMETIC
(24-PIN)



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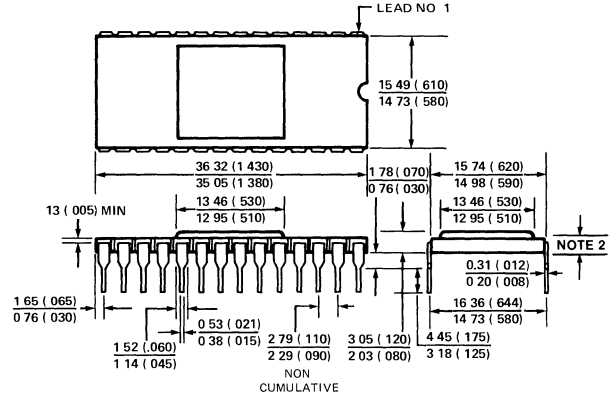

11

PACKAGE OUTLINES

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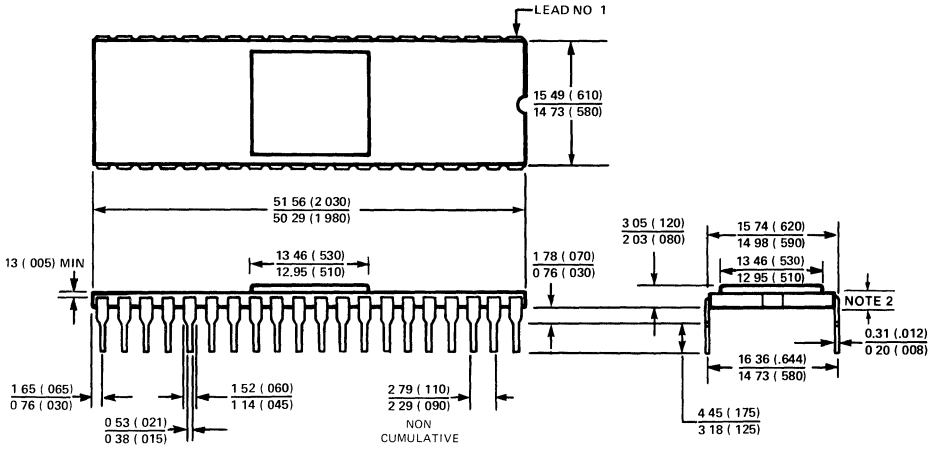
(40-PIN)



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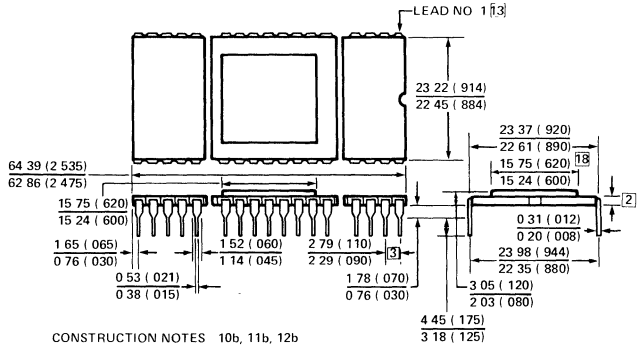

PACKAGE OUTLINES

N PACKAGE PLASTIC
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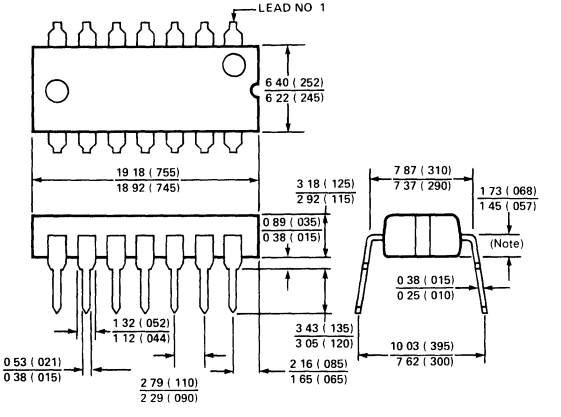

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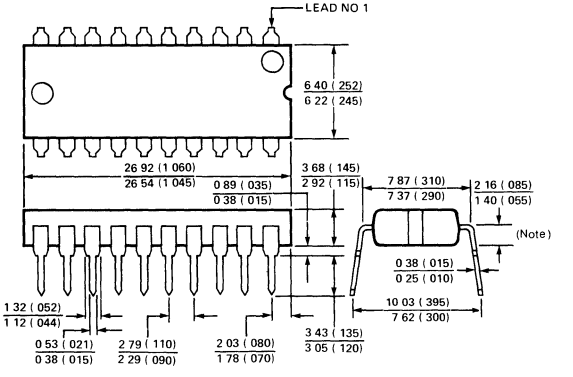
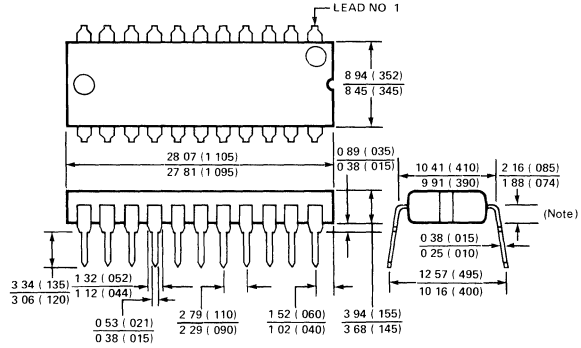
(20-PIN)



PACKAGE OUTLINES

N-PACKAGE-PLASTIC
(22-PIN)



N-PACKAGE-PLASTIC
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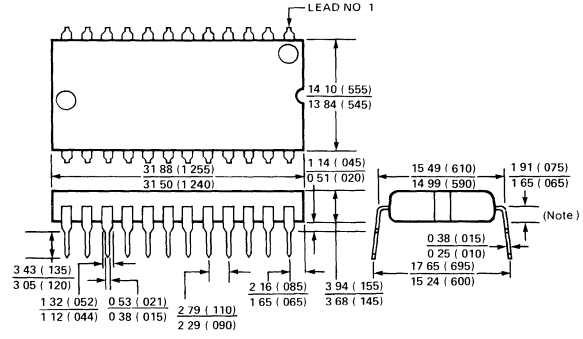
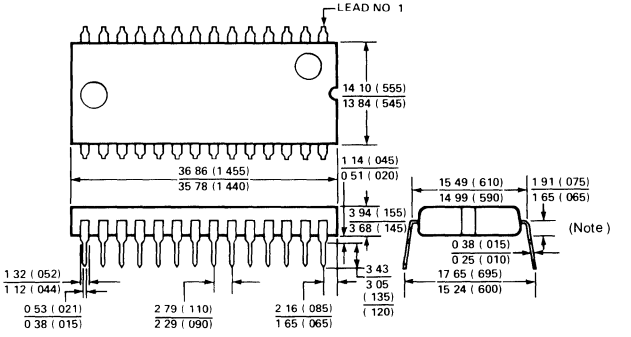


PACKAGE OUTLINES

N-PACKAGE-PLASTIC
(28-PIN)



N-PACKAGE-PLASTIC
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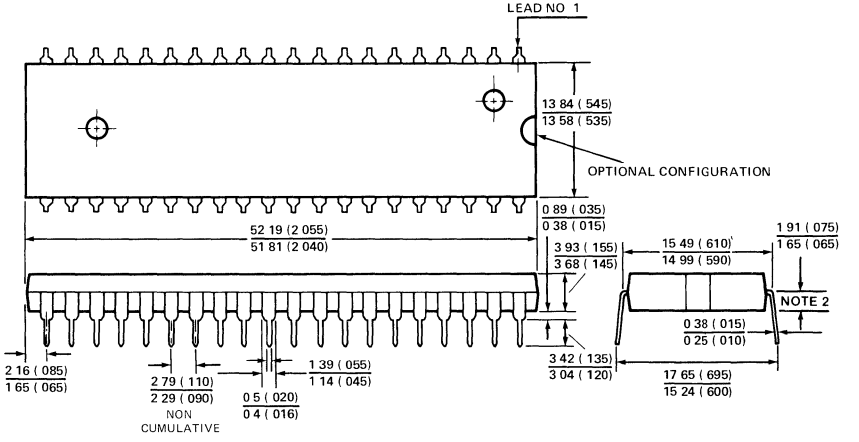

PACKAGE OUTLINES

N PACKAGE-PLASTIC
(50-PIN)

For current information
contact local sales offices

Y PACKAGE-CHIP CARRIER
(68-PIN)

For current information
contact local sales offices

Section 12
Sales Office

SALES OFFICES

SIGNETICS

HEADQUARTERS

811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Phone. (408) 739-7700

ARIZONA
Phoenix
Phone: (602) 265-4444

CALIFORNIA
Canoga Park
Phone: (213) 340-1431
Cupertino
Phone: (408) 725-8100
Inglewood
Phone: (213) 670-1101
Irvine
Phone: (714) 833-8980
(213) 588-3281
San Diego
Phone: (714) 560-0242

COLORADO
Aurora
Phone: (303) 751-5011

CONNECTICUT
Danbury
Phone: (203) 748-3722

FLORIDA
Clearwater
Phone: (813) 796-7086
Ft. Lauderdale
Phone: (305) 486-6300

GEORGIA
Atlanta
Phone (404) 953-0067

ILLINOIS
Schaumburg
Phone: (312) 843-7805

INDIANA
Kokomo
Phone: (317) 453-6462

KANSAS
Overland Park
Phone: (913) 341-8181

MARYLAND
Glen Burnie
Phone: (301) 787-0220

MASSACHUSETTS
Littleton
Phone: (617) 486-8411

MICHIGAN
Farmington Hills
Phone: (313) 476-1610

MINNESOTA
Edina
Phone: (612) 835-7455

NEW JERSEY
Parsippany
Phone: (201) 334-4405

NEW YORK
Liverpool
Phone: (315) 451-5470
Melville
Phone: (516) 752-0130
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