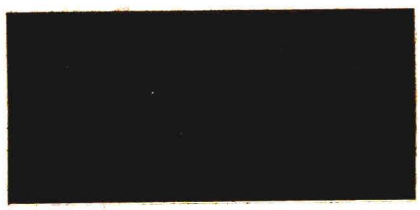
signetics

MICROPROCESSOR

INTRODUCING THE 3000



CONTENTS

INTRODUCING THE SERIES 3000 BIPOLAR MICROPROCESSOR

The introduction of the Signetics Series 3000 Bipolar Microprocessor Chip Set has brought new levels of high performance to microprocessor applications not previously possible with MOS technology. Combining the Schottky bipolar N3001 Microprogram Control Unit (MCU) and N3002 Central Processing Element (CPE) with industry standard memory and support circuits, microinstruction cycle times of 100 nanoseconds are possible.

In the majority of cases, the choice of a bipolar microprocessor slice, as opposed to an MOS device, is based on speed or flexibility of microprogramming. Starting with these characteristics, the design of the Signetics Series 3000 Microprocessor has been optimized around the following objectives:

- Fast cycle time
- All memory and support chips are industry standard
- Cooler operation
- Lower total system cost

Futhermore, systems built with large-scale integrated circuits are much smaller and require less power than equivalent systems using medium and/or small scale integrated circuits.

The two components of the Series 3000 chip set, when combined with industry standard memory and peripheral circuits, allows the design engineer to construct high-performance processors and/or controllers with a minimum amount of auxillary logic. Features such as the multiple independent address and data buses, tri-state logic, and separate output enable lines eliminate the need for time-multiplexing of buses and associated hardware.

Each Central Processing Element represents a complete 2-bit slice through the data processing section of a computer. Several CPE's may be connected in parallel to form a processor of any desired word length. The Microprogram Control Unit controls the sequence in which microinstructions are fetched from the microprogram memory (ROM/PROM), with these microinstructions controlling the step-by-step operation of the processor.

Each CPE contains a 2-bit slice of five independent buses. Although they can be used in a variety of ways, typical connections are:

Input M-bus:	Carries data from external memory
Input I-bus:	Carries data from input/output device
Input K-bus:	Used for microprogram mask or literal (constant) value input
Output A-bus:	Connected to CPE Memory Address Register
Output D-bus:	Connected to CPE accumulator.

As the CPE's are paralleled together, all buses, data paths, and registers are correspondingly expanded.

The microfunction input bus (F-bus) controls the internal operation of the CPE, selecting both the operands and the operation to be executed upon them. The arithmetic logic unit (ALU), controlled by the microfunction decoder, is capable of over 40 Boolean and binary operations as outlined in the FUNCTION DESCRIPTION section of the N3002 data sheet. Standard carry look-ahead outputs (X and Y) are generated by the CPE for use with industry standard devices such as the 74S182.

FEATURES OF THE SERIES 3000 MICROCESSOR CHIP SET

N3001

- Signetics Schottky TTL process
- 45 ns cycle time (typ.)
- Direct addressing of standard bipolar PROM or ROM
- 512 microinstruction addressability
- 4 bit program latch
- 3 flag registers
- 11 address control (jump) functions
- 8 flag control functions

N3002

- 45 ns cycle time (typ.)
- Easy expansion to 2N bits word length
- 11 general purpose registers
- Full function accumulator
- 2's complement arithmetic
- Logical AND, OR, NOT, Exclusive NOR
- Increment, decrement, shift left/right
- Bit testing and zero detect
- Carry look-ahead generation
- Masking via K-bus
- Nondestructive testing of data in accumulator and scratchpad
- 3 input buses
- 2 output buses

FEATURES OF COMPATIBLE PRODUCTS

82S100, 82S101 FPLA

- Field programmable (Ni-Cr Link)
- Input variables - 16
- Output functions - 8
- Product terms - 48
- Address access time - 50 ns
- Tri-state (82S100) or open collector (82S101) outputs
- 28 pin ceramic dip

82S115/123/129 PROMs

- Schottky TTL technology
- Single +5V power supply
- 32 x 8 organization (82S123)
- 256 x 8 organization (82S129)
- 512 x 8 organization (82S115)
- Field programmable (Nichrome)
- On-chip storage latches (82S115 only)
- Low current pnp inputs
- Tri-state outputs
- 35 ns typical access time
- Standard 24 pin DIP (82S115)
- Standard 16 pin DIP (82S123, 82S129)

82S25/82S116/82S11 RAMs

- Schottky TTL technology
- 16 x 4 organization (82S25)
- 256 x 1 organization (82S116)
- 1024 x 1 organization (82S11)
- On-chip address decoding
- 16 pin ceramic dip

8T26A/8T28 Quad Transceiver

- Schottky TTL technology
- Four pairs of bus drivers/receivers
- Separate drive and receive enable lines
- Tri-state outputs
- Low current pnp inputs
- High fan out - driver sinks 40mA
- 20 ns maximum propagation delay
- Standard 16 pin DIP

8T31 8-bit Bidirectional Port

- Schottky TTL technology
- Two independent bidirectional busses
- Eight bit latch register
- Independent read, write controls for each bus
- Bus A overrides if a write conflict occurs
- Register can be addressed as a memory location
- via Bus B Master Enable
- 30 ns maximum propagation delay
- Low input current: 500μA
- High fan out - sinks 20mA
- Standard 24 pin DIP

A typical processor configuration is shown in Figure 1. It should be remembered that in working with slice-oriented microprocessors, the final configuration may be varied to enhance speed, reduce component count, or increase data-processing capability. One method of maximizing a processor's performance is called pipelining. To accomplish this, a group of D-type flip-flops or latches (such as the 74174 Hex D-type Flip-Flop) are connected to the microprogram memory outputs (excluding the address control field AC_0 - AC_6) to buffer the current microinstruction

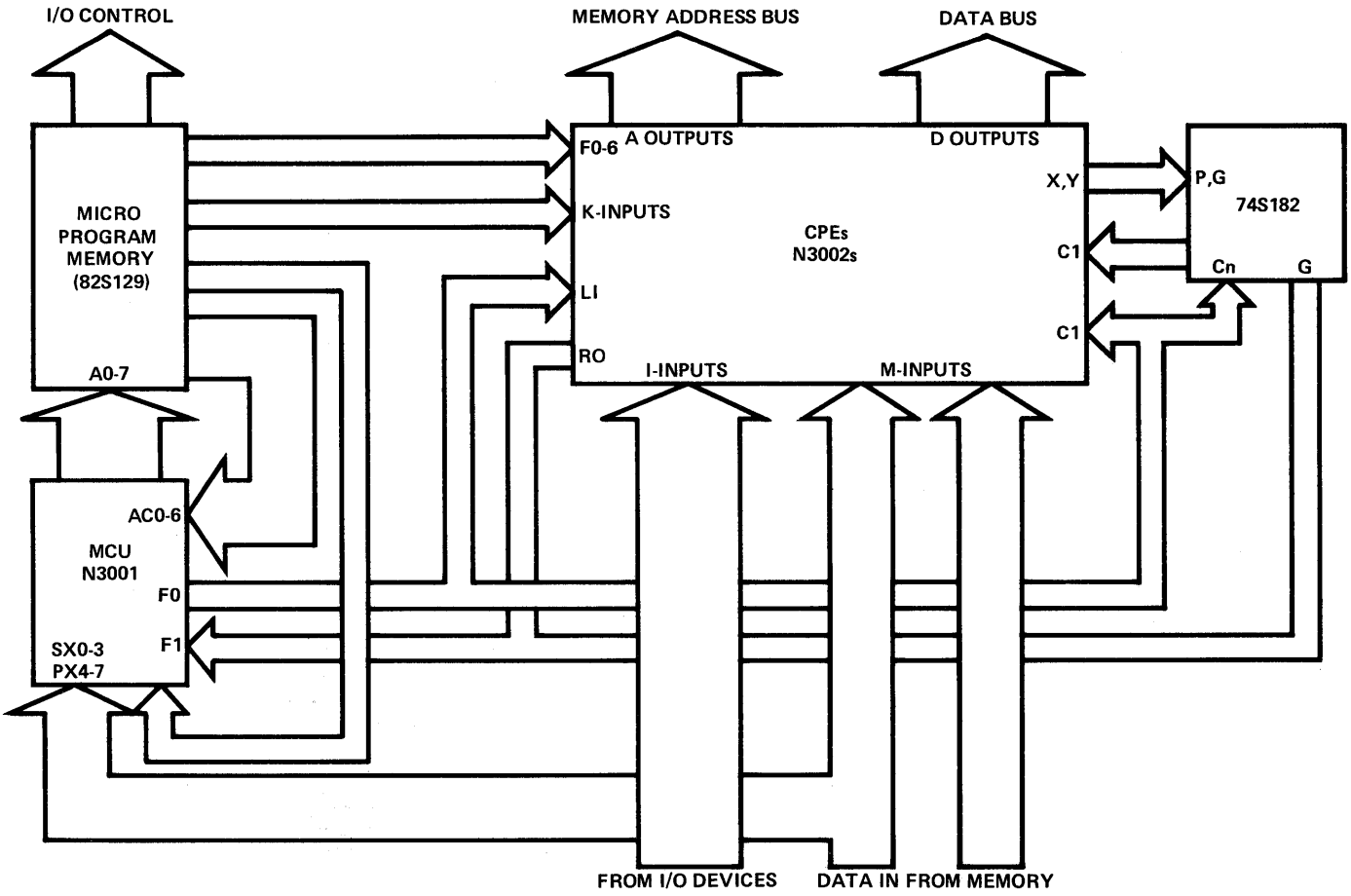


Figure 1: MICROCOMPUTER BLOCK DIAGRAM

and allow the MCU to overlap the fetch of the next instruction with the execution of the current one. The time saved in pipelining operations is the shorter of either the address set-up time to the microprogram memory (ROM/PROM) or the access time of the ROM/PROM. A convenient way of implementing pipelining is to use ROMs with on-board latches, such as the Signetics 82S115.

Figure 2 shows a typical microinstruction format using the 82S129 PROMs contained in the Signetics 3000 Microprocessor Designer's Evaluation Kit. Although this particular example is for a 40-bit word (10 PROMs), the allocation of bits for the mask (K-bus) and optional processor functions depands on the specific application of the system and the trade offs which the designer wishes to make.

In using the K-bus, it should be kept in mind that the K inputs are always ANDed with the B-multiplexer outputs into the ALU. Bit masking, frequently done in computer control systems, can be performed with the mask supplied to the K-bus directly from the microinstruction.

By placing the K-bus in either the all-one or all-zero condition (done with a single control bit in the microinstruction), the accumulator will either be selected or de-selected, respectively, in a given operation. This feature nearly doubles the amount of microfunctions in the CPE. A description of these various microfunctions can be found in the N3002 data sheet under the heading "FUNCTION DESCRIPTION" by referring to the K-bus conditions of all-ones (11) and all-zeros (00).

The MCU controls the sequence in which microinstructions are fetched from the microprogram memory (ROM/PROM). In its classical form, the MCU would use a next-address field in each microinstruction. However, the N3001 uses a modified classical approach in which the microinstruction field specifies conditional tests on the MCU bus inputs and registers. The next-address logic of the MCU also makes extensive use of a row/column addressing scheme, whereby the next address is defined by a 5-bit row address and 4-bit column address. Thus, from a particular address location, it is possible to jump unconditionally to any other location within that row or

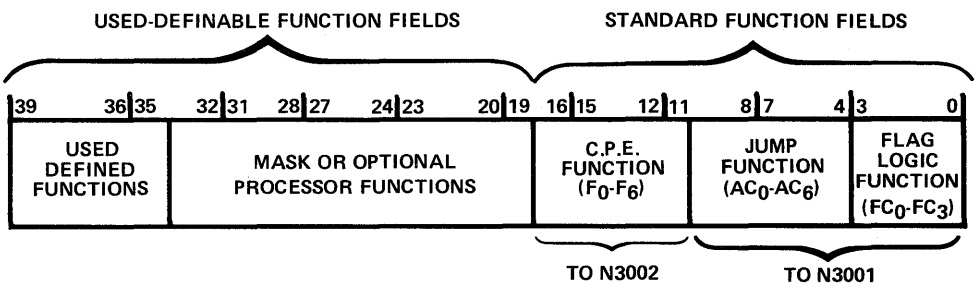


Figure 2: TYPICAL MICROINSTRUCTION FORMAT.

Note: The mask field need only be used during masking operations. At other times, it is entirely user definable.

column, or conditionally to other specified locations in one operation. Using this method, the processor functions can be executed in aprallel with program branches.

As an example of this flexibility, let us assume a disk controller is being designed. As part of the sequence logic, three bits of the disk drive status word must be tested and all three must be true in order to proceed with the particular sequencing operation. In any sequencing operation using a status word for conditional branch information, there are innumerable combinations of bits which must be tested throughout the sequencing operation. Using discrete logic techniques, this would involve several levels of gating.

However, the entire operation can be done in two microinstructions. First, the mask (K-bus) field in the microinstruction format is encoded with a one for each corresponding status bit to be tested and a zero for each bit to be discarded. The status word is input via the I-bus and ANDed with the K-bus mask using the CPE microfunction operation from F-Group 2, R-Group III. Assuming we are using low-true logic (TRUE = 0 Volts), we now test the result, which is located in the accumulator AC, for all zeros using the CPE microfunction operation from F-Group 5, R-Group III. Depending on the zero/non-zero status of AC, a one or zero will be loaded into the carryout CO bit. This bit can now be used as a condition for the next address jump calculation within the N3001 MCU. If the AC was zero (status word was true), we will jump to the next address within our controller sequence. If the AC was non-zero (status word not true), then a jump would be made back to the beginning of this two-microinstruction loop and the test sequence repeated until the status word (all three bits) is true.

Figure 3 shows a typical timing diagram for a system operating in the non-pipelined mode. Keep in mind that the maximum clock rate is dependent upon the total of propagation delay times plus required set-up times. It is at the designer's discretion to resolve the speed versus complexity tradeoffs.

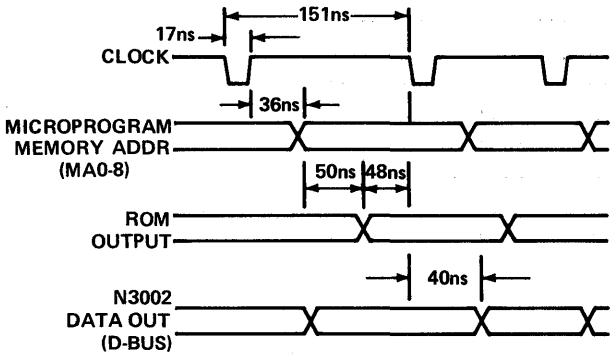


Figure 3: SYSTEM TIMING - NON-PIPELINED CONFIGURATION

PRELIMINARY INFORMATION

BIPOLAR MICROPROCESSOR

DESCRIPTION

The N3001 MCU is one element of a bipolar microcomputer set. When used with the 3002, 74S182, ROM or PROM memory, a powerful microprogrammed computer can be implemented.

The 3001 MCU controls the fetch sequence of micro-instructions from the microprogram memory. Functions performed by the 3001 include:

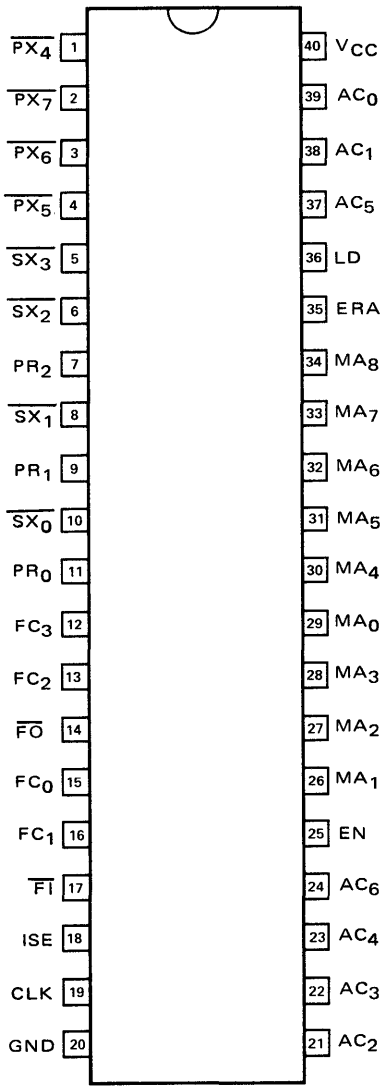
- Maintenance of microprogram address register
- Selection of next microinstruction address
- Decoding and testing of data supplied via several input busses
- Saving and testing of carry output data from the central processing (CP) array
- Control of carry/shift input data to the CP array
- Control of microprogram interrupts

FEATURES

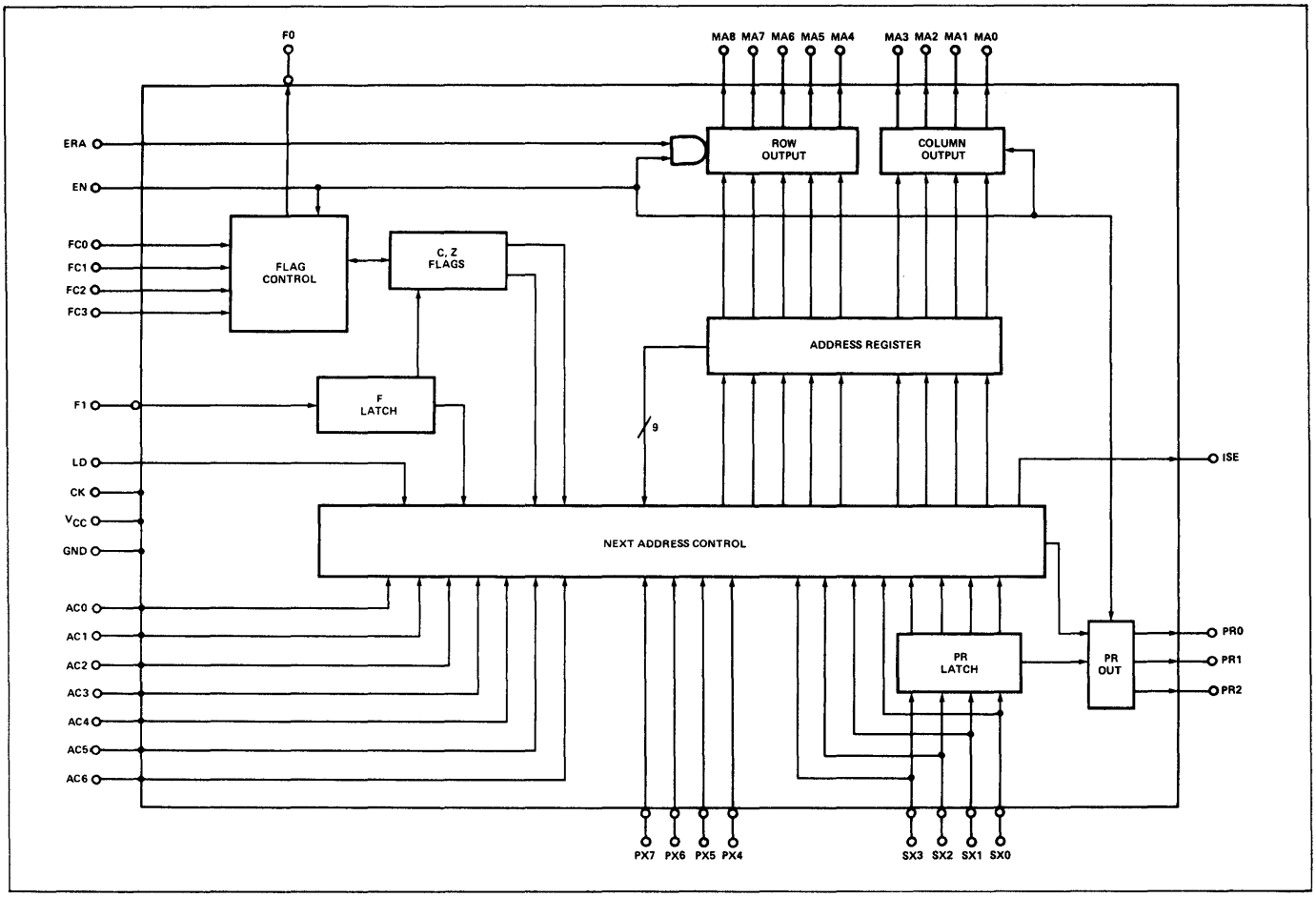
- SCHOTTKY TTL PROCESS
- 45ns CYCLE TIME (TYP.)
- DIRECT ADDRESSING OF STANDARD BIPOLAR PROM OR ROM
- 512 MICROINSTRUCTION ADDRESSIBILITY
- ADVANCED ORGANIZATION:
  - 9-BIT MICROPROGRAM ADDRESS REGISTER AND BUS ORGANIZED TO ADDRESS MEMORY BY ROW AND COLUMN
  - 4-BIT PROGRAM LATCH
  - 2 FLAG REGISTERS
- 11 ADDRESS CONTROL FUNCTIONS:
  - 3 JUMP AND TEST LATCH FUNCTION
  - 16 WAY JUMP AND TEST INSTRUCTION
- FLIGHT FLAG CONTROL FUNCTIONS:
  - 4 FLAG INPUT FUNCTIONS
  - 4 FLAG OUTPUT FUNCTIONS

PIN CONFIGURATION

I PACKAGE



N3001 BLOCK DIAGRAM



PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1–4	$\overline{PX_4}$–$\overline{PX_7}$	Primary Instruction Bus Inputs Data on the primary instruction bus is tested by the JPX function to determine the next microprogram address.	Active LOW
5, 6, 8, 10	$\overline{SX_0}$–$\overline{SX_3}$	Secondary Instruction Bus Inputs Data on the secondary instruction bus is synchronously loaded into the PR-latch while the date on the PX-bus is being tested (JPX). During a subsequent cycle, the contents of the PR-latch may be tested by the JPR, JLL, or JRL functions to determine the next microprogram address.	Active LOW
7, 9, 11	PR_0–PR_2	PR-Latch Outputs The PR-latch outputs are asynchronously enabled by the JCE function. They can be used to modify microinstructions at the outputs of the microprogram memory or to provide additional control lines.	Open Collector
12, 13, 15, 16	FC_0–FC_3	Flag Logic Control Inputs The flag logic control inputs are used to cross-switch the flags (C and Z) with the flag logic input (FI) and the flag logic output (FO).	Active HIGH
14	$\overline{FO}$	Flag Logic Output The outputs of the flags (C and Z) are multiplexed internally to form the common flag logic output. The output may also be forced to a logical O or logical 1.	Active LOW Three-state
17	$\overline{FI}$	Flag Logic Input The flag logic input is demultiplexed internally and applied to the inputs of the flags (C and Z). Note: The flag input data is saved in the F-latch when the clock input (CLK) is low.	Active LOW

PIN DESCRIPTION (Cont'd)

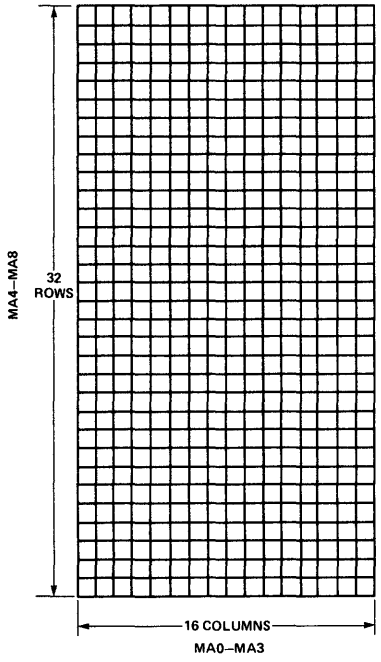
PIN	SYMBOL	NAME AND FUNCTION	TYPE
18	ISE	Interrupt Strobe Enable Output The interrupt strobe enable output goes to logical 1 when one of the JZR functions are selected (see Functional Description). It can be used to provide the strobe signal required by interrupt circuits.	Active HIGH
19	CLK	Clock Input	
20	GND	Ground	
21–24 37–39	AC_0–AC_6	Next Address Control Function Inputs All jump functions are selected by these control lines.	Active HIGH
25	EN	Enable Input When in the HIGH state, the enable input enables the microprogram address, PR-latch and flag outputs.	
26–29	MA_0–MA_3	Microprogram Column Address Outputs	Three-state
30–34	MA_4–MA_8	Microprogram Row Address Outputs	Three-state
35	ERA	Enable Row Address Input When in the LOW state, the enable row address input independently disables the microprogram row address outputs. It can be used to facilite the implementation of priority interrupt systems.	Active HIGH
36	LD	Microprogram Address Load Input When the active HIGH state, the microprogram address load input inhibits all jump functions and synchronously loads the date on the instructions busses into the microprogram register. However, it does not inhibit the operation of the PR-latch or the generation of the interrupt strobe enable.	Active HIGH
40	V_{CC}	+5 Volt Supply	

THEORY OF OPERATION

The MCU controls the sequence of microinstructions in the microprogram memory. The MCU simultaneously controls 2 flip-flops (C, Z) which are interactive with the carry-in and carry-out logic of an array of CPEs.

The functional control of the MCU provides both unconditional jumps to new memory locations and jumps which are dependent on the state of MCU flags or the state of the "PR" latch. Each instruction has a "jump set" associated with it. This "jump set" is the total group of memory locations which can be addressed by that instruction.

The MCU utilizes a two-dimensional addressing scheme in the microprogram memory. Microprogram memory is organized as 32 rows and 16 columns for a total of 512 words. Word length is variable according to application. Address is accomplished by a 9-bit address organized as row and column address.



ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Supply Voltages	7V
All Input Voltages	+5.5V
Output Currents	100mA

NOTE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
V_C	Input Clamp Voltage (All Input Pins)	V_{CC} = 4.75, I_C = −5mA		−0.8	−1.0	V
1_F	Input Load Current:	V_{CC} = 5.25V, V_F = 0.45V				
	CLK Input			−0.075	−0.75	mA
	EN Input			−0.05	−0.50	mA
	All Other Inputs			−0.025	−0.25	mA
1_R	Input Leakage Current:	V_{CC} = 5.25V, V_R = 5.25V				
	CLK				120	μA
	EN Input				80	μA
	All Other Inputs				40	μA
V_{IL}	Input Low Voltage	V_{CC} = 5.0V			0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{CC}	Power Supply Current	V_{CC} = 5.25V[2]		170	240	mA
V_{OL}	Output Low Voltage (All Output Pins)	V_{CC} = 4.75V, I_{OL} = 10mA		0.35	0.45	V
V_{OH}	Output High Voltage (MA_0–MA_8, ISE, FO)	V_{CC} = 4.75V, I_{OH} = −1mA	2.4	3.0		V
I_{os}	Output Short Circuit Current (MA_0–MA_8, ISE, FO)	V_{CC} = 5.0V	−15	−28	−60	mA
$I_{o\ (off)}$	Off-State Output Current:					
	PR_0–PR_2, MA_0–MA_2, FO	V_{CC} = 5.25V, V_o = 0.45V			−100	μA
	MA_0–MA_8, FO	V_{CC} = 5.25V, V_o = 5.25V			−100	μA

NOTES:
1. Typical values are for T_A = 25°C and 5.0 supply voltage.
2. EN input grounded, all other inputs and outputs open.

FUNCTIONAL DESCRIPTION

The following is a description of each of the eleven address control functions. The symbols shown below are used to specify row and column addresses.

SYMBOL	MEANING
row_n	5-bit next row address where n is the decimal row address.
col_n	4-bit next column address where n is the decimal column address.

UNCONDITIONAL ADDRESS CONTROL (JUMP) FUNCTIONS

The jump functions use the current microprogram address (i.e., the contents of the microprogram address register prior to the rising edge of the clock) and several bits from the address control inputs to generate the next microprogram address.

MNEMONIC	FUNCTION DESCRIPTION
JCC	Jump in current column. AC_0–AC_4 are used to select 1 of 32 row addresses in the current column, specified by MA_0–MA_3, as the next address.
JZR	Jump to zero row. AC_0–AC_3 are used to select 1 of 16 column addresses in row_0, as the next address.
JCR	Jump in current row. AC_0–AC_3 are used to select 1 of 16 addresses in the current row, specified by MA_4–MA_8, as the next address.
JCE	Jump in current column/row group and enable PR-latch outputs, AC_0–AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7–MA_8, as the next row address. The current column is specified by MA_0–MA_3. The PR-latch outputs are asynchronously enabled.

FLAG CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The jump/test flag functions use the current microprogram address, the contents of the selected flag or latch, and several bits from the address control function to generate the next microprogram address.

MNEMONIC	FUNCTION DESCRIPTION
JFL	Jump/test F-latch. AC_0–AC_3 are used to select 1 of 16 row addresses in the current row group, specified by MA_8, as the next row address. If the current column group, specified by MA_3, is col_0–col_7, the F-latch is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8–col_{15}, the F-latch is used to select col_{10} or col_{11} as the next column address.
JCF	Jump/test C-flag. AC_0–AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. If the current column group specified by MA_8 is col_0–col_7, the C-flag is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8–col_{15}, the C-flag is used to select col_{10} or col_{11} as the next column address.
JZF	Jump/test Z-flag. Identical to the JCF function described above, except that the Z-flag, rather than the C-flag, is used to select the next column address.

PX-BUS AND PR-LATCH CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The PX-bus jump/test function uses the data on the primary instruction bus (PX_4–PX_7), the current microprogram address, and several selection bits from the address control function to generate the next microprogram address. The PR-latch jump/test functions use the data held in the PR-latch, the current microprogram address, and several selection bits from the address control function to generate the next microprogram address.

MNEMONIC	FUNCTION DESCRIPTION
JPR	Jump/test PR-latch. AC_0–AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. The four PR-latch bits are used to select 1 of 16 possible column addresses as the next column address.
JLL	Jump/test leftmost PR-latch bits. AC_0–AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_2 and PR_3 are used to column addresses in col_4 through col_7 as the next column address.
JRL	Jump/test rightmost PR-latch bits. AC_0 and AC_1 are used to select 1 of 4 high-order row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_0 and PR_1 are used to select 1 of 4 possible column addresses in col_{12} through col_{15} as the next column address.
JPX	Jump/test PX-bus and load PR-latch. AC_0 and AC_1 are used to select 1 of 4 row addresses in the current row group, specified by MA_6–MA_8, as the next row address. PX_4–PX_7 are used to select 1 of 16 possible column addresses as the next column address. SX_0–SX_3 data is locked in the PR-latch at the rising edge of the clock.

PX-BUS AND PR-LATCH CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS (Continued)

The flag control functions of the MCU are selected by the four input lines designated FC_0–FC_3. Function code formats are given in "Flag Control Function summary".

The following is a detailed description of each of the eight flag control functions.

FLAG INPUT CONTROL FUNCTIONS

The flag input control functions select which flag or flags will be set to the current value of the flag input (FI) line. Data on FI is stored in the F-latch when the clock is low. The content of the F-latch is loaded into the C and/or Z flag on the rising edge of the clock.

MNEMONIC	FUNCTION DESCRIPTION
SCZ	Set C-flag and Z-flag to FI. The C-flag and the Z-flag are both set to the value of FI.
STZ	Set Z-flag to FI. The Z-flag is set to the value of FI. The C-flag is unaffected.
STC	Set C-flag to FI. The C-flag is set to the value of FI. The Z-flag is unaffected.
HCZ	Hold C-flag and Z-flag. The values in the C-flag and Z-flag are unaffected.

FLAG OUTPUT CONTROL FUNCTIONS

The flag output control functions select the value to which the flag output (FO) line will be forced.

MNEMONIC	FUNCTION DESCRIPTION
FFO	Force FO to O. FO is forced to the value of logical O.
FFC	Force FO to C. FO is forced to the value of the C-flag.
FFZ	Force FO to Z. FO is forced to the value of the Z-flag.
FF1	Force FO to 1. FO is forced to the value of logical 1.

STROBE FUNCTIONS

The load function of the MCU is controlled by the input line designated LD. If the LD line is active HIGH at the rising edge of the clock, the date on the primary and secondary instruction busses, PX_4–PX_7 and SX_0–SX_3, is loaded into the microprogram address register. PX_4–PX_7 are loaded into MA_0–MA_3 and SX_0–SX_3 are loaded into MA_4–MA_7. The high-order bit of the microprogram address register MA_8 is set to a logical 0. The bits from the primary instruction bus select 1 of 16 possible column addresses. Likewise, the bits from the secondary instruction bus select 1 of the first 16 row addresses.

The MCU generates an interrupt strobe enable on the output line designated ISE. The line is placed in the active high state whenever a JZR to col_{15} is selected as the address control function. Generally, the start of a macroinstruction fetch sequence is situated at row_0 and col_{15} so the interrupt control may be enabled at the beginning of

ADDRESS CONTROL FUNCTION SUMMARY

MNEMONIC	DESCRIPTION	FUNCTION							NEXT ROW					NEXT COL				
		AC_6	5	4	3	2	1	0	MA_8	7	6	5	4	MA_3	2	1	0
JCC	Jump in current column	0	0	d_4	d_3	d_2	d_1	d_0	d_4	d_3	d_2	d_1	d_0	m_3	m_2	m_1	m_0
JZR	Jump to zero row	0	1	0	d_3	d_2	d_1	d_0	0	0	0	0	0	d_3	d_2	d_1	d_0
JCR	Jump in current row	0	1	1	d_3	d_2	d_1	d_0	m_8	m_7	m_6	m_5	m_4	d_3	d_2	d_1	d_0
JCE	Jump in column/enable	1	1	1	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	m_2	m_1	m_0
JFL	Jump/test F-latch	1	0	0	d_3	d_2	d_1	d_0	m_8	d_3	d_2	d_1	d_0	m_3	0	1	f
JCF	Jump/test C-flag	1	0	1	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	c
JZF	Jump/test Z-flag	1	0	1	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	z
JPR	Jump/test PR-latch	1	1	0	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	p_3	p_2	p_1	p_0
JLL	Jump/test left PR bits	1	1	0	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	0	1	p_3	p_2
JRL	Jump/test right PR bits	1	1	1	1	1	d_1	d_0	m_8	m_7	1	d_1	d_0	1	1	p_1	p_0
JPX	Jump/test PX-bus	1	1	1	1	0	d_1	d_0	m_8	m_7	m_6	d_1	d_0	x_7	x_6	x_5	x_4

NOTE:
d_n = Data pm address control line n
m_n = Data in microprogram address register bit n
p_n = Data in PR-latch bit n
x_n = Data on PX-bus line n (active LOW)
f, c, z = Contents of F-latch, C-flag, or Z-flag, respectively

STROBE FUNCTIONS Cont'd.

the fetch/execute cycle. The interrupt control responds to the interrupt by pulling the enable row address (ERA) input line low to override the selected next row address from the MCU. Then by gating an alternative next row address on to the row address lines of the microprogram memory, the microprogram may be forced to enter an interrupt handling routine. The alternative row address placed on the microprogram memory address lines does not alter the contents of the microprogram address register. Therefore, subsequent jump functions will utilize the row address in the register, and not the alternative row address, to determine the next microprogram address.

Note, the load function always overrides the address control function on AC_0–AC_6. It does not, however, override the latch enable or load sub-functions of the JCE or JPX instruction, respectively. In addition, it does not inhibit the interrupt strobe enable or any of the flag control functions.

FLAG CONTROL FUNCTION SUMMARY

TYPE	MNEMONIC	DESCRIPTION	FC_1	0
Flag Input	SCZ	Set C-flag and Z-flag to f	0	0
	STZ	Set Z-flag to f	0	1
	STC	Set C-flag to f	1	0
	HCZ	Hold C-flag and Z-flag	1	1

TYPE	MNEMONIC	DESCRIPTION	FC_3	2
Flag Output	FF0	Force FO to 0	0	0
	FFC	Force FO to C-flag	0	1
	FFZ	Force FO to Z-flag	1	0
	FF1	Force FO to 1	1	1

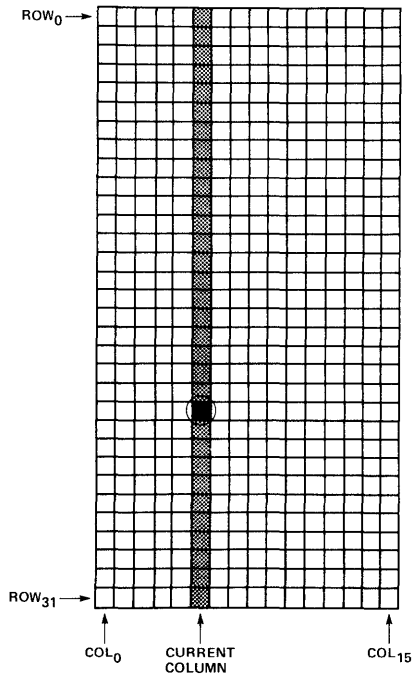
LOAD FUNCTION	NEXT ROW					NEXT COL				
LD	MA_8	7	6	5	4	MA_3	2	1	0
0	See Appendix A					See Appendix A				
1	0	x_3	x_2	x_1	x_0	x_7	x_6	x_5	x_4	

NOTE:
f = Contents of the F-latch
x_n = Data on PX- or SX-bus line n (active LOW)

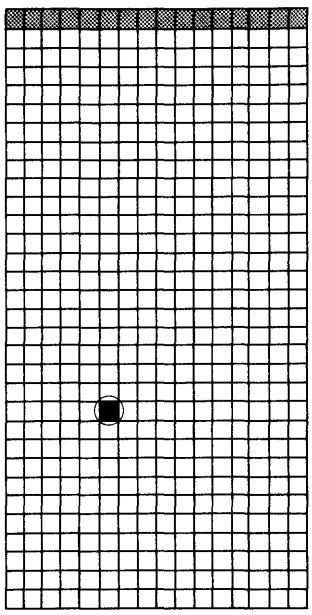
JUMP SET DIAGRAMS

The following ten diagrams illustrate the jump set for each of the eleven jump and jump/test functions of the MCU. Location 341 indicated by the circled square, represents one current row (row_{21}) and current column (col_5) address. The dark boxes indicate the microprogram locations that may be selected by the particular function as the next address.

JCC
JUMP IN CURRENT COLUMN

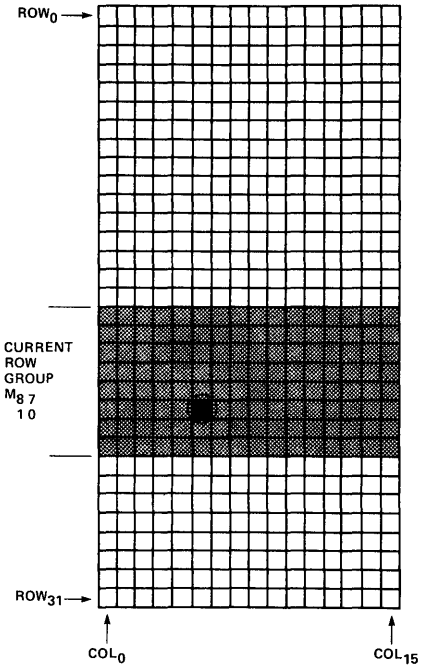


JZR
JUMP TO ZERO ROW

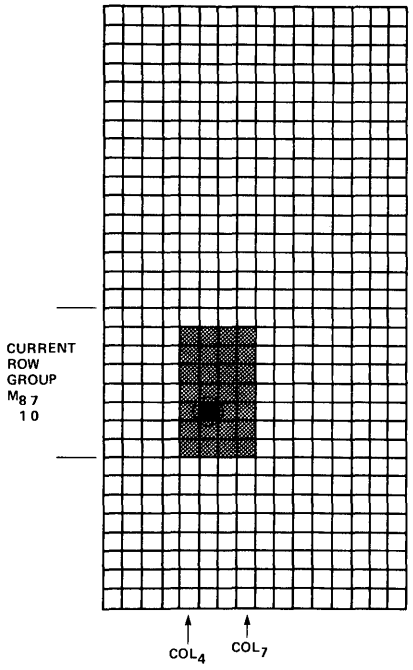


JUMP SET DIAGRAMS Cont'd.

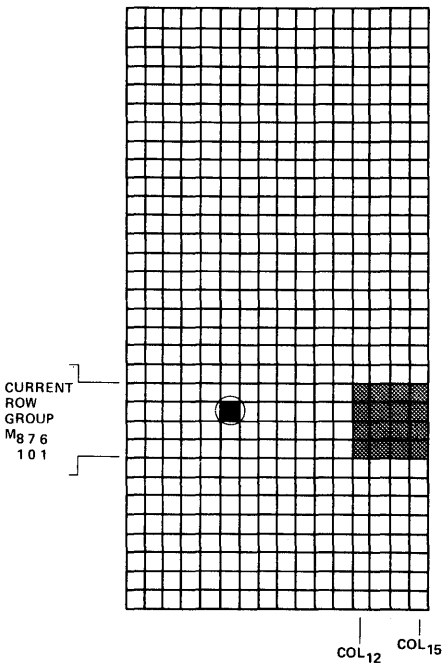
JPR
JUMP/TEST PR-LATCH



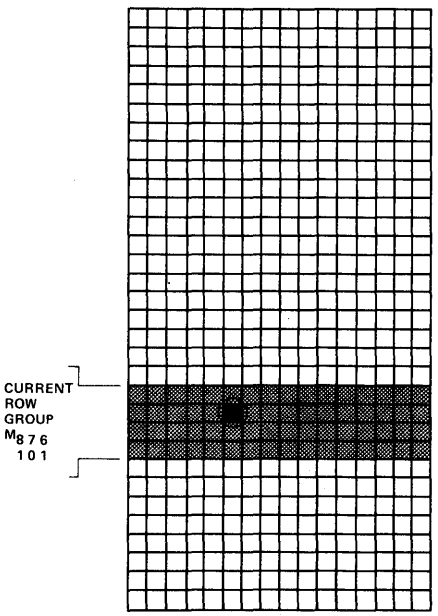
JLL
JUMP/TEST LEFT LATCH



JRL
JUMP/TEST RIGHT LATCH

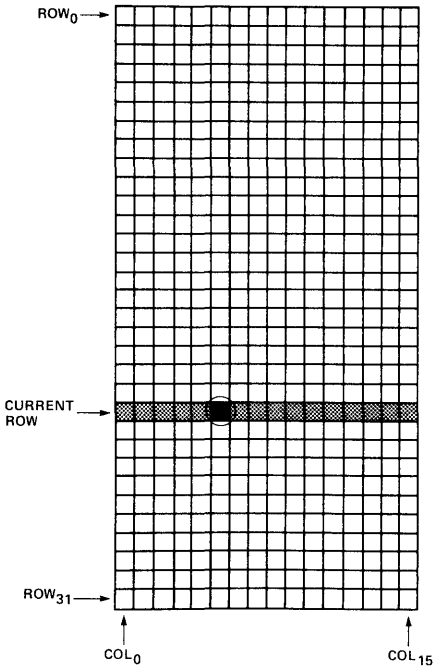


JPX
JUMP/TEST PX-BUS

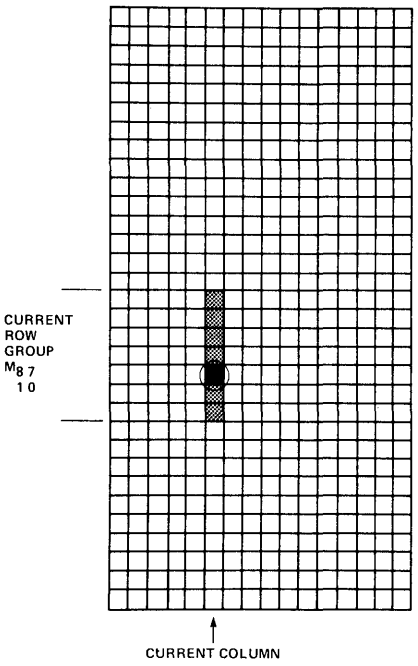


JUMP SET DIAGRAMS Cont'd.

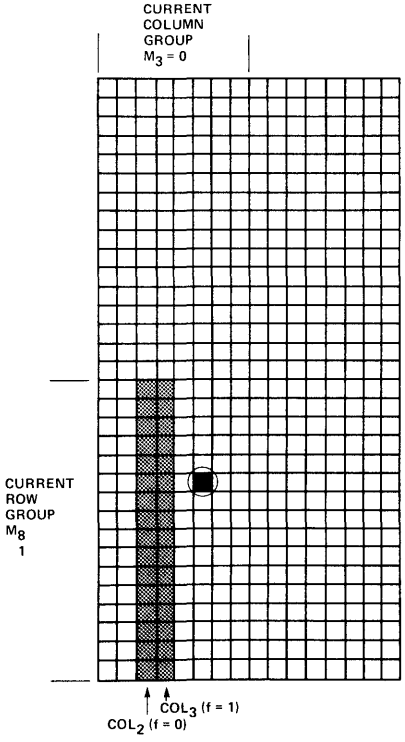
JCR
JUMP IN CURRENT ROW



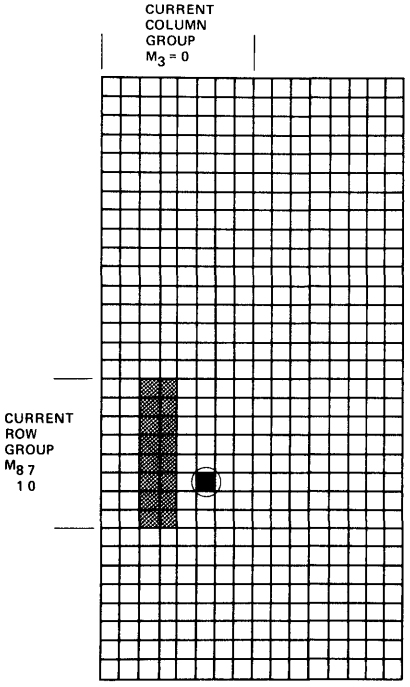
JCE
JUMP COLUMN/ENABLE



JFL
JUMP/TEST F-LATCH



JCF, JZF
JUMP/TEST C-FLAG
JUMP/TEST Z-FLAG



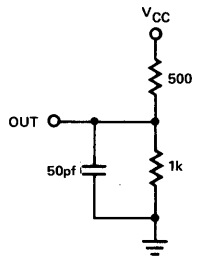
AC ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5.0V + 5%

	PARAMETER	LIMITS			UNIT
		MIN	TYP[1]	MAX	
t_{CY}	Cycle Time	60	45		ns
t_{WP}	Clock Pulse Width	17	10		ns
	Control and Data Input Set-Up Times:				
t_{SF}	LD, AC_0–AC_6	7	0		ns
t_{SK}	FC_0, FC_1	7	0		ns
t_{SX}	SX_0–SX_3, PX_4–PX_7	28	20		ns
t_{SI}	FI	12	0		ns
	Control and Data Input Hold Times:				
t_{HF}	LD, AC_0–AC_6	4	0		ns
t_{HK}	FC_0, FC_1	4	0		ns
t_{HX}	SX_0–SX_3, PX_4–PX_7	16	0		ns
t_{HI}	FI	16	6		ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (MA_0–MA_8, FO)		24	36	ns
t_{KO}	Propagation Delay from Control Inputs FC_2 and FC_3 to Flag Out (FO)		13	24	ns
t_{FO}	Propagation Delay from Control Inputs AC_0–AC_6 to Latch Outputs (PR_0–PR_2)		21	32	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (MA_0–MA_8, FO, PR_0–PR_2)		17	26	ns
t_{FI}	Propagation Delay from Control Inputs AC_0–AC_6 to Interrupt Strobe Enable Output (ISE)		19	32	ns

NOTE:
1. Typical values are for T_A = 25°C and 5.0 supply voltage.

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

TEST CONDITIONS

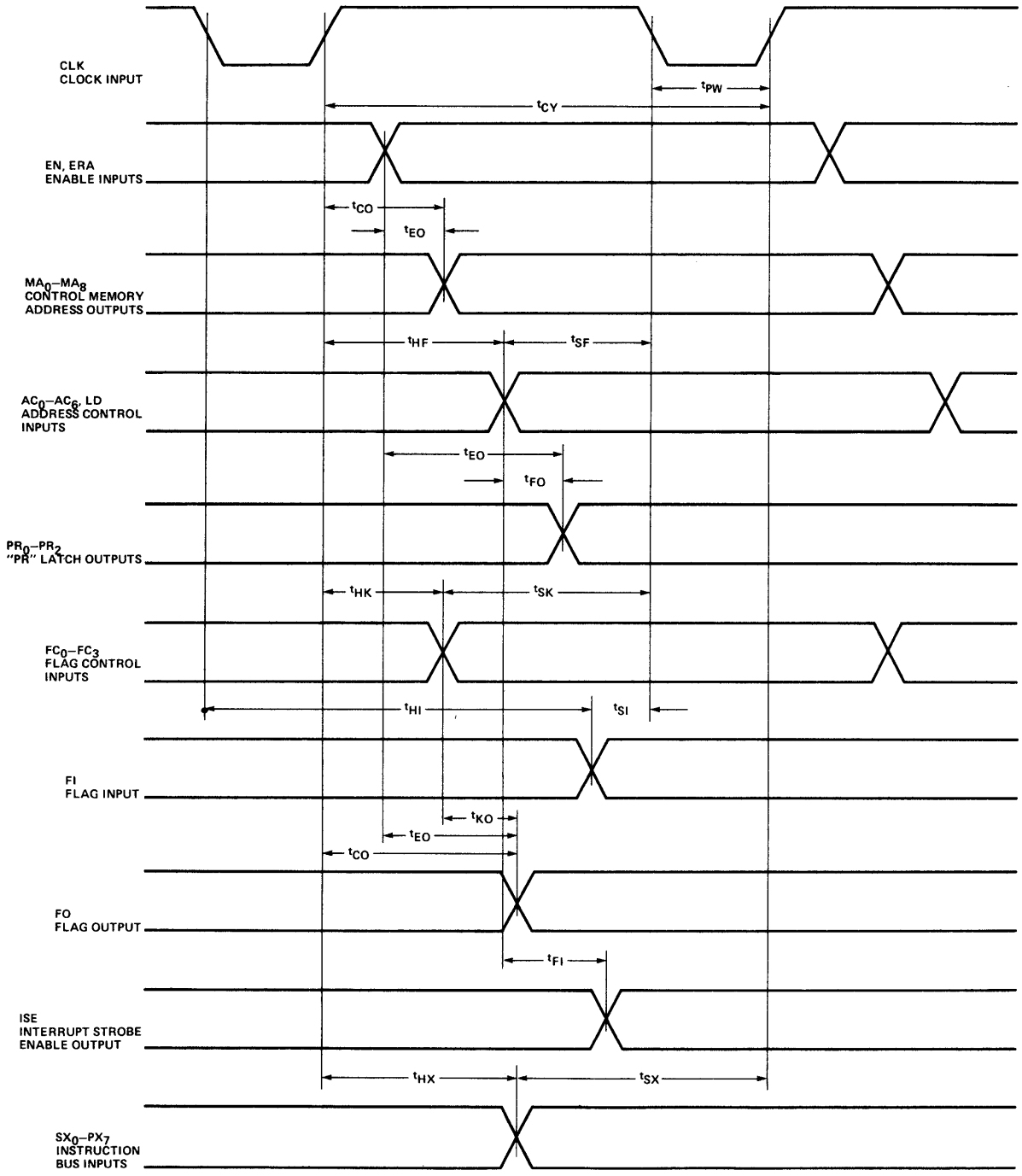
Input pulse amplitude of 2.5 volts.

Input rise and fall times of 5ns between 1 volt and 2 volts.

Output load of 10mA and 50pF.

Speed measurements are taken at the 1.5 volt level.

VOLTAGE WAVEFORMS



PRELIMINARY

BIPOLAR MICROPROCESSOR

DESCRIPTION

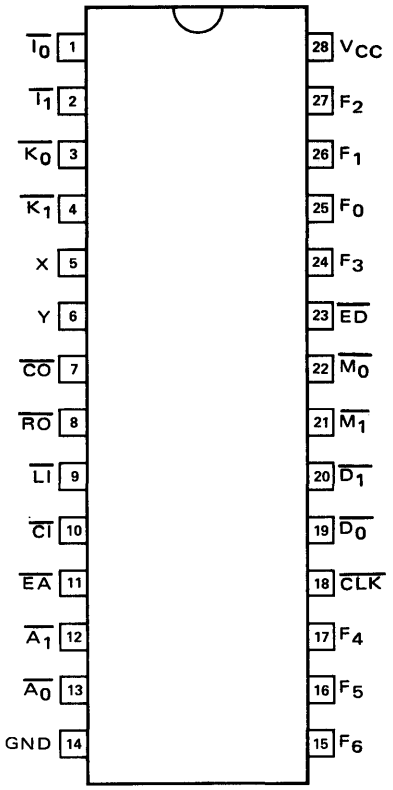
The N3002 Central Processing Element (CPE) is one part of a bipolar microcomputer set. The N3002 is organized as a 2-bit slice and performs the logical and arithmetic functions required by micro - instructions. A system with any number of bits in a data word can be implemented by using multiple N3002s, the N3001 microcomputer control unit, the N74S182 carry look-ahead unit and ROM or PROM memory.

FEATURES

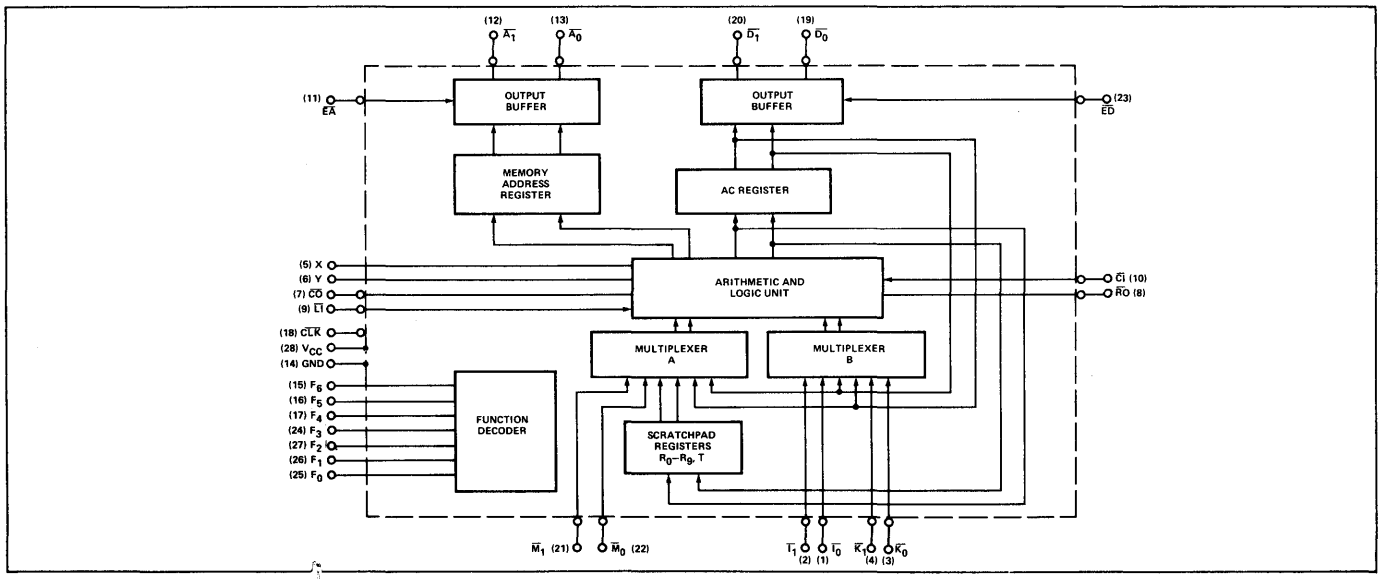
- 45ns CYCLE TIME (TYP.)
- EASY EXPANSION TO MULTIPLE OF 2 BITS
- 11 GENERAL PURPOSE REGISTERS
- FULL FUNCTION ACCUMULATOR
- USEFUL FUNCTIONS INCLUDE:
  - 2's COMPLEMENT ARITHMETIC
  - LOGICAL AND, OR, NOT, EXCLUSIVE-NOR
  - INCREMENT, DECREMENT
  - SHIFT LEFT/SHIFT RIGHT
  - BIT TESTING AND ZERO DETECTION
  - CARRY LOOK-AHEAD GENERATION
  - MASKING VIA K-BUS
  - CONDITIONED CLOCKING ALLOWING NON-DESTRUCTIVE TESTING OF DATA IN ACCUMULATOR AND SCRATCHPAD
- 3 INPUT BUSSES
- 2 OUTPUT BUSSES
- CONTROL BUS

PIN CONFIGURATION

I PACKAGE



BLOCK DIAGRAM



PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1, 2	I_0–I_1	External Bus Inputs The external bus inputs provide a separate input port for external input devices.	Active LOW
3, 4	K_0–K_1	Mask Bus Inputs The mask bus inputs provide a separate input port for the microprogram memory, to allow mask or constant entry.	Active LOW
5, 6	X, Y	Standard Carry Look-Ahead Cascade Outputs The cascade outputs allow high speed arithmetic operations to be performed when they are used in conjunction with the 74S182 Look-Ahead Carry Generator.	Active HIGH
7	CO	Ripple Carry Output The ripple carry output is only disabled during shift right operations.	Active LOW Three-state
8	RO	Shift Right Output The shift right output is only enabled during shift right operations.	Active LOW Three-state
9	LI	Shift Right Input	Active LOW
10	CI	Carry Input	Active LOW
11	EA	Memory Address Enable Input When in the LOW state, the memory address enable input enables the memory address outputs (A_0–A_1).	Active LOW
12–13	A_0–A_1	Memory Address Bus Outputs The memory address bus outputs are the buffered outputs of the memory address register (MAR).	Active LOW Three-state
14	GND	Ground	
15–17, 24–27	F_0–F_6	Micro-Function Bus Inputs The micro-function bus inputs control ALU function and register selection.	Active-HIGH
18	CLK	Clock Input	
19–20	D_0–D_1	Memory Data Bus Outputs The memory data bus outputs are the buffered outputs of the full function accumulator register (AC).	Active LOW Three-state
21–22	M_0–M_1	Memory Data Bus Inputs The memory data bus inputs provide a separate input port for memory data.	Active LOW
23	ED	Memory Data Enable Input When in the LOW state, the memory data enable input enables the memory data outputs (D_0–D_1).	Active LOW
28	V_{CC}	+5 Volt Supply	

SYSTEM DESCRIPTION

1. MICROFUNCTION DECODER AND K-BUS

Basic microfunctions are controlled by a 7-bit bus (F_0–F_6) which is organized into two groups. The higher 3 bits (F_4–F_6) are designated as F-Group and the lower 4 bits (F_0–F_3) are designated as the R-Group. The F-Group specifies the type of operation to be performed and the R-Group specifies the registers involved.

SYSTEM DESCRIPTION (Continued)

The F-Bus instructs the microfunction decoder to:

- Select ALU functions to be performed
- Generate scratchpad register address
- Control A and B multiplexer

The resulting microfunction action can be:

- Data transfer
- Shift operations
- Increment and decrement
- Initialize stack
- Test for zero conditions
- 2's complement addition and subtraction
- Bit masking
- Maintain program counter

2. A AND B MULTIPLEXERS

A and B multiplexers select the proper two operands to the ALU.

A multiplexer selects inputs from one of the following:

- M-bus (data from main memory)
- Scratchpad registers
- Accumulator

B multiplexer selects inputs from one of the following:

- I-bus (data from external I/O devices)
- Accumulator
- K-bus (literal or masking information from micro-program memory)

3. SCRATCHPAD REGISTERS

- Contains 11 registers (R_0–R_9, T)
- Scratchpad register outputs are multiplexed to the ALU via the A multiplexer
- Used to store intermediate results from arithmetic/logic operations
- Can be used as program counter

4. ARITHMETIC/LOGIC UNIT (ALU)

The ALU performs the arithmetic and logic operations of the CPE.

Arithmetic operations are:

- 2's complement addition
- Incrementing
- Decrementing
- Shift left
- Shift right

Logical operations are:

- Transfer
- AND
- Inclusive-OR
- Exclusive-OR
- Logic complement

ALU operation results are then stored in the accumulator and/or scratchpad registers. For easy expansion to larger arrays, carry look-ahead outputs (X and Y) and cascading shift inputs (LI, Ro) are provided.

5. ACCUMULATOR

- Stores results from ALU operations
- The output of accumulator is multiplexed into ALU via the A and B multiplexer as one of the operands

6. INPUT BUSES

M-bus Data bus from main memory

- Accepts 2 bits of data from main memory into CPE
- Is multiplexed into the ALU via the A multiplexer

I-bus Data bus from input/output devices

- Accepts 2 bits of data from external input/output devices into CPE
- Is multiplexed into the ALU via the B multiplexer

K-bus A special feature of the N3002 CPE

- During arithmetic operations, the K-bus can be used to mask portions of the field being operated on
- Select or remove accumulator from operation by placing K-bus in all "1" or all "0" state respectively
- During non-arithmetic operation, the carry circuit can be used in conjunction with the K-bus for word-wise-OR operation for bit testing
- Supply literal or constant data to CPE

7. OUTPUT BUSES

A-bus and Memory Address Register

- Main memory address is stored in the memory address register (MAR)
- Main memory is addressed via the A-bus
- MAR and A-bus may also be used to generate device address when executing I/O instructions
- A-bus has Tri-State outputs

D-bus Data bus from CPE to main memory or to I/O devices

- Sends buffered accumulator outputs to main memory or the external I/O devices
- D-bus has Tri-State outputs

FUNCTION DESCRIPTION

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
0	I	XX	–	$R_n + (AC \wedge K) + CI \rightarrow R_n, AC$	**Logically AND AC with the K-bus.** Add the result to R_n and carry input (CI). Deposit the sum in AC and R_n.
		OO	ILR	$R_n + CI \rightarrow R_n, AC$	Conditionally increment R_n and load the result in AC. Used to load AC from R_n or to increment R_n and load a copy of the result in AC.
		II	ALR	$AC + R_n + CI \rightarrow R_n, AC$	Add AC and CI to R_n and load the result in AC. Used to add AC to a register. If R_n is AC, then AC is shifted left one bit position.
0	II	XX	–	$M + (AC \wedge K) + CI \rightarrow AT$	**Logically AND AC with the K-bus.** Add the result to CI and the M-bus. Deposit the sum in AC or T.
		OO	ACM	$M + CI \rightarrow AT$	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		II	AMA	$M + AC + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.
0	III	XX	–	$AT_L \wedge \overline{(I_L \wedge K_L)} \rightarrow RO$ $LI \vee [(I_H \wedge K_H) \wedge AT_H] \rightarrow AT_H$ $[AT_L \wedge (I_L \wedge K_L)] \vee [AT_H \vee (I_H \wedge K_H)] \rightarrow AT_L$	None
		OO	SRA	$AT_L \rightarrow RO$ $AT_H \rightarrow AT_L$ $LI \rightarrow AT_H$	Shift AC or T, as specified, right one bit position. Place the previous low order bit value on RO and fill the high order bit from the data on LI. Used to shift or rotate AC or T right one bit.
1	I	XX	–	$K \vee R_n \rightarrow MAR$ $R_n + K + CI \rightarrow R_n$	**Logically OR R_n with the K-bus.** Deposit the result in MAR. Add the K-bus to R_n and CI. Deposit the result in R_n.
		OO	LMI	$R_n \rightarrow MAR$ $R_n + CI \rightarrow R_n$	Load MAR from R_n. Conditionally increment R_n. Used to maintain a macro-instruction program counter.
		II	DSM	$11 \rightarrow MAR$ $R_n - 1 + CI \rightarrow R_n$	Set MAR to all one's. Conditionally decrement R_n by one. Used to force MAR to its highest address and to decrement R_n.

F GROUP	R GROUP	K BUS	NAME	EQUATION	
1	II	XX	–	$K \vee M \rightarrow MAR$ $M + K + CI \rightarrow AT$	**Logically OR the M-bus with the K-bus.** Deposit the result in MAR. Add the K-bus to the M-bus and CI. Deposit the sum in AC or T.
		OO	LMM	$M \rightarrow MAR$ $M + CI \rightarrow AT$	Load MAR from the M-bus. Add CI to the M-bus. Deposit the result in AC or T. Used to load the address register with memory data for macro-instructions using indirect addressing.
		II	LDM	$11 \rightarrow MAR$ $M - 1 + CI \rightarrow AT$	Set MAR to all ones. Subtract one from the M-bus. Add CI to the difference and deposit the result in AC or T, as specified. Used to load decremented memory data in AC or T.
1	III	XX	–	$(\overline{AT} \vee K) + (AT \wedge K) + CI \rightarrow AT$	**Logically OR the K-bus with the complement of AC or T, as specified.** Add the result to the logical AND of specified register with the K-bus. Add the sum to CI. Deposit the result in the specified register.
		OO	CIA	$\overline{AT} + CI \rightarrow AT$	Add CI to the complement of AC or T, as specified. Deposit the result in the specified register. Used to form the 1's or 2's complement of AC or T.
		II	DCA	$AT - 1 + CI \rightarrow AT$	Subtract one from AC or T, as specified. Add CI to the difference and deposit the sum in the specified register. Used to decrement AC or T.
2	I	XX	–	$(AC \wedge K) - 1 + CI \rightarrow R_n$ **(See Note 1)**	**Logically AND the K-bus with AC.** Subtract one from the result and add the difference to CI. Deposit the sum in R_n.
		OO	CSR	$CI - 1 \rightarrow R_n$ **(See Note 1)**	Subtract one from CI and deposit the difference in R_n. Used to conditionally clear or set R_n to all 0's or 1's, respectively.
		II	SDR	$AC - 1 + CI \rightarrow R_n$ **(See Note 1)**	Subtract one from AC and add the difference to CI. Deposit the sum in R_n. Used to store AC in R_n or to store the decremented value of AC in R_n.
2	II	XX	–	$(AC \wedge K) - 1 + CI \rightarrow AT$ **(See Note 1)**	**Logically AND the K-bus with AC.** Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CSA	$CI - 1 \rightarrow AT$ **(See Note 1)**	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		II	SDA	$AC - 1 + CI \rightarrow AT$ **(See Note 1)**	Subtract one from AC and add the difference to CI. Deposit the sum in AC or T. Used to store AC in T, or decrement AC, or store the decremented value of AC in T.

FUNCTION DESCRIPTION (CONT'D)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
2	III	XX	–	(I ∧ K) – 1 + CI → AT (See Note 1)	**Logically AND the data of the K-bus with the data on the I-bus.** Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CAS	CI –1 → AT	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		II	LDI	I – 1 + CI → AT	Subtract one from the data on the I-bus and add the difference to CI. Deposit the sum in AC or T, as specified. Used to load input bus data or decremented input bus data in the specified register.
3	I	XX	–	R_n + (AC ∧ K) + CI → R_n	**Logically AND AC with the K-bus.** Add R_n and CI to the result. Deposit the sum in R_n.
		OO	INR	R_n + CI → R_n	Add CI to R_n and deposit the sum in R_n. Used to increment R_n.
		II	ADR	AC + R_n + CI → R_n	Add AC to R_n. Add the result to CI and deposit the sum in R_n. Used to add the accumulator to a register or to add the incremented value of the accumulator to a register.
3	II	XX	–	M + (AC ∧ K) + CI → AT	**Logically AND AC with the K-bus.** Add the result to CI and the M-bus Deposit the sum in AC or T.
		OO	ACM	M + CI → AT	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		II	AMA	M + AC + CI → AT	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.
3	III	XX	–	AT + (I ∧ K) + CI → AT	**Logically AND the K-bus with the I-bus.** Add CI and the contents of AC or T, as specified, to the result. Deposit the sum in the specified register.
		OO	INA	AT + CI → AT	Conditionally increment AC or T. Used to increment AC or T.
		II	AIA	I + AT + CI → AT	Add the I-bus to AC or T. Add CI to the result and deposit the sum in the specified register. Used to add input data or incremented input data to the specified register.

FUNCTION TRUTH TABLE

FUNCTION GROUP	F_6	F_5	F_4
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

REGISTER GROUP	REGISTER	F_3	F_2	F_1	F_0
I	R_0	0	0	0	0
	R_1	0	0	0	1
	R_2	0	0	1	0
	R_3	0	0	1	1
	R_4	0	1	0	0
	R_5	0	1	0	1
	R_6	0	1	1	0
	R_7	0	1	1	1
	R_8	1	0	0	0
	R_9	1	0	0	1
	T	1	1	0	0
	AC	1	1	0	1
II	T	1	0	1	0
	AC	1	0	1	1
III	T	1	1	1	0
	AC	1	1	1	1

SYMBOL	MEANING
I, K, M	Data on the I, K, and M busses, respectively
CI, LI	Data on the carry input and left input, respectively
CO, RO	Data on the carry output and right output, respectively
R_n	Contents of register n including T and AC (R-Group I)
AC	Contents of the accumulator
AT	Contents of AC or T, as specified
MAR	Contents of the memory address register
L, H	As subscripts, designate low and high order bit, respectively
+	2's complement addition
–	2's complement subtraction
∧	Logical AND
∨	Logical OR
$\overline{\oplus}$	Exclusive-NOR
→	Deposit into

NOTE:
1. 2's complement arithmetic adds 111 . . . 11 to perform subtraction of 000 . . . 01.

FUNCTION DESCRIPTION (CONT'D)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
4	I	XX	–	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$ $R_n \wedge (AC \wedge K) \rightarrow R_n$	**Logically AND the K-bus with AC.** Logically AND the result with the contents of R_n. Deposit the final result in R_n. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on the carry output (CO) line.
		OO	CLR	$CI \rightarrow CO$ $0 \rightarrow R_n$	Clear R_n to all 0's. Force CO to CI. Used to clear a register and force CO to CI.
		II	ANR	$CI \vee (R_n \wedge AC) \rightarrow CO$ $R_n \wedge AC \rightarrow R_n$	Logically AND AC with R_n. Deposit the result in R_n. Force CO to one if the result is non-zero. Used to AND the accumulator with a register and test for a zero result.
4	II	XX	–	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$ $M \wedge (AC \wedge K) \rightarrow AT$	**Logically AND the K-bus with AC.** Logically AND the result with the M-bus. Deposit the final result in AC or T. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on CO.
		OO	CLA	$CI \rightarrow CO$ $0 \rightarrow AT$	Clear AC or T, as specified, to all 0's. Force CO to CI. Used to clear the specified register and force CO to CI.
		II	ANM	$CI \vee (M \wedge AC) \rightarrow CO$ $M \wedge AC \rightarrow AT$	Logically AND the M-bus with AC. Deposit the result in AC or T. Force CO to one if the result is non-zero. Used to AND M-bus data to the accumulator and test for a zero result.
4	III	XX	–	$CI \vee (AT \wedge I \wedge K) \rightarrow CO$ $AT \wedge (I \wedge K) \rightarrow AT$	**Logically AND the I-bus with the K-bus.** Logically AND the result with AC or T. Deposit the final result in the specified register. Logically OR CI with the word-wise OR of the final result. Place the value of the carry OR on CO.
		OO	CLA	$CI \rightarrow CO$ $0 \rightarrow AT$	Clear AC or T, as specified, to all 0's. Force CO to CI. Used to clear the specified register and force CO to CI.
		II	ANI	$CI \vee (AT \wedge I) \rightarrow CO$ $AT \wedge I \rightarrow AT$	Logically AND the I-bus with AC or T, as specified. Deposit the result in the specified register. Force CO to one if the result is non-zero. Used to AND the I-bus to the accumulator and test for a zero result.
5	I	XX	–	$CI \vee (R_n \wedge K) \rightarrow CO$ $K \wedge R_n \rightarrow R_n$	**Logically AND the K-bus with R_n.** Deposit the result in R_n. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLR	$CI \rightarrow CO$ $0 \rightarrow R_n$	Clear R_n to all 0's. Force CO to CI. Used to clear a register and force CO to CI.
		II	TZR	$CI \vee R_n \rightarrow CO$ $R_n \rightarrow R_n$	Force CO to one if R_n is non-zero. Used to test a register for zero. Also used to AND K-bus data with a register for masking and, optionally, testing for a zero result.
5	II	XX	–	$CI \vee (M \wedge K) \rightarrow CO$ $K \wedge M \rightarrow AT$	**Logically AND the K-bus with the M-bus.** Deposit the result in AC or T, as specified. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLA	$CI \rightarrow CO$ $0 \rightarrow AT$	Clear AC or T, as specified, to all 0's. Force CO to CI. Used to clear the specified register and force CO to CI.
		II	LTM	$CI \vee M \rightarrow CO$ $M \rightarrow AT$	Load AC or T, as specified, from the M-bus. Force CO to one if the result is non-zero. Used to load the specified register from memory and test for a zero result. Also used to AND the K-bus with the M-bus for masking and, optionally, testing for a zero result.
5	III	XX	–	$CI \vee (AT \wedge K) \rightarrow CO$ $K \wedge AT \rightarrow AT$	**Logically AND the K-bus with AC or T, as specified.** Deposit the result in the specified register. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLA	$CI \rightarrow CO$ $0 \rightarrow AT$	Clear AC or T, as specified, to all 0's. Force CO to CI. Used to clear the specified register and force CO to CI.
		II	TZA	$CI \vee AT \rightarrow CO$ $AT \rightarrow AT$	Force CO to one if AC or T, as specified, is non-zero. Used to test the specified register for zero. Also used to AND the K-bus to the specified register for masking and, optionally, testing for a zero result.

FUNCTION DESCRIPTION (CONT'D)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
6	I	XX	–	$CI \vee (AC \wedge K) \rightarrow CO$ $R_n \vee (AC \wedge K) \rightarrow R_n$	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the result of the carry OR on CO. Logically OR R_n with the logical AND of AC and the K-bus. Deposit the result in R_n.
		OO	NOP	$CI \rightarrow CO$ $R_n \rightarrow R_n$	Force CO to CI. Used as a null operation or to force CO to CI.
		II	ORR	$CI \vee AC \rightarrow CO$ $R_n \vee AC \rightarrow R_n$	Force CO to one if AC is non-zero. Logically OR AC with R_n. Deposit the result in R_n. Used to OR the accumulator to a register and, optionally, test the previous accumulator value for zero.
6	II	XX	–	$CI \vee (AC \wedge K) \rightarrow CO$ $M \vee (AC \wedge K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the carry OR on CO. Logically OR the M-bus, with the logical AND of AC and the K-bus. Deposit the final result in AC or T.
		OO	LMF	$CI \rightarrow CO$ $M \rightarrow AT$	Load AC or T, as specified, from the M-bus. Force CO to CI. Used to load the specified register with memory data and force CO to CI.
		II	ORM	$CI \vee AC \rightarrow CO$ $M \vee AC \rightarrow AT$	Force CO to one if AC is non-zero. Logically OR the M-bus with AC. Deposit the result in AC or T, as specified. Used to OR M-bus with the AC and, optionally, test the previous value of AC for zero.
6	III	XX	–	$CI \vee (I \wedge K) \rightarrow CO$ $AT \vee (I \wedge K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of the I-bus and the K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Logically OR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	NOP	$CI \rightarrow CO$ $R_n \rightarrow R_n$	Force CO to CI. Used as a null operation or to force CO to CI.
		II	ORI	$CI \vee I \rightarrow CO$ $I \vee AT \rightarrow AT$	Force CO to one if the data on the I-bus is non-zero. Logically OR the I-bus to AC or T, as specified. Deposit the result in the specified register. Used to OR I-bus data with the specified register and, optionally, test the I-bus data for zero.

FUNCTION TRUTH TABLE

FUNCTION GROUP	F_6	F_5	F_4
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

REGISTER GROUP	REGISTER	F_3	F_2	F_1	F_0
I	R_0	0	0	0	0
	R_1	0	0	0	1
	R_2	0	0	1	0
	R_3	0	0	1	1
	R_4	0	1	0	0
	R_5	0	1	0	1
	R_6	0	1	1	0
	R_7	0	1	1	1
	R_8	1	0	0	0
	R_9	1	0	0	1
	T	1	1	0	0
	AC	1	1	0	1
II	T	1	0	1	0
	AC	1	0	1	1
III	T	1	1	1	0
	AC	1	1	1	1

SYMBOL	MEANING
I, K, M	Data on the I, K, and M busses, respectively
CI, LI	Data on the carry input and left input, respectively
CO, RO	Data on the carry output and right output, respectively
R_n	Contents of register n including T and AC (R-Group I)
AC	Contents of the accumulator
AT	Contents of AC or T, as specified
MAR	Contents of the memory address register
L, H	As subscripts, designate low and high order bit, respectively
+	2's complement addition
–	2's complement subtraction
$\wedge$	Logical AND
$\vee$	Logical OR
$\overline{\oplus}$	Exclusive-NOR
$\rightarrow$	Deposit into

NOTE:
1. 2's complement arithmetic adds 111 . . . 11 to perform subtraction of 000 . . . 01.

FUNCTION DESCRIPTION (CONT'D)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
7	I	XX	–	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$ $R_n \overline{\oplus} (AC \wedge K) \rightarrow R_n$	Logically OR CI with the word-wise OR of the logical AND of R_n and AC and the K-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive-NOR the result with R_n. Deposit the final result in R_n.
		OO	CMR	$CI \rightarrow CO \quad \overline{R_n} \rightarrow R_n$	Complement the contents of R_n. Force CO to CI.
		II	XNR	$CI \vee (R_n \wedge AC) \rightarrow CO$ $R_n \overline{\oplus} AC \rightarrow R_n$	Force CO to one if the logical AND of AC and R_n is non-zero. Exclusive-NOR AC with R_n. Deposit the result in R_n. Used to exclusive-NOR the accumulator with a register.
7	II	XX	–	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$ $M \overline{\oplus} (AC \wedge K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus and M-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive NOR the result with the M-bus. Deposit the final result in AC or T.
		OO	LCM	$CI \rightarrow CO \quad \overline{M} \rightarrow AT$	Load the complement of the M-bus into AC or T, as specified. Force CO to CI.
		II	XNM	$CI \vee (M \wedge AC) \rightarrow CO$ $M \overline{\oplus} AC \rightarrow AT$	Force CO to one if the logical AND of AC and the M-bus is non-zero. Exclusive-NOR AC with the M-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR memory data with the accumulator.
7	III	XX	–	$CI \vee (AT \wedge I \wedge K) \rightarrow CO$ $AT \overline{\oplus} (I \wedge K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of the specified register and the I-bus and K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Exclusive-NOR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	CMA	$CI \rightarrow CO \quad \overline{AT} \rightarrow AT$	Complement AC or T, as specified. Force CO to CI.
		II	XNI	$CI \vee (AT \wedge I) \rightarrow CO$ $I \overline{\oplus} AT \rightarrow AT$	Force CO to one if the logical AND of the specified register and the I-bus is non-zero. Exclusive-NOR AC with the I-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR input data with the accumulator.

FUNCTION TRUTH TABLE

FUNCTION GROUP	F_6	F_5	F_4
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

REGISTER GROUP	REGISTER	F_3	F_2	F_1	F_0
I	R_0	0	0	0	0
	R_1	0	0	0	1
	R_2	0	0	1	0
	R_3	0	0	1	1
	R_4	0	1	0	0
	R_5	0	1	0	1
	R_6	0	1	1	0
	R_7	0	1	1	1
	R_8	1	0	0	0
	R_9	1	0	0	1
	T	1	1	0	0
	AC	1	1	0	1
II	T	1	0	1	0
	AC	1	0	1	1
III	T	1	1	1	0
	AC	1	1	1	1

SYMBOL	MEANING
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–	2's complement subtraction
$\wedge$	Logical AND
$\vee$	Logical OR
$\overline{\oplus}$	Exclusive-NOR
$\rightarrow$	Deposit into

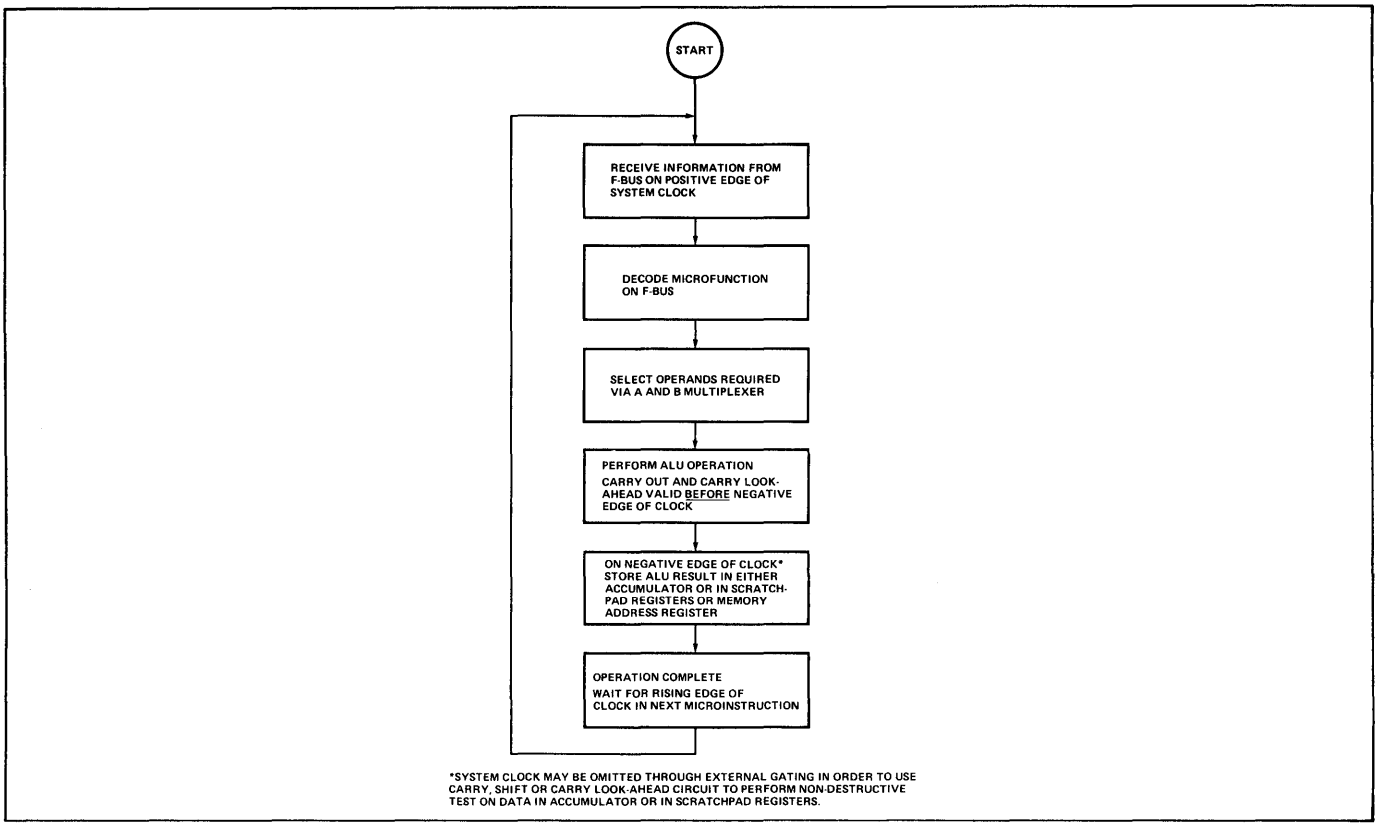
NOTE:
1. 2's complement arithmetic adds 111 . . . 11 to perform subtraction of 000 . . . 01.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +160°C
All Output and Supply Voltages	−0.5V to +7V
All Input Voltages	−1.0V to +5.5V
Output Currents	100mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

MICROCYCLE TIMING SEQUENCE



DC CHARACTERISTICS $T_A = 0°C$ to $+70°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
V_C	Input Clamp Voltage (All Input Pins)	V_{CC} = 4.75V, I_C = −5mA		−0.8	−1.0	V
I_F	Input Load Current:					
	F_0–F_6, CLK, K_0, K_1, EA, ED	V_{CC} = 5.25V, V_F = 0.45V		−0.05	−0.25	mA
	I_0, I_1, M_0, M_1, LI			−0.85	−1.5	mA
	CI			−2.3	−4.0	mA
I_R	Input Leakage Current:					
	F_0–F_6, CLK, K_0, K_1, EA, ED	V_{CC} = 5.25V, V_R = 5.25V			40	μA
	I_0, I_1, M_0, M_1, LI				60	μA
	CI				180	μA
V_{IL}	Input Low Voltage	V_{CC} = 5.0V			0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{CC}	Power Supply Current	V_{CC} = 5.25V[2]		145	190	mA
V_{OL}	Output Low Voltage Except X and Y	V_{CC} = 4.75V, I_{OL} = 10mA		0.3	0.45	V
	X and Y	V_{CC} = 4.75V, I_{OL} = 16mA		0.35	0.50	V
V_{OH}	Output High Voltage (All Output Pins)	V_{CC} = 4.75V, I_{OH} = −1mA	2.4	3.0		V
I_{OS}	Short Circuit Output Current (All Output Pins)	V_{CC} = 5.0V	−15	−25	−60	mA
$I_{O\ (off)}$	Off State Output Current	V_{CC} = 5.25V, V_O = 0.45V			−100	μA
	A_0, A_1, D_0 and D_1 Only	V_{CC} = 5.25V, V_O = 5.25V			100	μA

NOTES:
1. Typical values are for $T_A = 25°C$ and typical supply voltage.
2. CLK input grounded, other inputs open.

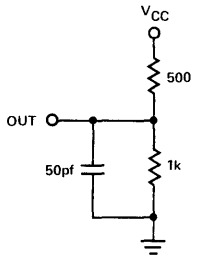
SWITCHING CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5%

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT
t_{CY}	Clock Cycle Time	70	45		ns
t_{WP}	Clock Pulse Width	17	10		ns
t_{FS}	Function Input Set-Up Time (F_0 through F_6)	48	31		ns
	Data Set-Up Time:				
t_{DS}	I_0, I_1, M_0, M_1, K_0, K_1	40	24		ns
t_{SS}	LI, CI	21	7		ns
	Data and Function Hold Time:				
t_{FH}	F_0 through F_6	4	0		ns
t_{DH}	I_0, I_1, M_0, M_1, K_0, K_1	4	0		ns
t_{SH}	LI, CI	12	0		ns
	Propagation Delay to X, Y, RO from:				
t_{XF}	Any Function Input		28	41	ns
t_{XD}	Any Data Input		18	33	ns
t_{XT}	Trailing Edge of CLK		33	48	ns
t_{XL}	Leading Edge of CLK	13	18→40	73	ns
	Propagation Delay to CO from:				
t_{CL}	Leading Edge of CLK	16	24→44	84	ns
t_{CT}	Trailing Edge of CLK		40	56	ns
t_{CF}	Any Function Input		35	52	ns
t_{CD}	Any Data Input		23	44	ns
t_{CC}	CI (Ripple Carry)		13	20	ns
	Propagation Delay to A_0, A_1, D_0, D_1 from:				
t_{DL}	Leading Edge of CLK		25	40	ns
t_{DE}	Enable Input ED, EA		12	20	ns

NOTE:
1. Typical values are for T_A = 25°C and typical supply voltage.

PARAMETER MEASUREMENT INFORMATION

TEST LOAD CIRCUIT

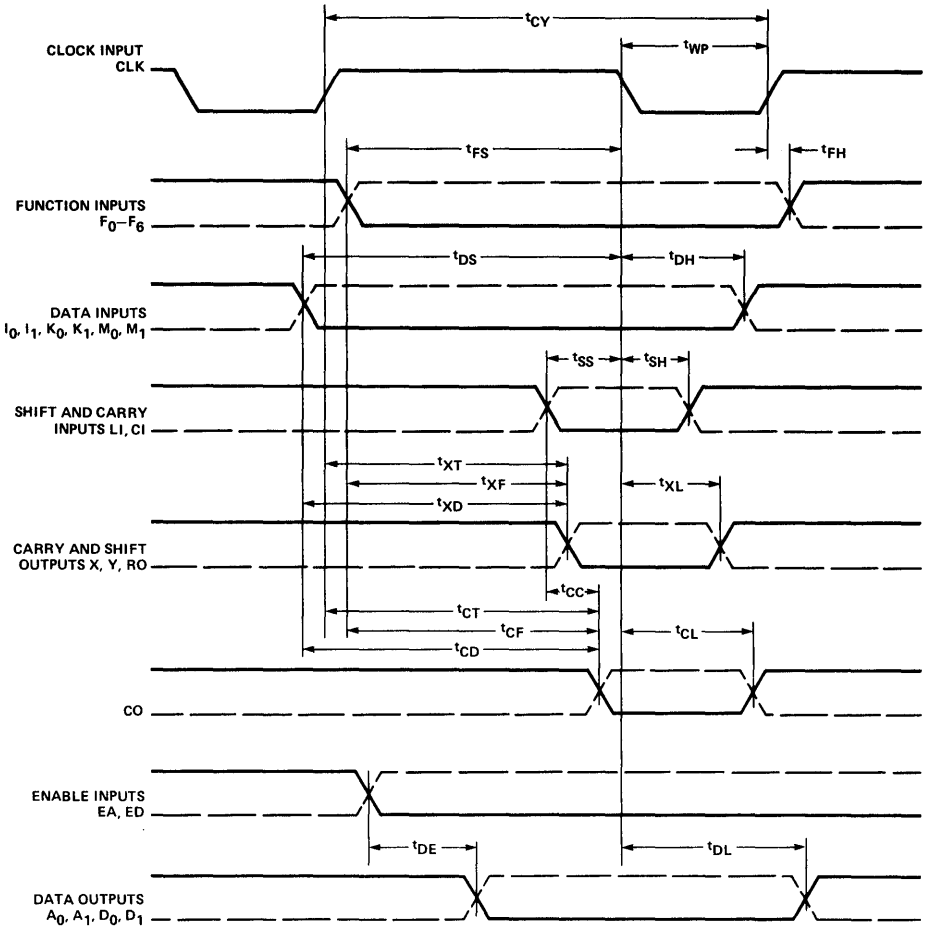


NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

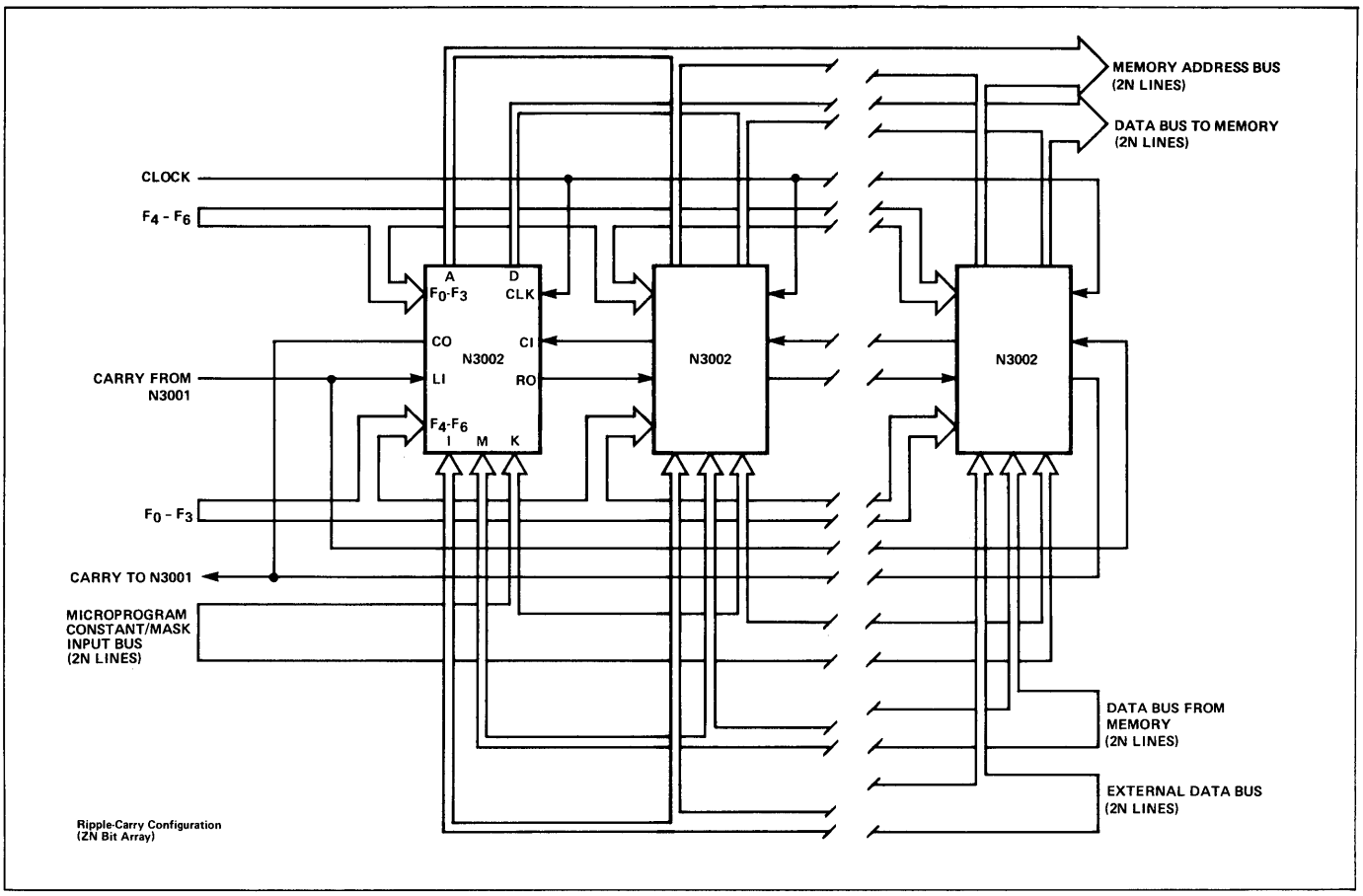
TEST CONDITIONS

Input pulse amplitude: 2.5V
Input rise and fall times of 5ns between 1 and 2 volts.
Output loading is 10mA and 50pF.
Speed measurements are made at 1.5 volt levels.

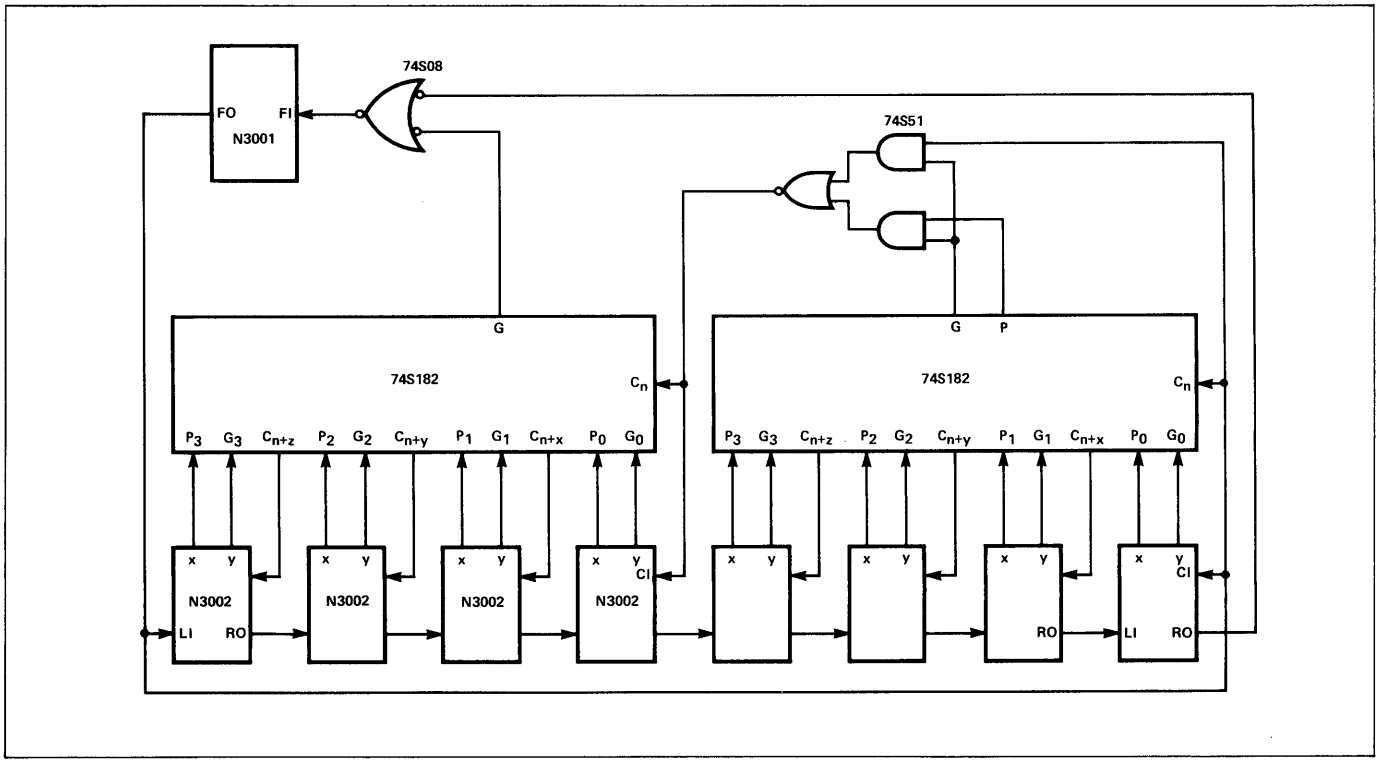
PARAMETER MEASUREMENT INFORMATION



TYPICAL CONFIGURATIONS



CARRY LOOK–AHEAD CONFIGURATION



DESCRIPTION

The S54S182 and N74S182 are high-speed, look-ahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

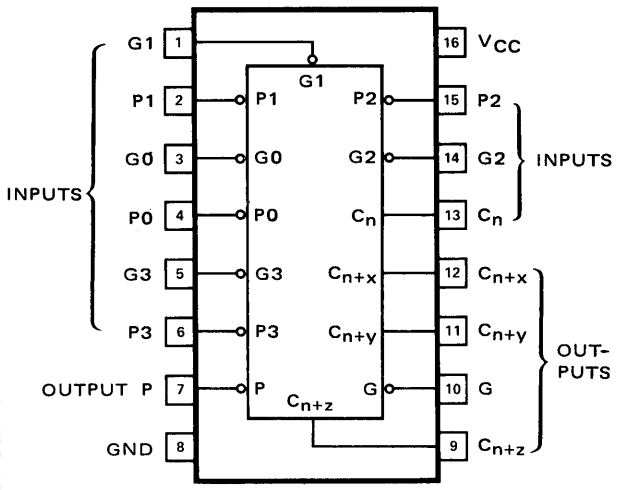
When used in conjunction with the '181, 'LS181, or 'S181 arithmetic logic unit (ALU), these generators provide high-speed carry look-ahead capability for any word length. Each '182 or 'S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading '182 or 'S182 circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the '181, 'LS181, and 'S181 ALU's are in their true form and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions as explained on the '181, 'LS181, and 'S181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the 'S182 are:

$$C_{n+x} = \overline{G}_0 + \overline{P}_0 C_n$$
$$C_{n+y} = \overline{G}_1 + \overline{P}_1 \overline{G}_0 + \overline{P}_1 \overline{P}_0 C_n$$
$$C_{n+z} = \overline{G}_2 + \overline{P}_2 \overline{G}_1 + \overline{P}_2 \overline{P}_1 \overline{G}_0 + \overline{P}_2 \overline{P}_1 \overline{P}_0 C_n$$
$$\overline{G} = \overline{G}_3 (\overline{P}_3 + \overline{G}_2) (\overline{P}_3 + \overline{P}_2 + \overline{G}_1) (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0)$$
$$\overline{P} = \overline{P}_3 \overline{P}_2 \overline{P}_1 \overline{P}_0$$

PIN CONFIGURATION (Top View)

B,F,W, PACKAGE



logic: see description

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
G0, G1, G2, G3	3, 1, 14, 5	ACTIVE-LOW CARRY GENERATE INPUTS
P0, P1, P2, P3	4, 2, 15, 6	ACTIVE-LOW CARRY PROPAGATE INPUTS
C_n	13	CARRY INPUT
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	CARRY OUTPUTS
G	10	ACTIVE-LOW CARRY GENERATE OUTPUT
P	7	ACTIVE-LOW CARRY PROPAGATE OUTPUT
V_{CC}	16	SUPPLY VOLTAGE
GND	8	GROUND

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54S182			74S182			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			-1			-1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER			TEST CONDITIONS[1]	54S182			74S182			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	C_N input	V_{CC} = MAX, V_I = 2.7V			50			50	μA
		P3 input				100			100	
		P2 input				150			150	
		P0, P1, or G3 input				200			200	
		G0 or G2 input				350			350	
		G1 input				400			400	
I_{IL}	Low-level input current	C_n input	V_{CC} = MAX, V_I = 0.5V			−2			−2	mA
		P3 input				−4			−4	
		P2 input				−6			−6	
		P0, P1, or G3 input				−8			−8	
		G0 or G2 input				−14			−14	
		G1 input				−16			−16	
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = 5V, See Note 3		35			35		mA
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX, See Note 4		69	99		69	109	mA

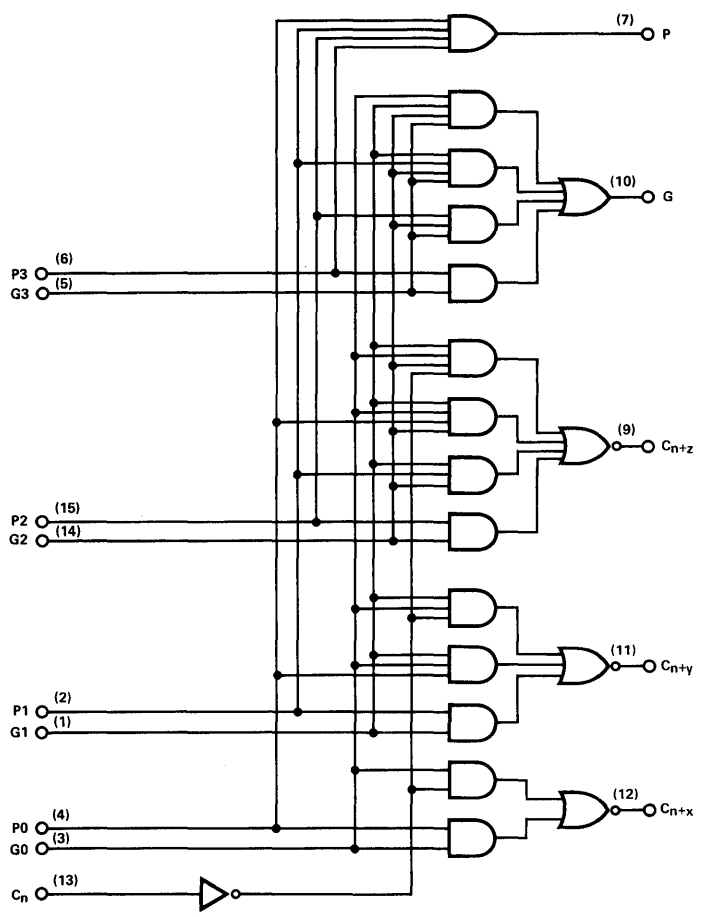
[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
[2] All typical values are at V_{CC} = 5V, T_A = 25°C.
[3] Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.
NOTES: 3. I_{CCH} is measured with all outputs open, inputs P3 and G3 at 4.5V, and all other inputs grounded.
4. I_{CCL} is measured with all outputs open, inputs G0, G1, and G2 at 4.5V, and all other inputs grounded.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

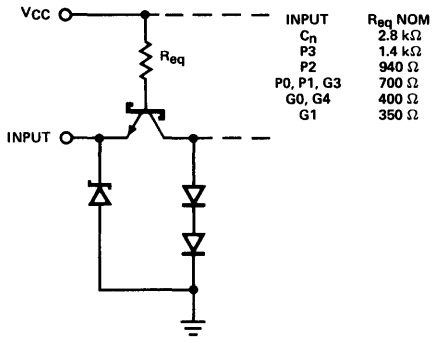
PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	G0, G1, G2, G3, P0, P1, P2, or P3	C_{n+x}, C_{n+y}, or C_{n+z}	C_L = 15pF, R_L = 280Ω		4.5	7	ns
t_{PHL}					4.5	7	
t_{PLH}	G0, G1, G2, G3, P1, P2, or P3	G			5	7.5	ns
t_{PHL}					7	10.5	
t_{PLH}	P0, P1, P2, or P3	P			4.5	6.5	ns
t_{PHL}					6.5	10	
t_{PLH}	C_n	C_{n+x}, C_{n+y}, or C_{n+z}			6.5	10	ns
t_{PHL}					7	10.5	

[1] t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

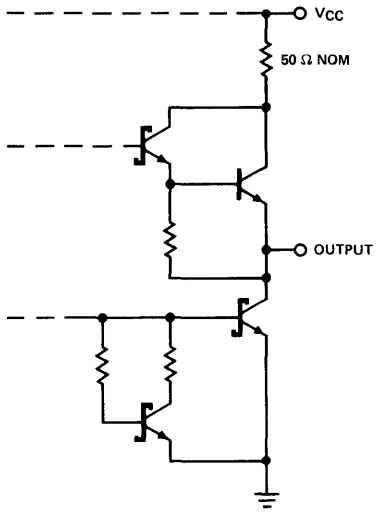
FUNCTIONAL BLOCK DIAGRAM AND SCHEMATICS OF INPUTS AND OUTPUTS



EQUIVALENT OF EACH INPUT

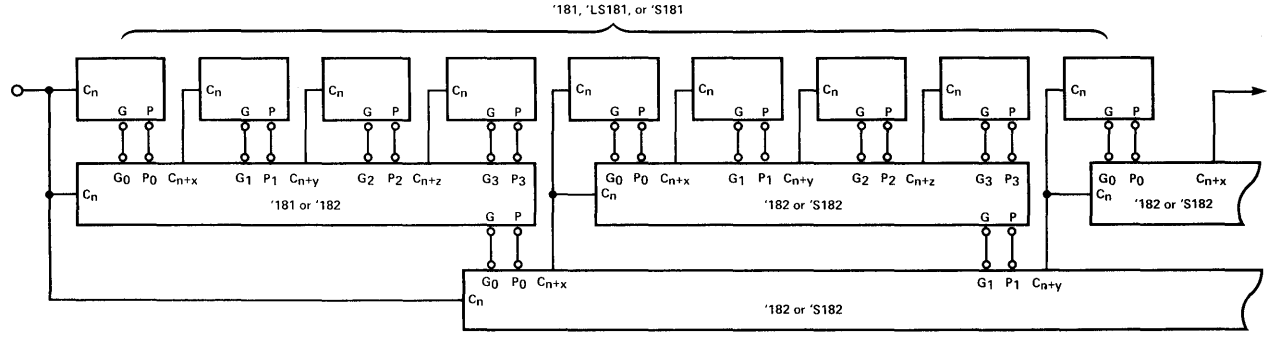


TYPICAL OF ALL OUTPUTS



TYPICAL APPLICATION DATA

64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS



A and B inputs and F outputs of S54/74S181 are not shown.

Load circuit and typical waveforms are shown at the front of this section.

signetics 576-BIT BIPOLAR RAM (64x9) 82S09

JUNE 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S09 is a 576-Bit, Schottky clamped TTL, random access memory, organized as 64X9. This organization allows byte manipulation of data, including parity. Where parity is not monitored, the ninth bit can be used as a flag or status indicator for each word stored. With a typical access time of 30ns, it is ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09 is fully TTL compatible, and features open collector outputs, chip enable input, and a very low current PNP input structure to enhance memory expansion.

During WRITE operation, the logic state of the device output follows the complement of the data input being written. This feature allows faster execution of WRITE-READ cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a WRITE cycle.

The 82S09 is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S09, I. For the military temperature range (−55°C to +125°C) specify S82S09, I.

FEATURES

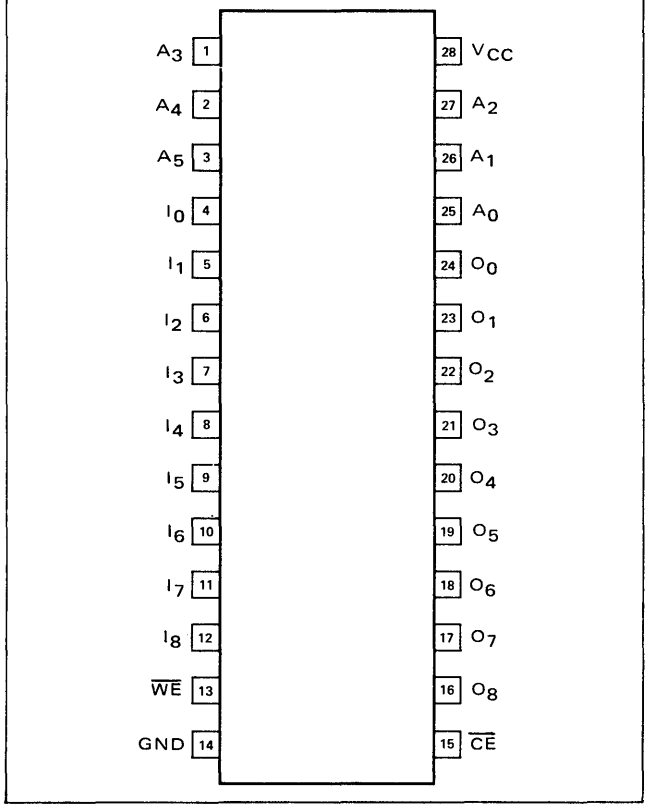
- ORGANIZATION – 64 X 9
- ADDRESS ACCESS TIME:
  - S82S09 – 80ns, MAXIMUM
  - N82S09 – 45ns, MAXIMUM
- WRITE CYCLE TIME:
  - S82S09 – 70ns, MAXIMUM
  - N82S09 – 45ns, MAXIMUM
- POWER DISSIPATION – 1.3mW/BIT TYPICAL
- INPUT LOADING:
  - S82S09 – (−150μA) MAXIMUM
  - N82S09 – (−100μA) MAXIMUM
- OUTPUT FOLLOWS COMPLEMENT OF DATA INPUT DURING WRITE
- ON-CHIP ADDRESS DECODING
- OPEN COLLECTOR OUTPUTS
- CHIP ENABLE FOR WORD EXPANSION
- BYTE I/O MANIPULATION, INCLUDING PARITY

APPLICATIONS

BUFFER MEMORY
CONTROL REGISTER
FIFO MEMORY
PUSH DOWN STACK
SCRATCH PAD

PIN CONFIGURATION

I PACKAGE

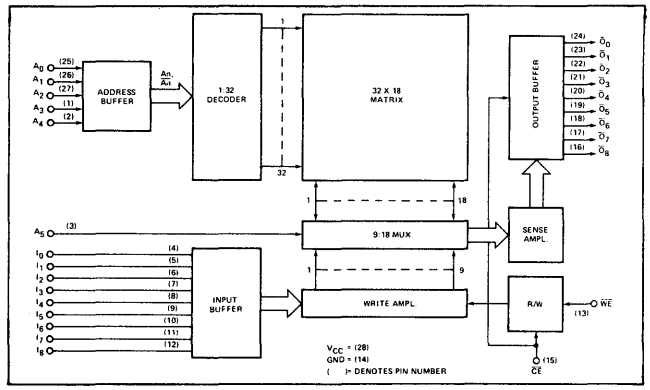


TRUTH TABLE

MODE	CE	WE	I_N	O_N
READ	0	1	X	Complement of Data Stored
WRITE "0"	0	0	0	1
WRITE "1"	0	0	1	0
DISABLED	1	X	X	1

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S10)	+5.5	Vdc
T_A	Operating Temperature Range		
	(N82S09)	0° to +75°	°C
	(S82S09)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS[7]

S82S09 $-55°C \leqslant T_A \leqslant +125°C$, $4.5V \leqslant V_{CC} \leqslant 5.5$
N82S09 $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25$

PARAMETER[1]		TEST CONDITIONS	S82S09			N82S09			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IL}	Low Level Input Voltage	V_{CC} = MIN			.80			.85	V
V_{IH}	High Level Input Voltage	V_{CC} = MAX	2.2			2.0			V
V_{IC}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −12mA (Note 5)		−1.0	−1.5		−1.0	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = MIN, I_{OL} = 6.4mA (Note 6)		0.35	0.50		0.35	0.5	V
I_{OLK}	Output Leakage Current	V_{CC} = MAX, V_{OUT} = 5.5V (Note 4)		1	60		1	40	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.45V		−10	−150		−10	−100	μA
I_{IH}	High Level Input Current	V_{IN} = 5.5V		1	40		1	25	μA
I_{CC}	V_{CC} Supply Current	V_{CC} = MAX (Note 3)		150	200		150	190	mA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V (Note 4)		8			8		pF

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{CC} is measured with the write enable and memory enable input grounded, all other inputs at 4.5V, and the outputs open.
4. Measured with V_{IH} applied to $\overline{CE}$.
5. Test each input one at the time.
6. Measured with the logic "0" stored. Output sink current is supplied through a resistor to V_{CC}.
7. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up.

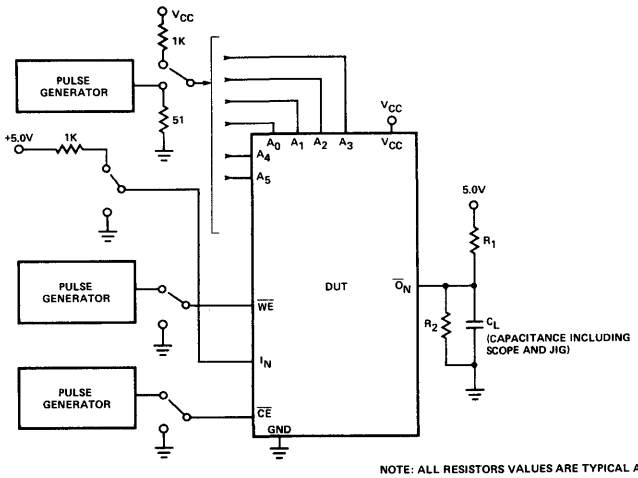
SWITCHING CHARACTERISTICS[3]

S82S09 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$
N82S09 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

PARAMETER		TEST CONDITIONS	S82S09			N82S09			UNIT
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Propagation Delays									
T_{AA}	Address Access Time	C_L = 30pF R_1 = 600Ω R_2 = 900Ω		30	80		30	45	ns
T_{CE}	Chip Enable Access Time			15	50		15	30	ns
T_{CD}	Chip Enable Output Disable Time			15	50		15	30	ns
Write Set-up Times									
T_{WSA}	Address to Write Enable		10	0		5	0		ns
T_{WSD}	Data In to Write Enable		50	25		35	25		ns
T_{WSC}	$\overline{CE}$ to Write Enable		10	0		5	0		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		10	0		5	0		ns
T_{WHD}	Data In to Write Enable		5	0		5	0		ns
T_{WHC}	$\overline{CE}$ to Write Enable		10	0		5	0		ns
T_{WP}	Write Enable Pulse Width (Note 2)		50	25		35	25		ns

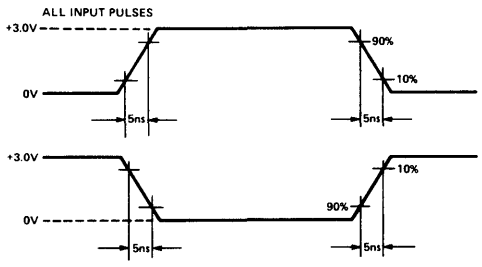
AC TEST LOAD

LOADING CONDITION



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

INPUT PULSES

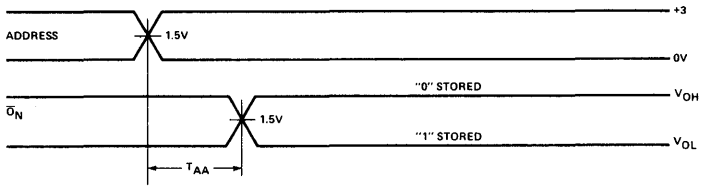


NOTES:
1. Typical values are at V_{CC} = +5.0V, and T_A = +25°C.
2. Minimum required to guarantee a WRITE into the slowest bit.
3. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up.

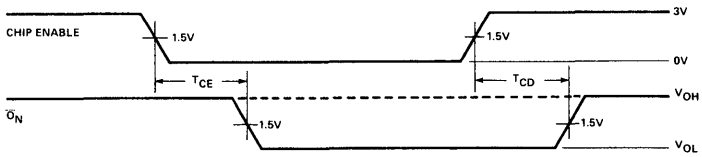
PARAMETER MEASUREMENT INFORMATION

READ CYCLE

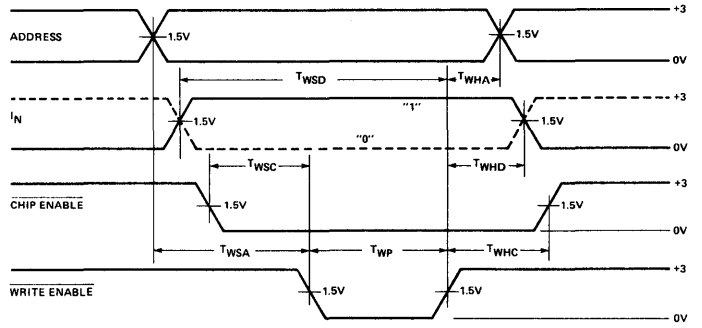
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

signetics

1024x1 BIT BIPOLAR RAM
OPEN COLLECTOR (82S10) TRI-STATE (8211)

82S10
82S11

FEBURARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

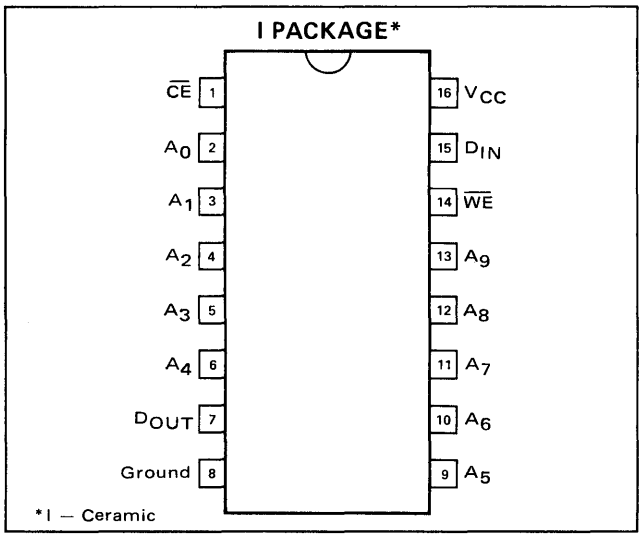
DESCRIPTION

The 82S10/11 is a high speed 1024-bit random access memory organized as 1024 words X 1 bit. With a typical access time of 30ns, it is ideal for cache buffer applications and for systems requiring very high speed main memory.

Both the 82S10 and 82S11 require a single +5 volts power supply and feature very low current PNP input structures. They are fully TTL compatible, and include on-chip decoding and a chip enable input for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S10 and 82S11 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S10/11, I. For the military temperature range (−55°C to +125°C) specify S82S10/11, I.

PIN CONFIGURATION



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	D_{OUT}	
				82S10	82S11
READ	0	1	X	STORED DATA	STORED DATA
WRITE "0"	0	0	0	1	High-Z
WRITE "1"	0	0	1	1	High-Z
DISABLED	1	X	X	1	High-Z

X = Don't care.

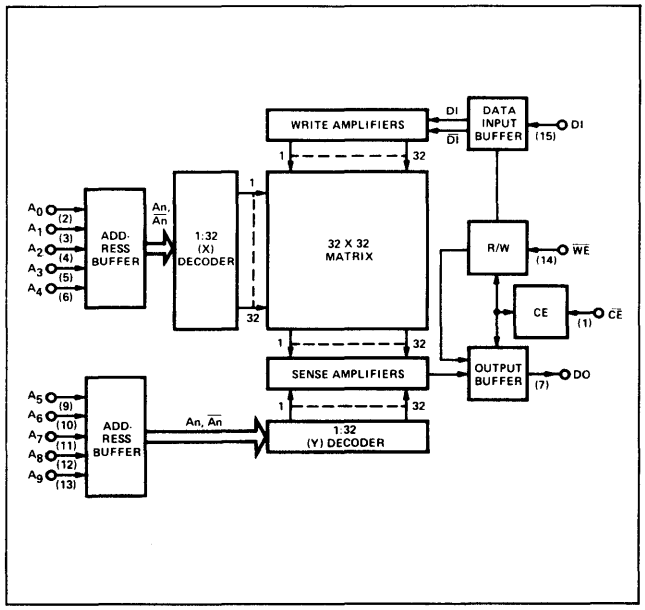
FEATURES

- ORGANIZATION — 1024 X 1
- ADDRESS ACCESS TIME:
  - S82S10/11 — 70ns, MAXIMUM
  - N82S10/11 — 45ns, MAXIMUM
- WRITE CYCLE TIME:
  - S82S10/11 — 75ns, MAXIMUM
  - N82S10/11 — 45ns, MAXIMUM
- POWER DISSIPATION — 0.5mW/BIT, TYPICAL
- INPUT LOADING:
  - S82S10/11 — (−150μA) MAXIMUM
  - N82S10/11 — (−100μA) MAXIMUM
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTIONS:
  - 82S10 — OPEN COLLECTOR
  - 82S11 — TRI-STATE
- NON-INVERTING OUTPUT
- BLANKED OUTPUT DURING WRITE
- 16 PIN CERAMIC PACKAGE

APPLICATIONS

HIGH SPEED MAIN FRAME
CACHE MEMORY
BUFFER STORAGE
WRITABLE CONTROL STORE

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S10)	+5.5	Vdc
V_O	Off-State Output Voltage (82S11)	+5.5	Vdc
T_A	Operating Temperature Range (N82S10/11) (S82S10/11)	 0° to +75° −55° to +125°	 °C °C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS[9]

S82S10/11 $-55°C \leqslant T_A \leqslant +125°C$, $4.5V \leqslant V_{CC} \leqslant 5.5$
N82S10/11 $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25$

PARAMETER		TEST CONDITIONS	S82S10/11			N82S10/11			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IL}	Low Level Input Voltage	V_{CC} = MIN (Note 1)			.80			.85	V
V_{IH}	High Level Input Voltage	V_{CC} = MAX (Note 1)	2.1			2.1			V
V_{IC}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −12mA (Note 1, 7)		−1.0	−1.5		−1.0	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = MIN, I_{OL} = 16mA (Note 1, 8)		0.35	0.50		0.35	0.45	V
V_{OH}	High Level Output Voltage (82S11)	V_{CC} = MIN, I_{OH} = −2mA (Note 1, 5)	2.4			2.4			V
I_{OLK}	Output Leakage Current (82S10)	V_{CC} = MAX, V_{OUT} = 5.5V (Note 6)		1	60		1	40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (82S11)	V_{CC} = MAX, V_{OUT} = 5.5V V_{CC} = MAX, V_{OUT} = 0.45V (Note 6)		1 −1	100 −100		1 −1	60 −60	μA μA
I_{IL}	Low Level Input Current	V_{IN} = 0.45V		−10	−150		−10	−100	μA
I_{IH}	High Level Input Current	V_{IN} = 5.5V		1	40		1	25	μA
I_{OS}	Short Circuit Output Current (82S11)	V_{CC} = MAX, V_{OUT} = 0V (Note 3)	−20		−100	−20		−100	mA
I_{CC}	V_{CC} Supply Current	V_{CC} = MAX (Note 4) $0 < T_A < 25°C$ $T_A \geqslant 25°C$ $T_A \leqslant 0°C$		 120 95	 155 130 170		 120 95	 155 130 170	 mA mA mA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		4			4		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V		7			7		pF

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Duration of the short-circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic "1" stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Test each input one at the time.
8. Measured with a logic "0" stored. Output sink current is supplied through a resistor to V_{CC}.
9. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   ϕ_{JA} Junction to Ambient at 400 fpm air flow — 50°C/Watt
   ϕ_{JA} Junction to Ambient — still air — 90°C/Watt
   ϕ_{JA} Junction to Case — 20°C/Watt

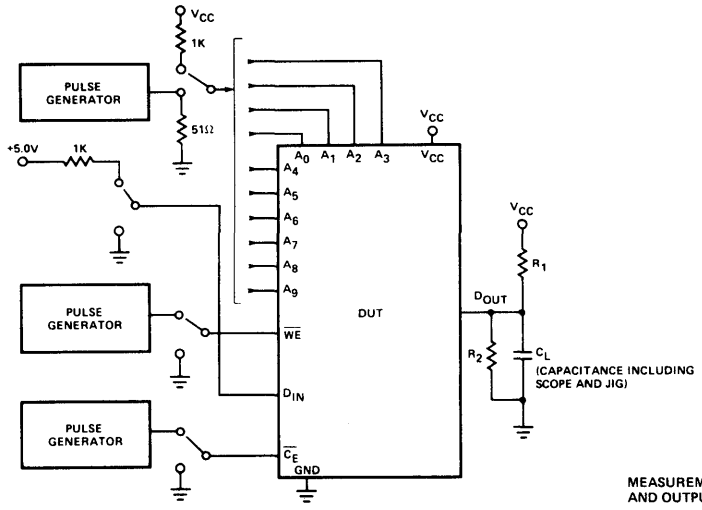
SWITCHING CHARACTERISTICS[3]

S82S10/11 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$
N82S10/11 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

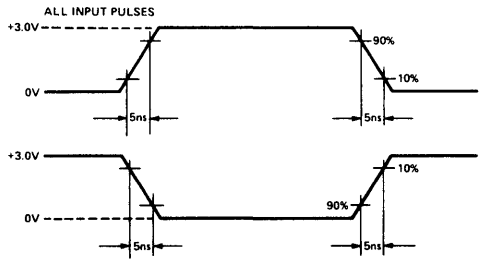
PARAMETER		TEST CONDITIONS	S82S10/11			N82S10/11			UNIT
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Propagation Delays									
T_{AA}	Address Access Time	C_L = 30pF R_1 = 270Ω R_2 = 600Ω		30	70		30	45	ns
T_{CE}	Chip Enable Access Time			15	45		15	30	ns
T_{CD}	Chip Enable Output Disable Time			15	45		15	30	ns
T_{WD}	Write Enable to Output Disable Time			20	45		20	30	ns
T_{WR}	Write Recovery Time			20	45		20	30	ns
Write Set-up Times									
T_{WSA}	Address to Write Enable		15	0		5	0		ns
T_{WSD}	Data In to Write Enable		55	35		40	35		ns
T_{WSC}	$\overline{CE}$ to Write Enable		5	0		5	0		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		10	0		5	0		ns
T_{WHD}	Data In to Write Enable		5	0		5	0		ns
T_{WHC}	$\overline{CE}$ to Write Enable		5	0		5	0		ns
T_{WP}	Write Enable Pulse Width (Note 2)		50	25		35	25		ns

AC TEST LOAD

LOADING CONDITION



INPUT PULSES



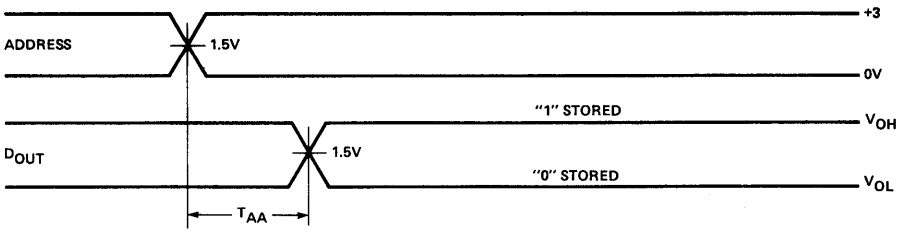
MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5V LEVEL OF INPUTS AND OUTPUT.

NOTES:
1. Typical values are at V_{CC} = +5.0V, and T_A = +25°C.
2. Minimum required to guarantee a WRITE into the slowest bit.
3. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} Junction to Ambient at 400 fpm air flow — 50° C/Watt
   θ_{JA} Junction to Ambient — still air — 90° C/Watt
   θ_{JA} Junction to Case — 20° C/Watt

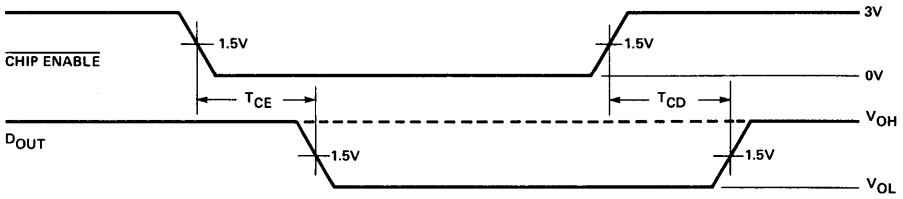
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

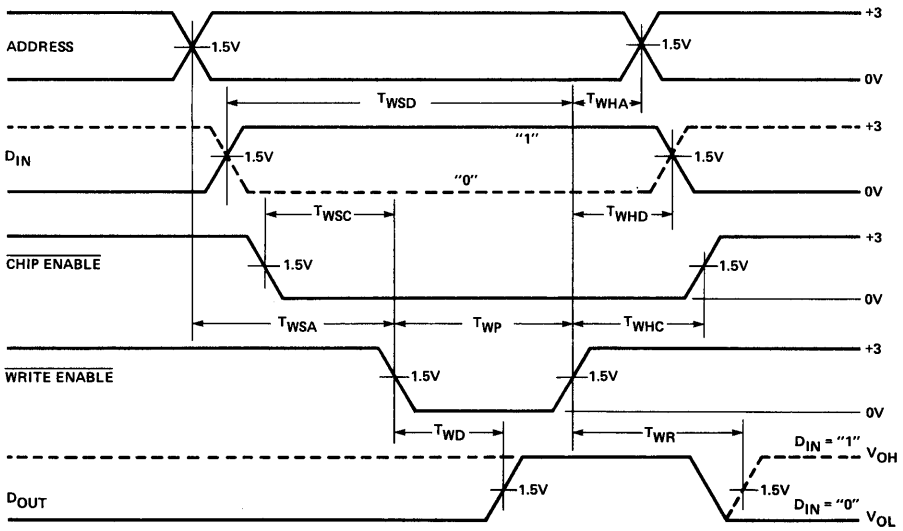
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{WR} Delay between end of WRITE ENABLE pulse and when DATA OUTPUT becomes valid. (Assuming ADDRESS still valid—not as shown.)

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT is in off state.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

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64-BIT BIPOLAR SCRATCH PAD MEMORY (16x4 RAM) 82S25

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S25 is a 64-bit, Schottky clamped TTL, Read-Write Random Access Memory ideal for use in scratch pad and high-speed buffer memory applications.

The 82S25 is a fully decoded memory array organized as 16 words of 4 bits each, with separate input and output lines. It features PNP inputs, one chip enable line, and open collector outputs for ease of memory expansion.

The outputs of the 82S25 assume a logic "1" state during write. This allows both memory inputs and outputs to share a common bus for minimizing interconnections, and more effective utilization of common I/O circuitry.

The 82S25 is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S25, B or F. For the military temperature range (−55°C to +125°C) specify S82S25, F only.

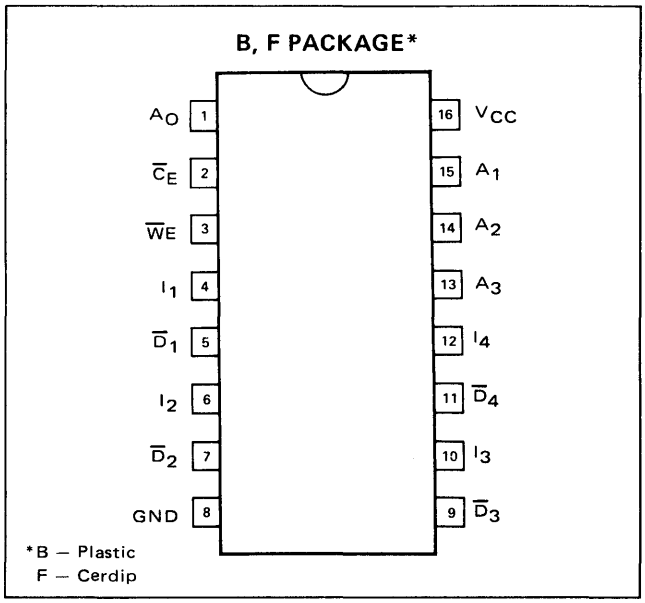
FEATURES

- ORGANIZATION – 16 X 4
- ADDRESS ACCESS TIME:
  S82S25 – 60ns, MAXIMUM
  N82S25 – 50ns, MAXIMUM
- WRITE CYCLE TIME:
  S82S25 – 50ns, MAXIMUM
  N82S25 – 35ns, MAXIMUM
- POWER DISSIPATION – 6.25mW/BIT, TYPICAL
- INPUT LOADING:
  S82S25 – (−150μA) MAXIMUM
  N82S25 – (−100μA) MAXIMUM
- OUTPUT BLANKING DURING WRITE
- ON-CHIP ADDRESS DECODING
- OPEN COLLECTOR OUTPUTS
- 16 PIN CERAMIC DIP

APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
PUSH DOWN STACKS
CONTROL STORE

PIN CONFIGURATION

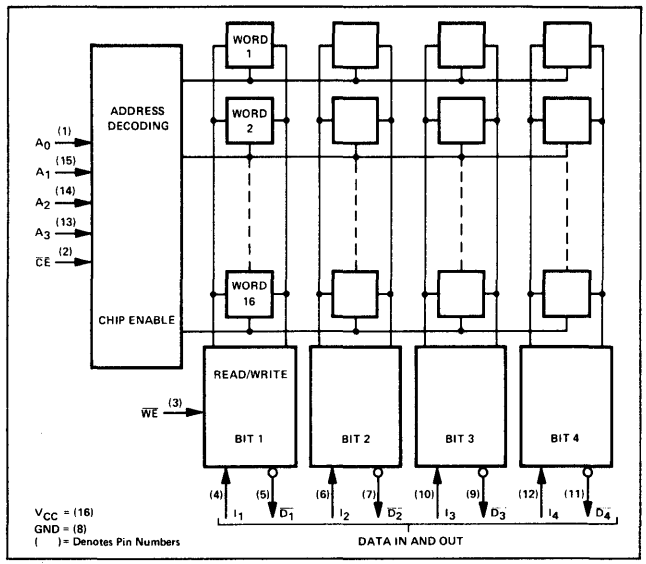


TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	In	$\overline{Dn}$
Read	0	1	X	Complement of data stored
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage	+5.5	Vdc
T_A	Operating Temperature Range		
	(N82S25)	0° to +75°	°C
	(S82S25)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S25 $-55°C \leqslant T_A \leqslant +125°C$, $4.5V \leqslant V_{CC} \leqslant 5.5V$
N82S25 $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS	S82S25[1,2,3]			N82S25[1,2,3]			UNIT
			MIN	TYP[8]	MAX	MIN	TYP[8]	MAX	
I_{IL}	"0" Input Current	V_{IN} = 0.45V		−10	−150		−10	−100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			25			10	μA
V_{IL}	"0" Level Input Voltage	V_{CC} = MIN			.80			.85	V
V_{IH}	"1" Level Input Voltage	V_{CC} = MAX	2.0			2.0			V
V_{IC}	Input Clamp Voltage	I_{IN} = −12mA, V_{CC} = MIN (Note 6)		−1.0	−1.5		−1.0	−1.5	V
V_{OL}	"0" Output Voltage	I_{OUT} = 16mA, V_{CC} = MIN (Notes 4, 5)		0.35	0.5		0.35	0.45	V
C_{IN}	Input Capacitance	V_{IH} = 2.0V, V_{CC} = 5.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, V_{CC} = 5.0V, $\overline{CE}$ = "1"		8			8		pF
I_{CC}	Power Supply Current	(Note 5)		80	120		80	105	mA
I_{OLK}	Output Leakage Current	$\overline{CE}$ = "1", V_{OUT} = 5.5V, V_{CC} = MIN		<1	100		<1.0	100	μA

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Positive current is defined as into the terminal referenced.
3. Positive logic definition: "1" = HIGH ≈ +5.0V; "0" = LOW ≈ GRD.
4. Output sink current is supplied through a resistor to V_{CC}.
5. All sense outputs in "0" state.
6. Test each input one at a time.
7. To guarantee a WRITE into the slowest bit.
8. Typical values are at V_{CC} = +5.0V and T_A = +25°C.

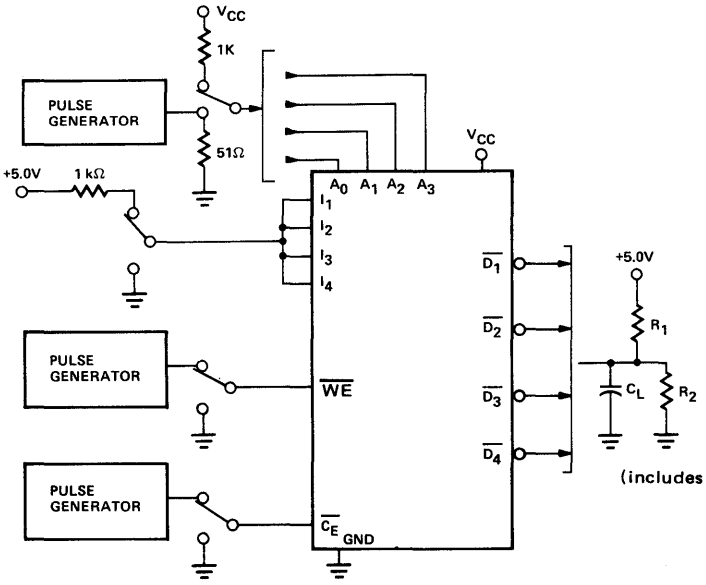
SWITCHING CHARACTERISTICS

S82S25 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S25 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S82S25			N82S25			UNIT
			MIN	TYP[8]	MAX	MIN	TYP[8]	MAX	
Propagation Delays									
T_{AA}	Address Access Time			35	60		35	50	ns
T_{CE}	Chip Enable Access Time			20	35		20	35	ns
T_{CD}	Chip Enable Output Disable Time			20	35		20	35	ns
T_{WD}	Write Enable to Output Disable Time			20	30		20	25	ns
T_{WR}	Write Recovery Time			35	60		35	50	ns
Write Set-up Times		$R_1 = 270\Omega$ $R_2 = 600\Omega$							
T_{WSA}	Address to Write Enable	$C_L = 30pF$	10	-8		0	-8		ns
T_{WSD}	Data In to Write Enable		25	5		20	5		ns
T_{WSC}	$\overline{CE}$ to Write Enable		0	-5		0	-5		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		10	0		5	0		ns
T_{WHD}	Data In to Write Enable		10	-3		5	-3		ns
T_{WHC}	$\overline{CE}$ to Write Enable		5	0		5	0		ns
T_{WP}	Write Enable Pulse Width (Note 7)		30	18		30	18		ns

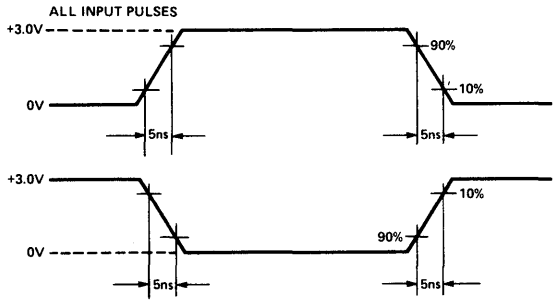
AC TEST LOAD AND WAVEFORMS

LOADING CONDITION



(includes jig and scope capacitance)

INPUT PULSES

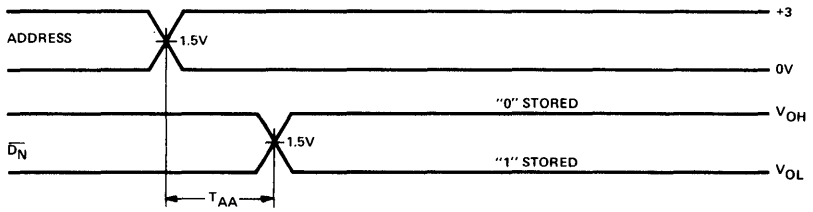


MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5V LEVEL OF INPUTS AND OUTPUT.

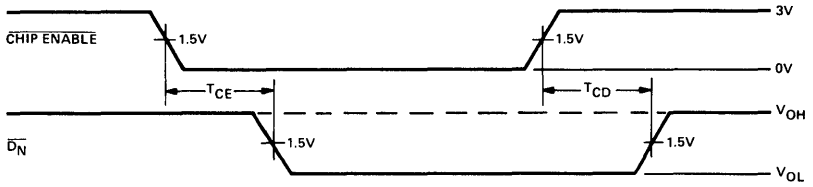
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

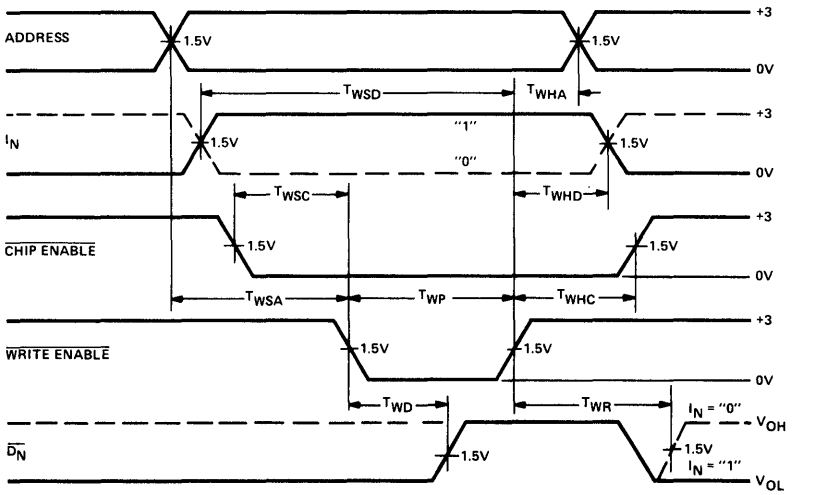
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

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T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

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T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

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T_{WP} Width of WRITE ENABLE pulse.

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T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT is in off state.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

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BIPOLAR FIELD-PROGRAMMABLE LOGIC ARRAY (16X8X48 FPLA) 82S101 (OPEN COLLECTOR) 82S100 (TRI-STATE)

82S100
82S101

OBJECTIVE SPECIFICATION

APRIL 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S100 (Tri-State Outputs) and the 82S101 (Open Collector Outputs) are Bipolar Programmable Logic Arrays, containing 48 Product terms (AND terms), and 8 output functions. Each output function can be programmed either true active-High (Fp), or true active-Low ($F\overline{p}$). The true state of the output functions is controlled via an output Sum (OR) Matrix by a logical combination of 16-input variables, or their complements, up to 48 terms.

Both devices are field-programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S100 and 82S101 are fully TTL compatible, and include a chip-enable clocking input for output deskewing and inhibit. They feature either Open Collector or Tri-State outputs for ease of expansion of product terms and/or input variables.

FEATURES

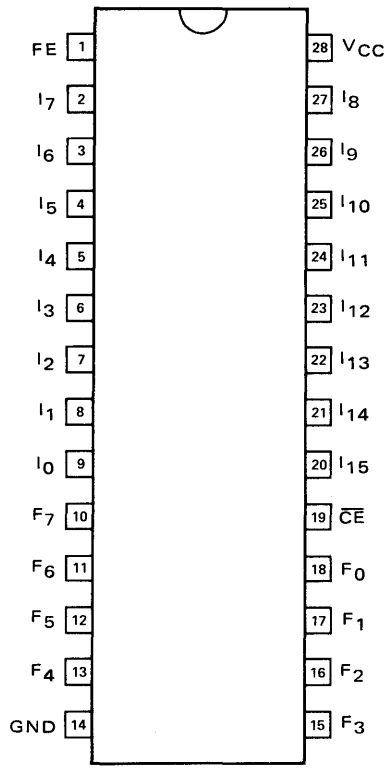
- FIELD PROGRAMMABLE (Ni-Cr LINK)
- INPUT VARIABLES – 16
- OUTPUT FUNCTIONS – 8
- PRODUCT TERMS – 48
- ADDRESS ACCESS TIME – 50ns, MAXIMUM
- POWER DISSIPATION – 600mW, TYPICAL
- INPUT LOADING – (–100μA), MAXIMUM
- OUTPUT OPTION:
  TRI-STATE OUTPUTS – 82S100
  OPEN COLLECTOR OUTPUTS – 82S101
- OUTPUT DISABLE FUNCTION:
  TRI-STATE – Hi-Z
  OPEN COLLECTOR – Hi
- CERAMIC DIP

APPLICATIONS

LARGE READ ONLY MEMORY
RANDOM LOGIC
CODE CONVERSION
PERIPHERAL CONTROLLERS
LOOK-UP AND DECISION TABLES
MICROPROGRAMMING
ADDRESS MAPPING
CHARACTER GENERATORS
SEQUENTIAL CONTROLLERS

PIN CONFIGURATION

I PACKAGE



TRUTH TABLE

LET:

$P_n = \Pi_0^{15} (k_m I_m + j_m \overline{I_m})$; k = 0, 1, X (Don't Care)

n = 0, 1, 2, ... , 47

where:

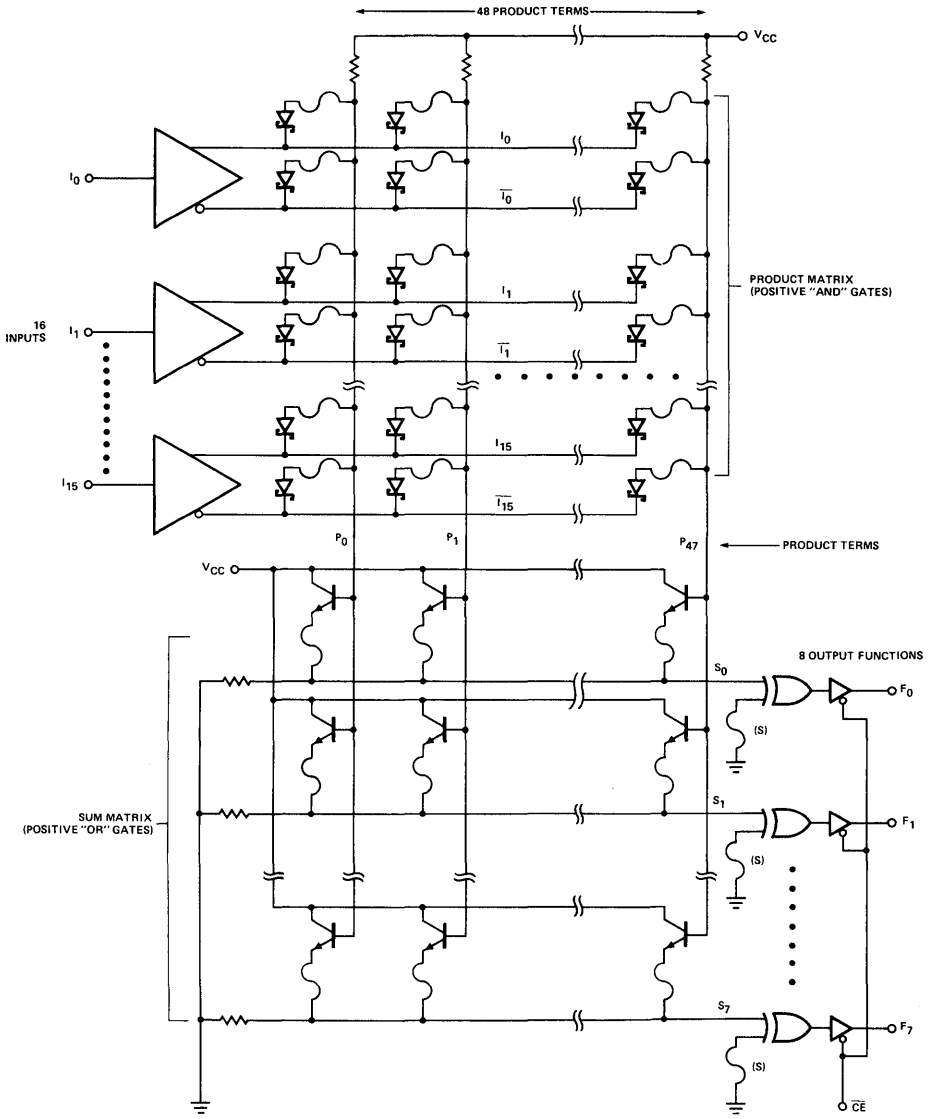
Unprogrammed state : $j_m = k_m = 0$

Programmed state : $j_m = \overline{k_m}$

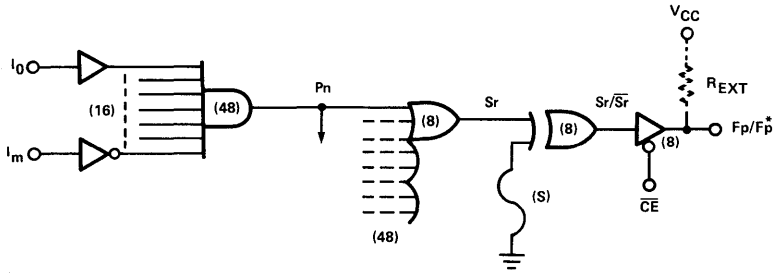
$S_r = f(\Sigma_0^{47} P_n)$; r $\equiv$ p = 0, 1, 2, ... , 7

MODE	P_n	$\overline{CE}$	F_p	F_p^*	$S_r \stackrel{?}{=} f(P_n)$
Disabled (82S101)	X	1	1	1	X
Disabled (82S100)			Hi-Z	Hi-Z	
Read	1	0	1	0	YES
	0	0	0	1	
	X	0	0	1	NO

BLOCK DIAGRAM



FPLA TYPICAL LOGIC PATH



NOTE:
FOR EACH OF THE 8 OUTPUTS, EITHER THE FUNCTION Fp (ACTIVE HIGH) OR $F\overline{p}^*$ (ACTIVE LOW) IS AVAILABLE, BUT NOT BOTH. THE REQUIRED FUNCTION POLARITY IS USER PROGRAMMABLE VIA FUSE (S).

$Pn = I_0 \overline{I_1}\,\overline{I_2}\,I_3 \ldots\ldots \overline{I_m}$
$Sr = P_0 + P_1 + P_2 + \ldots\ldots Pn$
$\overline{Sr} = \overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2} \bullet \ldots\ldots \overline{Pn}$
$Fp = (\overline{CE}) + (Sr) = (\overline{CE}) + (P_0 + P_1 + P_2 + \ldots\ldots Pn)$ @ S = SHORT
$F\overline{p}^* = (\overline{CE}) + (\overline{Sr}) = (\overline{CE}) + (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2} \bullet \ldots\ldots \overline{Pn})$ @ S = OPEN

ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S101)	+5.5	Vdc
V_O	Off-State Output Voltage (82S100)	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C$; $4.75V \leqslant V_{CC} \leqslant 5.25V$

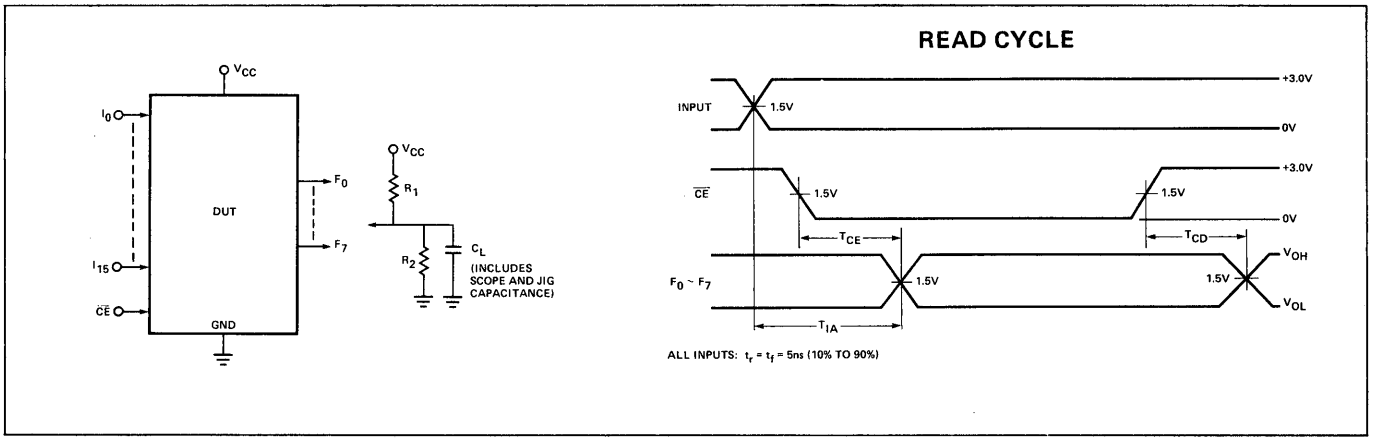
PARAMETER		TEST CONDITIONS		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT	NOTES
V_{IH}	High-Level Input Voltage	V_{CC} = 5.25V		2			V	1
V_{IL}	Low-Level Input Voltage	V_{CC} = 4.75V				0.8	V	1
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V, I_{IN} = −18mA			−0.8	−1.2	V	1, 7
V_{OH}	High-Level Output Voltage (82S100)	V_{CC} = 4.75V, I_{OH} = −2mA		2.4			V	1, 5
V_{OL}	Low-Level Output Voltage	V_{CC} = 4.75V, I_{OL} = 9.6mA			0.35	0.45	V	1, 8
I_{OLK}	Output Leakage Current (82S101)	V_{CC} = 5.25V	V_{OUT} = 5.25V		1	40	μA	6
$I_{O(OFF)}$	Hi-Z State Output Current (82S100)	V_{CC} = 5.25V	V_{OUT} = 5.25V		1	40	μA	6
		V_{CC} = 5.25V	V_{OUT} = 0.45V		−1	−40	μA	6
I_{IH}	High-Level Input Current	V_{IN} = 5.5V			<1	25	μA	
I_{IL}	Low-Level Input Current	V_{IN} = 0.45V			−10	−100	μA	
I_{OS}	Short-Circuit Output Current (82S100)	V_{CC} = 5.25V, V_{OUT} = 0V		−20		−70	mA	3, 7
I_{CC}	V_{CC} Supply Current (82S100, 82S101)	V_{CC} = 5.25V			120	170	mA	4
C_{IN}	Input Capacitance	V_{CC} = 5.0V	V_{IN} = 2.0V		5		pF	
C_O	Output Capacitance	V_{CC} = 5.0V	V_{OUT} = 2.0V		8		pF	6

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Duration of short circuit should not exceed one second.
4. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic "1" stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Test each output one at the time.
8. Measured with a programmed logic condition for which the output under test is at a "0" logic level. Output sink current is supplied thru a resistor to V_{CC}.

SWITCHING CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[2]	MAX	
Propagation Delay						
T_{IA}	Input to Output	C_L = 30pF		35	50	ns
T_{CD}	Chip Disable to Output	R_1 = 270		15	20	ns
T_{CE}	Chip Enable to Output	R_2 = 600		15	20	ns

AC TEST FIGURE AND WAVEFORM



NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, and T_A = +25°C.

OBJECTIVE PROGRAMMING PROCEDURE

The 82S100/101 are shipped in an unprogrammed state, characterized by:

A. All internal Ni-Cr links are intact.

B. Each product term (P-term) contains both true and complement values of every input variable I_m (P-terms always logically "FALSE").

C. The Sum Matrix contains all 48 P-terms.

D. The polarity of each output is set to active HIGH (F_p function).

E. All outputs are at a LOW logic level.

To program each of 8 Boolean logic functions of 16 true or complement variables, including up to 48 P-terms, follow the Program/Verify procedures for the Product Matrix, Sum Matrix, and Output Polarity outlined below.

OUTPUT POLARITY

PROGRAM ACTIVE LOW (F_p^* Function)

Program output polarity before programming Product Matrix and Sum Matrix. Program one output at the time.

1. Set GND (pin 14) to OV.
2. Do not apply power to the device (V_{CC}, pin 28, open).
3. Apply V_{OUT} = +18V to the appropriate output for 1ms, and return to OV.
4. Repeat step 3 to program other outputs.

VERIFY OUTPUT POLARITY

1. Set GND (pin 14) to OV, and V_{CC} (pin 28) to +5V.
2. Enable the chip by setting $\overline{CE}$ (pin 19) to LOW logic level.
3. Disable input variables by applying V_{IN} = +10V to all inputs I_0 through I_{15}.
4. Verify output polarity by sensing the logic state of outputs F_0 through F_7. All outputs at a HIGH logic level are programmed active HIGH (F_p function), while all outputs at a LOW logic level are programmed active LOW (F_p^* function).
5. Remove V_{IN} = +10V from inputs I_0 through I_{15}.

PRODUCT MATRIX

PROGRAM INPUT VARIABLE

Program one input at the time and one P-term at the time. All input variable links of unused P-terms are not required to be fused. However, unused input variables must be programmed as Don't Care for all programmed P-terms.

1. Set GND (pin 14) to OV, and V_{CC} (pin 28) to +5V.
2. Disable the chip by setting $\overline{CE}$ (pin 19) to HIGH logic level.
3. Disable input variables by applying V_{IN} = +10V to all inputs I_0 through I_{15}.
4. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to

outputs F_0 through F_5 with F_0 as LSB. Use standard TTL logic levels.

5a. If the P-term contains neither I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both I_0 and $\overline{I_0}$ links by executing both steps 5b and 5c, before continuing with step 7.

5b. If the P-term contains I_0, set to fuse the $\overline{I_0}$ link by lowering the input voltage to I_0 from V_{IN} = +10V to a HIGH logic level. Execute step 6.

5c. If the P-term contains $\overline{I_0}$, set to fuse the I_0 link by lowering the input voltage to I_0 from V_{IN} = +10V to a LOW logic level. Execute step 6.

6a. After 10μs delay, raise FE (pin 1) from 0V to +17V. The source must have a current limit of 250mA, and rise time of 10 to 50μs.

6b. After 10μs delay, pulse the $\overline{CE}$ input to +10V for a period of 1ms.

6c. After 10μs delay, return FE input to 0V.

7. Return input I_0 to a disable state by applying V_{IN} = +10V.

8. Repeat steps 5 through 7 for all other input variables.

9. Repeat steps 4 through 8 for all other P-terms.

10. Remove V_{IN} = +10V from all input variables.

VERIFY INPUT VARIABLE

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +5V.

2. Enable F_7 output by setting $\overline{CE}$ to +10V.

3. Disable input variables by applying V_{IN} = +10V to inputs I_0 through I_{15}.

4. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to outputs F_0 through F_5.

5. Interrogate input variable I_0 as follows:
   A. Lower the input voltage to I_0 from V_{IN} = +10V to a HIGH logic level, and sense the state of output F_7.
   B. Lower the input voltage to I_0 from a HIGH to a LOW logic level, and sense the logic state of output F_7.

The state of I_0 contained in the P-term is determined in accordance with the following truth table:

I_0	F_7	Input Variable State Contained In P-Term
0 1	1 0	$\overline{I_0}$
0 1	0 1	I_0
0 1	1 1	Dont Care
0 1	0 0	$(I_0), (\overline{I_0})$

Note that two tests are required to uniquely determine the state of the input variable contained in the P-term.

6. Return input I_0 to a disable state by applying V_{IN} = +10V.

7. Repeat steps 5 and 6 for all other input variables.

8. Repeat steps 4 through 7 for all other P-terms.

9. Remove V_{IN} = +10V from all input variables.

SUM MATRIX

PROGRAM PRODUCT TERM

Program one output at the time for one P-term at the time. All P_n links of unused P-terms in the Sum Matrix are not required to be fused.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +8.5V.

2. Disable the chip by setting $\overline{CE}$ (pin 19) to a HIGH logic level.

3. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5, with I_0 as LSB. Use standard TTL levels.

4a. If the P-term is contained in output function F_0 (F_0 = 1 or F_0^* = 0), go to step 6.

4b. If the P-term **is not** contained in output function F_0 (F_0 = 0 or F_0^* = 1), set to fuse the P_n link by applying V_{OUT} = +10V to output F_0.

5a. After 10μs delay, raise FE (pin 1) from 0V to +17V.

5b. After 10μs delay, pulse the $\overline{CE}$ input to +10V for a period of 1ms.

5c. After 10μs delay, return FE input to 0V.

6. Repeat steps 4 and 5 for all other output functions.

7. Repeat steps 3 through 6 for all other P-terms.

8. Remove +8.5V from V_{CC}.

VERIFY PRODUCT TERM

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +8.5V.

2. Enable the chip by setting $\overline{CE}$ (pin 19) to a LOW logic level.

3. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5, with I_0 as the LSB. Use standard TTL levels.

4. To determine the status of the P_n link in the Sum Matrix for each output function F_p or F_p^*, sense the state of outputs F_0 through F_7. The status of the link is given by the following truth table:

Output		P-term Link
Active HIGH (F_p)	Active LOW (F_p^*)	
0	1	FUSED
1	0	PRESENT

5. Repeat steps 3 and 4 for all other P-terms.

6. Remove +8.5V from V_{CC}.

signetics

2048-BIT BIPOLAR ROM (256x8 PROM)
4096-BIT BIPOLAR ROM (512x8 PROM)

82S114
82S115

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S114 and 82S115 are Schottky-clamped Read Only Memories, incorporating on-chip data output registers. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S114 and 82S115 are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S114 and 82S115 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature Tri-State outputs for optimization of word expansion in bussed organizations. A D-type latch is used to enable the Tri-State output drivers. In the TRANSPARENT READ mode, stored data is addressed by applying a binary code to the address inputs while holding STROBE high. In this mode the bit drivers will be controlled solely by $\overline{CE1}$ and CE2 lines. In the LATCHED READ mode, after the desired address is applied and both $\overline{CE1}$ and CE2 are enabled, data will enter the output latches following the positive transition of STROBE, and the data out lines will be locked into their last valid state following the negative transition of STROBE. The latches will remain set and the outputs enabled until the chip is disabled and STROBE is brought high.

Both 82S114 and 82S115 devices are available in the commercial temperature range. For the commercial temperature range, (0°C to +75°C) specify N82S114/115, I.

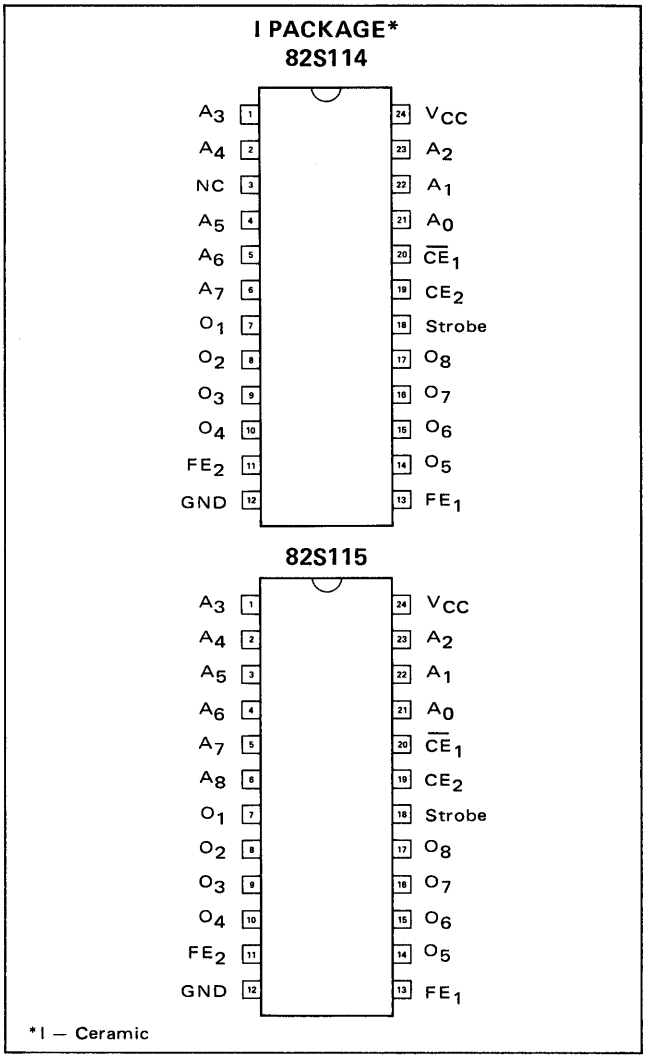
FEATURES

- **ORGANIZATION:**
  - **82S114 – 256 X 8**
  - **82S115 – 512 X 8**
- **ADDRESS ACCESS TIME – 60ns, MAXIMUM**
- **POWER DISSIPATION – 165μW/BIT, TYPICAL**
- **INPUT LOADING – (–100μA), MAXIMUM**
- **ON-CHIP ADDRESS DECODING**
- **ON-CHIP STORAGE LATCHES**
- **TRI-STATE OUTPUTS**
- **FAST PROGRAMMING – 5 SEC., MAXIMUM**
- **PIN COMPATIBLE TO N8204/N8205 ROMs**

APPLICATIONS

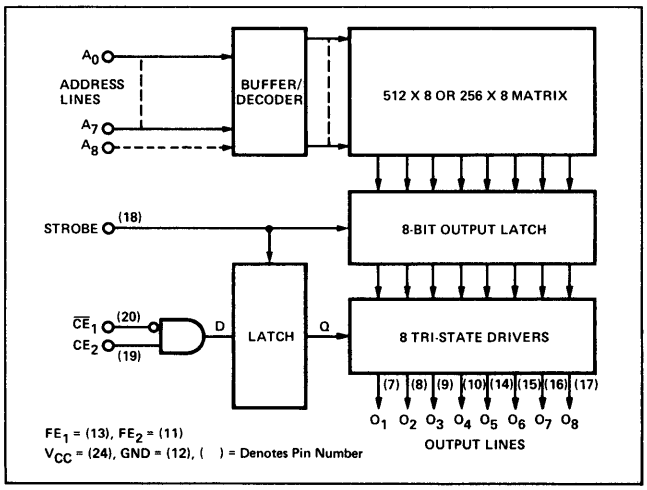
MICROPROGRAMMING
HARDWIRE ALGORITHMS
CHARACTER GENERATION
CONTROL STORE
SEQUENTIAL CONTROLLERS

PIN CONFIGURATION



*I – Ceramic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_O	Off-State Output Voltage	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25$

PARAMETER		TEST CONDITIONS	LIMITS[1]			UNIT
			MIN	TYP[2]	MAX	
I_{IL}	"0" Input Current	V_{IN} = 0.45V			−100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			25	μA
V_{IL}	"0" Level Input Voltage				.85	V
V_{IH}	"1" Level Input Voltage		2.0			V
V_{IC}	Input Clamp Voltage	I_{IN} = −18 mA		−0.8	−1.2	V
V_{OL}	"0" Output Voltage	I_{OUT} = 9.6 mA			0.5	V
V_{OH}	"1" Output Voltage	$\overline{CE_1}$ = "0", CE_2 = "1", I_{OUT} = −2 mA, "1" STORED	2.7	3.3		V
$I_{O(OFF)}$	HI-Z State Output Current	$\overline{CE_1}$ = "1" or CE_2 = 0, V_{OUT} = 5.5V			40	μA
		$\overline{CE_1}$ = "1" or CE_2 = 0, V_{OUT} = 0.5V			−40	μA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		5		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V, $\overline{CE_1}$ = "1" or CE_2 = 0		8		pF
I_{CC}	V_{CC} Supply Current			135	185	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 3)	−20		−70	mA

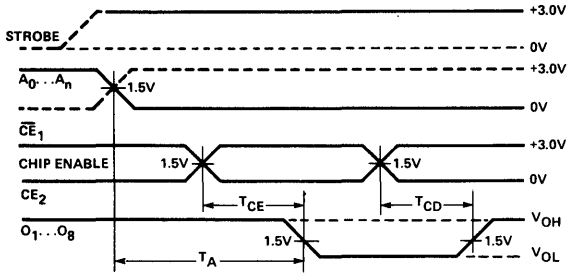
SWITCHING CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[2]	MAX	
T_{AA}	Address Access Time	LATCHED or TRANSPARENT READ		35	60	ns
T_{CE}	Chip Enable Access Time	R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF (Note 4)		20	40	ns
T_{CD}	Chip Disable Time			20	40	ns
T_{ADH}	Address Hold Time	LATCHED READ ONLY	0	−10		ns
T_{CDH}	Chip Enable Hold Time		10	0		ns
T_{SW}	Strobe Pulse Width		30	20		ns
T_{SL}	Strobe Latch Time	R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF (Note 5)	60	35		ns
T_{DL}	Strobe Delatch Time				30	ns
T_{CDS}	Chip Enable Set-up Time		40			ns

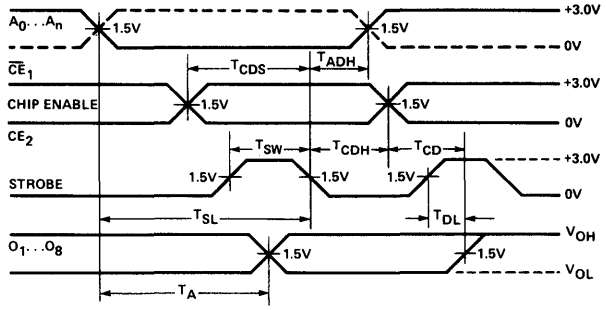
NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = +5.0V and T_A = +25°C.
3. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in "1" state.
4. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an "off" or high impedance state after it has been enabled.
5. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.

MEMORY TIMING

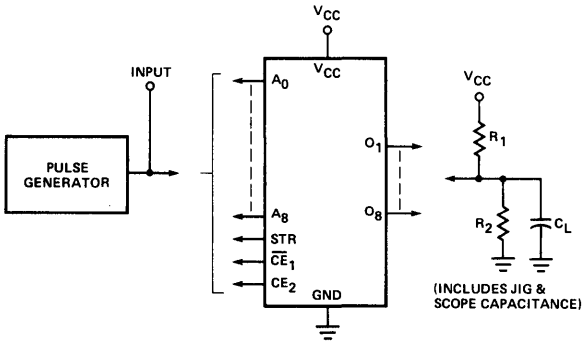
TRANSPARENT READ[5]
(Output Latches Not Used)



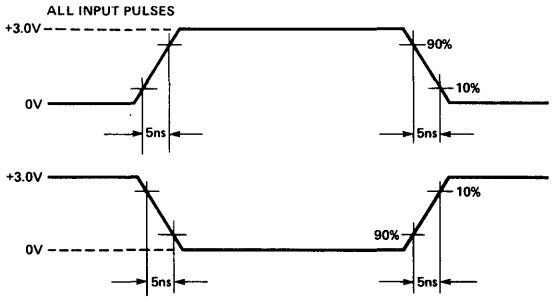
LATCHED READ[6]
(Output Latches Used)



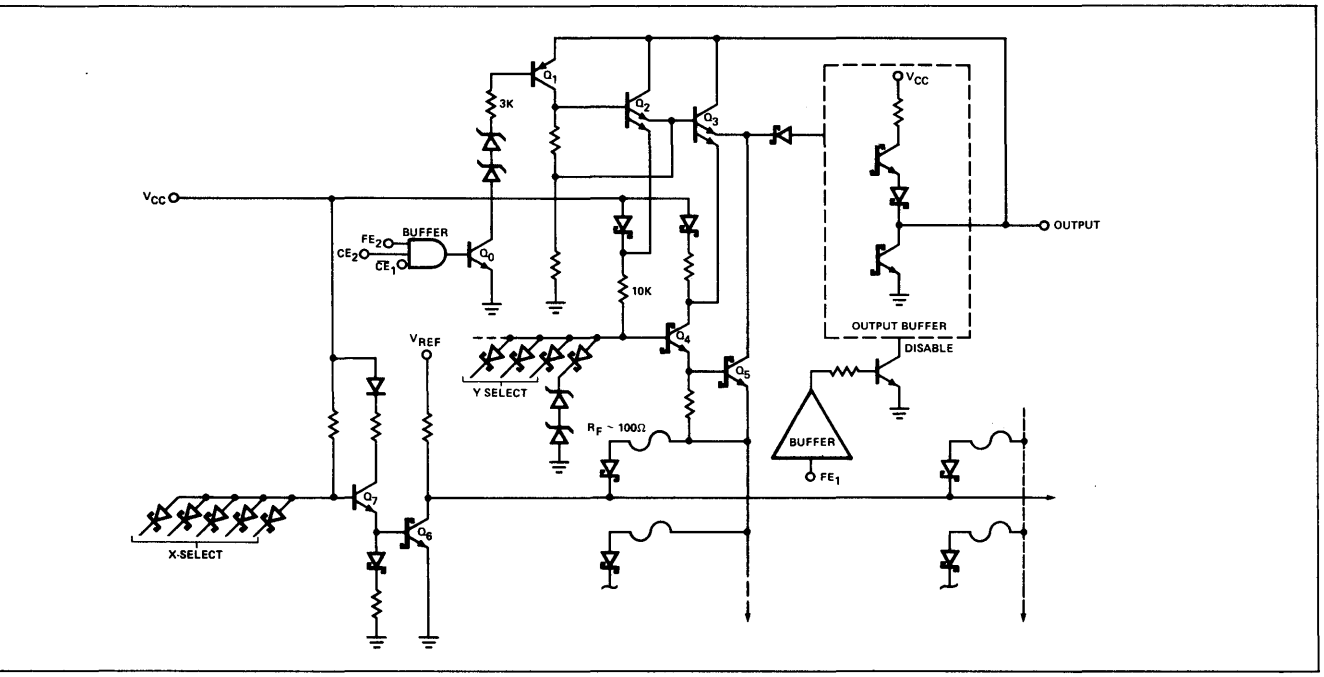
AC TEST LOAD AND WAVEFORMS



INPUT PULSES



TYPICAL FUSING PATH



RECOMMENDED PROGRAMMING PROCEDURE

The 82S114/115 are shipped with all bits at logical "0" (low). To write logical "1", proceed as follows:

SET-UP

a. Apply GND to pin 12.

b. Terminate all device outputs with a 10KΩ resistor to V_{CC}.

c. Set $\overline{CE}$ 1 to logic "0", and CE2 to logic "1" (TTL levels).

d. Set Strobe to logic "1" level.

PROGRAM-VERIFY SEQUENCE

Step 1 Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL "1" and "0" logic levels to the device address inputs.

Step 2 After 10μs delay, apply to FE1 (pin 13) a voltage source of +5.0 ± 0.5V, with 10 mA sourcing current capability.

Step 3 After 10μs delay, apply a voltage source of +17.0 ± 1.0V to the output to be programmed. The source must have a current limit of 200 mA. Program one output at the time.

Step 4 After 10μs delay, raise FE2 (pin 11) from 0V to +5.0 ± 0.5V for a period of 1ms, and then return to 0V. Pulse source must have a 10 mA sourcing current capability.

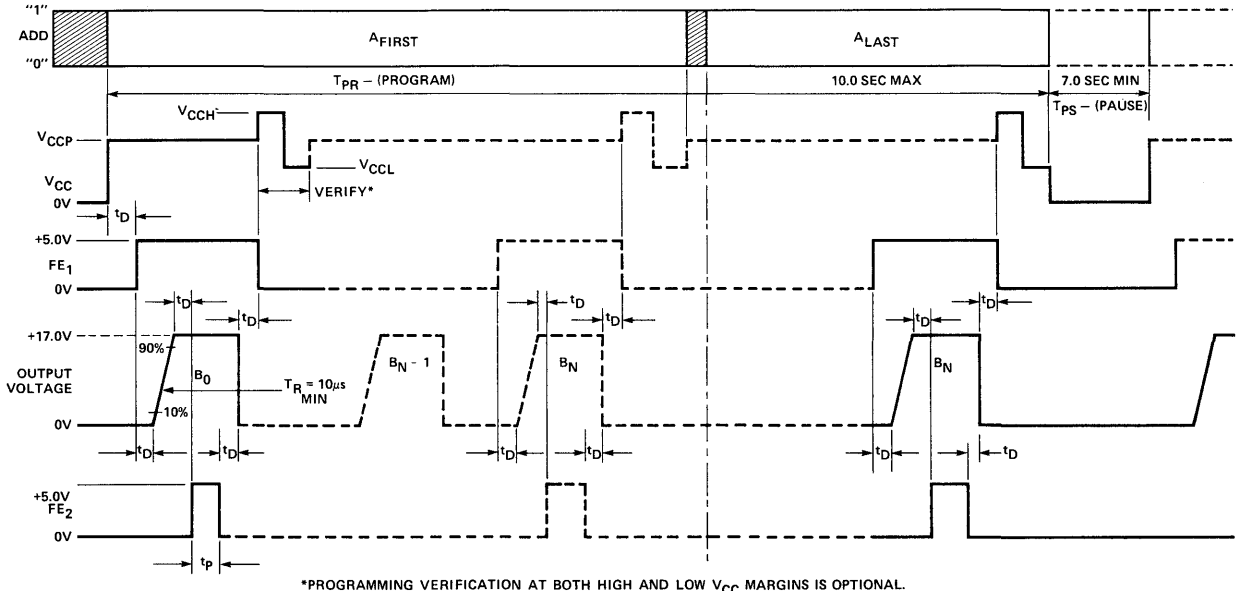
Step 5 After 10μs delay, remove +17.0V supply from programmed output.

Step 6 To verify programming, after 10μs delay, return FE1 to 0V. Raise V_{CC} to V_{CCH} = +5.5 ± .2V. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the "1" state.

Step 7 Raise V_{CC} to V_{CCP}, and repeat steps 2 through 6 to program other bits at the same address.

Step 8 Repeat steps 1 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



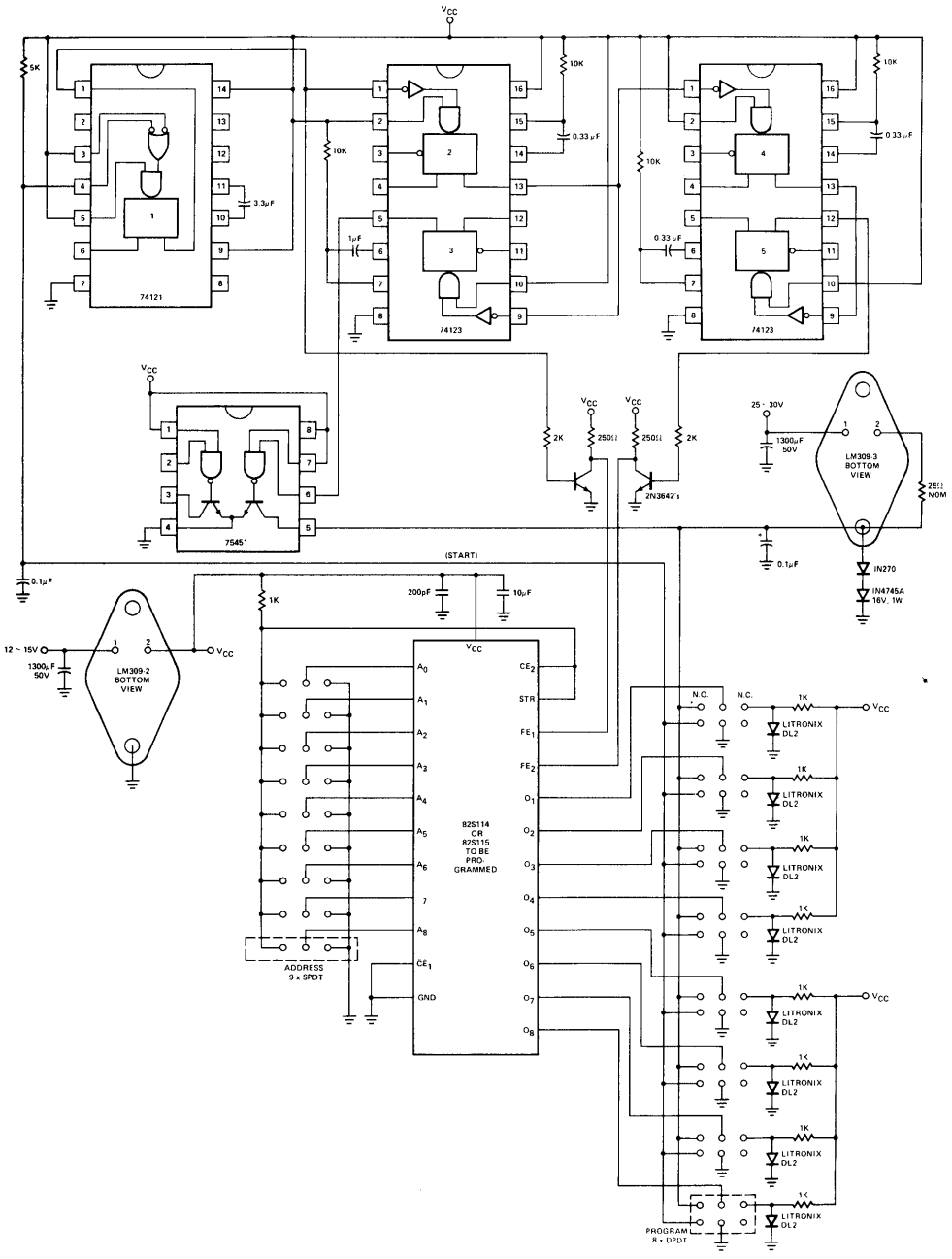
*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^{\circ}C$

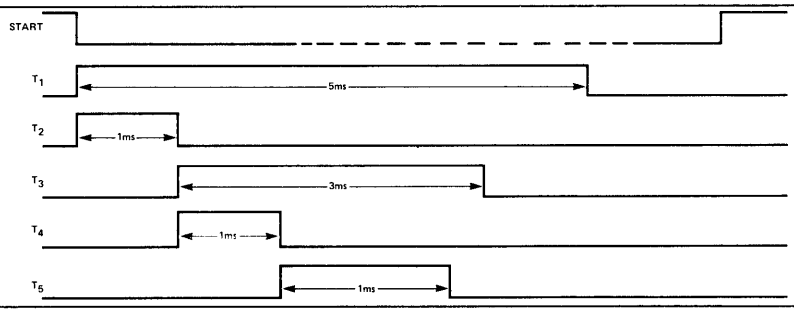
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	$I_{CCP} = 200 \pm 25$ mA (Transient or steady state)	4.75	5.0	5.25	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +5.0 \pm .25V$	175	200	225	mA
Input Voltage						
V_{IL}	Low Level Input Voltage		0	0.4	0.8	V
V_{IH}	High Level Input Voltage		2.4		5.5	V
Input Current (FE_1 & FE_2 Only)						
I_{IL}	Low Level Input Current	$V_{IL} = +0.45V$			-100	μA
I_{IH}	High Level Input Current	$V_{IH} = +5.5V$			10	mA
Input Current (Except FE_1 & FE_2)						
I_{IL}	Low Level Input Current	$V_{IL} = +0.45V$			-100	μA
I_{IH}	High Level Input Current	$V_{IH} = +5.5V$			25	μA
V_{OUT}[2]	Output Programming Voltage	$I_{OUT} = 200 \pm 20$ mA (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17 \pm 1V$	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
t_P	FE_2 Programming Pulse Width		1		1.5	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			10	sec
T_{PS}	Programming Pause	$V_{CC} = 0V$	7			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				60	%

NOTES:
1. Bypass V_{CC} to GND with a 0.01 μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 60% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period (V_{CC} = 0V) of 3 mS.

82S114/115 MANUAL PROGRAMMER



TIMING SEQUENCE



signetics

256-BIT BIPOLAR RAM (256x1 RAM) (82S116 TRI-STATE) (82S117 OPEN COLLECTOR)

82S116
82S117

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S116 and 82S117 are Schottky clamped TTL, read/write memory arrays organized as 256 words of one bit each. They feature either open collector or tri-state output options for optimization of word expansion in bussed organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading to 25μA for a "1" level, and -100μA for a "0" level.

During WRITE operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of WRITE-READ cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a WRITE cycle.

Both devices have fast read access and write cycle times, and thus are ideally suited in high-speed memory applications such as "Cache", buffers, scratch pads, writable control stores, etc.

Both 82S116 and 82S117 devices are available in the commercial temperature range. For the commercial temperature range, (0°C to +75°C) specify N82S116/117, B or F.

FEATURES

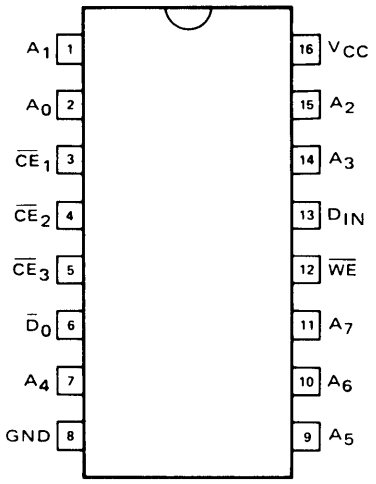
- ORGANIZATION – 256 X 1
- ADDRESS ACCESS TIME – 40ns, MAXIMUM
- WRITE CYCLE TIME – 25ns, MAXIMUM
- POWER DISSIPATION – 1.5mW/BIT. TYPICAL
- INPUT LOADING – (-100μA) MAXIMUM
- OUTPUT FOLLOWS COMPLEMENT OF DATA INPUT DURING WRITE
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTION:
  - TRI-STATE – 82S116
  - OPEN COLLECTOR – 82S117
- 16 PIN CERAMIC DIP

APPLICATIONS

BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK
SCRATCH PAD

PIN CONFIGURATION

B, F PACKAGE*



*B – Plastic
C – Cerdip

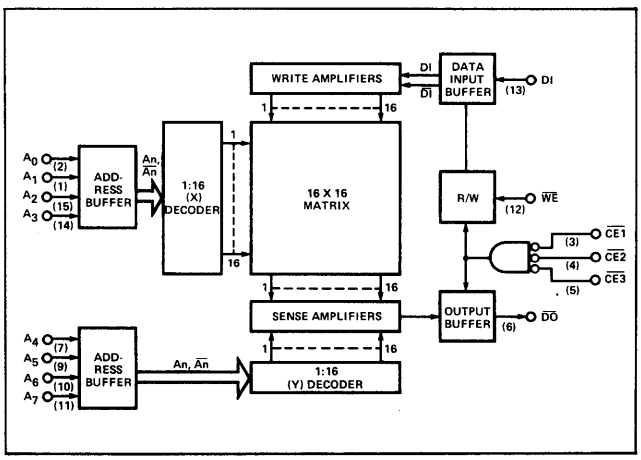
TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
				82S116	82S117
READ	0	1	X	STORED $\overline{DATA}$	STORED $\overline{DATA}$
WRITE "0"	0	0	0	1	1
WRITE "1"	0	0	1	0	0
DISABLED	1	X	X	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OUT}	High Level Output Voltage (82S117)	+5.5	Vdc
V_O	Off-State Output Voltage (82S116)	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT	NOTES
V_{IH}	High-Level Input Voltage	V_{CC} = 5.25V		2.0			V	
V_{IL}	Low-Level Input Voltage	V_{CC} = 4.75V				0.85	V	1
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V, I_{IN} = −12 mA			−1.0	−1.5	V	1,8
V_{OH}	High-Level Output Voltage (82S116)	V_{CC} = 4.75V, I_{OH} = −3.2 mA		2.6			V	1,6
V_{OL}	Low-Level Output Voltage	V_{CC} = 4.75V, I_{OL} = 16 mA			0.35	0.45	V	1,7
I_{OLK}	Output Leakage Current (82S117)	V_{OUT} = 5.5V			1	40	μA	5
$I_{O(OFF)}$	HI-Z State Output Current (82S116)	V_{OUT} = 5.5V			1	40	μA	5
		V_{OUT} = 0.45V			−1	−40	μA	5
I_{IH}	High-Level Input Current	V_{CC} = 5.25V, V_{IN} = 5.5V			1	25	μA	8
I_{IL}	Low-Level Input Current	V_{CC} = 5.25V, V_{IN} = 0.45V			−10	−100	μA	8
I_{OS}	Short-Circuit Output Current (82S116)	V_{CC} = 5.25V, V_O = 0V		−20		−70	mA	3
I_{CC}	V_{CC} Supply Current (82S116)	V_{CC} = 5.25V			80	115	mA	4
	V_{CC} Supply Current (82S117)	V_{CC} = 5.25V			80	115	mA	4
C_{IN}	Input Capacitance	V_{IN} = 2.0V	V_{CC} = 5.0V		5		pF	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V	V_{CC} = 5.0V		8		pF	

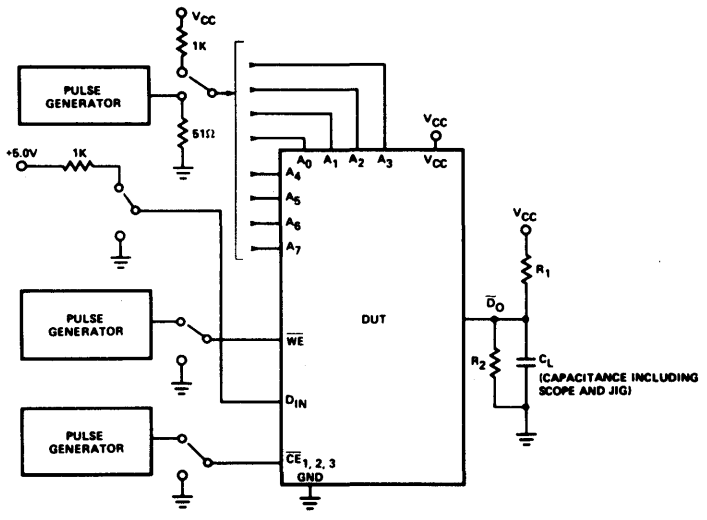
NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. Duration of the short-circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
6. Measured with a logic "0" stored and V_{IL} applied to $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{CE_3}$.
7. Measured with a logic "1" stored. Output sink current is supplied through a resistor to V_{CC}.
8. Test each input one at the time.

SWITCHING CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

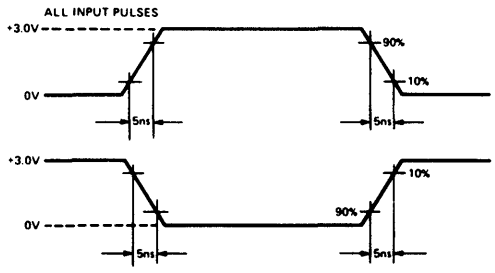
PARAMETER		TEST CONDITIONS	LIMITS			UNIT	NOTE
			MIN	TYP[1]	MAX		
Propagation Delays							
T_{AA}	Address Access Time	$R_1 = 270\Omega$ $R_2 = 600\Omega$ $C_L = 30pF$		30	40	ns	
T_{CE}	Chip Enable Access Time			15	25	ns	
T_{CD}	Chip Enable Output Disable Time			15	25	ns	
T_{WD}	Write Enable to Output Disable Time			30	40	ns	
Write Set-up Times							
T_{WSA}	Address to Write Enable		0	-5		ns	
T_{WSD}	Data In to Write Enable		25	15		ns	
T_{WSC}	$\overline{CE}$ to Write Enable		0	-5		ns	
Write Hold Times							
T_{WHA}	Address to Write Enable		0	-5		ns	
T_{WHD}	Data In to Write Enable		0	-5		ns	
T_{WHC}	$\overline{CE}$ to Write Enable		0	-5		ns	
T_{WP}	Write Enable Pulse Width		25	15		ns	2

AC TEST LOAD

LOADING CONDITION



INPUT PULSES



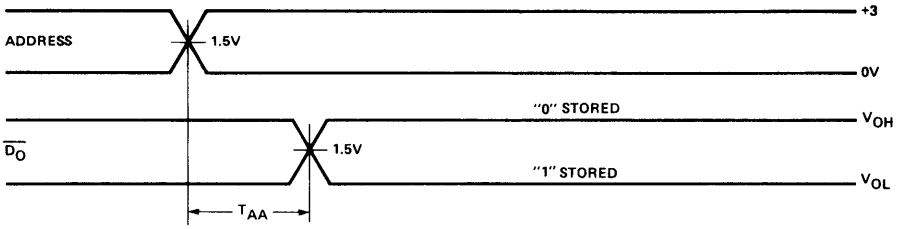
MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5V LEVEL OF INPUTS AND OUTPUT.

NOTES:
1. Typical values are at $V_{CC} = +5.0V$, and $T_A = +25°C$.
2. Minimum required to guarantee a WRITE into the slowest bit.

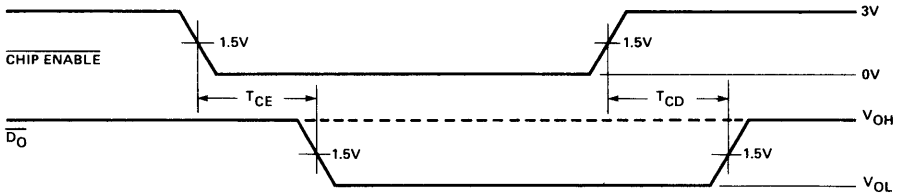
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

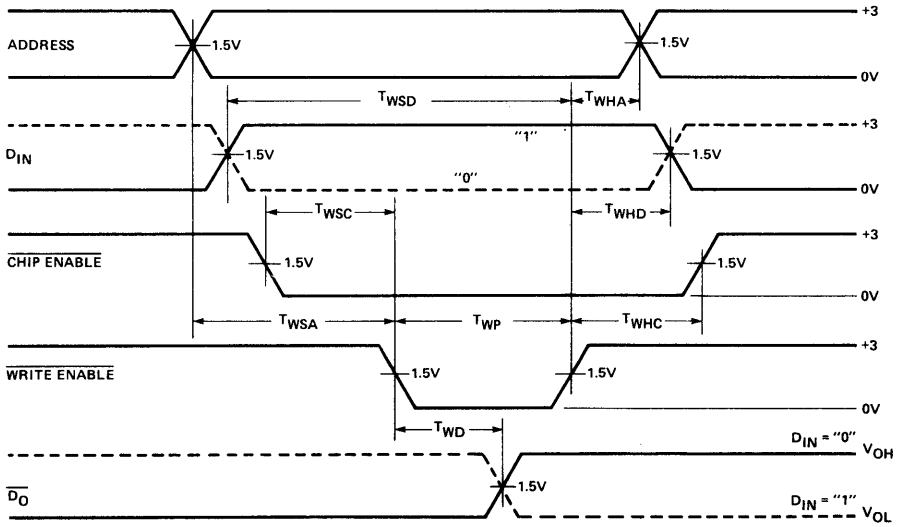
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT reflects complement of DATA INPUT.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

signetics

1024-BIT BIPOLAR PROGRAMMABLE ROM (256x4 PROM)

82S126
82S129

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S126 (Open Collector Outputs) and the 82S129 (Tri-State Outputs) are Bipolar 1024-Bit Read Only Memories, organized as 256 words by 4 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S126 and 82S129 devices are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S126 and 82S129 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S126 and 82S129 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S126/129, B or F. For the military temperature range (−55°C to +125°C) specify S82S126/129, F only.

FEATURES

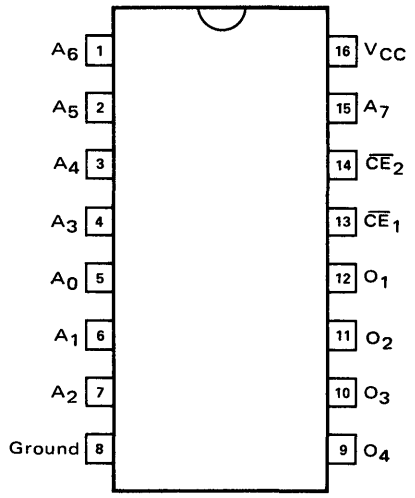
- ORGANIZATION – 256 X 4
- ADDRESS ACCESS TIME:
  - S82S126/129 – 70ns, MAXIMUM
  - N82S126/129 – 50ns, MAXIMUM
- POWER DISSIPATION – 0.5mW/BIT TYPICAL
- INPUT LOADING:
  - S82S126/129 – (−150μA) MAXIMUM
  - N82S126/129 – (−100μA) MAXIMUM
- TWO CHIP ENABLE INPUTS
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTION:
  - OPEN COLLECTOR – 82S126
  - TRI-STATE – 82S129
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- 16-PIN CERAMIC DIP

APPLICATIONS

PROTOTYPING/VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE
RANDOM LOGIC
CODE CONVERSION

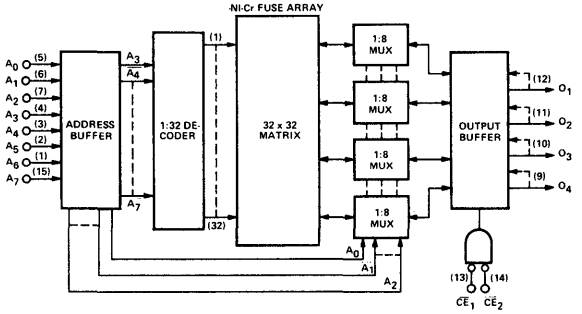
PIN CONFIGURATION

B, F PACKAGE*



*B – Plastic
F – Cerdip

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S126)	+5.5	Vdc
V_O	Off-State Output Voltage (82S129)	+5.5	Vdc
T_A	Operating Temperature Range		
	(N82S126/129)	0° to +75°	°C
	(S82S126/129)	-55° to +125°	°C
T_{stg}	Storage Temperature Range	-65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S126/S82S129 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S126/N82S129 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1]	S82S126/129			N82S126/129			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{OL}	"0" Output Voltage	I_{OUT} = 16mA			0.5			0.5	V
I_{OLK}	Output Leakage Current (82S126)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 5.5V			60			40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 5.5V			60			40	μA
		$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 0.5V			-60			-40	μA
V_{OH}	"1" Output Voltage (82S129)	$\overline{CE}_1$ = $\overline{CE}_2$ = "0", I_{OUT} = -2.0mA, "1" STORED	2.4			2.4			V
C_{IN}	Input Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, V_{CC} = 5.0V		8			8		pF
I_{IL}	"0" Input Current	V_{IN} = 0.45V			-150			-100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			50			40	μA
V_{IL}	"0" Level Input Voltage				.80			.85	V
V_{IH}	"1" Level Input Voltage		2.0			2.0			V
I_{CC}	V_{CC} Supply Current			105	125		105	120	mA
V_{IC}	Input Clamp Voltage	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	V
I_{OS}	Output Short Circuit Current (82S129)	V_{OUT} = 0V	-15		-85	-20		-70	mA

SWITCHING CHARACTERISTICS

S82S126/129 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S126/129 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S82S126/129			N82S126/129			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
	Propagation Delay								
T_{AA}	Address to Output	C_L = 30pF, R_1 = 270Ω, R_2 = 600Ω		35	70		35	50	ns
T_{CD}	Chip Disable to Output			15	35		15	20	ns
T_{CE}	Chip Enable to Output			15	35		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

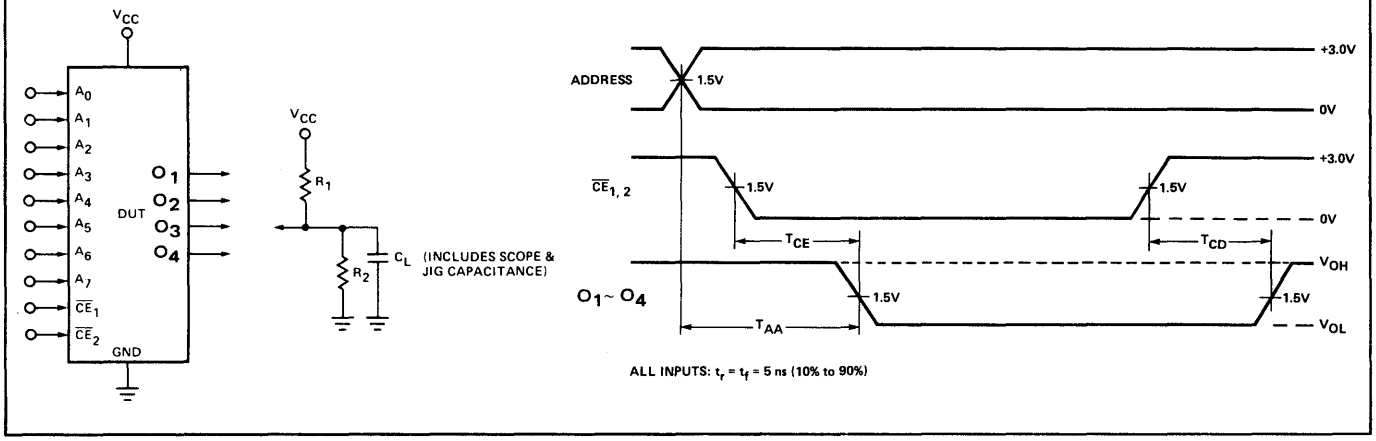
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	$I_{CCP} = 350 \pm 50mA$ (Transient or steady state)	8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +8.75 \pm .25V$	300	350	400	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.8	V
Input Current						
I_{IH}	Logical "1"	$V_{IH} = +5.5V$			50	μA
I_{IL}	Logical "0"	$V_{IL} = +0.4V$			-500	μA
V_{OUT}[2]	Output Programming Voltage	$I_{OUT} = 200 \pm 20mA$ (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17 \pm 1V$	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
t_P	$\overline{CE}$ Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0V$	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

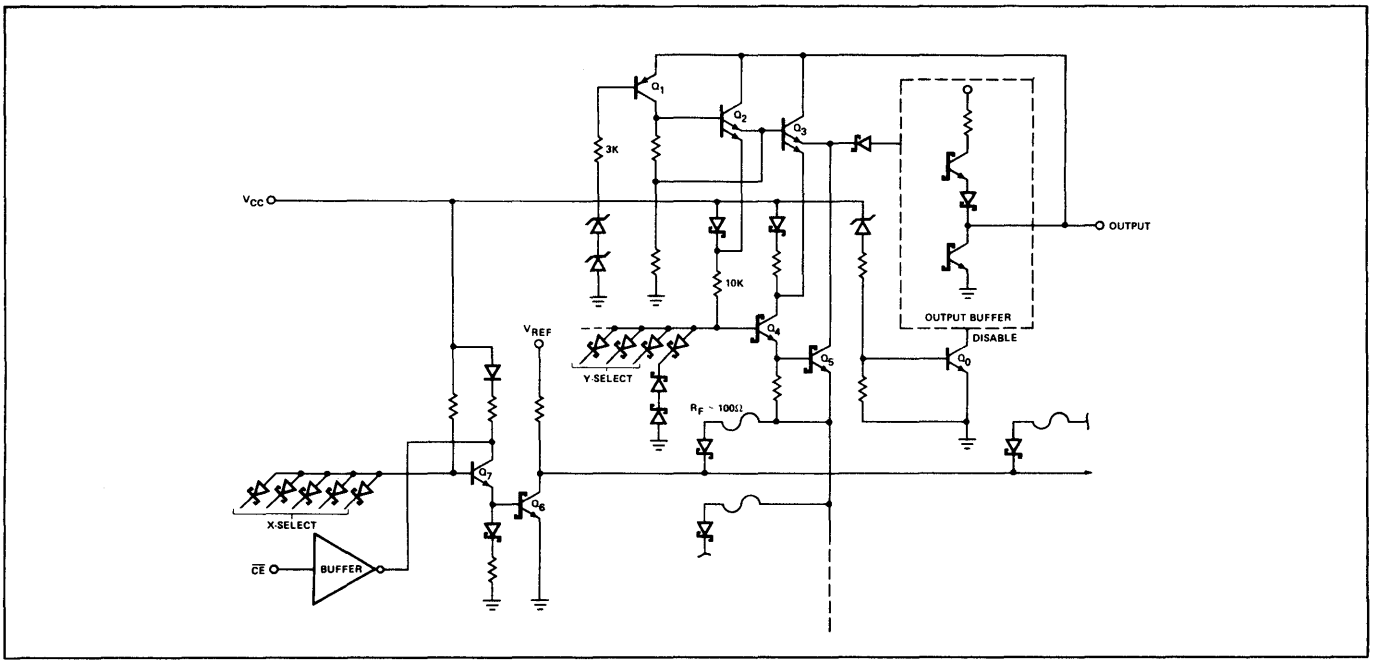
1. Terminate all device outputs with a 10KΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$.
3. After 10μs delay, apply $V_{OUT} = +17 \pm 1V$ to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse both $\overline{CE}$ inputs to logic "0" for 1 to 2 ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to $V_{CCH} = +5.5 \pm .2V$, and apply a logic "0" level to both $\overline{CE}$ inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2V$, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

NOTES:
1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period ($V_{CC} = 0V$) of 4ms.

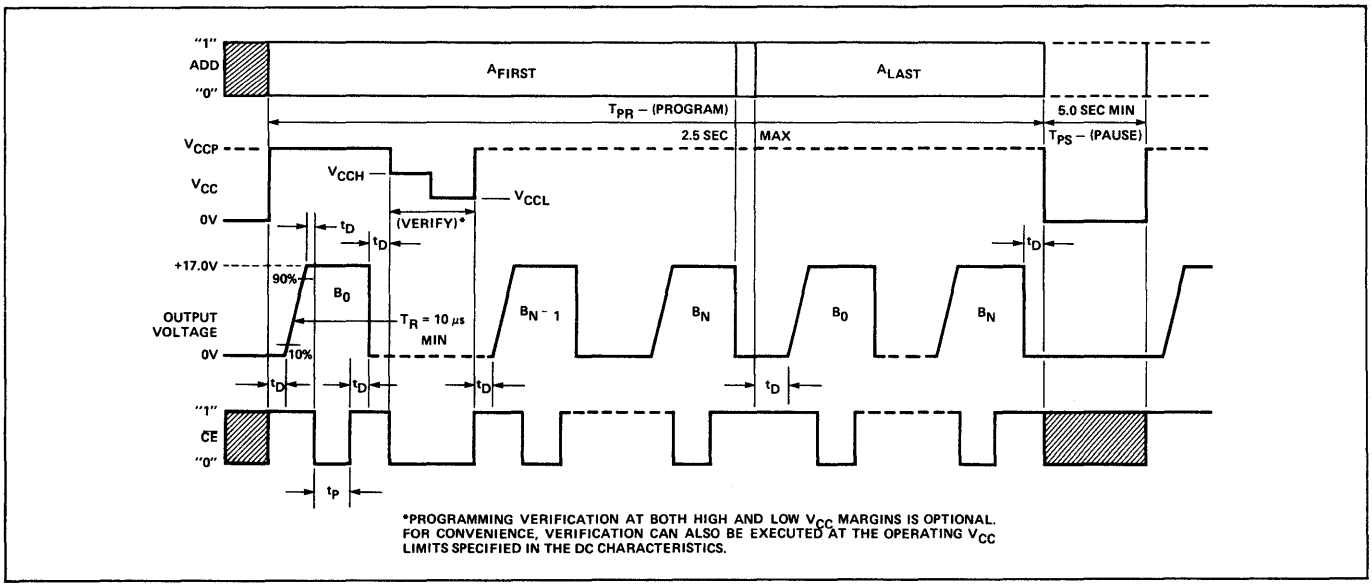
AC TEST FIGURE AND WAVEFORM



TYPICAL FUSING PATH

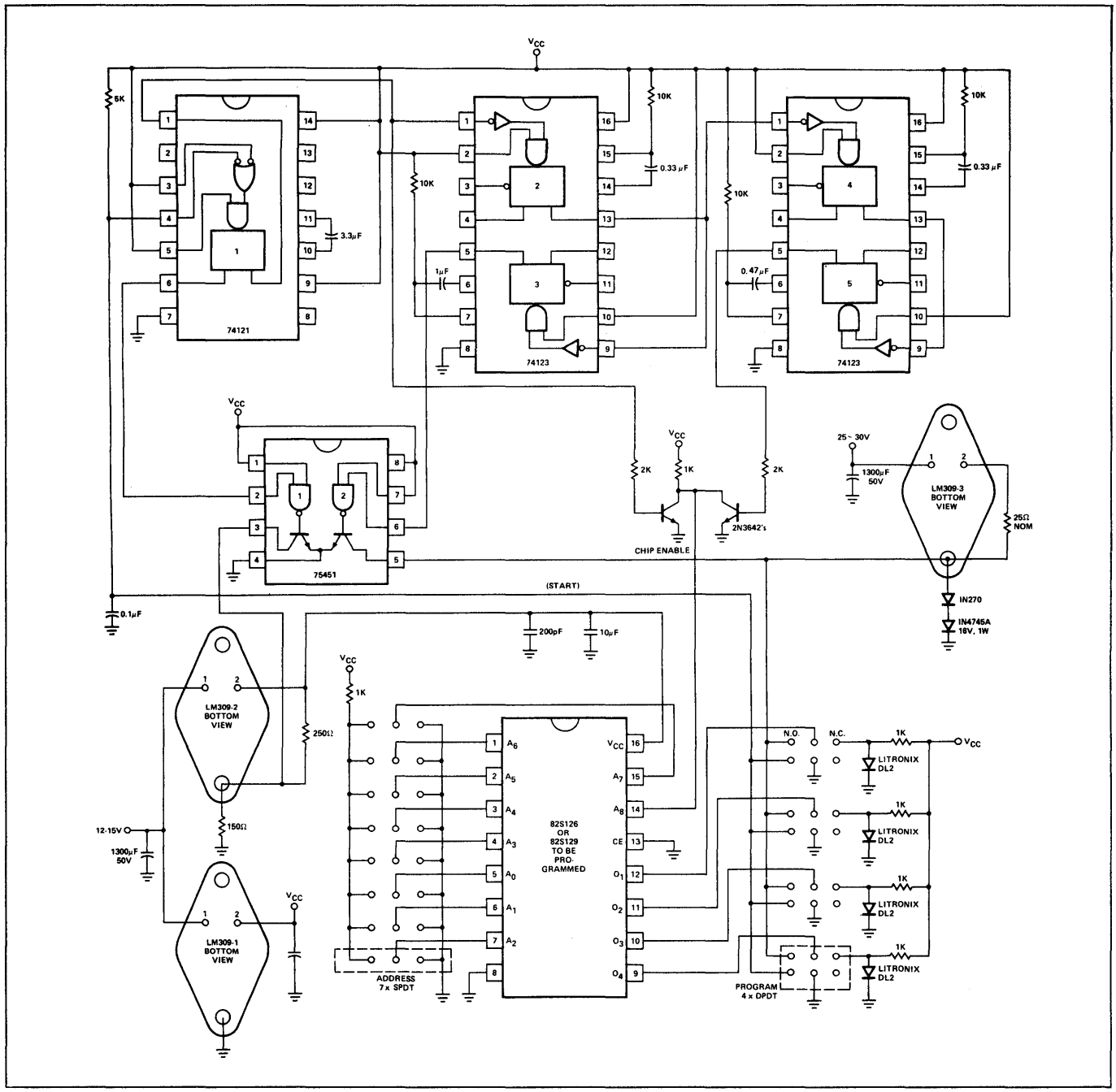


TYPICAL PROGRAMMING SEQUENCE

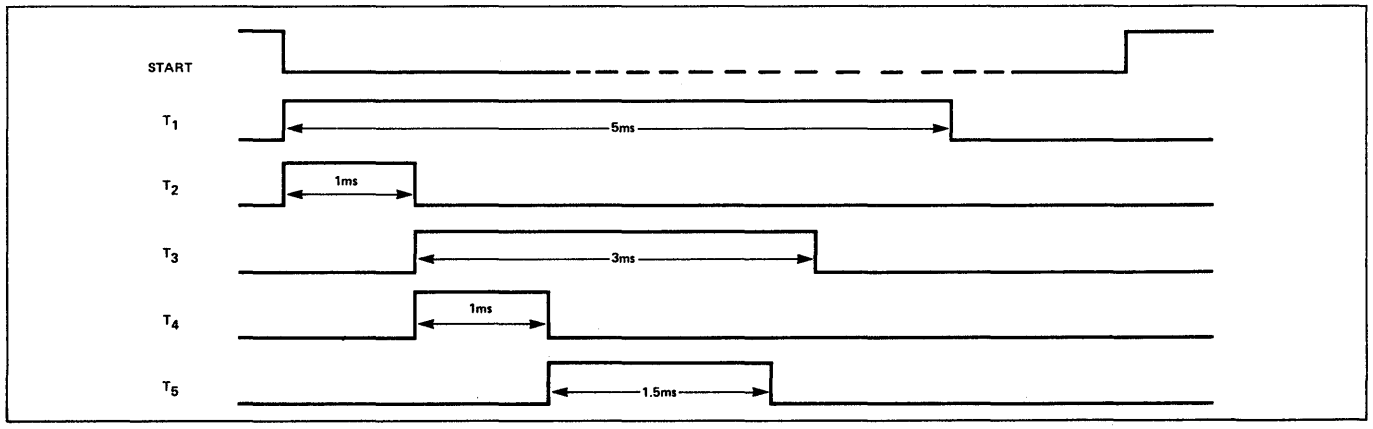


*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

MANUAL PROGRAMMER



TIMING SEQUENCE



DESCRIPTION

The 8T26A/28 consists of four pairs of Tri-State logic elements configured as Quad Bus Drivers/Receivers along with separate buffered receiver enable and driver enable lines. This single IC Quad Transceiver design distinguishes the 8T26A/28 from conventional multi-IC implementations. In addition, the 8T26/28's ultra high speed while driving heavy bus capacitance (300pF) makes these devices particularly suitable for memory systems and bidirectional data buses.

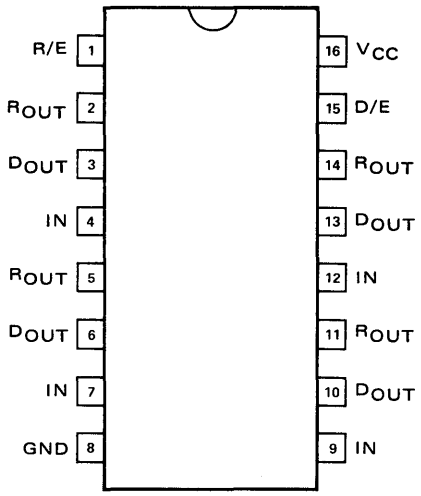
Both the Driver and Receiver gates have Tri-State outputs and low-current PNP inputs. Tri-State outputs provide the high switching speeds of totempole TTL circuits while offering the bus capability of open collector gates. PNP inputs reduce input loading to 200μA maximum.

FEATURES

- 8T26A HAS INVERTING OUTPUTS
- 8T28 HAS NON-INVERTING OUTPUTS
- SCHOTTKY-CLAMPED TTL
- TRI-STATE OUTPUTS (40mA CURRENT SINK)
- LOW CURRENT PNP INPUTS
- SCHOTTKY INPUT CLAMP DIODES
- HIGH SPEED (20ns WITH 300pF LOAD)

PIN CONFIGURATION

B, F PACKAGE

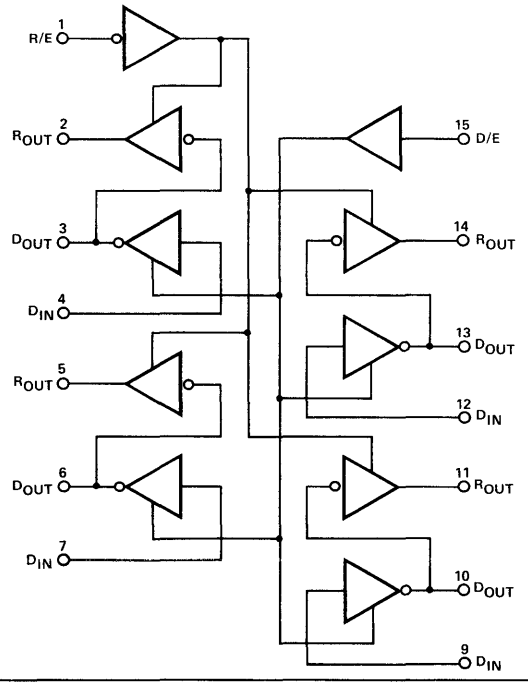


APPLICATIONS

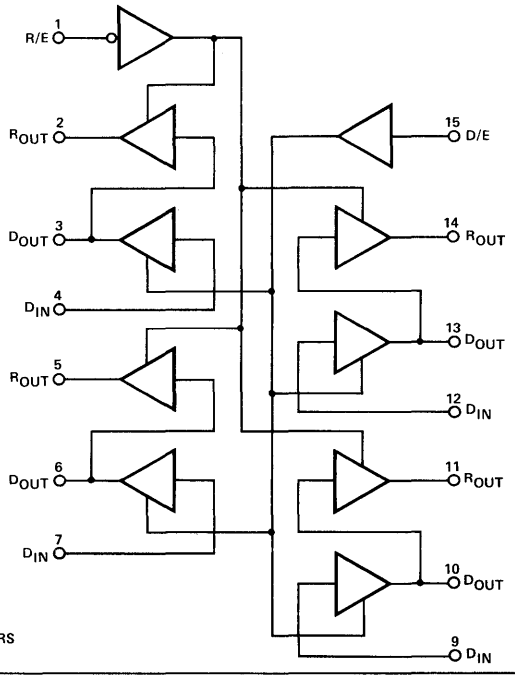
HALF-DUPLEX DATA TRANSMISSION
MEMORY INTERFACE BUFFERS
DATA ROUTING IN BUS ORIENTED SYSTEMS
HIGH CURRENT DRIVERS
MOS/CMOS-TO-TTL INTERFACE

LOGIC DIAGRAM

8T26A – INVERTING OUTPUT (TRI-STATE)



8T28 – NON-INVERTING OUTPUT (TRI-STATE)



VCC = (16)
GND = (8)
( ) = DENOTES PIN NUMBERS

ELECTRICAL CHARACTERISTICS

Commercial: V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C
Military: V_{CC} = 5.0V ± 10%, T_A = −55°C to +125°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Driver						
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−200	μA
I_{IL}	Low Level Input Current (Disabled)	V_{IN} = 0.4V			−25	μA
I_{IH}	High Level Input Current (D_{IN}, D_E)	V_{IN} = V_{CC} MAX			25	μA
V_{OL}	Low Level Output Voltage (Pins 3, 6, 10, 13)	I_{OUT} = 48mA (Note 8)			0.5	V
V_{OH}	High Level Output Voltage (Pins 3, 6, 10, 13)	I_{OUT} = −10mA, V_{CC} = V_{CC} MIN (Note 7)	2.4			V
I_{OS}	Short Circuit Output Current (Pins 3, 6, 10, 13)	V_{OUT} = 0V, V_{CC} = V_{CC} MAX (Note 12)	−50		−150	mA
Receiver						
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−200	μA
I_{IH}	High Level Input Current (R_E)	V_{IN} = V_{CC} MAX			25	μA
V_{OL}	Low Level Output Voltage	I_{OUT} = 20mA (Note 8)			0.5	V
V_{OH}	High Level Output Voltage (Pins 2, 5, 11, 14)	I_{OUT} = −100μA, V_{CC} = 5.0V I_{OUT} = −2.0mA (Note 7)	3.5 2.4			V V
I_{OS}	Short Circuit Output Current (Pins 2, 5, 11, 14)	V_{OUT} = 0V, V_{CC} = V_{CC} MAX	−30		−75	mA
Both Driver and Receiver						
V_{TL}	Low Level Input Threshold Voltage		0.85			V
V_{TH}	High Level Input Threshold Voltage				2	V
	Low Level Output Off Leakage Current	V_{OUT} = 0.5V			−100	μA
	High Level Output Off Leakage Current	V_{OUT} = 2.4V			100	μA
V_I	Input Clamp Voltage	I_{IN} = −12mA			−1.0	V
	Power/Current Consumption 8T26 8T28	 V_{CC} = V_{CC} MAX V_{CC} = V_{CC} MAX			 457/87 578/110	 mW/mA mW/mA

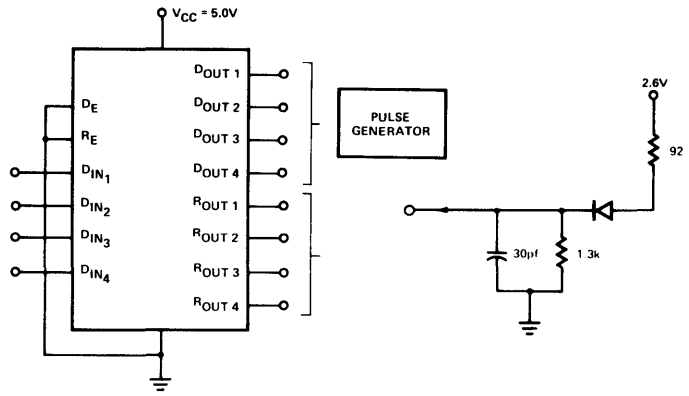
SWITCHING CHARACTERISTICS

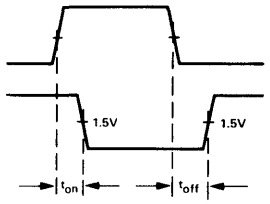
PARAMETER		TEST CONDITIONS	8T26A MAX	8T28 MAX	UNIT
Propagation Delay					
t_{ON}	D_{OUT} to R_{OUT}	C_L = 30pF, Note 9	14	17	ns
t_{OFF}	D_{OUT} to R_{OUT}		14	17	
t_{ON}	D_{IN} to D_{OUT}	C_L = 300pF, Note 9	14	17	ns
t_{OFF}	D_{IN} to D_{OUT}		14	17	
Data Enable to Data Output					
t_{PZL}	High Z to O	C_L = 300pF, Note 9	25	28	ns
t_{PLZ}	O to High Z		20	23	
Receiver Enable to Receiver Output					
t_{PZL}	High Z to O	C_L = 30pF, Note 9	20	23	ns
t_{PLZ}	O to High Z		15	18	

NOTES:
1. All voltage measurements are referenced to the ground terminal.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1"; "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings.
6. Measurements apply to each output and the associated data input independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC test circuits.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. V_{CC} = 5.25V.
12. Do not ground more than one output at a time.

AC TEST CIRCUITS AND WAVEFORMS

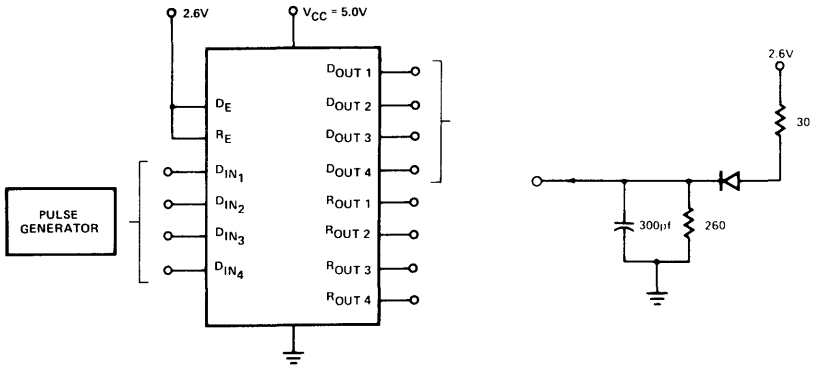
PROPAGATION DELAY (D_{OUT} TO R_{OUT})

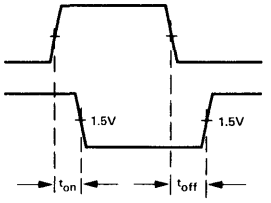




INPUT PULSE:
$t_r = t_f$ = 5ns (10% to 90%)
freq = 10MHz (50% duty cycle)
Amplitude = 2.6V

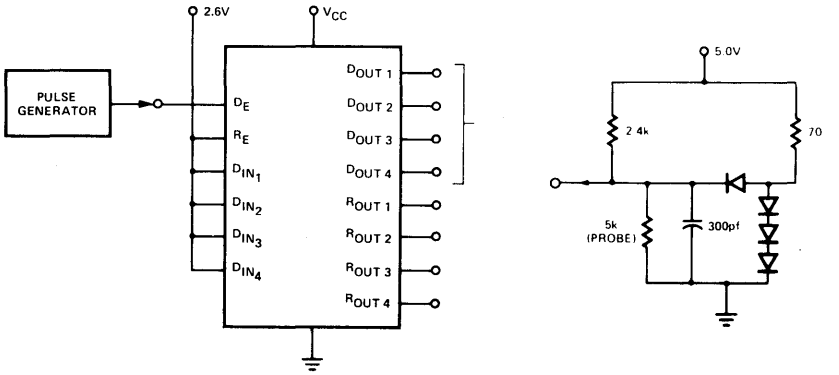
PROPAGATION DELAY (D_{IN} TO D_{OUT})

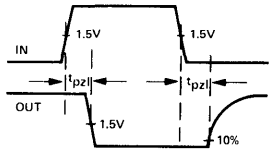




INPUT PULSE:
$t_r = t_f$ = 5ns (10% to 90%)
freq = 10MHz (50% duty cycle)
Amplitude = 2.6V

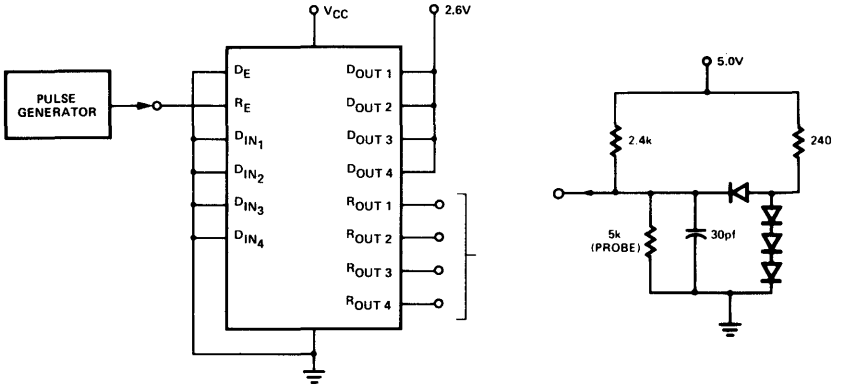
PROPAGATION DELAY (DATA ENABLE TO DATA OUTPUT)

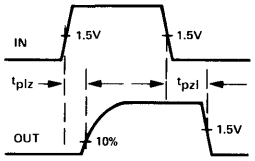




INPUT PULSE:
$t_r = t_f$ = 5ns (10% to 90%)
freq = 5MHz (50% duty cycle)
Amplitude = 2.6V

PROPAGATION DELAY (RECEIVE ENABLE TO RECEIVE OUTPUT)

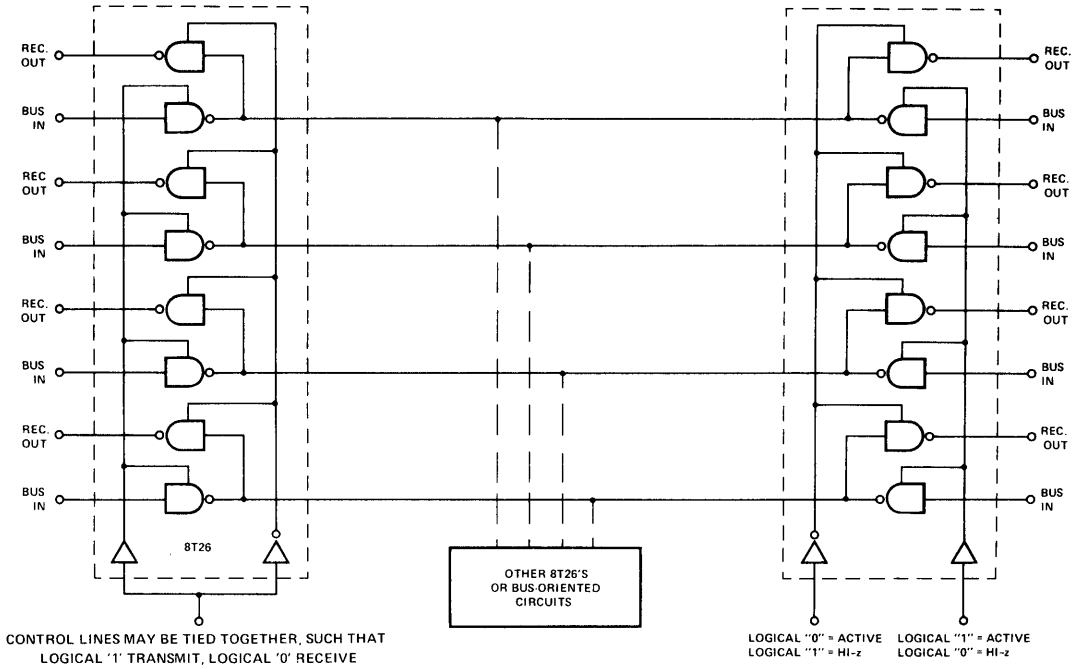




INPUT PULSE:
$t_r = t_f$ = 5ns (10% to 90%)
freq = 5MHz (50% duty cycle)
Amplitude = 2.6V

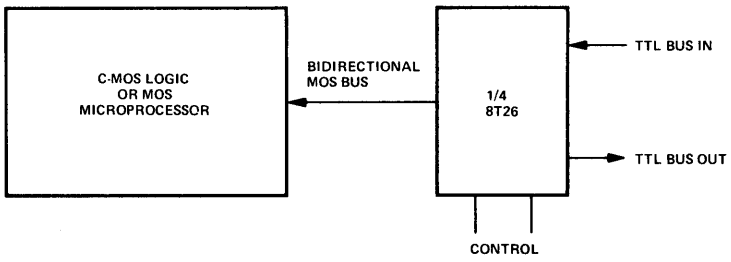
TYPICAL APPLICATIONS

BIDIRECTIONAL DATA BUS



BLOCK DIAGRAM

BIDIRECTIONAL MOS - CMOS TO TTL INTERFACE



ADVANCE INFORMATION

DESCRIPTION

The 8T31 8-bit Bidirectional I/O Port is designed to function as a general purpose I/O interface element in minicomputers, microcomputers and other bus oriented digital systems. It consists of 8 clocked latches with two sets of bidirectional inputs/outputs, Bus A (B_{A0}–B_{A7}) and Bus B (B_{B0}–B_{B7}). Each Bus has a write control line and a read control line. The two buses operate independently except for the case where the user is attempting to write data in from each bus simultaneously. In that case, the data on Bus A will be written into the latches while Bus B will be forced into a high impedance state. Data written into one Bus will appear inverted at the other Bus.

A master enable ($\overline{M}_E$) is provided that enables or disables Bus B regardless of the state of the other inputs.

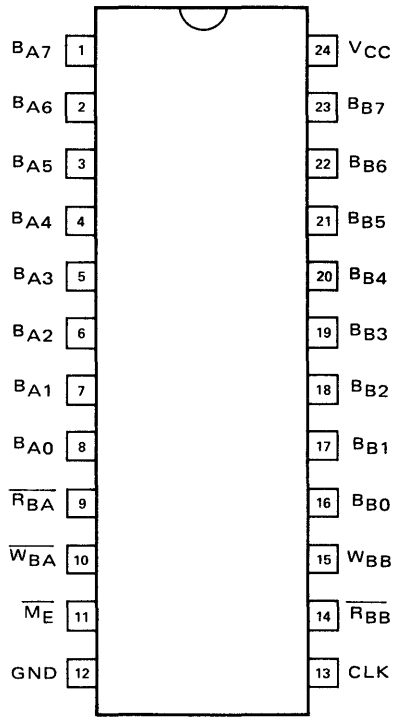
A unique feature of the 8T31 is its ability to start up in a predetermined state. If the clock is maintained at a voltage less than .8V until the power supply reaches 3.5V, Bus A will always be all logic 1 levels, while Bus B will be all logic 0 levels.

FEATURES

- LOW INPUT CURRENT—−500μA AT V_{IN}=.55V, 100μA AT V_{IN}=5.5V FOR EASY BUS INTERFACE AND MOS INTERFACE
- COMPLETE BIDIRECTIONAL CAPABILITY
- MASTER ENABLE FOR PORT SELECTION (BUS B ONLY)
- BUS A OVERRIDES IF BOTH BUSES ARE IN WRITE MODE SIMULTANEOUSLY
- HIGH FANOUT—I_{OL}=20mA MIN, AT V_{OL}=.55V 10 SCHOTTKY LOADS, 12 STANDARD TTL LOADS, 50 LOW POWER SCHOTTKY LOADS
- HIGH CAPACITIVE DRIVE CAPACITY—I_{OH}=−3.2mA AT V_{OH}=2.4V
- STARTS UP IN A KNOWN STATE (ALL LOGIC 1 LEVELS ON BUS A, ALL LOGIC 0 LEVELS ON BUS B) WHEN CLOCK IS HELD BELOW .8V UNTIL V_{CC} REACHES 3.5V

PIN CONFIGURATION

N, F PACKAGE

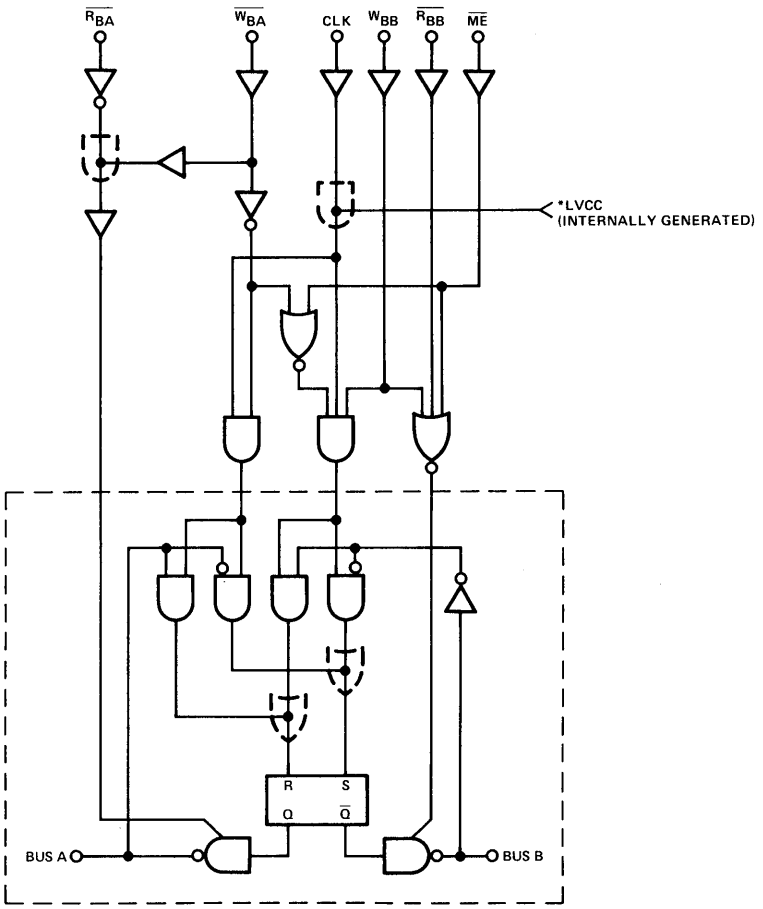


CONTROL FUNCTION TABLES

BUS A			
$\overline{R}_{BA}$	$\overline{W}_{BA}$	CLK	BUS A
X	0	1	WRITE (INPUT)
0	1	X	READ (OUTPUT)
1	1	X	HI-Z

BUS B					
$\overline{R}_{BB}$	W_{BB}	$\overline{W}_{BA}$	CLK	$\overline{ME}$	BUS B
X	X	X	X	1	HI-Z
1	0	X	X	0	HI-Z
X	1	0	X	0	HI-Z
0	0	X	X	0	READ (OUTPUT)
X	1	1	1	0	WRITE (INPUT)

SCHEMATIC



NOTE: CIRCUIT INSIDE DOTTED LINE IS FOR ONE BIT ONLY.
*LOW VOLTAGE CONTROL CIRCUIT

ELECTRICAL CHARACTERISTICS $0°C = T_A = 70°C$

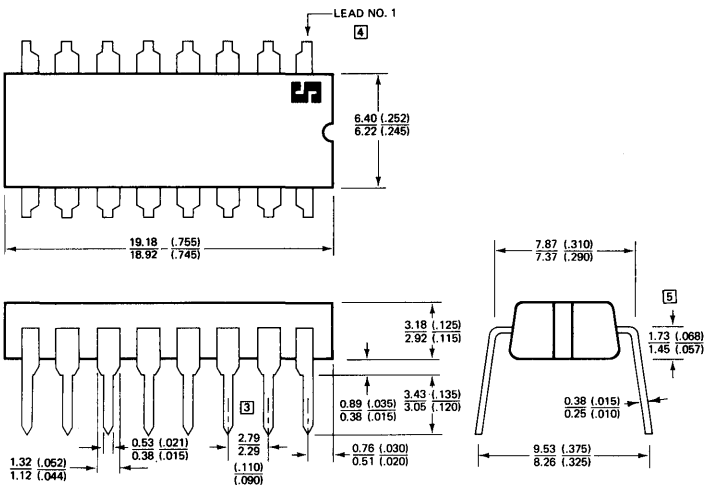
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{OH}	High Level Output Voltage	$I_{OUT} = -3.2mA$, $V_{CC} = 4.75V$	2.4			V
V_{OL}	Low Level Output Voltage	$I_{OUT} = 20mA$, $V_{CC} = 4.75V$			0.55	V
V_I	Input Clamp Voltage	$I_{IN} = -5mA$, $V_{CC} = 4.75V$			-1	V
I_{IH}	High Level Input Current	$V_{IN} = 5.5V$, $V_{CC} = 5.25V$			100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.55V$, $V_{CC} = 5.25V$			-500	μA
V_{IH}	High Level Input Voltage		2		5.5	V
V_{IL}	Low Level Input Voltage		-1		0.8	V
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0V$, $V_{CC} = 5.25V$	-20		-200	mA
I_{OHB}	Bus B High Level Output Current	$V_{OUT} = 2.0V$, $V_{CC} = 4.75V$	-10			mA
I_{CC}	Supply Current	$V_{CC} = 5.25V$			150	mA
C_{IN}	Input Capacitances					
	Control	$V_{IN} = 0V$			6	pF
	Data	$V_{IN} = 0V$			12	pF
		$V_{IN} = 3V$			9	pF

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{ZL}	Propagation Delay From Read ($\overline{R}_{BB}$), Write (W_{BB}) and Master Enable ($\overline{M}_E$) to Bus B	C_L = 300pF		27	45	ns
t_{ZH}		C_L = 300pF		29	50	ns
t_{ZL}		C_L = 30pF		17	30	ns
t_{ZH}		C_L = 30pF		14	25	ns
t_{LZ}		C_L = 30pF		13	20	ns
t_{HZ}		C_L = 30pF		17	30	ns
t_{SETUP}	Bus A Data Setup and Hold Times		0	−10		ns
t_{HOLD1}			10	4		ns
t_{HOLD0}			25	16		ns
t_{SETUP}	Bus A Write Setup and Hold Times		30	20		ns
t_{HOLD}			0	−30		ns
t_{SETUP}	Bus B Data Setup and Hold Times		*			ns
t_{HOLD}			0			ns

*The Bus B Data Setup Time is equal to the clock pulse width.

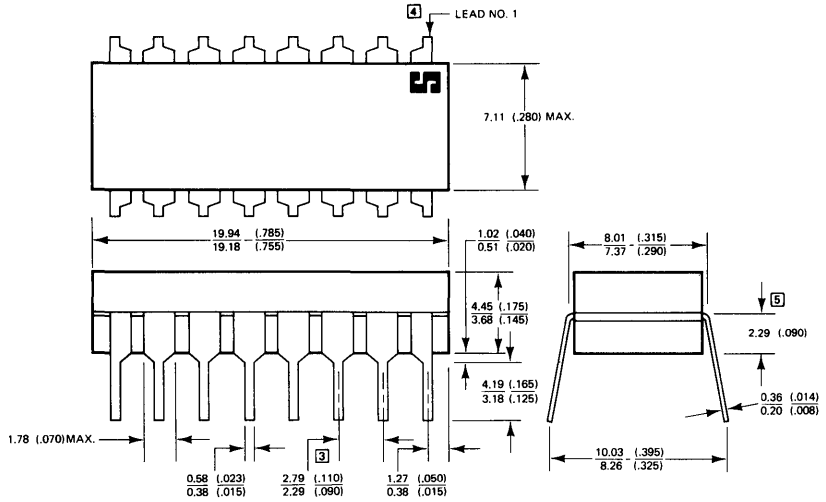
B PACKAGE



NOTES:

1. Lead Material: Alloy 42 or equivalent.
2. Body Material: Plastic.
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Body dimensions do not include molding flash.
7. Thermal Resistance: Θ Ja = .16°C/mW, Θ Jc = .08°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

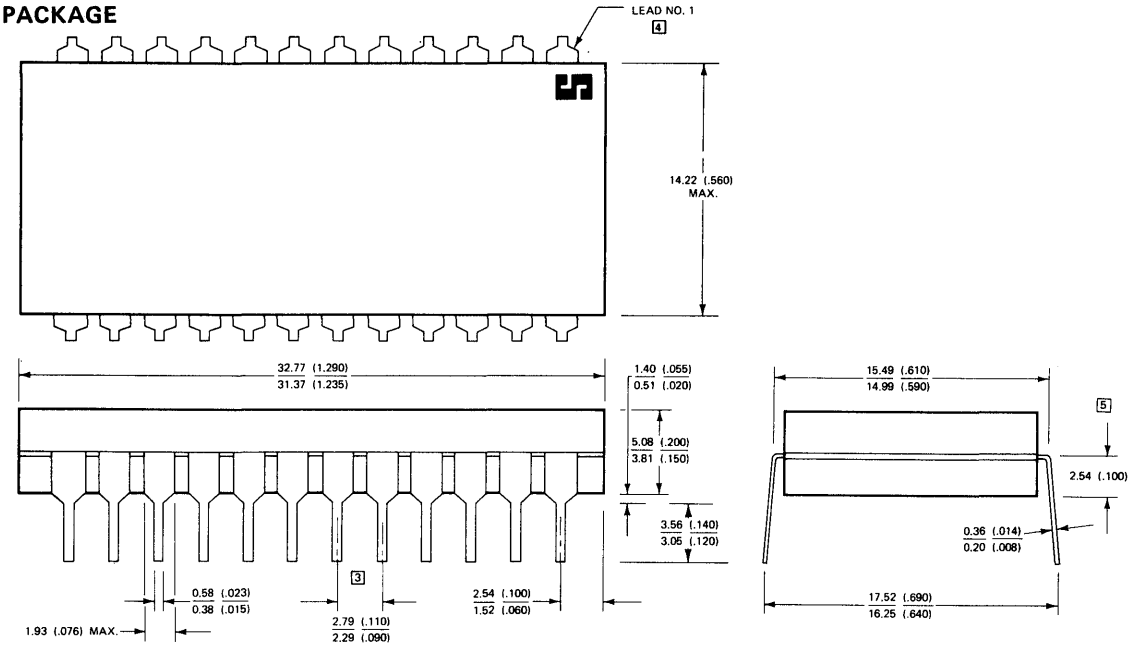
FJ PACKAGE



NOTES:

1. Lead material: Alloy 42 or equivalent, tin plated.
2. Body material: Ceramic with glass seal.
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Thermal resistance: Θ Ja = .090°C/mW, Θ Jc = .025°C/mW.
7. All dimensions shown in parentheses are English. (Inches)

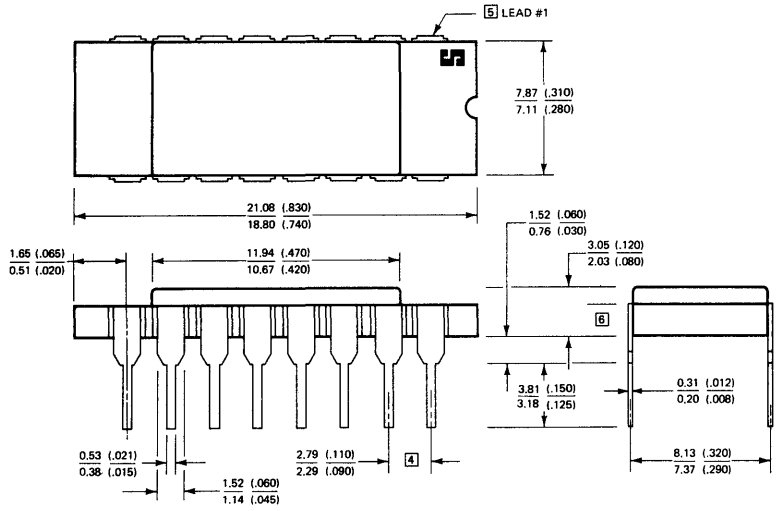
FN PACKAGE



NOTES:

1. Lead material: Alloy 42 or equivalent, tin plated.
2. Body material: Ceramic with glass seal.
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Thermal resistance: Θ Ja = .050°C/mW, Θ Jc = .012°C/mW.
7. All dimensions shown in parentheses are English. (Inches)

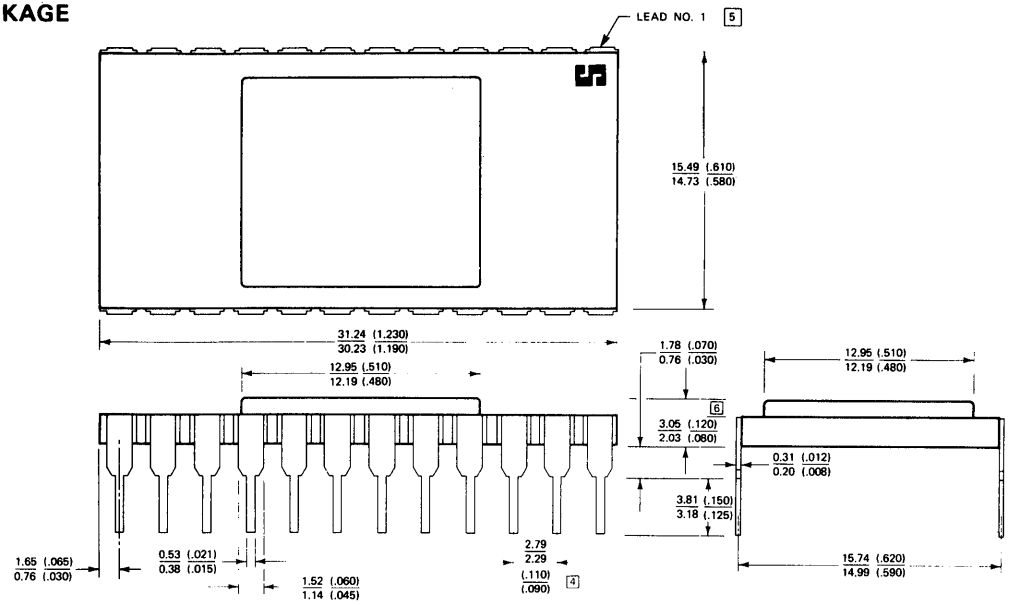
IJ PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, gold plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Kovar or equivalent, gold plated, alloy seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .080°C/mW, Θ Jc = .020°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

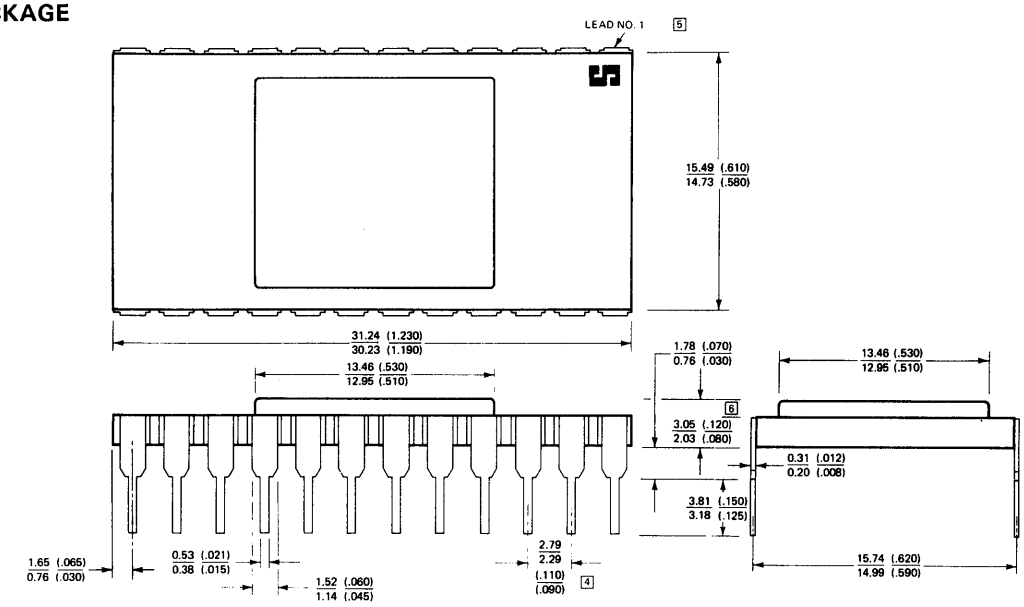
INB PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, gold plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Kovar or equivalent, gold plated, alloy seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .050°C/mW, Θ Jc = .015°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

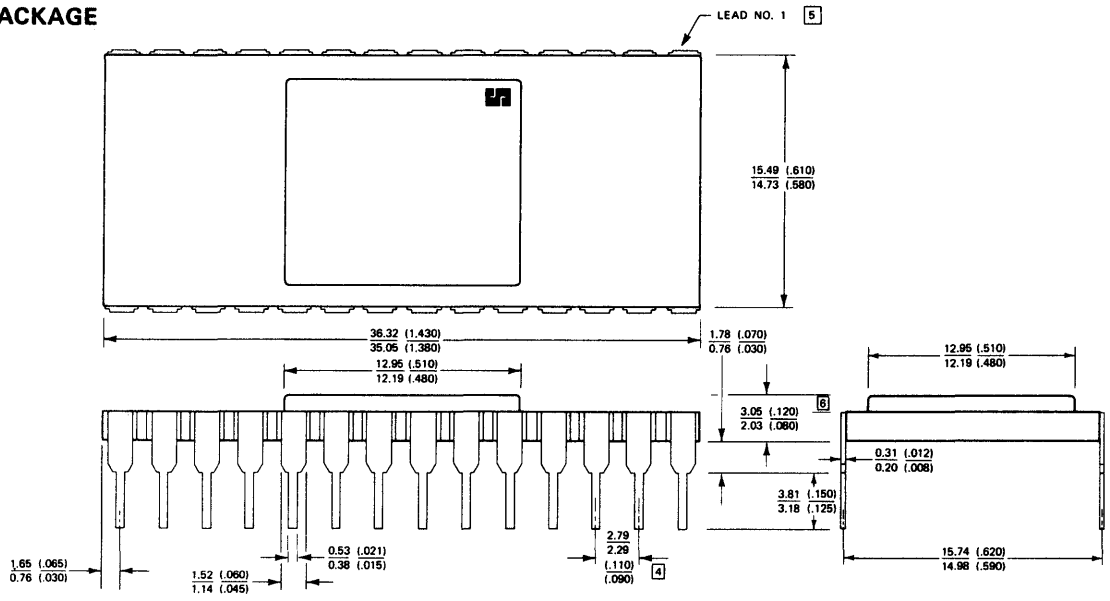
INC PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, tin plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Kovar or equivalent, gold plated, alloy seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .050°C/mW, Θ Jc = .015°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

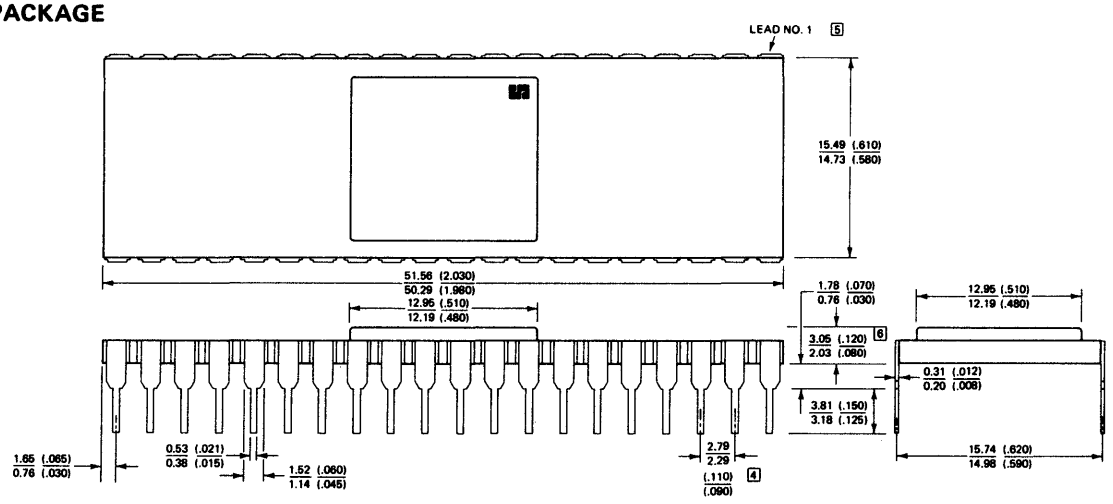
IQ PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, tin plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

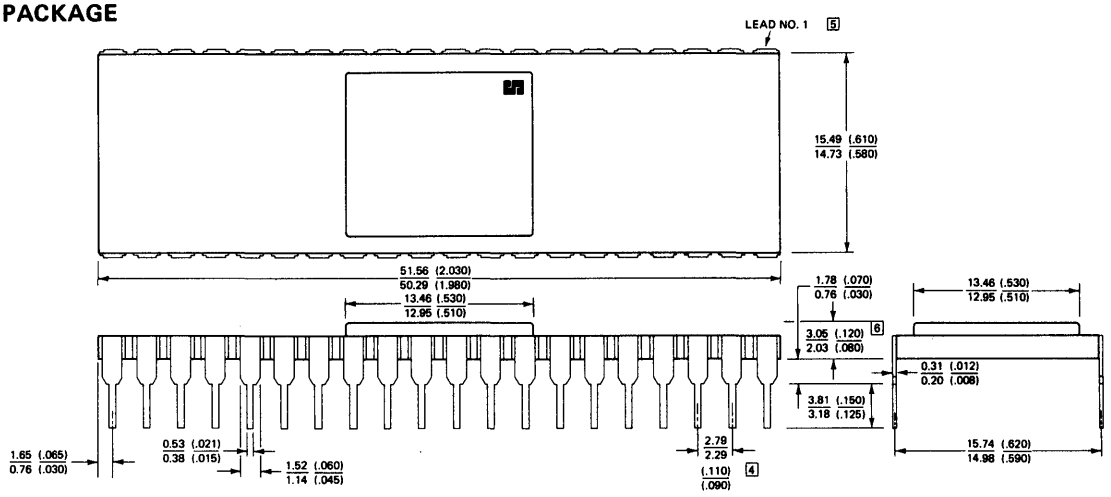
IW PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, gold plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Kovar or equivalent, gold plated, alloy seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

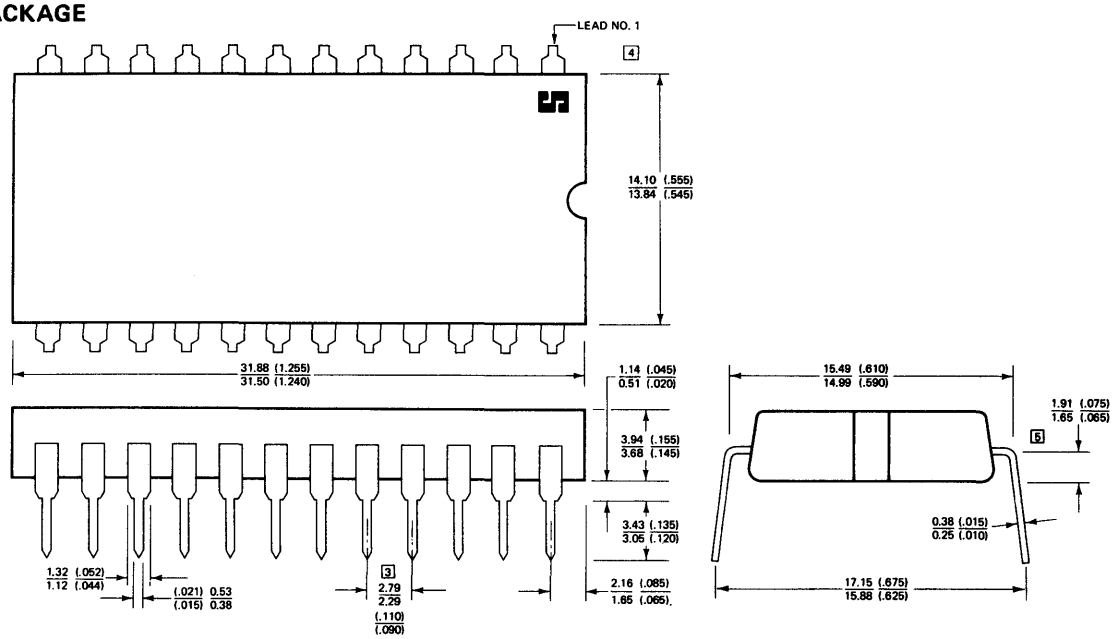
IWA PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, tin plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

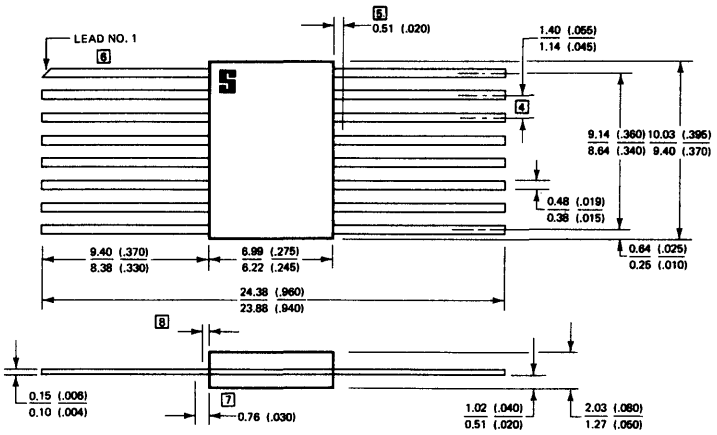
N PACKAGE



NOTES:

1. Lead Material: Alloy 42 or equivalent.
2. Body Material: Plastic
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Body dimensions do not include molding flash.
7. Thermal Resistance: Θ Ja = .12°C/mW, Θ Jc = .05°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

WJ PACKAGE



NOTES:

1. Lead material: Alloy 42 or equivalent, tin plated.
2. Body material: Ceramic with glass seal at leads.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Lead spacing shall be measured within this zone.
6. Signetics symbol or angle cut denotes Lead No. 1.
7. Recommended minimum offset before lead bend.
8. Maximum glass climb .010.
9. Thermal resistance: Θ Ja = .195 °C/mW, Θ Jc = .085°C/mW.
10. All dimensions shown in parentheses are English. (Inches)

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