Interfacing LCD Panels to Microcontrollers

Ken Green, Sharp Microelectronics of the Americas

INTRODUCTION

Modern industrial products on the market today are increasingly using LCD panels to provide a more sophisticated visual interface with the user. These panels have evolved into units that are easy to work with, bright, have high contrast, and come in a wide variety of sizes. The most popular LCD panels are the Amorphous Silicon Thin Film Transistor or a-SiTFT panels. This article discusses how to drive a TFT panel using typical processors found in embedded applications.

State of the art TFT panels typically have the input signals shown in Figure 1 and described in Table 1.

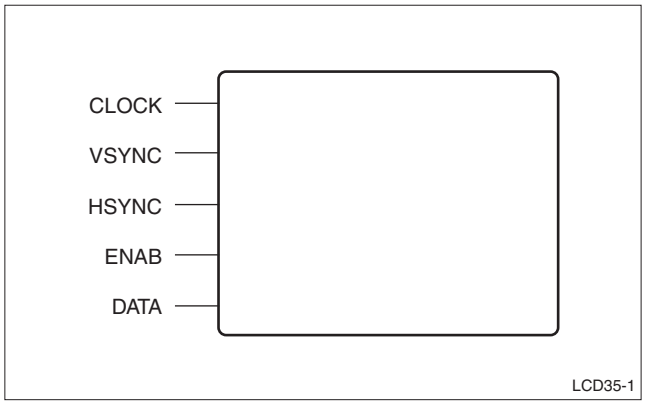

Figure 1. Typical LCD Input Signals

Table 1. Input Signals

SIGNAL	FUNCTION
CLOCK	Latches the pixel data.
VSYNC	Resets the internal circuitry so that the next active pixel will be in the upper left corner
HSYNC	Sets the next active pixel to be first pixel on the next line down
ENAB	Indicates valid pixel data (optional)
DATA (usually 18 to 24 lines)	Actual pixel data equally split between red, green, and blue.

Note that some small, lower end panels may not have all of the electronics included with them because of size or cost restraints. Some panels have a simple row and column interface. Some may need an external timing controller. Some have a processor bus type interface. Panels such as these are beyond the scope of this article. Depending on internal circuitry demands, some panels may include a few other signals, such as a reset line. Determining how to drive such simple signals is usually straightforward.

Many LCD controllers, including those integrated into microcontrollers, will directly drive the signals shown in Figure 1. This means that the biggest obstacle to quickly getting an image on the screen is generating the appropriate signal timing. The LCD controller is, of course, responsible for generating the timing; however software must be written to correctly program the controller for the target LCD panel. The interface between a Sharp™ LQ050Q5DR01 and a Freescale™ MC9328MXL will be used as an example.

MECHANICS OF AN LCD PANEL

An LCD panel comprises a matrix of pixels (picture elements), divided into red, green, and blue “sub-pixels”. Each sub-pixel is driven by a small transistor. Typically, LCD panels have internal row and column drivers, much like DRAM. A row is selected by the row driver, then the column driver sequences through each of the columns. After each of the columns has been written, the row driver selects the next row and the process repeats. The VSYNC signal resets both row and column drivers to the upper left pixel. The HSYNC causes the row driver to step to the new row. The clock sequences the column driver through each of the pixels, with each clock edge latching data values for the red, green, and blue sub-pixels. These values drive a form of D/A converter to store an electrical charge in a capacitor in each sub-pixel which controls the drive of the transistor; this in turn controls the brightness of the sub-pixel. A red-green-blue color mask is used to filter the light from each sub-pixel to form its corresponding color.

Like a DRAM, an LCD panel must be constantly refreshed or the image will fade. Most TFT LCD panels work fine when refreshed around 60 Hz. To refresh the charge in each of the sub-pixels, the entire image data must be rewritten to the panel. This is one the functions performed by the LCD controller. The image data is usually held in a section of main memory called a frame buffer. This means that the LCD controller is constantly accessing data from the frame buffer and sending it to the LCD panel. Depending on the resolution of the panel, transferring this refresh data may have a significant impact on bus bandwidth. This is why processors utilizing low bandwidth buses cannot be used to drive large TFT displays.

Each location in the frame buffer corresponds to a pixel on the LCD. The value in the location determines the color displayed for that pixel. See Figure 2. The size of the frame buffer depends on two things: the number of locations needed, and the size of each location.

The total number of locations needed is determined by the panel resolution. For instance, the resolution of the Sharp LQ050Q5DR01 panel is 320 × 240 pixels. Therefore 320 × 240 = 76,800 memory locations will be needed in the frame buffer — one for each pixel.

The size (or number of bits) of each location is slightly more complicated. The size depends primarily on the number of individual colors needed. A larger number of different colors will require more bits (or 'bits per pixel' (BPP)) to define it. For instance, 16 bits can describe 65,536 different colors. Therefore a display design employing a 320 × 240 panel displaying 65,536 different colors requires 76,800 16-bit locations (153,600 bytes) and 16 data lines from the processor to the panel. This assumes, of course, that each bit can be passed to the LCD panel on its own individual data line.

TFT panels typically have an input of at least 6 bits of red data, 6 bits of green data, and 6 bits of blue data. A panel with 6 red, 6 green, and 6 blue data lines is termed a 6-bit panel. If the processor or LCD controller doesn't drive as many data lines as the panel requires, use the data line configuration shown in Figure 3 or Figure 5.

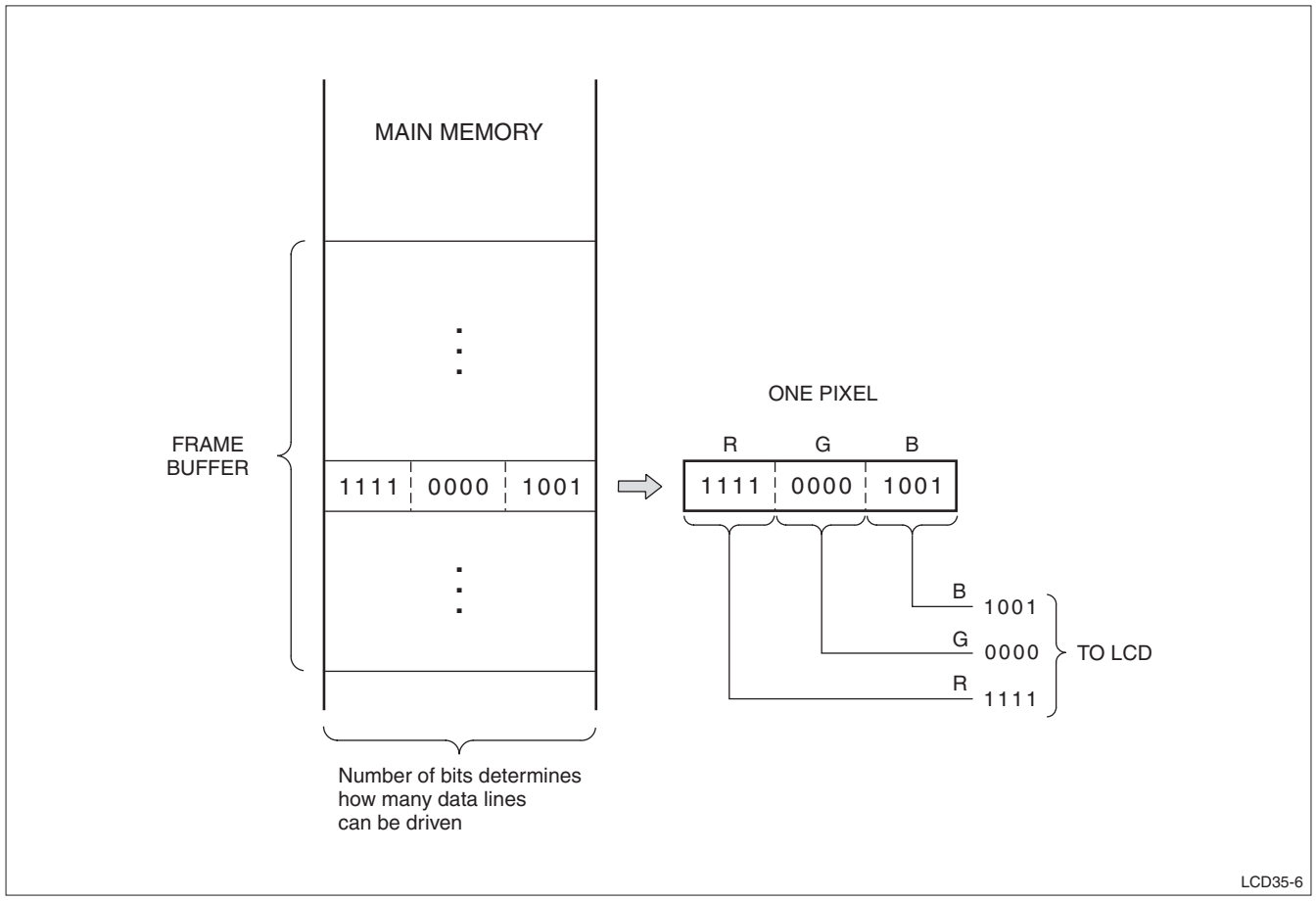

Figure 2. Direct Color Addressing

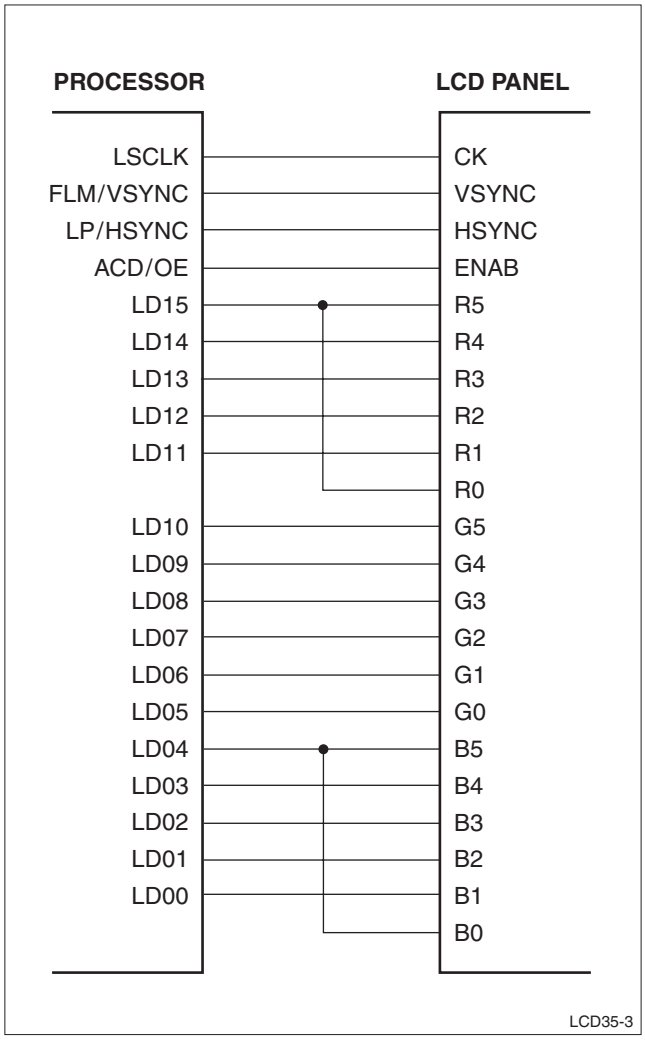

Figure 3. Driving a 18-bit Panel with 16 Data Lines

COLOR PALETTE

Most industrial applications don't require the full diversity of colors that a TFT panel can display. A common number is 256 different colors, with some applications requiring 16 or fewer. If an application only requires 256 colors for its maximum number of unique colors (or 8 bits per pixel), then a single byte can be used to describe each pixel. This means that the frame buffer size for a 320 × 240 display is now cut in half to 76,800 bytes. The question then becomes how to drive all of the display data lines with 8 bits of data. The answer is to use a color palette.

A color palette is a lookup table usually built into the LCD controller. The number of locations in the table corresponds to the number of bits per pixel in the frame buffer. Common values for bits per pixel (BPP) are 8, 4, or 2. For example, if the frame buffer stores 8 bits per pixel, there should be 256 locations in the color palette. The width of each location in the color palette is equal to the number of LCD data lines exiting the chip. Each used bit in a palette entry corresponds to an LCD data line. This scheme is shown in Figure 4.

Each location in the palette is programmed with a value corresponding to a color. For instance, location 0 may be all 0's which usually produces black. Location 1 may be all 1's producing white. Location 2 may turn on all the red data lines, and turn off the green and blue ones, and so on. In the frame buffer, a 0 would be stored to produce black for a given pixel, 1 for a white pixel, and 2 for a red pixel. The palette is populated with values for whatever colors will be used (up to 256 different colors for 8 BPP). As the LCD controller accesses each location in the frame buffer, the data is sent to the palette for translation. Then the result of the translation is sent to the panel.

HARDWARE INTERFACE

The hardware interface is shown in Figure 3 and 5. From this, it can be seen that the connections are very straight forward. However, as mentioned above, LCDs and microcontrollers can have differing numbers of data lines. Note that in our example, the LCD requires 18 data lines. However, the LCD Interface in our Freescale MXL series processor example only utilizes 12-to-16 data lines, depending on the number of bits per pixel selected.

For the Freescale MXL series processor, choosing 4- or 8-BPP causes its LCD interface to make only 12 data lines available to drive pixel data to 18 data lines of the panel. The connections shown in Figure 5 generate the smallest, most uniform gaps between color values caused by the lack of enough processor data lines to individually drive all of the panel data lines. All of the panel's pixel data lines are now driven so that the panel can achieve its full brightness. Note that all signal lines should be kept to 12 inches or less to avoid EMI and crosstalk issues. Longer distances can be accommodated using LVDS technology.

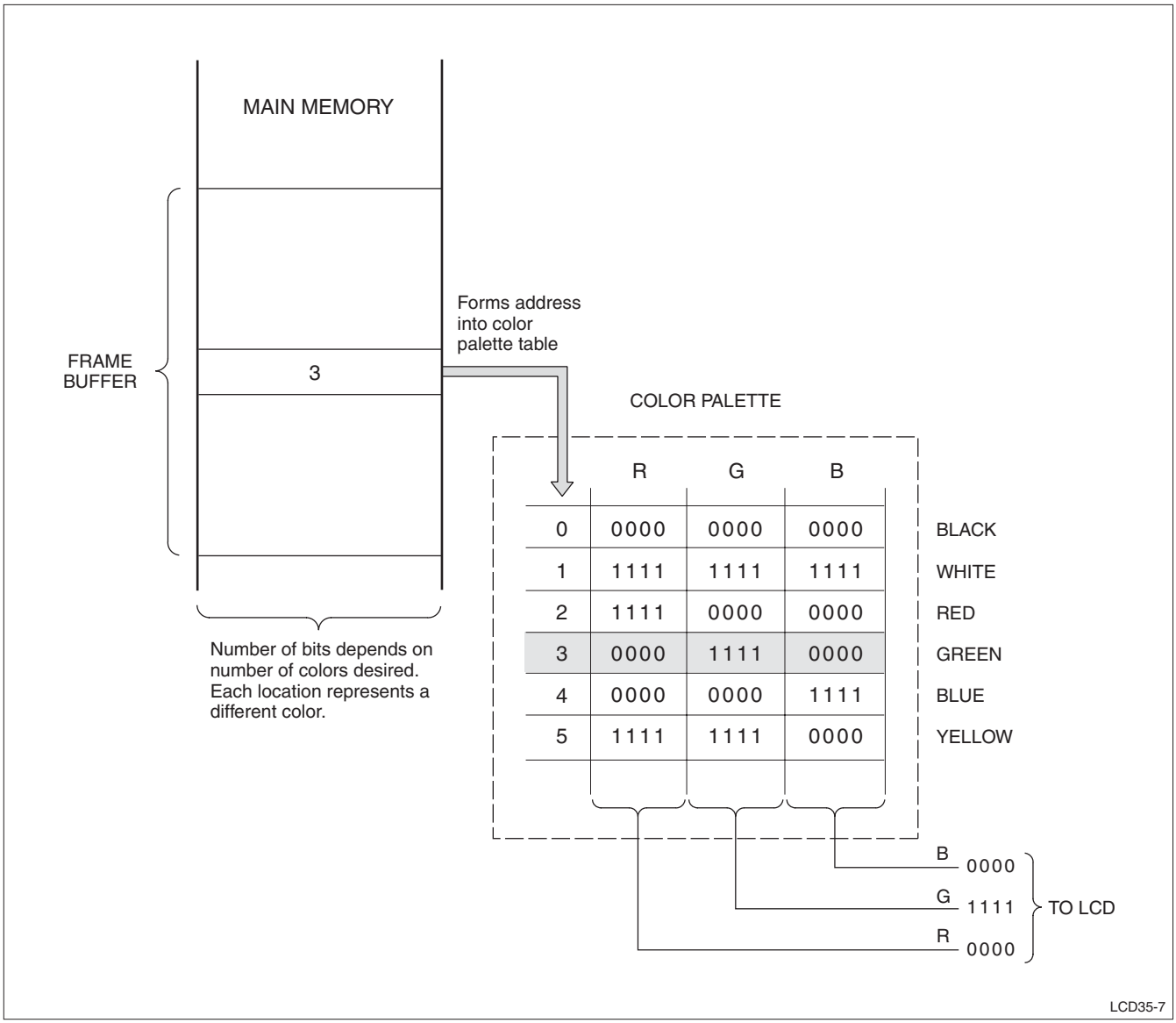

Figure 4. Palletized Addressing

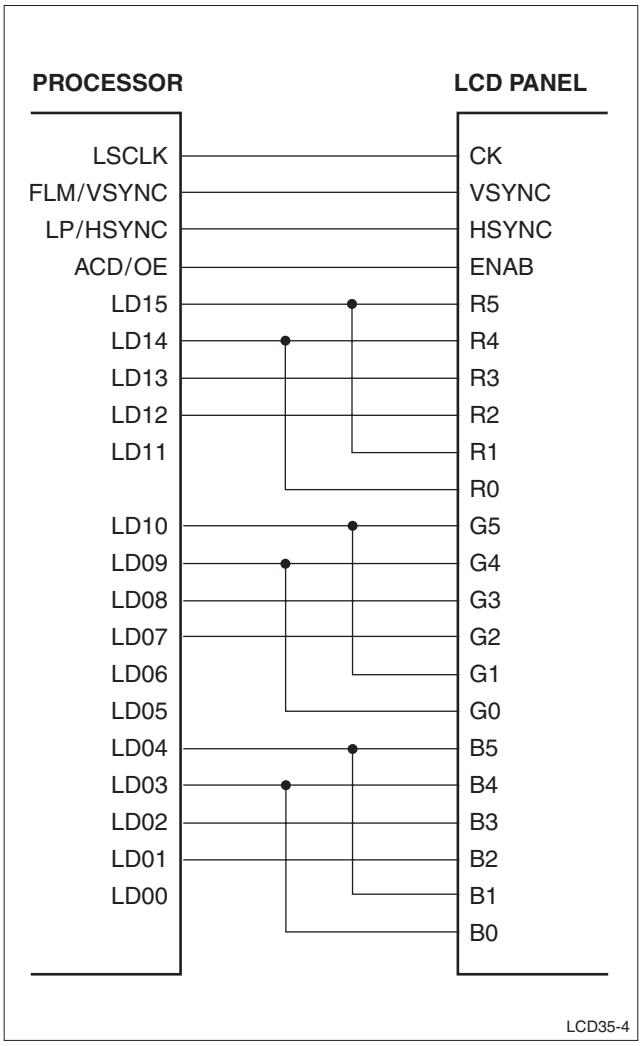

Figure 5. Driving a Panel with 12 Data Lines

PROGRAMMING THE LCD CONTROLLER

Before we proceed, let's take a moment to define a few terms. Many of these terms originate from the definitions of TV signals. As shown in Figure 6, horizontal and vertical timing is split into four areas: the sync pulse itself, the back porch, valid data, and front porch. The back porch (horizontal or vertical) historically refers to the period of time between the end of the sync pulse and the beginning of valid data. Valid data is the period where pixel data is actually clocked into the panel. The front porch is the time between the end of valid data and the beginning of the sync pulse.

A careful review of the panel's Data Sheet is necessary to correctly program the LCD controller. The information needed is split between the Timing Tables (Table 2 and Table 3), and the Timing Diagram (Figure 6). The Table shows values and the Diagram shows polarities. Most LCD panels will function over a wide variety of timing setups. Although some values are fixed, many others offer a high degree of flexibility.

Table 2. Horizontal Signals

PARAMETER		SYM.	MIN.	TYP.	MAX.	UNIT
Horizontal sync signal	Cycle	TH	50	63.5	80	µs
			THe + 308	400	440	clocks
	Pulse Width	THp	4	12	30	clocks
HSYNC to ENAB phase difference		THe	14		72	clocks
Horizontal display period		THd	320	320	320	clocks
HORZ auto start*		THe	72	72	72	clocks

Table 3. Vertical Signals

PARAMETER		SYM.	MIN.	TYP.	MAX.	UNIT
Vertical sync signal	Cycle	TV	246	263	330	lines
	Pulse width	TVp	1	—	—	lines
Vertical display start		TVs	6	6	6	lines
Vertical display period		TVd	240	240	240	lines

The easiest place to start in determining timing is with the horizontal timing. The formula for horizontal timing is:

TOTAL CLOCKS(TH) = HSYNC WIDTH(THp) + BACK PORCH(THe) + VALID DATA (THd) + FRONT PORCH

The Valid Data time (THd) is equal to the number of pixels in the horizontal direction, in this case 320. From the Timing Table we see that the typical value for the HSYNC pulse (THp) is 12, and the typical number of total clocks per line is 400. The remaining 400 – 320 – 12 = 68 clocks can be split in any combination between the back porch and the front porch as long as all minimums and maximums are met.

For most panels, THe represents the back porch, and is specified as the number of clocks between the end of HSYNC and the beginning of valid data. However, the Data Sheet for the LQ050Q5DR01 specifies THe from the beginning of HSYNC to the beginning of valid data. Therefore, in this case, the value for HSYNC should be subtracted from the value given in the data sheet for the back porch. Use this modified value when programming the controller. The value for the back porch should always be greater than 0 (which is common for most LCD panels, although no warning of this is given in the data sheet). In this case, we'll use 16 for the back porch, leaving 52 for the front porch.

The vertical timing is split into the same four areas as the horizontal timing. The formula is:

TOTAL LINES(TV) = VSYNC WIDTH(TVp) + BACK PORCH(TVs) + VALID DATA(TVd) + FRONT PORCH

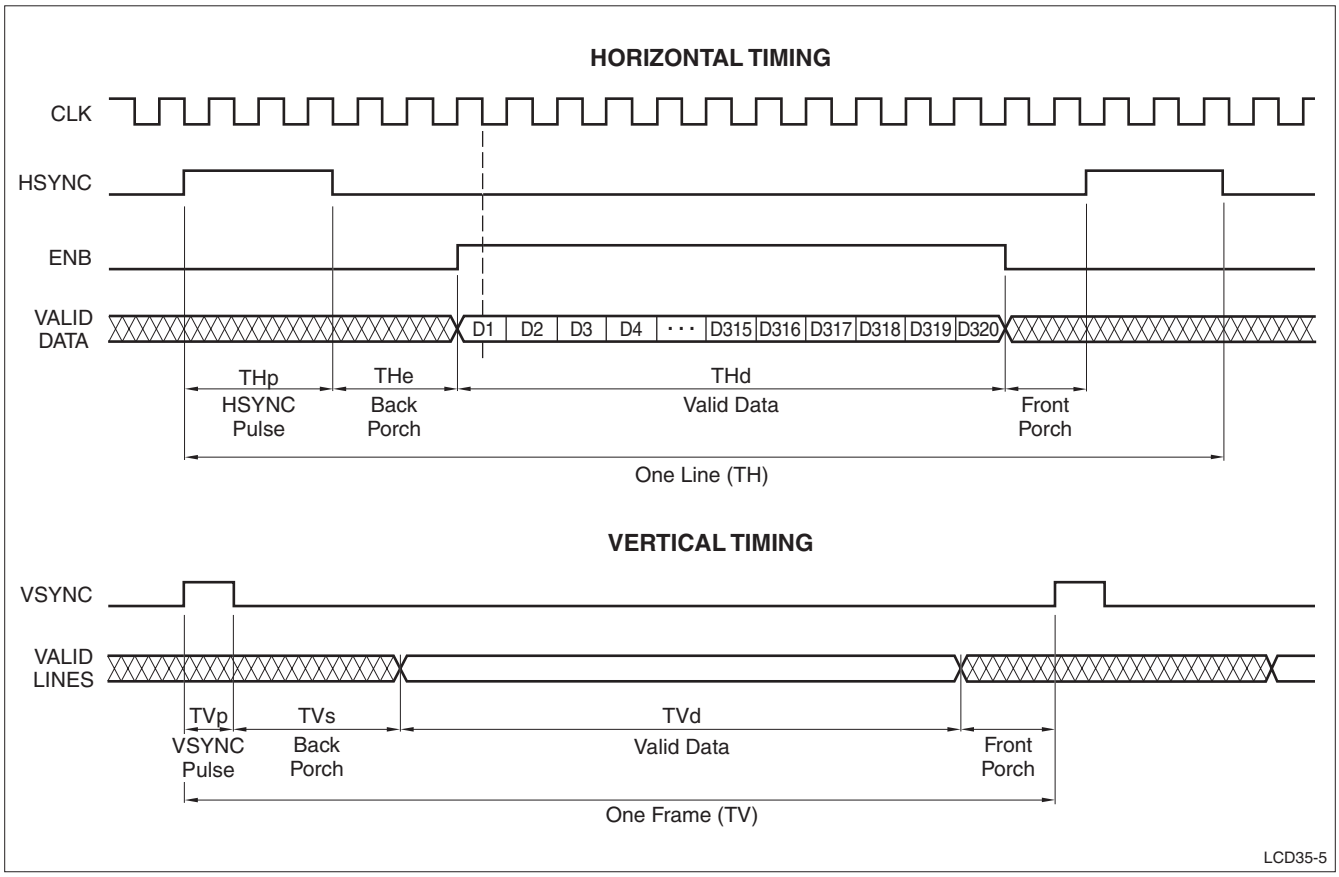

Figure 6. Video Data Timing

Note that the unit for vertical values is lines. The Valid Data time (TVd) is equal to the number of pixels in the vertical direction, in this case 240. The typical total number of lines per frame is shown on the data sheet as 263. As in the horizontal timing, TVs (for this data sheet) includes VSYNC (TVp). TVs is fixed at 6 in the specification. The minimum pulse width of VSYNC (from the Timing Table) is 1. We'll make the VSYNC pulse width 2 which leaves 4 for the back porch. The remainder, 263 – 240 – 2 – 4 = 17, will be the front porch.

The remaining item to determine is the clock speed. The formula for clock speed is:

CLOCK = TOTAL HORZ CLOCKS(TH) x TOTAL VERT LINES(TV) x REFRESH RATE

The 'ideal' clock (for 60 Hz refresh rate) then would be 400 x 263 x 60 = 6.312 MHz. Assuming that the Freescale MXL series processor is using a 32 kHz crystal, and the timing suggested in the processor reference manual (Table 12-11), the system clock (PLLCLK) will be 96 MHz. This clock is applied to a divider, PCLKDIV2, and then on to the LCD controller. Although PCLKDIV2 could be used to divide down PLLCLK (see section 12.5.2 in the Freescale User's Guide), that same clock runs the SDRAM and SPI logic. There is another divider (PCD) within the LCD controller section. Setting this divider to divide by 15 yields a clock speed of 6.4 MHz, a refresh rate of 60.84 Hz, and a line (cycle) time of 62.5 µs which meets the panel's specification.

Using these values, the critical registers are as shown in Table 4.

Table 4. Register Values

REGISTER	ADDRESS	FIELD	VALUE
SIZE	0x00205004	XMAX	320/16 = 20
SIZE	0x00205004	YMAX	240
PCR	0x00205018	TFT	1 for TFT
		COLOR	1 for color
		PBSIZ	Not used
		BPIX	Determined by user
		PIXPOL	0 (active HIGH)
		FLMPOL	0 (active HIGH)
		LPPOL	0 (active HIGH)
		CLKPOL	1 (active on negative edge)
		OEPOL	1 (active HIGH)
		SCLKIDLE	1 (leave CLK enabled)
		END_SEL	0 (little endian)
		SWAP_SEL	0 (no swap)
		REV_VS	0 (normal scan)
		ACDSEL	Not used for TFT
		ACD	Not used for TFT
		SCLKSEL	1 (continuous CLK)
		SHARP	0 (not needed for this panel
		PCD	15
HCR	0x0020501C	H_WIDTH	11 (HSYNC -1)
		H_WAIT_1	51 (front porch -1)
		H_WAIT_2	15 (back porch -1)
VCR	0x00205020	V_WIDTH	2 (VSYNC -1)
		V_WAIT_1	17 (front porch)
		V_WAIT_2	4 (back porch)

POWER-UP SEQUENCE

Another important consideration is the power-up sequence. To prevent latchup in the LCD driver logic, it is recommended that the data and control signals be active within 10 ms after applying Vcc to the panel. If the processor takes longer than this to boot up and configure the LCD controller, panel Vcc power should be controlled by the processor such that power is applied to the panel just before the LCD controller is configured.

See Figure 7 for an example of the overall flow.

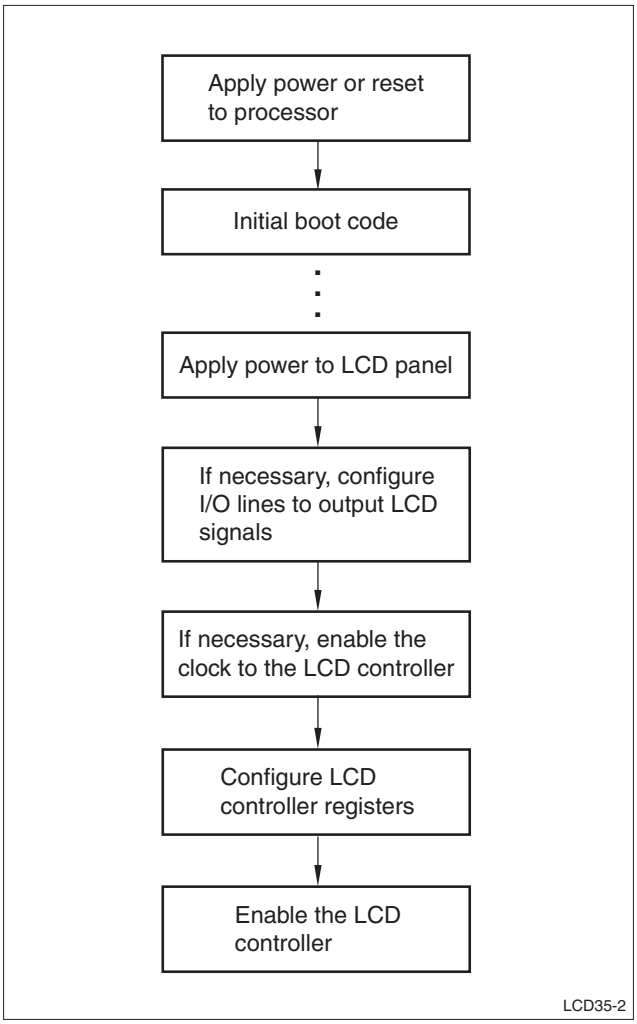

Figure 7. Power-up Sequence

LCD Backlight

Transmissive and transflective LCDs utilize a backlight. The most common types are cold cathode florescent tubes (CCFT) or LEDs. CCFTs require a high voltage (≥450 VAC) source. The simplest solution is to purchase an off-the-shelf DC-to-AC inverter specially built to drive LCD backlights. There are multiple suppliers for these inverters. Input voltages to the inverters are typically either 5 V or 12 V. Most inverters have provisions for dimming the backlight if desired. Be sure to consult the inverter manufacturer to determine the correct inverter for the desired panel.

Supplying power to LED backlights is much easier. These backlights put some or all of the LEDs in series; therefore input voltages are typically in the 15 V to 30 V range, with currents around 20 mA, depending on the number of LEDs used. There are multiple suppliers of DC-to-DC converters made specifically for driving white LED backlights. Just make sure to select one with the right voltage and current requirements.

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

Suggested applications (if any) are for standard use; See Important Restrictions for limitations on special applications. See Limited Warranty for SHARP's product warranty. The Limited Warranty is in lieu, and exclusive of, all other warranties, express or implied. ALL EXPRESS AND IMPLIED WARRANTIES, INCLUDING THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR USE AND FITNESS FOR A PARTICULAR PURPOSE, ARE SPECIFICALLY EXCLUDED. In no event will SHARP be liable, or in any way responsible, for any incidental or consequential economic or property damage.

SHARP®

NORTH AMERICA

SHARP Microelectronics of the Americas
5700 NW Pacific Rim Blvd.
Camas, WA 98607, U.S.A.
Phone: (1) 360-834-2500
Fax: (1) 360-834-8903
www.sharpsma.com

EUROPE

SHARP Microelectronics Europe
Division of Sharp Electronics (Europe) GmbH
Sonninstrasse 3
20097 Hamburg, Germany
Phone: (49) 40-2376-2286
Fax: (49) 40-2376-2232
www.sharpsme.com

JAPAN

SHARP Corporation
Electronic Components & Devices
22-22 Nagaike-cho, Abeno-Ku
Osaka 545-8522, Japan
Phone: (81) 6-6621-1221
Fax: (81) 6117-725300/6117-725301
www.sharp-world.com

TAIWAN

SHARP Electronic Components
(Taiwan) Corporation
8F-A, No. 16, Sec. 4, Nanking E. Rd.
Taipei, Taiwan, Republic of China
Phone: (886) 2-2577-7341
Fax: (886) 2-2577-7326/2-2577-7328

SINGAPORE

SHARP Electronics (Singapore) PTE., Ltd.
438A, Alexandra Road, #05-01/02
Alexandra Technopark,
Singapore 119967
Phone: (65) 271-3566
Fax: (65) 271-3855

KOREA

SHARP Electronic Components
(Korea) Corporation
RM 501 Geosung B/D, 541
Dohwa-dong, Mapo-ku
Seoul 121-701, Korea
Phone: (82) 2-711-5813 ~ 8
Fax: (82) 2-711-5819

CHINA

SHARP Microelectronics of China
(Shanghai) Co., Ltd.
28 Xin Jin Qiao Road King Tower 16F
Pudong Shanghai, 201206 P.R. China
Phone: (86) 21-5854-7710/21-5834-6056
Fax: (86) 21-5854-4340/21-5834-6057
Head Office:
No. 360, Bashen Road,
Xin Development Bldg. 22
Waigaoqiao Free Trade Zone Shanghai
200131 P.R. China
Email: smc@china.global.sharp.co.jp

HONG KONG

SHARP-ROXY (Hong Kong) Ltd.
3rd Business Division,
17/F, Admiralty Centre, Tower 1
18 Harcourt Road, Hong Kong
Phone: (852) 28229311
Fax: (852) 28660779
www.sharp.com.hk
Shenzhen Representative Office:
Room 13B1, Tower C,
Electronics Science & Technology Building
Shen Nan Zhong Road
Shenzhen, P.R. China
Phone: (86) 755-3273731
Fax: (86) 755-3273735

Reference Code SMA07001