Rockwell

PARALLEL PROCESSING SYSTEM (PPS) DATA SHEET

PPS-4/1 One-Chip Microcomputer Family

MM78

one-chip microcomputer system

SUMMARY

The Rockwell MM78 microcomputer is a complete, 4-bit parallel processing system. Its large instruction set is augmented by powerful multi-function instructions. 31 I/O ports further identify the power of this system. Serial I/O capability, which can be clocked simultaneously or externally controlled, extend their power.

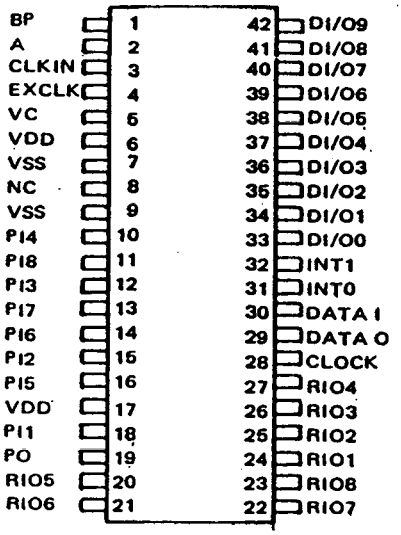
On a single LSI chip, the MM78 provides a complete 4-bit parallel processing system — Central Processing Unit (CPU), Program Memory (ROM), Data Memory (RAM), Program Counter (P), Instruction Decode, two Program Save registers, Data Address register (B), 10 I/O discrete drivers/receivers, two 4-bit parallel I/O channels, two 4-bit parallel input channels, a serial input/output port, interrupt and control logic, and a self-contained four-phase clock generator circuit.

In addition to stand-alone system applications, this microcomputer can be directly interfaced with other multi-chip systems as dedicated slave controllers or for other purposes. Also, two or more MM78 systems can be directly combined to perform parallel processing or control operations.

The MM78 may be ordered with combinations of the following features (not every combination is available).

Operating Temperature
- $0^{o}C$ to $+50^{o}C$ (Consumer)
- $0^{o}C$ to $+70^{o}C$ (Commercial)

Maximum Negative Voltage
- -30 Volts (Vacuum Fluorescent Drive)
- -15 Volts (Standard)



PPS–4/1 MM78 Pin Configuration

FEATURES

- 2048 8-bit bytes of program memory and 128 4-bit data words
- Clocked simultaneous serial input/output capability
- Externally controlled serial input/output capability
- Two interrupt request input lines
- TTL and CMOS compatible
- Arithmetic logic unit and six working registers
- Two-level subroutine nesting
- 31 input/output ports
- Easy circuit level testing by user
- Large instruction set — over 60 instructions
- Multifunction instructions increase throughput
- Single power supply operation (-15 volts ±5%)
- Low power (75 milliwatts typical, 125 milliwatts max)
- Powerful development aids:
  - SYSTEM 65 with built-in mini-floppy disks and PPS-4/1 Personality subsystem
  - XPO-1 Evaluation Microcomputer Module
  - Development Circuit (P/N A7899) provides address and data lines so that Program Memory can be in external PROM or RAM for emulation purposes
  - Scheduled and Special Training Courses
  - International Applications Engineering Support

Specifications subject to change without notice
Document No. 29000 D01
Rev. 6, May 1981

FUNCTIONAL DESCRIPTION

PROGRAM COUNTER (P), SA REGISTER, AND SB REGISTER

Program Counter contains the ROM address of the next program instruction. The address in the P Register is automatically incremented each cycle time during normal operation to address the next instruction. In addition, instructions are available to alter the address in the P Register as necessary to fetch an instruction from any address in program memory. After PO reset, the program counter contains address hex 3C0. This location must contain a NOP instruction.

The SA Register is a "save" register which saves the incremented value of current address in the P Register during subroutine execution. This provides a means of returning from a subroutine directly to the next instruction after the subroutine call.

The SB Register provides a second hardware stack register so that two levels of subroutines may be nested in the microcomputer.

PROGRAM MEMORY – READ ONLY MEMORY (ROM)

The ROM provides 2048 bytes of storage for instructions and constants required to operate the microcomputer. Under control of the Program Counter the ROM will read out the addressed instruction which is to be decoded and executed.

INSTRUCTION DECODE

The Instruction Decode logic circuitry interprets the instructions pulled from ROM to provide control for data transfers, arithmetic operations, other processing functions and input/output operations.

DATA ADDRESS REGISTER (B)

Data Address Register is 7 bits in length and is made up of two segments, B Upper (BU) and B Lower (BL). Data locations in RAM are addressed by all 7 bits and the discrete input/output ports are addressed by the 4 bits in BL when the value in BU is between 0 and 3.

A number of multifunction instructions simultaneously modify B Upper and cause B Lower to be automatically incremented or decremented and tested for overflow or underflow.

ACCUMULATOR AND ARITHMETIC LOGIC UNIT (A, ALU, AND C)

The Primary working register in the MM78 is the Accumulator (A). It is the Accumulator which ties with the Arithmetic Logic Unit (ALU) and the Carry flip-flop (C) to perform binary arithmetic. By means of software routines, decimal arithmetic can be performed. Constants may be loaded into the Accumulator from the read only memory or variable data may be loaded from, or exchanged with the random access memory (RAM) under control of the Data Address Register (B). The Accumulator is also the primary path for 4-bit parallel or serial input or output data.

A BUFFER

The contents of the Accumulator may be output for control, display, or data transfer functions through the A Buffer. The A Buffer holds the data for output until new data is received from the Accumulator or until the power is turned off.

X BUFFER

The X Buffer comprises four latches which will output the last bit pattern loaded until either a new Output X Register command is executed or power is turned off.

X REGISTER

The X Register is an auxiliary register which may be used as temporary storage for 4 bits of data without reference to data memory. The X Register is also used as a data path to the X Buffer output register and from receiver inputs.

CHANNEL 1 INPUT PORTS (PI1 through PI4)

The parallel input port P11 through P14 will be added to the contents of the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 1 time) so that asynchronous input signals may be used.

CHANNEL 2 INPUT PORTS (PI5 through PI8)

The inverted state of the inputs at parallel input ports PI5 thru PI8 will be loaded into the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 3 time) so that asynchronous input signals may be used.

CHANNEL A I/O PORTS (RI01 through RI04)

The contents of the Accumulator may be output for control or data transfer purposes through the A Buffer. The A Buffer will hold the data output until new data is output or power is turned off.

CHANNEL X I/O PORTS (R105 through R108)

The four parallel input/output ports of Channel X function as described in X Buffer and X Register paragraphs.

CONDITIONAL INTERRUPTS (INT0 and INT1)

The conditional interrupts INT0 and INT1 may be used to detect external signals and set internal control flip-flops. The receivers are TTL compatible and synchronized with INT0 sampled at phase 3 and INT1 sampled at phase 1.

DISCRETE INPUT/OUTPUT PORTS (DI/O0 through DI/O9)

There are ten discrete input or output lines each of which can be controlled individually under program control. The receivers are fully synchronized so that asynchronous input signals may be used.

CLOCK CONTROL (VC, CLKIN, EXCLK, AND OSCILLATOR)

The internal Oscillator and Clock circuit generates a four Phase A and $\overline{B}$ clock signal used for all internal logic functions. The A and $\overline{B}$ terms are also brought out so external logic can be synchronized. The clock frequency is a nominal 90 kHz ±40%. When precise timing is required, a reference frequency may be input at CLKIN.

DATA MEMORY (RAM)

The Random Access Memory (RAM) used for data memory contains 128 4-bit characters. Data memory can be used to buffer input or output values, hold intermediate results, or be used as a register for timers, counters, comparators, etc., when the MM78 is used as a universal logic element.

S REGISTER – SERIAL INPUT/OUTPUT – SHIFT COUNTER

The S Register is a 4-bit serial-in/serial-out, parallel exchange, register which is used as either an auxiliary storage register or buffer for the simultaneous serial input/output functions. The shift rate can be controlled either internally or externally.

PPS-4/1 MM78 INSTRUCTION SET

RAM Addressing Instructions

XAB	Exchange A with BL
LBA	Load BL from A
LB	Load BL, BU → O
EOB	Exclusive OR BU
LBL	Load B Long
INCB	Increment B
DECB	Decrement B
SAG	Special Address Generation

Bit Manipulation Instructions

SB	Set Bit
RB	Reset Bit
SKBF	Skip on Bit False

Register to Register Instructions

LXA	Load X from A
XAS	Exchange A and S
XAX	Exchange A and X

Arithmetic Instructions

A	Add Memory to A
AC	Add Memory with Carry to A
ACSK	Add Memory with Carry to A and Skip on Carry-out
DC	Decimal Correction
COM	Complement A
RC	Reset Carry
SC	Set Carry
SKNC	Skip on No Carry
LAI	Load A with Immediate Field
AISK	Add Immediate and Skip on No Carry-out

ROM Addressing Instructions

RT	Return from Subroutine
RTSK	Return and Skip
T	Transfer on Page
NOP	No Operation
TL	Transfer Long
TLB	Transfer Long Banked
TM	Transfer and Mark
TML	Transfer and Mark Long
TMLB	Transfer and Mark Long Banked

Logical Comparison Instructions

SKMEA	Skip If Memory Equals A
SKBEI	Skip If BL Equals Immediate Field
SKAEI	Skip If A Equals Immediate Field
TAB	Table Look Up

Input/Output Instructions

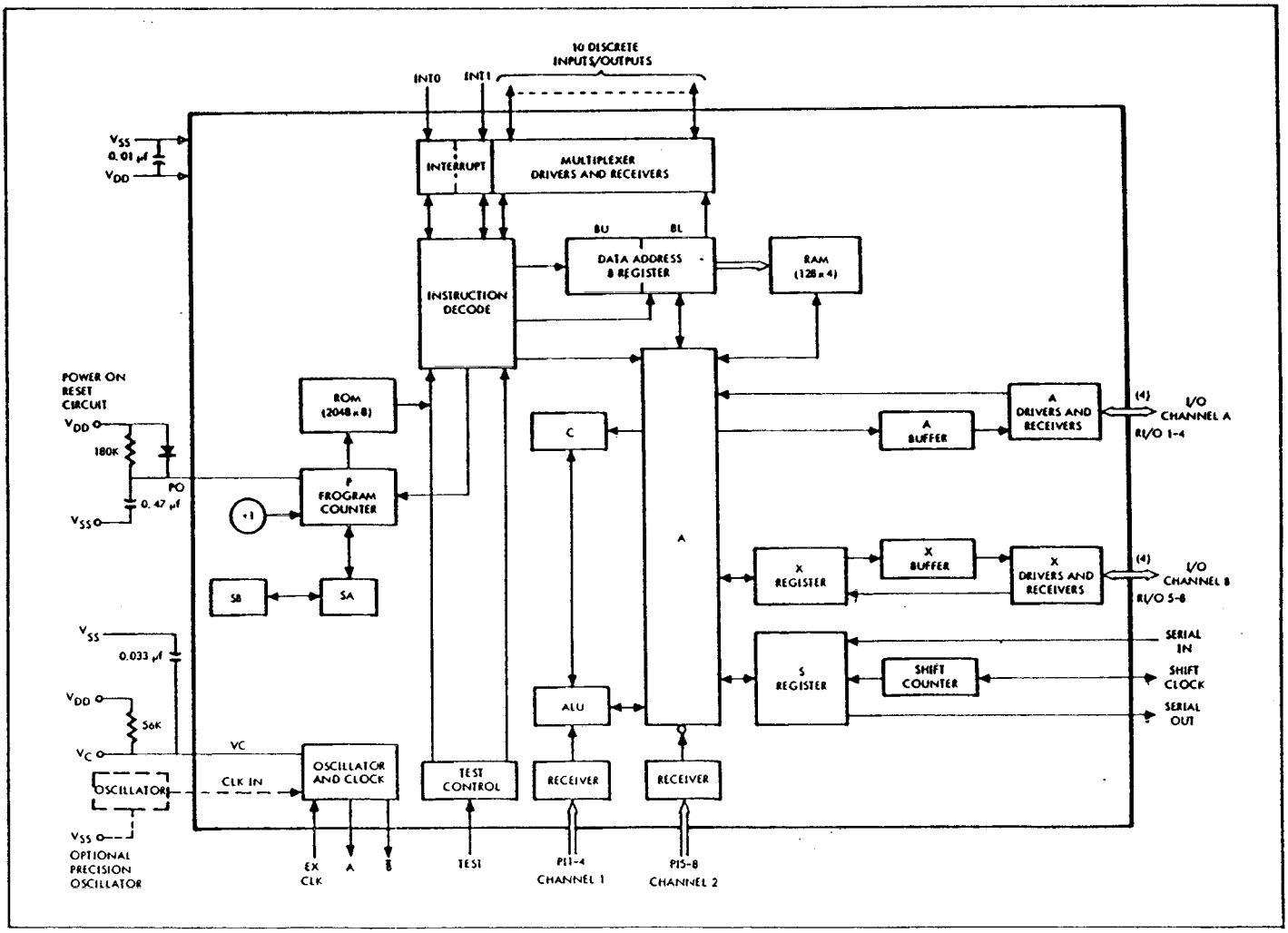
SOS	Set Output Selected
ROS	Reset Output Selected
SKISL	Skip on Input Selected Low
IX	Input X from RIO 5-8
OX	Output X to RIO 5-8
IOA	Input A Receivers to A and output A to RIO 1-4
IOS	Serial Input/Output
I1SK	Input Channel 1. Add to A, Skip If No Carry
I2C	Input Channel 2 and Complement
INT1L	Skip if INT1 Input is Low
INT0H	Skip if INT0 Input is High

Conditional Transfer Instructions

TC	Transfer on Carry Set
TNC	Transfer on No Carry Set
TLC	Transfer Long on Carry Set
TLNC	Transfer Long on No Carry Set
TBF	Transfer on Bit in Memory False
TBT	Transfer on Bit in Memory True
TLBF	Transfer Long on Bit in Memory False
TLBT	Transfer Long on Bit in Memory True
TE	Transfer on A = Memory
TNE	Transfer on A ≠ Memory
TLE	Transfer Long on A = Memory
TLNE	Transfer Long on A ≠ Memory
TIH	Transfer if Input High
TIL	Transfer if Input Low
TLIH	Transfer Long if Input High
TLIL	Transfer Long if Input Low

Register Memory Instructions

L	Load A from Memory
X	Exchange A and Memory
XDSK	Exchange A with Memory. Decrement BL and Skip if BL Counts to 15
XNSK	Exchange A with Memory. Increment BL and Skip if BL Counts to 0



PPS-4/1 MM78 System Block Diagram

SPECIFICATIONS

OPERATING CHARACTERISTICS

Supply Voltage
V_{DD} = -15 Volts ±5%
(Logic "1" = most negative voltage V_{IL} and V_{OL}.)
V_{SS} = 0 Volts (Gnd)
(Logic "0" = most positive voltage V_{IH} and V_{OH}.)
System Operating Frequencies:
90 kHz ±40% with external resistor
Device Power Consumption:
75 mw, typical
Input Capacitance:
<5 pf
Input Leakage:
<10 μa

Open Drain Driver Leakage (R OFF):
<10 μa at -30 Volts
Operating Ambient Temperature (T_A):
0°C to 70°C (Commercial)
0°C to 50°C (Consumer)
Storage Temperature:
-65°C to 120°C

ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 Volts
Maximum positive voltage on any pin +0.3 Volt

TEST CONDITIONS: V_{DD} = -15V ±5%, T_A = 0-70°C

FUNCTION	SYMBOL	LIMITS (VSS = 0) MIN	TYP	MAX	LIMITS (VSS = +5V) MIN	TYP	MAX	TIMING (SAMPLE/ GOOD)	TEST CONDITIONS
Supply Current (Average) for VDD	IDD		5 ma	8 ma		5 ma	8 ma		
Discrete I/O's	V_{IH}	-1.0V			+4.0V			ϕ3	
DI/O 0-DI/O 9	V_{IL}			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	ϕ4*	3.0 ma max.
Channel 1 Input	V_{IH}	-1.5V			+3.5V			ϕ1	
PI1-PI4	V_{IL}			-4.2V			+0.8V		
Channel 2 Input	V_{IH}	-1.5V			+3.5V			ϕ3	
PI5-PI8	V_{IL}			-4.2V			+0.8V		
I/O Channel A	V_{IH}	-1.5V			+3.5V			ϕ3	
RI/O1-RI/O4	V_{IL}			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	ϕ4*	3.0 ma max.
I/O Channel X	V_{IH}	-1.0V			+4.0V			Not sync. Must be stable at ϕ1 and 2.	
RI/O5-RI/O8	V_{IL}			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	ϕ4*	3.0 ma max.
DATA I	V_{IH}	-1.0V			+4.0V			ϕ4	
	V_{IL}			-4.2V			+0.8V		
DATA O	RON							ϕ4**	
INT0	V_{IH}	-1.5V			+3.5V			ϕ3	
	V_{IL}			-4.2V			+0.8V		
INT1	V_{IH}	-1.5V			+3.5V			ϕ1	
	V_{IL}			-4.2V			+0.8V		
Clock	V_{OH}	-1.0V			+4.0V				CL = 50 pf (max.)
A, BP, ($\bar{B}$)	V_{OL}			-10.0V			-5.0V		
EXCLK	V_{IH}	-1.5V			+3.5V			STRAP	F max = 80 kHz
	V_{IL}			-7.0V			-2.0V		
CLK IN	V_{IH}	-1.0V			+4.0V				
	V_{IL}			-10.0V			-5.0V		
Shift Clock	V_{IH}	-1.0V			+4.0V			ϕ34	
Clock	V_{IL}			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	ϕ4**	2.0 ma max.
VC***	V_{IH}								66K ±6%
	V_{IL}								
PO	V_{IH}	-2.0V			+3.0V				Special circuit
	V_{IL}			-6.0V			-1.0V		

* State established by ϕ2 (minimum impedance during ϕ4).
** Same as above except ϕ4 minimum at ϕ2 of next cycle.
*** Connect VC to VDD through a 66KΩ resistor for 90 kHz.

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Telex: J22198

YOUR LOCAL REPRESENTATIVE

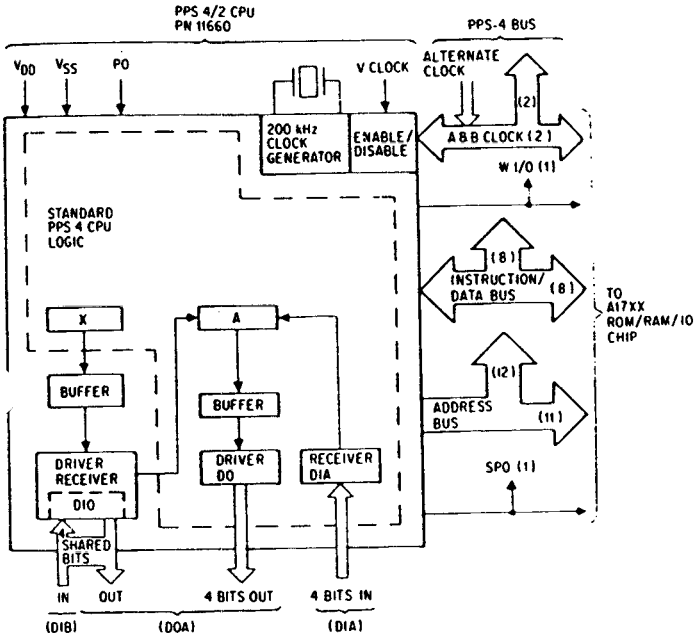
4-bit microprocessor, PMOS

PPS-4, PPS-4/2

Rockwell International Microelectronic Devices
P.O. Box 3669
Anaheim, CA 92803
(714) 632-3729

Alternate sources: AEG Telefunken.

Forming either a three or two-chip processor, the PPS-4 and PPS-4/2 central processor chips provide over 50 instructions and 12 dedicated I/O lines. The 4/2 CPU is a newer version of the 4 and can operate with an inexpensive 3.58 MHz crystal. The PPS-4 requires an external clock. Both processors, though, are totally instruction compatible and have 8-bit instruction/data buses and 11-bit address buses. The one major difference is that the PPS-4/2 CPU automatically floats all output lines when power is turned on; the PPS-4 doesn't. And, the 4/2 can directly drive low-power LED display segments.



The straightforward architecture of the PPS-4 and 4/2 revolves around the 4-bit accumulator and the three four-bit I/O buses. All lines are designed for direct MOS-level interfaces so to connect to other logic families buffer circuits must be used. The PPS-4 requires an external clock while the 4/2 just needs an external crystal.

Comments

The instruction set contains a total of 50 commands that can be grouped as follows: 10 arithmetic and logic, 24 data transfer, six transfer, five skip, four I/O and one special address generation instruction.

Software support for the PPS-4 and 4/2 includes a Fortran IV simulator and cross assembler for use on in-house computer systems and time-share networks as well as resident assemblers, supervisors, text editors and debug routines for use on the PPS MP Universal Assemulator hardware and software development system.

Special features of the software include the capability to perform an automatic memory address modification in addition to the basic data transfer instruction, and software controllable interrupts.

Hardware support for the PPS-4 and 4/2 starts with simple CPU modules designed to plug into the PPS MP Universal Assemulator. Other modules available as plug-ins include memory boards, I/O boards and prototyping modules.

Specifications

Data word size:	4 bits
Address bus size:	12 bits
Direct addressing range:	4096 words
Instruction word size:	8 bits
Number of basic instructions:	50
Shortest instruction/time (Transfer):	5 μs
Longest instruction/time (Load B long):	10 μs
Clock frequency (min/max):	199 kHz
Clock phases/voltage swing:	4/12 V (PPS-4); Internal (PPS-4/2)
Dedicated I/O control lines:	12
Package:	42-pin QUIL
Power requirements:	17 V/26 mA

Hardware

Model	Description	Price (100 qty)
PPS-4	CPU	$18.15*
PPS-4/2	CPU	10.00*
10706	Clock generator	7.45
10738	Bus interface	4.50
11049	Interval timer	8.50
10696	General purpose I/O	8.50
10930	Serial data controller	15.00

*Price as of Oct. 1. Peripheral chip prices were also cut on Oct. 1. Consult distributors for current cost.

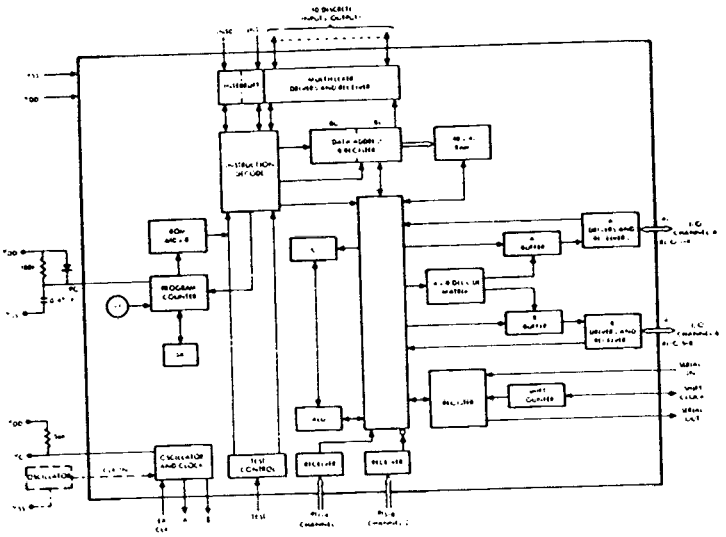
4-bit microcomputer, PMOS

PPS-4/1 family

Rockwell International
P.O. Box 3669
Anaheim, CA 92803
(714) 632-3729

Alternate sources: AEG Telefunken.

A family of 4-bit, single-chip, microcomputers, the PPS-4/1 Models MM75, 76, 77 and 78 include CPU, RAM, ROM, I/O and clock circuitry on a single chip. On-board ROM ranges from 640 to 2048 bytes and on-chip RAM spans 48 to 128 4-bit words. Three special versions of the MM76 are also available—the E version with an expanded ROM, the D version with an a/d converter and the C model with a high-speed counter.



The architecture of the PPS-4/1 devices resembles that of a complete minicomputer—all the necessary circuits are included on a single chip. All chips except the MM77 and 78 have a 48 × 4 bit on-board RAM. The 77 and 78 contain 96 × 4 and 128 × 4 RAMs, respectively. All chips have one 8-bit bidirectional port as well as two conditional interrupt lines, except for the MM75 which has only one interrupt.

Comments

The instruction set of the PPS-4/1 processors is divided into nine basic categories—RAM addressing commands, bit-manipulation directions, register-to-register operations, arithmetic instructions, ROM addressing commands, logic comparison instructions, I/O directions, conditional transfer operations and register/memory instructions.

Software support for the PPS-4/1 family consists of a Fortran IV cross assembler available either for direct purchase or on time-sharing networks (GE and Tymshare). Also available is the PPS MP Universal Assemulator that contains supervisors, assemblers, and a text editor as well as debug routines.

Software features include specialized instructions for the software controllable converter and counter in the MM76D and C versions, as well as a large number of general-purpose I/O commands.

Hardware support for the PPS-4/1 family consists of various processor modules that plug into the PPS MP Universal Assemulator—the complete resident development system for the family. There are also a wide number of support modules for the Assemulator—memory, I/O, personality and prototyping cards are available.

Specifications

Data word size:	4 bits
Address bus size:	internal
Direct addressing range:	internal
Instruction word size:	8 bits
Number of basic instructions:	67 to 69
Shortest instruction/time (Most):	12.5 μs
Clock frequency (min/max):	40/120 kHz
Clock phases/voltage swing:	internal
Dedicated I/O control lines:	22 to 39
Package:	28 pin DIP or 42 and 52-pin QUILs
Power requirements:	15 V/5 mA

Hardware

Model	Description	Price (1000 qty)
MM75	CPU with 640 bytes of ROM	$6.10
MM76	CPU with 640 bytes of ROM	8.00
MM76C	CPU with counter	
MM76D	CPU with a/d converter	
MM76E	CPU (expanded MM76)	
MM77	CPU with 1344 bytes of ROM	9.50
MM78	CPU with 2048 bytes of ROM	10.75

Rockwell

PARALLEL PROCESSING SYSTEM (PPS) DATA SHEET

PPS-4/1 One-Chip Microcomputer Family

MM78L

low-voltage, low power one-chip microcomputer system

SUMMARY

The Rockwell MM78L microcomputer is a complete 4-bit parallel processing system. The MM78L is a low voltage (6.5 to 11 volt range), very low power (15 milliwatts typical) version of the well known PPS-4/1 one-chip microcomputer. All of the microcomputers in the family of PPS-4/1 microcomputers fit the needs of Equipment Designers seeking low-cost systems capable of performing functions in the range of medium complexity. However, the MM78L is especially desirable where low-cost battery operation as the primary or backup power source is required, or where power consumption or heat dissipation is a consideration or where portability is required. The entire PPS-4/1 family of microcomputers is distinguished from competitive microprocessors by superior I/O capability, and by other functional features identified on this page.

On a single LSI chip the MM78L provides a complete system consisting of a versatile Central Processing Unit (CPU), Instruction Decode, two Program Save Registers, Program Memory (ROM), Data Memory (RAM), Program Counter (P), Data Address Register (B), 10 I/O discrete Drivers/Receivers, two 4-bit parallel I/O channels, two 4-bit parallel input channels, a Serial I/O port, Interrupt and Control logic, and a self-contained four-phase Clock Generator circuit.

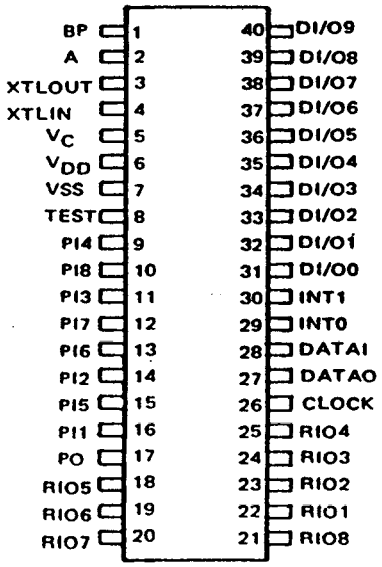
In addition to stand-alone applications, the MM78L can be directly included in other multi-chip systems as a dedicated controller or in other functions. Also two or more MM78L microcomputers can be directly combined to perform parallel processing or control operations. In the design of families of end-products, a total range of features can be designed so that increasingly higher levels of performance can be produced by low-cost wiring changes and chip additions, minimizing design costs and production inventories.

The MM78L may be ordered with combinations of the following features (not every combination is available).

Operating Temperature
- 0°C to +50°C (Consumer)
- 0°C to +70°C (Commercial)
- -40°C to +85°C (Industrial)

Maximum Negative I/O Voltage
- -11 Volts (Standard)
- -30 Volts (Vacuum Fluorescent Drive)

Nominal Internal Clock Frequency
- 100 kHz (±30%) with VC to VDD



MM78L Pin Configuration

ELECTRICAL FEATURES

- Battery Compatible (-6.5 to -11.0 volt operation)
- Low Power 15 milliwatts nominal @ -8.5 volts
- 4 Clock Modes including external crystal
- Low Impedance Drivers
  - DI/O less than 100 ohm @ 10 ma
  - RIO less than 250 ohm @ 6 ma
- Mask Programmed pull-down Resistors on Outputs
- Mask Programmed Enhancement FET pull-downs on Inputs

FUNCTIONAL FEATURES

- Standard 40-pin Dual-In-Line (DIP) package
- MM78L – 2048 8-bit bytes of program memory
- 128 4-bit words (512 bits) of data memory
- Serial input/output capability
- Two interrupt request input lines
- TTL and CMOS compatible
- Six working registers
- 31 input/output ports
- Large instruction set – over 60 instructions
- Multifunction instructions increase throughput
- Single power supply operation (-8.5 volts, -2.5, +2.0 volts)
- Low power (15 milliwatts typical)
- Powerful development aids:
  - SYSTEM 65 with built-in mini-floppy disks and PPS-4/1 Personality subsystem
  - XPO-1 Evaluation Microcomputer module
  - Development Circuit (P/N B7899) provides address and data lines so that Program Memory can be in external PROM or RAM for emulation purposes
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SKMEA	Skip If Memory Equals A
SKBEI	Skip If BL Equals Immediate Field
SKAEI	Skip If A Equals Immediate Field
TAB	Table Look Up

Input/Output Instructions

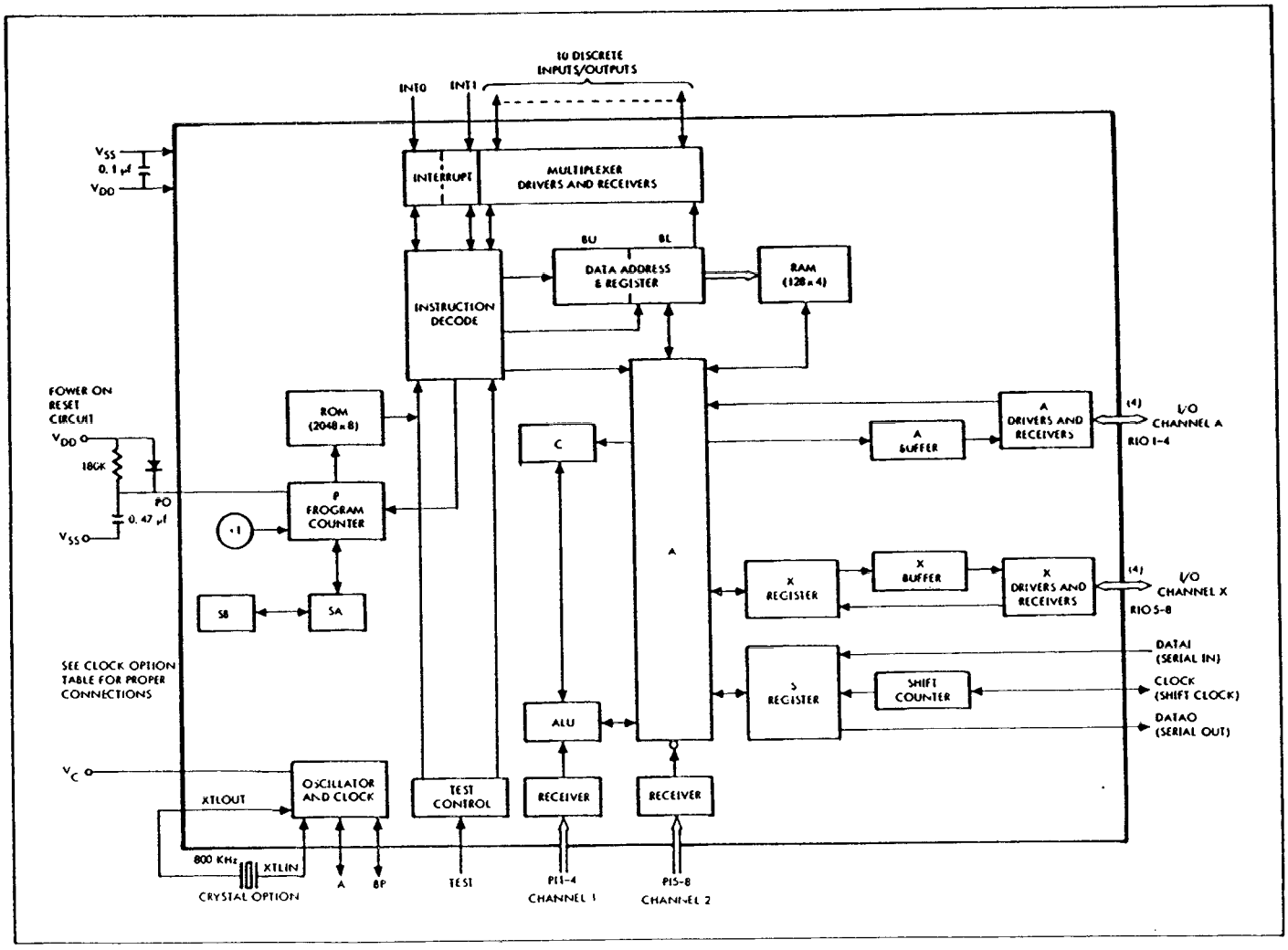
SOS	Set Output Selected
ROS	Reset Output Selected
SKISL	Skip on Input Selected Low
IX	Input X from RIO 5-8
OX	Output X to RIO 5-8
IOA	Input A Receivers to A and output A to RIO 1-4
IOS	Serial Input/Output
I1SK	Input Channel 1. Add to A, Skip If No Carry
I2C	Input Channel 2 and Complement
INT1L	Skip If INT1 Input is Low
INT0H	Skip If INT0 Input is High

Conditional Transfer Instructions

TC	Transfer on Carry Set
TNC	Transfer on No Carry Set
TLC	Transfer Long on Carry Set
TLNC	Transfer Long on No Carry Set
TBF	Transfer on Bit in Memory False
TBT	Transfer on Bit in Memory True
TLBF	Transfer Long on Bit in Memory False
TLBT	Transfer Long on Bit in Memory True
TE	Transfer on A = Memory
TNE	Transfer on A ≠ Memory
TLE	Transfer Long on A = Memory
TLNE	Transfer Long on A ≠ Memory
TIH	Transfer If Input High
TIL	Transfer If Input Low
TLIH	Transfer Long If Input High
TLIL	Transfer Long If Input Low

Register Memory Instructions

L	Load A from Memory
X	Exchange A and Memory
XDSK	Exchange A with Memory. Decrement BL and Skip If BL Counts to 15
XNSK	Exchange A with Memory. Increment BL and Skip If BL Counts to 0



PPS-4/1 MM78L System Block Diagram

PROGRAM COUNTER (P), SA REGISTER AND SB REGISTER

The Program Counter contains the ROM address of the next program instruction. The address in the P Register is automatically incremented each cycle time during normal operation to address the next instruction. In addition, instructions are available to alter the address in the P Register as necessary to fetch an instruction from any address in program memory. After PO reset, the program counter contains address hex 3C0. This location must contain a NOP instruction.

The SA Register is a "save" register which saves the incremented value of current address in the P Register during subroutine execution. This provides a means of returning from a subroutine directly to the next instruction after the subroutine call.

The SB Register provides a second hardware stack register so that two levels of subroutines may be nested in the microcomputer.

PROGRAM MEMORY – READ ONLY MEMORY (ROM)

The ROM provides 2048 bytes of storage for instructions and constants required to operate the microcomputer. Under control of the Program Counter the ROM will read out the addressed instruction which is to be decoded and executed.

INSTRUCTION DECODE

The Instruction Decode logic circuitry interprets the instructions pulled from ROM to provide control for data transfers, arithmetic operations, other processing functions and input/output operations.

DATA ADDRESS REGISTER (B)

The Data Address Register is 7 bits in length and is made up of two segments, B Upper (BU) and B Lower (BL). Data locations in RAM are addressed by all 7 bits and the discrete input/output ports are addressed by the 4 bits in BL when the value in BU is between 0 and 3.

ACCUMULATOR and ARITHMETIC LOGIC UNIT (A, ALU, AND C)

The Primary working register in the MM78L is the Accumulator (A). It is the Accumulator which ties with the Arithmetic Logic Unit (ALU) and the Carry flip-flop (C) to perform binary arithmetic. By means of software routines, decimal arithmetic can be performed. Constants may be loaded into the accumulator from the read only memory or variable data may be loaded from, or exchanged with the random access memory (RAM) under control of the Data Address Register (B). The Accumulator is also the primary path for 4-bit parallel or serial input or output data.

DATA MEMORY (RAM)

The Random Access Memory (RAM) used for data memory contains 128 (MM78L) 4-bit words. The Data Memory can be used to buffer input or output values, hold intermediate results, or be used as a register for timers, counters, comparators, etc.

CLOCK CONTROL (VC, XTLIN, XTLOUT, A, and BP)

The internal Oscillator and Clock circuit generates a four-phase A BP clock signal used for all internal logic functions. The A and BP clock terms are also brought out so external logic can be synchronized. The clock for the MM78L can be selected to operate in one of four modes as shown by the table below. These options are selected by control voltages applied to the VC and XTLIN pins.

A BUFFER

The contents of the Accumulator may be output for control, display, or data transfer functions through the A Buffer. The A Buffer holds the data for output until new data is received from the Accumulator or until the power is turned off.

X BUFFER

The X Buffer is a 4-bit latch that will output the last bit pattern loaded until either a new Output X Register command is executed or power is turned off.

CHANNEL 1 INPUT PORTS (PI1 through PI4)

The parallel input port PI1 through PI4 will be loaded into the contents of the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 1 time) so that asynchronous input signals may be used.

CHANNEL 2 INPUT PORTS (PI5 through PI8)

The inverted state of the inputs at parallel input ports PI5 thru PI8 will be loaded into the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 3 time) so that asynchronous input signals may be used.

CHANNEL A I/O PORTS (RIO1 through RIO4)

The contents of the Accumulator may be output for control or data transfer purposes through the A Buffer. The A Buffer will hold the data output until new data is output or power is turned off.

CHANNEL X I/O PORTS (RIO5 through RIO8)

The four parallel input/output ports of Channel X function as described in X Buffer and X Register paragraphs.

CONDITIONAL INTERRUPTS (INT0 and INT1)

The conditional interrupts INT0 and INT1 may be used to detect external signals and set internal control flip-flops. The receivers are TTL compatible and synchronized.

DISCRETE INPUT/OUTPUT PORTS (DI/O0 through DI/O9)

There are ten discrete input or output lines each of which can be controlled individually under program control. The receivers are fully synchronized to that asynchronous input signals may be used.

X REGISTER

The X Register is an auxiliary register which may be used as temporary storage for 4 bits of data without reference to data memory. The X Register is also used as a data path to the X Buffer output register and from receiver inputs.

S REGISTER – SERIAL INPUT/OUTPUT – SHIFT COUNTER

The S register is a 4-bit serial-in/serial-out, parallel exchange, register which is used as either an auxiliary storage register or buffer for the simultaneous serial input/output functions. The shift rate can be controlled either internally or externally.

Mode	Pins					Frequency
	VC	XTLIN	XTLOUT	A	BP	
INTERNAL	*V_C	VSS	–	OUT	OUT	100 kHz ±30% @ -8.5V
EXTERNAL	VSS	CLOCK	–	OUT	OUT	400 – 800 kHz @ -8.0V
CRYSTAL**	VSS	XTAL	XTAL	OUT	OUT	800 kHz @ -8.0V
SLAVE	V_{DD}	V_{DD}	–	IN	IN	50 kHz – 100 kHz @ -8.5V

*Can be adjusted to vary frequency – Normally set to V_{DD}

**Suggest Murata part number CSB800A4 with 2-120 pF shunt capacitors.

SPECIFICATIONS

OPERATING CHARACTERISTICS

Supply Voltage:
- V_{DD} = -8.5 Volts, -1.5, +2.0 Volts (MM78L-1)
- V_{DD} = -8.5 Volts, -2.5, +2.0 Volts (MM78L)
- (Logic "1" = most negative voltage V_{IL} and V_{OL}.)
- V_{SS} = 0 Volts (Gnd)
- (Logic "0" = most positive voltage V_{IH} and V_{OH}.)

System Operating Frequencies:
- (1) Internal: 100 kHz Nominal at V_{DD} = -8.5V
- (2) External 800 kHz Crystal: 100 kHz

Device Power Consumption: 15 mw, typical

Input Capacitance: <5 pf
Input Leakage: <10 μa
Open Drain Driver Leakage (R OFF): <10 μa at -30 Volts
Operating Ambient Temperature (T_A):
- 0°C to +70°C (Commercial): MM78L
- 0°C to +50°C (Consumer): MM78L-1
- -40°C to +85°C (Industrial): MM78L-2

Storage Temperature: -55°C to 125°C

ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 Volts
Maximum positive voltage on any pin +0.3 Volts

TEST CONDITIONS: V_{DD} = -8.5V, T_A = 0-70°C

INPUT/OUTPUT	SYMBOL	LIMITS (VSS = 0) MIN	TYP	MAX	LIMITS (VSS = +5V) MIN	TYP	MAX	TIMING (SAMPLE/GOOD)	TEST CONDITIONS
Supply Current	IDD		1.75 ma	3 ma		1.75 ma	3 ma		Internal Clock
(Average) for VDD			3.0 ma	6 ma		3.0 ma	6 ma		Slave Clock
Discrete I/O's DI/O 0-9	V_{IH}	-1.0V			+4.0V			ϕ3, ϕ4	
	V_{IL}			-4.2V			+0.8V		
	RON			100 ohms			100 ohms	ϕ4*	10.0 ms max.
Channel 1 Input PI1-PI4	V_{IH}	-1.5V			+3.5V			ϕ1	
	V_{IL}			-4.2V			+0.8V		
Channel 2 Input PI5-PI8	V_{IH}	-1.5V			+3.5V			ϕ3	
	V_{IL}			-4.2V			+0.8V		
I/O Channel A RIO1-RIO4	V_{IH}	-1.5V			+3.5V			ϕ4	
	V_{IL}			-4.2V			+0.8V		
	RON			250 ohms			250 ohms	ϕ4*	6.0 ms max.
I/O Channel B RIO5-RIO8	V_{IH}	-1.5V			+3.5V			ϕ4	
	V_{IL}			-4.2V			+0.8V		
	RON			250 ohms			250 ohms	ϕ4*	6.0 ms max.
DATAI	V_{IH}	-1.0V			+4.0V			ϕ4	
	V_{IL}			-4.2V			+0.8V		
DATAO	RON			500 ohms			500 ohms	ϕ4**	3.0 ms max.
INT0	V_{IH}	-1.5V			+3.5V			ϕ3	
	V_{IL}			-4.2V			+0.8V		
INT1	V_{IH}	-1.5V			+3.5V			ϕ1	
	V_{IL}			-4.2V			+0.8V		
A, BP	V_{OH}	-0.3V			+4.7V				CL = 50 pf (max) Int, Ext or XTL Clock
	V_{OL}			-4.7V			+0.3V		
A, BP	V_{IH}	-0.6V			+4.4V				Slave Clock
	V_{IL}			-4.4V			+0.6V		
XTLIN	V_{IH}	-1.0V			+3.5V			-4.0V	
	V_{IL}			-6.0V			-1.0V		
CLOCK	V_{IH}	-1.0V			+4.0V			ϕ3, ϕ4	
	V_{IL}			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	ϕ4**	2.0 ms max.
VC	V_{IH}								V = 11.0V max.
	V_{IL}								
PO	V_{IH}	-2.5V			+2.5V				Special circuit
	V_{IL}			-5.0V			0V		

*State established by ϕ2 (minimum impedance during ϕ4).
**Same as above except ϕ4 minimum at ϕ2 of next cycle.

NOTES:

MASK PROGRAMMED PULL-DOWN RESISTORS ON OUTPUTS

Resistor pull-downs are available as an option on all RIO, CLOCK, DATAO and DI/O outputs. These pull-downs are connected to V_{DD}. The following values ±50% are available: 5K, 10K, 25K, or Open Circuit. The 5K ohm option is not available on the clock or DATAO outputs.

PULL-DOWNS ON INPUTS

MOS FET pull-downs are also available as an option on the PI, INT, and DATAI inputs. The output current is 50 μa ±35 μa with the input grounded and V_{DD} at -8.5 volts.

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YOUR LOCAL REPRESENTATIVE

)CKWELL PARALLEL PROCESSING SYSTEM (PPS)

PS-4/1 ONE-CHIP
ICROCOMPUTERS

PRODUCT DESCRIPTION
OCTOBER 1978
REVISION: 4
DOCUMENT NO. 29410 N42

SERIES MM77

ONE-CHIP MICROCOMPUTERS

Rockwell International

Rockwell Microelectronic Devices
P.O. Box 3669
Anaheim, Calif. 92803

PPS-4/1 SUPPORTING DOCUMENTATION

The following documents provide additional PPS-4/1 design information for aiding in the implementation of this device in your system:

- PPS-4/1 Programming Manual — Document #29410N38
- PPS-4/1 Prototyping using the PROM Evaluation Module — Document #29410N20
- PPS-4/1 Operator's Manual for Universal Assemulator — Document #29400N37

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PPS-4/1 MM77, MM78 SINGLE CIRCUIT MICROCOMPUTER SYSTEMS

INTRODUCTION

The PPS-4/1 MM77 and MM78 are members of a family of single-circuit microcomputers from Rockwell International. The circuits contain a read only memory for the program memory functions, a random access memory for data, parameter and working storage, and a sophisticated input/output capability which provides a high degree of flexibility for microcomputer and controller applications. The combination of these functions provide the most powerful one chip microprocessors available to date.

The PPS-4/1 MM77 and MM78 are designed to supplement the PPS-4/2, the PPS-4, the PPS-8, and the PPS-8/2 microcomputer systems by providing a low-cost, stand-alone capability for less complex systems or to provide peripheral control functions to directly augment the larger PPS family systems.

PPS-4/1 systems may be operated in tandem to perform parallel processing functions in multi-computer configurations.

FEATURES

- MM77 - 1344 8-bit bytes of program memory (10752 bits)
- MM78 - 2048 8-bit bytes of program memory (16384 bits)
- MM77 - 96 4-bit data words (384 bits)
- MM78 - 128 4-bit data words (512 bits)
- Table look up instruction
- Automatic address modification
- Two 4-bit input channels
- Two 4-bit input/output channels
- 10 discrete input/output lines
- Clocked simultaneous serial input/output capability
- Pulse output capability
- Two interrupt request input lines
- TTL and CMOS compatible
- Arithmetic logic unit and 5 working registers
- On-chip resistor controlled 80 kHz (nominal) clock operator which may be externally synchronized
- One clock cycle execution (nominal 12.5 microseconds) for most instructions
- Easy circuit level testing by user
- Large instruction set — over 50 instructions
- Multifunction instructions increase throughput
- Single power supply operation (15 volts ±5%)
- Two-level subroutine nesting
- Compact quad-in-line 42-pin package
- Sophisticated development aids
  - General Electric Software Assembler
  - Development Circuit with PROM Module for Program Memory
  - PPS Universal Assemulator with PPS-4/1 Personality Board for Program and Hardware Development
  - XPO-1 Development Microcomputer
  - Scheduled and Special Training Courses
  - International Applications Engineering Support
- Low power (75 milliwatts typical, 125 milliwatts max)

SYSTEM DESCRIPTION

The PPS-4/1 MM77, MM78 circuits have been designed to provide low-cost flexible, circuit elements which may be used by themselves, in conjunction with other PPS-4/1 circuits, or in conjunction with other PPS families of circuits (PPS-4/2, PPS-4, or PPS-8). The PPS-4/1 MM77 and MM78 may each be used as as compact stand-alone microcomputer, as a low-cost special controller, as a programmable peripheral controller for one of the larger PPS systems, or as a universal logic element. The PPS-4/1 MM77 or MM78 as a universal logic element can economically perform functions such as counting, time delays, comparisons, sequencing, function generation, etc. to control a set of output lines based upon conditions presented on a set of input lines.

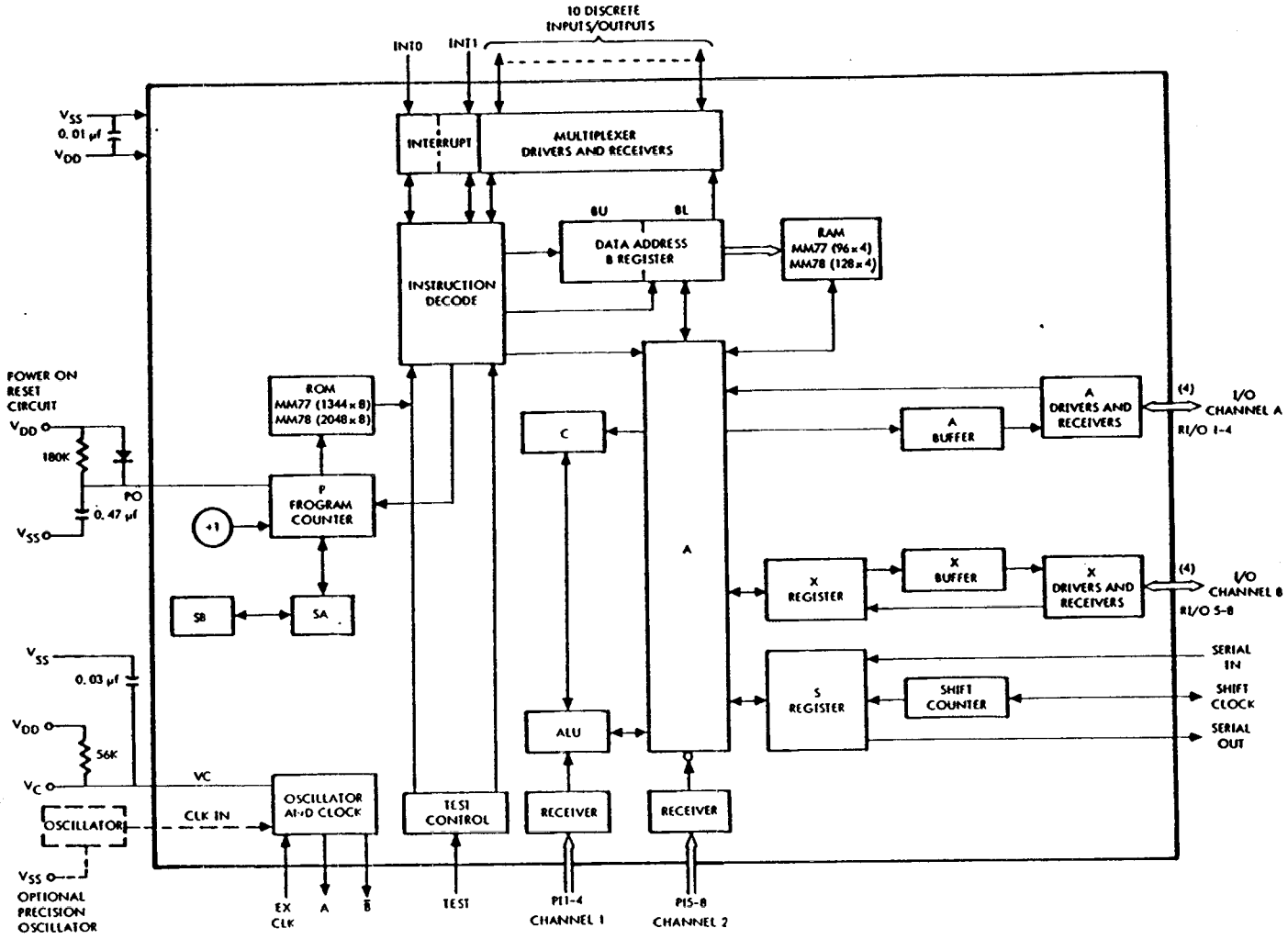
A block diagram of the PPS-4/1 MM77 or MM78 is shown in Figure 1.

ACCUMULATOR AND ARITHMETIC LOGIC UNIT (A, ALU, AND C)

The primary working register in the PPS-4/1 MM77, MM78 is the Accumulator (A Register). It is the Accumulator which ties with the Arithmetic Logic Unit (ALU) and the carry flip-flop (C) to perform either binary or decimal arithmetic. Constants may be loaded into the Accumulator by appropriate instructions from the read only memory or variable data may be loaded from, or exchanged with the random access memory (RAM) under control of the Data Address Register (B). The Accumulator is also the primary path for 4-bit parallel or serial input or output data although either the X or S Registers may also be involved.

A BUFFER

The contents of the Accumulator may be output for control or data transfer purposes through the A Buffer. The A Buffer consists of four latched open drain circuits which will hold the data output until new data is output or power is turned off.



Note: The development circuits for the PPS-4/1 are identical to the PPS-4/1 MM77, MM78 production circuits except that, in place of the ROM, terminals are brought out to an external memory and control system.

Figure 1. BLOCK DIAGRAM OF PPS-4/1 MM77, MM78 MICROCOMPUTERS

DRIVER AND RECEIVER CIRCUITS

The outputs of each of the latches in the A Buffer, X Buffer and discrete input/output flip-flops are through open drain drivers which drive to either the VSS logic level or float. When power is applied, the power on reset circuit (PO) causes all of the outputs to be automatically set to a float condition. (All output flip-flops are reset.)

Input signals share the same lines as outputs for the A and X Register (RIO 1-8) lines and the discrete input/output lines. To use one of these lines as an input, it is necessary to set the output on that line into a float condition. The external signal may then either take the line high to VSS or to the appropriate low logic level. The input command, in effect, samples the logic level on the pin and inputs it appropriately.

If the external circuit is designed so that it may be connected to VSS, the mechanization of the PPS-4/1 MM77 and MM78 allow a software masked input capability. To mask out any input bits, the output in that bit position is set to the VSS level rather than the float situation. The external input in that position will always be input on the VSS level while other bits, input through the floating lines, will be at logic one or zero levels as determined by the external system. This is in effect a logical AND between the buffer latches and the input signal.

X REGISTER

The X Register is an auxiliary register which may be used temporary storage for 4 bits of data without reference to data memory. The X Register is also used as a data path to the X Buffer output register and from receiver inputs as discussed above and in the Electrical Interface Section of this document.

X BUFFER

The X Buffer comprises four latches which will output the last bit pattern loaded until either a new Output X Register command is executed or power is turned off. The power on reset signal resets all of the latches so the outputs float.

S REGISTER - SERIAL INPUT/OUTPUT - SHIFT COUNTER

The S Register is a 4-bit parallel-in/parallel-out, serial shift register which is used as either an auxiliary storage register or a buffer for the simultaneous serial-in/serial-out capabilities in the microcomputer. The 4 bits to be serially output are loaded into the S Register by exchanging the contents of the Accumulator and the S Register. The state of the serial output line is immediately set by the contents of the most significant bit position. When an Input/Output Serial instruction is executed, or an external shift clock input is provided the four bit contents of the S Register are shifted out (most significant bit first). The data shift rate is under the control of the Shift Counter and is one half the rate of the internal clock frequency when the IOS instruction is used. The Input/Output Serial instruction also causes the Shift Counter to provide four shift clock signals to the external system. Under external shift control by a signal on the same shift clock line, the shift rate may be any value at or below the clock frequency. Both the serial data and shift clock outputs are open drain drivers which are set to the float state when power is turned on.

At the same time that the 4-bit data is being shifted out through the serial output line, 4 bits of data are shifted into the S Register from the serial input line. An exchange of the Accumulator and S Register brings the 4 bits of serial input data into the Accumulator where it can be processed or stored. The S Register may be simultaneously reloaded if more than 4 bits of data are being transmitted.

When the external clocking mode is used it may be necessary for the system designer to establish a handshake protocol to establish when data is to be moved and when the move is completed.

DISCRETE INPUT/OUTPUT PORTS (DI/00 THROUGH DI/09)

There are ten discrete input or output lines and two special sets of request interrupt input lines. Buffer flip-flops associated with all 12 of these channels may be individually set, or reset under program control. They are all reset when power is applied. There is a buffer flip-flop associated with each of these channels which is selected by the least significant 4 bits of the Data Address Register. A Set Output Selected instruction causes the selected output to be at the VSS level and a Reset Output Selected instruction causes it to float. When the output is floating, an input signal level on that port may be tested by a Skip On Input Selected Low instruction. When the buffer flip-flops are not used specifically for input/output functions, they may be used as one bit status registers. In this case external pull up resistors connected to VDD must be used.

CONDITIONAL INTERRUPTS (INT0 AND INT1)

The conditional interrupt request lines may be used in a number of different ways. In some respect these ports are similar to the discrete input/output channel in that they may be addressed by the B Lower portion of the B Register (BL = decimal 11 selects INT0 and BL = decimal 10 selects INT1) to set or reset the selected flip-flop.

However, they differ in several respects. The Skip On Input Selected Low instruction tests the state of the flip-flop and not the state of the input line. To test the state of the signal on the input line it is not necessary to set the flip-flop to any predetermined state as there is no output driver on these signal lines. The level on these two lines may be tested directly by an INT0H or INT1L instruction for INT0 and INT1 inputs respectively without any pre-conditioning. This gives a pseudo interrupt capability by allowing a direct test of the input signal. The INT0H instruction causes the next instruction to be skipped if the input on INT0 is high and the INT1L instruction will cause it to skip if the signal on the INT1 line is low.

Another difference in these two signals is that they may be used to detect a pulse input of a duration longer than one clock cycle. In this case, the associated flip-flop is preset to the set state so that an incoming high signal (positive pulse) on INT0 or an incoming low signal (negative pulse) on INT1 which lasts longer than a clock cycle will reset the flip-flop. The state of the flip-flop may then be tested by addressing it with BL and executing a Skip On Input Selected Low instruction.

CHANNEL 1

Channel 1 is a 4-bit input port which automatically adds the input value to the contents of the Accumulator and skips the next instruction if no carry is generated. Many times

a microcomputer is called upon to react to a specific value when it is input. This input channel may be used to input and test the value in a single cycle time. If it is desired to just input the value, the Accumulator can be loaded with zero and then when the Input Channel 1 instruction is executed it will load the input value into the Accumulator.

CHANNEL 2

Channel 2 is a 4-bit input port which on command replaces the contents of the Accumulator with the complement of the value on the input lines. If the input value is from TTL or CMOS logic, the inversion causes the equivalent value to appear in the Accumulator.

PROGRAM COUNTER (P)

The 11-bit Program Counter is set to a specific initial value (hexadecimal address 3C0) when power is applied to the microcomputer. The contents of the Program Counter address read-only memory to identify the specific instruction to be executed. Then, unless the instruction is a transfer instruction, the contents of the Program Counter are incremented so that the next instruction may be selected. This process repeats until a transfer or transfer and mark instruction is executed. The transfer instruction may set a specific location into the least significant 6 bits (T), the least significant 10 bits (TL) while setting bit 11 to zero, or the least significant 10 bits with bit 11 set to one (TLB).

Similar alternatives are available for the transfer and mark instructions which are used to call subroutines. The TM instruction selects one of 64 locations in a specific area, the TML and TMLB sets the least significant 10 bits and sets the most significant bit as above. These instructions, however, mark a return location so that the subroutines may return to the next instruction location after the one that called it. This is accomplished by incrementing the Program Counter prior to setting the new value into it, and saving the incremented value in the SA Register.

SA REGISTER

When a subroutine call is executed by one of the transfer and mark instructions, the contents of the SA Register are pushed into the SB Register and are then replaced by the incremented value of the Program Counter.

When a return instruction is executed in the subroutine, the contents of the SA Register are popped into the Program Counter and the SA Register contents are replaced by the contents of the SB Register.

SB REGISTER

The SB Register provides a second hardware stack register so that two levels of subroutines may be nested in the microcomputer. Software techniques discussed later show how to extend the number of levels of subroutines.

READ ONLY MEMORY (ROM)

The Read Only Memory (ROM) provides the storage for instructions and constants (as immediate field portions of instructions) for the microcomputer. It is controlled by the Program Counter to read out each instruction to be executed. The MM77 contains 1344 instruction bytes and the MM78 contains 2048 instruction bytes.

INSTRUCTION DECODE

The instructions are decoded in the Instruction Decode circuits which then issue control signals to all appropriate portions of the microcomputer as necessary to perform the desired operations.

DATA ADDRESS REGISTER (BU AND BL)

The Data Address Register is 7 bits in length and is made up of two segments, B Upper (BU) and B Lower (BL). Data memory in RAM is addressed by all 7 bits and discrete input/output ports are addressed by the 4 bits in BL when the most significant bit of B Upper is zero.

The BL portion is also an up-down counter which may be automatically incremented or decremented and tested for overflow or underflow by the Exchange Increment and Skip, Exchange Decrement and Skip, Increment B, or Decrement B instructions.

DATA MEMORY (RAM)

The Random Access Memory (RAM) is used for data memory words of 4 bits each. This memory is used to buffer input or output values, hold intermediate results and also may be used as registers used for timers, counters, comparators, etc. when the microcomputer is used as a universal logic element. The MM77 RAM contains 96 words and the MM78 RAM contains 128 words.

CLOCK CONTROL (VC, CLKIN, EXCLK, AND OSCILLATOR)

The microcomputer may be driven by either its internal clock or an external clock source. Regardless of the source, a resistor must be connected between the VC input and VDD. The resistor value may be used to slightly vary the operating frequency; typical values are 56K ohms for 80 kHz and 47K ohms for 100 kHz.

The nominal 80 kHz internal clock may be used to drive the microcomputer in systems where precise timing is not required. The internal clock is selected by tying the CLKIN pin to VDD and the EXCLK pin to VSS. The A and $\overline{B}$ clock terms are brought out so external logic can be synchronized.

An external frequency reference in the range 40 kHz to 100 kHz may be used in systems when precise timing is required. When the EXCLK pin is tied to VDD, the microcomputer will be driven by an external square wave oscillator input through the CLKIN pin.

A specific definition of the clock waveforms is discussed in the section on Electrical Interface.

S-4/1 TESTABILITY (TEST)

Another advantage of the PPS-4/1 microcomputer family is testability both at the factory and user levels. When a test state is indicated by the test input line, the PPS-4/1 goes into a test mode which tests ROM and allows testing of the RAM and instruction logic.

POWER SUPPLY

When inputs and outputs interface with other PMOS devices, or CMOS devices, VSS = GND and VDD = -15V ±5% provide proper interface levels. When interfacing with TTL devices, VSS should be +5 and VDD at -10 volts.

POWER ON RESET (PO)

The PO signal is derived from an external resistor, diode, and capacitor pulse shaping network which is tied to the power supply as shown in Figure 1. When power comes on, this circuit automatically sets the Program Counter to a fixed starting location and all outputs are set to a "float" (-V) state. The Program Counter then initiates the first instruction (which must be a Set Carry, Reset Carry or NOP instruction) to be read from the read only memory (ROM) into the instruction decode logic. After executing the first instruction the Program Counter increments so that the second and subsequent instructions may be recalled from memory and executed.

PPS-4/1 MM77, MM78 INSTRUCTIONS

The PPS-4/1 MM77 and MM78 have an extremely sophisticated instruction set which is summarized in Table 1.

Table 1. MM77, MM78 INSTRUCTION SET

Op Code	Bytes	Cycles	Description
RAM Addressing Instructions			
XAB	1	1	Exchange Accumulator with B Lower (least significant 4 bits)
LBA	1	1	Load B Lower from Accumulator
*LB**	1	1	Load B Upper with zero and B Lower with immediate field
*EOB**	1	1	Exclusive OR B Upper with three bit immediate field
†*LBL**	2	2	Load B Register Long with 7 bit (4 bits 1st byte, 3 bits 2nd byte) immediate field. This instruction should not be skipped.
†*INCB	2	2	Increment B Lower and modify B Upper with 2 bit immediate field; Skip if BL counts to 0. This instruction should not be skipped.
†*DECB	2	2	Decrement B Lower and modify B Upper with 2 bit immediate field; Skip if BL counts to 15. This instruction should not be skipped.
SAG	1	1	Special address generation. Uses 011 for B Upper and actual value of B Lower for addressing memory or Discrete I/O for next cycle only. Does not change B Upper in the register.
Bit Manipulation Instructions			
*SB	1	1	Set Bit in word in memory. Specific bit designated by 2 bit immediate field and specific word addressed by B Register.
*RB	1	1	Reset Bit in word in memory. Specific bit designated by 2 bit immediate field and specific word addressed by B Register.
*SKBF	1	1	Skip on designated Bit in addressed Memory when bit is false (zero). Bit is selected by 2 bit immediate field.

Table 1. MM77, MM78 INSTRUCTION SET (continued)

Op Code	Bytes	Cycles	Description
Register to Register Instructions			
LXA	1	1	Load X Register from Accumulator
XAX	1	1	Exchange Accumulator and X Register contents
XAS	1	1	Exchange Accumulator and S Register contents
Register Memory Instructions			
*L	1	1	Load Accumulator from Memory and modify B Upper with 2-bit immediate field
*X	1	1	Exchange Accumulator with Memory and modify B Upper with 2-bit immediate field
*XDSK	1	1	Exchange Accumulator with Memory and modify B Upper with 2-bit immediate field; Decrement B Lower and Skip if BL counts to 15
*XNSK	1	1	Exchange Accumulator with Memory and modify B Upper with 2-bit immediate field; Increment B Lower and Skip if BL counts to zero
Arithmetic Instructions			
A	1	1	Add Memory to Accumulator (carry not used or set)
AC	1	1	Add Memory and Carry to Accumulator; form sum and carry
ACSK	1	1	Add Memory and Carry to Accumulator; Skip if resulting Carry equals "one"
DC	1	1	Decimal Correct (Add 6 with no carry in or out and no skip)
COM	1	1	Complement Accumulator
RC	1	1	Reset Carry
SC	1	1	Set Carry
SKNC	1	1	Skip on No Carry
*LAI***	1	1	Load Accumulator with contents of immediate field
*AISK	1	1	Add Accumulator and Immediate field; Skip on No Overflow. No Carry is set or used. (AISK 6 = DC so no skip occurs)
ROM Addressing Instructions			
RT	1	2	Return from Subroutine
RTSK	1	3	Return from Subroutine and Skip first instruction. All transfer bytes may be skipped. Only macro instructions marked † may not be skipped.
T	1	2	Transfer on-page to 6 bit immediate field location
NOP	1	1	No Operation

Table 1. MM77, MM78 INSTRUCTION SET (continued)

Op Code	Bytes	Cycles	Description
ROM Addressing Instructions (continued)			
TL	2	3	Transfer Long off-page to pages 0 through 15 (addresses #000 thru #3FF)
TLB	3	4	Transfer Long Banked to pages 16 through 29 (addresses #400 thru #77F)
TM	1	2	Transfer and Mark to special subroutine page SR0 (addresses #7CO thru #7FF)
TML	2	3	Transfer and Mark Long to subroutine on pages 0 through 15 (addresses #000 through #3FF)
TMLB	3	4	Transfer and Mark Long Banked to subroutine on pages 16 through 29 (addresses #400 thru #77F)
Logical Comparison Instructions			
SKMEA	1	1	Skip on Memory Equals Accumulator
*SKBEI	2	2	Skip on B Lower Equals Immediate field
*SKAEI	2	2	Skip on Accumulator Equals Immediate field (SKAEI #15 is not valid)
TAB	1	3+N	Table Look Up. Based upon value in Accumulator (N), execute 1 instruction byte, then skip next N+1 instruction bytes before executing next instruction.
Input/Output Instructions			
SOS	1	1	Set Output, bit selected by B Lower to VSS
ROS	1	1	Reset Output, bit selected by B Lower, to -V
SKISL	1	1	Skip on Input Selected Low (-V) on bit selected by B Lower. Bit sampled during prior cycle.
IX	1	1	Input to X Register from RIO lines 5 thru 8
OX	1	1	Output from X Register to RIO lines 5 thru 8
IOA	1	1	Input A Receivers to Accumulator and Output A to A Buffer to RIO lines 1 thru 4 (mask option to also output X to X Buffer)
IOS	1	1	Serial Input and Output from S – shifting takes 8 cycles concurrent with other instruction operations
I1SK	1	1	Input Channel 1, Add to A and Skip if No Carry is generated
I2C	1	1	Input Channel 2 to A and complement
INT1L	1	1	Skip on INT1 equals -V
INT0H	1	1	Skip on INT0 equals VSS

Table 1. MM77, MM78 INSTRUCTION SET (continued)

Op Code	Bytes	Cycles	Description
Conditional Transfer Instructions†			
†TC	2	3-2	Transfer within page on Carry Set
†TNC	3	4-3	Transfer within page on No Carry Set
†TLC	3	4-3	Transfer Long on Carry Set
†TLNC	4	5-3	Transfer Long on No Carry Set
†TBF	3	4-3	Transfer within page on Bit in Memory False
†TBT	2	3-2	Transfer within page on Bit in Memory True
†TLBF	4	5-3	Transfer Long on Bit in Memory False
†TLBT	3	4-3	Transfer Long on Bit in Memory True
†TE	3	4-3	Transfer within page on A Equal Memory
†TNE	2	3-2	Transfer within page on A Not Equal Memory
†TLE	4	5-3	Transfer Long on A Equal Memory
†TLNE	3	4-3	Transfer Long on A Not Equal Memory
†TIH	2	3-2	Transfer within page if Input Selected by B Lower is High
†TIL	3	4-3	Transfer within page if Input Selected by B Lower is Low
†TLIH	3	4-3	Transfer Long on Input Selected High
†TLIL	4	5-3	Transfer Long on Input Selected Low

*The immediate field (IF) is two, three, four or six bits which are included as part of the 8-bit instruction. If not specified otherwise the immediate field is 4 bits.

**When LB, EOB or LBL instructions appear in sequence as a string of LB, EOB or LBL or mixtures of LB, EOB and LBL instructions only the first one of them will be executed. The remainder of the LB, EOB or LBL instructions in the sequence will be ignored except that the first EOB after an executed LB instruction will also be executed.

***When more than one LAI instruction occurs in sequence, only the first LAI instruction encountered will be executed. The remainder of the LAI instructions in the string will be ignored.

†These are all macro instructions which must not be preceded by an instruction which executes a skip. For the conditional transfer instructions, the first number in the cycles column indicates number of cycles when condition is met and second number indicates number of cycles when the condition for transfer is not met.

Numbers preceded by # are hexadecimal numbers.

Note 1: Whenever an instruction is skipped (i.e., ignored) the number of cycles required is equal to the number of bytes in the skipped instruction (e.g. TL takes two cycles to skip).

Note 2: A subroutine called by a TM may not execute an SKBEI or SKAEI when they are followed by a transfer from the extension page (SR1) to the entry page (SR0) prior to executing the return (RT or RTSK) instruction.

MULTIFUNCTION INSTRUCTIONS

Much of the power of the MM77, MM78 instruction set comes from a group of multifunction instructions which in addition to performing a basic function such as load or exchange also set up the next address and perhaps test to see if the function is complete so a computational loop may be terminated automatically.

To understand these instructions it is necessary to understand the operation of the Data Address Register B. The B Register has two segments, B Upper and B Lower. B Lower is four bits in capacity and B Upper is three as shown in Figure 2. The bits in the B Register may be modified in groups of 2, 3, 4 or 7 bits as shown in Table 2. It can be seen from the data memory map (Figure 3), that B Upper addresses a row and B Lower selects the column within that row.

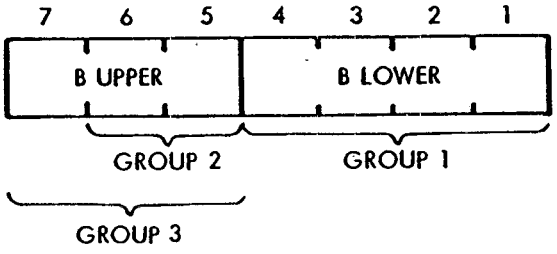


Figure 2. ADDRESS REGISTER ORGANIZATION

Suppose that a number is in a register, REGISTER 1, which occupies Row 2, Columns 0 through 5. The program to initially set the B Register address to Row 2, Column 5, and then shift the contents of the register left 1 decimal place with a zero loaded into the vacated position is as follows:

```
ONE     LBL     #25
TWO     LAI     0
LSFT    XDSK    0
FOUR    T       LSFT
```

Instruction ONE sets the B Register to hexadecimal 25 (the # symbol indicates a hexadecimal number rather than a decimal number). Instruction TWO loads zero into the Accumulator. The instruction in location LSFT (XDSK) causes the contents of the Accumulator to be exchanged with the addressed memory cell (initially #25), decrements the B Lower address to point to #24 and leaves the B Upper register alone since 0 Exclusively ORed with anything leaves it unchanged.

The XDSK instruction also tests to see if the complete register has been shifted by checking the decremented B Lower. If B Lower decrements from zero to #F, then the next instruction will be skipped. Since, after completion of the 1st XDSK instruction, B Lower is 4, no skip occurs. Consequently the transfer instruction is not skipped and the process is repeated. The prior contents of #25 which are in the Accumulator are exchanged with #24 and the address is decremented and tested again. Subsequently the

Table 2. DATA ADDRESS MODIFICATION

Instruction		Address Bits Modified			Condition to Automatically Terminate Process
Op Code	Immediate Field	Group 3 All Bits of BU	Group 2 2 LSBs of BU	Group 1 BL	
XAB*	—	—	—	Exchanged with A	—
LBA	—	—	—	Replaced with A	—
LBL	Upper/Lower	Replaced (2nd)	—	Replaced (first)	—
LB	Lower	Zero	—	Replaced	—
EOB	Upper	Exclusive OR	—	No Change	—
INCB*	2 bit Upper	—	Exclusive OR	Increment and Test for 0	BL counts to 0
DECB*	2 bit Upper	—	Exclusive OR	Decrement and Test for #F	BL counts to #F
L	2 bit Upper	—	Exclusive OR	No Change	—
X	2 bit Upper	—	Exclusive OR	No Change	—
XDSK*	2 bit Upper	—	Exclusive OR	Decrement and Test for #F	BL counts to #F
XNSK*	2 bit Upper	—	Exclusive OR	Increment and Test for 0	BL counts to 0
SAG	—	Unchanged but effectively 011 for 1 cycle	—	—	—

*In the cycle immediately following these instructions, the contents of BU and BL registers are correct as modified. However, in the cycle immediately following the address modification instruction, instructions which address memory will have B Upper modifications completed but the old value of BL will be used in forming the effective memory address.

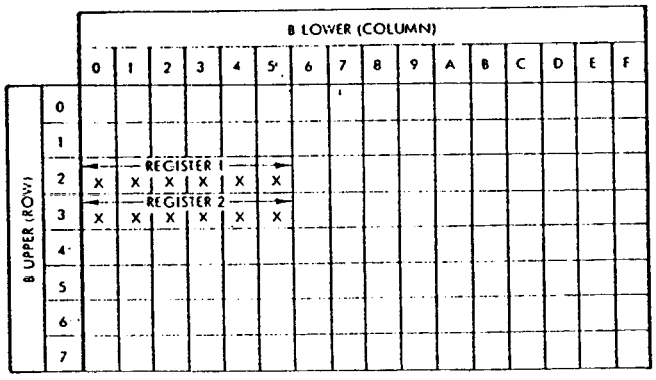
contents of #24 are moved to #23, #23 to #22, #22 to #21 and #21 to #20. Note that when this last operation is performed the B Lower register will decrement from 0 to #F causing the transfer instruction to be skipped and the process terminated.

Suppose that the contents of REGISTER 1 are to be complemented and moved to the register called REGISTER 2 in Row 3. The program to do this follows:

```
ONE     LBL     #25     Point to hex 25
TWO     L       1       Load and point to hex 35
THREE   COM             Complement
FOUR    XDSK    1       Exchange, Point to #24, test
FIVE    T       TWO     Not thru, repeat
```

The Exclusive OR function between 01 from the immediate field of instruction TWO (L 1) and 10 in bits 6 and 5 of the B Register converts the B Register address to 011 0101 (#35) as well as loading the Accumulator. Similarly the 01 in the immediate field of the instruction in location FOUR causes the 11 bits in locations 6 and 5 to be converted to 10 (2) and the B Lower is also decremented and tested in addition to performing the exchange. Consequently, the B Register at the conclusion of this instruction is 010 0100 (#24) which is pointing at the next data to be complemented.

The process is repeated again until the complemented value of memory cell #20 is stored in #30 and then the process automatically terminates because B Lower will decrement from 0 to #F after the exchange.



APPLICABLE TO THE MM77 ONLY

*ADDRESSES #48-#4F AND #58-#5F ADDRESS THE SAME MEMORY CELLS AS ADDRESSES #40-#47

**ADDRESSES #68-#6F AND #78-#7F ADDRESS THE SAME MEMORY CELLS AS ADDRESSES #60-#67

Figure 3. DATA MEMORY MAP FOR PPS-4/1 MM77, MM78

A program to move the data from REGISTER 1 to REGISTER 2 is as follows:

```
        LBL     #25
MOVE    L       1
        XDSK    1
        T       MOVE
```

The same program will move 16 four-bit words if the process is started at #2F instead of #25:

```
        LBL     #2F
MOVE    L       1
        XDSK    1
        T       MOVE
```

The PPS-4/1 is particularly efficient for using subroutines which may operate for different lengths of data registers in memory. For instance if it is desired to use one subroutine with two entry points to either move 6 characters or 16 characters respectively, the following program may be used:

```
        TM      MOVF    subroutine call to
RETN    [NEXT   INSTR]  move 16 characters

MOVF    LBL     #2F
MOV6    LBL     #25
MOVE    L       1
        XDSK    1
        T       MOVE
        RT
```

The PPS-4/1 ignores LBL instructions in a string except for the first one executed. Consequently, for this example, the B Register is loaded with #2F and the LBL #25 is ignored so 16 bytes will be moved. A TM MOV6 instruction would load the B Register with #25 so that 6 characters would be moved. After moving the 16 or 6 characters the T MOVE instruction will be ignored and the RT instruction causes the program counter to return to the next instruction after the TM MOVF or TM MOV6 instruction so that the main program can continue from that point. If more than one subroutine call is used in the program (the usual case for subroutines) the program will always continue with the next instruction after the specific one which called the subroutine when the subroutine has completed its process.

Since the MM77 may address 128 data memory cells and there are actually 96 memory cells, the MM77 has two groups of eight memory cells which have three addresses. The remaining 80 memory cells each have unique

addressing. By this triple addressing technique system designers using the MM77 have the option of considering data memory to be six 16-character rows or four 16-character rows and four 8-character rows or a combination of both. Thus the system designers can use the addressing scheme which optimizes the MM77 to their specific design.

There are three types of unconditional transfer instructions (T, TL, and TLB) and three types of transfer and mark instructions (TM, TML, and TMLB). The ROM Map Table (Table 3) will help explain their usage.

There are 64 program memory bytes on a page. An unconditional transfer to another location on the same page requires a one byte T instruction which contains as part of the instruction the specific location for the next instruction be be executed. If the next instruction is not on the same page and is not in pages 16 through 29, then a two byte instruction TL is used. If the next instruction is in pages 16 through 29, then a TLB instruction is used.

The subroutine call instructions TML and TMLB are similar. However, the TML instruction is used when the first instruction of the subroutine is on any of the general program area pages (even if it is the same page) and TMLB is used to call a subroutine on pages 16 through 29.

The TM instruction operates differently. The TM instruction is one byte long and always transfers to a subroutine on page SR0 of the primitive subroutine area. The primitive subroutine area (SR0 and SR1) is special in that it comprises two 64 byte sections, 31 and 30 respectively. One byte transfers are used to go between the two sections. This area is intended for easy access to primitive subroutines which are often used and do not call other subroutines. Two levels nested subroutines can be accommodated in the hardware Stack Registers, SA and SB.

The subroutine may be self-contained within that area or the subroutine may perform an unconditional transfer to anywhere in memory via a TL or TLB instruction. In this latter case the subroutine may call another subroutine.

The PPS-4/1 conserves ROM by allowing these simplified one byte subroutine calls to be used for the high usage subroutines. This is a unique capability in the PPS family which effectively increases the amount of ROM available for other functions.

A capability provided in the MM77, MM78 versions of the PPS-4/1 is a table look-up instruction designated (TAB). The TAB instruction uses the initial contents of the Accumulator to select one of up to 16 alternatives. The alternatives may be code conversion, program jump tables or combinations of both.

Table 3. ROM MAP

Page No.	Program Memory (ROM) Allocation		
0	64 bytes general program area - Not used MM77	on page transfers (T) – one byte; off page transfers (TL) – two bytes	TML Subroutine area
1	64 bytes general program area		
2	64 bytes general program area		
3	64 bytes general program area		
4	64 bytes general program area		
5	64 bytes general program area		
6	64 bytes general program area		
7	64 bytes general program area		
8	64 bytes general program area - Not used MM77		
9	64 bytes general program area		
10	64 bytes general program area		
11	64 bytes general program area		
12	64 bytes general program area		
13	64 bytes general program area		
14	64 bytes general program area		
15	byte 0 = power on location - remainder general area		
16-24	64 bytes banked program area - Not used MM77	on page transfers (T) – one byte; off page transfers to page in this area (TLB) – three bytes	TMLB Subroutine area
25	64 bytes banked program area		
26	64 bytes banked program area		
27	64 bytes banked program area		
28	64 bytes banked program area		
29	64 bytes banked program area		
31(SR0)	TM address area (1 byte subroutine calls start here and extend to page SR1 (30) or to other sections of memory)		
30(SR1)	Extension of primitive subroutine area from page SR0 (31)		

Note: The development circuit for the PPS-4/1 MM77 (Part No. A7799) can use all 2048 addressable bytes for developing programs. Consequently pages 0, 8 and 16-24 may be used as necessary during the development and the final programs condensed to the addresses shown above for the production program.

A more complete description of programming techniques is in the PPS-4/1 Programming and Applications Manual. Features of the assembly, editing, and emulation capabilities on the PPS Universal Assemulator development hardware are discussed in the PPS-4/1 Operators Manual for Universal Assemulator. An assembly capability for the MM77, MM78 is also available in FORTRAN IV and on the General Electric Information Services system. That assembler is described in the PPS-4/1 Single Circuit Microcomputer Series Programming Manual.

DECIMAL ADDITION

EXAMPLE

To further illustrate the flexibility and efficiency of the PPS-4/1 MM77, MM78 instruction set, a decimal addition subroutine which has multiple entry points will be discussed. These different entry points allow the contents of different memory registers to be added together and the resulting sum left in the designated one of the two registers involved in the addition and also illustrate decimal addition with differing numbers of decimal digits. In the PPS-4/1 system the same subroutine may be used for both types of functions. This decimal add subroutine is as follows:

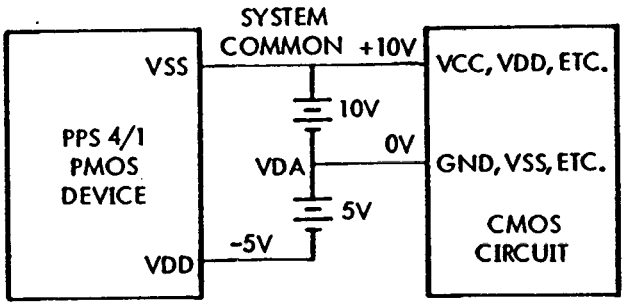
AD10	LB	#09	Entry to Add 10 digit register pair 1*
AD12	LBL	#3B	Entry to Add 12 digit Register Pair 2*
AD5	LBL	#44	Entry to Add 5 digit Register Pair 3*
DADD	RC		Reset carry for initial digit add
LOOP	L	1	Load digit from 1st register and point to 2nd
	DC		Decimal correct (add 6)
	ACSK		Add digit from 2nd register, skip if carry is generated
	AISK	10	Recorrect if no carry (add 10 with no carry — skip if a carry from prior instruction
	XDSK	1	Store answer digit, point to next digit in first register, skip if BL = 15
	T LOOP		Repeat until last digit added
	RT		Through so return from subroutine to next location after subroutine call

*Register pair 1 adds Register #00-#09 to #10-#19 and puts answer in #10-#19.
Register pair 2 adds Register #30-#3B to #20-#2B and puts answer in #20-#2B.
Register pair 3 adds Register #40-#44 to #50-#54 and puts answer in #50-#54.
DADD is a general subroutine entry which may be used to add from 1 to 16 decimal digits in rows 0 to 1, 1 to 0, 2 to 3 and 3 to 2, or from 1 to 8 decimal digits in rows 4 to 5, 5 to 4, 6 to 7 or 7 to 6. The specific registers and the number of decimal digits to be added are dependent upon the initial value in the B Register.

ELECTRICAL INTERFACE

This section and Table 4 define the electrical specifications.

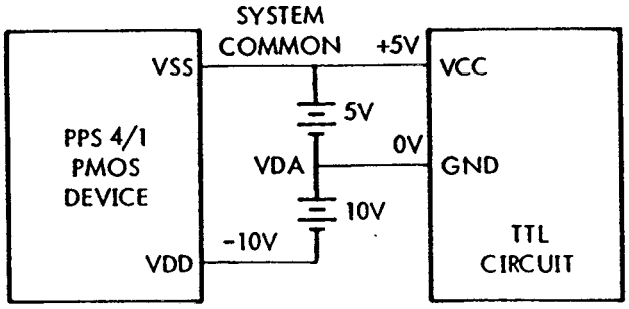
The power supply for the PPS-4/1 microcomputer requires a 15 volts ±5% supply. This may be obtained by a single 15 volt or +10, 0, -5 volt supply when the input/output system is interfacing with CMOS as shown in Figure 4 or may be obtained from +5, 0, -10 volt supply when interfacing with TTL circuits as shown in Figure 5.



NOTE: The PPS-4/1 VSS must be connected to most positive CMOS terminal.

The PPS-4/1 requires a 15 volt supply. CMOS operates with an 8V to 15V input. (If CMOS is only receiving PMOS inputs, the input can range from 3V to 15V.)

Figure 4. TYPICAL PMOS TO CMOS POWER INTERFACE



NOTE: The PPS-4/1 requires a 15 volt supply. TTL uses a 5 volt supply.

Figure 5. TYPICAL PMOS TO TTL POWER INTERFACE

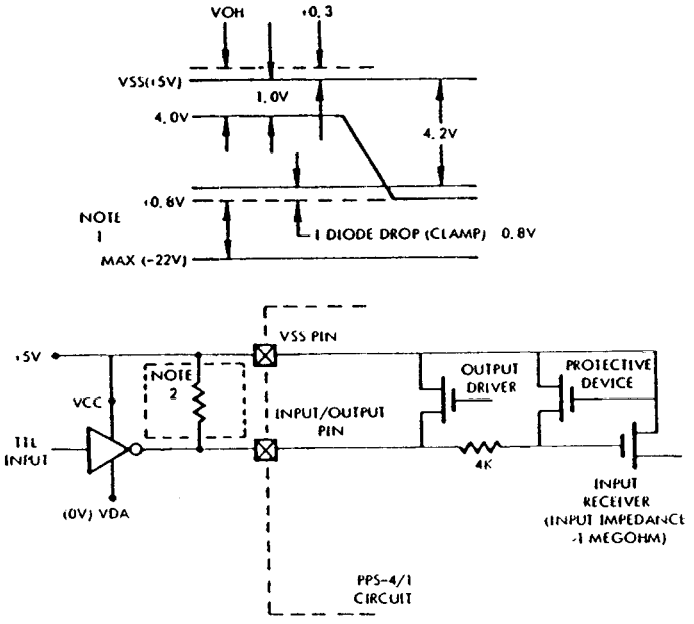
DISCRETE I/O PORTS

The ten discrete I/O ports (DI/O 0 thru DI/O 9) are selected by setting bit 7 of the B Register to zero and B Lower to the appropriate value (i.e., #01, #11, #21, or #31 will select DI/O 1). Issuing a set output selected (SOS) instruction will connect the output port to VSS through 500 ohms maximum. Issuing a reset output selected (ROS) instruction will cause the output to float, allowing

an external resistance to pull the output to a -V level. The output will be stable by Ø2 of the following instruction. Minimum impedance is reached after Ø4. The output circuit capable of sinking 3 ma maximum when all circuits are in use. To use as an input, the port must be selected by BL and the Skip on Input Selected Low instruction issued. A skip will be produced if the input is more negative, relative to VSS, than -4.2 volts. The inputs are fully synchronized so that an asynchronous input signal may be used. The sampling occurs during phase 3 (see Figure 9). The technique for interfacing with TTL logic is shown in Figures 6 and 7.

PARALLEL I/O PORTS (RIO1-RIO4)

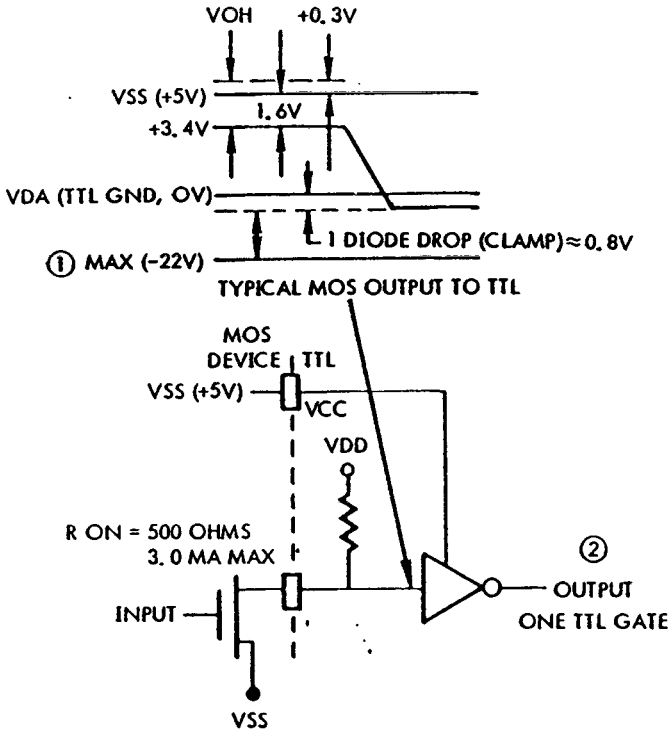
The data in the parallel input/output ports RIO1 through RIO4 will be exchanged with the Accumulator upon issuing an Input/Output A (IOA) command. When used as an output a "1" in any bit position in the Accumulator will cause the corresponding output bit to float, while a "0" in the Accumulator will cause the output to be connected to VSS through 500 ohms maximum. The outputs will be stable by the following Ø2 time and the impedance to VSS when the output is in the high state will be less than 500 ohms after Ø4. The outputs are buffered through a register such that any state will be held until another exchange is executed. The output drivers will sink 3 milli-amperes when all circuits are sinking current.



NOTES:

1. Maximum voltage which may be applied to any input/output pin is -30 volts relative to VSS.
2. Only an Open Collector Driver requires the Pull-Up Resistor.

Figure 6. TTL TO PPS-4/1 SYNCHRONIZED INPUT RECEIVER INTERFACE



NOTES:

1. Maximum voltage which may be applied to any input/output pin is -30V relative to VSS.
2. SOS command causes gate output to be low. "1" in A or X causes the gate output to be high.

Figure 7. PPS-4/1 OUTPUT DRIVER TO TTL INTERFACE

In order to use any bit position as an input, the corresponding bit of the output buffer must be loaded with a "1" before the exchange is performed so that the output driver will be floated and may be set high or low by the external signal to be input. By outputting zeros on any of the bit positions prior to interpreting an input the bits input from those positions will automatically be masked so that independent of their state, zeros will be input. The inputs are fully synchronized (sampled at Ø3 time) and will recognize a voltage more negative than -4.2 volts (related to VSS) as a "1" and a voltage between +0.3 and -1.5 as a "0". The outputs will be initialized to the float state with power on.

PARALLEL I/O PORTS (RIO5-RIO8)

The parallel input/output ports RIO5 through RIO8 work through the X Register by means of two commands. The output X (OX) command will cause the X Register to be copied into the output X Buffer Register and held after Ø2 of the next instruction until another load instruction is executed. A "1" in the X Buffer will cause the output port to float. (An alternate version of the IOP instruction, output X and A (OXA) is available as a mask option. This alternate instruction causes a simultaneous execution of an IOA and an OX instruction to occur so that 8 bits may be output with a single command.)

Table 4. MM77, MM78 ELECTRICAL SPECIFICATIONS

OPERATING CHARACTERISTICS

Supply Voltage:
VDD = 15 Volts ±5%
(Logic "1" = most negative voltage V_{IL} and V_{OL}.)

VSS = 0 Volts (Gnd.)
(Logic "0" = most positive voltage V_{IH} and V_{OH}.)

System Operating Frequencies:
80 kHz ±50% with external resistor

Device Power Consumption:
75 mw, typical

Input Capacitance:
<5 pf

Input Leakage:
<10 μa

Open Drain Driver Leakage (R OFF):
< 10 μa at -30 Volts

Operating Ambient Temperature (TA):
0°C to 70°C (TA = 25°C unless otherwise specified)

Storage Temperature:
-55°C to 120°C

ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 volts.

Maximum positive voltage on any pin +0.3 volts.

Function	Symbol	Limits (VSS = 0) Min	Typ	Max	Limits (VSS = +5V) Min	Typ	Max	Timing (Sample/ Good)	Test Conditions
Supply Current (Average) for VDD	IDD		5 ma	8 ma		5 ma	8 ma		VDD = -15.75V T = 25°C
Discrete I/O's DI/O0-DI/O9	VIH	-1.0V			+4.0V			Ø3 & Ø4	
	VIL			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	Ø2*	3.0 ma max.
Channel 1 Input PI1-PI4	VIH	-1.5V			+3.5V			Ø1	
	VIL			-4.2V			+0.8V		
Channel 2 Input PI5-PI8	VIH	-1.5V			+3.5V			Ø3	
	VIL			-4.2V			+0.8V		
I/O Channel A RI/O1-RI/O4	VIH	-1.5V			+3.5V			Ø3	
	VIL			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	Ø2*	3.0 ma max.
I/O Channel X RI/O5-RI/O8	VIH	-1.0V			+4.0V			Not sync. Must be stable at Ø1 and 2.	
	VIL			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	Ø2*	3.0 ma max.
DATAI	VIH	-1.0V			+4.0V			Ø4	
	VIL			-4.2V			+0.8V		
DATAO	RON							Ø4**	
INT0	VIH	-1.5V			+3.5V			Ø3	
	VIL			-4.2V			+0.8V		
INT1	VIH	-1.5V			+3.5V			Ø1	
	VIL			-4.2V			+0.8V		
Clock A, BP, ($\overline{B}$)	VOH	-1.0V			+4.0V				CL = 50 pf (max)
	VOL			-10.0V			-5.0V		
EXCLK	VIH	-1.5V			+3.5V			STRAP	F max = 80 kHz
	VIL			-7.0V			-2.0V		
CLK IN	VIH	-1.0V			+4.0V				
	VIL			-10.0V			-5.0V		
Shift Clock Clock	VIH	-1.0V			+4.0V			Ø3 & Ø4	
	VIL			-4.2V			+0.8V		
	RON			500 ohms			500 ohms	Ø4**	2.0 ma max.
VC***	VIH								56K ±5%
	VIL								
PO	VIH	-2.0V			+3.0V				Special circuit
	VIL			-6.0V			-1.0V		

*State established by Ø2 (minimum impedance after Ø4).
**Same as above except Ø4 minimum at Ø2 of next cycle.
***Connect VC to VDD through a resistor: 56KΩ for 80 kHz or 47KΩ for 100 kHz.

The Input X (IX) command will cause the state of the port to be copied into the X Register. These inputs are not synchronized so that they must be used for straps, signals which cannot change at the time sampling occurs, or signals which have been externally synchronized. Any change in state of the external signals must occur during phase 3 or 4 so that the input is stable during phases 1 and 2. An input signal more negative than -4.2 volts will be a logic 1 and +0.5 to -1.0 volts will be a logic 0.

PARALLEL INPUT PORTS (PI1-PI4)

The parallel input ports PI1 through PI4 will be added to the contents of the Accumulator upon execution of an I1SK instruction and the next instruction will be skipped if no carry is generated. The inputs are fully synchronized during phase 1 and are TTL compatible. An input signal more negative than -4.2 volts will be a logic 1 and a "0" range is from +0.3 to -1.5 volts.

PARALLEL INPUT PORTS (PI5-PI8)

The inverted state of the parallel inputs PI5 through PI8 will be copied into the Accumulator upon receipt of an I2C instruction. The inputs are synchornized during phase 3 and are TTL compatible.

CONDITIONAL INTERRUPTS (INT0 AND INT1)

The conditional interrupt ports may be utilized in two different ways. The first way is that the input logic level can be tested directly by means of the conditional interrupt 0 or conditional interrupt 1 instructions, INT0H or INT1L. A skip will be produced when the INT0 signal is at V_{SS} and when the INT1 signal is at -V.

The second way of using the conditional interrupt capability is to test the state of a flip-flop associated with each input in a manner similar to the discrete I/O ports. The flip-flops are selected by BL (BL = decimal 11 for INT0 and decimal 10 for INT1) and may be set or reset by the discrete I/O instructions (SOS or ROS). If the flip-flop for INT0 is placed in the set state and a transition occurs on the input from the -V state to the V_{SS} state for one bit time or more, the flip-flop will be reset. Consequently, the signal to activate a conditional interrupt need only be a pulse, as long as it is at least one clock period long. The state of the flip-flop may then be tested and will indicate that a -V to V_{SS} level pulse did occur even though the V_{SS} level has gone away.

The INT1 signal performs in the same manner except that a transition from a V_{SS} level to a -V level for one bit time will cause the flip-flop to be reset. (The development circuit is supplied as described above.)

However, in production circuits there are options available to make both inputs reset when either positive pulses (-V to V_{SS} to -V) or negative pulses (V_{SS} to -V to V_{SS}) occur by means of mask changes. An additional feature which may be included as a mask option will cause the pulse transition on the INT1 port to reset the flip-flop associated with DI/O0 and thus cause the discrete output to float so that an automatic echo signal may be provided. The inputs are sampled at phase 1 for INT1 and phase 3 for INT0 and are TTL level compatible as shown in Figure 6.

SERIAL I/O

A register is built into the circuit which may be used as a serial IN/OUT buffer and may also be used for parallel exchange with the Accumulator. Data to be output is loaded into the Accumulator and transferred to the Serial Register by the Exchange A and S (XAS) command. The serial I/O (IOS) command causes the data to be shifted out along with a clock for clocking external devices. Each bit of data is presented at the output for two bit times and the clock will make the negative to positive transition in the middle of this time so as to be compatible with CMOS clocking requirements. Data may be input at the same time and then transferred to the Accumulator.

The data and clock outputs are 500 ohm maximum open ended devices capable of sinking 3 milli-amperes maximum and are TTL compatible as shown in Figure 7. The serial input is sampled during phase 4 and TTL compatible as shown in Figure 6.

Data may also be shifted into or out of the S Register under external shift clock control. A shift clock signal may be applied to the CLOCK signal line to cause the internal S Register to shift and perform a serial input/output function at the PPS-4/1 clock rate. If shift rates lower than this are desired, the shifting must be done in synchronism with the A clock signal for the particular shift pulse. The shift clock input is sampled at $\phi 4$ time and is TTL compatible as shown in Figure 6.

The basic timing for the serial input/output capability is shown in Figure 8.

The pin connections for the MM77, MM78 microcomputers are summarized in Table 5. The pin connections for the A7799 and A7899 personality module development circuits are shown in Table 6. The pin connections for the A7798 and A7898 development circuits, used for customer prototyping with external memory, are shown in Table 7. The basic timing for the PPS-4/1 is summarized in Figure 9.

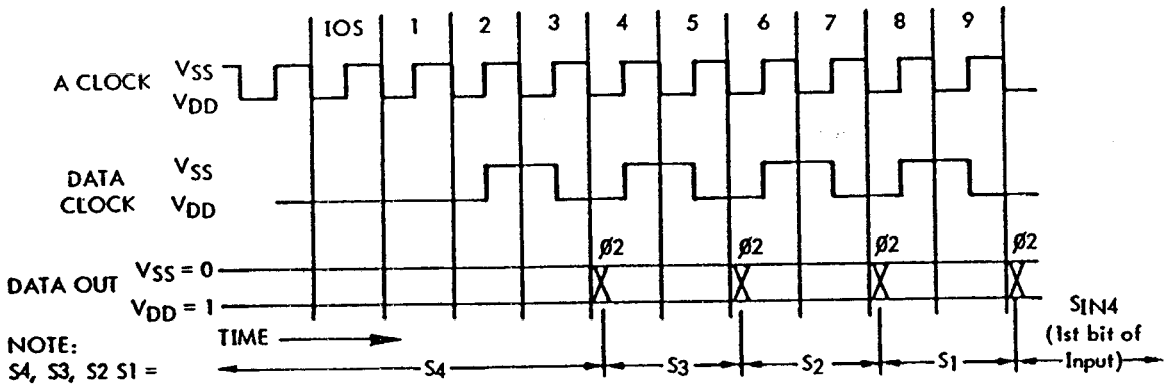


Figure 8a. INTERNALLY CONTROLLED SERIAL INPUT/OUTPUT

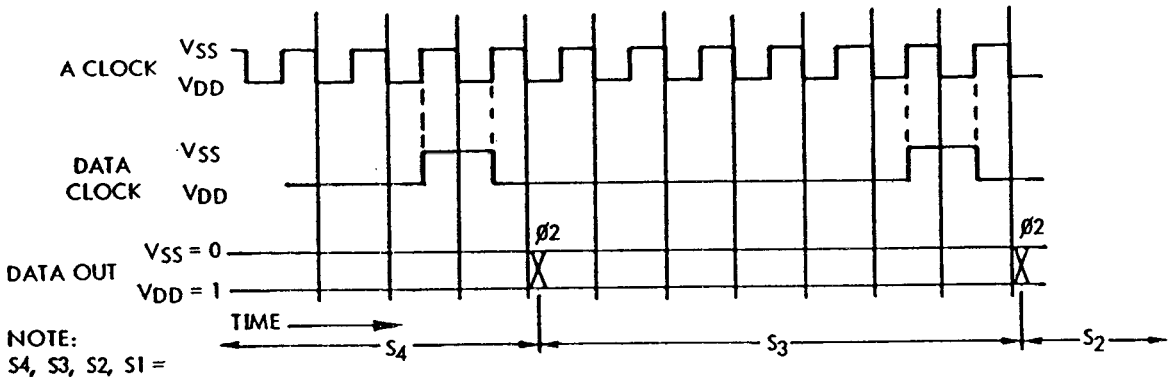


Figure 8b. EXTERNALLY CONTROLLED SERIAL INPUT/OUTPUT WITH DATA CLOCK SYNCHRONIZED WITH A CLOCK SIGNAL

Figure 8. TIMING OF SERIAL INPUT/OUTPUT

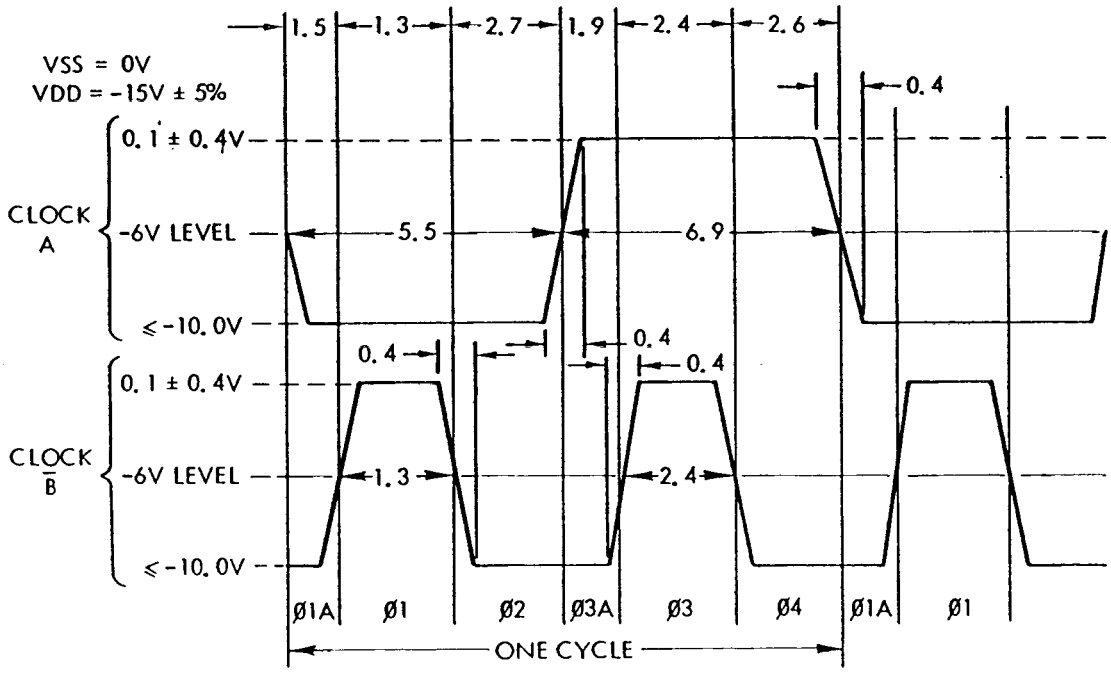


Figure 9. TYPICAL CLOCK WAVEFORMS WITH EXTERNAL 56K OHM RESISTOR

Table 5. PPS-4/1 MM77, MM78 SIGNALS (Part No. A77XX and A78XX)

Pin No.	Signal Name	Function
1	BP	B Prime System Clock
2	A	A System Clock
3	CLKIN	External Clock square wave input (VSS when not used)
4	EXCLK	External Clock selection (VDD = External VSS = Internal)
5	VC	Resistor frequency control R to VDD
6	VDD	-15 Volt Supply (1st pin)
7	VSS	VSS Positive Power Supply Terminal
8	-	
9	TEST	Commands Test Mode (VSS normal operation)
10	PI4	Channel 1 bit 4
11	PI8	Channel 2 most significant bit (4)
12	PI3	Channel 1 bit 3
13	PI7	Channel 2 bit 3
14	PI6	Channel 2 bit 2
15	PI2	Channel 1 bit 2
16	PI5	Channel 2 bit 1
17	VDD	-15 Volt Supply (2nd pin)
18	PI1	Channel 1 bit 1
19	PO	Power On reset input
20	RIO5	X I/O Channel Least Significant Bit (1)
21	RIO6	X I/O Channel bit 2
22	RIO7	X I/O Channel bit 3
23	RIO8	X I/O Channel bit 4
24	RIO1	A I/O Channel bit 1
25	RIO2	A I/O Channel bit 2
26	RIO3	A I/O Channel bit 3
27	RIO4	A I/O Channel bit 4
28	CLOCK	Shift Clock Output or Input (VDD if serial register not used)
29	DATAO	Serial Output signal
30	DATAI	Serial Input signal
31	INT0	Interrupt 0 input
32	INT1	Interrupt 1 input
33	DI/O0	Discrete I/O line 0
34	DI/O1	Discrete I/O line 1
35	DI/O2	Discrete I/O line 2
36	DI/O3	Discrete I/O line 3
37	DI/O4	Discrete I/O line 4
38	DI/O5	Discrete I/O line 5
39	DI/O6	Discrete I/O line 6
40	DI/O7	Discrete I/O line 7
41	DI/O8	Discrete I/O line 8
42	DI/O9	Discrete I/O line 9

Table 6. PPS-4/1 MM77, MM78 PERSONALITY MODULE DEVELOPMENT CIRCUIT SIGNALS
(Part No. A7799 and A7899)

Pin No.	Signal Name	Function	Pin No.	Signal Name	Function
1	—		33	(P5B3)	PC bit 5, BL bit 3
2	RIO6	Same as A77XX	34	(P4B2)	PC bit 4, BL bit 2
3	RIO7	Same as A77XX	35	(P3B1)	PC bit 3, BL bit 1
4	RIO8	Same as A77XX	36	CLKIN	Same as A77XX
5	RIO1	Same as A77XX	37	EXCLK	Same as A77XX
6	RIO2	Same as A77XX	38	(I8)	Instruction bit 8
7	—		39	(I7)	Instruction bit 7
8	RIO3	Same as A77XX	40	—	
9	RIO4	Same as A77XX	41	VC	Same as A77XX
10	CLOCK	Same as A77XX	42	VDD	Same as A77XX
11	DATAO	Same as A77XX	43	(P11B7)	PC bit 11, BU bit 7
12	DATAI	Same as A77XX	44	(P8I4)	PC bit 8, Inst bit 4
13	(P2I2)	PC bit 2, Inst bit 2	45	(P9I6)	PC bit 9, Inst bit 6
14	(P6B4)	PC bit 6, BL bit 4	46	(P10I5)	PC bit 10, Inst bit 5
15	INT0	Same as A77XX	47	(P7I3)	PC bit 7, Inst bit 3
16	INT1	Same as A77XX	48	TEST	Same as A77XX
17	DI/O 0	Same as A77XX	49	PI4	Same as A77XX
18	DI/O 1	Same as A77XX	50	PI8	Same as A77XX
19	DI/O 2	Same as A77XX	51	PI3	Same as A77XX
20	DI/O 3	Same as A77XX	52	PI7	Same as A77XX
21	DI/O 4	Same as A77XX	53	PI6	Same as A77XX
22	DI/O 5	Same as A77XX	54	PI2	Same as A77XX
23	—		55	PI5	Same as A77XX
24	(P1I1)	PC bit 1, Inst bit 1	56	PI1	Same as A77XX
25	—		57	PO	Same as A77XX
26	DI/O 6	Same as A77XX	58	(B5)	BU bit 5
27	DI/O 7	Same as A77XX	59	(B6)	BU bit 6
28	VSS	Same as A77XX	60	(SKIP)	Skip indicator
29	DI/O 8	Same as A77XX	61	—	
30	DI/O 9	Same as A77XX	62	—	
31	BP	Same as A77XX	63	—	
32	A	Same as A77XX	64	RI/O 5	Same as A77XX

PC outputs during phase 2 in complement form. (0 = -V, 1 = VSS)
B outputs during phase 4 in complement form. (0 = -V, 1 = VSS)
Inst inputs at end of phase 4 in true form. (0 = VSS, 1 = -V)
Skip output is -V during Ø4 if next instruction is to be skipped.

Table 7. PPS-4/1 MM77, MM78 DEVELOPMENT CIRCUIT SIGNALS
(Part No. A7798, and A7898)

Pin No.	Signal Name	Function	Pin No.	Signal Name	Function
1	DI/O1	Same as A77XX	27	PI4	Same as A77XX
2	DI/O2	Same as A77XX	28	PI8	Same as A77XX
3	DI/O3	Same as A77XX	29	PI3	Same as A77XX
4	DI/O4	Same as A77XX	30	PI7	Same as A77XX
5	(P1I1)	PC bit 1, Inst bit 1	31	PI6	Same as A77XX
6	DI/O5	Same as A77XX	32	PI2	Same as A77XX
7	DI/O6	Same as A77XX	33	PI5	Same as A77XX
8	DI/O7	Same as A77XX	34	PI1	Same as A77XX
9	DI/O8	Same as A77XX	35	PO	Same as A77XX
10	DI/O9	Same as A77XX	36	(P6B4)	PC bit 6, BL bit 4
11	BP	Same as A77XX	37	(P2I2)	PC bit 2, Inst bit 2
12	A	Same as A77XX	38	VSS	Same as A77XX
13	(P5B3)	PC bit 5, BL bit 3	39	RIO5	Same as A77XX
14	(P4B2)	PC bit 4, BL bit 2	40	RIO6	Same as A77XX
15	(P3B1)	PC bit 3, BL bit 1	41	RIO7	Same as A77XX
16	CLKIN	Same as A77XX	42	RIO8	Same as A77XX
17	EXCLK	Same as A77XX	43	RIO1	Same as A77XX
18	(I8)	Inst bit 8	44	RIO2	Same as A77XX
19	(I7)	Inst bit 7	45	RIO3	Same as A77XX
20	VC	Same as A77XX	46	RIO4	Same as A77XX
21	VDD	Same as A77XX	47	CLOCK	Same as A77XX
22	(P11B7)	PC bit 11, BU bit 7	48	DATAO	Same as A77XX
23	(P8I4)	PC bit 8, Inst bit 4	49	DATAI	Same as A77XX
24	(P9I6)	PC bit 9, Inst bit 6	50	INT0	Same as A77XX
25	(P10I5)	PC bit 10, Inst bit 5	51	INT1	Same as A77XX
26	(P7I3)	PC bit 7, Inst bit 3	52	DI/O0	Same as A77XX

PC outputs during phase 2 in complement form. (0 = -V, 1 = VSS)
B outputs during phase 4 in complement form. (0 = -V, 1 = VSS)
Inst inputs at end of phase 4 in true form. (0 = VSS, 1 = -V)

IASK OPTIONS

'ell offers several mask options for the MM77 series ...crocomputers. These options are selected by the ustomer at ROM order time, and may be used to simplify particular application

NOTE

The mask options are not incorporated into the MM77 development circuits, so customers requiring these options in their production devices may wish to simulate them during development with either external circuitry or program modifications.

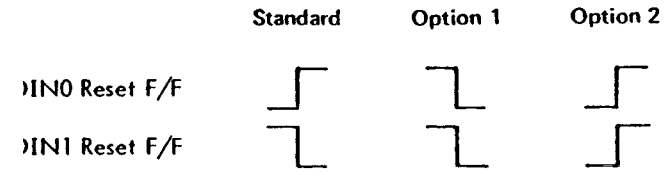
KIP OPTIONS

hese options effect skip instructions DIN0 and DIN1. ı the development circuits, these instructions perform as ollows:

- DIN0 — The flip-flop associated with DIN0 will be reset with a positive-going pulse at the input. Upon testing, the skip will occur if the flip-flop is reset.

  DIN1 — Same as DIN0, except that the flip-flop is reset with a negative-going pulse at the input.

Aask options are available which will invert these inputs s shown below.



he skip on level test is unaffected by these options.

:CHO BACK OPTION

n the standard devices, the DIO0 flip-flop is independent ıf the DIN1 input and the DIN1 flip-flop. The Echo Back ıption causes the DIO0 flip-flop to be reset when the lip-flop associated with DIN1 is reset if both flip-flops ıave been set by the program. A transition on the DIN1 nput causes the reset of the DIN1 flip-flop.

3-BIT PARALLEL OPTION

e standard devices the contents of the accumulator are exchanged with RIO1 through RIO4 upon execution of the IOA instruction. The contents of the X Register are output on RIO5 through RIO8 by a separate instruction, OX. An option is available which causes both of these operations to occur upon execution of the IOA instruction. In this case, the Output X instruction (OX) has no effect. The Input X instruction (IX) remains unaltered.

Instruction	Standard	8-Bit Option
IOA	A—RIO1-4	A—RIO1-4 X—RIO5-8
OX	X—RIO5-8	---

SYSTEM DEVELOPMENT AIDS

ASSEMULATOR

A sophisticated Universal Assemulator (assembler and emulator unit)is available for PPS-4/1 systems development. A personality module which is compatible with all members of the PPS-4/1 family connects the Universal Assemulator to a functioning PPS-4/1 microcomputer with very flexible development aids. This unit converts a program written in an easy to use assembler language to the machine language code which is interpreted by a special evaluation version of the PPS-4/1 circuit. The Assemulator also has flexible editing capabilities for modifying the assembly language program and sophisticated debugging capabilities for aiding in checking out the computer program and integrating the microcomputer into the final system configuration.

XPO-1

The XPO-1 is a complete microprocessor system with keyboard and display on a single printed circuit board. XPO-1 is an effective system development tool for the PPS-4/1 microcomputers. XPO-1 provides a cost effective method of familiarizing personnel with the operation, programming, and capabilities of the PPS-4/1 microcomputers. It can be used to develop and debug the software program including assembly, and it can then be used to exercise the program in real-time in prototype equipment.

DEVELOPMENT CIRCUIT AND EVALUATION MODULES

The special development versions of the PPS-4/1 MM77, MM78 circuits are identical to the production version of the MM77, MM78 microcomputers except that there is no read only memory. In place of the read only memory area on the circuit chip, address and memory output bonding points are provided so that leads are brought out to an external memory interface. This allows the program for the PPS-4/1 development circuit to be stored in an external PROM or RAM memory. The external memory may be as large as 2048 bytes. Consequently, the program may be loaded, debugged and modified as necessary to perform the

desired functions for each specific system application until a final program for that application is satisfactory. The program may then be formed in ROM on the production circuit.

The development PPS-4/1 A7798 or A7898 circuit is available on a module for development and evaluation which may be incorporated directly into the user's equipment for demonstration, product evaluation etc.

SOFTWARE AND TRAINING

Other system support will include application and programming services software packages and training programs to facilitate easy introduction of the PPS-4/1 microcomputer into the user's system. PPS-4/1 programs may be assembled using FORTRAN IV. The FORTRAN IV program is also available on the General Electric Information Services timesharing system.

THE ULTIMATE LOWEST COST SYSTEM

Rockwell is the microcomputer company which has a full spectrum of microcomputer capabilities ranging from custom circuits at one end of the spectrum to the extremely flexible, almost minicomputer capability of the PPS-8 system. Rockwell is the microcomputer company which has the broad spectrum and the applications staff to assist its customers in obtaining the lowest cost total system to do each specific total system requirements. Rockwell makes use of sophisticated microcomputer architecture using the lowest cost technology so that whatever the complexity of the application, a specific Rockwell system will always be the lowest cost.

THE PPS-4/1 APPLICATION AREAS

The PPS-4/1 family of single circuit microcomputers fits the spectrum of microcomputer application requirements by forming a bridge between the custom circuits at one end of its application area and the PPS-4/2 family of circuits at the other end. The PPS-4/1 family fills in an application niche between the more sophisticated microcomputer families and the less costly custom circuits specifically tailored to specific applications.

The PPS-4/1 allows new low cost products to be conceived, developed, and put into production in moderate quantities. Thereby it meets a specific need in the marketplace for low cost, readily tailorable controller systems.

The PPS-4/1 also provides an opportunity for low cost market evaluation of products which may have a potential of very large production quantities. In these cases, the PPS-4/1 provides a low cost stepping stone to establish demand prior to initiating a custom design for a still more lower cost production custom circuit. The system cost is minimized because the custom circuit can strip away any uneeded capabilities in the PPS-4/1 system to provide the lowest cost most competitive ultimate product and may also have the input output modified to incorporate some of the external hardware in the production version. The final production system development cost is also reduced because the final custom microcomputer can still make use of all of the software developed on the trial production unit.

The PPS-4/1 also provides a capability for a low cost version of a product which may be available in systems having more features and more flexibility when implemented in the larger scale PPS-4/2 or PPS-4 families.

POTENTIAL APPLICATIONS

The PPS-4/1 microcomputer family is designed to facilitate integration with a variety of different kinds of systems ranging from general purpose monitoring and control functions through peripheral equipment controller and multi PPS-4/1 microcomputer systems.

The specific selection of which member of the PPS-4/1 microcomputer family may be used for any specific application is a function of the computational complexity for the specific application. The input/output capabilities of all of the current members of the family are basically identical so that the differences in special features and the software to perform the associated functions are the determining factors. For this reason, the applications defined in the following examples are unspecific as to which member of the PPS-4/1 family should be used. A few of these applications are discussed in this section.

GENERAL PURPOSE MONITOR/CONTROLLER

A block diagram of the general purpose monitor/controller is shown in Figure 10. This controller makes use of the extensive input and output capabilities of the PPS-4/1 microcomputer circuit and illustrates a possible hierarchy in the assignments of primary and secondary control functions and primary and secondary status inputs.

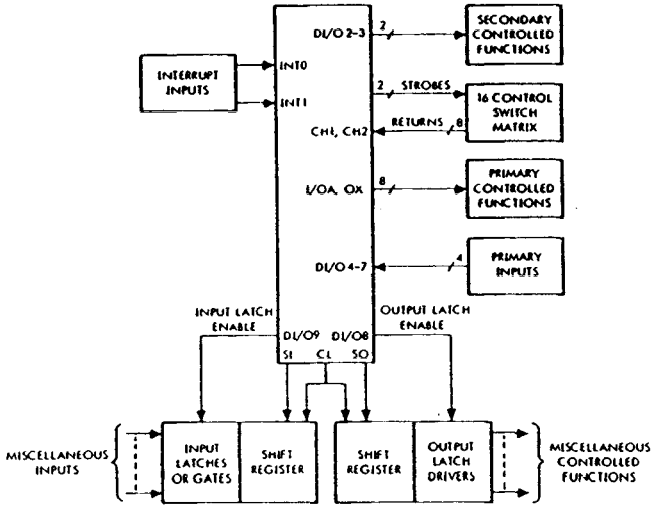


Figure 10. PPS-4/1 GENERAL PURPOSE MONITOR/CONTROLLER

ut Examples

nals labeled interrupt inputs are the highest y inputs and these could be used in control systems ere virtually immediate action is called for by the crocomputer.

e next level of inputs are the primary inputs that in this mple have been assigned to discrete I/O lines of 4 ough 7. These would be inputs that require a response m the system but perhaps not as quick a response as the errupt inputs would.

16 control switch matrix such as the one shown in the ock diagram could be used to detect momentary switch ntacts, limit switches, etc. where not more than one ntact would be closed at a time.

e last type of input is illustrated in the general purpose nitor/controller as miscellaneous inputs that feed in ough input latches which are enabled from one of the screte output lines to a serial shift register which is ifted in to be processed on demand.

utput Examples

the example general purpose monitor/controller, the imary control functions are obtained from the buffered tput from the X Register and the Accumulator, and the condary control functions are output from discrete input/ lines (in this particular example, lines 2 and 3).

more control functions are required, a serial shift gister which is loaded from the serial output from the PS-4/1 may be used. A discrete I/O line is used to ansfer the contents from the serial to the parallel ternal register latches so that they may be held ationary until it is time to change the control functions some way.

Of course, in a real system application with differing ratios f input to output requirements, the input and output nctions of the discrete input/output lines could be ompletely reassigned. An indefinite number of iscellaneous inputs and miscellaneous outputs may be btained by adding external parallel-to-serial or serial-to-arallel shift registers as required to get the desired umber of input or output parameter signals.

MICROWAVE OVEN CONTROLLER

A microwave oven controller example of a PPS-4/1 nicrocomputer application is illustrated in Figure 11. In his case, one interrupt line is used to provide real time clock inputs so that cooking time may be accurately neasured. The other interrupt is used as an interlock input o that if the microwave oven door is opened a signal is ided to the controller which indicates that cooking is ot proceeding. Opening the door will automatically cut off power to the oven without action from the micro-computer; consequently a time out situation exists. Since the real time, 50 or 60 cycles input frequency has a possibility of two values, the discrete input/output line zero identifies to the controller which frequency is actually being applied. For instance, if the oven is being shipped to a country that has 50-cycle power, the selector line could be set to VSS and if it is being sold in a country which has 60-cycle power, the input line could be set to the VDD voltage.

In this controller it is assumed that input parameters are entered by means of a 28-key keyboard. These parameters include: (1) time settings, (2) indications of the type of food being cooked so that cooking rate can be established, (3) whether or not the food placed in the oven is frozen, (4) the desired degree of doneness, etc.

In this example, it is assumed that time information and perhaps other status information is to be displayed in a 6 digit, seven segment decimal display and status indication in 8 status indicator lights. The strobe lines for the key matrix, the 6-digit display and the indicator lights are obtained from one set of seven discrete output lines (DI/O 1-7). The four-bit parallel input to channel one is used for the return lines from the key matrix.

The buffered outputs from the Accumulator and the X Register are used as segment drivers for the digit and indicator light sections and also are used as an input to an 8-bit latch circuit which is enabled by the discrete input/output 8 line to provide control signals to the magnitron, browner, light, fan, stirrer and audible alarm devices.

In this specific example, no requirements are specifically identified for the use of the serial input/output capability; however, if there is a requirement for further controls or if the timing function which is available in the circuit is used to control other devices such as a conventional oven or surface cooking units, the shift register outputs may be used as desired.

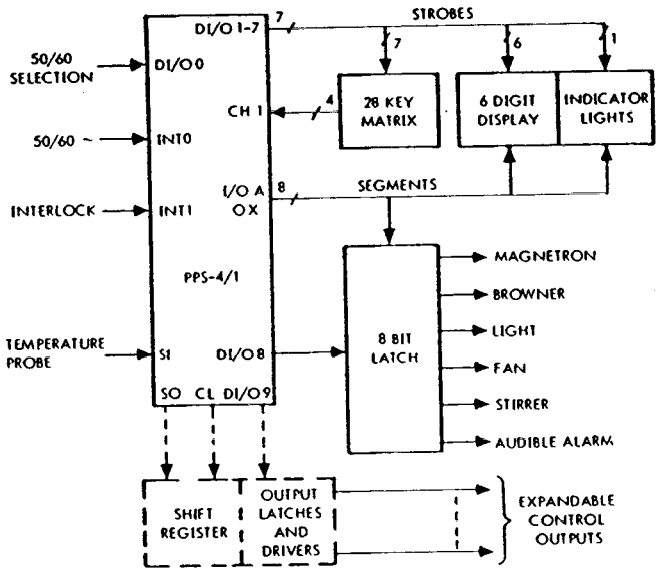


Figure 11. PPS-4/1 MICROWAVE OVEN CONTROLLER

MATRIX PRINTER CONTROLLER

The next potential application shows the use of a PPS-4/1 microcomputer coupled to an external read only memory for character generation for a matrix printer. This is illustrated in Figure 12.

In this case 8-bit data comes to the PPS-4/1 controller over the channel 1 and channel 2 input ports and any necessary handshaking is accomplished through the discrete input/output lines signifying that the printer is ready or that the data is available to be input to the printer controller system.

Control lines to the printer come from discrete input/output lines 5 through 9 and the status and timing information comes back from the printer over the interrupt 0 and interrupt 1 lines. The 8 lines out from the buffered Accumulator and X Register outputs are used to supply a character code to the external ROM and discrete input/output lines zero through 2 are used to identify the vertical column through the character that is to be output to control the matrix solenoid drivers directly from the character generator ROM.

This same general technique could be used any time that there is some type of code conversion and, when, necessary, the output from the read only memory could be loaded back into the PPS-4/1 through the serial input port.

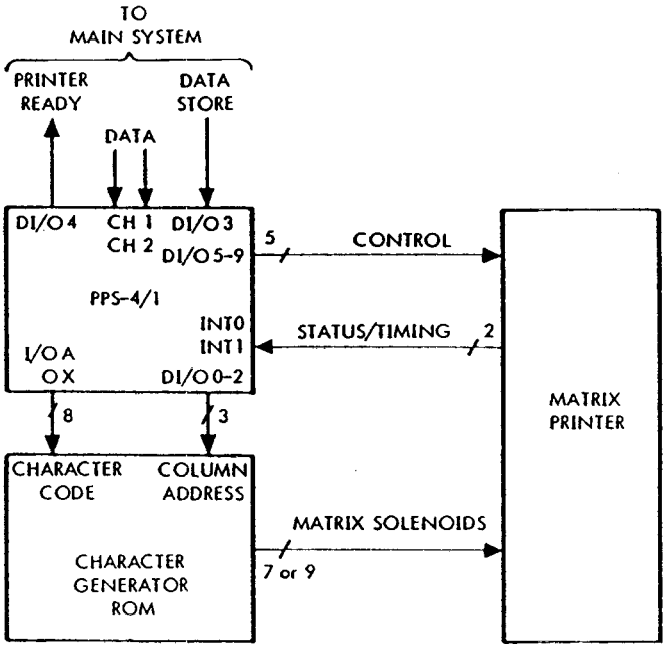


Figure 12. PPS-4/1 MATRIX PRINTER CONTROLLER

COPIER CONTROLLER

Figure 13 shows another potential application of a PPS-4/1 microcomputer circuit as the primary control element in a copier. Functionally, this block diagram resembles that of the microwave oven controller (Figure 11). The major differences are the use of an external clock, the number of keys in the keyboard, and the number of seven segment displays and status lamps. Of course, the controller program and the significance of each of the input/output lines is tailored specifically to the copier control functions.

In this system, the discrete input/output lines 0 through 5 are used as strobe lines to a 24-key keyboard and four displays and as many as 16 status lamps. The four return lines from the keyboard return to the channel 1 input and the outputs from both the Accumulator and the X Register are used for selection of the segment and the status lines. These two buffered outputs also provide the input to an 8-bit latch circuit when enabled by the discrete input/output line 6 signal. Preliminary status inputs come in through channel 2 and the primary control functions are output from the 8-bit latch circuit. Another input comes in through discrete input/output line 8 and the motor on/off control is a discrete output from discrete input/output 7. An interrupt line is used as an interlock that will inhibit operation of the system when a cabinet door is opened.

This example illustrates the use of an external square wave oscillator to provide clock signals to the controller so that instruction operation time is precisely controlled. Internal timing functions may be accomplished to a precision equivalent to the precise clock cycle time by counting instruction cycles and adjusting appropriate internal counters as required.

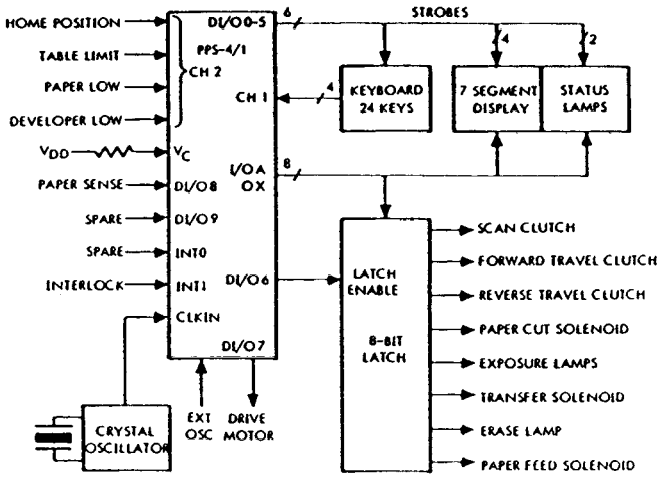


Figure 13. PPS-4/1 COPIER CONTROLLER

REDIT CHECKING TERMINAL

:k diagram of a PPS-4/1 microcomputer circuit pried to a credit checking terminal is shown in Figure 14. ie functions of this terminal are to accept information om a 48-key matrix which inputs the customer identification number and amount of purchase, to display this iformation on a 6-digit display and to transmit this iformation through a UART and a modem over a telephone ne to a central credit agency. The controller then is nplemented to receive credit verification information ver a telephone line through a modem back to the UART nd to display the results of that verification on indicator ghts associated with the display.

Most of the techniques used with this application have een discussed in earlier examples with one exception. he DS signal going from the PPS-4/1 to the UART is erived from the serial output channel using that output as n additional discrete output. The status of the most ignificant bit in the S Register is always available on the erial output channel so that when the serial output :apability is not required that line may be used as an additional discrete. Note that the serial output capability can also be used as a pulse output which is 2 or 4 or 6 clock cycles wide. This is accomplished by outputting a serial four bit word with one of the following bit patterns: 0100, or 0110 or 0111.

The error indication on discrete input/output line 7 is derived from an OR gate which combines the three classes of error indications provided by the UART. If more detailed information is required, then the serial input/output capability could be used for providing the control and status information between the UART and the PPS-4/1 circuit.

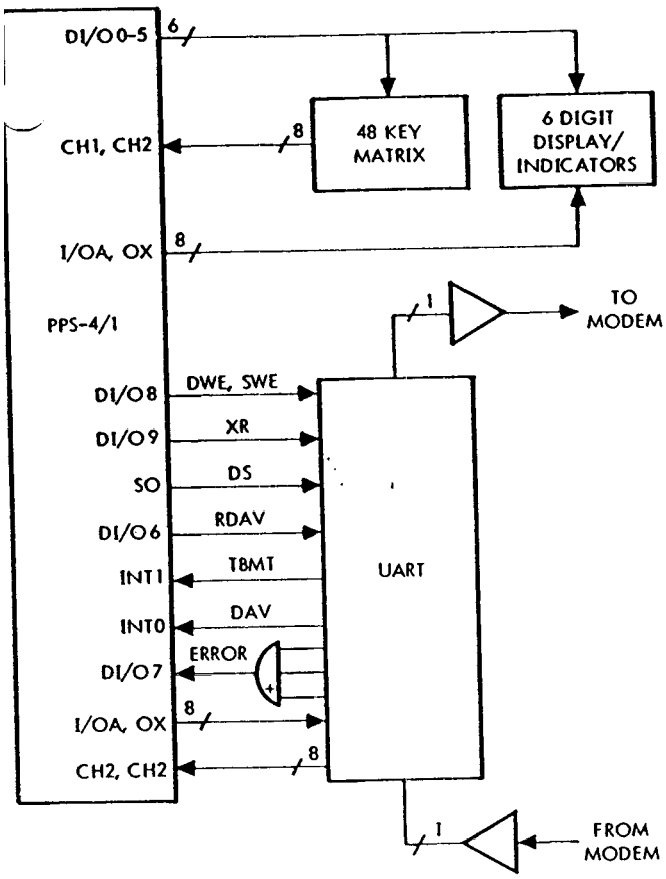


Figure 14. PPS-4/1 CREDIT CHECKING TERMINAL (PARALLEL INTERFACE)

ANALOG INTERFACE

A PPS-4/1 system may also be used in applications which have a primary interface which is analog. There are many digital to analog and analog to digital converters available which may be interfaced with a PPS-4/1. A PPS-4/1 may provide this interface directly when coupled with an appropriate network. A block diagram for such a system is shown in Figure 15.

In this example, the buffered outputs from the Accumulator and X Register are used to drive a resistor network. This network ratios the voltage reference into the network as controlled by the bit pattern supplied from the Accumulator and X Register. The voltage generated is applied to an operational amplifier. The resulting voltage is directly proportional to the 8-bit number output.

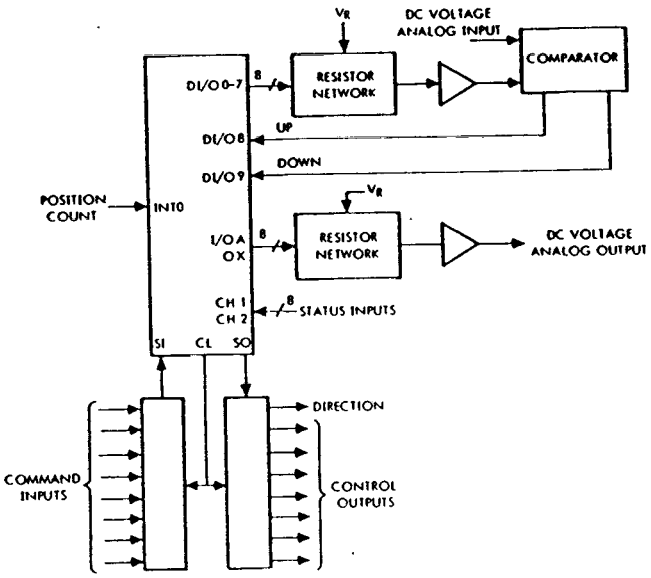


Figure 15. PPS-4/1 ANALOG INTERFACE

A similar network is driven from discrete input/output lines zero through 7 through an operational amplifier to a comparator to provide a DC voltage analog to digital conversion capability. In this case, the unknown analog voltage is compared with the voltage derived from the resistor network. The output of the comparator provides up or down control signals through discrete input/output lines 8 or 9. The software in the PPS-4/1 then modifies the number output to the resistor network in a successive approximation technique until the voltage derived from the network matches the unknown analog input. When the match occurs, the digital number output through the discrete channels is identical to the representation of the analog input.

If the DC voltage analog output is driving a servo motor and its shaft provides an incremental feedback as the shaft rotates, the interrupt zero (INT0) line may be used to provide continuous updating to the PPS-4/1 system so that the servo can be controlled by an internally stored profile of error magnitude versus output voltage control signal desired. Since the motor may be driven in either direction, an output from the serial output is used to indicate direction. The remaining input/outputs from the serial I/O are used in this example as status inputs, command inputs and control outputs. The control outputs may be controlling an external analog multiplexer and sample and hold circuits so that the digital to analog conversion and the analog to digital conversion networks shown may be multiplied over several channels.

LOW COST CASH REGISTER

The low cost cash register example shown in Figure 16 illustrates another capability which is available in the PPS-4/1 microcomputer system. This capability allows more than one PPS-4/1 microcomputer to be used in a system.

Communication between PPS-4/1 microcomputers can be accomplished over any of the input/output lines. In this specific example, the communication is accomplished through the serial input and output lines of both PPS-4/1 units.

Handshaking information and status information is communicated over the discrete input/output lines 8 and 9 in one unit and 3 and 4 in the other unit to establish a communications protocol between the two units. The unit that has data ready to transmit indicates over its data ready I/O line and the unit which will receive the data indicates over its receiver ready line that communication can now occur. The transmitting PPS-4/1 then outputs the contents of its S Register to the receiving PPS-4/1 S Register. The clock circuits may be tied together without interference since in a nonoperating status the clock lines

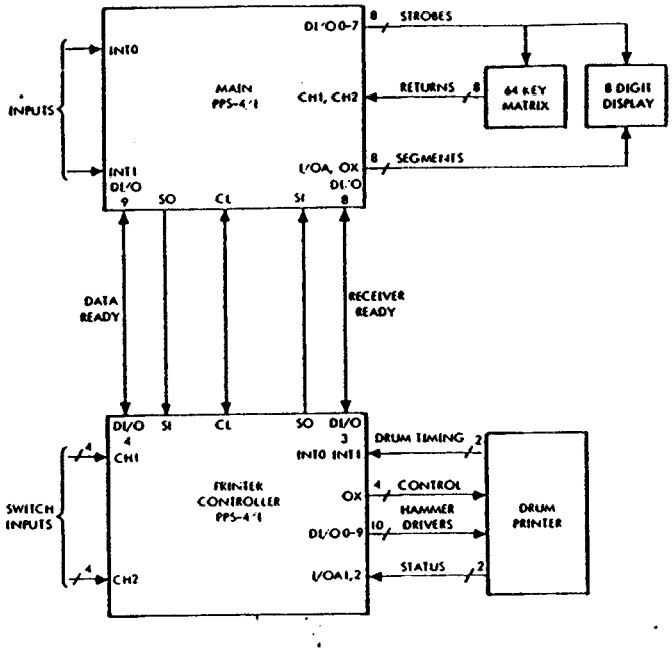


Figure 16. PPS-4/1 LOW COST CASH REGISTER

float. The transmitting unit clocks the information into the receiving unit and turns off the data ready signal. The receiving system shifts the information into its S Register under control of the external shift clock and turns off the receiver ready signal until the data is removed from the S Register. Of course, at the same time that the second unit is shifting information in, it may be shifting information out so that an exchange of information may be readily accomplished at the same time.

In this particular application, one of the PPS-4/1 microcomputers is used as the primary controller for the cash register and handles the primary inputs and the display functions. The second unit provides the primary control for a print mechanism and may provide additional computations such as tax tables.

APPLICATIONS SUMMARY

The potential applications which have been outlined are intended to illustrate various techniques which may be used in specific applications in any combination as required. The examples illustrate the input/output flexibility, expandability, and compatibility with both analog and digital external systems. The flexibility of the PPS-4/1 microcomputer family allows use as a complete controller, as a shared controller with other PPS-4/1 microcomputers or as a peripheral control device for working in more sophisticated computer systems.

APPENDIX A
MM77L AND MM78L LOW VOLTAGE, LOW POWER VERSIONS

INTRODUCTION

The MM77L and MM78L are functionally the same as the MM77 and MM78, respectively, except that the MM77L has a 1536x8 ROM whereas the MM77 has a 1344x8 ROM. The major electrical difference is that the MM77L and 78L operate on any voltage between -6.5 volts and -11 volts and require only 15 milliwatts nominal power at -8.5 volts. This wide voltage range and low power requirement is compatible with standard 9-volt battery outputs making the MM77L and 78L ideal for portable equipment or equipment requiring a battery backup power supply.

The clock circuit has been modified to operate in any of four modes. See the Clock Control paragraph.

Another added electrical feature is that mask programmable pull-down resistor options are available on the inputs and outputs. Refer to the Notes on the SPECIFICATION page for details. The desired coding information is provided along with the ROM coding information on the ROM Code order form.

The major physical difference is that the MM77L and 78L are packaged in a standard 40-pin DIP instead of 42-pin quad package used for the MM77. This package is available with an operating range of -40°C to 85°C on special order.

SPECIAL ELECTRICAL FEATURES

- Battery Compatible (-6.5 to -11 volt operation)
- Low Power 15 milliwatts nominal @ -8.5 volts
- Four Clock Modes including external crystal
- Low Impedance Drivers
  - DI/O less than 100 ohm @ 10 ma
  - RIO less than 250 ohm @ 6 ma
- Mask Programmed Resistors on Outputs
- Mask Programmed Resistors on Inputs

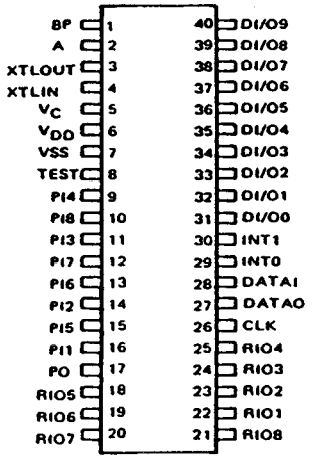


Figure A-1. MM77L AND MM78L PIN CONFIGURATION

CLOCK CONTROL (VC, XTLIN, XTLOUT, A, AND BP)

The internal Oscillator and Clock circuit generates a four-phase A BP clock signal used for all internal logic functions. The A BP clock terms are also brought out so external logic can be synchronized. The clock for the MM77L and 78L can be selected to operate in one of four modes as shown by the table below. These options are selected by control voltages applied to the VC and XTLIN pins.

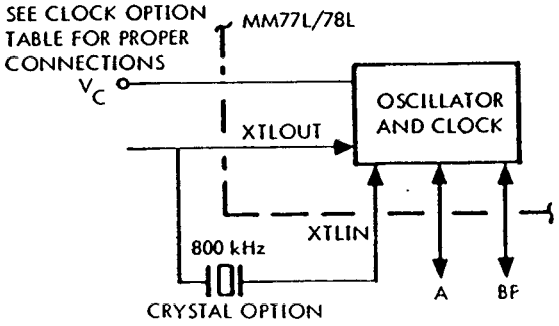


Figure A-2. MM77L AND MM78L CLOCK CIRCUIT

Mode	Pins					Frequency
	VC	XTLIN	XTLOUT	A I/O	BP I/O	
INTERNAL	*VC	VSS	–	OUT	OUT	100 kHz ±30% @ 8.5V
EXTERNAL	GRD	CLOCK	–	OUT	OUT	400 – 800 kHz @ 8.0V
CRYSTAL	GRD	XTAL	XTAL	OUT	OUT	400 – 800 kHz @ 8.0V
SLAVE	VDD	VDD	–	IN	IN	100 kHz – 50 kHz @ 8.5V

*Can be adjusted to vary frequency – Normally set to V_{DD}

/STEM DEVELOPMENT AIDS

ll of the development aids described for the MM77 are in support of MM77L and 78L program development. ...ever, due to the lower operating voltage, the optional pull-down selections, and the physically different package, the MM77 development aids cannot directly simulate the MM77L electrical interfaces. The B7898 Development Circuit is made specifically for the MM77L and 78L and will simulate the electrical interfaces where required.

Table A-1. MM77L AND 78L ELECTRICAL SPECIFICATIONS

OPERATING CHARACTERISTICS

Supply Voltage:
VDD = -8.5 Volts -2.5, +2.0 Volts
(Logic "1" = most negative voltage V_{IL} and V_{OL}.)
VSS = 0 Volts (GND)
(Logic "0" = most positive voltage V_{IH} and V_{OH}.)

System Operating Frequencies:
(1) Internal: 100 kHz Nominal at VDD = -8.5V
(2) External 800 kHz Crystal: 100 kHz

Device Power Consumption:
15 mw, typical

Input Capacitance:
<5 pf

...t Leakage:
<10 μa

Open Drain Driver Leakage (R OFF):
⩽10 μa at -30 Volts

Operating Ambient Temperature (T_A):
0°C to 70°C (Commercial)
-40°C to +85°C (Industrial

Storage Temperature:
-55°C to 120°C

ABSOLUTE MAXIMUM VOLTAGE RATINGS
(with respect to VSS)

Maximum negative voltage on any pin -30 volts.

Maximum positive voltage on any pin +3.0 volts.

TEST CONDITIONS: VDD = 8.5V, T = 25°C

Input/Output	Symbol	Limits (VSS = 0) Min	Typ	Max	Limits (VSS = +5V) Min	Typ	Max	Timing (Sample/ Good)	Test Conditions
Supply Current (Average) for VDD	I_{DD}		1.75 ma	3 ma		1.75 ma	3 ma		
Discrete I/O's DI/O0-DI/O9	V_{IH} V_{IL}	-1.0V		 -4.2V	+3.0V		 +0.8V	Ø3, 4	
DI/O0-9	R_{ON}			100 ohms			100 ohms	Ø2*	10.0 ma max.
Channel 1 Input PI1-PI4	V_{IH} V_{IL}	-1.5V		 -4.2V	+3.5V		 +0.8V	Ø1	
Channel 2 Input PI5-PI8	V_{IH} V_{IL}	-1.5V		 -4.2V	+3.5V		 +0.8V	Ø3	
I/O Channel A RIO1-RIO4	V_{IH} V_{IL}	-1.5V		 -4.2V	+3.5V		 +0.8V	Ø4	
	R_{ON}			250 ohms			250 ohms	Ø2*	6.0 ma max.
...Channel B RIO5-RIO8	V_{IH} V_{IL}	-1.5V		 -4.2V	+3.5V		 +0.8V	Ø4	
	R_{ON}			250 ohms			250 ohms	Ø2*	6.0 ma max

Table A-1. MM77L AND 78L ELECTRICAL SPECIFICATIONS (continued)

Input/Output	Symbol	Limits (VSS = 0) Min	Typ	Max	Limits (VSS = +5V) Min	Typ	Max	Timing (Sample/ Good)	Test Conditions
DATAI	V_{IH} V_{IL}	-1.0V		-4.2V	+4.0V		+0.8V	ø4	
DATAO	R_{ON}			500 ohms			500 ohms	ø4**	3.0 ma max.
INT0	V_{IH} V_{IL}	-1.5V		-4.2V	+3.5V		+0.8V	ø3	
INT1	V_{IH} V_{IL}	-1.5V		-4.2V	+3.5V		+0.8V	ø1	
Clock A, BP	V_{OH} V_{OL}	-1.0V		-5.0V	+4.0V		0V		CL=50 pf (max)
XTLIN	V_{IH} V_{IL}	-1.0V		-6.0V	+3.5V		-1.0V	-4.0V	
Shift Clock Clock	V_{IH} V_{IL}	-1.0V		-4.2V	+4.0V		+0.8V	ø3, 4	
	R_{ON}			500 ohms			500 ohms	ø4**	2.0 ma max.
VC	V_{IH} V_{IL}								V=11.0V max.
PO	V_{IH} V_{IL}	-2.5V		-5.0V	+2.5V		0V		Special circuit

*State established by ø2 (minimum impedance after ø4).
**Same as above except ø4 minimum at ø2 of next cycle.

NOTES:

Mask Programmed Pull-Down Resistors on Outputs

Resistor pull-downs are available as an option on all RIO and DI/O outputs. These pull-downs are connected to VDD. The following values ±25% are available: 3K, 5K, 10K, 15K, 25K, and Open Circuit.

Pull-Downs on Inputs

MOS FET pull-downs are also available as an option on the PI, INT, and DATAI inputs. The output current is 50 μa ±25 μa with the input grounded and VDD at -8.5 volts.

Table A-2. PPS-4/1 MM77L, MM78L SIGNALS (Part No. B77XX and B78XX)

Pin No.	Signal Name	Function
1	BP	B Prime System Clock
2	A	A System Clock
3	XTLOUT	Crystal Output
4	XTLIN	Crystal Input
5	VC	Resistor frequency control R to VDD
6	VDD	-15 Volt Supply (1st pin)
7	VSS	VSS Positive Power Supply Terminal
8	TEST	Commands Test Mode (VSS normal operation)
9	PI4	Channel 1 bit 4
10	PI8	Channel 2 most significant bit (4)
11	PI3	Channel 1 bit 3
12	PI7	Channel 2 bit 3
13	PI6	Channel 2 bit 2
14	PI2	Channel 1 bit 2
15	PI5	Channel 2 bit 1
16	PI1	Channel 1 Bit 1
17	PO	Power On reset input
18	RIO5	X I/O Channel Least Significant Bit (1)
19	RIO6	X I/O Channel bit 2
20	RIO7	X I/O Channel bit 3
21	RIO8	X I/O Channel bit 4
22	RIO1	A I/O Channel bit 1
23	RIO2	A I/O Channel bit 2
24	RIO3	A I/O Channel bit 3
25	RIO4	A I/O Channel bit 4
26	CLOCK	Shift Clock Output or Input (VDD if serial register not used)
27	DATAO	Serial Output signal
28	DATAI	Serial Input signal
29	INT0	Interrupt 0 input
30	INT1	Interrupt 1 input
31	DI/O 0	Discrete I/O line 0
32	DI/O 1	Discrete I/O line 1
33	DI/O 2	Discrete I/O line 2
34	DI/O 3	Discrete I/O line 3
35	DI/O 4	Discrete I/O line 4
36	DI/O 5	Discrete I/O line 5
37	DI/O 6	Discrete I/O line 6
38	DI/O 7	Discrete I/O line 7
39	DI/O 8	Discrete I/O line 8
40	DI/O 9	Discrete I/O line 9

Table A-3. PPS-4/1 MM77L, MM78L PERSONALITY MODULE DEVELOPMENT CIRCUIT SIGNAL
(Part No. B7899)

Pin No.	Signal Name	Function	Pin No.	Signal Name	Function
1	—		33	(P5B3)	PC bit 5, BL bit 3
2	RIO 6	Same as B77XX	34	(P4B2)	PC bit 4, BL bit 2
3	RIO 7	Same as B77XX	35	(P3B1)	PC bit 3, BL bit 1
4	RIO 8	Same as B77XX	36	XTLOUT	Same as B77XX
5	RIO 1	Same as B77XX	37	XTLIN	Same as B77XX
6	RIO 2	Same as B77XX	38	(I8)	Instruction bit 8
7	—		39	(I7)	Instruction bit 7
8	RIO 3	Same as B77XX	40	—	
9	RIO 4	Same as B77XX	41	VC	Same as B77XX
10	CLOCK	Same as B77XX	42	VDD	Same as B77XX
11	DATAO	Same as B77XX	43	(P11B7)	PC bit 11, BU bit 7
12	DATAI	Same as B77XX	44	(P8I4)	PC bit 8, Inst bit 4
13	(P2I2)	PC bit 2, Inst bit 2	45	(P9I6)	PC bit 9, Inst bit 6
14	(P6B4)	PC bit 6, BL bit 4	46	(P10I5)	PC bit 10, Inst bit 5
15	INT0	Same as B77XX	47	(P7I3)	PC bit 7, Inst bit 3
16	INT1	Same as B77XX	48	TEST	Same as B77XX
17	DI/O 0	Same as B77XX	49	PI4	Same as B77XX
18	DI/O 1	Same as B77XX	50	PI8	Same as B77XX
19	DI/O 2	Same as B77XX	51	PI3	Same as B77XX
20	DI/O 3	Same as B77XX	52	PI7	Same as B77XX
21	DI/O 4	Same as B77XX	53	PI6	Same as B77XX
22	DI/O 5	Same as B77XX	54	PI2	Same as B77XX
23	—		55	PI5	Same as B77XX
24	(P1I1)	PC bit 1, Inst bit 1	56	PI1	Same as B77XX
25	—		57	PO	Same as B77XX
26	DI/O 6	Same as B77XX	58	(B5)	BU bit 5
27	DI/O 7	Same as B77XX	59	(B6)	BU bit 6
28	VSS	Same as B77XX	60	(SKIP)	Skip indicator
29	DI/O 8	Same as B77XX	61	—	
30	DI/O 9	Same as B77XX	62	—	
31	BP	Same as B77XX	63	—	
32	A	Same as B77XX	64	RI/O 5	Same as B77XX

PC outputs during phase 2 in complement form. (0 = -V, 1 = VSS)
B outputs during phase 4 in complement form. (0 = -V, 1 = VSS)
Inst inputs at end of phase 4 in true form. (0 = VSS, 1 = -V)
Skip output is -V during Ø4 if next instruction is to be skipped.

Table A-4. PPS-4/1 MM77L, MM78L DEVELOPMENT CIRCUIT SIGNAL

(Part No. B7898)

Pin No.	Signal Name	Function	Pin No.	Signal Name	Function
1	DI/O1	Same as B77XX	27	PI4	Same as B77XX
2	DI/O2	Same as B77XX	28	PI8	Same as B77XX
3	DI/O3	Same as B77XX	29	PI3	Same as B77XX
4	DI/O4	Same as B77XX	30	PI7	Same as B77XX
5	(P1I1)	PC bit 1, Inst bit 1	31	PI6	Same as B77XX
6	DI/O5	Same as B77XX	32	PI2	Same as B77XX
7	DI/O6	Same as B77XX	33	PI5	Same as B77XX
8	DI/O7	Same as B77XX	34	PI1	Same as B77XX
9	DI/O8	Same as B77XX	35	PO	Same as B77XX
10	DI/O9	Same as B77XX	36	(P6B4)	PC bit 6, BL bit 4
11	BP	Same as B77XX	37	(P2I2)	PC bit 2, Inst bit 2
12	A	Same as B77XX	38	VSS	Same as B77XX
13	(P5B3)	PC bit 5, BL bit 3	39	RIO5	Same as B77XX
14	(P4B2)	PC bit 4, BL bit 2	40	RIO6	Same as B77XX
15	(P3B1)	PC bit 3, BL bit 1	41	RIO7	Same as B77XX
16	XTLOUT	Same as B77XX	42	RIO8	Same as B77XX
17	XTLIN	Same as B77XX	43	RIO1	Same as B77XX
18	(I8)	Inst bit 8	44	RIO2	Same as B77XX
19	(I7)	Inst bit 7	45	RIO3	Same as B77XX
20	VC	Same as B77XX	46	RIO4	Same as B77XX
21	VDD	Same as B77XX	47	CLOCK	Same as B77XX
22	(P11B7)	PC bit 11, BU bit 7	48	DATAO	Same as B77XX
23	(P8I4)	PC bit 8, Inst bit 4	49	DATAI	Same as B77XX
24	(P9I6)	PC bit 9, Inst bit 6	50	INT0	Same as B77XX
25	(P10I5)	PC bit 10, Inst bit 5	51	INT1	Same as B77XX
26	(P7I3)	PC bit 7, Inst bit 3	52	DI/O0	Same as B77XX

PC outputs during phase 2 in complement form. (0 = -V, 1 = VSS)
B outputs during phase 4 in complement form. (0 = -V, 1 = VSS)
Inst inputs at end of phase 4 in true form. (0 = VSS, 1 = -V)