QLogic Corporation

ISP1080 Intelligent SCSI Processor

Data Sheet

Features

- Compliance with draft ANSI X3.302-199x Ultra2 SCSI (SPI-2) standard
- 64-bit PCI host bus interface, compliant with *PCI Local Bus Specification* rev 2.1
- Compliance with *PCI Bus Power Management Interface Specification* Revision 1.0 (PC97)
- Up to 80 Mbytes/sec parallel SCSI transfer rates
- SCSI initiator and target modes of operation
- Onboard RISC processor to execute operations at the I/O control-block level from the host memory
- Supports PCI dual-address cycle (64-bit addressing)
- No host intervention required to execute SCSI operations from start to finish

- Simultaneous, multiple logical threads
- JTAG boundary scan support

Product Description

The ISP1080 adds Ultra2 (Fast-40) SCSI support to the expanding functionality of the ISP. The product is a single-chip, highly integrated bus master, SCSI I/O processor for SCSI initiator and target applications. This device interfaces the PCI bus to an ANSI Ultra2 (Fast-40) SCSI bus and contains an onboard RISC processor. The product is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from start to finish without host intervention. The ISP1080 provides power management feature support in accordance with the *PCI Bus Power Management Interface Specification*. The ISP1080 is host-software compatible with the QLogic ISP1020 and ISP1040 chips. The ISP1080 block diagram is illustrated in figure 1.
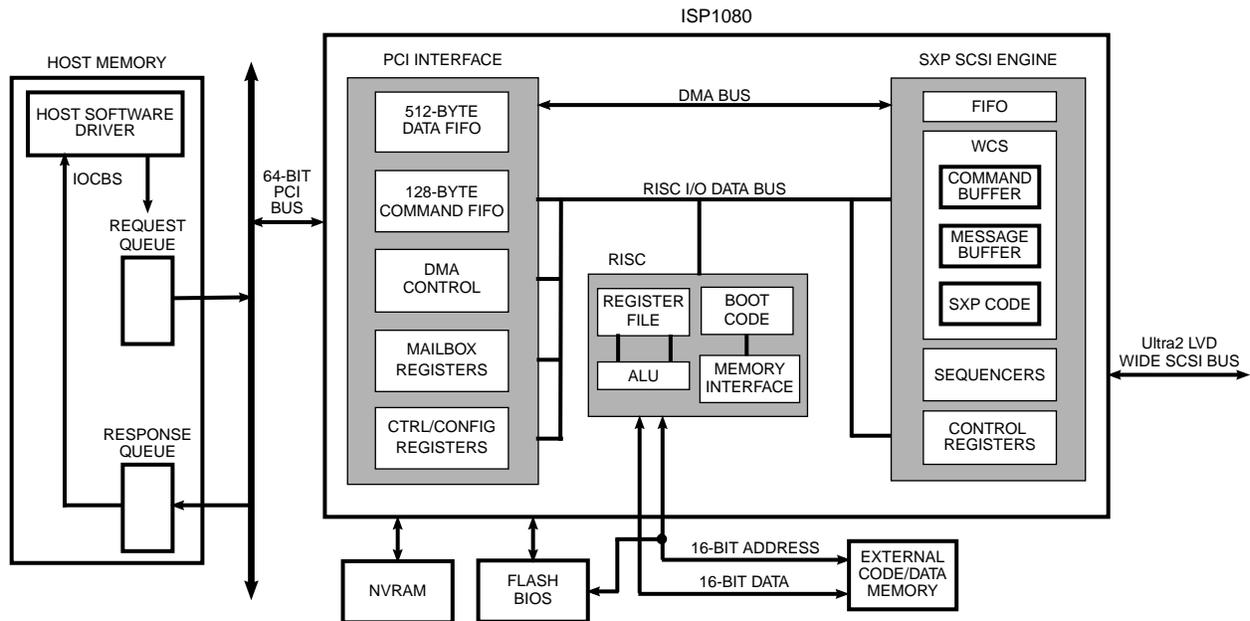

Figure 1. ISP1080 Block Diagram

ISP Initiator and Target Firmware

The ISP1080 firmware implements a cooperative, multitasking host adapter that provides the host system with complete SCSI command and data transport capabilities, thus freeing the host system from the demands of the SCSI bus protocol. The firmware provides two interfaces to the host system: the command interface and the SCSI transport interface. The single-threaded command interface facilitates debugging, configuration, and error recovery, while the multithreaded SCSI transport interface maximizes use of the SCSI and host buses. The ISP1080 can switch between initiator and target modes.

Software Drivers

BIOS firmware is available for the ISP1080. Software drivers are available for the following operating systems:

- AIX
- I$_2$O
- DOS/Windows
- Novell NetWare
- OS/2
- SCO UNIX
- UnixWare
- Windows 95
- Windows NT

Subsystem Organization

To maximize I/O throughput and improve host and SCSI bus utilization, the ISP1080 incorporates a high-speed proprietary RISC processor; an intelligent SCSI bus controller (SCSI executive processor [SXP]); and a host bus, dual-channel, first-party DMA controller. The SCSI bus controller and the host bus DMA controller operate independently and concurrently under the control of the onboard RISC processor for maximum system performance. The ISP1080 RISC interface requires external program data memory.

The complete I/O subsystem solution including the ISP1080 and associated supporting memory devices is shown in figure 2.
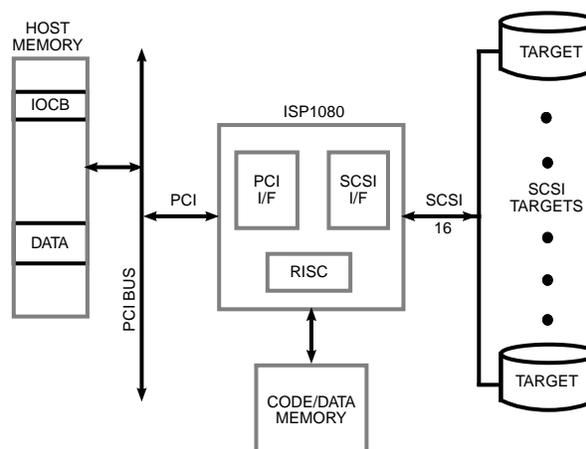

Figure 2.   I/O Subsystem Design Using the ISP1080

Interfaces

The ISP1080 interfaces consist of the PCI bus interface, SCSI interface, RISC interface, BIOS PROM interface, and NVRAM interface. Pins that support these interfaces and other chip operations are shown in figure 3.
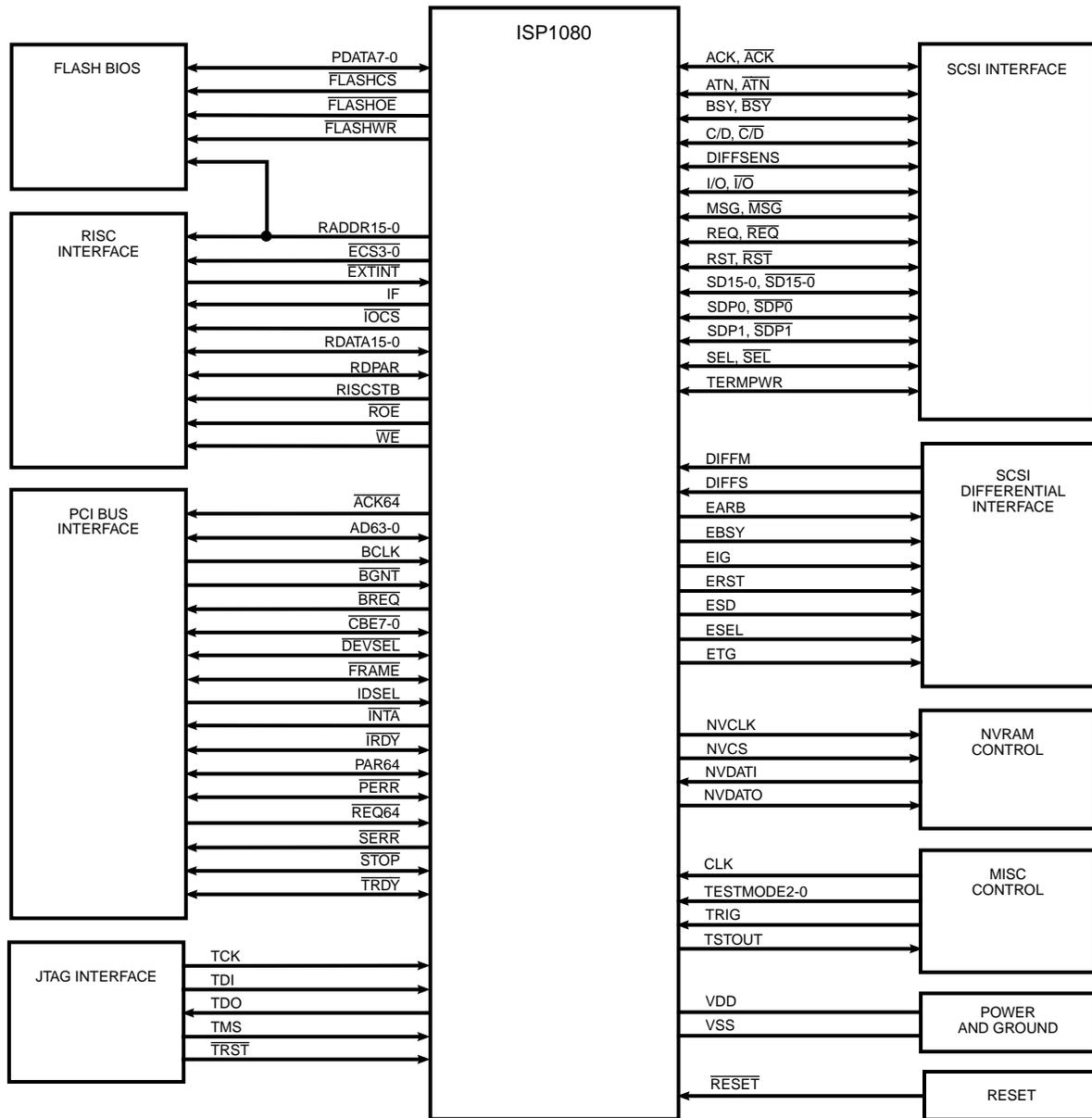
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Figure 3. ISP1080 Functional Signal Grouping

PCI Interface

The ISP1080 PCI interface supports the following:

- 64-bit (address and data), intelligent bus master, burst DMA host interface for fetching I/O control blocks and data transfers
- Supports PCI dual-address cycle (64-bit addressing)
- Backward compatible to 32-bit PCI
- Dual-channel DMA controller

- Data DMA FIFO and command DMA FIFO with threshold control
- 16-bit slave mode for communication with host
- Pipelined DMA registers for efficient scatter and gather operations
- 32-bit DMA transfer counter for I/O transfer lengths of up to four gigabytes
- Support for subsystem ID
- Support for flash BIOS PROM

- Support for PCI cache commands
- 3.3V and 5.0V tolerant PCI I/O buffers

The ISP1080 is designed to interface directly to the PCI bus and operate as a 64-bit DMA bus master. This operation is accomplished through a PCI bus interface unit (PBIU) that contains an onboard DMA controller. The PBIU generates and samples PCI control signals, generates host memory addresses, and facilitates the transfer of data between host memory and the onboard DMA FIFO. It also allows the host to access the ISP1080 internal registers and communicate with the onboard RISC processor through the PCI target mode operation.

The ISP1080 onboard DMA controller consists of two independent DMA channels that initiate transactions on the PCI bus and transfer data between the host memory and DMA FIFO. The two DMA channels are the command DMA channel and the data DMA channel. The command DMA channel is used mainly by the RISC processor for small transfers such as fetching commands from and writing status information to the host memory over the PCI bus. The data DMA channel transfers data between the SCSI bus and the PCI bus.

The PBIU internally arbitrates between the data DMA channel and the command DMA channel and alternately services them. Each DMA channel has a set of DMA registers that are programmed for transfers by the RISC processor.

SCSI Executive Processor

The ISP1080 SXP supports the following:

- Ultra and Ultra2 (Fast-40) SCSI synchronous data transfer rates up to 80 Mbytes/sec
- Asynchronous SCSI data transfer rates up to 12 Mbytes/sec

- Programmable SCSI processor
  - ❏ Specialized instruction set with 16-bit microword
  - ❏ 384-bit by 16-bit internal RAM control store
- 32-bit, configurable SCSI transfer counter
- Command, status, message in, and message out buffers
- Device information storage area
- On-chip, LVD SCSI transceivers
- Programmable active negation

The SXP provides an autonomous, intelligent SCSI interface capable of handling complete SCSI operations. The SXP interrupts the RISC processor only to handle higher level functions such as threaded operations or error handling.

RISC Processor

The ISP1080 RISC processor supports the following:

- Execution of multiple I/O control blocks from the host memory
- Reduced host intervention and interrupt overhead
- One interrupt or less per I/O operation

The onboard RISC processor enables the ISP1080 to handle complete I/O transactions with no intervention from the host. The ISP1080 RISC processor controls the chip interfaces; executes simultaneous, multiple input/output control blocks (IOCB); and maintains the required thread information for each transfer.

Packaging

The ISP1080 is available in a 352-pin, thermally enhanced ballgrid array (TE BGA) package.

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