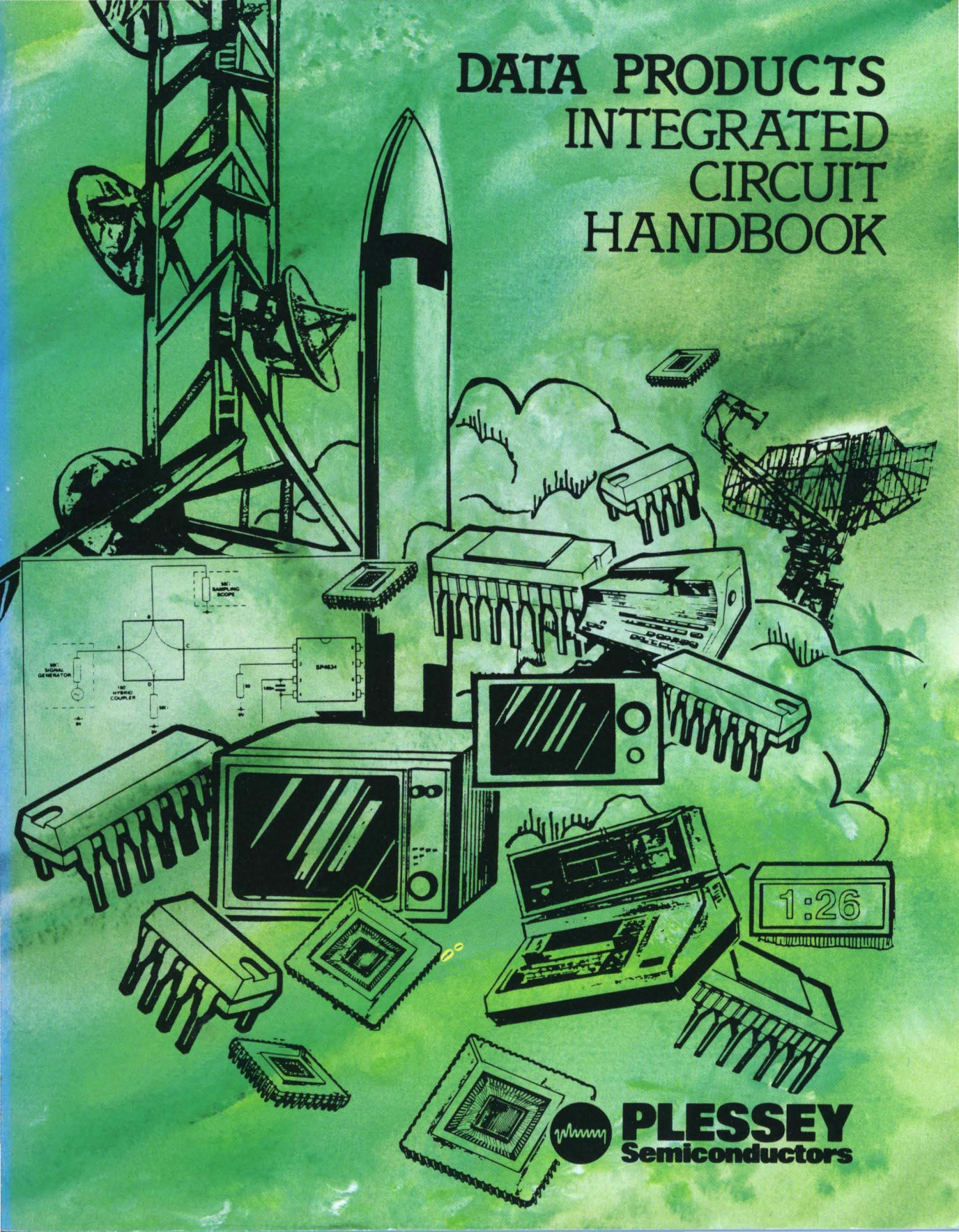
DATA PRODUCTS INTEGRATED CIRCUIT HANDBOOK



PLESSEY
Semiconductors

DATA PRODUCTS INTEGRATED CIRCUIT HANDBOOK

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Semiconductors

Publication No.P.S.1989 September 1985

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EXP products are new designs designated 'Experimental' but which are, nevertheless, serious development projects. Details given may, therefore, change without notice and no undertaking is given or implied as to future availability. Please consult your local Plessey sales office for details of the current status

Equivalents

TYPE NO.	DESCRIPTION	PLESSEY SEMICONDUCTORS EQUIVALENT
AD9685	Ultra fast comparator with latch	**SP9685**
AD9687	Ultra fast dual comparator with latch	**SP9687**
AD9768	High speed 8-bit multiplying D-A converter	**SP9768**
AM685	Ultra fast comparator with latch	**SP9685***
AM687	Ultra fast dual comparator with latch	**SP9687***
MC1648	Voltage-controlled oscillator	**SP1648**
MC1650	Dual A-D comparator	**SP1650**
MC1658	Voltage-controlled multivibrator	**SP1658**
MC1660	Dual 4-input OR/NOR gate	**SP1660,SP16F60***
MC1662	Quad 2-input NOR gate	**SP1662**
MC1664	Quad 2-input OR gate	**SP1664**
MC1670	Master/Slave type D flip-flop	**SP1670**
MC1672	Triple 2-input Exclusive-OR gate	**SP1672**
MC1674	Triple 2-input Exclusive-NOR gate	**SP1674**
MC1692	Quad line receiver	**SP1692**
MC10131	ECL dual type D flip-flop	**SP9131***
MC102131	ECL dual type D flip-flop	**SP9131***
MC105131	ECL dual type D flip-flop	**SP9131***
MC10H131	ECL dual type D flip-flop	**SP9131***
SP1660	Dual 4-input OR/NOR gate	**SP16F60***

*** Higher performance pin-compatible versions**

The quality concept

In common with most semiconductor manufacturers, Plessey Semiconductors perform incoming piece parts check, in-line inspections and final electrical tests. However, quality cannot be inspected into a product; it is only by careful design and evaluation of materials, parts and processes - followed by strict control and ongoing assessment to ensure that design requirements are still being met - that quality products will be produced.

In line with this philosophy, all designs conform to standard layout rules (evolved with performance and reliability in mind), all processes are thoroughly evaluated before introduction and all new piece part designs and suppliers are investigated before authorisation for production use.

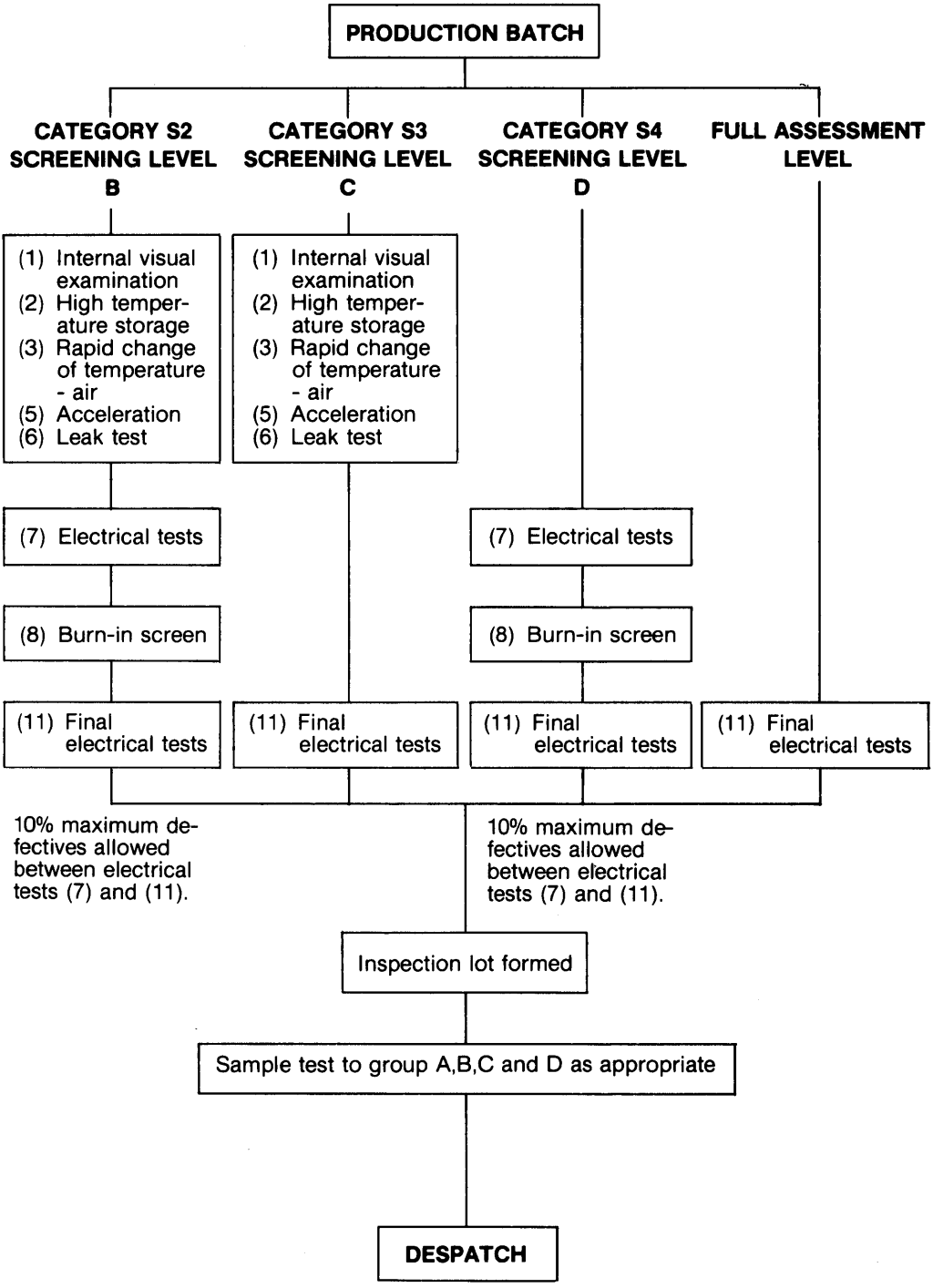
The same basic system of evaluation, appraisals and checks is used on all products up to and including device packing for shipment. It is only at this stage that extra operations are performed for certain customers in terms of lot qualification or release procedure.

By working to common procedures for materials and processes for all types of customers advantages accrue to all users - the high reliability user gains the advantage of scale hence improving the confidence factor in the quality achieved whilst the large scale user gains the benefits associated with basic high reliability design concepts.

Plessey Semiconductors have the following factory approvals. **BS9300** and **BS9400** (BSI Approval No. 1053/M).
DEF-STAN 05-21 (Reg. No. 23H POD).

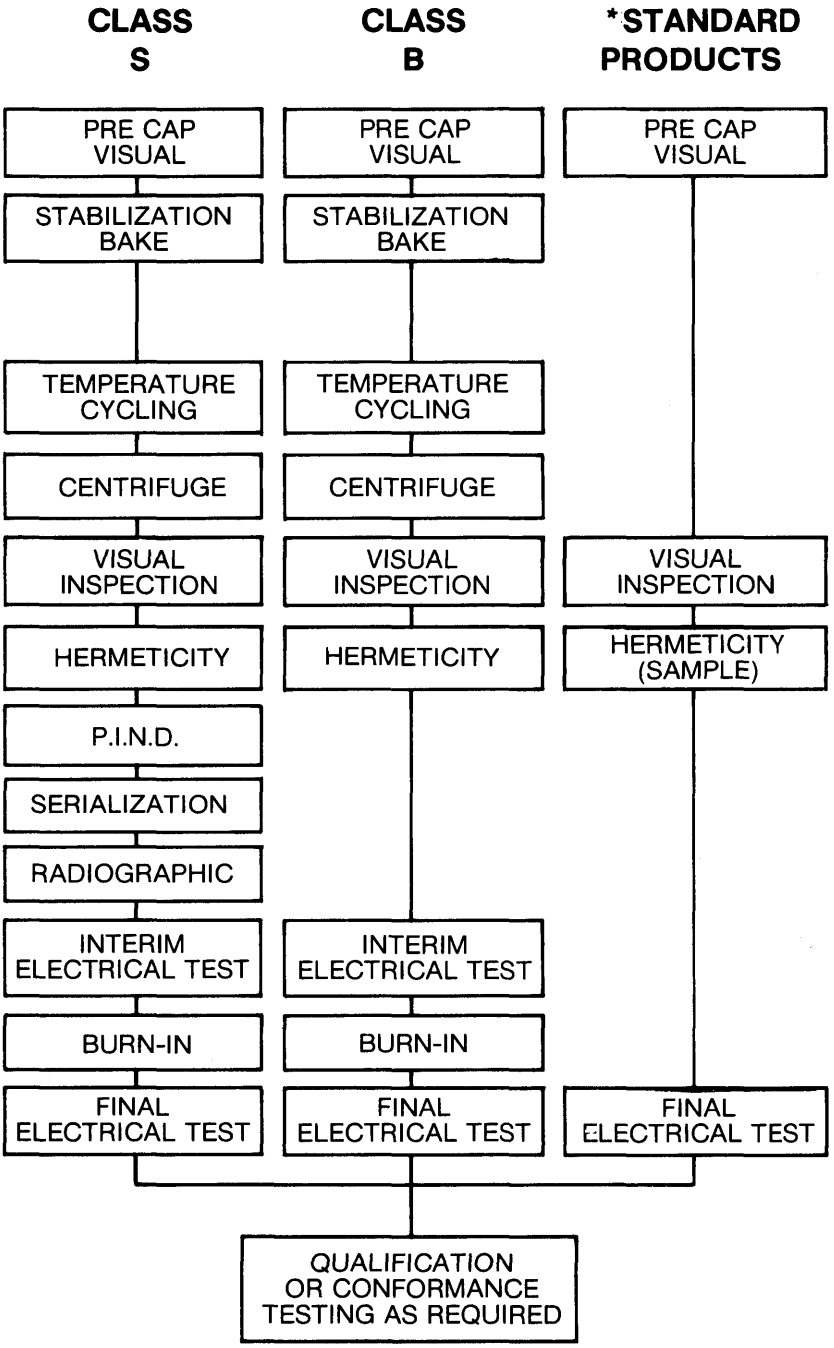
In addition a number of U.S., European and British customers manufacturing electronics for space have approved our facilities.

Screening to BS9400



Plessey Hi-Rel screening

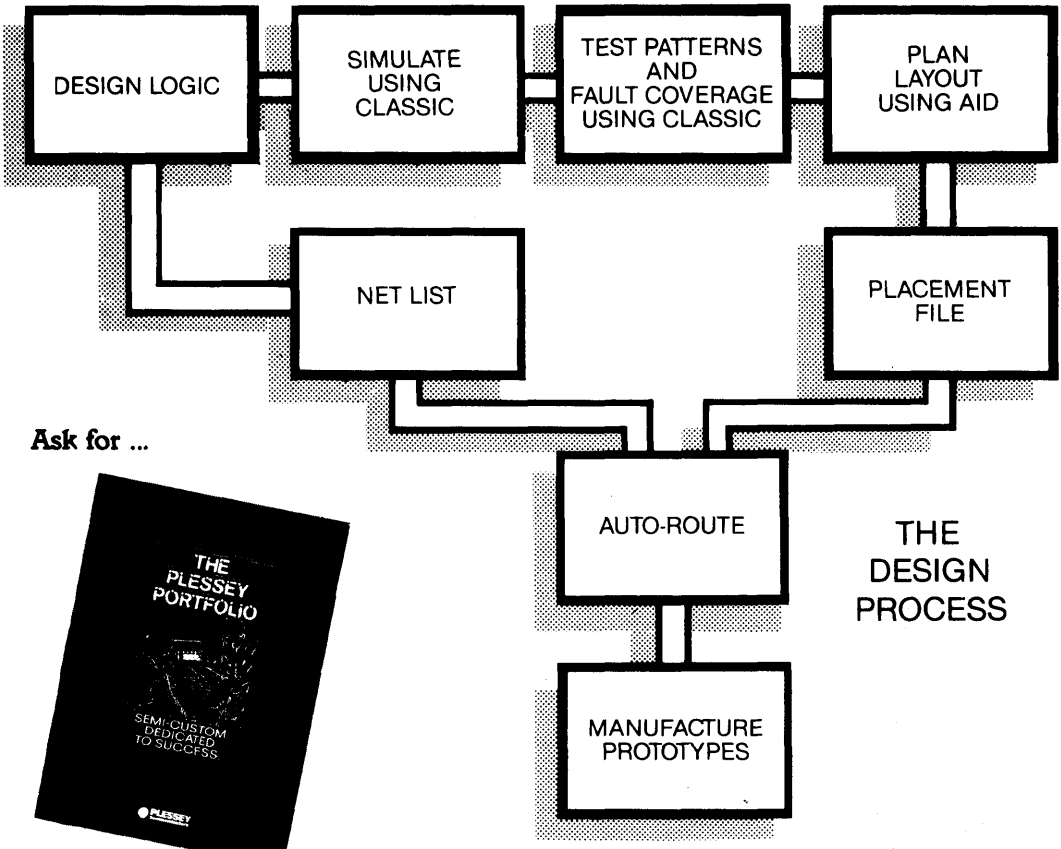
The following Screening Procedures are available from Plessey Semiconductors.



* Plessey Semiconductors reserve the right to change the Screening Procedure for Standard Products.

Semi-custom design

Plessey Semiconductors' advanced work in the Semi-Custom field enables us to offer our customers the opportunity to develop their own high performance circuits using our CLASSIC software. Among the many advantages are:
• CLASSIC is cost effective and user friendly • Prototypes in as little as 3 weeks • Close coordination with customer throughout design and production process • State-of-the-art high performance produces • Up to 10044 gates available



Ask for ...

Microgate-C (Si-Gate CMOS)

CLA 2000 SERIES

- Double layer metallisation
- 5 micron channel length
- Product family:
  CLA 21XX 840 Gates
  CLA 23XX 1400 Gates
  CLA 25XX 2400 Gates
- 7ns max. prop delay
  (2 input NAND fanout of 2 with 2mm track 0-70° C 4.5-5.5V)
- 14MHz system clock rate
- 30MHz toggle rate
- Fully auto-routed

CLA 3000 SERIES

- Double layer metallisation
- 4 micron channel length
- Product family:
  CLA 31XX 840 Gates
  CLA 33XX 1440 Gates
  CLA35XX 2400 Gates
  CLA 37XX 4200 Gates
  CLA 39XX 6000 Gates
- 5ns max. prop delay
- 20MHz system clock rate
- 50MHz toggle rate
- Fully auto-routed

CLA 5000 SERIES

- Double layer metallisation
- 2 micron channel length
- Product family:
  CLA 51XX 640 Gates
  CLA 52XX 1232 Gates
  CLA 53XX 2016 Gates
  CLA 54XX 3060 Gates
  CLA 55XX 4408 Gates
  CLA 56XX 5984 Gates
  CLA 58XX 8064 Gates
  CLA 59XX 10044 Gates
- 2.5ns max. prop delay
- 40MHz system clock rate
- 100MHz toggle rate
- Fully auto-routed

Circuit board design

Devices within this data book are processed on the Plessey high speed bipolar process. The resultant edge speeds obtained will not cause current spikes and voltage ringing if care and attention to layout and line termination is observed. Eurocard or vero board construction is not advised, as it is almost impossible to decouple and provide adequate grounding for the rise times these devices can achieve. This is mostly regardless of the frequency at which the application is functioning. Alternative prototyping circuitry can in most cases be constructed on Wainwright pad system, as this provides a solid ground plane that ceramic chip capacitors can be soldered to directly. Supply decoupling and tolerancing are the major cause for devices failing to meet the data sheet requirements. Most devices in this data book require a 0V and -5.2V supply. The supply tolerance is $\pm$0.25V.

Devices can fail if switch on supply transients occur. These can be of such short duration that the offending spike can only be seen using a high bandwidth scope (1GHz).

The decoupling of supplies should be performed close to the device pins. Low frequency decoupling should also be provided in most cases.

Thermal design

The temperature of any semiconductor device has an important effect upon its long term reliability. For this reason, it is important to minimise the chip temperature; and in any case, the maximum junction temperature should not be exceeded.

Electrical power dissipated in any device is a source of heat. How quickly this heat can be dissipated is directly related to the rise in chip temperature: if the heat can only escape slowly, then the chip temperature will rise further than if the heat can escape quickly. To use an electrical analogy: energy from a constant voltage source can be drawn much faster by using a low resistance load than by using a high resistance load.

The thermal resistance to the flow of heat from the semiconductor junction to the ambient temperature air surrounding the package is made up of several elements. These are the thermal resistance of the junction-to-case, case-to-heatsink and heatsink-to-ambient interfaces. Of course, where no heatsink is used, the case-to-ambient thermal resistance is used.

These thermal resistances may be represented as

$\theta_{ja} = \theta_{jc} + \theta_{ch} + \theta_{ha}$

where θ_{ja} is thermal resistance junction-to-ambient °C/W
θ_{jc} is thermal resistance junction-to-case °C/W
θ_{ch} is thermal resistance case-to-heatsink °C/W
θ_{ha} is thermal resistance heatsink-to-ambient °C/W

The temperature of the junction is also dependent upon the amount of power dissipated in the device — so the greater the power, the greater the temperature.

Just as Ohm's Law is applied in an electrical circuit, a similar relationship is applicable to heatsinks.

$T_j = T_{amb} + P_D (\theta_{ja})$
T_j = junction temperature
T_{amb} = ambient temperature
P_D = dissipated power

From this equation, junction temperature may be calculated, as in the following examples.

Example 1

An SP1650 is to be used at an ambient temperature of +50° C. θ_{ja} for the DG14 package with a chip of approximately 1mm sq is 110° C/W; from the datasheet, P_D = 380mW and $T_j$max = 150° C.

$T_j = T_{amb} + P_D \theta_{ja}$
$= 50 + (0.38 \times 110)$
$= 91.8°$ C (typ.)

Where operation in a higher ambient temperature is necessary, the maximum junction temperature can easily be exceeded unless suitable measures are taken:

Thermal design (cont'd)

Example 2

An SP1650 (T_{amb} max. = +175° C) is to be used at an ambient temperature of +150° C. Again, θ_{ja} = 107° C/W, P_D = 330mW and T_j max. = +175° C.

$$T_j = 150 + (0.33 \times 107)$$
$$= +185.3° C \text{ (typ.)}$$

This clearly exceeds the maximum permissible junction temperature and therefore some means of decreasing the junction-to-ambient thermal resistance is required.

As stated earlier, θ_{ja} is the sum of the individual thermal resistances; of these, θ_{jc} is fixed by the design of device and package and so only the case-to-ambient thermal resistance, θ_{ca}, can be reduced.

If θ_{ca}, and therefore θ_{ja}, is reduced by the use of a suitable heatsink, then the maximum T_{amb} can be increased:

Example 3

Assume that an IERC LIC14A2U dissipator and DC000080B retainer are used. This device is rated as providing a θ_{ja} of 55° C/W for the DG14 package. Using this heatsink with the SP1650 operated as in Example 2 would result in a junction temperature given by:

$$T_j = 150 + (0.33 \times 55)$$
$$= 168° C$$

Nevertheless, it should be noted that these calculations are not necessarily exact. This is because factors such as θ_{jc} may vary from device type to device type, and the efficacy of the heatsink may vary according to the air movement in the equipment.

In addition, the assumption has been made that chip temperature and junction temperature are the same thing. This is not strictly so, as not only can hot spots occur on the chip, but the thermal conductivity of silicon is a variable with temperature, and thus the θ_{jc} is in fact a function of chip temperature. Nevertheless, the method outlined above is a practical method which will give adequate answers for the design of equipment.

It is possible to improve the dissipating capability of the package by the use of heat dissipating bars under the package, and various proprietary items exist for this purpose.

Under certain circumstances, forced air cooling can become necessary, and although the simple approach outlined above is useful, more factors must be taken into account.

Technical data

PLESSEY
Semiconductors

SP1648

VOLTAGE-CONTROLLED OSCILLATOR

The SP1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with ECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The device may also be used in phase locked loops and many other applications requiring a fixed or variable frequency clock source of high spectral purity.

The SP1648 may be operated from a +5.0V dc supply or a -5.2V dc supply, depending upon system requirements.

Operating temperature range:
-30° C to +85° C (Ceramic)
0° C to +75° C (Plastic)

SUPPLY VOLTAGE	GND PINS	SUPPLY PINS
+5.0V dc	7,8	1,14
-5.2V dc	1,14	7,8

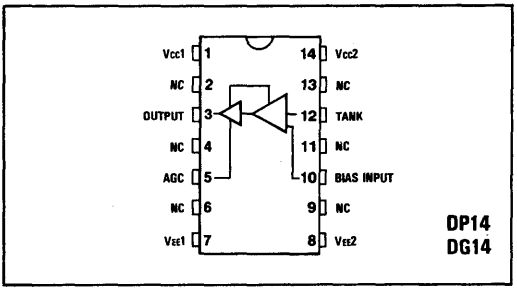


Fig.1 Block diagram and pin connections (top view)

ORDERING INFORMATION

SP1648DP (Commercial - plastic package)
SP1648DG (Commercial - ceramic package)
SP1648BB DG (Plessey High Reliability Specification)

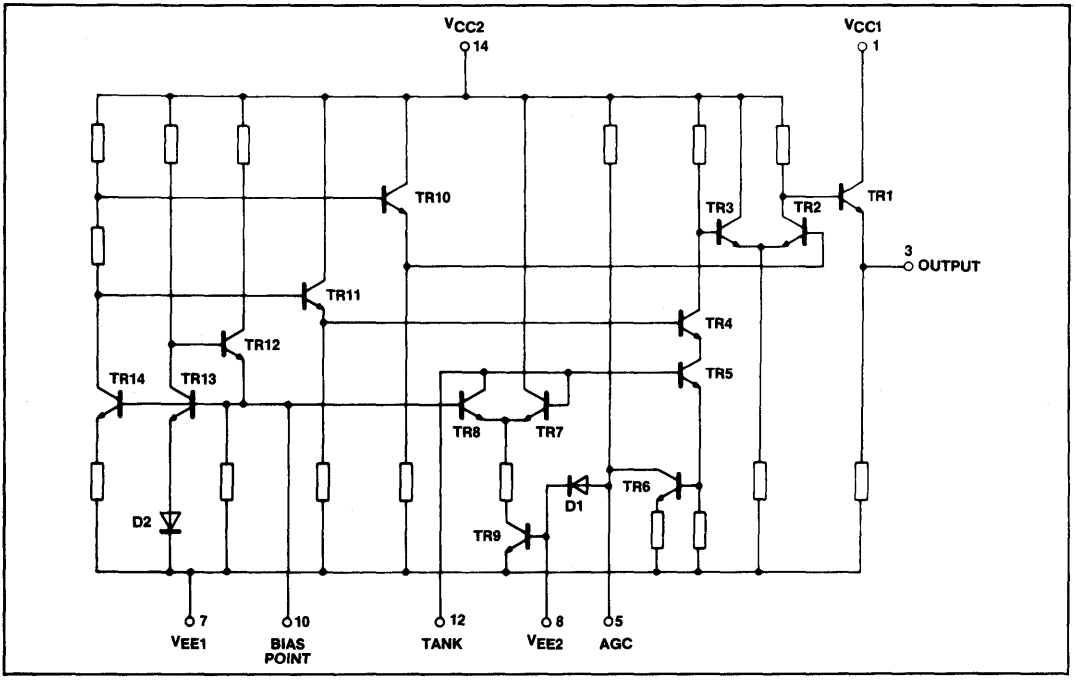


Fig.2 Circuit diagram of SP1648

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\lvert V_{CC} - V_{EE} \rvert$ 8V
Output source current	<40mA
AGC input	V_{CC} to V_{EE}
Storage temperature range	-55°C to +150°C (Ceramic)
	-55°C to +125°C (Plastic)
Operating junction temperature	<175°C

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0V

Characteristic	Symbol	Pin under test	SP1648 Test Limits -30°C Min.	-30°C Max.	+25°C Min.	+25°C Max.	+85°C Min.	+85°C Max.	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH} Max.	V_{IL} Max.	V_{CC}	I_L	V_{EE} (Gnd)
Power supply drain current	I_E	8	-	-	-	40	-	-	mAdc	-	-	1,14	-	7,8
Logic '1' output voltage	V_{OH}	3	3.94	4.18	4.04	4.25	4.11	4.36	Vdc	-	12	1,14	3	7,8
Logic '0' output voltage	V_{OL}	3	3.16	3.40	3.20	3.43	3.23	3.46	Vdc	12	-	1,14	3	7,8
Bias voltage	V_{bias}*	10	1.51	1.86	1.40	1.70	1.28	1.58	Vdc	-	-	1,14	-	7,8
			Min.	Typ. Max.	Min.	Typ. Max.	Min.	Typ. Max.						
Peak-to-peak tank voltage	V_{p-p}	12	-	- -	-	500 -	-	- -	mV	See Fig.4	-	1,14	3	7,8
Output duty cycle	V_{DC}	3	-	- -	-	50 -	-	- -	%	See Fig.4	-	1,14	3	7,8
Oscillation frequency	f_{max}	-	-	- -	200	225 -	-	- -	MHz	See Fig.4	-	1,14	3	7,8

Thermal characteristics

DG14 $\theta_{JA} = 125°C/W$, $\theta_{JC} = 40°C/W$

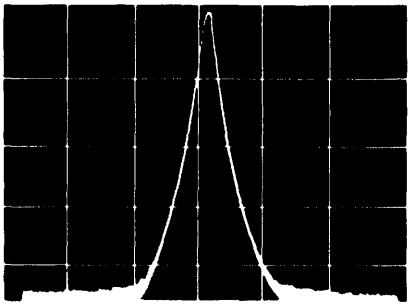
DP14 $\theta_{JA} = 175°C/W$

Supply Voltage = -5.2V

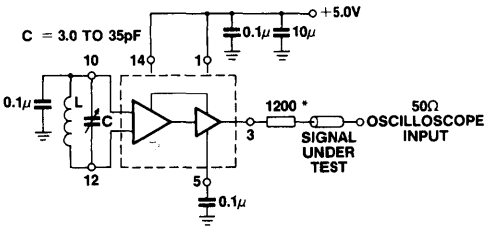
Characteristic	Symbol	Pin under test	SP1648 Test Limits -30°C Min.	-30°C Max.	+25°C Min.	+25°C Max.	+85°C Min.	+85°C Max.	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH} Max.	V_{IL} Max.	V_{CC}	I_L	V_{EE} (Gnd)
Power supply drain current	I_E	8	-	-	-	41	-	-	mAdc	-	-	7,8	-	1,14
Logic '1' output voltage	V_{OH}	3	1.045	-0.815	-0.960	-0.750	-0.890	-0.650	Vdc	-	12	7,8	3	1,14
Logic '0' output voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	12	-	7,8	3	1,14
Bias voltage	V_{bias}*	10	-3.690	-3.340	-3.800	-3.500	-3.920	-3.620	Vdc	-	-	7,8	-	1,14
			Min.	Typ. Max.	Min.	Typ. Max.	Min.	Typ. Max.						
Peak-to-peak tank voltage	V_{p-p}	12	-	- -	-	500 -	-	- -	mV	See Fig.4	-	7,8	3	1,14
Output duty cycle	V_{DC}	3	-	- -	-	50 -	-	- -	%	See Fig.4	-	7,8	3	1,14
Oscillation frequency	f_{max}	-	-	- -	200	225 -	-	- -	MHz	See Fig.4	-	7,8	3	1,14

Test temp.	TEST VOLTAGE/CURRENT: Volts V_{IH} Max.	Volts V_{IL} Min.	Volts V_{CC}	mAdc I_L
-30°C	+1.960	+1.410	5.0	5.0
+25°C	+1.800	+1.300	5.0	5.0
+85°C	+1.680	+1.180	5.0	5.0

Test temp.	TEST VOLTAGE/CURRENT: Volts V_{IH} Max.	Volts V_{IL} Min.	Volts V_{CC}	mAdc I_L
-30°C	-3.240	-3.790	5.2	5.0
+25°C	-3.400	-3.900	5.2	5.0
+85°C	-3.520	-4.020	5.2	5.0

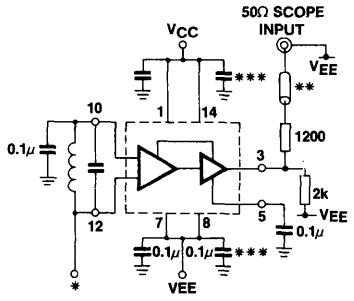


B.W. = 10kHz
Center Frequency = 100MHz
Scan Width = 50kHz/div
Vertical Scale = 10dB/div



*The 1200Ω resistor and the scope termination impedance constitute a 25:1 attenuator probe.

Fig.3 Spectral purity of signal at output



*Use high impedance probe (>1.0MΩ must be used).
**The 1200Ω resistor and the scope termination impedance constitute a 25:1 attenuator probe.

***Bypass only that supply opposite ground.

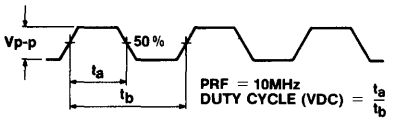


Fig.4 Test circuit and waveforms

OPERATING CHARACTERISTICS

Fig.1 illustrates the circuit schematic for the SP1648. The oscillator incorporates positive feedback by coupling the base of transistor TR7 to the collector of TR8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (TR7 and TR8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (TR4) is used to translate from the emitter follower (TR5) to the output differential pair TR2 and TR3. TR2 and TR3, in conjunction with output transistor TR1, provide a highly buffered output which produces a square wave. Transistors TR10 through TR14 provide this bias drive for the oscillator and output buffer. Fig.3 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Fig.5), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} (≈1.4V for positive supply operation).

When the SP1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Fig.6.

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figs.7,8 and 9. Figs.7 and 9 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6pF typical). Fig.8 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1kΩ resistor in Figs.7 and 8 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased.

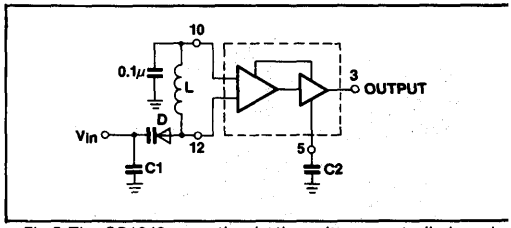


Fig.5 The SP1648 operating in the voltage-controlled mode

The larger-valued resistor (51kΩ) in Fig.9 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D\,(max) + C_S}}{\sqrt{C_D\,(min) + C_S}}$$

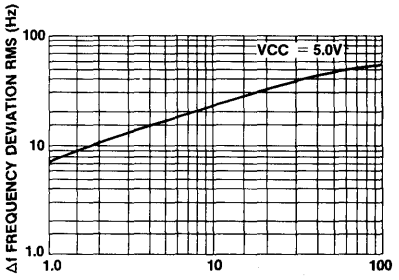
$$\text{where } f_{min} = \frac{1}{2\pi\sqrt{L\,(C_D\,(max) + C_S)}}$$

C_S = shunt capacitance (input plus external capacitance).
C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency by-passing is necessary on the power supply pins (see Fig.3).

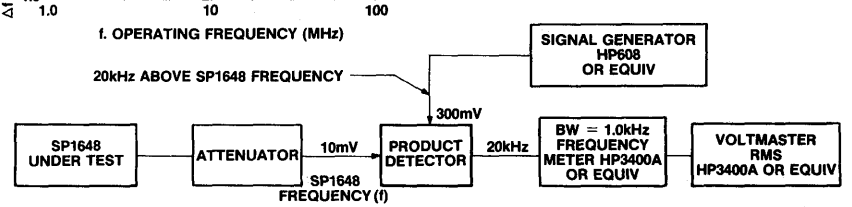
Capacitors (C1 and C2 of Fig.5) should be used to bypass the AGC point and the VCO input (varactor diode) guaranteeing only dc levels at these points.

For output frequency operation between 1MHz and 50MHz a 0.1μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly



OSCILLATOR TANK COMPONENTS (CIRCUIT OF FIGURE 5)

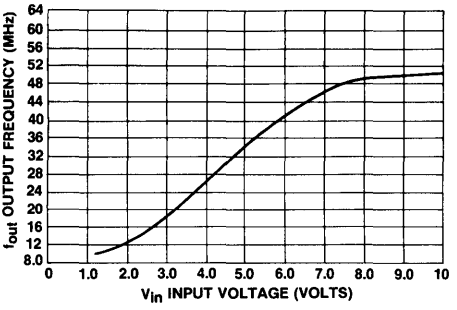
f MHz	D	L μH
1.0-10	MV2115	100
10-60	MV2115	2.3
60-100	MV2106	0.15



$$\text{FREQUENCY DEVIATION} = \frac{\text{(HP5210A OUTPUT VOLTAGE) (FULL SCALE FREQUENCY)}}{\text{1.0VOLT}}$$

Note: Any frequency deviation caused by the signal generator and SP1648 power supply should be determined and minimised prior to testing.

Fig.6 Frequency deviation test circuit



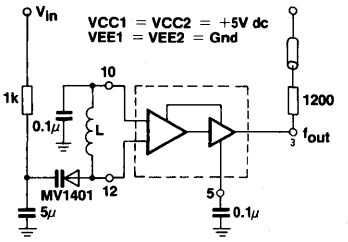
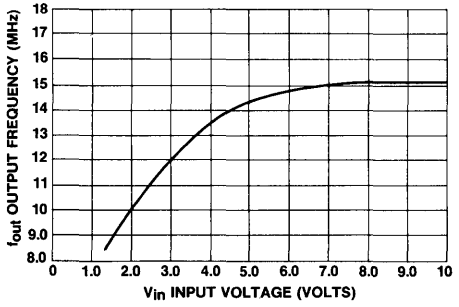


Fig.7



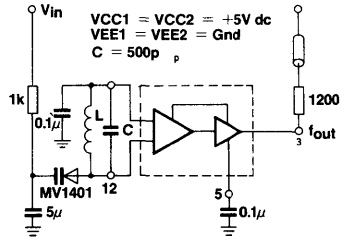
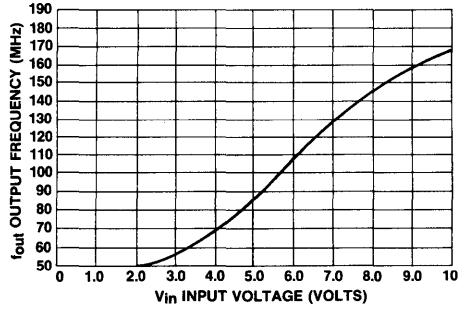


Fig.8



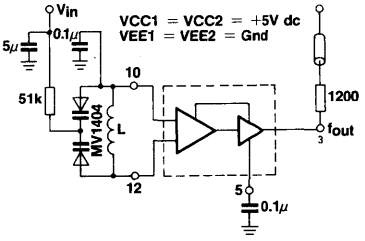


Fig.9

upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimise unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the SP1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0V supply is used, -5.2V if a negative supply is used).

At frequencies above 100MHz typ. it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the SP1648. This is accomplished by attaching a series resistor (1kΩ minimum) from the AGC to the most positive power potential (+5.0V if a +5.0V supply is used, ground if a -5.2V supply is used).

PLESSEY
Semiconductors

SP1650
DUAL A/D COMPARATOR

The SP1650 is a very high speed comparator utilising differential amplifier inputs to sense analogue signals above or below a reference level. An output latch provides a unique sample-hold feature.

Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection, transmitters, receivers, memory translation, sense amplifiers and more.

The clock iinputs ($\overline{C}_a$ and $\overline{C}_b$) operate from ECL III or ECL 10,000 digital levels. When $\overline{C}_a$ is at a logic high level, Q_a will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q}_a$ is the logic complement of Q_a. When the clock in to a low logic level, the outputs are latched in their present state.

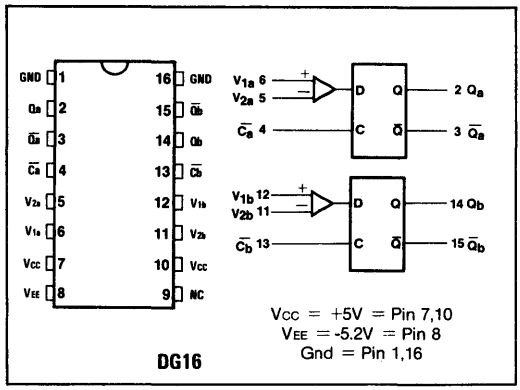


Fig.1(a) Pin connections (top view) Fig.1(b) Logic diagram

FEATURES

- P_D = 330mW typ/pkg (No Load)
- t_{pd} = 3.5ns typ.
- Input Slew Rate = 350V/µs
- Differential Input Voltage: -5.0V to +5.0V (-30°C to +85°C)
- common Mode Range: -3.0V to +2.5V (-30°C to +85°C)
- Resolution: ⩽20mV (-30°C to +85°C)
- Drives 50Ω lines

TRUTH TABLE

$\overline{C}$	V_1 V_2	Qn + 1	$\overline{Qn}$ + 1
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	Q_n	$\overline{Q}_n$

ϕ = Don't Care

ORDERING INFORMATION

SP1650DG (Commercial - ceramic package)
SP1650BB DG (Plessey High Reliability Specification)

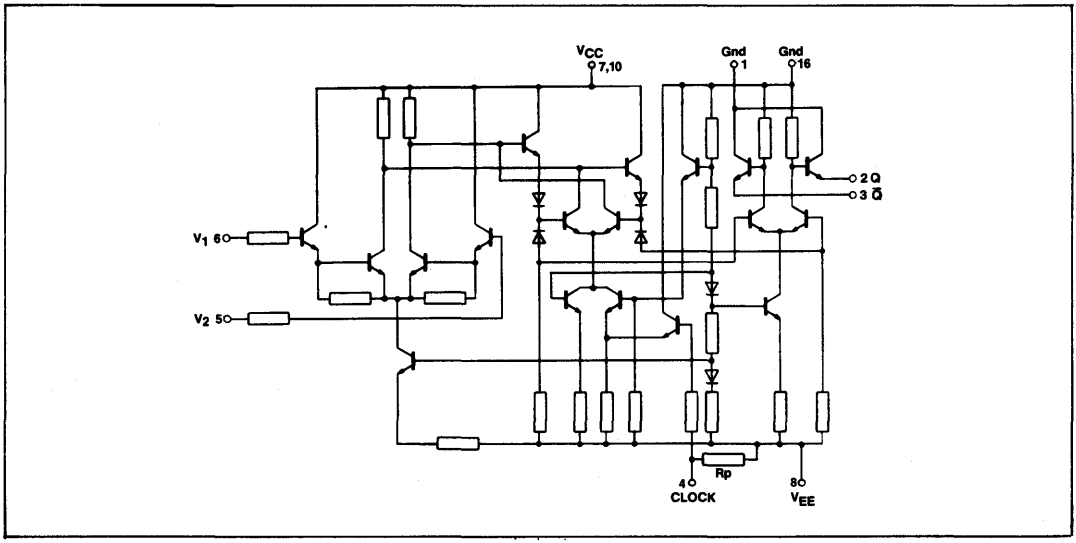


Fig.2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50Ω resistor to -2.0V dc.

Test temp.	TEST VOLTAGE (V)											
	V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} (3)	V_{EE} (3)
-30°C	-0.875	-1.890	-1.180	-1.515	+0.020	-0.020	See Note (4)				+5.0	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020					+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020					+5.0	-5.2

Characteristic	Symbol	Pin under test	SP1650 Test Limits (1)						Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW												Gnd
			-30°C		+25°C		+85°C			V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} (3)	V_{EE} (3)	
			Min.	Max.	Min.	Max.	Min.	Max.														
POWER SUPPLY																						
Drain current																						
Positive	I_{CC}	7,10	-	-	-	25*	-	-	mAdc	-	4,13	-	-	6,12	-	-	-	-	-	7,10	8	1,5,11,16
Negative	I_E	8	-	-	-	55*	-	-	mAdc	4,13	-	-	-	6,12	-	-	-	-	-	7,10	8	1,5,11,16
Input current	I_{IN}	6	-	-	-	10	-	-	μAdc	4	13	-	-	12	-	6	-	-	-	7,10	8	1,5,11,16
Input leakage current	I_R	6	-	-	-	7	-	-	μAdc	4	13	-	-	12	-	-	-	6	-	7,10	8	1,5,11,16
Input clock current	I_{INH}	4	-	-	-	350	-	-	μAdc	4	13	-	-	6,12	-	-	-	-	-	7,10	8	1,5,11,16
	I_{INL}	4	-	-	0.5	-	-	-	μAdc	-	13	-	-	6,12	-	-	-	-	-	7,10	4,8	1,5,11,16
Logic '1' output voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4,13	-	-	-	6,12	-	-	-	-	-	7,10	8	1,5,11,16
		2									-	-	-	-	5,11	-	-	-	-			1,6,12,16
		2									-	-	-	-	-	6,12	5,11	-	-			1,16
		2									-	-	-	-	-	-	-	5,11	6,12			1,16
		3									-	-	-	-	6,12	-	-	-	-			1,5,11,16
		3									-	-	-	5,11	-	-	-	-	-			1,6,12,16
		3									-	-	-	-	-	5,11	6,12	-	-			1,16
		3									-	-	-	-	-	-	-	6,12	5,11			1,16
Logic '0' output voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4,13	-	-	-	-	6,12	-	-	-	-	7,10	8	1,5,11,16
		2									-	-	-	5,11	-	-	-	-	-			1,6,12,16
		2									-	-	-	-	-	5,11	6,12	-	-			1,16
		2									-	-	-	-	-	-	-	6,12	5,11			1,16
		3									-	-	-	6,12	-	-	-	-	-			1,5,11,16
		3									-	-	-	-	5,11	-	-	-	-			1,16,12,16
		3									-	-	-	-	-	6,12	5,11	-	-			1,16
		3									-	-	-	-	-	-	-	5,11	6,12			1,16
Logic '0' threshold voltage (2) 1	V_{OHA}	2	-1.065	-	-0.980	-	-0.910	-	Vdc	-	13	4	-	6	-	-	-	-	-	7,10	8	1,5,16
2		2		-		-		-		-		-	4	-	6	-	-	-	-			
3		3		-		-		-		-		4	-	-	6	-	-	-	-			
4		3		-		-		-		-		-	4	6	-	-	-	-	-			
Logic '0' threshold voltage (2) 1	V_{OLA}	3	-	-1.630	-	-1.600	-	-1.555	Vdc	-	13	4	-	6	-	-	-	-	-	7,10	8	1,5,16
2		3	-		-		-			-		-	4	-	6	-	-	-	-			
3		2	-		-		-			-		4	-	-	6	-	-	-	-			
4		2	-		-		-			-		-	4	6	-	-	-	-	-			

NOTES
1. All data is for ½ SP1650 except data marked (*) which refers to the entire package.
2. These tests done in order indicated. See Figure 6.
3. Maximum Power Supply Voltages (beyond which device life may be impaired):
   $|V_{EE}| + |V_{CC}| < 12V$ dc.
4. At all temperatures, $V_{A3} = +3.000V$, $V_{A4} = +2.980V$, $V_{A5} = -2.500V$ and $V_{A6} = -2.480V$.

Test temp.	TEST VOLTAGE (V) V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} (1)	V_{EE} (1)
-30°C	+2.000	See Note (4)		+1.040	+2.00	+7.00	-3.20
+25°C	+2.000			+1.110	+2.00	+7.00	-3.20
+85°C	+2.000			+1.190	+2.00	+7.00	-3.20

See Figure 4

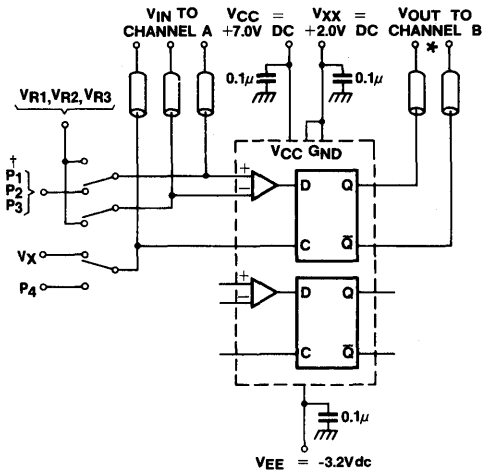
Characteristic	Symbol	Pin under test	SP1650 Test Limits -30°C Min.	-30°C Max.	+25°C Min.	+25°C Max.	+85°C Min.	+85°C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} (1)	V_{EE} (1)	P1	P2	P3	P4
SWITCHING TIMES	t_{6+2+}	2	2.0	5.0	2.0	5.0	2.0	5.7	ns	5	-	-	4	1,11,16	7,10	8	6	-	-	-
Propagation delay	t_{6+2+}	2								-	5	-					-	6	-	-
(50% to 50%)	t_{6+2+}	2								-	-	5					-	-	6	-
V-input to output	t_{6+3-}	3								5	-	-					6	-	-	-
	t_{6+3-}	3								-	5	-					-	6	-	-
	t_{6+3-}	3								-	-	5					-	-	6	-
	t_{6-2-}	2								5	-	-					6	-	-	-
	t_{6-2-}	2								-	5	-					-	6	-	-
	t_{6-2-}	2								-	-	5					-	-	6	-
	t_{6-3+}	3								5	-	-					6	-	-	-
	t_{6-3+}	3								-	5	-					-	6	-	-
	t_{6-3+}	3								-	-	5					-	-	6	-
Clock to output (2)	t_{4+2+}	2	2.0	4.7	2.0	4.7	2.0	5.2	ns	5	-	-	-	1,11,16	7,10	8	6	-	-	4
	t_{4+2-}	2								6	-	-	-				5	-	-	
	t_{4+3+}	3								6	-	-	-				5	-	-	
	t_{4+3-}	3								5	-	-	-				6	-	-	
Clock enable time (3)	t_{setup}	6	-	-	2.5	-	-	-	ns	5	-	-	-	1,11,16	7,10	8	6	-	-	4
Clock aperture time (3)	t_{ap}	6	-	-	1.5	-	-	-	ns	5	-	-	-	1,11,16	7,10	8	6	-	-	4
Rise time	t_{2+}	2	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	-	-	4	1,11,16	7,10	8	6	-	-	-
(10% to 90%)	t_{3+}	3	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	-	-	4	1,11,16	7,10	8	6	-	-	-
Fall time	t_{2-}	2	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	-	-	4	1,11,16	7,10	8	6	-	-	-
(10% to 90%)	t_{3-}	3	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	-	-	4	1,11,16	7,10	8	6	-	-	-

NOTES AND MAXIMUM RATINGS

1. Maximum power supply voltages (beyond which device life may be impaired):
   $|V_{CC}| + |V_{EE}| = 12VDC$
2. Unused clock inputs may be tied to ground.
3. See Fig. 10.
4. At all temperatures, $V_{R2} = +4.9000V$ and $V_{R3} = -0.400V$.
5. Storage temperature: -55 °C to +150 °C
6. Operating junction temperature <175 °C

Thermal characteristics

$\theta_{JA} = 107°C/W$
$\theta_{JC} = 31°C/W$



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

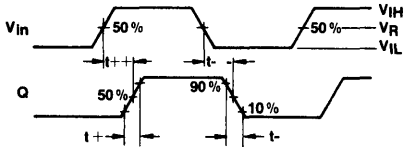
†Refer to Fig.4 for input pulse definitions.

*Complement of output under test should always be loaded with 50-ohms to ground.

Fig.3 Switching time test circuit at +25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

V - INPUT TO OUTPUT

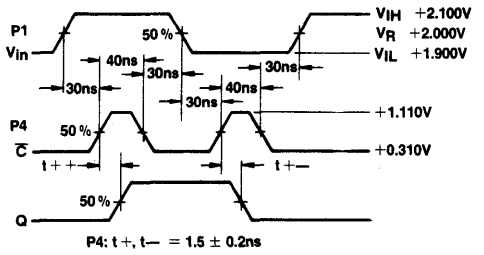


Test Pulses:
t+, t- = 1.5 ± 0.2ns (10% to 90%)
f = 5.0MHz
50% DUTY CYCLE
VIH IS APPLIED TO $\overline{C}$ DURING TESTS

TEST PULSE LEVELS

	Pulse 1	Pulse 2	Pulse 3
V_{IH}	+2.100V	+5.000V	-0.300V
V_R	+2.000V	+4.900V	-0.400V
V_{IL}	+1.900V	+4.800V	-0.500V

Clock to Output



P4: t+, t— = 1.5 ± 0.2ns

Fig.4 Switching and propagation waveforms @ 25°C

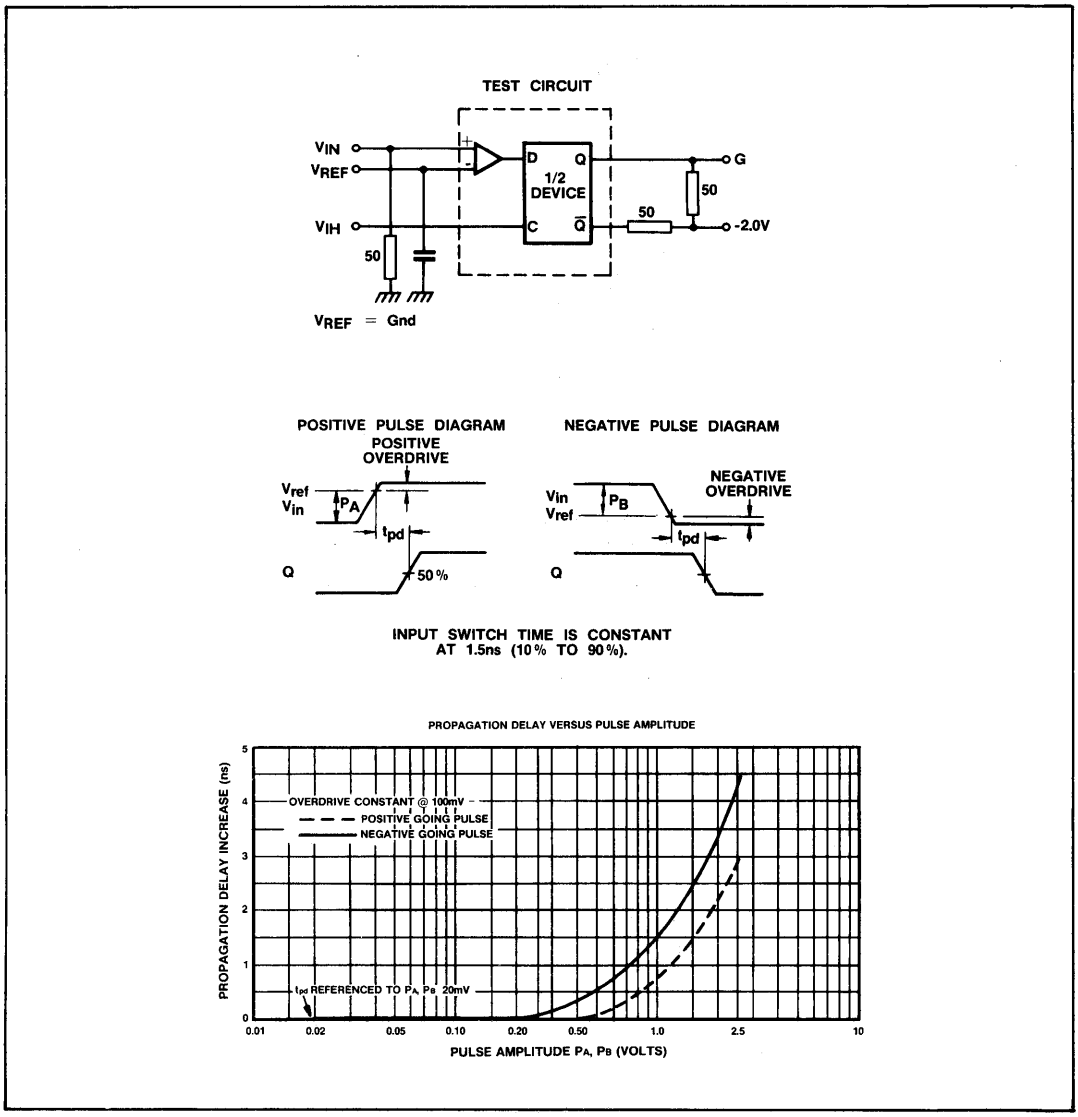


Fig.5 Propagation delay (tpd) v. input pulse amplitude and constant overdrive

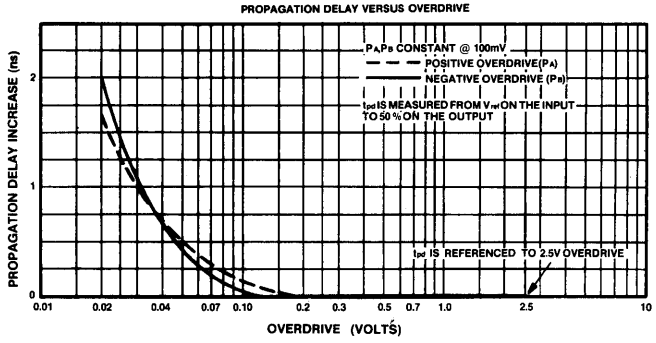


Fig.5 (continued)

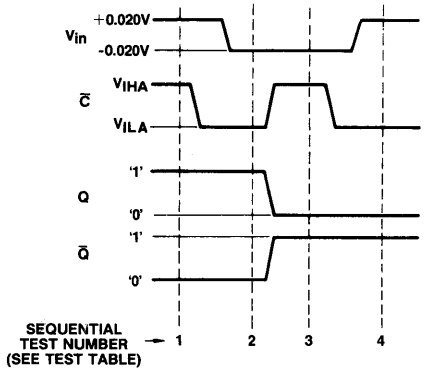


Fig.6 Logic threshold tests (waveform sequence diagram)

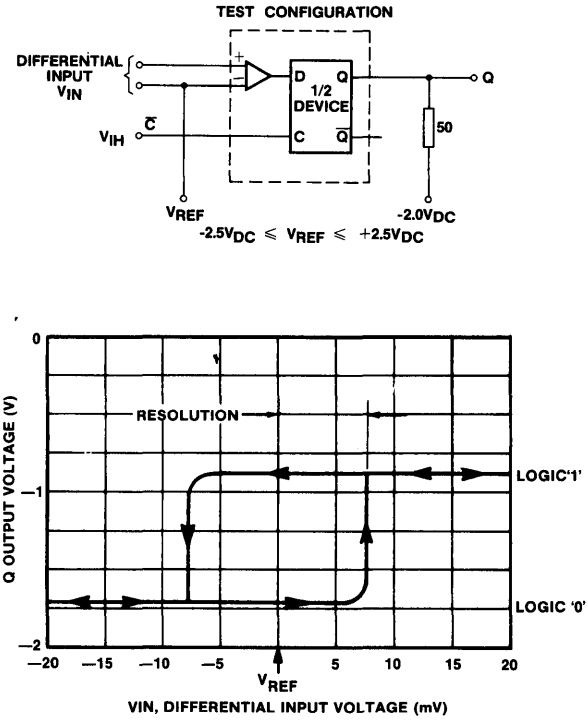


Fig.7 Transfer characteristics (Q v. V_{in})

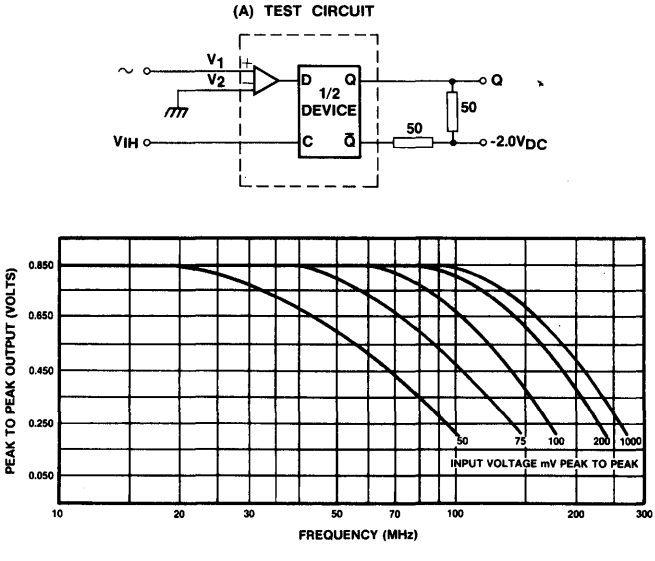
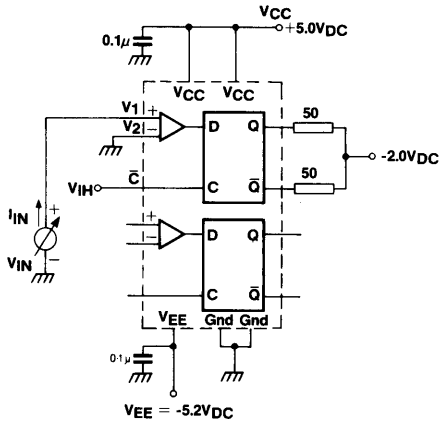


Fig.8 Output voltage swing v. frequency

TEST CIRCUIT



TYPICAL SP1650 (COMPLEMENTARY INPUT GROUNDED)

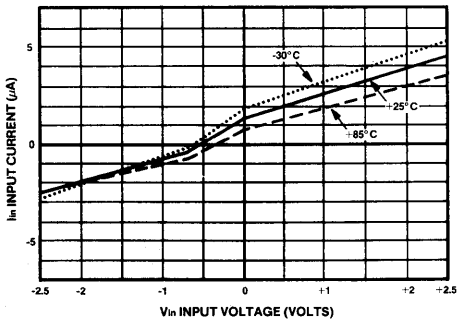
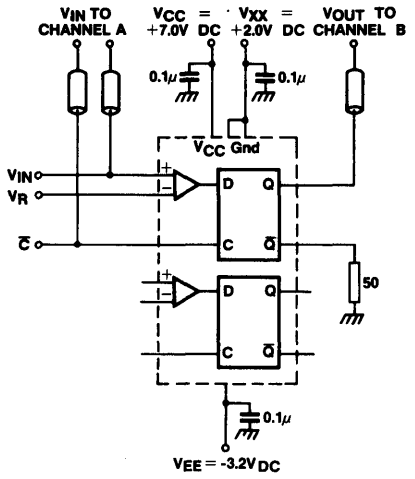


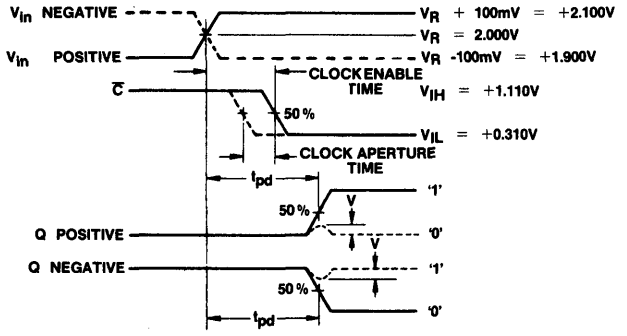
Fig.9 Input current v. input voltage



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

ANALOG SIGNAL POSITIVE AND NEGATIVE SLEW CASE



—— Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200ps.

---- Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150mV.

Fig.10 Clock enable and aperture time test circuit and waveforms @ 25° C

PLESSEY
Semiconductors

SP1658

VOLTAGE-CONTROLLED MULTIVIBRATOR

The SP1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with ECL III and ECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.

The SP1658 is useful in frequency modulation, phase-locked loops, frequency synthesiser and clock signal generation applications for instrumentation, communication and computer systems.

FEATURES

- Operating Temperature Range:
  -30°C to +85°C (Ceramic)
  0°C to +75°C (Plastic)
- Supply Voltages -5.2V, 0V
- Oscillator Frequency Max. 190MHz
- Voltage Controlled

ORDERING INFORMATION

SP1658DP (Commercial - plastic package)
SP1658DG (Commercial - ceramic package)
SP1658BB DG (Plessey High Reliability Specification)
SP1658LC (Under Development) (LCC)

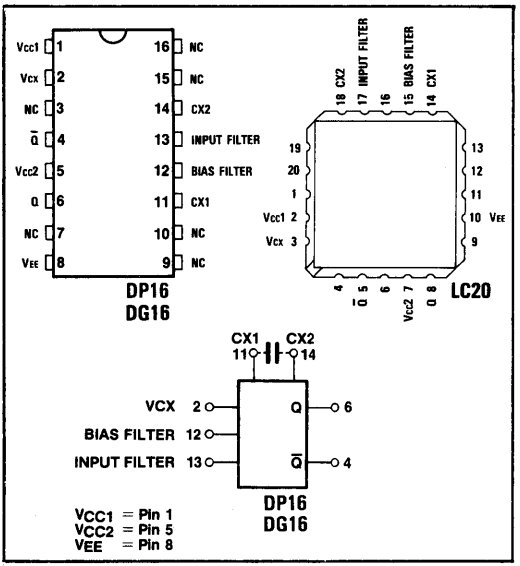


Fig.1 Pin connections(top view)and block diagram

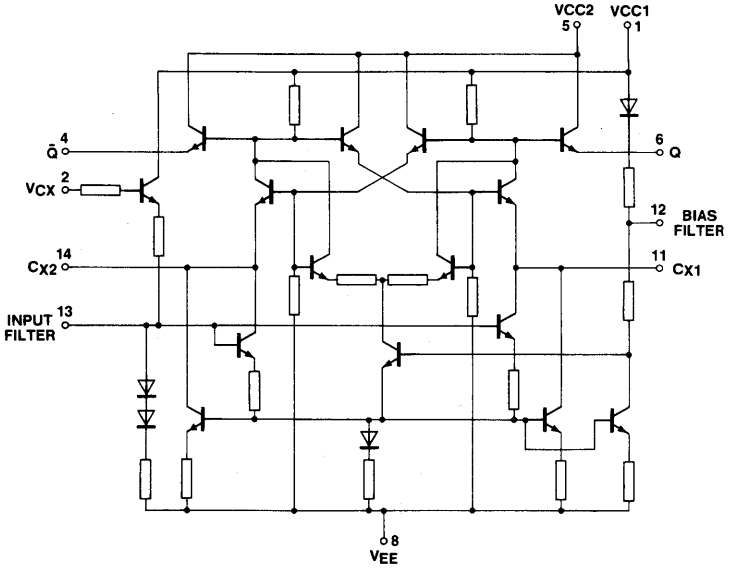


Fig.2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0V.

Test temp.	TEST VOLTAGE (V) V_{CX1}	V_{CX2}	V_{CX3}	V_{EE}
-30°C	0.0	-2.0	-1.0	-5.2
+25°C	-0.0	-2.0	-1.0	-5.2
+85°C	-0.0	-2.0	-1.0	-5.2

Characteristic	Symbol	Pin under test	SP1658 Test Limits -30°C Min.	-30°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+85°C Min.	+85°C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{CX1}	V_{CX2}	V_{CX3}	V_{EE}	V_{CC} (GND)
POWER SUPPLY															
Drain current	I_E	8*	-	-	-	-	32	-	-	mAdc	2	-	-	8	1,5
		8**	-	-	-	-	32	-	-	mAdc	2	-	-	8	1,5
Input current	I_{INH}	2*	-	-	-	-	350	-	-	μAdc	2	-	-	8	1,5
Input leakage current	I_{INL}	2*	-	-	-0.5	-	-	-	-	μAdc	-	2	-	8	1,5
High output voltage Q	V_{OH}	4*	-1.045	-0.875	-0.960	-	-0.810	-0.890	-0.700	Vdc	-	-	2	8	1,5
$\overline{Q}$		6**	-1.045	-0.875	-0.960	-	-0.810	-0.890	-0.700	Vdc	-	-	2	8	1,5
Low output voltage Q	V_{OL}	4**	-1.890	-1.650	-1.850	-	-1.620	-1.830	-1.575	Vdc	-	-	2	8	1,5
$\overline{Q}$		6*	-1.890	-1.650	-1.850	-	-1.620	-1.830	-1.575	Vdc	-	-	2	8	1,5
AC characteristics (Fig.3)											C_{X1}	C_{X2}	V_{CX} +2.0V	V_{EE} -3.2V	V_{CC} +2.0V
Tests shown for one output, but checked on both															
Rise time (10 % to 90 %)	t_+	6	-	3.6	-	-	3.5	-	3.8	ns	-	11,14	2	8	1,5
Fall time (10 % to 90 %)	t_-	6	-	3.1	-	-	3.0	-	3.3	ns	-	11,14	2	8	1,5
Oscillator frequency	f_{osc1}	-	130	-	130	155	190	110	-	MHz	-	11,14	2	8	1,5
	f_{osc2}	-	-	-	78	90	120	-	-	MHz	11,14	-	2	8	1,5
Tuning ratio test †	TR	-	-	-	3.1	4.5	-	-	-	-	11,14	-	-	8	1,5

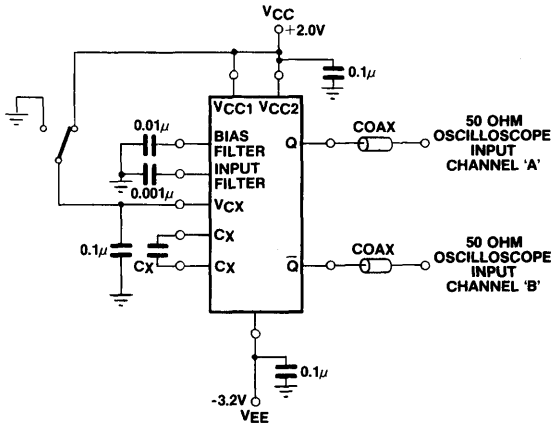
* Germanium diode (0.4 drop) forward biased from 11 to 14 (11 ——▶|—— 14)

**Germanium diode (0.4 drop) forward biased from 14 to 11 (11 ——|◀—— 14)

†TR = $\frac{\text{Output frequency at } V_{CX} = +2.0V}{\text{Output frequency at } V_{CX} = \text{Gnd}}$

CX1 = 10pF connected from pin 11 to pin 14

CX2 = 5pF connected from pin 11 to pin 14



The +2 and -3.2V supplies enable the output load to be connected to ground.

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1 inch from TP_{in} to input pin and TP_{out} to output pin.

Chip capacitors are advised for the input bias filters and supply decoupling.

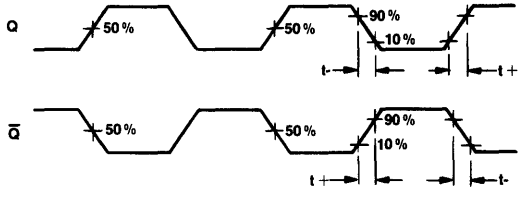


Fig.3 Switching time test circuit and waveforms

ABSOLUTE MAXIMUM RATINGS

Power supply	$\lvert V_{CC} - V_{CC} \rvert$ 8V
Output source current	<40mA
V_{CX} input	-2.5 to V_{CC}
Storage temperature range	-55° C to +150° C (Ceramic and LC)
	-55° C to +125° C (Plastic)
Operating junction temperature	<175° C

Thermal characteristics	
DG16	θ_{JA} = 120° C/W
	θ_{JC} = 40° C/W
LC20	θ_{JA} = 125° C/W
	θ_{JC} = 20° C/W
DP16	θ_{JA} = 180° C/W

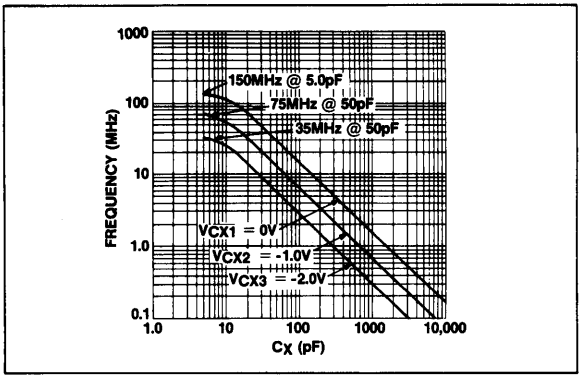


Fig.4 Output frequency v. capacitance for three values of input voltage

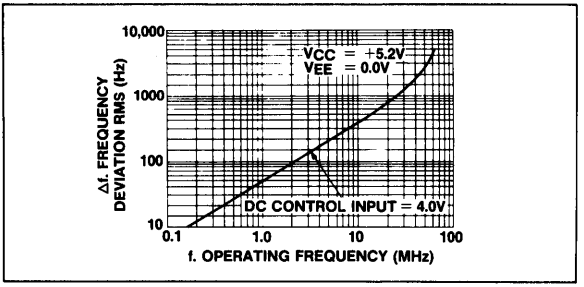


Fig.5 RMS noise deviation v. operating frequency

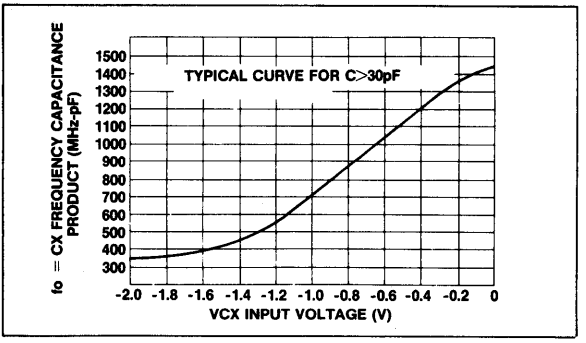


Fig.6 Frequency-capacitance product v. control voltage Vcx

PLESSEY
Semiconductors

SP1660

DUAL 4-INPUT OR/NOR GATE

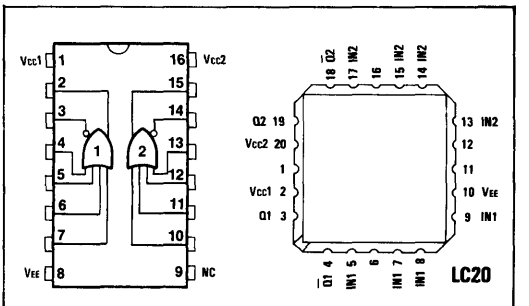
SP1660 provides simultaneous OR-NOR output functions with the capability of driving 50Ω lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (-30°C to +85°C). The input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

FEATURES

- Operating Temperature Range -30°C to +85°C
- Gate Switching Speed 1ns Typ.
- ECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems



DG16

DC Input Loading Factor = 1
DC Output Loading Factor = 70
t_{pd} = 0.9ns typ (510-ohm load)
= 1.1ns typ (50-ohm load)
P_D = 120mW typ/pkg (No load)
Full Load Current, I_L = -25mA dc max.

Fig.1 Logic and pin connections (top view)

ORDERING INFORMATION

SP1660DG (Commercial - Ceramic package)
SP1660BB DG (Plessey High Reliability Specification)
SP1660LC (under development)

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\|V_{CC} - V_{EE}\|$ 8V
Input voltages	0V to V_{EE}
Output source current	<40mA
Storage temperature range	-55°C to +150°C
Junction operating temperature	<+175°C

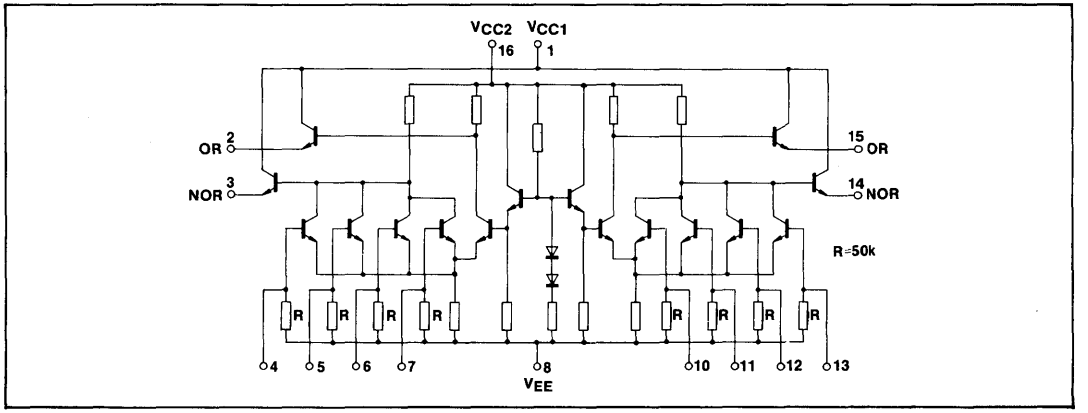


Fig.2 Circuit diagram

Thermal characteristics

DG16	θ_{JA} = 107° C/W
	θ_{JC} = 31° C/W
LC20	θ_{JA} = 147° C/W
	θ_{JC} = 30 °C/W

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50Ω resistor to -2.0V dc.

@ Test Temperature	TEST VOLTAGE VALUES (V) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1660 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Units	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mA	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μA	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μA	–	*	–	–	8	1,16
NOR Logic 1 Output Voltage	V_{OH}	3	-1.045	-0.875	-0.960	-0.810	-1.890	-0.700	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 0 Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 1 Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 0 Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 1 Threshold Voltage	V_{OHA}	3	-1.065	–	-0.980	–	-0.910	–	V	–	–	–	4	8	1,16
				–		–		–		–	–	–	5		
				–		–		–		–	–	–	6		
				–		–		–		–	–	–	7		
NOR Logic 0 Threshold Voltage	V_{OLA}	3	–	-1.630	–	-1.600	–	-1.555	V	–	–	4	–	8	1,16
			–		–		–			–	–	5	–		
			–		–		–			–	–	6	–		
			–		–		–			–	–	7	–		
OR Logic 1 Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	V	–	–	4	–	8	1,16
				–		–		–		–	–	5	–		
				–		–		–		–	–	6	–		
				–		–		–		–	–	7	–		
OR Logic 0 Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	V	–	–	–	4	8	1,16
			–		–		–			–	–	–	5		
			–		–		–			–	–	–	6		
			–		–		–			–	–	–	7		
Switching Times (50Ω Load)										Pulse In	Pulse Out			-3.2V	+2.0V
Propagation Delay	t_{4+3-}	3	–	1.8	–	1.7	–	1.9	ns	4	3	–	–	8	1,16
	t_{4-2-}	2	–	1.8	–	1.7	–	1.9			2	–	–		
	t_{4+2+}	2	–	1.6	–	1.5	–	1.7			2	–	–		
	t_{4-3+}	3	–	1.6	–	1.5	–	1.7			3	–	–		
Rise Time	t_{3+}	3	–	2.2	–	2.1	–	2.3	ns	4	3	–	–	8	1,16
	t_{2+}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{3-}	3	–	2.2	–	2.1	–	2.3	ns	4	3	–	–	8	1,16
	t_{2-}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to the input under test.

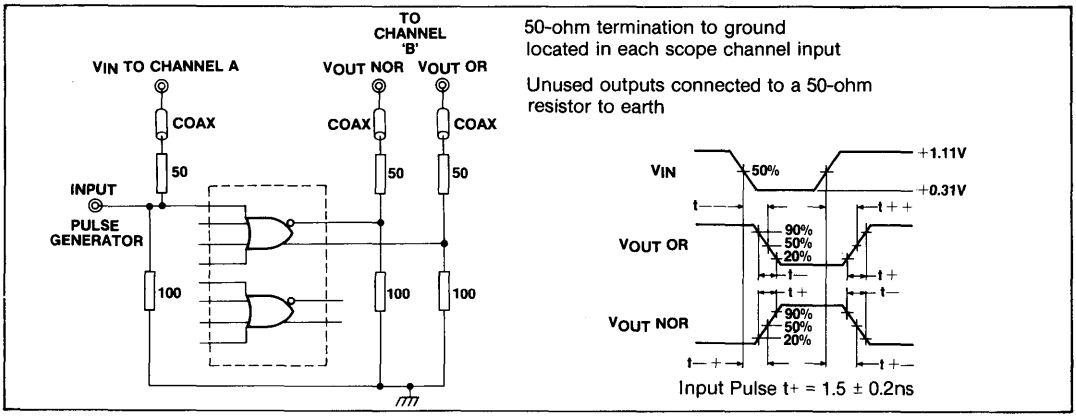


Fig.3 Switching time test circuit and waveforms at +25° C

PLESSEY
Semiconductors

SP1662

QUAD 2-INPUT NOR GATE

The SP1662 comprises four 2-input NOR gating functions in a single package. An internal bias reference voltage ensures that the threshold point remains in the centre of the transition region over the temperature range (0° C to +75° C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

FEATURES

- Gate Switching Speed 1ns Typ.
- ECL II and ECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

ORDERING INFORMATION

SP1662DG (Commercial-ceramic package)

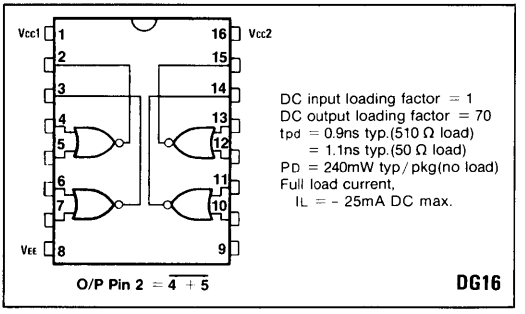


Fig.1 Logic diagram

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\lvert V_{CC} - V_{EE} \rvert$ 8V
Base input voltage	0V to V_{EE}
Output source current	<40mA
Storage temperature range	-55° C to +150° C
Junction operating temperature	<+175° C

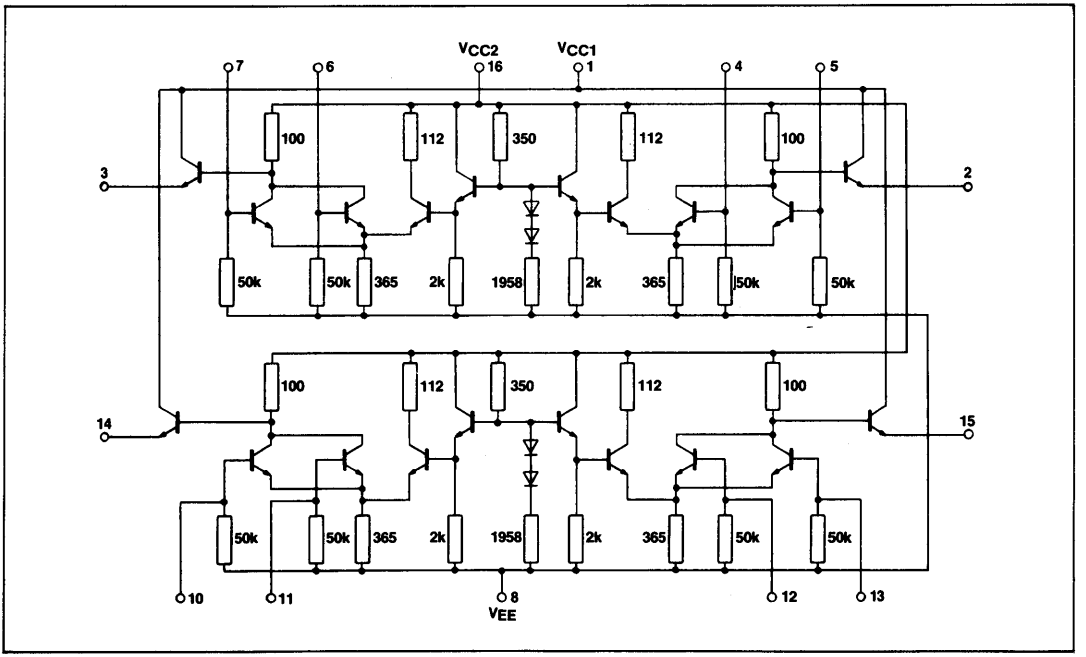


Fig.2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs are tested with a 50Ω resistor to -2.0V dc.

Test temp.	TEST VOLTAGE (V) V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}
0°C	-0.840	-1.870	-1.350		-1.500
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+75°C	-0.720	-1.830	-1.035	-1.460	-5.2

Characteristic	Symbol	Pin under test	SP1662 Test Limits 0°C Min.	0°C Max.	+25°C Min.	+25°C Max.	+75°C Min.	+75°C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}	GND
POWER SUPPLY															
Drain current	I_E	8	-	-	-	56	-	-	mA	-	-	-	-	8	1,16
Input current	I_{INH}	*	-	-	-	350	-	-	μA	*	-	-	-	8	1,16
	I_{INL}	*	-	-	0.5	-	-	-	μA	-	*	-	-	8	1,16
Logic '1' output voltage	V_{OH}	2	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	V	-	4	-	-	8	1,16
		2	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	V	-	5	-	-	8	1,16
Logic '0' output voltage	V_{OL}	2	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	V	4	-	-	-	8	1,16
		2	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	V	5	-	-	-	8	1,16
Logic '0' threshold voltage	V_{OHA}	2	-1.020	-	-0.980	-	-0.920	-	V	-	-	-	4	8	1,16
		2	-1.020	-	-0.980	-	-0.920	-	V	-	-	-	5	8	1,16
Logic '0' threshold voltage	V_{OLA}	2	-	-1.615	-	-1.600	-	-1.575	V	-	-	4	-	8	1,16
		2	-	-1.615	-	-1.600	-	-1.575	V	-	-	5	-	8	1,16
SWITCHING TIME (50 ohm load)			Typ.	Max.	Typ.	Max.	Typ.	Max.		Pulse in	Pulse out			-3.2V	+2.0V
Propagation delay	t_{4-2-}	2	1.0	1.5	1.0	1.5	1.1	1.7	ns	4	2	-	-	8	1,16
	t_{4+2+}	2	1.1	1.7	1.1	1.7	1.2	1.9	ns	4	2	-	-	8	1,16
Rise time	t_{2+}	2	1.4	2.1	1.4	2.1	1.5	2.3	ns	4	2	-	-	8	1,16
Fall time	t_{2-}	2	1.2	2.1	1.2	2.1	1.3	2.3	ns	4	2	-	-	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to input under test.

Thermal characteristics θ_{JA} = 120° C/W
θ_{JC} = 40° C/W

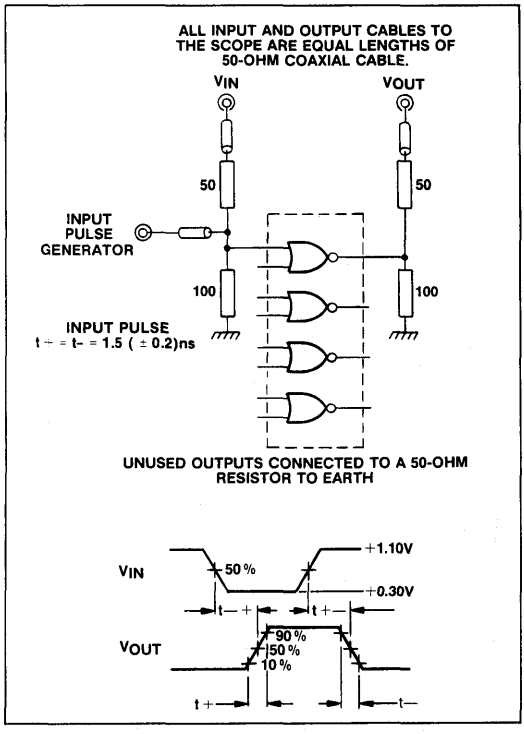


Fig.3 Switching time test circuit and waveforms at + 25 °C

PLESSEY
Semiconductors

SP1664

QUAD 2-INPUT OR GATE

The SP1664 comprises four 2-input OR gating functions in a single package. An internal bias reference voltage ensures that the threshold point remains in the centre of the transition region over the temperature range (0° C to +75° C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

FEATURES

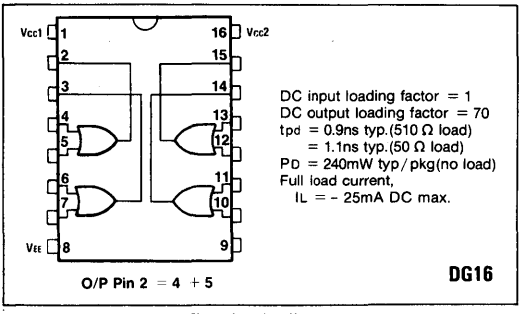
- Gate Switching Speed 1ns Typ.
- ECL II and ECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation with Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

ORDERING INFORMATION

SP1664DG (Commercial-ceramic package)



DC input loading factor = 1
DC output loading factor = 70
tpd = 0.9ns typ.(510 Ω load)
= 1.1ns typ.(50 Ω load)
PD = 240mW typ/pkg(no load)
Full load current,
IL = - 25mA DC max.

Fig.1 Logic diagram

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\lvert V_{CC} - V_{EE} \rvert$ 8V
Base input voltage	0V to V_{EE}
Output source current	<40mA
Storage temperature range	-55° C to +150° C
Junction operating temperature	< +175° C

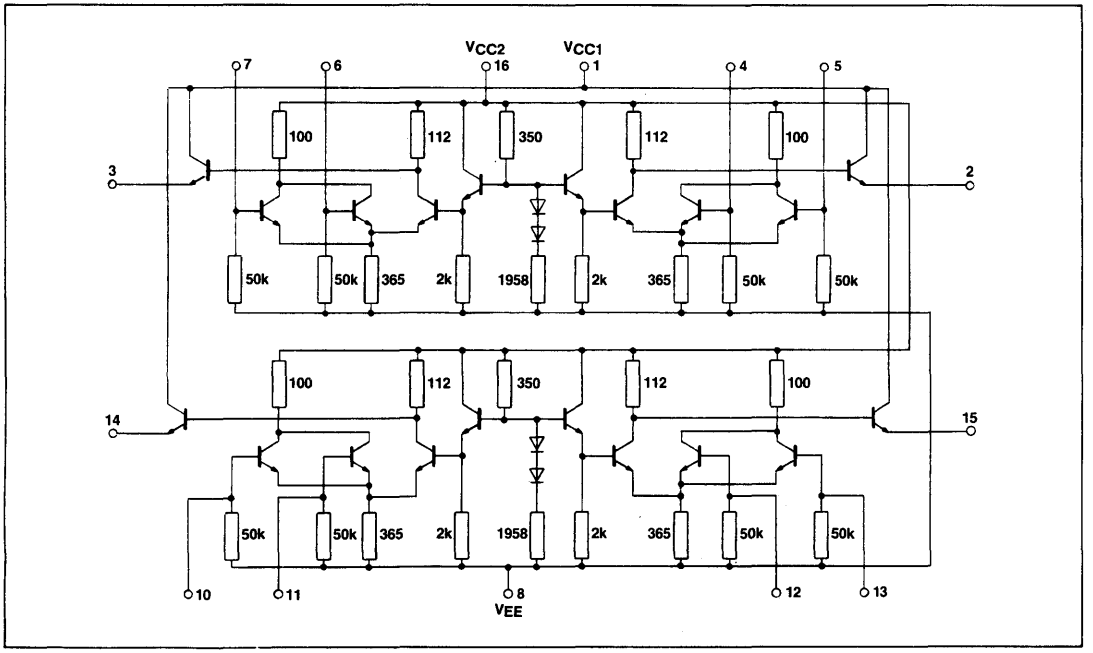


Fig.2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs are tested with a 50Ω resistor to -2.0V dc.

Test temp.	TEST VOLTAGE (V) V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}
0°C	-0.840	-1.870	-1.350	-1.500	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+75°C	-0.720	-1.830	-1.035	-1.460	-5.2

Characteristic	Symbol	Pin under test	SP1664 Test Limits 0°C Min.	0°C Max.	+25°C Min.	+25°C Max.	+75°C Min.	+75°C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}	GND
POWER SUPPLY															
Drain current	I_E	8	-	-	-	56	-	-	mA	-	-	-	-	8	1,16
Input current	I_{INH}	*	-	-	-	350	-	-	μA	*	-	-	-	8	1,16
	I_{INL}	*	-	-	0.5	-	-	-	μA	-	*	-	-	8	1,16
Logic '1' output voltage	V_{OH}	2	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	V	4	-	-	-	8	1,16
		2	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	V	5	-	-	-	8	1,16
Logic '0' output voltage	V_{OL}	2	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	V	-	4	-	-	8	1,16
		2	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	V	-	5	-	-	8	1,16
Logic '0' threshold voltage	V_{OHA}	2	-1.020	-	-0.980	-	-0.920	-	V	-	-	4	-	8	1,16
		2	-1.020	-	-0.980	-	-0.920	-	V	-	-	5	-	8	1,16
Logic '0' threshold voltage	V_{OLA}	2	-	-1.615	-	-1.600	-	-1.575	V	-	-	-	4	8	1,16
		2	-	-1.615	-	-1.600	-	-1.575	V	-	-	-	5	8	1,16
SWITCHING TIME (50 ohm load)			Typ.	Max.	Typ.	Max.	Typ.	Max.		Pulse in	Pulse out			-3.2V	+2.0V
Propagation delay	t_{4-2-}	2	1.0	1.5	1.0	1.5	1.1	1.7	ns	4	2	-	-	8	1,16
	t_{4-2+}	2	1.1	1.7	1.1	1.7	1.2	1.9	ns	4	2	-	-	8	1,16
Rise time	t_{2-}	2	1.5	2.1	1.5	2.1	1.6	2.3	ns	4	2	-	-	8	1,16
Fall time	t_{2+}	2	1.4	2.1	1.4	2.1	1.5	2.3	ns	4	2	-	-	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

Thermal characteristics θ_{JA} = 120° C/W
θ_{JC} = 40° C/W

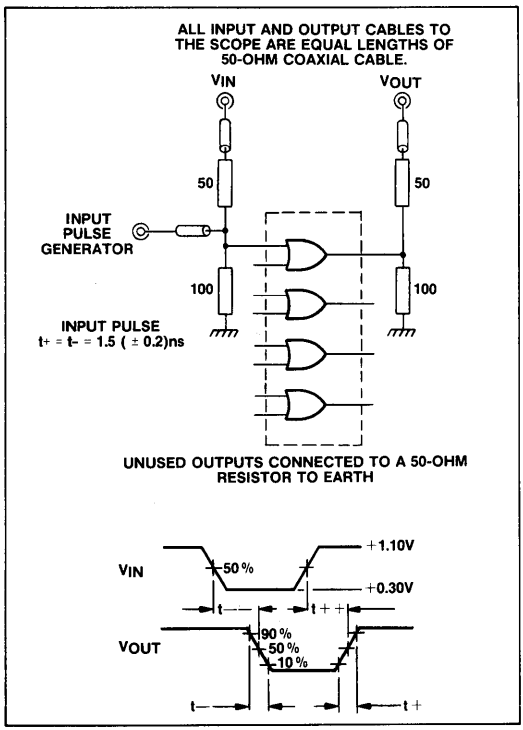


Fig.3 Switching time test circuit and waveforms at + 25 °C

PLESSEY
Semiconductors

SP1670

MASTER/SLAVE TYPE D FLIP-FLOP

The SP1670 is a D-type Master-Slave Flip-Flop designed for use in high speed digital applications. Master-slave construction renders the SP1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

When both clock inputs (C1 and C2) are in the low state, the data input affects only the Master portion of the flip-flop. The data present in the Master is transferred to the Slave when clock inputs (C1 OR C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 OR C2 is in the high state the Master (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

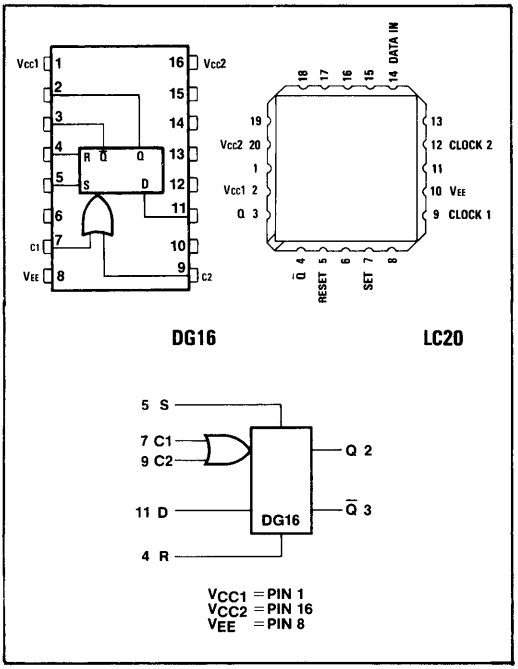


Fig.1(a) DG package Fig.1(b) LC package Fig.1(c) Logic diagram

FEATURES

- Operating Temperature Range -30°C to +85°C
- Toggle Frequency 300MHz
- ECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

ORDERING INFORMATION

SP1670DG (Commercial - ceramic package)
SP1670LC (Under Development)

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\lvert V_{CC} - V_{EE} \rvert$ 8V
Input voltages	V_{CC} to V_{EE}
Output source current	<40mA
Storage temperature range	-55°C to +150°C
Operating junction temperature	<175°C

TRUTH TABLE

R	S	D	C	$Q_n + 1$
L	H	Φ	Φ	H
H	L	Φ	Φ	L
H	H	Φ	Φ	ND
L	L	L	L	Q_n
L	L	L		L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H		H
L	L	H	H	Q_n

Φ = Don't Care
ND = Not Defined
C = C1 + C2

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifictions shown in the characteristics table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0V.

Test temp.	TEST VOLTAGE (V) V_{IH} Max.	V_{IL} Min.	V_{IHA} Max.	V_{ILA} Max.	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin under test	SP1670 Test Limits -30°C Min.	-30°C Max.	+25°C Min.	+25°C Max.	+85°C Min.	+85°C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}	P_1	P_2	P_3	V_{CC} Gnd
POWER SUPPLY																		
Drain current	I_E	8	-	-	-	48	-	-	mAdc	7,9	-	-	-	8	-	-	-	1,16
Input current	I_{INH}	4	-	-	-	550	-	-	µAdc	4	-	-	-	8	-	-	-	1,16
		5	-	-	-	550	-	-		5	-	-	-		-	-	-	
		9	-	-	-	250	-	-		9	-	-	-		-	-	-	
		7	-	-	-	250	-	-		7	-	-	-		-	-	-	
		11	-	-	-	270	-	-		11	-	-	-		-	-	-	
	I_{INL}	4	-	-	0.5	-	-	-	µAdc	9	4	-	-	8	-	-	-	1,16
		5	-	-		-	-	-		9	5	-	-		-	-	-	
		9	-	-		-	-	-		7	9	-	-		-	-	-	
		7	-	-		-	-	-		9	7	-	-		-	-	-	
		11	-	-		-	-	-		9	11	-	-		-	-	-	
Logic '1' output voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	-	4,7,11	-	-	8	9	5	-	1,16
		3								11	5,9	-	-		7	4	-	
		2								11	5,7	-	-		4	9	-	
		3								-	4,9,11	-	-		5	7	-	
Logic '0' output voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	11	5,7	-	-	8	9	4	-	1,16
		3								-	4,9,11	-	-		7	5	-	
		2								-	4,7,11	-	-		5	9	-	
		3								11	5,9	-	-		4	7	-	
Logic '1' threshold voltage	V_{OHA}	2	-1.065	-	-0.980	-	-0.910	-	Vdc	4,7,11	-	-	8	9	-	5	1,16	
		3		-		-		-		11	5,9	-	-		7	-	4	
		2		-		-		-		11	5,7	-	-		4	-	9	
		3		-		-		-		-	4,9,11	-	-		5	-	7	
		2		-		-		-		-	5,7	11	-		4	9	-	
		3		-		-		-		-	4,9	-	11		5	7	-	
Logic '0' threshold voltage	V_{OLA}	2	-	-1.630	-	1.600	-	1.555	Vdc	11	5,7	-	-	8	9	-	4	1,16
		3	-		-		-			-	4,9,11	-	-		7	-	5	
		2	-		-		-			-	4,7,11	-	-		5	-	9	
		3	-		-		-			11	5,9	-	-		4	-	7	
		2	-		-		-			-	4,7	-	11		5	9	-	
		3	-		-		-			-	5,9	11	-		4	7	-	
														-3.2 Vdc				+2.0 Vdc
Switching parameters																		
Clock to output delay	t_{9-2}	9,2	1.0	2.7	1.1	2.5	1.1	2.9	ns	-	-	-	-	8	-	-	-	1,16
(See Fig.1)	t_{9-2}	9,2								-	-	-	-		-	-	-	
	t_{9-3}	9,3								-	-	-	-		-	-	-	
	t_{9-3}	9,3								-	-	-	-		-	-	-	
Set to output delay	t_{5-2}	5,2								-	-	-	-		-	-	-	
(See Fig.2)	t_{5-3}	5,3								-	-	-	-		-	-	-	
Reset to output delay	t_{4-2}	4,2								-	-	-	-		-	-	-	
(See Fig.2)	t_{4-3}	4,3								-	-	-	-		-	-	-	
Output																		
Rise time	t_{2-}, t_{3-}	2,3	0.9	2.7	1.0	2.5	1.0	2.9		-	-	-	-		-	-	-	
Fall time (See Fig.2)	t_{2-}, t_{3-}	2,3	0.5	2.1	0.6	1.9	0.6	2.3		-	-	-	-		-	-	-	
Set up time	t_S '1'	2	-	-	-	0.4	-	-		-	-	-	-		-	-	-	
(See Fig.3)	t_S '0'	2	-	-	-	0.5	-	-		-	-	-	-		-	-	-	
Hold time	t_H '1'	2	-	-	-	0.3	-	-		-	-	-	-		-	-	-	
(See Fig.3)	t_H '0'	2	-	-	-	0.5	-	-		-	-	-	-		-	-	-	
Toggle frequency	f_{TOG}	2	270	-	300	-	270	-	MHz	-	-	-	-		-	-	-	-
(See Fig.4)																		

Thermal characteristics

DG16 θ_{JA} = 107° C/W
θ_{JC} = 31° C/W

LC20 θ_{JA} = 147° C/W
θ_{JC} = 30° C/W

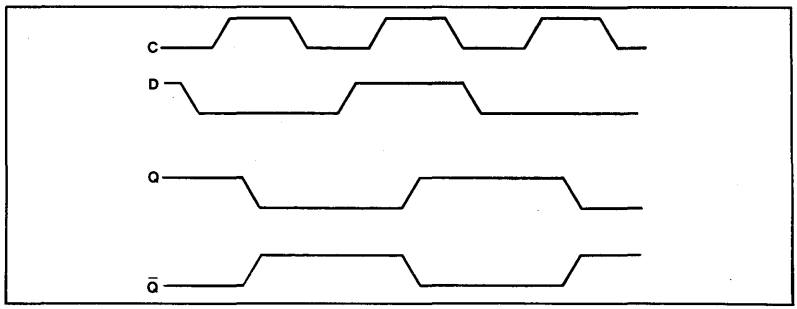


Fig.2 Timing diagram

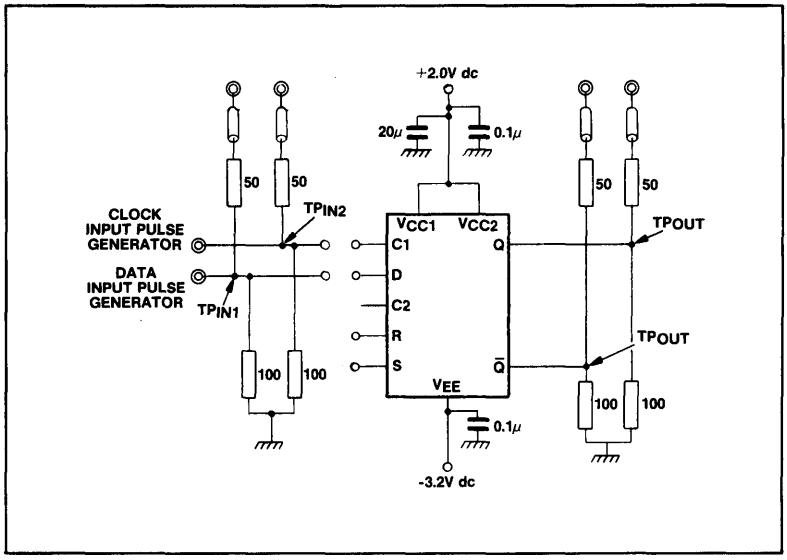


Fig.3 Propagation delay test circuit

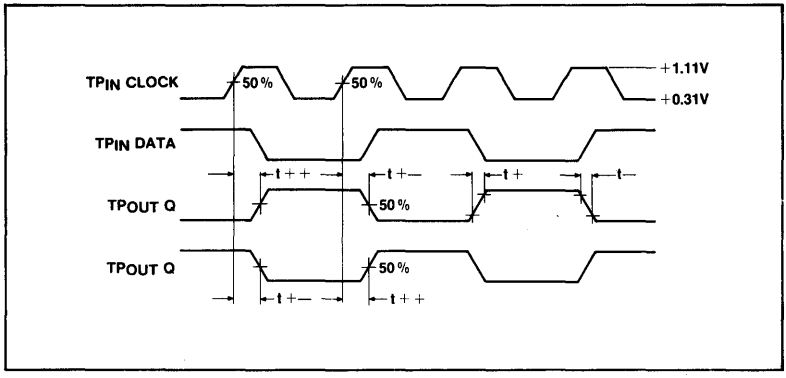


Fig.4 Clock delay waveforms at +25°C

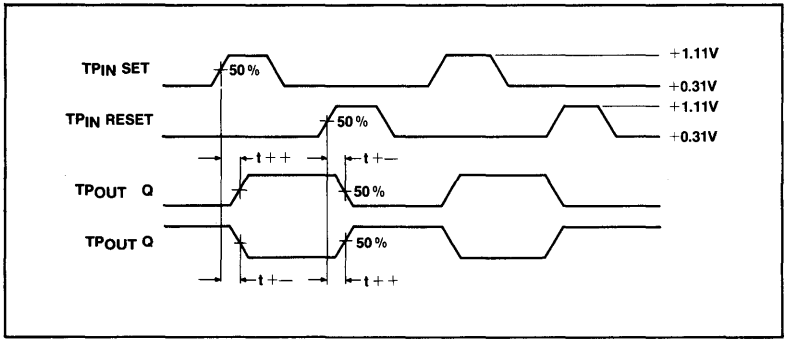


Fig.5 Set/reset delay waveform at +25°C

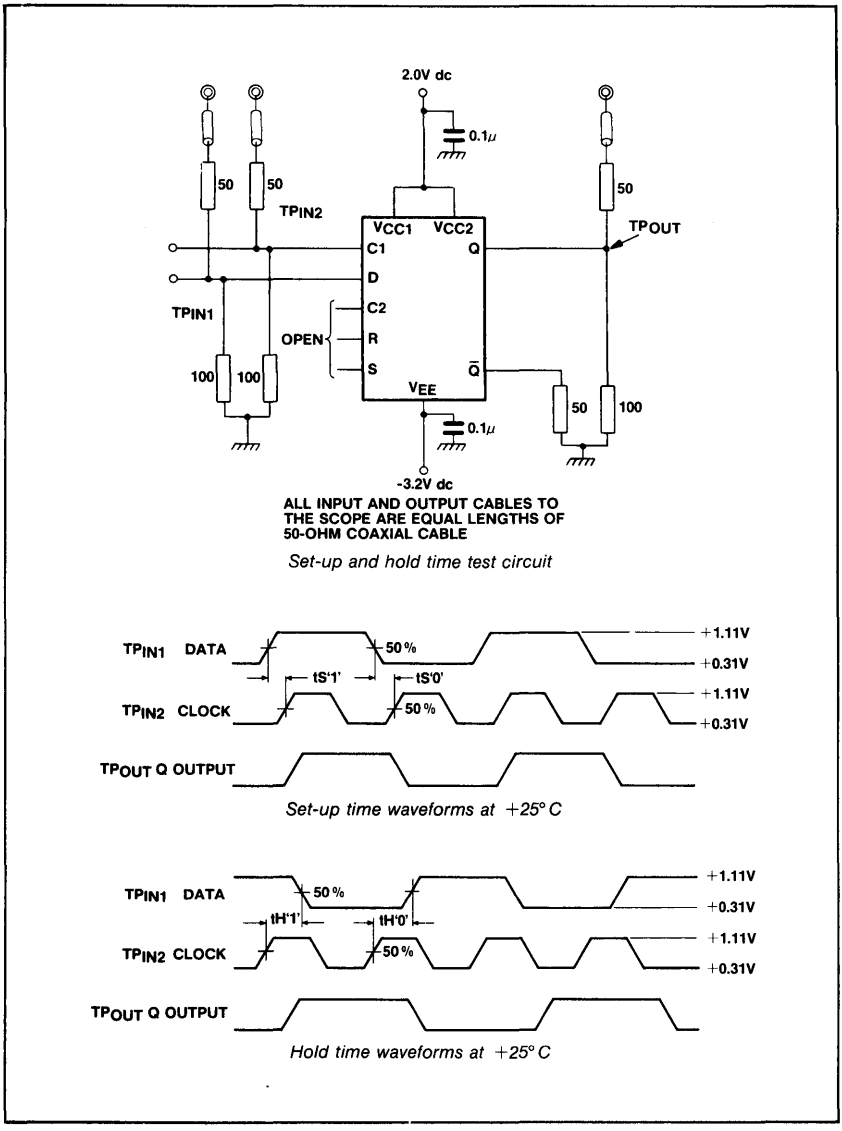


Fig.6 Set-up and hold time test circuit

Set up time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.

Hold time is the minimum time after the positive transition of the clock (C) that information must remain unchanged at the data (D) input.

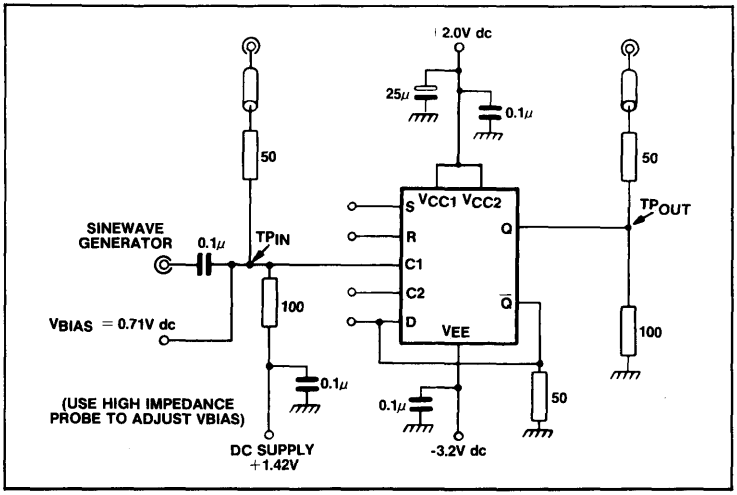


Fig.7 Toggle frequency test circuit

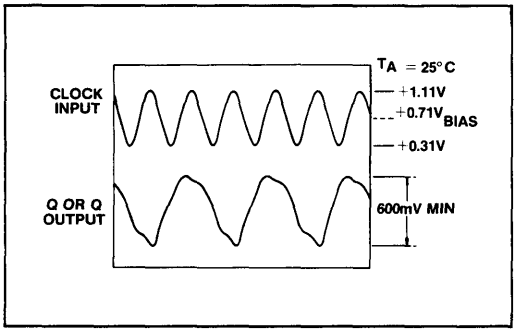


Fig.8 Toggle frequency waveforms

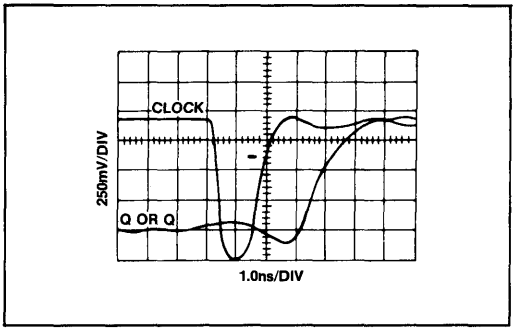


Fig.9 Minimum 'down time' to clock (Output load = 50Ω)

The maximum toggle frequency of the SP1670 has been exceed when either:

1. The output peak-to-peak voltage swing falls below 600mV OR
2. The device ceases to toggle (divide by two). V_{Bias} is defined by the test circuit Fig.7 and by the waveform in Fig.8.

Figs.9 and 10 illustrate minimum clock pulse width recommended for reliable operation of the SP1670.

Temperature	-30°C	+25°C	+85°C
V_{Bias}	+0.660V	+0.710V	+0.765V

Table 1 Variation of V_{Bias} with temperature

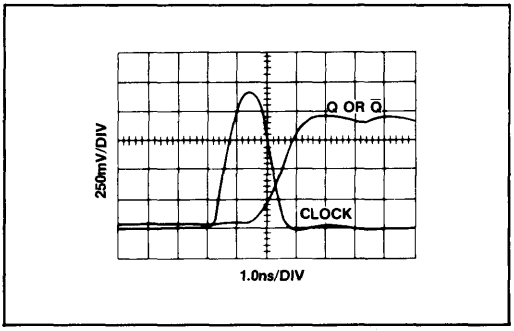


Fig.10 Minimum 'up time' to clock (Output load = 50Ω)

Operation of the Master-Slave Type D Flip-Flop

In the circuit of Fig.11 assume that initially Q, C, R, S and D are at 0 levels and that Q is at the 1 level. Since the clock is low, transistors TR3 and TR22 are conducting. In the slave section only transistors TR25 and TR26 are in series with TR22. The output of the slave section is fed back to these two transistors in order to form a latch. Thus, when the clock is low, the output state of the slave is maintained. In the master section, the current path is through TR3 and TR9.

Now assume that the data input goes high. The high-input signal on the base of TR4 causes it to conduct, and TR9 to turn off. The voltage drop across resistor RC1 causes a low-state voltage on the base and therefore on the emitter of TR11. Since there is essentially no current flow through RC2, the base of transistor TR10 is in a high state. This is reflected in the emitter, and in turn is transferred to the base of TR6. TR6 is biased for conduction but, since there is no current path, does not conduct.

Now allow the clock to go high. As the clock signal rises, transistor TR2 turns on and transistor TR3 turns off. This provides a current path for the common-emitter transistors TR5, TR6, TR7 and TR8. Since the bases of all these devices except TR6 are in the low state, current flow is through TR6. This maintains the base and emitter of TR11 low, and the base and emitter of TR10 high. The high state on TR10 is transferred to TR23 of the slave section. As the clock continues to rise TR21 begins to turn on and TR22 to turn off. (Reference voltages in the master and slave units are slightly offset to ensure prior clocking of the master section.) With transistor TR21 conducting and the base of TR23 in a high state, the current path now includes TR21, TR23, and resistor RC3. The voltage drop across the resistor places a low state voltage on the base, and therefore the emitter, of TR30. The lack of current flow through RC4 causes a high state input to the base of TR29. These states are fed back to the latch transistors, TR25 and TR26.

As the clock voltage falls, transistor TR21 turns off and TR22 turn on. This provides a current path through the latch transistors, locking-in the slave output.

In the master section the falling clock voltage turns on transistor TR3 and turns off TR2. This enables the input transistor TR4 so that the master section will again track the D input.

The separation of thresholds between the master and slave flip-flops is caused by R8. The current through this resistor produces an offset between the thresholds of the transistor pairs TR2:TR3 and TR21:TR22. This offset disables the D input of the master flip-flop prior to the enabling of the information transfer from master to slave via transistors TR23 and TR28. This disabling operation prevents false information from being transferred directly from master to slave during the clock transition, particularly if the D input changes at this time (such as in a counting operation where the Q output is tied back to D). The offsetting resistor also allows a relatively slow-rising clock wveform to be used without the danger of losing information during the transition of the clock.

The set and reset inputs are symmetrically connected. Therefore, their action is similar although results are opposite. As a logic 1 level is applied to the S input transistor, TR2 begins to conduct because its base is now being driven through TR19 which is in turn connected to S. Transistor TR5 is now on and the feedback devices TR6 and TR7 latch this information into the master flip-flop. A similar action takes place in the slave with transistors TR21, TR24, TR25, and TR26.

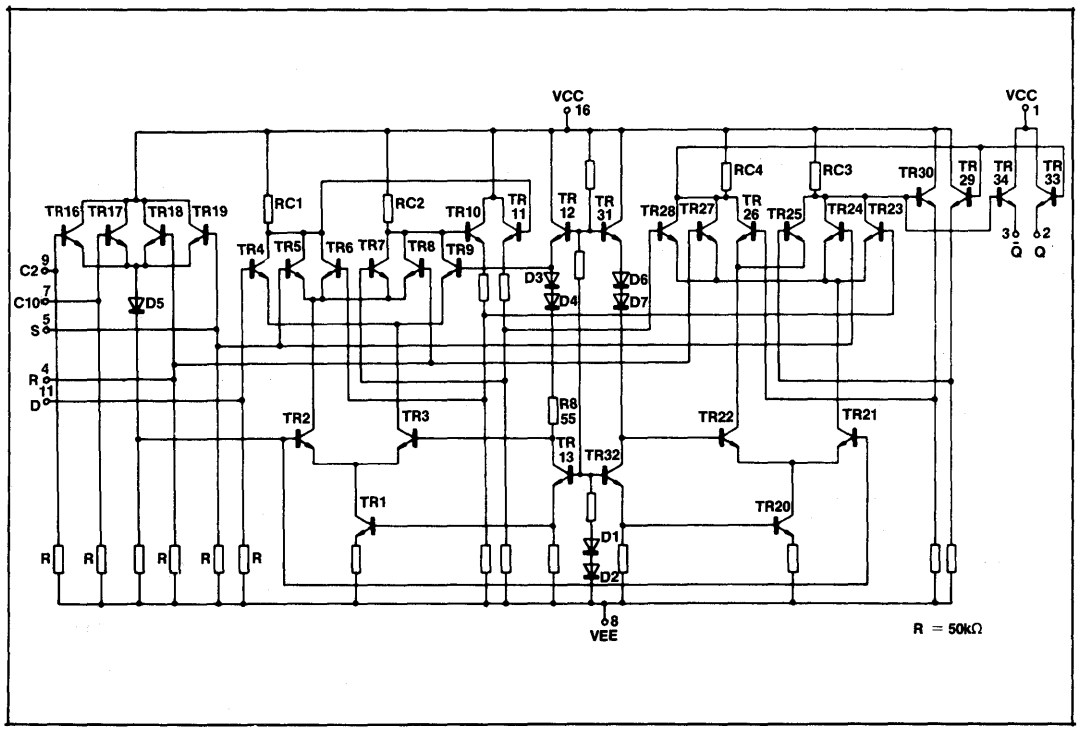


Fig.11 SP1670 circuit diagram

PLESSEY
Semiconductors

SP1672

TRIPLE 2-INPUT EXCLUSIVE-OR GATE

This three gate ECL array is designed to provide the positive logic Exclusive-OR function in high speed applications. These devices contain a temperature compensated internal bias which ensures that the threshold point remains in the centre of the transition region over the temperature range (0° C to +75° C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

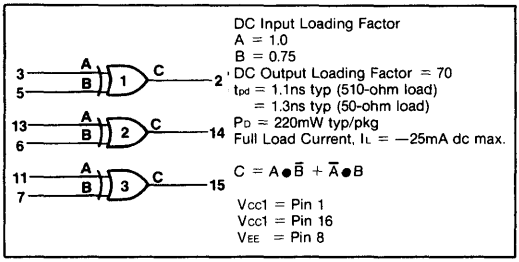


Fig.1 Logic diagram of SP1672

ORDERING INFORMATION

SP1672DG (Commercial-ceramic package)

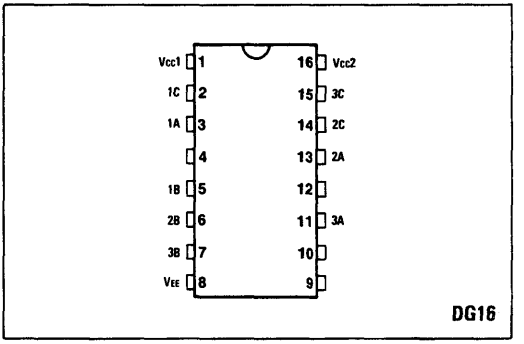


Fig.2 Pin connections (top view)

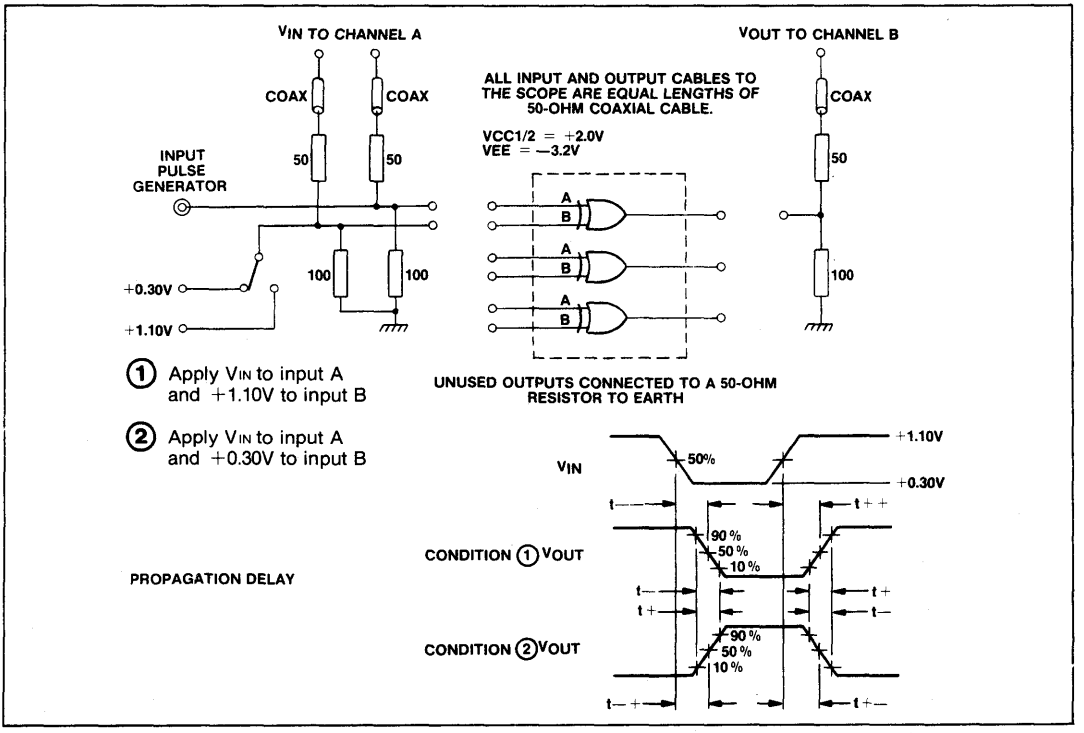


Fig.3 Switching time test circuit and waveforms at +25° C

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Outputs are tested with a 50Ω resistor to -2.0V dc.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	| V_{CC} - V_{EE}| 8V
Input voltages	V_{CC} to V_{EE}
Output source current	<40mA
Storage temperature range	-55° C to +150° C

Thermal characteristics
DG16
θ_{JA} = 107° C/W
θ_{JC} = 31° C/W

Test temp.	TEST VOLTAGE (V) V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}
0° C	-0.840	-1.870	-1.350		-1.500
+25° C	-0.810	-1.850	-1.095	-1.485	-5.2
+75° C	-0.720	-1.830	-1.035	-1.460	-5.2

Characteristic	Symbol	Pin under test	SP1672 Test Limits 0° C Min.	0° C Max.	+25° C Min.	+25° C Max.	+75° C Min.	+75° C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}	GND
POWER SUPPLY															
Drain current	I_E	8	-	-	-	55	-	-	mAdc	All inputs	-	-	-	8	1,16
Input current	I_{INH}	3,11,13	-	-	-	350	-	-	μAdc	*	-	-	-	8	1,16
	0.75 I_{INH}	5,6,7	-	-	-	270	-	-	μAdc	*	-	-	-	8	1,16
	I_{INL}	*	-	-	0.5	-	-	-	μAdc	-	*	-	-	8	1,16
Logic '1' output voltage	V_{OH}	2	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	3	5	-	-	8	1,16
		2	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	5	3	-	-	8	1,16
Logic '0' output voltage	V_{OL}	2	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	3,5	-	-	-	8	1,16
		2	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	-	3.5	-	-	8	1,16
Logic '0' threshold voltage	V_{OHA}	2	-1.020	-	-0.980	-	-0.920	-	Vdc	-	-	3	5	8	1,16
		2	-1.020	-	-0.980	-	-0.920	-	Vdc	-	-	5	3	8	1,16
Logic '0' threshold voltage	V_{OLA}	2	-	-1.615	-	-1.600	-	-1.575	Vdc	-	-	3,5	-	8	1,16
		2	-	-1.615	-	-1.600	-	-1.575	Vdc	-	-	-	3,5	8	1,16
SWITCHING TIME (50 ohm load)			**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**			-	**Pulse in**	**Pulse out**	**-3.2V**	**+2.0V**
Propagation delay	t_{3+2+}	2	1.3	1.8	1.3	1.8	1.5	2.2	ns	-	-	3	2	8	1,16
	t_{3-2+}	2	1.3	1.8	1.3	1.8	1.5	2.2		-	-				
	t_{3+2-}	2	1.4	1.9	1.4	1.9	1.6	2.3		-	-				
	t_{3-2-}	2	1.4	1.9	1.4	1.9	1.6	2.3		-	-				
	t_{5+5+}	2	1.7	2.3	1.7	2.3	1.9	2.7		-	-	5			
	t_{5-2+}	2								-	-				
	t_{5+2-}	2								-	-				
	t_{5-2-}	2								-	-				
Rise time	t_{2+}	2	1.9	2.5	1.9	2.5	2.1	2.8	ns	-	-	3	2	8	1,16
Fall time	t_{2-}	2	1.6	2.2	1.6	2.2	1.8	2.5	ns	-	-	3	2	8	1,16

PLESSEY
Semiconductors

SP1674

TRIPLE 2-INPUT EXCLUSIVE-NOR GATE

This three gate ECL array is designed to provide the positive logic Exclusive-NOR function in high speed applications. These devices contain a temperature compensated internal bias which ensures that the threshold point remains in the centre of the transition region over the temperature range (0° C to +75° C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

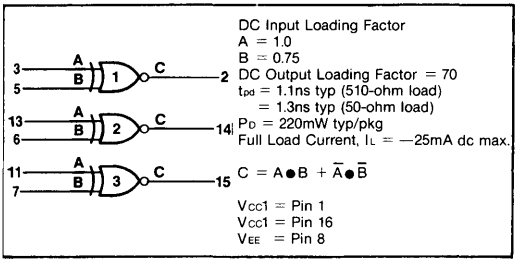


Fig.1 Logic diagram of SP1674

ORDERING INFORMATION

SP1674DG (Commercial-ceramic package)

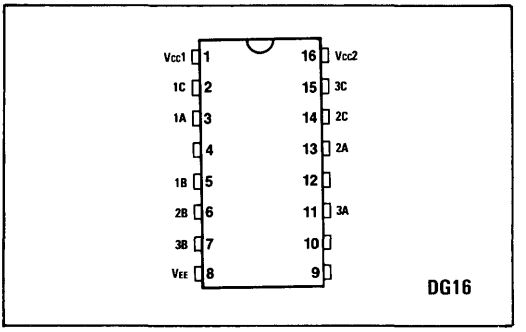


Fig.2 Pin connections (top view)

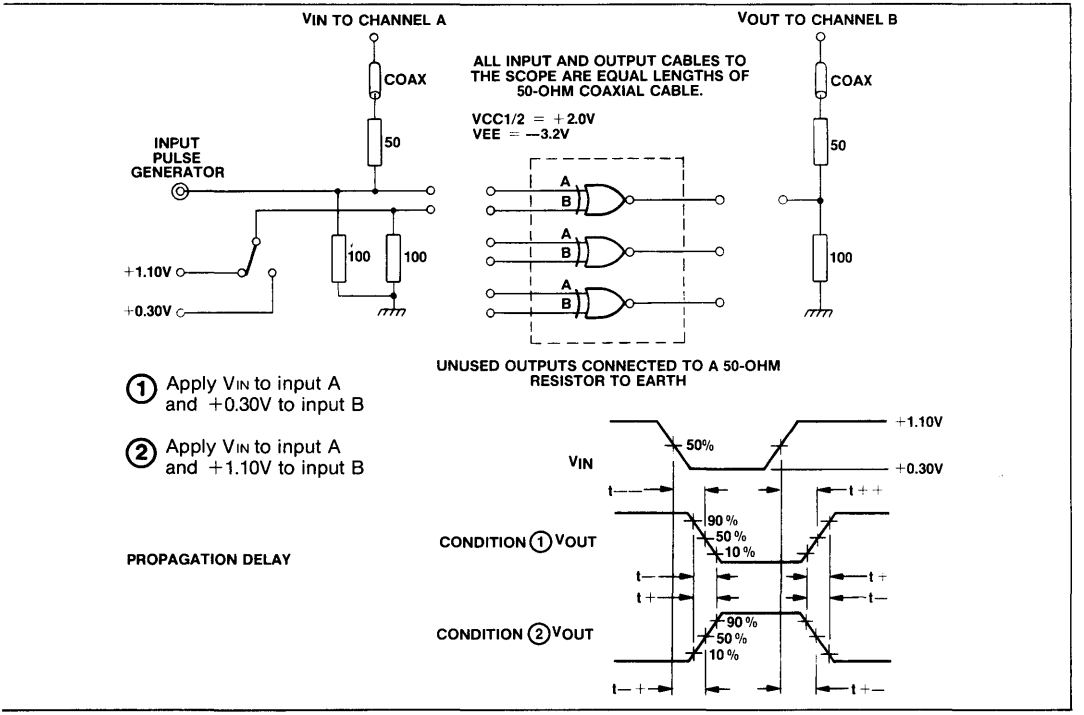


Fig.3 Switching time test circuit and waveforms at +25° C

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Outputs are tested with a 50Ω resistor to -2.0V dc.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\lvert V_{CC} - V_{EE} \rvert$ 8V
Input voltages	V_{CC} to V_{EE}
Output source current	<40mA
Storage temperature range	-55° C to +150° C

Thermal characteristics
DG16
θ_{JA} = 107° C/W
θ_{JC} = 31° C/W

Test temp.	TEST VOLTAGE (V) V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}
0° C	-0.840	-1.870	-1.350	-1.500	-5.2
+25° C	-0.810	-1.850	-1.095	-1.485	-5.2
+75° C	-0.720	-1.830	-1.035	-1.460	-5.2

Characteristic	Symbol	Pin under test	SP1674/SP1675 Test Limits 0° C Min.	0° C Max.	+25° C Min.	+25° C Max.	+75° C Min.	+75° C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}	GND
POWER SUPPLY															
Drain current	I_E	8	-	-	-	55	-	-	mAdc	All inputs	-	-	-	8	1,16
Input current	I_{INH}	3,11,13	-	-	-	350	-	-	μAdc	*	-	-	-	8	1,16
	0.75 I_{INH}	5,6,7	-	-	-	270	-	-	μAdc	*	-	-	-	8	1,16
	I_{INL}	*	-	-	0.5	-	-	-	μAdc	-	*	-	-	8	1,16
Logic '1' output voltage	V_{OH}	2	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	3,5	-	-	-	8	1,16
		2	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	-5	3,5	-	-	8	1,16
Logic '0' output voltage	V_{OL}	2	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	3,5	-	-	-	8	1,16
		2	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	-	3.5	-	-	8	1,16
Logic '0' threshold voltage	V_{OHA}	2	-1.020	-	-0.980	-	-0.920	-	Vdc	-	-	3,5	-	8	1,16
		2	-1.020	-	-0.980	-	-0.920	-	Vdc	-	-	-	3,5	8	1,16
Logic '0' threshold voltage	V_{OLA}	2	-	-1.615	-	-1.600	-	-1.575	Vdc	-	-	3	5	8	1,16
		2	-	-1.615	-	-1.600	-	-1.575	Vdc	-	-	5	3	8	1,16
SWITCHING TIME (50 ohm load)			**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**			-	**Pulse in**	**Pulse out**	**-3.2V**	**+2.0V**
Propagation delay	t_{3+2+}	2	1.3	1.8	1.3	1.8	1.5	2.2	ns	-	-	3	2	8	1,16
	t_{3-2+}	2	1.2	1.8	1.3	1.8	1.5	2.2		-	-				
	t_{3+2-}	2	1.4	1.9	1.4	1.9	1.6	2.3		-	-				
	t_{3-2-}	2	1.4	1.9	1.4	1.9	1.6	2.3		-	-				
	t_{5+5+}	2	1.7	2.3	1.7	2.3	1.9	2.7		-	-	5			
	t_{5-2+}	2								-	-				
	t_{5+2-}	2								-	-				
	t_{5-2-}	2								-	-				
Rise time	t_{2+}	2	1.9	2.5	1.9	2.5	2.1	2.8	ns	-	-	3	2	8	1,16
Fall time	t_{2-}	2	1.6	2.2	1.6	2.2	1.8	2.5	ns	-	-	3	2	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

PLESSEY
Semiconductors

SP1692

QUAD LINE RECEIVER

Four differential amplifiers with emitter follower outputs are provided.

The device can be configured as a differential line receiver or by using the internal V_{BB} reference single ended ECL signals can be received. The SP1692 is also ideally suited for use in expanding the fan out of ECL circuits, or inverting ECL logic.

FEATURES

- ECL 10000 Compatible
- 50Ω Line Driving Capability
- Single or Differential Operation
- Operating Temperature Range -30°C to +85°C

ORDERING INFORMATION

SP1692DG (Commercial ceramic package)
SP1692BB DG (Plessey High Reliability Specification)

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\lvert V_{CC} - V_{EE} \rvert$ 8V
Input voltage	0V to V_{EE}
Output source current	<40mA
Storage temperature range	-55°C to +150°C
Junction operating temperature	<+175°C

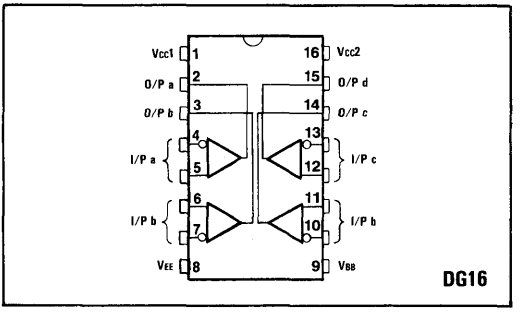


Fig.1 Pin connections (top view)

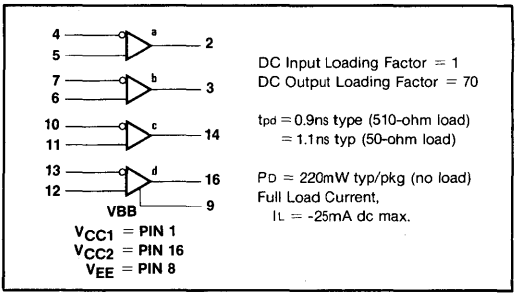


Fig.2 Logic diagram of SP1692

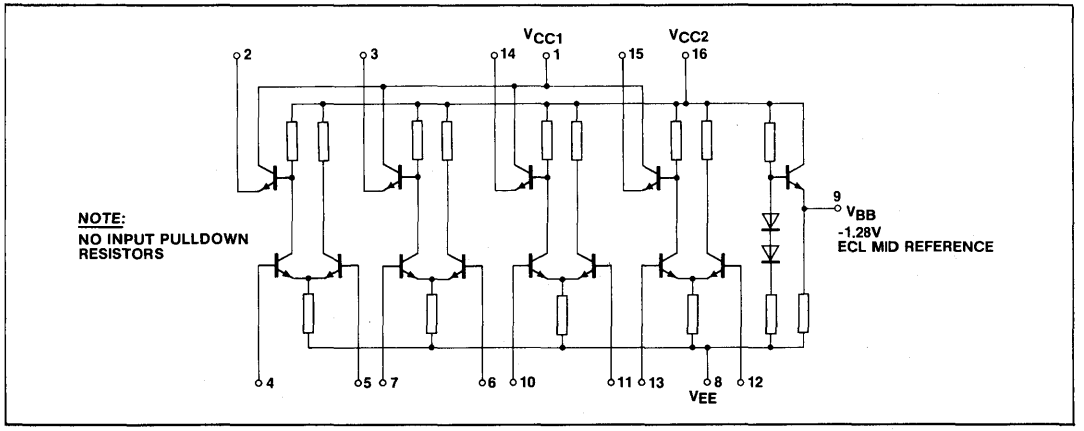


Fig.3 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0V dc.

Test temp.	TEST VOLTAGE (V) V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{BB}	V_{EE}
-30° C	-0.875	-1.890	-1.180	-1.515	From	-5.2
+25° C	-0.810	-1.850	-1.095	-1.485	Pin	-5.2
+85° C	-0.700	-1.830	-1.025	-1.440	9	-5.2

Characteristic	Symbol	Pin under test	SP1692 Test Limits -30° C Min.	-30° C Max.	+25° C Min.	+25° C Max.	+85° C Min.	+85° C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{BB}	V_{EE}	V_{CC} (GND)
POWER SUPPLY																
Drain current	I_{EE}	8	-	-	-	50	-	-	mAdc	-	4,7,10,13	-	-	5,6,11,12	8	1,16
Input current	I_{INH}	4	-	-	-	250	-	-	μAdc	4	7,10,13	-	-	5,6,11,12	8	1,16
Input leakage current	I_{INL}	4	-	-		100	-	-	μAdc	-	7,10,13	-	-	5,6,11,12	8,4	1,16
Logic '1' output voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	7,10,13	4	-	-	5,6,11,12	8	1,16
Logic '0' output voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4	7,10,13	-	-	5,6,11,12	8	1,16
Logic '1' threshold voltage	V_{OHA}	2	-1.065	-	-0.980	-	-0.910	-	Vdc	-	7,10,13	-	4	5,6,11,12	8	1,16
Logic '0' threshold voltage	V_{OLA}	2	-	-1.630	-	-1.600	-	-1.555	Vdc	-	7,10,13	4	-	5,6,11,12	8	1,16
Reference voltage	V_{BB}	9	-1.420	-1.280	-1.350	-1.230	-1.295	-1.150	Vdc	-	-	-	-	5,6,11,12	8	1,16
SWITCHING TIMES (50 ohm load)										**Pulse in**		**Pulse out**			**-3.2V**	**+2.0V**
Propagation delay	t_{4-2+}	2	-	1.6	-	1.5	-	1.7	ns	4		2		5,6,11,12	8	1,16
	t_{4+2-}	2	-	1.8	-	1.7	-	1.9	ns	4		2		5,6,11,12	8	1,16
Rise time	t_{2+}	2	-	2.2	-	2.1	-	2.3	ns	4		2		5,6,11,12	8	1,16
Fall time	t_{2-}	2	-	2.2	-	2.1	-	2.3	ns	4		2		5,6,11,12	8	1,16

Thermal characteristics $\theta_{JA} = 120°$ C/W
$\theta_{JC} = 40°$ C/W

PLESSEY
Semiconductors

SP16F60

DUAL 4-INPUT OR/NOR GATE

SP16F60 provides simultaneous OR-NOR output functions with the capability of driving 50Ω lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (—30° C to +85° C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

FEATURES

- Operating Temperature Range -30°C to +85°C
- Gate Switching Speed 550ps Typ.
- ECL III and ECL 10K Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation
- Pin and Power Compatible With SP1660

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems
- Nucleonics

ORDERING INFORMATION

SP16F60DG (Commercial - ceramic package)
SP16F60BB DG (Plessey High Reliability Specification)
SP16F60LC (Under development) (LCC)

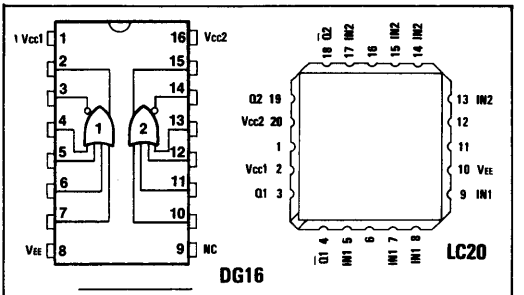


Fig.1(a) Logic and pin connections (top view) DG package
Fig.1(b) Pin connections LC package

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\|V_{CC} - V_{EE}\|$ 8V
Input voltages	0V to V_{EE}
Output source current	<40mA
Storage temperature range	-55° C to +150° C
Junction operating temperature	<+175° C

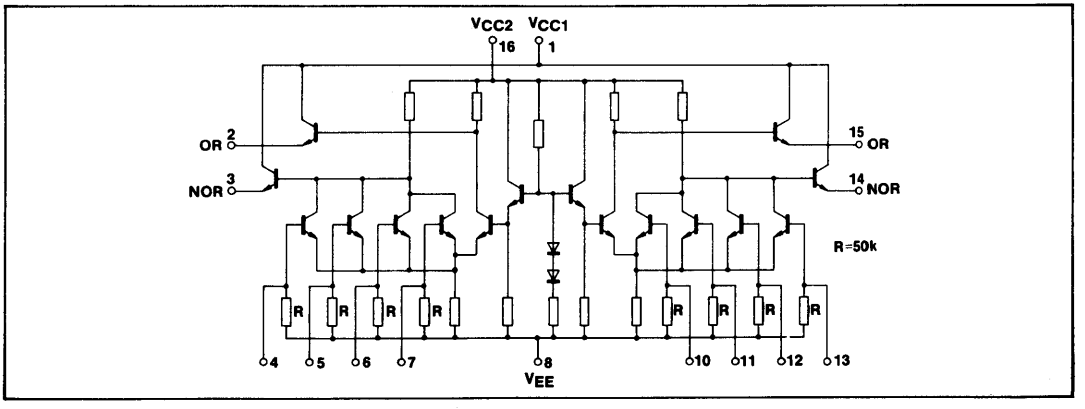


Fig.2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50Ω resistor to -2.0V dc.

Thermal characteristics

DG16
θ_{JA} = 107° C/W
θ_{JC} = 31° C/W

LC20
θ_{JA} = 147° C/W
θ_{JC} = 30° C/W

@ Test Temperature	TEST VOLTAGE VALUES (V) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP16F60 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Units	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mA	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μA	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μA	–	*	–	–	8	1,16
NOR Logic 1 Output Voltage	V_{OH}	3	-1.045	-0.875	-0.960	-0.810	-1.890	-0.700	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 0 Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 1 Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 0 Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 1 Threshold Voltage	V_{OHA}	3	-1.065	–	-0.980	–	-0.910	–	V	–	–	–	4	8	1,16
				–		–		–		–	–	–	5		
				–		–		–		–	–	–	6		
				–		–		–		–	–	–	7		
NOR Logic 0 Threshold Voltage	V_{OLA}	3	–	-1.630	–	-1.600	–	-1.555	V	–	–	4	–	8	1,16
			–		–		–			–	–	5	–		
			–		–		–			–	–	6	–		
			–		–		–			–	–	7	–		
OR Logic 1 Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	V	–	–	4	–	8	1,16
				–		–		–		–	–	5	–		
				–		–		–		–	–	6	–		
				–		–		–		–	–	7	–		
OR Logic 0 Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	V	–	–	–	4	8	1,16
			–		–		–			–	–	–	5		
			–		–		–			–	–	–	6		
			–		–		–			–	–	–	7		
Switching Times (50Ω Load)			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out			-3.2V	+2.0V
Propagation Delay	t_{4+3-}	3	–	–	0.55	0.8	–	–	ns	4	3	–	–	8	1,16
	t_{4-2-}	2	–	–			–	–			2	–	–		
	t_{4+2+}	2	–	–			–	–			2	–	–		
	t_{4-3+}	3	–	–			–	–			3	–	–		
Rise Time 20% to 80%	t_{3+}	3			0.4	0.6	–	–	ns	4	3	–	–	8	1,16
	t_{2+}	2			0.35	0.6	–	–	ns	4	2	–	–	8	1,16
Fall Time 20% to 80%	t_{3-}	3			0.4	0.6	–	–	ns	4	3	–	–	8	1,16
	t_{2-}	2			0.35	0.6	–	–	ns	4	2	–	–	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to the input under test.

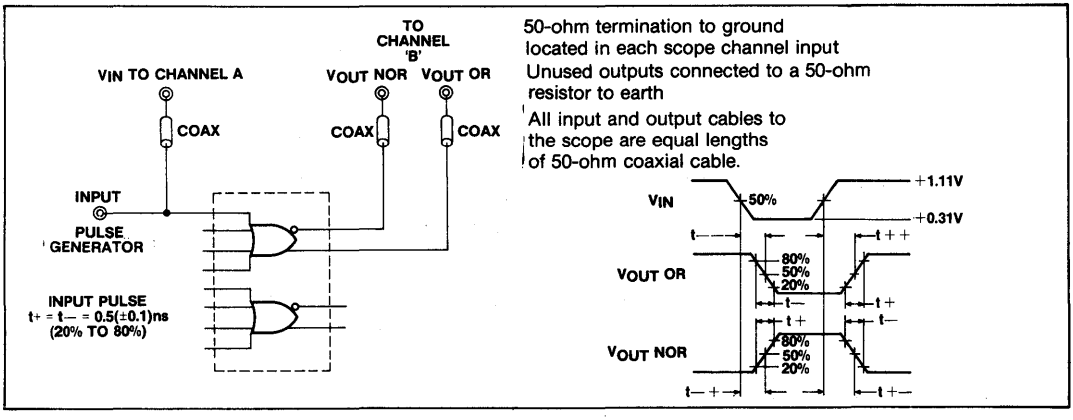


Fig.3 Switching time test circuit and waveforms at +25° C

PLESSEY
Semiconductors

ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SP9131

520MHz ECL DUAL D FLIP-FLOP

The SP9131 Dual D type flip-flop is pin compatible with 10131, but has improved dynamic performance.

FEATURES

- Guaranteed Operation at 520MHz
- Separate or Common Clock
- Independent Set and Reset Inputs
- Master Slave Operation
- -5.2V Supply
- Operating Temperature Range -30°C to +85°C
- ECL 10K Compatible
- Pin Compatible with MC10131/102131/105131/ 10H131-But Faster

ORDERING INFORMATION

SP9131DG (Commercial - ceramic package)
SP9131BB DG (Plessey High Reliability Specification)
SP9131LC (Under development) (LCC)

R-S TRUTH TABLE

R	S	Qn+1
L	L	Qn
L	H	H
H	L	L
H	H	ND

CLOCKED TRUTH TABLE

C	D	Qn+1
L	X	Qn
H	L	L
H	H	H

X = Don't care
C = CE + CC
A clock H is a clock transition from a low to a high state.

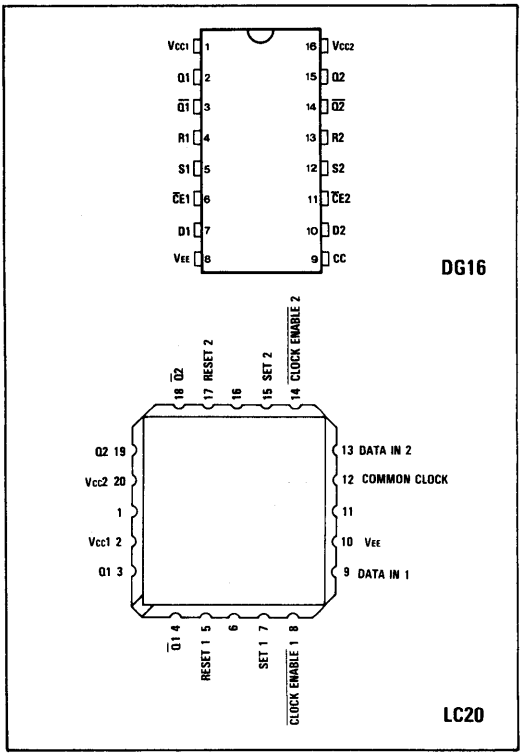


Fig.1 Pin connections - top view

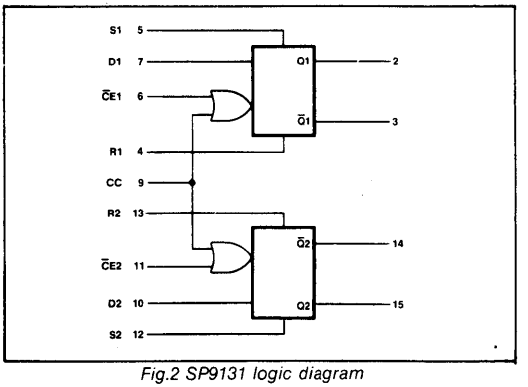


Fig.2 SP9131 logic diagram

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	|VCC - VEE| 8V
Base input voltage	0V to VEE
Output source current	<40mA
Storage temperature range	-55°C to +150°C
Junction operating temperature	<+175°C

THERMAL CHARACTERISTICS

DG16	θ_{JA} = 120° C/W
	θ_{JC} = 40° C/W
LC20	θ_{JA} = 125° C/W
	θ_{JC} = 20° C/W

ELECTRICAL CHARACTERISTICS

The SP9131 circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to -2 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

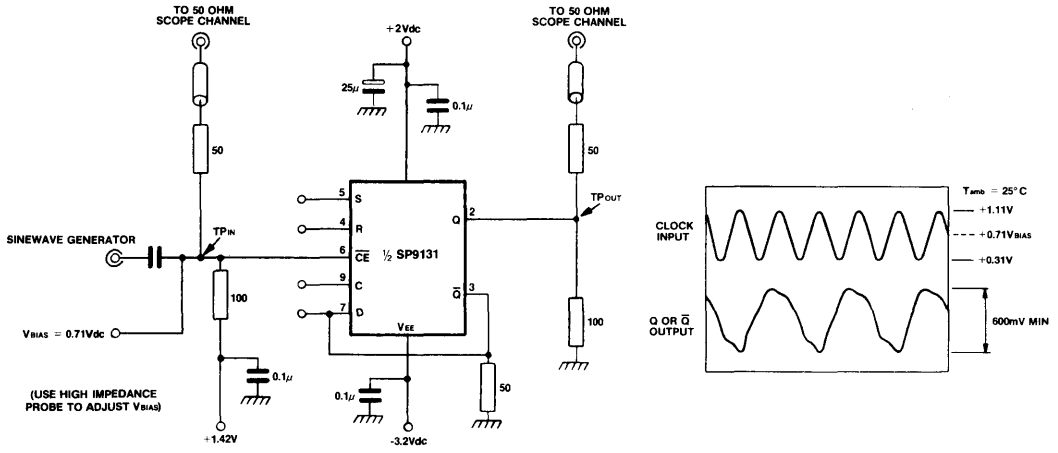
Test temp.	TEST VOLTAGES (V) V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}
-30° C	-0.89	-1.89	-1.205	-1.500	-5.2
+25° C	-0.81	-1.85	-1.105	-1.475	-5.2
+85° C	-0.70	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin under test	Test limits -30° C Min.	-30° C Max.	+25° C Min.	+25° C Typ.	+25° C Max.	+85° C Min.	+85° C Max.	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}	V_{CC} (GND)
Power supply current	I_E	8	-	95	-	70	87	-	95	mA	-	-	-	-	8	1.16
Input current	I_{inH}	4	-	-	-	-	600	-	-	µA	4	-	-	-	8	1.16
		5	-	-	-	-	600	-	-		5	-	-	-		
		6	-	-	-		300	-	-		6	-	-	-		
		7	-	-	-	-	300	-	-		7	-	-	-		
		9	-	-	-	-	420	-	-		9	-	-	-		
Input leakage current	I_{inL}	4,5 (Note 1)	-	-	0.5	-	-	-	-	µA	-	-	-	-	8	1.16
		6,7,9 (Note 1)	-	-	0.5	-	-	-	-	µA	-	-	-	-	8	1.16
Logic '1' output voltage	V_{OH}	2	-1.06	-0.89	-0.96	-	-0.81	-0.89	-0.70	V	5	-	-	-	8	1.16
		2 (Note 2)	-1.06	-0.89	-0.96	-	0.81	-0.89	-0.70	V	7	-	-	-	8	1.16
Logic '0' output voltage	V_{OL}	3	-1.89	-1.675	-1.85	-	-1.65	-1.825	-1.615	V	5	-	-	-	8	1.16
		3 (Note 2)	-1.89	-1.675	-1.85	-	-1.65	-1.825	-1.615	V	7	-	-	-	8	1.16
Logic '1' threshold voltage	V_{OHA}	2	-1.08	-	-0.98	-	-	-0.91	-	V	-	-	5	-	8	1.16
		2 (Note 2)	-1.08	-	-0.98	-	-	-0.91	-	V	-	-	7	9	8	1.16
Logic '0' threshold voltage	V_{OLA}	3	-	-1.655	-	-	-1.63	-	-1.595	V	-	-	5	-	8	1.16
		3 (Note 2)	-	-1.655	-	-	-1.63	-	-1.595	V	-	-	7	9	8	1.16
SWITCHING TIMES											+1.11V		Pulse in	Pulse out	-3.2V	+2.0V
Clock input propagation delay	t_{9+2-}	2	0.5	1.8	0.5	1.0	1.8	0.6	2.1	ns	-	-	9	2	8	1.16
	t_{9+2+}	2	-	-				-	-		7	-	9	2		
	t_{6+2+}	2	-	-				-	-		7	-	6	2		
	t_{6+2-}	2	-	-				-	-		-	-	6	2		
Rise time (20 to 80 %)	t_{2+}	2	0.5	1.5	0.5	1.0	1.5	0.5	1.6		7	-	9	2		
Fall time (20 to 80 %)	t_{2-}	2	0.4	1.4	0.4		1.4	0.5	1.5		-	-	9	2		
Set input propagation delay	t_{5+2+}	2	0.5	2.0	0.5	1.0	2.0	0.6	2.3	ns	-	-	5	2	8	1.16
	t_{12+15+}	15	-	-				-	-		6	-	12	15		
	t_{5+3-}	3	-	-				-	-		-	-	5	3		
	t_{12+14-}	14	-	-				-	-		9	-	12	14		
Reset input propagation delay	t_{4+2-}	2	-	-		1.0		-	-	ns	-	-	4	2	8	1.16
	t_{13+15-}	15	-	-				-	-		6	-	13	15		
	t_{4+3-}	3	-	-				-	-		-	-	4	3		
	t_{13+14+}	14	-	-				-	-		9	-	13	14		
Setup time	t_{setup}	7	1.0	-	1.0	-		1.0	-	ns	-	-	6.7	2	8	1.16
Hold time	t_{hold}	7	0.2	-	0.2	-		0.2	-	ns	-	-	6.7	2	8	1.16
Toggle frequency (max.)	f_{Top}	2	520	-	520	600	-	500	-	MHz	-	-	6	2	8	1.16

NOTES
1. Individually test each input: apply V_{IL} min to pin under test.
2. Output level to be measured after a clock pulse has been applied to the CE input (pin 6).

V_{IH} max.
V_{IL} min.

TEST CIRCUIT DETAILS

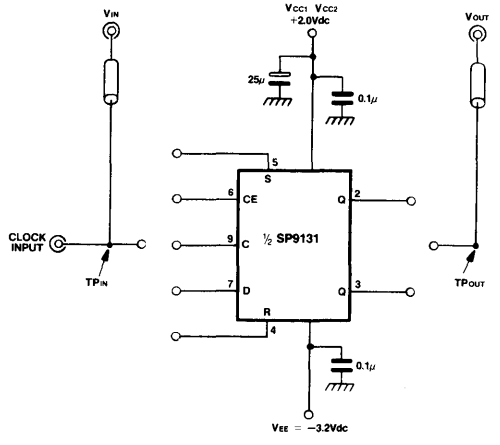


50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be $<\frac{1}{4}$ inch from TP_{IN} to input pin and TP_{OUT} to output pin.

The +2V and -3.2V supplies allow the output load to be connected to ground.

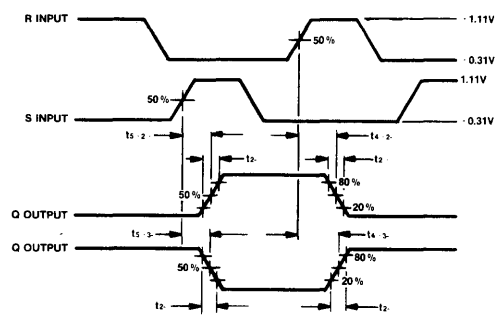
Fig.3 Toggle frequency test circuit

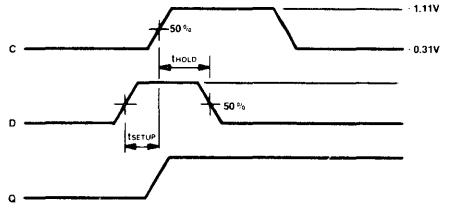


50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be $<\frac{1}{4}$ inch from TP_{IN} to input pin and TP_{OUT} to output pin.

iNPUT PULSE
$t+ = t- = 1.0nsec \pm 0.2nsec$ (20 to 80%).





NOTE

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

Fig.4 Switching time test circuit and waveforms at 25° C

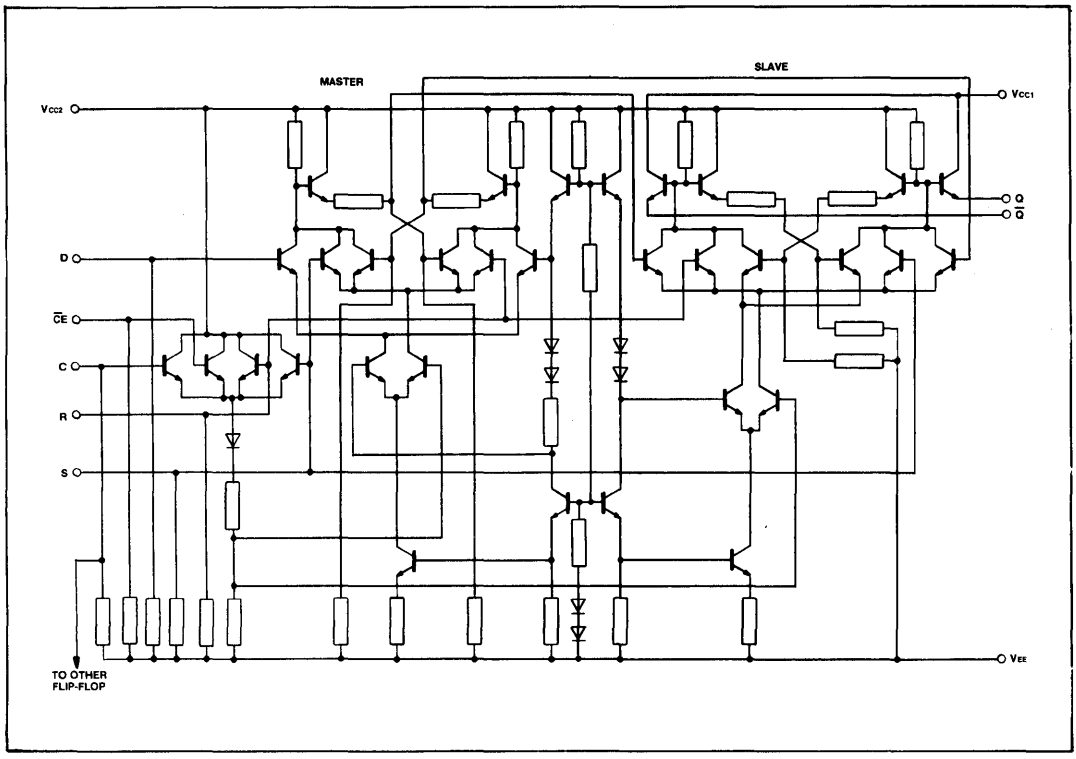


Fig.5 Circuit schematic (½ of circuit shown)

PLESSEY
Semiconductors

ADVANCE INFORMATION

ıdvance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still ıave *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to ıe representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office ɔr details of current status.

SP9210

200MHz 8-BIT LATCH

The SP9210 is a dual 4-bit master/slave D-type flip-flop with asynchronous set and reset which override the clock input.

Data is entered into the master when the clock is low and is transferred to the slave on the positive transition of the clock, the device being edge-sensitive.

On-chip pulldown resistors eliminate the need to tie unused inputs to VEE.

FEATURES

- Dual 4-Bit Master/Slave D-Type Flip-Flop
- Clock Rate in Excess of 200MHz
- -5.2V Supply
- Current Consumption Typically 145mA
- Input Current Less Than 330µA
- Operating Temperature Range -30°C to +85°C
- Set and Reset Inputs Provided
- ECL 10K Compatible
- Dual Clock Inputs

ORDERING INFORMATION

SP9210DG (Commercial - ceramic package)
SP9210BB DG (Plessey High Reliability Specification)
SP9210LC (Under development) (LCC)

PIN NAMES

S1-4	Set input for 1-4
S5-8	Set input for 5-8
VEE	Supply voltage (-VE)
D1-8	Data inputs 1-8
CLK1-4	Clock latch for 1-4
CLK5-8	Clock latch for 5-8
Q1-8	Outputs latches 1-8
R1-4	Reset input latch for 1-4
R5-8	Reset input latch for 5-8

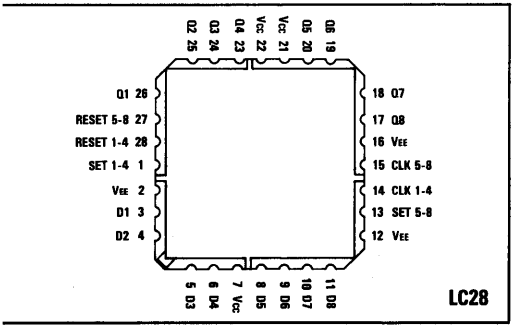


Fig.1(b) Pin connections, surface mounting package (top view)

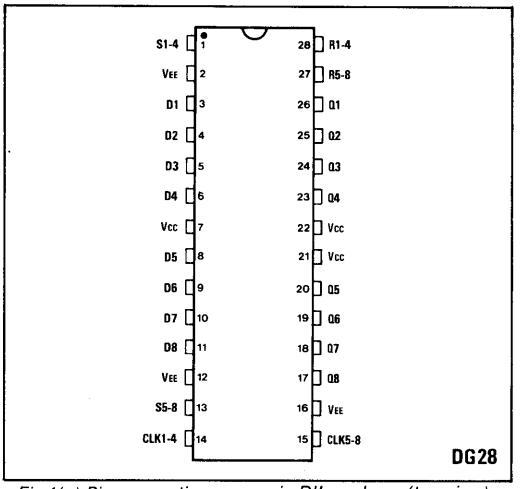


Fig.1(a) Pin connections, ceramic DIL package (top view)

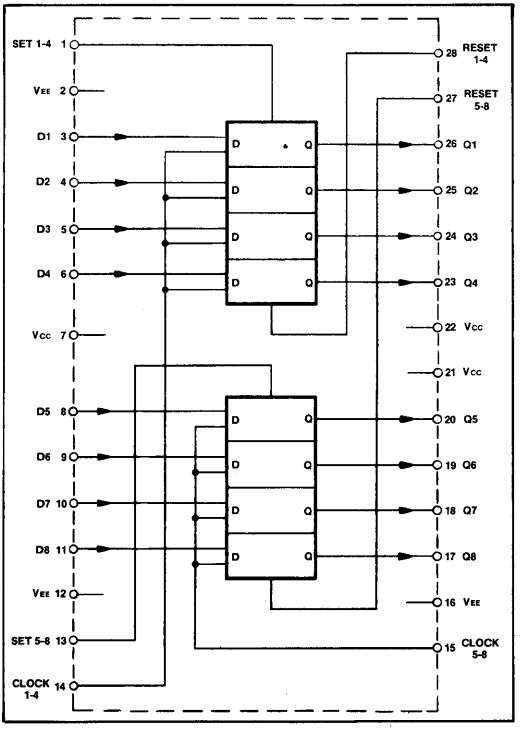


Fig.2 SP9210 block diagram

ELECTRICAL CHARACTERISTICS

Each circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to -2 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

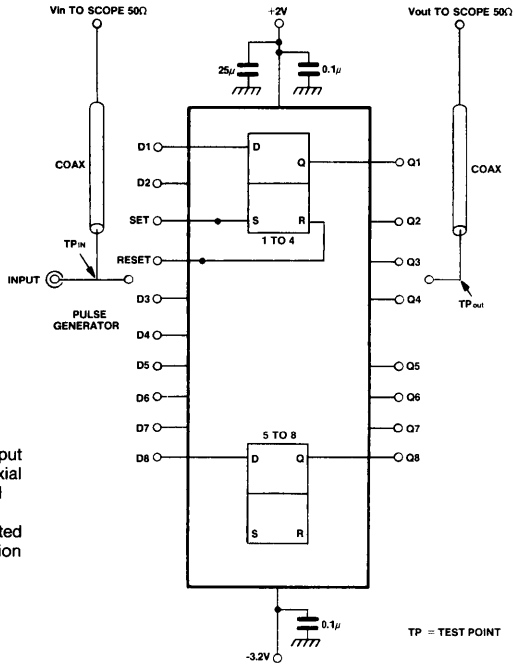
Test temp.	TEST VOLTAGES (V) V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}
-30° C	-0.89	-1.89	-1.205	-1.500	-5.2
+25° C	-0.810	-1.850	-1.105	-1.475	-5.2
+85° C	-0.70	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin under test	-30° C Min.	-30° C Max.	+25° C Min.	+25° C Typ.	+25° C Max.	+85° C Min.	+85° C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX.	V_{IL} MIN.	V_{IHA} MIN.	V_{ILA} MAX.	V_{EE}	V_{CC} (GND)
POWER SUPPLY																
Drain current	I_{EE}	2,12,16	-	200	-	145	180	-	200	mA	-	-	-	-	2,12,16	7,21,22
Input current	I_{INH}	Set/Reset	-	-	-	-	330	-	-	µA	Note 1	-	-	-	2,12,16	7,21,22
		Clock	-	-	-	-	310	-	-	µA	Note 1	-	-	-	2,12,16	7,21,22
		Data	-	-	-	-	310	-	-	µA	Note 1	-	-	-	2,12,16	7,21,22
Input leakage current	I_{INL}	All inputs	-	-	0.5	-	-	-	-	µA	-	Note 1	-	-	2,12,16	7,21,22
Logic '1' output voltage	V_{OH}	All outputs (Note 2)	-1.06	-0.89	-0.96	-	-0.81	-0.89	-0.70	V	Data inputs	-	-	-	2,12,16	7,21,22
Logic '0' output voltage	V_{OL}	All outputs (Note 2)	-1.89	-1.675	-1.85	-	-1.65	-1.825	-1.615	V	-	Data inputs	-	-	2,12,16	7,21,22
Logic '1' threshold voltage	V_{OHA}	All outputs (Note 2)	-1.08	-	-0.98	-	-	-0.91	-	V	-	-	Data inputs	-	2,12,16	7,21,22
Logic '0' threshold voltage	V_{OLA}	All outputs (Note 2)	-	-1.655	-	-	-1.63	-	-1.595	V	-	-	-	Data inputs		
SWITCHING TIMES											**+1.11V**	**+0.3V**	**Pulse in**	**Pulse out**	**-3.2V**	**+2.0V**
Clock input propagation delay	t_{d+}	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.4	ns	Data inputs	-	Clock inputs	Outputs	2,12,16	7,21,22
	t_{d-}	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.4	ns	-	Data inputs	Clock inputs	Outputs	2,12,16	7,21,22
Rise time (20 % - 80 %)	t_r	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.3	ns	Data inputs	-	Clock inputs	Outputs	2,12,16	7,21,22
Fall time (20 % - 80 %)	t_f	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.3	ns	-	Data inputs	Clock inputs	Outputs	2,12,16	7,21,22
Set propagation delay	t_{set}	All outputs	1.5	4.0	1.5	2.5	4.0	1.4	4.5	ns	-	-	Set inputs	Outputs	2,12,16	7,21,22
Reset propagation delay	t_{rset}	All outputs	1.5	4.0	1.5	2.5	4.0	1.4	4.5	ns	-	-	Reset inputs	Outputs	2,12,16	7,21,22
Set up time	t_s	Data inputs	1.5	-	1.5	-	-	1.5	-	ns	-	-	Data,Clock	Outputs	2,12,16	7,21,22
Hold time	t_h	Data inputs	1.0	-	1.0	-	-	1.0	-	ns	-	-	Data,Clock	Outputs	2,12,16	7,21,22
Max.clock frequency	f_{CLK}	All outputs	-	-	200	-	-	-	-	MHz	Data inputs	-	Clock inputs	Outputs	2,12,16	7,21,22

NOTES
1. Each input pin tested individually.
2. Output level to be measured after a clock pulse has been applied.

Thermal characteristics

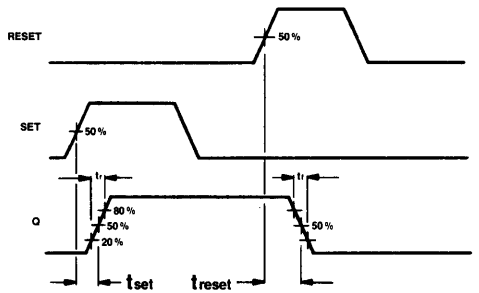
DG28	θ_{JA} = 40° C/W
	θ_{JC} = 15° C/W
LC28	θ_{JA} = 125° C/W
	θ_{JC} = 20° C/W



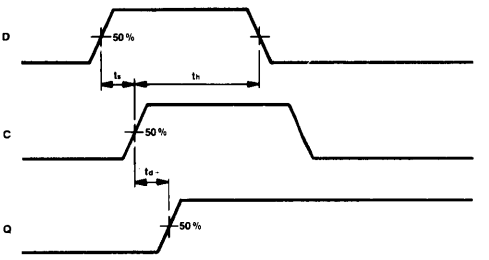
50 ohm to ground located in each scope channel input. All input and output cables to the scope are equal length of 50 ohm coaxial cable. Wire length should be ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin.

With supply voltages at 2V and -3.2V outputs should be terminated with 50 ohms to ground; this results in an output level translation giving V_{OH} = 1.11V and V_{OL} = +0.31V.

SET AND RESET TIMING DIAGRAM



CLOCK AND DATA TIMING DIAGRAM



NOTE

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at data input (D).

Fig.3 Test circuit details for dynamic test

R - S TRUTH TABLE

R	S	Qn + 1
L	L	Qn
L	H	H
H	L	L
H	H	ND

R = Reset, S = Set,
ND = Not defined

CLOCKED TRUTH TABLE

C	D	Qn + 1
L	X	Qn
↓	L	L
↑	H	H

C = Clock, D = Data,
↑ = Rising edge,
X = Don't care

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\|V_{CC} - V_{EE}\|$ 7V
Input voltages	V_{CC} to V_{EE}
Output source current	<40mA
Storage temperature range	-55° C to +150° C
Junction operating temperature	<175° C

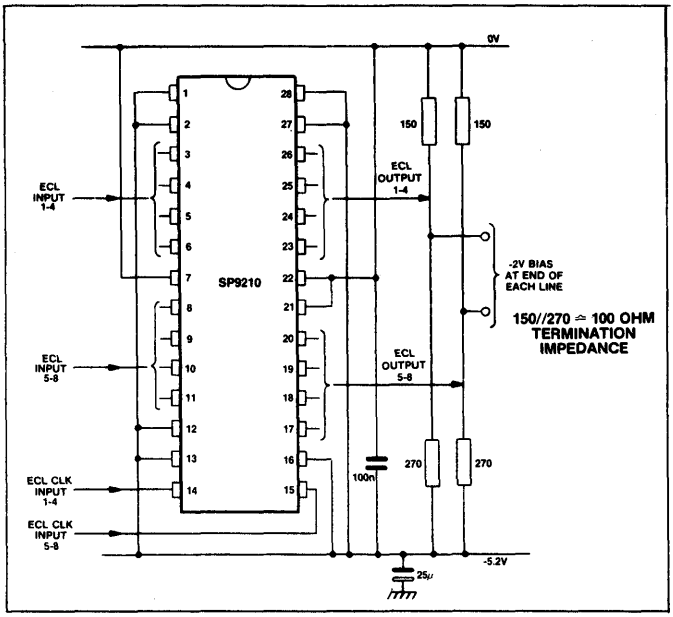


Fig.4 ECL 4 + 4 latch with 100Ω output termination

PLESSEY
Semiconductors

SP9680

ULTRA FAST COMPARATOR

The SP9680 is an ultra fast comparator manufactured using a high performance bipolar process which makes possible very short propagation delays (2.4ns typ.).

The circuit has differential inputs and complementary ECL outputs, capable of driving 50 Ω lines.

The device is manufactured in a low cost mini-dip package and is intended as an alternative to the faster SP9685 in applications where performance premium and the latch facility are not required.

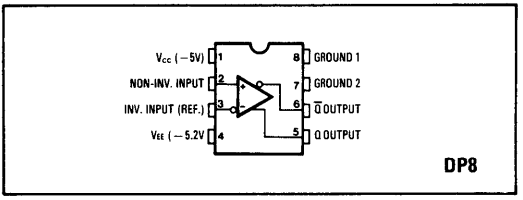
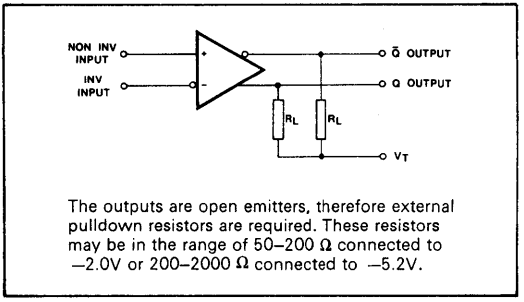


Fig. 1 Pin connections

FEATURES

- Propagation Delay 2.4ns Typ.
- Complementary ECL Outputs
- 50 Ω Line Driving Capability
- Excellent Common Mode Rejection
- 8-Lead Plastic Package
- Supply Voltages +5, −5.2V
- Operating Temperature Range −30°C to +70°C



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200 Ω connected to −2.0V or 200–2000 Ω connected to −5.2V.

Fig. 2 Functional diagram

ORDERING INFORMATION

SP9680DP (Commercial - plastic package)

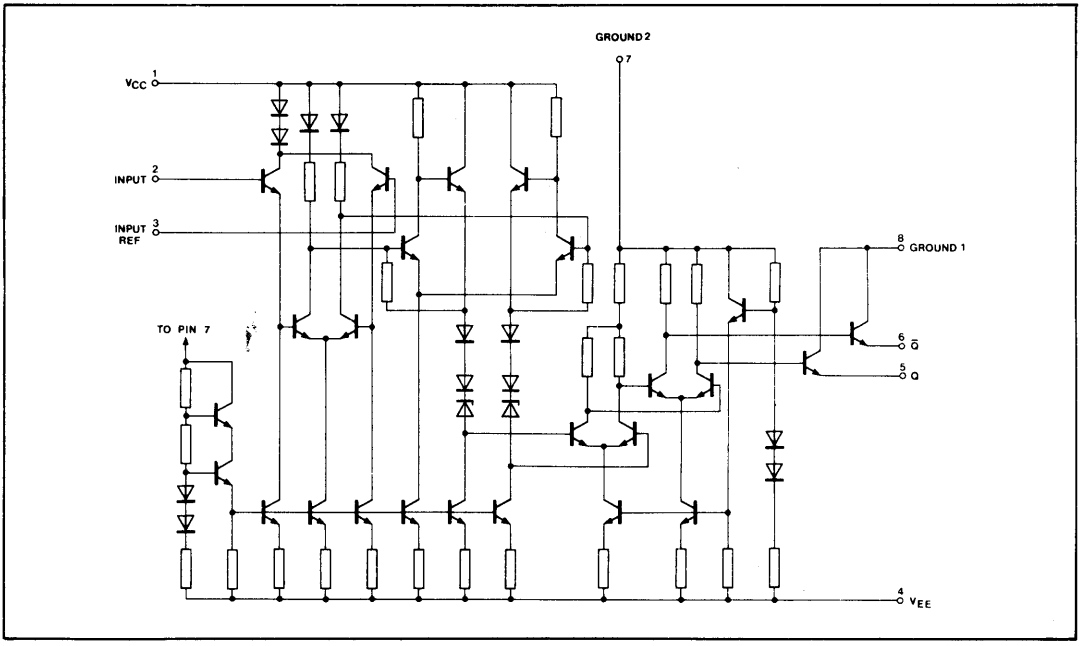


Fig. 3 SP9680 circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25°C
V_{CC} = 5.00V ± 0.25V
V_{EE} = −5.2V ± 0.25V
R_L = 50 Ω
V_T = −2.0V (See Fig. 2)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	−6		+6	mV	R_S <100 Ω
Input bias current		20	40	µA	
Input offset current			10	µA	
Supply current I_{CC}		18	25	mA	
I_{EE}		22	35	mA	
Total power dissipation		200	300	mW	
Input to Q output delay		2.4	4	ns	} 100mV pulse,10mV overdrive
Input to $\overline{Q}$ output delay		2.4	4	ns	
Common mode range	−2		+2	V	
Common mode rejection ratio		80		dB	
Output logic levels					
Output HIGH	−0.96		−0.81	V	
Output LOW	−1.85		−1.65	V	
Input capacitance		3.5		pF	
Input resistance	50			kΩ	
Operating temperature range	−30		+70	°C	

Thermal characteristics θ_{JA} = 180° C/W

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage V_{CC} +6V
Negative supply voltage V_{EE} −6V
Output current 30mA
Input voltage ±3V
Differential input voltage 3.5V
Storage temperature −55°C to +125°C
Operating junction temperature <125° C

PLESSEY
Semiconductors

SP9685, SP9685AB

ULTRA FAST COMPARATOR

The SP9685 is an ultra-fast comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50Ω terminated transmission lines. The high resolution available makes the device ideally suited to analog-to-digital signal processing applications.

A latch function is provided to allow the comparator to be used in a sample-hold mode. When the latch enable input is ECL high, the comparator functions normally. When the latch enable is driven low, the outputs are forced to an unambiguous ECL logic state dependent on the input conditions at the time of the latch input transition. If the latch function is not used, the latch enable may be connected to ground.

The device is pin compatible with the AM685 but operates from conventional +5V and -5.2V rails. It is pin and voltage compatible with AD9685.

FEATURES

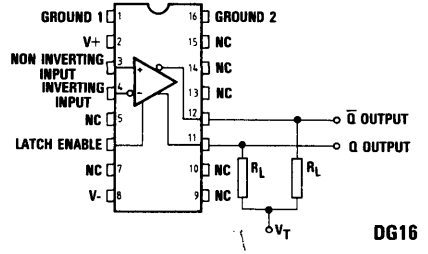
- Propagation Delay 2.2ns Typ.
- Latch Set-up Time 1ns Max.
- Complementary ECL Outputs
- Supply +5V, -5.2V (±0.25V)
- 50Ω Line Driving Capability
- Excellent Common Mode Rejection
- Operating Temperature Range:
  SP9685 — -30°C to +85°C
  SP9685AB — 55°C to +125°C
- Pin Compatible with AD9685
- Pin Compatible with AM685 — But Faster

APPLICATIONS

- Ultra High Speed A/D Converter
- Ultra High Speed Line Receivers
- Peak Detectors
- Threshold Detectors

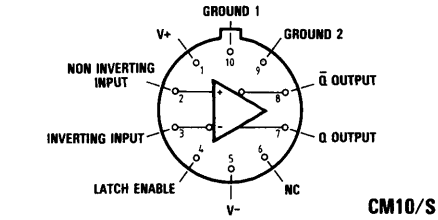
ORDERING INFORMATION

SP9685CM (Commercial - CM package)
SP9685DG (Commercial - ceramic package)
SP9685LC (Commercial - LCC package)
SP9685AB DG (Manufactured to Plessey High Reliability Specification)



THE OUTPUTS ARE OPEN EMITTERS, THEREFORE EXTERNAL PULLDOWN RESISTORS ARE REQUIRED. THESE RESISTORS MAY BE IN THE RANGE OF 50-200Ω CONNECTED TO -2.0V OR 200-2000Ω CONNECTED TO -5.2V.

Fig.1 DIL pin connections (top view) and function diagram



ON CM PACKAGE, PIN 5 IS CONNECTED TO CASE.

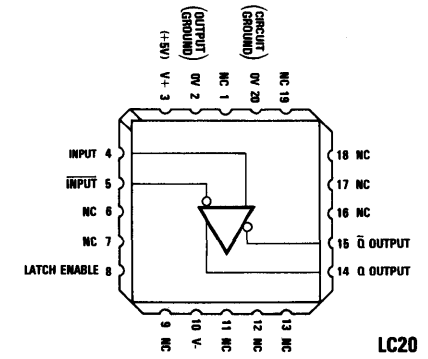


Fig.2 Metal package (CM10/S) and surface mounting (LC20) package pin connections (top view)

ABSOLUTE MAXIMUM RATINGS

Postive supply voltage	6V	Storage temperature range	-55° C to +150° C
Negative supply voltage	-6V	Operating junction temperature	<175° C
Output current	30mA	Lead temperature (soldering 60 sec)	300° C
Input voltage	±3V	Vibration	196m/s²
Differential input voltage	3.5V	Shock	14700m/s² peak 0.5ms duration
Power dissipation	350mW		

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 5.00V: V_{EE} = -5.2V: R_L = 50Ω: V_T = 2.0V (see Fig.1)

Characteristic	Value				Units	Conditions
	SP9685		SP9685AB			
	Min.	Max.	Min.	Max.		
Input offset voltage	-5	+5	-5	+5	mV	Rs< 100Ω 25° C
	-7	+7	-8	+8	mV	Rs< 100Ω
Input bias current		20		20	μA	25° C
		30		40	μA	
Input offset current		5		5	μA	25° C
		8		12	μA	
Input resistance	60		60		kΩ	25° C
Input capacitance		Typ.3		Typ.3	pF	25° C
Supply current I_{EE}		34		34	mA	25° C
		36		37	mA	
Supply current I_{CC}		23		23	mA	25° C
		24		25	mA	
Total power dissipation *	210	350			mW	25° C
Common mode range	-2.5	+2.5	-2.5	+2.5	V	
Output logic levels						
Output high	-0.96	-0.81	-0.96	-0.81	V	25° C
	-1.045	-0.875	-1.060	-0.89	V	T_{amb} = Min.
	-0.89	-0.70	-0.88	-0.69	V	T_{amb} = Max.
Output low	-1.85	-1.65	-1.85	-1.65	V	25° C
	-1.89	-1.65	-1.90	-1.65	V	T_{amb} = Min.
	-1.83	-1.575	-1.82	-1.55	V	T_{amb} = Max.
Min. latch set up time *		1		1	ns	Notes 1,2 25° C
		2		2.5	ns	
Input to output delay *		3		3	ns	Note 1 (Q and $\overline{Q}$) 25° C
		4		4.5	ns	
Latch to output delay *		3		3	ns	Notes 1,2 (Q and $\overline{Q}$) 25° C
		4.5		5	ns	
Minimum latch pulse width *		3		3	ns	25° C
Minimum hold time *		1		1	ns	25° C
Input capacitance *		Typ.3			pF	25° C
Input resistance *	60				kΩ	25° C
Common mode rejection ratio *	70				dB	25° C
Supply voltage rejection ratio *	50				dB	25° C

* Guaranteed but not tested.

NOTES
1. +100mV pulse with -10mV overdrive.
2. Switching measurements involving the latch are particularly difficult to perform and cannot be tested in production. Circuit analysis shows that at least 95% of devices will meet these specifications.

Thermal characteristics

CM10	θ_{JA} = 220° C/W
	θ_{JC} = 65° C/W
DG16	θ_{JA} = 120° C/W
	θ_{JC} = 40° C
LC20	θ_{JA} = 125° C/W
	θ_{JC} = 20° C/W

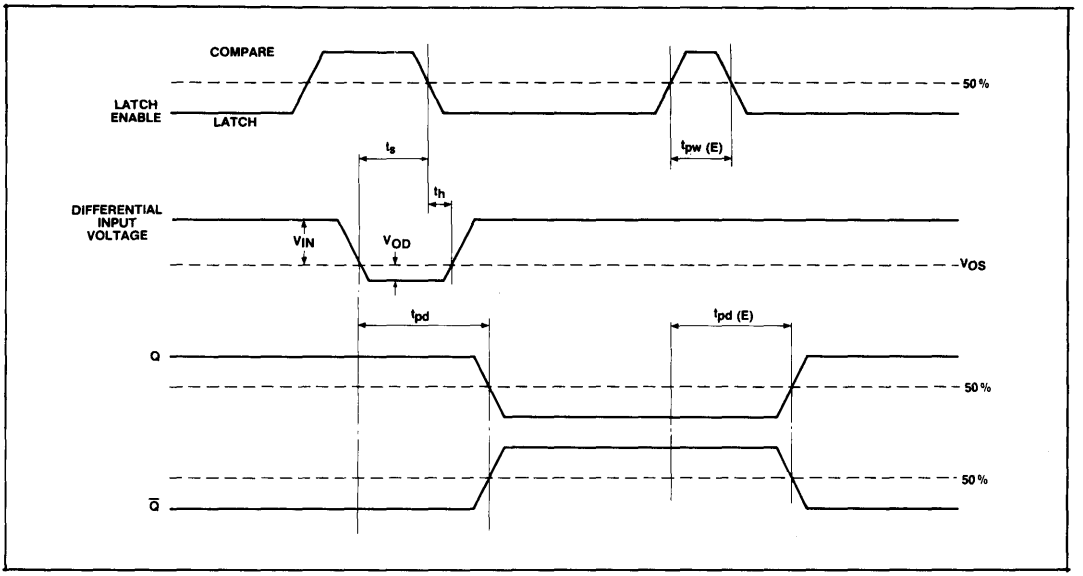


Fig.3 Timing diagram

OPERATING NOTES

Timing diagram

The timing diagram, Fig. 3, shows in graphic form a sequence of events in the SP9685. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse switches the comparator over after a time t_{pd}. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch falling edge, and must be maintained for a time t_h after the latch falling edge, in order to be acquired. After t_h, the output ignores the input status until the latch is again strobed. A minimum latch pulse width $t_{pw(E)}$ is required for the strobe operation, and the output transitions occur after a time $t_{pd(E)}$.

Measurement of propagation and latch delays

A simple test circuit is shown in Fig.4. The operating sequence is:

1. Power up and apply input and latch signals. Input = 100mV square wave, latch ECL levels. Connect monitoring scope(s).
2. Select 'offset null'.
3. Adjust offset null potentiometer for an output which switches evenly between states on clock pulses.
4. Measure input/outut and latch/output delays at 5mV offset, 10mV offset and 25mV offset.

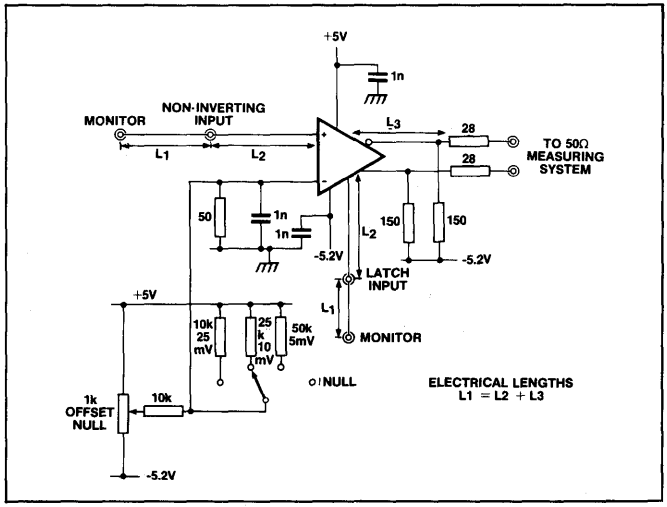


Fig.4 SP9685 test circuit

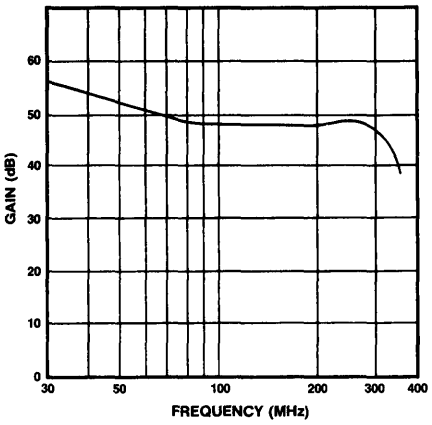


Fig.5 Open loop gain as a function of frequency

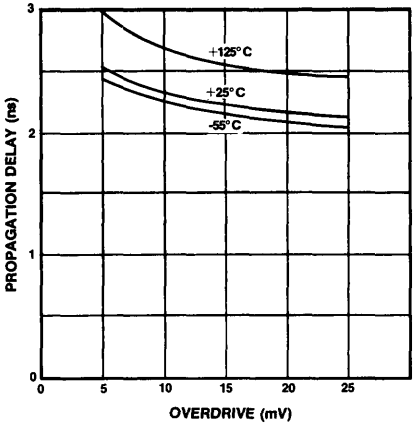


Fig.6 Propagation delay, latch to output as a function of overdrive

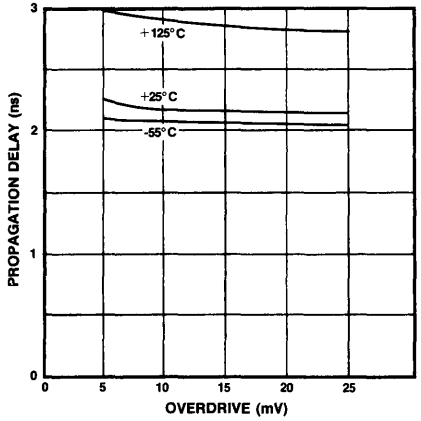


Fig.7 Propagation delay, input to output as a function of overdrive

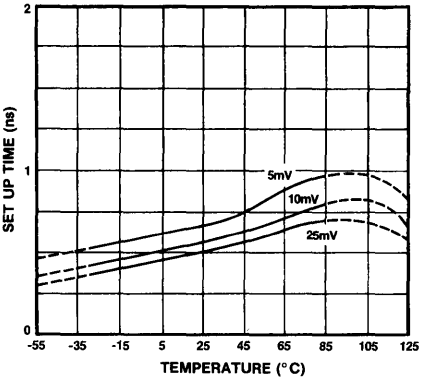


Fig.8 Set-up time as as function of temperature

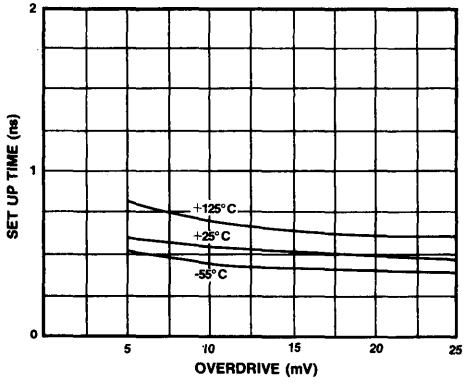


Fig.9 Set-up time as a function of input overdrive

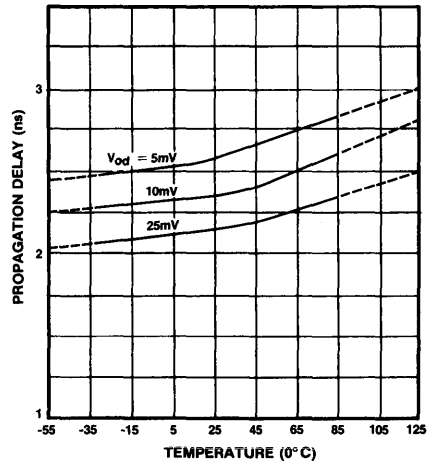


Fig.10 Propagation delay, input to output as a function of temperature

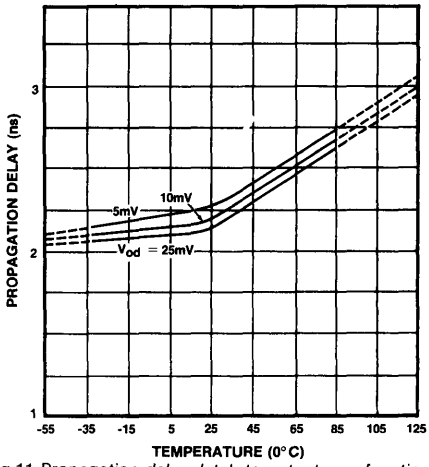


Fig.11 Propagation delay, latch to output as a function of temperature

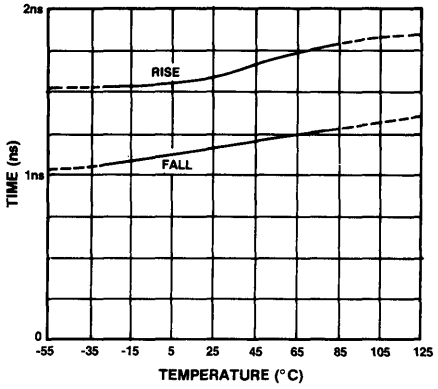


Fig.12 Output rise and fall times as a function of temperature

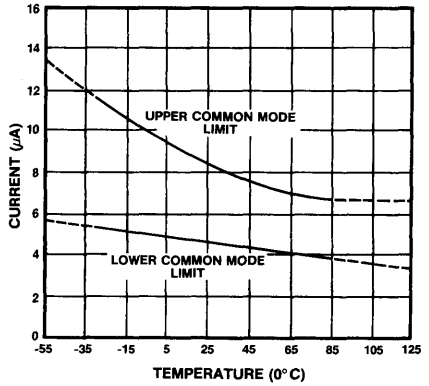


Fig.13 Input bias currents as a function of temperature

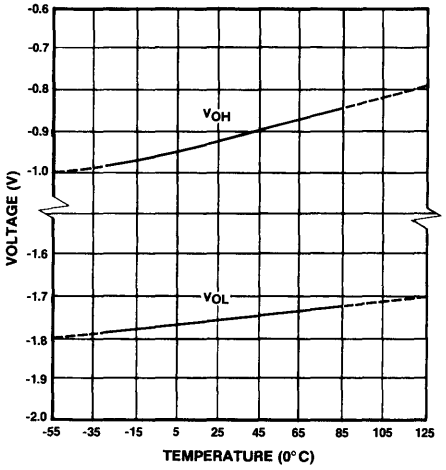


Fig.14 Output levels as a function of temperature

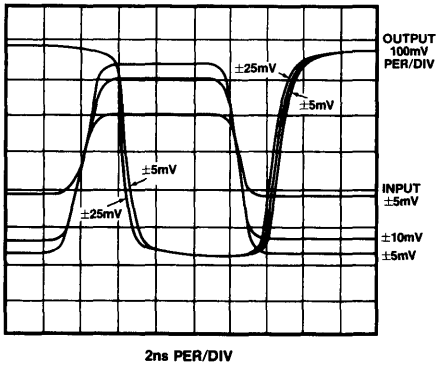


Fig.15 Response to various input signal levels

PLESSEY
Semiconductors

SP9687, SP9687AB

ULTRA FAST COMPARATOR

The SP96857is an ultra-fast dual comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50Ω terminated transmission lines. The high resolution available makes the device ideally suited to analog-to-digital signal processing applications.

A latch function is provided to allow the comparator to be operate in the follow-hold or sample-hold mode. The latch function inputs are intended to be driven from the complementary outputs of a standard ECL gate. If LE is high, and LE is low, the comparator function is in operation. When LE is driven low and LE high, the outputs are locked into the logical states at the time of arrival of the latch signal. If the latch function is not used, LE must be connected to ground.

The device is pin compatible with the AM687 and operates from conventional +5V and -5.2V rails.

FEATURES

- Propagation Delay 2.2ns Typ.
- Latch Set-up Time 1ns Max.
- Complementary ECL Outputs
- 50Ω Line Driving Capability
- Excellent Common Mode Rejection
- Supply Voltages +5V, -5.2V
- Operating Temperature Range -
  SP9687: -30 °C to +85 °C
  SP9687AB: -55 ° to +125 °C
- Pin Compatible with AD9687
- Pin Compatible with AM687 — But Faster
- Comparators within each SP9687 are matched as follows:
  Input to Output Delay 200ps (typ)
  Latch to Output Delay 200ps (typ)

ORDERING INFORMATION

SP9687DG (Commercial - ceramic package)
SP9687AB DG (Plessey High Reliability Specification)
SP9687LC (Commercial - LCC package)

OPERATING NOTES

Timing diagram

The timing diagram, Fig. 3, shows in graphic form a sequence of events in the SP9687. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse switches the comparator over after a time t_{pd}. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch falling edge, and must

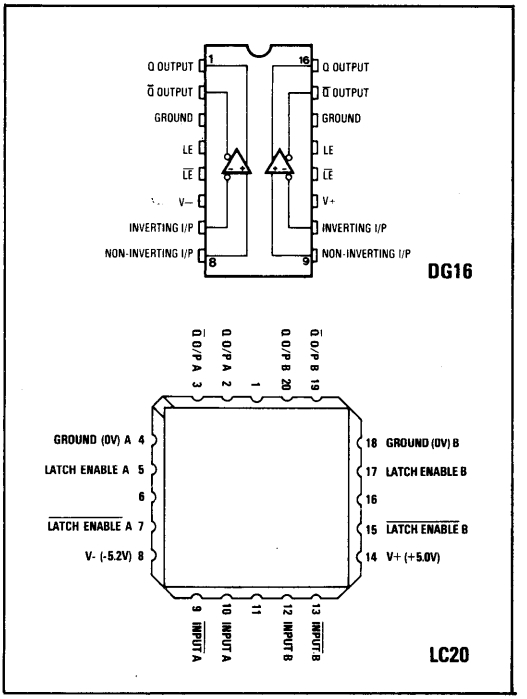
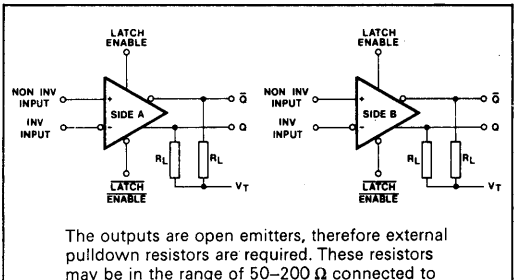


Fig.1 Pin connections



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200 Ω connected to –2.0V or 200–2000 Ω connected to –5.2V.

Fig.2 Functional diagram

be maintained for a time t_h after the latch falling edge, in order to be acquired. After t_h, the output ignores the input status until the latch is again strobed. A minimum latch pulse width $t_{pw(E)}$ is required for the strob operation, and the output transitions occur after a time $t_{pd(E)}$. The LE input is omitted for clarity.

ABSOLUTE MAXIMUM RATINGS

Postive supply voltage	6V	Differential latch voltage	3.5V
Negative supply voltage	-6V	Power dissipation	590mW
Output current	30mA	Storage temperature range	-55° C to +150° C
Input voltage	±3V	Operating junction temperature	<175° C/W
Differential input voltage	3.5V	Lead temperature (soldering 60 sec)	300° C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

The characteristics apply over the following ambient temperature ranges.
SP9687AB -55°C to +125°C and SP9687 -30°C to +85°C. See Note 1.
Supply voltage V_{CC} = +5V ± 0.25V V_{EE} = -5.2V ± 0.25V
Load resistance 50 and V_T = -2.0V (see Fig. 2).

Characteristic	Value				Units	Conditions
	SP9687		SP9687AB			
	Min.	Max.	Min.	Max.		
Input offset voltage	-5	+5	-5	+5	mV	Rs< 100Ω 25° C
	-7	+7	-8	+8	mV	Rs< 100Ω
Input bias current		20		20	μA	25° C
		30		40	μA	
Input offset current		5		5	μA	25° C
		8		12	μA	
Input resistance	60		60		kΩ	25° C
Input capacitance		3		3	pF	25° C
Supply current I_{EE}		68		68	mA	Note 2 25° C
		75		75	mA	
Supply current I_{CC}		46		46	mA	Note 2 25° C
		50		50	mA	
Common mode range	-2.5	+2.5	-2.5	+2.5	V	
Output logic levels						
Output high	-0.96	-0.81	-0.96	-0.81	V	25° C
	-1.045	-0.875	-1.060	-0.89	V	T_{amb} = Min.
	-0.89	-0.70	-0.88	-0.69	V	T_{amb} = Max.
Output low	-1.85	-1.65	-1.85	-1.65	V	25° C
	-1.89	-1.65	-1.90	-1.65	V	T_{amb} = Min.
	-1.83	-1.575	-1.82	-1.55	V	T_{amb} = Max.
Min. latch set up time *		1		1	ns	Notes 3,4 25° C
		2		2.5	ns	
Input to output delay *		3		3	ns	Note 3 (Q and $\overline{Q}$) 25° C
		4		4.5	ns	
Latch to output delay *		3		3	ns	Notes 3,4 (Q and $\overline{Q}$) 25° C
		4.5		5	ns	
Minimum latch pulse width *		3		3	ns	25° C
Minimum hold time *		1		1	ns	25° C

* Guaranteed but not tested.

NOTES

1. If the SP9687AB is to be operated with an ambient temperature in excess of 100°C it must be provided with an external heat sink or forced air cooling to ensure that the junction temperature does not exceed 175°C
2. Refers to entire package. Other data in this table applies to each half.
3. +100mV pulse with -100mV overdrive see Figs. 6 to 8.
4. Switching measurements involving the latch are particularly difficult to perform and cannot be tested in production. Circuit analysis shows that at least 95% of devices will meet these specifications.

Thermal characteristics

DG16	θ_{JA} = 107° C/W
	θ_{JC} = 31° C/W
LC20	θ_{JA} = 147° C/W
	θ_{JC} = 25° C/W

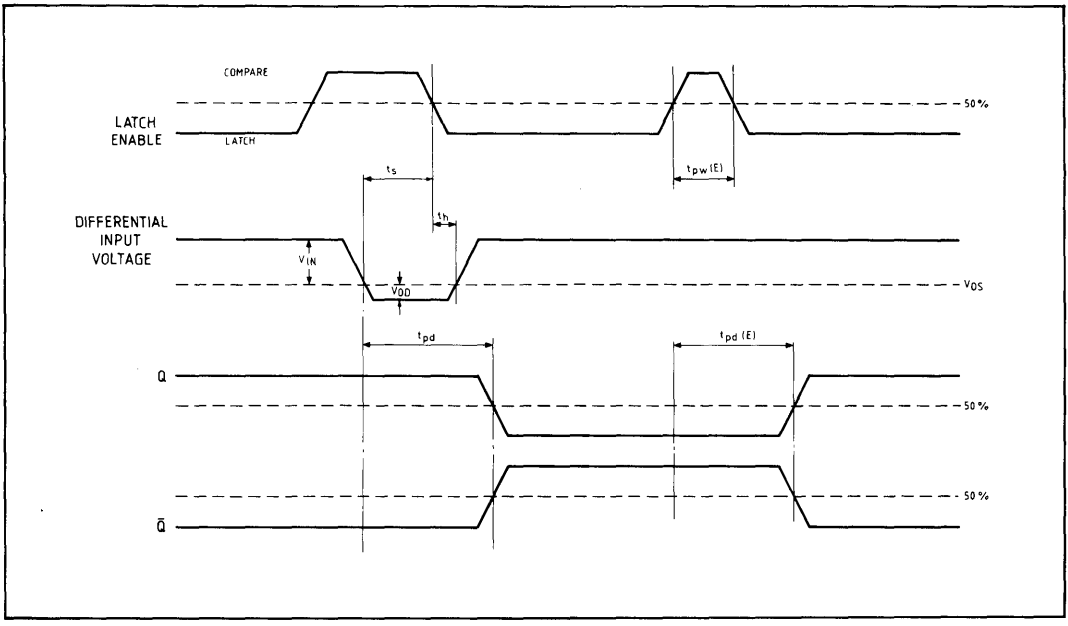


Fig.3 Timing diagram

PERFORMANCE CURVES

Unless otherwise specified, standard conditions for all curves are T_{amb} = 25°C, V_{CC} = 5.0V, V_{EE} = -5.2V

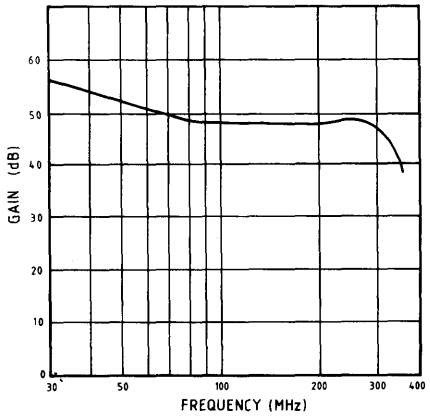


Fig.4 Open loop gain as a function of frequency

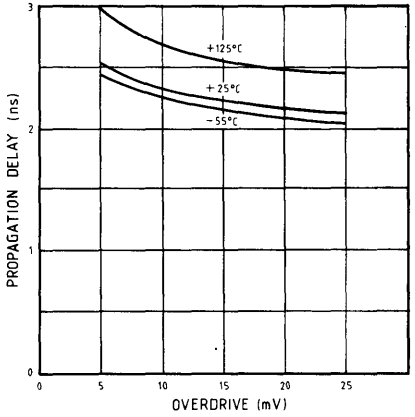


Fig.5 Propagation delay, latch to output as a function of overdrive

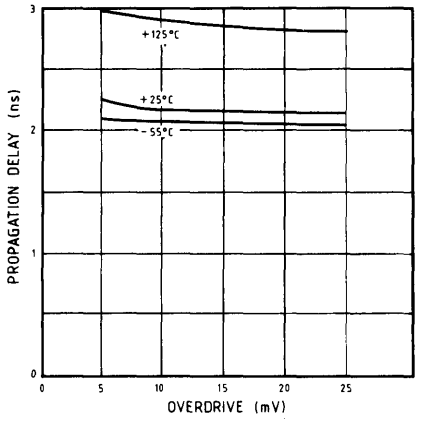


Fig.6 Propagation delay, input to output as a function of overdrive

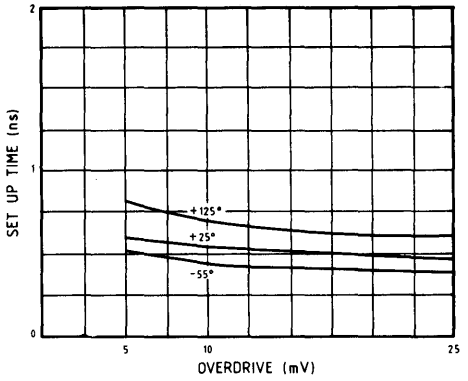


Fig.7 Set-up time as a function of temperature

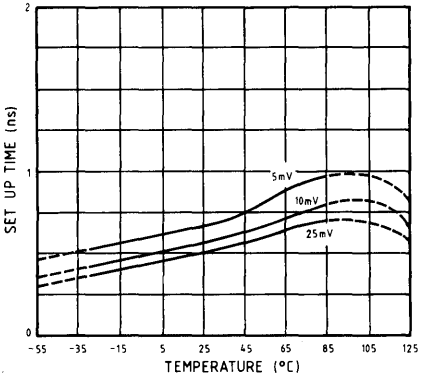


Fig.8 Set-up time as a function of input overdrive

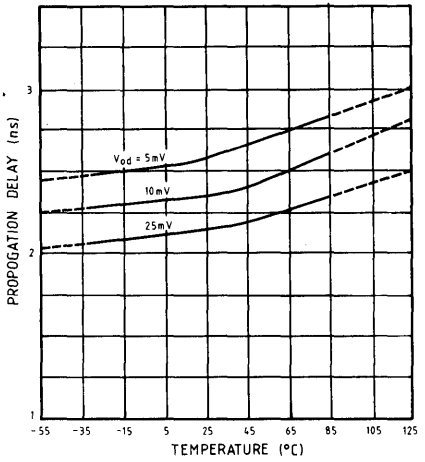


Fig.9 Propagation delay, input to output as a function of temperature

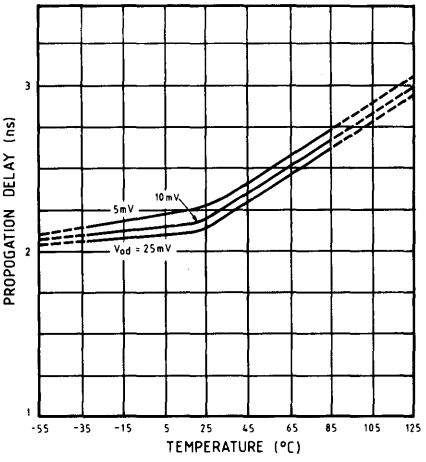


Fig.10 Propagation delay, latch to output as a function of temperature

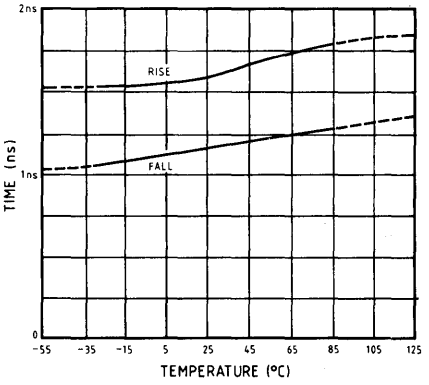


Fig.11 Output rise and fall times as a function of temperature

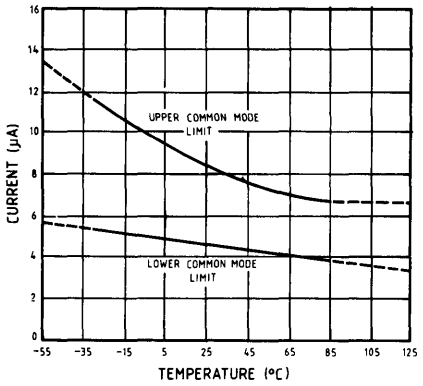


Fig.12 Input bias currents as a function of temperature

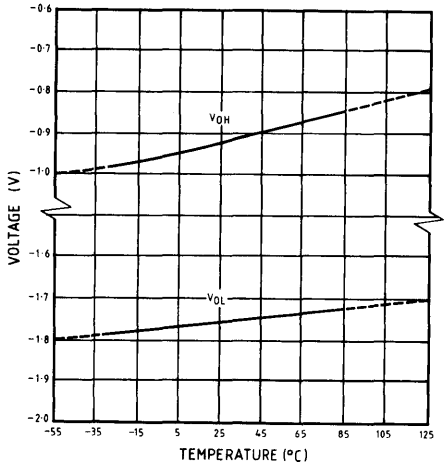


Fig.13 Output levels as a function of temperature

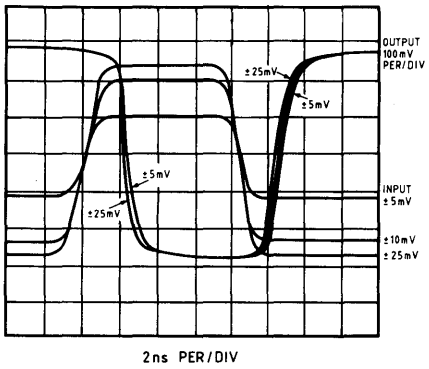


Fig.14 Response to various input signals levels

PLESSEY
Semiconductors

SP9754

HIGH SPEED FOUR BIT EXPANDABLE A TO D CONVERTER

The SP9754 is a fast 4 bit A-D converter, expandable up to 8 bits without additional encoding circuitry.

It can convert at sample rates from DC to 110 MHz, with analog inputs up to Nyquist frequencies. All output levels are ECL compatible

The latch function to the device provides on-chip sampling which allows the converter to operate without an external sample and hold. Data is clocked through the device in master/slave fashion, ensuring that all outputs are synchronous.

The SP9754 operates from a +5V, -7V supply.

FEATURES

- Operating Temperature Range -30°C to +85°C
- No External Components For 4-Bit Conversion
- 110MHz Conversion Rate
- On-Chip Encoding For Expansion to 8 Bits
- No External Sample and Hold Needed
- On-Chip Resistor Reference Divider
- Bit Size 10-100mV
- ECL Compatible
- Over 100MHz Full Power Bandwidth
- 10ps Aperture Uncertainty Time
- 8-Bit Accuracy (When Expanded)

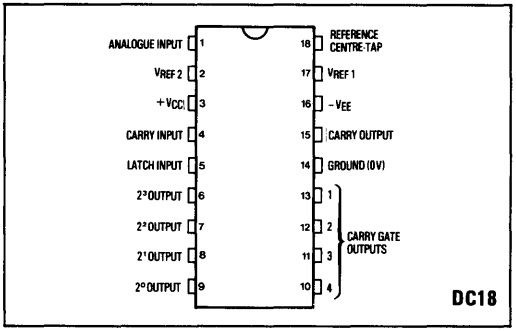


Fig.1 Pin connections (top view)

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	-7.5V
Storage temperature range	-55° C to +150° C
Junction operating temperature	<175° C
Lead temperature (soldering 60 sec)	300° C

ORDERING INFORMATION

SP9754DC (Commercial - side brazed ceramic package)
SP9754BB DC (Plessey High Reliability Specification)

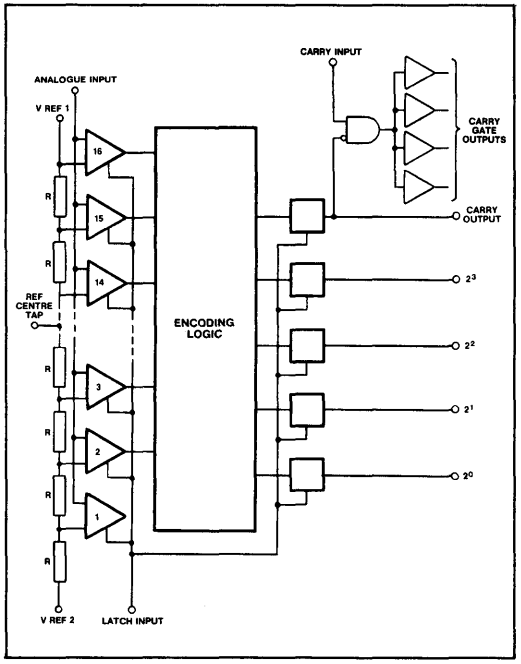


Fig.2 Functional diagram

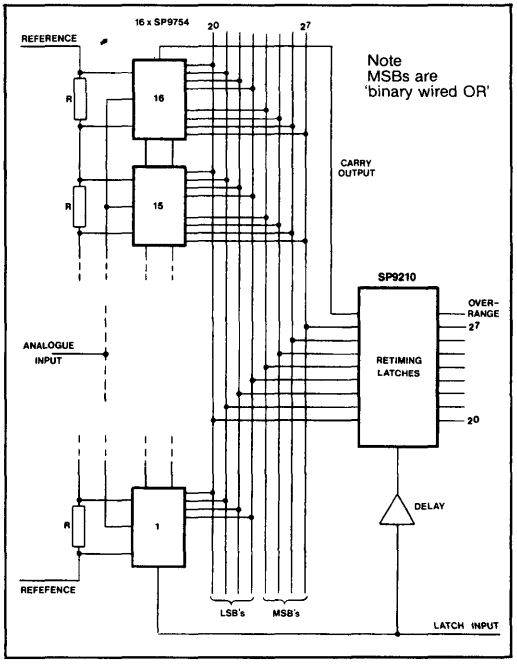


Fig.3 8-bit all-parallel system

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{AMB} = 25°C
V_{CC} = +5V ±0.25V
V_{EE} = -7V ±0.25V
R_L = 100 ohms to -2V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Analog input current	I_B		30	100	μA	V_{IN} = 0V
Analog input capacitance	C_{IN}		10		pF	
Common mode range	V_{CM}	-2		+2	V	
Maximum input slew rate			1000		V/μsec	
Latch input capacitance	C_{IN}		2		pF	
Positive supply current	I_{CC}		55	70	mA	See Fig.11
Negative supply current	I_{EE}		85	100	mA	See Fig.11
Reference resistor chain			25		Ω	total
Reference bit size		10		100	mV	
Comparator offset voltage	V_{OS}	-5		+5	mV	
Total power dissipation	P_{DISS}		950	1160	mW	All outputs loaded
Input & output logic levels						
Logic high	V_{OH}	-0.930		-0.720	V	for 100 ohm load
Logic low	V_{OL}	-1.90		-1.620	V	to -2V
Min. latch set-up time	ts		1.5	2	nsec	10mV overdrive
Latch to output propagation delay:						
Latch enable to output high	t_{pd} + (E)		6	8	nsec	
Latch enable to output low	t_{pd} - (E)		5	8	nsec	
Carry input to MSB delay	t_{pd} (C)		3	5	nsec	
Max. sample rate	$F_{c\,max.}$	100	110		MHz	
Aperture uncertainty time	ta		10		psec	

Thermal characteristics θ_{JA} = 85° C/W
θ_{JC} = 16° C/W

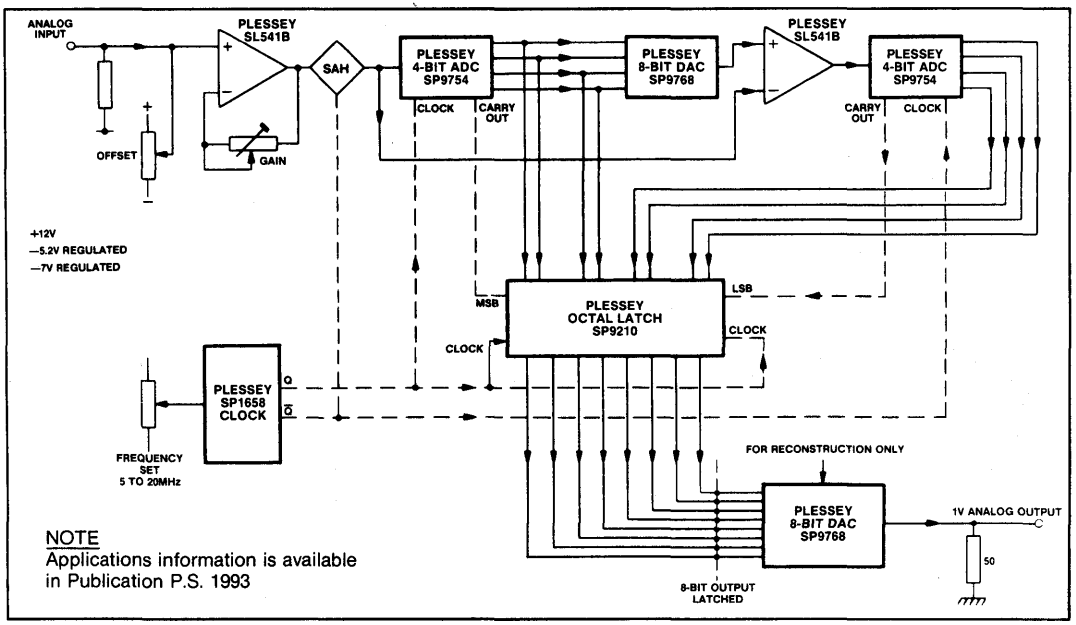


Fig.4 Subranging or parallel-series-parallel system

PERFORMANCE CURVES

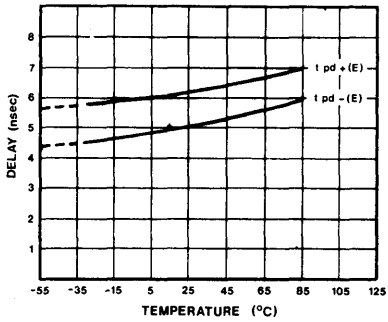


Fig.5 Latch to output propagation delay as a function of temperature

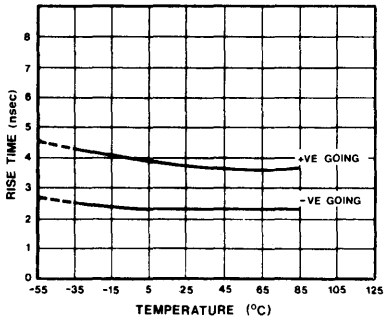


Fig.6 Output rise/fall times as a function of temperature

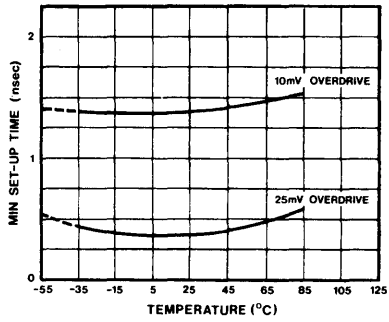


Fig.7 Set-up time as a function of temperature

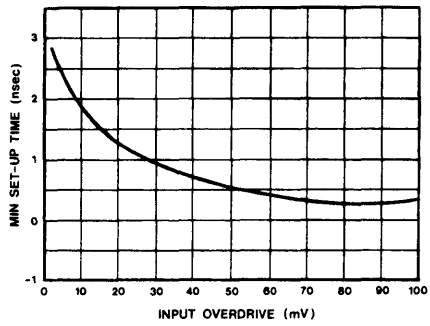


Fig.8 Set-up time as a function of overdrive

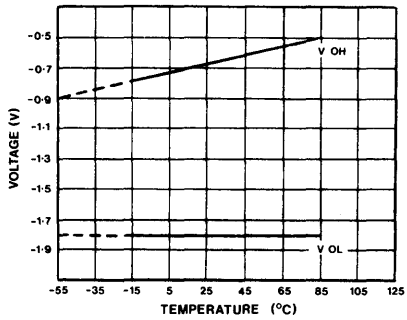


Fig.9 Output logic levels as a function of temperature

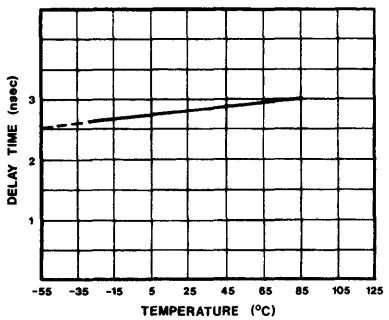


Fig.10 Carry input to MSB output delay as a function of temperature

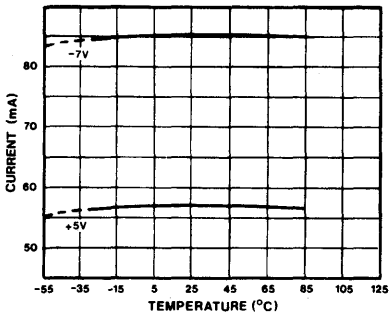


Fig.11 Supply current as a function of temperature

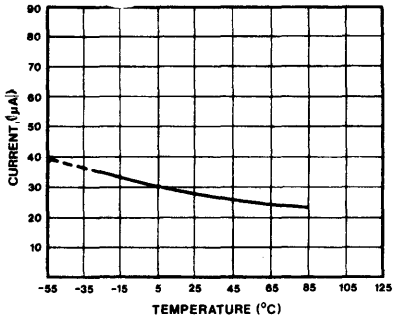


Fig.12 Analog input current as a function of temperature

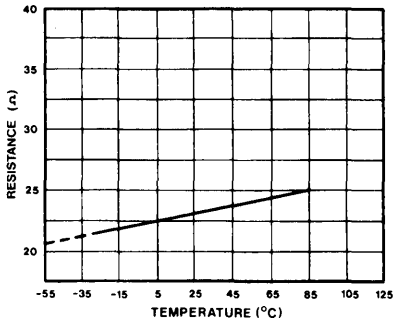


Fig.13 Network resistance as a function of temperature

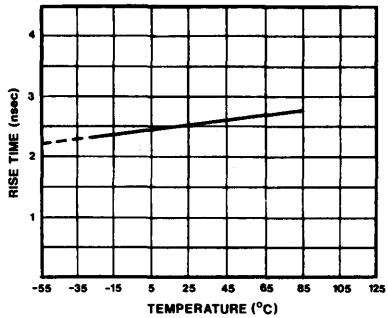


Fig.14 MSB output edge speeds as a function of temperature

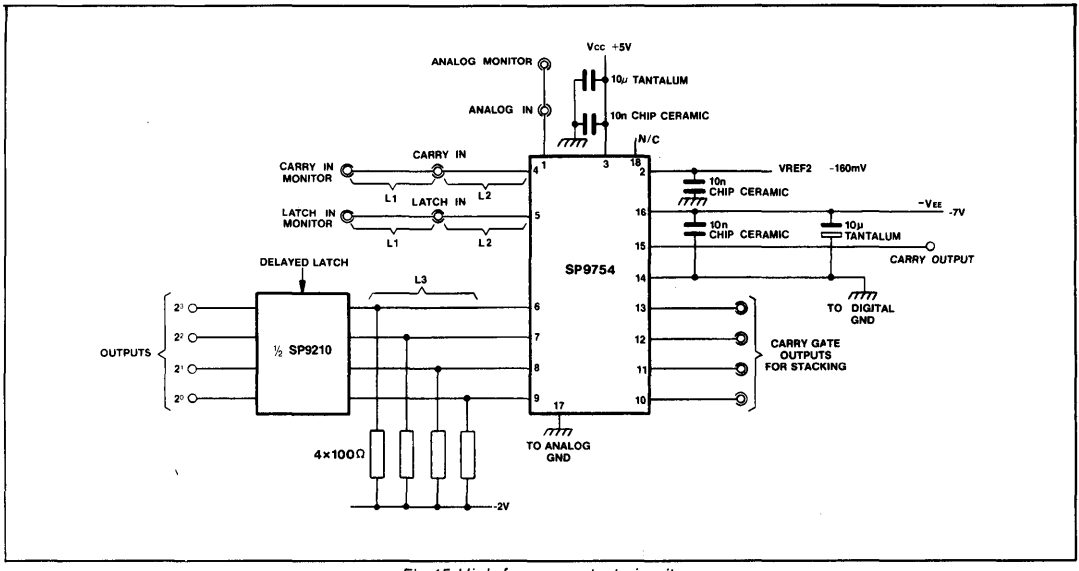


Fig.15 High frequency test circuit
NOTE At latch frequencies below 60MHz the SP9210 can be ommitted.

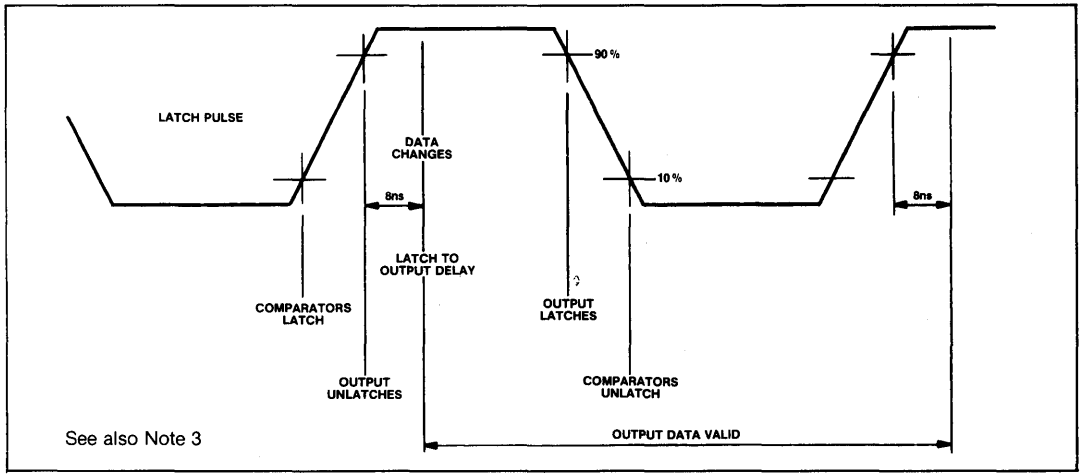


Fig.16 Timing diagram

OPERATING NOTES

1. Carry output (pin 15) is high when the analog input exceeds the top reference voltage (pin 17).

Then the carry gate outputs (pins 10 to 13) go low regardless of carry input (pin 4). When the analog input is between V_{REF} and V_{REF2} and the carry output is low, the carry gate output will be high if the carry input is also high. Similarly if the carry input is low then the carry gate outputs will be low.

2. When used in an ambient temperature in excess of 75° C the SP9754 must be provided with an external electrically isolated heatsink or forced air cooling. This will ensure that the junction temperature does not exceed 175° C.

3. At operating clock frequencies above 60MHz clock edges should have rise and fall no faster than 4nsec.

SP9756-6 EXP

6-BIT HIGH SPEED ADC

The Plessey SP9756-6 is a 6-bit flash ECL analog-to-digital converter. It incorporates 64 individual comparators, a clock driver circuit reference chain and a D-type output latch. This flash ADC is capable of sampling in excess of 100MHz, with a wide analog bandwidth and good dynamic performance.

A variety of features have been included within the device to benefit both flexibility and simplicity of system design.

FEATURES

- Monotonic over the Full Frequency Range
- 110MHz Conversion Rate (130MHz Typ)
- Full Power Bandwidth 250MHz (To -3dB) at 1V Input
- 50MHz Bandwidth to High Accuracy
- Operates on a Single -5.2V Supply
- Internal ECL 6-Bit Latched Output (7ns Minimum Valid Data at 100MHz)
- No External Latch Required
- On-Chip Band-Gap Reference for Good Temperature Stability
- No External Clock Buffer Needed (Provided Internally)
- No External Sample and Hold Needed
- On-Chip Reference Chain
- Sense Outputs for Precision Reference Voltage Setting
- Mode Input to Program Over-Range Condition
- Low Propagation Delay (3ns Typ.)

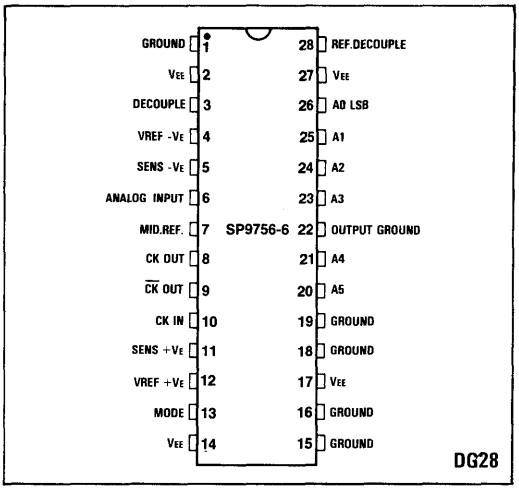


Fig.1 Pin connections (top view)

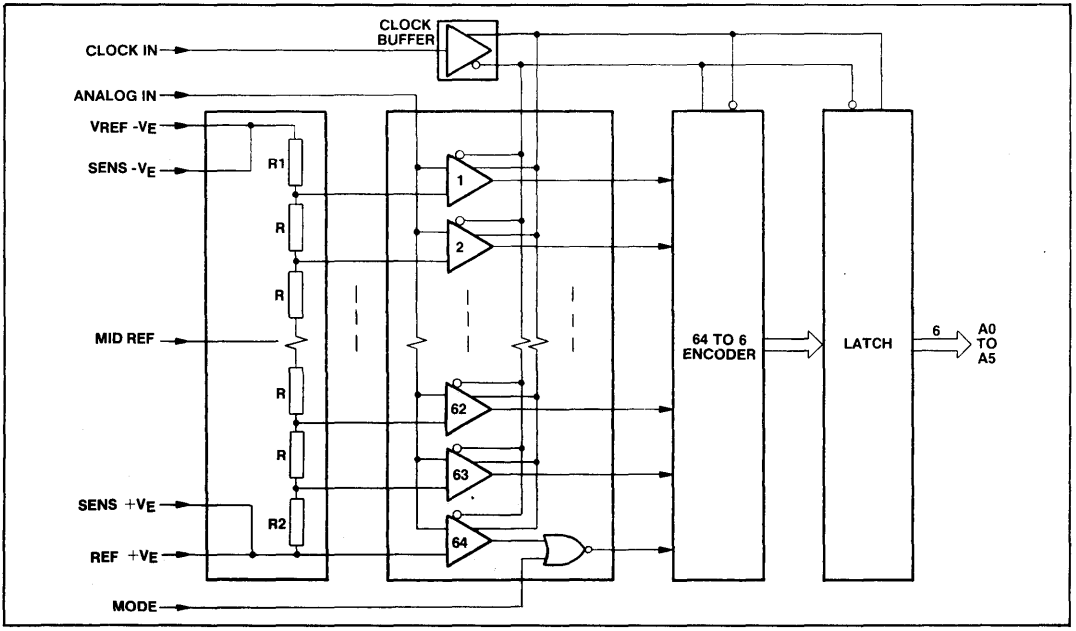


Fig.2 SP9756-6 functional block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25° C, V_{EE} = -5.2V ± 0.25V

Characteristic	Pin	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply current, I_{EE}			-220	- 270	mA	Excludes ECL O/P & ref. currents
Supply voltage, V_{EE}	2	- 4.5		- 5.5	V	
Dynamic range				2	V	Degrades below -30° C
				1	V	-31° C to -55° C
Analog input capacitance			20		pF	
Analog input current				0.8	mA	
Minimum reference bit size			8		mV	
Power dissipation			1.4	1.8	W	Outputs loaded
Differential linearity at 7kHz input				±½	LSB	1V p-p input, 100MHz clock, measured using histogram test. See Figs. 5 to 8 and reference 1 measurement techniques.
at 50MHz input				±¾	LSB	
Integral linearity at 7kHz input				±½	LSB	
at 50MHz input				±½	LSB	
Aperture jitter			25		ps	
Full power 3dB bandwidth			250		MHz	
S/N ratio (RMS) at 50MHz analog, 101MHz sample rate		32			dB	
Data out A_0 to A_5	20-21, 23-26					
O/P V_{HIGH}			-0.9		V	
O/P V_{LOW}			-1.8		V	
R_{Chain}	3,12		25		Ω	
V_{mode} High	13	-50		+100	mV	All zero's over-range
V_{mode} Low	13	$-V_{EE}$		-0.500	V	All one's over-range
Sample rate	10	110	130		MHz	No missing codes
T_{data}		7			ns	
t_{prop}			3		ns	
t_1				1.5	ns	
t_{sto}			1.2		ns	

ABSOLUTE MAXIMUM RATINGS

Clock & Mode input	0V to -3.5V
Supply voltage	-7V
Maximum junction temperature	175° C
Storage temperature range	-55° C to +150° C
Thermal characteristics	
θ_{JA}	40 deg C/W (typ)
θ_{JC}	15 deg C/W (typ)
T_{amb}	-40° C to +70° C (still air)
T_{amb}	-55° C to +125° C (in 500LFPM of air across package)

OPERATING NOTES

Analog Input

The input voltage range is 0.0V to -2.0V. Optimum performance is achieved with an input of 1V p-p i.e. DC offset to -0.5V for symmetrical limiting.

The input capacitance is of the order of 20pF therefore the source impedance should be low. The device is specified using an input drive from a 50Ω generator into a 50Ω termination resistor, i.e. 25Ω looking out of the device. The 25Ω should be considered as a maximum source impedance.

Reference Voltage

For optimum performance REF +VE (pin 12) should be connected to 0V (analog GND) and REF -VE (pin 4) to a -1V supply. This supply should be decoupled with a good quality, high frequency capacitor to the analog GND. The maximum REF voltage difference is -2V for an undistorted output, although the analog bandwidth of the ADC may be adversely affected above 1V p-p reference voltage. The minimum recommended REF voltage difference is 0.5V, below this the linearity of the device will be adversely affected.

An input signal above V_{REF} +VE will give an 'all ones' output provided that pin 13 is connected to -2V (see mode input).

Sense pins (SENS +VE, pin 11 and SENS -VE, pin 5) are available on both REF +VE and REF -VE. These allow Kelvin applied voltages to be used for precision setting of the reference chain.

The reference chain can be used dynamically for applications using AGC. When doing so a low impedance drive should be used.

Clock Input

As the SP9756 features an internal differential clock driver, a single ended ECL clock drive signal is suitable. The outputs of this drive are available on pins 8 and 9 (not ECL levels).

The aperture uncertainty of the device is in the order of 25ps, so the clock signal should have low edge jitter to be compatible.

Clock Timing

The first sample of the analog input is taken approximately 1.2ns after the rising edge of the clock. The input comparators then latch, holding their state until the falling edge.

When the SP9756 receives the first falling edge the device commences decoding and the input comparators are released. The binary data becomes available at the outputs 3.5ns after the second rising edge of the clock.

The SP9756 incorporates an output D-type latch. The data out from this latch is valid for over 70 % of the clock cycle, at 100MHz. This greatly simplifies data acquisition of the binary information, as timing is not so critical as with many ADCs.

Mode Input

The MODE input (pin 13) selects the output code when V_{IN} is higher than REF +VE. For normal operation this pin should be connected to -2V. The SP9756 will then give an all ones output for any input greater than REF +VE. If the mode input is tied to GND the device will give all zeros when the input is higher than REF +VE.

CIRCUIT BOARD LAYOUT

As with most PCB layouts for analog-to-digital conversion, the best performance from the SP9756 can be achieved by separating the ground plane into two sections, analog GND, and digital GND. This aids the device performance by reducing the amount of digital switching noise fed back into the analog section of the converter.

The digital noise is produced mainly by the ECL binary outputs, which ideally should be terminated through a 100 Ω load to a -2V supply.

The device supplies are also a source of digital feedback, as they can be modulated by the digital output current. Therefore it is wise to decouple the SP9756 close to the device supply pins with good quality high frequency capacitors. It is also advisable to direct the current returned from the output load towards pin 22 and away from other digital grounds. One way of achieving this is by creating a second digital ground plane which should connect to the main digital ground at pin 22 of the device, the ground connection between the ADC and the device aquiring the data is then made to this second digital ground plane.

The following should be referred to the digital GND: V_{EE}, REF decouple (pin 20), -2V supply for output termination, clock termination, device GND pins 1, 15 and 22.

The following should be referred to the analog GND: Ref +VE, REF -VE, input termination or buffer.

MEASUREMENT TECHNIQUES

Reference 1

Refer to: *Dynamic Performance of A to D Converters, Hewlett Packard Product Note 5180A-Z.*

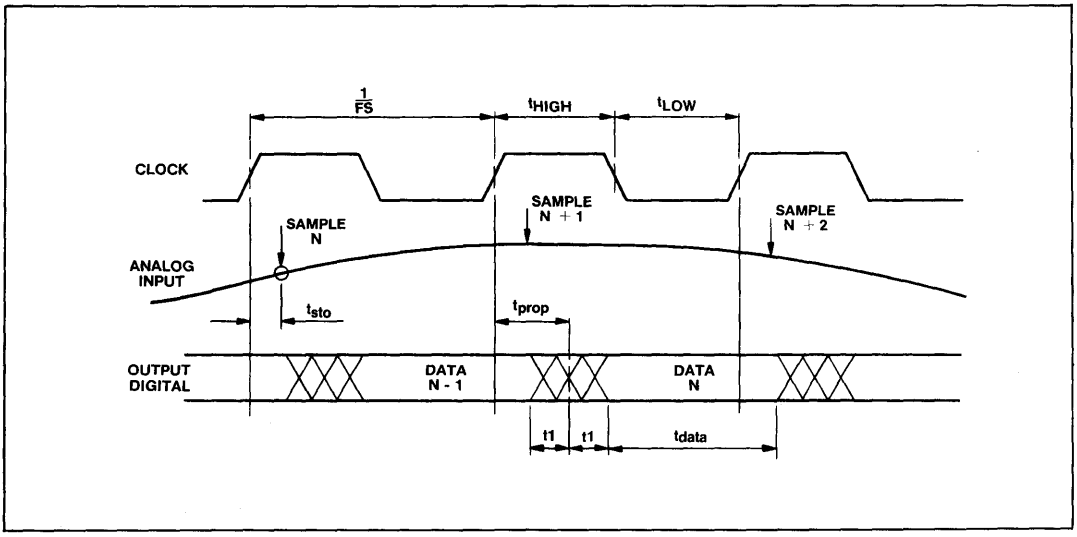
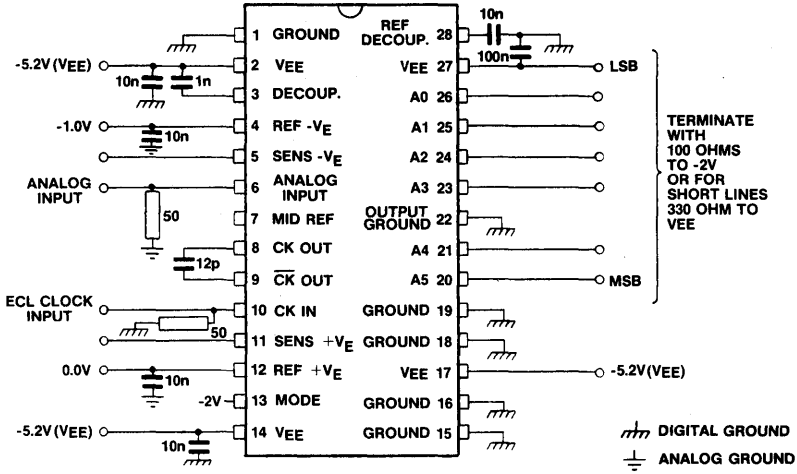


Fig.3 Timing diagram



NOTES ON APPLICATION

1. MODE drives output either 'all zeros' or 'all ones' on over-range.
2. Kelvin connections can be made to the reference chain via SENS (+VE) and SENS (-VE).
3. REF DECOUPLE (Pin 28) gives access to DC bias reference for logic. This gives ability to eliminate possible crosstalk by allowing capacitor to remove edge noise.
4. Keep OUTPUT GROUND separate from GROUND.

Fig.4 Test and applications circuit

TYPICAL LINEARITY DATA

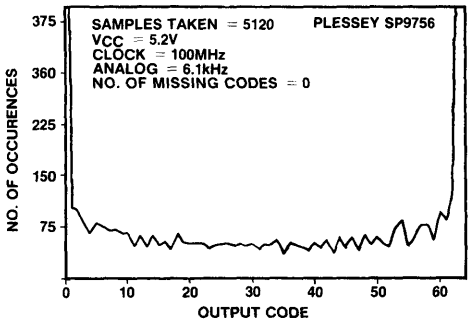


Fig.5 Histogram (state occupancy test)

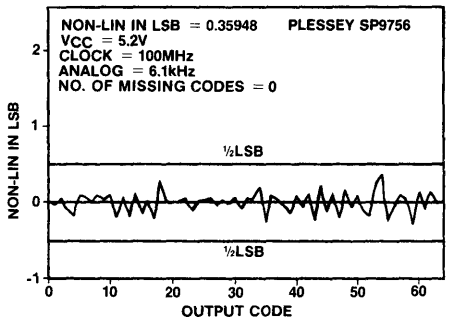


Fig.6 Differential linearity in LSB

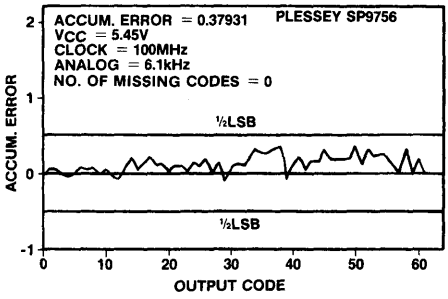


Fig.7 End point integral linearity

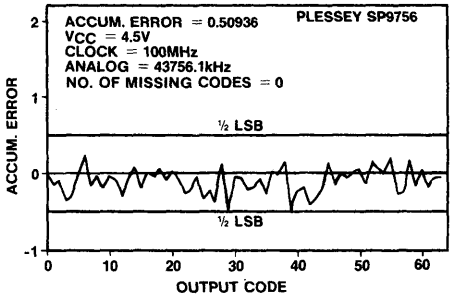


Fig.8 End point integral linearity (near Nyquist input frequency)

PLESSEY Semiconductors

ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SP9768

8-BIT HIGH SPEED MULTIPLYING D-A CONVERTER

The SP9768 is an ECL 10K compatible 8-bit DAC. The 5nsec settling time allows a 150 megasample per second conversion time. An inherently low glitch design is used and the complementary current outputs are suitable for direct transmission line drive. The SP9768 design includes a high performance voltage reference and reference amplifier.

Both current and voltage multiplying modes are available.

FEATURES

- 5ns Settling Time 1 LSB Typically
- 8 Bits ±½ LSB Integral and Differential Linearity
- Current Output
- Operating Temperature Range -30°C to +85°C
- ECL 10K Standard Inputs
- Complementary Outputs, 20mA Full Scale
- Reference Temperature Coefficient Typically 40ppm/°C

ORDERING INFORMATION

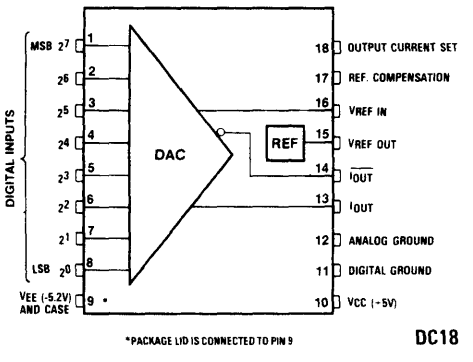
SP9768DC (Commercial - side brazed ceramic package)
SP9768BB DC (Plessey High Reliability Specification)
SP9768LC (Under development) (LCC)

APPLICATIONS

- Data Conversion
- Video Graphic Displays
- Instrumentation
- Waveform Generators
- High Speed Modems
- ADC Evaluation

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	-5.7V
Digital input voltage	0 to -4.5V
Minimum R_{SET} (from 0V)	175Ω
Maximum R_{SET}	2.5kΩ
Output reference supply (V_L)	0 to +3V
Reference input	±2V
Storage temperature range	-55°C to +150°C
Operating junction temperature	<175°C
Lead temperature (soldering 60 sec)	300°C



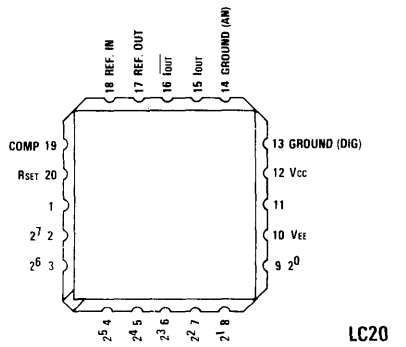


Fig.1 Pin connections - top view

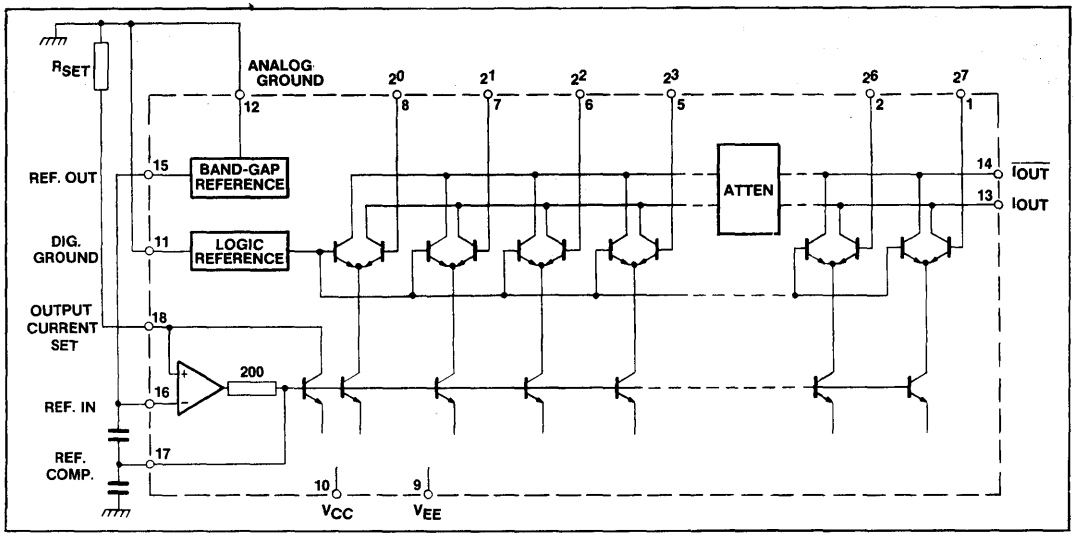


Fig.2 SP9768 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25°C; V_{CC} = +5.00V ± 5%; V_{EE} = -5.2V ± 5%; R_{SET} = 240Ω; Input voltage: High = -0.81V, Low = -1.85V

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply current I_{CC}	7.0	12.0	20.0	mA	All inputs at
Supply current I_{EE}	55.0	66.0	30.0	mA	-1.8V
Logic inputs:					
V_{IH}	-0.96		-0.81	V	Standard ECL
V_{IL}	-1.85		-1.65	V	10K compatible
$I_{IN(HI)}$		115	200	μA	All inputs HI
Reference voltage V_{REF}	-1.250	-1.280	-1.300	V	
Reference voltage temp. coeff.		40	80	ppm/°C	-30°C to +85°C
Output current - full scale	2		30	mA	R_{SET} 175 - 250Ω
Output current - full scale	20.2	21.3	22.4	mA	R_{SET} = 240Ω
Output compliance	-1.0		+1.0	V	T_{amb} = 25°C See
	-0.7		+1.0	V	T_{amb} = 85°C Note 4
Bit size (LSB)	78.9	83.2	87.5	μA	Current output
Resolution	8			Bits	
	0.391			%	
Integral non-linearity			0.5	LSB	
Differential non-linearity			0.5	LSB	
Output dynamic parameters (see Note 1)					
Rise time		1.2	2.0	ns	10 to 90%
Settling time - full scale		5	10	ns	To 1 LSB
Glitch energy		90	150	psV	Mid-point
Glitch duration			4	ns	transition
Noise output		-90	-83	dBm	See Note 2
Multiplying mode - voltage (see Fig.5) (See Note 1)					
Multiplying input voltage range	-2		0	V	
Reference input resistance		10		kΩ	
Multiplying input bandwidth		200		kHz	-3dB see Note 3
Transfer function non-linearity		0.2	1.0	%FS	DC

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Multiplying mode - current (see Fig.6) (See Note 1)					
Multiplying input current range	0.5		8.0	mA	
Set current input resistance		400		Ohms	
Multiplying input bandwidth		20		MHz	-30dB
Transfer function non-linearity		1.0	3.0	%FS	DC

NOTES
1. Dynamic parameters guaranteed but not 100% tested.
2. Noise in any 10kHz band in the range 0.1 to 500MHz, for any digital input.
3. Voltage-mode multiplying bandwidth is limited by the reference compensation capacitor on the loop amplifier output (pin 23). For the minimum recommended value of 3.9nF, the -3dB point is typically 200kHz. However, the loop amplifier output slew rate is asymmetrical at high frequencies; the maximum frequency at which no significant distortion is introduced is typically 35kHz.
4. The output positive compliance can be increased beyond +1.0V at the expense of linearity. See Fig.4 for circuit configuration.
5. Analog and digital grounds should be connected together at the device pins (pin 11 and pin 12).

Thermal characteristics $\theta_{JA} = 85°$ C/W
$\theta_{JC} = 16°$ C/W

OPERATION

The pinout of the device is shown in Fig.1. External components are the current setting resistor and decoupling capacitors.

The DAC has current outputs, with a nominal full-scale of 20mA, corresponding with a 1 volt drop across a 50Ω load.

The actual output current is determined by the on-chip reference voltage and an off-chip current setting resistor. Output current, I_{OUT}, is given by

$$I_{OUT} = 4 \times \frac{V_{REF}}{R_{SET}} \text{ at full scale}$$

A complementary I_{OUT} is also provided. If single output operation only is employed it must be ensured that the complementary output is terminated in an identical manner to the used output. The setting resistor, R_{SET}, is typically 240Ω, giving a full-scale output current of 21mA, and should have a temperature coefficient similar to that of the output load resistor.

The reference voltage source is nominally -1.280 volts and is of a modified bandgap type. Samples show average temperature coefficients of 50ppm/° C over the range -55° C to +125° C. This precision voltage reference can be used as an independent part.

The reference supply is internally compensated; however, to reduce the possibility of instability or noise generation, pin 21 should be decoupled as shown in Fig.4. The current loop technique has been used with a high performance loop amplifier. The current is set by an external resistor as described above. Stabilisation of the loop amplifier is achieved by a single capacitor from pin 23 to ground. Minimum value is 3900pF, although a 10nF chip ceramic is recommended.

Fig.3 shows a suggested circuit for a conventional D to A using the on-chip voltage reference.

RECOMMENDATION

For low output noise it is best to use a chip capacitor on pin 23 to the 0V (GND) plane. The use of split analog and digital ground planes for this device is not recommended. Eurocard construction is not recommended. Ringing or time skew on digital inputs should be avoided.

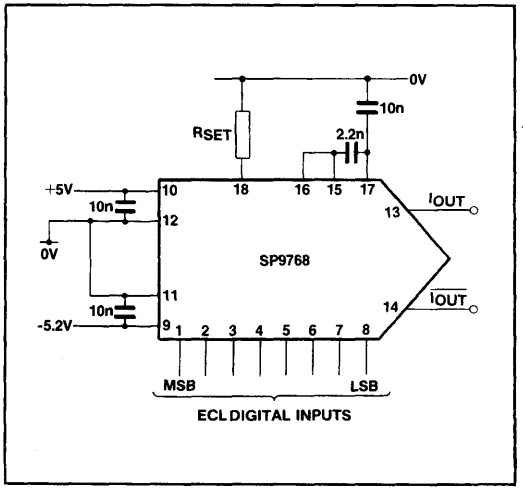


Fig.3 Conventional D/A operation using on-chip reference

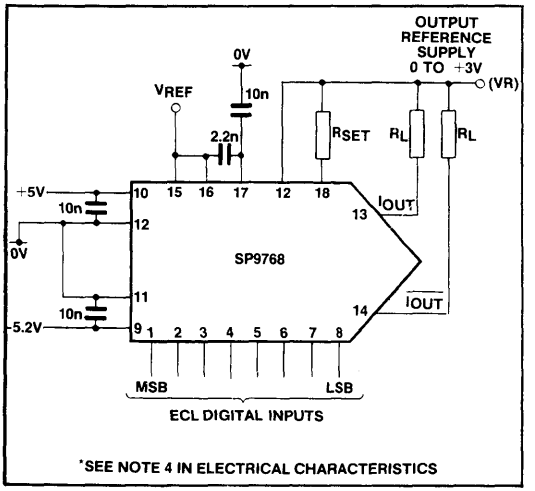


Fig.4 Voltage output referred to a positive voltage

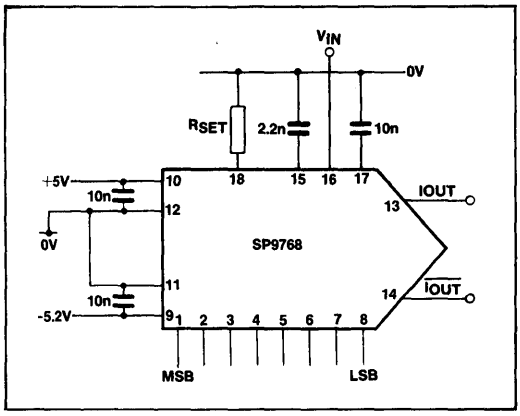


Fig.5 Multiplying mode operation (voltage mode)

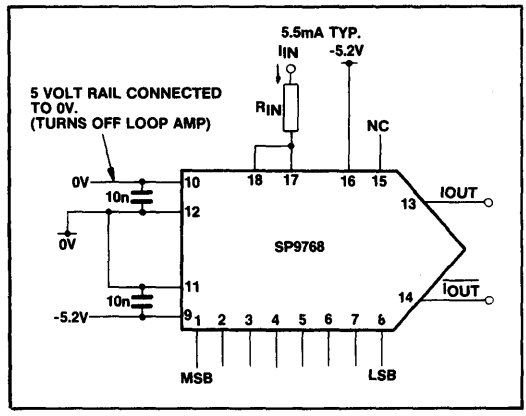


Fig.6 Multiplying mode operation (current mode)

OPERATING NOTES

Output Compliance

Fig.4 shows the method of using the SP9768 with a load resistor not referred to ground, allowing a larger output swing than the conventional connection of Fig.3. Connecting pin 12 and the current setting resistor R_{SET} to the load reference supply ensures that the scale factor of the output is independent of the load reference.

As pointed out in Note 4 of the Electrical Characteristics, extending the compliance beyond +1V may cause sight degradation of linearity.

Multiplying Mode

Multiplying operation of the DAC is available in two modes: either a voltage applied in place of the internal reference, or a current supplied via the current set pin.

Voltage A circuit for using the DAC in voltage multiplying mode is shown in Fig.5. The transfer function is approximately: I_{OUT} (Full Scale) = 4 x V_{IN}/R_{SET}. While this mode offers the best linearity of operation, the frequency response limitations outlined in Note 3 mean that the maximum useable bandwidth is limited to approximately 35kHz.

Current A circuit for using the DAC in current multiplying mode is shown in Fig.6. The transfer function is approximately: I_{OUT} (Full Scale) = 4 x I_{IN}. In this mode the current setting loop amplifier is not used, and any possibility of instability or interference can be averted by turning off the amplifier by connecting V_{CC} to 0V as shown.

The operational bandwidth of the current input to -3dB is at least 20MHz.

A 1V output is obtained into 50 ohm when a current of approximately 5.5mA is fed into pin 17/18 and the input code is selected for full output current.

PLESSEY
Semiconductors

ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SP9770B & C

10-BIT HIGH SPEED MULTIPLYING D-A CONVERTER

The SP9770 is an ECL 10K compatible 10-bit DAC. The 12nsec settling time allows a 75 megasample per second conversion time. An inherently low glitch design is used and the complementary current outputs are suitable for direct transmission line drive. The SP9770 design includes a high performance voltage reference and reference amplifier.

FEATURES

- Operating Temperature Range -30°C to +85°C
- 12ns Settling Time 1 LSB Typically
- **SP9770B** 10 Bits ±½ LSB Integral and ±½ LSB Differential Linearity
- **SP9770C** 10 Bits ±½ LSB Integral and ±1 LSB Differential Linearity
- Current Output
- ECL 10K Standard Inputs
- Complementary Outputs, 20mA Full Scale
- Reference Temperature Coefficient Typically 40ppm/°C

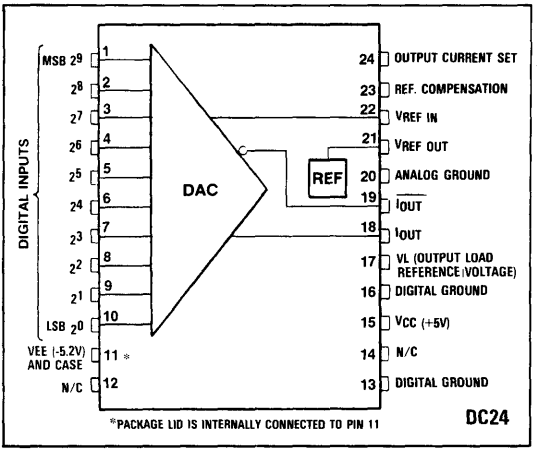


Fig.1 Pin connections - top view

ORDERING INFORMATION

SP9770B DC (Commercial - side brazed ceramic package)
SP9770C DC (Commercial - side brazed ceramic package)
SP9770BB DC (Plessey High Reliability Specification)

APPLICATIONS

- Data Conversion
- Video Graphic Displays
- Instrumentation
- Waveform Generators
- High Speed Modems

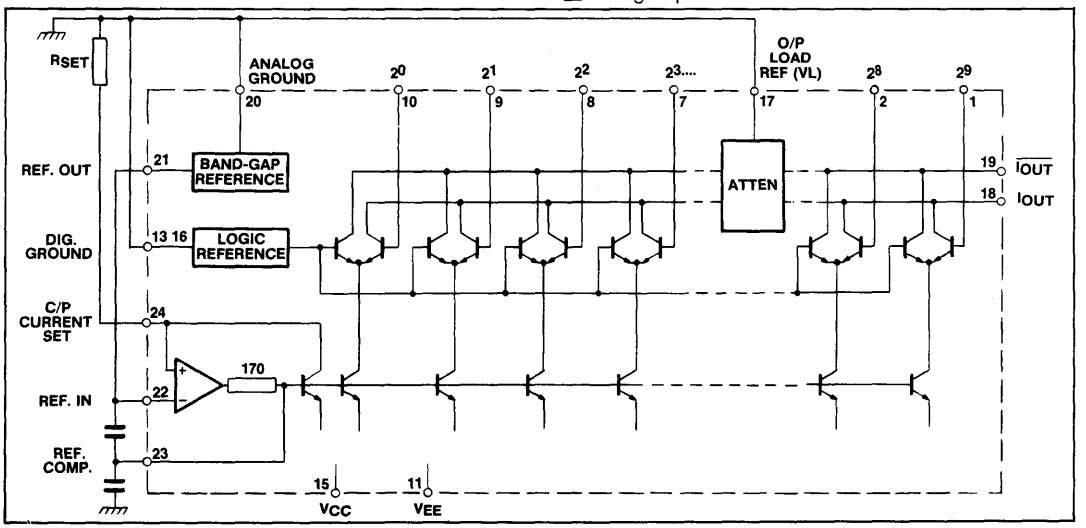


Fig.2 SP9770 block diagram

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V	Output reference supply (V_L)	0 to +3V
Negative supply voltage	-5.7V	Reference input	±2V
Digital input voltage	0 to -4.5V	Storage temperature range	-55° C to +150° C
Minimum R_{SET} (from 0V)	175Ω	Junction operating temperature	<175° C
Maximum R_{SET}	2.5kΩ	Lead temperature (soldering 60 sec)	300° C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25° C; V_{CC} = +5.00V ± 5%; V_{EE} = -5.2V ± 5%; R_{SET} = 240Ω; Input voltage: High = -0.81V, Low = -1.85V

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply current I_{CC}	7.0	12.0	17.0	mA	All inputs at
Supply current I_{EE}	45.0	56.0	70.0	mA	-1.8V
Logic inputs:					
V_{IH}	-0.96		-0.81	V	Standard ECL
V_{IL}	-1.85		-1.65	V	10K compatible
$I_{IN(HI)}$		115	200	μA	All inputs HI
Reference voltage V_{REF}	-1.250	-1.280	-1.300	V	
Reference voltage temp. coeff.		40	80	ppm/°C	-30° C to +85° C
Output current - full scale	2		30	mA	R_{SET} 175 - 250Ω
Output current - full scale	20.2	21.3	22.4	mA	R_{SET} = 240Ω
Output compliance	-1.0		+1.0	V	T_{amb} =25° C See
	-0.7		+1.0	V	T_{amb} =85° C Note 4
Bit size (LSB)	19.7	20.8	21.9	μA	Current output
Resolution	10			Bits	
	0.098			%	
Integral non-linearity			0.5	LSB	
Differential non-linearity			0.5	LSB	SP9770B
			1.0	LSB	SP9770C
Output dynamic parameters (see Note 1)					
Rise time		2.0	3.0	ns	10 to 90%
Settling time - full scale		12	20	ns	To 1 LSB
Glitch energy		90	150	psV	Mid-point
Glitch duration			4	ns	transition
Noise output		-90	-83	dBm	See Note 2
Multiplying mode - voltage (see Fig.5)					
Multiplying input voltage range	-2		0	V	
Reference input resistance		10		kΩ	
Multiplying input bandwidth		200		kHz	-3dB see Note 3
Transfer function non-linearity		0.2	1.0	%FS	DC

NOTES
1. Dynamic parameters guaranteed but not 100% tested.
2. Noise in any 10kHz band in the range 0.1 to 500MHz, for any digital input.
3. Voltage-mode multiplying bandwidth is limited by the reference compensation capacitor on the loop amplifier output (pin 23). For the minimum recommended value of 3.9nF, the -3dB point is typically 200kHz. However, the loop amplifier output slew rate is asymmetrical at high frequencies; the maximum frequency at which no significant distortion is introduced is typically 35kHz.
4. The output positive compliance can be increased beyond +1.0V at the expense of linearity. See Fig.4 for circuit configuration.

Thermal characteristics θ_{JA} = 65° C/W
θ_{JC} = 15° C/W

OPERATION

The pinout of the device is shown in Fig.1. External components are the current setting resistor and decoupling capacitors.

The DAC has current outputs, with a nominal full-scale of 20mA, corresponding with a 1 volt drop across a 50Ω load.

The actual output current is determined by the on-chip reference voltage and an off-chip current setting resistor. Output current, I_{OUT}, is given by

$$I_{OUT} \triangleq 4 \times \frac{V_{REF}}{R_{SET}} \text{ at full scale}$$

A complementary I_{OUT} is also provided. If single output operation only is employed it must be ensured that the complementary output is terminated in an identical manner to the used output. The setting resistor, R_{SET}, is typically 240Ω, giving a full-scale output current of 21mA, and should have a temperature coefficient similar to that of the output load resistor.

The reference voltage source is nominally -1.280 volts and is of a modified bandgap type. Samples show average temperature coefficients of 50ppm/° C over the range -55° C to +125° C. This precision voltage reference can be used as an independent part.

The reference supply is internally compensated; however, to reduce the possibility of instability or noise generation, pin 21 should be decoupled as shown in Fig.4. The current loop technique has been used with a high performance loop amplifier. The current is set by an external resistor as described above. Stabilisation of the loop amplifier is achieved by a single capacitor from pin 23 to ground. Minimum value is 3900pF, although a 10nF chip ceramic is recommended.

Fig.3 shows a suggested circuit for a conventional D to A using the on-chip voltage reference.

RECOMMENDATIONS

For low output noise it is best to use a chip capacitor on pin 23 to the 0V (GND) plane. The use of split analog and digital ground planes for this device is not recommended.

For low glitch output it is essential that the input time skew and ringing is minimised. The Plessey SP9210 is a suitable high speed latch for this purpose.

Eurocard construction is not recommended.

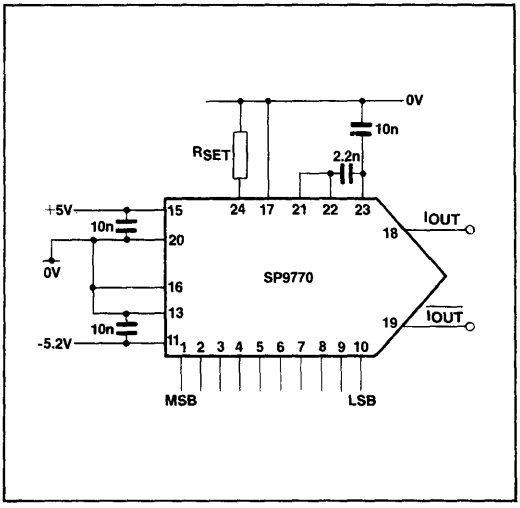


Fig.3 Conventional D/A operation using on-chip reference

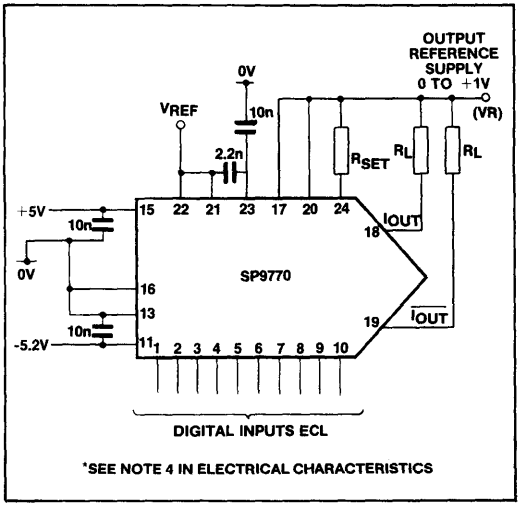


Fig.4 Voltage output referred to a positive voltage for outputs biased above ground

OPERATING NOTES

Output Compliance

Fig.4 shows the method of using the SP9770 with a load resistor not referred to ground, allowing a larger output swing than the conventional connection of Fig.3. Connecting pins 17 and 20, and the current setting resistor R_{SET} to the load reference supply ensures that the scale factor of the output is independent of the load reference.

As pointed out in Note 4 of the Electrical Characteristics, extending the compliance beyond +1V may cause slight degradation of linearity.

Voltage multiplying. A circuit for using the DAC in voltage multiplying mode is shown in Fig.5. The transfer function is approximately: I_{OUT} (Full Scale) = 4 x V_{IN}/R_{SET}. While this mode offers the best linearity of operation, the frequency response limitations outlined in Note 3 mean that the maximum useable bandwidth is limited to approximately 35kHz.

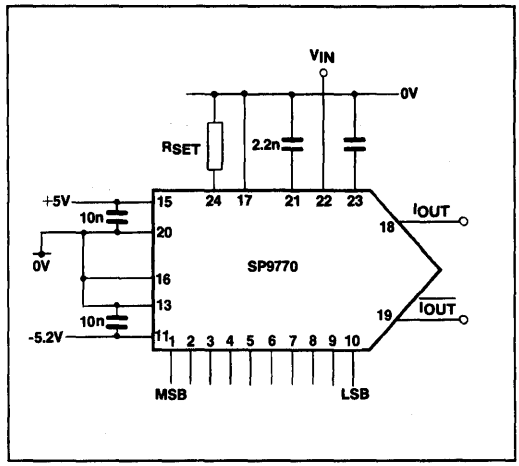


Fig.5 Multiplying mode operation (voltage mode)

PLESSEY
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SP705B

TTL CRYSTAL CONTROLLED INTEGRATED CIRCUIT OSCILLATOR

The SP705B is a square wave oscillator circuit designed to operate in conjunction with an AT cut quartz crystal of effective series resistance less than 300 ohms. Four TTL outputs are provided, related in frequency to the crystal frequency f as follows: f/2, f/4, $\overline{f/2}$ and $\overline{f/4}$. The SP705B is therefore ideally suited to either single or multi-phase TTL clock applications.

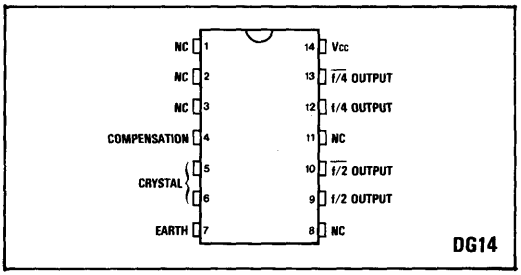


Fig.1 Pin connections

FEATURES

- Operating Frequency up to 10MHz
- f/2 and f/4 Outputs
- 4 TTL Level Outputs
- Operates from +5V TTL Supply

ORDERING INFORMATION

SP705DG (Commercial - Ceramic Package)
SP705BB DG (Plessey High Reliability Specification)

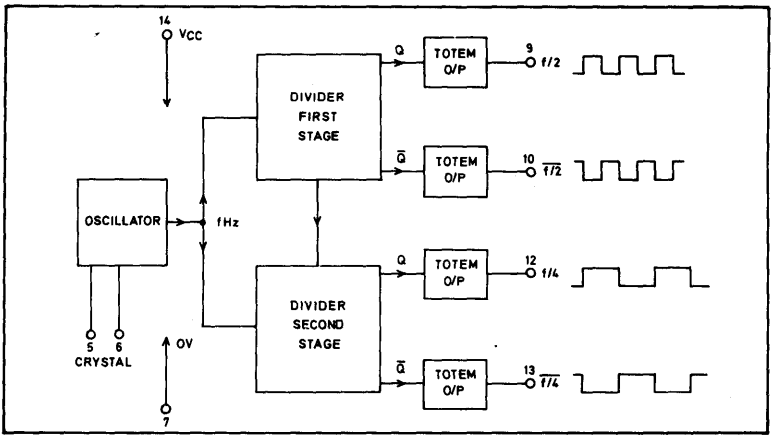


Fig.2 SP705B block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Vcc = +5V

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
High state output voltage	V_{OH}	2.6		V	V_{CC} = 4.75V I_{OH} = 0.2mA
Low state output voltage	V_{OL}		0.4	V	V_{CC} = 5.25V I_{OL} = 8mA
Supply current	I_{CC}		35	mA	V_{CC} = 5V
Output rise time (10 % to 90 %)	t_R		20	ns	V_{CC} = 5V
Output fall time (90 % to 10 %)	t_F		20	ns	V_{CC} = 5V
Operating frequency (f)			10	MHz	
Operating temperature range		0	70	°C	

Thermal characteristics $\theta_{JA} = 125°C/W$
$\theta_{JC} = 40°C/W$

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	| Vcc - GND | 7V
Output current	-16mA
Storage temperature range	-55° C to +150° C
Junction operating temperature	<175° C

CIRCUIT DESCRIPTION

The crystal maintaining circuit consists of an emitter-coupled oscillator, with the emitter resistors replaced by constant-current generators. The crystal is connected, usually in series with a 20pF capacitor, between pins 5 and 6. The 20pF capacitor can be replaced with a mechanical trimmer to allow small changes in frequency to be made, as shown in Fig.3.

The circuit is designed to provide low crystal drive levels - typically, less than 0.15mW at 5MHz. This is well within crystal manufacturers' limit of 0.5mW.

The compensation point, pin 4 is made available so that the compensation capacitance can be increased if necessary. However the 14pF capacitor included on the chip is usually sufficient to prevent spurious oscillation at high frequencies.

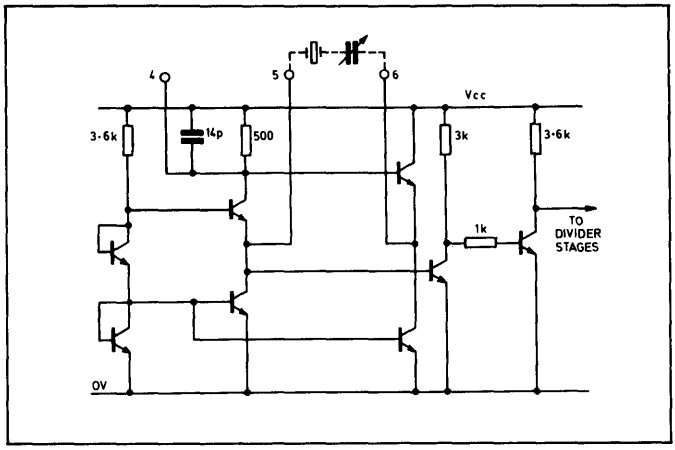


Fig.3 Circuit diagram of SP705B oscillator

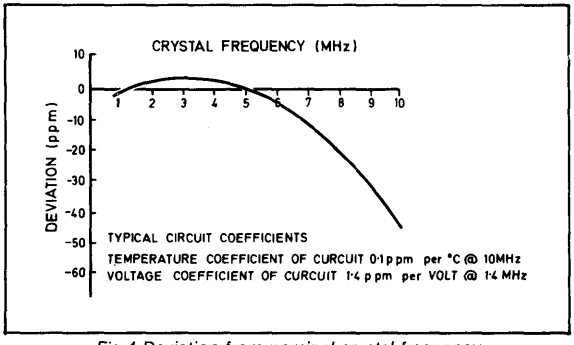
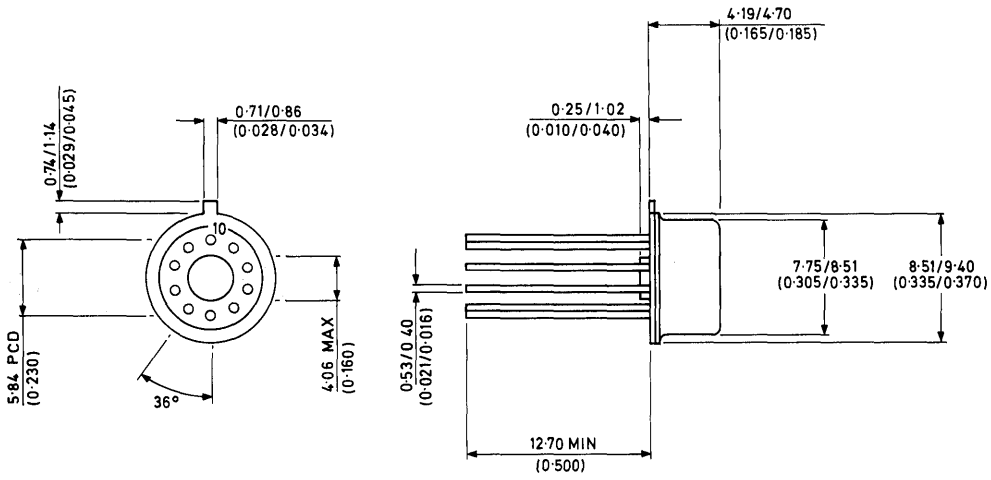
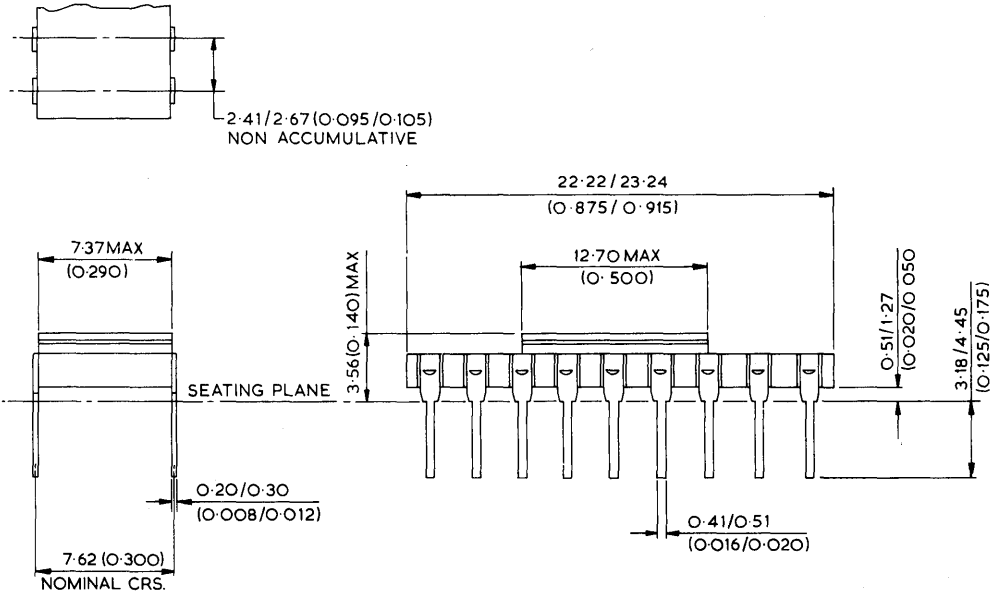


Fig.4 Deviation from nominal crystal frequency

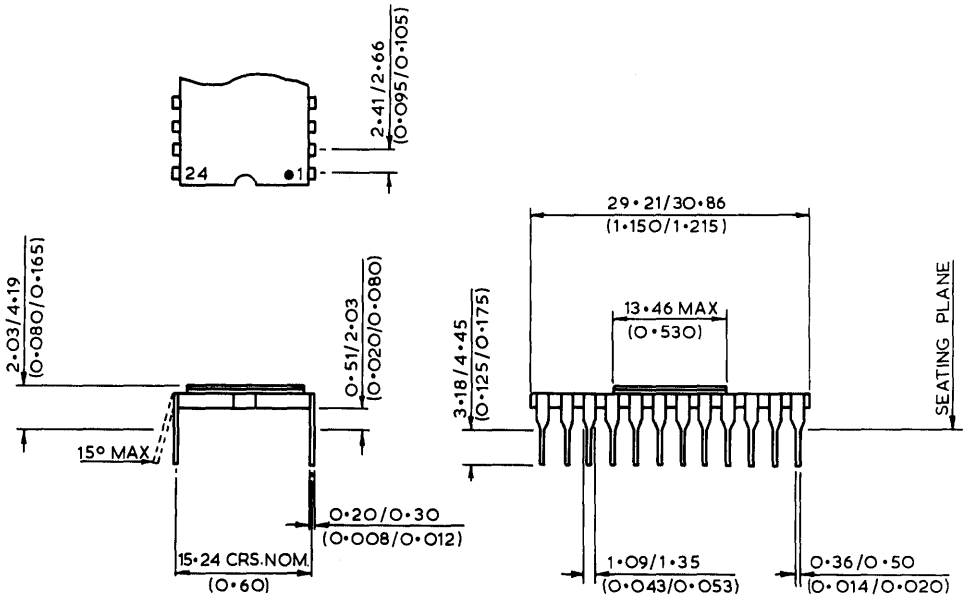
Package Outlines



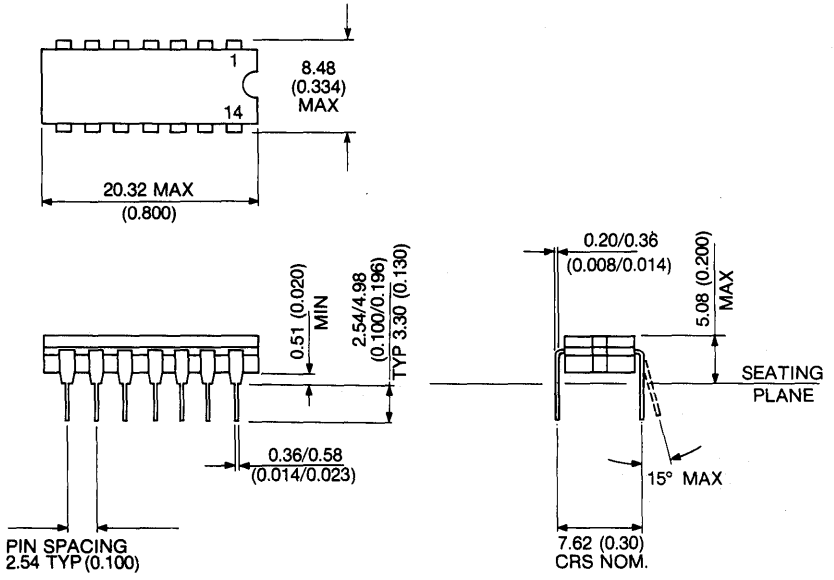
10-LEAD METAL/CERAMIC (5.84mm PCD)
WITH STANDOFF - CM10/S



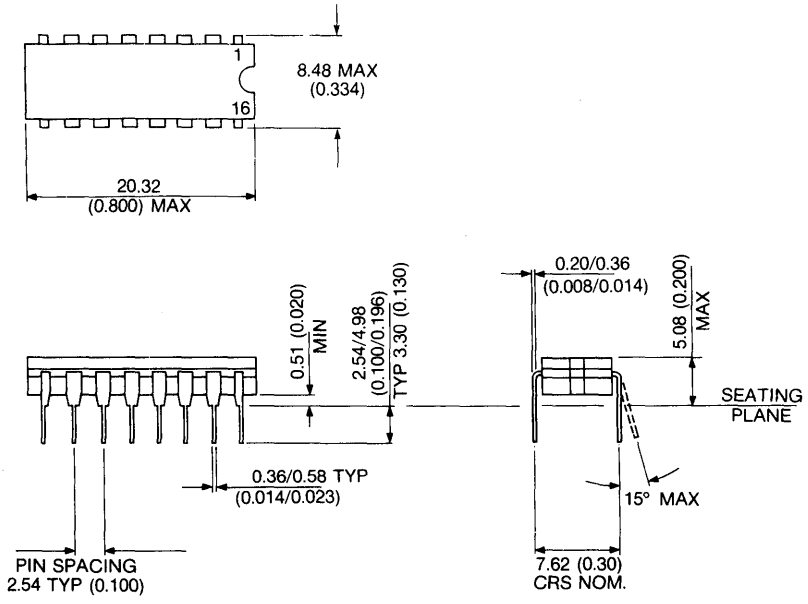
18-LEAD SIDEBRAZED CERAMIC DIL - DC18



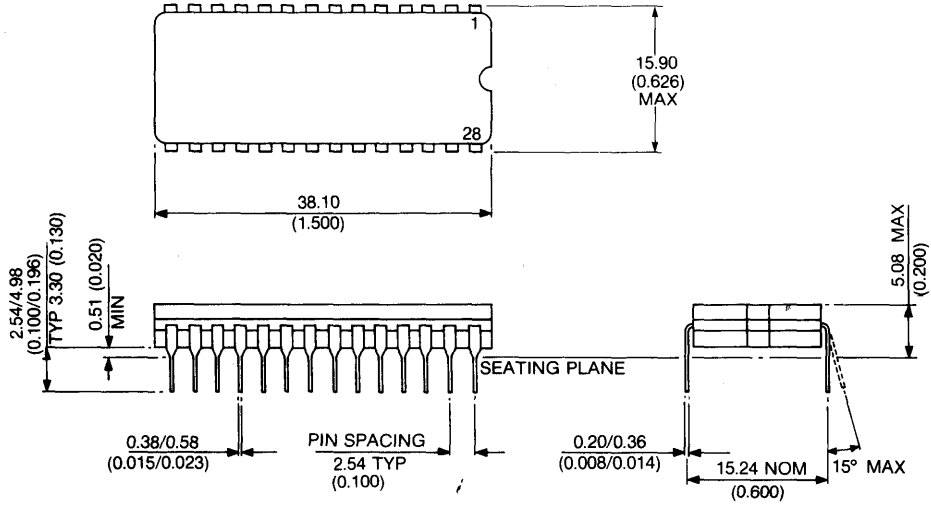
24-LEAD SIDEBRAZED CERAMIC DIL - DC24



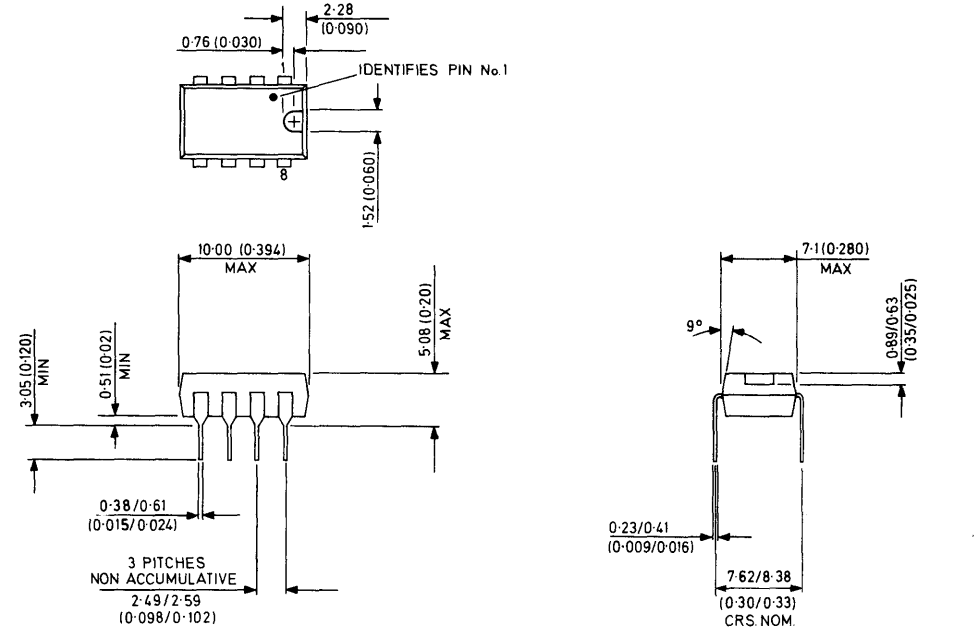
14 LEAD CERAMIC DIL
CERDIP - DG14



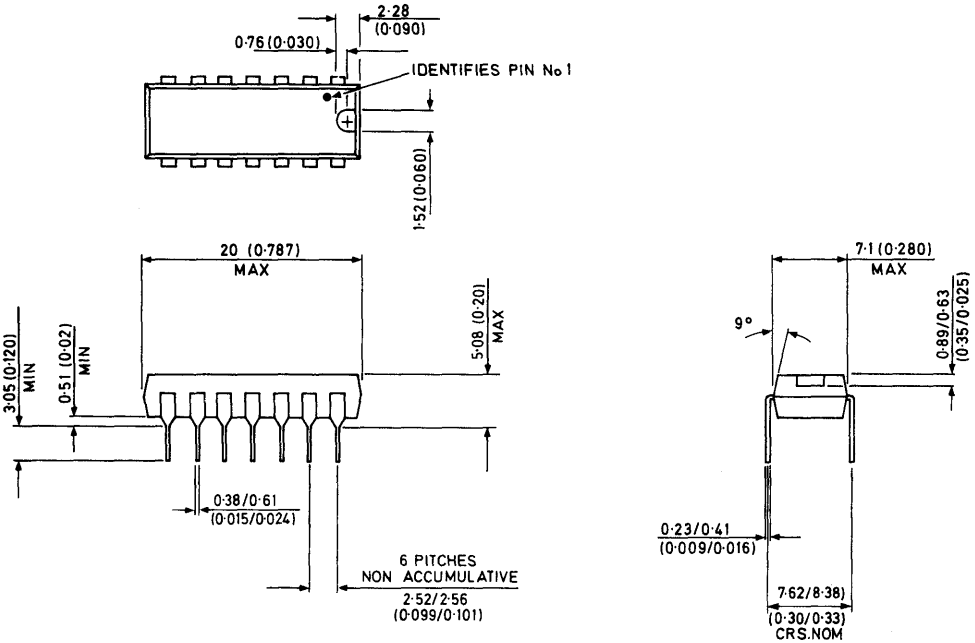
16 LEAD CERAMIC DIL CERDIP - DG16



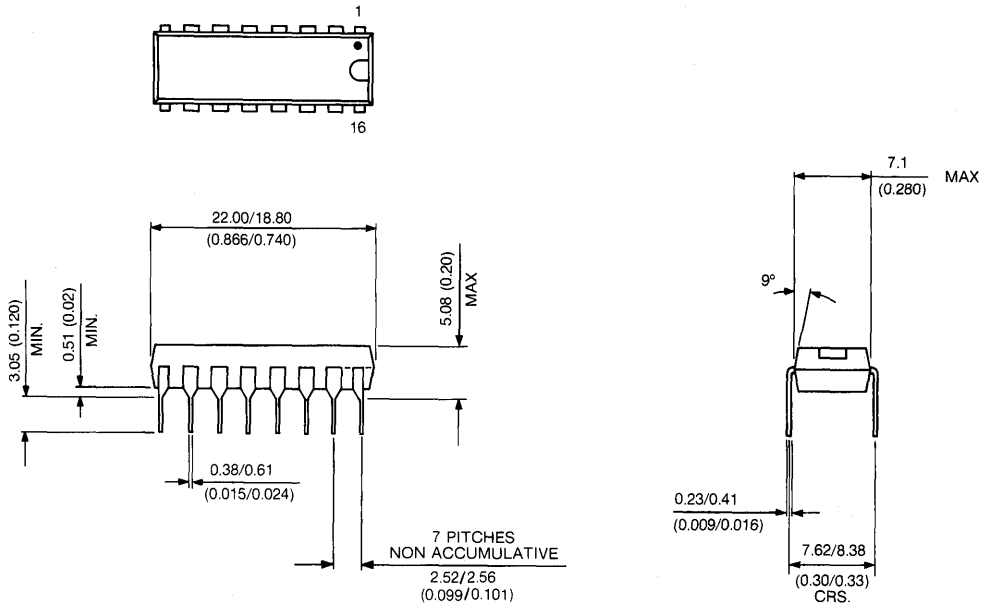
28-LEAD CERAMIC DIL
CERDIP - DG28



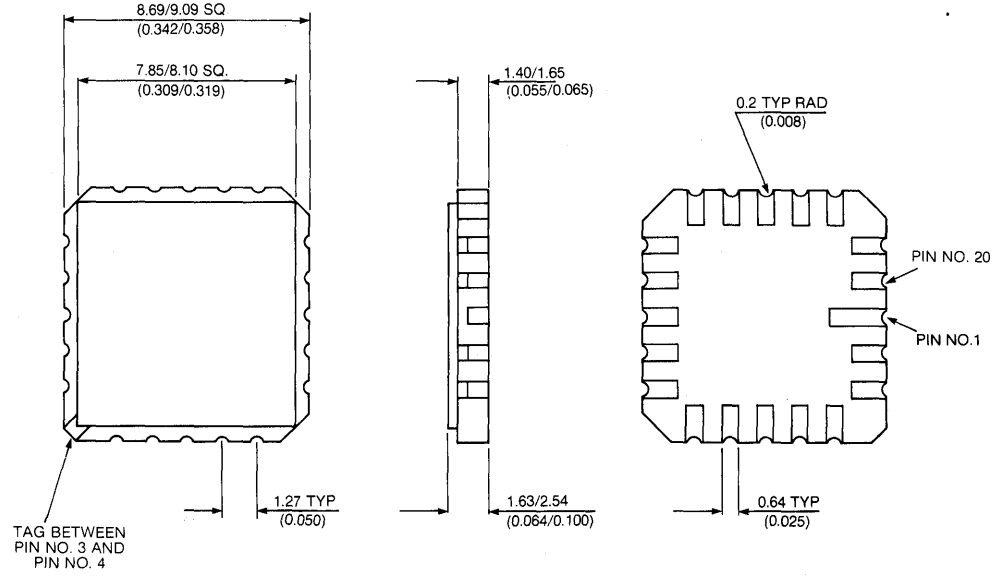
8-LEAD PLASTIC DIL - DP8



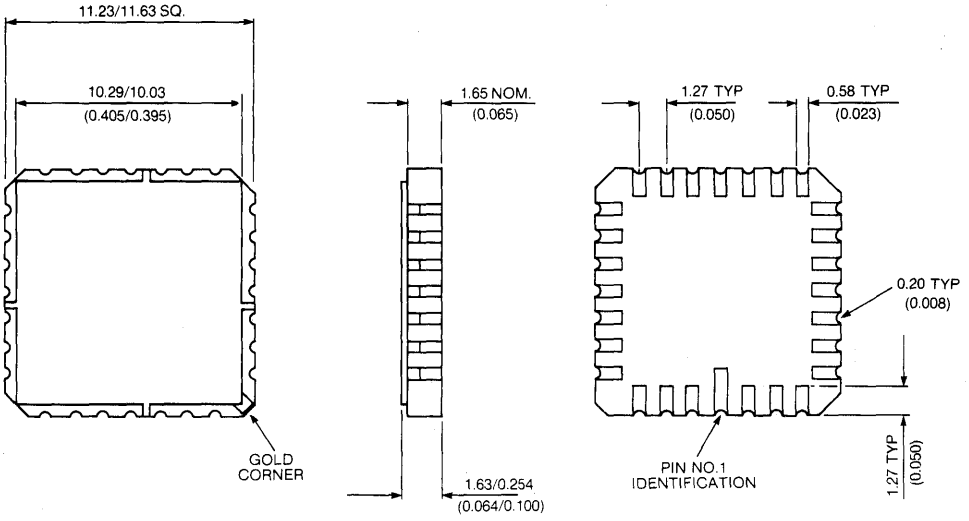
14-LEAD PLASTIC DIL - DP14



16-LEAD PLASTIC DIL - DP16



20-PIN LEADLESS CHIP CARRIER - LC20
(HERMETIC)



28-PIN LEADLESS CHIP CARRIER - LC28

Ordering information

Plessey Semiconductor integrated circuits are allocated type numbers which take the following general form

WW XXXX Y/ZZ

where **WW** is a two-letter code identifying the product group and/or technology, **XXXX** is a three or four numeral code uniquely specifying the particular device, **Y** is a single letter which denotes the precise electrical or thermal specification for certain devices and **ZZ** is a two-letter code defining the package style. Digits **WW**, **XXXX** and **Y** must always be used when ordering; digits **ZZ** need only be used where a device is offered in more than one package style. For example, the **SP9131** is offered in **DG** (Ceramic dual-in-line) and **LC** (Leadless chip chip carrier) packages so the full ordering number for this device in ceramic DIL would be **SP9131/DG** and **SP9131/LC** for the leadless chip carrier version.

The Pro-Electron standard is used for package codes wherever possible. The two letters of this code have the following meanings:

FIRST LETTER (indicates general shape)

A Pin-Grid Array
C Cylindrical
D Dual-in-Line (DIL)
F Flat Pack (leads on two sides)
G Flat Pack (leads on four sides)
Q Quad-in-Line

M Miniature (for Small Outline)
L Leadless Chip Carrier — Not yet designated by Pro-Electron
H Leaded Chip Carrier

SECOND LETTER (indicates material)

C Metal-Ceramic (Metal Sealed)
G Glass-Ceramic (Glass Sealed)
M Metal
P Plastic
E Epoxy

Please Note:

Leadless Chip Carriers

LC Metal-Ceramic 3 Layer (Metal Sealed)
LG Glass-Sealed Ceramic
LE Epoxy-Sealed 1 Layer
LP Plastic

Note: The above information refers generally to Plessey Semiconductors integrated circuit products and does not necessarily apply to all the devices contained in this handbook.

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