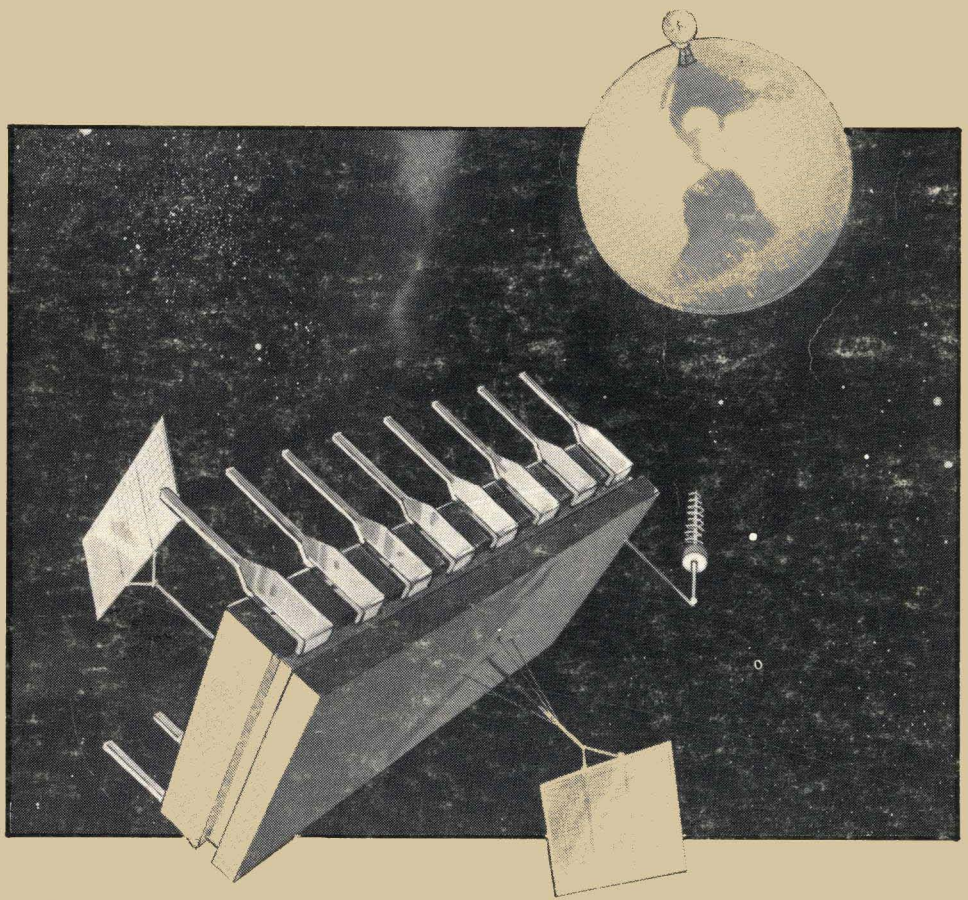
Telecom IC Handbook



Plessey Semiconductors

Telecommunications IC Handbook

$2.00

PLESSEY Semiconductors

TELECOM
IC HANDBOOK

NOVEMBER 1980

Plessey Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

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Contents

PRODUCT INDEX

1. Product Information

Building Block IC's

Plessey integrated circuits are on the leading edge of technology without pushing the ragged edge of capability.

We developed the first 2 GHz counter. And a family of prescalers and controllers for your TV, radio and instrumentation frequency synthesizers.

We have a monolithic 1 GHz amplifier. And a complete array of complex integrated function blocks for radar signal processing and radio communications.

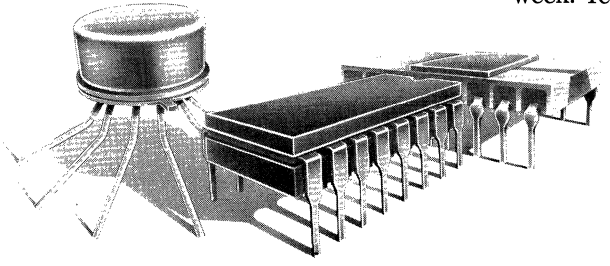
We can supply data conversion devices with propagation delays of just 2½ nanoseconds.

And a range of MNOS logic that stores data for a year when you remove the power, yet uses only standard supplies and is fully TTL/CMOS-compatible.

To develop this edge, we developed our own processes, both bipolar and MOS. The processes were designed for quality and repeatability, then applied to our high volume lines. Most of our IC's are available screened to MIL-STD-883B, and our quality levels exceed the most stringent military, TV and automotive requirements.

Millions of Plessey complex function building block IC's are being used in TV sets and car radios; CATV, navigation and radar systems; frequency synthesizers and telecommunications equipment.

Our global scope of operations, our high volume manufacturing facilities, our proprietary processes ensure that we will continue to deliver state-of-the-art technology and reliability in IC devices at the appropriate prices and in the required volumes. Day after day. Week after week. Year after year.



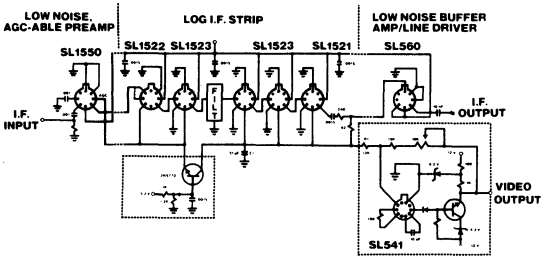
Plessey Semiconductors

1641 Kaiser Avenue, Irvine, CA 92714. (714) 540-9979

Radar Signal Processing

Since the performance of a radar receiver is critically dependent on the performance of its I.F. strip, we offer a range of "building block" IC's that can be used in systems with different performance requirements and configurations.

The logarithmic I.F. strip shown is an example of a low cost, high performance strip fabricated with Plessey IC's. It uses only five devices and a single interstage filter to achieve a logging range of 90 dB, ±1 dB accuracy, −90 dBm tangential sensitivity and a video rise time of 20 ns or less.



Three other Plessey IC's complete the system simply and economically. The AGC-able SL1550 on the front end improves noise figure, dynamic range and sensitivity. The SL541 lets you vary video output levels, with on-chip compensation making it easy to use. And the SL560 is a "gain block" that replaces your hybrid and discrete amplifiers, usually with no external components.

Another advanced system function block is the Plessey SL531 True Log Amplifier. A 6-stage log strip requires a minimum of external components (one capacitor, one resistor per stage), yet has a band-width of 500 MHz, a dynamic range of 70 dB and has a phase shift of only ±3° over its entire range. As with most of our other devices, it operates over the full MIL-temp range and is available screened to MIL-STD-883.

The chart summarizes our Radar Signal Processing IC's. Whether you're working with radar and ECM, weapons control or navigation and guidance systems, our IC's are a simpler, less expensive, more flexible alternative to whatever you're using now for any I.F. strip up to 160 MHz.

For more details, please use the postage-paid reply card at the back of this book to order our RADAR AND RADIO COMMUNICATIONS IC HANDBOOK, or contact your nearest Plessey Semiconductors representative.

PLESSEY IC'S FOR RADAR I.F.'S

Wideband Amplifiers for Successive Detection Log Strips

SL521	30 to 60 MHz center frequency, 12 dB gain.
SL523	Dual SL521 (series).
SL1521	60 to 120 MHz center frequency, 12 dB gain.
SL1522	Dual SL1521 (parallel).
SL1523	Dual SL1521 (series).

Low Phase Shift Amplifiers

SL531	True log I.F. amplifier, 10-200 MHz, ±0.5°/10 dB max phase shift.
SL532	400 MHz bandwidth limiting amplifier, 1° phase shift max. when overdriven 12 dB.

Linear Amplifiers

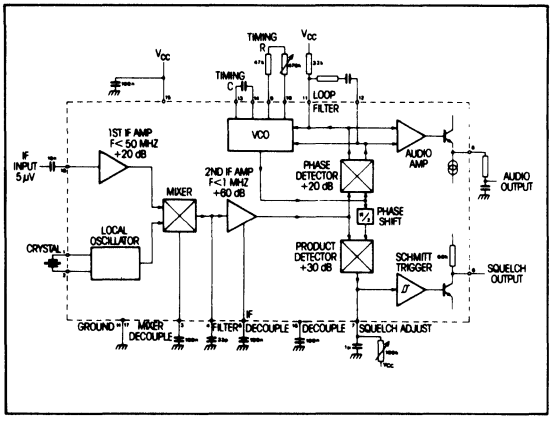
SL550	125 MHz bandwidth, 40 dB gain, 25 dB swept gain control range, 1.8 dB noise figure, interfaces to microwave mixers.
SL1550	320 MHz bandwidth version of SL550.
SL560	300 MHz bandwidth, 10 to 40 dB gain, 1.8 dB noise figure drives 50 ohm loads, low power consumption.

Video Amplifiers and Detectors

SL510	Detector (DC to 100 MHz) and video amplifier (DC to 24 MHz) may be used separately, 11 dB incremental gain 28 dB dynamic range.
SL511	Similar to SL510 with DC to 14 MHz video amplifier, 16 dB incremental gain.
SL541	High speed op amp configuration, 175 V/μs slew rate 50 ns settling time, stable 70 dB gain, 50 ns recovery from overload.

Radio Communications

Our comprehensive line of radio system function blocks is cutting costs, increasing reliability and reducing the size of systems in applications that range from commercial communications to military manpack radios.



Using our bipolar Process I, the Plessey SL600 Series (hermetic) and SL1600 Series (plastic DIP) feature a high degree of integration, low power consumption and exceptional system design flexibility for I.F.'s up to 10.7 MHz.

Our SL6000 Series uses our bipolar Process III to extend our building block concept even further. Devices all feature advanced circuit design techniques that permit higher levels of integration, lower power consumption and exceptional performance.

Typical is our SL6600, a monolithic IC that contains a complete IF amplifier, detector, phase locked loop and squelch control. Power consumption is a meager 1.5 mA at 6 V, S/N ratio is 50 dB, dynamic range is 120 dB and THD is just 1.3% for 5 kHz peak deviation. The SL6600 can be used at I.F. frequencies up to 50 MHz, with deviations up to 10 kHz.

If any of the Plessey devices appear interesting, use the postage-paid reply card at the back of this book to order our RADAR AND RADIO COMMUNICATIONS IC HANDBOOK. The Handbook includes full details on our integrated circuits, along with a number of applications circuits and design tips that will help you get the maximum system benefits from Plessey products.

Or if your need is more urgent, contact your nearest Plessey Semiconductors representative.

PLESSEY RADIO IC'S

Amplifiers		
SL610	SL1610	140 MHz bandwidth, 20 dB gain, 50 dB AGC range, low 4 dB N.F., low distortion.
SL611	SL1611	100 MHz bandwidth, 26 dB gain, sim. to SL610.
SL612	SL1612	15 MHz bandwidth, 34 dB gain, 70 dB AGC range, 20 mW power consumption.
SL613		145 MHz bandwidth, 12 dB gain, limiting amp/detector.
Mixers		
SL640	SL1640	Double balanced modulator eliminates diode rings up to 75 MHz, standby power 75 mW typical.
Detectors and AGC Generators		
SL620	SL1620	AGC with VOGAD (Voice Operated Gain Adjusting Device).
SL621	SL1621	AGC from detected audio.
SL623	SL1623	AM SSB detector and AGC from carrier.
	SL1625	AM detector and AGC from carrier.
SL624		AM/FM/SSB/CW detector with audio amplifier.
Audio Amplifiers		
SL622		Microphone amp. with VOGAD and sidetone amp.
SL630	SL1630	250 mW microphone/headphone amplifier.
I.F. Amplifiers/Detectors		
SL6600		FM double conversions with PLL detector.
SL6640		FM single conversion, audio stage (10.7 MHz).
SL6650		FM single conversion (10.7 MHz).
SL6690		FM single conversion, low power for pagers (455 kHz).
SL6700		AM double conversion.
Audio Amplifiers		
SL6270		Microphone amplifier with AGC.
SL6290	SL6270	with speech clipper, buffer and relay driver.
SL6310		Switchable audio amplifier (400 mW/9V/8 ohms).
SL6440		High-level mixer.

R. F. Hybrids

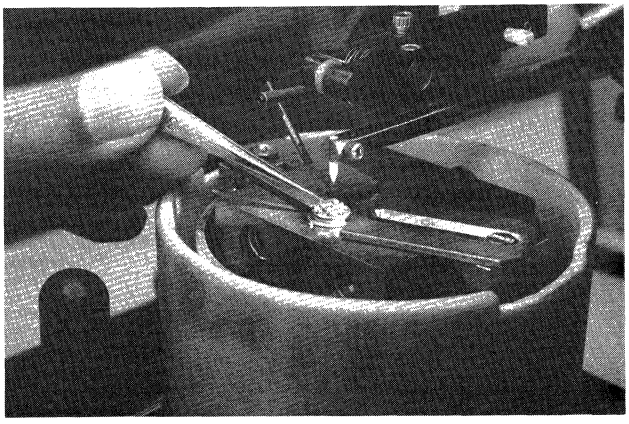
To enhance your systems even further, we have established an R.F. hybrid manufacturing facility in our Irvine, California, U.S.A. headquarters.

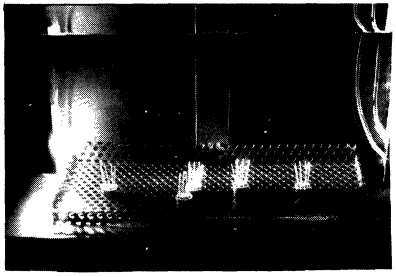
For small production quantities or extremely complex functions, our hybrid capabilities can save you time and money while improving your system performance, reducing system size and increasing system reliability. We can help with your I.F. strips, instrumentation front ends, synthesizer subsystems, high speed A-to-D and D-to-A converters and other complex high-frequency functions.

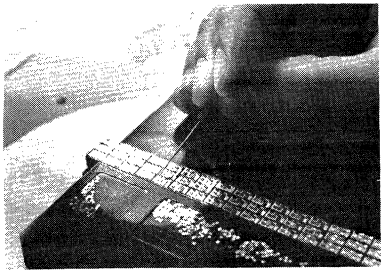
They can be fabricated to MIL-STD-883 using thick and thin film techniques, using our own integrated circuits in combination with discrete transistors, diodes and other components.

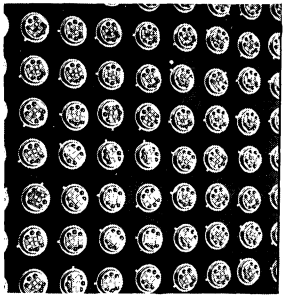
Our IC functions represent the state-of-the-art in high frequency integration, with f_t's as high as 5 GHz. The chips are backed by an in-depth in-house systems knowledge that encompasses radar, radio communications, telecommunications analog and digital conversion, frequency synthesis and a broad range of applications experience.

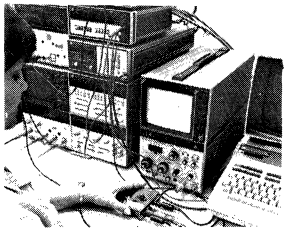
We can work to your prints, or we can design a full system based on your "black box" specifications. For more information, please contact: Plessey Semiconductors, 1641 Kaiser Avenue, Irvine CA 92714, (714) 540-9979.

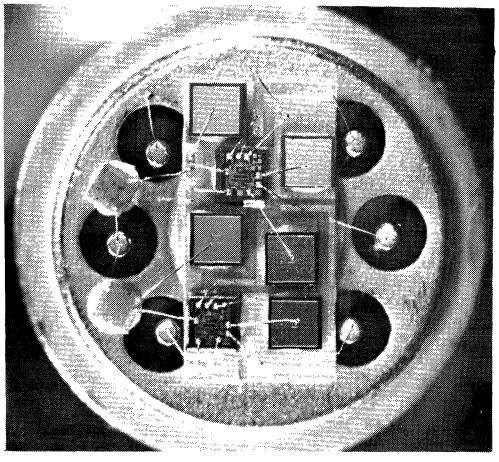












Frequency Synthesis

Plessey's IC's offer a quick and easy way to lower synthesizer costs while increasing loop response and channel spacing all the way from dc through the HF, VHF, UHF, TACAN and satellite communications bands.

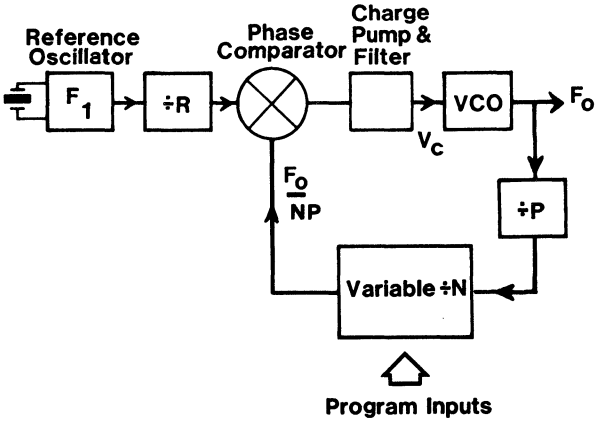
Our single-modulus prescalers operate at frequencies all the way up to 1.8 GHz. They feature self-biasing clock inputs, TTL/CMOS-compatibility and all guaranteed to operate to at least the frequencies shown, most of them over the temperature range from −55°C to +125°C.

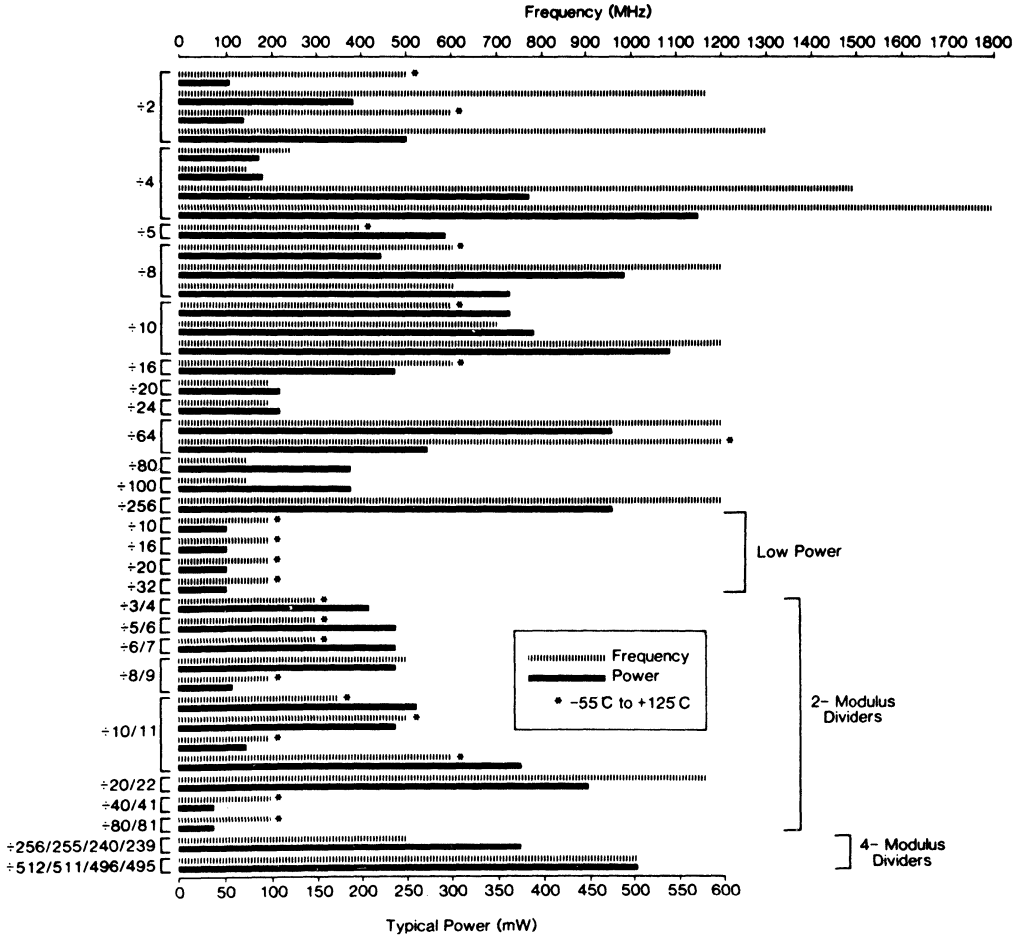
Our 2-modulus and 4-modulus dividers expand your system flexibility and allow even tighter channel spacing. All of them provide low power consumption, low propagation delay and ECL-compatibility.

To simplify your systems even further, we also offer highly integrated control chips. Our NJ8811, for example, includes a crystal oscillator maintaining circuit, a programmable reference divider, a programmable divider to control the four-modulus prescaler and a high performance phase/frequency comparator so that you can phase lock your synthesizer to a crystal with none of the usual headaches and hassles.

We've put together a FREQUENCY SYNTHESIZER IC HANDBOOK that details all of the Plessey IC's and includes a number of applications circuits, practical examples of how Plessey integrated circuits can simplify your designs and improve system performance.

For your copy of the Handbook, please use the postage-paid reply card at the back of this book, or contact your nearest Plessey Semiconductors representative.




Frequency (MHz)
0 100 200 300 400 500 600 700 800 900 1000 1100 1200 1300 1400 1500 1600 1700 1800
÷2
÷4
÷5
÷8
÷10
÷16
÷20
÷24
÷64
÷80
÷100
÷256
÷10
÷16
÷20
÷32
÷3/4
÷5/6
÷6/7
÷8/9
÷10/11
÷20/22
÷40/41
÷80/81
÷256/255/240/239
÷512/511/496/495
Low Power
2- Modulus Dividers
4- Modulus Dividers
Frequency
Power
* -55°C to +125°C
0 50 100 150 200 250 300 350 400 450 500 550 600
Typical Power (mW)

Telecommunications

Plessey functional building block IC's are exceptionally versatile. Designed from a systems standpoint, they reduce complexity and lower costs while increasing the performance of telecommunications systems.

Our SL600 Modulator/Phase Locked Loops are used in waveform generators and in AM, PAM, FM, FSK, PSK, PWM, tone burst and Delta modulators.

Our SL1000 Series amplifiers meet the most stringent demands of telephone transmission equipment.

Our transistor arrays with up to five electrically and thermally matched transistors on a chip are ideal for discrete and hybrid amplifiers and mixers. In addition to standard second-source devices that plug directly into your designs, we have a number of devices designed for your low noise and ultra-high frequency applications.

The Plessey TELECOMMUNICATIONS IC HANDBOOK contains complete information on all of these devices, as well as application notes, to help you get the most out of them. To get your copy, please use the postage-paid reply card at the back of this book or call your nearest Plessey Semiconductors representative.

Telecommunications Devices

MJ1440	HDB3 encoder/decoder
MJ1444	PCM synchronizing word generator
MJ1445	PCM synchronizing word receiver
MJ1471	HDB3/AMI encoder/decoder

Data Communications MOS

MP3812	32 x 8-bit FIFO memory, serial or parallel, up to 0.25 MHz data rates, easily stacked.
MJ2841	64 x 4-bit FIFO memory, 5 MHz clock rate.

Modulator/Phase Locked Loops

SL650	Modulator/PLL for AM, PAM, SCAM, FM, FSK, PSK, tone-burst and Delta modulation; VFO variable 100:1.
SL651	Similar to SL650 without auxiliary amplifier.
SL652	Similar to SL650, low cost.

Telephone Circuits

SL1001	Modulator/demodulator, 50 dB carrier and signal suppression, −112 dBm noise level.
SL1021	3 MHz channel amplifier, stable remote gain control.
SL1025	FDM balanced modulator, 50 dB carrier and signal suppression, 5 dB conversion gain.
SL1030	200 MHz wideband amplifier, programmable gain, low noise.

Transistor Arrays

PLESSEY PART NO.	2ND-SOURCE PART NO.	PLESSEY PART NO.	2ND-SOURCE PART NO.
SL3081	CA3081	SL3051	CA3951
SL3082	CA3082	SL355	NONE
SL3083	CA3083	TBA673	TBA673
SL3183	CA3183	SL1495	CA1495L
SL3146	CA3146	SL1496	MC1496G
SL3093	CA3093	SL1496	MC1496L
SL3018	CA3018	SL1595	MC1595L
SL3018A	CA3018A	SL1596	MC1596G
SL3118A	CA3118A	SL1596	MC1596L
SL3118	CA3118	SL3054	CA3054
SL3050	CA3050	SL3086	CA3086

SL360	High frequency matched pair, f_t=2.5 GHz.
SL363	Low noise matched pair, f_t=2.2 GHz.
SL2363/4	5GHz dual long-tailed pair.
SL3145	Five transistor array, f_t=2.5 GHz.

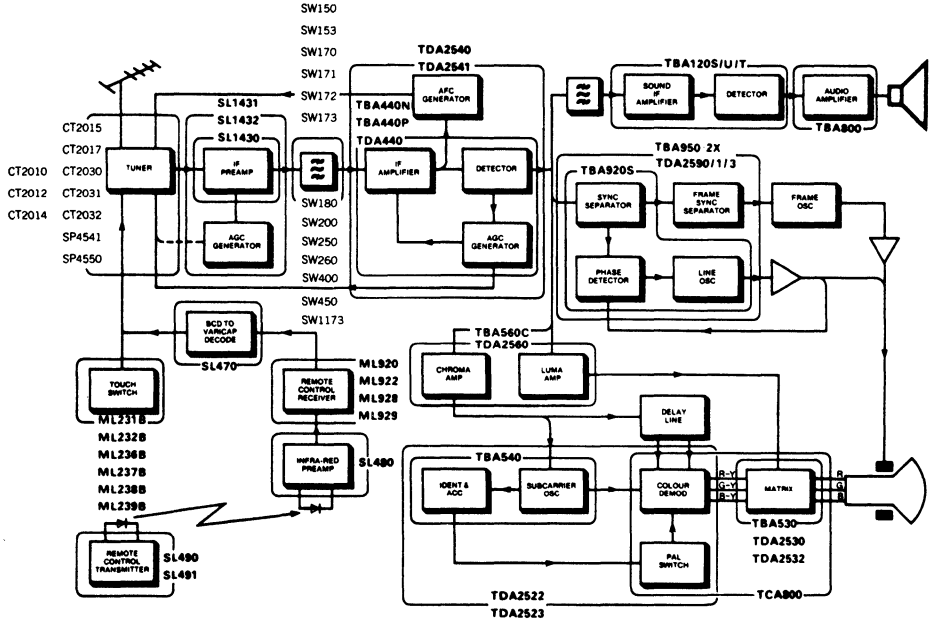
Television IC's

Plessey integrated circuits are in millions of homes, in television sets around the world.

Economical and reliable, our devices cover the range from remote controls to touch tuners to frequency synthesizers, as well as a range of second-source devices for the IF color processing and line oscillators.

For the 1980's, we have introduced the Plessey KEY System, designed for maximum flexibility, simplicity and ease of manufacture. The KEY System frequency synthesizer offers accurate, high stability frequency selection, channel and program identification, and the very finest digital fine tuning. It can be configured to receive up to four completely different standards (PAL, SECAM, SECAMF, and NTSC) in a single TV set. It has 100 channel capability per standard, and includes a 32-program non-volatile memory that contains channel, fine tuning and standards information. And it can be interfaced to a Plessey or other microprocessor for games, Teletext or similar applications.

Complete data on all our television devices has been assembled in our TELEVISION IC HANDBOOK, along with application notes to make them even easier to use. Please use the postage-paid reply card at the back of this book to order your copy, or simply contact your nearest Plessey Semiconductors representative.



ALL TBA, TCA, TDA DEVICES ARE SECOND-SOURCED.

ECL III Logic and Data Conversion

As radar and communications systems become faster and more complex, the need arises for digital processing. We have developed a family of functions with speeds unequalled anywhere.

Part of our family is a range of ECL III logic that is a direct plug-in replacement for MECL logic, including low impedance as well as high impedance devices. We extended the range by adding functions with lower delays and much higher operating speeds. Our SP16F60, for example, is the world's fastest dual 4-input OR/NOR gate, with a switching speed of just 500 picoseconds. Devices can also be selected for certain specifications (such as threshold voltage or slew rate on our SP1650/1, toggle rates or delays on our SP1670) to handle your most demanding applications. We've also developed a family of high speed comparators and circuits for ultra-high speed A-to-D converters. Our latching SP9750 high speed comparator features a maximum settling time of 2 ns, a propagation delay of 3.5 ns and is capable of operating at rates up to 100 million samples per second.

Currently, our devices are being used in radar and video processing, nucleonics systems, transient recorders and secure speech transmission systems. We have compiled a number of application notes and details on the devices in our ECL III LOGIC AND DATA CONVERSION IC HANDBOOK. To get your copy, please use the postage-paid reply card at the back of this book, or contact your nearest Plessey Semiconductors representative.

HIGH SPEED ECL III LOGIC

SP1648	Voltage controlled oscillator
SP1650	Dual A/D comparator, Hi-Z
SP1651	Dual A/D comparator, Lo-Z
SP1658	Voltage controlled multivibrator
SP1660	Dual 4-I/P OR/NOR gate, Hi-Z
SP1661	Dual 4-I/P OR/NOR gate, Lo-Z
SP1662	Quad 2-I/P NOR gate, Hi-Z
SP1663	Quad 2-I/P NOR gate, Lo-Z
SP1664	Quad 2-I/P OR gate, Hi-Z
SP1665	Quad 2-I/P OR gate, Lo-Z
SP1666	Dual clocked R-S Flip-Flop, Hi-Z
SP1667	Dual clocked R-S Flip-Flop, Lo-Z
SP1668	Dual clock latch, Hi-Z
SP1669	Dual clock latch, Lo-Z
SP1670	Master-slave D Flip-Flop, Hi-Z
SP1671	Master-slave D Flip-Flop, Hi-Z
SP1672	Triple 2-I/P exclusive-OR gate, Hi-Z
SP1673	Triple 2-I/P exclusive-OR gate, Lo-Z
SP1674	Triple 2-I/P exclusive-NOR gate, Hi-Z
SP1675	Triple 2-I/P exclusive-NOR gate, Lo-Z
SP1692	Quad line receiver
SP16F60	Dual 4-I/P OR/NOR gate

HIGH SPEED DATA CONVERSION PRODUCTS

SP9680	High speed latched comparator.
SP9685	Ultra-fast comparator; 0.5 ns typical set-up time; typical 2.2 ns propagation delay; excellent CMR.
SP9687	Dual SP 9685.
SP9750	High speed latched comparator with precision current source, wired-OR decoding; 2 ns min. set-up time; 2.5 ns propagation delay.
SP9752	2-bit ADC expandable to 6-bit ADC; very fast 125 MHz clock.
SP9754	4-bit ADC expandable to 8-bit ADC; very fast 100 MHz clock.
SP9768	8-bit DAC; extremely fast; available 3rd quarter 1980.
SP9778	8-bit SAR; works with SP9768 to make a two-chip successive approximation ADC (20 MHz clock); available 4th quarter 1980.

MNOS Non-Volatile Logic

As semiconductors become more pervasive in military and commercial applications, the need for non-volatile data retention becomes more and more critical.

Plessey NOVOL MNOS devices answer that need, and will retain their data for at least a year (−40°C to +70°C) in the event of "power down" or a system crash.

Our devices all operate from standard MOS supplies and are fully compatible with your TTL/CMOS designs. The high voltages normally associated with electrically-alterable memories are generated on-chip to make system interface simpler and less expensive.

Plessey NOVOL devices provide a reliable, sensible alternative to CMOS with battery back-up or mechanical, electro-mechanical and magnetic devices. Applications include metering, security code storage, microprocessor back-up, elapsed time indicators, counters, latching relays and a variety of commercial, industrial and military systems.

For more information, contact your nearest Plessey Semiconductors representative, or use the postage-paid reply card at the back of this brochure to order your copy of the Plessey NOVOL literature package.

PLESSEY NOVOL MNOS

MN9102	4-bit Data Latch (+5V, −12V)
MN9105	4-Decade Up/Down Counter (+5V, −12V)
MN9106	6-Decade Up Counter (12V only)
MN9107	100-Hour Timer (12V only)
MN9108	10,000-Hour Timer (12V only)
MN9110	6-Decade Up Counter with Carry (12V only)
MN9210	64 x 4-Bit Memory
*	8 x 4-Bit Memory
*	6-Decade Up/Down Counter, BCD Output
*	6-Decade Up/Down Counter with Preset BCD Output

* COMING SOON

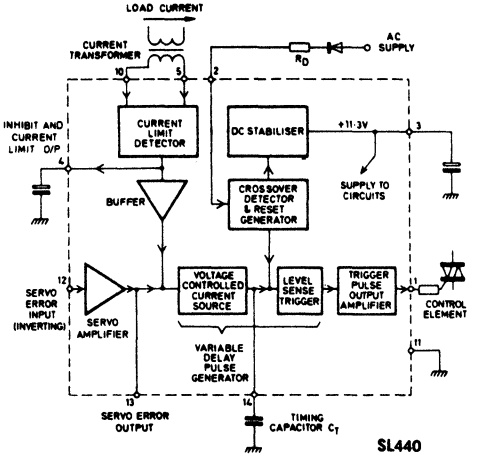
Power Control

Plessey power control devices are highly integrated not just to solve the problems, but to solve them at a lower cost than any other available method.

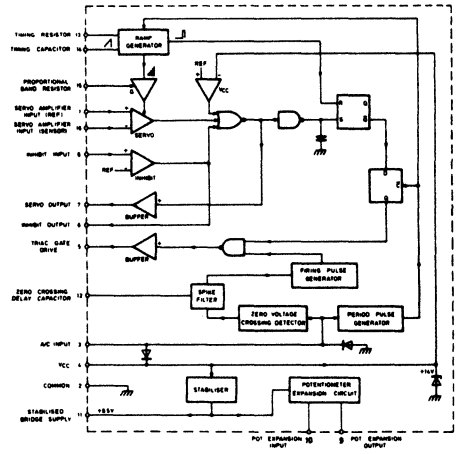
For timing, our devices use a pulse integration technique that eliminates the need for expensive electrolytic capacitors, thus increasing accuracy and repeatability while reducing costs. An integral supply voltage sensing circuit inhibits triac gate drive circuitry if the supply is dangerously low to prevent half-wave firing and firing without achieving complete bulk conduction. A zero-voltage spike filter prevents misfiring on noise inputs. Symmetrical control prevents the introduction of dc components onto the power lines.

Devices have been tailored for specific applications as indicated in the chart. For more information, please use the postage-paid reply card at the back of this book to order our POWER CONTROL IC HANDBOOK, or contact your nearest Plessey Semiconductors representative.

SL440	**Proportional phase control for motors, lamps and lower power, fast response heating.**
SL441	**Similar to SL440, with proportional temperature control and thermister malfunction sensing, for hairdryers, soldering irons and food warmers.**
SL442	**Switch mode power supply control, up to 40 kHz, integral oscillator, variable ratio space/mark pulses, soft-start, dynamic current limiting, OVP.**
SL443	**Similar to SL441 with manual power control, long timing periods for hot plates, electric blankets and traffic lights.**
SL444	**Similar to SL441 for 240V permanent magnet motor with thermal trip, current limit detector.**
SL445	**Proportional or On/Off control, temperature trip/inhibit circuitry, LED and alarm drive facilities, for ovens, heaters, industrial temperature controllers.**
SL446	**On/Off servo loop temperature controller, low external component count, for water and panel heaters, refrigerators, irons.**
TBA1085	**Motor speed control**



SL440



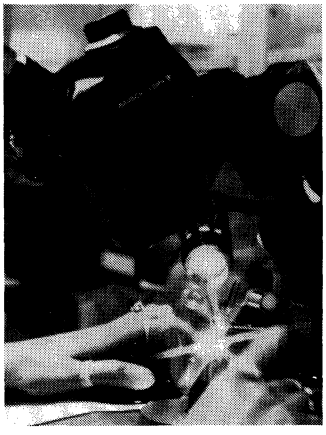
SL445

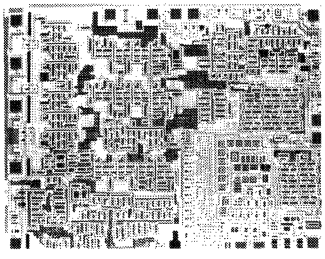
Processes, Testing and Quality Control

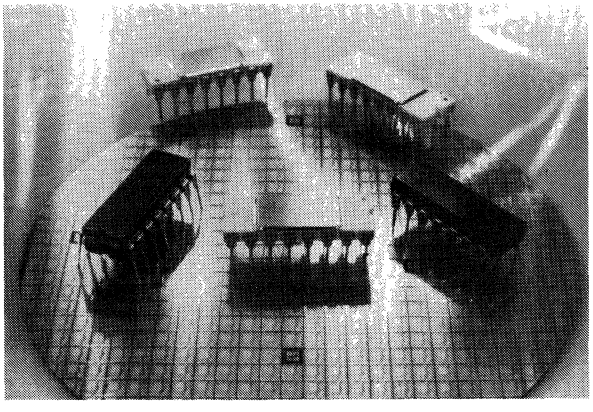
Just as we applied our systems knowledge to the partitioning of functions to make our IC's extremely flexible and cost effective, we also developed an internal system concept to ensure that we could deliver our state-of-the-art solutions year after year.

Our concept of standard processes and rigid design rules ensures that our devices are reproducible this year, next year and five years from now. Our continuing investment in research and development ensures that any new products we introduce will be on the leading edge of technology, yet with the same high performance and reliability that our customers have come to expect as the Plessey standard.

The result is that millions of Plessey devices have been built into TV sets and car radios; CATV, navigation and radar systems; frequency synthesizers and telecommunications equipment.





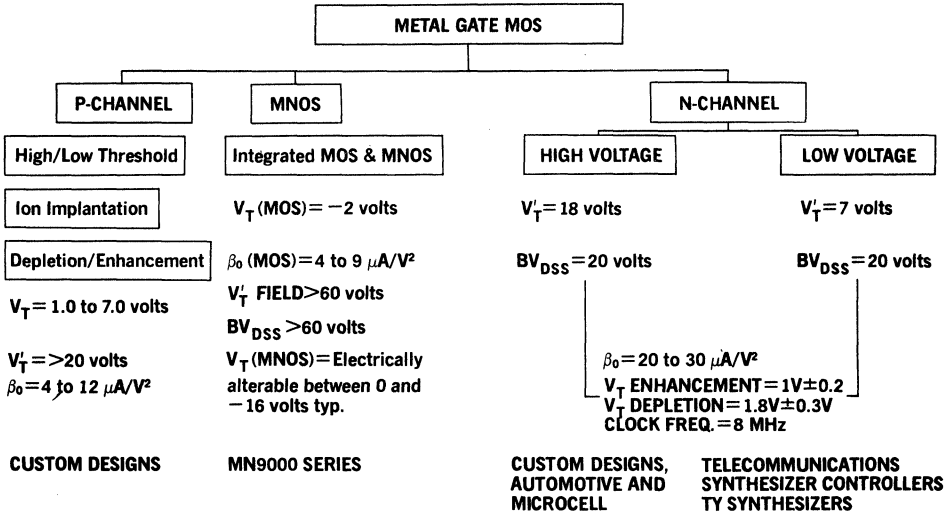


Plessey MOS Processes

P-channel metal gate MOS has been in production for years and is used for both standard Plessey products and custom LSI. Using ion implantation to modify transistor and field threshold voltages, we can reproduce virtually any p-channel metal gate process, with or without depletion loads.

MNOS (non-volatile) is essentially a p-MOS process with variable threshold memory transistors fabricated alongside conventional MOS transistors. A modified oxide-nitride gate dielectric permits the injection and retention of charge to change the threshold voltage. Current Plessey products will retain an injected charge for at least a year, and include an on-chip high voltage generator so that they may be used with standard supply voltages.

N-channel metal gate MOS uses an auto-registration co-planar process with layout similar to our p-MOS. Ion implantation is used to define the threshold voltage of the depletion and enhancement transistors. The constant-current-like characteristics of depletion load devices give the most effective driving capability, and enhancement-depletion technology simplifies design and increases packing density. The field threshold voltage is also controlled by an ion implant, allowing the use of a lightly doped substrate. This reduces both the body constant and the junction capacitance and results in faster switching speeds.



Plessey Bipolar Processes

Bipolar Process I is a conventional buried +N layer diffusion process with f_t=600 MHz and other characteristics similar to industry-standard processes. Applications range from high reliability military devices to high volume consumer products.

Process Variant	A	B	G	D
Application	General Purpose	Non Saturating Logic	Saturating Logic	Linear Consumer
BV_{CBO} @ 10μA	20V min.	10V min.	10V min.	45V min.
BV_{EBO} @ 10μA	5.3V to 5.85V	5.15V min.	5.15V min.	6.8V to 7.4V
LV_{CEO}	12V min.	8V min.	8V min.	20V min.
$V_{CE\ (SAT)}$ @ I_B=1mA, I_C=10mA	0.43V max.	0.32V max.	0.43V max.	0.6V max.
h_{FE} @ I_C=5mA, V_{CE}=5V	40 to 200	50 min.	50 min.	50 to 200
f_T @ I_C=5mA, V_{CE}=5V	500 MHz	500 MHz min.	500 MHz min.	350 MHz min.

Bipolar High Voltage (HV) Process is a variant of Process I that yields an LV_{ceo} greater than 45 volts. Doping levels can be controlled and an extra diffusion used to fabricate a buried avalanche diode with a 40 V breakdown for absorbing powerful noise transients without being destroyed.

Process Variant	CA
BV_{CBO} @ 10μA	80V min.
BV_{EBO} @ 10μA	7.2V to 8.0V
LV_{CEO}	45V min.
$V_{CE\ (SAT)}$ @ I_B=1mA, I_C=10mA	0.4V max.
h_{FE} @ I_C=5mA V_{CE}=5V,	80 to 300
f_T @ I_C=5mA, V_{CE}=5V	250 MHz min.

Bipolar Process III uses very shallow diffusion and extremely narrow spacing for high frequency integrated circuits with unusually low power consumption and high packing densities. An f_t of 2.5 GHz allows us to routinely produce analog amplifiers with bandwidths as high as 300 MHz and low power dividers and prescalers that operate at frequencies up to 1.2 GHz. Process variants allow us to produce devices with an extended β, higher breakdown voltages and very small geometries.

Process Variant	WE
Application	Digital
BV_{CBO} @ 10μA	10V min.
BV_{EBO} @ 10μA	5.1V to 5.8V
LV_{CEO}	7V min.
$V_{CE\ (SAT)}$ @ I_B=1mA, I_C=10mA	0.5V max.
h_{FE} @ I_C=5mA, V_{CE}=2V	40 to 200
f_T @ I_C=5mA, V_{CE}=2V	1.8 GHz

Bipolar Process 3V is an extension of our Process III. Ion implantation and washed emitters have given the process an f_t=6.5 GHz, allowing us to produce dividers working at 2 GHz, logic gates with delays of less than 500 picoseconds and linear amplifiers at 1 GHz.

Process Variant	WV
Application	Digital
BV_{CBO} @ 10μA	8V min.
BV_{EBO} @ 10μA	3.0V to 5.0V
LV_{CEO}@ 5mA	6V min.
$V_{CE\ (SAT)}$ @ I_B=1mA, I_C=10mA	0.5V max.
h_{FE} @ I_C=10mA, V_{CE}=5V	40 to 120
f_T @ I_C=5mA, V_{CE}=2V	6.5 GHz

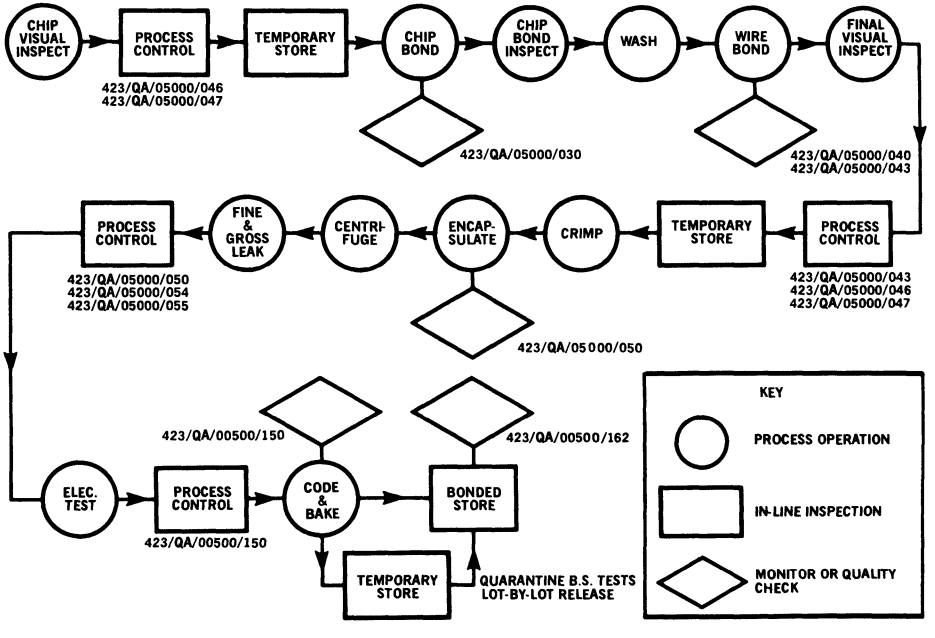
Testing and Quality Control

A major thrust of our development work is to ensure that our processes will routinely produce reliable devices. Our Process III has a projected MTBF of 400,000 hours while our Process I is even better.

Our facilities include the latest test equipment (such as the Macrodata MD501, Teradyne J324 and Fairchild Sentry VII and Sentinel) to allow us to perform all the necessary functional and parametric testing in-house. We have an internal capability to provide specific applications-oriented screening, and most Plessey IC's are available screened to MIL-STD-883 and other international specifications. Our quality levels exceed the most stringent military, TV and automotive requirements as a matter of course.

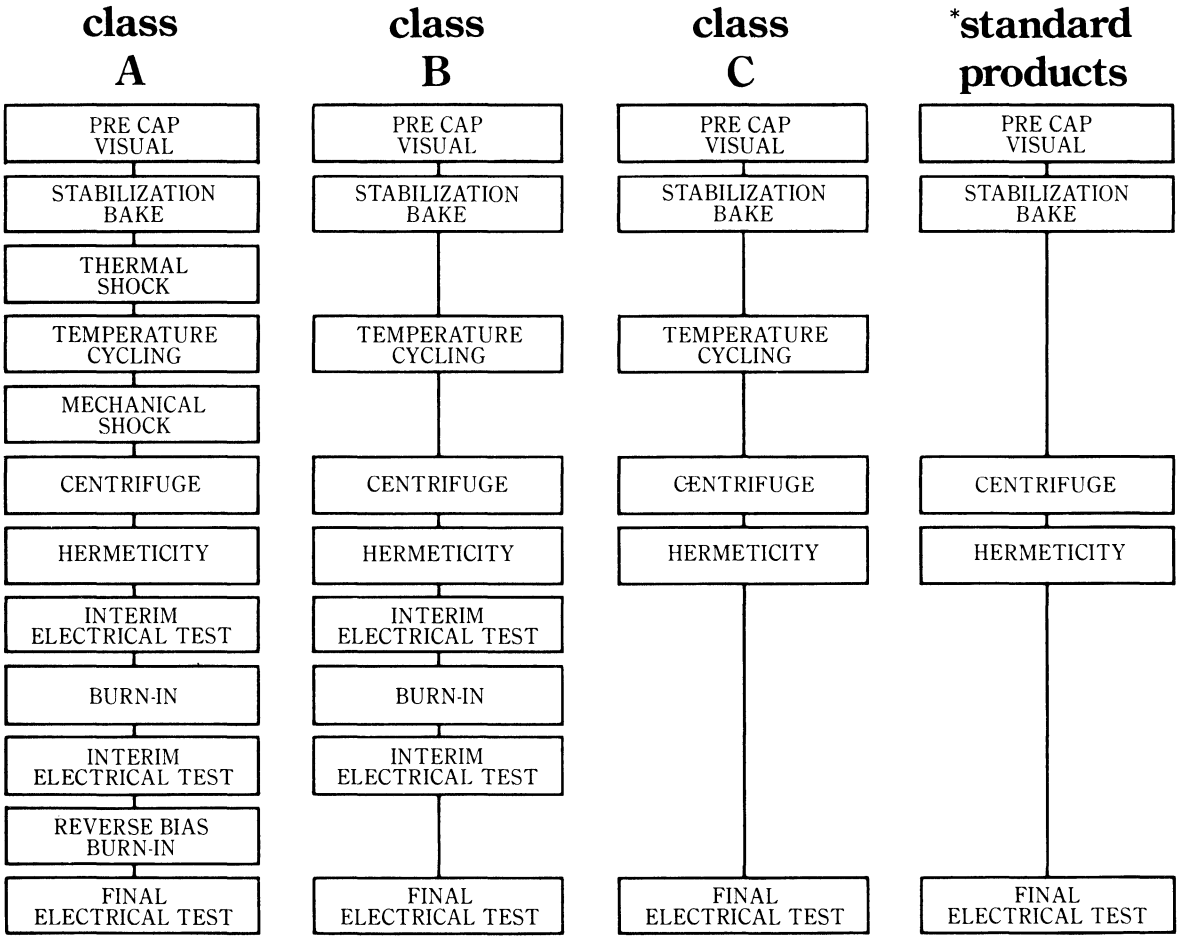
But the best proof of all these claims is our products themselves. After you've reviewed the products that could help you with your systems, use the postage-paid reply card or contact your nearest Plessey representative for complete details.

ASSEMBLY OF INTEGRATED CIRCUITS
QUALITY ASSURANCE



I.C. Screening to MIL-STD-883

The following Screening Procedures are available from Plessey Semiconductors



Plessey Semiconductors reserve the right to change the Screening Procedure for Standard Products.

2. TAB1040 Series OP AMP Applications

1. An economical track-and-hold amplifier

One of the secondary properties of some programmable operational amplifiers is that when the programming current is reduced to zero the output impedance rises to a high value, limited only by the leakage properties of the output devices. This happens because the programme current controls the bias currents of all stages of the amplifier, including the output stage. Without bias current, the amplifier shuts off and no output current will flow.

This means that such an amplifier can be used as an effective analogue switch combined with the normal functions of an operational amplifier. One application for such a combination is in a track and hold circuit.

The Plessey TAB 1042/3/4 family of quad programmable op-amps can be used in this way. The TAB 1043 is particularly effective since its '3 + 1' configuration allows one amplifier to be switched while the other three are used in conventional applications.

Track and hold configuration

The basic circuit configuration is shown in Fig. 1, the bias current being switched between zero and the value appropriate to the tracking function.

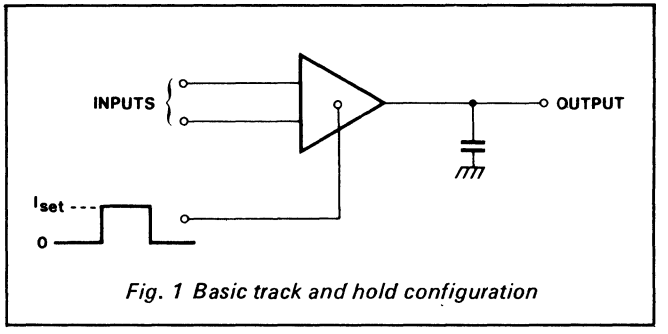


Fig. 1 Basic track and hold configuration

In order to track the input signal, the amplifer will normally be used in a closed – loop mode. This means that the feedback path must be connected to the output, and hence to the storage capacitor, providing an unwanted leakage path. To minimise this, a high value resistor is used, preferably over 1 Megohm.

The effect of connecting a moderately large value capacitor to the amplifier output is to reduce the output

phase margin, so that severe ringing may result from large transients, such as in the bias switching technique. The phase margin can be protected by running the amplifier at a moderate gain, such as 100; this also has the benefit that the input source resistance is much lower than the 1 Megohm feedback, so that input offset current errors are reduced. Obviously if such gain is unwanted in the system context, the input signal can be voltage-divided before sampling. The good noise performance of the TAB 1043 ensures that the noise penalty incurred is small.
The resulting circuit is shown in Fig. 2.

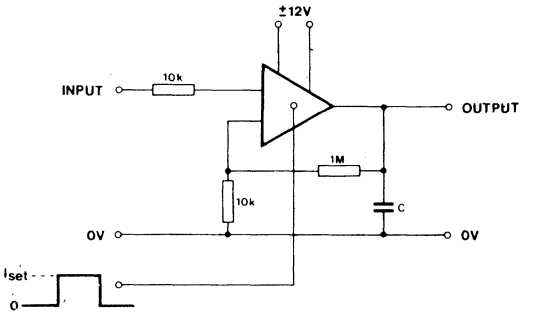


Fig. 2 Practical track and hold circuit

The value of C is selected to meet the acquisition and droop requirements. The fastest acquisition will occur with the highest value of Iset; for Iset of 18μA per amplifier or more, the typical output current capability is around 5 mA, so that the output acquisition/track rate is 5/C V/μ s for C in nF. The droop rate depends on the signal amplitude; for a typical peak signal of 5V, the droop rate is 5/C V/ms (neglecting output load effects). Of course, this droop rate will be affected by any current drawn from the output; it is a good idea to use an additional amplifier in the TAB 1043 package as a high input impedance output buffer. If the set current is kept low (say 1.5 to 2μA per amplifier), the input bias current of a unity-gain buffer will be typically less than 100nA, which will affect the droop rate by only 2 per cent.

The turn off condition is most effectively achieved by actively clamping the bias input to the negative supply; this avoids any risk of low-level turn-on bv small leakage currents, e.g. across the board surface.

Fig. 3 shows a complete track and hold circuit with TTL-compatible control input and a buffered low-impedance output. The overall gain is unity, and the

circuit will track +5V input signals at 0.5V/μs, and hold for up to 100μs with a droop error of 1 per cent peak (50mV).

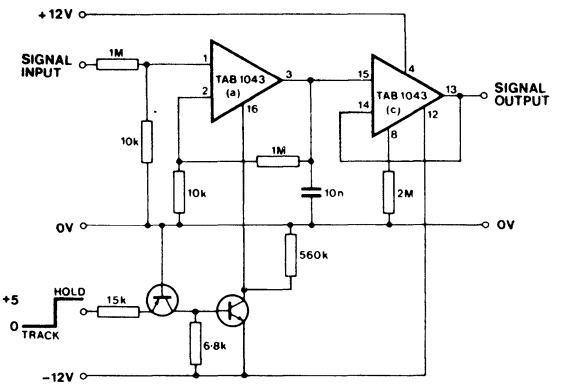


Fig. 3 Complete track and hold circuit

2. Simple active filters

Active filters are frequently used instead of passive circuits because they avoid the use of inductors, which are both bulky and expensive, particularly at low frequencies.

By using modern operational amplifiers, active filters can now be realised both easily and economically with highly predictable characteristics.

Apart from the very simplest, the majority of active filters require several operational amplifiers, so the benefits of using a multiple op. amp package are obvious.

The Plessey TAB1042 family is especially suited to active filter applications, since the programmable feature enables the filter characteristics to be optimised with maximum power economy.

Filter characteristics

Filter characteristics may be classified in terms of the phase response, passband flatness, stop-band rejection, steepness of cut-off, etc. The commonest forms of classification are as follows:-

BESSEL – maximally linear phase (flat time delay); amplitude roll-off gradual, starting at zero frequency.

BUTTERWORTH – maximally flat pass band; moderate phase response; moderate roll-off.

CHEBYCHEV – maximum roll-off rate (for all pole transfer characteristic); equal amplitude pass band ripples; amplitude related to roll-off required; poor phase response.

CAUER (OR ELLIPTIC) – maximum roll-off rate, achieved by transfer zero(es) in the stop band; relatively poor stop band rejection; poor phase response.

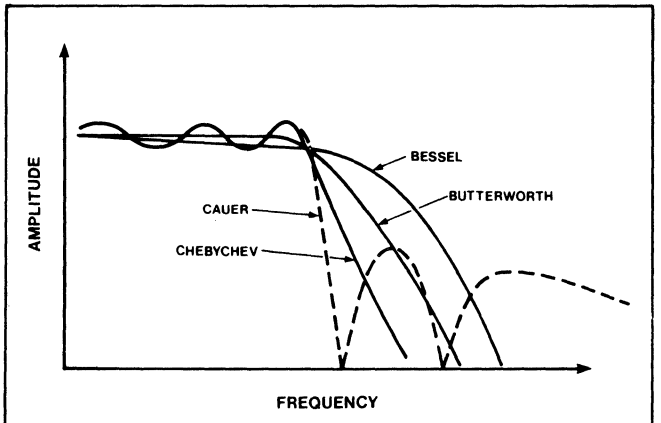


Fig. 1 Normalised filter responses

In this application note we shall only be discussing the simple all-pole realisations, but the Cauer response is included in this discussion for completeness.

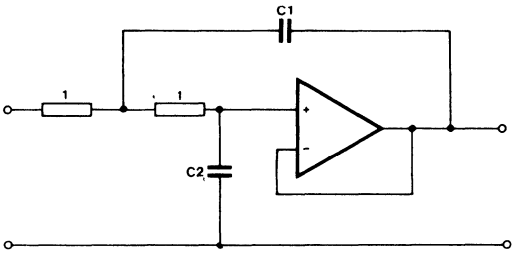
For all three all-pole filter responses, the final roll-off rate is determined by the order of the filter,ie. how many poles are created, in the relationship 6dB/octave/pole.

This enables the designer to determine the necessary order and complexity of the filter needed in his system. The response form is determined by the positions of the poles on the complex frequency plane, or S-plane; each active stage generates a complex conjugate pair of poles. For odd order filters, a single pole on the real axis can be generated by a passive RC network.

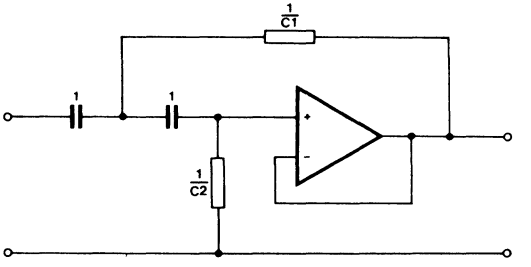
Filter realisations

In general, any of the all-pole responses can be realised by each of a large number of circuit forms. The selection of the best possible circuit may be a complex trade-off of sensitivities, parameter interdependence, system requirements, etc.

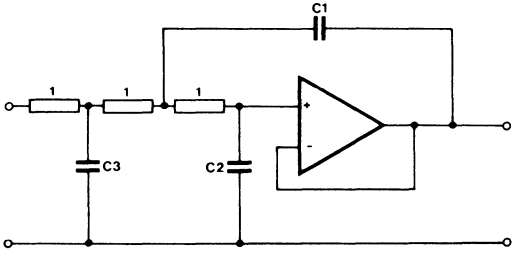
However, for many purposes, a simple basic circuit forms a useful building block to create filters up to moderate orders.



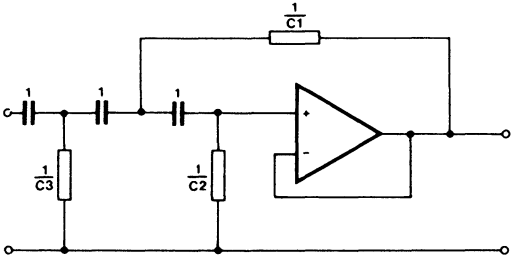
(a) Low-pass, 2nd order



(b) High-pass, 2nd order



(c) Low-pass, 3rd order



(d) High-pass, 3rd order

Fig. 2 Unity gain Sallen-Key stage

Such a building block is the Sallen-Key circuit, also known as the VCVS (voltage controlled voltage source) realisation. Its major advantages are that it uses only one op. amp per stage, and it can be used in a unity gain configuration. This means that signal amplitudes are maintained irrespective of the filter order.

The unity-gain Sallen-Key stage is shown in Fig 2(a) and (b) in both low pass and high pass forms.

The component values are for normalised parameters, and demonstrate the transforms which link the two forms.

For odd order filters, the first stage includes an additional RC circuit to generate the real axis pole, as in Fig. 2(c) and (d).

These filter stages may then be combined, in parallel or in cascade, to form the required overall response. The component values may be de-normalised by calculation of the required pole positions, or by the use of tables.

Tables 1, 2, 3 and 4 give values for low pass Bessel, Butterworth and Chebychev filters of up to 6th order, for 1dB and 3dB passband ripple for the Chebychev type, normalised to one radian/second.

These tables may be used as follows; having picked the filter type and order, the capacitive values, in Farads, are read from the table. These are the values normalised for a −3dB cut off frequency of 1 radian/second; they are therefore divided by $2\pi fc$ where fc is the required cut off frequency in Hertz.

This gives a valid set of scaled values for the required filter; however, the resistor values are all 1 ohm, and the capacitor values will still be very large. This RC imbalance is corrected by selecting a suitable arbitrary impedance scaling factor M. The resistor values are multiplied by M and the capacitor values are divided by M to give the final component values.

It is useful to note that since each filter stage has a low impedance output, directly from the op. amp output, there is negligible interaction between the stages.

It is therefore possible, and often desirable, to use different values of impedance scaling factor M for each stage, to achieve convenient component values.

The same procedure is followed for high pass filters, except that the initial values, as indicated in Fig 2, are the reciprocal of the table figures, in ohms, for the resistors and 1 Farad for the capacitors. Frequency and impedance scaling procedures are then identical.

Poles	Stage No.	C1	C2	C3
2	1	0.907	0.680	—
3	1	1.42	0.254	0.988
4	1	0.735	0.675	—
	2	1.01	0.390	—
5	1	1.01	0.310	0.871
	2	1.04	0.310	—
6	1	0.635	0.610	—
	2	0.723	0.484	—
	3	1.07	0.256	—

Table 1 Bessel filter

Poles	Stage No.	C1	C2	C3
2	1	1.41	0.707	—
3	1	3.55	0.202	1.39
4	1	1.08	0.924	—
	2	2.61	0.382	—
5	1	1.75	0.421	1.35
	2	3.24	0.309	—
6	1	1.04	0.966	—
	2	1.41	0.707	—
	3	3.86	0.259	—

Table 2 Butterworth filter

Poles	Stage No.	C1	C2	C3
2	1	2.22	0.606	—
3	1	16.2	0.0643	2.57
4	1	3.13	1.27	—
	2	7.55	0.149	—
5	1	8.88	0.254	3.94
	2	11.6	0.0936	—
6	1	4.41	1.90	—
	2	6.02	0.312	—
	3	16.5	0.0643	—

Table 3 1dB Chebychev filter

Poles	Stage No.	C1	C2	C3
2	1	3.10	0.456	—
3	1	4.34	0.0253	3.63
4	1	4.86	1.05	—
	2	11.7	0.0943	—
5	1	15.8	0.160	5.92
	2	18.2	0.059	—
6	1	7.01	1.61	—
	2	9.58	0.200	—
	3	26.2	0.004	—

Table 4 3dB Chebychev filter

Amplifier programming

In general, the filter characteristics will be largely independant of the amplifier parameters, provided that the amplifier gain-bandwidth product is around ten times the highest frequency of interest. This effectively limits the use of active filters based on the TAB1042 family to cut off frequencies up to about 100kHz. However, acceptable, though degraded, results may be obtained at higher frequencies.

Below this limit, it is obviously advantageous to reduce the programming current to minimise power consumption, without degrading the filter response. The above relationship is a rough guide, but the optimum economy is best found by experiement, since it may depend on signal amplitude if slew rate becomes the limiting factor.

For the maximum economy, in a multistage filter, the TAB1043 offers the possibility of programming only the most critical stage to a higher level than the others.

This will normally be the last stage especially in the Chebychev filters, where the peak response at the highest frequency is relatively sensitive to the amplifier response.

References: R. R. Shepard – Active Filters, Part 13 – Electronics August 18 1969
D. Lancaster – Active Filter Cookbook – Howard Sams & Co. 1975

3. A post-sampling reconstitution filter using the TAB1043

Introduction

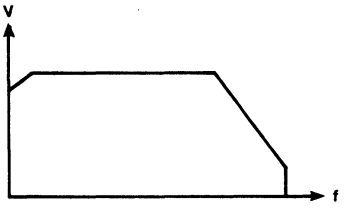
The process of time-sampling a data waveform for multiplexing. computer processing or other purposes, imposes certain restraints and modifications on the frequency spectrum of the data. Within these limits, it is possible completely to reconstitute the data, given a filter with appropriate characteristics. This note describes such a low-pass filter, suitably configured for the reconstitution of sampled data in a voice-frequency system. This is based on the standard telecommunications bandwidth of 3.5kHz, using a sampling frequency of 8kHz. It can be satisfactorily implemented using three operational amplifiers and the use of the TAB1043 quad programmable operational amplifier is discussed. The use of the fourth op. amp of the TAB1043 to provide the sample-and-hold function preceding the filter is also described.

Sampled data systems

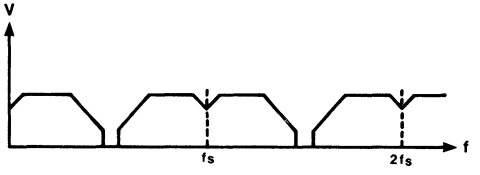
Provided that a data waveform has been sampled at a rate at least equal to twice highest frequency component present, sampling theory shows that the data can be fully reconstituted without any distortion or loss of information. Having decided the highest frequency component of interest and therefore the minimum sampling frequency, the appropriate relationship is normally ensured by pre-filtering the data before sampling. The relationships in the frequency domain are illustrated in Fig. 4, together with an example of the effects of failing to ensure properly band-limited input data. This 'reflection' of excess high frequency components back into the data band causing distortion and interference, is known as aliasing.

Given that the input data has been appropriately band-limited, it is clear that the effect of taking discrete samples of the data is to add high frequency signals in the form of repetitions of the input spectrum symmetrically placed about the harmonics of the sampling frequency. If these high frequency additions are removed by suitable filtering, the original baseband data can be fully restored; a straightforward low-pass filter with a cut-off at or just below half the sampling frequency is all that is required.

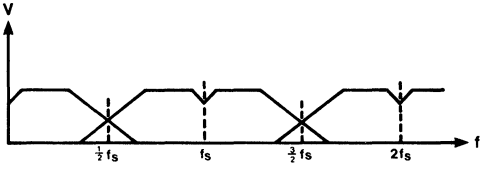
This simple treatment is based on the use of the theoretical delta function (zero-width) discrete samples.



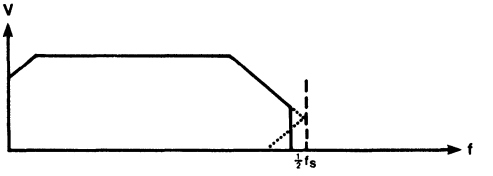
(a) Baseband data



(b) Spectrum sampling data (f_S = sampling frequency)



(c) Sampled data, insufficiently band limited



(d) Low pass cut-off at $f_S/2$;
data from (b) correctly reconstituted
data from (c) includes interference

Fig. 4 Sampled data spectra

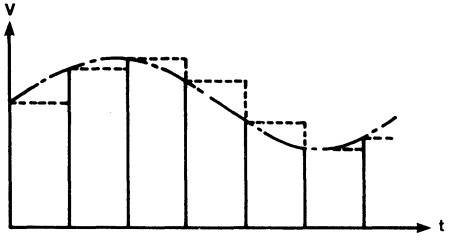
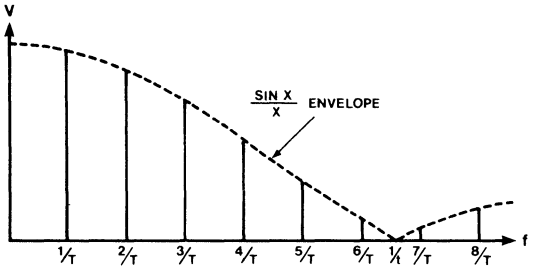


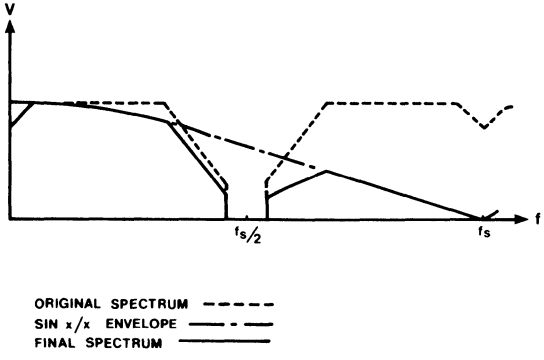
Fig. 5 Discrete and stretched samples

Such a sample sequence is approximated by the demultiplexed output of many sampled-data systems such as time-division multiplexed transmission and telemetry systems, real-time data processing output etc., where the data sample mark-space ratio is less than about 0.05. With such low values of m/s ratio however, and given the limited peak amplitudes of practical systems, the average output is very low, leading to low signal-to-noise ratios. This may be overcome by using a sample-and-hold to 'stretch' the samples to fill in the intervals (see Fig. 5).

This technique considerably increases the signal power available and gives a filtered output of essentially the same amplitude as the sampled input. It also introduces another unlooked-for side effect which is shown in Fig. 6.



(a) Pulse train spectrum: t = pulse width 1/T × prf



(b) Sampled data spectrum, 'stretched' samples

Fig. 6 Pulse train and sample spectra

Spectrum distortion in reconstruction

It is well known that the spectrum of a pulse train is a series of discrete harmonics within an envelope of the form sin x/x where $x = \pi f t$ in radians, f is the frequency variable and t is the pulse width. The implication of this on the sampled data spectrum is shown in Fig. 6; when the pulse (i.e. sample) width is stretched as described on the previous page to equal the sampling period, the spectrum is modified by the sin x/x envelope with its first zero at the sampling frequency. This means that the low-pass filter reconstituting the data needs to have the inverse of this function over its passband to ensure that undistorted data is available. The necessary filter response is shown in Fig. 7. The idealised form shows a rise of 3.9 dB just before the cut-off at half the sampling frequency; a practical approximation can be achieved with a final roll-off of 36 dB/octave, implying a 6-pole filter which can be realised with three active filter stages.

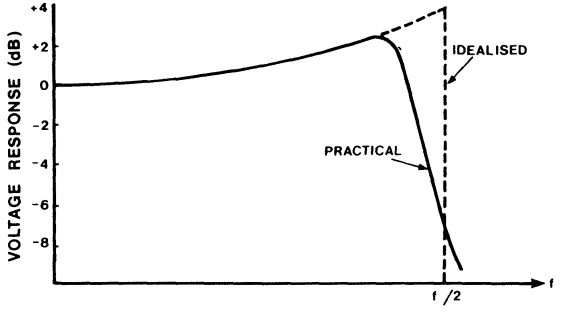


Fig. 7 Required filter response

A voice frequency reconstitution filter

A useful area of application is in voice-frequency systems in telecommunications and related fields, where a sampling rate of 8000 samples per second is used, based on a data band up to approximately 3.5 kHz. A target characteristic for such applications is shown in Fig. 8a; the inverse sin x/x function is maintained up to over 3.2 kHz, following which the response rolls off to a final rate of 36 dB/octave, achieving —7dB at the half sampling rate of 4 kHz. The combination of this with the sin x/x sampled-data spectrum envelope provides a target response with the following key parameters:-

Passband flat to 3.2 kHz
0 to —2 dB at 3.5 kHz
—10 dB at 4. kHz
—25 dB at 5 kHz and above

This characteristic was synthesised using the amplifiers of a Plessey Semiconductors TAB1043 quad programmable op. amp. The synthesis was based on the standard Sallen-Key circuit with the individual stages adjusted to give the required combined characteristics; computer-based analysis and simulation were used to assist in choosing the individual stage characteristics. The circuit is shown in Fig. 9b and the achieved characteristic is compared with the target in Fig. 8b.

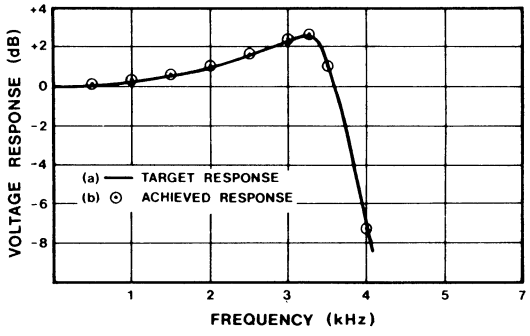


Fig. 8 Voice frequency filter responses

As can be seen, the achieved response conforms closely to the theoretical target. This response was obtained using normal tolerance components and without special timing; since no high-Q stages are needed, component sensitivity is not a severe problem.

The TAB1043 is a 3 + 1 programmable op.amp; that is, one of the four amplifiers may be programmed independently of the other three. The filter is implemented on the three jointly programmed amplifiers for which adequate bandwidth is ensured by a programming current of only 6μA (2μA per amp). It is worth noting that at this level of bias, the three amplifiers are drawing a supply current of only about 180μA total, so that it is a circuit which is well suited to battery-powered systems. The fourth amplifier is available for other uses and may be programmed accordingly.

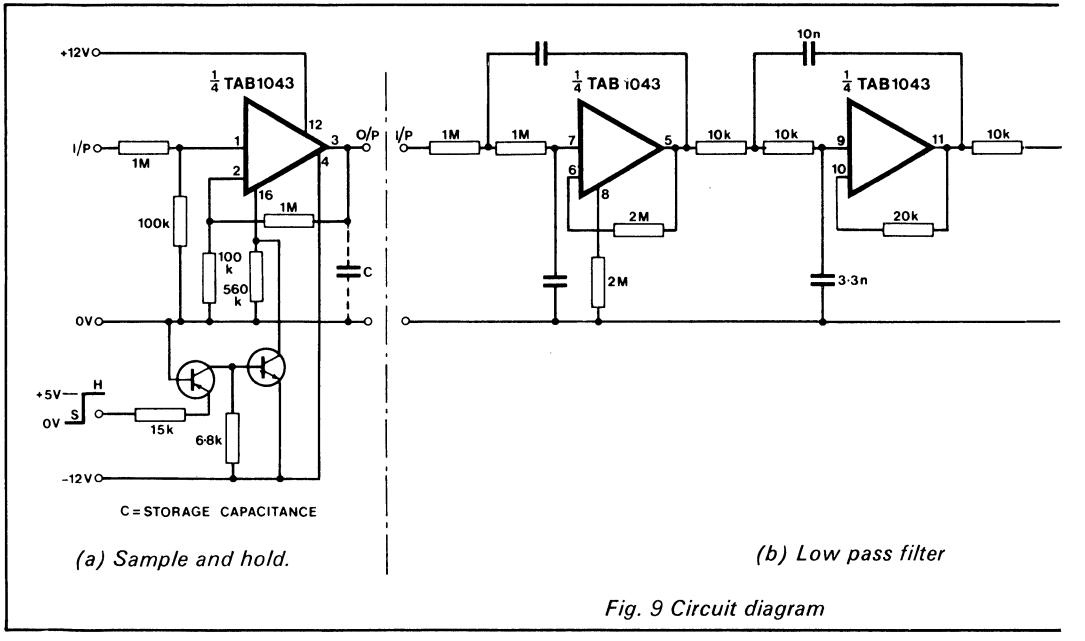
Integral sample-and-hold circuit

If the programming current for the fourth amplifier is reduced to zero, the output stages are switched off and the output impedance rises to a high value. This property may be used to make a sample-and-hold circuit to work with the filter which has been described. It is particularly interesting that such a sample-and-hold does not have to be particularly good; provided that

the sample value is acquired accurately, quite substantial droop levels can be tolerated with only small effects on the filter output level and spectrum shape. A circuit for such a sample-and-hold is shown in Fig. 9a.

It will be noted that the filter input has been arranged to have a fairly high input impedance, in order to work directly from the hold storage capacitor. In practice, it was found that in a bread-board arrangement the stray capacitance provided sufficient storage, in conjunction with the high impedances of the switched amplifier output and the filter input, to give quite satisfactory data recovery without any overt storage capacitor being connected, despite gross droop levels up to 50%. However, this would be dependent on the physical construction of the circuit, and in many cases, a small capacitor would be advisable. This does however, point up dramatically the fact that a very droopy sample-and-hold performance is quite acceptable in this application. The advantage of this is that a small storage capacitor can be rapidly charged, reducing the acquisition time in the same mode; this is further expedited by using a fairly large programming current in the sampling mode. The value used, approximately 25μA for the one amplifier, gave an acquisition time of around 15μsec.

As an illustration of the overall effectiveness of this



(a) Sample and hold.

(b) Low pass filter

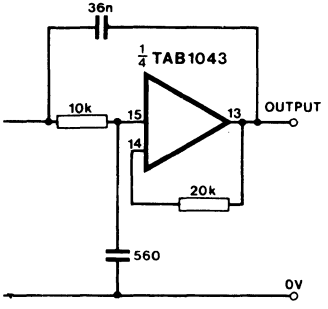
Fig. 9 Circuit diagram

scheme the data spectrum of the combined sample-and-hold and filter is shown in Fig. 10. The key parameters of the response are:

Passband 0 –	3.2 kHz	±0.3dB
	3.5 kHz	–2dB
	4 kHz	–10.5dB
	5 kHz	–29 dB

Comparing this response with the target figures shows that the objectives have been met or exceeded in all respects. The passband flatness to within ±0.3 dB indicates good compensation of the sin x/x roll-off, and with careful layout the stopband rejection can exceed 55 dB over the whole band from 7 kHz upwards.

This response would not be adequate for the most demanding applications in, for example, national telecommunications networks, where data may be passed through such filters many times. However, it shows a very use performance for a large number applications in small communications systems, voice-frequency telemetry systems, reconstitution of analogue data following computer processing etc. It also demonstrates that excellent results may be obtained in such systems with a relatively simple, non-critical filter design, based on an economical quad op.amp with very low power consumption, the TAB1043.



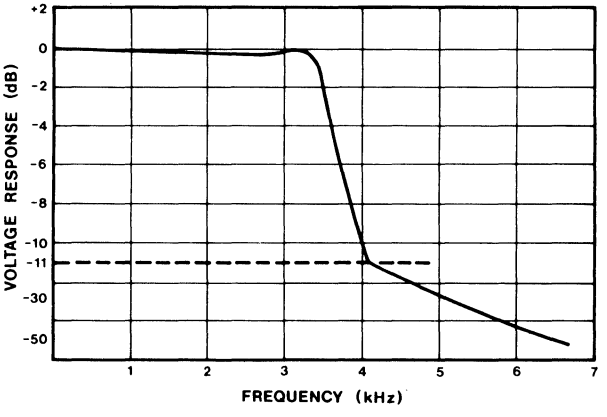


Fig. 10 Filter response with sample and hold.

3. TAB1040 Series Active Filter Applications

1. Operational amplifier characteristics

The term operational amplifier was used many years ago for valve amplifiers which could be connected with resistors and capacitors to produce a particular output for a specified input. Their main use was in analogue computer type applications where their expense could be justified. Nowadays, in integrated circuit form, the operational amplifier is available very cheaply with a price comparable to that of a single transistor and a pair of resistors and in packs containing one, two, three or four amplifiers per package. Their cheapness changes design techniques in much the same way as did the production of integrated circuit logic packs in that it becomes economic to use multi-amplifier packs even if all the circuits contained are not used. Each stage in a system may have its own amplifier dedicated to it rather than trying to combine two processes in a single amplifier stage. This often simplifies design.

The operational amplifier is obviously an amplifier; that is, the output is a larger version of the input. It operates at DC and also responds to changes of input up to a moderate frequency. The amplification or 'Gain' is usually expressed as the ratio of output voltage to input voltage and for small input signals is very large, typically 100,000. Expressed in decibels (dB) this is 20 $\log_{10}$ 100,000 = 100dB.

The usual operational amplifier has two input terminals, one output terminal, and two supply line terminals. The diagram Fig. 1. shows the usual representation of the amplifier but sometimes, to avoid complicating a circuit diagram, the connections to the supply lines or power supplies are omitted. In practice, the power supply connections *must* be made.

The input terminals are called 'inverting' and 'non-inverting' and may be given the symbols − or + respectively.

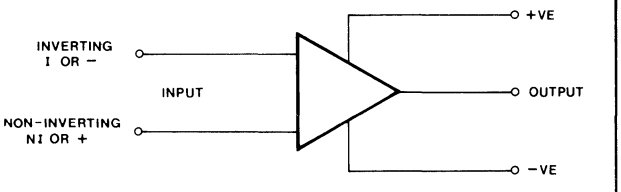


Fig.1 Basic operational amplifier

Differential or Difference Operation

The amplifying behaviour of an operational amplifier may be compared to the action of forces on a see-saw. Assume initially the system sets out at zero or the level position, that is there is no output. One end may be forced down by either a push down on that end or a pull up on the other end. More effect may be obtained by a simultaneous push down and pull up on opposite ends. The overall effect is due to the difference of the turning effects produced by forces applied to each end. For the operational amplifier, the output depends mainly on the difference of the two voltages applied to the two input terminals. As in the see-saw analogy the direction of the push/pull sets the direction of the movement change, so the polarity of the difference voltage sets the direction of the voltage output change. With one input terminal selected as a reference, a voltage applied to the other input terminal may give a larger output voltage change of the same polarity, in which case the input is said to be applied to the 'non-inverting' terminal. If the output is of the opposite polarity to that applied to the input, the input is said to be applied to the 'inverting' terminal.

The ratio between the output voltage change and the difference input voltage is called the signal voltage gain and for linear and therefore non distorted operation should be constant irrespective of signal size. In practice the gain tends to be a little less for large signals than for small. The large signal gain is usually the gain quoted as it represents worst case operation. The large signal voltage gain of 95dB for the TAB 1042 is equivalent to antilog 95/20 = 56,234.

Common Mode Operation

Taking the see-saw analogy again, if equal pull downs or push ups are applied simultaneously to both ends, there is little effect. Similarly with the operational amplifier, if the input voltages are equal (that is there is zero difference input voltage), equal changes of input voltages have little effect. The gain given by the ratio of the output voltage change to the so called common mode input voltage change is small. The ratio of the difference gain to the common mode voltage gain is referred to as the Common Mode Rejection Ratio (CMRR). If this is 110dB and the difference gain is 95dB, the common mode gain is −15dB or 0.18. To illustrate the significance, a 50μV difference signal will produce an output change of 2.8V whereas a common mode input signal of 15.6V is required to give the same output change. In practice, it is therefore reasonable to assume that the mean level of the input signals has negligible effect compared to the difference between their levels.

Maximum Size of Input Signal

There is a limit to the size of input signal which may be applied. Consider first the difference signal. The maximum input difference signal for normal operation is likely to be 100mV or less to sweep the two transistors connected to

the input terminals over their normal operating region. Greater input voltage will result in one transistor's base emitter junction being reversed biased and its reverse breakdown voltage can be exceeded if the difference voltage is too high. The result may be catastrophic.

Similarly, if the common mode voltage is too great (positive or negative), breakdown damage can occur. Also the amplifier will cease operating correctly if an internal transistor becomes saturated or turned off and this will occur at values less than the external supply voltages. There are two ratings therefore for the common mode input voltage, one to guard against damage and a lower voltage rating to ensure that the amplifier will still be capable of amplifying the difference voltage.

Output Conditions

It is possible for the output voltage to be taken differentially, much as the input voltage is applied, but most operational amplifier applications have the output connected to a load which is also connected to earth or the supply terminals. For this reason, most operational amplifiers need only a single output terminal and the output voltage is then developed relative to earth or one of the power supplies depending on the application. The single output terminal also reduces the required number of pin connections. This is a particular advantage in multi-amplifier packs.

The maximum available output voltage must be less than the supply voltages due to voltage drops in internal amplifier components. The output current of most operational amplifiers is usually limited internally to some safe value and expressed as the 'short circuit current'. If the amplifier is of the programmable type, that is, the current which it draws from the supply under normal conditions can be set as required up to some maximum value depending on design, then this too will affect the maximum output current which can be taken. There is clearly a relationship between output voltage, load resistance and current under normal operating conditions and this load current is less than the short-circuit current. For example, with ± 12V supplies and a 4 kilohm load between the output terminal and the 0 volt line, the maximum output voltage swing can be ± 10V and therefore the current swing is a maximum of ± 2.5mA whereas the short circuit current may be quoted as 4mA.

Supply Voltages and Current

Most electronic amplifying devices are unidirectional devices, that is they only respond to particular polarities of input voltage and current. The bipolar transistor for linear operation requires the base emitter junction to be forward biased and the base collector junction to be reverse biased. Under these conditions, the input/output characteristics of base emitter voltage and collector current are as shown in Fig. 2. For the silicon transistors of integrated circuits, a

base emitter voltage of about 0.6V is required before any collector current starts to flow. If the base emitter voltage is set to about 0.65V, a small change of voltage about this level produces a proportional change of collector current.

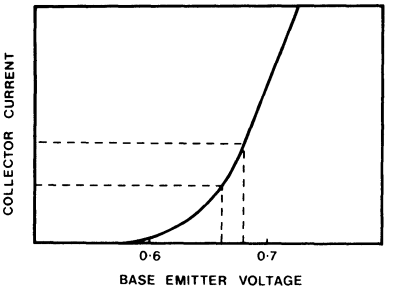


Fig.2 Input/output characteristics

If this current were flowing through a resistor connected in series with the collector, the change of current could produce a change of voltage drop which is larger than the change of base emitter voltage which produced it. As far as voltage changes are concerned, this represents amplification.

The operational amplifier contains many cascaded transistor amplifier stages all of which must be biased 'on' to produce the proportional larger change of output voltage for a change in input voltage. Supply voltage and current are needed to set up these conditions which are called 'bias conditions'. There is a minimum collector emitter voltage which can be obtained even with large signal drive and this limits the maximum output voltage obtainable to less than the supply voltage.

As quoted in the previous section the best linear output with ±12V supplies may be only ±10V.

If, by mistake, power supplies of the wrong polarity are connected the amplifier may be destroyed.

Why are two supplies quoted, are they both necessary? The answer is that two supplies can give a more convenient system than a single supply but in some applications a single supply only is needed. The bias conditions represent an offset of input and output on which the amplification is produced. If the system is a DC one, both input and output must be capable of being positive or negative with respect to their reference, and ideally give zero output voltage for zero input voltage. Clearly, two voltage supplies are necessary, one positive with respect to the reference and the other negative. The two supply voltages are usually equal but opposite. Fig.3 shows the arrangement with a possible way of simulating two supplies with one floating supply. It has however the disadvantage of requiring a large current

through the potential divider, probably several times that passing through the amplifier to give an effective zero voltage reference.

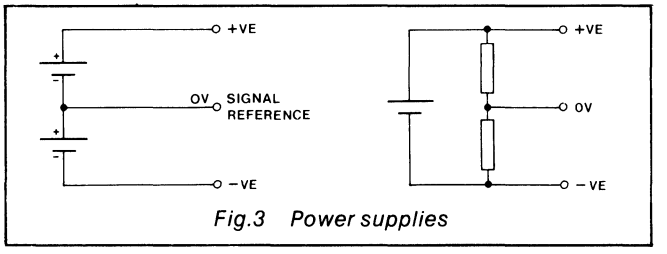


Fig.3 Power supplies

If signals with no DC component are to be amplified, the circuit of Fig.4 may be used with the changing input signal and output signal isolated from the bias levels by means of capacitors. R_3 is necessary to avoid the inputs being shorted together and producing zero difference input signal voltage. It is usually sensible to set R_1 and R_2 equal so that the input bias level is midway between the supplies with R_1 and R_2 passing a current of several times the input bias current. (See Input Bias Current, P. 8

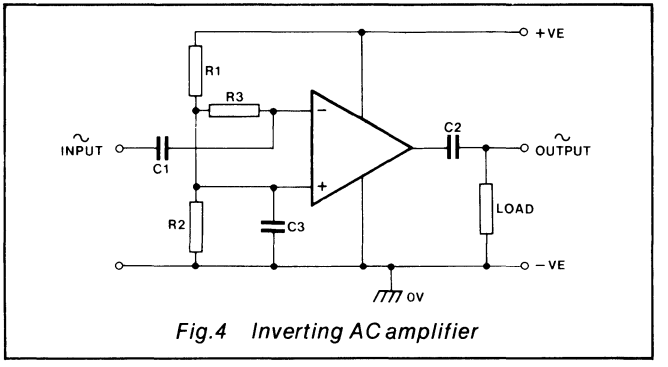


Fig.4 Inverting AC amplifier

C_3 makes the junction of R_1 and R_2 zero voltage to the alternating input signals provided that C_3 is large enough. The input signal is effectively applied between the inverting input of the amplifier and the non-inverting input which is AC earthed through C_3.

In general, the current drawn by the operational amplifier depends on the load current. The amplifier draws the current required to bias each transistor on and the current supplied to the load. For example, in the two supply configuration, the amplifier may draw 1.6mA when the output voltage and therefore the load current is zero, yet with a steady output voltage of +10V across a load of 4kilohms, the positive supply may be required to deliver 4mA and the negative supply only about 1.5mA.

Programmable Amplifiers

Some operational amplifiers are called 'programmable'. This describes the facility of selecting, within limits, the supply current required of the operational amplifier. The older range of operational amplifiers did not have this provision and therefore in applications where only perhaps 1mA of output current was required from an amplifier which was capable of delivering an output current of 20mA and needed comparable supply current, the system was wasteful in current and power. In complicated systems or battery operated systems waste of current may be unacceptable. The programmable operational amplifiers allow the supply currents demanded by the amplifier to be related to the output current required. This results in economies in power supplies and reduced heat generation. There is a price to pay for lower current operation however; the impedance levels are higher leading to more noise and pick-up problems and the lower bias current leads to a reduction in the frequency response and the slew rate (definitions given later).

Supply Voltage Rejection Ratio (SVRR)

Ideally the output voltage of an amplifier should not change if the supply voltage changes. The SVRR gives the sensitivity of the output to supply voltage. An SVRR of 96dB with a voltage gain of 95dB shows that the 'gain' to supply voltage is −1dB. A 1 volt change in supply can produce a 0.9V change in output voltage equivalent to a difference input voltage of 16μV. With the two-supply system, equal but opposite changes tend to compensate each other.

Input Bias Current

The section on power supplies described the need for bias in order that the transistors within the amplifier operate in the linear input/output region. Each transistor is biassed with its base emitter voltage about 0.65V. However direct current is required into the base for collector current to flow and therefore for the amplifier to operate. This base direct current must be supplied from an external source for the two input transistors whose bases are connected to the non-inverting and inverting terminals. In a two supply system, it is sufficient for the current to be supplied through a resistor between the input terminal and the reference voltage (or earth). In a negative feedback configuration as in Section 3, a resistor connected from output to the inverting input terminal can supply the current to that input and only the other input needs a separate resistor connected to earth. If the input transistors are NPN types, current flows into the bases in the conventional sense, and the volt drop across these base bias supply resistors will mean that each input is biassed slightly negative with respect to the reference. An input bias current of 250nA flowing through a resistor of 10kΩ gives a voltage drop of 2.5mV.

Input Offset Current and Voltage

An FET input stage preceeding, or integral to, the amplifier reduces the input current required by several orders of magnitude and such amplifiers can be used in applications where bias currents give difficulties.

The ideal operational amplifier has identical transistors connected to the input terminals so that the gain performance from each input differs only in their inverting or non-inverting gain property. In practice, the transistors are nearly but not quite identical so that the input bias currents and the base-emitter voltages for the same collector current may differ slightly. Equal input bias currents and voltages result in a non zero output voltage.

These difference effects are termed input offset current and input offset voltage and the quoted values represent the limits of the unbalance of the amplifier adjusted to give zero output voltage. A typical input bias current is quoted as 250nA and is an average input bias current to be expected. The input offset current may be quoted as 20nA so that the input bias currents may range from 240 to 260nA.

The input offset voltage may be quoted as 1mV which means that if the amplifier gain is 56,000 and both inputs are shorted together, the output would try to reach 56V. In practice, this means that the output voltage would be close to one of the supply voltages depending on the direction of the offset. Negative feedback generally reduces the effect.

Some operational amplifiers incorporate means by which the user may balance out the offset using an external potentiometer.

For most purposes, such offset adjustment is unnecessary, as the selected closed loop gain is small.

Frequency Response

Internal to the transistors of the operational amplifier is capacitance. As the frequency of operation rises, this reduces the gain of the transistors but increases the phase lag between alternating input and output voltages so that in a multi-transistor unit such as an operational amplifier, phase shifts of more than 180° over those at low frequencies can be expected at high frequencies. Many applications of operational amplifiers use negative feedback as covered in Section 3, and so with possible extra phase shift of 180°, the feedback may become positive. If the feedback loop is considered, should the loop gain be more than 1 at a frequency where the loop phase shift is 0 or 360°(resulting from the 180° innate in negative feedback with an additional 180° from the extra phase shift through the amplifier) the signal will regenerate itself around the loop. This represents oscillation and makes the amplifying system useless.

To overcome this problem, manufacturers often include an extra capacitor within the amplifier circuit. This forms, with internal resistance, a dominating time constant so that

the resulting frequency response of the amplifier falls off at 6dB per octave from a low frequency and has a maximum extra phase lag of 90° to a frequency at which the gain has fallen to 1. It is impossible to make such an amplifier system oscillate without deliberately applying positive feedback.

The frequency response may be presented either in the form of a graph, as a gain bandwidth product, or the frequency at which the gain has fallen to 1. If the system gain is ten times or 20dB and the bandwidth is found to be 50kHz, then the gain bandwidth product is 500kHz. The usefulness of this figure for the simple dominating time constant system is illustrated in Section 3 in predicting the expected response of a particular gain configuration. There is a price to be paid for the freedom from oscillation. The manufacturer 'compensates' the amplifier by means of the capacitor for the worst conditions which is 100% negative feedback. The capacitance worsens the frequency response of the amplifier from that in the uncompensated form. If less than 100% feedback is applied the compensation is greater than necessary and the resulting frequency response worse than necessary.

Some amplifiers are produced so that the designer may select his own value of compensating capacitor, but he could make an error and produce an oscillating system.

Slew Rate

The slew rate describes how fast the output voltage can change and represents the limit of its performance without its internal circuits becoming overdriven and the resulting output waveform becoming non-linear and distorted. In compensated amplifiers, the component which sets the slew rate is the compensating capacitor.

If the quoted slew rate is 1.5V/μs, a step voltage at the input no matter how large or fast, cannot make the output change faster than 10V in 15μs. For a sine wave signal with frequency f, a 1V peak signal has a maximum rate of change of $2\pi f$. For the maximum rate of change of 1.5Vμs, the amplifier is able to provide a peak output signal of 1V at a frequency of 240kHz. If a 10V peak output signal is required without slew rate distortion, the maximum frequency at which the stage output could be obtained is 24kHz. Should the amplifier be overdriven, the waveform appears to 'triangulate'.

The slew rate cannot be improved without adding an extra voltage amplifying stage to the amplifier output and this is difficult using discrete components. If the slew rate of a particular amplifier is insufficient, the best solution is to select another amplifier. Such amplifiers are likely to be more expensive.

If the amplifier feeds into a very capacitive load, the slew rate may be limited by the maximum output current. If this output current is 4mA, then into a 4nF load the voltage

cannot rise faster than 1V/us, (dV/dt = i/c). If this is the limitation, a current amplifier such as an emitter follower (as in Section 2) can speed up the system to the original slew rate.

Relationship Between Frequency Response and Slew Rate

There is often a confusion between frequency response and slew rate. In case the distinction is not clear consider the following example.

In Section 3 a feedback system is designed for a gain of about 30 and the frequency response extends to 117kHz. The slew rate is unaffected by the feedback since this is a limiting, or non-linear, phenomenon and is 1.5V/μs. At 100kHz the maximum output is therefore limited to 2.4V peak. For an input signal giving an output of 2.4V peak the response is constant up to 100kHz.

However, for an input signal which gave an output of 10V peak at low frequencies, the output would become distorted at frequencies above 24Khz due to the slew rate distortion. The rise time of the output is also a function of either the frequency response or the slew rate. It is defined as the time taken for a 'step' output to rise or fall between 10% and 90% of its final value and for small output signals (not limited by slew rate) is $0.35/f_3$ where f_3 is the 3dB frequency for the simple systems.

The initial rate of rise is $2\pi f_3 V_{OUT}$ V/s, where V_{OUT} is the final step and distortion will occur if the attempted rise exceeds the slew rate.

Temperature effects

The main effect of temperature on the performance of the operational amplifiers is to change the bias conditions and the offsets. Compensation tends to be difficult because the temperature coefficients are difficult to match with passive components even if those coefficients are known.

Noise

Noise is unwanted signals appearing in the output and some noise is unavoidable. Most amplifiers have an optimum source resistance for minimum noise and some amplifiers are designed to have less noise contribution than others. Some authors recommend a small (typically 3pF but depends on application) capacitor to be placed across the feedback resistor in feedback applications for least noise. If the input signal to be processed is in the mV region, there is usually little trouble from noise.

2. The operational amplifier as a comparator

The operational amplifier has a very large gain to difference signals but small gain to common mode signals. If the gain of the amplifier to difference signals is 50,000 then the output can change the maximum possible of ± 10V from supply voltages of ±12V for a difference signal of 20/50,000 = 0.4mV.

The output of the operational amplifier therefore can signify which of two inputs is the greater to an accuracy of 0.4mV. Any input offset of the amplifier may increase this value but it is still small. Therefore the operational amplifier is useful to compare which is the greater of two input signals.

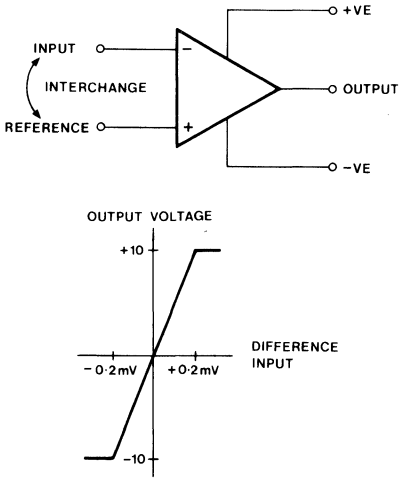


Fig.5 Comparator and characteristics

The basic comparator connection and characteristics are shown in Fig. 5. Depending on the application, the input is connected either to the inverting or non-inverting input terminal and the reference to the other. The mean level of the threshold of changeover represents a common mode signal and may have a slight effect. It will be best chosen to be midway between the supply voltages where the common mode signal is effectively zero.

An application is shown in Fig. 6. The input circuit is that of a bridge with the reference set by means of a potential divider from the supply. In the other branch is an element whose voltage drop can vary with the physical conditions

which we wish to detect. For example, it could be a thermistor whose resistance falls with increase of temperature or, as shown, a photo-transistor whose current is a function of the light intensity.

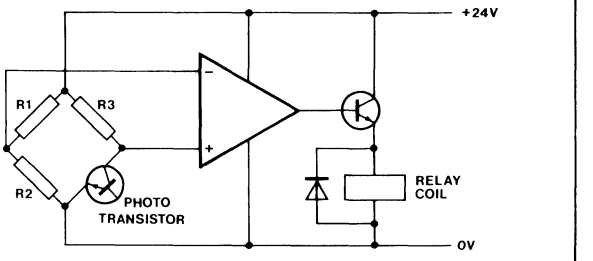


Fig.6 Light operated switch

Example Design the circuit as a unit to detect the light level at which auxiliary lighting is to be switched on. A relay contact is required to switch the mains lighting.

We need to know about the characteristics of the detector. Let the chosen photo-transistor pass a current of 0.1mA in the dark and 1mA in good light. Design for extra lamps to be switched on corresponding to a transistor current of 0.4mA. Look for a relay which seems suitable. Firstly, it should have contacts which can carry the lamp currents and secondly it should be compatible with the operational amplifier output. A particular relay seems suitable in that it has a resistance of 500 ohms and an operating current of 40mA which means a voltage of 20V across it. Whereas this voltage level fits in with the operational amplifier, the current required is in excess of that from many amplifiers and an emitter follower current amplifier can be used to boost the output current of the operational amplifier from 1mA say to the 40mA needed. The transistor is required to have a minimum current gain of 40 which is relatively modest.

In this application, a single voltage supply of 24V will be adequate and the input threshold level can be set conveniently to 12V. For R_3 to drop 12V when the photo transistor passes 0.4mA, R_3 equals 30 kilohms assuming that the input current to the amplifier is negligibly small (it is much less than 0.4mA). R_1 and R_2 are equal to get the 12V reference and can be chosen as 30 kilohms also, for convenience. Check that the circuit operates in the right sense. In full light, the photo-transistor passes 1mA and R_3 tries to drop 30V. The calculation shows that the photo-transistor's current is limited by saturation to less than 24/30k = 0.8mA. The collector voltage, which is the same as at the non-inverting input terminal, is small and the amplifier output voltage is

about the minimum of 2V giving 1.3V across the relay coil. In the dark conditions, R_3 drops 3V with the 0.1mA flowing through it, the non-inverting input is at 21V, some 9V above the inverting input and the output of the amplifier rises to the maximum of 22V. The voltage across the relay coil is 0.7V below, giving 21.3V to drive current through the relay coil. Provided that the relay is not energised with 1.3V across it under light conditions, the circuit should work as required. There may be a need to protect the transistor's output from large voltages induced if the relay current is changed abruptly during switch-off. A diode is often used as shown. (Fig.6).

Problems of Using Operational Amplifiers as Comparators

1 Comparators can be subject to latch-up which is a condition in which too great an input difference voltage causes the output to go to a value near to one of the supplies and not respond to subsequent changes of input voltage. A well designed comparator is free from this problem. Series resistors in the inputs may be helpful preventatives.
2 The maximum allowable input voltages and difference voltages must not be exceeded. These tend to cause junction breakdown in the input transistors and make circuit operation abnormal and perhaps produce irreversible damage to the amplifier.
3 The major characteristic which gives problems is the speed of response. A slew rate of 1.5V/μs means that the output takes 30μs at least to change between extremes. The main reason for this rather long time is the compensating capacitor included within the amplifier so that it cannot oscillate under negative feedback conditions. For faster operation of a comparator, either an uncompensated amplifier or a custom designed comparator will be required.
4 Common mode effects are likely to be negligible.
Some designers include resistance in series with the inputs of a few thousand ohms. This is intended to avoid latch-up and the possibility of excessive loading of the input sources but are often not necessary with a well designed comparator. If included, the resistors should not be large enough to give too great a series voltage drop with input bias current or to slow up the rise of input in conjunction with the input capacitance.

Zero Crossing Detector

The comparator can detect when an input crosses the zero voltage threshold if the reference is zero. Offset and speed of response can give errors.

Window Comparators and Out of Bounds Detectors

A comparator detects whether or not an input is above or below a threshold. Two comparators can detect whether an input is between or outside two threshold values and their outputs may be combined in a gate to detect the required conditions.

3. The operational amplifier as a linear amplifier

The operational amplifier is made with a gain which is too high for many purposes and because of small production differences, the gain of a particular amplifier is not known accurately. Negative feedback is used to set the gain of a system containing the operational amplifier to a value chosen by the circuit designer. Other advantages of negative feedback include improving the frequency response, modifying the input and output impedances, reducing the distortion and improving the noise performance of the circuit compared with that of the amplifier alone. The price to be paid is a smaller system gain than the basic amplifier has.

Simple Theory of Negative Feedback

Rather than give a general treatment of the effects of negative feedback, the two simple feedback circuits for a defined voltage gain system are considered. First the circuit of Fig. 7 shows the output connected to the inverting terminal through a resistor R_1. The inverting terminal is also connected through R_2 to the reference line or earth. (It is assumed that the operational amplifier is supplied with both a positive and negative supply with respect to the reference line). The signal input to the system is supplied to the non-inverting terminal and for completeness, a resistor R_3 is connected from this terminal to the earth. This resistor may be necessary to provide the bias current to the input or, the bias (direct) current may be provided through the signal source.

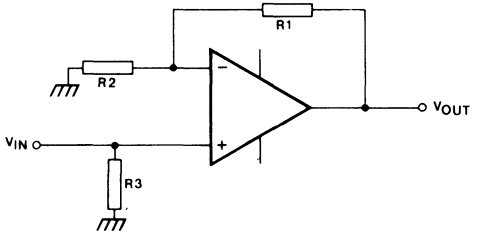


Fig.7 Inverting feedback op. amp.

Assume the amplifier has infinite gain, zero input current and output voltage unaffected by output current.

By potential divider action, the voltage at the inverting input is

$$\frac{V_{out}\,R_2}{R_1 + R_2} \quad \text{----------} \quad (1)$$

and for an infinite gain amplifier, this must be the same as V_{in}, the voltage at the non-inverting input. The system gain is, therefore,

$$\frac{V_{out}}{V_{in}} = \frac{R_1 + R_2}{R_2} \quad \text{----------} \quad (2)$$

The resistance presented to the signal source is R_3 as no signal current flows into the non-inverting input terminal.

Assuming that the amplifier is perfect gives very easy calculations but these may be too inaccurate for some purposes. For example, there is no prediction of what the likely frequency response will be. Rather than carry out a complete analysis, we complicate the analysis only as much as it is necessary to give an accurate enough answer.

If the amplifier is assumed to be perfect apart from having a non-infinite gain A_v, then the voltage at the non-inverting input is still as shown in (1) but the voltage across the input terminals to the operational amplifier is now

$$\frac{V_{out}}{A_V} \quad \text{----------} \quad (3)$$

rather than the negligible voltage for an infinitely high gain amplifier. The input voltage V_{in} applied to the non-inverting terminal is, therefore

$$V_{in} = \frac{V_{out}\,R_2}{R_1 + R_2} + \frac{V_{out}}{A_V} \quad \text{--------} \quad (4)$$

The system gain becomes

$$\frac{V_{out}}{V_{in}} = \frac{1}{\left(\frac{R_2}{R_1 + R_2}\right) + \left(\frac{1}{A_V}\right)} \quad \text{--------} \quad (5)$$

$$= \frac{R_1 + R_2}{R_2} \cdot \frac{1}{1 + \left(\frac{R_1 + R_2}{R_2}\right)\frac{1}{A_V}} \quad \text{-----} \quad (6)$$

As would be expected, if A_v is very large then

$$\frac{1}{A_v} \text{ and} \left(\frac{R_1 + R_2}{R_2}\right) \frac{1}{A_v} \text{ --------- (7)}$$

are very small and the expression simplifies into that shown in eqn (2).

However the voltage gain of the operational amplifier falls as the frequency increases. The simplest way of representing this fall-off is to assume that it is due to a single dominating capacitance and therefore a dominating time constant within the amplifier.

This response is such that at high frequencies the output halves as the frequency doubles, that is, it falls at 6dB/octave. Mathematically the gain of the operational amplifier may be written as

$$A_v = \frac{A_O}{1 + j\frac{f}{f_3}} \text{ ---------- (8)}$$

where A_0 is the DC and low frequency gain, j is the complex operator, f is the frequency being considered and f_3 is the frequency at which the gain has fallen to 0.707 or 3dB of the low frequency value. (The gain is 1dB down at $f_3/2$, 3dB down at f_3, 5dB down at $2f_3$, 12dB down af $4f_3$ etc.)

If this expression is inserted into the expression for system gain (6) and it is assumed $1/A_O$ is small compared to 1, the system gain is

$$\frac{V_{out}}{V_{in}} = \left(\frac{R_1 + R_2}{R_2}\right) \cdot \frac{1}{1 + j\frac{f}{f_3} \cdot \frac{1}{A_O}\left(\frac{R_1 + R_2}{R_2}\right)} \text{ -- (9)}$$

showing that the response of the system now falls to 3dB down at a frequency of

$$\left(\frac{R_2}{R_1 + R_2}\right) \cdot A_O f_3 \text{ --------- (10)}$$

In this simple feedback system, the product of system gain and 3dB frequency is constant at $A_O f_3$, that is the gain bandwidth product without feedback. For example, if the gain bandwidth product without feedback is 4MHz, a system gain of 1 has a bandwidth of 4MHz, a system gain of 10 has a bandwidth of 400kHz etc. (Where 'bandwidth is used synonymously with the term '3dB frequency').

In a similar way the effect of the small input current drawn by the amplifier may be taken into account. If the amplifier has an apparent resistance of R_{in} to signals across its input terminals, the current flowing into the non-inverting terminals is, by Ohms Law

$$\frac{V_{out}}{A_v} \cdot \frac{1}{R_{in}} \quad \text{----------} \quad (11)$$

Analysis shows that the system gain now becomes

$$\frac{V_{out}}{V_{in}} = \frac{R_1 + R_2}{R_2} \cdot \frac{1}{1 + \left(\frac{R_1 + R_2}{R_2}\right)\frac{1}{A_v} + \frac{R_1}{R_{in}A_v}} \quad (12)$$

The additional effect of R_{in} on the signal source is to place, in parallel with R_3, a resistor of $R_{in}A_v$ divided by the system gain.

The effect on the output resistance may be found with some little complication. If without feedback the amplifier operates as though it had a resistor in series with its output terminals of R_{OUT}, then the system acts as though it has a resistor of

$$R_{out} \cdot \left(\frac{R_1 + R_2}{R_2}\right)\frac{1}{A_v} \quad \text{--------} \quad (13)$$

in series with its output terminals (neglecting the effect of R_{in} and assuming

$$\left(\frac{A_v R_2}{R_1 + R_2}\right) \quad \text{----------} \quad (14)$$

is large compared to 1).

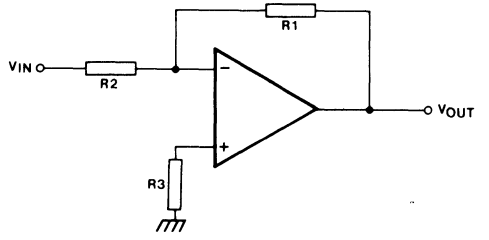


Fig.8 Non-inverting feedback op. amp.

The feedback system of Fig. 7 gives a non-inverting gain. The circuit of Fig. 8 gives an inverting gain and uses the same number of components. R_3 again may be omitted provided that provision is made for the bias current to flow into the input to the amplifier. In the simplified analysis the

amplifier is ideal. There is no amplifier input current and therefore no voltage dropped across R_3. For very large gain the voltage across the amplifier input terminals is small and the voltage at the inverting input terminal must be near zero, therefore the current flowing into R_2 is V_{in}/R_2 (from left to right) and is equal to V_{out}/R_1 flowing through R_1 (from right to left). The system gain therefore is

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_1}{R_2} \quad \text{---------} \quad (15)$$

where the negative sign indicates that the output signal is inverted with respect to the input signal. The resistance to the signal source is R_2.

If, as before, the amplifier has a gain of A_v but otherwise is ideal, the system gain becomes

$$-\frac{R_1}{R_2} \cdot \frac{1}{\left(1 + \frac{R_1 + R_2}{R_2} \cdot \frac{1}{A_V}\right)} \quad \text{-----} \quad (16)$$

and the system frequency response is

$$\frac{R_2 A_V}{R_1 + R_2} \quad \text{---------} \quad (17)$$

times that without feedback as in the case of the non-inverting system. If the input resistance of the amplifier is considered, the resulting voltage gain of the system is slightly reduced from that for the ideal amplifier divided by the near unity factor

$$1 + \left(\frac{R_1 + R_2}{R_2}\right) \cdot \frac{1}{A_V} \cdot \left(\frac{R_3 + R_{in}}{R_{in}}\right) \quad \text{----} \quad (18)$$

The resistance presented to the signal source is slightly increased; it is R_2 divided by the near unity factor

$$1 - \frac{R_1}{R_2} \cdot \frac{R_3 + R_{in}}{R_{in}} \cdot \frac{1}{A_V} \quad \text{------} \quad (19)$$

and the expression for the system's output resistance is identical to that of the non-inverting system (which is not surprising as the circuits look identical to a load on the output).

The expressions for the circuit behaviour are complicated if imperfections of the amplifier are considered but we should be sure that the approximations are justified.

Before a particular design can be completed, the effect of the bias conditions need to be considered.

It is necessary for DC bias currents to be provided to the amplifier input terminals for it to work at all. The bias is supplied through resistors which may also be those which are chosen to set the gain of the system.

The basic amplifying circuits of Fig. 7 and Fig. 8 are identical as far as bias is concerned and it can be arranged in the calculations that any path to DC from the signal source is taken into account by appropriately modifying the values of R_3 or R_2.

Fig. 9 shows the general circuit. Once again a full analysis is complicated but an accurate enough answer can be obtained by simpler means. What we need to ensure is that

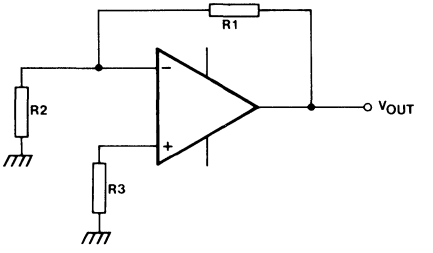


Fig.9 General amplifier circuit

the amplifier operates so that sufficient output is obtained and that any offset of the output from the designed-for value is acceptable.

Consider the effects of bias currents flowing into the two input terminals of the operational amplifier. Let them be I_I and I_N for the inverting and non-inverting terminals respectively. The voltage of the non-inverting terminal is $-R_3I_N$ by Ohm's Law. If the amplifier is assumed to have infinite gain, then the voltage at the inverting terminal is $-R_3I_N$. Summing currents at this point,

$$\frac{V_{out} + I_N R_3}{R_1} + \frac{I_N R_3}{R_2} = I_I \text{ ------- (20)}$$

Therefore the output voltage with R_2 and R_3 earthed, corresponding to zero signal voltage is

$$V_{out} = I_I R_1 - I_N \left(\frac{1}{R_1} + \frac{1}{R_2}\right) R_3 R_1 \text{ --- (21)}$$

If $I_I = I_N$, that is there is no offset bias current, the output offset voltage due to bias current will be zero if R_3 is chosen equal to R_1 in parallel with R_2.

For this value of R_3 and the two bias currents unequal, the output offset voltage is $(I_I - I_N)\ R_1 = I_{os}\ R_1$ (where I_{os} is the input offset current). Whether it is worth choosing the resistor values in this way will depend on the application.

In the subsequent designs, the optimum value of R_3 is usually chosen and only the offsets due to offset bias current and voltage considered. In practice, the tolerances of the resistor values could be taken into account if necessary by inserting maximum and minimum values into the equations.

If the input offset voltage is considered, we can consider its effect as being in series with the non-inverting terminal. It is therefore amplified as if it were a signal applied to the non-inverting input and produces an output offset (R_1+R_2/R_2) times. Since the offsets may be in any direction depending on the imbalance of the input transistors, the maximum output offset which may be expected is the sum of the offsets considered separately although in some cases they might compensate for each other.

Input Resistance

For the two amplifier feedback configurations the input resistance, that is the resistance seen by the source, is set by R_3 or R_2. These in turn are set by the offset specification. Increase in input resistance can be made by using an amplifier with an FET input stage or, if the input resistance can be lower at DC, the input may be bootstrapped. (For this technique consult the technical literature).

TYPICAL DESIGN OF A SYSTEM WITH A VOLTAGE GAIN OF 30 AND INPUT RESISTANCE OF 47 KILOHMS

Non-inverting Circuit

For this system, the circuit of Fig.7 is used. The gain is approximately

$$\frac{R_1 + R_2}{R_2} = \frac{R_1}{R_2} + 1 \quad \text{------} \quad (22)$$

and therefore $R_1 = 29R_2$. The input resistance is given by R_3. R_3 is chosen to be 47 kilohms. If we want minimum voltage offset at the output, then R_1 in parallel with R_2 should be about 47 kilohms. The nearest 10% preferred value of resistance is 47 kilohms for R_2 making R_1 = 1.5Mohm. The simple formula makes the gain 32.9 with resistors equal to the nominal value. If the resistor spread is ±5%, the spread of gain may be ±10% making the design accuracy seem reasonable.

Taking typical figures of 95dB for the basic amplifier voltage gain without feedback, that is antilog_{10} 95/20 or 56,234 (roughly 50,000) the error in the gain's being non-infinite is 1 part in 1,700. If the amplifier's input resistance is 0.6Mohm, the resulting error is 1 part in 21,000 for the system voltage gain, and the input resistor R_3 of 47 kilohms is shunted with a resistance of 1,026Mohm if the theory is to be believed. The amplifier may have typical output resistance of 100 ohm without feedback. The feedback

theoretically reduces the system output resistance to 0.06 ohms which in practice is swamped by the resistance of connecting leads.

Offset Voltage

What about the offset of the output voltage? If the operational amplifier has an input offset voltage of 1mV typically, this will produce a ±32.9mV offset in the output. If the input offset current is 20nA and the input bias current is 250nA this implies that the input bias current ranges between 240nA and 260nA. Using the expression previously derived, the maximum output voltage offset due to bias offset current is ±42mV giving a maximum offset of ±75mV. Tolerance of the resistors could increase this value. If a low resistance source were connected across R_3 without a DC blocking capacitor thereby making the effective resistance of R_3 small to bias current, the offset of the output due to bias current would increase to +360mV and the maximum offset to +393mV. This may be unacceptably large.

Frequency Response

The voltage gain of the basic operational amplifier without feedback falls by 3dB at a frequency of 100Hz say. With the designed system gain of 32.9 the expected frequency at which this gain has fallen by 3dB (that is to 23.3) is (56,234/32.9) x 100Hz = 17kHz (or 4MHz/32.9/122Hz if a gain bandwidth product of 4MHz is assumed).

The design method outlined is not critical. For a given gain, the ratio of R_1 and R_2 is set. For small offset at the output due to the bias current the resistance of R_1 should be reasonably small. The parallel combination of R_1 and R_2 is made roughly equal to the designed-for input resistance in the circuit. Small R_1 also reduces the effect of stray capacitance, the most significant probably being that across R_1 which produces a feedback signal. However the output of the amplifier feeds current into R_1 reducing the available current to the load. The value of R_1 should therefore not be too small. If the output voltage swing is ±10V from the supply of ±12V and the maximum output current is 4mA, then allowing no more than about 0.4mA to flow back into the feedback is reasonable and this makes $R_1 + R_2 =$ 10V/0.4mA = 25kilohms at a minimum. The other result of having R_1 too small is that either the offset may be larger than necessary or R_3 and therefore the input resistance is small.

The values derived for this design seem to be satisfactory.

Inverting Circuit

The circuit of Fig. 9 is used. Calculations give identical values to the non-inverting circuit when preferred resistor values are chosen. The theoretical gain of $-R_1/R_2 = -31.9$ for the nominal values. The offset, the frequency response and the output resistance are almost identical to the non-inverting example.

DESIGN FOR A UNITY VOLTAGE GAIN SYSTEMS WITH INPUT RESISTANCE OF 1 MEGOHM

When the system gain is reduced, the differences between the non-inverting and inverting circuits become more significant. The two unity gain circuits are shown in Fig.10.

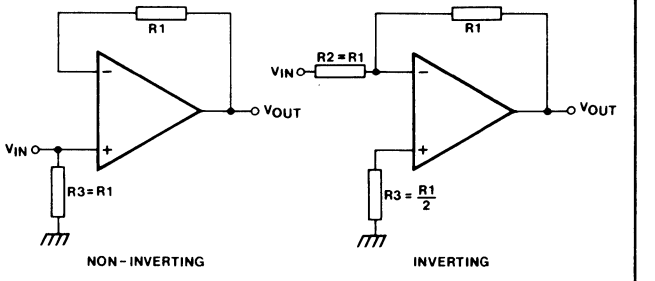


Fig.10 Unity gain amplifier

Non-Inverting Circuit

R_2 is effectively infinite so that $R_1 + R_2/R_2 = 1$, and R_1 can be zero ohms if the resulting increased output offset voltage due to input bias current in R_3 is of little importance. If not, R_1 is made equal to R_3. Assume an input resistance to the system of 1 Mohm is required, then $R_3 = 1$ Mohms. With an amplifier gain of 56,234 (95dB) the gain is unity less 1 part in 56,234. The effect on the system of the amplifier's differential input resistance of 0.6 Mohms is to shunt the 1 Mohm resistor with 33 Gohms if the theory is applicable at such an extreme value. If the amplifier has a gain bandwidth product of 4MHz, the frequency response is 3dB down at 4MHz. The theoretical output resistance is negligibly small at 0.18 mohms.

An input offset voltage of 1mV produces an output voltage offset of ±1mV. If $R_1 = R_3$ the offset corresponding to an input offset current of 20nA is 20mV giving a total maximum offset voltage at the output of ±21mV. Now if R_1 or R_3 is zero, the maximum bias current of 260nA produces a maximum offset of ±260mV at the output to which the ±1mV offset due to input offset voltage must be added.

The circuit is often used as an impedance buffer, for example in 'sample and hold' circuits. The voltage is sampled and stored as a voltage across a capacitor. This voltage is coupled by the unity non-inverting gain system (called a voltage follower) to an output where for example it can be digitised. The buffer circuit provides current to the digitising unit but ideally does not take current from the capacitor thereby discharging it and producing an error. The main problem in practice is having a high enough input resistance. This may be accomplished by omitting R_3, but then the input bias current must be supplied by the charged capacitor.

If the time between samples is too long for the resulting error to be acceptable, the bias current can be supplied by a separate current generator connected to the non-inverting input. The simplest circuit is that of a large resistor connected from the positive supply.

Inverting Circuit

For an input resistance of 1 Mohm, R_2 = 1 Mohm = R_1 for unity inverting gain. R_3 = 470 kilohms (npv) for low offset. The gain is unity to 1 part in 28,117 and the frequency response is half that of the non-inverting circuit at 2MHz. The output resistance is negligibly small. The output offset is ±2mV due to input offset voltage and due to the input offset current of 20nA is ±20mV. If R_3 is set to zero, the output voltage offset due to a bias current of 260nA is ±260mV.

The major difference in performance compared with the non-inverting circuit is the lower frequency response.

DESIGN OF A SYSTEM WITH GAIN OF 1000 AND AN INPUT RESISTANCE OF 47 KILOHMS

Referring to Fig.7 the required gain prescribes that the ratio of R_1 to R_2 should be 999 which if R_3 is to be 47 kilohms should give R_2 of much the same value for low offset. This would make R_1 about 47 Mohms which is not practicable. Set R_1 to 4.7Mohms and R_2 to 4.7kilohms (npv). The resulting gain is 1,001 and the 3dB frequency about 4kHz. The offset voltage at the output due to an input offset voltage of ±1mV is ±1V. An input bias current of 260nA produces an output voltage offset of about +10V to +11V. The design is not satisfactory.

Inverting Circuit

Referring to Fig. 9, R_2 is 47 kilohms to set the required input resistance and this makes R_1 the impracticable value of 47 Mohms. The design is not satisfactory.

There is a circuit modification which can overcome the problem of the large value for the feedback resistor R_1. It is shown in fig.11. Instead of the outputs being fed back directly, a potentially divided part of the output is fed back.

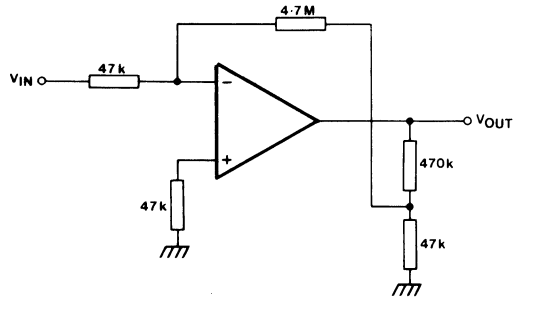


Fig.11 Reducing the value of feedback resistor

Set R_1 to 4.7 Mohms, then the potential divider gives one tenth of the output voltage for R_1 to have an effective value of 47 Mohms. Values could be 470 kilohms and 47 kilohms (npv). The offset due to the input offset voltage and current is unchanged from that of the basic circuits by this modification and will total about ±2V.

The modified design seems reasonable except for offset considerations and the frequency response of about 4kHz is rather low.

Cascading Two Stages of Gain 31.6

The design of these stages has already been made and there was little to choose between the performances of the non-inverting and inverting circuits. Use the previous design values. The overall frequency response will be 6dB down at about 171kHz with 3dB contribution from each amplifier. The overall frequency response is 3dB down at $171\sqrt{(\sqrt{2}-1)}$kHz = 110kHz, which is better than the single amplifier with gain 1,000. The only problem may be offset. The offset of the input stage is multiplied by the gain of the second stage and so the overall offset voltage may be a maximum of ±75mV x 32.9 ±75mV=±2.54V.This resulting offset is comparable to that of the single and amplifier system of gain 1,000 and may be acceptable.

Our conclusion is that cascading two compensated amplifiers each with a negative feedback gives better frequency response and comparable offset than using one compensated amplifier alone to get the same gain. It may not be the correct conclusion were we able to select the compensation required for the amplifiers.

Reduction of Offset Voltage

The examples show that the output offset voltage may be a nuisance. Offset is temperature sensitive so it is possible to compensate for it completely only at one temperature. If the amplifier has no provision for offset adjustment, the earth connection to R_2 or R_3 for the non-inverting and inverting systems respectively, may be connected to a source of voltage from the slider of a potentiometer connected

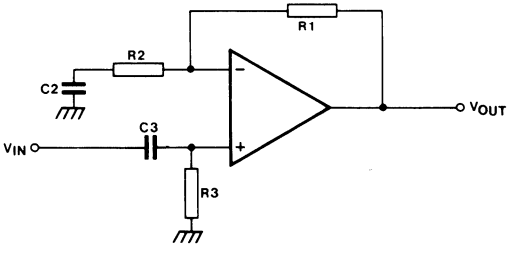


Fig.12 AC coupled amplifiers

between the supply lines. The potentiometer is only required to vary the voltage to the amplifier by a few mV and can be adjusted to give zero output voltage for zero input voltage.

Systems which are not required to work down to very low frequencies, for example audio systems, may be AC coupled. This reduces the offset of each stage and eliminates the problem of the offset of input stages having their offset multiplied by the gains of the following stages. Fig.12 shows such a system where offset is drastically reduced for the price of two capacitors.

Take the gain of 30 and input resistance of 47 kilohms as before. R_3 = 47 kilohms = R_1 for low offset due to input bias current. At moderate frequency, the reactance of C_2 is negligibly small compared with the resistance of R_2 and the system gain is

$$\frac{R_1 + R_2}{R_2} \quad \text{----------} \quad (23)$$

This gives R_2 a value of 1.6 kilohms (or 1.5 kilohms npv) and a gain of 32.3. To offset current, the system is that of a voltage follower and using the previous values the offset is $\pm$1mV$\pm$20nAx47 kilohm = $\pm$2mV. C_3 blocks the offset of the preceding stage from affecting the output, but omitting it and cascading two stages will give small offset.

To calculate the value for the capacitors, assume the system gain falls by 3dB at 20Hz as the frequency is reduced from medium frequencies. C_2 will turn out to be the larger of the two capacitors and we will select this to set the response. For the 3dB frequency to be 20Hz, C_2 should be at least

$$\frac{1}{2\pi \times 20 \times 1.5 \times 10^3} \quad F \simeq 5\mu F(npv) \text{---} (24)$$

Let the effect of C_3 come in at the lower frequency of 5Hz where the gain has already dropped off due to C_2

$$C_3 = \frac{1}{2\pi \times 5 \times 4700} = 0.68\mu F \text{ (npv)} \quad (25)$$

The design will have the upper 3dB frequency at about 170kHz as before. The design of the inverting system is similar. The input signal is fed through a capacitor to R_2 but there is no need for another capacitor. R_2 is 47 kilohms, R_1 is 1.5 Mohms, R_3 is 1.5 Mohms for low offset. C_2 can be 0.17 μF or the nearest larger preferred value for a 3dB frequency of 20Hz. because R_1 is larger than in the non-inverting case the offset is larger at $\pm$1mV$\pm$20nA x 1.5 Mohms = $\pm$31mV. The value is sufficiently small not to cause much of a problem.

APPLICATIONS

Variable Gain Amplifiers

If R_1 or R_2 can be made voltage variable resistors, the system gain may be voltage controlled. Audio range compressors are one such application and a gate voltage controlled FET is often used to adjust the effective value of R_2.

Mixer Amplifiers — Differential Amplifier

It is sometimes required to add, subtract or mix signals. The general circuit is shown in Fig.13. The gain analysis is quite easy if the amplifier is considered to be ideal. Ignore initially the dotted inputs shown in the diagram and consider only the inputs V_4, V_5 and V'_4.

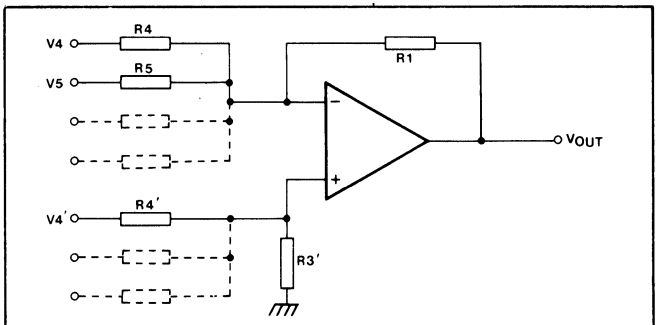


Fig.13 Mixer amplifier

The system has two inputs connected to the inverting input through resistors and one connected to the non-inverting input through a resistor. The voltage at the non-inverting input is

$$\frac{V'_4 R'_3}{R'_3 + R'_4} \quad \text{---------} \quad (26)$$

and this is the voltage at the inverting input for an infinite gain amplifier. Summing the currents to zero at the inverting input, the expression for the output voltage is

$$V_{out} = -V_4 \frac{R_1}{R_4} - V_5 \frac{R_1}{R_5} + V'_4 \frac{R'_3 R_1 \left(\frac{1}{R_4} + \frac{1}{R_5} + \frac{1}{R_1}\right)}{(R'_3 + R'_4)} \quad (27)$$

More complicated systems are dealt with similarly. By selecting the relative values of the resistors to which the voltages are applied the output can be any sum and difference of the input voltages. There is one drawback to the circuit. For inputs connected to the non-inverting side, the presence of R'_3 will result in signals appearing on the other input sources by potential divider action. The negative feedback makes the effective resistance to earth at the inverting input small and therefore little interaction

results between inputs connected to it. It may therefore be of advantage to sum or mix using only the inverting side and use a unity gain inverting amplifier to invert inputs like V'_4 which would be connected to the non-inverting side. The calculations are easier too!

If offsets and frequency responses are to be predicted, the effective values for R_2 and R_3 are obtained at DC and moderate frequencies respectively and are put into the appropriate expressions much as in the previous examples.

In instrumentation applications, the circuit could be used as a differential or difference circuit with single inputs connected to each side. For output voltage of K times the input voltage difference, $R_4 = R'_4 = R$, $R_1 = R'_3 = KR$. Accuracy is a function of the accuracy of resistor matching and also the common mode gain. Unfortunately, the input resistances in practice are often too low.

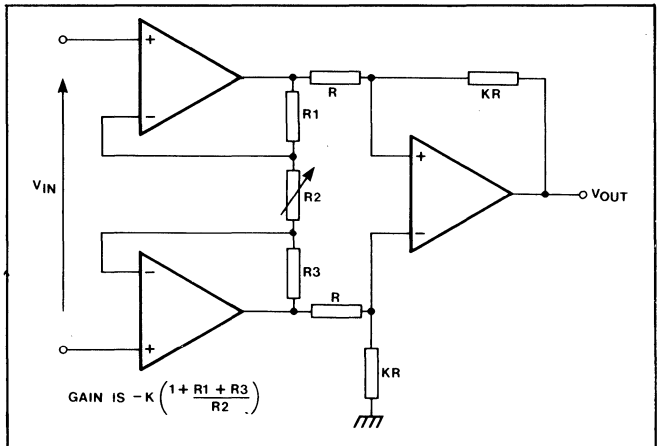


Fig.14 Instrumentation difference amplifier

To overcome the problems, a three amplifier circuit can be used as in Fig.14. The two input amplifiers are voltage followers which have good common mode behaviour and high input resistance. R_2 can set the gain of the input stages. This reduces the gain required of the output stage and improves its common mode performance.

Systems of Tailored Frequency Response

The design of systems for a required shape of frequency response is filter design. Operational amplifiers are often used in so-called active filters which are principally designed as filters avoiding the need for inductors. In general, a particular circuit configuration is investigated and the types and values of the components found, but the subject is too large to consider any more than one example. The record replay equaliser for magnetic pick-ups is one such application. The response is to fall from 50Hz at 6dB per octave,

flatten at 500Hz and start to fall again at 6dB per octave from 2.1kHz. The gain at 1kHz should be about 30 to bring the expected input level of 5mV to other possible amplifier inputs. (This specification comes from curve fitting of the replay characteristic.) The transfer function (the ratio of output to input) is

$$\frac{k(1 + jf/f_2)}{(1 + jf/f_1)(1 + jf/f_3)} \quad \text{--------} \quad (28)$$

where k is a constant, f is the frequency under consideration, $f_1 = 50Hz$, $f_2 = 500Hz$ and $f_3 = 2.1kHz$.

The next move is to find a suitable circuit. That shown in Fig. 3.8. is a possibility.

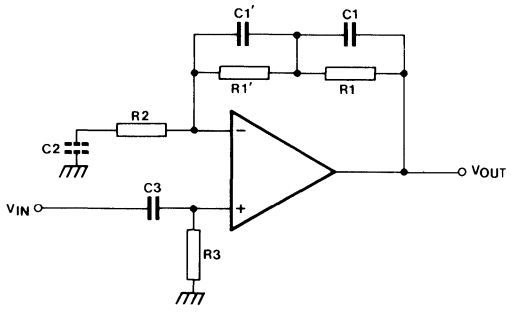


Fig.15 Magnetic pickup preamplifier

Using the general expression for the non-inverting gain configuration, the gain is $1 + (Z_1/R_2)$. For the circuit shown it works out to be

$$\left[\frac{R_1 + R'_1 + R_2}{R_2}\right] \times$$

$$\left[\frac{1 + \dfrac{j2\pi f(R_1C_1R'_1 + R'_1C'_1R_1 + R_1C_1R_2 + R'_1C'_1R_2)}{R_1 + R'_1 + R_2} + \dfrac{(j2\pi f)^2R_1C_1R'_1C'_1R_2}{R_1 + R'_1 + R_2}}{(1 + 2\pi fC_1R_1)(1 + 2\pi fC_2R_2)}\right] \quad (29)$$

If the j^2 term has negligible effect, the circuit will give the required response. The gain at 1kHz is to be 30, so extrapolating back to frequencies below 50Hz, the gain should be 300. Therefore

$$\frac{R_1+R'_1R_2}{R_2} = 300 \quad \text{--------} \quad (30)$$

$$\frac{1}{2\pi C_1 R_1} = 50\text{Hz} \quad \text{--------} \quad (31)$$

$$\frac{1}{2\pi C'_1 R'_1} = 2.1\text{kHz} \quad \text{---------} \quad (32)$$

$$\frac{1}{\dfrac{2\pi (R_1C_1R'_1+R'_1C'_1R_1+R_1C_1R_2+R'_1C'_1R_2)}{R_1 + R'_1 + R_2}} = 500\ \text{Hz} \quad (33)$$

To simplify the calculations, as the gain expression suggests that R_2 is small, ignore the terms involving R_2 in the frequency equations. This gives $R_1 = 11.8R'_1$ and from the gain expression, $R_1 = 278R_2$. Put a capacitor in series with R_2 to give a roll-off of response at frequencies below 20Hz, then to minimise offset let $R_1 = R_3 = 47$kilohms. Therefore $R'_1 = 3.9$kilohms and $R_2 = 180$ohms, $C_1 = 0.068\mu$F and $C'_1 = 0.022\mu$F (npv). To get the 20Hz roll-off, C_2 is at least 53μF. For C_3 to have small effect on the response, its value should be about 1μF.

Offsets are likely to low from the experience gained by the previous examples and although C_1 and C'_1 are large, at the small audio frequency output voltages we expect no difficulties due to slew rate.

The Inverting Integrator or Charge Amplifier

This commonly used circuit is shown in Fig.16.

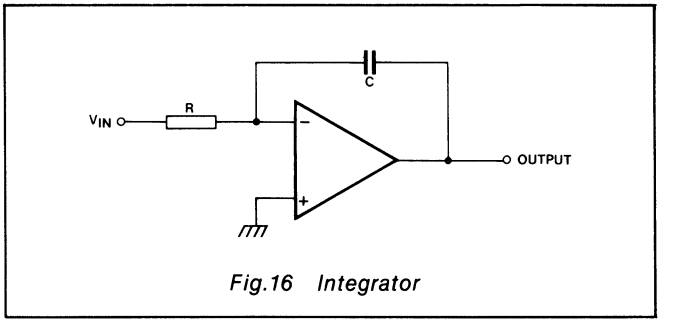


Fig.16 Integrator

The operation of the circuit is as follows. If the amplifier is ideal, the voltage at the inverting terminal is zero and no current flows into the input of the amplifier. The current flowing in R is V_{in}/R and must flow into the right hand plate of the capacitor C. The same amount of current must flow from the right hand plate and this represents the capacitor's

charging with its right hand plate and therefore the output voltage of the amplifier going negative.

The expression for the voltage across a capacitor is

$$\frac{\text{Charge}}{\text{Capacitance}} = \frac{\text{Current time integral}}{\text{Capacitance}}$$

Let R = 100 kilohms and C = 1nF. If a +1V step of voltage is suddenly applied for 1ms when the output voltage is zero, the output will start falling linearly to −10V in 1ms. If the input voltage is suddenly changed to −1V for 2ms the output will rise linearly with time from −10V to +10V. If the input voltage is then reduced to zero the output voltage should remain at + 10V and the capacitor retain its charge.

With this circuit, a square wave input should give a triangular wave output unless limited by amplifier saturation.

There are inaccuracies however. Bias current must flow. This means that the current through the resistor is not quite equal to that through the capacitor. Offset voltage will produce errors as will the finite gain of the amplifier. The errors exhibit themselves as 'drift' where the output will change even if the input voltage is zero. Supplying the bias current from an external source such as a large resistor connected to the power supply and providing a small voltage from a potential divider connected between the supply lines and feeding the non-inverting input to compensate for offset can be tried but as the effects are temperature sensitive, such solutions are not wholly stisfactory. An amplifier with an FET input stage will reduce the problem due to input bias current but that due to offset voltage may well be worse. Probably the best solution is to clamp the output until it is required to change. In repetitive systems, the system design is usually satisfactory provided the time scale is below 1 sec.

Design of precision integrators is difficult.

Voltage to Voltage Converters — Constant Voltage Sources

For constant voltage sources it should be obvious that the basic non-inverting or inverting feedback amplifier with a reference voltage input will give an output voltage of the resistor ratio times the reference. For larger current, constant voltage sources or regulated voltage supplies, an emitter follower circuit can be used as in Fig. 17.

Voltage to Current Converters — Constant Current Sources

Occasionally constant current sources are needed, for example some transducers need to be supplied with constant current.

The constant current sources work similarly to the constant voltage system in that they maintain the voltage across a fixed resistor constant and therefore its current is maintained constant. Fig. 18 shows two such circuits.

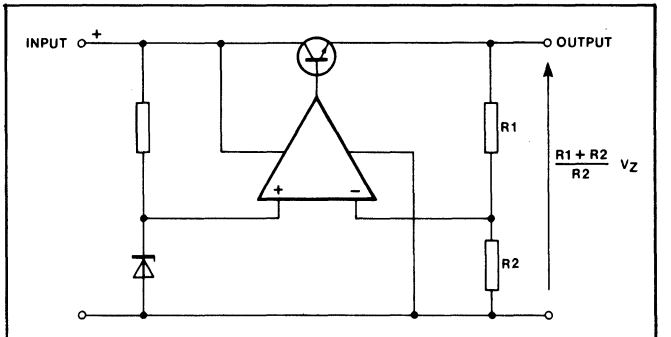


Fig.17 Constant voltage source

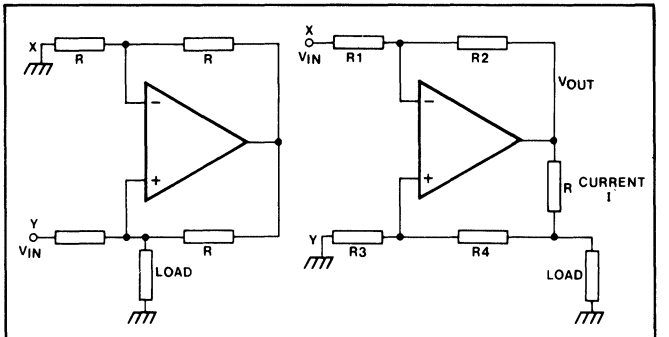


Fig.18 Constant current sources

The first circuit is the less useful but is very easily analysed for equal resistors. The voltage across the load is $V_{out}/2$ and the load current is the sum of that from V_{in} and V_{out} and works out to be V_{in}/R.

The second circuit uses much less source current. The voltage at the non-inverting input is

$$(V_{out} - IR)\left(\frac{R_3}{R_3 + R_4}\right) \text{ -------- (34)}$$

and this is roughly equal to that at the inverting terminal. Summing the currents at the inverting input to zero and if the ratios

$$\frac{R_3}{R_3 + R_4} = \frac{R_1}{R_1 + R_2} \text{ --------- (35)}$$

(which is a balanced bridge condition) then

$$I = \frac{-V_{in}R_2}{RR_1} \text{ ---------- (36)}$$

Imbalance in the resistance ratio can make the current either fall or rise slightly as the load resistance changes.

Note that points X and Y can be earthed or fed by the source depending upon whether inversion or non-inversion of polarities is wanted.

Current to Voltage Converters

Some transducers give out a current which is a function of the variable which is being measured. It is easy to convert this into a proportional voltage, since Fig.8 is in effect that of a current to voltage converter. Current I through R_2 gives an output voltage of $-R_1 I$. The simplest converter merely replaces R_2 by the current source. If the output is to be offset or if bias currents produce a problem, a current from a large resistor connected to the supply and also feeding the inverting input may be added.

4. Regenerative switches

Section 2 discussed the use of an operational amplifier as a comparator. In some applications where the input voltage fluctuates slightly each side of the reference voltage, the resulting fluctuating output may be undesirable e.g. controlling a relay. Also there are applications where a signal output change is required only if an input strays outside set limits. Such a circuit will exhibit 'hysteresis' or 'backlash' that is when the input voltage rises above some set threshold, the output goes positive say, but the input must be reduced considerably before the output voltage is restored to its original less positive state.

For the dual power supply system, the characteristics are shown below in Fig. 19 for non-inverting and inverting systems triggered at voltages each side of zero. It can be arranged that the two triggering levels are of the same polarity.

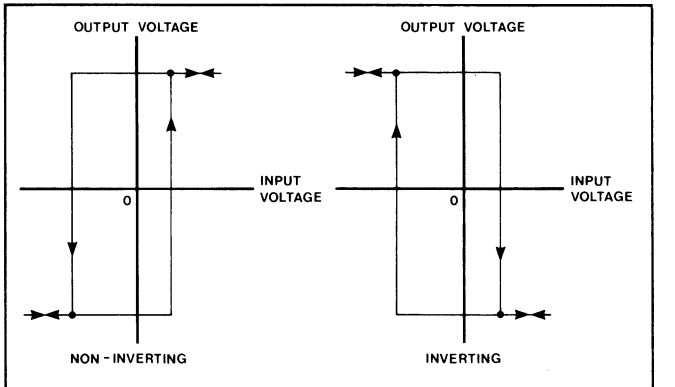


Fig.19 Regenerative switch characteristics

The mechanism which can produce such characteristics is positive feedback. Suitable circuits are shown in Fig.20. These circuits are called Schmitt Trigger Circuits.

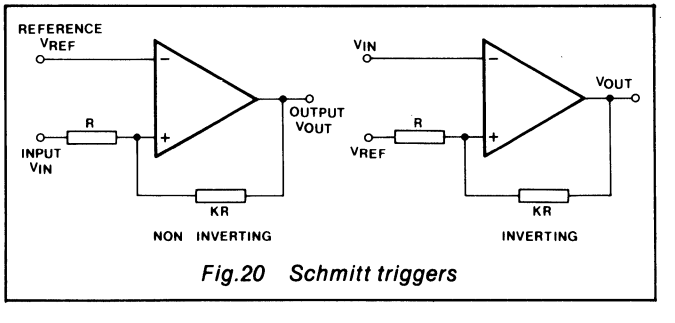


Fig.20 Schmitt triggers

Consider the operation of the non-inverting circuit. Let the reference voltage V_{ref} be positive and the output voltage be at the maximum negative $-V_N$. The voltage V at the non-inverting input for no input current to the amplifier is

$$V = \frac{-V_N}{K+1} + \frac{K}{K+1} \cdot V_{in} \quad \text{--------(37)}$$

If V_{in} increases so does V until, once it becomes slightly larger than V_{ref}, there is a small positive voltage between the non-inverting and the inverting input terminals. The output voltage changes by this voltage multiplied by the amplifier's difference gain in a positive direction. Through KR, V increases and further increases the difference voltage and therefore the amplifier's output voltage. This positive feedback around the feedback loop causes a regenerative action only halted by the output voltage of the amplifier reaching its maximum positive value V_P and occurs in a very short time after the start of the action. The voltage at the non-inverting input is then

$$\frac{KV_{in}}{K+1} + \frac{V_P}{K+1} \quad \text{---------- (38)}$$

which is more positive than the input voltage and so the system stays in that output condition unless the input voltage is reduced sufficiently that a net small negative voltage is produced between the non-inverting and inverting input terminals. The output voltage falls rapidly to $-V_N$ by regenerative action.

Triggering occurs at the two levels at which the voltage at the non-inverting input terminal reaches V_{ref}. In general the trigger levels are given by

$$V_{in} = \frac{-V_{out}}{K} + V_{ref}\,\frac{K+1}{K} \quad \text{------ (39)}$$

Example Design a trigger circuit for triggering levels of +3V and +1V using a dual supply system and where the output voltage of the amplifier can range between ±10V from ±12V supplies.
The two equations are

$$3 = \frac{+10}{K} + V_{ref}\,\frac{K+1}{K} \quad \text{--------(40)}$$

$$\text{and } 1 = \frac{-10}{K} + V_{ref}\,\frac{K+1}{K} \quad \text{------ (41)}$$

Subtracting gives K = 10 and then V_{ref} = 1.8V. For not too much current from the output of the amplifier and the input source, let R = 10 kilohms and KR = 100 kilohms.

For the non-inverting circuit the action of the circuit and the design is similar. The switching levels are given by

$$V_{in} = \frac{V_{out}}{K+1} + \frac{K}{K+1} V_{ref} \quad -------$$

so for the previous design specification, K = 9 and with R = 10 kilohms and KR = 90 kilohms, V_{ref} = 2.2V.

To obtain the reference supply, a potential divider from the supply voltages may be used. The current through the potential divider should be many times that of the maximum input current to the amplifier. If the switching levels are symmetrical, no reference voltage is required and the reference is connected to the common earth of the supplies.

An alternative method of obtaining asymmetric switching levels either side of zero is to make KR a resistor in parallel with a series resistor diode circuit. In the voltage condition in which the diode is conducting, the effective value of KR is reduced. However, accurate design may be complicated by the forward voltage drop of the conducting diode. If the switching levels are both of the same polarity, the single voltage supply system may be used.

There is a major drawback of using the operational amplifier in these trigger circuits. The slew rate of the amplifier sets the switching speed irrespective of the input conditions as these circuits operate on the input voltage threshold. For a slew rate of 1.5V/μs, the 20V transistion will take 13.3μs. which may be too slow for some applications. Since the slew rate is mainly set by the compensating capacitor, either an uncompensated amplifier or a special purpose-designed comparator must be used for increased operating speeds.

Uses of the Trigger Circuits

1 The basic circuit can be used to detect when a particular voltage level is reached and in this form is made in integrated muilti-circuit packs. It ensures that in logic systems a signal must be higher than a particular level to be accepted as logic 1 and lower than another level to be accepted as logic 0. For alarm systems, the basic circuit used to indicate when a danger level has been exceeded and then ensure that before being reset, the level is drastically reduced well below the danger level.

2 If fed with a voltage ramp the circuit will trigger when the output voltage reaches the designed-for level. If this level is adjustable, an output signal can be produced at a controllable time after the start of the ramp. This adjustable delay may be useful.

3 In conjunction with a resistor capacitor combination, the circuit may be made into a multivibrator square wave generator. In Fig.21, as the output switches, current flows

through R′ charging or discharging C. This controls the time taken for the voltage at the inverting input terminal to change between $\pm V_{OUT}/K + 1$ and cause switching. The idealised waveforms are shown in Fig.22 and the expression for the frequency works out to be

$$\frac{1}{2CR \log_e \frac{2+K}{K}} \quad \text{for } V_N = V_P. \text{ ------ (43)}$$

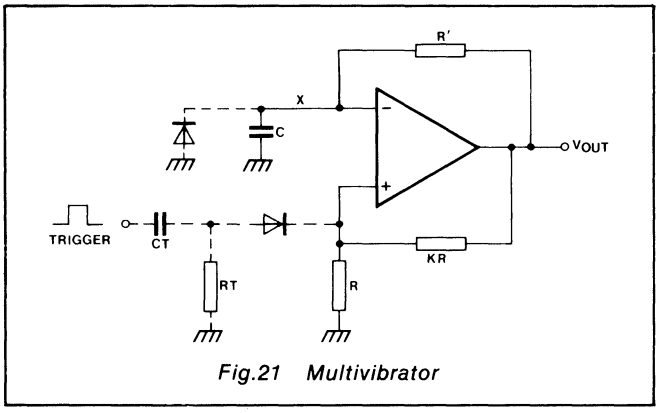


Fig.21 Multivibrator

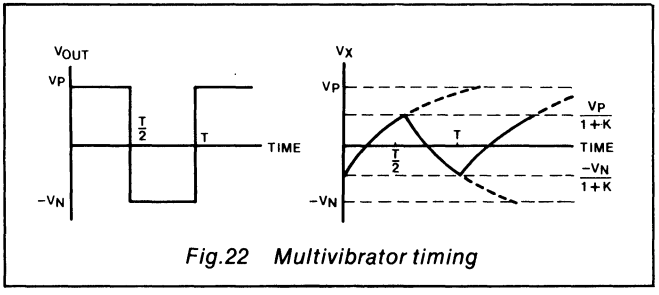


Fig.22 Multivibrator timing

Example Design the multivibrator of Fig.21 for a frequency of 1kHz. The period of 1ms is large compared with the slew rate. From the waveforms we deduce that the charge and discharge curves should be steep at the crossover so that small voltage errors do not affect the period significantly. Let K = 1 and R + 10kilohms. Now $\log_e 3 = 1.1$ and so CR′ = 0.4545ms. If C = 10nF, R′ = 45.45kilohms or 47kilohms (nearest preferred value).

For a circuit which gives an output pulse for a triggering input pulse (i.e.) to a monostable circuit, the basic circuit needs to be modified so that its free running action is halted and then started for one period by the incoming pulse. A diode connected across C will hold the non-inverting input

terminal within 0.65V of earth. Assume we wish for a 0.5ms positive going pulse output. Under no pulse conditions, the output is negative and so is the voltage at the non-inverting input terminal. To remain in this state, the voltage at the inverting terminal must be more positive and the diode must stop that voltage from dropping below −0.65V but provide the current flowing through R'. No current is required from C. A trigger pulse can be applied to the non-inverting input terminal and, if large enough to raise its voltage above −0.65V, will cause the circuit to trigger for a time set by the R'C combination. To make sure that only the positive edge of the pulse gives the transition, a differentiating circuit and diode is used. The connections are shown dotted in Fig. 21.

The values previously derived will give a 0.5ms pulse going from −10V to +10V and for these values the input pulse should be at least 5V for the circuit to be switched. Typical values for C_TR_T would be $R_T = 10$ kilohms and the CR product 0.1 of the input pulse length. If this is 10μs, $C_T =$ 100pF which is larger than the stray capacitance and the reverse biased diode capacitance and should therefore be satisfactory. If not, its value can be increased and R_T's value decreased proportionally. The trigger source impedance needs to be considered if R_T becomes too small.

4 Another circuit for a square wave generator is shown in Fig. 23 and has the added advantage of producing a triangular waveform. It uses the inverting integrator described in section 3 and the non-inverting trigger. The circuit operation is straightforward. Let the ouput of the trigger circuit be positive V_P. Current of V_P/R' flows through R' and into the capacitor C and therefore the output of the integrator goes negative linearly with the constant current charging of C. When the output voltage has fallen sufficiently, the trigger circuit operates and its output voltage falls to $-V_N$. Current of $-V_N/R'$ flows through R' from C which as a result makes the output voltage of the integrator rise. When it rises high enough the trigger operates and the cycle is repeated. The trigger levels are V_P/K and V_N/K and the time taken for the capacitor to charge or discharge through this voltage is therefore

$$\frac{V_P + V_N}{KC} \quad \text{----------} \quad (44)$$

divided by the charging current. For simplicity assume that $V_P = V_N$ then the total cycle period is $4/KCR'$.

Example Design as before for a frequency of 1kHz. For linear operation, the excursion of the triangular wave must

be limited well within V_P and $-V_N$, let it be halfway. This gives K = 2 and with R = 10kilohms, KR = 20kilohms. CR′ = 0.5ms, so with R′ = 10kilohms, C= 50nF.

The problem of increasing the frequency is mainly the slew rate limitation which slows up the edges of the square wave, puts a flat on the peaks of the triangular wave and increases the period over that designed for.

Reducing the frequency is limited by the maximum value of R′ set by the errors produced by input bias current and the size, cost and current leakage of C.

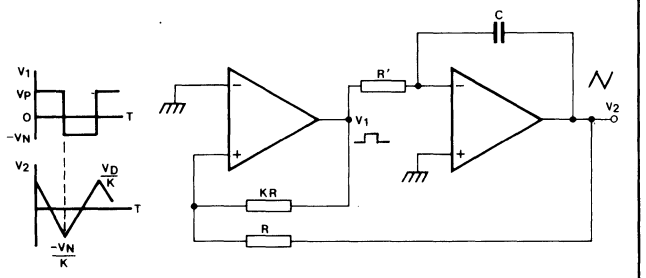


Fig.23 Square and triangular waveform generator

5 A sawtooth generator can be produced by combining the trigger and integrator circuits but some means has to be found for increasing the discharge current demanded by the capacitor in the fast voltage change region. For example, to discharge a 50nF capacitor 10v in 1μs requires an average current of 0.5A. A Transistor used as a switch connected across the integrator capacitor and controlled by the trigger circuit is the best solution but the design can be tricky.

Some designers use a four diode bridge circuit current fed and controlled by the trigger circuit to switch current into and out of the integrator's resistor. In general the complication and expense are not justified but for some applications it allows the current through the integrator's resistor to be controlled and changes the effective value of the resistor and therefore the frequency of operation.

5. Miscellaneous applications

Sections 2, 3 and 4 cover the main uses of operational amplifiers but there are a large number of other applications most of which are variations of the basic circuits already discussed.

Non Linear Negative Feedback Systems

The negative feedback circuits set the gain of the system in terms of the input and feedback impedances. If one of these impedances is made non-linear, the characteristics of the circuit are modified. The simplest application is for bounding the output voltage of the amplifier or the comparator by having the feedback element a diode or a Zener diode. Fig.24 shows a system where the output voltage is held at the operating voltage of the double Zener diode and gives the characteristics shown. The design should ensure that the diodes have enough current to operate them in the constant voltage region and this is a function of the current through R_2.

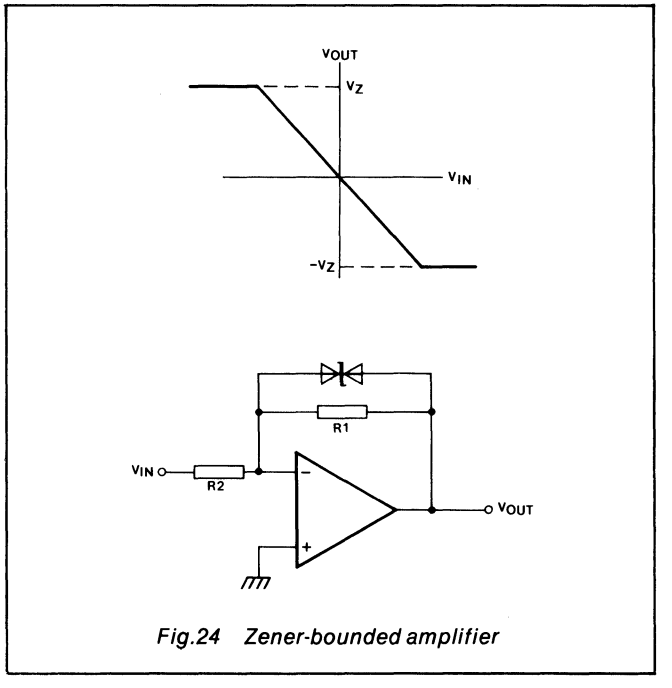


Fig.24 Zener-bounded amplifier

The same technique will produce the circuit of the so called 'precision rectifier', the circuit of which is shown in Fig. 25.

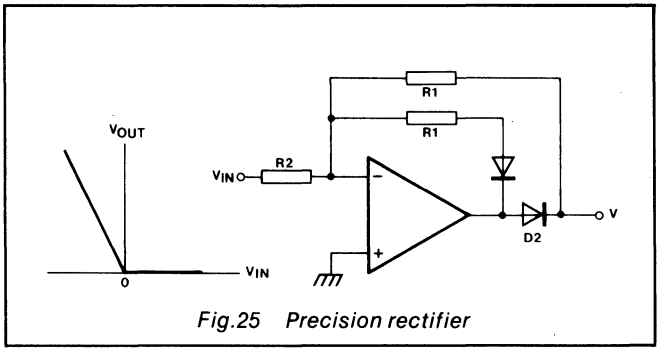


Fig.25 Precision rectifier

The circuit is a half wave one with the diodes connected to give a positive output voltage with a negative input voltage. With a negative input voltage the output of the amplifier goes positive, diode D_2 conducts and by summing currents at the inverting input, the voltage V is $-V_{in}\,(R_1/R_2)$. With a positive input voltage, the output of the amplifier goes negative, D_1 conducts to absorb the current of R_1 and the output V is zero. The major problem of the circuit is that the amplifier slew rate limits the accuracy of operation. To convert to full wave operation, the output of the half wave circuit is fed into a summer-inverter circuit such as that of Section 3 and added to the non-inverted input. If the scaling is such that the rectified signal is twice as effective as the original input, a full wave rectified output is obtained.

To make a peak detector, all that is necessary is for a capacitor to be connected across the output. In conjunction with the resistance of the load it will set the time of recovery between peaks. It is usual to add a small resistor in series with D_2 to limit the peak current required from the amplifier. The decay time constant is C·(R_1 in parallel with the load R_L).

Another application is the logarithmic amplifier which gives out a voltage proportional to the logarithm of its input voltage. The principle is that a current through a diode or transistor is related to the voltage across it by the expression $i = I_0(e^{AV} - 1)$ which approximates to $i = I_0 e^{AV}$.
Rearranging the expression becomes $V = 1/A\ (\log i - \log I_0)$. If the diode or transistor replaces R_1 in the inverting amplifier circuit then as

$$i = I_{R2} = \frac{V_{in}}{R_2}, \quad -V_{out} = \frac{1}{A}\left(\log \frac{V_{in}}{R_2} - \log I_O\right) \simeq B \log kV_{in} \quad (45)$$

In practice, operation over several decades of current and over a range of temperature makes accurate design difficult and it may be advisable to buy a ready made unit. The anti-logarithm system uses the diode in place of R_2 but this application is rarer.

A further application is for sinusoidal oscillators. The problem with designing oscillators is that for the oscillations to start up, the gain around the feedback loop must be greater than 1 but when the oscillations have built up sufficiently, the gain around the loop must be limited to 1 for stable operation. At the oscillation frequency, the phase shift is effectively zero so that the system feeds itself in magnitude and phase. The limiting must be done by non-linearity which could also result in the outputs being distorted. The Wien bridge oscillator shown in Fig.26 has a frequency set by $1/2\pi CR$ from the phase shift criterion and requires an amplifier gain of 3 from the loop gain criterion. An operational amplifier with negative feedback can give this gain but also results in the amplifier's being a very linear system. The amplitude of oscillations is therefore limited by the amplifier saturating at positive and negative peaks giving a peak clipped output. The usual suggestion to overcome this difficulty is to make $R_2 > 2R_1$ and shunt R_2 with an FET acting as a non-linear resistance controlled by the peak detected output voltage. This is easier said than done in practice and it may be easier to replace R_1 by a thermistor. As the output voltage rises, the current in the thermistor increases and its resistance decreases. This lowers the amplifier gain and stabilises the output signal at a value which avoids peak clipping.

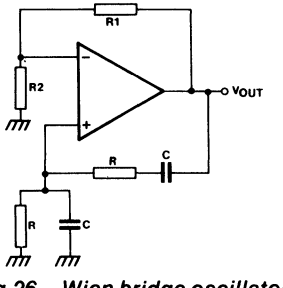


Fig.26 Wien bridge oscillator

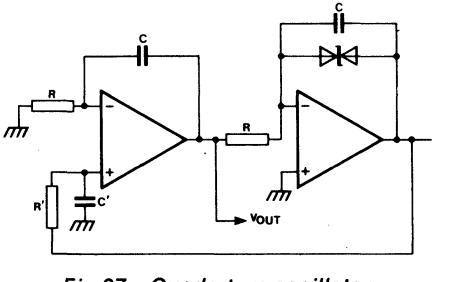


Fig.27 Quadrature oscillator

The oscillator system shown in Fig.27 is called a quadrature oscillator' and uses two integrator type circuits. To limit the amplitude, the Zener diode limiter is used. Typically the diodes would operate at ±5V for amplifiers which would limit at ±10V. The frequency is $1/2\pi RC$ and RC is made equal to R'C' with R' a little larger than R to start the oscillation. An alternative three amplifier configuration cascades two inverting integrators with a unity gain inverting amplifier and has the advantage of using one less capacitor for the price of the extra amplifier. The loop filters out the distortion to some extent.

For these oscillator circuits,the maximum operating frequency is set by the output required and the slew rate. For a slew rate of 1.5V/μs, an output of 5V peak only can be obtained up to a frequency of 48kHz (See Section 1). For operation at this frequency, R = 10 kilohms, C = 330pF.

Switched Systems

The units of Sections 2 and 4 can be incorporated into more complicated systems. For example the triangular wave generator of Fig.23 fed into a comparator whose reference voltage is varied can give a pulse width modulator. The integrator fed with a series of short pulses will give an output stepped like a staircase and the time for an integrator's output to change between two voltage levels as detected by a comparator is inversely proportional to the input voltage. These circuits may be used in a voltage to frequency converter, a voltage to time converter and so for an analogue to digital converter.

The property which has not been discussed is the programmability except for setting up the amplifier's operating current. It is often possible with programmable amplifiers to switch them on and off using the programming input terminal. If so, the unit may be used to sample a signal for a 'sample and hold' circuit, be used as a pulse amplitude modulator or as a controlled channel in multi-amplifier systems.

4. SL650/51 Applications

Circuit Data

The circuits consist of a voltage controlled oscillator (VCO) of exceptional stability, with internal logic to enable selection of one of four preset frequencies, and a phase comparator with current-controlled gain and a high gain limiting amplifier at its signal input. The SL650 also has a separate auxiliary amplifier with a CCITT-compatible output. The auxiliary amplifier is intended for use as a limiting amplifier or a comparator and has an open-loop gain of 60dB but may also be used in closed loop applications with gains of 20dB or more. A block diagram of the SL650 is given in Fig 1; the SL651 has no auxiliary amplifier but is in other respects identical to the SL650. Throughout the rest of this application note only the SL650 will be referred to, although all applications not requiring the auxiliary amplifier may equally well be accomplished with the SL651.

The circuit diagram of the SL650 is shown in Fig 2. Transistors TR1 to TR22 form the VCO, TR23 to TR33 and TR78 the current switching logic in the frequency selection system, TR34 to TR60 the phase comparator and TR61 to TR77 (which are not present in the SL651) form the auxiliary amplifier.

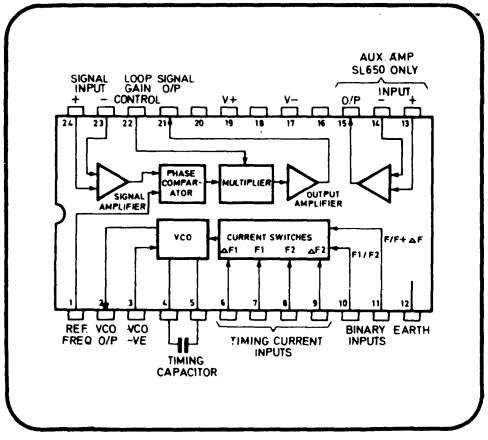


Fig. 1 Block diagram of SL650/SL651.

THE POWER SUPPLY

The SL650 requires both positive and negative supplies, (normally ±5V) connected to Pins 19 and 17 respectively. The centre earth is connected to Pin 12. The circuit will operate from supplies between ±3.5V and ±7.5V. Although the positive and negative supplies are usually equal the positive rail may have a higher voltage than the negative rail, but not vice versa.

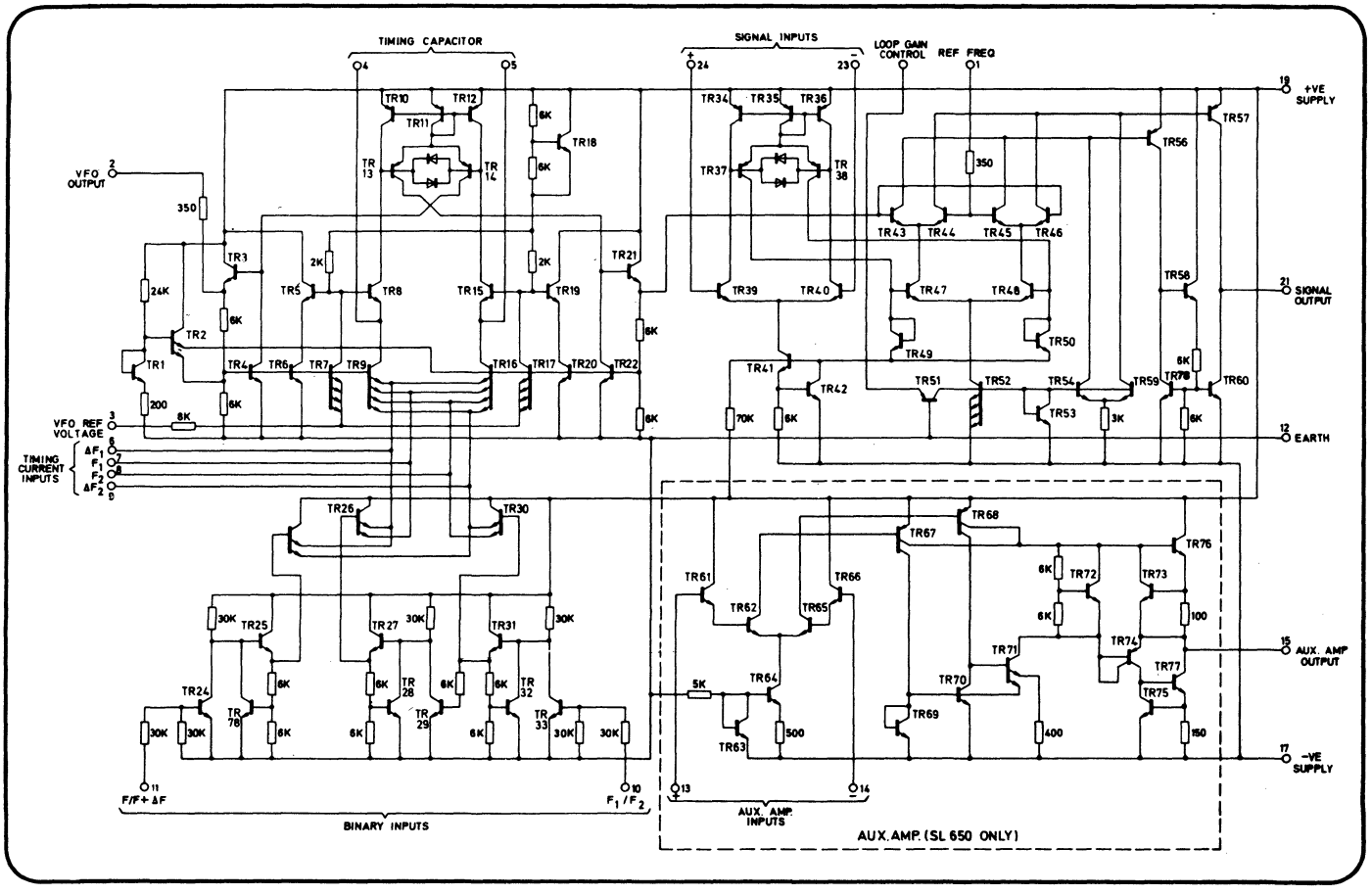


Fig. 2 Circuit diagram of SL650/SL651.

The supplies should be reasonably free from ripple and stable under load but they do not, in most cases, need to be stabilised against external supply variations. The current consumption is about 1.5mA off load between the positive and negative rails. In this application note supply voltages of ±5V are assumed unless otherwise stated.

THE VOLTAGE CONTROLLED OSCILLATOR

The voltage controlled oscillator – also referred to as the variable frequency oscillator (VFO) – is exceptionally accurate. Typically, its frequency is within 2% of its design equation, its mark-space ratio within 1% and its temperature coefficient less than ±20 ppm/°C at 200μA timing current. The oscillator in the SL650B always has a temperature coefficient less than ±20 ppm/°C at this current.

Although the VCO is conservatively specified to work over a 100:1 range of timing current (20μA to 2mA), a 250:1 range of timing current with better than 2% linearity of current/frequency over most of the range can nearly always be attained. To achieve maximum timing range the positive supply should be greater than the negative supply. The VCO frequency variation with power supply is typically ±20 ppm/%.

Unlike most integrated circuit VCOs, the SL650 VCO uses current threshold sensing rather than voltage threshold sensing. This means that FM noise in the output is much lower than in a comparable oscillator using voltage threshold sensing. Hence, an SL650 used as an FM transmitter gives a cleaner signal and used as phase-locked FM detector gives a better signal-to-noise ratio. Such a low level of jitter is very difficult to measure accurately and at present no absolute measurements exist although we hope to be able to specify jitter on future editions of the data sheet. It is safe to say, however, that the jitter of the SL650 is some 15 to 20 times less than that of other manufacturers' similar phase-locked loop circuits using voltage threshold sensing.

This low jitter and temperature drift must be paid for. The circuits which are used to achieve such high performance use PNP transistors with quite low f_t, limiting the maximum frequency of oscillation to about 500kHz. The circuit should not, therefore, be used in high stability applications at frequencies much over 50-100kHz, although it will work at frequencies as low as 1/10Hz.

The simplest oscillator circuit using the SL650 consists of a timing capacitor connected between pins 4 and 5 and a single timing resistor connected from pin 7 to the negative supply (pin 3). The voltage on pin 7 is within a few millivolts of the centre rail so the timing current is accurately defined by this resistor and the negative supply voltage. The frequency of this oscillator is 1/CR to within about 2%. To minimise df/dT the timing current should be between 75 and 400μA and the capacitor should exceed 1000pF. Capacitors as small as 100pF may be used, at frequencies up to 500kHz or sometimes a little higher, but frequency stability is reduced above 150kHz. The graph in Fig 3 demonstrates the excellent frequency stability possible at medium frequencies.

To achieve high frequency stability it is necessary to choose the timing components with great care. There is little point in using an integrated circuit with a temperature coefficient of under 20 ppm/°C in conjunction with resistors and capacitors having coefficients of hundreds of ppm/°C. The resistor should be a high stability metal oxide or wire-wound type and the capacitor should be, preferably, a very high stability silver

mica type, bearing in mind that it may be cheaper to select resistors and capacitors with equal and opposite temperature coefficient than to use components with zero coefficients.*

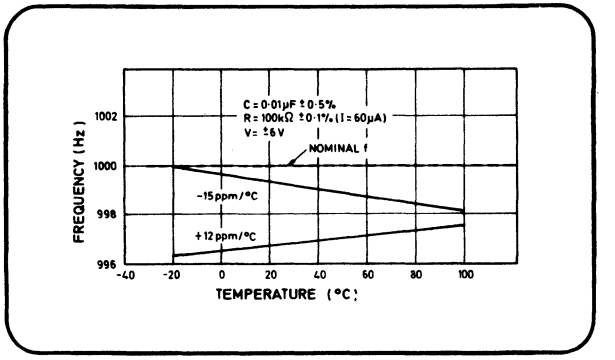


Fig. 3 VCO stability

This simple oscillator may be frequency-modulated by introducing an additional current at pin 7 (positive or negative, provided that the total current in pin 7 is never, even transiently, less than 20μA) which provides a convenient low impedance earth potential summing point. The frequency is given by I/CV_{ref} where I is the total timing current into the timing pin or pins in use, and V_{ref} is the value of the negative voltage on pin 3. As is shown by Fig 4 this expression holds with good accuracy over a wide range of current.

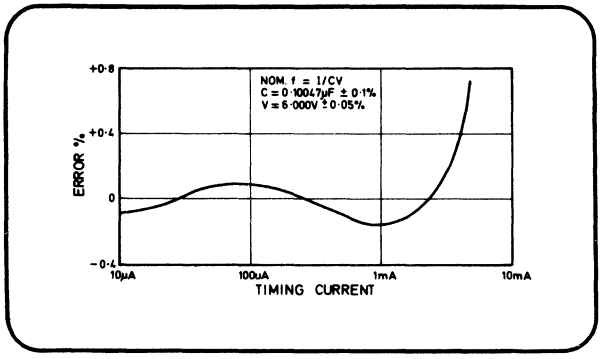


Fig. 4 VCO linearity

If the negative end of the timing resistor is held at a constant negative potential (usually the negative supply) the period of the oscillator is proportional to the negative voltage on pin 3 which may vary between −0.5V and −7.5V but which must not be greater in magnitude than the positive supply, V+. The resistance between pin 3 and earth is about 8kΩ.

*It is interesting to note that the capacitor used in telephone modems using the SL650 is as expensive as the SL650 itself.

In the more usual case the frequency is varied by applying a control input, V_{in}, to the negative end of the timing resistor while pin 3 is held at a constant potential — generally that of the negative supply. V_{in} may have any negative value from a few hundred millivolts upwards but the timing current should not exceed about 5mA.

To summarise: the basic oscillator frequency is given by the expression $f = I/CV_{ref}$. If a timing resistor is used it becomes $f = Vr/CRV_{ref}$ and if the negative end of the resistor is connected to pin 3 this further simplifies to $f = 1/CR$. It is evident that if pin 3 and the timing resistor are both connected to the negative supply the frequency of oscillation is independent of supply voltage. In these expressions f is in kHz, I in mA, V in volts, C in μF and R in kΩ. V_{ref} is the potential on pin 3 and V_r is the potential on the timing resistor.

The timing capacitor (pins 4 and 5) charges in both directions (see Fig 12). Consequently polar electrolytic capacitors are not suitable for use in this application, but any other type able to withstand the 4V which is the maximum ever applied to it may be used provided that the temperature coefficient is suitably low.

The VCO is a balanced circuit and normally operates the phase comparator with a balanced drive. One of the two connections is made externally, however, by connecting the VCO output (pin 2) to the phase comparator input on pin 1. Pins 1 and 2 must always be connected together (except when frequency division is required between the VCO and the phase comparator) but an external output may also be taken from pin 2 via a 10kΩ resistor. The output voltage at pin 2 is 0V at logic '0' and 1.1V at logic '1' and may therefore need to be buffered to drive external logic. To drive TTL a single transistor is usually sufficient.

If frequency division is required between the VCO and the phase comparator, the divided signal applied to pin 1 must be large enough to override the signal on the internal connection from the VCO to the phase comparator. A signal swing from −0.2V to +2.4V is sufficient and generally may be derived from TTL via an emitter follower with a 1kΩ load connected to V−.

The timing current inputs are pins 6, 7, 8 and 9, which are summing junctions, and are selected by logic inputs described in the following paragraph. The input (or inputs) in use are held at a potential very near to earth while the unused ones are at about +0.6V. Current (conventional) must always flow out of these pins, never into them. Thus if timing pins 6 and 7 are selected some current must flow from at least one of the two and no attempt should be made to put current into the other even if the net timing current remains in the correct direction.

BINARY INTERFACE (FREQUENCY SELECTION LOGIC)

Logic inputs on pins 10 and 11 select which of the timing inputs are used. Unused timing inputs should be left open-circuit and unused logic inputs may be open-circuit or connected to earth. Logic '0' is less than +0.6V and the logic '1' is greater than +2.4V. The input resistance on these pins is usually about 30kΩ but they can draw up to 400μA at +2.4V. TTL is thus perfectly suitable for driving these inputs but they may also be driven from DTL, RTL and, with suitable precautions, some types of MOS logic.

The truth table for the logic is shown below. If two timing pins are in use the

currents into them are added together when calculating the oscillator frequency e.g., if the calculations are with timing resistors the two resistors in use are assumed to be connected in parallel. This has the advantage when the logic is used for FSK modulation that only the main timing resistor need be very accurate – the resistor controlling the frequency increment is much higher in value and therefore need not be as accurate.

PIN 10	PIN 11	TIMING PINS IN USE
0	0	7
0	1	6 & 7
1	0	8
1	1	8 & 9

Truth Table – Binary Interface Logic

PHASE COMPARATOR

The phase comparator consists of a high gain differential limiting amplifier driving a double-balanced modulator, the output of which is buffered by an amplifier with current-controlled gain. As is already described, the carrier signal to the phase comparator is obtained from the VCO, both internally and via an external link between pins 1 and 2. If the VCO is not required, the external connection from pin 1 to pin 2 is omitted and a signal large enough to swamp the internal VCO signal applied to pin 1. If pins 1 and 2 are simply left unconnected, however, with no external signal applied to pin 1, the internal connection of the VCO to the phase comparator is not sufficient to keep the system functioning since the phase comparator input is then unbiased.

The signal input to the phase comparator is applied first to a high gain limiting amplifier with a differential input having high common mode rejection. The inverting and non-inverting inputs are pins 23 and 24 respectively. The input stage of this amplifier is a long-tailed pair with a common-mode range of ±4V when using ±6V supplies. Its bias current is typically 150nA but may be as high as 2μA, and its offset is 2mV. An input of 2mV r.m.s. will drive this amplifier to limiting. It may be applied differentially or to one input only, in which case the other input must be decoupled and held at the same DC potential. Although the input will limit with such a small signal it can accept signals up to within 0.5V of the supplies without overloading.

The output of the phase comparator is controlled by a current input to pin 22. The output is a current and the output voltage can rise to within 0.7V of the supply rails. With the current into pin 22 (I_{22}) at 250μA the transconductance of the comparator is 250mA/V but with I_{22} = zero the output is also zero and the output pin (pin 21) is

isolated. The voltage gain from pins 23 and 24 to pin 21 with I_{22} = 250μA and R_{load} = 10kΩ is 2,500. Since the output is a current, pin 21 may be short-circuited to earth or to either supply without damage.

In normal use pin 22 is connected to the positive supply via a 22kΩ resistor and the amplifier is effectively gated fully on. In some applications it is gated on and off as necessary and very occasionally an application calls for variable gain, in which instance control is applied to pin 22. The phase relationship of the various inputs of the comparator is such that if pins 1 and 24 have positive inputs there will be a positive output on pin 21.

When the SL650 is used as an oscillator, rather than as a PLL, the phase comparator may be used as an output stage by connecting pins 22 and 23 together and to a positive supply via a 22kΩ resistor, pin 24 to earth, and pins 1 and 2 together. This ensures that the output stage is turned on and the signal input amplifier biased to limiting in one direction.

AUXILIARY AMPLIFIER

The final circuit element to be described is the auxiliary amplifier (which is not present in the SL651). This was originally designed as a voltage comparator having an output meeting CCITT interface specifications. It will also function well as an operational amplifier provided that the closed loop gain is in excess of 10 in order to ensure stability. Its open loop gain is over 5000.

The inverting and non-inverting inputs of the auxiliary amplifier are pins 14 and 13 respectively and its common mode range is ±4V. The bias current is typically 25nA and the input offset 2mV. The output stage contains a circuit which limits the current at a nominal 6.5mA (4mA min.) so that the output (pin 15) may be short-circuited to earth or either rail without causing damage. The output swing, with ±6V supplies, is ±4.8V.

The versatility of the auxiliary amplifier is such that it may be used in a wide variety of filters, comparators, buffers, triggers and amplifiers. Some of its possible uses are described in the application notes that follow.

Applications

MODULATORS

The SL650 may be used in a wide variety of modulators, some of which are described below.

Frequency-shift Keyer

A frequency shift keyer using the SL650 is shown in Fig 5. The input applied to pin 11 selects either R1 or the parallel combination of R1 and R2 as the timing resistor. R1 must be as accurate as necessary to ensure the required accuracy of frequency but since R2 only determines the increment in frequency it need not be as accurate as R1. If two channels are required pin 10 is used for channel selection and the frequencies of the second channel are governed by R3 and R4. If only one channel is required pins 8 and 9 should be left unconnected and pin 10 should either be earthed or left unconnected.

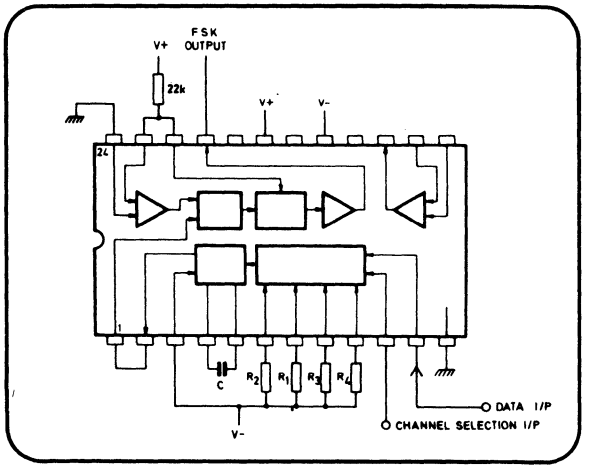


Fig. 5 A frequency-shift keyer

The phase comparator is used here as the output amplifier. It is turned on by connecting the positive supply to pin 22 via a 22kΩ resistor and the signal input is unbalanced (to allow the VCO carrier signal to pass through to the output) by earthing pin 24 and connecting pin 23 to pin 22, which is slightly positive. The output is a unity mark-space square wave of about 8V p-p, the logic '0' frequency is 1/CR1 and the logic '1' frequency is $1/C(R1R2/(R1+R2))$.

If four-frequency FSK is required both pins 10 and 11 must be used to programme it.

Frequency Modulator

The frequency of the VCO, as described in section 1, varies in direct proportion to the timing current and inversely with the potential on pin 3. Either of these parameters may be used to frequency-modulate the VCO, but if linear modulation is required it is better to vary the timing current.

Fig 6 shows such a system. As in the FSK system the comparator is used as the output stage. The input voltage may vary widely provided that the timing current is between 50μA and 2mA: this gives a 40:1 frequency variation. If narrow band FM is required either the input resistor R2 can be increased or the input voltage swing reduced.

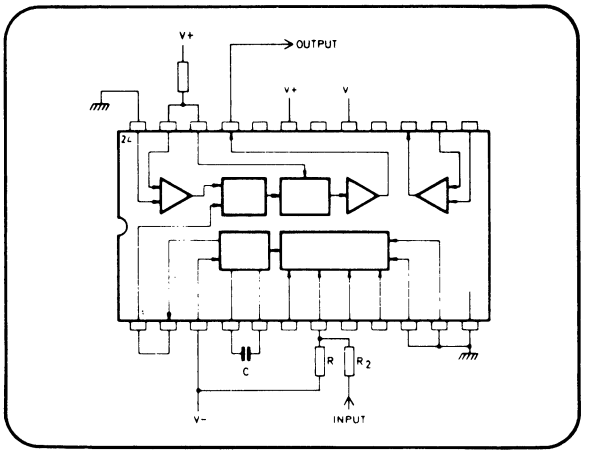


Fig. 6 Frequency modulator

Amplitude Modulators

There are two ways of amplitude modulating the output of the VCO, both of which use the variable gain facility of the phase comparator. They are illustrated in Figs 7(a) and 7(b).

In the simpler version of Fig 7(a), modulation is applied to pin 22, to vary the gain of the phase comparator output amplifier and hence the output level. As in the previous systems the signal input is biased to allow the VCO signal to pass through the double-balanced modulator. The preset potentiometer sets the current in pin 22 such that the peak-to-peak output at pin 21 is about half its maximum value. The input resistor may be adjusted to give about 95% modulation with any desired input signal.

The above technique gives reasonable results but the technique illustrated in Fig 7(b) uses the auxiliary amplifier to give linearities which are far better. The modulating signal in this case is applied to the non-inverting input of the auxiliary amplifier, used in this instance as a comparator. The phase comparator is again used as an output stage and its signal input biased to allow the carrier to pass through. The output from pin 21 is applied to the inverting input of the auxiliary amplifier, where it is compared with the input on pin 13. When the signal on pin 21 is negative, the

auxiliary amplifier output voltage is positive and the diode does not conduct; when pin 21 goes more positive than the input signal the comparator output goes negative, the diode conducts, and the output on pin 21 reduces until the comparator output goes positive again. Thus the auxiliary amplifier, acting as a voltage comparator, ensures that positive half cycles of the system output always have the same amplitude as the input signal. Since the capacitor on pin 22 has a time constant which is long compared with the VCO period but short compared with the highest modulating frequency the negative output half cycles will be the same amplitude as the positive ones. The system thus performs as a very linear amplitude modulator.

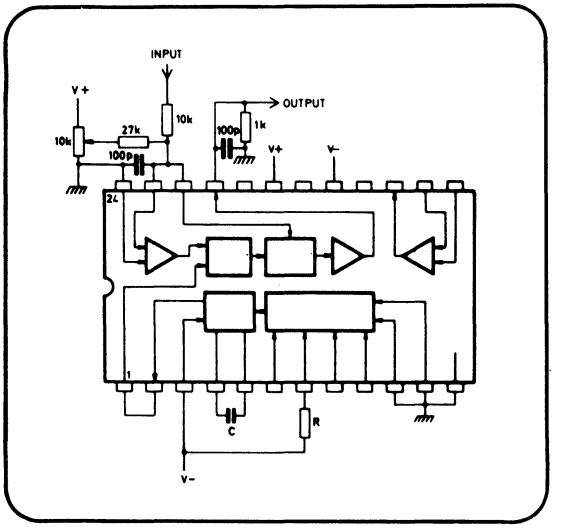


Fig. 7(a) Simple amplitude modulator

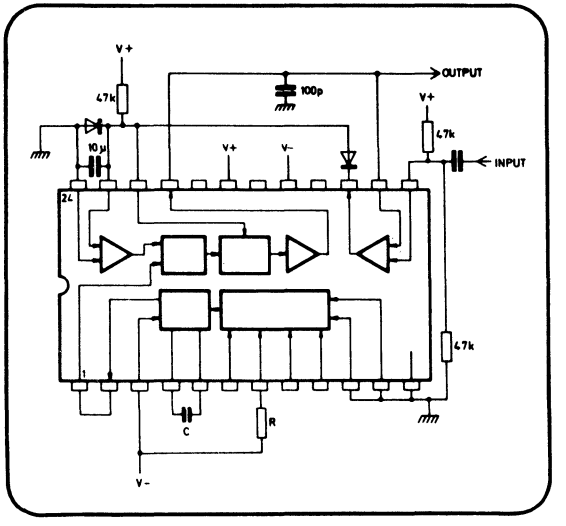


Fig. 7(b) A more linear amplitude modulator

Pulse Amplitude Modulation (PAM)

The output from either of the above systems of amplitude modulation consists of an amplitude modulated square wave carrier rather than an amplitude modulated sine wave carrier. It is thus very simple to convert this AM to PAM by removing the negative half cycles, with a diode or a transistor.

Suppressed Carrier AM (SCAM or DSB)

Since the phase comparator consists of a double-balanced modulator fed with carrier from the VCO it may be used, like any other double-balanced modulator, to produce DSB.

A system such as this is illustrated in Fig 8. To achieve carrier rejection it is necessary to adjust the preset potentiometer to bias the input amplifier at its mid-point. The input signal must be low enough not to limit the amplifier. Since both the amplifier gain and the bias point for zero carrier leak are affected by temperature this technique, and the AM technique described above, are really more of academic interest than of practical importance. Nevertheless, several useful signal processing systems can be derived from the various AM techniques which use the SL650.

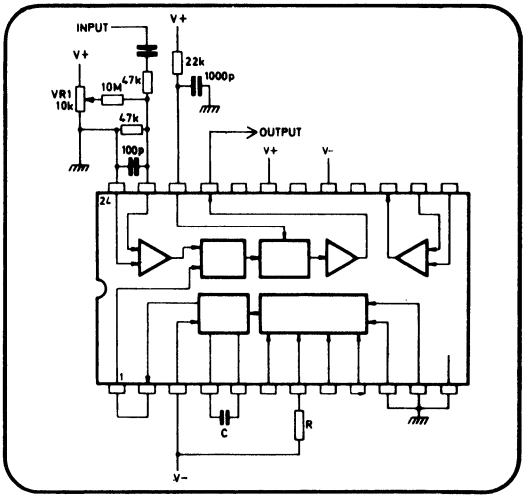


Fig. 8 ***A DSB modulator. The carrier is nulled using VR1***

Tone Burst

The output from the VCO can be gated by applying TTL or similar logic levels to pin 22 via a 6.8kΩ resistor. This application has considerably more utility than the above ones since it may be used to gate the output of one of several SL650 oscillators into a common line. Provided that only one is gated at a time the other outputs will not significantly load the common line.

Phase-shift Keying

Since the phase comparator is a double-balanced modulator the phase of the carrier signal which has passed through it will depend on the polarity of the input to the

signal amplifier. If pins 22 and 23 are connected together and to the positive supply via a 22kΩ resistor the phase comparator output will be turned on and a bias of +0.7V will be applied to the inverting input of the differential amplifier (pin 23). The output signal will be in phase with the signal on pins 1 and 2 if pin 24 is more positive than +0.7V, otherwise it will be 180° out of phase.

A phase shift keyer using this principle is shown in Fig 9. The auxiliary amplifier is used here to amplify the reference signal from pins 1 and 2. The amplifier shown here is non-inverting, but can be used as an inverting amplifier by reversing the connections to pins 13 and 14. If a low-level reference output of about 1V p-p is acceptable then it may be taken from pins 1 and 2 direct. The auxiliary amplifier is not then required and an SL651 can be used.

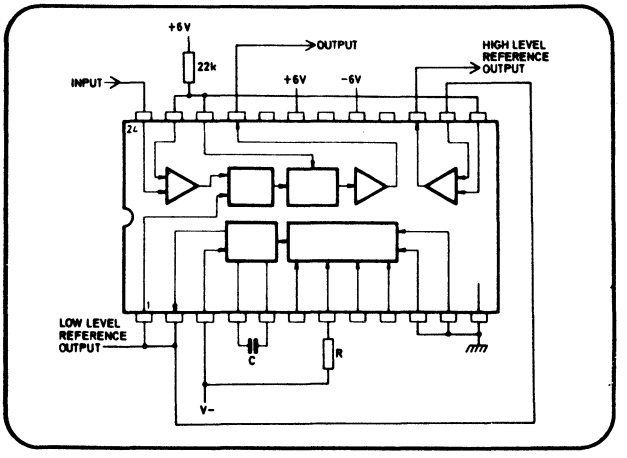


Fig. 9 Phase-shift keyer

Delta Modulation

An excellent delta modulator using relatively few components is illustrated in Fig 10. The VCO runs at the basic clock rate and its output at pins 1 and 2 is differentiated by a 100pF capacitor, the resulting brief current spike being used to gate 'on' the phase comparator output stage. This is connected only to the inverting input of the auxiliary amplifier and the short output current spike charges the stray capacity of the node which has a low enough leakage current to hold the charge until the next clock pulse.

The other input to the auxiliary amplifier is earthed and its output is the modulator output. The modulator output is integrated and applied to the inverting input of the phase comparator signal amplifier while the input signal is applied to its non-inverting input. Thus the integrated output tracks the input and the system is a true delta modulator.

Pulse Width Modulation (PWM)

The pulse width modulator using the SL650 and illustrated in Fig 11 is another example of the versatility of the circuit. It uses only three resistors and two capacitors in addition to the SL650 itself.

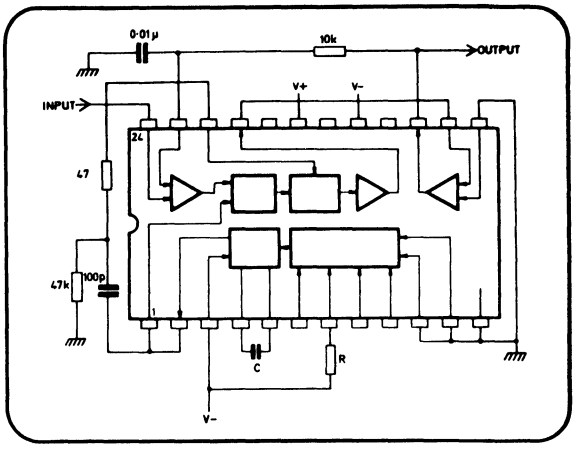


Fig. 10 Delta modulator

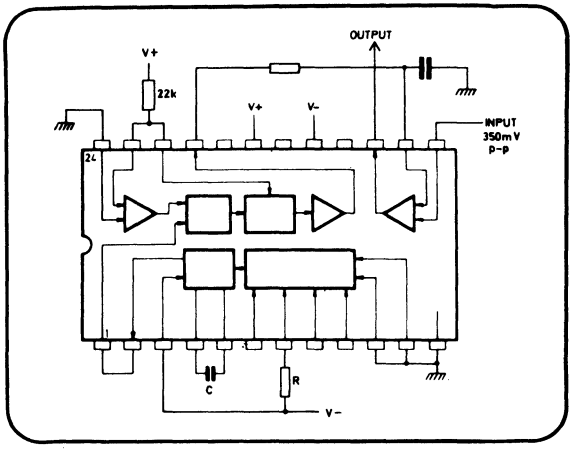


Fig. 11 Pulse width modulator

The VCO provides the clock and it is buffered through the phase comparator, which is used as a high level output stage in the usual way. The phase comparator output is integrated with a resistor and a capacitor to produce a triangular waveform of about 400mV p-p. The amplitude of this waveform could be greatly increased (at the cost of some loss of linearity) in which case the input signal may also be increased.

The triangular waveform is applied to one input of the auxiliary amplifier and the input signal applied to the other. The output is a PWM signal of about 7V p-p. The amplitude of the input should never exceed that of the triangular wave.

WAVEFORM GENERATORS

The distinction between modulators and waveform generators is a somewhat artificial one since all the modulators described above could equally well be considered as waveform generators where the output waveform is related in some way to an input

signal. However, in this section waveform generators are described which do not use an external input signal.

The basic waveforms of the SL650 are illustrated in Fig 12, which shows the oscillator output and timing capacitor waveforms as well as the effect on the phase comparator output of the gate current on pin 22 and of changing the sign of the input on pins 23 and 24. Several other waveforms may be obtained from the SL650, however, by making special connections or by the use of a small amount of external circuitry.

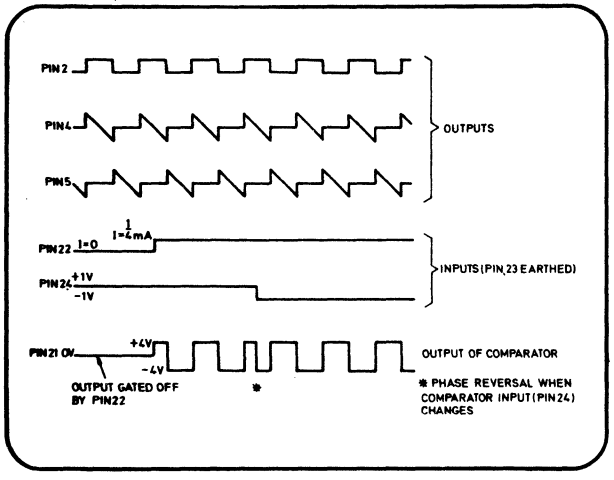


Fig. 12 SL650 waveforms

Sine and Triangular Waves

Triangular waves may, of course, be produced by the integrator that is part of the pulse width modulator described above, but the circuit shown in Fig 13 produces sinewaves with less than 1% harmonic distortion, triangular waves, and (rather less often required) trapezoidal waves.

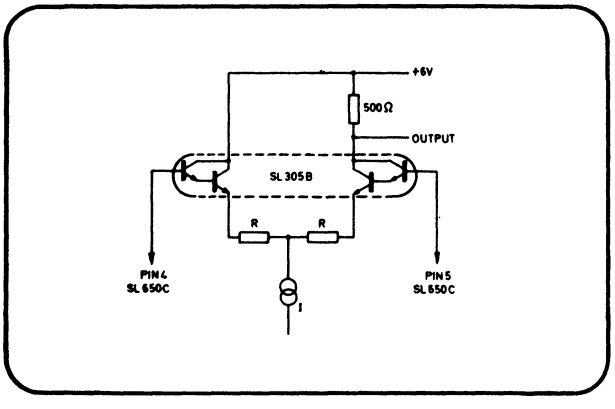


Fig. 13 Sinewave convertor

The different waveforms are produced by varying I and R. It should be noted that a constant current is far better than a resistor in the 'tail' due to the shape of the timing waveforms at pins 4 and 5. The amplitude of the timing waveforms at pins 4 and 5 depends on the potential on pin 3 and this sinewave circuit works best when the potential is −0.8V.

Since the amplitude of these waveforms is low and their source impedance 500Ω it is generally necessary to have an external buffer amplifier before they are applied to other circuitry. Connecting this circuit to pins 4 and 5 reduces the oscillator stability such that emitter follower buffers may be required.

Variable Mark/Space Ratio Rectangular Waves

The normal output of the VCO has a mark-space ratio which is unity to within better than 1%. If a waveform having other than unity mark-space ratio is required extra circuitry is necessary. The simplest way to achieve other than unity mark-space ratio is to alternate the timing resistor every half cycle by applying the oscillator output, obtained directly from pin 2 or, better, buffered using the phase comparator as an output stage, to pin 10. The timing resistors should be on pins 7 and 8 and the duration of each half cycle may be independently varied. This system is illustrated in Fig 14(a).

Fig 14(b) shows an arrangement of two resistors and a potentiometer which, used in place of the two separate timing resistors in Fig 14(a), gives a constant output frequency from the oscillator (although it may be varied if a variable negative voltage is connected to it instead of V−) but a mark/space ratio variable from 1:200 to 200:1.

Finally Fig 14(c) shows how, by the use of an external flip-flop, the oscillator may be programmed to have four successive half-cycles of different durations before the whole cycle repeats itself.

A Staircase Waveform Generator

The staircase waveform generator in Fig 15 was designed as a result of the work on the delta modulator. As in the delta modulator the VCO is used as a clock and the differentiated leading edge of each clock pulse is applied to the gate of the phase comparator output stage. This produces a pulse of output current which charges not just the stray capacity this time but also an external capacitor. The phase comparator output is still connected to pin 14 of the auxiliary amplifier, however, but the auxiliary amplifier is connected as a large hysteresis trigger circuit, the output of which goes back to the phase comparator signal input.

When the circuit is turned on the trigger is latched in an arbitary direction. This governs the polarity of the output pulses into the capacitor which charges a little more on each clock pulse until it has sufficient potential to change the state of the trigger circuit. The change of state alters the output pulse polarity and the potential on the capacitor steps down on each clock pulse until the trigger trips and the cycle starts again. A very high impedance buffer is required if the staircase is to drive external circuitry as any input current in the buffer will tend to alter the capacitor potential between clock pulses.

If 'step-up only' or 'step-down only' generators are required the output pulse polarity is held constant by a permanent bias on pin 23 or 24 and the trigger is used

only to recharge the capacitor. This recharging must be done through a diode to prevent the system oscillating independently of the VCO.

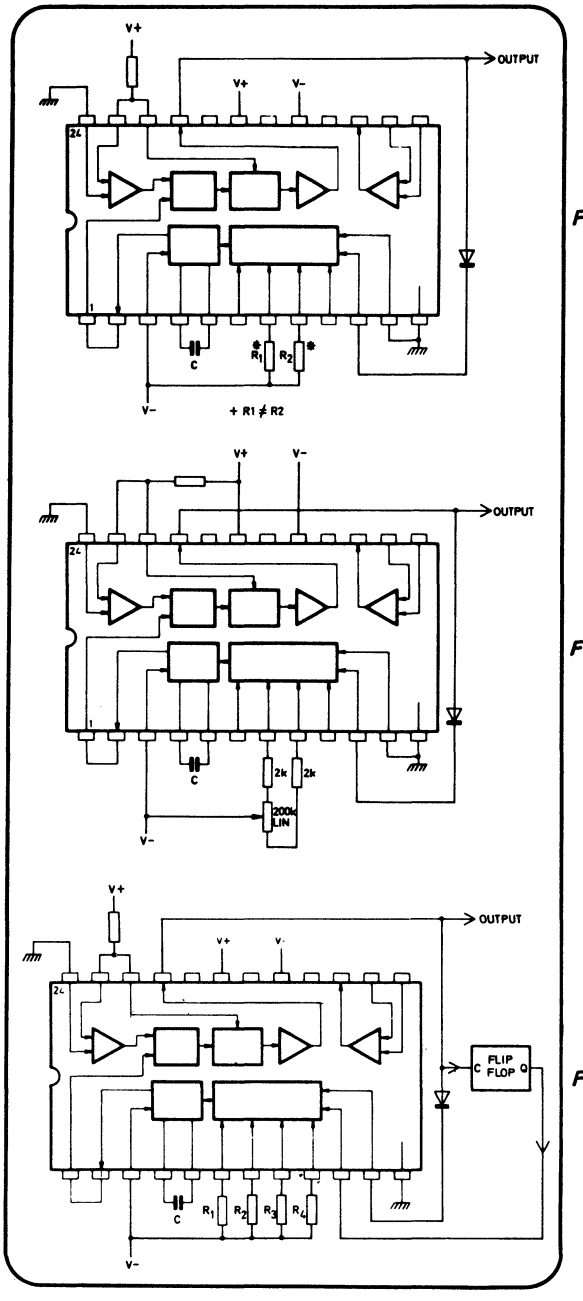


Fig. 14(a) Variable mark/space oscillator

Fig. 14(b) Variable mark/space constant frequency oscillator

Fig. 14(c) Four-period oscillator

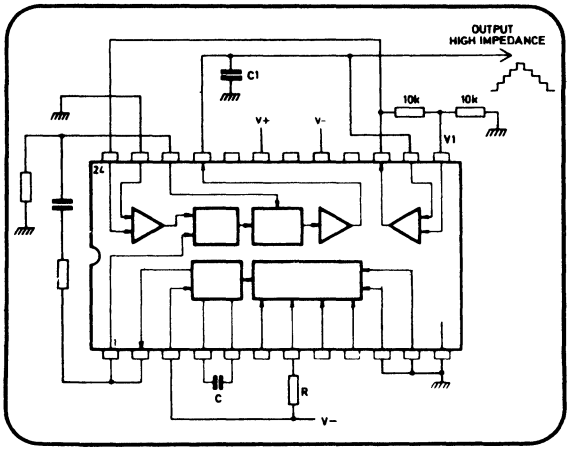


Fig. 15 Staircase waveform generator

DEMODULATORS

Most demodulators use the SL650 as a phase-locked loop, and the device was, in fact primarily designed to be used as a first order phase-locked loop in FSK detectors. Fig 16 shows a basic first order PLL built with the SL650. Its centre frequency, f_c, is defined by R_c and C according to the formula: $1/CR_c$. Being a first order loop, its lock and capture ranges are equal and defined by $1/CR_f$, and the response time constant is $CR_f/4$.

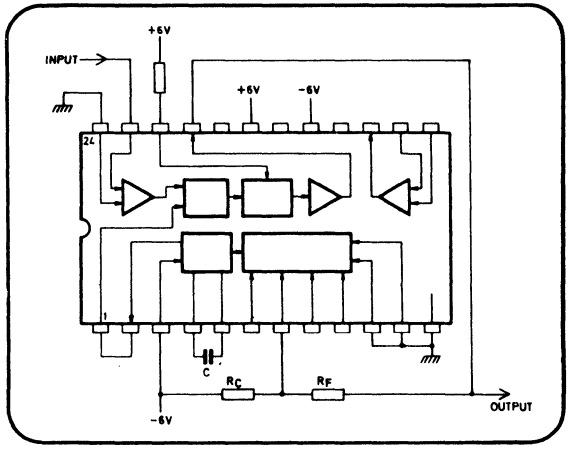


Fig. 16 Phase-locked loop FM detector

Three variants of the first order loop using the SL650 are shown in Figs 17, 18 and 19. The first two have variable lock range and the last (Fig 19) is interesting in that its output is proportional to the amount by which the period of the input frequency f_{in} varies from the period of the centre frequency f_c, rather than to the difference in frequencies.

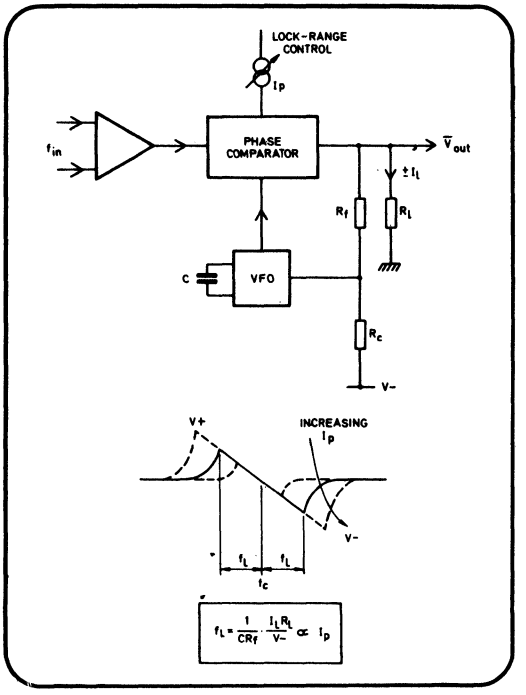


Fig. 17 ***Lock range control – constant output slope***

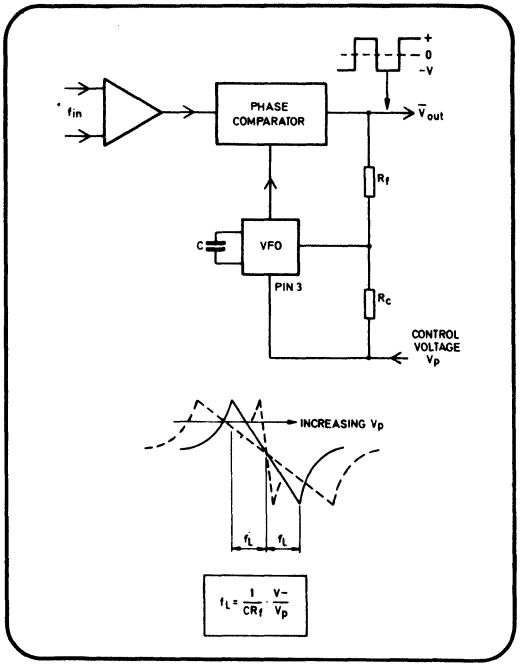


Fig. 18 ***Lock range control – constant output amplitude***

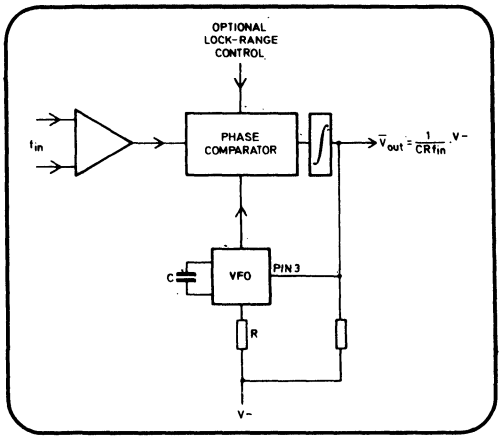


Fig. 19 ***First-order loop having output proportional to signal period***

In the circuit in Fig 17 the lock range is varied by varying the gain-control current to the phase comparator output stage (pin 22) (the output of the phase comparator must not saturate). This limits the lock range but does not affect the relationship between the input frequency and the output voltage dV/df. V is the mean output voltage after smoothing by an integrator, the output at pin 21 being a rectangular waveform whose amplitude is varied by I_{22} and whose mark/space ratio depends on the phase error between f_{in} and f_c.

The slope of dV/df_{in} is varied in the PLL in Fig 18 but the output voltage at the limits of the lock range does not vary with this slope. This is achieved by applying the lock range control as a voltage to pin 3 and the bottom of R_c, but it might equally well be done by varying R_f in which case the output of the phase comparator must be saturated.

If the comparator output is applied to pin 3 rather than to a timing current input (as in Fig 19), the PLL so produced will have an output proportional to period rather than frequency.

Tone Detectors, Lock Indicators and AM Demodulators

If the auxiliary amplifier, or an external high gain differential amplifier, is connected with its inputs across the timing capacitor its output will be in quadrature (90° out of phase) with the VCO and hence in phase with the incoming signal if the PLL is locked. This phenomenon may be used as an indication of phase locking — and hence in tone detectors — or in AM demodulators.

If the incoming signal is applied to one input of a double-balanced modulator and the in-phase signal applied to the other input, the output, when the VCO frequency and its harmonics have been removed by a low pass filter, will be a voltage proportional to the phase difference between the incoming signal and the in-phase signal. This voltage will be a DC signal which is zero when there is no phase error in the loop and can be used to indicate when the loop is locked.

A PLL designed with a limited lock and capture range and connected to a lock indicator as described above (and illustrated in Fig 20) will lock only when a frequency within its lock range is present. Hence, indication of phase lock is indication

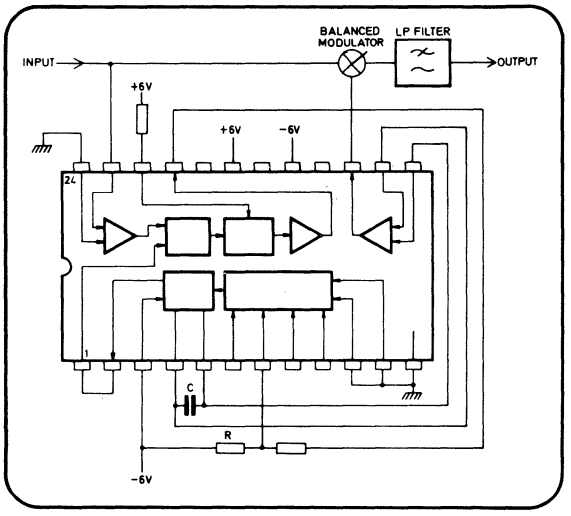


Fig. 20 Lock or AM detector

of the presence of a frequency within the lock range and the system acts as a tone detector. Such tone detectors employing the SL650 are very simple and exhibit high stability provided that stable timing components are used, although the lock time may affect their response. They may be used in multi-channel control systems with tone access, touch-tone decoders and almost any other system where accurate tone decoding is required. Their greatest advantage over most other tone detector systems is the absence of inductors.

If the input to the lock detector described above is amplitude modulated, the system acts as a synchronous demodulator. Such a circuit can be constructed with two SL650s but the input to the demodulating SL650 must be very small; it would be simpler and cheaper to use an SL650 as the PLL and an SL640* as the extra double-balanced modulator.

FM and FSK Demodulators

Since the loop feedback signal is proportional to the input frequency the basic PLL is an FM demodulator. If the basic circuit in Fig 16 is built with f_c equal to the carrier and the capture and lock range about 50% larger than the expected deviation (to allow for system tolerances and a faster capture) it will perform as an excellent FM demodulator. The output should be passed through a low pass filter to remove the VCO frequency and its harmonics.

FSK is demodulated in much the same way as FM but the system constants should be arranged so that the mean output is +1.5V on 'mark' and −1.5V on 'space'. If the output is connected through a low pass filter to the non-inverting input of the auxiliary amplifier, the inverting input being earthed, the output can be increased to +4V on 'mark' and −4V on 'space'.

FSK demodulators are also described in some detail in the following section.

* See SL600 series Applications Manual

SYSTEMS

With a circuit as versatile as the SL650, it is impossible to give details of all the systems in which it might be used with advantage and it is hoped that the preceding application notes will suggest a large number of uses where the SL650 will replace more complex or more expensive systems. This section will be restricted to descriptions of the use of the SL650 in low speed data modems for the transmission of data over telephone lines and, as an example of its use outside this field, in a simple DVM (digital voltmeter) circuit.

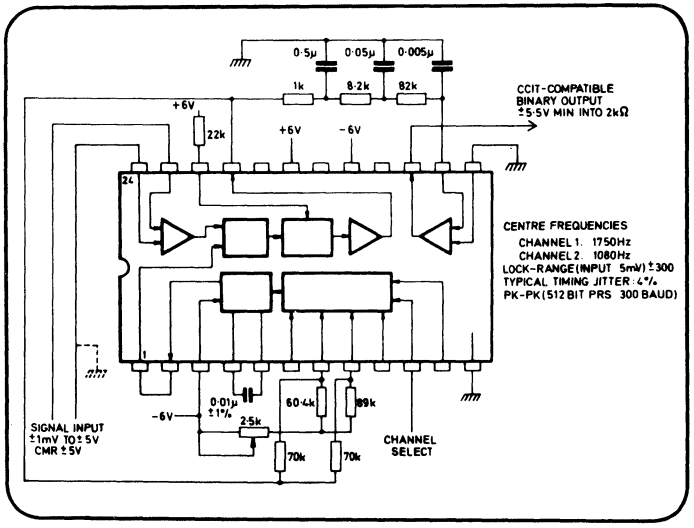


Fig. 21 Two channel modem receiver

A Two-Channel Modem Receiver

A two channel modem receiver working at centre frequencies of 1080 and 1750Hz is shown in Fig 21. In addition to the SL650 it uses only nine resistors and four capacitors and it gives a CCITT-compatible binary output on ±7.5V rails.

The receiver consists of a simple first order PLL as described on page 19 with centre frequencies of 1080 or 1750Hz (selected by a logic signal on pin 10) and a lock/capture range of ±300Hz. The output from the PLL passes through a three stage low pass filter to the auxiliary amplifier and emerges as a CCITT-compatible binary output. If a single channel receiver is required pin 10 is left unconnected and the two resistors on pin 8 are omitted.

The low pass filter characteristics determine the amount of jitter on the output signal. If the carrier and its harmonics are attenuated by over 40dB, jitter should be under 1%.

A Two-Channel Modem Transmitter

Fig 22 shows a two-channel modem transmitter working with the same channel centre frequencies as the receiver described above, and a 200Hz shift. Like the receiver

it may be converted to single channel operation by isolating pin 10 and removing the timing resistors on pins 8 and 9. Provided that the timing resistors and capacitor are sufficiently stable this modem transmitter will meet most countries' Post Office specifications for modem frequency stability.

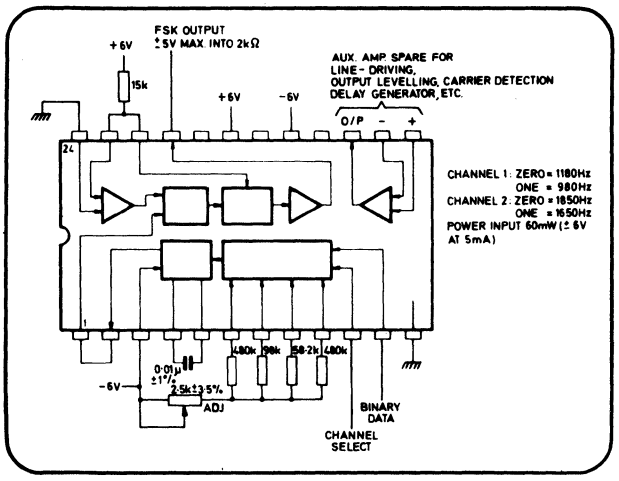


Fig. 22 Two channel modem transmitter

A Single Channel Simplex Modem Transceiver

A complete modem transceiver, using only thirteen components and small enough to fit in the base of a normal telephone, is illustrated in Fig 23. It is basically a combination of the receiver and transmitter described above but of course can only be

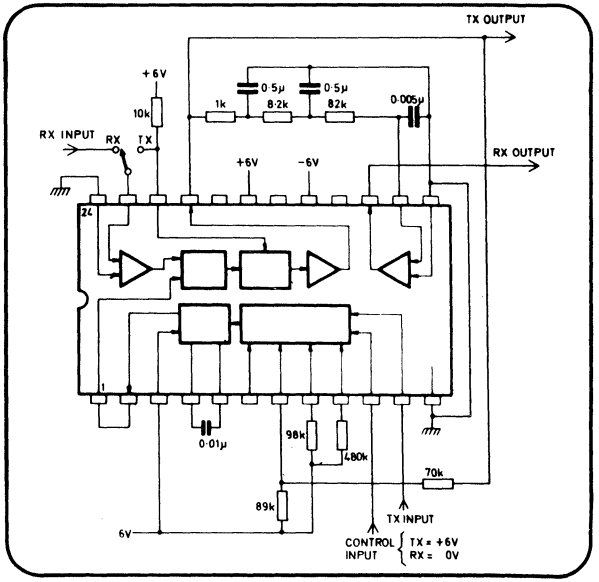


Fig. 23 Single channel modem transceiver for 1080Hz

made to work on one channel unless the timing resistors are switched externally. It is also a simplex system i.e., it cannot transmit and receive simultaneously but must be switched from transmit to receive. It is nevertheless most useful as a simple basic modem.

A Dual Channel Duplex Modem Transceiver

A full duplex modem capable of working at up to 300 bauds is shown in block form in Fig 24. Essentially it consists of a receiver and transmitter as shown in Figs 21 and 22, combined with channel filters, buffer amplifiers and some control logic.

In operation, the incoming signal passes through a filter which removes the outgoing signal and is then detected by the SL650 FSK detector. In this case the PLL is second order and the loop filter characteristics are chosen to minimise jitter on the received data output. The post detector filter removes any remaining carrier from the received data before it leaves the modem. This filter is usually a third or fifth order Butterworth active filter.

The transmitter signal is generated from the data input in the basic SL650 FSK modulator circuit. It then passes through a filter (which removes harmonics) to the transmitter buffer amplifier and thence out to the line. This filter also prevents the received carrier getting into the FSK modulator.

The form of channel selection and carrier detection varies from modem to modem. The simplest system always transmits on one channel and receives on the other and may not even have a carrier detector (although this is unusual). This involves no channel switching at all. More usually the channel selection logic operates by deciding, according to a fixed convention, whether the local modem is calling or being called

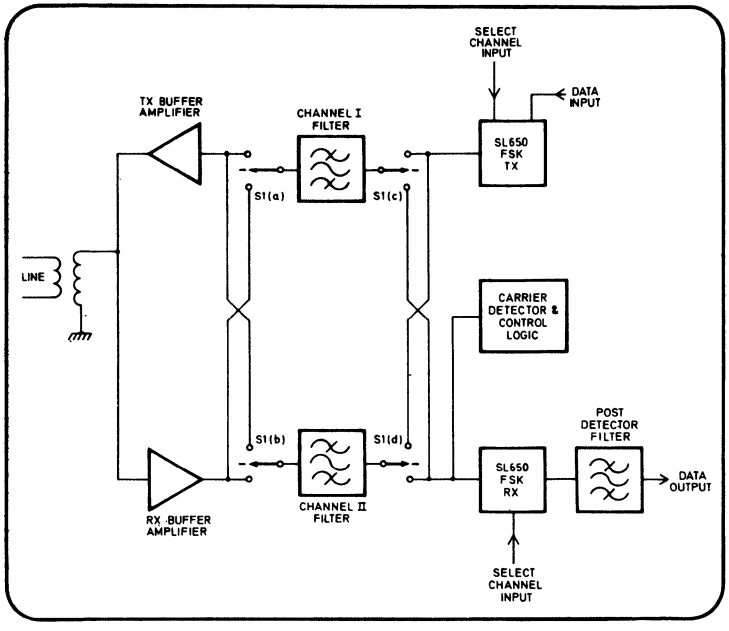


Fig. 24. Full duplex modem

and choosing transmit and receive channels accordingly – the system used by the British Post Office. It is perfectly possible, however, to instal frequency-sensing logic to sense which channel a caller is using and to reply on the other.

Carrier detection in British Post Office systems uses a level sensing circuit. This has disadvantages and many other systems use a lock detector in the PLL FSK demodulator which will only respond to a carrier and not to other sorts of signal. An advantage of the lock detector is that most of the circuitry is present in the FSK demodulator and need not be duplicated.

Using SL650s this modem can also be made small enough to fit into a telephone base and it uses so little power that it may be run from an inverter on the telephone lines themselves. It is obviously a very valuable circuit.

A Digital Voltmeter

A digital voltmeter using an SL650 is shown in Fig 25. It is of the dual integration type – the VCO runs at 100kHz until the ÷ 1,000 counter is full (meanwhile charging C_{int} at constant current) and then runs at a frequency proportional to the input voltage (which must be negative) until the charge on C_{int}, which is being removed at the same rate that it was put in, reaches zero. The contents of the counter are then displayed and the cycle repeats. The auxiliary amplifier is used as a comparator to sense when C_{int} is fully discharged. Such a system relies heavily on having a VCO whose frequency is truly proportional to voltage, but does not need a particularly good integration capacitor. The count and display logic and set reset flip-flop may be made with any suitable logic.

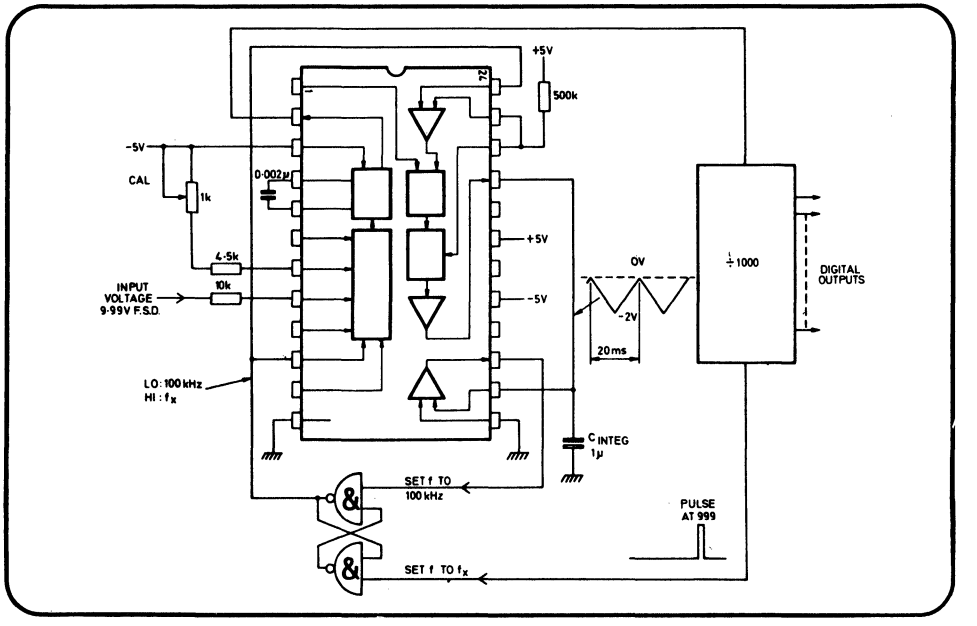


Fig. 25 A digital voltmeter

Glossary

AM Amplitude Modulation – a form of modulation where the amplitude of a carrier is varied by the modulating signal.

Baud A unit of signalling speed equal to the number of data bits per second.

Capture Range The band of frequencies where a PLL will establish lock with an input.

Capture Time Constant The average time for a PLL to acquire lock with a particular signal.

Delta Modulation A form of clocked digital modulation where the digital output need only be integrated to regain the analogue modulating signal.

DSB (or SCAM) Double Sideband (or Suppressed Carrier AM) – a form of amplitude modulation where the carrier itself is not transmitted, merely the information carrying sidebands. In the absence of modulation there is no signal.

Duplex (Full or Half) A communication mode where a transciever (radio, data or whatever) simultaneously transmits and receives. In full duplex the transmitted signal is suppressed at the transmitter end, in half duplex the signal, as well as being transmitted, is reproduced at its home transceiver. (See 'Simplex').

Error Signal The voltage out of the phase comparator of a PLL which is proportional to the difference of phase between the two inputs.

FM Frequency Modulation – a form of modulation where the frequency of the transmitted signal is instantaneously proportional to the modulating signal.

FSK Frequency Shift Keying – a form of digital transmission where logic '0' is represented by one frequency and logic '1' by another.

Handshaking Exchange of control signals at the commencement of communication between two data sets.

High Pass Filter Often abbreviated to HPF. A circuit which only passes frequencies above a certain frequency known as its cut-off frequency.

Lock A PLL is said to be locked to an incoming signal when it is maintaining its VCO so as to track the incoming signal.

Lock Indicator A circuit which indicates when a PLL is locked to an incoming signal.

Lock Range The range of frequencies over which a PLL can remain locked to an incoming signal. This is always greater than, or equal to, the capture range (qv).

Low Pass Filter Often abbreviated to LPF. A circuit which only passes frequencies below a certain frequency known as its cut-off frequency.

Modem An equipment which encodes and decodes digital data so that it may be transmitted and received over wire or radio circuits. The majority of modems transmit and receive FSK.

PAM Pulsed Amplitude Modulation – a form of modulation where the instantaneous amplitude of the pulses in a pulse train is varied by the modulating signal.

PCM Pulse Code Modulation – a form of modulation where analogue data is sampled and converted to digital form for transmission.

PLL Phase Locked Loop. PLLs are sometimes classified as 1st or 2nd (or higher) order loops – this is a function of the filter between the phase detector and the VCO, by varying the characteristics of this filter such characteristics of the PLL as capture time and capture range (qv) may be adjusted.

PM Phase Modulation – a form of modulation where the information (analogue or digital) is carried in the variation of phase of a carrier relative to its unmodulated state.

PPM Abbreviation for Pulse Position Modulation – a form of modulation where the displacement of a pulse from its nominal position in a pulse train is proportional to the modulating signal.

PWM Pulse Width Modulation – a form of modulation where the instantaneous width of a pulse in a pulse train is proportional to the modulating signal.

Simplex A communication mode where a transceiver can either transmit or receive at any one time but not both. (See 'Duplex').

Tone Detector A circuit which gives an output if a tone within a particular frequency range is present at its input. A PLL with its capture range equal to the band of interest and equipped with a lock detector will perform this function.

VCO Voltage Controlled Oscillator – an oscillator whose frequency is a function of a control voltage. A VCO is a form of VFO (qv).

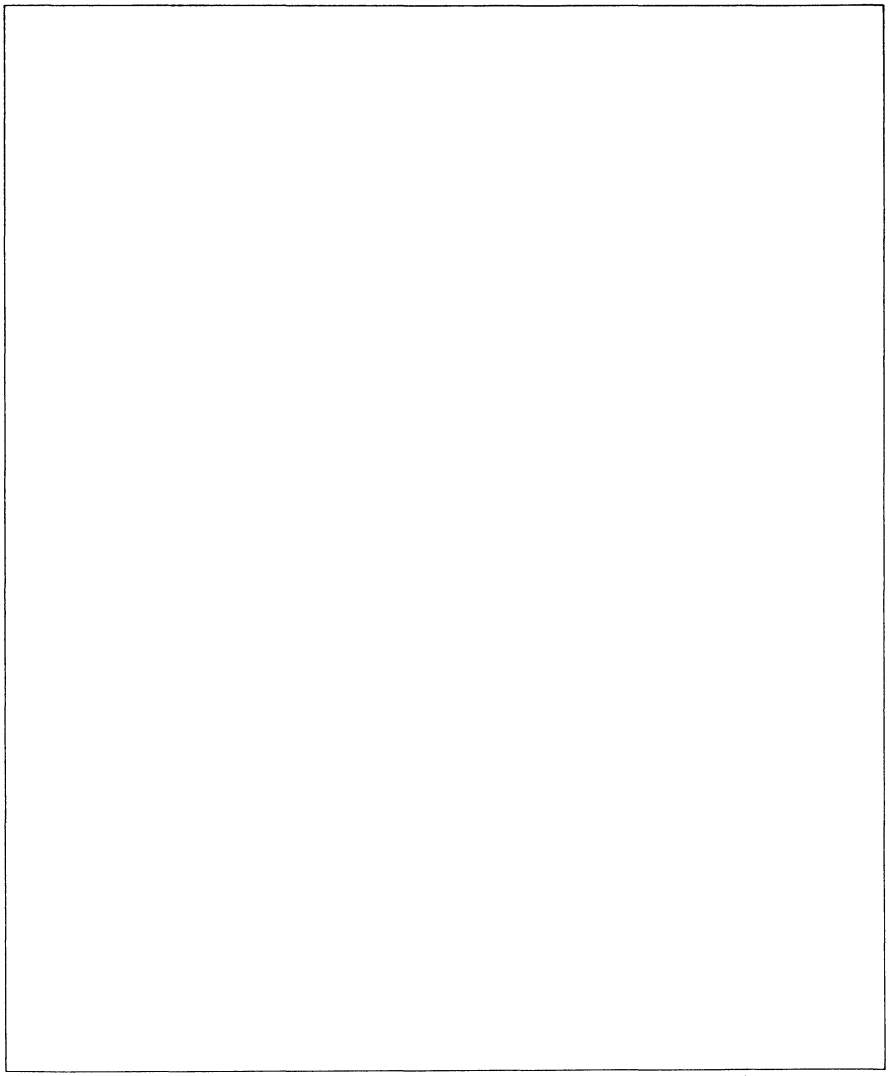
VFO Variable Frequency Oscillator.

5. SL362 Applications

technical communication

Plessey Semiconductors

Using the SL 362C low noise transistor pair



The SL362C is a bipolar integrated circuit consisting of a pair of NPN transistors with exceptionally good noise performance and an f_T in excess of 1.6 GHz. It is in the same family as the SL360C, with the same close tracking of parameters inherent in a monolithic circuit, and is therefore suitable for use in circuits requiring a pair of well matched, high frequency, low noise transistors. A typical application in a DC to 200 MHz low noise amplifier is described in detail, but some general data on the noise performance of the SL362C is given first.

LOW NOISE TRANSISTOR STRUCTURE

At frequencies between the low frequency flicker noise region and the high frequency region in which the noise increases due to gain fall off effects, the dominant parameter contributing to noise in the transistor is base resistance. The base resistance inherent in a particular transistor process can be reduced by connecting a number of elementary transistors in parallel to form a larger transistor with much reduced base resistance. Using this technique, the base resistance of the SL362C has been reduced to 30Ω compared with 250Ω for the SL360C. Fig.1 shows a typical noise figure for the SL362C versus emitter current at the optimum source resistance for each current. This optimum source resistance is shown against emitter current in Fig.2.

The major trade-off in the design of this type of low noise transistor structure is noise performance against high frequency performance. However, the high f_T of the SL362C (see Fig.3) makes it possible to use the device at frequencies well in excess of 60 MHz.

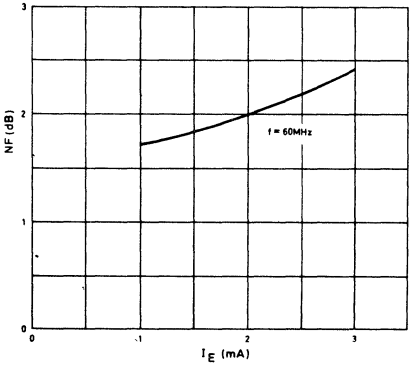


Fig.1 Typical noise figure at optimum source resistance

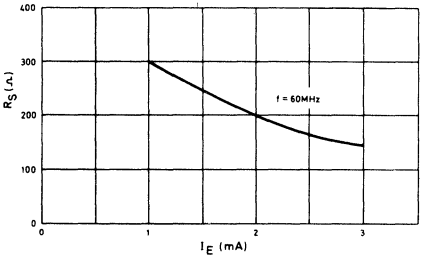


Fig.2 Optimum source resistance

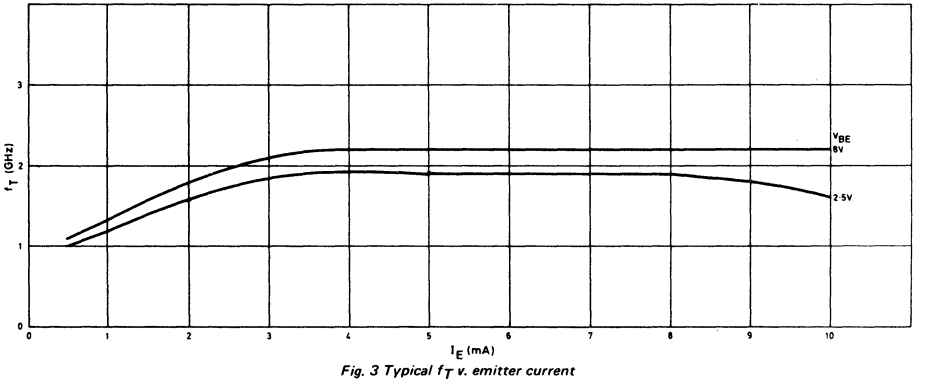


Fig. 3 Typical f_T v. emitter current

SIMPLE FEEDBACK AMPLIFIER (FIG.4)

The amplifier has a response down to DC achieved by the use of a long-tailed pair in the input stage, which also gives low offset voltages and a convenient method of applying negative feedback. The input is applied to Tr 1 and negative feedback applied to Tr 2 via resistors R 6 and R 7. Tr 3 is current-driven from the long-tailed pair and gives the output voltage across R 3. It is important to keep the stray capacitance from R 3 to ground as small as possible for the best high frequency performance. By the use of the very high f_T transistor pair SL360C for Tr 3 and Tr 4 any shunting effect of transistor capacitances across R 3 is reduced.

The frequency response of the amplifier shown in Fig.5 is flat to within ± 1 dB from DC to 240 MHz. The small peak at 200 MHz is not layout dependent but is due to parasitic lead inductance in the transistor packages. Measurements were made with a 50Ω source impedance and a load of 0.1 MΩ + 2.5 pF. The amplifier will drive a 50Ω load up to 150 MHz if required. For simplicity the noise figure was measured with a 50Ω source impedance and a spot noise figure of 4.2 dB was measured at frequencies of 30 to 200 MHz. The calculated variation of noise figure with source impedance is shown in Fig.6, which indicates an optimum noise figure of 2.5 dB at 200Ω source impedance.

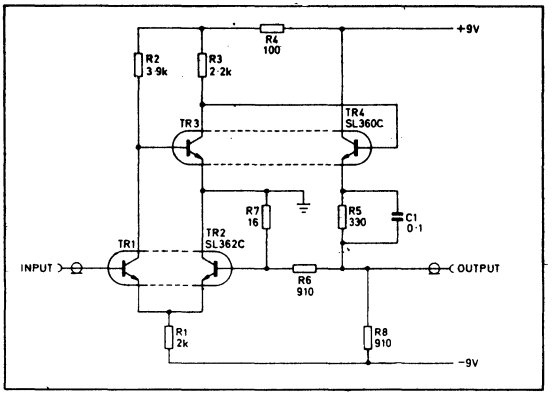


Fig.4 Circuit diagram

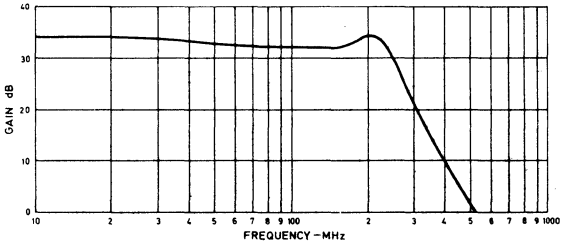


Fig.5 Frequency response of wide band amplifier

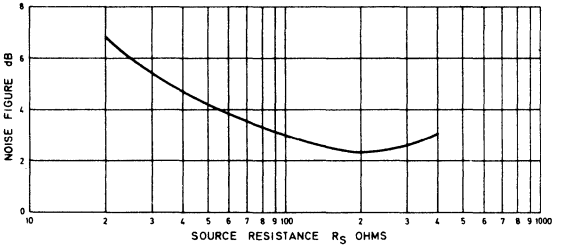


Fig.6 Calculated noise figure v. source impedance

LAYOUT

It has been found that the circuit is not particularly sensitive to layout change, but the obvious precautions in constructing VHF circuits should be observed. Transistor leads should be kept as short as possible, in particular the emitters of Tr 1, Tr 2 and Tr 3. The leads of R 7 should also be short and if accurate gain stability is not required, a carboncomposition resistor will give minimum inductance.

NOISE REDUCTION

Two techniques are available to reduce the noise figure at low source impedances. One is to use a transformer to produce a source resistance nearer to the optimum of 200Ω. The other method is to connect two transistors in parallel as shown in Figure 7. The effect of this combination is compared with a single transistor in Figure 8. The graph shows the calculated noise figure versus emitter current with a 50Ω source impedance for both long tailed pair and common emitter configurations. As can be seen, a noise figure of 1.6 dB at 50Ω source can be achieved with the arrangement of Figure 7 in a grounded emitter configuration. The parallel connected combination will, of course, have double the output capacitance of the single device, but the effect of this on the high frequency performance can be reduced by feeding into a low impedance. Also, the combination will have a lower f_T than a single transistor at a given operating current. However, if the current is doubled in the combination, little degradation will occur.

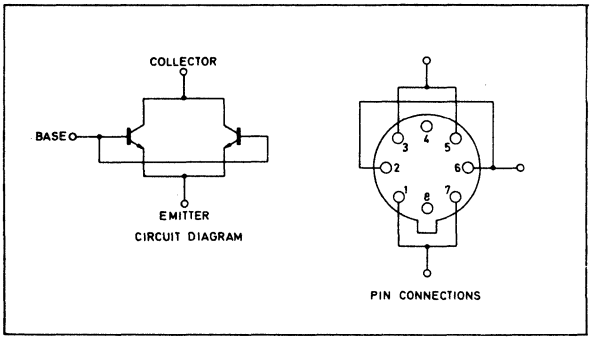


Fig.7 Parallel connection of two transistors

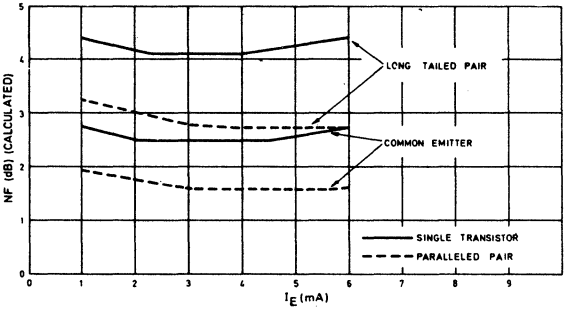


Fig.8 Noise figure at 50Ω source impedance

6. Technical Data

PLESSEY
SEMICONDUCTORS

SL300 SERIES
MATCHED TRANSISTORS

SL301K SL301L
DUAL NPN TRANSISTORS

The SL301K and SL301L are dual NPN transistors manufactured as monolithic integrated circuits. Their close parameter matching and thermal tracking are considerably better than conventional 'two chip' duals; the frequency response is equally superior.

The SL301K and L have identical electrical specifications but differ in packaging. The SL301 is pin compatible with existing SL300 series products and available in both metal can (CM) and ceramic dual-in-line (DG) packages. The SL301K is available only in metal can (CM) and is pinned to be compatible with conventional discrete 'two chip' products. Note, however, that an extra connection is required to allow the substrate to be connected to the most negative part of the circuit.

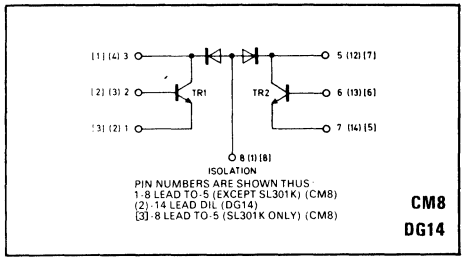


Fig. 1 SL301 circuit diagram

ORDERING CODES:

SL301K - CM
SL301L - CM
SL301L - DG

QUICK REFERENCE DATA

- Max voltage 12V to 20V
- Operating temperature range −55°C to +175°C

VOLTAGE RATING

The maximum voltage allowed between collector and emitter of each transistor is limited by dissipation and voltage breakdown. Assuming dissipation is low the rating may be determined from the following details:

(a) Forward bias condition

If the transistor is conducting the maximum collector-emitter voltage allowable is at least equal to V_{CEO} (12V). In cases where the collector current does not exceed 5mA and a resistor R is connected between base and emitter the V_{CER} rating may be determined from Fig. 8; this voltage lies between 12V and 20V depending on the value of R.

(b) Unbiased condition

If the transistor is operated with no connection to the base the maximum safe collector-emitter voltage is V_{CEO} (12V). In cases where the base emitter voltage has been reduced so the transistor is conducting at a low level it is generally permissible to increase this towards V_{CBO} (20V).

(c) Reverse biased condition

If the base of the transistor is connected via the resistor to a supply voltage equal to, or more negative than, the emitter voltage the maximum collector-emitter voltage V_{CEX} allowable (assuming negligible collector current) is limited by V_{CBO} (20V). For example, if the base is at −5V with respect to the emitter, the maximum collector voltage will be +15V.

FEATURES

- Close V_{BE} Matching
- High Gain
- Good Frequency Response
- Excellent Thermal Tracking

APPLICATIONS

- Differential Amplifier
- Comparator
- Stable Current Source

ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors: thermal ratings apply to total package dissipation.

The isolation pin must always be negative with respect to the collectors.

No one transistor may dissipate more than 75% of the total power.

Storage temperature	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance:	
TO-5 (CM)	250°C/W
Ceramic DIL	106°C/W
Chip-to-case thermal resistance:	
TO-5 (CM)	80°C/W
Ceramic DIL (DG)	39°C/W
V_{CBO}	20V
V_{CEO}	12V
V_{CER}	12V to 20V (see graph)
V_{EBO}	5V
V_{CIO}	25V
I_{CM}	50mA

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = +25°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Each Transistor					
BV_{CBO}	20			V	I_C = 10 µA
BV_{CEO}	12			V	I_C = 5mA
BV_{EBO}	5			V	I_E = 10 µA
BV_{CIO}	25			V	I_C = 10 µA
h_{FE}	30	50			V_{CE} = 5V, I_C = 10 µA
	40	70			V_{CE} = 5V, I_C = 100 µA
	60	100			V_{CE} = 5V, I_C = 1mA
	50	80			V_{CE} = 5V, I_C = 10mA
$V_{CE\ (SAT)}$		0.36	0.6	V	I_C = 10mA, I_B = 1mA
$V_{BE\ (SAT)}$	0.7	0.8	0.9	V	I_C = 10mA, I_B = 1mA
I_{CBO}			10	nA	V_{CB} = 10V
I_{EBO}			10	nA	V_{EB} = 2V
I_{CIO}			10	nA	V_{CI} = 10V
C_{OB}			2	pF	V_{CB} = 5V
C_{IB}			4	pF	V_{BE} = Ov
C_{CI}			6	pF	V_{CI} = 5V
f_T	400	680		MHz	V_{CE} = 5V, I_C = 5mA
Matching					
h_{FE1}/h_{FE2}	0.9		1.1		V_{CE} = 5V, I_C = 100 µA
	0.9		1.1		V_{CE} = 5V, I_C = 1mA
ΔV_{BE}			3	mV	V_{CE} = 5V, I_C = 100 µA
			3	mV	V_{CE} = 5V, I_C = 1mA
$\frac{\partial \Delta V_{BE}}{\partial T_{amb}}$			10	µV/°C	V_{CE} = 5V, I_C = 100 µA

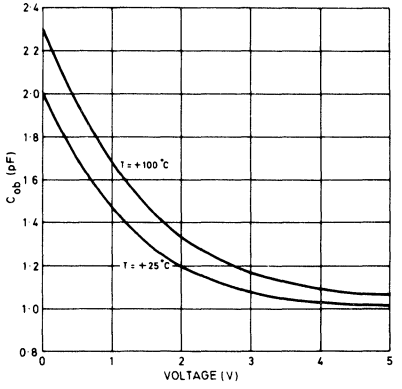


Fig. 2 Output capacitance (C_{ob}) v. voltage

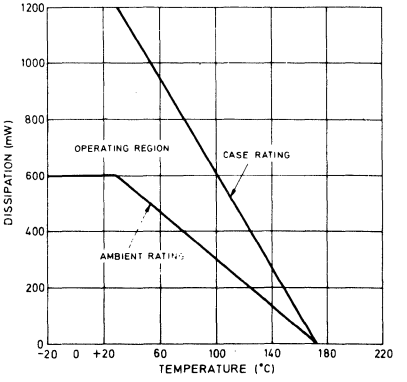


Fig. 3 Power dissipation derating curves (TO-5 package)

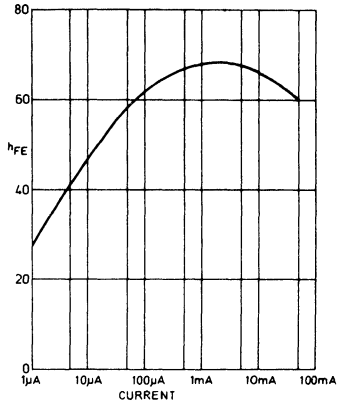


Fig. 4 Typical variation of h_{FE} with collector current

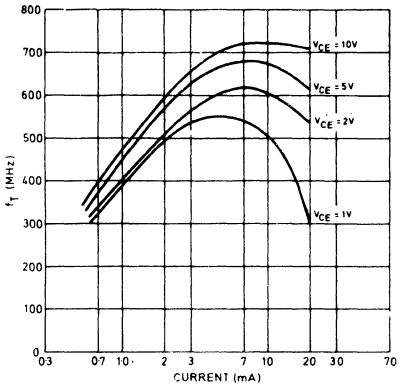


Fig. 5 f_T v. collector current ($f_T = f|h_{fe}|$. f = 100 MHz)

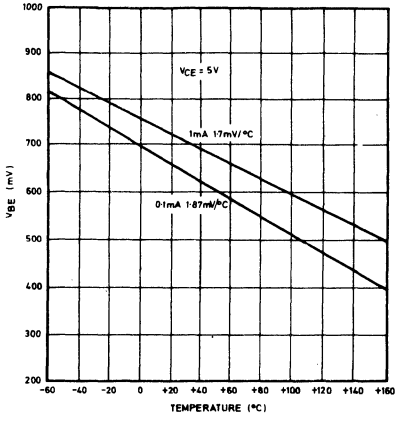


Fig. 6 V_{BE} v. temperature

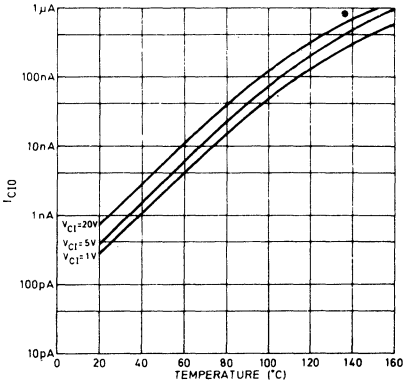


Fig. 7 Typical I_{CIO} v. temperature

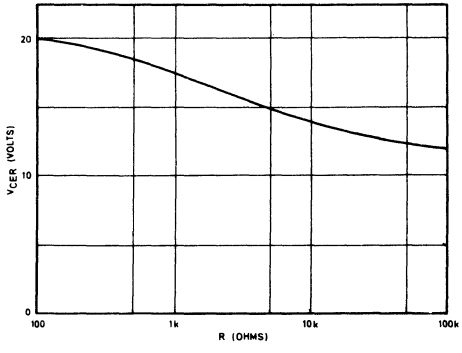


Fig. 8 Relationship between V_{CER} and R_{BE}

PLESSEY
SEMICONDUCTORS

SL300 SERIES
MATCHED TRANSISTORS

SL303L
TRIPLE NPN TRANSISTORS

The SL303 is a silicon monolithic integrated circuit comprising three separate transistors, two of which have closely matched parameters; the third transistor may be used as, for example, a tail transistor. The SL303 devices are available in 10-lead TO—5 (CM) and 14-lead dual-in-line (DG) packages.

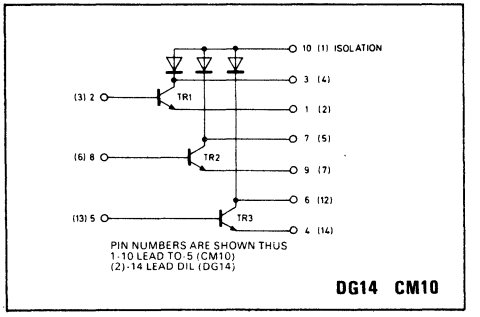


Fig. 1 Circuit diagram

ORDERING CODES:

SL303L — CM

SL303L — DG

FEATURES

- Close V_{BE} Matching
- High Gain
- Good Frequency Response
- Excellent Thermal Tracking

APPLICATIONS

- Differential Amplifier
- Comparator

QUICK REFERENCE DATA

Max voltage	12V to 20V
Operating temperature range	−55°C to +175°C

VOLTAGE RATING

The maximum voltage allowed between collector and emitter of each transistor is limited by dissipation and voltage breakdown. Assuming dissipation is low the rating may be determined from the following details:

(a) Forward bias condition

If the transistor is conducting the maximum collector-emitter voltage allowable is at least equal to V_{CEO} (12V). In cases where the collector current does not exceed 5mA and a resistor R is connected between base and emitter the V_{CER} rating may be determined from Fig. 8; this voltage lies between 12V and 20V depending on the value of R.

(b) Unbiased condition

If the transistor is operated with no connection to the base the maximum safe collector-emitter voltage is V_{CEO} (12V). In cases where the base emitter voltage has been reduced so the transistor is conducting at a low level it is generally permissible to increase this towards V_{CBO} (20V).

(c) Reverse biased condition

If the base of the transistor is connected via the resistor to a supply voltage equal to, or more negative than, the emitter voltage the maximum collector-emitter voltage V_{CEX} allowable (assuming negligible collector current) is limited by V_{CBO} (20V). For example, if the base is at −5V with respect to the emitter, the maximum collector voltage will be +15V.

ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors: thermal ratings apply to total package dissipation.

The isolation pin must always be negative with respect to the collectors.

No one transistor may dissipate more than 75% of the total power.

Storage temperature	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance:	
TO-5 (CM)	250°C/W
Ceramic DIL	106°C/W
Chip-to-case thermal resistance:	
TO-5 (CM)	80°C/W
Ceramic DIL (DG)	39°C/W
V_{CBO}	20V
V_{CEO}	12V
V_{CER}	12V to 20V (see graph)
V_{EBO}	5V
V_{CIO}	25V
I_{CM}	50mA

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = +25°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Each Transistor					
BV_{CBO}	20			V	I_C = 10 µA
BV_{CEO}	12			V	I_C = 5mA
BV_{EBO}	5			V	I_E = 10 µA
BV_{CIO}	25			V	I_C = 10 µA
h_{FE}	30	50			V_{CE} = 5V, I_C = 10 µA
	40	70			V_{CE} = 5V, I_C = 100 µA
	60	100			V_{CE} = 5V, I_C = 1mA
	50	80			V_{CE} = 5V, I_C = 10mA
$V_{CE\ (SAT)}$		0.36	0.6	V	I_C = 10mA, I_B = 1mA
$V_{BE\ (SAT)}$	0.7	0.8	0.9	V	I_C = 10mA, I_B = 1mA
I_{CBO}			10	nA	V_{CB} = 10V
I_{EBO}			10	nA	V_{EB} = 2V
I_{CIO}			10	nA	V_{CI} = 10V
C_{OB}			2	pF	V_{CB} = 5V
C_{IB}			4	pF	V_{BE} = Ov
C_{CI}			6	pF	V_{CI} = 5V
f_T	400	680		MHz	V_{CE} = 5V, I_C = 5mA
Matching(TR1, TR2 only)					
h_{FEI}/h_{FE2}	0.9		1.1		V_{CE} = 5V, I_C = 100 µA
	0.9		1.1		V_{CE} = 5V, I_C = 1mA
ΔV_{BE}			3	mV	V_{CE} = 5V, I_C = 100 µA
			3	mV	V_{CE} = 5V, I_C = 1mA
$\frac{\partial \Delta V_{BE}}{\partial T_{amb}}$			10	µV/°C	V_{CE} = 5V, I_C = 100 µA

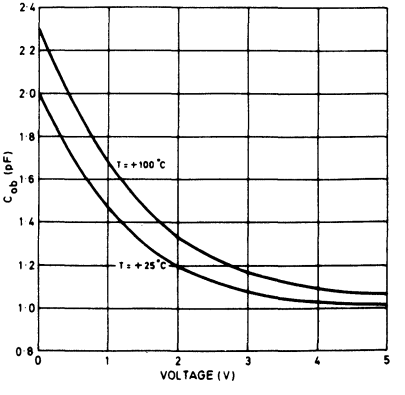


Fig. 2 Output capacitance (C_{ob}) v. voltage

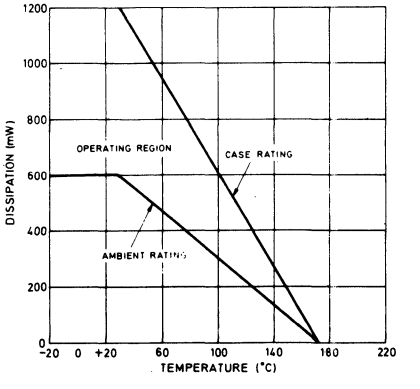


Fig. 3 Power dissipation derating curves (TO-5 package)

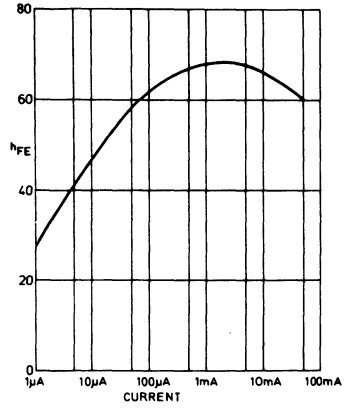


Fig. 4 Typical variation of h_{FE} with collector current

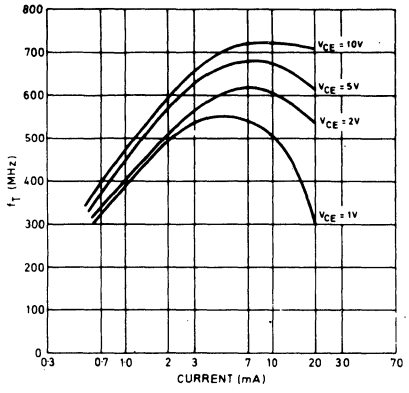


Fig. 5 f_T v. collector current ($f_T = f|h_{fe}|$. f = 100 MHz)

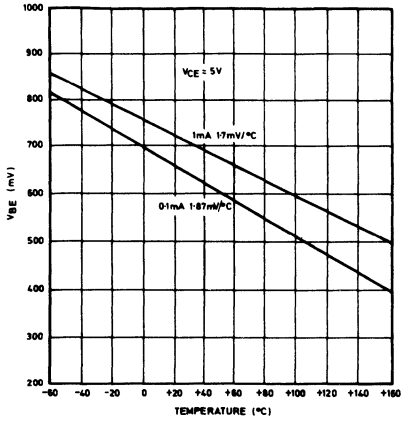


Fig. 6 V_{BE} v. temperature

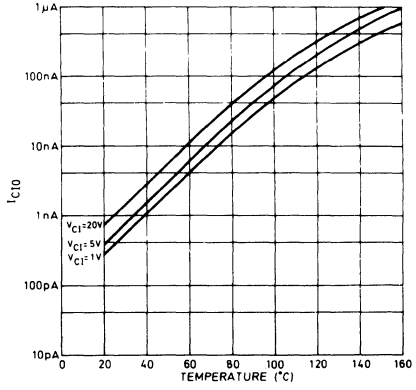


Fig. 7 Typical I_{C10} v. temperature

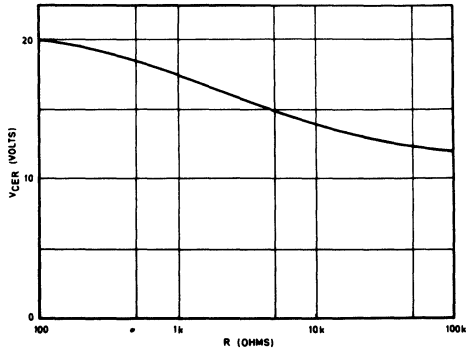


Fig. 8 Relationship between V_{CER} and R_{BE}

PLESSEY
SEMICONDUCTORS

MODULATOR DEMODULATOR

SL355C TBA673C

4-TRANSISTOR MODULATOR/DEMODULATOR

The TBA673 and SL355 are monolithic integrated 4-transistor modulator/demodulator circuits. Featuring close similarity in the characteristics of the individual transistors and optimal tracking of parameters with temperature, these devices give better balancing (and therefore less carrier leakage) than discrete circuits. The use of transistors instead of the more conventional diodes results in an improved isolation between input and output circuits.

The choice between TBA673 and SL355 will depend largely on the application. For example, the TBA673 has higher voltage characteristics than the SL355, but the SL355 would be used where high frequency performance is the prime consideration.

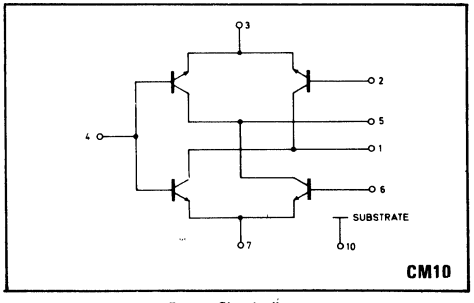


Fig. 1 Circuit diagram

FEATURES

- ΔV_{BE} = ±5mV Max.
- Close h_{FE} Matching
- High f_T : 250 MHz (TBA673)
  600 MHz (SL355)

APPLICATIONS

- DSB/DSBSC/AM Modulation
- Synchronous Detection
- FM Detection
- Choppers
- Signal Routeing
- Telephone Transmission (TBA673)

ABSOLUTE MAXIMUM RATINGS

Electrical (Each Transistor)

Rating	Symbol	TBA673	SL355	Units
Collector-emitter voltage	V_{CEO}	45	12	V
Collector base voltage	V_{CBO}	80	20	V
Emitter-base voltage	V_{EBO}	7.2	5	V
Collector-isolation voltage	V_{CI}	80	25	V
Collector current	I_C	100	20	mA

Power

Total power dissipation: See Fig. 3

Temperature

Storage temperature, T_{stg}: −35° to +125°C
Operating temperature, T_{amb}: See Fig. 3

NOTE

The substrate pin must be more negative than each of the collectors.

ELECTRICAL CHARACTERISTICS – TBA673

Test conditions (unless otherwise stated):
T_{amb} = +25°C
Characteristics apply to each transistor

Characteristic	Symbol	Value			Units	Condition
		Min.	Typ.	Max.		
Each transistor						
Collector-base breakdown voltage	BV_{CBO}	80			V	I_C = 10μA, I_E = 0
Collector-emitter sustaining voltage	LV_{CEO}	45			V	I_C = 5mA, I_B = 0
Emitter-base breakdown voltage	BV_{EBO}	7.2		8.0	V	I_E = 10μA, I_C = 0
Collector-isolation breakdown voltage	BV_{CIO}	80			V	I_C = 10μA
Collector-base leakage current	I_{CBO}			10	nA	V_{CB} = 10V, I_E = 0
Emitter-base leakage current	I_{EBO}			1	nA	V_{EB} = 2V, I_C = 0
Collector-isolation leakage current	I_{CIO}			3	nA	V_{CI} = 10V
Large signal current transfer ratio	h_{FE}	80		300		I_C = 5mA, V_{CE} = 5.0V
Transition frequency	f_T	250			MHz	I_C = 5mA, V_{CE} = 5.0V
Collector-isolation capacitance	C_{CI}			6.5	pF	V_{CS} = 0V
Matching characteristics						
Base-emitter voltage difference						
TR1–TR2	$V_{BE1}-V_{BE2}$		2.0	5.0	mV	
TR3–TR4	$V_{BE3}-V_{BE4}$		2.0	5.0	mV	V_{CE} (all transistors) = 5.0V
Large signal current ratio matching						
TR1/TR2	h_{FE1}/h_{FE2}	0.9				I_E (all transistors) = 100μA
TR3/TR4	h_{FE3}/h_{FE4}	0.9				

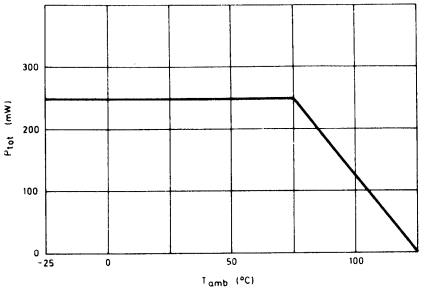


Fig. 2 Power dissipation

ELECTRICAL CHARACTERISTICS – SL355

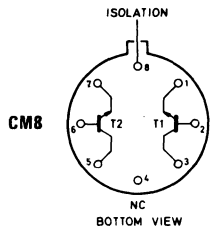
Test conditions (unless otherwise stated):
T_{amb} = +25°C
Characteristics apply to each transistor

Characteristic	Symbol	Value			Units	Condition
		Min.	Typ.	Max.		
Each transistor						
Collector-base breakdown voltage	BV_{CBO}	25			V	I_C = 10μA, I_E = 0
Collector-emitter sustaining voltage	LV_{CEO}	12	18		V	I_C = 5mA, I_B = 0
Emitter-base breakdown voltage	BV_{EBO}	5			V	I_E = 10μA, I_C = 0
Collector-isolation breakdown voltage	BV_{CIO}	25			V	I_C = 10μA
Collector-base leakage current	I_{CBO}		0.3	1	nA	V_{CB} = 10V, I_E = 0
Emitter-base leakage current	I_{EBO}		1	10	nA	V_{EB} = 2V, I_C = 0
Collector-isolation leakage current	I_{CIO}		1	10	nA	V_{CI} = 10V
Large signal current transfer ratio	h_{FE}	10	55			I_C = 100μA, V_{CE} = 5.0V
Transition frequency	f_T		600		MHz	I_C = 5mA, V_{CE} = 5.0V
Collector-isolation capacitance	C_{CI}			6.5	pF	V_{CS} = 0V
Matching characteristics						
Base-emitter voltage difference						
TR1–TR2	$V_{BE1}-V_{BE2}$		2.0	5.0	mV	
TR3–TR4	$V_{BE3}-V_{BE4}$		2.0	5.0	mV	V_{CE} (all transistors) = 5.0V
Large signal current ratio matching						
TR1/TR2	h_{FE1}/h_{FE2}	0.9				I_E (all transistors) = 100μA
TR3/TR4	h_{FE3}/h_{FE4}	0.9				

PLESSEY
SEMICONDUCTORS

SL300 SERIES
MATCHED TRANSISTORS

SL360C
2·5GHz MATCHED TRANSISTOR PAIR



CM8

The SL360C is a bipolar monolithic chip comprising a pair of integrated circuit transistors designed for applications where close parameter matching and thermal tracking are of prime importance. They have a very high f_t (typically 2.5 GHz) and low capacitances.

ELECTRICAL CHARACTERISTICS @ T_{amb} = +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	15	32		V	I_C = 10μA
BV_{CEO}	8	15		V	I_C = 10μA
LV_{CEO}	8	14		V	I_C = 5mA
BV_{CIO}	30	60		V	I_C = 10μA
BV_{EBO}	4.8			V	I_E = 10μA
h_{FE}	30	65			V_{CE} = 2V, I_E = 5mA
f_T	1.6	2.5		GHz	V_{CE} = 2.5V, I_E = 5mA, f = 200MHz
		3.2		GHz	V_{CE} = 5V, I_E = 25mA
$V_{BE1} - V_{BE2}$ (note 1)		3	10	mV	V_{CE} = 2V, I_E = 1mA
h_{FE1}/h_{FE2} (note 1)		1.1			V_{CE} = 2V, I_E = 5mA
V_{CE} (Sat)		0.25	0.4	V	I_E = 10mA, I_b = 1mA
C_{ob} (note 2)		0.7		pF	V_{CB} = 0V
C_{TE} (note 2)		1.5		pF	V_{BE} = 0V
C_{CI} (note 3)		2.7		pF	V_{CI} = 0V
V_{be} (on)		720		mV	I_E = 1mA, V_{CE} = 2V
I_{CBO}			1	nA	V_{CB} = 10V
I_{CIO}			1	nA	V_{CE} = 10V
I_{EBO}			1	nA	V_{EB} = 2V

NOTES

1. It is assumed here that device suffixed 1 has the greater numerical value.
2. These capacitances include stray header capacitance which is about 0.1pF.
3. These capacitances include stray header capacitance which is about 0.9pF.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Storage temperature	−55°C to +175°C
Operating junction temperature	+175°C max.

Maximum Dissipation (Note 5)

Dissipation at 25°C free air temperature	600mW
Dissipation at 100°C free air temperature	300mW

Maximum Voltages

BV_{CBO} : 15V
BV_{CEO} : 8V
BV_{EBO} : 4.8V
BV_{CIO} : 30V (note 6)

4 The maximum ratings are limiting absolute values above which life or satisfactory performance may be impaired.

5. These ratings give a junction temperature of 175° with a junction-to-ambient thermal resistance of 250°C/W (derating factor 4 mW/°C.)

6. The isolation pin should be negative with respect to the collectors.

PLESSEY
SEMICONDUCTORS

SL300 SERIES
MATCHED TRANSISTORS

SL 362C LOW NOISE TRANSISTOR PAIR

CM8

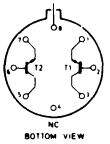


Fig.1 Pin connections

The SL362C is a bipolar monolithic integrated circuit comprising a pair of transistors designed for applications where low noise and very high frequency operation are of prime importance. A typical noise figure at 60MHz is less than 1.6dB.

ELECTRICAL CHARACTERISTICS @ T_{amb} = 25°C

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Conditions
BV_{CBO}	12	24		V	I_E = 10μA
BV_{CEO}	8	15		V	I_C = 10μA
BV_{CIO}	20	40		V	I_C = 10μA
BV_{EBO}	5			V	I_C = 10μA
h_{FE}	30	70			I_E = 1mA, V_{CE} = 2V
		60			I_E = 10mA, V_{CE} = 2V
f_T	1	1.6		GHz	I_E = 2mA, V_{CE} = 2V
	1.4	2.2		GHz	I_E = 10mA, V_{CE} = 10V
$V_{BE1} - V_{BE2}$		5		mV	I_E = 1mA, V_{CE} = 2V
Noise figure (note 1)		1.6	2.0	dB	I_E = 1mA, R_s = 200Ω f = 60MHz
C_{OB}		1.0		pF	V = 0
C_{CI}		0.9		pF	V = 0
C_{TE}		15.0		pF	V = 0

Note 1; The noise figures are quoted at 60MHz. Typically, they are constant from 10kHz to 200MHz.

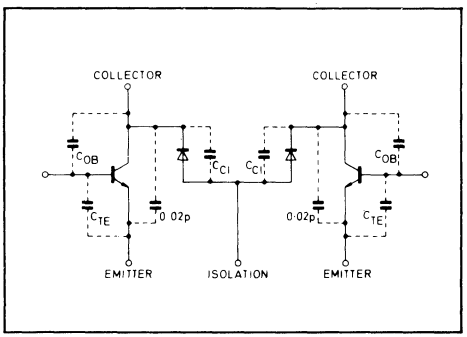


Fig.2 Equivalent circuit

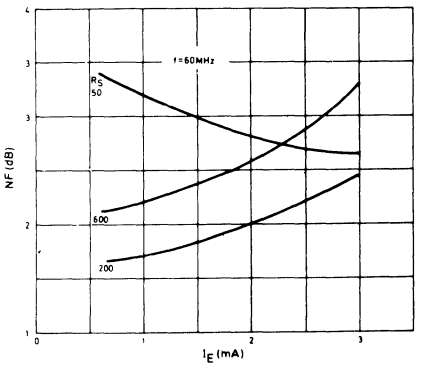


Fig.3 Typical noise figure v. emitter current

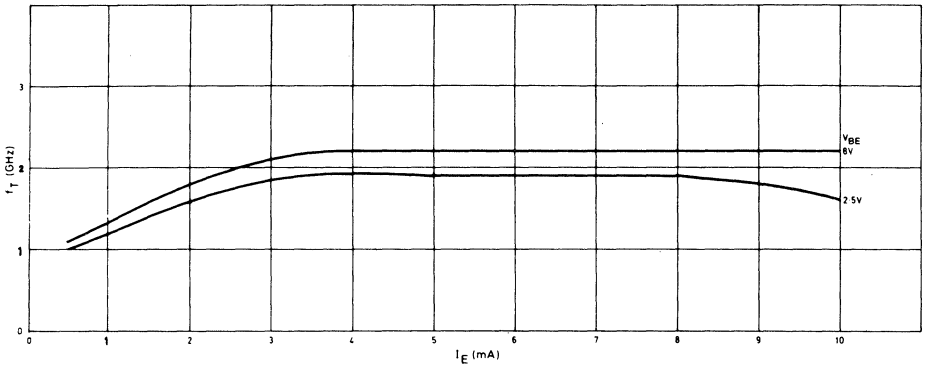


Fig.4 Typical f_T v. emitter current

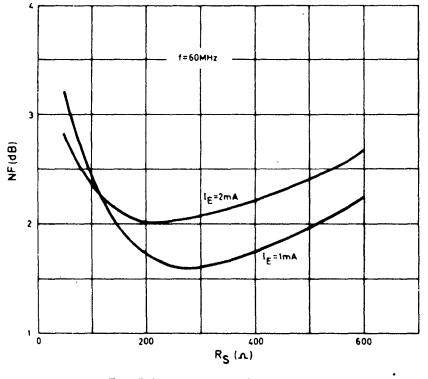


Fig. 5 Typical noise figure v. source impedance

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−55°C to +150°C
Operating Junction temperature	150°C
Total Dissipation	300mW
Collector current	50mA
BV_{CBO} :	12V
BV_{CEO} :	8V
BV_{EBO} :	5V
BV_{CIO} :	20V

Note: The isolation pin should be negative with respect to the collectors.

SIMPLE FEEDBACK AMPLIFIER (FIG.6)

The amplifier has a response down to DC achieved by the use of a long-tailed pair in the input stage, which also gives low offset voltages and a convenient method of applying negative feedback. The input is applied to Tr 1 and negative feedback applied to Tr 2 via resistors R 6 and R 7. Tr 3 is current-driven from the long-tailed pair and gives the output voltage across R 3. It is important to keep the stray capacitance from R 3 to ground as small as possible for the best high frequency performance. By the use of the very high f_T transistor pair SL360C for Tr 3 and Tr 4 any shunting effect of transistor capacitances across R 3 is reduced.

The frequency response of the amplifier shown in Fig.7 is flat to within ± 1 dB from DC to 240 MHz. The small peak at 200 MHz is not layout dependent but is due to parasitic lead inductance in the transistor packages. Measurements were made with a 50Ω source impedance and a load of 0.1 MΩ + 2.5 pF. The amplifier will drive a 50Ω load up to 150 MHz if required. For simplicity the noise figure was measured with a 50Ω source impedance and a spot noise figure of 4.2 dB was measured at frequencies of 30 to 200 MHz. The calculated variation of noise figure with source impedance is shown in Fig.8, which indicates an optimum noise figure of 2.5 dB at 200Ω source impedance.

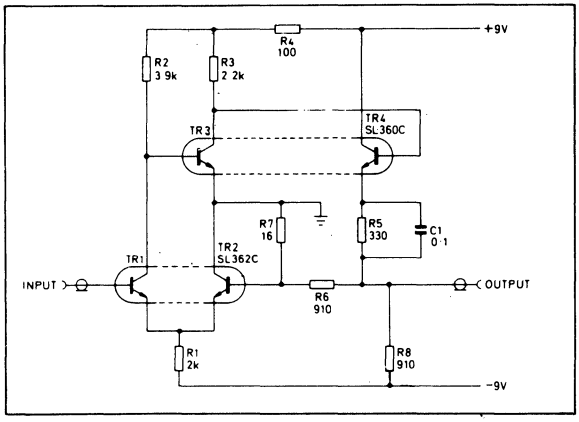


Fig. 6 Circuit diagram

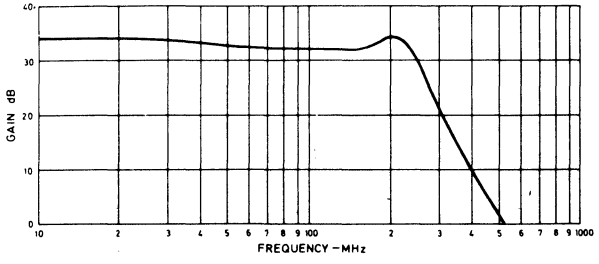


Fig. 7 Frequency response of wide band amplifier

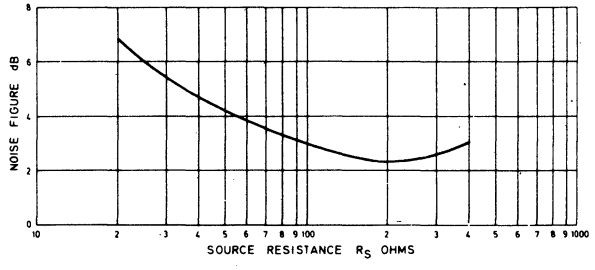


Fig. 8 Calculated noise figure v. source impedance

LAYOUT

It has been found that the circuit is not particularly sensitive to layout change, but the obvious precautions in constructing VHF circuits should be observed. Transistor leads should be kept as short as possible, in particular the emitters of Tr 1, Tr 2 and Tr 3. The leads of R 7 should also be short and if accurate gain stability is not required, a carboncomposition resistor will give minimum inductance.

NOISE REDUCTION

Two techniques are available to reduce the noise figure at low source impedances. One is to use a transformer to produce a source resistance nearer to the optimum of 200Ω. The other method is to connect two transistors in parallel as shown in Figure 9. The effect of this combination is compared with a single transistor in Figure 10. The graph shows the calculated noise figure versus emitter current with a 50Ω source impedance for both long tailed pair and common emitter configurations. As can be seen, a noise figure of 1.6 dB at 50Ω source can be achieved with the arrangement of Figure 9 in a grounded emitter configuration. The parallel connected combination will, of course, have double the output capacitance of the single device, but the effect of this on the high frequency performance can be reduced by feeding into a low impedance. Also, the combination will have a lower f_T than a single transistor at a given operating current. However, if the current is doubled in the combination, little degradation will occur.

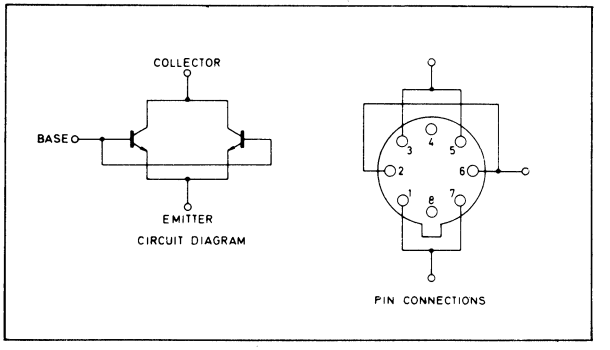


Fig. 9 Parallel connection of two transistors

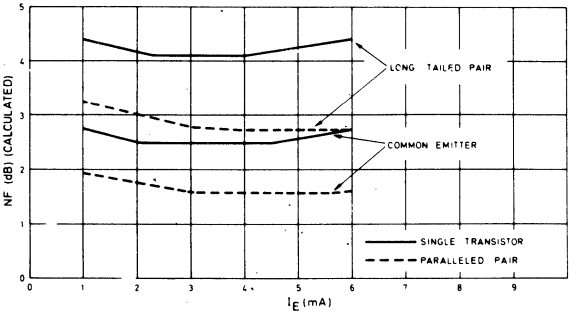


Fig. 10 Noise figure at 50Ω source impedance

NEW PRODUCT DATA

SL650B & C SL651B & C

MODULATOR/PHASE LOCKED LOOP CIRCUITS

The SL650/1 are versatile integrated circuits capable of performing all the common modulation functions (AM, PAM, SCAM, FM, FSK, PSK, PWM, tone-burst, delta-modulation, etc.). A wide variety of phase-locked loops can be realised using the SL650 or SL651, with all parameters accurately controllable; they can also be used to generate precise waveforms at frequencies up to 0.2MHz.

The highly accurate and stable variable frequency oscillator is programmable over a wide range of frequency by voltage, current, resistor or capacitor. In addition direct selection of one of four spot frequencies is facilitated by using the on-chip binary interface, which accepts standard logic levels at very low logic '1' input currents.

The differential input phase comparator has a wide common mode input voltage range. It has a high gain limiting amplifier at its input requiring only 1mV input to maintain lock range in a typical phase-locked loop. The current output is programmable from zero to over 2mA by an external resistor or current input, and the gain is voltage –, current –, or resistance – programmable from zero to greater than 10,000.

An auxiliary amplifier with a voltage gain of, typically, 5000 is incorpated in the SL650 for use when it is required to interface to specified levels and impedances. The auxiliary amplifier features low bias current (typically 25nA), fast recovery from overload, and a short-circuit output current of ±7.5mA.

The auxiliary amplifier is omitted from the SL651.

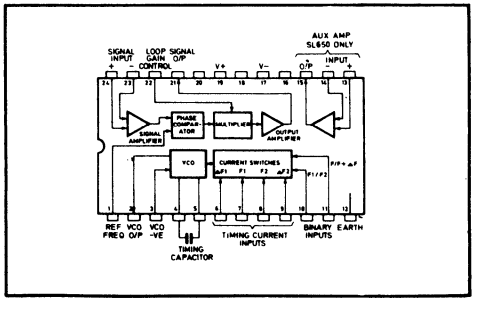


Fig.1 Pin connections (top view)

FEATURES

- VFO Frequency Variable Over 100:1 Range With Same Capacitor: Linearity 0.2%
- VFO Temperature Coefficient:
  'B' Types 20 ppm/°C Max.
  'C' Types 20 ppm/°C Typ.
- Supply sensitivity 20 ppm/% Typ.
- VFO Phase-Continuous at Transitions
- Binary Interface
- Phase Comparator O/P Can Swing to Supply Voltages
- On-Chip Auxiliary Amplifier (SL650)

APPLICATIONS

- Modems
- Modulators
- Demodulators
- Tone Decoders
- Tracking Filters
- Waveform Generators

QUICK REFERENCE DATA

Supply Voltages	±6V
Operating Temperature Range	–55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test Conditions

Supply voltage: ±6V
Supply currents: 1.5mA
T_A: +25°C ±5°C

Characteristics	Pins	Value			Units	Conditions
		Min.	Typ.	Max.		
Variable frequency oscillator						
Initial frequency offset error		−3	±1	+3	%	
Normal mark/space ratio		0.98	1.00	1.02	–	
Temp. coefficient of frequency			±20		ppm/°C	See note 1
Frequency variation with supplies	17, 19		±20		ppm/%	
Voltage at timing current inputs	6, 7, 8, 9		±10		mV	See note 2
VFO output, 'low' state	2		0	0.2	V	
VFO output, 'high' state	2	+1.1	+1.3		V	$R_L \geq 10k\Omega$
Max. freq. of oscillation			0.5		MHz	
Binary inputs						
V_{in} to guarantee logic 'low'	10, 11			+0.6	V	See note 3
V_{in} to guarantee logic 'high'	10, 11	+2.4			V	
Input current	10, 11		0.05	0.25	mA	V_{in} = +3.0V
Phase comparator						
Differential I/P offset voltage	23, 24		±2		mV	V_{out} = 0V
Input bias current	23, 24		0.05	2.5	μA	V_{in} = 0V
Differential input resistance	23, 24		100		kΩ	
Common mode I/P voltage range	23, 24	±4			V	
Differential I/P to limit (AC)	23, 24		1.0	10	mV	See note 4
Output current	21, 22	±1.0	±2.0	±5.0	mA	I_{22} = 250μA
Current gain (pin 22 to pin 21)	21, 22	±4	±10		–	See note 5
Transconductance, O/P/diff.I/P	21,23,24	±100	±250		mA/V	See note 5
Output voltage, linear range	21	±5	±5.5		V	
Output current	21			±2	μA	I_{22} = 0
Phase comparator I/P 'low'	1	−4		−0.2	V	
Phase comparator I/P 'high'	1	+1.9		+5.3	V	
Auxiliary amplifier (SL650 only)						
Differential I/P offset voltage	13, 14		±2		mV	V_{out} = 0V
Input bias current	13, 14		.0.025	0.5	μA	V_{in} = 0V
Differential I/P resistance	13, 14	0.2	3		MΩ	
Common mode I/P voltage range	13, 14	±4			V	
Voltage gain (13–14) to 15	13,14,15	1000	5000		–	
Output voltage range	15	±4	±4.8		V	$R_L \geq 2k\Omega$
Output current limit	15	±4	±6.5	±12	mA	

NOTES

1. With a timing current of 60μA and f = 1kHz (C = 0.01μF, R = 100kΩ, supply voltages = ±6V), the temperature coefficient of frequency of the SL650C is typically ±2.5ppm/°C over the range 0°C to +40°C.
2. This voltage applies for timing currents in the range 20μA to 2mA and with the relevant input selected. In the unselected state the voltage is typically +0.6V.
3. The 'low' state is maintained when the inputs are open-circuited.
4. Limiting will occur earlier if the output (pin 21) voltage-limits first.
5. For a control current input to pin 22 of 250μA The sign of the transconductance is positive when the signal input is positive and the VFO output (or phase comparator input) is 'high'.

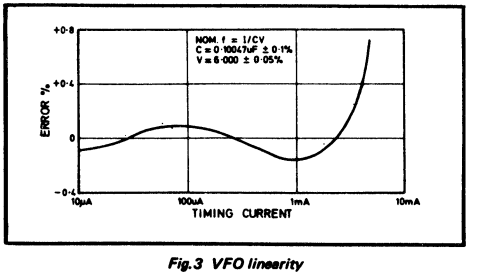


Fig.3 VFO linearity

ABSOLUTE MAXIMUM RATINGS

Supply voltages	± 7.5V
Storage temperature	−55° to +175°C
Operating temperature	−55° to +125°C
Input voltages	Not greater than supplies

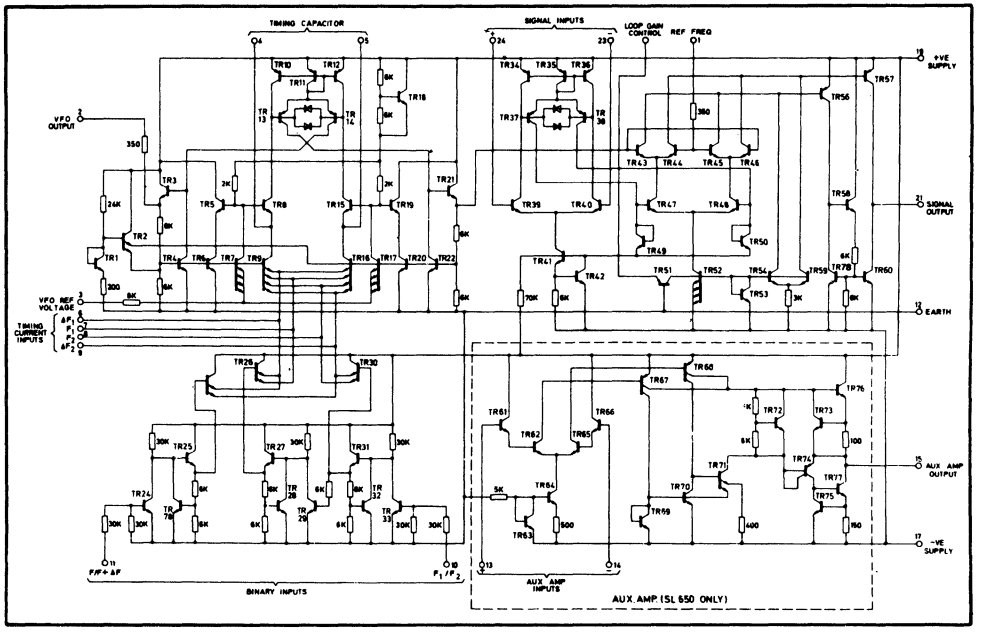


Fig. 2 Circuit diagram of SL650/SL651

OPERATING NOTES

Basic VFO Relationships

The VFO free-running frequency is inversely proportional to the value of the tuning capacitor C, connected to pins 4 and 5, and directly proportional to the VFO timing current (see Fig.4). Four current switches, controlled by TTL-compatible logic inputs on pins 10 and 11 select a combination of external resistors (connected to pins 6, 7, 8 and 9) which determine the VFO timing current. When both logic inputs are low, open-circuit, or connected to 0V however, then only the current switch associated with pin 7 is closed. The VFO timing current is then determined solely by the value of one resistor (R2 in Fig.4), and by the negative voltage connected to that resistor.

In this simplified configuration, as shown in Fig.5, the VFO frequency is determined by the relationship.

$$f = \frac{1}{CR} \cdot \frac{V_R}{V_3}$$

where f is in kHz, I in mA, V in volts, C in μF and R in kΩ.

If the timing resistor R is returned to the VFO negative supply (pin 3), then

$$V_R = V_3$$

$$\text{and } f = \frac{1}{CR}$$

Pin 3 is normally connected to the chip negative supply; if, however, pin 3 is connected to a separate negative supply then the VFO can be voltage-controlled, and the VFO frequency will be:

$$f = \frac{1}{CR} \cdot \frac{V-}{V_C}$$

where V– is the chip and timing resistor negative supply and V_C is the control voltage connected to pin 3

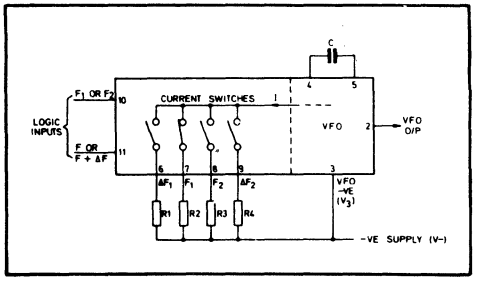


Fig.4 VFO and binary interface

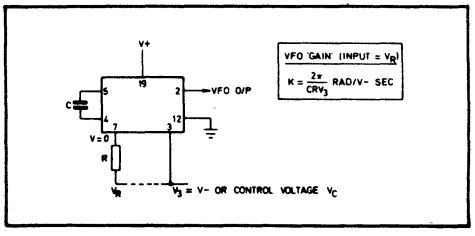


Fig.5 VFO basic configuration

The timing current I should be between 20μA and 2mA, corresponding to a value for R between 3kΩ and 300kΩ with supplies of ±6V. For accurate timing, CR should be greater than 5μs.

When the binary interface is used as shown in Fig.4, the VFO free-running frequency is dependent on the logic input states, as shown in Table 1.

Pin 10	Pin 11	Timing Pins	VFO Frequency
LO	LO	7	$\frac{1}{CR_2}$
LO	HI	6 & 7	$\frac{1}{CR_2}+\frac{1}{CR_1}$
HI	LO	8	$\frac{1}{CR_3}$
HI	HI	8 & 9	$\frac{1}{CR_3}+\frac{1}{CR_4}$

Table 1 Binary interface relationships

Phase Comparator

The phase comparator parameters are defined as follows (see Fig.6):

$$\text{Overall transconductance} = \frac{I_{21}}{V_{24}-V_{23}}$$

$$\text{Overall voltage gain} = \frac{V_{21}}{V_{24}-V_{23}}$$

The input amplifier will limit when the peak input ($V_{24}-V_{23}$) exceed ±5mV (typ.). It is recommended that R_L is kept below 5kΩ to avoid saturating the output and introducing de-saturation delays.

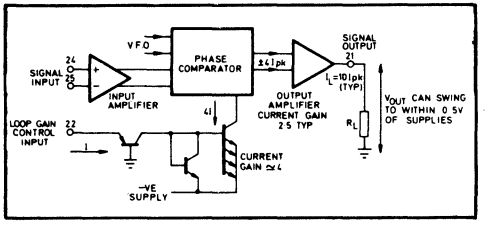


Fig.6 Phase comparator

PLESSEY
SEMICONDUCTORS

SL700 SERIES
OPERATIONAL AMPLIFIERS

SL701B&C SL702B&C SL751B&C

The SL701B, SL701C, SL702B, SL702C, SL751B and SL751C are monolithic, bipolar integrated circuit, high gain D-C amplifiers, intended primarily for use as operational amplifiers or in instrumentation applications. The SL701 basic circuit has an internal zener and provides an output symmetrical about earth when using the specified supply voltage. The SL702 basic circuit is non-symmetrical, with a direct output, but may be used with an external zener to permit a symmetrical output to be obtained at other supply voltages. The SL751 basic circuit has both the internal zener and a direct output and may be used in either application.

The SL701C, SL702C and SL751C differ from their equivalent devices with suffix B mainly in having higher maximum input offset voltage.

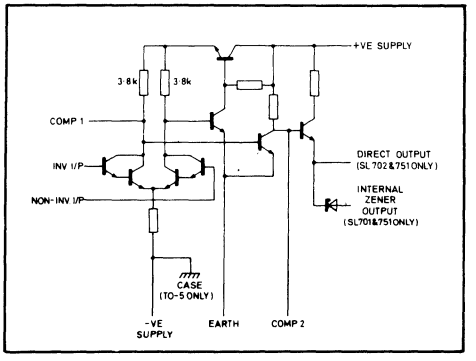


Fig. 2 Circuit diagram

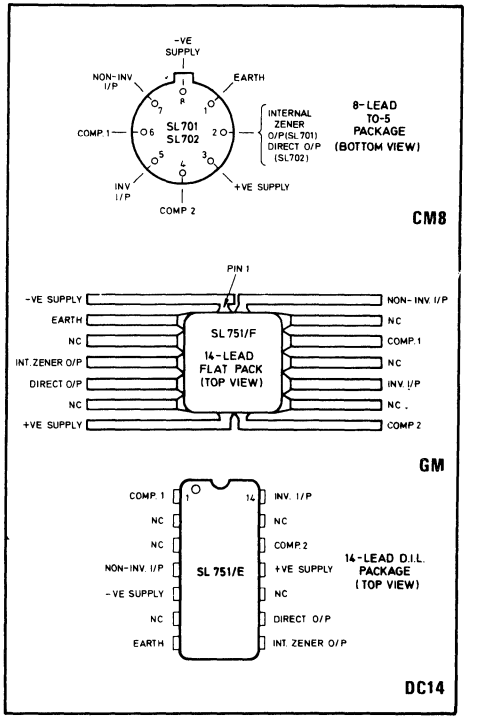


Fig. 1 Pin connections

ELECTRICAL CHARACTERISTICS

Test Conditions: (unless otherwise stated)

T_{amb} = +22°C ± 2°C

Supplies = +12V and −12V

A 6.0V zener is added to SL702 except where otherwise stated. (See test circuits)

Characteristic	Circuit	Value			Units	Test conditions	Test Fig. 3
		Min.	Typ.	Max.			
Open loop gain (Fig. 5)	All	66	70	78	dB	Frequency = 30kHz	A
Change of gain with temperature	All		±2		dB	Frequency = 20kHz −25°C to +100°C	A

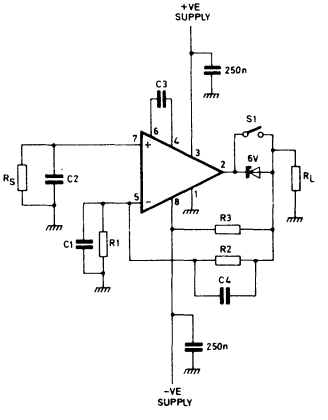
Characteristic	Circuit	Value			Units	Test Conditions	Test Fig. 3
		Min.	Typ.	Max.			
Open loop bandwidth (Fig. 5)	All	250	500		kHz	High frequency −3dB point	A
Output resistance	All		100		Ω	1kHz	A
Input resistance	All		100		kΩ	1kHz	A
180° phase shift frequency (Fig. 5)	All	20	35		MHz		A
Input offset voltage	SL701B, SL702B and SL751B			5	mV		1
Input offset voltage	SL701C, SL702C and SL751C			20	mV		1
Input offset voltage change with temperature	All		15		μV/°O		1
Input current	SL701B, SL702B and SL751B			1	μA		G & H
Input current	SL701C, SL702C and SL751C			3	μA		G & H
Input offset current	SL701B, SL702B and SL751B			0.3	μA		F
Input offset current	SL701C, SL702C and SL751C			1.8	μA		F
Input offset current change with temperature (see Note)	All		0.4		μA	−25°C to +100°C	F
Common mode rejection ratio (Fig. 4)	SL701B, SL702B and SL751B	70	80		dB	+0.5V to −3V input square wave	
Common mode rejection ratio (Fig. 4)	SL701C, SL702C and SL751C	60	80		dB	+0.5V to −3V input square wave	
Supply line rejection	All	60	70		dB	1.0V square wave on supply line	
Positive output clipping level (DC)	All	+3.9	+4.3		V		C
Negative output clipping level (DC)	All	−6.0	−6.5		V		C
Positive output clipping level (DC)	SL702B & C SL751B & C (direct O/P)	+ 9.9	+10.3		V	No external zener	C(S1 closed)
Negative output clipping level (DC)	SL702B & C SL751B & C (direct O/P)	0	−0.5		V	No external zener	C(S1 closed)
Positive supply line current	All	9.5	12	14.5	mA	Output at 0V (R3 ± 2% tolerance)	A
Negative supply line current	All	7.5	9	10.5	mA	Output at Ov (R3 ± 2% tolerance)	A
Spot noise	All		See Fig. 7			Open loop	

NOTE

Total change in offset current over specified range

Test reference	$R_S(\Omega)$	R_1 (kΩ)	R_2 (kΩ)	R_3 (kΩ)	R_L	*C_1 (μF)	C_2 (nF)	C_3	C_4 (pF)	Remarks
A (Fig. 5 & 10)	50	o/c	100	2.2	o/c	30	o/c	o/c	o/c	Open loop AC gain (Figs. 5 and 10)
B (Fig. 5)	50	o/c	100	2.2	o/c	30	o/c	33pF	o/c	Compensated open loop AC gain (Fig. 5)
C (Fig. 6 & 10)	50	1	99	2.2	o/c	o/c	o/c	33pF	o/c	Gain of 100 (Figs 6 and 10)
D (Fig. 6 & 10)	50	1	9	2.2	o/c	o/c	o/c	33pF	4.7	Gain of 10 (Figs. 6 and 10)
E (Fig. 8)	50	1	99	Varied	Varied	30	o/c	o/c	o/c	Negative swing/load resistance (Fig. 8)
F	100k	o/c	100	2.2	o/c	4	1	1nF	o/c	Input offset current
G	100k	o/c	s/c	2.2	o/c	4	1	1nF	o/c	Input current
H	s/c	o/c	100	2.2	o/c	4	o/c	1nF	o/c	Input current
I	s/c	o/c	s/c	2.2	o/c	4	o/c	1nF	o/c	Input offset voltage

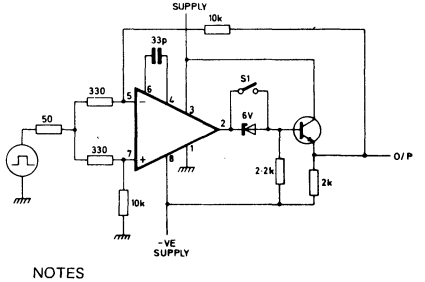
*C_1 should be a non-polarized tantalum or paper type.



NOTES

1. AMPLIFIER PIN CONNECTIONS SHOWN APPLY TO SL701 (S1 CLOSED) AND SL702 (S1 OPEN EXCEPT WHERE OTHERWISE STATED). FOR SL751 CONNECTIONS SEE FIG. 1.

Fig. 3 Test circuit



NOTES

1. THE 330Ω RESISTORS ARE MATCHED TO 0.02% AND THE 10kΩ RESISTORS ARE MATCHED TO 0.05%.
2. AMPLIFIER PIN CONNECTIONS SHOWN APPLY TO SL701 (S1 CLOSED) AND SL702 (S1 OPEN). FOR SL751 CONNECTIONS SEE FIG. 1.

Fig. 4 Common mode test circuit

The test circuit of Fig. 3 is used for measuring all electrical characteristics except common mode rejection. Component values for tests A to I using Fig. 3 are given in the following table.

Frequency Response and Feedback Stabilization

The typical gain/phase frequency response of the device is given in Fig. 5. When the external feedback connections are made the resultant loop gain must be cut at a mean rate of less than 9–10 db/octave. A single dominant time constant is often the simplest solution. For example, in the SL701 and similar amplifiers, a capacitor between pins 5

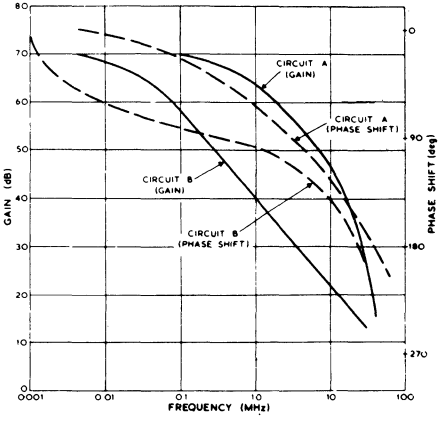


Fig. 5 Open loop gain and phase shift v frequency

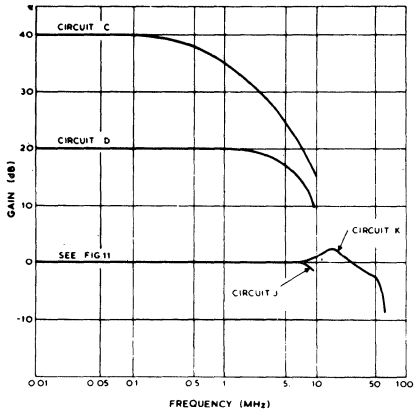


Fig. 6 Gain with feedback v frequency

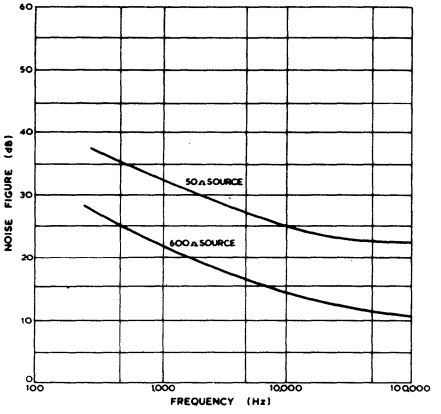


Fig. 7 Spot noise v frequency (open loop)

and 7 with a value between a few tens and a few hundred pF (depending on the feedback fraction) will give a suitable dominant high frequency cut-off. In general, however, when a particular feedback loop is designed, an appropriate stabilizing arrangement, to suit it, will be needed. Except when maximum bandwidth is required, a dominant lag provided by a 33 pF stabilizing capacitor will be found satisfactory for loop gains up to about 20 dB short of the full forward gain of the amplifier; gain curves for this configuration are given in Fig. 6.

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistance	80°C/W
Supply voltage (Fig. 11)	+ 14V and −14V
Output current	20mA
Input voltage (either input, opposite input at 0V)	+1V to − 10V.

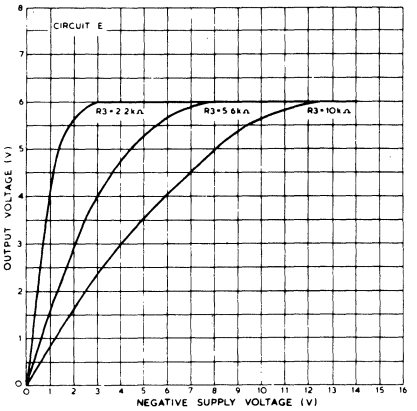


Fig. 8 Max. negative swing as a function of load resistance

Amplifier dissipation at different supply voltages

The curves assume zero load current is drawn from the output. Assuming that a resistor R_3 (zener bias resistor — Fig. 8) is connected between the output and the negative line, the total maximum dissipation will be obtained by adding the power term:

$$\frac{|-V|.|+V|}{R_3}$$

to the value obtained from Fig. 11.

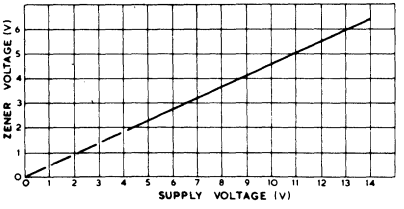


Fig. 9 Zener voltage v supply voltage for symmetrical output about earth

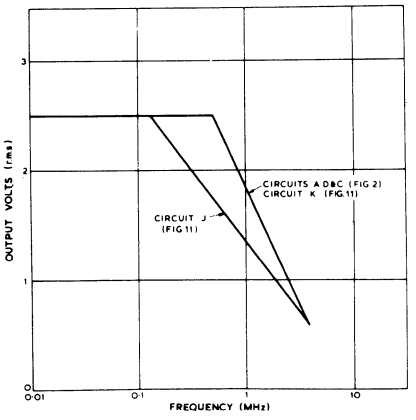


Fig. 10 Typical max. output v frequency

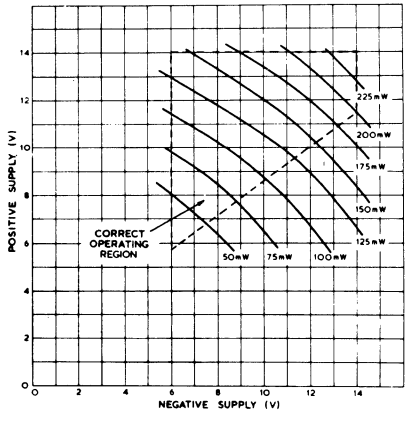


Fig. 11 Amplifier dissipation at different supply voltages

OPERATING NOTES

Lower Supply Voltages (SL702 and SL751 – with direct output)

The balance of the collector currents of the input transistors is maintained by an auxiliary internal feedback loop, enabling a range of supply voltages to be used, as shown in Fig. 9 and Fig. 11. Since the collector currents of the input transistor are controlled by a 3k Ω 'tail' resistor, the input base current and offset current will decrease and the input resistance will increase as the negative supply rail voltage is reduced. The open loop gain is also affected by this rail voltage and is virtually proportional to it. A reduction in the positive rail voltage does little except decrease various currents and voltages within the circuit; together with the negative supply this decreases the maximum available output level. In order to avoid internal limiting, the magnitude of the positive supply must not be very much lower than that of the negative supply; hence at levels less than the nominal ± 12 volts, attention must be paid to the tolerance of the supplies. Typical characteristics for operation under these conditions are given below.

Test conditions: Supply voltages +6V and −6V
Ambient temperature = +20°C
External zener = 2.7V
Test circuits as above

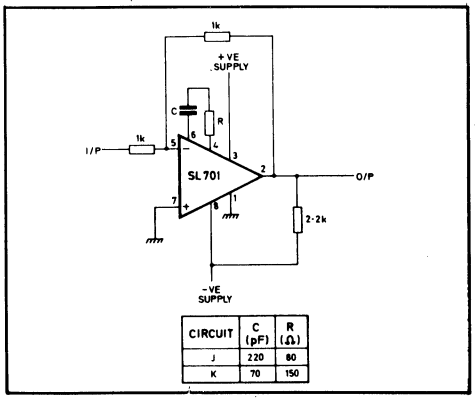


Fig. 12 Unity gain test circuit (tests J and K)

Characteristic	Value	Units	Test conditions
Open loop gain	62	dB	
Input resistance	200	kΩ	
Max. input base current (SL702B, SL751B) (see note)	500	nA	
Max. input base current (SL702C, SL751C) (see note)	1.5	μA	
Max. input offset current (SL702B, SL751B) (see note)	150	nA	
Max. input offset current (SL702C, SL751C) (see note)	900	nA	
Supply current (+ve)	8	mA	R_3 = 1.2k Ω ± 2%
Supply current (−ve)	6.5	mA	R_3 = 1.2k Ω ± 2%
Output clipping level (+ve)	2	V	
Output clipping level (−ve)	3	V	

NOTE

These figures are not guaranteed, but indicate relation to full specification at ± 12V supplies.

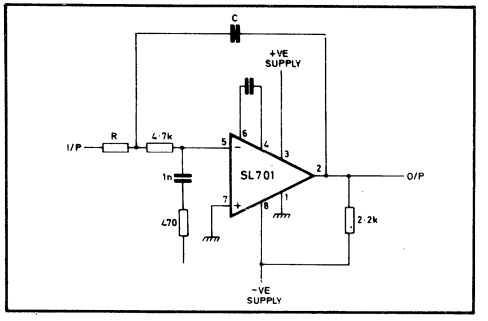


Fig. 13 Integrator circuit

Unity Gain

For unity gain more than one method of compensation may be employed; the simplest is shown in Fig. 12. The disadvantages of the method suggested are that some peculiar overload characteristics may be observed at high frequencies and the maximum signal output without limiting is lower than at higher circuit gains. Circuit K on Fig. 12 gives compensation for wideband response, allowing approximately 1 dB gain rise above the gain at low frequencies. For maximum signal handling, but reduced noise performance, the method as indicated in Fig. 13 may be used.

DEFINITION OF TERMS

Decibel (dB) Units Refers to the conventional expression of a voltage ratio in logarithmic units, i.e. 20 $\log_{10} V_2/V_1$ dB.

Open Loop Bandwidth The frequency at which the open loop gain falls by 3 dB (factor $\sqrt{2}$) below the value at 1kHz.

Output Resistance The ratio of change in output voltage to the change in output current, measured at the output terminal, under open loop conditions and with zero volts d.c. output level.

Input Resistance The resistance between the input terminals, equivalent at low frequencies to the resistance between input and earth with the other input earthed.

180° Phase Shift Frequency The lowest frequency at which the output phase is shifted 180°, relative to the low frequency value, compared to the input signal under open loop conditions with no compensation capacitors.

Input Offset Voltage The voltage between the input terminals to set the DC output voltage to zero.

Input Current The base current of either input transistor when the DC output voltage is set to zero.

Input Offset Current The difference between the input currents when the output quiescent voltage is zero.

Common mode rejection The ratio between the common mode signal and a differential signal producing the same magnitude of output (dB units).

Supply Line Rejection The ratio between the supply line signal and a differential input producing the same magnitude of output (dB units).

Output Clipping Levels The DC voltage at the output terminal when a voltage of ± 0.1V is applied between the input terminals (Gain x 100, circuit C).

PLESSEY
SEMICONDUCTORS

SL700 SERIES
OPERATIONAL AMPLIFIERS

SL748A&C
PRECISION OPERATIONAL AMPLIFIER

The SL748 is a monolithic Precision Operational Amplifier. It is an excellent choice when performance versus cost trade-offs are possible between super beta or FET input operational amplifier and low cost general purpose operational amplifiers. The low offset and bias currents of the SL748 improve system accuracy in applications such as long term integrators, sample and hold circuits and high source impedance summing amplifiers. Even though the input bias current is extremely low, the SL748 maintains full ±30V differential voltage range. The internal construction utilizes isothermal layout and special electrical design to maintain system performance despite variations in temperature or output load. High common mode input voltage range, latch-up protection, short circuit protection and simple frequency compensation make the device versatile and easy to use.

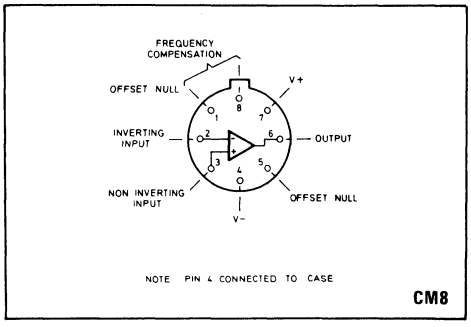


Fig. 1 Pin connections

FEATURES

- Low Offset Voltage and Offset Current
- Low Offset Voltage and Current Drift
- Low Input Bias Current
- Low Input Noise Voltage
- Large Common-mode and Differential Voltage Ranges

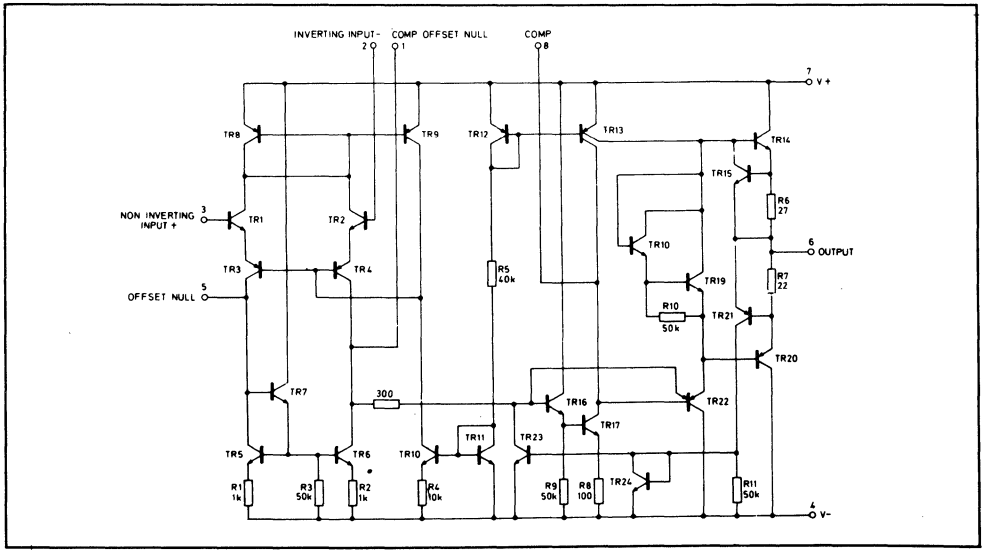


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS (SL748A)

Test conditions (unless otherwise stated)
$V_S = \pm 15V$
$T_A = +25°C$
$C_C = 30pF$

Characteristic	Value			Units	Condition
	Min.	Typ.	Max.		
Input offset voltage		1.0	5.0	mV	$R_S \leqslant 10k\Omega$
Input offset current		20	200	nA	
Input bias current		80	500	nA	
Input resistance	0.3	2.0		MΩ	
Input capacitance		2.0		pF	
Offset voltage adjustment range		±15		mV	
Large signal voltage gain	50000	200000		V/V	$R_L \geqslant 2k\Omega$ $V_{OUT} = \pm 10V$
Output resistance		75		Ω	
Output short-circuit current		25		mA	
Supply current		1.9	2.8	mA	
Power consumption		60	85	mW	
Transient response (voltage follower, gain of 1)					$V_{IN} = 20mV$, $C_C = 30pF$, $R_L = 2k\Omega$, $C_L \leqslant 100pF$
Risetime		0.3		μs	
Overshoot		5.0		%	
Slew rate (voltage follower, gain of 1)		0.5		V/μs	$R_L \geqslant 2k\Omega$, $C_C = 30pF$
Transient response (voltage follower, gain of 10)					$V_{IN} = 20mV$, $C_C = 3.5pF$, $R_L = 2k\Omega$, $C_L \leqslant 100pF$
Risetime		0.2		μs	
Overshoot		5.0		%	
Slew rate (voltage follower, gain of 10)		5.5		V/μs	$R_L \geqslant 2k\Omega$, $C_C = 3.5pF$
The following specifications apply for $-55°C \leqslant T_A \leqslant +125°C$					
Input offset voltage		1.0	6.0	mV	$R_S \leqslant 10k\Omega$
Input offset current		10	200	nA	$T_A = +125°C$
		50	500	nA	$T_A = -55°C$
Input bias current		0.03	0.5	μA	$T_A = +125°C$
		0.3	1.5	μA	$T_A = -55°C$
Input voltage range	±12	±13		V	
Common mode rejection ratio	70	90		dB	$R_S \leqslant 10k\Omega$
Supply voltage rejection ratio		30	150	μV/V	$R_S \leqslant 10k\Omega$
Large signal voltage gain	25000			V/V	$R_L \geqslant 2k\Omega$, $V_{OUT} = \pm 10V$
Output voltage swing	±12	±14		V	$R_L \geqslant 10k\Omega$
	±10	±13		V	$R_L \geqslant 2k\Omega$
Supply current		1.5	2.5	mA	$T_A = +125°C$
		2.0	3.3	mA	$T_A = -55°C$
Power consumption		45	75	mW	$T_A = +125°C$
		60	100	mW	$T_A = -55°C$

ELECTRICAL CHARACTERISTICS (SL748C)

Test conditions (unless otherwise stated)
$V_S = \pm 15V$
$T_A = +25°C$
$C_C = 30pF$

Characteristic	Value			Units	Condition
	Min.	Typ.	Max.		
Input offset voltage		2.0	6.0	mV	$R_S \leqslant 10k\Omega$
Input offset current		20	200	nA	
Input bias current		80	500	nA	
Input resistance	0.3	2.0		MΩ	
Input capacitance		2.0		pF	
Offset voltage adjustment range		±15		mV	
Large signal voltage gain	20000	150000		V/V	$R_L \geqslant 2k\Omega$, $V_{OUT} = \pm 10V$
Output resistance		75		Ω	
Output short-circuit current		25		mA	
Supply current		1.9	2.8	mA	
Power consumption		60	85	mW	
Transient response (voltage follower, gain of 1)					$V_{IN} = 20mV$, $C_C = 30pF$, $R_L = 2k\Omega$ $C_L \leqslant 100pF$
Risetime		0.3		μs	
Overshoot		5.0		%	
Slew rate (voltage follower, gain of 1)		0.5		V/μs	$R_L \geqslant 2k\Omega$, $C_C = 30pF$
Transient response (voltage follower, gain of 10)					$V_{IN} = 20mV$, $C_C = 3.5pF$, $R_L = 2k\Omega$, $C_L \leqslant 100pF$
Risetime		0.2		μs	
Overshoot		5.0		%	
Slew rate (voltage follower, gain of 10)		5.5		V/μs	$R_L \geqslant 2k\Omega$, $C_C = 3.5pF$
The following specifications apply for $0°C \leqslant T_A \leqslant +70°C$					
Input offset voltage			7.5	mV	$R_S \leqslant 10k\Omega$
Input offset current			300	nA	
Input bias current			800	nA	
Input voltage range	±12	±13		V	
Common mode rejection ratio	70	90		dB	$R_S \leqslant 10k\Omega$
Supply voltage rejection ratio		30	150	μV/V	$R_S \leqslant 10k\Omega$
Large signal voltage gain	15000			V/V	$R_L \geqslant 2k\Omega$, $V_{OUT} = \pm 10V$
Output voltage swing	±12	±14		V	$R_L \geqslant 10k\Omega$
	±10	±13		V	$R_L \geqslant 2k\Omega$
Power consumption		60	100	mW	

ABSOLUTE MAXIMUM RATINGS

Supply voltage	±22V (SL748A) ±18V (SL748C)
Internal power dissipation	500mW
Differential input voltage	±30V
Input voltage	±15V
Storage temperature range	−65°C to +150°C
Operating temperature range	
Military (SL748A)	−55°C to +125°C
Commercial (SL748C)	0°C to 70°C
Lead temperature (soldering 60 seconds)	300°C
Output short-circuit duration	Indefinite

PLESSEY
SEMICONDUCTORS

SL1000 SERIES
TELECOMMUNICATIONS CIRCUITS

SL1001A & B
MODULATOR/DEMODULATOR

The SL1001A and B are bipolar monolithic integrated circuit double balanced modulators, designed primarily for use in telephone transmission equipment, but equally suitable for any application where the modulation function is required.

The devices employ conventional 'tree' configuration multiplier circuits. Careful design of the circuit layout results in low carrier and signal leak levels, with high dynamic range and good linearity. Internal bias is provided, allowing direct balanced transformer input, or single-ended capacitor drive.

A two-stage common collector output structure is used to provide a low output impedance.

A pair of diodes is included to provide optional carrier input limiting.

FEATURES

- High Carrier and Signal Suppression: 50dB
- Unity Conversion Gain
- Low Noise Level: −112dBmp
- High Intermodulation Suppression: 58dB
- Low Supply Current: 4mA
- Diodes included for Limiting

APPLICATIONS

- Telephone Transmission Equipment
- Suppressed Carrier and Amplitude Modulation
- Synchronous Detection
- FM Detection
- Phase Detection

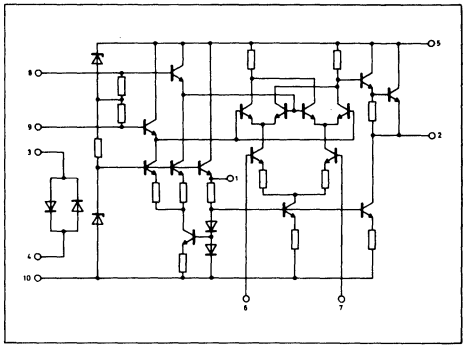


Fig.1 Circuit diagram

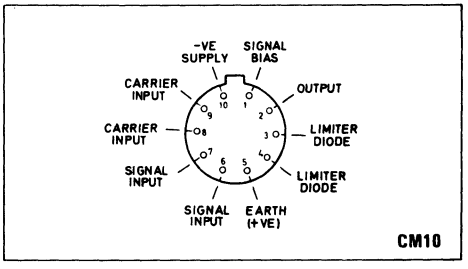


Fig.2 Pin connections (bottom)

QUICK REFERENCE DATA

Supply Voltage	−15V
Supply Current SL1001A	6mA
Supply Current SL1001B	4mA
Carrier Level	125mVrms (MIN.)
Signal Level	Up to 600mVrms
Output Current SL1001A	3.5mA peak (TYP.)
Output Current SL1001B	2.0mA peak (TYP.)
Temperature Range	−25°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 22°C ± 2°C
Circuit ref: Figs.3 and 4

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max		
Conversion gain	−1	0	+1	dB	
Signal input impedance		150		kΩ	Pins 6 & 7
Carrier input impedance	7	10	13	kΩ	Pins 8 & 9
	3.3	5	6.7	kΩ	Pins 8 & 5 or 9 & 5
Output impedance					
SL1001A		12		Ω	Pin 2
SL1001B		25		Ω	Pin 2
Signal suppression	20	50		dB	Signal 170mV, Carrier 500mV
Carrier suppression	20	40		dB	
2nd harmonic suppression		40		dB	
Carrier compression			0.1	dB	For ± 3dB on 500mV
Supply line suppression	50			dB	Line impedance 500Ω
Sig. and carrier band width	200			kHz	
Carrier level	125			mVrms	
Signal level			600	mVrms	
Output current					
SL1001A		3.5		mApk	
SL1001B		2.0		mApk	
Noise level		−112	−105	dBmp	Weighted speech band
Intermod. products		−58		dB	Signals 2 X 170mV
Gain stability		0.12		dB	+5°C to +55°C
		0		dB	± 10% supply
Adjusted carrier suppression		70		dB	See Fig.5

ABSOLUTE MAXIMUM RATINGS

Supply voltage (via 820Ω)	−30V
Storage temp. range	−55°C to + 175°C
Free air operating temp. range	−40°C to + 150°C

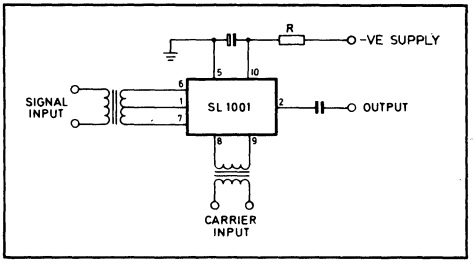


Fig.3 Transformer input

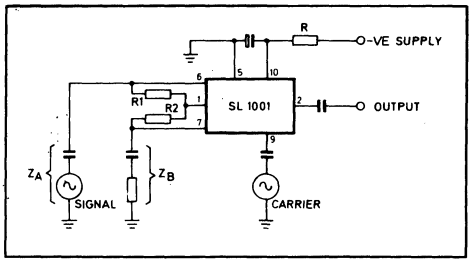


Fig.4 Unbalanced input

OPERATING CONDITIONS (see Figs.3 and 4)

Parameter	Value	Units	Condition
Supply voltage	−15	V	Pin 10
Supply current			
SL1001A	6	mA	
SL1001B	4	mA	
Input bias current	5	μA	Pins 6 & 7
Dynamic resistance	8	kΩ	Pins 5 to 10
Output quiescent voltage	−3	V	Pins 2 to 5
Temperature range	−25 to +125	°C	

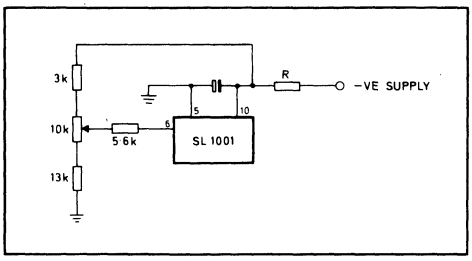


Fig.5 Carrier suppression adjustment

OPERATING NOTES

1. A resistance in series with the supply (Pin 10) is usually advisable, to improve the supply rejection and reduce the circuit voltage.
2. For good carrier suppression, the signal input bias resistors should be equal and have a value less than 5kΩ
3. For improved intermodulation suppression, Pin 1 may be decoupled, preferably with a 100Ω resistor in series with Pin 1.

   If Pin 1 is not decoupled, noise is optimised when an unbalanced drive is used, by providing equal source impedances for Pins 6 and 7.
4. Low leakage input capacitors are advisable for the input connections to avoid inducing carrier or signal leakage.
5. Carrier suppression may be improved by using the circuit of Fig.5, and adjusting for minimum leakage.

PLESSEY
SEMICONDUCTORS

SL1000 SERIES
TELECOMMUNICATIONS CIRCUITS

SL1021 A & B
CHANNEL AMPLIFIER

The SL1021 A and B are bipolar monolithic integrated circuit amplifiers designed for use as channel amplifiers in telephone transmission equipment and satisfy the requirements of the British Post Office channel translating apparatus (RC5467).

The two variants A and B are distinguished by guaranteed output levels of +10dBm and +13dBm, respectively, other parameters being identical.

The main feature of these devices is the provision of a temperature-stable DC operated remote gain control facility having an adjustable range of control.

The connections provided allow a variety of uses, including fixed gain amplification with various feedback configurations.

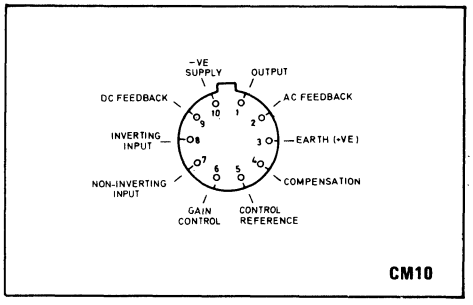


Fig. 1 Pin connections

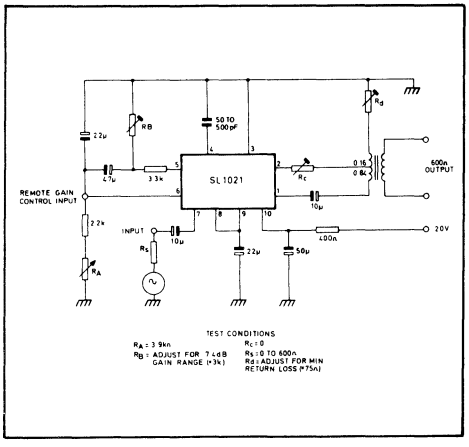


Fig. 2 SL1021 test circuit and typical application

FEATURES

- Up to +13dBm O/P into 600Ω (Class A)
- Temperature insensitive remote DC gain control
- Non-interactive adjustment of:
  - Gain
  - Gain Range
  - Output Return Loss
- 1:1 600Ω Transformer output can be optimized for low inductance using 2-element filter configuration
- Power Bandwidth: 150kHz (fixed gain, Fig. 4)
- Small Signal gain Bandwidth: 3MHz (see Fig. 4)

QUICK REFERENCE DATA

Supply Voltage	−20V (via 400Ω)
Supply Current	9mA
Gain Control Current	0.5mA
Temperature Range	−25°C to +125°C

APPLICATIONS

- Telephone Communications
- Channel Group Translation Equipment
- Radio – communications
- Small Signal Processing

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} 22°C ± 2°C

These characteristics are those obtained using the test circuit of Fig.1, the gain range and output impedance being adjusted as indicated.

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Gain (reference gain G)	24.5	26	27.5	dB	
Gain/R_S			28	dB	R_S = 600Ω to 3kΩ
Gain range		7.4		dB	Adjusted
Gain law					
R_A = 125Ω	3.9	4.1	4.3	dB	Relative to G
R_A = 9kΩ	−3.5	−3.3	−3.1	dB	
Gain/temperature	−0.1		+0.1	dB	Relative to G, T = 10°C to 45°C
Gain/V_S			0.1	dB	V_S = −20V ± 1V
Distortion					
2nd harmonic			−36	dBm0	At 10dBm output
3rd harmonic			−45	dBm0	
Overload					
SL1021A	10	13		dBm	Class A operation
SL1021B	13	15		dBm	
Noise			−76	dBmP	Proportional to G
Output impedance		600		Ω	Adjusted
Return loss	20			dB	250Hz to 3.4kHz
Input impedance	10			kΩ	Variable with R_A and R_S
Gain at reduced V_S	25.5			dB	V_S = −17.5V See Fig.1
Overload at reduced V_S	7			dBm	V_S = −17.5V
Gain control interaction between channels (change in gain for 3.3 mA current change)			0.25	dB	Equivalent to 11 channels, Common R_A earth return
Frequency response	240		3400	Hz	±0.05dB ref. 800Hz
Bandwidth			100	kHz	C_C = 50pF

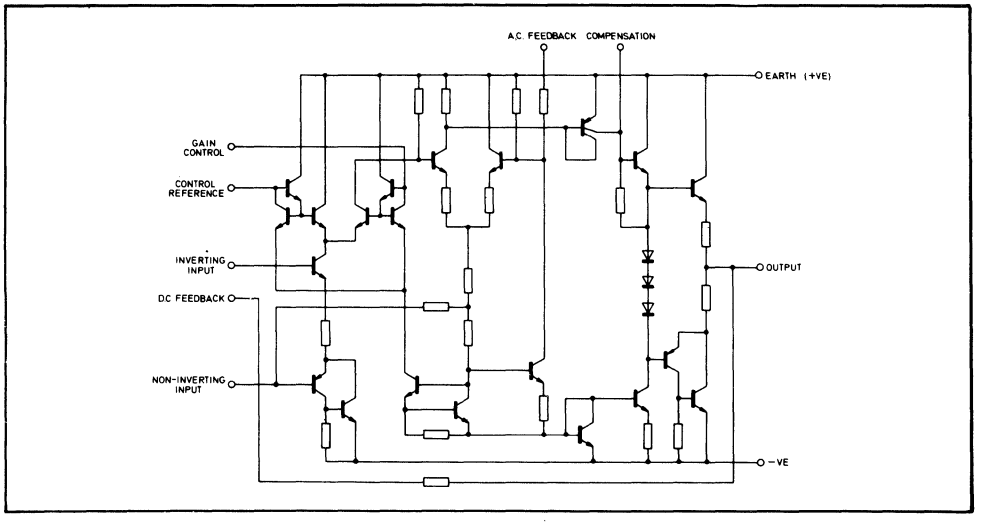


Fig. 3 SL1021 equivalent circuit

OPERATING CONDITIONS (See Fig. 1)

Parameter	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		9	11.0	mA	$R_A = 0$
		7.0		mA	$R_A = 11k\Omega$
Supply voltage		−20		V	Via 400Ω
Supply voltage on chip		−17		V	Pin 10
Supply maximum			−23	V	Pin 10
Control current		0.5		mA	$R_A = 0$
		0.26		mA	$R_A = 10k\Omega$
Control current change			0.3	mA	$R_A = 0$ to $11k\Omega$
Operational temp.	−25		+125	°C	
Fixed gain application (see Fig. 4)					
Optimum load		100		Ω	
Power output		20		mW	Class AB
Power bandwidth		150		kHz	10mW
Gain		20		dB	Values as Fig. 4
Frequency response		3		MHz	Small signal

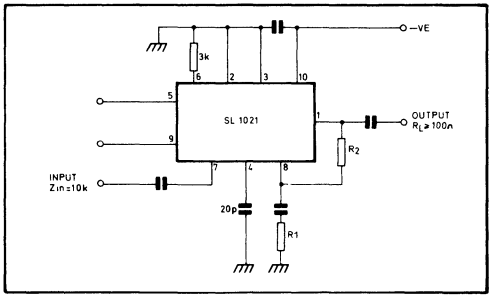


Fig. 4 Fixed gain amplifier, Class A or AB

OPERATING NOTES

1. The control decoupling capacitors should be of a low leakage type.
2. Other values of control resistors are possible if other gains/gain ranges are required. However, the parallel resistance to earth from pins 5 and 6 should be ⩽8kΩ at all settings.
3. If the control resistance is increased or open circuited, the amplifier gain will decrease to zero. (See Fig. 4 for fixed gain use).
4. The compensation capacitor C_c can be increased to reduce the frequency response at the expense of the power bandwidth.
5. The gain may be increased from the value of Fig. 1 (26dB nominal) by increasing R_c, the gain increase being given by:

$$\frac{R_c + 8.5}{8.5} \pm 20\%$$

where R_c is in kΩ.

Because of temperature coefficient mismatch between R_C and internal resistors, the gain stability may be degraded with temperature.

6. The case is connected to pin 10 (−ve supply). To avoid damage to the device when operating with a positive earth system, care should be taken to prevent the case from becoming earthed.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (via 400Ω)	−30V
Storage temp. range	−55°C to +175°C
Free air operating temp. range	−40°C to +130°C

PLESSEY
SEMICONDUCTORS

SL1000 SERIES
TELECOMMUNICATIONS CIRCUITS

SL1025B
BALANCED MODULATOR

The SL1025B is a bipolar integrated circuit intended for use as a double balanced modulator. Although primarily designed for FDM telephone transmission equipment as a channel modulator/demodulator, it is equally suitable for use as an analogue multiplier.

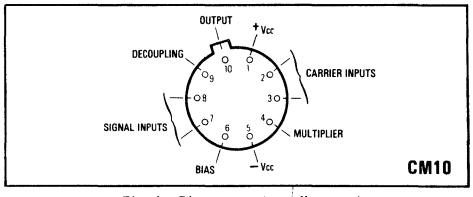


Fig. 1 Pin connections (bottom)

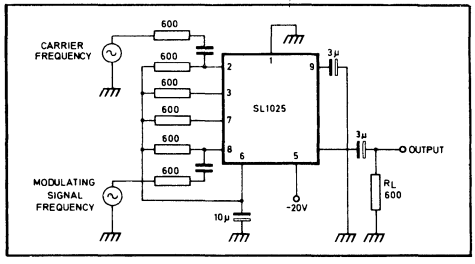


Fig. 2 Modulator using single supply voltage

FEATURES

- High Carrier and Signal Suppression: 50dB typ.
- High Conversion Gain: 5dB typ.
- Low Supply Current: 2.5mA max.
- Can be used as an Analogue Multiplier.

APPLICATIONS

- Telephone Transmission Equipment
- Suppressed Carrier and Amplitude Modulation
- Synchronous Detection
- AC and DC Multipliers
- Automatic Gain Control
- Frequency Doublers

QUICK REFERENCE DATA

- Supply Voltage 20V
- Operating Temperature Range −20°C to +85°C
- Supply Current 2mA typ

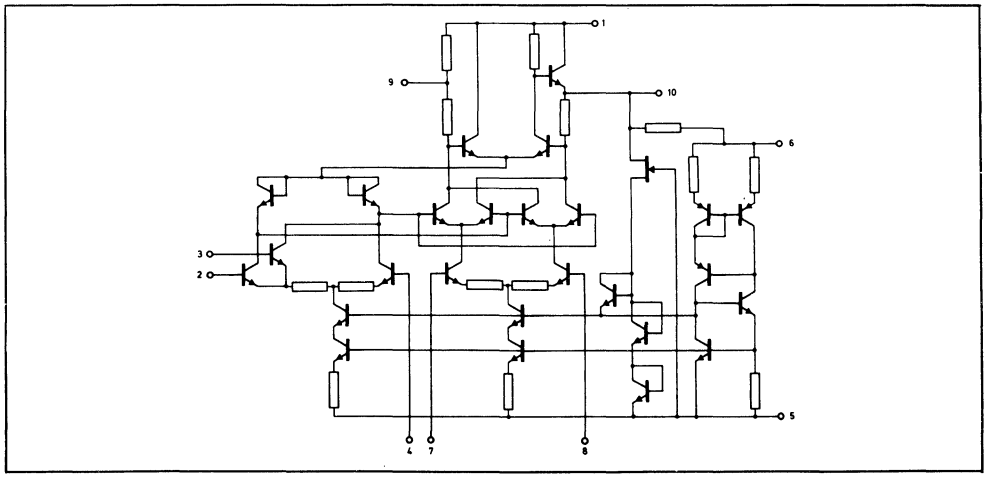


Fig. 3 Circuit diagram of SL1025

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Supply voltages: ±10V
T_A: +25°C
Carrier frequency: 130kHz
Signal frequency: 25kHz
Circuit ref.: Fig. 2.

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Total supply voltage operating range	12		30	V	Pin 1 (pos), pin 5 (neg.)
Supply current		2	2.5	mA	Vcc=±10V
Input bias current			2	μA	Inputs 2, 3
			2	μA	Inputs 2, 4
			4	μA	Inputs 7, 8
Quiescent output voltage	+5.4	+6.2	+6.8	V	Pin 10, no signal or carrier inputs
Differential output voltage		25	100	mV	Pins 9, 10
Reference voltage		+2.5		V	Pin 6
Input impedance		30		kΩ	Input 2, 3
		300		kΩ	Inputs 2, 4
		150		kΩ	Inputs 7, 8
Output voltage swing	1	1.3		Vp-p	Pin 10
Output impedance		3	10	Ω	Pin 10
Conversion gain	4.5	5.0	5.5	dB	Output 140mV, carrier 150mV
Signal suppression	35	50		dB	Signal 200mV, 25kHz
Carrier suppression	35	50		dB	Carrier 200mV, 130kHz
Second harmonic suppression		75		dB	Signal, carrier 200mV
Intermodulation products		−60		dB	Signal, carrier 200mV

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	30V
Differential input voltage	±5V
Power dissipation (70°C)	300mW
Storage temperature	−55°C to 150°C
Operating temperature	−20°C to +85°C

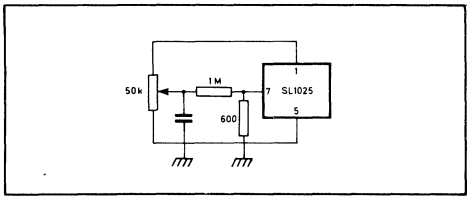


Fig. 4 Adjusting carrier leakage of SL1025

APPLICATIONS

Modulator

The basic circuit of a double sideband, suppressed carrier, double balanced modulator is shown in Fig. 2. When separate positive and negative supplies are used pin 6 is left open circuit; the input coupling capacitors are no longer required and inputs are referred to 0V.

To ensure the modulated output has an amplitude dependent only on the signal input the carrier is internally amplitude limited. A carrier input of approximately 150mV RMS is normally sufficient to allow this.

Conversion gain is substantially independent of temperature, supply voltage and frequency up to 1MHz. Carrier leakage increases substantially over 1MHz and it becomes necessary to provide some form of nulling adjustment. A suitable circuit is shown in Fig. 4.

Output levels are chosen as a compromise between distortion at high levels and leakage or noise at low levels. Outputs in the region of 150mV RMS are normally used. If the circuit is required to drive low impedance loads (300 ohms and below) it is advisable to connect a 15k resistor externally between pins 5 and 10.

Multiplier

To use the SL1025 as a multiplier then inputs 2 and 4 become 'X' inputs; 7 and 8 are the 'Y' inputs. The Y channel has slightly lower offset voltage and lower distortion but the performance is still sufficient to build a four quadrant DC multiplier with less than 1% overall distortion.

The Scale Factor (approximately 3.2) is virtually independent of supply voltage, temperature and frequency up to 1MHz. Typical transfer characteristics are shown in Fig. 5.

To obtain complementary outputs for driving an operational amplifier it is permissable to use pin 9 in addition to the normal output, pin 10. It is generally necessary to add external resistors between pin 9 and the voltage supplies to improve linearity and voltage swing.

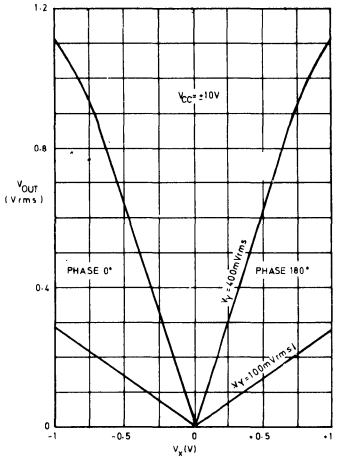


Fig. 5 Transfer characteristics in multiplier mode

PLESSEY
SEMICONDUCTORS

TELECOMMUNICATIONS
CIRCUITS

SL1030C

200MHz WIDEBAND AMPLIFIER

The SL1030 is a silicon integrated circuit designed for use as a general purpose very wideband amplifier. External components enable users to tailor the characteristics of the amplifier for particular applications. The gain can be selected between 20 and 60dB; the input impedance can be 50Ω, 75Ω or 1kΩ, and the compromise between current consumption and output swing can be selected by the external components.

A regulator is provided on the chip, enabling supply voltages from 8 to 15 volts to be used with no variation in characteristics. Alternatively, the regulator can be bypassed and supplies from 4.0 to 10 volts used.

The amplifier is protected against damage from input voltage transients and is stable when driving capacitive and inductive loads.

FEATURES

- Bandwidth up to 200 MHz
- Low Noise
- Single Supply
- Input Impedance Adjustable – 50Ω, 75Ω or 1kΩ
- Gain Programmable between 20dB and 60dB
- Drives Capacitive or Inductive Loads

APPLICATIONS

- Wideband Pulse Amplifiers
- Frequency Selective IF Amplifiers
- Low Noise Preamplifiers

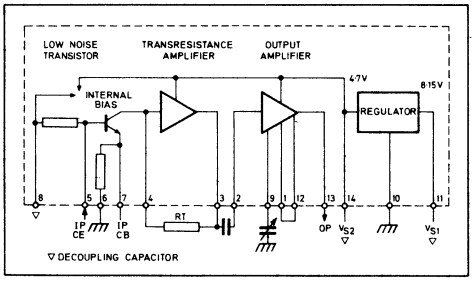


Fig. 1 General schematic

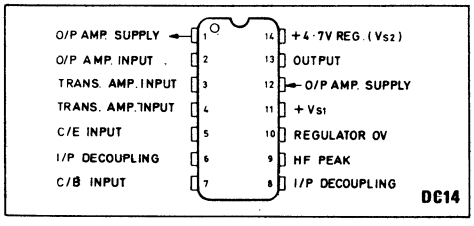


Fig. 2 Pin connections (top)

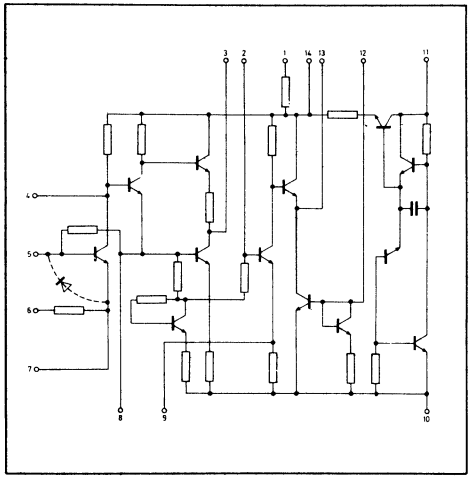


Fig. 3 Circuit diagram

QUICK REFERENCE DATA

Supply Voltage	+4V to +15V
Supply Current at V_S = 10V	20 mA (Typ.)
Voltage Gain at 100 MHz	40dB (Typ.)
Noise Figure at 100 MHz, R_S = 50Ω	3dB (Typ.)
Second Order Intermodulation Distortion	–50dB (Typ.)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} 22°C ± 2°C
V_{S1} 10V
R_1 = 1 kilohm
R_2 = 32 kilohms

Characteristic	Test Cct.	Value Min.	Value Typ.	Value Max.	Units	Conditions
Voltage gain	A	28	30	32	dB	f = 100 MHz
	B	37	40	43	dB	,, ,, ,,
Gain flatness			± 0.5		dB	f = 10 kHz to 150 MHz (Note 1)
Noise figure	A		6.5	8.0	dB	f = 100 MHz, R_S 50Ω
	B		3.0	4.5	dB	
Gain compression	A		0.2	1.0	dB	f = 100 MHz, load impedance = 50Ω P_{out} = 0dBm
Output voltage	B		1		V pk/pk	f = 10 MHz, load impedance = 100Ω
Rise time	B		3		ns	V_{out} = 1.0 V pk/pk
Input VSWR	A		1.2			f = 10 kHz to 150MHz w.r.t. 50Ω
Supply current			20	30	mA	V_{S1} = 10V or V_{S2} = 5V
Regulation $\Delta V_{S2}/\Delta V_{S1}$			1	5	%	V_{S1} = 10V to 15V
Intermodulation distortion						
2nd order	A		−50		dB*	P_{out} = 0dBm (Note 2), V_{S2} = 10V
3rd order	A		−60		dB*	
Harmonic distortion						
2nd harmonic	A		−30		dB*	f = 100 MHz, P_{out} = 0dBm,
3rd harmonic	A		−40		dB*	V_{S2} = 10V, R_L = 50Ω
Input impedance						
Common base			16		Ω	f < 10 MHz
Common emitter			1		kΩ	,, ,,

NOTES

1. The gain flatness is dependent on layout and on the value of the peaking capacitor. See OPERATING NOTES for details.
2. In each of two tones at 10 and 10.5 MHz, R_L = 50Ω

* Referred to output.

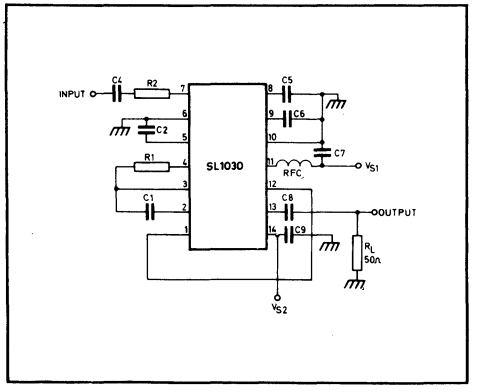


Fig. 4 Test circuit A — common base

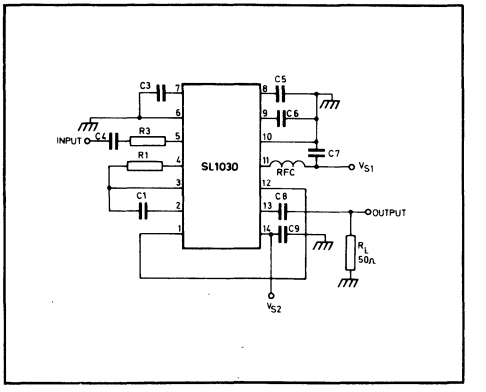


Fig. 5 Test circuit B — common emitter

TYPICAL ELECTRICAL CHARACTERISTICS

The following conditions apply to the characteristics given in Figs. 6 to 16 unless otherwise stated:

Free air temperature	22°C
Load resistance	50Ω
R_T	1 kΩ

Intermodulation products (Fig. 6) are measured with specified output power in each of two tones at 10 MHz and 10.5 MHz.

The values for C_P quoted in Figs. 12 and 13 were selected with R_L = 50Ω but will vary with load impedance and circuit layout.

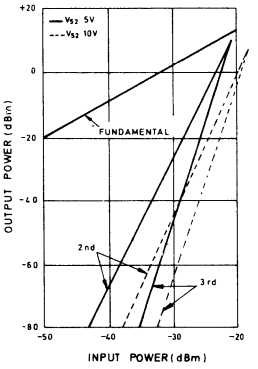


Fig. 6 Intermodulation products

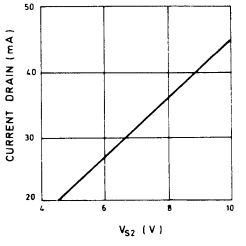


Fig. 7 Supply current v. unreg. supply voltage

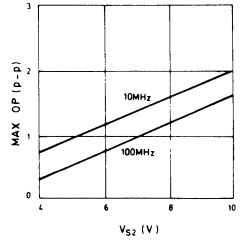


Fig. 8 Max o/p voltage v. unreg. supply voltage

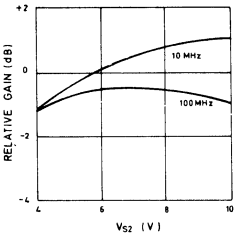


Fig. 9 Common base gain v. unreg. supply voltage

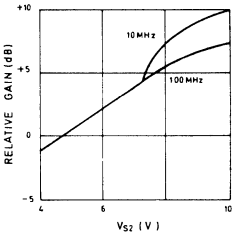


Fig. 10 Common emitter gain v. unreg. supply voltage

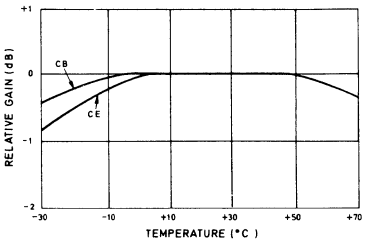


Fig. 11 Gain v. temperature

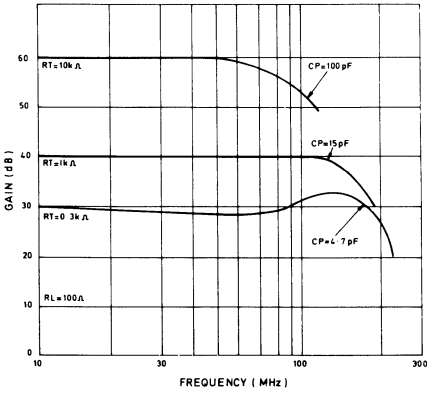


Fig. 12 Common emitter gain v. frequency

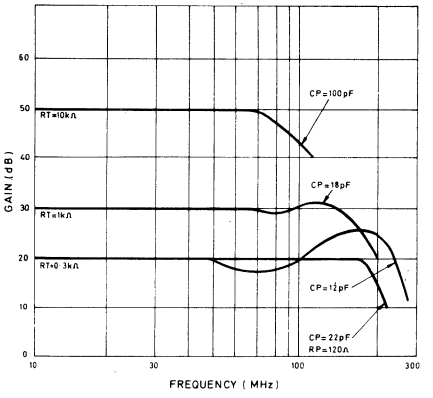


Fig. 13 Common base gain v. frequency

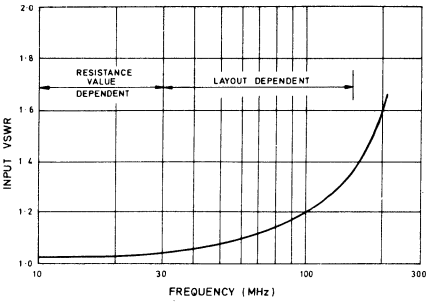


Fig. 16 Input VSWR v. frequency

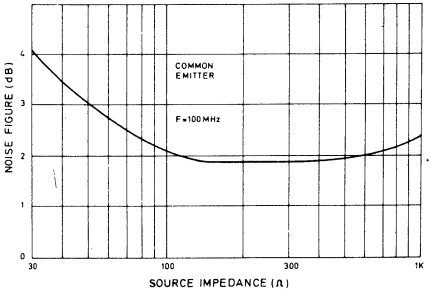


Fig. 14 Noise figure v. source impedance

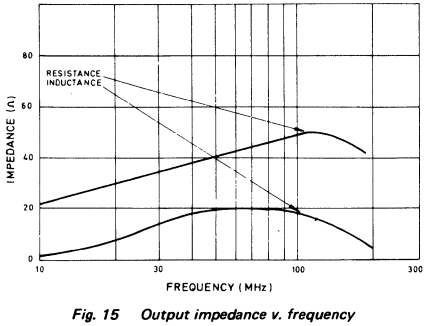


Fig. 15 Output impedance v. frequency

OPERATING NOTES

Low Noise Input Stage

As shown in Fig. 1, the input transistor can be used in common base or common emitter by using either pin 7 or pin 5 as the input, the other pin being decoupled. If a well-defined 50 or 75Ω input impedance is required, then a circuit similar to test circuit A (Fig. 4) should be used. An accuracy of ± 5% can be expected in the input impedance of this circuit since the input impedance of the common base stage is very reproducible and also is to some extent masked by the external resistor. A return loss of 30dB up to 100 MHz can be achieved with careful layout and the use of a physically small, accurate external resistor. The value of the resistor should be 56Ω for 75Ω input impedance and 33Ω if 50Ω input impedance is required.

The noise figure of this transistor is flat from the flicker noise knee around 10 Hz to over 150 MHz.

Transresistance Amplifier

The transresistance amplifier will operate correctly for values of R_T from 200Ω to 10 kΩ. The voltage gain of the complete amplifier is of course directly proportional to R_T. See Figs. 12 and 13.

Output Stage

When the internal regulator is bypassed for applying the supply voltage to pin 14, some control of the quiescent current is possible. The biasing circuitry has been designed so that the individual currents track together with the supply voltage and with each other. This enables a significant improvement to be made in the output swing into low impedance loads at the expense of increased current consumption. See Fig. 7. The quiescent current of the first device also increases, giving an increase in gain in the common emitter configuration. The quiescent current in the output stage can be varied by means of an external resistor. The link between pins 1 and 12 must be removed and a resistor added between pins 14 and 12. The current is 10 mA with 2.5 kΩ and is approximately inversely proportional to the resistor value.

Peaking Capacitor C_P

The frequency response of the amplifier is dominated by the output emitter follower which begins to roll off at about 50 MHz. The high frequency peaking capacitor is used to compensate for this roll-off and also that due to stray inductance and capacity in the external circuitry. The values of peaking capacitor used in the test circuits have been selected for best gain flatness in the test fixture but are not necessarily typical of the values required in different layouts since the stray reactances associated with a plug-in test facility are inevitably higher than in a directly wired circuit. The typical curves were measured with an SL1030 directly soldered into a PC board and the values of the peaking capacitor given will be more typical of the normal situation.

Layout and Stability

Since gains of 40dB are available up to VHF frequencies normal high frequency layout precautions are necessary with respect to grounding and decoupling. Decoupling capacitors should be low inductance ceramic types (Erie Weecons are ideal) and to ensure good earth connections a continuous ground plane should be provided around and underneath the circuit. Decoupling of pins 5 or 7 is critical and inadequate decoupling of pin 14 can cause instability. Since no overall feedback is used, the amplifier is very tolerant of load reactance and no instability has been observed even with pure capacitive loads. A certain amount of care is needed when using the internal regulator. If the decoupling on pin 11 is effective above 200 MHz, then instability can occur within the regulator. This can be completely stopped by inserting an inductance of a few hundred nanohenries between the decoupling capacitor and pin 11 as shown on the test circuits.

ABSOLUTE MAXIMUM RATINGS

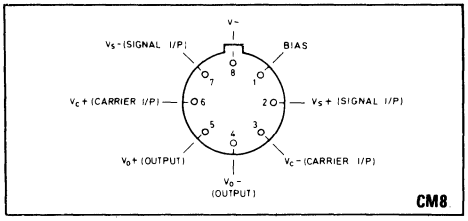
V_{S1} (Pin 11)	+15V
V_{S2} (Pin 14)	+10V
Storage temperature	−55°C to +150°C
Operating temperature (ambient)	−55°C to +125°C

PLESSEY
SEMICONDUCTORS

SL1696C

DOUBLE-BALANCED MODULATOR/DEMODULATOR

The SL1696 is a versatile monolithic integrated circuit double balanced modulator/demodulator, designed for use where the output voltage is the product of the signal input voltage and the switching carrier voltage. The SL1696 has an operating temperature range of 0°C to +70°C.



FEATURES

- Carrier Suppression 65dB Typ. @500 kHz, 50dB Typ. @ 10 MHz
- Common Mode Rejection 85dB Typ.
- Gain and Signal Handling Both Adjustable
- Balanced Inputs and Outputs

APPLICATIONS

- DSB, DSBSC, AM Modulation
- Synchronous Detection
- FM Detection
- Phase Detection
- Chopper and Signal Routeing Applications

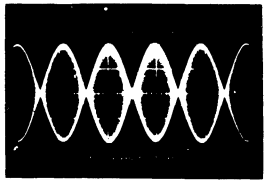


Fig. 1 Suppressed carrier output waveform

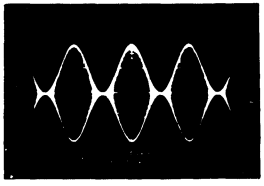


Fig. 2 AM output waveform

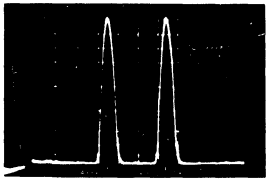


Fig. 3 Suppressed carrier spectrum

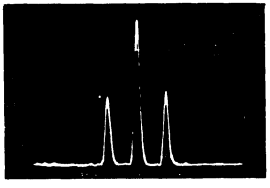


Fig. 4 AM spectrum

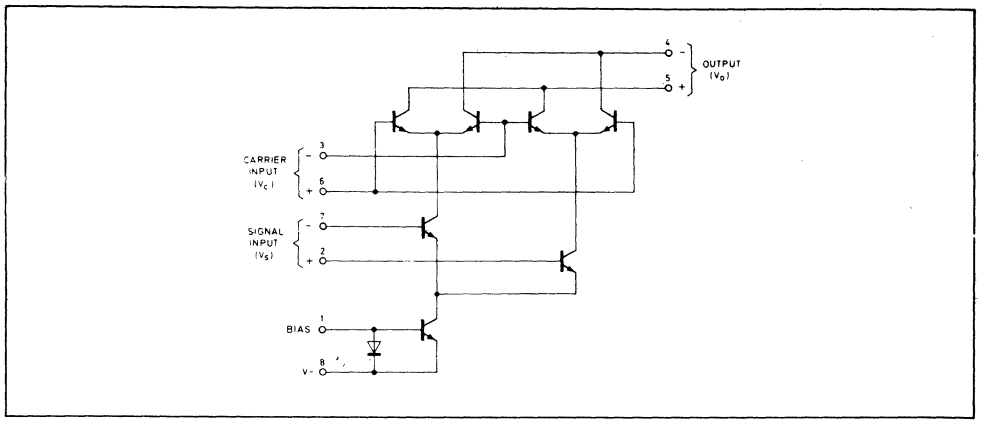


Fig. 5 Circuit diagram

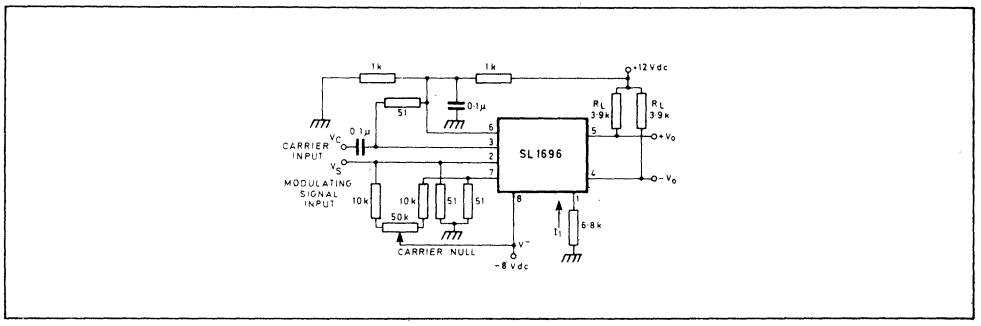


Fig. 6 Typical modulator circuit

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C, unless otherwise stated

Rating	Symbol	Value	Units
Applied Voltage ($V_5 - V_6$, $V_3 - V_2$, $V_4 - V_6$, $V_4 - V_3$, $V_6 - V_7$, $V_6 - V_2$, $V_3 - V_7$, $V_5 - V_3$)	ΔV	20	VDC
Differential Input Signal	$V_6 - V_3$	+5.0	VDC
	$V_7 - V_2$	± 5	VDC
Maximum Bias Current	I_1	10	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		575	mW
Derate above T_A = +25°		3.85	mW/°C
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
V^+ = +12V DC, V^- = −8V DC, I_1 = 1.0 mA DC, R_L = 3.9 kΩ, T_A = +25°C
All input and output characteristics single-ended, unless otherwise stated.

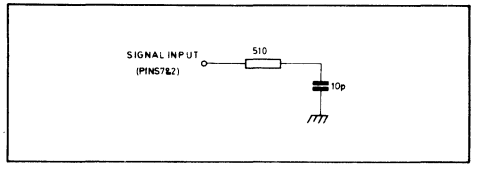
Characteristic	Fig.	Note	Symbol	Value			Units
				Min.	Typ.	Max.	
Carrier Feedthrough	7	1	V_{CFT}				μV(rms)
V_C = 60 mV(rms) sinewave and f_C = 1.0 kHz				–	40	–	
offset adjusted to zero f_C = 10 MHz				–	140	–	
V_C = 300 mVp-p square wave							mV(rms)
offset adjusted to zero f_C = 1.0 kHz				–	0.04	0.4	
offset not adjusted f_C = 1.0 kHz				–	20	200	
Carrier Suppression	7	2	V_{CS}				dB
f_S = 10 kHz, 300 mV(rms)							
f_C = 500 kHz, 60 mV(rms) sinewave				40	65	–	
f_C = 10 MHz, 60 mV(rms) sinewave				–	50	–	
Transadmittance Bandwidth (R_L = 50 ohms)	10	8	BW_{3dB}				MHz
Carrier Input Port, V_C = 60 mV(rms) sinewave				–	300	–	
f_S = 1.0 kHz, 300 mV(rms) sinewave							
Signal Input Port, V_S = 300 mV(rms) sinewave				–	80	–	
V_C = 0.5 V DC							
Signal Gain	12	3	A_{VS}	2.5	3.5	–	V/V
V_S = 100 mV(rms), f = 1.0 kHz; V_C = 0.5 V DC							
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz	8	–					
Parellel Input Resistance			r_{ip}	–	200	–	kΩ
Parallel Input Capacitance			c_{ip}	–	2.0	–	pF
Single-Ended Output Impedance, f = 10 MHz	8	–					
Parallel Output Resistance			r_{op}	–	40	–	kΩ
Parallel Output Capacitance			c_{op}	–	5.0	–	pF
Input Bias Current	9	–					μA
$I_{bS} = \frac{I_2 + I_7}{2}$; $I_{bC} = \frac{I_6 + I_3}{2}$			I_{bS}	–	12	30	
			I_{bC}	–	12	30	
Input Offset Current	9	–					μA
$I_{ioS} = I_2 - I_7$; $I_{ioC} = I_6 - I_3$			I_{ioS}	–	0.7	7.0	
			I_{ioC}	–	0.7	7.0	
Average Temperature Coefficient of Input Offset Current (T_A = −55°C to +125°C)	9	–	TC_{Iio}	–	2.0	–	nA/°C
Output Offset Current ($I_5 - I_4$)	9	–	I_{oo}	–	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = −55°C to +125°C)	9	–	TC_{Ioo}		90	–	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	11	4	CMV	–	5.0	–	Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz, $\|V_C\|$ = 0.5 V DC	11	–	A_{CM}	–	−85	–	dB
Common-Mode Quiescent Output Voltage (Pin 5 or Pin 4)	12	–	V_o	–	8.0	–	V DC
Differential Output Voltage Swing Capability	12	–	V_{out}	–	8.0	–	Vp-p
Power Supply Current	9	6					mA DC
$I_5 + I_4$			I_D^+	–	1.0	2.0	
I_8			I_D^-	–	2.0	3.0	
DC Power Dissipation	9	5	P_D	–	33	–	mW

Note 10 – Output Signal, V_o

The output signal is taken from pins 5 and 4, either balanced or single-ended.

Note 11 – Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



An alternative method for low-frequency applications is to insert a 1 k-ohm resistor in series with the inputs, pins 2 and 7. In this case input current drift may cause serious degradation of carrier suppression.

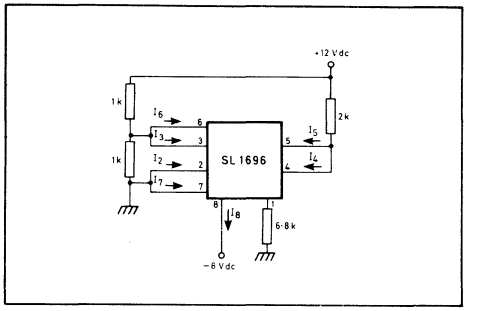


Fig. 9 Bias and offset currents

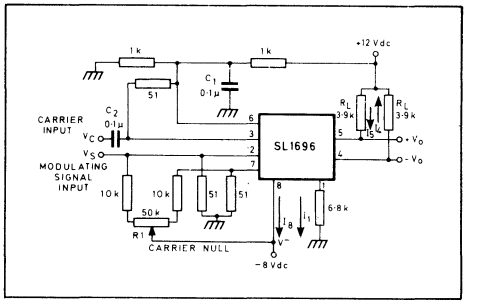


Fig. 10 Transconductance bandwidth

TEST CIRCUITS (FIGS. 7 TO 12)

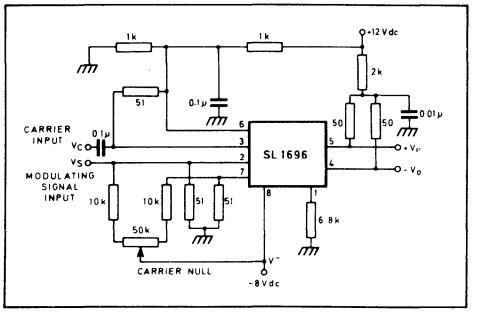


Fig. 7 Carrier rejection and suppression

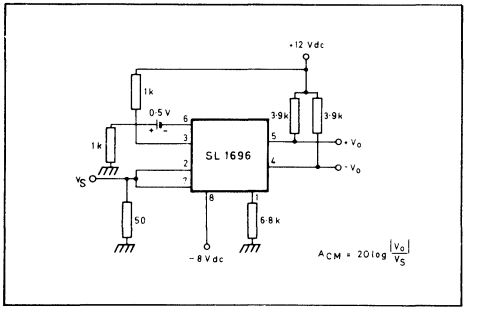


Fig. 11 Common-mode gain

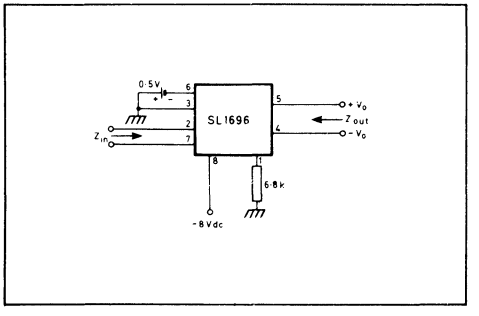


Fig. 8 Input/output impedance

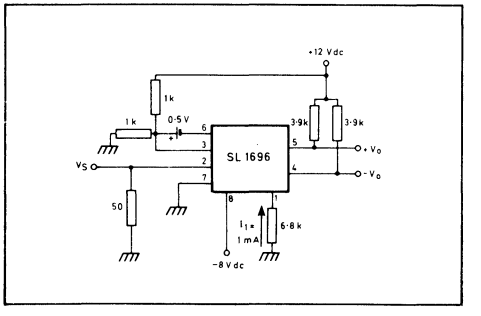


Fig. 12 Signal gain and output swing

OPERATING NOTES

Note 1 – Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R_1 of Fig. 7).

Note 2 – Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The SL1696 has been characterized with a 60 mV(rms) sinewave carrier input signal.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair – or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Note 3 – Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{2r_e}$$

$$r_e = \frac{26mV}{I_1\ (mA)}$$

A constant DC potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 V). This in effect forms a cascode differential amplifier.

Note 4 – Common-Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen (see Note 6).

Note 5 – Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming $V_4 = V_5$, $I_1 = I_5 = I_4$ and ignoring base current, $P_D = 2I_1 (V_5 - V_8) + I_1 (V_1 - V_8)$ where subscripts refer to TO-5 package pin numbers.

Note 6 – Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions.

A. Operating Current

The internal bias currents are set by the conditions at pin 1 Assume:

$$I_4 = I_5 = I_1$$

$$I_B \ll I_C \text{ for all transistors}$$

then:

$$R_1 = \frac{V^- - \theta}{I_1} - 500\Omega$$

where: R_1 is the resistor between pin 1 and ground

θ = 0.75 V at T_A = +25°C

The SL1696 has been characterized for the condition I = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_4 = V_5 = V^+ - I_1 R_L$$

Note 7 – Biasing

The SL1696 requires three DC bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$20V \geqslant [(V_5\ V_4) - (V_6\ V_3)] \geqslant 2V$$
$$20V \geqslant [(V_6\ V_3) - (V_2\ V_7)] \geqslant 2.7V$$
$$20V \geqslant [(V_2\ V_7) - (V_1)] \geqslant 2.7V$$

The foregoing conditions are based on the following approximations:

$$V_5 = V_4 \qquad V_6 = V_3 \qquad V_2 = V_7$$

Bias currents flowing into pins 2, 7, 6 and 3 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Note 8 – Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3 dB bandwidth of the device forward transadmittance as defined by:

$$Y_{21C} = \frac{i_o\ (\text{each sideband})}{V_S\ (\text{signal})} \Bigg| V_o = 0$$

Signal transadmittance bandwidth is the 3 dB bandwidth of the device forward transadmittance as defined by:

$$Y_{21S} = \frac{i_o\ (\text{signal})}{V_S\ (\text{signal})} \Bigg| V_C = 0.5\ \text{Vdc}, V_o = 0$$

Note 9 – Coupling and Bypass Capacitors C_1 and C_2

Capacitors C_1 and C_2 (Fig. 7) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

OPERATING PRINCIPLES

The SL1696, a monolithic balanced modulator circuit, is shown in Fig. 5.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with a current source. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant multiplied by the product of the two input signals.

Mathematical analysis of linear AC signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, double balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristcs.

External load resistors are employed at the device output.

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant time the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier and lower differential amp has its emitters internally connected, this voltage applies to the input ports for all conditions.

The gain from the modulating signal input port to the output is the SL1696 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the SL1696 for a low-level modulating signal input and the following carrier input conditions:

1) Low-level DC
2) High-level DC
3) Low-level AC
4) High-level AC

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level DC	$\frac{R_L V_C}{4r_e \frac{KT}{q}}$	f_M
High-level DC	$\frac{R_L}{2r_e}$	f_M
Low-level AC	$\frac{R_L V_C(rms)}{2\sqrt{2}\frac{KT}{q} 2r_e}$	$f_C \pm f_M$
High-level AC	$\frac{0.637 R_L}{2r_e}$	$f_C \pm f_M, 3f_C \pm f_M$ $5f_C \pm f_M, \ldots$

Table 1 Voltage gain and output frequencies

NOTES:

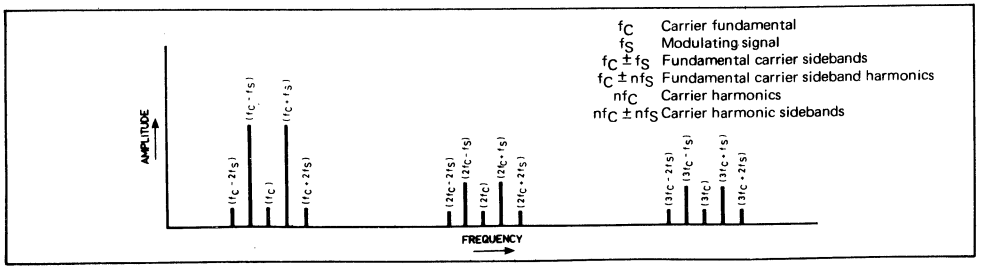
1. Low-level Modulating Signal, V_M assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. r_e = Transistor dynamic emitter resistance, At +25°C;

$$r_e \approx \frac{26\ mV}{I_s\ (mA)}$$

6. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26\ mV \text{ at room temperature}$$

DEFINITIONS



APPLICATION NOTES

Double sideband suppressed carrier modulation is the basic application of the SL1696. The suggested circuit for this application is shown in Fig. 6, on page 2 of this data sheet.

In some applications, it may be necessary to operate the SL1696 with a single DC supply voltage instead of dual supplies. Fig. 13 shows a balanced modulator designed for operation with a single +12V supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Fig. 14 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Fig. 14 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Fig. 15.

Product Detector

The SL1696 makes an excellent SSB product detector (see Fig. 16).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1μF capacitors on pins 6 and 3 should be increased to 1.0μF. Also, the output filter at pin 4 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

Double Balanced Mixer

The SL1696 may be used as a double balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Fig. 17 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The SL1696 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figs. 18 and 19 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The SL1696 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the SL1696 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The SL1696 will then provide an output which is a function of the input signal frequency,

TYPICAL APPLICATIONS (FIGS. 13 TO 19)

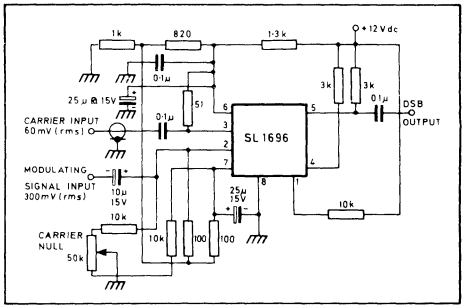


Fig. 13 Balanced modulator (+12V single supply)

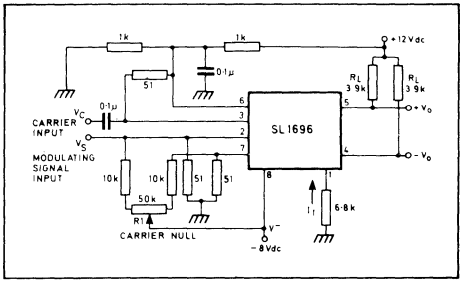


Fig. 14 Balanced modulator/demodulator

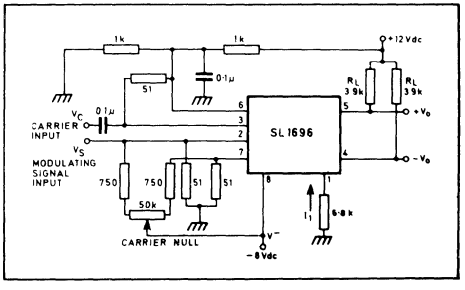


Fig. 15 AM modulator

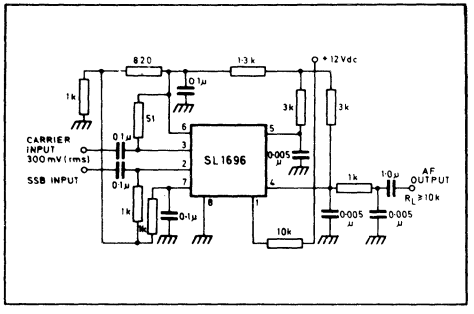


Fig. 16 Product detector (+12V single supply)

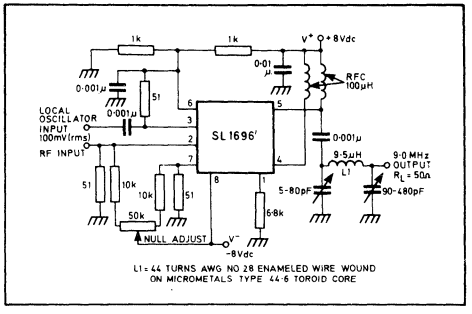


Fig. 17 Double-balanced mixer (broadband inputs, 9.0 MHz tuned output)

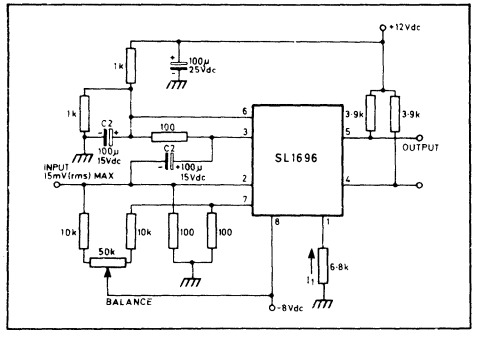


Fig. 18 Low frequency doubler

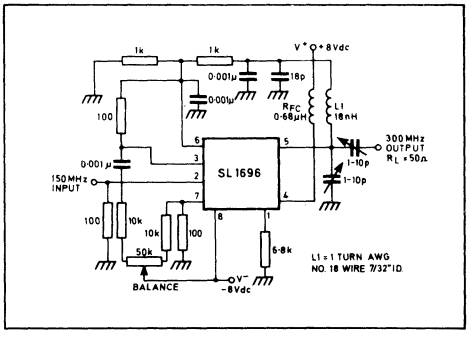


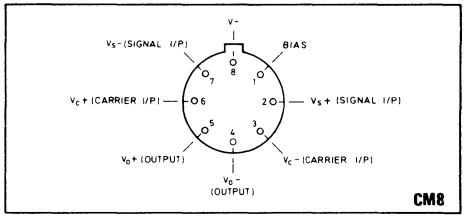
Fig. 19 150 to 300 MHz doubler

PLESSEY
SEMICONDUCTORS

SL1796C

DOUBLE-BALANCED MODULATOR/DEMODULATOR

The SL1796 is a versatile monolithic integrated circuit double balanced modulator/demodulator, designed for use where the output voltage is the product of the signal input voltage and the switching carrier voltage. The SL1796 has an operating temperature range of 0°C to +70°C.



FEATURES

- Carrier Suppression 65dB Typ. @500 kHz, 50dB Typ. @10 MHz
- Common Mode Rejection 85dB Typ.
- Gain and Signal Handling Both Adjustable
- Balanced Inputs and Outputs

APPLICATIONS

- DSB, DSBSC, AM Modulation
- Synchronous Detection
- FM Detection
- Phase Detection
- Chopper and Signal Routeing Applications

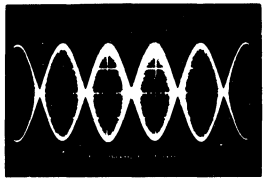


Fig. 1 Suppressed carrier output waveform

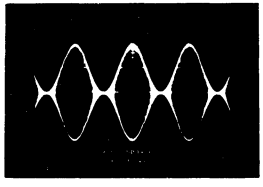


Fig. 2 AM output waveform

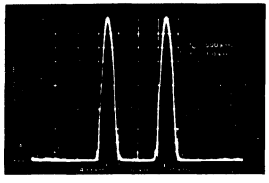


Fig. 3 Suppressed carrier spectrum

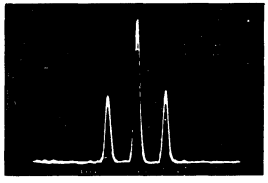


Fig. 4 AM spectrum

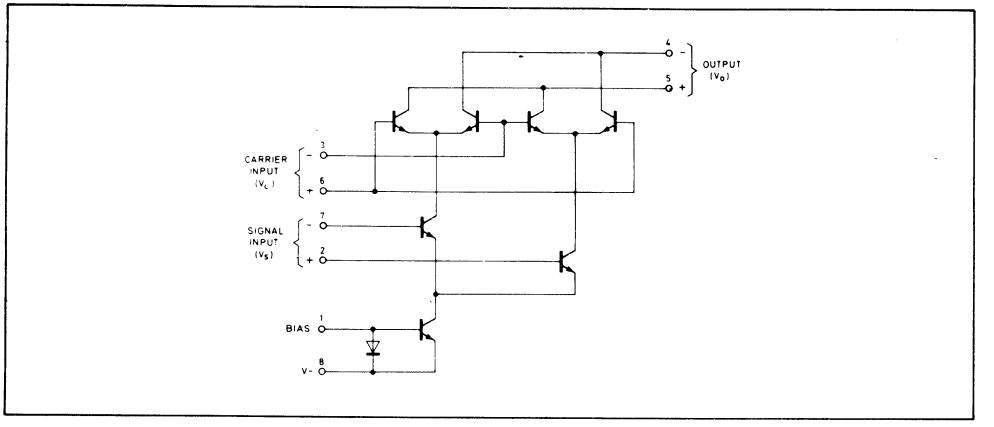


Fig. 5 Circuit diagram

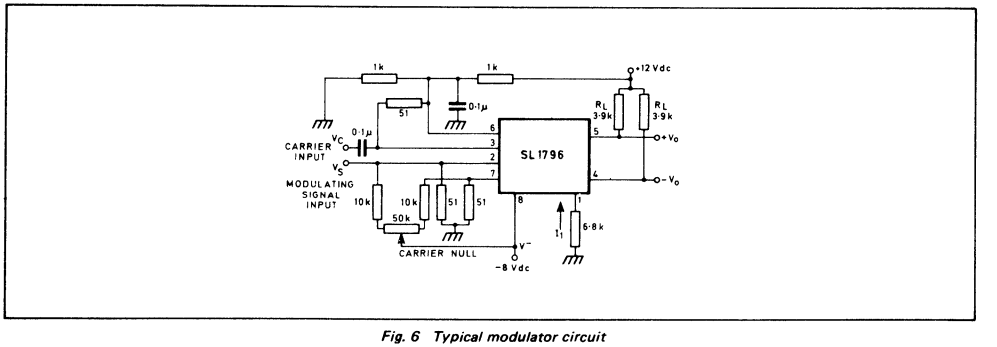


Fig. 6 Typical modulator circuit

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C, unless otherwise stated

Rating	Symbol	Value	Units
Applied Voltage ($V_5 - V_6$, $V_3 - V_2$, $V_4 - V_6$, $V_4 - V_3$, $V_6 - V_7$, $V_6 - V_2$, $V_3 - V_7$, $V_5 - V_3$)	ΔV	45	VDC
Differential Input Signal	$V_6 - V_3$	+5.0	VDC
	$V_7 - V_2$	± 5	VDC
Maximum Bias Current	I_1	10	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		575	mW
Derate above T_A = +25°		3.85	mW/°C
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
V^+ = +12V DC, V^- = −8V DC, I_1 = 1.0 mA DC, R_L = 3.9 kΩ, T_A = +25°C
All input and output characteristics single-ended, unless otherwise stated.

Characteristic	Fig.	Note	Symbol	Value			Units
				Min.	Typ.	Max.	
Carrier Feedthrough	7	1	V_{CFT}				μV(rms)
V_C = 60 mV(rms) sinewave and f_C = 1.0 kHz				–	40	–	
offset adjusted to zero f_C = 10 MHz				–	140	–	
V_C = 300 mVp-p square wave							mV(rms)
offset adjusted to zero f_C = 1.0 kHz				–	0.04	0.4	
offset not adjusted f_C = 1.0 kHz				–	20	200	
Carrier Suppression	7	2	V_{CS}				dB
f_S = 10 kHz, 300 mV(rms)							
f_C = 500 kHz, 60 mV(rms) sinewave				40	65	–	
f_C = 10 MHz, 60 mV(rms) sinewave				–	50	–	
Transadmittance Bandwidth (R_L = 50 ohms)	10	8	BW_{3dB}				MHz
Carrier Input Port, V_C = 60 mV(rms) sinewave				–	300	–	
f_S = 1.0 kHz, 300 mV(rms) sinewave							
Signal Input Port, V_S = 300 mV(rms) sinewave				–	80	–	
V_C = 0.5 V DC							
Signal Gain	12	3	A_{VS}	2.5	3.5	–	V/V
V_S = 100 mV(rms), f = 1.0 kHz; V_C = 0.5 V DC							
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz	8	–					
Parallel Input Resistance			r_{ip}	–	200	–	kΩ
Parallel Input Capacitance			c_{ip}	–	2.0	–	pF
Single-Ended Output Impedance, f = 10 MHz	8	–					
Parallel Output Resistance			r_{op}	–	40	–	kΩ
Parallel Output Capacitance			c_{op}	–	5.0	–	pF
Input Bias Current	9	–					μA
$I_{bS} = \frac{I_2 + I_7}{2}$; $I_{bC} = \frac{I_6 + I_3}{2}$			I_{bS}	–	12	30	
			I_{bC}	–	12	30	
Input Offset Current	9	–					μA
$I_{ioS} = I_2 - I_7$; $I_{ioC} = I_6 - I_3$			$\|I_{ioS}\|$	–	0.7	7.0	
			$\|I_{ioC}\|$	–	0.7	7.0	
Average Temperature Coefficient of Input Offset Current (T_A = −55°C to +125°C)	9	–	$\|TC_{Iio}\|$	–	2.0	–	nA/°C
Output Offset Current ($I_5 - I_4$)	9	–	$\|I_{oo}\|$	–	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = −55°C to +125°C)	9	–	$\|TC_{Ioo}\|$		90	–	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	11	4	CMV	–	5.0	–	Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz, $\|V_C\|$ = 0.5 V DC	11	–	A_{CM}	–	−85	–	dB
Common-Mode Quiescent Output Voltage (Pin 5 or Pin 4)	12	–	V_o	–	8.0	–	V DC
Differential Output Voltage Swing Capability	12	–	V_{out}	–	8.0	–	Vp-p
Power Supply Current	9	6					mA DC
$I_5 + I_4$			I_D^+	–	2.0	4.0	
I_8			I_D^-	–	3.0	5.0	
DC Power Dissipation	9	5	P_D	–	33	–	mW

OPERATING NOTES

Note 1 – Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R_1 of Fig. 7).

Note 2 – Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The SL1796 has been characterized with a 60 mV(rms) sinewave carrier input signal.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair – or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Note 3 – Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{2r_e}$$

$$r_e = \frac{26mV}{I_1\ (mA)}$$

A constant DC potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 V). This in effect forms a cascode differential amplifier.

Note 4 – Common-Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen (see Note 6).

Note 5 – Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming $V_4 = V_5$, $I_1 = I_5 = I_4$ and ignoring base current, $P_D = 2I_1 (V_5 - V_8) + I_1 (V_1 - V_8)$ where subscripts refer to TO-5 package pin numbers.

Note 6 – Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions.

A. Operating Current

The internal bias currents are set by the conditions at pin 1 Assume:

$$I_4 = I_5 = I_1$$
$$I_B \ll I_C \text{ for all transistors}$$

then:

$$R_1 = \frac{V^- - \theta}{I_1} - 500\Omega$$

where: R_1 is the resistor between pin 1 and ground

θ = 0.75 V at T_A = +25°C

The SL1796 has been characterized for the condition I = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_4 = V_5 = V^+ - I_1 R_L$$

Note 7 – Biasing

The SL1796 requires three DC bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$20V \geq [(V_5\ V_4) - (V_6\ V_3)] \geq 2V$$
$$20V \geq [(V_6\ V_3) - (V_2\ V_7)] \geq 2.7V$$
$$20V \geq [(V_2\ V_7) - (V_1)] \geq 2.7V$$

The foregoing conditions are based on the following approximations:

$$V_5 = V_4 \qquad V_6 = V_3 \qquad V_2 = V_7$$

Bias currents flowing into pins 2, 7, 6 and 3 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Note 8 – Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3 dB bandwidth of the device forward transadmittance as defined by:

$$Y_{21C} = \frac{i_o\ (\text{each sideband})}{V_S\ (\text{signal})} \Bigg| V_o = 0$$

Signal transadmittance bandwidth is the 3 dB bandwidth of the device forward transadmittance as defined by:

$$Y_{21S} = \frac{i_o\ (\text{signal})}{V_S\ (\text{signal})} \Bigg| V_C = 0.5\ \text{Vdc}, V_o = 0$$

Note 9 – Coupling and Bypass Capacitors C_1 and C_2

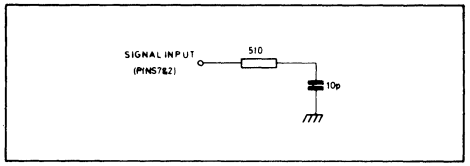
Capacitors C_1 and C_2 (Fig. 7) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

Note 10 – Output Signal, V_o

The output signal is taken from pins 5 and 4, either balanced or single-ended.

Note 11 – Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



An alternative method for low-frequency applications is to insert a 1 k-ohm resistor in series with the inputs, pins 2 and 7. In this case input current drift may cause serious degradation of carrier suppression.

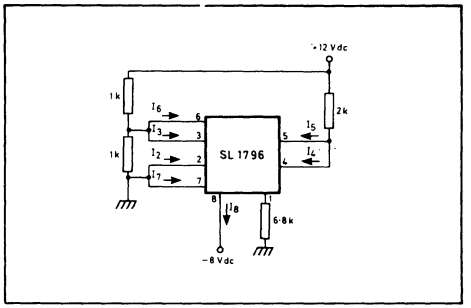


Fig. 9 Bias and offset currents

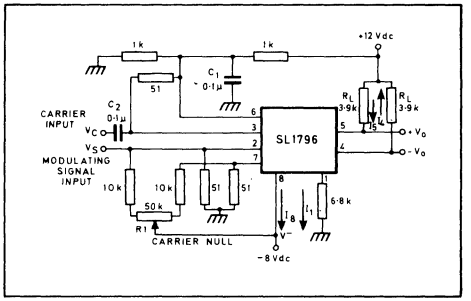


Fig. 10 Transconductance bandwidth

TEST CIRCUITS (FIGS. 7 TO 12)

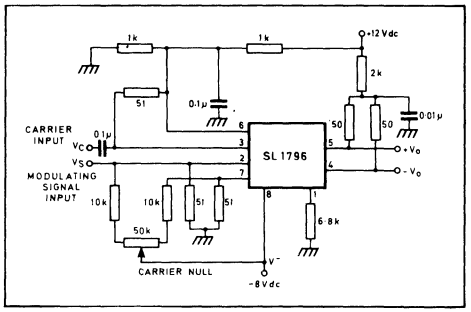


Fig. 7 Carrier rejection and suppression

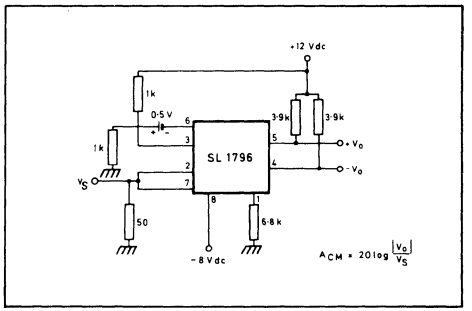


Fig. 11 Common-mode gain

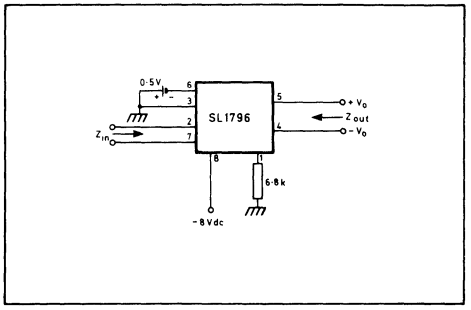


Fig. 8 Input/output impedance

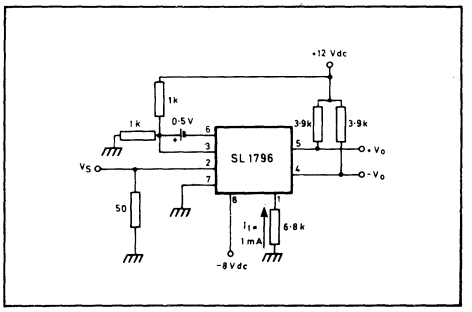


Fig. 12 Signal gain and output swing

OPERATING PRINCIPLES

The SL1796, a monolithic balanced modulator circuit, is shown in Fig. 5.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with a current source. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant multiplied by the product of the two input signals.

Mathematical analysis of linear AC signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, double balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristcs.

External load resistors are employed at the device output.

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant time the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier and lower differential amp has its emitters internally connected, this voltage applies to the input ports for all conditions.

The gain from the modulating signal input port to the output is the SL1796 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the SL1796 for a low-level modulating signal input and the following carrier input conditions:

1) Low-level DC
2) High-level DC
3) Low-level AC
4) High-level AC

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level DC	$\frac{R_L V_C}{4r_e \frac{KT}{q}}$	f_M
High-level DC	$\frac{R_L}{2r_e}$	f_M
Low-level AC	$\frac{R_L V_C(rms)}{2\sqrt{2}\frac{KT}{q} 2r_e}$	$f_C \pm f_M$
High-level AC	$\frac{0.637 R_L}{2r_e}$	$f_C \pm f_M, 3f_C \pm f_M$ $5f_C \pm f_M, \ldots$

Table 1 Voltage gain and output frequencies

NOTES:

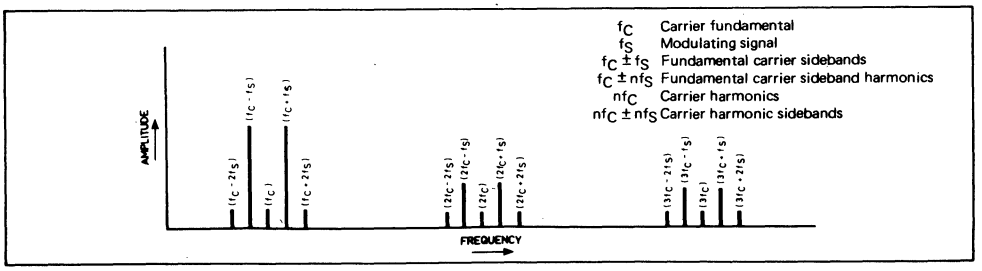
1. Low-level Modulating Signal, V_M assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. r_e = Transistor dynamic emitter resistance, At +25°C;

$$r_e \approx \frac{26\ mV}{I_5\ (mA)}$$

6. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26\ mV \text{ at room temperature}$$

DEFINITIONS



APPLICATION NOTES

Double sideband suppressed carrier modulation is the basic application of the SL1796. The suggested circuit for this application is shown in Fig. 6, on page 2 of this data sheet.

In some applications, it may be necessary to operate the SL1796 with a single DC supply voltage instead of dual supplies. Fig. 13 shows a balanced modulator designed for operation with a single +12V supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Fig. 14 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Fig. 14 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Fig. 15.

Product Detector

The SL1796 makes an excellent SSB product detector (see Fig. 16).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1μF capacitors on pins 6 and 3 should be increased to 1.0μF. Also, the output filter at pin 4 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

Double Balanced Mixer

The SL1796 may be used as a double balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Fig. 17 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The SL1796 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figs. 18 and 19 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The SL1796 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the SL1796 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The SL1796 will then provide an output which is a function of the input signal frequency,

TYPICAL APPLICATIONS (FIGS. 13 TO 19)

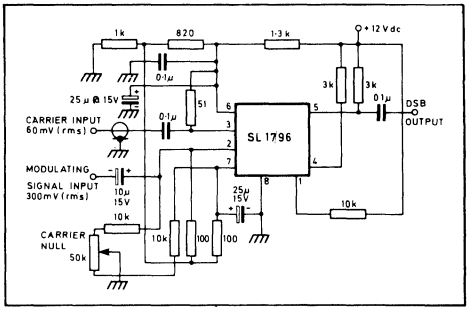


Fig. 13 Balanced modulator (+12V single supply)

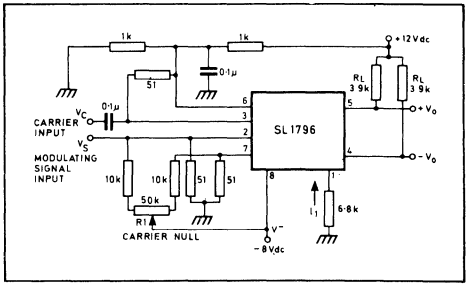


Fig. 14 Balanced modulator/demodulator

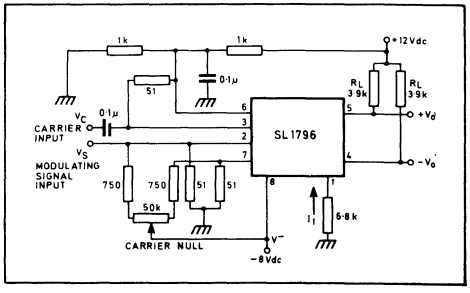


Fig. 15 AM modulator

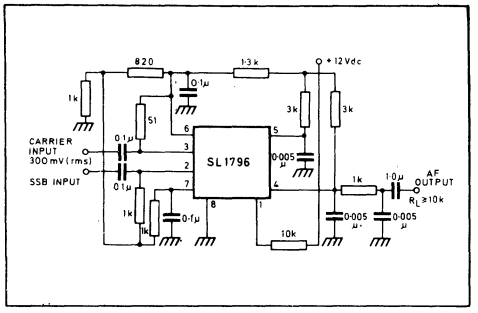


Fig. 16 Product detector (+12V single supply)

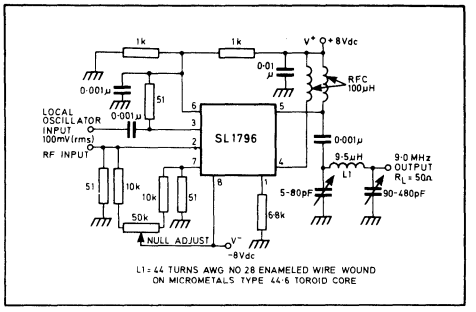


Fig. 17 Double-balanced mixer (broadband inputs, 9.0 MHz tuned output)

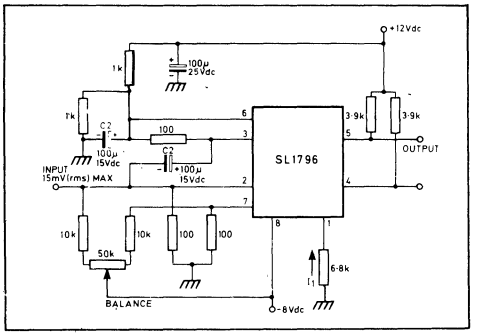


Fig. 18 Low frequency doubler

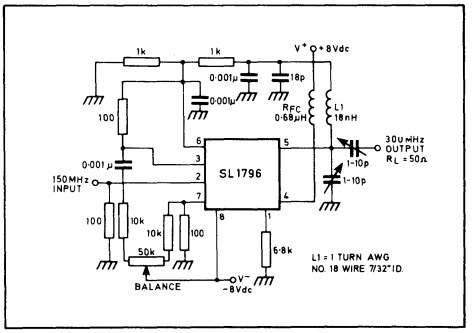


Fig. 19 150 to 300 MHz doubler

PLESSEY
Semiconductors

SL2363C & SL2364C

VERY HIGH PERFORMANCE TRANSISTOR ARRAYS

The SL2363C and SL2364C are arrays of transistors internally connected to form a dual long-tailed pair with tail transistors. They are monolithic integrated circuits manufactured on a very high speed bipolar process which has a minimum useable f_T of 2.5 GHz, (typically 5GHz).

The SL2363 is in a 10 lead TO5 encapsulation.

The SL2364 is in a 14 lead DIL ceramic encapsulation.

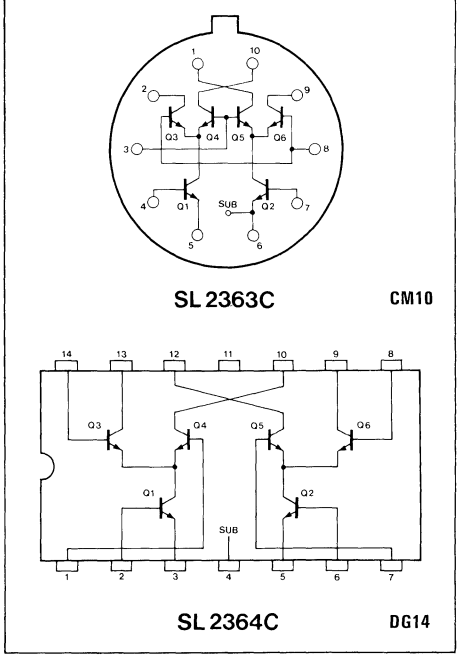


Fig. 1 Pin connections (top view)

FEATURES

- Complete Dual Long-Tailed Pair in One Package.
- Very High f_T – Typically 5 GHz
- Very Good Matching Including Thermal Matching

APPLICATIONS

- Wide Band Amplification Stages
- 140 and 560 MBit PCM Systems
- Fibre Optic Systems
- High Performance Instrumentation
- Radio and Satellite Communications

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ±2°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	10	20		V	I_C = 10μA
LV_{CEO}	6	9		V	I_C = 5mA
BV_{EBO}	2.5	5.0		V	I_E = 10μA
BV_{CIO}	16	40		V	I_C = 10μA
h_{FE}	20	80			I_C = 8mA, V_{CE} = 2V
f_T	2.5	5		GHz	I_C (Tail) = 8mA, V_{CE} = 2V
ΔV_{BE} (See note 1)		2	5	mV	I_C (Tail) = 8 mA, V_{CE} = 2V
$\Delta V_{BE}/T_{AMB}$					I_C (Tail) = 8 mA, V_{CE} = 2V
C_{CB}			0.5	pF	V_{CB} = 0
C_{CI}			1	pF	V_{CB} = 0

NOTE 1 ΔV_{BE} applies to $|V_{BEQ3} - V_{BEQ4}|$ and $|V_{BEQ5} - V_{BEQ6}|$

TYPICAL CHARACTERISTICS

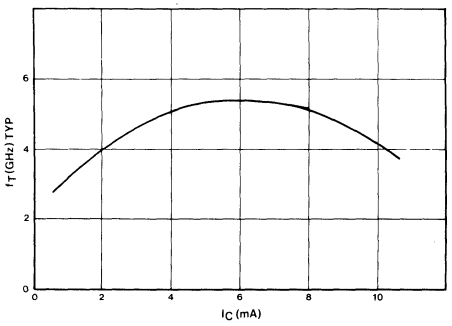


Fig. 2 Collector current

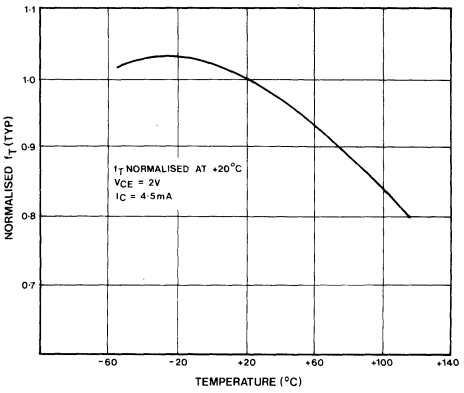


Fig. 3 Chip temperature

ABSOLUTE MAXIMUM RATINGS

Maximum individual transistor dissipation 200mW

Storage temperature	−55°C to +150°C
Maximum junction temperature	+150°C

Package thermal resistance (°C/W):

Chip to case	40 (DG14)	65 (CM10)
Chip to ambient	120 (DG14)	225 (CM10)

V_{CBO} = 10V, V_{EBO} = 2.5V, V_{CEO} = 6V, V_{CIO} = 15V

PLESSEY
SEMICONDUCTORS

SL3000 SERIES
TRANSISTOR ARRAYS

SL3045C SL3046C
TRANSISTOR ARRAYS

The SL3045 and SL3046 are monolithic arrays of five general purpose high frequency transistors arranged as a differential pair and three isolated transistors. The transistors feature a V_{BE} matching of, typically, better than ± 5mV between any pair, an f_T of 300MHz and a low noise figure.

The SL3045 is available only in a ceramic dual-in-line package; the SL3046 is packaged in plastic dual-in-line.

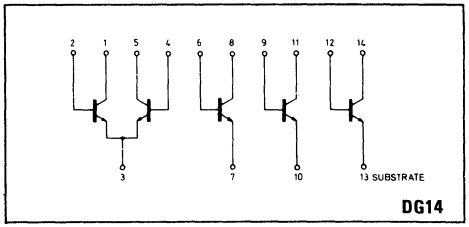


Fig. 1 Pin connections

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = +25°C

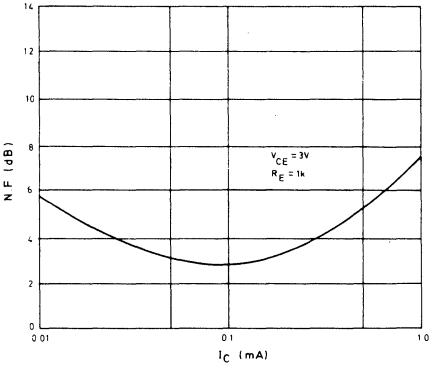
Static Characteristics

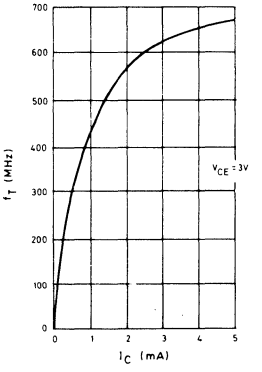
Symbol	Characteristic	Value			Units	Test conditions
		Min.	Typ.	Max.		
BV_{EBO}	Emitter-base breakdown	5			V	I_E = 10μA
BV_{CEO}	Collector-emitter breakdown	15			V	I_C = 1mA
BV_{CBO}	Collector-base breakdown	20	50		V	I_C = 10μA
BV_{CIO}	Collector-substrate breakdown	20	70		V	I_C = 10μA
I_{CEO}	Collector cut off current			0.5	μA	V_{CE} = 10V, I_B = 0
I_{CBO}	Collector cut off current			4	nA	V_{CB} = 10V, I_E = 0
$V_{BE(ON)}$	Base emitter voltage		0.71		V	V_{CE} = 3V I_C = 1mA
			0.78		V	V_{CE} = 3V I_C = 10mA
$V_{CE(SAT)}$	Collector-emitter saturation		0.3		V	I_B = 1mA I_C = 10mA
h_{FE}	Static forward current-transfer ratio		120			V_{CE} = 3V I_C = 10mA
		40	100			V_{CE} = 3V I_C = 1mA
			50			V_{CE} = 3V I_C = 10μA
I_{10}	Input offset current—differential pair		0.2	2	μA	V_{CE} = 3V I_C = 1mA
ΔV_{BE1}	Input offset voltage—differential pair		0.35	5	mV	V_{CE} = 3V I_C = 1mA
ΔV_{BE2}	Input offset voltage-isolated transistors		0.45	5	mV	V_{CE} = 3V I_C = 1mA
$\frac{\partial \Delta_{BE}}{\partial T}$	Temperature co-efficient of input offset voltage		2		μV/°C	V_{CE} = 3V I_C = 1mA
$\frac{\partial V_{BE(ON)}}{\partial T}$	Temperature co-efficient of base emitter-voltage		1.8		mV/°C	V_{CE} = 3V I_C = 1mA

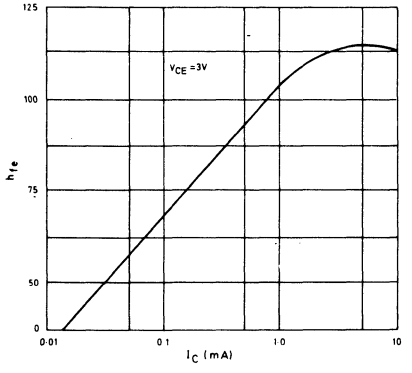
Dynamic Characteristics

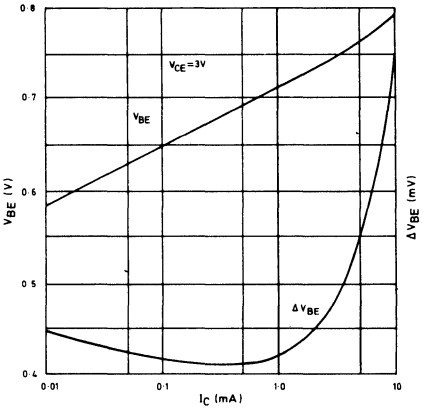
Symbol	Characteristic	Value			Units	Test conditions
		Min.	Typ.	Max.		
N.F.	Wide band noise figure		3.5		dB	f = 10Hz to 10kHz V_{CE} = 3V I_C = 100μA Source resistance = 1kΩ
Y_{fe}	Forward transfer admittance		31–j1.5		mmho	
Y_{ie}	Input admittance		0.3–j0.04		mmho	f = 1MHz
Y_{oe}	Output admittance		0.003+j0.04		mmho	V_{CE} = 3V I_C = 1mA
Y_{re}	Reverse transfer admittance		0.000–j0.003		mmho	
h_{fe}	Forward current transfer ratio		110			
h_{ie}	Short cct. input impedance		3.5		kΩ	f = 1kHz
h_{oe}	Open cct. output admittance		15.6		μmho	V_{CE} = 3V I_C = 1mA
h_{re}	Open circuit reverse voltage transfer ratio		$1.8x10^{-4}$			
f_t	Gain-bandwidth product	500	600		MHz	V_{CE} = 3V I_C = 3mA
C_{IB}	Emitter-base capacitance		1.7		pF	V_{EB} = 3V I_E = 0
C_{OB}	Collector-base capacitance		1.5		pF	V_{CB} = 3V I_C = 0
C_{CI}	Collector-substrate capacitance		3.0		pF	V_{CS} = 3V I_C = 0

CHARACTERISTIC GRAPHS









ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors. The isolation pin must always be negative with respect to the collectors.

V_{CBO} = 20V V_{EBO} = 15V I_C = 50mA I_B = 25mA
V_{CEO} = 15V V_{CIO} = 20V I_E = 50mA

SL3045C — DG

Storage temperature	—55 °C to +175 °C
Junction temperature	+175 °C
Package dissipation	750mW (derate linearly from 55 °C to +175 °C)

SL3046C — DP

Storage temperature	—55 °C to +125 °C
Junction temperature	+125 °C
Package dissipation	500mW (derate linearly from 55 °C to +125 °C)

PLESSEY
SEMICONDUCTORS

SL 3000 SERIES
TRANSISTOR ARRAYS

SL3081D SL3082D

GENERAL PURPOSE HIGH CURRENT NPN TRANSISTOR ARRAYS

The SL3081 and SL3082 consist of seven high current (100mA max) silicon NPN transistors on a common monolithic substrate. The SL3081 is connected in a common emitter configuration and the SL3082 is connected in a common collector configuration.

The SL3081 and SL3082 are capable of directly driving both incandescent seven segment displays and LED seven segment displays.

A separate substrate connection is provided, for maximum flexibility in circuit design.

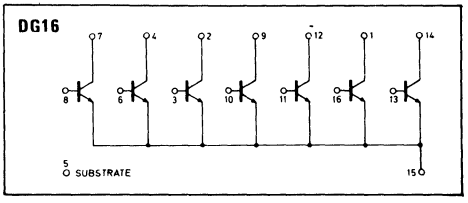


Fig. 1 SL3081 pin connections

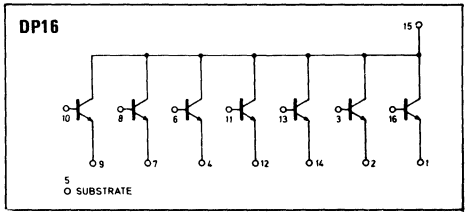


Fig. 2 SL3082 pin connections

FEATURES

- Seven Transistors Permit a Wide Range of Applications
- Common Emitter (SL3081) or Common Collector (SL3082) Configuration
- High I_C 100mA max (each transistor)
- Low $V_{CE\ SAT}$ 0.4V Typ. @ 50mA

APPLICATIONS

- Drivers for Incandescent Display Devices
- SL3081: Driver for Common Anode 7-Segment LED Displays
- SL3082: Driver for Common Cathode 7-Segment LED Displays
- MOS Clock and Calculator Display Interface Circuits
- Relay and Solenoid Drivers
- Thyristor and Triac Control Circuitry

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C

All electrical ratings apply to individual transistors; termal ratings apply to total package dissipation.

The collector of each transistor of the SL3081 and SL3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and to provide normal transistor operation. To avoid undesired coupling, the substrate (pin 5) should be maintained at either DC or signal (AC) earth.

Electrical Ratings

V_{CEO} = 12V, V_{CBO} = 20V, V_{EBO} = 5V, V_{CIO} = 20V,
$I_C = I_E$ = 100mA
Power dissipation 500mW

Thermal Ratings

Storage temperature −55°C to +175°C
Junction operating temperature +175°C

ELECTRICAL CHARACTERISTICS @ T_A = 22°C ±2°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Collector-base breakdown	BV_{CBO}	20	50		V	I_C = 500μA, I_E = 0
Collector-substrate breakdown	BV_{CIO}	20	70		V	I_{CI} = 500μA I_B = 0
Collector-emitter breakdown	BV_{CEO}	12	20		V	I_C = 1mA, I_B = 0
Emitter-base breakdown	BV_{EBO}	5	5.6		V	I_E = 500μA
DC forward current transfer ratio	h_{FE}	30	68			V_{CE} = 0.5V, I_C = 30mA
		40	70			V_{CE} = 0.8V, I_C = 50mA
Collector emitter saturation	$V_{CE(SAT)}$					
SL3081, SL3082			0.27	0.5	V	I_C = 30mA, I_B = 1mA
SL3081			0.4	0.7	V	I_C = 50mA, I_B = 5mA
SL3082			0.4	0.8	V	I_C = 50mA, I_B = 5mA
Collector cut-off current	I_{CEO}			10	μA	V_{CE} = 10V, I_B = 0
Collector cut-off current	I_{CBO}			1	μA	V_{CB} = 10V, I_E = 0

PLESSEY
SEMICONDUCTORS

SL3000 SERIES
TRANSISTOR ARRAYS

SL3083D
GENERAL PURPOSE HIGH CURRENT NPN TRANSISTOR ARRAY

The SL3083 is an array of five independent high current (100mA max) NPN transistors on a common monolithic substrate. In addition, two of the transistors (TR1 and TR2) are matched at low currents (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design.

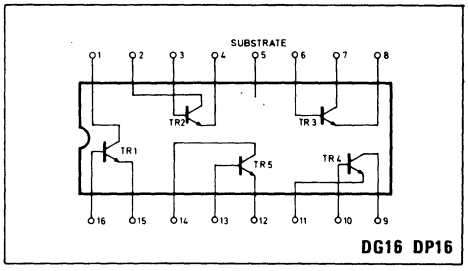


Fig. 1 SL3083 pin connections

FEATURES

- High I_C 100mA Max
- Low V_{CESAT} 0.7V Max @ 50mA
- Matched Pair (TR1 and TR2)
  - ΔV_{BE} ±5mV Max
  - I_{IO} 2.5μA Max @ 1mA
- 5 Independent Transistors plus Separate Substrate Connection

APPLICATIONS

- Signal Processing and Switching Systems Operating From DC to VHF
- Lamp, Relay, Solenoid Driver
- Differential Amplifier
- Temperature Compensated Amplifier
- Thyristor Firing

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C

Electrical Ratings

V_{CEO} = 12V V_{CBO} = 20V, V_{EEO} = 5V, V_{CIO} = 20V,
$I_C = I_E$ = 100mA
Power dissipation 500mW

Thermal Ratings

Storage temperature −55°C to +175°C
Junction operating temperature +175°C

All electrical ratings apply to individual transistors; thermal ratings apply to total package dissipation.

The collector of each transistor of the SL3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and to provide normal transistor operation. To avoid undesired coupling, the substrate (pin 5) should be maintained at either DC or signal (AC) earth.

ELECTRICAL CHARACTERISTICS @ T_A = 22°C ±2°C

Characteristic	Symbol	Value			Units	Condition
		Min.	Typ.	Max.		
Co' ector-base breakdown	BV_{CBO}	20	50		V	I_C = 100μA, I_E = 0
Collector-emitter breakdown	BV_{CEO}	12	20		V	I_C = 1mA, I_B = 0
Collector-substrate breakdown	BV_{CIO}	20	70		V	I_{CI} = 100μA, I_E = 0 I_B = 0
Emitter-base breakdown	BV_{EBO}	5	5.6		V	I_E = 500μA, I_C = 0
Collector cut off current	I_{CEO}			10	μA	V_{CE} = 10V, I_B = 0
Collector cut off current	I_{CBO}			1	μA	V_{CB} = 10V, I_E = 0
DC forward current transfer ratio	h_{FE}	40	120			V_{CE} = 3V I_C = 10mA
DC forward current transfer ratio	h_{FE}	40	80			V_{CE} = 3V I_C = 50mA
Base emitter voltage	$V_{BE\ (ON)}$	0.65	0.74	0.85	V	V_{CE} = 3V I_C = 10mA
Collector emitter saturation	$V_{CE\ (SAT)}$		0.4	0.7	V	I_C = 50mA, I_B = 5mA
FOR TRANSISTORS T1 AND T2 (As a differential amplifier)						
Input offset voltage	ΔV_{BE}		1.2	5	mV	V_{CE} = 3V
Input offset current	I_{10}		0.7	2.5	μA	I_C = 1mA

PLESSEY
SEMICONDUCTORS

SL3000 SERIES
TRANSISTOR ARRAYS

SL3127C
HIGH FREQUENCY NPN TRANSISTOR ARRAY

The SL3127 consists of five general-purpose silicon NPN transistors on a common substrate. The monolithic construction provides close electrical and thermal matching of the five transistors. Each of the transistors exhibits a low noise figure (3.6 dB typ. @ 60 MHz) and a value of f_T greater than 1.5 GHz. Each of the transistors is individually accessible and a separate substrate connection is provided, which is used to ensure isolation between each transistor.

The SL3127 is pin compatible with RCA CA3127E.

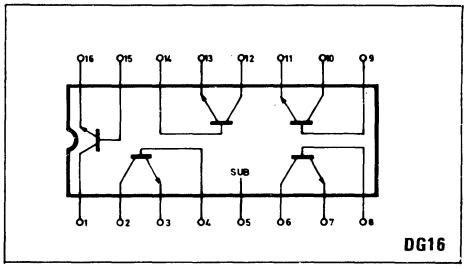


Fig. 1 Pin connections, top view

ABSOLUTE MAXIMUM RATINGS at $T_A = 25°C$

Power dissipation	
Any one transistor	150mW
Total package	300mW
Ambient temperature range	
Storage	−55 to +150°C
Operating	−55 to 125°C

The following limiting values apply to each device:

Collector to emitter voltage V_{CEO}	15V
Collector to base voltage V_{CBO}	20V
Collector to substrate V_{CIO}*	20V
Collector current I_C	20mA

*The collector of each transistor is isolated from the substrate by an integral diode. The substrate (pin 5) must be connected to the most negative point in the external circuit to maintain isolation between the transistors.

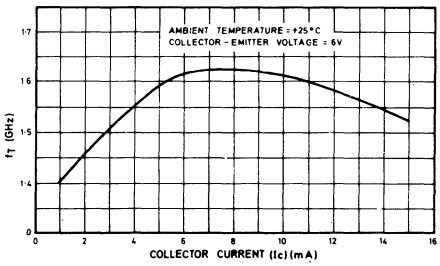


Fig. 2 Typical gain-bandwidth product (f_T) V. collector current

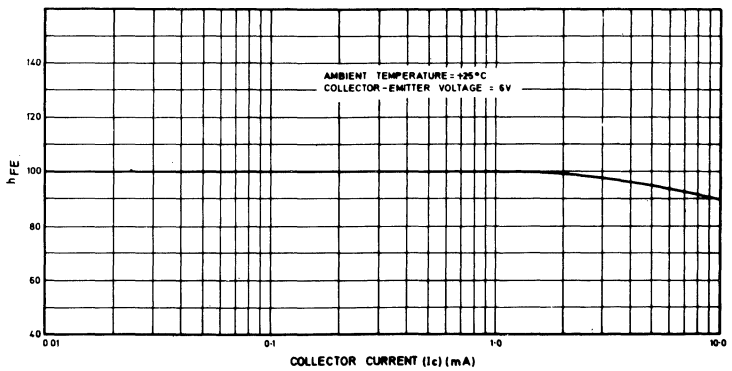


Fig. 3 DC forward current transfer ratio v. collector current

ELECTRICAL CHARACTERISTICS at T_A = +25°C for each transistor

Static characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max		
Collector-base breakdown voltage	BV_{CBO}	20	30		V	I_C = 1μA, I_E = 0
Collector-emitter breakdown voltage	BV_{CEO}	15	18		V	I_C = 1μA, I_B = 0
Collector-substrate breakdown voltage	BV_{CIO}	20	55		V	I_C = 1μA, I_B = 0, I_E = 0
Emitter-base breakdown voltage	BV_{EBO}	4.5	5.5		V	I_E = 10μA, I_C = 0
DC forward current transfer ratio	h_{FE}					V_{CE} = 6V
		40	95			I_C = 5mA
		40	100			I_C = 1mA
		40	100			I_C = 0.1mA
Base-emitter voltage	V_{BE}	0.64	0.74	0.84	V	V_{CE} = 6V, I_C = 1mA
Collector-emitter saturation voltage	$V_{CE(SAT)}$		0.26	0.5	V	I_C = 10mA, I_B = 1mA
Magnitude of difference in V_{BE}	ΔV_{BE}		0.5	5	mV	V_{CE} = 6V, I_C = 1mA
Magnitude of difference in I_B	ΔI_B		0.02	3	μA	V_{CE} = 6V, I_C = 1mA

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Gain-bandwidth product	f_T		1.6		GHz	V_{CE} = 6V, I_C = 5mA
Noise Figure	NF		3.6		dB	V_{CE} = 6V, R_S = 200Ω
						f = 60MHz, I_C = 2mA
Knee of I/f noise figure curve	–		<1		kHz	V_{CE} = 6V, R_S = 200Ω
						I_C = 2mA

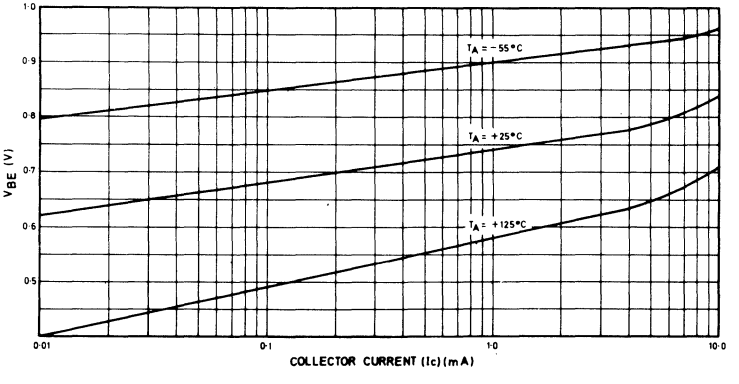


Fig. 4 Base-emitter voltage (V_{BE}) v. collector current

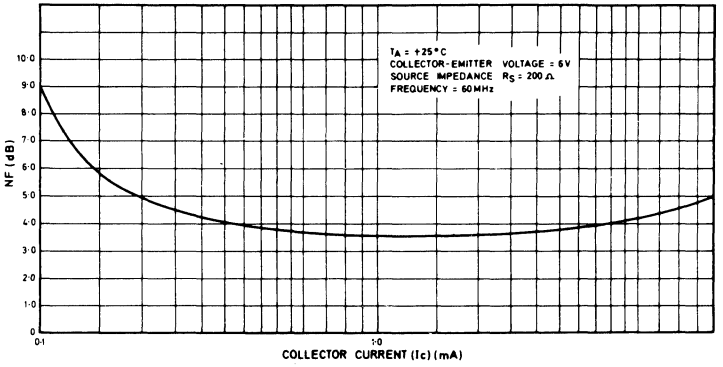


Fig. 5 Noise figure v. collector current

PLESSEY
SEMICONDUCTORS

SL300 SERIES
MATCHED TRANSISTORS

SL3145C
2·5 GHz TRANSISTOR ARRAY

The SL3145 is a monolithic array of five general purpose high frequency transistors arranged as a differential pair and three isolated transistors.

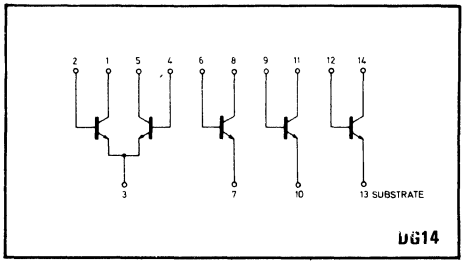


Fig. 1 Schematic and pin diagram

FEATURES

- f_T = 2.5 GHZ
- Wideband Noise Figure = 3dB
- V_{BE} Matching = Better than 5 mV
- Pin-Compatible with SL3045

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

T_{amb} = +25°C ±5°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Base-Isolation Voltage	10			V	I_B = 1μA
Emitter-base breakdown	5			V	I_C = 10μA
Collector-emitter breakdown	8	15		V	I_C = 10μA
Collector-base breakdown	12	24		V	I_E = 10μA
Collector-substrate breakdown	20	40		V	I_C = 10μA
Base-emitter voltage		0.73		V	V_{CE} = 2V, I_C = 1mA
Static forward current transfer ratio	30	80			V_{CE} = 2V, I_C = 1mA
Input offset current (differential pair)		0.2	2	μA	V_{CE} = 2V, I_C = 1mA
Input offset voltage (differential pair)		0.35	5	mV	V_{CE} = 2V, I_C = 1mA
Input offset voltage (others)		0.45	5	mV	V_{CE} = 2V, I_C = 1mA
Temperature coefficient input offset voltage		2		μV/°C	V_{CE} = 2V, I_C = 1mA
Temperature coefficient base emitter voltage		1.6		mV/°C	V_{CE} = 2V, I_C = 1mA
Wideband noise figure		3.0		dB	V_{CE} = 2V, I_C = 100μA R_S = 1kΩ
Gain-Bandwidth product		2.5		GHz	V_{CE} = 2V, I_C = 10mA
$V_{CE(SAT)}$		0.35		V	I_C = 10mA, I_B = 1mA
$V_{BE(SAT)}$		0.95		V	I_C = 10mA, I_B = 1mA
I_{CBO}		0.3		nA	V_{CB} = 16V
I_{CIO}		0.6		nA	V_{CI} = 20V
I_{BIO}		1.2		nA	V_{BI} = 10V
C_{eb}		0.4		pF	Bias = 0V
C_{cb}		0.4		pF	Bias = 0V
C_{cl}		0.8		pF	Bias = 0V

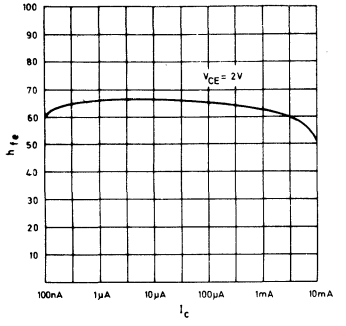


Fig. 2 Typical variation of h_{fe} with I_c

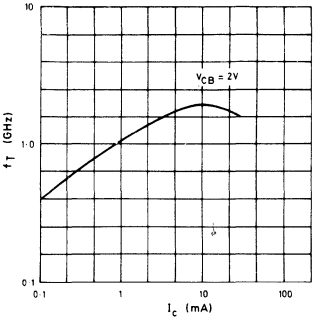


Fig. 3 Typical f_T v. collector current ($f_T = f/h_{fe}$, f = 200MHz)

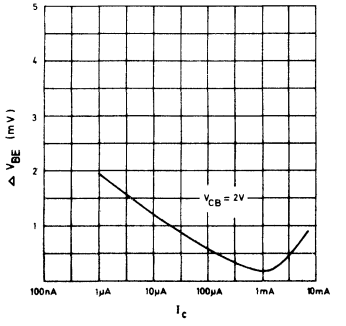


Fig. 4 Typical V_{BE} mismatch v. I_C

ABSOLUTE MAXIMUM RATINGS

Storage temperature:		−55°C to +150°C
Junction operating temperature:		150°C
V_{CBO}: 12V	V_{EBO}: 5V	I_C :20mA
V_{CEO}: 8V	V_{CIO}: 20V	
Maximum individual transistor dissipation:		200mW
Total package dissipation:		350mW

PLESSEY
SEMICONDUCTORS

SL3000 SERIES
TRANSISTOR ARRAYS

SL3146A, SL3146C
SL3183A, SL3183C
HIGH VOLTAGE TRANSISTOR ARRAYS

The Plessey Semiconductors SL3146A, SL3146, SL3183A and SL3183 are general-purpose high-voltage silicon NPN transistor arrays on a common monolithic substrate.

SL3146A and SL3146 (high voltage versions of SL3046) each consist of five transistors with two of the transistors connected to form a differential pair. These types are recommended for use in the DC to VHF range. The SL3146A and SL3146 are supplied in either 14 lead plastic DIL package (temperature range −40°C to +85°C) or 14-lead ceramic DIL package (temperature range −55°C to +125°C).

SL3183A and SL3183 consist of five high-current transistors with independent connections for each transistor. In addition, two of these transistors (TR1 and TR2) are matched at low current (i.e. 1mA) for applications where offset parameters are of special importance. A special substrate terminal is also included for greater flexibility in circuit design. The SL3183A and SL3183 are high-voltage versions of the SL3083 and are supplied in either 16-lead plastic DIL package (temperature range −40°C to +85°C) or 16-lead ceramic package (temperature range −55°C to +125°C).

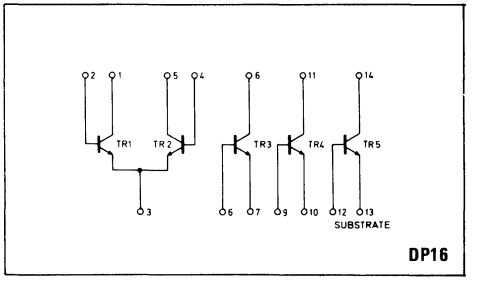


Fig. 1 SL3146/A pin connections

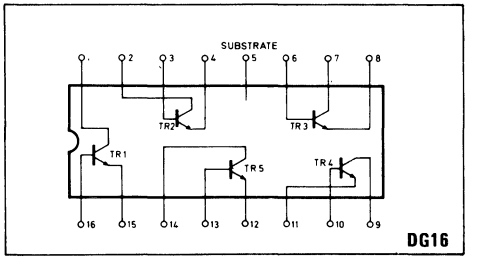


Fig. 2 SL3183/A pin connections

FEATURES

- Matched General Purpose Transistors
- V_{BE} Matched to ±5mV Max.
- Operation from DC to 120MHz (SL3146/A)
- Low Noise Figure: 3.2dB Typ. @ 1kHz (SL3146/A)
- High I_C: 75mA Max. (SL3183/A)

APPLICATIONS

- Signal Processing Systems, DC – VHF
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- Lamp and Relay Drivers (SL3183/A)
- Thyristor Firing (SL3183/A)

ELECTRICAL CHARACTERISTICS @ T_A = +25°C (SL3146/A)

Static Characteristics

Characteristic	Symbol	Value						Units	Test Conditions
		SL3146A			SL3146C				
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Collector-base breakdown	BV_{CBO}	50	72		40	72		V	I_C = 10μA, I_E = 0
Collector-emitter breakdown	BV_{CEO}	40	56		30	56		V	I_C = 1mA, I_B = 0
Collector-substrate breakdown	BV_{VIO}	50	72		40	72		V	I_{CI} = 10μA, I_E = 0, I_B = 0
Emitter-base breakdown	BV_{EBO}	5	7.5		5	7.5		V	I_E = 10μA, I_C = 0
Collector cut-off current	I_{CEO}			5			5	μA	V_{CE} = 10V, I_B = 0
Collector cut-off current	I_{CBO}			100			100	nA	V_{CE} = 10V, I_E = 0
DC forward current transfer ratio	h_{FE}		85			85		–	I_C = 10mA
		30	100		30	100		–	I_C = 10μA V_{CE} = 5V
			90			90		–	I_C = 1mA
Base-emitter voltage	$V_{BE(ON)}$	0.63	0.73	0.83	0.63	0.73	0.83	V	V_{CE} = 3V, I_C = 1mA
Collector-emitter saturation	$V_{CE(SAT)}$		0.33			0.33		V	I_C = 10mA, I_B = 1mA
For Transistors TR1 and TR2 (as a Differential Amplifier)									
Input offset voltage	ΔV_{BE}		0.48	0.5		0.48	0.5	mV	V_{CE} = 5V, I_E = 1mA
Base-emitter temperature coefficient	$\frac{\partial V_{BE(ON)}}{\partial T}$		1.9			1.9		mV/°C	V_{CE} = 5V, I_E = 1mA
Input offset voltage temperature coefficient	$\frac{\partial \Delta V_{BE}}{\partial T}$		1.1			1.1		μV/°C	V_{CE} = 5V, I_{C1} = I_{C2} = 1mA
Input offset current	I_{IO}		0.3	2		0.3	2	μA	V_{CE} = 5V, I_{C1} = I_{C2} = 1mA

Dynamic Characteristics

Low frequency noise figure	NF		3.25			3.25		dB	f = 1kHz, V_{CE} = 5V, I_C = 100μA, R_S = 1kΩ
Low Frequency Small Signal Equivalent Circuit Characteristics									
Forward current transfer ratio	h_{fe}		100			100		–	f = 1kHz, V_{CE} = 5V, I_C = 1mA
Short-circuit input impedance	h_{ie}		2.7			3.5		kΩ	
Open-circuit output admittance	h_{oe}		15.6			15.6		μmho	
Open-circuit reverse voltage transfer ratio	h_{re}		1.8×10^{-4}			1.8×10^{-4}		–	
Admittance Characteristics									
Forward transfer admittance	Y_{fe}		31–j1.5			31–j1.5		mmho	f = 1MHz, V_{CE} = 5V, I_C = 1mA
Input admittance	Y_{ie}		0.35+j0.04			0.35+j0.04		mmho	
Output admittance	Y_{oe}		0.001+j0.03			0.001+j0.03		mmho	
Reverse transfer admittance	Y_{re}		0.001–j0.001			0.001–j0.001		mmho	
Gain bandwidth product	f_t	300	500		300	500		MHz	V_{CE} = 5V, I_C = 3mA
Emitter-base capacitance	C_{BE}		0.7			0.7		pF	V_{EB} = 5V, I_E = 0
Collector-base capacitance	C_{OB}		0.37			0.37		pF	V_{CB} = 5V, I_C = 0
Collector-substrate capacitance	C_{C1}		2.2			2.2		pF	V_{CI} = 5V, I_C = 0

ELECTRICAL CHARACTERISTICS @ T_A = +25°C (SL3183/A)

Static Characteristics

Characteristic	Symbol	Value						Units	Conditions
		SL3183A			SL3183C				
		Min.	Typ.	Max.	Min.	Typ.	Max.		
For each transistor									
Collector-base breakdown voltage	BV_{CBO}	50			40			V	I_C = 100μA, I_E = 0
Collector-emitter breakdown voltage	BV_{CEO}	40			30			V	I_C = 1mA, I_B = 0
Collector-substrate breakdown voltage	BV_{CIO}	50			40			V	I_{CI} = 100μA, I_B = 0, I_E = 0
Emitter-base breakdown voltage	BV_{EBO}	5			5			V	I_E = 500μA, I_C = 0
Collector cut-off current	I_{CEO}			10			10	μA	V_{CE} = 10V, I_B = 0
Collector cut-off current	I_{CBO}			1			1	μA	V_{CE} = 10V, I_E = 0
DC forward current transfer ratio	h_{FE}	40			40				V_{CE} = 3V, I_C = 10mA
		40			40				V_{CE} = 5V, I_C = 50mA
Base-emitter voltage	V_{BE}	0.65	0.75	0.85	0.65	0.75	0.85	V	V_{CE} = 3V, I_C = 10mA
Collector-emitter saturation voltage	*$V_{CE(SAT)}$		1.7	3.0		1.7	3.0	V	I_C = 50mA, I_B = 5mA
For transistors TR1 and TR2 (as a differential amplifier)									
Absolute input offset voltage	$\lvert V_{IO} \rvert$		0.47	5.0		0.47	5.0	mV	V_{CE} = 3V, I_C = 1mA
Absolute input offset current	$\lvert I_{IO} \rvert$		0.78	2.5		0.78	2.5	μA	V_{CE} = 3V, I_C = 1mA

*A maximum dissipation of 5 transistors x 150mW = 750mW is possible for a particular application.

ABSOLUTE MAXIMUM RATINGS @ T_A = 25°C

	SL3146C	SL3146A	SL3183C	SL3183A	
Power dissipation (per transistor)	300	300	500	500	mW
Power dissipation (total package)					
Up to +55°C	750	750	750	750	mW
Above +55°C		Derate linearity 6 - 67			mW/°C
Operating temperature range					
Plastic package	−40 to +85	−40 to +85	−40 to +85	−40 to +85	°C
Ceramic package	−55 to +125	−55 to +125	−55 to +125	−55 to +125	°C
Storage temperature range					
Plastic package	−65 to +150	−65 to +150	−65 to +150	−65 to +150	°C
Ceramic package	−65 to +175	−65 to +175	−65 to +175	−65 to +175	°C
The following ratings apply to individual transistors					
Collector-emitter voltage, V_{CEO}	30	40	30	40	V
Collector-base voltage, V_{CBO}	40	50	40	50	V
Collector-substrate voltage, V_{CIO}	40	50	40	50	V
Emitter-base coltage, V_{EBO}	5	5	5	5	V
Collector current, I_C	50	50	75	75	mA
Base current, I_B			20	20	mA

*The collector of each transistor is isolated from the substrate by an integral diode.

NOTE: The substrate pin must always be negative with respect to the collectors.

PLESSEY
Semiconductors

TELECOMMUNICATIONS

CIRCUIT

TAB1042

QUAD PROGRAMMABLE OPERATIONAL AMPLIFIER

The TAB1042 is an advanced bipolar integrated circuit containing four separate programmable operational amplifiers. The four amplifiers are programmed by current into a common bias pin which determines the main characteristics of each amplifier, supply current, frequency response and slew rate.

For example, with a suitable choice of bias current, the TAB1042 will perform in a manner similar to four amplifiers of the 741 type, but with improved frequency response and input characteristics.

The TAB1042 is especially suitable for use in active filter applications.

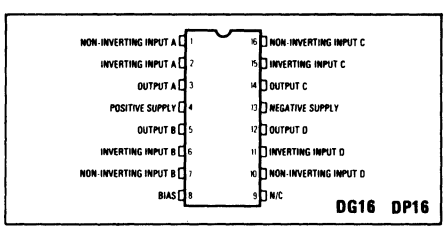


Fig. 1 Pin connections

FEATURES

- Four Independent Op. Amps. in One Package
- Internally Compensated
- Wide Range of Supply Voltages from ±1.5V to ±12V
- No Latch-Up
- Programmable Over 100:1 Current Range
- Gain Bandwidth Product Up to 4MHz
- Built-In Short Circuit Protection

APPLICATIONS

- Active Filters
- Oscillators
- Low Voltage Amplifiers

QUICK REFERENCE DATA

- Supply Voltages ±1.5V to ±12V
- Supply Current ±40μA to ±2mA
- Operating Frequency Range 1MHz
- Gain 95dB

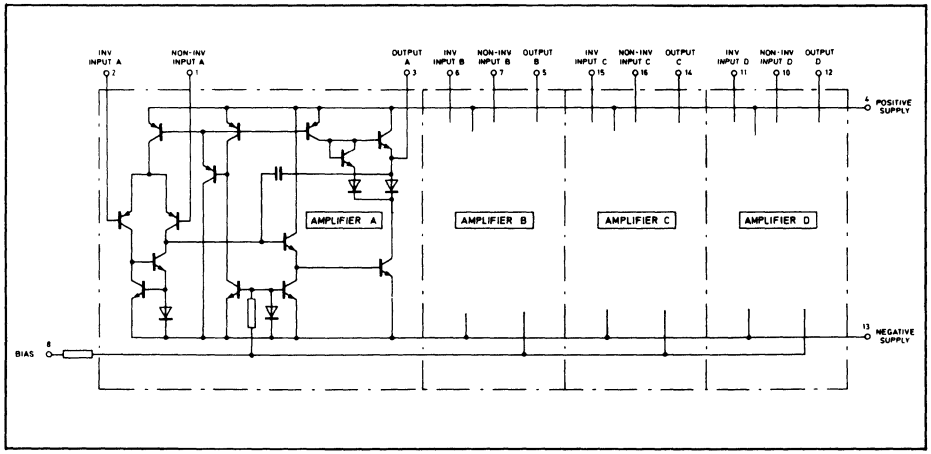


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 25°C
Operating mode A: Supply volts ±12V Bias set current 75µA
Operating mode B: Supply volts ±12V Bias set current 1µA
Operating mode C: Supply volts ±1.5V Bias set current 1µA

Characteristics	Operating Mode									Units	Conditions
	A			B			C				
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input offset voltage		1	5		1	5		1	5	mV	Rs 10kΩ
Input offset current		20	200		5	50		5	50	nA	
Input bias current		250	500		30	100		30	100	nA	
Input resistance	0.1	0.6		0.5	2		0.5	2		MΩ	
Supply current	1000	1600	2200		42		20	40	60	µA	
Large signal volt gain	74	95		66	90		66	90		dB	RL = 4kΩ(A) RL=100kΩ (B) RL=100kΩ (C)
Input voltage range	10	10.5		10	10.5		0.2	0.4		±V	Rs 10kΩ
Common mode rejection ratio	70	110			82			82		dB	
Output voltage swing	9	10.8		9	10.8		0.2	0.3		±V	RL=4kΩ(A) RL=100kΩ(B) RL=4kΩ(C)
Supply voltage rejection ratio	75	96		75	86		75	86		dB	Rs 10kΩ
Short circuit current	2.5	4		0.1	0.25			0.22		mA	Tamb 0°C to 70°C
Gain bandwidth product		3.5			50			50		kHz MHz	Gain=20dB
Slew rate		1.5			0.02			0.02		V/µs	Gain=20dB

OPERATING NOTES

Bias set current

The amplifiers are programmed by the I_{SET} current into the BIAS pin to determine the frequency response, slew rate and the value of supply current. The relationship is summarised as follows:

Gain bandwidth product	I_{SET} x 50kHz
Power supply current (each supply)	I_{SET} x 25µA
Slew rate	I_{SET} x 0.02 V/µs (I_{SET} in µA)

The open loop voltage gain is largely unaffected by change in bias set current but tends to peak slightly at 10µA.

Since the voltage on the BIAS pin is approximately 0.65V more positive than the negative supply, a resistor may be connected between the bias pin and either 0V or the positive supply to set the current. Thus, if the resistor is connected to 0V, the I_{SET} current is determined by:

$$I_{SET} = \frac{Vs - 0.65}{R}$$

where R is value of the 'set' resistor.

The output goes high if the non-inverting input is taken lower than 1V above the negative power supply.

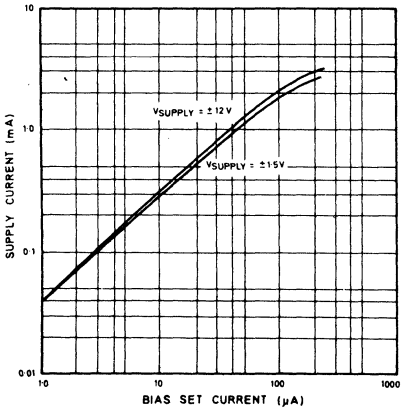


Fig. 3 Supply current (each supply) v. bias set current

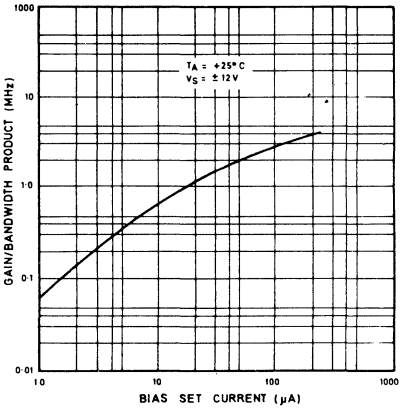


Fig. 4 Gain bandwidth product v. I_{SET}

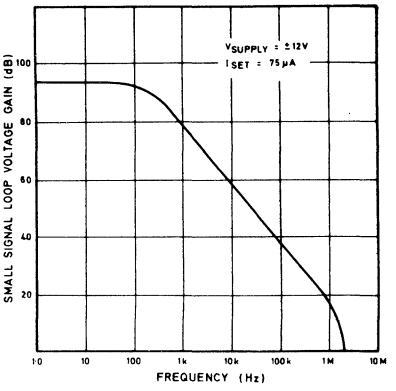


Fig. 5 Typical frequency response

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±15V
Common mode input voltage	Not greater than supplies
Differential input voltage	±25V
Bias set current	10mA
Storage and junction temperature	55°C to +150°C
Power dissipation	800mW at 25°C
	Derate at 7mW/°C above 25°C

TAB 1043

QUAD PROGRAMMABLE OPERATIONAL AMPLIFIER

The TAB1043 is an advanced bipolar integrated circuit containing four separate operational amplifiers. The amplifiers are programmed by current into the appropriate bias pin. Pin 8 (Bias 2) programmes amplifiers B, C and D and pin 16 (Bias 1) programmes amplifier A.

For example, with a suitable choice of bias current, the TAB1043 will perform in a manner similar to four amplifiers of the 741 type, but with improved frequency response and input characteristics.

The TAB1043 is especially suitable for use in active filter applications.

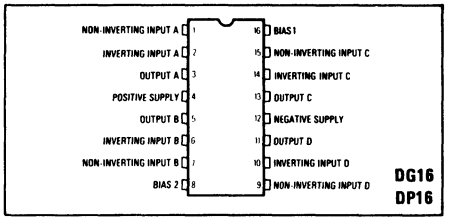


Fig. 1 Pin connections

FEATURES

- Four Independent Op. Amps. in One Package
- Internally Compensated
- Wide Range of Supply Voltages from ±1.5V to ±12V
- No Latch-Up
- Programmable Over 100:1 Current Range
- Gain Bandwidth Product Up to 4MHz
- Built-In Short Circuit Protection

APPLICATIONS

- Active Filters
- Oscillators
- Low Voltage Amplifiers

QUICK REFERENCE DATA

- Supply Voltages ±1.5V to ±12V
- Supply Current ±40μA to ±2mA
- Operating Frequency Range 1MHz
- Gain 95dB

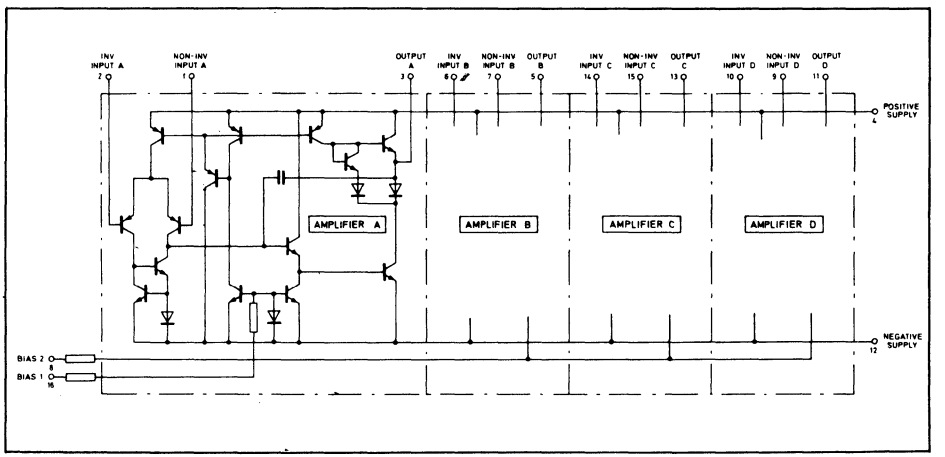


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 25°C
Operating mode A: Supply volts ±12V Bias set current 75μA
Operating mode B: Supply volts ±12V Bias set current 1μA
Operating mode C: Supply volts ±1.5V Bias set current 1μA
} sum of currents into pins 8 and 16

Characteristics	Operating Mode									Units	Conditions
	A			B			C				
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input offset voltage		1	5		1	5		1	5	mV	Rs 10kΩ
Input offset current		20	200		5	50		5	50	nA	
Input bias current		250	500		30	100		30	100	nA	
Input resistance	0.1	0.6		0.5	2		0.5	2		MΩ	
Supply current	1000	1600	2200		42		20	40	60	μA	
Large signal volt gain	74	95		66	90		66	90		dB	RL = 4kΩ(A) RL=100kΩ (B) RL=100kΩ (C)
Input voltage range	10	10.5		10	10.5		0.2	0.4		±V	Rs 10kΩ
Common mode rejection ratio	70	110			82			82		dB	
Output voltage swing	9	10.8		9	10.8		0.2	0.3		±V	RL=4kΩ(A) RL=100kΩ(B) RL=4kΩ(C)
Supply voltage rejection ratio	75	96		75	86		75	86		dB	Rs 10kΩ
Short circuit current	2.5	4		0.1	0.25			0.22		mA	Tamb 0°C to 70°C
Gain bandwidth product		3.5			50			50		kHz MHz	Gain=20dB
Slew rate		1.5			0.02			0.02		V/μs	Gain=20dB

OPERATING NOTES

Bias set current

The amplifiers are programmed by the I_{SET} current into the BIAS pins to determine the frequency response, slew rate and the value of supply current. The relationship is summarised as follows, where I_{SET} is the total set current into pins 8 and 16:

Gain bandwidth product	I_{SET} x 50kHz
Power supply current (each supply)	I_{SET} x 25μA
Slew rate	I_{SET} x 0.02 V/μs (I_{SET} in μA)

The open loop voltage gain is largely unaffected by change in bias set current but tends to peak slightly at 10μA.

Since the voltage on either BIAS pin is approximately 0.65V more positive than the negative supply, a resistor may be connected between the bias pin and either 0V or the positive supply to set the current. Thus, if the resistor is connected to 0V, the I_{SET} current is determined by:

$$I_{SET} = \frac{Vs - 0.65}{R}$$

where R is value of the 'set' resistor.

The output goes high if the non-inverting input is taken lower than 1V above the negative power supply.

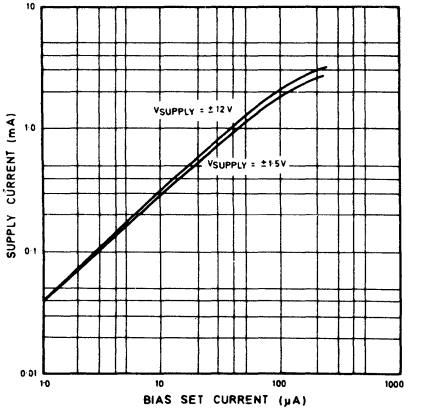


Fig. 3 Supply current (each supply) v. bias set current

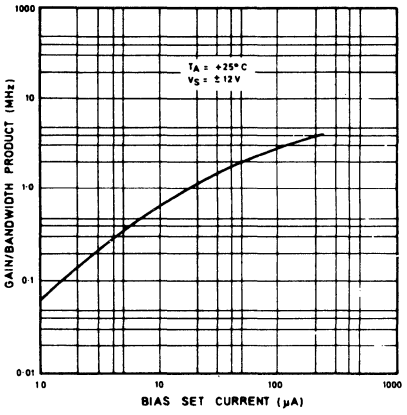


Fig. 4 Gain bandwidth product v. I_{SET}

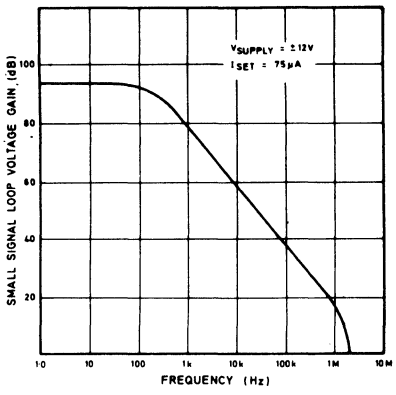


Fig. 5 Typical frequency response

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±15V
Common mode input voltage	Not greater than supplies
Differential input voltage	±25V
Bias set current	10mA each pin
Storage and junction temperature	55°C to +150°C
Power dissipation	800mW at 25°C
	Derate at 7mW/°C above 25°C

TAB 1044

QUAD PROGRAMMABLE OPERATIONAL AMPLIFIER

The TAB1044 is an advanced bipolar integrated circuit containing four separate programmable operational amplifiers. The four amplifiers are programmed by current into a common bias pin which determines the main characteristics of each amplifier, supply current, frequency response and slew rate.

The TAB1044 is similar to the TAB1042 but has an exceptionally high short circuit current, making it particularly suitable for driving capacitive loads.

The TAB1044 is especially suitable for use in active filter applications.

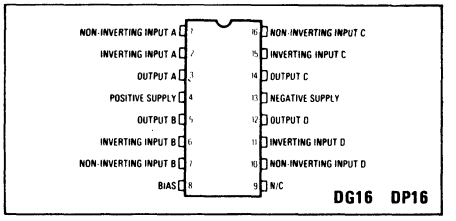


Fig. 1 Pin connections

FEATURES

- Four Independent Op. Amps. in One Package
- Internally Compensated
- Wide Range of Supply Voltages from ±3.0V to ±12V
- No Latch-Up
- Programmable Over 100:1 Current Range
- Gain Bandwidth Product Up to 4MHz
- Built-In Short Circuit Protection

APPLICATIONS

- Active Filters
- Oscillators
- Low Voltage Amplifiers

QUICK REFERENCE DATA

- Supply Voltage ±3.0V to ±12V
- Supply Current ±200μA to ±2mA
- Operating Frequency Range 1MHz
- Gain 95dB

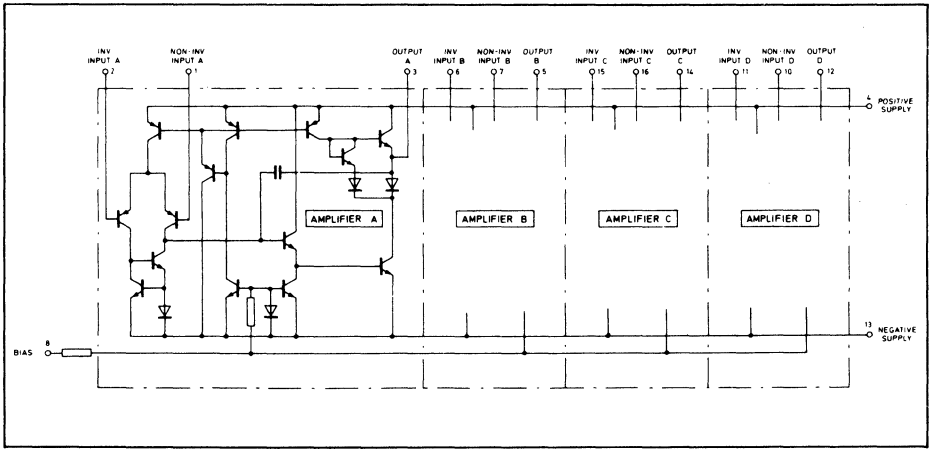


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 25°C
Operating mode A:Supply volts ±12V Bias set current 75µA
Operating mode B:Supply volts ±12V Bias set current 1µA
Operating mode C:Supply volts ±3.0V Bias set current 1µA

Characteristics	Operating Mode									Units	Conditions
	A			B			C				
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input offset voltage		1	5		1	5		1	5	mV	Rs 10kΩ
Input offset current		20	200		5	50		5	50	nA	
Input bias current		250	500		30	100		30	100	nA	
Input resistance	0.1	0.6		0.5	2		0.5	2		MΩ	
Supply current	1000	1700	2500		220		100	200	400	µA	
Large signal volt gain	74	95		66	90		66	90		dB	RL = 4kΩ(A) RL=100kΩ (B) RL=100kΩ (C)
Input voltage range	10	10.5		10	10.5		1.5	1.7		±V	Rs 10kΩ
Common mode rejection ratio	70	110			82			82		dB	
Output voltage swing	9	10.5		9	10.5		0.7	0.8		±V	RL=4kΩ(A) RL=100kΩ(B) RL=100Ω(C)
Supply voltage rejection ratio	75	96		75	86		75	86		dB	Rs 10kΩ
Short circuit current	12	20		1.1	2.5		1.0	2.2		mA	Tamb 0°C to 70°C
Gain bandwidth product		3.5			50			50		kHz MHz	Gain=20dB
Slew rate		1.5			0.02			0.02		V/µs	Gain=20dB

OPERATING NOTES

Bias set current

The amplifiers are programmed by the I_{SET} current into the BIAS pin to determine the frequency response, slew rate and the value of supply current. The relationship is summarised as follows:

Gain bandwidth product	I_{SET} x 50kHz
Power supply current (each supply)	(I_{SET} x 25) + 200µA
Slew rate	I_{SET} x 0.02 V/µs (I_{SET} in µA)

The open loop voltage gain is largely unaffected by change in bias set current but tends to peak slightly at 10µA.

Since the voltage on the BIAS pin is approximately 0.65V more positive than the negative supply, a resistor may be connected between the bias pin and either 0V or the positive supply to set the current. Thus, if the resistor is connected to 0V, the I_{SET} current is determined by:

$$I_{SET} = \frac{Vs - 0.65}{R}$$

where R is value of the 'set' resistor.

The output goes high if the non-inverting input is taken lower than 1V above the negative power supply.

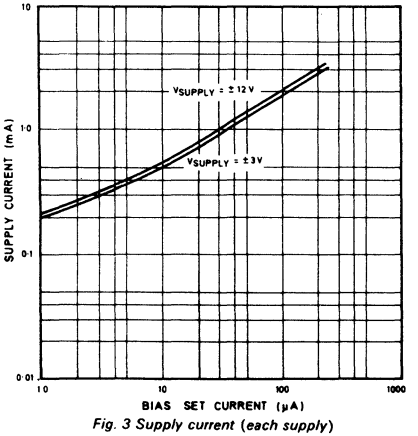


Fig. 3 Supply current (each supply) v. bias set current

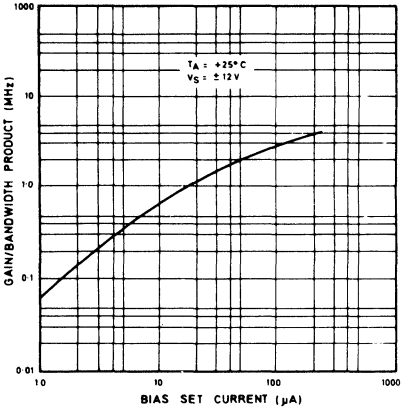


Fig. 4 Gain bandwidth product v. I_{SET}

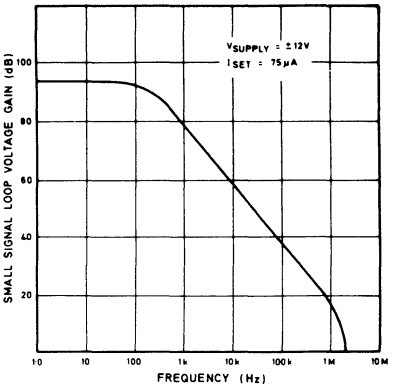


Fig. 5 Typical frequency response

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±15V
Common mode input voltage	Not greater than supplies
Differential input voltage	±25V
Bias set current	10mA each pin
Storage and junction temperature	55°C to +150°C
Power dissipation	800mW at 25°C
	Derate at 7mW/°C above 25°C

PLESSEY
Semiconductors

NOVOL
NON-VOLATILE LOGIC

MN9102

NON-VOLATILE QUAD LATCH

The Plessey MN9102 is a non-volatile 4-bit data latch which uses MNOS transistors as memory elements to retain stored data in the absence of applied power. The data that is applied to the four inputs is written into the memory when the $\overline{SAVE}$ control is taken to a logic '0' level and the data subsequently appears on the four outputs. The stored data is also automatically restored to the outputs whenever power is re-applied to the device.

An OUTPUT ENABLE is also available, which when taken to logic '0' level presents a high impedance state on each data output line, permitting multiplexed operation.

The high voltage usually associated with MNOS memory devices is generated internally, requiring only a single external capacitor to act as a charge reservoir for supplying current when writing into the memory. The device therefore operates from standard voltage rails and requires no additional drive circuitry.

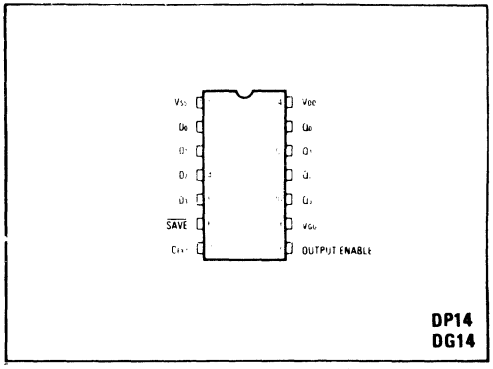


Fig. 1. Pin connections (top)

FEATURES

- Data Retention for One Year at 70°C in the Absence of Applied Power
- Simple to Use
- Standard Power Supplies Only (+5V, −12V)
- CMOS/TTL Compatible
- 14-lead DIL Package

APPLICATIONS

- Metering Systems
- Elapsed Time Indicators
- Security Code Storage
- Last Channel Memory for Digital Tuning

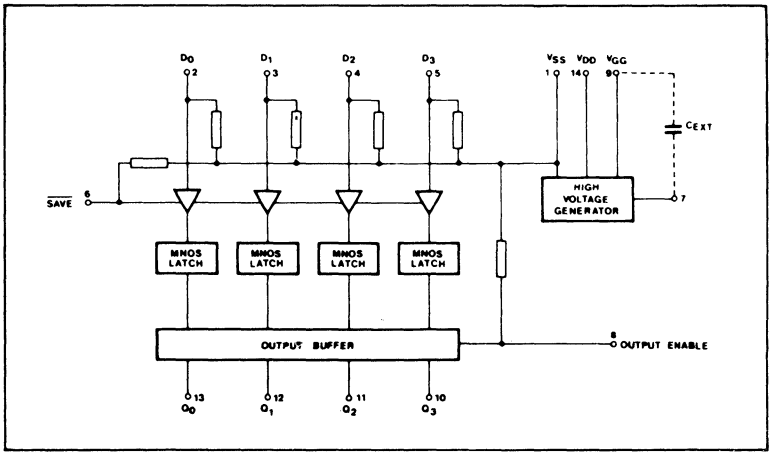


Fig. 2 Block diagram of MN9102

ELECTRICAL CHARACTERISTICS

Operating conditions (unless otherwise stated):

V_{SS} + 5V ± 5%
V_{DD} 0V
V_{GG} −12V ± 5%
Output loading 1 TTL load
Ambient operating temperature range including data retention in the absence of applied power: −40°C to + 85°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Logic '0' input voltage	V_{IL}			0.8	V	Nominal 20k ohms internal pullup
Logic '1' input voltage	V_{IH}	V_{SS}–1			V	resistor to V_{SS} on all inputs
Logic '0' output voltage	V_{OL}			0.4	V	Output current 1.6mA
Logic '1' output voltage	V_{OH}	V_{SS}—1			V	Output current −100 µA
Output leakage current		−10		+10	µA	$V_{SS} \geqslant V_{OUT} \geqslant V_{DD}$ with OUTPUT ENABLE V_{DD}
External reservoir capacitance	C_{EXT}	100		220	nF	
Output voltage on C_{EXT}			−38		V	See note 2
External leakage on C_{EXT}				2.0	µA	
Data set-up time	t_s	1			µs	
Data hold time	t_h	1			µs	
Data settling time	t_d			7	µs	C_{LOAD} = 47pf
Output enable delay	t_o			2.5	µs	C_{LOAD} = 47pf
SAVE time	t_{SAVE}	10			ms	See note 1
SAVE duty cycle				10	%	See note 2
SAVE cycles		10^6				See note 4
SAVE rise and fall times	t_e			10	µs	
Data retention time		12			months	T_{amb} = −40°C to 70°C
		3			months	T_{amb} = −40°C to 85°C
Power dissipation			50	100	mW	See note 3

ABSOLUTE MAXIMUM RATINGS

(all voltages with respect to V_{SS})

Voltage on C_{EXT} −46 to + 0.3V
Voltage on V_{GG} −20 to + 0.3V
Voltage on any other pin −7 to + 0.3V
Storage temperature −55°C to + 125°C
Ambient operating temperature −40°C to + 85°C

The above limits are absolute limiting values beyond which the lifetime and performance of the device may be impaired. No guarantee is implied that the device will function at any condition other than specified under the operating conditions.

OPERATING NOTES

1.
Data can be entered into the latch with SAVE times much less than ten milliseconds, however the retention time is then significantly reduced. It is therefore important that spurious SAVE pulses do not occur, particularly when power is applied to the device.

2.
An external capacitor is required to act as a charge reservoir for the high voltage which is generated on chip from a high impedance source. Excessive external leakage current on this capacitor or exceeding the quoted duty cycle can cause appreciable loading of the high voltage resulting in reduced data retention times. If operation outside of these limits is required, then an external high voltage (−38 volts ± 5%) may be used to maintain the voltage level.

3.
The majority of the power dissipation arises from the current flow between V_{SS} and V_{GG}. The current level on V_{DD} is the sum of the logic '0' level current plus leakage currents.

4.
Exceeding this number of SAVE cycles can cause permanent damage to the device. It should also be noted that rapid changes of data in excess of 10^6 may cause a reduction in the data retention time.

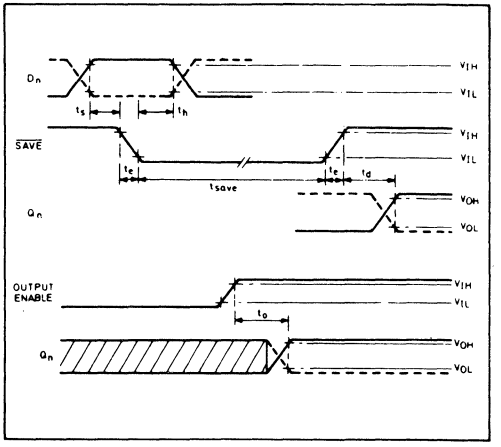


Fig. 3 Timing diagram

ANTI-STATIC PRECAUTIONS

All inputs have suitable protection devices to minimise the possibility of damage due to static discharge. Care should still be taken when handling the device and the leads should at all times be shorted together until actually incorporated in the circuit in which the device is being used. Care should be taken to avoid static charges occurring in the circuit before completion and soldering should be carried out with an earthed bit.

To ensure no damage occurs during transit, the devices are supplied packed in conducting foam or other suitable carriers.

PLESSEY
Semiconductors

NOVOL
NON-VOLATILE LOGIC

MN9105

QUAD DECADE UP/DOWN COUNTER

The Plessey MN9105 is a 4-decade BCD counter which counts up or down on negative transitions of the CLOCK input. In parallel with the counter is a 16-bit non-volatile MNOS memory into which the contents of the counter can be written by holding CLOCK low and then taking $\overline{\text{SAVE}}$ to a low level. When data has been written into the memory, it can be retained even in the absence of applied power, and then subsequently be recalled from the memory to preset the counter.

Also associated with each counter decade is a 4-bit latch, the outputs of which follow the count sequence when $\overline{\text{LOAD}}$ is low. When $\overline{\text{LOAD}}$ goes high, the latches retain the data present at the time of the transition. The outputs from each latch are multiplexed onto a 4-bit data highway under the control of a 2-bit address (MX1, MX2). All four outputs may be put into a high output impedance state by holding $\overline{\text{OUTPUT ENABLE}}$ high, so allowing multiplexed operation between devices.

The final decade has a CARRY output to enable devices to be cascaded in series. An input CLOCK pulse ripples through to the CARRY output when the counter is in the 'up' mode and the '9999' state or when in the 'down' mode and the '0000' state.

The high voltage usually associated with MNOS devices is generated internally, requiring only a single capacitor to act as a charge reservoir for supplying current when writing into the memory. The device therefore operates from standard voltage rails and requires no additional drive circuitry.

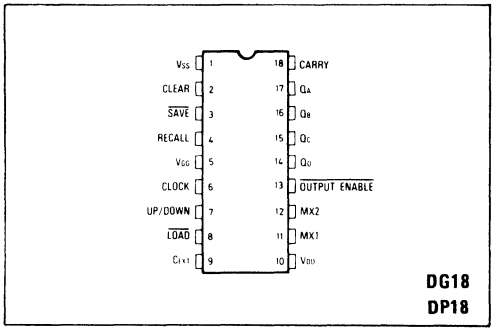


Fig. 1 Pin connections (top)

FEATURES

- Data Retention for One Year at 70°C in the Absence of Applied Power
- DC to 250 kHz Count Frequency
- Up/Down Count Facilities
- Standard Power Supplies (+5V, −12V)
- TTL/CMOS Compatibility
- 18-pin DIL Package

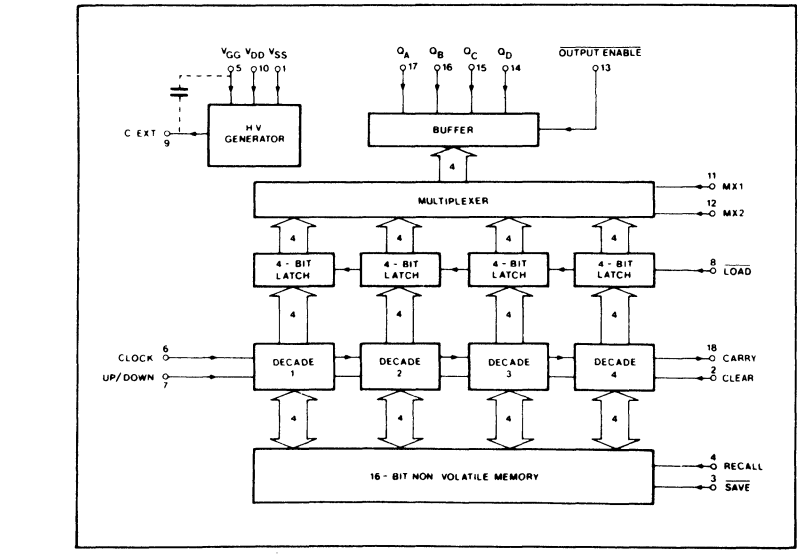


Fig. 2 MN9105 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{SS} + 5V 5%
V_{DD} 0V
V_{GG} —12V 5%
Output loading 1 TTL load
Ambient operating temperature range including data retention in the absence of applied power: —40°C to 85°C

Characteristic	Symbol	Value Min.	Typ.	Max.	Units	Conditions
Logic '0' input voltage	V_{IL}			0.8	V	
Logic '1' input voltage	V_{IH}	V_{SS}–1			V	
Logic '0' output voltage	V_{OL}			0.4	V	Output current = 1.6mA
Logic '1' output voltage	V_{OH}	V_{SS}–1			V	Output current −100µA
Output leakage current		−10		10	µA	$V_{SS} > V_{OUT} > V_{DD}$ with $\overline{\text{OUTPUT ENABLE}}$ V_{SS}
External capacitor	C_{EXT}	0.1		0.22	µF	
Output voltage on C_{EXT}			−38		V	
External leakage on C_{EXT}				2.0	µA	} See Note 3
SAVE duty cycle				10	%	
SAVE cycles		10^6				See Note 2
Data retention time		12			months	T_{amb} = −40°C to 70°C
		3			months	T_{amb} = −40°C to 85°C
Total integrated RECALL time between SAVE cycles		10^6			secs	
Power dissipation			250	500	mW	See Note 1

OPERATING NOTES

1. The majority of the power dissipation arises from current flow between V_{SS} and V_{GG}. The current level on V_{DD} is the sum of the logic '0' level currents plus leakage current only.
2. Exceeding this number of SAVE cycles can cause permanent damage to the device. It should also be noted that rapid changes of data in excess of 10^6 may cause a reduction in the data retention time.
3. An external capacitor is required to act as a charge reservoir for the high voltage which is generated on-chip from a high impedance source. Excessive external leakage on this capacitor or exceeding the quoted duty cycle can cause appreciable loading of the high voltage resulting in reduced data retention times. If operation outside these limits is required then an external high voltage (—38 volts 5%) may be used to maintain the voltage level.
4. The CARRY pulse is equivalent to a CLOCK pulse which ripples through the counter when in the correct count sequence. For CLOCK pulse widths greater than or equal to 5 µs, the CARRY output may be connected directly to the input of a following device. For smaller widths, then pulse stretching must be used on the CARRY output to maintain the pulse width.
5. Data can be entered into the memory with SAVE times much less than 10 milliseconds; however the data retention time is then significantly reduced. It is therefore important that spurious SAVE pulses do not occur particularly when power is applied to the device.

MX2	MX1	$\overline{OE}$	Q_D, Q_C, Q_B, Q_A
*	*	1	High output impedance
0	0	0	Decade 1
0	1	0	Decade 2
1	0	0	Decade 3
1	1	0	Decade 4

$\overline{SAVE}$	CLOCK	CLEAR	RECALL	UP/DOWN	MODE
1	↓	0	0	0	Count up
1	↓	0	0	1	Count down
1	*	↓	0	*	Set counter to 0000
1	*	0	↓	*	Preset counter from memory
0	0	0	0	*	Write into memory

* Logic '0' or '1' level
↓ Logic '1' to '0' transition

Table 1 Function table

ABSOLUTE MAXIMUM RATINGS

(all voltage with respect to V_{SS})

Voltage on C_{EXT} −46 to + 0.3V
Voltage on V_{GG} —20 to + 0.3V
Voltage on any other pin —7 to + 0.3V
Storage temperature —55 C to + 125 C
Ambient operating temperature —40 C to + 85 C

The above limits are absolute limiting values beyond which the lifetime and performance of the device may be impaired. No guarantee is implied that the device will function at any condition other than specified under the operating conditions.

ANTI-STATIC PRECAUTIONS

All inputs have suitable protection devices to minimise the possibility of damage due to static discharge. Care should still be taken when handling the device and the leads should at all times be shorted together until actually incorporated in the circuit in which the device is being used. Care should be taken to avoid static charges occurring in the circuit before completion and soldering should be carried out with an earthed bit.

To ensure no damage occurs during transit, the devices are supplied packed in conducting foam or other suitable carriers.

SWITCHING CHARACTERISTICS

Loading = 1TTL LOAD

C_L = 10pF

Parameter	Symbol	Value			Units	Notes
		Min.	Typ.	Max.		
Clock Frequency				250	KHz	
Up/Down select time	t_s	1			µs	
Clock pulse width	t_p	2			µs	
Clear pulse width	t_c	1			µs	
Recall pulse width	t_r	2			µs	
Save pulse width	t_{save}	10			ms	Note 5
Clear to clock set up time	t_{cp}	2			µs	
Recall to clock set up time	t_{rp}	2			µs	
Clock to load set up time	t_{pl}	2			µs	
Clock to save set up time	t_{ps}	0			µs	
Clear to output delay	t_{cd}			2	µs	
Recall to output delay	t_{rd}			4	µs	
Clock to output delay	t_{pd}			4	µs	
MX1/MX2 to output delay	t_{md}			4	µs	
Load to output delay	t_{ld}			4	µs	
Clock to carry output delay	t_{pc}			4	µs	
Carry output width	t_{cry}	2			µs	t_p = 5µs (Note 4)
Input rise and fall times				10	µs	

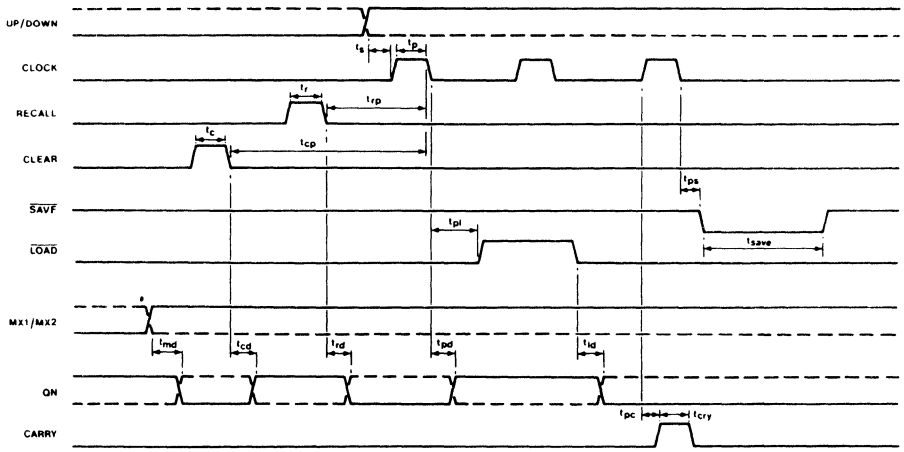


Fig. 3 Timing diagram

PLESSEY
Semiconductors

NOVOL
NON-VOLATILE LOGIC

MN9106/7/8

SIX-DECADE UP COUNTERS

The MN9106 is a six decade up counter in parallel with a twenty four bit MNOS memory which can provide non-volatile data storage of the current count position. An overflow latch and memory bit are also available to indicate a counter overflow condition. In addition to the conventional counter controls, RECALL and $\overline{\text{SAVE}}$ inputs are provided to control the two way transfer of data between the counter and memory.

Output data is presented in the form of multiplexed seven segment outputs and six digit strobes. The multiplexing sequence is controlled by an internal oscillator which may also be forced from an external oscillator on the SCAN input. The device operates from a single 12 volts supply and the higher voltage required for the MNOS memory is provided internally by a generator which requires only a single external capacitor.

The MN9107 and MN9108 are adaptations of the basic device intended specifically for timer applications. Certain decades in these devices have been replaced with divide-by six elements to give the facility of counting hours, minutes and seconds when provided with the correct input frequency.

MN9107 99 hours, 59 minutes, 59 seconds
MN9108 9999 hours, 59 minutes
or 9999 minutes, 59 seconds

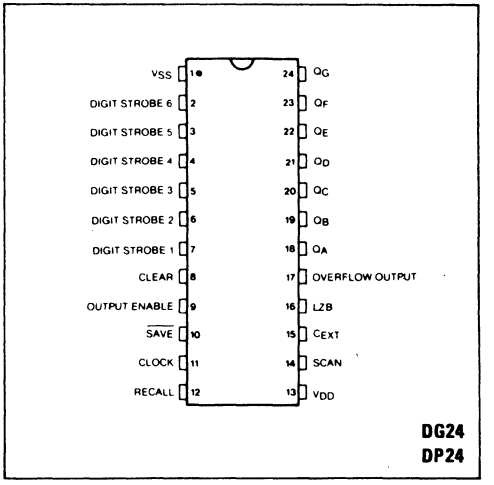


Fig. 1 Pin connections (top)

FEATURES

- Data Retention Guaranteed For One Year In The Absence of Applied Power over Temperature Range of −40°C to +70°C
- DC to 200kHz Count Frequency
- Operation From Single 12V Supply with CMOS Compatible Inputs
- Leading Zero and Full Blanking Facilities
- Multiplexed Seven-Segment Outputs
- Counter Overflow Indicator
- Self Scanning Multiplexing
- Operation from Split Supplies (+5, −7V) Allowing Inputs to Interface with TTL
- Data SAVE Time of 10 Milliseconds.

ABSOLUTE MAXIMUM RATINGS

(all voltages with respect to Vss)

Voltage on C_{EXT} −46V to + 0.3V
Voltage on any other pin −15V to + 0.3V
Storage temperature −55°C to + 125°C
Ambient operating temperature −40°C to + 85°C

The above limits are absolute limiting values beyond which the lifetime and performance of the device may be impaired. No guarantee is implied that the device will function at any condition other than specified under the operating conditions.

ANTI-STATIC PRECAUTIONS

All inputs have suitable protection devices to minimise the possibility of damage due to static discharge. Care should be taken when handling the device and the leads should at all times be shorted together until actually incorporated in the circuit in which the device is being used. Care should be taken to avoid static charges occurring in the circuit before completion and soldering should be carried out with an earthed bit.

To ensure no damage occurs during transit, the devices are supplied packed in conducting foam or other suitable carriers.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{Amb} 40 C to +85 C

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Supply voltage	V_{DD}	V_{SS} 13		V_{SS} 11	V	
Supply current	I_{DD}	6		22	mA	OUTPUT ENABLE = V_{IL} SCAN = open circuit
Logic '0' input voltage	V_{IL}			V_{SS} 4	V	
Logic '1' input voltage	V_{IH}	V_{SS} 1			V	
Input leakage current		−1		+1	μA	$V_{DD} \leq V_{IN} \leq V_{SS}$(Except SCAN input)
Scan input current (Logic '0')		−12			mA	$V_{IN} = V_{SS} - 6$
Scan input current (Logic '1')				+120	μA	$V_{IN} = V_{SS} - 1$
Logic '1' output resistance - segments			150	300	Ω	$V_{OUT} = V_{SS} - 3$
Logic '1' output resistance - overflow			150	300	Ω	$V_{OUT} = V_{SS} - 3$
Logic '1' output resistance digit strobes			500	1000	Ω	$V_{OUT} = V_{SS} - 3$
Logic '0' output leakage current		−10		+1	μA	$V_{DD} \leq V_{OUT} \leq V_{SS}$
Output loading - segments				15	mA	
Output loading - overflow				15	mA	See note 6
Output loading - digit strobes				5	mA	
High voltage output			V_{SS}-40		V	
External reservoir capacitance	C_{EXT}	100		220	nF	
External leakage current on C_{EXT}				2.0	μA	See note 3
Save duty cycle				5	%	
Number of save cycles		10^6				See note 4
Data retention time		12			Months	T_A = 70°C
Data retention time		3			Months	T_A = 85°C
Total integrated RECALL time between SAVE cycles		10^6			secs	
Count frequency	f			200	kHz	
Clock width		2.5			μs	See note 2
Recall width		5			μs	See note 2
Clear width		5			μs	See note 2
Save width		10			ms	See notes 2 and 5
Input rise and fall times				10	μs	
Internal scan frequency			1		kHz	SCAN capacitance 100nF
External scan frequency				25	kHz	

Output Enable	Count Position	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G
0	*	0	0	0	0	0	0	0
1	0	1	1	1	1	1	1	0
1	1	0	1	1	0	0	0	0
1	2	1	1	0	1	1	0	1
1	3	1	1	1	1	0	0	1
1	4	0	1	1	0	0	1	1
1	5	1	0	1	1	0	1	1
1	6	1	0	1	1	1	1	1
1	7	1	1	1	0	0	0	0
1	8	1	1	1	1	1	1	1
1	9	1	1	1	1	0	1	1
1	Invalid†	0	1	1	1	1	1	0

Table 1 — Output function table

Segment identification

* Don't care condition

† Incorrect use of the device may cause invalid BCD characters to appear in the counter.

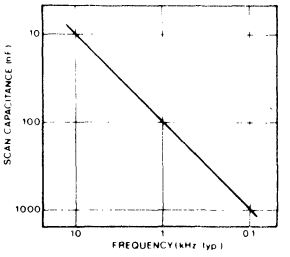


Fig. 2 Scan frequency v. capacitance (typical)

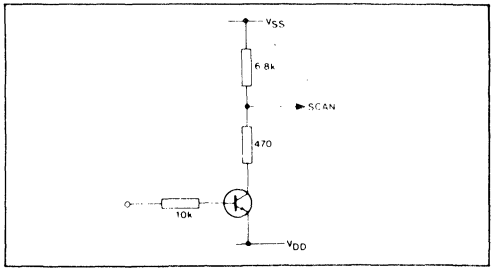


Fig. 3 Typical external drive circuit for SCAN input

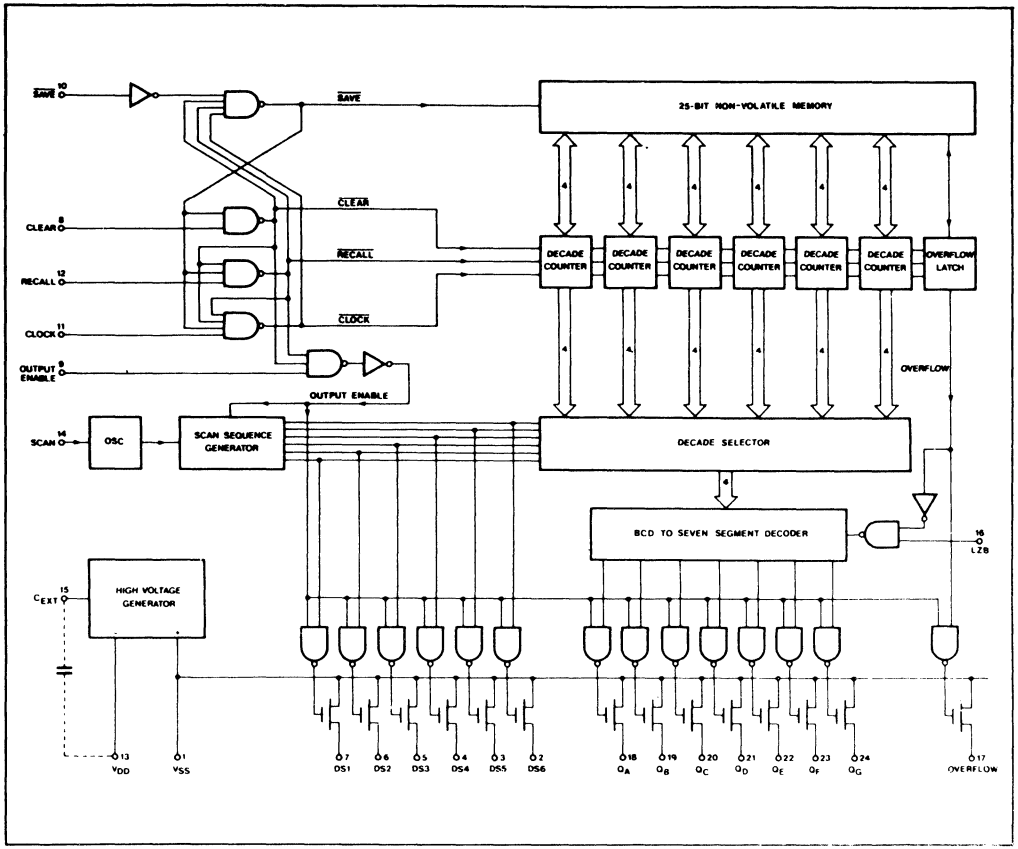


Fig. 4 MN9106 block diagram

OPERATING NOTES

1. The counter is a synchronous six decade counter multiplexed onto a four bit data highway and then decoded into seven segment format which drives open drain MOS transistors. An additional output transistor is also driven directly from the overflow latch.
Multiplexing is provided internally from an oscillator whose frequency is determined by a capacitor between the SCAN input and V_{SS} (Fig.2). This oscillator may also be forced externally from a signal which must be capable of sinking and sourcing current on the SCAN input (Fig.3). The decoded data and the corresponding digit strobe output are available for an entire oscillator period and the multiplex control scans the decades in sequence from most significant (DS6) to least significant (DS1). The scan position changes on negative transitions of the SCAN input.
With OUTPUT ENABLE held at a low level, the blanking facility turns off the segment outputs, the digit strobe outputs and the overflow output. The multiplexing scan sequence is reset to the most significant decade at this time. A similar blanking and reset function also occurs whenever the device is put into recall or clear modes.
With LZB at a high level, leading zeros are blanked provided that the overflow latch is not at a high level. Leading zero blanking is not applicable to the MN9107 and applies only to three most significant decades in the MN9108.

2. Clear mode:— In clear mode the counter and overflow latch are reset to zero, all outputs are turned off and the multiplexing sequence is reset. The device is put into clear mode by taking CLEAR to a high level while $\overline{SAVE}$ is also held high. Once the clear function has begun, any subsequent changes on the $\overline{SAVE}$ input are inhibited. RECALL and CLOCK inputs are always inhibited when the CLEAR input is high.
Recall mode:— In recall mode the counter and overflow latch are preset from the memory, all outputs are turned off and the multiplexing sequence is reset. The device is put into recall mode by taking RECALL to a high level while CLEAR is low and $\overline{SAVE}$ is high. Once the recall function has begun, any subsequent changes on the $\overline{SAVE}$ input are inhibited. The CLOCK input is always inhibited when the RECALL input is high.
Count mode:— In count mode the counter will increment on negative transitions of the clock input. If the counter is in the "999999" state, the next counting edge will set the overflow latch to a high level and counting will begin again at "000000". The device is in count mode when RECALL and CLEAR are at a low level and $\overline{SAVE}$ is high. However, once the CLOCK input has been taken high, any subsequent changes on the $\overline{SAVE}$ input are inhibited until the CLOCK returns to a low level.

Save mode:— In save mode the data in the counter and overflow latch is written into the non-volatile memory. The device is put into save mode by taking $\overline{SAVE}$ to a low level while all other inputs are at a low level. Once the save function has begun, any subsequent changes on the other inputs are inhibited until $\overline{SAVE}$ returns to a high level.

	Clock	Recall	Clear	$\overline{SAVE}$
Clear mode	*	*	1	1†
Recall mode	*	1	0	1†
Count mode	1	0	0	1†
Save mode	0†	0†	0†	0

TABLE 2. Control Truth Table

* Don't care condition.

† These conditions need only apply to enter the specified mode, once this has happened, changes on these inputs are inhibited internally until that particular mode is completed. Should the $\overline{SAVE}$ input be taken to a low level simultaneously with any other input going high, then a race condition will exist and although it is not possible to predict which mode will be entered, the device will not malfunction. The device may switch directly from one operating mode to another provided the minimum mode times are maintained. These features mean that no external synchronisation is required between the $\overline{SAVE}$ and other inputs and ensures that valid data is present before saving and that the data is fixed during the save period.

3. The high voltage for the memory is generated internally from a high impedance source and an external capacitor is needed on C_{EXT} to provide a charge reservoir. Exceeding the save duty cycle or excessive external leakage from C_{EXT} may cause appreciable loading of this high voltage resulting in reduced data retention. Should it be required to operate outside the specified limits then an external voltage supply may be used to maintain the high voltage level.

4. Exceeding the specified number of save cycles may cause a reduction in data retention time and eventually the device may suffer permanent damage.

5. Data can be entered into the memory with save times much less than ten milliseconds, however, the retention time is then significantly reduced. It is therefore important that spurious save pulses do not occur which could disturb or corrupt the stored data. This is most likely to occur at power on and power off. To eliminate this possibility it is sufficient to ensure that the $\overline{SAVE}$ input remains within one volt of V_{SS} at all times except during valid save periods.

6. Current limiting resistors should always be included on all outputs to prevent excessive output current.

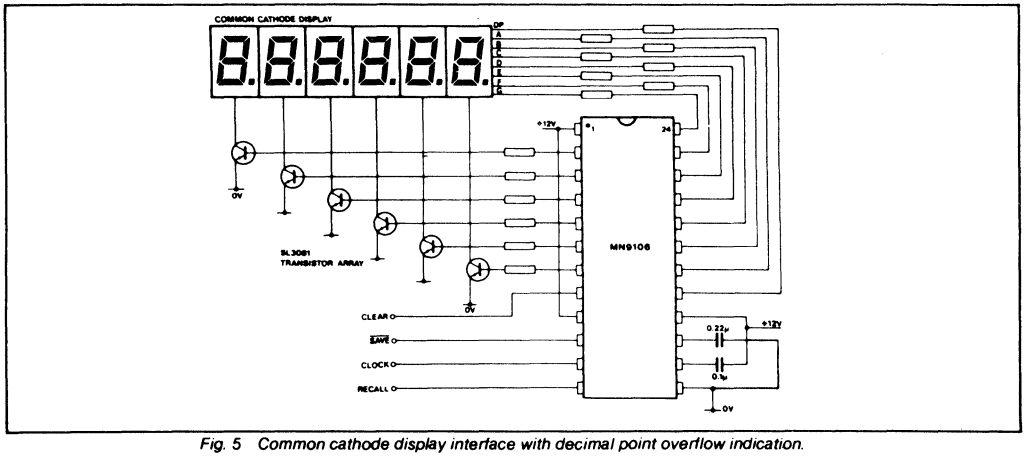


Fig. 5 Common cathode display interface with decimal point overflow indication.

PLESSEY
Semiconductors

2 MBIT PCM SIGNALLING CIRCUIT

MJ1440

HDB3 ENCODER/DECODER

The 2.048 MBit PCM Signalling Circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 MBit PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5 volt supply, relevant inputs and outputs are TTL compatible.

The MJ1440 is an encoder/decoder for the pseudo-ternary transmission code, HDB3 (CCITT Orange Book Vol III.2 Annex to Rec. G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding, all ones detection and loss of input (all zeroes detection). In addition a loop back function is provided for terminal testing.

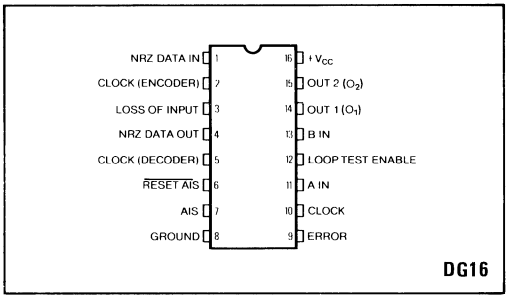


Fig. 1 Pin connections

FEATURES

- 5v ± 5% Supply — 40mA Max
- HDB3 Encoding and Decoding to CCITT rec. G703.
- Asynchronous Operation.
- Simultaneous Encoding and Decoding.
- Clock Recovery Signal Generated from Incoming HDB3 Data.
- Loop Back Control.
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm (All Zeros Detector).
- Decode Data in NRZ Form.

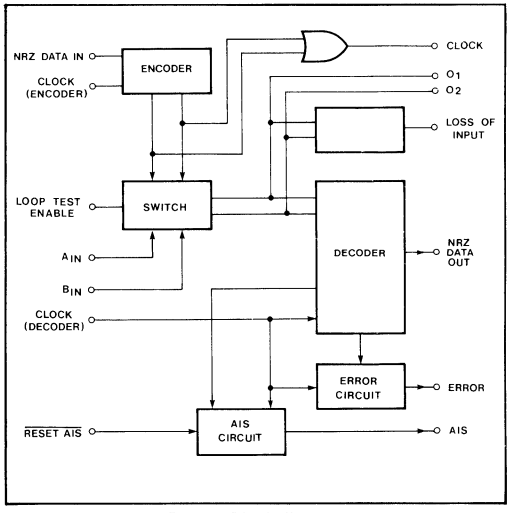


Fig. 2 Block diagram

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd — 0.3V
Outputs	Vcc, Gnd —0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
35°C/Watt	120°C/Watt

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient temperature, $T_{amb} = +22°C \pm 2°C$

Static characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min	Typ	Max		
Low level input voltage	V_{IL}	1,2,5,6 10,11,12,13	-0.3		0.8	V	
Low level input current	I_{IL}			1	50	µA	
High level input voltage	V_I		2.5		V_{cc}	V	
High level input current	I_{IH}			1	50	µA	
Low level output voltage	V_{OL}	10,14,15			0.5	V	Isink = 0.08µA
		3,4,7,9			0.4	V	Isink = 1.6mA
High level output voltage	V_{OH}	3,4,7,9	2.7			V	Isource = 60µA
		14,15	2.8			V	Isource = 2mA
		10	2.8			V	Isource = 1mA
Supply current	I_{cc}			20	40	mA	All inputs to 0V All outputs open circuit

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Max. Clock (Encoder) frequency	$fmax_{enc}$	4.0	10		MHz	Figs 10,15
Max. Clock (Decoder) frequency	$fmax_{dec}$	2.2	5		MHz	Figs 11,15
Propagation delay Clock (Encoder) to O_1, O_2	tpd1			100	ns	Figs 10, 15. See Note 1
Propagation delay Clock (Encoder) to Clock	tpd3			150	ns	Loop test enable = 1, Figs 13,15
Setup time of NRZ data in to Clock (Encoder)	ts3	75			ns	Figs 10,15
Hold time of NRZ data in	th3	55			ns	Figs 10,15
Propagation delay A_{in}, B_{in} to Clock	tpd2			150	ns	Loop test enable = '0' Figs 13,15
Propagation delay Clock (Decoder) to error	tpd4			200	ns	Figs 12,15
Propagation delay $\overline{\text{Reset AIS}}$ to AIS, loss of input	tpd5			200	ns	Loop test enable = '0' Figs 14,15
Propagation delay Clock (Decoder) to NRZ data out	tpd6			150	ns	Figs 11,15. See Note 2
Setup time of A_{in}, B_{in} to Clock (Decoder)	ts1	75			ns	Figs 11,15
Hold time of A_{in}, B_{in} to Clock (Decoder)	th1	55			ns	Figs 11,15
Hold time of $\overline{\text{Reset AIS}}$ = '0'	th2	100			ns	Figs 14,15
Setup time Clock (Decoder) to $\overline{\text{Reset AIS}}$	ts2	-75			ns	Figs 14,15

NOTES
1. Encoded HDB3 outputs (O_1, O_2) are delayed by 4 clock periods from NRZ data in (Fig.3)
2. The decoded NRZ output is delayed by 3 clock periods from the HDB3 inputs (A_{IN}, B_{IN}) (Fig.4)

FUNCTIONAL DESCRIPTION

Functions Listed by pin number

1. NRZ Data in
Input data for encoding into ternary HDB3 form. The NRZ data is clocked by the negative edge of the Clock (Encoder).

2. Clock (Encoder)
Clock for encoding data on pin 1

3. Loss of input alarm
This output goes to logic '1' if eleven consecutive zeroes are detected in the incoming HDB3 data. The output is set to logic '0' on receipt of a '1'

4. NRZ data out
Decoded data in NRZ form from ternary HDB3 input data (A_{in},B_{in}), data is clocked out by positive going edge of clock (Decoder).

5. Clock (Decoder)
Clock for decoding ternary data A_{in}, B_{in}.

6. $\overline{\text{Reset AIS}}$
Logic '0' resets decoded zero counter and sets AIS output to '0' provided 3 or more zeroes have been decoded in the preceding $\overline{\text{Reset AIS}}$ = '1' period. Logic '1' enables the decoded zero counter and sets the AIS output to '1' if less than 3 zeroes have been decoded in the preceding $\overline{\text{Reset AIS}}$ = '1' period.

7. AIS
A logic '1' on this output indicates that internal circuitry has counted less than 3 zeroes in the preceding $\overline{\text{Reset AIS}}$ = '1' period. In practice $\overline{\text{Reset AIS}}$ is derived from TSO every alternate frame by the MJ1444* or MJ1445* and the AIS output goes high if the synchronising word is not present (X0011011). AIS is set to logic '0' by pin 6 if 3 or more zeros were decoded in the preceding $\overline{\text{Reset AIS}}$ = '1' period. AIS changes on a negative going edge of $\overline{\text{Reset AIS}}$.

8. Ground
Zero volts

9. Error
A logic '1' indicates that a violation of the HDB3 coding has been received i.e. 3 '1's of the same polarity.

10. Clock
'OR' function of A_{in}, B_{in} for clock regeneration when pin 12 = '0', 'OR' function of O_1, O_2 when pin 12 = '1'.

11,13. A_{in},B_{in}
TTL inputs representing the received ternary HDB3 PCM signal. A_{in} = '1' represents a positive going '1', B_{in} = '1' represents a negative going '1'. A_{in} and B_{in} are sampled by the positive going edge of the Clock (Decoder). A_{in} and B_{in} may be interchanged.

12. Loop test enable
A TTL input to select normal or loop back operation. Pin 12 = '0' selects normal operation, encode and decode are independent and asynchronous. When pin 12 = '1' O_1 is connected internally to A_{in}, O_2 is connected internally to B_{in}. Clock becomes the OR function $O_1 + O_2$. **N.B.** A decode clock has to be supplied. The delay from NRZ in to NRZ out is 7½ clock periods in the loop back condition.

14, 15. O_1, O_2
Outputs representing the ternary encoded data for line transmission O_1 = '1' representing a positive going '1', O_2 = '1' represents a negative going '1'. O_1 and O_2 may be interchanged.

16. V_{cc}
Positive supply, 5V ± 5%

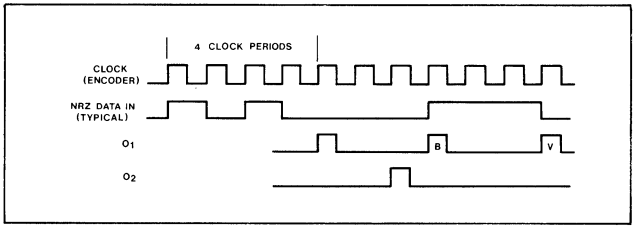


Fig. 3 Encode waveforms

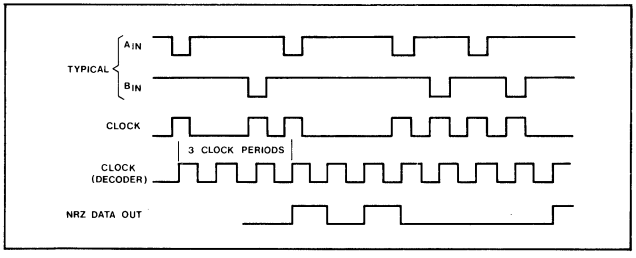


Fig. 4 Decode waveforms

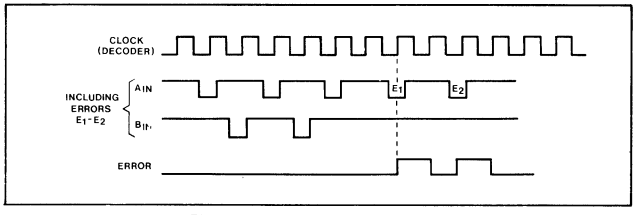


Fig. 5 HDB3 error output waveforms

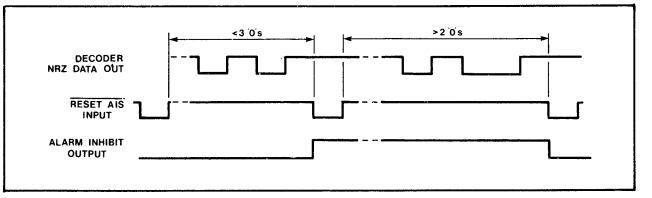


Fig. 6 AIS error and reset waveforms

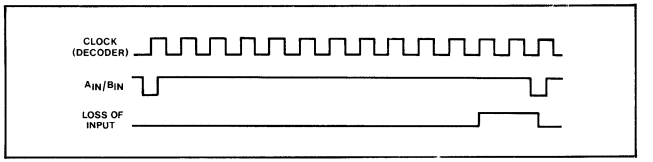


Fig. 7 Loss of input waveforms

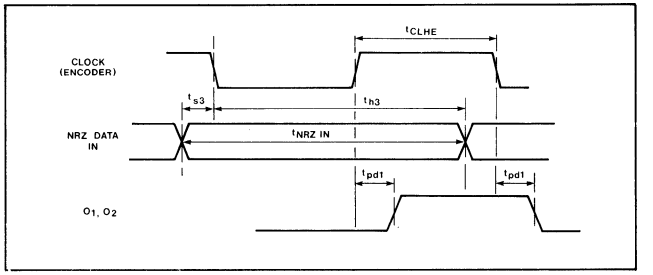


Fig. 8 Encoder timing relationship

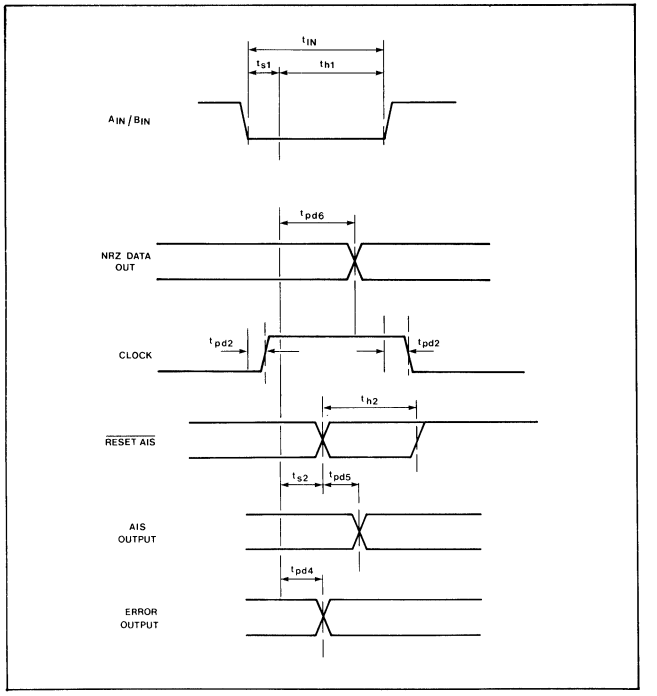


Fig. 9 Decoder timing relationship

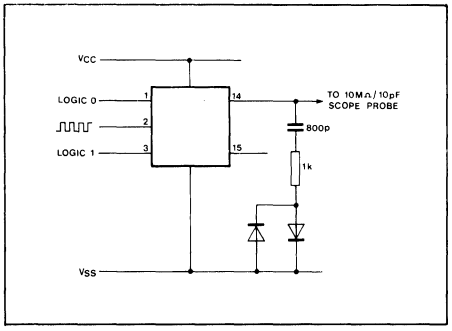


Fig. 10

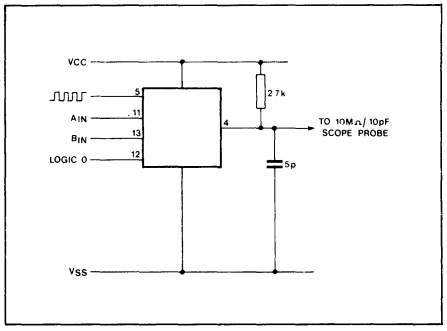


Fig. 11

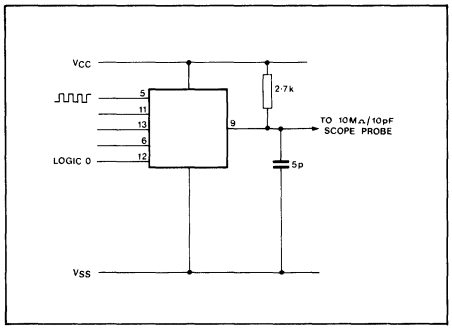


Fig. 12

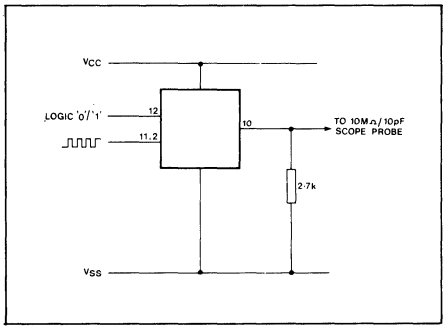


Fig. 13

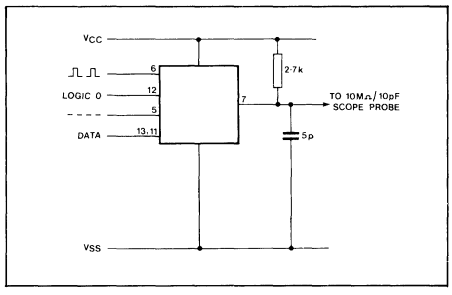


Fig. 14

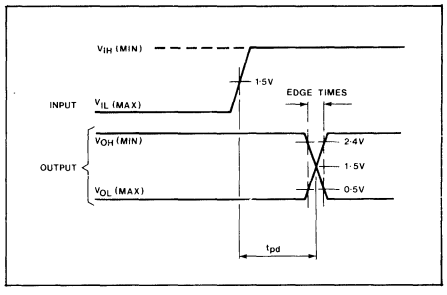


Fig. 15 *Test timing definitions*

DEFINITION OF THE HDB3 CODE

Coding of a binary signal into an HDB3 signal is done according to the following rules:

1. The HDB3 signal is psuedo-ternary; the three states are denoted B_+, B_- and O.

2. Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces however, special rules apply (see 4. below).

3. Marks in the binary signal are coded alternately as B_+ and B_- in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (see 4. below).

4. Strings of four spaces in the binary signal are coded according to the following rules:

a The first space of a string is coded as a space if the preceding mark of the HDB3 signal has a polarity opposite to the polarity of the preceding violation and is not a violation by itself; it is coded as a mark, i.e. not a violation (i.e. B_+, B_-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.
This rule ensures that successive violations are of alternative polarity so that no DC component is introduced.

b The second and third spaces of a string are always coded as spaces.

c The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V_+ or V_- according to their polarity.

PLESSEY
Semiconductors

2 MBIT PCM SIGNALLING CIRCUIT

MJ 1444

PCM SYNCHRONISING WORD GENERATOR

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5 volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1444 generates the synchronising word in accordance with CCITT recommendations G732. The MJ1445 has been designed to detect this synchronising word when received at the remote end of the transmission system.

The synchronising word is injected onto the PCM data highway during time slot 0 in alternate frames. The spare time slot 0 data bits, bit 1 in every frame and bits 3 to 8 inclusive in alternate frames (i.e. those not containing the synchronising word) are available as parallel inputs and are output onto the PCM data highway.

The data output of the MJ1444 is 'open collector' and can be wire-OR'd directly onto the highway.

The device also provides a time slot 0 channel pulse 'TS0', time slot 0 non-sync. frame 'TS0 $\overline{SF}$', and time slot 16 'TS16' outputs.

FEATURES

- 5V ± 5% Supply — 20 mA Typical
- Fully Conforms to CCITT Recommendation G732
- Outputs Directly Onto PCM Data Highway
- Provides Both Time Slot 0 and Time Slot 16 Channel Pulses
- All Inputs and Outputs are TTL Compatible

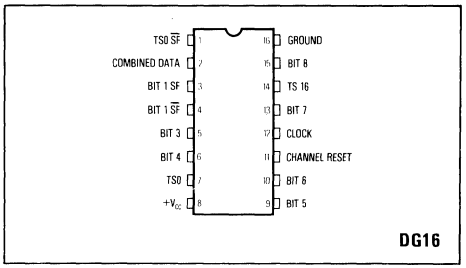


Fig.1 Pin connections

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
35°C/Watt	120°C/Watt

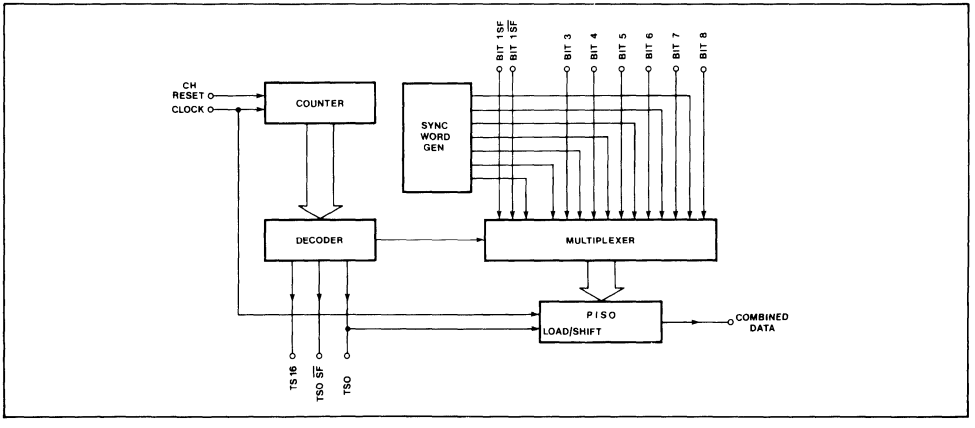


Fig.2 MJ1444 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient temp., $T_{amb} = 22°C \pm 2°C$

Static Characteristics
Ambient operating temperature −10°C to +70°C

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	1, 2, 3, 4, 5, 7, 11, 12, 13, 14.	−0.3		0.8	V	
Low level input current High level input current	I_{IN}	11		1	50	μA	
High level input voltage	V_{IH}	11	2.4		V_{CC}		
Low level output voltage	V_{OL}	6, 9, 15			0.5	V	$I_{sink} = 2mA$
		10			0.7	V	$I_{sink} = 5mA$
High level output voltage	V_{OH}	6, 9, 15	2.8			V	$I_{source} = 200\mu A$
High level output leakage current	I_{OH}	10			20	μA	$V_{OUT} = V_{CC}$
Supply current	I_{CC}			20	40	mA	$V_{CC} = 5.25V$

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max clock frequency	F_{max}	3	5		MHz	
Propagation delay, clock to TS0, TS0 $\overline{SF}$, TS16 and combined data outputs.	t_P	80		200	ns	See Figs.5 and 6
Set up time channel reset to clock	T_{S1}	100		450	ns	$f_{clock} = 2.048MHz$
Hold time of channel reset input	t_{H1}	20		400	ns	
Set up time of bit 1 (SF) to datum B	t_{S2}	100			ns	
Hold time of bit 1 (SF) wrt datum B	t_{H2}	300			ns	
Set up time of bit 1 ($\overline{SF}$) and data bits 3—8 to datum B	t_{S2}	100			ns	
Hold time of bit 1 ($\overline{SF}$) and data bits 3—8 wrt datum B	t_{H2}	300			ns	

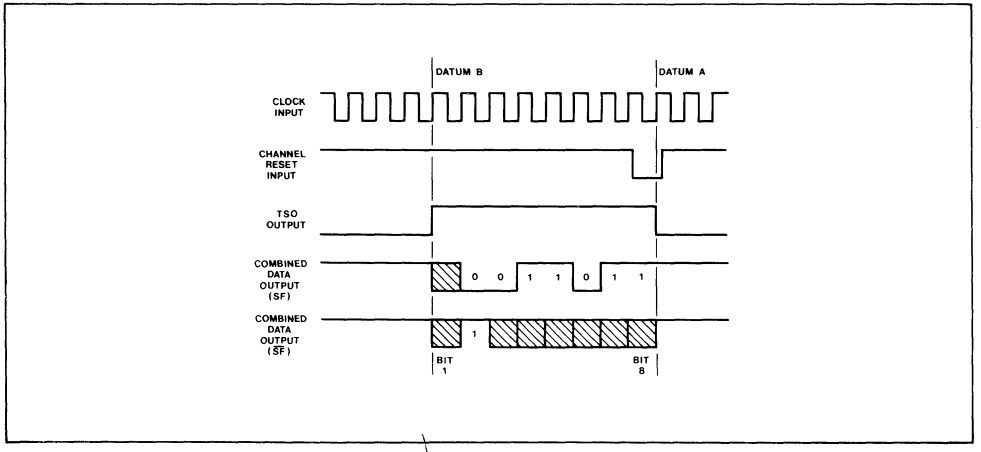


Fig.3 Data timing

FUNCTIONAL DESCRIPTION

Functions Listed by pin number

1, 2, 5, 7, 13, 14. Bits 3 to 8

Parallel data on these inputs is asynchronously loaded into bits 3 to 8 of the PISO shift register for transmission during Time slot 0 of non-sync. frames.

3. Channel Reset

A low going pulse at this input synchronises the MJ1444 with the other devices at the transmit end of the PCM link. It may be applied as a start pulse or repeated at the same instant in successive frames.

4. Clock

System clock input (2.048MHz for a 2 Mbit PCM system).

6. TS16

This output provides a positive pulse equivalent to 8 clock periods during time slot 16 of every 30 + 2 channel PCM frame.

8. GND

Zero volts.

9. TS0 $\overline{SF}$

This output provides a positive pulse equivalent to 8 clock periods during time slot 0 of non-sync. frames.

10. Combined data

This 'open collector' output injects the contents of the PISO shift register onto the PCM data highway during time slot 0 in successive frames. The contents of the PISO shift register are defined as follows:

	Bit 1	2	3	4	5	6	7	8
Sync. Frame	X	0	0	1	1	0	1	1
Non-sync. frame	X	1	X	X	X	X	X	X

X — indicates that these bits may be set according to the parallel data inputs.

11. Bit 1 SF

Data on this input is asynchronously loaded into bit 1 of the PISO shift register for transmission during time slot 0 of sync. frames.

12. Bit 1 $\overline{SF}$

Data on this input is asynchronously loaded into bit 1 of the PISO shift register for transmission during time slot 0 of non-sync. frames.

15. TS0

This output provides a positive pulse equivalent to 8 clock period during time slot 0 of every 30 channel PCM frame.

16. V_{CC}

Positive supply, 5V ±5%.

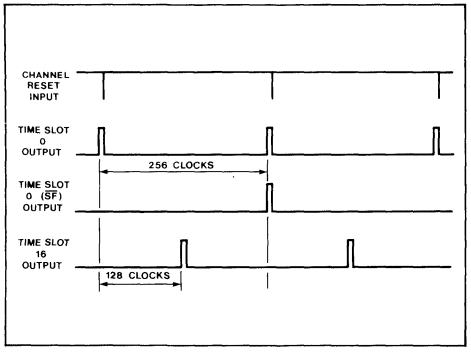


Fig.4 Sync. timing

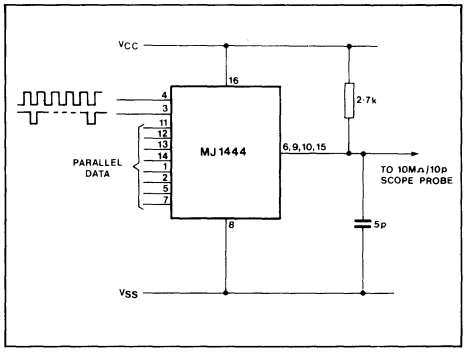


Fig.5 Test conditions (all outputs)

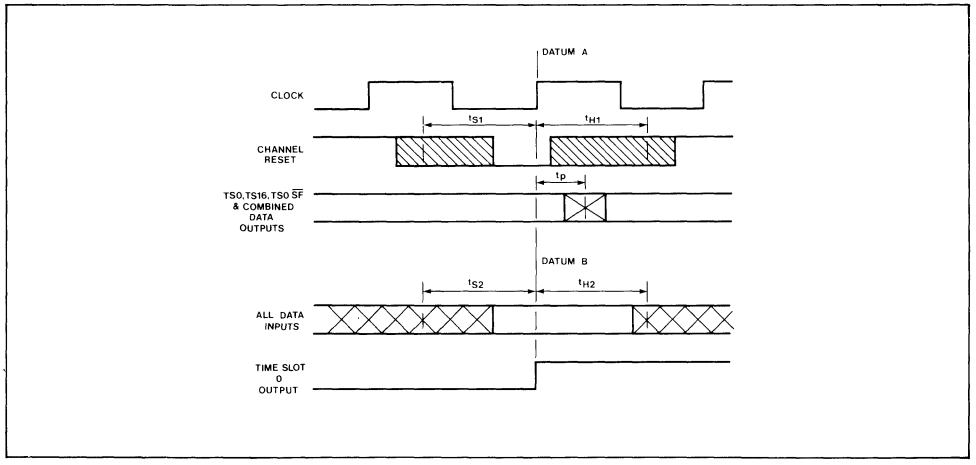


Fig.6 Timing definitions

PLESSEY
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PCM SYNCHRONISING WORD RECEIVER

MJ1445

2 MBIT PCM SIGNALLING CIRCUIT

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 MBit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1445 establishes synchronisation by detecting the synchronising word when it is received at the remote end of the transmission system. The MJ1444 has been designed to generate this synchronisation word at the sending end of the system in accordance with CCITT recommendation G732.

Corruption of individual synthronisation words is signified by an 'Error' output, loss of synchronisation is indicated by a 'Sync Alarm' output and follows CCITT G732 in that loss of synchronism is assumed when 3 consecutive synchronisation words have been received with errors.

The 'Channel Reset' output goes low for the first period of the clock after time slot 0 in sync frames whenever the MJ1445 has established that the receiver terminal is in synchronisation in order that the rest of the receiver terminal may be reset.

The 'TSO' output is high for a period of 8 bits starting from the end of the first bit of the synchronising word. The spare data bits from the synchronising word are provided as parallel outputs.

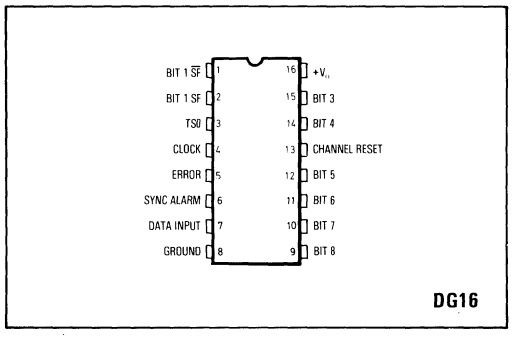


Fig.1 Pin connections

FEATURES

- 5V ±5% Supply – 20mA Typical.
- Conforms to CCITT Recommendation G732
- Synchronising Word Error Monitor
- Out of Sync. Alarm
- All Inputs and Outputs are TTL Compatible

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd – 0.3V
Outputs	Vcc, Gnd –0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
35°C/Watt	120°C/Watt

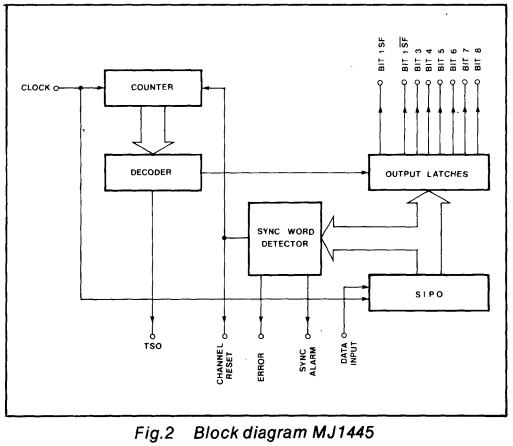


Fig.2 Block diagram MJ1445

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5\,V \pm 0.25\,V$
Ambient temperature, $T_{amb} = +22°C \pm 2°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	4, 7	−0.3		0.8	V	
Low level input current High level input current	I_{IN}	4, 7		1	50	μA	
High level input voltage	V_{IH}	4, 7	2.4		V_{CC}	V	
Low level output voltage	V_{OL}	1, 2, 3, 5, 6 9, 10, 11, 12 13, 14, 15			0.5	V	$I_{sink} = 2\,mA$
High level output voltage	V_{OH}		2.8				$I_{source} = 200\,\mu A$
Supply current	I_{CC}			20	40	mA	$V_{CC} = 5.25\,V$

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Clock frequency	f_{max}	2.2	4.5		MHz	
Input delay of data input	$t_{d\,data}$	20		200	ns	$f_{clock} = 2.048\,MHz$
Propagation delay, clock to TS0 output	$t_{d\,TS0}$	80		200	ns	Fig. 3
Propagation delay clock to error output, sync alarm, spare bits and CH. Reset output high	t_d	50		400	ns	Fig. 3
Propagation delay, clock to CH. Reset output Low $(T - t_p)$	t_p	100		450	ns	Fig. 3

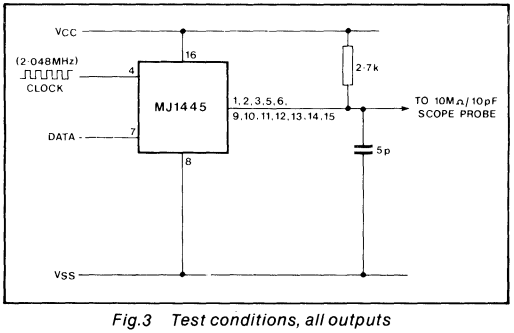


Fig.3 Test conditions, all outputs

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. Bit 1 $\overline{SF}$
This output is set to the level of data bit 1 during time slot 0 of non sync frames. The data becomes true at the end of the first bit of time slot 1.

2. Bit 1 SF
This output is set to the level of data bit 1 during time slot 0 of sync frames. The data becomes true at the end of the first bit of time slot 1.

3. TS0
This output provides a positive pulse of 8 clock periods in every frame starting from the end of the first bit of the synchronising word of the received data.

4. Clock
System clock input (2.048MHz for a 2MBit PCM system).

5. Error
This output goes high at the end of time slot 0 in the 3rd sync frame following the frame with sync word errors. If consecutive sync words occur with errors this output will remain high. If a sync alarm is generated this output will remain high until sync is regained.

6. Sync Alarm
This output goes high at the end of time slot 0 output in the 3rd consecutive sync frame containing sync word errors. It returns low at the end of TS0 output in the 3rd consecutive frame received correctly (sync and non sync).

7. Data input
Serial data (2MBit/s) at this input is clocked through the SIPO shift register and examined by the sync word detector.

8. GND
Zero volts

9, 10, 11, 12, 14, 15. Bits 3 to 8
These paraliel outputs are set to the level of the spare data bits (3 to 8) of time slot 0 of non sync frames. The data becomes true at the end of the first bit of time slot 1.

13. Channel reset
This output goes low for the first period of the clock after time slot 0 of the received data as long as synchronisation has been established. This pulse can be used to reset the rest of the receiver terminal.

16. V_{CC}
Positive supply $5\,V \pm 5\%$.

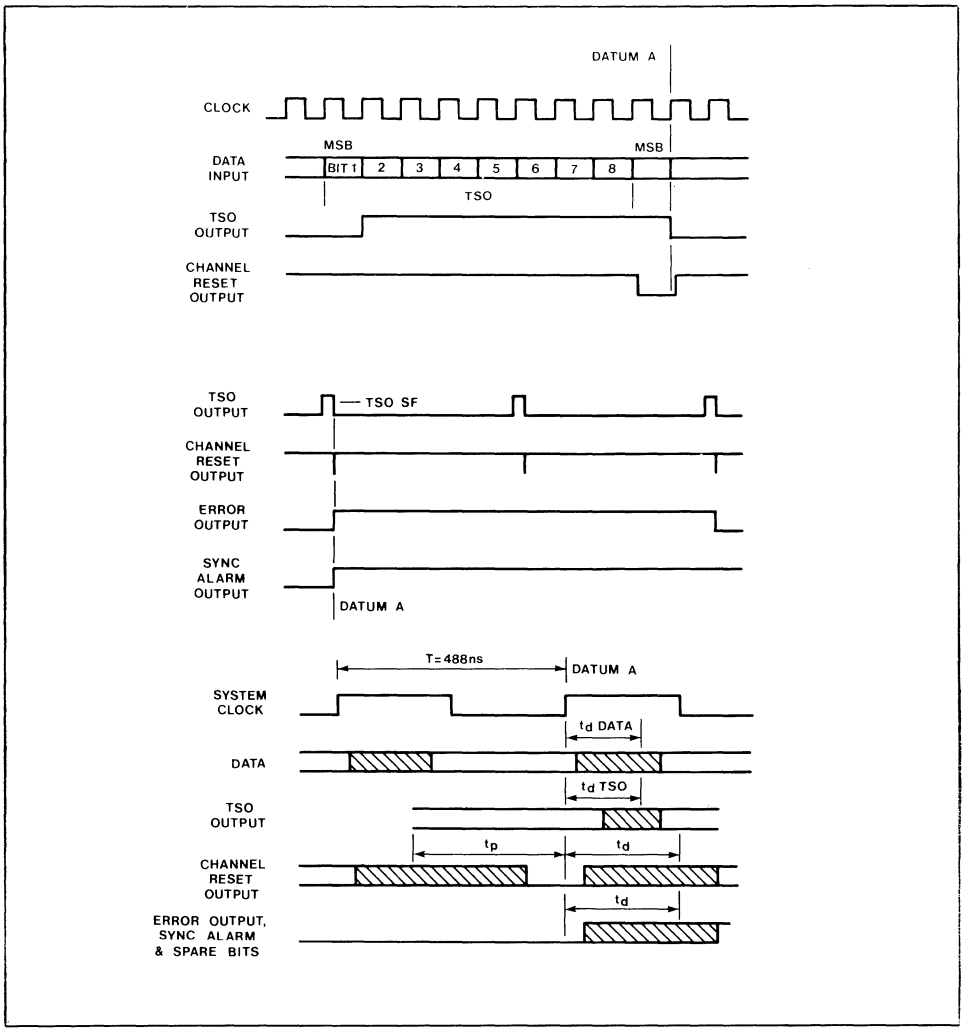


Fig.4 Timing diagram and output waveforms

PLESSEY
Semiconductors

2 MBIT PCM SIGNALLING CIRCUIT

MJ1446

TIME SLOT 16 RECEIVER AND TRANSMITTER

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1446 has two modes of operation dependant on the state of the mode control input. With the mode control high the device is in the transmit mode and with the mode control low the device is in the receive mode.

In the transmit mode the device accepts 64kbits/sec signalling information in either binary or AMI format and outputs it at 2Mbits/sec on to the digital highway during time slot 16.

In the receive mode the device accepts 2Mbit/sec information from the digital highway, during time slot 16 and output is at 64kbits/sec in both binary and AMI format.

In both receive and transmit mode there is an AMI coded clock output, AMI output and $\overline{\text{AMI}}$ output which conforms to CCITT recommendation no G372 for a 64kbits/sec contradirectional interface. The alarm inhibit input causes the 8kHz timing signal to be removed from the AMI clock output.

The device is reset in both modes by a time slot 16 channel pulse and the alarm output provides an indication that the internal counter is operating correctly.

Also provided are 64kHz, 16kHz and 8kHz clock outputs.

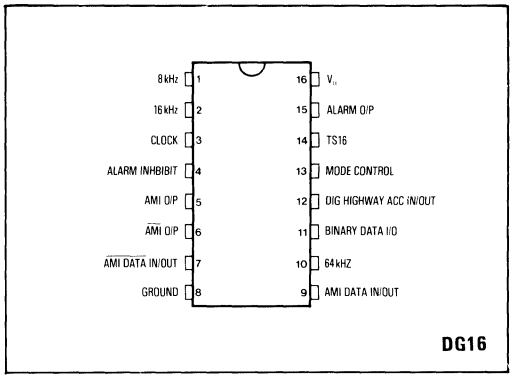


Fig.1 Pin connections

FEATURES

- 5V ±5% Supply—20mA Typical
- Conforms to CCITT Recommendations
- Provides Both AMI and Binary Format Data Outputs
- Single Chip Receive or Transmit
- All Inputs and Outputs are TTL Compatible.

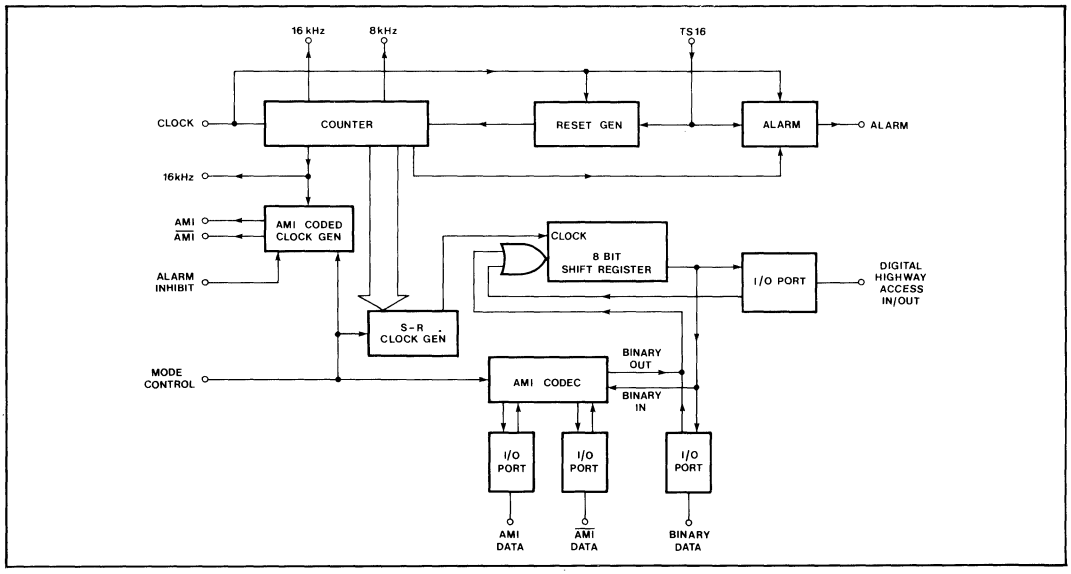


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage $V_{CC} = 5V \pm 0.25V$
Ambient temperature $T_{amb} = 22°C \pm 2°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	3, 4, 7, 9, 11, 12, 13, 14	-0.3		0.8	V	
Low level input current	I_{IN}	11		1	50	μA	
High level input current							
High level input voltage	V_{IH}	11	2.4		V_{CC}	V	
Low level output	V_{OL}	1, 2, 5, 6, 7, 9, 10, 11, 15			0.5	V	$I_{sink} = 2mA$
		12			0.5	V	$I_{sink} = 5mA$
High level output voltage	V_{OH}	1, 2, 10, 5, 6, 15	2.8			V	$I_{source} = 200\mu A$
High level output leakage current	I_{CH}	7, 9, 11, 12			20	μA	$V_{OUT} = V_{CC}$
Supply current	I_{CC}			20		mA	$V_{CC} = 5.25V$

Dynamic Characteristics (f_{clock} = 2.048 MHz)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Propogation delay clock to data out to digital highway	t_p	20		200	ns	Fig.7
Propogation delay clock to 64 kHz out	t_p	20		200	ns	Fig.7
Input delay, clock to digital highway access	$t_{d\,DATA}$	20		200	ns	
Input delay, clock to time slot 16	$t_{d\,TS16}$	80		200	ns	
Output delay 64 kHz to 16 kHz output	$t_{p\,16}$			70	ns	Fig.7
Output delay, 64 kHz to 8kHz output	$t_{p\,8}$			170	ns	Fig.7
Output delay, 64 kHz to binary data output (64 kHz)	$t_{p\,BIN}$	20		450	ns	Fig.8
Output delay 64 kHz to AMI, $\overline{AMI}$, AMI data & $\overline{AMI}$ data o/p's	$t_{p\,AMI}$	20		400	ns	Fig.8
Input delay, 64 kHz to binary data in (64 kHz)	$t_{d\,BIN}$			100	ns	

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. 8 kHz
8kHz square wave output.

2. 16 kHz
16 kHz square wave output.

3. Clock
System clock input (2.048 MHz for a 2 Mbit PCM system)

4. Alarm inhibit
A high level on this input inhibits the 8kHz timing signal on the AMI clock outputs.

5. AMI output
Alternative Mark Inversion coded 64 kHz.

6. $\overline{AMI}$ output

7. $\overline{AMI}$ Data in/out
In the transmit mode 64 kHz signalling data in AMI format is accepted at these inputs for output to PCM highway during time slot 16.

9. AMI Data in/out
In the receive mode data accepted from the PCM highway during time slot 16 appears on these outputs at 64 kbits/sec in AMI format.

8. GND
Zero volts.

10. 64 kHz
64 kHz square wave output.

11. Binary data in/out
In the transmit mode 64 k bit/sec signalling data in binary form is accepted at this input for output to the PCM data highway during time slot 16. In the receive mode data is accepted from the PCM highway during TS16 and appears at this output at 64 Kbits/sec in binary format.

12. Digital Highway access in/out
In the receive mode 2 Mbit/sec signalling data is accepted at this input during time slot 16 from the PCM digital highway. In the transmit mode signalling data is output to the PCM digital highway during time slot 16 at 2 Mbits/sec.

13. Mode control

A high level on this input causes the MJ1446 to operate in the transmit mode while a low level causes it to operate in the receive mode.

14. TS16

This input should be connected to time slot 16 channel pulse of the PCM system to synchronise the MJ1446 with the rest of the system.

15. Alarm output

A high level on this output indicates that the internal counter has stopped or is out of synchronisation with the time slot 16 channel pulse.

16 V_{CC}

Positive supply 5V ±5%.

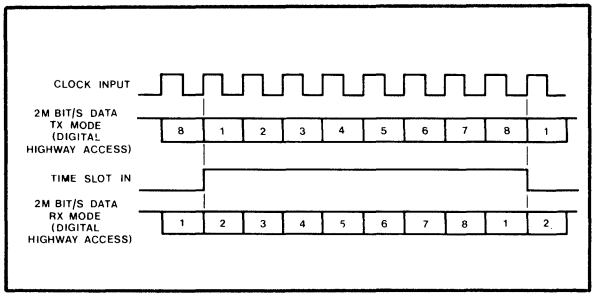


Fig.3 2MBit/s operation

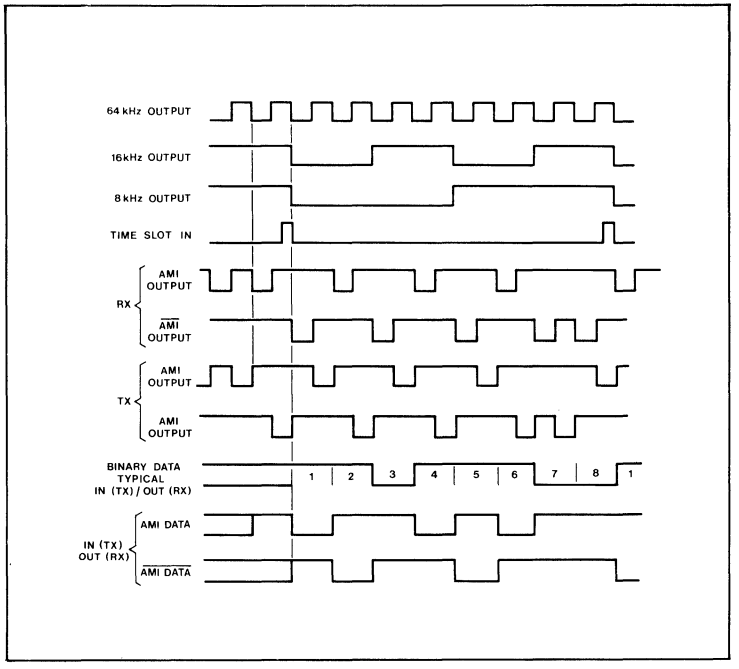


Fig.4 64kBit/s operation

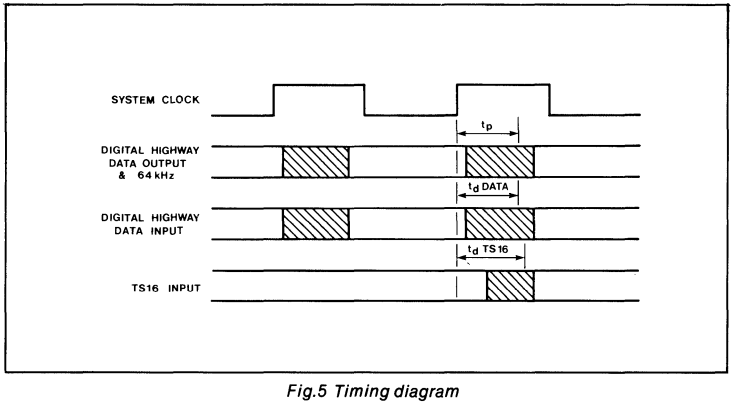


Fig.5 Timing diagram

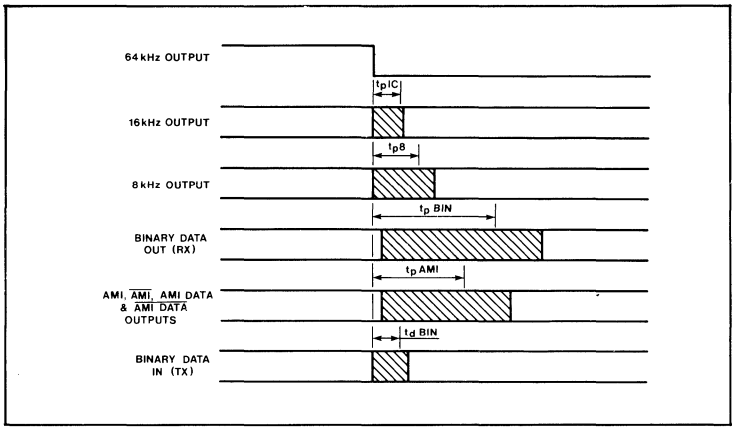


Fig.6 Timing diagram

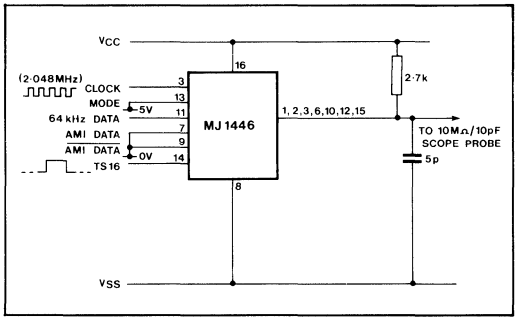


Fig.7 Test conditions

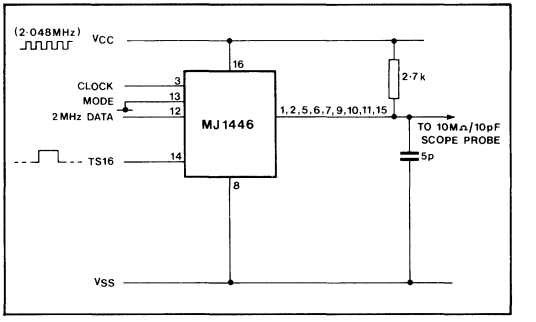


Fig.8 Test conditions

PLESSEY
Semiconductors

2 MBIT PCM SIGNALLING CIRCUIT

MJ1471

HDB3 OR AMI ENCODER/DECODER

The MJ1471 is an encoder/decoder for pseudo-ternary transmission codes. The codes are true Alternate Mark Inversion (AMI) or AMI modified according to HDB3 rules (CCITT Orange Book Vol 111-2, Annex to Rec.G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding and all ones detection (AIS). In addition a loop test function is provided for terminal testing.

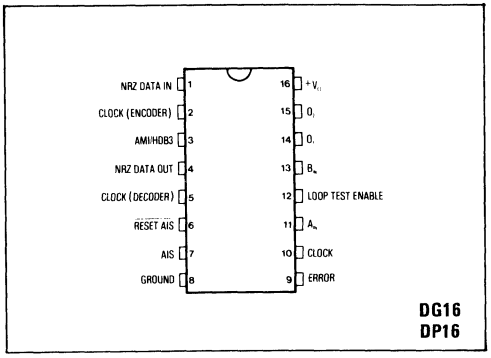


Fig.1 Pin connections (top view)

FUNCTIONS

- 5V ±5% Supply — 40mA Max.
- AMI or HDB3 Operation — TTL Selectable
- Loop Back Facility
- 'All Ones' Error Monitor to Detect Loss of Synchronising Word (Time Slot Zero)
- Error Monitor of HDB3 Incoming Code
- Decoded Data in NRZ Form

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. NRZ data in
Input data for encoding into ternary form (TTL) the data is clocked by the negative going edge of the Clock (Encoder).

2. Clock (Encoder)
Clock for encoding data on pin 1.

3. AMI/HDB3
MJ1471 operates in HDB3 if pin 3 is at logic '1'. AMI if pin 3 is at logic '0'.

4. NRZ Data out
Decoded data from ternary inputs A_{in}, B_{in}.

5. Clock (Decoder)
Clock for decoding ternary data A_{in}, B_{in}.

6. $\overline{\text{Reset AIS}}$
Logic '0' resets decoded zero counter and sets AIS output to '0' provided that more than 3 zeroes have been decoded in the preceeding period between $\overline{\text{Reset AIS}}$ signals. Logic '1' enables decoded zero counter.

7. $\overline{\text{AIS}}$
A logic '1' on this output indicates that internal circuitry has counted less than three zeroes in each of two successive periods between reset AIS pulses. In practice the $\overline{\text{Reset AIS}}$ is derived from TS0 by the MJ1445 and the AIS output goes high if the synchronising word (X0011011) is not present. AIS is set to logic '0' by pin 6 if more than 2 '0's were decoded during the preceeding reset AIS = '1' period. AIS changes on the negative edge of $\overline{\text{Reset AIS}}$.

8. Ground
Zero volts.

9. Error
A logic '1' indicates that a violation of the HDB3 encoding law has been decoded i.e. 3 '1's of the same polarity.

10. Clock
OR function of A_{in}, B_{in} for clock regeneration when pin 12 = '0', OR function of O_1 O_2 when pin 12 = '1'.

11, 13. A_{in}, B_{in}
TTL inputs representing the received ternary PCM signal. A_{in} = '1' represents a positive going '1', B_{in} = '1' represents a negative going '1'. A_{in} and B_{in} are sampled by the positive going edge of the clock decoder. A_{in} and B_{in} may be interchanged.

12. Loop test enable
TTL input to select normal or loop back operation. Pin 12 = '0' selects normal operation, encode and decode are independent and asynchronous.

When pin 12 = '1' O_1 is connected internally to A_{in} and O_2 to B_{in}. Clock becomes the OR function of O_1 O_2. **N.B.** a decode clock has to be supplied. The delay from NRZ in to NRZ out is 7½ clock periods in loop back.

14, 15, O_1, O_2
Outputs representing the ternary encoded PCM AMI/HDB3 signal for line transmission. O_1 and O_2 are in Return to zero form and are clocked out on the positive going edge of the encode clock. The length of O_1 and O_2 pulses is set by the positive clock pulse length.

16. $+V_{CC}$
Positive 5V ±5% supply.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage $V_{CC} = 5V \pm 0.25V$
Ambient temperature $T_{amb} = 22°C \pm 2°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min	Typ	Max		
Low level input voltage	V_{IL}	1,2,3,5,6 10,11,12,13	-0.3		.8	volts	
Low level input current	I_{INL}			1	50	µA	
High level input voltage	V_{IN}		2.5		V_{cc}	V	
High level input current	I_{INH}			1	50	µA	
Low level output voltage	V_{OL}	10,14,15			.5	V	Isink = 0.08µA
		4,7,9			.4	V	Isink = 1.6mA
High level output voltage	V_{OH}	4,7,9	2.7			V	Isource = 60µA
		14,15	2.8			V	Isource = 2mA
		10	2.8			V	Isource = 1mA
Supply current	I_{cc}			20	40	mA	All inputs to 0v All outputs open circuit

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Max. Clock (Encoder) frequency	$fmax_{enc}$	4.0	10		MHz	Figs 9 and 14
Max. Clock (Decoder) frequency	$fmax_{dec}$	2.2	5		MHz	Figs 10 and 14
Propagation delay Clock (Encoder) to O_1, O_2	tpd1			100	ns	Figs 9 and 14 See note 1.
Propagation delay Clock (Encoder) to Clock	tpd3			150	ns	Loop test enable=1, Figs 9 and 14
Setup time of NRZ data in to Clock (Encoder)	ts3	75			ns	Figs 9 and 14
Hold time of NRZ data in	th3	55			ns	Figs 9 and 14
Propagation delay A_{in}, B_{in} to Clock	tpd2			150	ns	Loop test enable='0' Figs 12, 14
Propagation delay Clock (Decoder) to error	tpd4			200	ns	Figs 11 and 14
Propagation delay $\overline{\text{Reset AIS}}$ to AIS, loss of input	tpd5			200	ns	Loop test enable = '0' Figs 13,14
Propagation delay Clock (Decoder) to NRZ data out	tpd6			150	ns	Figs 10 and 14 See note 2
Setup time of A_{in}, B_{in} to Clock (Decoder)	ts1	75			ns	Figs 10 and 14
Hold time of A_{in}, B_{in} to Clock (Decoder)	tH1	55			ns	Figs 10 and 14
Hold time of $\overline{\text{Reset AIS}}$ = '0'	tH2	100			ns	Figs 13 and 14
Setup time Clock (Decoder) to $\overline{\text{Reset AIS}}$	ts2	-75			ns	Figs 13 and 14

NOTES
1. The Encoded ternary outputs (O_1, O_2) are delayed by 4 clock periods from NRZ data in (Fig.3)
2. The decoded NRZ output is delayed by 3 clock periods from the HDB3 inputs (A_{IN}, B_{IN}) (Fig.4)

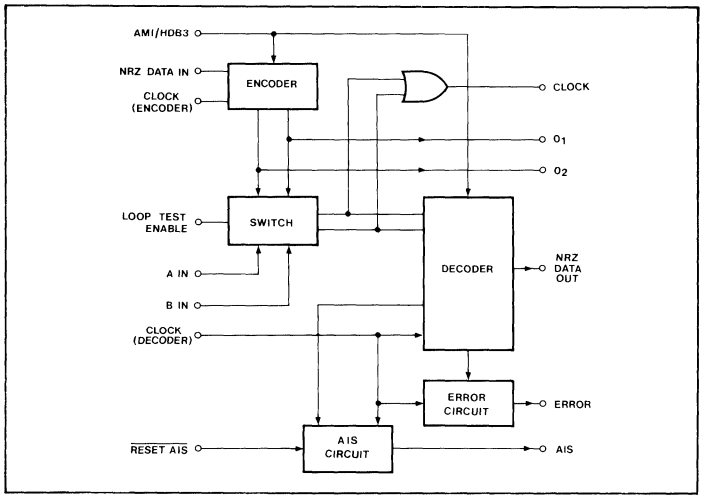


Fig. 2 MJ1471 Block diagram

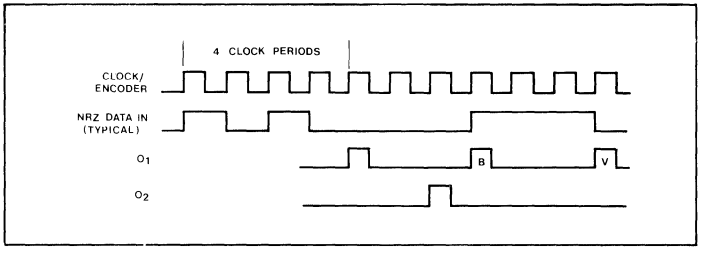


Fig. 3 Encode waveforms

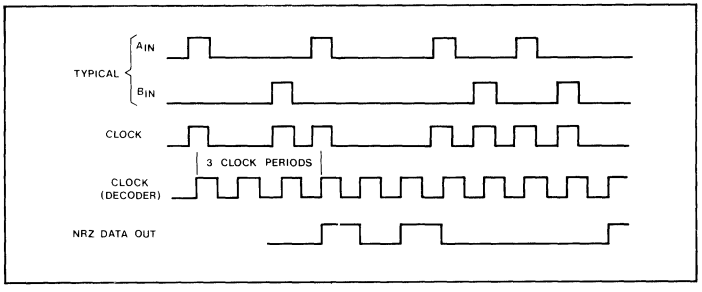


Fig. 4 Decode waveforms

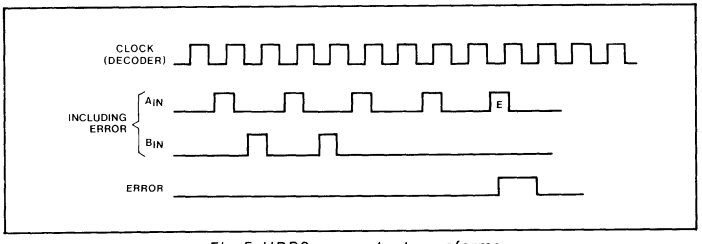
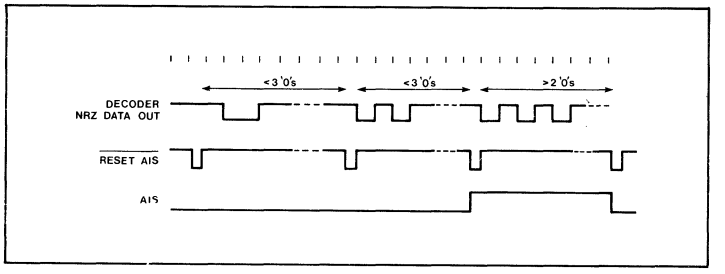


Fig. 5 HDB3 error output waveforms



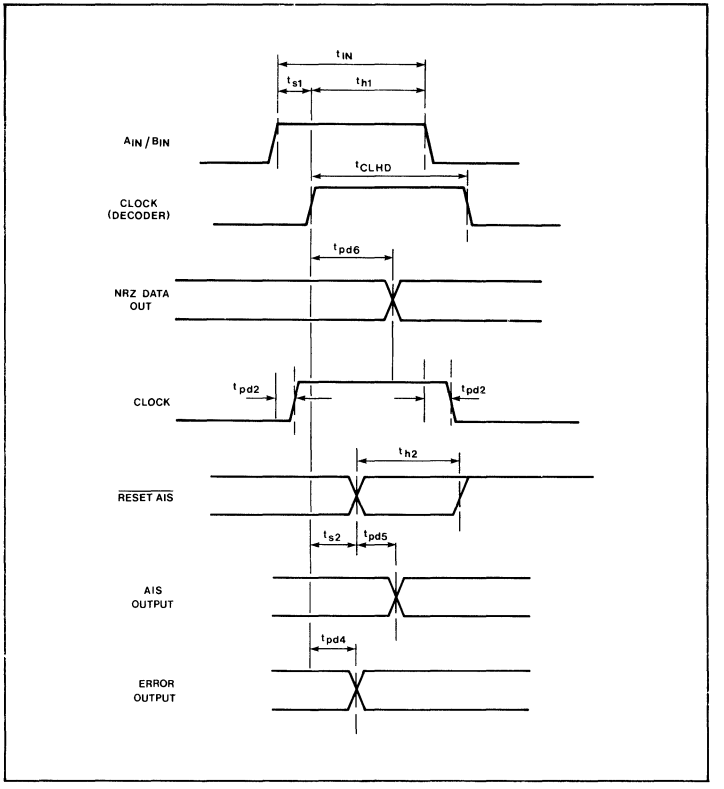


Fig. 7 Decoder timing relationship

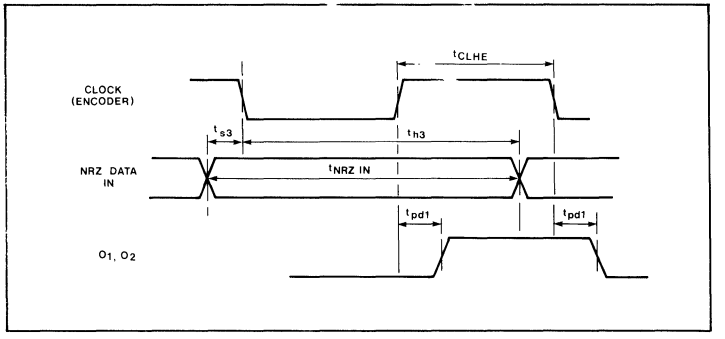


Fig. 8 Encoder timing relationship

DEFINITION OF THE HDB3 CODE

Coding of a binary signal into an HDB3 signal is done according to the following rules:

1. The HDB3 signal is psuedo-ternary; the three states are denoted B_+, B_- and O.

2. Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces however, special rules apply (see 4. below).

3. Marks in the binary signal are coded alternately as B_+ and B_- in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (see 4. below).

4. Strings of four spaces in the binary signal are coded according to the following rules:

a The first space of a string is coded as a space if the preceding mark of the HDB3 signal has a polarity opposite to the polarity of the preceding violation and is not a violation by itself; it is coded as a mark, i.e. not a violation (i.e. B_+, B_-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.

This rule ensures that successive violations are of alternative polarity so that no DC component is introduced.

b The second and third spaces of a string are always coded as spaces.

c The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V_+ or V_- according to their polarity.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
35°C/Watt	120°C/Watt

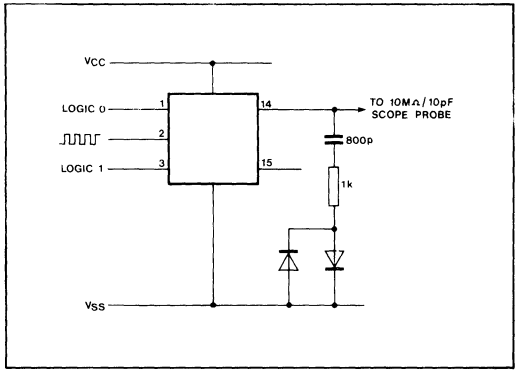


Fig. 9

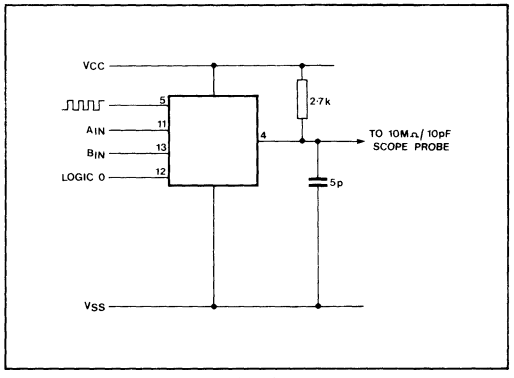


Fig. 10

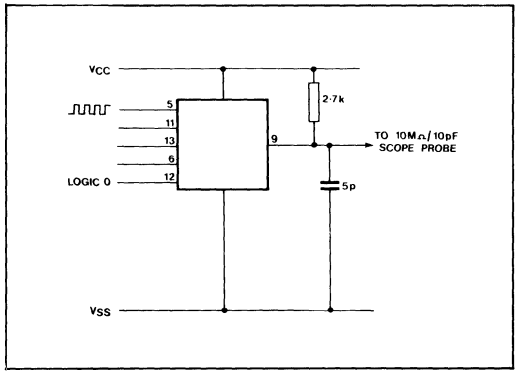


Fig. 11

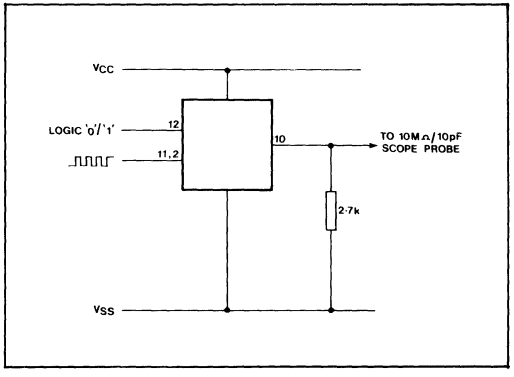


Fig. 12

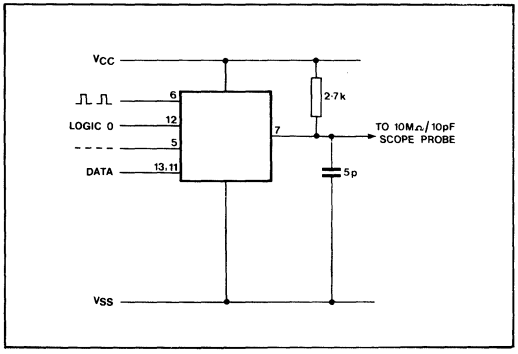


Fig. 13

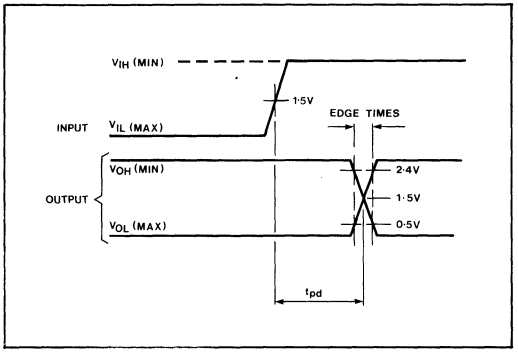


Fig. 14 Test timing definitions

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MJ2812, MJ2812M 32 WORDS x 8 BIT FIFO MEMORY
MJ2813, MJ2813M 32 WORDS x 9 BIT FIFO MEMORY

The MJ2812 and MJ2813 are 32-word by 8-bit and 9-bit first-in first-out memories, respectively. Both devices have completely independent read and write controls and have three state outputs controlled by an output enable pin (OE). Data on the data inputs (D_O — D_7) is written into the memory by a pulse on load (PL). The data word automatically ripples through the memory until it reaches the output or another data word.

Data is read from the memory by applying a shift out pulse on PD. This dumps the word on the outputs (Q_O — Q_7) and the next word in the buffer moves to the output. An output ready signal (OR) indicates that data is available at the output and also provides a memory empty signal. An input ready signal (IR) indicates that the device is ready to accept data and also provides a memory full signal.

Both the MJ2812 and MJ2813 have master reset inputs which initialise the FIFO control logic and clear all data from the device (reset to all lows). A FLAG signal goes high when the memory is approximately half full.

The MJ2812 can perform input and output data transfer on a bit-serial basis as well as on 8-bit parallel words. The input buffer is an 8-bit shift register which can be loaded in parallel by the PL command or can be loaded serially through the D_O input by using the SL clock. When 8 bits have been shifted into the input buffer serially, the 8-bit word automatically moves in parallel through the memory. The output includes a built in parallel-to-serial converter, so that data can be shifted out of the Q7 output by using the SD clock. After 8 clock pulses a new 8-bit word appears at the outputs.

The timing and function of the four control signals PL, IR, PD and OR are designed so that two FIFOs can be placed end-to-end, with OR of the first driving PL of the second and IR of the second driving PD of the first. With this simple interconnection, strings of FIFOs can control each other reliably to make a FIFO array any number of words deep.

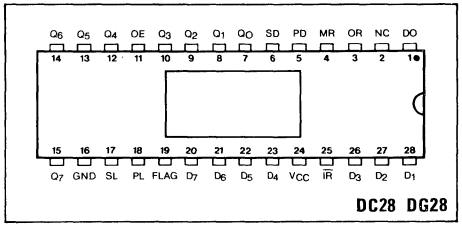


Fig. 1 MJ2812 (32 x 8) pin connections

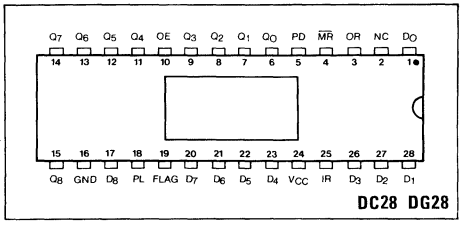


Fig. 2 MJ2813 (32 x 9) pin connections

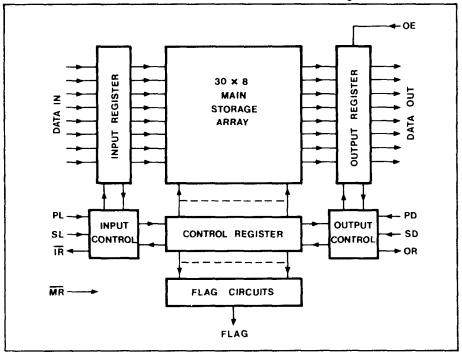


Fig. 3 MJ2812 simplified block diagram

FEATURES

- Serial or Parallel Inputs and Outputs (MJ2812 only)
- 32 Words x 8 Bits (MJ2812) and 32 Words x 9 Bits (MJ2813)
- Easily Stacked — Sideways or Lengthways
- Independent Reading and Writing
- Half-Full FLAG
- Data Rates up to 2.0 Mhz
- TTL — Compatible Tri-state Outputs
- Input and Output Ready Signals
- Master Reset
- Single +5V Supply

APPLICATIONS

- Smoothing Data Rates from Keyboards
- Buffer Between Differently-Clocked Systems (Short Fast Bursts into Steady Data Stream, and Vice Versa)
- Temporary Storage in Error Removing Systems which use Repeated Transmission
- Buffer Store in Interrupt-Orientated Systems
- Computer-to-Line Printer Buffer

OPERATING RANGE

Type number	Ambient temperature	V_{CC}	Ground
MJ2812/MJ2813	0°C to +70°C	5.0V ±5%	0V
MJ2812M/MJ2813M	−55°C to +125°C	5.0V ±5%	0V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
As specified in Operating Range table (above)

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4			V	$I_{OH} = -0.3mA$
Output low voltage	V_{OL}			0.4	V	$I_{OL} = 1.6mA$
Input high voltage	V_{IH}	2.5			V	
Input low voltage	V_{IL}			0.8	V	
Input leakage current	V_{IL}			10	µA	$V_{IN} = 0V$
Input high current	V_{IH}			10	µA	$V_{IN} = 5.25V$
V_{CC} current	I_{CC}		70	114	mA	$T_A = 0°C$ to +70°C
			70	120	mA	$T_A = -55°C$ to +125°C

Switching Characteristics

Characteristic	Symbol	Type	Value			Units	Conditions
			Min.	Typ.	Max.		
Maximum parallel load or dump frequency	f_p	2812/3	2.0			Mhz	
		2812M/3M	1.5			MHz	
Delay, PL or SL high to IR inactive	t_{IR+}	2812/3	25	90	200	ns	
		2812M/3M	20	90	250	ns	
Delay, PL or SL low to IR active	t_{IR-}	2812/3	60	140	350	ns	
		2812M/3M	55	140	400	ns	
Minimum PL or PD high time	$t_{pwH(P)}$	All			80	ns	
Minimum PL or PD low time	$t_{pwL(P)}$	All			100	ns	
Minimum SL or SD high time	$t_{pwH(S)}$	All			80	ns	
Minimum SL or SD low time	$t_{pwl(S)}$	All			80	ns	
Data hold time	$t_{h(D)}$	All		130	200	ns	
Data set-up time	$t_{s(D)}$	All			0	ns	to PL
		All			0	ns	to SL
Delay, PD or SD high to OR low	t_{OR+}	2812/3	45	110	240	ns	OE high
		2812M/3M	40	110	260	ns	OE high
Delay, PD or SD low to OR high	t_{OR-}	2812/3	64	180	400	ns	DE high
		2812M/3M	60	180	400	ns	DE high
Ripple through time	t_{PT}	2812/3	0.4	1.0	2.5	µs	FIFO empty
		2812M/3M	0.4	1.0	3.0	µs	FIFO empty
Delay, OR low to data out changing	t_{DH}	All	35	90		ns	PD=low
Delay, data out to OR high	t_{DA}	All	0	70		ns	PD=high
Minimum reset pulse width	t_{MRW}	2812/3			290	ns	
		2812M/3M			300	ns	
Delay, OE low to output off	t_{DO}	All			250	ns	
Delay, OE high to output active	t_{EO}	All			250	ns	
Delay from PL or SL low to FLAG high or PD or SD low to FLAG low	t_{DF}	All			1.0	µs	
Input capacitance	c_I	All			7	pF	

NOTES
1. IR is active high on MJ2813 and active low on MJ2812
2. Minimum and maximum delays generally occur at opposite temperature extremes. Devices at approximately the same temperature will have compatible switching characteristics and will drive each other.

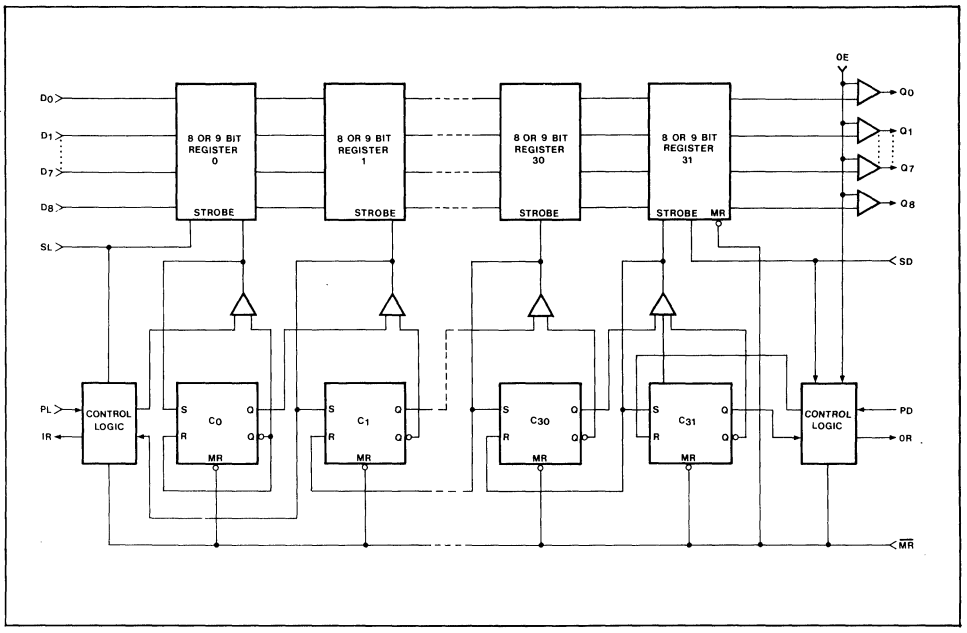


Fig. 4 Logic block diagram

MJ2812 AND MJ2813 FIFO OPERATION

The MJ2812 and MJ2813 FIFO's consist internally of 32 data registers and one 32-bit control register, as shown in the logic block diagram. A '1' in a bit of the control register indicates that a data word is stored in the corresponding data register. A '0' in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the (n)th bit of the control register contains a '1' and the (n+1)th bit contains a '0', then a strobe is generated causing the (n+1)th data register to read the contents of the (n)th data register, simultaneously setting the (n+1)th control register bit and clearing the (n)th control register bit, so that the control strobe moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are 'empty' locations ahead of it. The fall through operation stops when the data reaches a register n with a '1' in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the data inputs by applying a low-to-high transition on the parallel load (PL) input. A '1' is placed in the first control register bit simultaneously. The first control register bit is returned buffered, to the input ready (IR) output, and this pin goes inactive indicating that data has been entered into the first data register and the input is now 'busy', unable to accept more data. When PL next goes low, the fall-through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This caused IR to go active, indicating the inputs are available for another data word.

Note: The device will malfunction if a data load is attempted when the inputs are not ready (as indicated by the IR output signals).

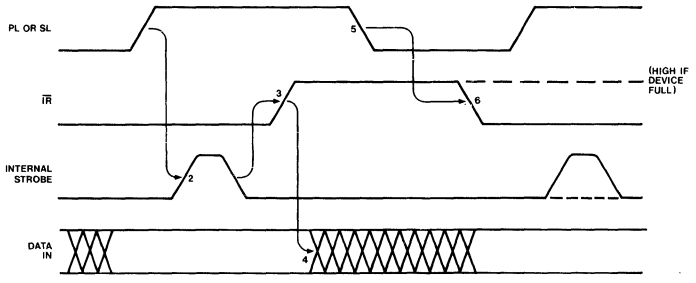
The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A high on OR indicates there is a '1' in the last control register bit and therefore there is valid data on the data outputs. A parallel dump command is used to shift the data word out of the FIFO. A low-to-high transition on PD clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When PD goes low, the '0' which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The '0' in the control register than 'bubbles' back toward the input as the data shifts toward the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and PD goes high, OR will go low as before, but when PD next goes low, there is no data to move into the last location, so OR remains low until more data arrives at the output. Similarly, when the memory is full data written into the first location will not shift into the second when PL goes low, and IR will remain inactive instead of returning to an active state.

The pairs of input and output control signals are designed so that the PD input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the PL input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFO's to operate together.

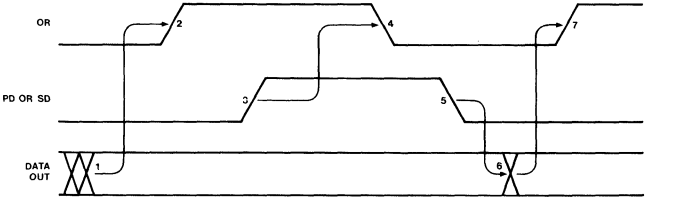
ABSOLUTE MAXIMUM RATINGS

Storage temperature	−65°C to +150°C
Temperature (ambient) under bias	−55°C to +125°C
Voltage on any pin w.r.t. ground (0V)	−0.3V to +9V
DC input voltage	−0.3V to +6V



MJ2812 INPUT TIMING

When data is steady PL is brought high (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes high (3) and data may be changed (4). $\overline{IR}$ remains high until PL is brought low (5); then $\overline{IR}$ goes low (6) indicating new data may be entered.



MJ2812 OUTPUT TIMING

When data out is steady (1), OR goes high (2). When PD goes high (3), OR goes low (4). When PD goes low again (5), the output data changes (6) and OR returns high (7).

The input and output timing diagram above illustrate the sequence of control on the MJ2812. Note that PL matches OR and $\overline{IR}$ matches PD in time, as though the signals were driving each other. The MJ2813 pattern is similar, but IR is active high instead of active low.

Fig. 5 MJ2812 timing diagram

Because the input ready signal is active low on the MJ2812 a peculiarity occurs when several devices are placed end-to-end. When the second unit of two MJ2812's fills up, the data out of the first is not dumped immediately. That is, no shift out command occurs, so that the data last written into the second device remains on the output of the first until an empty location bubbles up from the output. The net effect is that n MJ2812s connected end-to-end store 31n+1 words (instead of 32n). The MJ2813 stores 32n words in this configuration, because IR is active high and does dump the last word written into the second device.

Flag Output

A flag output is available on the MJ2812 and MJ2813 to indicate when the FIFO is approximately half full. Assuming the memory is empty, the flag output will go high within 1μs of the 14th word being loaded into the memory (14 high-low transitions on PL or 112 transitions on SL). Assuming a full memory the flag output will go low within 1μs of the 20th PD or 160th SD high-low transition, ie. when 13 words remain in the memory.

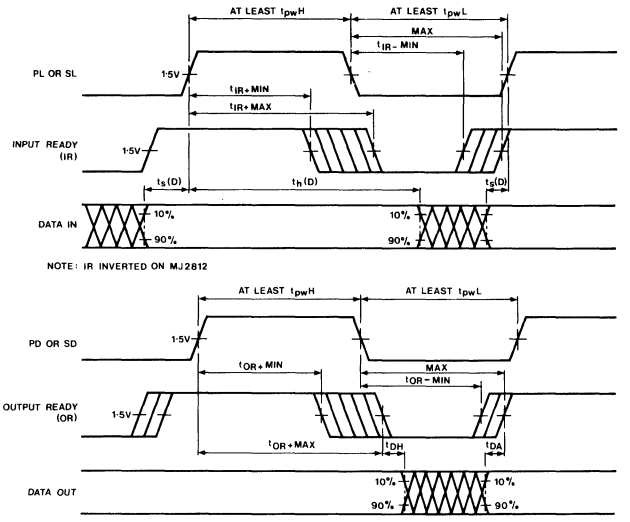
Serial Input and Output (MJ2812 Only)

The MJ2812 also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using the serial load input and applying data to D_0 input.

The SL signal operates just like the PL input, causing IR to go high and low as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they have been loaded in parallel. Following the 8th SL pulse, IR will remain inactive if the FIFO is full.

A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the Q_7 output. OR moves high and low with SD exactly as it does with PD. When 8 bits have been shifted out, the next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and the new 8-bit word is brought to the output. OR will stay low if the FIFO is empty.

When the serial input or output clock is used, the corresponding parallel control line should be grounded and when the PD or PL controls are used the corresponding serial clocks should be grounded.



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DONT CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

Fig. 6 Timing diagram

OPERATING NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain low, indicating data at the output is not valid.

2. When the output data changes as a result of a pulse on PD, the OR signal always goes low before there is any change in output data and always stays low until after the new data has appeared on the outputs, so anytime OR is high, there is good, stable data on the outputs.

3. If PD is held high while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go high for one internal cycle (at least t_{OR+}) and then will go back low again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until PD has been brought low.

4. When the master reset is brought low, the control register and the outputs are cleared and the control logic is initialised. $\overline{IR}$ and OR go low. If PL is high when the master reset goes high then $\overline{IR}$ will remain in the high state until PL is brought low. If PL is low when the master reset is ended, then $\overline{IR}$ will be low until PL goes high.

5. The output enable pin OE inhibits dump commands while it is low and forces the Q outputs to a high impedance state.

6. The serial load and dump lines should not be used for interconnecting two FIFOs. Use the parallel interconnection instead.

7. If less than eight bits have been shifted in using the serial load command, a parallel load pulse will destroy the data in the partially filled input register.

8. The $\overline{IR}$ and OR signals are provided to ensure that data is written into, or read out of, the FIFO correctly. If the specified minimum pulse widths, for PL, SL, PD or SD are not provided *after* an $\overline{IR}$ or OR transition the memory may corrupt and lock out any further data input. The memory should be cleared to restore normal operation.

PLESSEY
Semiconductors

MJ2841

64-WORD x 4-BIT FIRST-IN FIRST-OUT SERIAL MEMORY

The MJ2841 is an asynchronous first-in first-out memory stack, organized as 64 four-bit words. The device accepts a four bit parallel word D_0-D_3 under control of the shift in (SI) input. Data entered into the FIFO immediately ripples through the device to the outputs Q_0-Q_3. Up to 64 words may be entered before any words are read from the memory. The stored words line up at the output end in the order in which they were written.

A read command on the shift out input (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals act as memory full and memory empty flags and also provide the necessary pulses for interconnecting FIFO's to obtain deeper stacks.

Parallel expansion to wider words only requires that rows if FIFO's be placed side by side. Reading and writing operations are completely independent, so the device can be used as a buffer between two digital machines operating asynchronously and at widely differing clock rates.

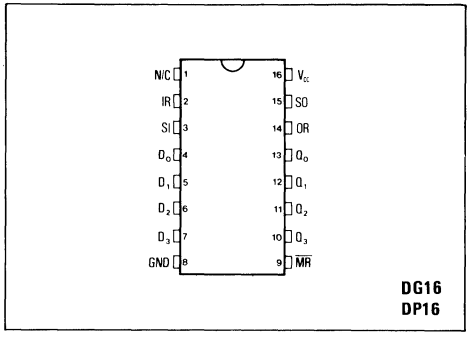


Fig.1 Pin connections (top view)

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-55°C to +125°C
Ambient operating temperature	-10°C to +85°C
Lead temperature (soldering, 10s max.)	330°C
Voltage on any pin with respect to ground	-0.3V to +7V

FEATURES

- Single 5V Supply
- 1.75MHz Guaranteed Data Rate (Typically 4MHz)
- Pin Compatible with AM2841/Fairchild 3341
- Asynchronous Buffer For Up To 64 Four Bit Words
- Easily Expandable To Larger Buffers

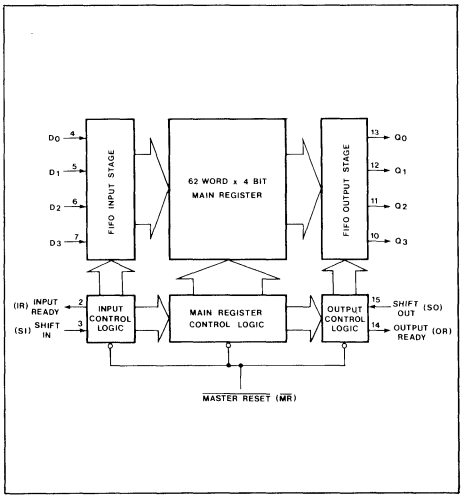
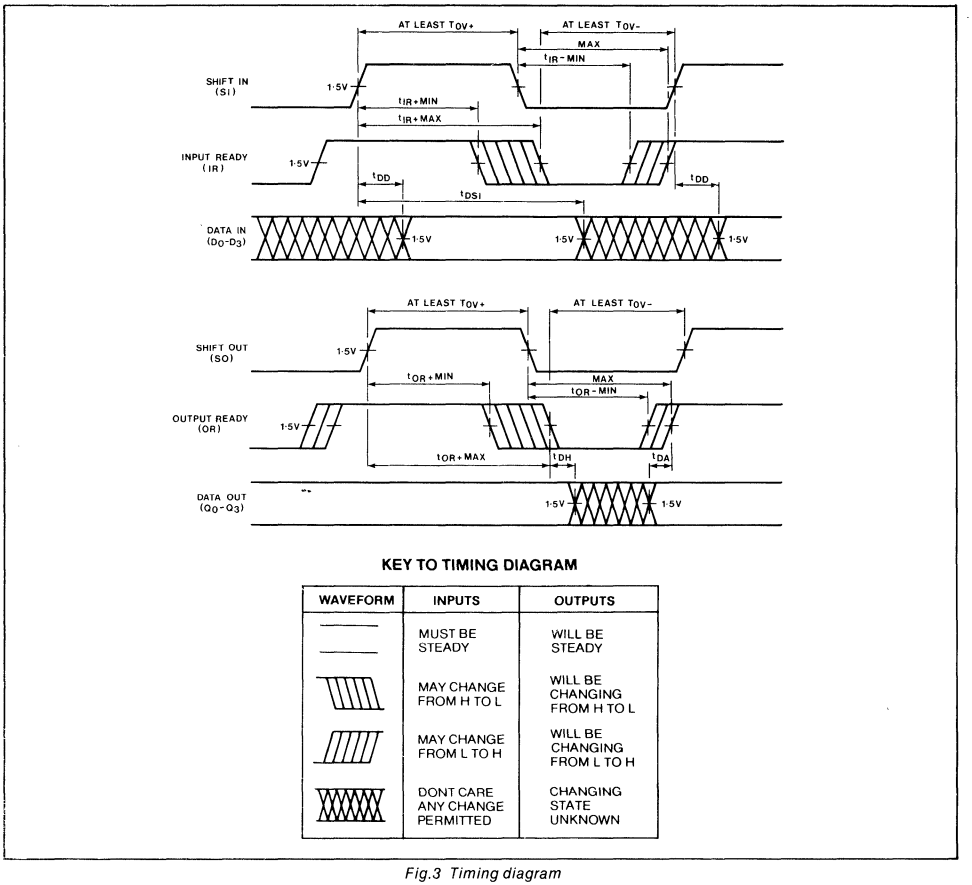


Fig.2 Block diagram

MJ2841 FIFO OPERATION

The MJ2841 FIFO consists internally of 64 four-bit data registers and one 64-bit control register, as shown in the logic block diagram. A '1' in a bit of the control register indicates that a four-bit data word is stored in the corresponding data register. A '0' in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the n^{th} bit of control register contains a '1' and the (n+1)th bit contains a '0', then a strobe is generated causing the (n+1)th data register to read the contents of the n^{th} data register, simultaneously setting the (n+1)th control register bit, so that the control flag moves with the data. In this fashion, data in the data register moves down the stack of data registers toward the output as long as there are 'empty' locations ahead of it. The fall through operation stops when the data reaches a register n with a '1' in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the four data inputs D_0-D_3 by applying a low to high transition on the shift in (SI) input. A '1' is placed in the first control register bit simultaneously. The first control register bit is returned, buffered, to the input ready (IR) output, and this pin goes low indicating that data has been entered into the first data register and



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DONT CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

Fig.3 Timing diagram

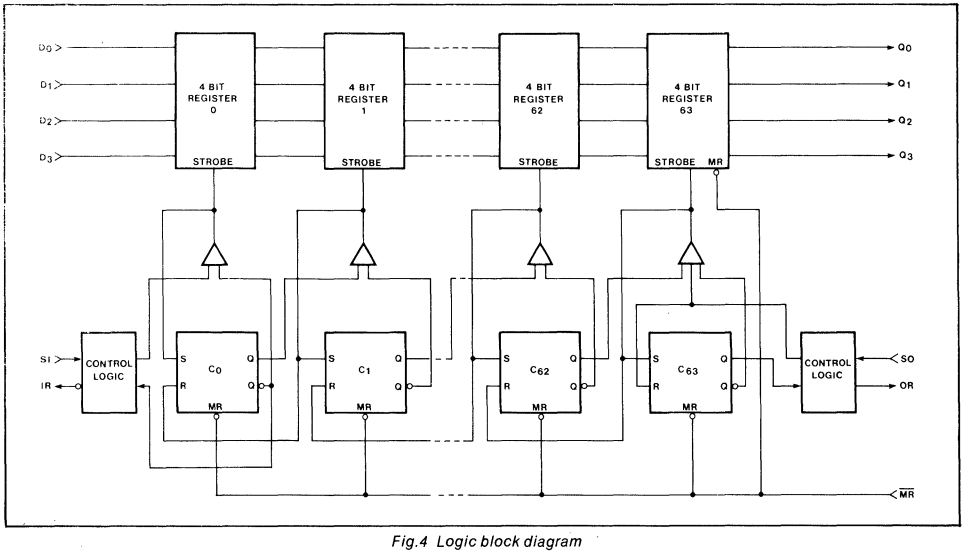


Fig.4 Logic block diagram

the input is now 'busy' unable to accept more data. When SI next goes low the fall-through process begins, (assuming that at least the second location is empty). The data in the first register is copied into the second and the first control register bit is cleared. This causes IR to go high indicating the inputs are available for another data word.

The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output ready (OR). A high on OR indicates there is a '1' in the last control register bit and therefore there is valid data on the four data outputs Q_0-Q_3. An input signal, shift out (SO) is used to shift the data out of the FIFO. A low to high transition on SO clears the last register bit, causing OR to go low, indicating that the data on the outputs may no longer be valid. When SO goes low, the '0' which is now present at the last register allows the data in the next to last register position to move into the last register position and on to the outputs. The '0' in the control register then 'bubbles' back towards the input as the data shifts towards the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and SO goes high, OR will go low as before, but when SO next goes low, there is no data to move into the last location so OR remains low until more data arrives at the output. Similarly, when the memory is full, data written into the first location will not shift into the second when SI goes low, and IR will remain low instead of returning to a high state.

The pairs of input and output control signals are designed so that the SO input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the SI input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFO's to operate together.

An over-riding master reset ($\overline{MR}$) is used to reset all control register bits and remove the data from the output (i.e. reset the outputs to all low).

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage (V_{CC}) = +5V ±5%, T_{amb} = 0°C to +70°C
Typical Values at V_{CC} = 5V and T_{amb} = +25°C
All voltages with respect to ground

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
O/P high voltage	V_{OH}	2.7	3.2		V	I_{OH} = -0.2mA
O/P low voltage	V_{OL}		0.2	0.5	V	I_{OL} = 2mA
I/P high level	V_{IH}	2.5			V	
I/P low level	V_{IL}			0.8	V	
I/P leakage current	I_{IL}	-5		+10	μA	V_{IN} = 0V or 5V
Supply current	I_{CC}		50	81	mA	

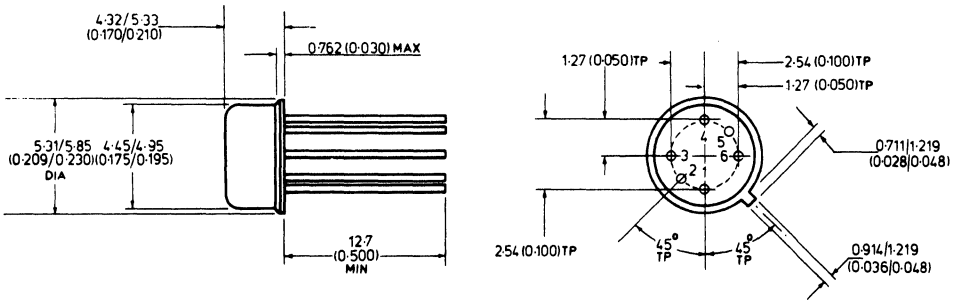
Switching Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. SI or SO frequency	f_{MAX}	1.75	4.4		MHz	
Delay, SI high to IR low	$t_{IR}+$		50	120	ns	
Delay, SI low to IR high	$t_{IR}-$		80	200	ns	
Min. time SI and IR both high	$t_{OV}+$		<25	45	ns	
Min. time SI and IR both low	$t_{OV}-$		<25	45	ns	
Data release time	t_{DSI}		45	110	ns	
Data set-up time	t_{DD}		45	110	ns	
Delay, SO high to OR low	$t_{OR}+$		80	190	ns	
Delay, SO low to OR high	$t_{OR}-$		120	290	ns	
Ripple through time	t_{PT}		2.5	7	μs	FIFO empty
Delay, OR low to data out	t_{DH}	50	85		ns	SO = low
Min. reset pulse width	t_{MRW}		20	50	ns	
Delay, data out to OR high	t_{DA}	0	35		ns	SO = high
Input capacitance	CI			7	pF	Any pin

OPERATING NOTES

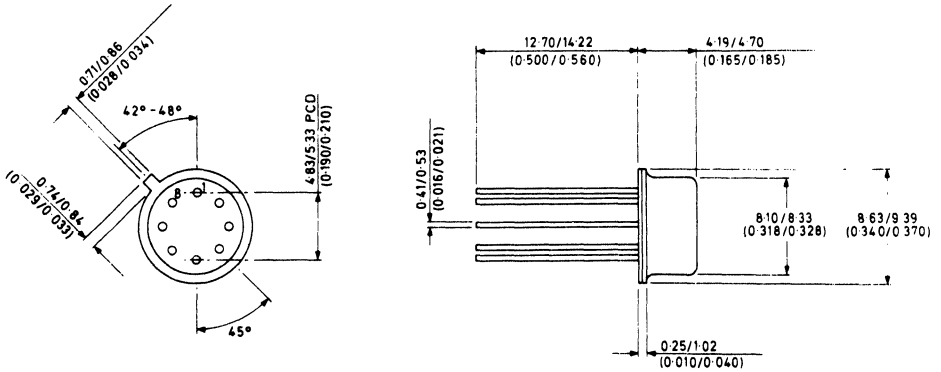
1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However OR will remain low, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes low before there is any change in output data and always stays low until after the new data has appeared on the outputs, so anytime OR is high, there is good, stable data on the outputs.
3. If SO is held high while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go high for one internal cycle (at least $t_{OR}+$) and then will go back to low again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought low.
4. When the master reset is brought low, the control register and the outputs are cleared. IR goes high and OR goes low. If SI is high when the master reset goes high then the data on the inputs will be written into the memory and IR will return to the low state until SI is brought low. If SI is low when the master reset is ended, the IR will go high, but the data on the inputs will not enter the memory until SI goes high.

7. Packages



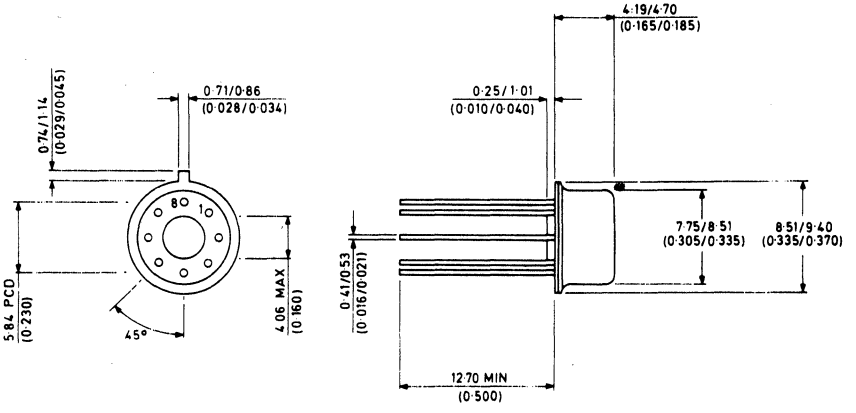
6 LEAD TO-71

CM6



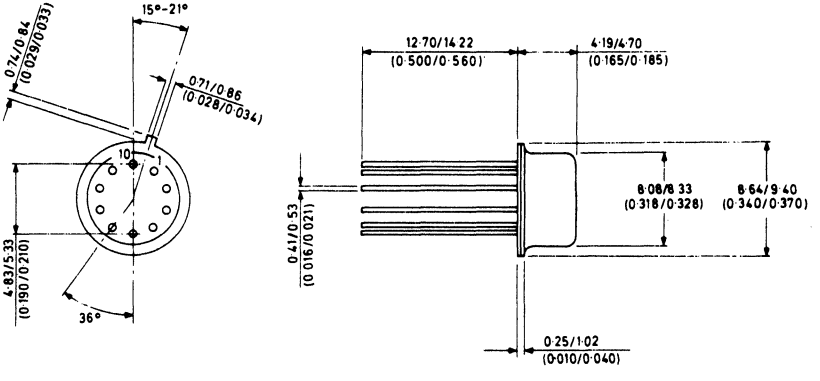
8 LEAD TO-5 (5·08mm PCD)

CM8



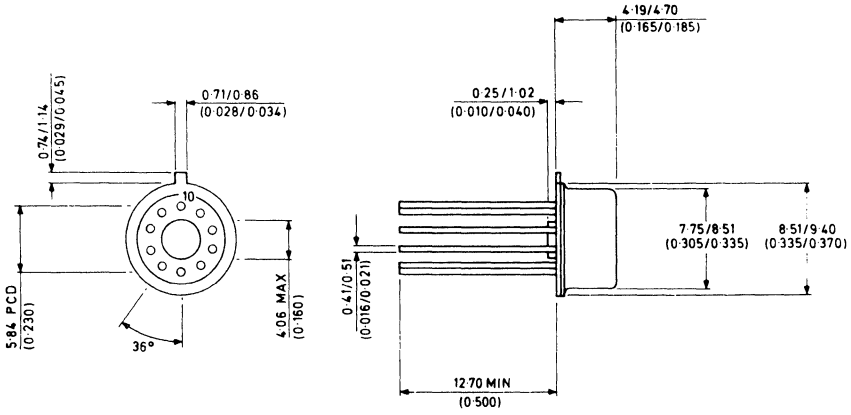
8 LEAD TO-5 (5·84mm PCD) WITH STANDOFF

CM8



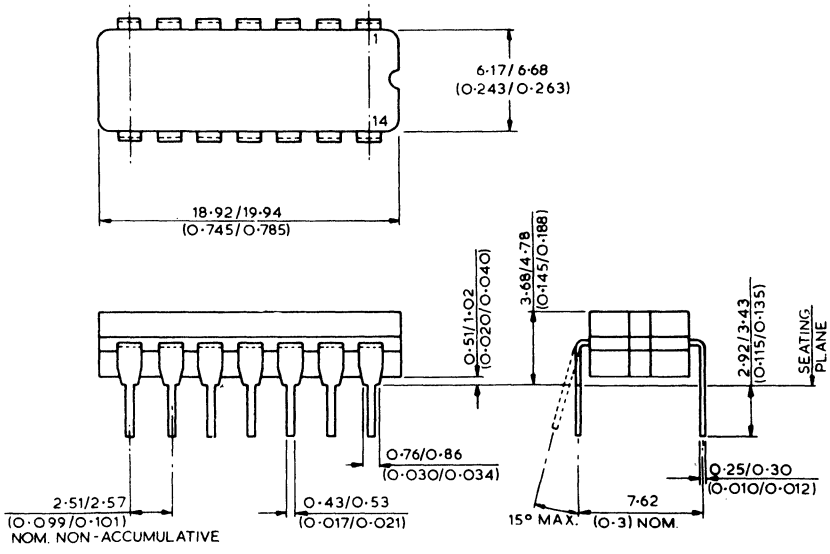
10 LEAD TO-5

CM10



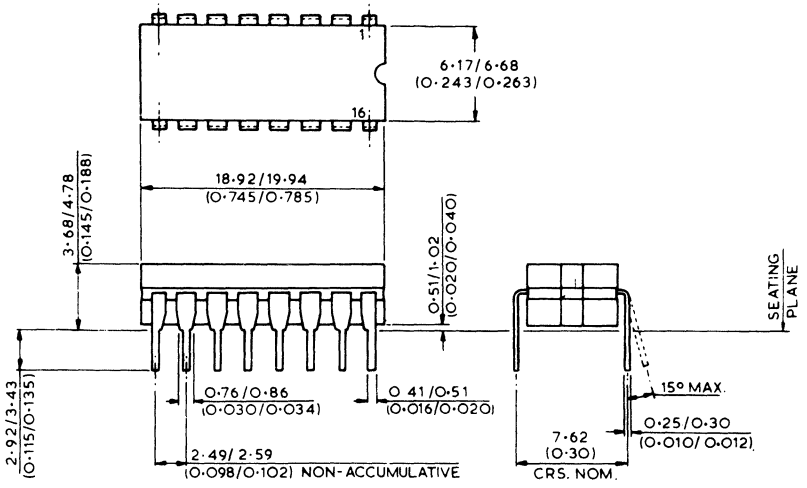
10 LEAD TO-100 (5·84 mm PCD) WITH STANDOFF

CM10



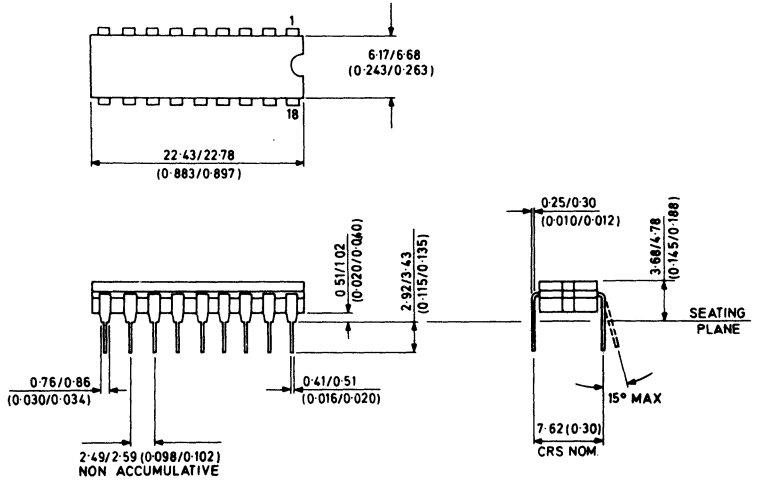
DG14

14 LEAD CERAMIC D.I.L.



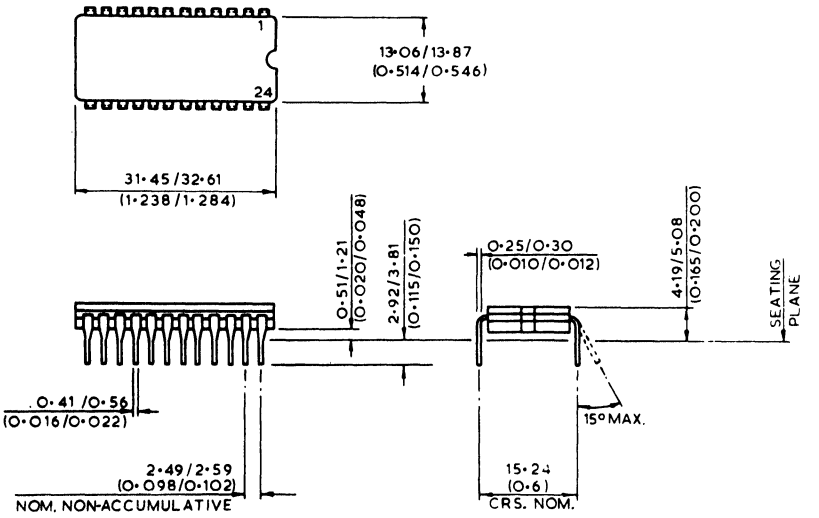
16 LEAD CERAMIC D.I.L.

DG16

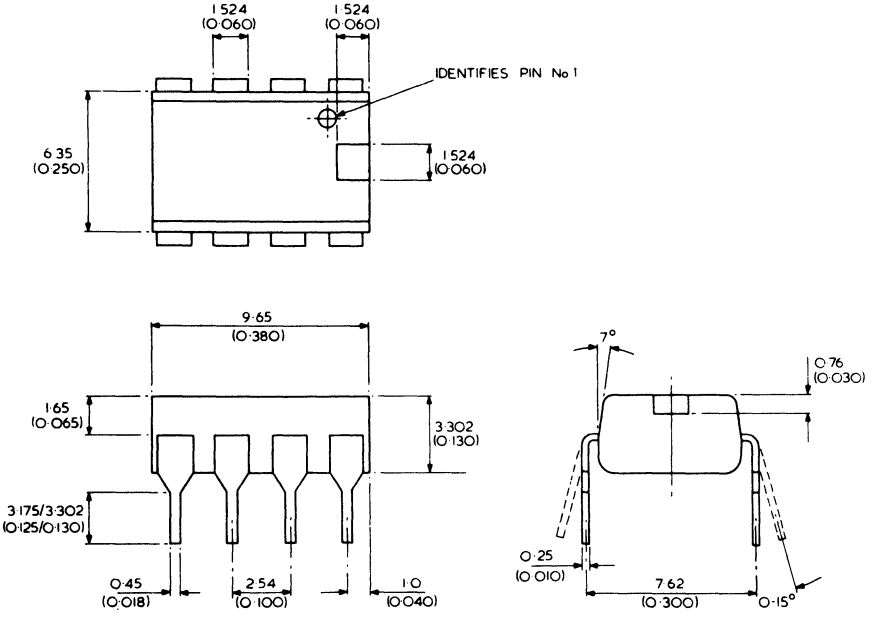


18 LEAD CERAMIC DIL

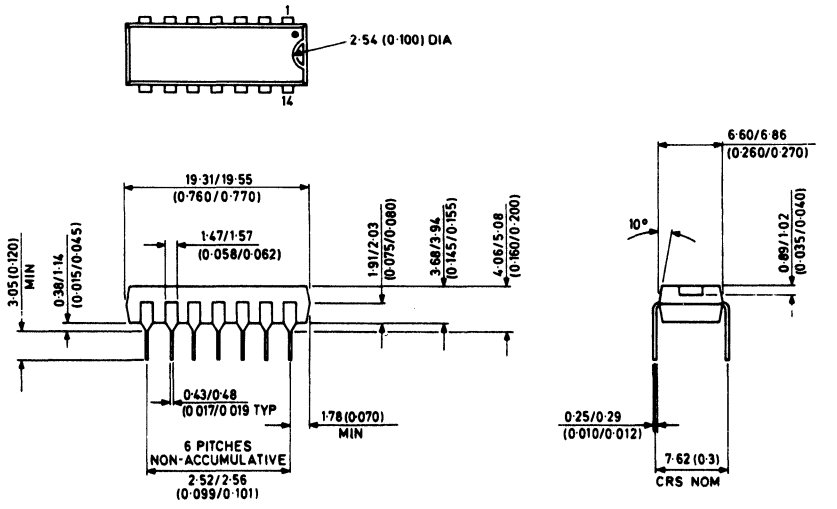
DG18



DG24 24 LEAD CERAMIC D.I.L.

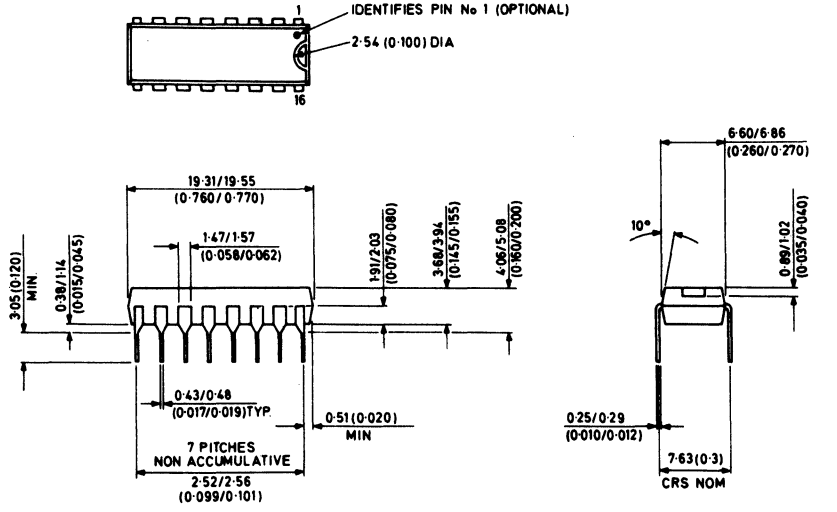


DP8 8 LEAD PLASTIC D.I.L.



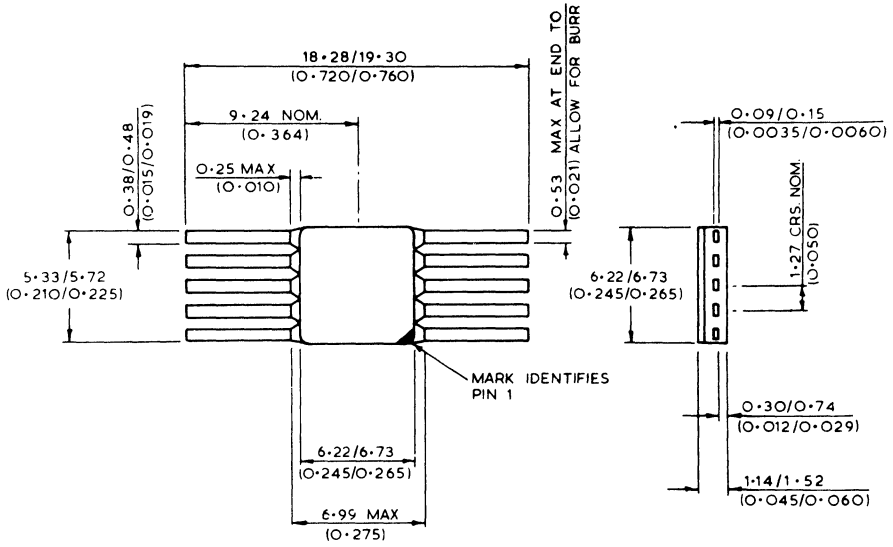
14 LEAD PLASTIC D.I.L.

DP14

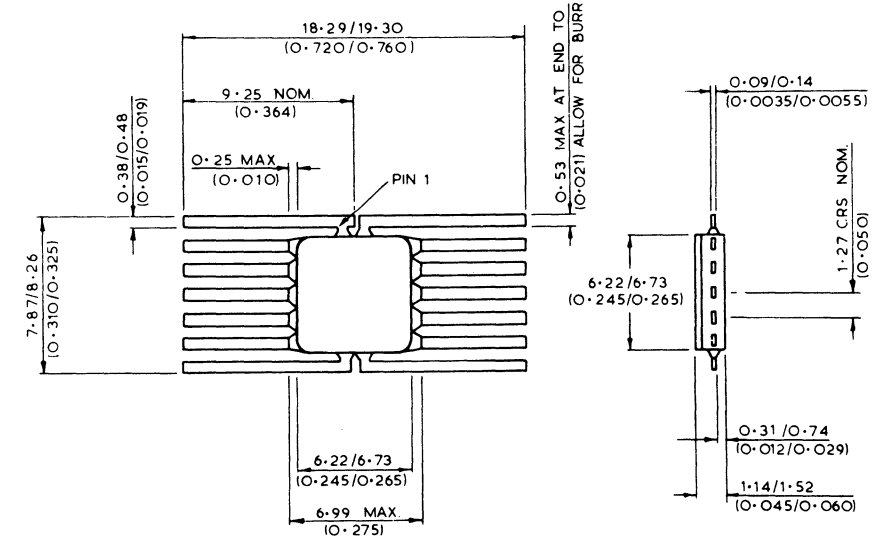


16 LEAD PLASTIC DIL

DP16



GM10 10 LEAD FLAT PACK



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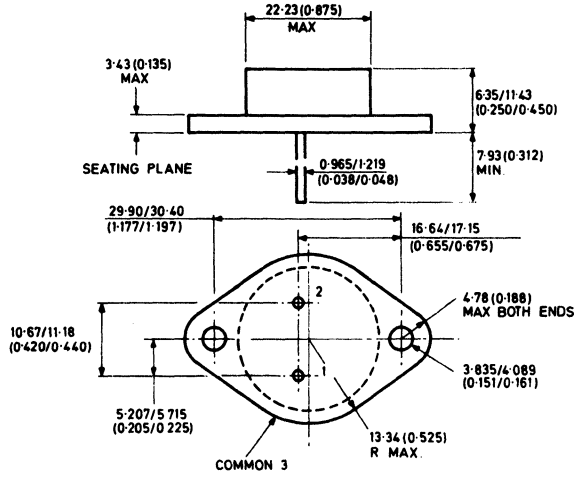
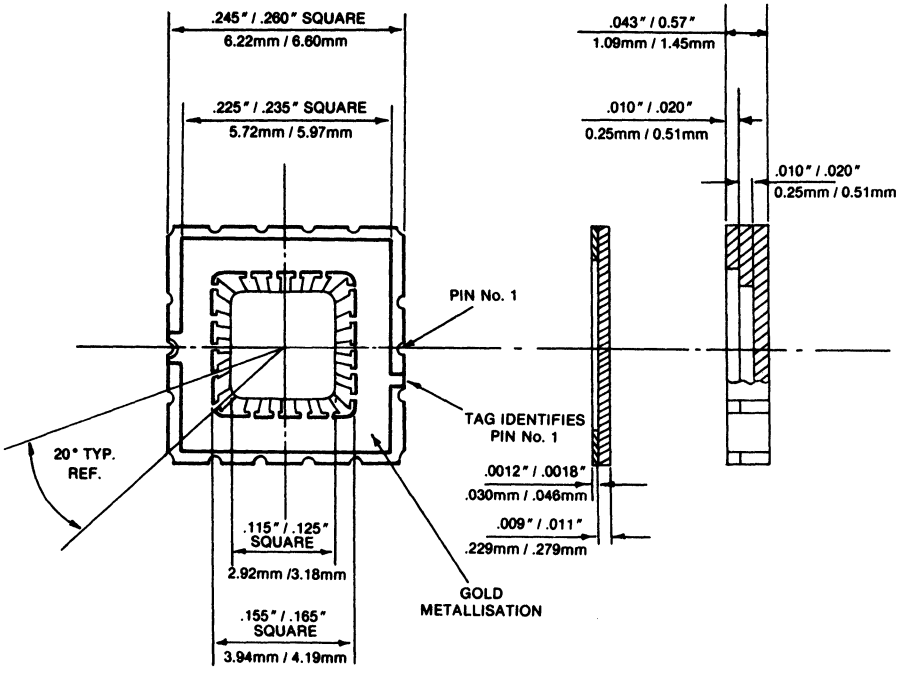


NOTE : CASE IS THIRD ELECTRICAL CONNECTION

TO-3

KM 3



18 LEAD LEADLESS CARRIER

GC 18

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