OTI-069 - VIDEO PIXEL CLOCK GENERATOR

Introduction

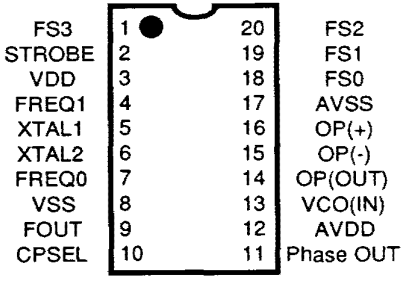
The OTI-069 Pixel Clock Generator is an integrated circuit specifically designed for generating the video pixel frequencies required by display adapter cards based on the OTI-067. Utilizing CMOS technologies to implement all linear, digital, and memory functions, the OTI-069 provides a low power, low cost, small footprint solution to the generation of video pixel clocks. Output frequencies provide compatibility with VGA, EGA, MCGA, CGA, MDA, as well as higher frequencies needed for advanced applications in Desktop Publishing and Workstation graphics. Phase-locked-loop circuitry permits rapid, glitch-free transitions between clock frequencies.

A 14.31818 MHz series-resonant crystal with no additional external components is all that is required for generating the video pixel frequencies. A 6 MHz bandwidth CMOS op-amp, included in the device, permits fast frequency acquisition and decreases phase jitter and susceptibility to externally generated noise. All output circuits are optimized for TTL compatibility.

Features

- Low power CMOS device technology
- Low cost solution
- Small footprint - 20 pin DIP
- Advanced PLL - low phase jitter
- High frequency operation for extended video modes
- Fast acquisition of selected frequencies

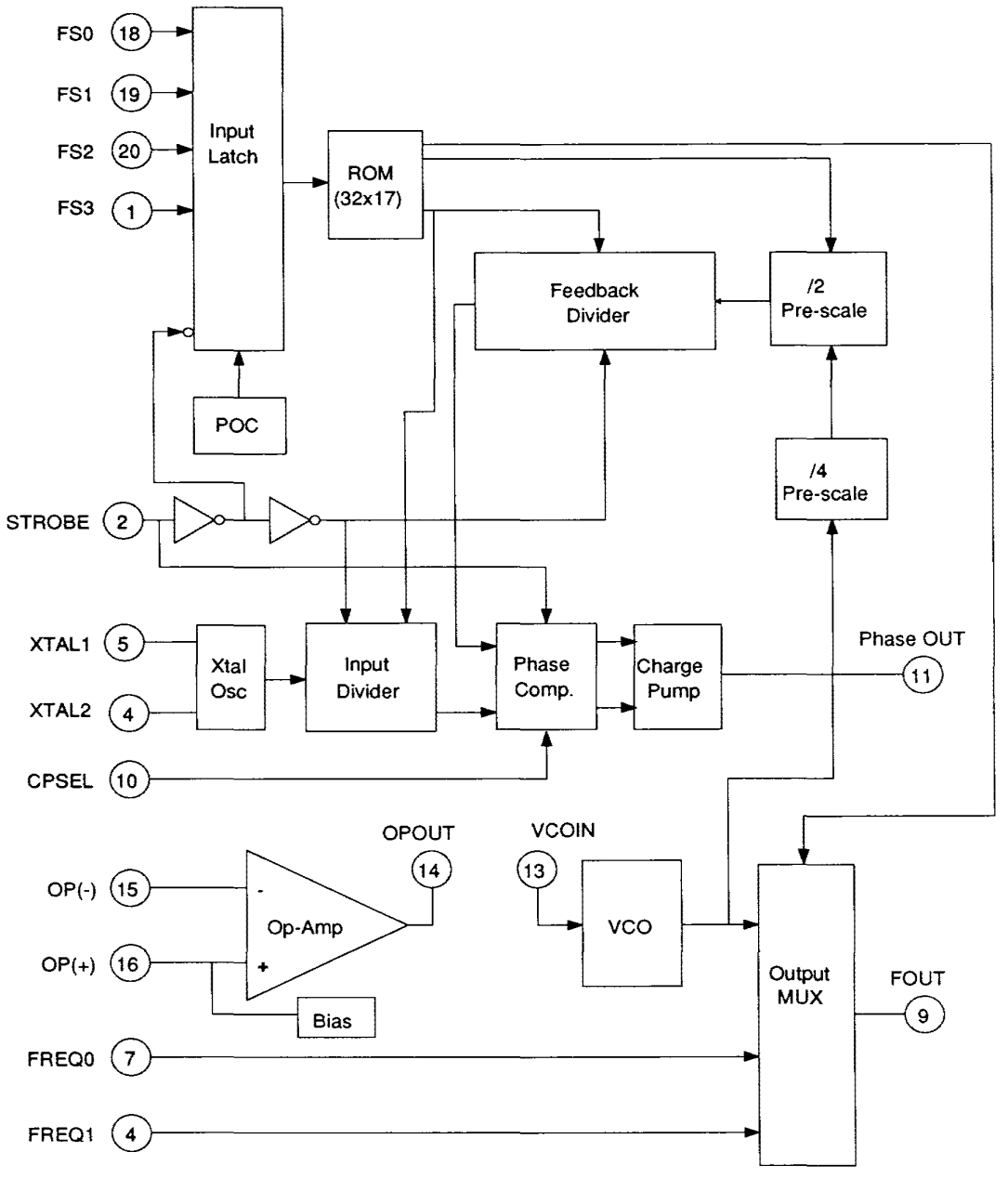
Pin Connections



Pin Functions

Pin Name	Pin Number	Description
FS0	18	Frequency Select input, TTL compatible (LSB)
FS1	19	Frequency Select input, TTL compatible (LSB)
FS2	20	Frequency Select input, TTL compatible (LSB)
FS3	1	Frequency Select input, TTL compatible (MSB)
STROBE	2	Negative edge clock for select inputs, TTL compatible
FREQ0	7	Externally generated frequency input
FREQ1	4	Externally generated frequency input
FOUT	9	Clock output, TTL compatible
XTAL1	5	Crystal interface / External oscillator input
XTAL2	6	Crystal interface
VDD	3	5-Volt digital power pin
AVDD	12	5-Volt analog power pin
VSS	8	Digital ground
AVSS	17	Analog ground
CPSEL	10	Phase comparator polarity select (pull up to VDD if left open)
OUT	11	Phase comparator output
VCO(IN)	13	Voltage-controlled oscillator input
OP(OUT)	14	Op-amp output
OP(–)	15	Op-amp negative input
OP(+)	16	Op-amp positive input (AVDD referenced, if open)

Block Diagram



Applications

Utilizing the OTI-069 with the OTI-067 is simple, but does require precautions in board layout if satisfactory jitter-free performance is to be realized. A low series inductance bypass capacitor of 0.047μF should be connected between digital VSS and VDD. AVSS should be connected to +5-volts at the card edge connector. Care should be exercised in insuring that components not related to the OTI-069 do not use this ground. AVDD should be isolated from VDD with a 100Ω resistor and be decoupled with a 75μF tantalum capacitor in parallel with a 0.047μF ceramic capacitor. The 0.047μF ceramic capacitor should be as physically close to AVDD as is practical, to insure low lead inductances between AVDD and AVSS. A 5.1-volt zener diode and appropriate dropping resistor to power the analog circuitry may be used instead of the 75μF tantalum capacitor. This should be connected to the +12-volt supply, and will provide improved noise rejection and require less board space. The 0.047μF capacitor should still be utilized to provide high frequency bypassing.

The internal op-amp should be configured as the loop filter. VCO frequency is determined by the voltage that exists between AVDD and VCO(IN), with frequency increasing as VCO(IN) approaches AVSS. The positive input to the internal op-amp, OP+ is internally biased and bypassed to AVDD. An additional 0.047μF ceramic capacitor should be connected between OP+ and AVSS to provide adequate low frequency decoupling. Normally, a 100KΩ resistor should connect FOUT and OP–. A 1μF tantalum capacitor in series with a 150Ω resistor should be connected between OP(OUT) and OP–, with the positive lead of the capacitor connected to OP(OUT). OP(OUT) should be directly connected to VCO(IN). This configuration provides a noise immune virtual ground, and eliminates noise induced phase jitter in the output frequency spectrum. All passive loop filter components should be laid out tightly to minimize noise pickup. Digital signals should be spaced well away from these components.

CPSEL determines the polarity of the charge pump output. It is internally pulled high, but should be connected directly to VDD for improved noise immunity if the op-amp or any other external active filter which inverts the signal is used. Connect CPSEL to VSS when using passive filter configurations.

If rapid selection of new pixel clock frequencies is desired, logic which utilizes the strobed input option should be employed. This forces phase correction information to be in the proper direction immediately after a frequency change is requested. This consequently results in a minimum time lapse in locking in the new frequency.

FS0, FS1, FS2, and FS3 are the TTL-compatible frequency select inputs. They accept the binary code corresponding to the frequency desired. STROBE transfers these inputs on the positive edge. In addition, STROBE causes the output of the charge pump to assume the high impedance state and forces the feedback and reference dividers to a zero count while STROBE is high. When STROBE is returned low, both feedback and reference dividers are enabled along with the charge pump. The phase comparator will respond correctly to whichever divider clocks out first with a correction pulse in the appropriate direction. The internal power-on-clear signal will force an initial frequency code corresponding to an all-zeros input state.

The internal reference oscillator contains all of the passive components required. A 14.31818 MHz series resonant crystal should be connected between XTAL1 and XTAL2. Maintain short lead lengths between the crystal and the OTI-069. Solder the crystal to the ground plane to minimize noise pickup.

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects FOUT and other components in the system should be kept as short as possible. It may be helpful to place a ferrite bead in this signal path to limit the propagation of high-order harmonics of FOUT. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the OTI-069. A 33Ω to 47Ω series resistor in this path may be necessary to reduce capacitive loading of the signal, and may reduce phase jitter as well as EMI.

Clock Select Frequencies

As shown in the following table, only three frequency select inputs are required for selecting one of the eight clock frequencies required by the OTI-069.

Primary Table (FS3 = 0)

FS3	FS2	FS1	FS0	CLOCK (MHz)
0	0	0	0	25.175
0	0	0	1	28.322
0	0	1	0	65.000
0	0	1	1	44.900
0	1	0	0	14.161
0	1	0	1	18.000
0	1	1	0	40.000
0	1	1	1	36.000

Alternate Table (FS3 = 1)

FS3	FS2	FS1	FS0	CLOCK (MHz)
1	0	0	0	25.175
1	0	0	1	28.322
1	0	1	0	78.000
1	0	1	1	65.000
1	1	0	0	63.000
1	1	0	1	72.000
1	1	1	0	40.000
1	1	1	1	50.000

Typical Operating Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage	DV_{DD}, AV_{DD}	4.5	5.0	5.5	Volts
Digital Supply Current (FOUT = 50 MHz, internal xtal oscillator used for Fref.)	DI_{DD}		11	25	mA
Analog Supply Current (FOUT = 50 MHz)	AI_{DD}		3.2	4.5	mA
Output Impedance	Z_{OUT}		33	100	Ohms
Output Drive Current	I_{source}, I_{sink}		4		mA

Op Amp Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Output Voltage Swing (Open Circuit)			AV_{SS}(0)	AV_{DD}(+5)	Volts
Gain Bandwidth Product	VGBW		6		MHz

Phase Comparator Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Gain Constant	K		0.4		Volts/Radian

Bus Timing

Parameter	Symbol	Min	Typ	Max	Units
Setup Timing FS0-FS3 relative to STROBE	T_{setup}	10			nS
Hold Time FS0-FS3 relative to STROBE	T_{hold}	10			nS

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{DD}	-0.5	+7	Volts
Input Voltage	V_{IN}	-0.5	V_{DD}+0.5	Volts
Output Voltage	V_{OUT}	-0.5	V_{DD}+0.5	Volts
Clamp Diode Current	I_{ik} & I_{ok}	-30	30	mA
Output Current	I_{out}	-50	50	mA/Pin
Storage Temperature	T_s	-85	+150	° C
Power Dissipation	P_d		500	mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to ≥ VSS and ≤ VDD.

Low Cost VGA System

Figure 1 shows a block diagam of a low cost VGA adapter using the OTI-067 VGA Graphics Controller, the OTI-066 High Speed, 256 x 18 Color Palette Video DAC, and the OTI-069 Video Pixel Clock Generator.

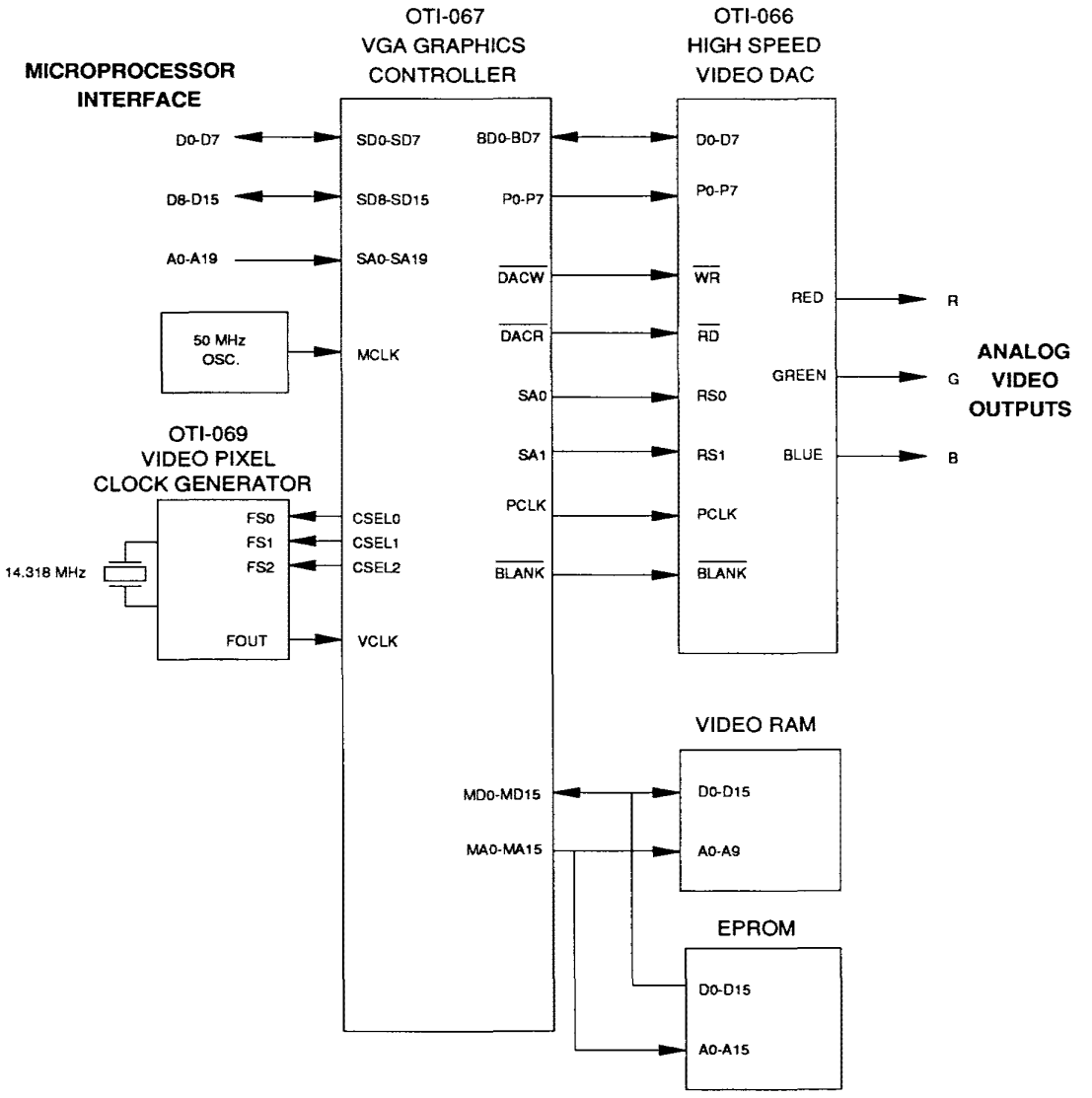


Figure 1. Low-Cost VGA Adapter, Block Diagram

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