NCR
Microelectronics

NCR Microelectronics Short-Form Catalog–1985

NCR Microelectronics

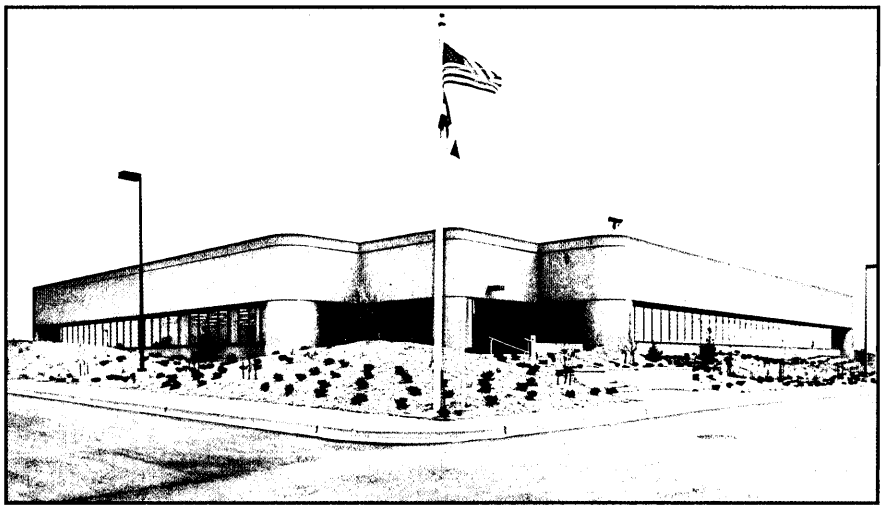
NCR, a multi-billion-dollar manufacturer of computer systems, terminal products, and semiconductors, established its first microelectronics laboratory in 1963 to stay abreast of the emerging semiconductor technology. The laboratory was expanded in 1966 to provide limited quantities of prototype microcircuits designed for use in a number of new products. By 1968 the first MOS circuits were produced, and by 1970 a complete family of circuits had been designed, produced in prototype quantities, and incorporated into new NCR products. Based upon knowledge gained in this research and confidence in the ultimate advantages of MOS, the decision was made to expand the internal production capability. In 1971, the Miamisburg, Ohio plant was completed.

To meet internal demand, NCR expanded its microelectronics operation in 1975 with the addition of a second production facility in Colorado Springs, Colorado, and in 1979 added a third facility in Ft. Collins, Colorado. The Colorado Springs facility was replaced in 1982 by a new plant occupying 100,000 square feet. This new plant is one of the most modern, best-equipped facilities of its kind anywhere.

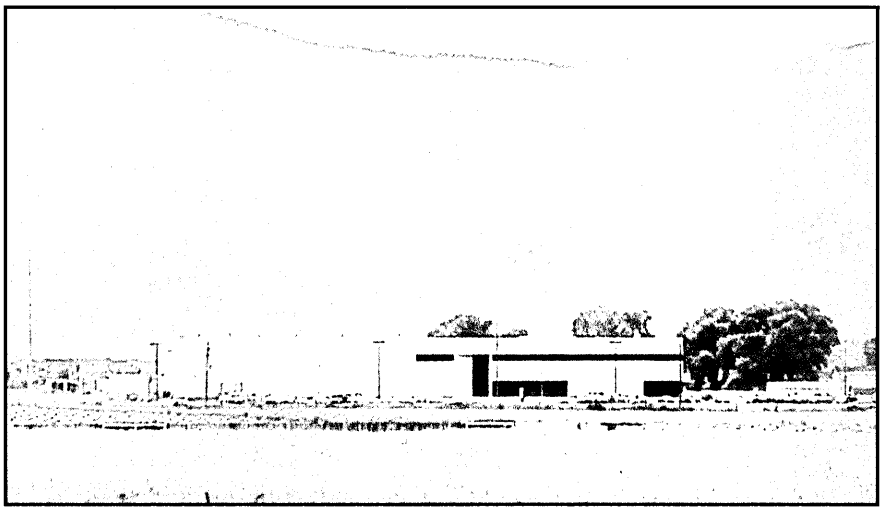
NCR Microelectronics manufactures state-of-the-art NMOS, CMOS, and non-volatile SNOS components which provide a competitive advantage to its computer systems and terminal product lines.

In mid-1981 NCR announced its entry into the merchant semiconductor market. The strength and discipline gained in 10 years of internal supply is now being made available to our customers. This experience, together with a family of innovative products and services, establishes NCR as a leading supplier of semiconductor devices and services.

Colorado Springs, Colorado



Fort Collins, Colorado



Miamisburg, Ohio

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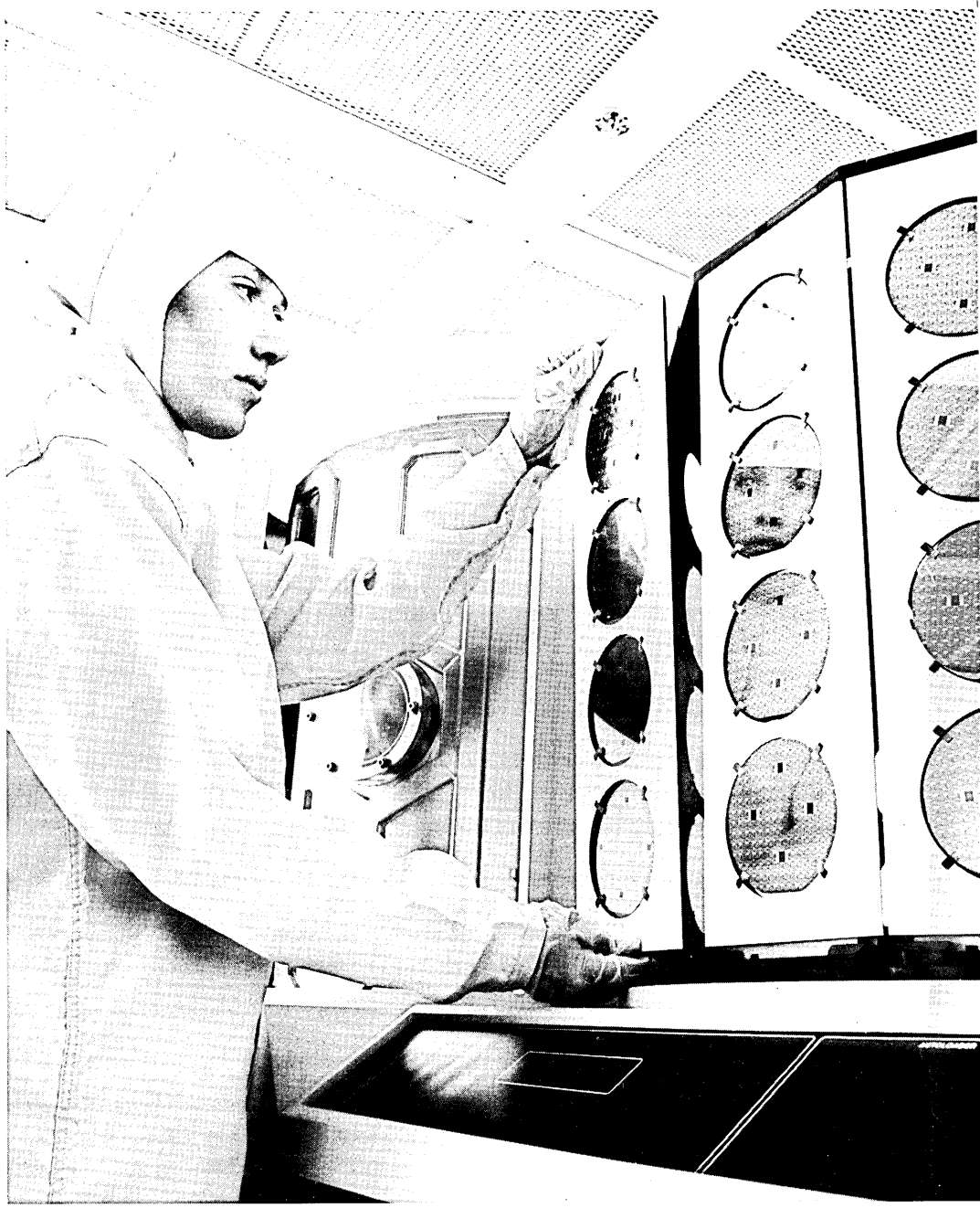
NCR's Commitment to Quality

As a pioneer in microelectronic technology, NCR has been manufacturing components for its own product line since 1971. This experience has provided opportunities to learn about user application problems, the importance of component quality and reliability, and their effects on total system reliability. The net result of such experience is a dedication to manufacturing superior components based on a firm commitment to quality and reliability.

NCR Quality Assurance completes a rigorous evaluation of each product to ensure conformance of the product to its specification. Once a component is approved for production, stringent process and assembly controls along with detailed inspections are used to build in reliability. Comprehensive electrical testing is performed to guarantee the performance of each component; finished products are inspected before shipment to assure the conformance to specification of each lot of devices, and sampling plans are constantly revised and updated to improve quality.

Essential to any reliability program is feedback from the system user—communication that is vital for reliability growth. NCR strives to "close the loop" by communicating with users to evaluate problems and respond with corrective action. The closed-loop concept results in better understanding of user needs while improving reliability.

The NCR commitment to quality and reliability is an integral part of corporate philosophy originating from and emphasized by the highest levels of NCR management. This management direction, combined with NCR's manufacturing and user application experience, provides a solid framework for continued improvement in quality and reliability.



Read Only Memories

NCR offers a full line of high performance Read Only Memories (ROM) with a variety of pinouts and access times. All NCR ROMs are 5 volt only in both commercial and industrial operating temperature ranges. The NCR NMOS and CMOS processes and experience in the ROM market allow NCR to provide fast turnaround of prototype and production quantities plus provide the customer service and support required of a major supplier of ROMs in today's market. Look to NCR for your ROM requirements to insure that your products reach the market place in time for maximum market penetration.

NMOS Read Only Memory Family

Function	Part Number	Organization	Access Time Max (ns)	Supply current Max (mA)		No. of Pins	Characteristics
				Operating	Standby		
16K ROM	NCR 2316-20	2Kx8	200	75	—	24	Static/2716
	NCR 2316-25	2Kx8	250	75	—	24	Static/2716
	NCR 2316-30	2Kx8	300	75	—	24	Static/2716
	NCR 2316-45	2Kx8	450	75	—	24	Static/2716
32K ROM	NCR 2332-20	4Kx8	200	75	—	24	Static/2532
	NCR 2332-25	4Kx8	250	75	—	24	Static/2532
	NCR 2332-30	4Kx8	300	75	—	24	Static/2532
	NCR 2332-45	4Kx8	450	75	—	24	Static/2532
	NCR 2333-20	4Kx8	200	75	—	24	Static/2732
	NCR 2333-25	4Kx8	250	75	—	24	Static/2732
	NCR 2333-30	4Kx8	300	75	—	24	Static/2732
	NCR 2333-45	4Kx8	450	75	—	24	Static/2732
64K ROM	NCR 2364-20	8Kx8	200	60	—	24	Static/2564
	NCR 2364-25	8Kx8	250	60	—	24	Static/2564
	NCR 2364-30	8Kx8	300	60	—	24	Static/2564
	NCR 2364-45	8Kx8	450	60	—	24	Static/2564
	NCR 2364S-20	8Kx8	200	60	10	24	Static/Standby
	NCR 2364S-25	8Kx8	250	60	10	24	Static/Standby
	NCR 2364S-30	8Kx8	300	60	10	24	Static/Standby
	NCR 2364S-45	8Kx8	450	60	10	24	Static/Standby
	NCR 2364A-45*	Two 4Kx8 Banks	450	60	—	24	Static/Bank Select
	NCR 2365-20	8Kx8	200	60	—	28	Static/2764
	NCR 2365-25	8Kx8	250	60	—	28	Static/2764
	NCR 2365-30	8Kx8	300	60	—	28	Static/2764
	NCR 2365-45	8Kx8	450	60	—	28	Static/2764
	NCR 2365S-20	8Kx8	200	60	10	28	Static/Standby
	NCR 2365S-25	8Kx8	250	60	10	28	Static/Standby
	NCR 2365S-30	8Kx8	300	60	10	28	Static/Standby
	NCR 2365S-45	8Kx8	450	60	10	28	Static/Standby
128K ROM	NCR 23128-15†	16Kx8	150	75	—	28	Static/27128
	NCR 23128-20	16Kx8	200	75	—	28	Static/27128
	NCR 23128-25	16Kx8	250	75	—	28	Static/27128
	NCR 23128-30	16Kx8	300	75	—	28	Static/27128
	NCR 23128-45	16Kx8	450	75	—	28	Static/27128
	NCR 23128S-15†	16Kx8	150	75	10	28	Static/Standby
	NCR 23128S-20	16Kx8	200	75	10	28	Static/Standby
	NCR 23128S-25	16Kx8	250	75	10	28	Static/Standby
	NCR 23128S-30	16Kx8	300	75	10	28	Static/Standby
	NCR 23128S-45	16Kx8	450	75	10	28	Static/Standby
	NCR 23128A-30*	Four 4Kx8 Banks	300	110	—	24	Static/Bank Select
	NCR 23128A-45*	Four 4Kx8 Banks	450	110	—	24	Static/Bank Select

*Licensed under U.S. Patent Number 4368515

† Product available 3Q85

NMOS Read Only Memory Family (Continued)

Function	Part Number	Organization	Access Time Max (ns)	Supply current Max (mA)		No. of Pins	Characteristics
				Operating	Standby		
256K ROM	NCR 23256-15†	32Kx8	150	75	—	28	Static/27256
	NCR 23256-20	32Kx8	200	75	—	28	Static/27256
	NCR 23256-25	32Kx8	250	75	—	28	Static/27256
	NCR 23256-30	32Kx8	300	75	—	28	Static/27256
	NCR 23256-45	32Kx8	450	75	—	28	Static/27256
	NCR 23256S-15†	32Kx8	150	75	10	28	Static/Standby
	NCR 23256S-20	32Kx8	200	75	10	28	Static/Standby
	NCR 23256S-25	32Kx8	250	75	10	28	Static/Standby
	NCR 23256S-30	32Kx8	300	75	10	28	Static/Standby
	NCR 23256S-45	32Kx8	450	75	10	28	Static/Standby
	NCR 23257-15†	32Kx8	150	75	—	28	Static/Alt. Pin Out
	NCR 23257-20	32Kx8	200	75	—	28	Static/Alt. Pin Out
	NCR 23257-25	32Kx8	250	75	—	28	Static/Alt. Pin Out
	NCR 23257-30	32Kx8	300	75	—	28	Static/Alt. Pin Out
	NCR 23257-45	32Kx8	450	75	—	28	Static/Alt. Pin Out
	NCR 23257S-15†	32Kx8	150	75	10	28	Static/Standby
	NCR 23257S-20	32Kx8	200	75	10	28	Static/Standby
	NCR 23257S-25	32Kx8	250	75	10	28	Static/Standby
	NCR 23257S-30	32Kx8	300	75	10	28	Static/Standby
	NCR 23257S-45	32Kx8	450	75	10	28	Static/Standby

Commercial Operating Temperature of 0°C to 70°C is standard for all NCR NMOS ROMs.
Industrial Operating Temperature of –40°C to 85°C is also available.

CMOS Read Only Memory Family

Function	Part Number	Organization	Access Time Max (ns)	Supply current Max (mA)		No. of Pins	Characteristics
				Operating	Standby		
64K ROM	NCR 23C64-15	8Kx8	150	25	0.01	24	Static/2564
	NCR 23C64-20	8Kx8	200	25	0.01	24	Static/2564
	NCR 23C64-25	8Kx8	250	25	0.01	24	Static/2564
	NCR 23C65-15	8Kx8	150	25	0.01	28	Static/2764
	NCR 23C65-20	8Kx8	200	25	0.01	28	Static/2764
	NCR 23C65-25	8Kx8	250	25	0.01	28	Static/2764
128K ROM	NCR 23C128-15	16Kx8	150	35	0.04	28	Static/27128
	NCR 23C128-20	16Kx8	200	35	0.04	28	Static/27128
	NCR 23C128-25	16Kx8	250	35	0.04	28	Static/27128
256K ROM	NCR 23C256-15	32Kx8	150	35	0.04	28	Static/27256
	NCR 23C256-20	32Kx8	200	35	0.04	28	Static/27256
	NCR 23C256-25	32Kx8	250	35	0.04	28	Static/27256
512K ROM	NCR 23C512-15†	64Kx8	150	40	0.04	28	Static/27512
	NCR 23C512-20	64Kx8	200	40	0.04	28	Static/27512
	NCR 23C512-25	64Kx8	250	40	0.04	28	Static/27512
1024K ROM	NCR 23C1000-25†	128Kx8	250	50	0.1	28	Static

†Product available 3Q85
Commercial operating temperature of 0°C to 70°C is standard for all NCR CMOS ROMs.

Non-Volatile RAM

Non-volatile RAM (NVRAM) circuits combine high performance static RAM with electrically erasable PROM on a single integrated circuit. The primary advantage NVRAMs offer the system designer is its ease of interfacing with a microprocessor without affecting system performance. This is possible because an NVRAM looks and performs like a static RAM during normal operation. During a system power failure the entire contents of the static RAM can be stored in the EEPROM array and are available for recall when system power returns to normal levels. NCR NVRAMs are offered in commercial, industrial, and military temperature ranges.

Non-Volatile RAM

Function	Part Number	Organization	Access Time Max (ns)	Power Supply (Volts)	No. of Pins	Operating Range (°C)
256 Bit NVRAM	NCR 52210	64x4	300	+5	18	0 to +70
	NCR 52210 I	64x4	300	+5	18	−40 to +85
	NCR 52210 HR	64x4	450	+5	18	−55 to +125
512 Bit NVRAM	NCR 52211	128x4	300	+5	18	0 to +70
	NCR 52211 I	128x4	300	+5	18	−40 to +85
	NCR 52211 HR	128x4	450	+5	18	−55 to +125
1K NVRAM	NCR 52212	256x4	300	+5	18	0 to +70
	NCR 52212 I	256x4	300	+5	18	−40 to +85
	NCR 52212 HR	256x4	450	+5	18	−55 to +125
1K NVRAM	NCR 52001	128x8	250	+5	24	0 to +70
	NCR 52001 I	128x8	300	+5	24	−40 to +85
	NCR 52001 HR	128x8	350	+5	24	−55 to +125
2K NVRAM	NCR 52002	256x8	250	+5	24	0 to +70
	NCR 52002 I	256x8	300	+5	24	−40 to +85
	NCR 52002 HR	256x8	350	+5	24	−55 to +125
4K NVRAM	NCR 52004	512x8	250	+5	24/28	0 to +70
	NCR 52004 I	512x8	300	+5	24/28	−40 to +85
	NCR 52004 HR	512x8	350	+5	24/28	−55 to +125

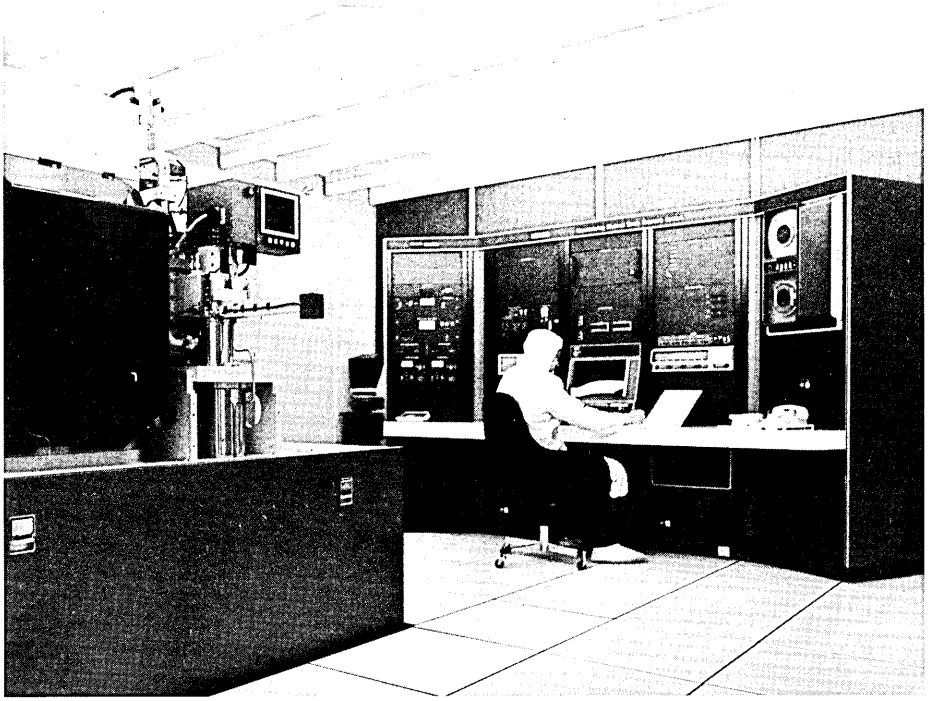
Electrically Erasable PROM

The NCR family of EEPROMs includes small organization serial devices for applications requiring a limited amount of storage capability. The NCR family also includes high density by eight devices for applications requiring maximum data storage. All members of the NCR EEPROM family are 5 volt only devices with all erase/write voltages being generated on chip. This combination of high density and 5 volt only operation places NCR in the leadership position in EEPROMs. NCR EEPROMs are offered in commercial, industrial, and military temperature ranges.

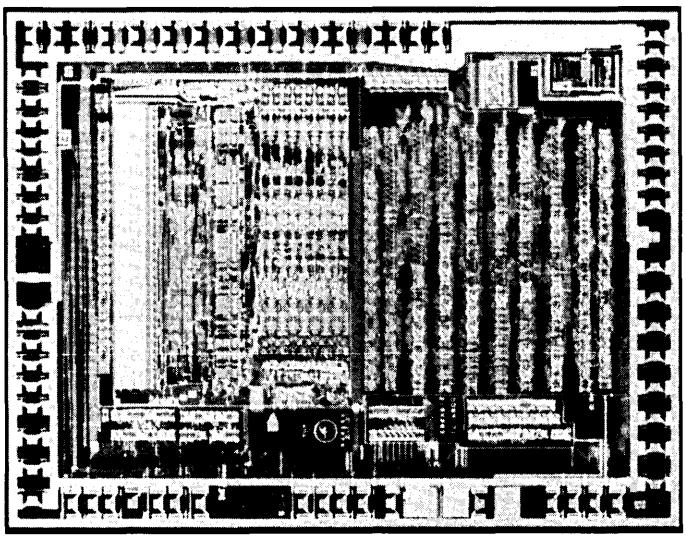
Electrically Erasable PROM

Function	Part Number	Organization	Access Time Max	Power Supply (Volts)	Operating Range (°C)	No. of Pins	Characteristics
256 Bit EEPROM	NCR 52801	16x16	125 kHz	+5	0 to +70	14	Serial
	NCR 52801 I	16x16	125 kHz	+5	−40 to +85	14	Serial
	NCR 59306	16x16	250 kHz	+5	0 to +70	8	Serial
	NCR 59306 I	16x16	250 kHz	+5	−40 to +85	8	Serial
1K EEPROM	NCR 59308	64x16	500 kHz	+5	0 to +70	8	Serial
	NCR 59308 I	64x16	500 kHz	+5	−40 to +85	8	Serial
32K EEPROM	NCR 52832	4Kx8	300 ns	+5	0 to +70	28/32*	Parallel
	NCR 52832 I	4Kx8	450 ns	+5	−40 to +85	28/32*	Parallel
	NCR 52832 HR	4Kx8	450 ns	+5	−55 to +125	28/32*	Parallel
64K EEPROM	NCR 52864 HR	8Kx8	300/450 ns	+5	−55 to +125	28/32*	Parallel

*28 Pin DIP or 32 Pin LCC



NCR Semicustom Design



Standard Cell Microcomputer with Core Microprocessor, Sound Generator, I/O and Random Cell Logic.

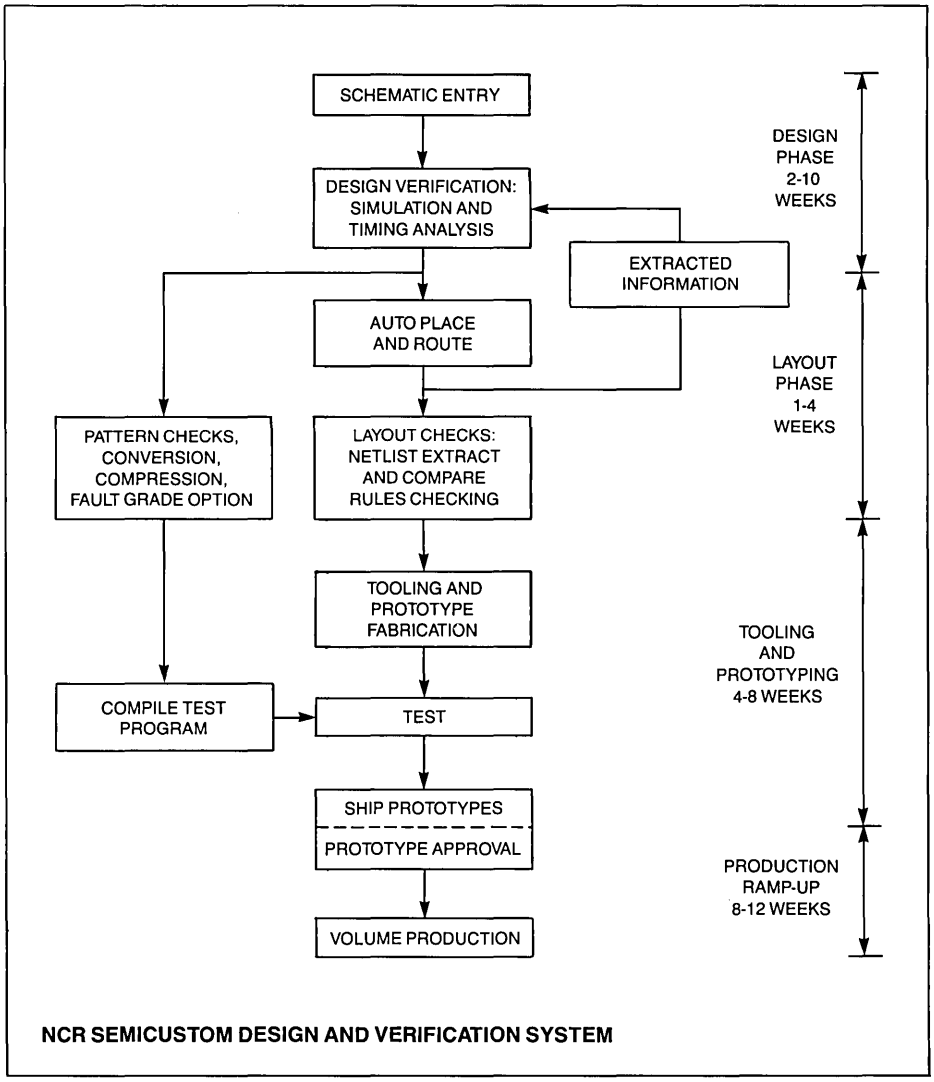
NCR Semicustom Design offers you the same high performance, design flexibility and breadth of functions as a fully-customized integrated circuit, while simultaneously minimizing development time and cost. Key elements of the NCR system include computer-aided design (CAD) tools, advanced process technologies, total technical support and a wide selection of cell functions in a state-of-the-art CMOS standard cell library.

You can take the lead in design and development with NCR technical expertise and foundry facilities to aid you in finding and implementing the optimal solution to your needs. Every phase of the design and development process is followed up with the NCR state-of-the-art support system, permitting more freedom and security to explore alternatives at minimal cost.

- Performance—propagation delays less than LSTTL and HCMOS technologies
- Advanced process technology—low power CMOS
- Directly TTL and HCMOS Compatible—no interface or pull-ups required
- Sophisticated CAD System—minimizes risk while easing and speeding design providing a first pass working part
- Optional ROM, Static RAM, and PLA — Customer definable in size and organization, with the option of analog and a core microprocessor on the same chip
- Silicon Efficient—no fixed-routing channels or cell locations. NCR Semicustom Design allows close packing of high-level functions for minimum die size and lowest overall cost of any semicustom solution
- Many 7400/5400 equivalent functions
- Versatile in-house assembly capability for plastic and ceramic dual-in-line and chip carrier package types

Cost

Compared to discrete logic, the use of an NCR cell library device to integrate system logic greatly reduces system power requirements, board space, component cost, manufacturing cost, weight, and overhead costs such as rework, inventory and purchasing. Reliability and performance will also be improved. All these factors directly impact unit pricing, particularly in volume production, making a cell library device a mandatory design choice.



NCR SEMICUSTOM DESIGN AND VERIFICATION SYSTEM

Design and Applications Assistance

You have the option of using one of the Semicustom Design Centers for design services and support, or you may prefer to purchase a workstation and design your device in your facility. In either case, NCR will provide full engineering support.

Options include:

- completing design verification in your facility
- designing the device at the NCR facility or an NCR Design Center
- permitting NCR or an NCR Design Center to perform design verification and provide a device which meets your logic specifications

CAD Tools

Semicustom design and development are done with the most sophisticated tools available. NCR is committed to retaining the position of industry leader in technology, applications support and service. To meet this commitment, NCR has acquired and/or developed the best CAD tools that the industry can offer.

Engineering Workstation Support

NCR is a leader in the support of the most popular and powerful engineering workstations. Presently, you have your choice of the Daisy™ or Mentor Graphics™ Workstations, and in 1985 the Valid™ Workstation. All of these workstations have powerful user-friendly software which is well suited to the design of semicustom integrated circuits as well as for other applications. NCR has ported its proprietary software, such as VITA™, to these workstations and interfaced to the resident software. This means that you can perform total design capture and verification on the workstation without the need for any resimulations by NCR. In addition, NCR has developed documentation specific to each workstation to guide you in the use of the NCR Semicustom Design and Verification System™ with the commands and procedures specific to that workstation. NCR Design Centers and applications engineers are available full-time to assist you in every phase of design and development, including hands-on training on a workstation. NCR is actively involved with engineering workstation industry leaders to continue the evolution of design capabilities and tools.

Timing Analysis

For timing analysis, NCR has developed the VITA™ (VLSI Timing and Interconnect Analysis) package of programs. NODE DELAY and PATH DELAY feature user prompts and keep track of signal names for ease of use. PLUG DELAY provides feedback to logic simulators for "realtime" simulations. These programs can be run both before layout, using estimated interconnect capacitances, and after layout, using extracted interconnect RC values, and rise/fall effects on cell delays.

For analog simulations, NCR will provide SPICE models for the cells, and full characterization data sheets.

Layout

Layout, using NCR enhancements to industry standard auto-place-and-route (APR) programs, has become a streamlined activity producing excellent results. Customers have the option of having NCR perform the layout from a provided netlist and specifications, or by obtaining an industry standard APR for in-house use. NCR is also cooperating with industry efforts to develop APR capability on engineering workstations.

Test Program Generation

NCR developed the SENTPEX™ (Sentry Test Pattern Extractor) package of programs. This software checks simulations of workstations or TEGAS™ V for compatibility with industry standard IC testers, converts them to tester format and compresses the patterns. The results are combined with DC parameters and compiled to generate the test programs used in prototype testing and production testing of the device.

CAD Software Tools

- Schematic entry and check
- Netlist extraction
- Logic simulation—TEGAS™ V and/or workstation-based simulation, to verify functionality and provide vectors for testing the device
- Timing Analysis—The VITA™ (VLSI Interconnect and Timing Analysis) package uses both estimated interconnect loading and extracted interconnect RC loading and rise/fall effects to accurately model signal delays. It calculates path delays as well as providing timing information to include in logic simulation.
- Automatic Place and Route—CPR3 and CAL-MP™ optimize placement of cells and automatically route the entire circuit, taking into account any specified critical paths.
- Layout Verification—includes comparison of the netlist extracted from the layout to the original netlist to verify accuracy and eliminate all possible layout errors, ERCs (Electrical Rule Checks) and DRCs (Design Rule Checks).
- Fault Grading—verifies test pattern quality; performed primarily with TEGAS.™
- Test Pattern Generation—SENTPEX™ package checks simulation pattern compatibility with testers, converts and compresses the patterns and compiles the test program.

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Mentor Graphics™ is a registered trademark of Mentor Graphics Corporation.
Valid™ is a registered trademark of Valid Logic Systems, Inc.

NCR Semicustom Process Technology

The NCR fine-geometry CMOS process provides excellent performance. Options include precision capacitors for analog and double level metal. NCR's CMOS is immune to most latch-up situations with protection of 90 mA at 12V. Worst case ESD (electrostatic discharge) is rated at 3.0kV. NCR's CMOS technology has proven to be a very reliable high volume process which provides circuit densities and performances which are extremely competitive in today's market.

Manufacturing

Whether your semicustom design is performed by NCR, a design house, or yourself, NCR will complete your device development, produce the masks and fabricate the wafers in-house.

Assembly

NCR's fast-turn assembly facility permits short development cycles and rapid ramp-up for initial production. In-house packaging includes plastic and ceramic DIPs and chip carriers. Off-shore packaging capabilities offer high volume economies on all packaging alternatives.

Second Source

NCR maintains an extensive second source agreement with Standard Microsystems Corporation which enables customers to activate second-sourcing at any point during the design, development or manufacturing process.

NCR CMOS II Digital Cell Library

The variety of cells offered allows for optimization of silicon area. A smaller die size means better performance and lower costs.

SSI Functions:

- Buffers and Inverters
  —drive and tristate options
- NAND and NOR
  —available with 2,3,4 inputs
- AND and OR—up to 8 inputs
- AOI, OAI, EXOR
- "Combinational" logic cells
  —for denser and faster devices
- Delay Cells
- Two-phase Clock Driver

Flip-Flops/Latches:

- Cross coupled latches
  both NOR and NAND
- Level sensitive transparent latches
  with Reset
  without Reset
  with clock driver
- Edge triggered D Flip-flops
  with Reset
  with Set and Reset
  without Set and Reset
  with clock driver, Set and Reset
- Edge triggered JK flip-flops
  with Set and Reset
  with Set, Reset and clock driver

MSI Functions:

- Single-bit cascadeable loaded shift register with serial or parallel in, and serial out, with or without clock driver
- Single-bit cascadeable, loadable, up-down counter with Reset and Enable, carry in and carry out

Input/Output Pads and Buffers

Options give optimal size in pad-limited designs. Levels are directly TTL and CMOS compatible.

- Input Cells—choice of standard TTL or variety of Schmitt trigger levels
- Output Cells—variety of drive options, open drain, pullup options
- Tristate—combination of I/O options

CMOS II Analog Cell Library

- Op Amps
- Comparators
- Analog Switch
- Bandgap Voltage References
- Oscillators
- D/A Converters
- A/D Converters
- Flash A/D Converter
- Sound Generator
- Negative Supply Generators
- Bias Generators
- Logic Level Shifter
- Power-On-Reset

CMOS II Supercell Library

- Modular ROM
- Modular RAM
- Modular PLA
- Counter/Timer
- 65CX02 Core-microprocessor

Gate Array Technology

Gate arrays are a viable option if you have a low volume design or one requiring fewer functions and therefore fewer gates. Design and development cycles are customarily shorter and less costly for gate arrays. The trade-off is in design flexibility and production costs, since a cell library device is smaller and less costly in larger production quantities.

NCR design engineers will assist you in making the most cost-effective decision to meet your needs, whether it is a cell library device or a gate array.

NCR Quality Assurance

The NCR Microelectronics goal in all design projects is to meet or exceed the customer's quality and reliability requirements by building quality in. Each of NCR's processes and products has been extensively characterized and qualified. Design Assurance Engineers have worked closely with Standard Cell Designers and Computer-Aided Design Software Engineers to help assure first pass design success for all customers using Standard Cells. Each cell has been fully characterized and subjected to the same rigorous reliability testing used to qualify the process itself. In addition to the initial qualification, the Quality Assurance Department samples parts from each product and performs on-going reliability testing to maintain a high level of confidence in fabrication and assembly operations. Each part receives full functional testing and visual inspection prior to shipment.

As a result of exceedingly high standards and the desire to be a leader, NCR Microelectronics has one of the lowest part reject records in the industry.

Digital Signal Processing

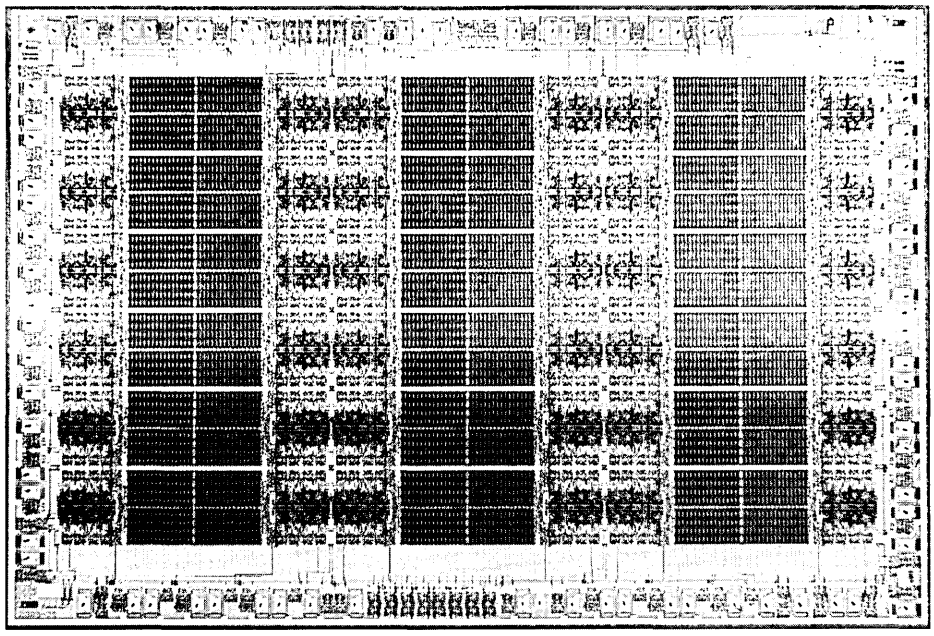
NCR now offers two DSP VLSI devices: the NCR45CG72 is the Geometric Arithmetic Parallel Processor chip (GAPP) and the NCR45CM16 is the Multiplier Accumulator chip. Both of these devices are targeted for emerging digital signal processing applications. The 45CM16 is aimed at microprocessor-based systems that perform multiply intensive tasks. Examples include process control, robotics, and electronic instruments. The GAPP is well suited for applications in which operations are repetitively applied over large arrays of data. This includes many image processing applications such as pattern recognition, automatic inspection, convolution, correlation, data compression, and machine vision.

Geometric Arithmetic Parallel Processor

FEATURES

- 6 x 12 systolic array of processors in CMOS VLSI
- Highly parallel architecture
- Nearest neighbor communication between processors
- GAPP devices fully cascadeable
- Overlapped I/O and computation
- On-chip 128-Bit SRAM per processor

The GAPP is a revolutionary architecture that is comprised of 72 individual processors elements arranged in a 6 x 12, two-dimensional array. Each of the processors operates in parallel with each processor being able to manipulate different data. The massive parallelism inherent in the chip's architecture provides the processing power of 72 processors on a single piece of silicon.



Geometric Arithmetic Parallel Processor (GAPP)

Within each processor is a bit-serial ALU, 128 bits of RAM, and four single-bit latches. Three of these latches hold inputs to the ALU and the fourth latch allows I/O operations to be performed without interrupting the program execution. Thus, I/O operations can be overlapped with computation. Each of these processors is able to communicate and exchange data with its four immediate neighbors: one to the East, West, North, and South.

GAPP chips are cascadeable and allow system designers to implement processor arrays of arbitrary size in multiples of 6 x 12 elements. For instance, two GAPP chips can be configured to form a 12 x 12 processor array, eight chips can be used to form a 24 x 24 array of processors, and so on. The advantage of cascading arrays of GAPP chips in systems is that system throughput increases linearly with the number of chips used in the system. Thus, a system of two GAPP chips offers twice the processing throughput of a single GAPP chip, while a system of eight chips offers eight times the processing throughput of a single GAPP chip and four times the processing throughput of a two GAPP chip system. This ability to trade off performance versus chip count offers the system designer virtually unlimited freedom in designing systems around the GAPP to meet specific performance needs. In addition, software compatibility can be maintained as system designers expand their systems by adding more GAPP chips to increase system performance.

The GAPP architecture is typically described by such terms as "systolic array," or SIMD (Single Instruction, Multiple Data). Regardless of how one describes it, the GAPP is an undeniable departure from the traditional vonNeumann architecture which processes data utilizing a single data element. The vonNeumann architecture, for example, depends upon component technology to attain processing throughput. The GAPP, on the other hand, exploits parallelism rather than relying on component speed to achieve its throughput. Hence, the GAPP is able to achieve throughput rates unattainable by vonNeumann architectures.

GAPP Development System

To support software development, there is a GAPP Evaluation Module which consists of a software development package and hardware accelerator board for IBM compatible personal computers. Development software for the Evaluation Module includes the GAPP Algorithm Language compiler, and a program debugger which allows single and multiple step execution. In addition, the programmer is able to examine and change internal registers and RAM locations in each processor element.

Also available is a GAPP Simulator/Assembler which allows the programmer to simulate GAPP programs on processor arrays of arbitrary size. The Simulator/Assembler allows the user to write and debug programs in GAPP micro-code, and examine internal registers and RAM locations.

16 x 16 Single Port Multiplier/Accumulator Chip

FEATURES

- 24-pin ceramic or plastic DIP
- 40-bit accumulator
- 190ns cycle time (typ)
- Fully static operation—no clock required
- Single port allows easy interfaces to microprocessor bus

The NCR45CM16 is a 24-pin CMOS multiplier/accumulator chip for use with 16-bit microprocessor systems. All input and output data are transferred through a single 16-bit bidirectional data bus in signed two's complement format. This device is TTL/CMOS compatible and requires no clock due to its totally static (asynchronous) operation. The 45CM16 may be attached to a microprocessor bus in a way similar to a 16-bit wide static RAM.

The single port design of the 45CM16 makes it much more compact than three port devices. Another comparative advantage of the 45CM16 relative to three port multiply/accumulate chips is that there is no need to use a lot of glue logic to interface it to the microprocessor bus. Static operation frees the system designer from having to generate clock signals to control the device. These three attributes: small package, ease of interface to microprocessor bus, and static operation mean that boards designed with the 45CM16 will be more compact and easier to design.

An 8086 or 68000 using the 45CM16 can realize a 3X enhancement in overall multiplication speed compared with performing the multiplication operation in software using the 68000 instruction set. The 40-bit accumulator allows 32-bit partial products to be accumulated up to 256 times before the contents of the accumulator must be read.

NCR/32
Processor Family

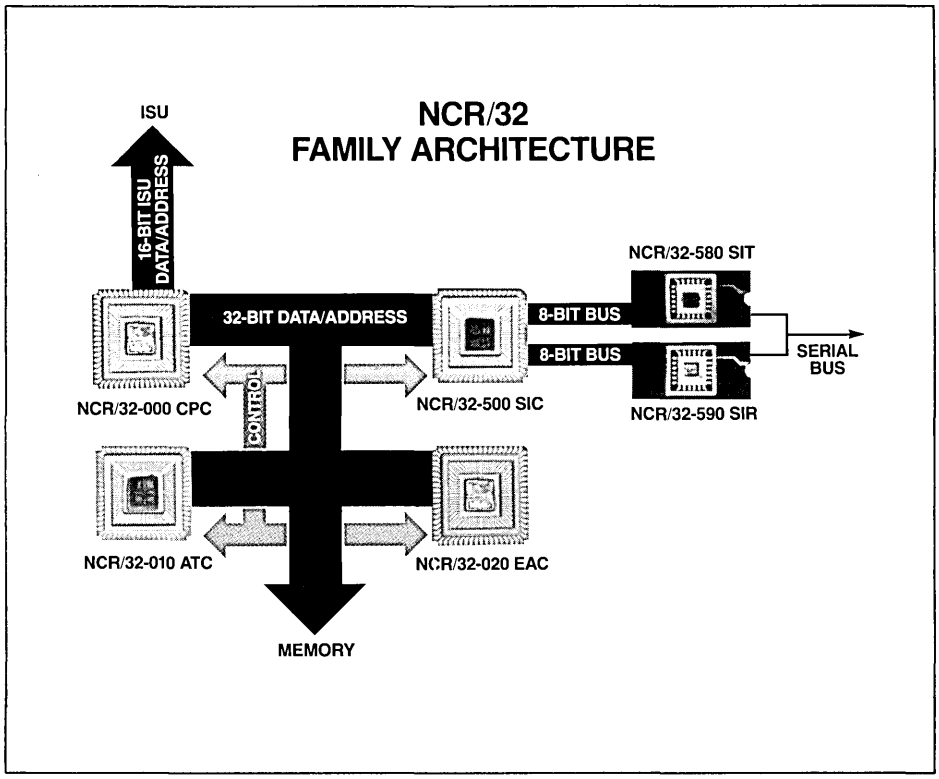
Features

- 32-bit system architecture
- 13.3 Megahertz frequency
- Effective emulation of mid-range mainframes
- Externally microprogrammable
- Real and virtual memory operation
- Large direct memory addressing
- Interface provided to slower peripherals
- On-chip error check and correction

Functional Description

The NCR/32 VLSI Processor family combines the latest advances in semiconductor technology with experience gained in three generations of computer mainframe design to provide a comprehensive microprogrammable 32-bit system architecture. With external microprogram capability, an extremely flexible microinstruction set, and a powerful set of internal registers, the NCR/32 offers flexibility and high performance advantages not available with other microprocessors.

Along with an existing set of VLSI family support devices, the NCR/32 offers effective emulation of register, stack and descriptor-based system architectures, as well as execution of high-level languages directly from microcode. The NCR/32 is well suited for applications requiring direct addressing of a large memory space, high numeric precision, and very-high-speed execution such as bit-mapped graphics, robotics, artificial intelligence, and relational data bases.



The NCR/32 VLSI Processor family consists of the Central Processor Chip (CPC), the Address Translation Chip (ATC), and the System Interface Controller (SIC). Additional members of the family include the Extended Arithmetic Chip (EAC), the System Interface Transmitter (SIT) and Receiver (SIR) chips, and the Bus Assist Chip (BAC).

The CPC performs the basic microprocessing function using four 32-bit internal data paths, complemented by two independent external data paths: the 32-bit Processor Memory (PM) Bus and the 16-bit Instruction Storage Unit (ISU) Bus. An integral part of the CPC is the Arithmetic Logic Unit (ALU) which is used for performing decimal and binary arithmetic functions and logical operations. There are two sets of registers in the CPC. The Register Storage Unit consists of 16, 32-bit registers used for storage and manipulation of data; the additional 22 registers of the Internal Register Unit are used as jump address registers and operand pointer registers. A three-stage pipeline insures that one microinstruction is being fetched, another read, and a third executed in the same time frame.

The system clock is a two-phase, non-overlapping clock operating at 13.3MHz. This yields a 150 nanosecond clock cycle with 90% of the microinstructions executing in one cycle.

The ATC provides memory management functions using either virtual or real memory addressing. To support virtual memory operations in the NCR/32 chipset, an extra PM bus cycle precedes the standard memory access. Two 32-bit registers, the TOD Register/Counter and the Interval Timer Monitor Register, are used for time interval monitoring. An NCR-patented "scrubbing" technique checks, and corrects if necessary, a 64K word block of memory every 1.048 seconds. The ATC has three virtual address page sizes: 1K, 2K, and 4K bytes.

The EAC is a performance booster used during arithmetic operations. Fixed point, decimal, and hexadecimal floating point formats are all handled by the EAC. (Hexadecimal floating point format is compatible with the IBM/370.) Results are in either single (one word) or double (two words) precision. Conversion operations between formats are also handled.

The SIC performs communication management between the NCR/32 chipset and the I/O devices. Used with the SIT and SIR (which perform data format conversions) the SIC sends and receives messages at up to 24 megabits per second per channel. The SIC/SIT/SIR communications subsystem operates in either Data Link Control mode or Local Area Network mode. In the Data Link Control mode, the SIC has access to eight transmission channels through a polling scheme. This mode is designed to control multiple peripheral devices on a system. The Local Area Network mode is designed for high-speed transmissions in a network environment, using two different channels of access.

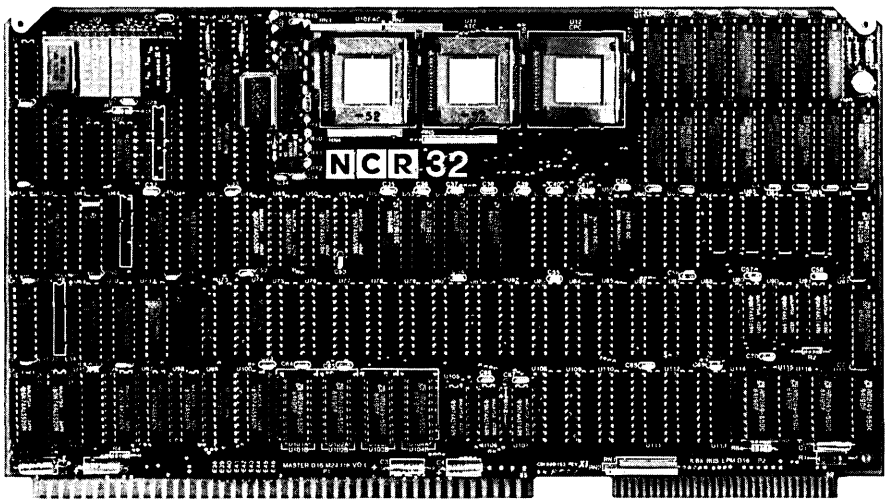
The NCR/32 Development System is available to help in evaluating the NCR/32 chipset and in developing microcode for particular system applications. A complete development system consists of two NCR components, the NCR/32-796A Board and the NCR/32 Debug Monitor along with the following:

- An IBM-compatible PC
- A relocatable, linkable assembler
- A Multibus™ development environment, including:
  —a chassis
  —an adapter kit consisting of a Multibus board and a PC board
  —a memory board

In addition, experienced NCR applications engineers can assist in determining the suitability of the NCR/32 family for solving applications problems. These engineers can provide extensive training on the NCR/32 systems architecture, individual chips, and the use of design support tools.

*Multibus is a registered trademark of Intel Corp.

NCR/32-796A Board



Board Highlights

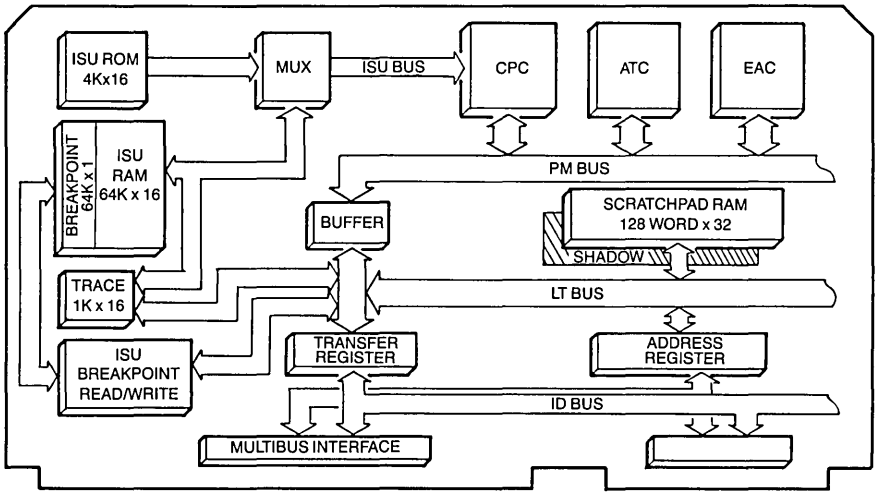
- Dual port main memory access capability using either Multibus or iLBX*
- Full 32-bit VLSI Chip Set
  —Central Processor Chip (CPC)
  — Address Translation Chip (ATC)
  — Extended Arithmetic Chip (EAC)
- 150ns instruction/PM bus cycles
- Real and virtual memory operations
- On-board breakpoint and movable window trace capability
- 4K words of ROM containing diagnostics and debug routines
- 16K words of on-board RAM for user-defined microcode

The NCR/32-796A board, featuring the NCR/32 Chip Set, provides new opportunities for microcode generation at the microprocessor level. The board provides an alternate iLBX I/O port for high-speed memory transfers. A wide range of user applications include:

- Dedicated algorithmic processing
- File processing in intelligent networks
- Graphics co-processing
- Robotics control
- Virtual machine emulation
- High-level language acceleration
- Image recognition.

The NCR/32-796A board includes an Instruction Storage Unit (ISU) providing 16K words of storage for user microcode. Use of the Extended Arithmetic Chip (EAC) offers the following math capabilities: single and double precision fixed-point binary multiplication and division, single and double precision floating-point hexadecimal (IBM format), floating-point decimal, and format conversion.

Resident microcode-development firmware makes breakpoint and trace logic readily accessible via onboard ROM. Additional development interface and assembler software is also available.



BOARD BLOCK DIAGRAM

*Multibus and iLBX are trademarks of Intel Corporation.

Special Function Chips

SCSI

NCR 5380 SCSI Protocol Controller

Supports latest ANSI X 3T9.2 SCSI draft-proposed standard. Asynchronous data transfers to 1.5 Megabytes/sec. Operates in both initiator and target roles. Supports arbitration including reselection. Contains on-chip open collector (48 mA at .5V) bus transceivers. Requires +5V supply in a 40 pin DIP.

NCR 5385E SCSI Protocol Controller

Enhanced 5385 supports the latest ANSI X 3T9.2 SCSI Standard. Asynchronous data transfers to 1.5 Megabytes/Sec. Operates in both initiator and target roles. Supports arbitration including reselection. Uses external open collector or differential pair transceivers. Double buffered data registers, 24-bit transfer counter and automatic protocol handling provides high performance interface. Requires +5V supply in a 48 pin DIP.

NCR 5386 SCSI Protocol Controller

Replacement for NCR 5385. Updates all SCSI timings to latest ANSI specification with operational enhancements. Production June '85.

Graphics

NCR 7250 CRT Controller

On-chip character ROM with 192 characters. Addresses a 2Kx8 video RAM. Generates VSYNC, HSYNC and VIDEO to interface directly with CRT monitor. Eight screen and six field functions are under software control. Dot clocks up to 20MHz with +5V supply in a 40 pin DIP.

NCR 7300 Color Graphics Controller

Translates high level commands from host computer into video operations such as drawing and text manipulation, and provides video output to monitor. Supports a displayable screen resolution of 640x480 pixels at 60Hz, and a frame buffer of 1024x1024. Has analog RGB outputs, and pixel rates to 30 MHz. Interfaces to 8-bit or 16-bit processor. Housed in 68 pin package and uses +5V supply.

NCR 7301 Memory Interface Controller

Companion chip to NCR 7300. Multiplexes and Demultiplexes between four and sixteen bit busses. Designed for implementation of high performance graphics systems and similar applications requiring rapid data handling. Requires +5V supply in a 28 pin DIP.

Other

NCR 8301 Bar Code Processor

Decodes code 39 and interleaved 2 of 5, bidirectional decoding, velocity of 1 to 50 in/sec with 32-character tag buffer. Standalone or peripheral mode with +5V supply in a 40 Pin DIP.

NCR 8489 Sound Generator

Functionally and pin compatible with SN76489A. Three programmable tone generators. Programable white noise generator with 4 MHz (max) clock input. Requires +5V supply in a 16 pin DIP.

NCR Microprocessors

NCR 6518	8-bit Microprocessor utilizing the 6507 CPU. Contains 128x8 Static RAM, two bi-directional programmable I/O ports, programmable interval timer.
NCR 65C02	8-bit Microprocessor, software compatible with the NMOS 6502. 2 or 3 MHz operation, 64K-byte addressable memory, low power consumption 4mA @ 1 MHz.
NCR 65C21	Peripheral Interface Adapter, with two 8-bit bidirectional I/O ports, and four peripheral control/interrupt input lines.
NCR 65C22	Versatile interface adapter with internal timer/counters. Compatible with NMOS 6522. Two powerful 16-bit programmable internal timer/counters. Latched input/output registers on both I/O parts.
NCR 65CX02	Identical to 65C02 except for the addition of four bit manipulation instructions (SMB, RMB, BBS, BBR). Will operate at 2, 3, or 4 MHz.

Microcomputers

Part Number	All parts have I/O capabilities of 32 bi-directional lines, are powered by a 5V power supply, and are packaged in a 40 pin DIP.					
	Memory		Technology	Counter/Timer	Internal Frequency	Other Features
	ROM	RAM				
NCR 6500/1	2048 X 8	64 X 8	NMOS	16-bit Programmable	1,2,3 MHZ	
NCR 6500/11	3072 X 8	192 X 8	NMOS	(2) 16-bit Programmable	1 or 2 MHz	Full Duplex UART 10 Interrupts
NCR 65C00/1	2048 X 8	64 X 8	CMOS	16-bit Programmable	1,2,4 MHz	Low Power 4mA/MHz Max 1mA/MHz Typical
NCR 65C00/2	3072 X 8	64 X 8	CMOS	16-bit Programmable	1,2,4 MHz	Low Power 4mA/MHz Max 1mA/MHz Typical
NCR 65C00/3	4096 X 8	128 X 8	CMOS	16-bit Programmable	1,2,4 MHz	Low Power 4mA/MHz Max 1mA/MHz Typical

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