National Semiconductor
Memory Systems

# BLC 0512

# TECHNICAL MANUAL



National Semiconductor
Memory Systems



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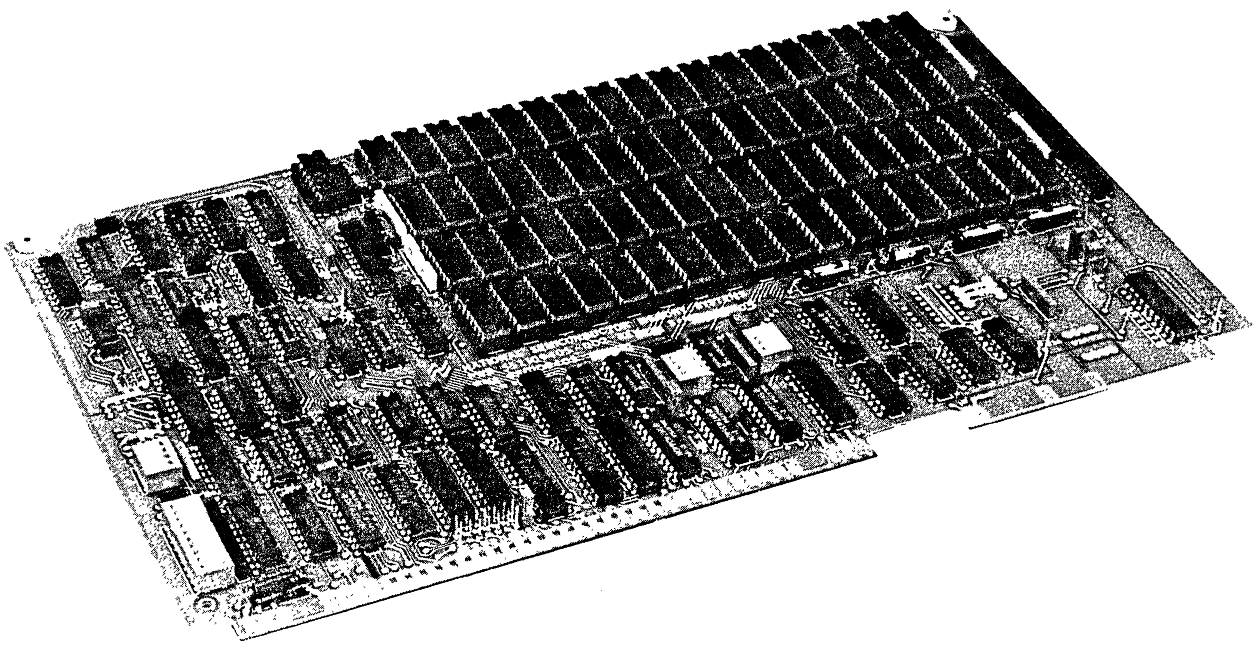
CONTENTS

## FIGURES



## TABLES



BLC 0512 PHOTOGRAPH

Chapter 1

## 1.1 INTRODUCTION

The BLC 0512 memory module is an add-in memory for computers using the Multibus or BLC series computers. It is IEEE 796 BUS compatible, compliance level D16 M24 I16 V0. The flexibility of the BLC 0512 makes it compatible with a wide variety of system configurations.

## 1.2 PHYSICAL DESCRIPTION

The BLC 0512 is contained on a single four layer PC board which plugs directly into the BLC 604 or BLC 614 modular backplanes and card cages or any backplane conforming to IEEE 796 BUS specification. It has two sets of edge connectors: one 86 pin on .156 inch centers for the system bus and a 60 pin on .100 inch centers for auxiliary power and optional bus signals. The dimensions of the PC board are:

| | |
|---|---|
| Thickness | 0.062 +/- .005 inches |
| Width | 6.750 +/- .005 inches |
| Length | 12.00 +/- .005 inches |

The maximum component height shall not exceed 0.375 inches and the maximum total thickness of the finished assembly will be less than 0.490 inches.

## 1.3 POWER REQUIREMENTS

The BLC 0512 requires only +5 vdc. Jumper points are provided to implement battery back-up.

### 1.3.1 Parameters and Conditions

The BLC 0512 requires the following voltages at the specified current:

| | Standby | | Operating | |
|---|---|---|---|---|
| Voltage | Maximum | Typical | Maximum | Typical |
| +5v+/-5% | 3.0 | 2.8 | 3.1 | 2.9 |

### 1.3.2 Battery Back-up Voltage Requirements

The battery back-up (protected) voltages must meet the following requirements:

1. +5v +/- 5% @1.5A

## 1.4 ACCESS AND CYCLE TIMES

The performance of the BLC 0512 memory card is as follows:

| Function | Access Time (maximum) | Cycle Time (maximum) | Notes |
|---|---|---|---|
| Memory Read | 275 ns | 400 ns | 1,2,3 |
| Memory Write | 110 ns | 400 ns | 1,2,3 |
| I/O Read | 90 ns | 150 ns | 2,3 |
| I/O Write | 90 ns | 150 ns | 2,3 |

Notes:

1. If a memory operation is requested during a refresh cycle, a delay of up to 500 ns can be added to access and cycle time.

2. Read access is defined as MRDC* or IORC* asserted to XACK* asserted. Write cycle access time is defined as MWTC* or IOWC* asserted to XACK* asserted

3. Cycle time is defined as command asserted to internal busy negated.

## 1.5 OPTIONS

The BLC 0512 is available with a variety of options to enhance the card.

### 1.5.1 Memory Capacity

The standard capacity of the BLC 0512 is 524,288 bytes by 9 bits (512K x 9). Optional capacities are available from a minimum of 131,072 bytes by 8 bits to a maximum of 524,288 bytes by 9 bits in increments of 131,072 by 8 or 9 bits.

### 1.5.2 Parity Generation and Check

The BLC 0512 is available with or without the parity option. This option includes parity storage, parity generation and checking and a special software addressable register for controlling the parity and interrupt functions and logging the location of parity errors. The on-board register will be referred to as the CSR (Control and Status Register). Refer to Sections 3.4 and 3.5 for details of parity operation and the CSR.

### 1.5.3 Refresh

The standard configuration of the BLC 0512 is with internally controlled, transparent refresh. The external refresh option, if selected, may be used as either synchronous or asynchronous refresh input.

### 1.5.4 Advanced Acknowledge

Advanced Acknowledge (AACK*) can be jumper selected to one of three different times to enhance system performance, or a jumper can be removed to completely isolate AACK* from the interface.

### 1.5.5 Battery Back-up

Battery or protected voltages may be supplied via the P2 connector to protect against data loss when unprotected power supplies are out of tolerance. In the battery back-up mode circuitry on the BLC 0512 that is necessary to maintain data is kept operational but external cycles may not be performed.

## 1.6 RELIABILITY

The BLC 0512 was designed and built to the best commercial standards of workmanship. Vigorous testing is conducted (including testing over the operating temperature and voltage ranges) to ensure reliable service of 10 years at 24 hours per day. To further enhance reliability, only pre-conditioned parts are used (National's A+ conditioning or equivalent).

# Chapter 2

# SPECIFICATIONS

## 2.1 INTRODUCTION

This chapter describes the operating environment and electrical specifications of the BLC 0512.

## 2.2 ENVIRONMENTAL SPECIFICATIONS

The BLC 0512 was designed to operate over a wide range of environmental conditions. Listed below are the environmental specifications:

### 2.2.1 Operating Specifications

- Temperature . . . Ambient air temperature range of $0^{\circ}C$ to $+55^{\circ}C$
- Thermal Shock . . No greater than $30^{\circ}C$ per hour.
- Humidity . . . . . 0% to 95% relative humidity without condensation.
- Altitude . . . . . -1000 feet msl to +10,000 feet msl.
- Cooling . . . . . . Suggested minimum air flow of 25 cfm.

### 2.2.2 Shipping and Storage Specifications

- Temperature . . . . $-40^{\circ}C$ to $+85^{\circ}C$.
- Thermal Shock . . . Not greaterthan $10^{\circ}C$ per minute.
- Altitude . . . . . A shipping altitude of 40,000 feet msl can be withstood.

o Mechanical Shock — The BLC 0512, housed in its shipping container, can tolerate mechanical shock resulting from drop tests performed in accordance with MIL-STD-810B, Method 516, Procedure V, without exhibiting damage or degradation.

## 2.3 ELECTRICAL SPECIFICATIONS

This section contains information regarding logic states, signal levels, bus timing and receiver/driver characteristics.

### 2.3.1 Logic States

The signal name will indicate whether or not a signal is active high or active low. If the signal name ends with an asterisk, it indicates the signal is active low and its logical-electrical relationship is as follows:

| Logical State | Electrical State |
|---|---|
| 0 | H=TTL High |
| 1 | L=TTL Low |

If the signal name has no asterisk, then it is active high and its logical-electrical relationship is as follows:

| Logical State | Electrical State |
|---|---|
| 0 | L=TTL Low |
| 1 | H=TTL High |

### 2.3.2 Driver and Receiver Characteristics

Table 2.1 lists the characteristics of the drivers and receivers used on the BLC 0512. Current levels are given in mA's.

TABLE 2.1

| Signal | Type | Drivers IOL (min) | Drivers IOH (min.) | Drivers CO (max.) | Receivers ITL (max.) | Receivers ITH (max.) | Receivers CI |
|---|---|---|---|---|---|---|---|
| DAT0*-DATF* | TRI | 24 | -15 | 300 | -.4 | 20 | 18 |
| ADR0*-ADR17* | | | | | -.4 | 20 | 18 |
| MRDC* | | | | | -.4 | 50 | 18 |
| MWTC* | | | | | -.4 | 50 | 18 |
| IORC* | | | | | -.4 | 20 | 18 |
| IOWC* | | | | | -.4 | 20 | 18 |
| XACK* | TRI | 24 | -2.6 | 300 | | | |
| AACK* | TRI | 24 | -2.6 | 300 | | | |
| INIT* | | | | | -.4 | 20 | 18 |
| INT0*-INT7* | O.C | 60 | +250 (max.) | 300 | | | |
| MPRO* | | | | | -.4 | 20 | 18 |
| INH1* | | | | | -.4 | 20 | 18 |
| M1 | | | | | -.4 | 20 | 18 |

### 2.3.3 Bus Logic Levels

Signals used on the bus that the BLC 0512 interfaces to should meet the following requirements:

| | At Receiver | At Driver |
|---|---|---|
| Voltage High | 5.25v>H>2.0v | 5.25>H>2.4v |
| Voltage Low | .8v>L>-.5v | .5v>L>0v |

### 2.3.4 Bus Timing

Figures 2.1 thru 2.4 are the timing diagrams that pertain to the BLC 0512. Table 2.2 lists the parameter values.

```
               |<--------tCMD---------->|
               |                        |
               |                        |
--------------\|                        |/-----------------
MRDC*          |\______________________/|
          |    |                        |     |
          |<-->|---tAS                  |<--->|---tAH
          |    |                        |     |
ADDRESS--\|/-----------------------------------\|/----------
LINES____/ \___________________________________/ \__________
          |                    |        |       |
          |<--------tXACK----->|        |<----tXAH---->|
          |                    |        |       |
XACK*------------------------------\    |              |/---
          |                         \___|______________/|
          |                         |   |              |
          |                         |   |<----tDHR---->|
          |           |<---tDXL--->|    |              |
          |                         |   |              |
DATA-----------------\|/-------------------------------\|/---
LINES________________/|\_______________________________/ \___
```

Figure 2.1  Memory Read Timing

```
               |<--------tCMD---------->|
               |                        |
               |                        |
--------------\|                        |/--------------
MWTC*          |\______________________/|
          |    |                        |     |
          |<tAS>|                       |<--->| tAH
          |    |                        |     |
ADDRESS--\|/-----------------------------------\|/--------
LINES____/ \___________________________________/ \________
               |           |            |         |
               |           |            |         |
               |<---tXACK--->|          |<--tXAH--> |
               |           |            |         |
XACK* ---------|-----------\|           |         /-----
               |            \___________|_________/
        |      |                        |       |
        |<-tDS->|                       |<--tDH-->|
        |      |                        |       |
DATA---\|/--------------------------------------\|/-------
LINES__/ \______________________________________/ \_______
```

Figure 2.2  Memory Write Timing

```
                |<--------tCMD--------->|
                |                       |
                |                       |
IORC*----------\|                       |/-----------------
                |\_____________________/|
          |     |                       |      |
          |<tAS>|                       |<---->| tAH
          |     |                       |      |
ADDRESS--\|/----------------------------------\|/-----------
LINES____/ \__________________________________/ \___________
                |                       |          |
                |                       |          |
                |<-----tXACK----->|     |<--tXAH-->|
                |                 |     |          |
XACK*----------------------------\|     |          |/------
                                  |\____|_________/|
                            |     |     |
                        tDXL|<--->|     |<-----tDHR---->
                            |     |     |              |
DATA-----------------------\|/------------------------\|/--
LINES______________________/ \________________________/ \__
```

Figure 2.3 I/O Read Timing

```
                |<--------tCMD--------->|
                |                       |
                |                       |
IOWC*----------\|                       |/------------------
                |\_____________________/|
          |     |                       |         |
          |<tAS>|                       |<--tAH-->|
          |     |                       |         |
ADDRESS--\|/-------------------------------------\|/---------
LINES____/ \_____________________________________/ \_________
                |            |          |             |
                |            |          |             |
                |<--tXACK--> |          |<--tXAH-->   |
                |            |          |             |
XACK* ----------|-----------\|          |             /------
        |       |             \_________|____________/
        |       |                       |         |
        |<-tDS->|                       |<--tDH-->|
        |       |                       |         |
DATA---\|/---------------------------------------\|/---------
LINES__/ \_______________________________________/ \_________
```

Figure 2.4 I/O Write Timing

Table 2.2 Timing Parameters

| PARAMETER | MIN | MAX |
|---|---|---|
| tCMD | 100 ns. | DC |
| tAS | 50 ns. | |
| tAH | 50 ns. | |
| tDS | 50 ns. | |
| tDH | 50 ns. | |
| tXACK | 0 ns. | |
| tXAH | 0 ns | 65 ns. |
| tDXL | 0 ns. | |
| tDHR | | 65 ns. |

## Chapter 3

## THEORY OF OPERATION

### 3.1 INTRODUCTION

This section contains a description of the interface of the BLC 0512. Signals used on the Multibus which are not used on this card are not mentioned. Tables 3.1 and 3.2 are pin listings of the BLC 0512 card edge connectors.

### 3.2 INTERFACE

The following describes the interface of the BLC 0512. It is IEEE 796 compatible and Multibus compatible with the ability to add via jumpers other bus signals which are not standard but will not affect the operation of the bus. The signals at the interface will be divided into four basic groups: Address, Data, Control, and Non-standard.*

* Non-standard refers to all signals not specified in IEEE specification 796 "Proposed Microcomputer System Bus Standard", Oct. 1980.

Table 3.1

Pin Assignment Connector P1

| | (Component Side) | | | Circuit Side | | |
|---|---|---|---|---|---|---|
| | Pin | Mnemo-nic | Description | Pin | Mnemo-nic | Description |
| Power Sup-plies | 1 | GND | Signal GND | 2 | GND | Signal GND |
| | 3 | +5V | +5Vdc | 4 | +5V | +5Vdc |
| | 5 | +5V | +5Vdc | 6 | +5V | +5Vdc |
| | 7 | | | 8 | | |
| | 9 | | | 10 | | |
| | 11 | GND | Signal GND | 12 | GND | Signal GND |
| Bus Con-trol | 13 | | | 14 | INIT* | Initialize |
| | 15 | BPRN* | Bus Pri. In | 16 | BPRO* | Bus Pri. Out |
| | 17 | | | 18 | | |
| | 19 | MRDC* | Mem Read Cmd | 20 | MWTC* | Mem Write Cmd. |
| | 21 | IORC* | IO Read Cmd | 22 | IOWC* | IO Write Cmd. |
| | 23 | XACK* | XFER Ack-nowledge | 24 | INH1* | Inhibit 1 (disable RAM) |
| Bus Con-trol and Ad-dress | 25 | | | 26 | | |
| | 27 | BHEN | Byte High Enable | 28 | AD10* | |
| | 29 | | | 30 | AD11* | Address Bus |
| | 31 | | | 32 | AD12* | |
| | 33 | | | 34 | AD13* | |
| Inter-rupts | 35 | INT6* | Parallel Interrupt Requests | 36 | INT7* | Parallel Interrupt Requests |
| | 37 | INT4* | | 38 | INT5* | |
| | 39 | INT2* | | 40 | INT3* | |
| | 41 | INT0* | | 42 | INT1* | |

Table 3.1 (Cont.)

| | (Component Side) | | | Circuit Side | | |
|---|---|---|---|---|---|---|
| | Pin | Mnemonic | Description | Pin | Mnemonic | Description |
| Address | 43 | ADRE* | | 44 | ADRF* | |
| | 45 | ADRC* | | 46 | ADRD* | |
| | 47 | ADRA* | Address | 48 | ADRB* | Address |
| | 49 | ADR8* | Bus | 50 | ADR9* | Bus |
| | 51 | ADR6* | | 52 | ADR7* | |
| | 53 | ADR4* | | 54 | ADR5* | |
| | 55 | ADR2* | | 56 | ADR3* | |
| | 57 | ADR0* | | 58 | ADR1* | |
| Data | 59 | DATE* | | 60 | DATF* | |
| | 61 | DATC* | | 62 | DATD* | |
| | 63 | DATA* | Data | 64 | DATB* | Data |
| | 65 | DAT8* | Bus | 66 | DAT9* | Bus |
| | 67 | DAT6* | | 68 | DAT7* | |
| | 69 | DAT4* | | 70 | DAT5* | |
| | 71 | DAT2* | | 72 | DAT3* | |
| | 73 | DAT0* | | 74 | DAT1* | |
| Power Supplies | 75 | GND | Signal GND | 76 | GND | Signal GND |
| | 77 | | | 78 | | |
| | 79 | | | 80 | | |
| | 81 | +5V | +5Vdc | 82 | +5V | +5Vdc |
| | 83 | +5V | +5Vdc | 84 | +5V | +5Vdc |
| | 85 | GND | Signal GND | 86 | GND | Signal GND |

Table 3.2

Connector Pin Assignments

| Pin | (Component Side) Mnemonic | | Pin | Mnemonic | Circuit Side Description |
|---|---|---|---|---|---|
| 1 | GND | Signal Ground | 2 | | |
| 3 | +5VB | +5Vdc battery | 4 | +5VB | +5Vdc battery |
| 5 | | | 6 | | |
| 7 | | | 8 | | |
| 9 | | | 10 | | |
| 11 | | | 12 | | |
| 13 | | | 14 | | |
| 15 | | | 16 | | |
| 17 | | | 18 | | |
| 19 | | | 20 | MPRO* | Memory Protect |
| 21 | | | 22 | | |
| 23 | | | 24 | | |
| 25 | | | 26 | | |
| 27 | | | 28 | | |
| 29 | | | 30 | | |
| 31 | EX REF | External Refresh | 32 | | |
| 33 | | | 34 | | |
| 35 | | | 36 | | |
| 37 | | | 38 | | |
| 39 | | | 40 | | |
| 41 | | | 42 | | |
| 43 | | | 44 | | |
| 45 | | | 46 | | |
| 47 | | | 48 | | |
| 49 | | | 50 | | |
| 51 | | | 52 | | |
| 53 | | | 54 | | |
| 55 | ADR16* | Address Bus | 56 | ADR17* | Address Bus |
| 57 | ADR14* | | 58 | ADR15* | |
| 59 | | | 60 | | |

### 3.2.1 Address and Inhibit Lines

The address and inhibit lines are comprised of the following signals:

| | |
|---|---|
| Address | ADR0* thru ADR17* |
| Byte High Enable | BHEN* |
| Inhibit | INH1* |

#### 3.2.1.1 Address (ADR0* - ADR17*)

These 24 lines are used to specify a memory location out of 16 megabytes if all 24 lines are used or 1 megabyte if 20 lines are used. Either 8 or 16 of these lines are used to specify an I/O address that will enable access to the onboard CSR (Port address).

#### 3.2.1.2 Byte High Enable (BHEN*)

BHEN*, when asserted enables the upper byte (8-F) onto the data bus.

#### 3.2.1.3 Inhibit 1 (INH1*)

When INH1* is asserted no later than 50 nanoseconds after MRDC* or MWTC*, the memory will be disabled from driving any signals active on the bus and will be inhibited from performing any write cycles.

### 3.2.2 Data Lines

The data lines are comprised of the following signals:

| | |
|---|---|
| Data | DAT0* - DATF* |

These 16 lines provide data to the memory during a write and are driven by the memory during a memory read. If BHEN* is not asserted, the lower 8 lines are used (DAT0* - DAT7*) to do byte transfers only. If BHEN* is asserted, and ADR0* is not asserted, all 16 data lines are used. If both BHEN* and ADR0* are asserted, only the upper 8 bits (DAT8*-DATF*) are used. Table 3.3 shows the different data transfer modes.

Table 3.3

DATA TRANSFER MODES

| BHEN* | ADR0* | FUNCTION |
|---|---|---|
| 0 | 0 | Transfer lower (even) byte on DAT0*-DAT7* |
| 0 | 1 | Transfer high (odd) byte on DAT0*-DAT7* |
| 1 | 0 | Transfer 16 bit word on DAT0-DATF* |
| 1 | 1 | Transfer high (odd) byte on DAT8*-DATF* |

### 3.2.3 Control Lines

The control lines are comprised of the following signals:

| | |
|---|---|
| Interrupt Requests | INT0* - INT7* |
| Bus Priority | BPRN* - BPRO* |
| Initialize | INIT* |
| Memory Read Command | MRDC* |
| Memory Write Command | MWTC* |
| I/O Read Command | IOWC* |
| I/O Write Command | IOWC* |
| Transfer Acknowledge | XACK* |

#### 3.2.3.1 Memory Read Command (MRDC*)

MRDC* indicates that a memory read cycle is to be performed and an address is valid on ADR0* - ADR17*. The memory must respond with XACK* and drive data on DAT0*-DATF* within 1.5 microseconds if an in-range address was present at the leading edge of MRDC*. Refer to Figure 2.1 for memory read timing.

#### 3.2.3.2 Memory Write Command (MWTC*)

MWTC* is an indication to the memory that a valid address and and data are on the bus and a write cycle is to be performed if an in-range address was present at the leading edge of MWTC*. If an in-range address was present, the memory must respond with XACK* within 1.5 microseconds. Refer to Figure 2.2 for memory write timing.

#### 3.2.3.3 I/O Read Command (IORC*)

IORC* is an indication to the CSR that a valid address is present on ADR0* - ADRF* if 16 bit addressing is selected or on ADR0* - ADR7* if 8 bit I/O addressing is selected. If the address matches that of the on board CSR, it must respond within 1.5 microseconds by asserting XACK* and driving the data lines. Either 8 bit or 16 bit data transfers may be performed. Refer to Figure 2.3 for I/O read timing.

#### 3.2.3.4 I/O Write Command (IOWC*)

IOWC* is an indication to the CSR that valid addresses and data are on the bus (8 or 16 bit address or data). If the address matches that of the CSR it must respond with XACK* within 1.5 microseconds and write those bits in the CSR which may be written (Bits 4 thru 15 are read only bits.) Refer to Figure 2.4 for I/O write timing.

3.2.3.5 Transfer Acknowledge (XACK*)

The BLC 0512 will respond with XACK* whenever an in-range address was present during the leading edge of a command signal. It will not be asserted until the BLC 0512 is ready to release the bus on a write cycle or data is valid on the bus during a read cycle.

3.2.3.6 Initialize (INIT*)

INIT* will clear bits 0-3 in the CSR, and clear the interrupt flip flop.

3.2.3.7 Interrupt Requests (INT0* - INT7*)

One of eight interrupt requests may be jumper selected on the BLC 0512. The selected interrupt request will be driven active when a parity error occurs and bit 1 in the CSR, (enable parity reporting) is set to a 1. The BLC 0512 will accommodate non-bus vectored interrupts only. The interrupt request will be cleared when an I/O write is performed writing a zero into bits 2 or 3 (parity error byte 0 byte 1) of the CSR, or INIT* is asserted.

3.2.3.8 Bus Priority (BPRN*, BPRO*)

The bus priority signals are not used or driven by the BLC 0512. They are jumpered together on the memory to maintain the bus priority daisy chain.

3.2.4 Non Standard Signals

This special group of signals may be connected to the interface via jumpers if desired. Normally, they are not connected. The signals in this group are:

| | |
|---|---|
| Advanced Acknowledge | AACK* |
| External Refresh | M1* |

3.2.4.1 Advanced Acknowledge

Advanced Acknowledge can be jumper selected at one of three different timing taps referenced to setting the Read/Write flip flop. If the use of AACK* is not desired, it may be isolated from the interface connector by removing a jumper. AACK* will only be asserted on memory read or write cycles.

#### 3.2.4.2 External Refresh M1*

M1* can be used as either a synchronous or an asynchronous refresh input. Refer to Figure 3.1 for external refresh timing.

```
   |<---------------15+/-1 us----------->|<->|----100 ns min.
   .---.                                  .---.
   |   |                                  |   |
---|   |----------------------------------|   |-------------
```

Figure 3.1 External Refresh

### 3.3 ADDRESSING

The BLC 0512 will operate with either 20 or 24 bit memory addressing. Addresses ADR1* - ADR13* are received by 74LS533 bus receiver/latches. ADR14* -ADR17* are received by 74LS244 bus receivers and then routed to 74LS533's to be latched. The latched outputs of ADR1* -ADR17 are routed to multiplexers to generate the RAM addresses, to the CSR address selection logic, the CSR error address latch, and the memory selection logic. The outputs of the multiplexers are wire-ORed with the RAM refresh addresses and then routed to a MOS driver for driving the RAM array. If a CSR cycle is to be performed, the CSR address selection logic will generate a -SELIO if the correct address is provided on the bus. If a memory cycle is to be performed, the memory selection logic will generate a LSEL signal if an in range address is present on the bus.

### 3.4 DATA AND PARITY

The BLC 0512 receives and drives data on a bi-directional data bus and also uses a common bi-directional data bus internally. Refer to Figure 3.2 for a block diagram of the data flow. There are four basic components attached to the internal data bus, the bus transceivers which receive data from and transmit data to the system data bus, the data latches which latch data into and from the memory, parity generator/checkers, and the RAM array.

The bus transceivers are 74LS640 octal bus transceivers with the "A" side connected to the system bus and the "B" side connected to the internal bus. Three of these devices are used. One for the lower byte, one for the upper byte and one is used to "swap" the upper byte internal bus to the lower byte system bus.

The data latches are 74LS373 octal transparent latches with three state outputs. The same device is used to latch data into and from the memory. Therefore, both the D inputs and Q outputs are connected to the internal bus. On both read and write cycles the latch is left "open" and the outputs in the high impedance state until data is valid on the internal bus. After data is valid the latches are enabled and the outputs turned on to the active state.

Odd parity is generated on a byte basis and stored in a ninth bit in the RAM array whenever a write cycle is performed. On a read cycle parity is generated from the stored data and compared with the stored parity bit. The result is checked to verify no parity or data errors have occurred. Nine-bit parity generation chips are used, one connected to the upper internal data bus and the other to the lower internal data bus. Both are 74S280's. Additional circuitry is used to control the ninth bit for read and write cycles and to force parity errors if bit 0 of the CSR (Write Wrong Parity) is set.

The RAM array is comprised of 72 64K dynamic RAM's. It is in two 9 x 256K sections, each section being 8 bit x 256K plus 1 x 256 parity storge. Whenever a read cycle is performed on the BLC 0512 a full word read is done internally and only the appropriate byte(s) are driven onto the data bus. If only one byte is written, the other byte will be received but not written into memory. If a full word is written, both bytes are written simultaneously. This is done because the RAM array is structured as a 256K x 18 bit array with only write enable (WE) being unique to each byte.

## 3.5 CONTROL AND STATUS REGISTER (CSR)

The CSR is a hardware register on the BLC 0512 that is used to log the address where a parity error has occurred, indicate which byte it occurred in and control the diagnostic mode. It is accessible as an I/O port using either 8 bit, 12 bit, or 16 bit addressing. If 8 bit addressing is used, the CSR may be assigned to one of 16 different locations in the range 0E to FE. If 12 or 16 bit addressing is used, the CSR may be assigned to one of 256 locations in the range F00E to FFFE. The CSR will respond to one word location or two consecutive byte locations. The bit assignments of the CSR are as follows:

```
15  14  13  12  11  10  9  8  7  6  5  4  3  2  1  0

                                          P  P  W  E
A                                      A  a  a  r  n
d                                      d  r  r  i  a
d                                      d  i  i  t  b
r<------------------------------------>r  t  t  e  l
e                                      e  y  y     e
s                                      s        W
s                                      s  E  E  r  P
                                          r  r  o  a
17  16  15  14  13  12 11 10  F  E  D  C  r  r  n  r
                                          o  o  g  i
                                          r  r     t
                                                P  y
                                          B  B  a
                                          1  0  r  R
                                                i  e
                                                t  p
                                                y  o
                                                   r
                                                   t
```

Bit 0 - Enable Parity Report - Setting this bit to a logical 1 will enable parity reporting. INIT* or writing a zero will clear this bit.

Bit 1 - Write Wrong Parity - Setting this bit to a logical 1 will force incorrect parity to be written. INIT* or writing a zero will clear this bit and allow correct parity to be written.

Bits 2, 3 - Parity Error - Byte 0, 1 - Read/Write bits set to a logical one when a parity error occurs in the respective byte. They are cleared by writing a logical zero or INIT*.

Bits 4-15 - Address C thru Address 17. Read only bits. These bits will store the most significant 12 bits of the address location where the most recent parity error has occurred. These bits cannot be cleared or written.

## 3.6 ARBITRATION

The purpose of arbitration logic on the BLC 0512 is to resolve conflicts between cycles requested by the system bus and refresh cycle requests which are generated internally. Only memory read or write cycles go through the arbitration logic. I/O reads or writes are not arbitrated since they do not require any access to the RAM array. Figure 3.8 is a simplified logic diagram of the arbitration logic. The system cycle request follows a path with mininal time delays, whereas the refresh request follows a path with greater time delays. If a refresh cycle is requested prior to a bus cycle, the bus cycle will be held off by gate 1 until the refresh cycle is completed.

If the bus cycle request is asserted prior to a refresh request, the refresh request will be held off by gate 2 until the bus cycle is complete. If both cycles are requested at about the same time, the bus cycle will be given priority and the refresh request will be blocked at gate 2 and/or 3.

## 3.7 TIMING AND CONTROL

All timing is generated from a single delay line. Various taps from this delay line, gated with control signals from the system bus, provide all necessary timing and control to the other functional blocks of the BLC 0512.

# Chapter 4

# INSTALLATION AND MAINTENANCE

## 4.1 INTRODUCTION

This section contains the basic information necessary to install and maintain the National Semiconductor BLC 0512 Multibus memory module. The BLC 0512 is designed to operate in a variety of configurations including 8 or 16 bit data busses, 20 or 24 bit memory addressing and 8 or 16 bit I/O addressing. Other options which can be selected are internal or external refresh, a CSR (Control and Status Register), selectable interrupts to indicate parity errors, advance acknowledge (AACK) and battery back-up. The following information describes how to install or remove each of these options. Table 4.1 provides descriptions of each jumper option.

## 4.2 TOOLS REQUIRED

No special tools are required for installation. A ball-point pen or small stylus may be needed to set the switches mounted on the memory module.

## 4.3 UNPACKING AND INSPECTION

Carefully unpack the memory module and visually examine it for physical shipping damage; i.e. broken, bent or dented parts.

**CAUTION!**

Do not attempt to install or operate the memory module if damage is apparent.

## 4.4 BACKPLANES

The BLC 0512 memory module is designed to operate in any standard Multibus backplane or any backplane conforming to the IEEE-796 specification. It is slot-independent but should be placed as close to the processor as possible.

## 4.5 PROCESSORS

The BLC 0512 will operate with any standard Multibus processor or processors which conform to the IEEE specification 796.

Table 4.1 Jumper Definitions

| | |
|---|---|
| W10-W17 | I = Installing one of these jumpers connects INT0-INT7, respectively, to the interrupt flip flop on the BLC 0512.<br><br>R = Removing these jumpers isolates the interrupt flip flop from the interface. |
| W18 | I = BPRN* connected to BPRO*<br>R = BPRN* isolated from BPRO* |
| W20, W21 | I = +5 volt battery<br>R = +5 volt standard |
| W22, W23 | I = +5 volt standard<br>R = +5 volt battery |
| W24 | I = Internal Refresh<br>R = External Refresh |
| W25 | I = External Refresh<br>R = Internal Refresh |
| W26 | I = MPRO* installed<br>R = MPRO* isolated from receiver |
| W29 | I = 80 ns tap to AACK*<br>R = 80 ns tap isolated from AACK* |
| W30 | I = 50 ns tap to AACK*<br>R = 50 ns tap isolated from AACK* |
| W31 | I = 30 ns tap to AACK*<br>R = 30 ns tap isolated from AACK* |
| W32 | I = 16 Bit I/O Addressing<br>R = 8 or 12 bit I/O Addressing |
| W33 | I = 12 or 16 bit I/O Addressing<br>R = 8 bit I/O Addressing |
| W34 | I = AACK* to P1-25<br>R = AACK* isolated from P1-25 |
| W35 | I = CSR inhibited<br>R = CSR on |

I = Install

R = Remove

NOTE: All jumpers not listed are installed at the factory and should not be altered.

## 4.6 POWER CONSIDERATIONS

The BLC 0512 requires only +5 volts DC. Jumper points are provided to implement battery back-up if desired. To implement battery back up, refer to Table 4.2. Table 4.3 lists power requirements.

Table 4.2 POWER JUMPERS

| VOLTAGE | INSTALL | REMOVE | AT PINS |
|---|---|---|---|
| +5VDC Standard | W22,W23 | W20,W21 | See Pin List |
| +5VDC Battery | W20,W21 | W22,W23 | P2-3,P2-4 |

Table 4.3 POWER REQUIREMENTS

| VOLTAGE | CURRENT REQUIREMENT (MAX.) |
|---|---|
| +5VDC Standard | 3.1A |
| +5VDC Battery | 1.5A |

## 4.7 ADDRESS RANGE SELECTION

The BLC 0512 will accept either 20 or 24 bit memory addressing. To use 24-bit addressing, close Switch S2-1. To use 20-bit memory addressing, open Switch S2-1. To use fewer than 20 address lines, unused upper-address lines must be pulled up to a voltage high level, and the directions for 20 bit addressing must be followed.

The starting address may be set on any 16K word boundary (32K byte) in the 16 megabyte address range. The starting address is set via DIP Switch S2. Tables 4.4 and 4.5 list the required switch settings if 24 address lines are being used. In this case the starting address is the sum of the starting address in Table 4.4 and the bank address in Table 4.5.

If only 20-bit addressing is used, open Switches S2-6 thru S2-9 and use only Table 4.4 to determine the starting address.

## 4.8 MEMORY SIZE SELECTION

The total memory capacity of the BLC 0512 can be set in 64K Byte increments from 64K to 512K Bytes. This is done via Switches S1-1 thru S1-3. Refer to Table 4.6 for appropriate switch settings.

## Table 4.4 STARTING ADDRESS SELECT

### 0-1024K ADDRESS RANGE

| MULTIBUS STARTING ADDRESS (HEX.) | MEMORY STARTING ADDRESS (K BYTE) | S2-5 | S2-4 | S2-3 | S2-2 | S2-10 |
|---|---|---|---|---|---|---|
| 000000 | 0KB | O | O | O | O | O |
| 008000 | 32KB | O | O | O | O | C |
| 010000 | 64KB | O | O | O | C | O |
| 018000 | 96KB | O | O | O | C | C |
| 020000 | 128KB | O | O | C | O | O |
| 028000 | 160KB | O | O | C | O | C |
| 030000 | 192KB | O | O | C | C | O |
| 038000 | 224KB | O | O | C | C | C |
| 040000 | 256KB | O | C | O | O | O |
| 048000 | 288KB | O | C | O | O | C |
| 050000 | 320KB | O | C | O | C | O |
| 058000 | 352KB | O | C | O | C | C |
| 060000 | 384KB | O | C | C | O | O |
| 068000 | 416KB | O | C | C | O | C |
| 070000 | 448KB | O | C | C | C | O |
| 078000 | 480KB | O | C | C | C | C |
| 080000 | 512KB | C | O | O | O | O |
| 088000 | 544KB | C | O | O | O | C |
| 090000 | 576KB | C | O | O | C | O |
| 098000 | 608KB | C | O | O | C | C |
| 0A0000 | 640KB | C | O | C | O | O |
| 0A8000 | 672KB | C | O | C | O | C |
| 0B0000 | 704KB | C | O | C | C | O |
| 0B8000 | 736KB | C | O | C | C | C |
| 0C0000 | 768KB | C | C | O | O | O |
| 0C8000 | 800KB | C | C | O | O | C |
| 0D0000 | 832KB | C | C | O | C | O |
| 0D8000 | 864KB | C | C | O | C | C |
| 0E0000 | 896KB | C | C | C | O | O |
| 0E8000 | 928KB | C | C | C | O | O |
| 0F0000 | 960KB | C | C | C | C | O |
| 0F8000 | 992KB | C | C | C | C | C |

*K = 1024

O = OPEN
C = CLOSED

Table 4.5 ADDRESS BANK SELECT

1024K - 16,384K ADDRESS RANGE

| MULTIBUS ADDRESS (HEX.) | MEMORY STARTING ADDRESS | S2-9 | S2-8 | S2-7 | S2-6 |
|---|---|---|---|---|---|
| 000000 | 1024K* | O | O | O | O |
| 100000 | 2048KB | O | O | O | C |
| 200000 | 3072KB | O | O | C | O |
| 300000 | 4096KB | O | O | C | C |
| 400000 | 5120KB | O | C | O | O |
| 500000 | 6144KB | O | C | O | C |
| 600000 | 7168KB | O | C | C | O |
| 700000 | 8192KB | O | C | C | C |
| 800000 | 9216KB | C | O | O | O |
| 900000 | 10240KB | C | O | O | C |
| A00000 | 11264KB | C | O | C | O |
| B00000 | 12288KB | C | O | C | C |
| C00000 | 13312KB | C | C | O | O |
| D00000 | 14336KB | C | C | O | C |
| E00000 | 15360KB | C | C | C | O |
| F00000 | 16384KB | C | C | C | C |

K = 1024 O = OPEN
C = CLOSED

Table 4.6

MEMORY SIZE SWITCH SETTINGS

| Memory Size | Switches S1-3 | S1-2 | S1-1 |
|---|---|---|---|
| 64KB | O | O | O |
| 128KB | O | O | C |
| 192KB | O | C | O |
| 256KB | O | C | C |
| 320KB | C | O | O |
| 384KB | C | O | C |
| 448KB | C | C | O |
| 512KB | C | C | C |

KB = 1024 Byte O = OPEN
C = CLOSED

## 4.9 CSR ADDRESS SELECTION

The CSR may be configured to respond to either 8 bit, 12 bit or 16 bit I/O addressing. Refer to Table 4.7 for selection of I/O addressing. If 8 bit addressing is used, the CSR may be assigned to one of 16 possible word addresses. If either 12 or 16 bit addressing is used, the CSR may be assigned to one of 256 word addresses. Refer to Table 4.8 for 8 bit CSR address assignments, also use Table 4.9 if 12 or 16 bit addressing is used.

To inhibit the operation of the CSR, install jumper W35. With the CSR inhibited parity reporting via the Multibus interrupts is enabled. If parity reporting is not desired when W35 is installed, it is necessary to remove the interrupt jumpers.

| I/O Addressing | JUMPERS Install | JUMPERS Remove |
|---|---|---|
| 8 bit | NONE | W32, W33 |
| 12 bit | W33 | W32 |
| 16 bit | W32, W33 | NONE |

Table 4.7 I/O Addressing

| CSR ADDRESS | Switch Settings S3-4 | S3-3 | S3-2 | S3-1 |
|---|---|---|---|---|
| 0E | C | C | C | C |
| 1E | C | C | C | O |
| 2E | C | C | O | C |
| 2E | C | C | O | O |
| 4E | C | O | C | C |
| 5E | C | O | C | O |
| 6E | C | O | O | C |
| 7E | C | O | O | O |
| 8E | O | C | C | C |
| 9E | O | C | C | O |
| AE | O | C | O | C |
| BE | O | C | O | O |
| CE | O | O | C | C |
| DE | O | O | C | O |
| EE | O | O | O | C |
| FE | O | O | O | O |

Table 4.8

LSB, 8-bit CSR Address Assignment

| CSR ADDRESS | Switch Settings | | | |
|---|---|---|---|---|
| | S4-4 | S4-3 | S4-2 | S4-1 |
| F0XX | C | C | C | C |
| F1XX | C | C | C | O |
| F2XX | C | C | O | C |
| F3XX | C | C | O | O |
| F4XX | C | O | C | C |
| F5XX | C | O | C | O |
| F6XX | C | O | O | C |
| F7XX | C | O | O | O |
| F8XX | O | C | C | C |
| F9XX | O | C | C | O |
| FAXX | O | C | O | C |
| FBXX | O | C | O | O |
| FCXX | O | O | C | C |
| FDXX | O | O | C | O |
| FEXX | O | O | O | C |
| FFXX | O | O | O | O |

Table 4.9 MSB, CSR Address

## 4.10 SELECTABLE INTERRUPTS (INT0* THRU INT7*)

Jumpers maybe installed to drive an interrupt request when parity error occurs. Any one of the eight interrupt request lines INT0-INT7 may be selected. The interrupt will be generated when a parity error occurs and parity reporting is enabled via the CSR or the CSR is inhibited by installing jumper W35. See Section 3.4 and 3.5 for a complete description of parity and CSR operation. Table 4.10 lists jumpers for implementing interrupts.

Table 4.10

SELECTABLE INTERRUPT JUMPERS

| INTERRUPT | INSTALL** |
|---|---|
| INT0* | W10 |
| INT1* | W11 |
| INT2* | W12 |
| INT3* | W13 |
| INT4* | W14 |
| INT5* | W15 |
| INT6* | W16 |
| INT7* | W17 |

** Install only one of these jumpers, all others should be removed.

## 4.11 ADVANCE ACKNOWLEDGE (AACK*)

Advance acknowledge can be jumper-selected at one of three different timing taps. If advance acknowledge is not used, it should be isolated from the interface connector by removing jumper W34.

Table 4.11 AACK JUMPERS

| Time from Command* | INSTALL |
|---|---|
| 30ns | W31 |
| 50ns | W30 |
| 80ns | W29 |

* AACK will be held off if a refresh cycle is in progress. This could add up to 400ns to these times.

## 4.12 INTERNAL/EXTERNAL REFRESH

The BLC 0512 can be operated with internal (transparent) refresh or with external refresh. To implement internal refresh, install jumper W24 and remove jumper W25. To implement external refresh, install jumper W25 and remove W24. External refresh may be from either a synchronous or an asynchronous source and will trigger on a low-to-high voltage transition at the interface. See Figure 3.1 for required refresh timing.

## 4.13 INSTALLING MEMORY MODULES

The memory module must be inserted into the backplane with components facing Row 1. Make certain the module is firmly seated in the connector.

CAUTION!
--------

Do not attempt to install or remove memory modules with DC power applied to the backplane. Damage to the memory may occur.

4.14 VERIFYING MEMORY OPERATION

When memory modules are installed, apply DC power and verify operation by running system diagnostics; in particular, those that test the memory.

4.15 MAINTENANCE

The memory itself does not require routine maintenance on a regularly scheduled basis. System diagnostics should be performed from time to time to verify correct operation.

4.16 TROUBLESHOOTING

In the event problems are encountered:

- o Are all power supplies turned on? Verify that +5V is applied to the backplane.

- o Are the correct power jumpers installed?

- o Is the system configured properly? Verify that all modules are firmly seated.

- o Are all system cables properly installed? Check that the cables are connected at each end.

# Chapter 5

# COMPATIBLE EQUIPMENT

## 5.1 INTRODUCTION

The BLC 0512 is designed to interface with any series 80 boards via the system bus as described in the IEEE specification 796 (P796 Bus). The following paragraphs describe the compatibility of the BLC 0512 memory module.

## 5.2 BACKPLANES

The BLC 0512 is designed to be compatible with BLC 604/614 Modular Backplane and Cardcage or any backplane/cardcage that conforms mechanically and electrically to IEEE specification 796.

## 5.3 OTHER MODULES

The BLC 0512 will be compatible with any other modules which are Multibus compatible and that conform completely with IEEE Specification 796.

## Chapter 6

## APPENDIX A

This appendix contains the schematic, assembly drawing and bill of materials pertaining to the BLC 0512 memory card.

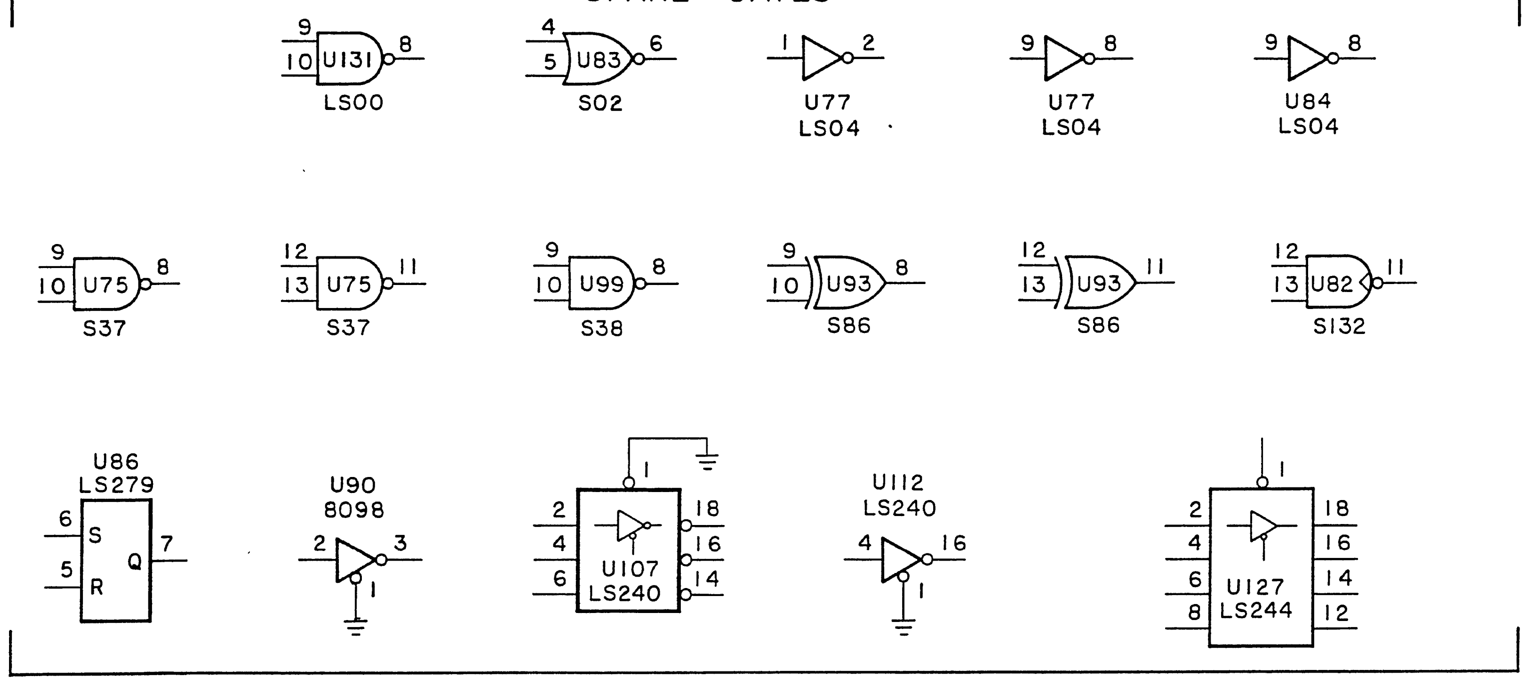
| | |
|---|---|
| 980109405 | Assembly Drawing and Bill of Materials |
| 870109405 | Schematic Diagram |

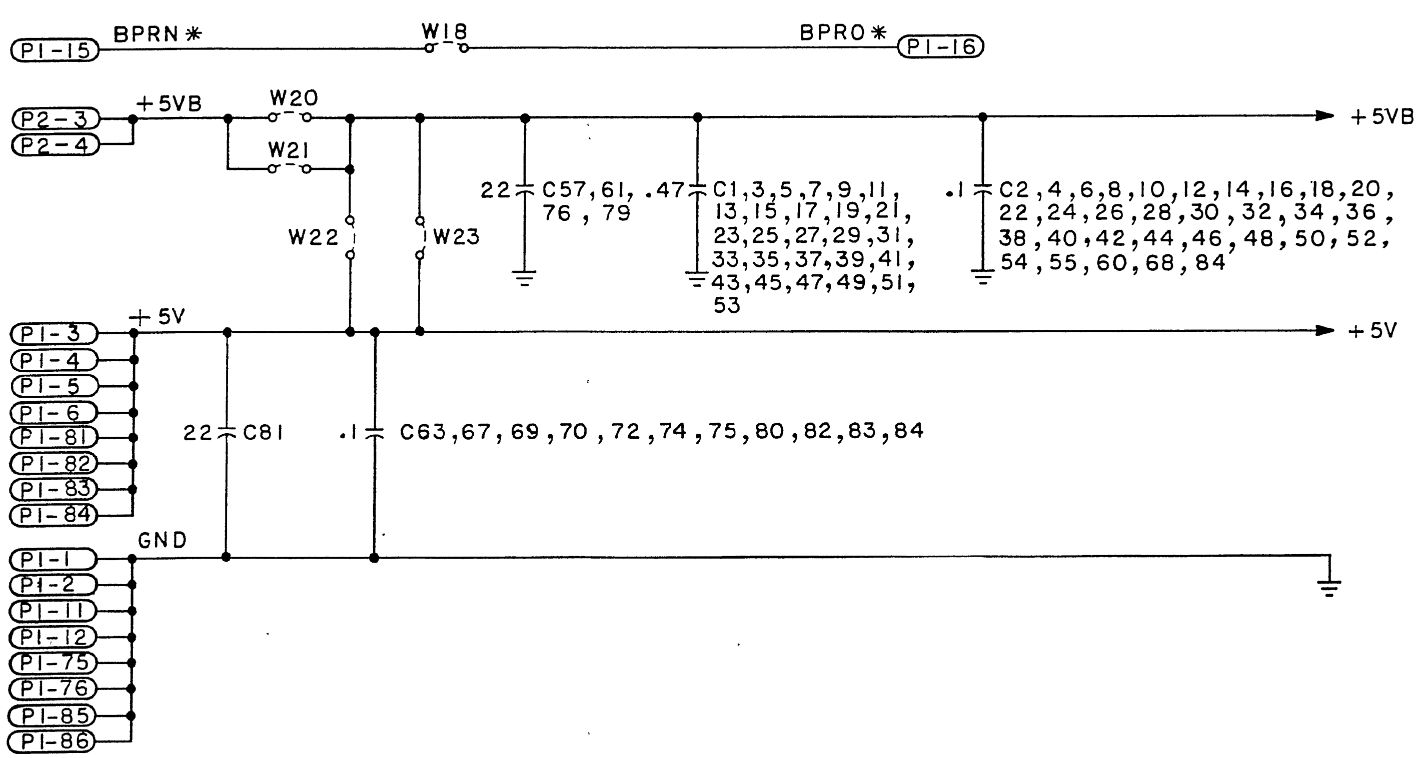
| REVISIONS | | | |
|---|---|---|---|
| REV | DATE | ECO NO. | APPVD |
| A | 9-3-81 | PCO 24146 | |
| A1 | 11-4-81 | PCO 24182 | |
| A2 | 11-4-81 | PCO 24183 | |

## REFERENCE DESIGNATION

| LAST USED | NOT USED | LAST USED | NOT USED |
|---|---|---|---|
| C84 | C64 73 | W56 | |
| R20 | | | |
| RP10 | | | |
| S4 | | | |
| U131 | | | |

## SPARE GATES




## VOLTAGE CHART

| TYPE | +5V | +5VB | GND | REFERENCE DESIGNATION |
|---|---|---|---|---|
| 74LS00 | | 14 | 7 | U74, 129, 131 |
| 74S00 | 14 | | 7 | U125, 126 |
| 74S00 | | 14 | 7 | U87 |
| 74LS02 | 14 | | 7 | U98 |
| 74LS02 | | 14 | 7 | U83 |
| 74LS04 | | 14 | 7 | U77, 84 |
| 74S04 | | 14 | 7 | U78 |
| 74S08 | | 14 | 7 | U89 |
| 74S10 | | 14 | 7 | U88 |
| 74S10 | 14 | | 7 | U95 |
| 74LS21 | 14 | | 7 | U104 |
| 74S22 | | 14 | 7 | U100 |
| 74S32 | 14 | | 7 | U94 |
| 74S32 | | 14 | 7 | U75, 128, 130 |
| 74S38 | 14 | | 7 | U99 |
| 74LS74 | | 14 | 7 | U81 |
| 74S85 | 16 | | 8 | U105, 106 |
| 74S86 | 14 | | 7 | U93 |
| 74S132 | | 14 | 7 | U82 |
| 74S139 | | 16 | 8 | U73 |
| 74S157 | 16 | | 8 | U124 |
| 74S175 | 16 | | 8 | U108 |
| 74LS240 | 20 | | 10 | U107, 112 |
| 74LS244 | | 20 | 10 | U127 |
| 74S257 | 16 | | 8 | U102, 103 |
| 74S260 | | 14 | 7 | U97 |
| 74LS279 | | 16 | 8 | U86 |
| 74S280 | 14 | | 7 | U101, 123 |
| 74S283 | 16 | | 8 | U96, 110, 111 |
| 74LS373 | 20 | | 10 | U118, 122 |
| 74LS374 | 20 | | 10 | U114, 115 |
| 74S374 | 20 | | 10 | U92 |
| 74LS393 | | 14 | 7 | U91 |
| 74LS533 | 20 | | 10 | U113, 116, 117 |
| 74LS640 | 20 | | 10 | U119, 120, 121 |
| LM555 | | 8 | 1 | U80 |
| 3628 | 20 | | 10 | U85 |
| 8098 | | 16 | 8 | U90 |

NOTES. UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS, 1/8W, ±5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS, 25V, $^{+80}_{-20}$%.

| NEXT ASSY | USED ON |
|---|---|
| | |

MATERIAL

FINISH

TOLERANCE ANG. 2 PL 3 PL

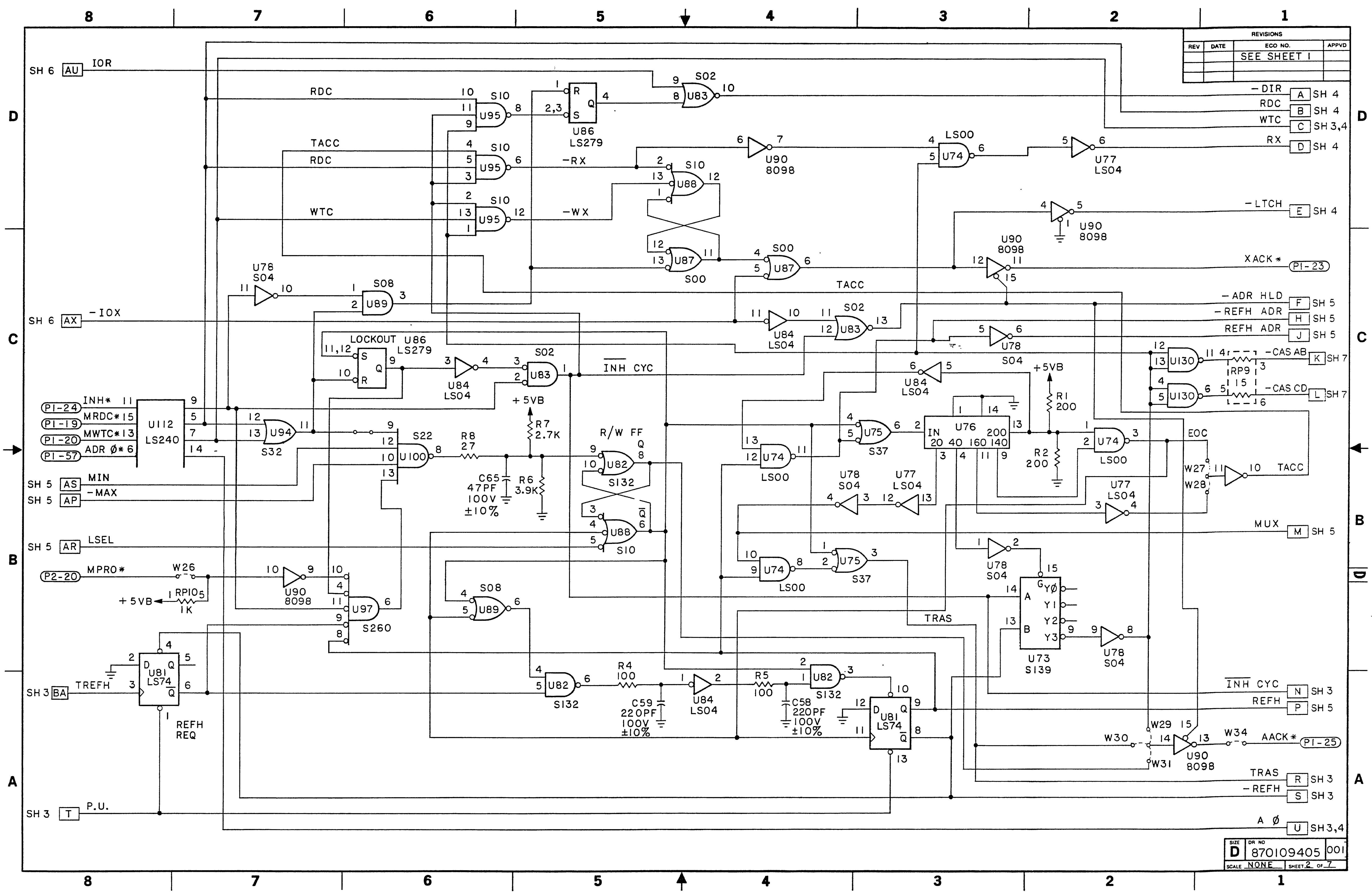
DR BY W. Yako 25AUG81
CHK BY
ME
EE
PE 9-3-81

UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES BREAK SHARP CORNERS .015 MAX.

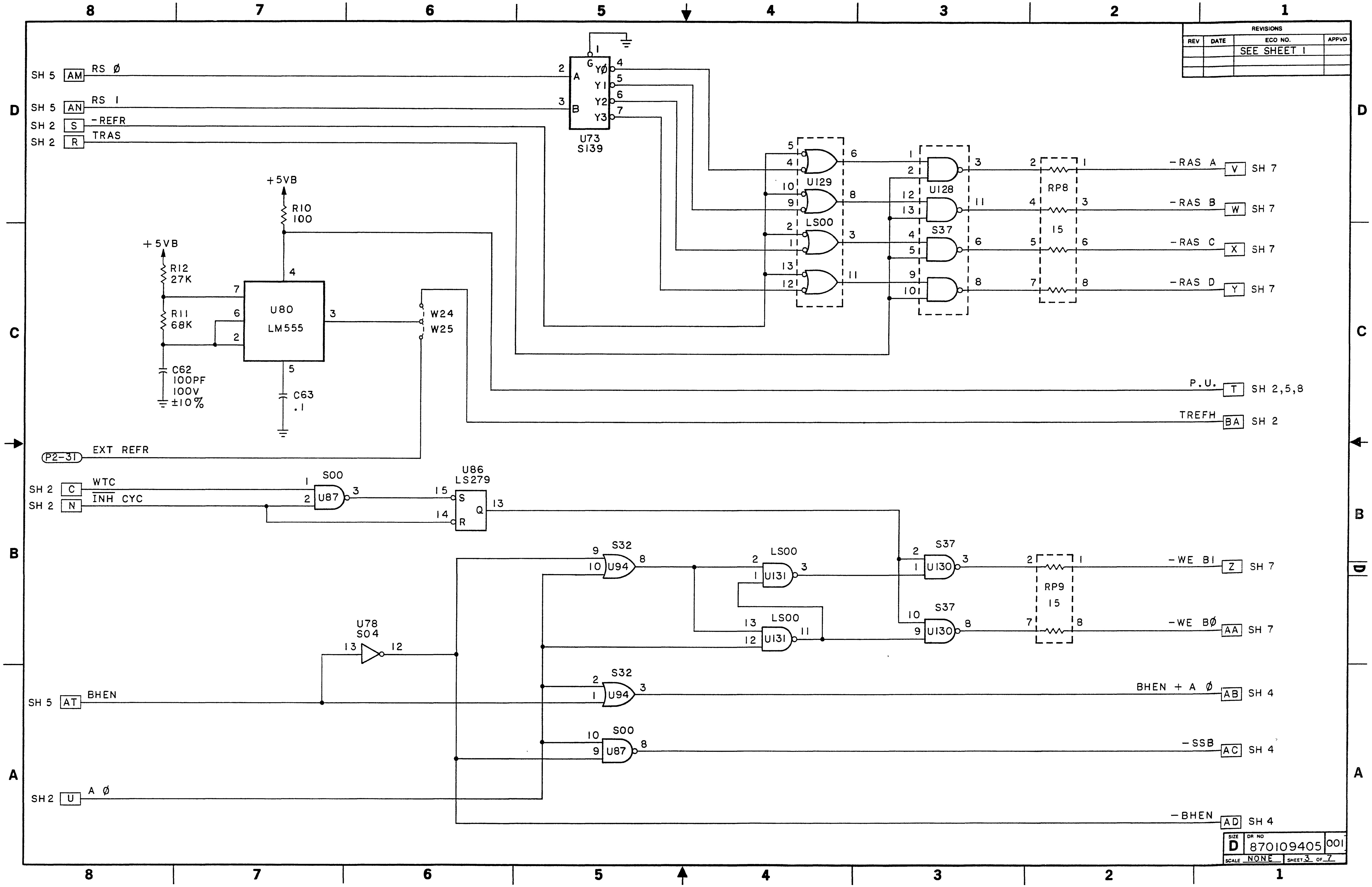
National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SCHEMATIC DIAGRAM
BLC 0512

SIZE D DR NO 870109405 001
SCALE NONE SHEET 1 OF 7



REVISIONS
REV DATE ECO NO. APPVD
SEE SHEET I
SH 6 AU IOR
RDC
TACC
RDC
WTC
-RX
-WX
S10 U95
U86 LS279
S02 U83
S10 U88
S00 U87
U90 8098
LS00 U74
U77 LS04
-DIR A SH 4
RDC B SH 4
WTC C SH 3,4
RX D SH 4
-LTCH E SH 4
XACK* P1-23
TACC
-ADR HLD F SH 5
-REFH ADR H SH 5
REFH ADR J SH 5
-CAS AB K SH 7
-CAS CD L SH 7
RP9
U130
SH 6 AX -IOX
U78 S04
S08 U89
LOCKOUT U86 LS279
U84 LS04
INH CYC
P1-24 INH*
P1-19 MRDC*
P1-20 MWTC*
P1-57 ADR Ø*
U112 LS240
S32 U94
S22 U100
R8 27
+5VB
R7 2.7K
C65 47PF 100V ±10%
R6 3.9K
R/W FF
S132 U82
S10 U88
U75 S37
U76 IN 20 40 160 140 200
R1 200
R2 200
EOC
W27 W28
TACC
MUX M SH 5
SH 5 AS MIN
SH 5 AP -MAX
SH 5 AR LSEL
P2-20 MPRO* W26
+5VB RP10 1K
S260 U97
U73 S139
TRAS
SH 3 BA TREFH
U81 LS74
REFH REQ
R4 100
C59 220PF 100V ±10%
R5 100
C58 220PF 100V ±10%
INH CYC N SH 3
REFH P SH 5
W29 W30 W31 W34
AACK* P1-25
TRAS R SH 3
-REFH S SH 3
SH 3 T P.U.
A Ø U SH 3,4
SIZE D DR NO 870109405 001
SCALE NONE SHEET 2 OF 7


REVISIONS
REV | DATE | ECO NO. | APPVD
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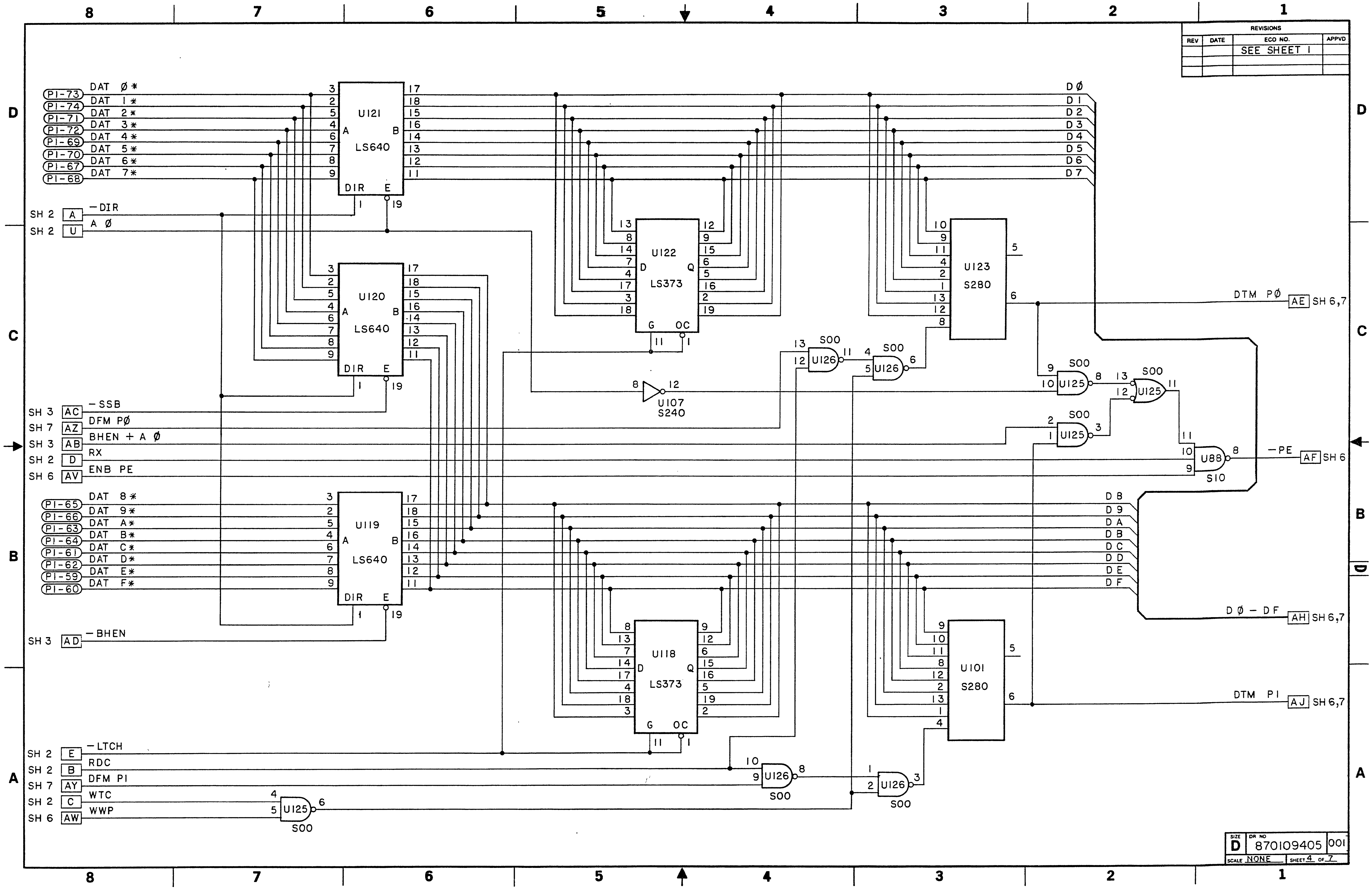
SH 5 AM RS Ø
SH 5 AN RS 1
SH 2 S -REFR
SH 2 R TRAS
U73
S139
G
A
B
YØ
Y1
Y2
Y3
U129
LS00
U128
S37
RP8
15
-RAS A V SH 7
-RAS B W SH 7
-RAS C X SH 7
-RAS D Y SH 7
+5VB
R10
100
R12
27K
R11
68K
C62
100PF
100V
±10%
U80
LM555
C63
.1
W24
W25
P.U. T SH 2,5,8
TREFH BA SH 2
P2-31 EXT REFR
SH 2 C WTC
SH 2 N INH CYC
S00
U87
U86
LS279
S
R
Q
S32
U94
LS00
U131
S37
U130
RP9
15
-WE B1 Z SH 7
-WE BØ AA SH 7
U78
S04
SH 5 AT BHEN
BHEN + A Ø AB SH 4
-SSB AC SH 4
SH2 U A Ø
-BHEN AD SH 4
SIZE D
DR NO 870109405 001
SCALE NONE
SHEET 3 OF 7



REVISIONS
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P1-73 DAT Ø*
P1-74 DAT 1*
P1-71 DAT 2*
P1-72 DAT 3*
P1-69 DAT 4*
P1-70 DAT 5*
P1-67 DAT 6*
P1-68 DAT 7*
U121 LS640
U120 LS640
U119 LS640
U122 LS373
U118 LS373
U123 S280
U101 S280
U107 S240
U125 S00
U126 S00
U88 S10
DØ D1 D2 D3 D4 D5 D6 D7
D8 D9 DA DB DC DD DE DF
SH 2 A -DIR
SH 2 U AØ
SH 3 AC -SSB
SH 7 AZ DFM PØ
SH 3 AB BHEN + AØ
SH 2 D RX
SH 6 AV ENB PE
P1-65 DAT 8*
P1-66 DAT 9*
P1-63 DAT A*
P1-64 DAT B*
P1-61 DAT C*
P1-62 DAT D*
P1-59 DAT E*
P1-60 DAT F*
SH 3 AD -BHEN
SH 2 E -LTCH
SH 2 B RDC
SH 7 AY DFM P1
SH 2 C WTC
SH 6 AW WWP
DTM PØ AE SH 6,7
-PE AF SH 6
DØ - DF AH SH 6,7
DTM P1 AJ SH 6,7
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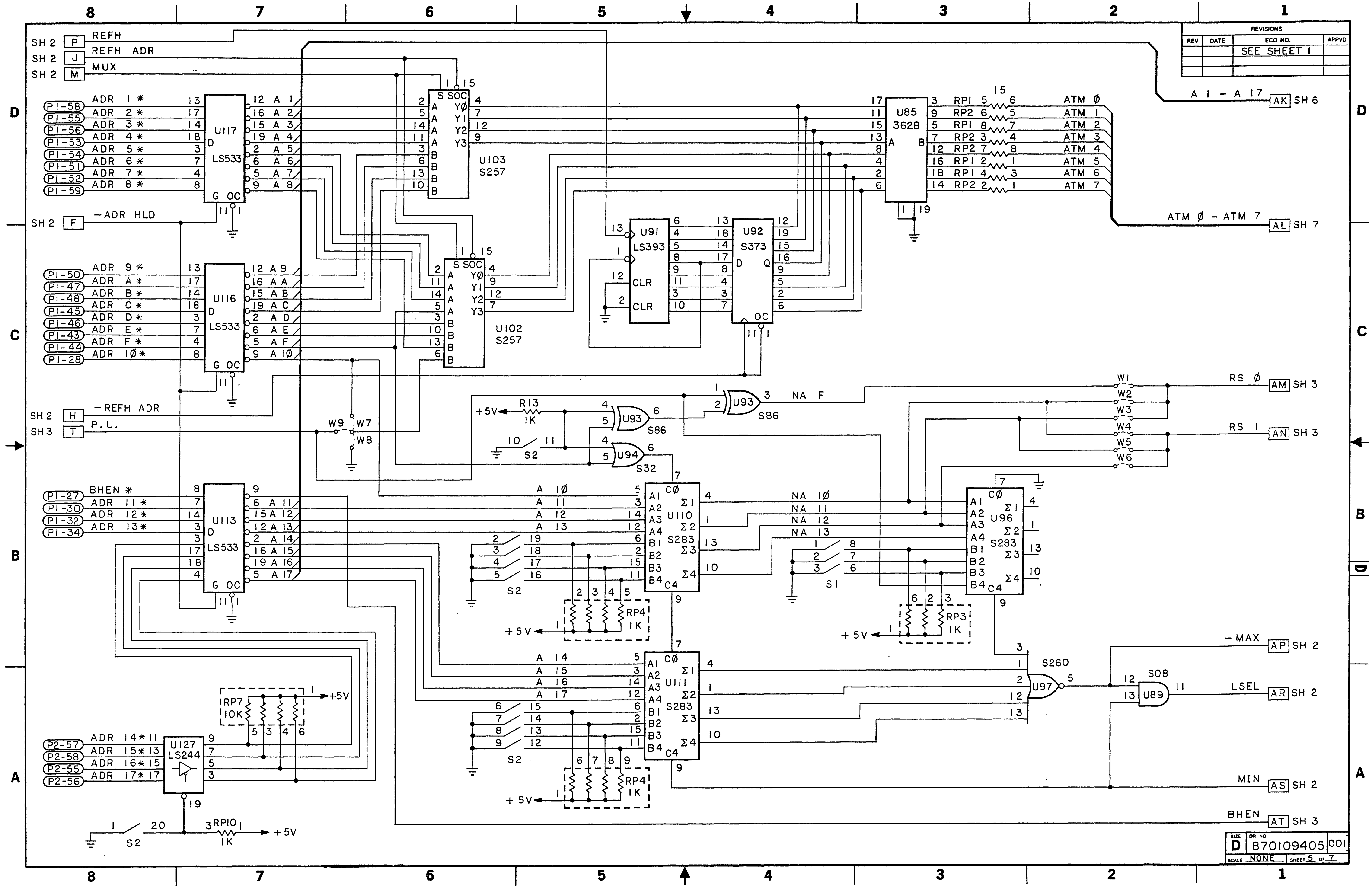
REVISIONS
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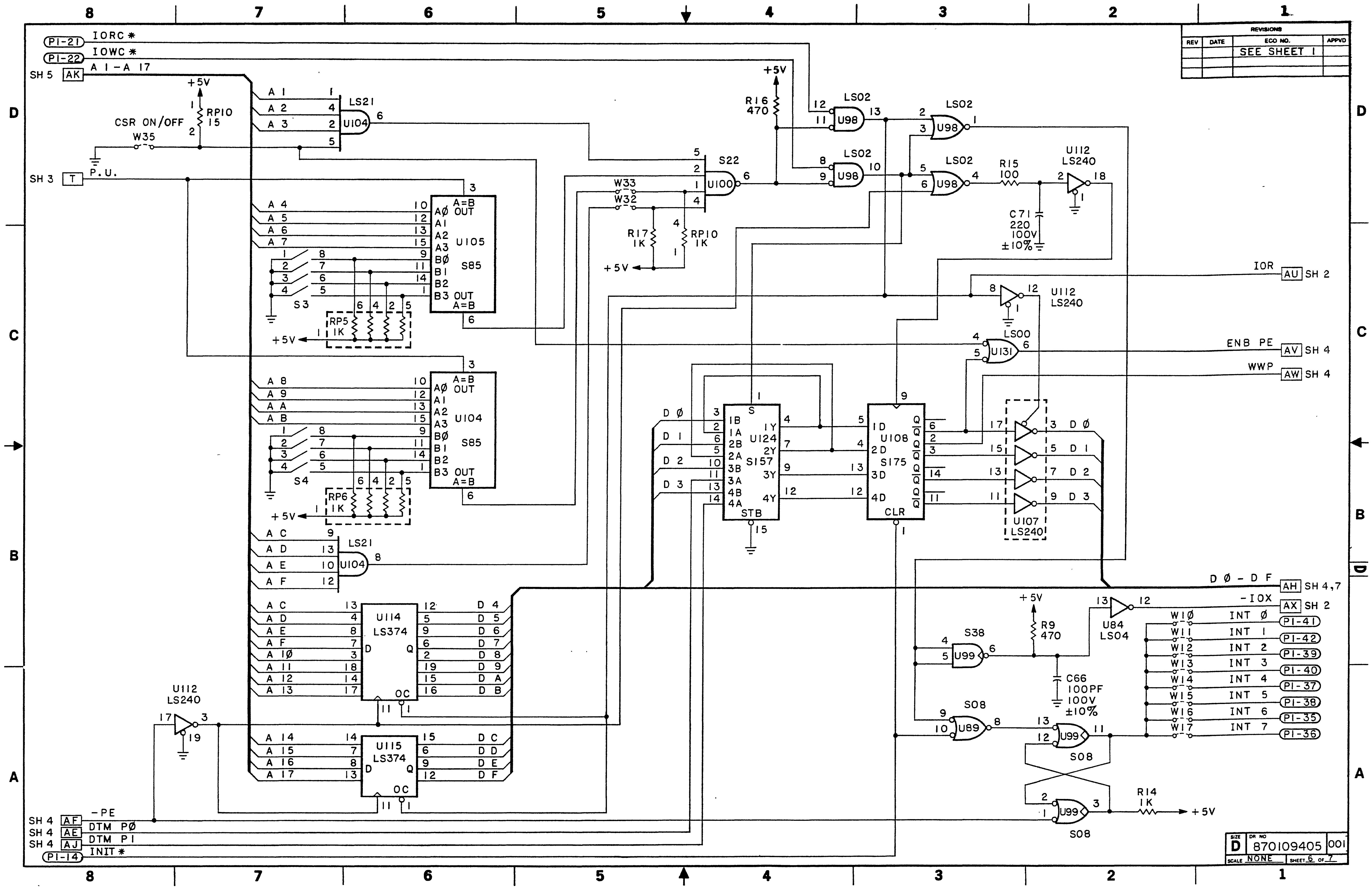
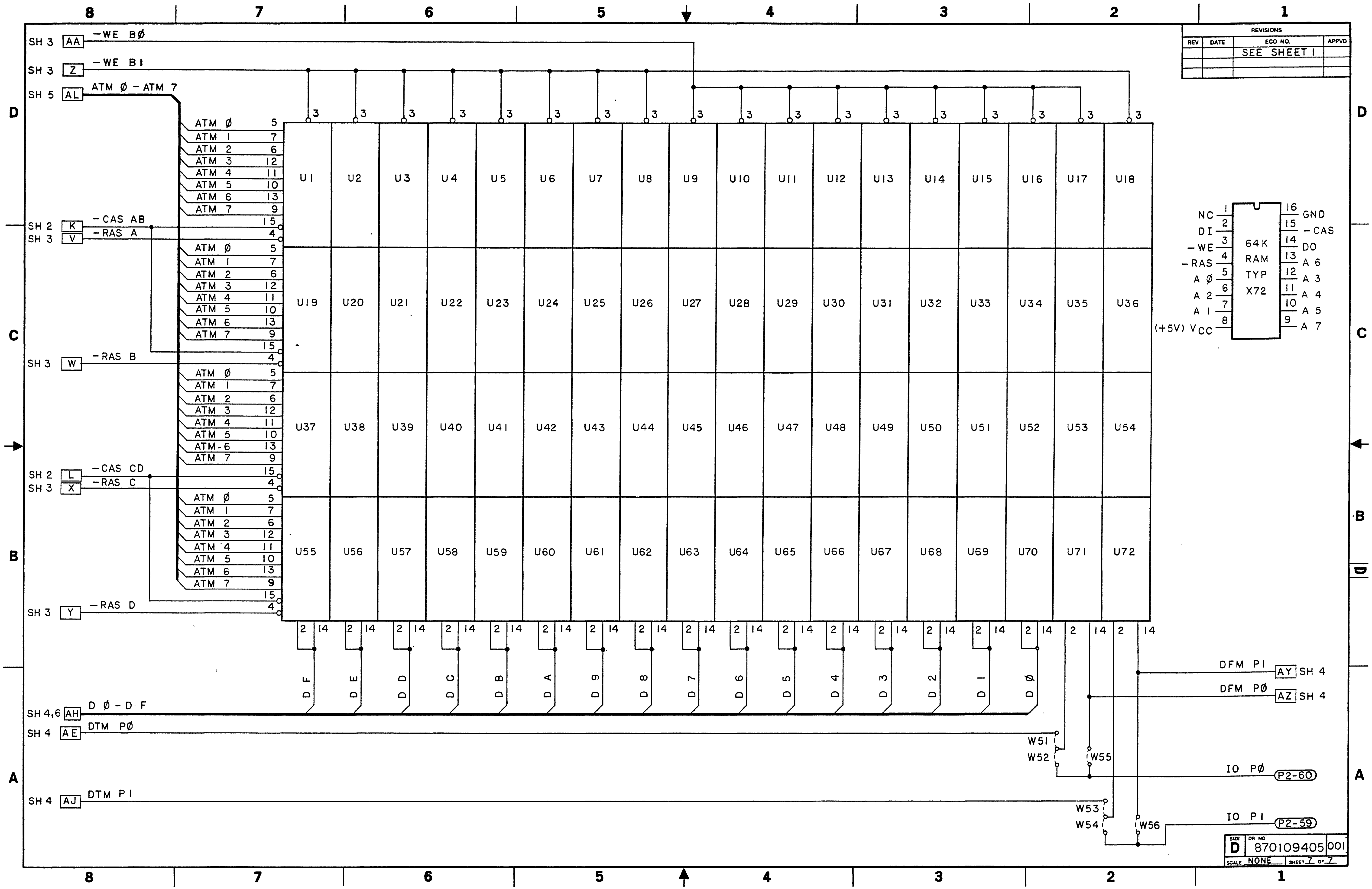
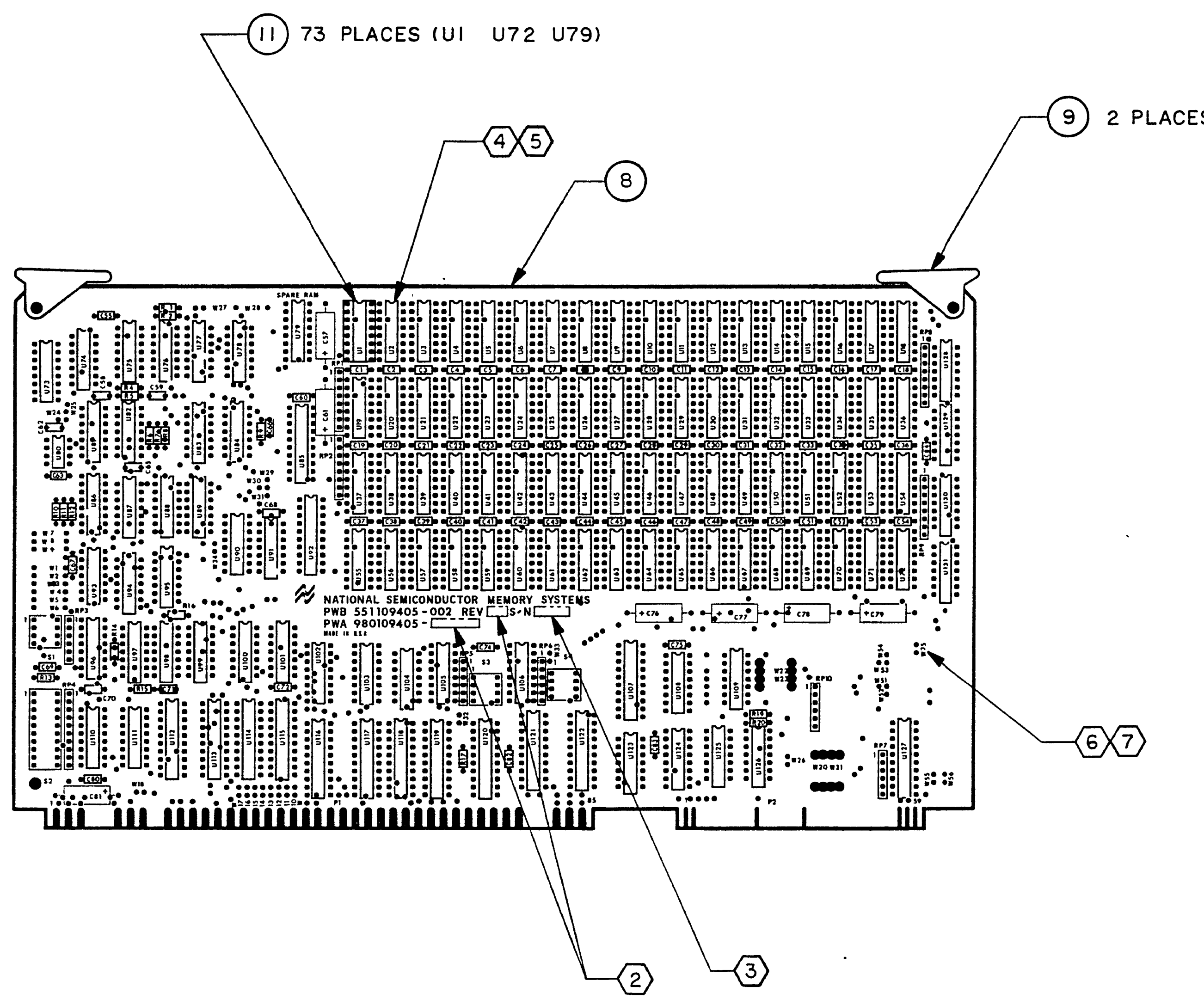
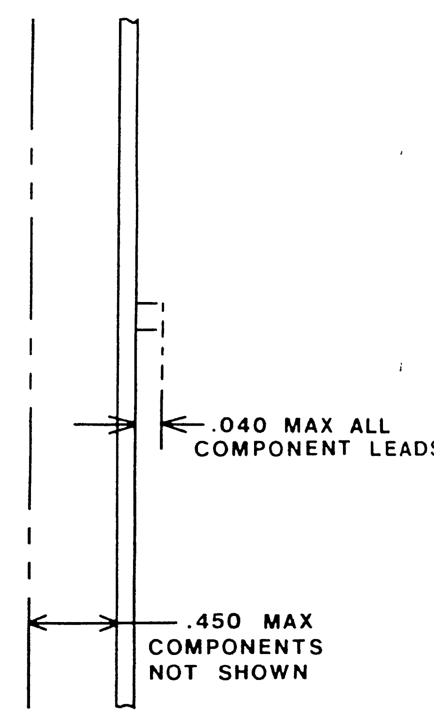
SEE SHEET 1
SH 2 P REFH
SH 2 J REFH ADR
SH 2 M MUX
ADR 1* ADR 2* ADR 3* ADR 4* ADR 5* ADR 6* ADR 7* ADR 8*
P1-58 P1-55 P1-56 P1-53 P1-54 P1-51 P1-52 P1-59
U117 LS533
U103 S257
U102 S257
U85 3628
RP1 RP2
ATM Ø ATM 1 ATM 2 ATM 3 ATM 4 ATM 5 ATM 6 ATM 7
A 1 - A 17 AK SH 6
ATM Ø - ATM 7 AL SH 7
SH 2 F -ADR HLD
U91 LS393
U92 S373
ADR 9* ADR A* ADR B* ADR C* ADR D* ADR E* ADR F* ADR 1Ø*
P1-50 P1-47 P1-48 P1-45 P1-46 P1-43 P1-44 P1-28
U116 LS533
SH 2 H -REFH ADR
SH 3 T P.U.
W9 W7 W8
+5V R13 1K
S2
U93 S86
U94 S32
NA F
W1 W2 W3 W4 W5 W6
RS Ø AM SH 3
RS 1 AN SH 3
BHEN*
ADR 11* ADR 12* ADR 13*
P1-27 P1-30 P1-32 P1-34
U113 LS533
U110 S283
NA 1Ø NA 11 NA 12 NA 13
U96 S283
S1
RP4 1K
RP3 1K
+5V
U111 S283
U97 S260
U89 S08
-MAX AP SH 2
LSEL AR SH 2
MIN AS SH 2
BHEN AT SH 3
RP7 10K
ADR 14* ADR 15* ADR 16* ADR 17*
P2-57 P2-58 P2-55 P2-56
U127 LS244
RP10 1K
SIZE D DR NO 870109405 001
SCALE NONE SHEET 5 OF 7


REVISIONS
REV DATE ECO NO. APPVD
SEE SHEET 1
IORC *
IOWC *
A 1 - A 17
CSR ON/OFF
W35
RP10 15
+5V
P.U.
LS21 U104
S22 U100
W33
W32
R17 1K
RP10 1K
R16 470
LS02 U98
R15 100
C71 220 100V ±10%
U112 LS240
U105 S85
U104 S85
S3
S4
RP5 1K
RP6 1K
A=B OUT
IOR
ENB PE
WWP
LS00 U131
U124 S157
U108 S175
U107 LS240
D Ø - D F
-IOX
U114 LS374
U115 LS374
U84 LS04
S38 U99
R9 470
C66 100PF 100V ±10%
S08 U89
S08 U99
R14 1K
W1Ø W11 W12 W13 W14 W15 W16 W17
INT Ø INT 1 INT 2 INT 3 INT 4 INT 5 INT 6 INT 7
P1-41 P1-42 P1-39 P1-40 P1-37 P1-38 P1-35 P1-36
-PE
DTM PØ
DTM P1
INIT *
SH 2
SH 4
SH 4,7
SH 5
SH 3
SIZE D
DR NO 870109405 001
SCALE NONE
SHEET 6 OF 7


REVISIONS
REV DATE ECO NO. APPVD
SEE SHEET I
SH 3 AA -WE BØ
SH 3 Z -WE B1
SH 5 AL ATM Ø - ATM 7
SH 2 K -CAS AB
SH 3 V -RAS A
SH 3 W -RAS B
SH 2 L -CAS CD
SH 3 X -RAS C
SH 3 Y -RAS D
ATM Ø 5
ATM 1 7
ATM 2 6
ATM 3 12
ATM 4 11
ATM 5 10
ATM 6 13
ATM 7 9
U1 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12 U13 U14 U15 U16 U17 U18
U19 U20 U21 U22 U23 U24 U25 U26 U27 U28 U29 U30 U31 U32 U33 U34 U35 U36
U37 U38 U39 U40 U41 U42 U43 U44 U45 U46 U47 U48 U49 U50 U51 U52 U53 U54
U55 U56 U57 U58 U59 U60 U61 U62 U63 U64 U65 U66 U67 U68 U69 U70 U71 U72
DF DE DD DC DB DA D9 D8 D7 D6 D5 D4 D3 D2 D1 DØ
SH 4,6 AH DØ - DF
SH 4 AE DTM PØ
SH 4 AJ DTM P1
DFM P1 AY SH 4
DFM PØ AZ SH 4
W51 W52 W53 W54 W55 W56
IO PØ P2-60
IO P1 P2-59
NC 1
DI 2
-WE 3
-RAS 4
A Ø 5
A 2 6
A 1 7
(+5V) VCC 8
64K RAM TYP X72
16 GND
15 -CAS
14 DO
13 A 6
12 A 3
11 A 4
10 A 5
9 A 7
SIZE D
DR NO 870109405 001
SCALE NONE
SHEET 7 OF 7

| REVISIONS | | | |
|---|---|---|---|
| REV | DATE | ECO NO | APPVD |
| A | — | PCO 24158 | |
| B | 10-24-1 | PCO 24161 | [signature] |




1. ASSEMBLE AND SOLDER PER NSC SPEC. 429306098.
2. MARK ASSY. DASH NO. AND REV. LEVEL WITH .12 – .18 HIGH CHARACTERS WHERE SHOWN.
3. MARK ASSY. S/N WITH .12 – .18 HIGH CHARACTERS WHERE SHOWN.
4. INSTALL MEMORY I.C.'S SPECIFIED IN THE MEMORY ELEMENT PART NUMBER CHART.
5. INSTALL MEMORY I.C.'S ACCORDING TO THE MEMORY ELEMENT POPULATION CHART.
6. INSTALL JUMPERS ACCORDING TO THE TEST CONFIGURATION JUMPER TABLE.
7. AFTER TEST AND BEFORE FINAL CPU TEST, INSTALL JUMPERS ACCORDING TO THE FACTORY INSTALLED JUMPER TABLE.

| LAST USED | NOT USED |
|---|---|
| C84 | C64,73 |
| R20 | |
| RP10 | |
| S4 | |
| U131 | |

MATERIAL
FINISH
TOLERANCE: ANG — 2 PL — 3 PL —

DR BY W. Yaka 23 OCT 81
CHK BY
ME
EE Paul Lubeck 10-24-81
PE Paul Lubeck 10-24-81

UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX

National Semiconductor Corporation
2900 Semiconductor Drive Santa Clara Calif 95051

PWB ASSEMBLY DRAWING
BLC 0512

SIZE D | DR NO 980109405 | 000
SCALE 1:1 | SHEET 1 OF 3

| REVISIONS | | | |
|---|---|---|---|
| REV | DATE | ECO NO. | APPVD |
| | | SEE SHEET 1 | |

## ④ MEMORY ELEMENT PART NUMBER CHART

| VERSION | ITEM FIND NUMBER | DESCRIPTION |
|---|---|---|
| -00Z | 89 | 64K X 1 , DRAM , CERAMIC , 200NS |
| -01Z * | 90 | 32K X 1 , DRAM , CERAMIC , 200NS , UPPER |
| -02Z * | 91 | 32K X 1 , DRAM , CERAMIC , 200NS , LOWER |
| -03Z * | 92 | 16K X 1 , DRAM , CERAMIC , 200NS |
| -50Z | 93 | 64K X 1 , DRAM , PLASTIC , 200NS |
| -51Z * | 94 | 32K X 1 , DRAM , PLASTIC , 200NS , UPPER |
| -52Z * | 95 | 32K X 1 , DRAM , PLASTIC , 200NS , LOWER |
| -53Z * | 96 | 16K X 1 , DRAM , PLASTIC , 200NS |
| -04Z | | |
| -05Z | | |
| -06Z | | |
| -07Z | | |
| -54Z | | |
| -55Z | | |
| -56Z | | |
| -57Z | | |

* PLANNED FUTURE PRODUCT.

## DASH NUMBER DEFINITIONS - REFERENCE ONLY - XYZ

| X | Y | Z |
|---|---|---|
| 0 = CERAMIC RAM<br>5 = PLASTIC RAM | 0 = 64K RAM , 200NS<br>1 = 32K RAM , 200NS , UPPER<br>2 = 32K RAM , 200NS , LOWER<br>3 = 16K RAM , 200NS | 0 = UNPOPULATED<br>1 = 512K WITH PARITY<br>2 = 384K WITH PARITY<br>3 = 256K WITH PARITY<br>4 = 128K WITH PARITY<br>5 = 512K W/O PARITY<br>6 = 384K W/O PARITY<br>7 = 256K W/O PARITY<br>8 = 128K W/O PARITY |

## ⑤ MEMORY ELEMENT POPULATION CHART

| VERSION | INSTALL LOCATIONS | | | NOTES |
|---|---|---|---|---|
| | -00Z , -50Z | -01Z , -02Z , -51Z , -52Z | -03Z , -53Z | |
| -XY0 | NONE | NONE | NONE | UNPOPULATED |
| -XY1 | U1 - U72 , U79 | N/A | N/A | 512K BYTE WITH PARITY |
| -XY2 | U1 - U54 , U79 | N/A | N/A | 384K BYTE WITH PARITY |
| -XY3 | U1 - U36 , U79 | U1 - U72 , U79 | N/A | 256K BYTE WITH PARITY |
| -XY4 | U1 - U18 , U79 | U1 - U36 , U79 | U1 - U72 , U79 | 128K BYTE WITH PARITY |
| -XY5 | U1 - U16 , U19 - U34 , U37 - U52 , U55 - U70 , U79 | N/A | N/A | 512K BYTE W/O PARITY |
| -XY6 | U1 - U16 , U19 - U34 , U37 - U52 , U79 | N/A | N/A | 384K BYTE W/O PARITY |
| -XY7 | U1 - U16 , U19 - U34 , U79 | U1 - U16 , U19 - U34 , U37 - U52 , U55 - U70 , U79 | N/A | 256K BYTE W/O PARITY |
| -XY8 | U1 - U16 , U79 | U1 - U16 , U19 - U34 , U79 | U1 - U16 , U19 - U34 , U37 - U52 , U55 - U70 , U79 | 128K BYTE W/O PARITY |

| SIZE | DR NO | |
|---|---|---|
| D | 980109405 | 000 |
| SCALE 1 : 1 | SHEET 2 OF 3 | |

| REVISIONS | | | |
|---|---|---|---|
| REV | DATE | ECO NO. | APPVD |
| | | SEE SHEET 1 | |

## ⑥ TEST CONFIGURATION JUMPER TABLE

| VERSION | INSTALL | ITEM FIND NUMBER | REMOVE |
|---|---|---|---|
| -X0Z | W3 W6 , W7 , W27 | 14 | W1 , W2 , W4 , W5 , W8 , W9 , W28 |
| -X1Z | W2 , W5 , W9 , W27 | 14 | W1 , W3 , W4 , W6 – W8 , W28 |
| -X2Z | W2 , W5 , W8 , W27 | 14 | W1 , W3 , W4 , W6 , W7 , W9 , W28 |
| -X3Z | W1 , W4 , W7 , W27 | 14 | W2 , W3 , W5 , W6 , W8 , W9 , W28 |
| -X4Z | W3 , W6 , W7 , W28 | 14 | W1 , W2 , W4 , W5 , W8 , W9 , W27 |
| -X5Z | W2 , W5 , W9 , W28 | 14 | W1 , W3 , W4 , W6 – W8 , W27 |
| -X6Z | W2 , W5 , W8 , W28 | 14 | W1 , W3 , W4 , W6 , W7 , W9 , W27 |
| -X7Z | W1 , W4 , W7 , W28 | 14 | W2 , W3 , W5 , W6 , W8 , W9 , W27 |
| ALL | W10 , W18 , W24 , W29 , W32 , W34 , W52 , W54 – W56 | 13 | W11 – W17 , W20 , W21 , W25 , W26 , W30 , W31 , W35 , W51 , W53 |
| ALL | W22 , W23 , W33 | 14 | |

## ⑦ FACTORY INSTALLED JUMPER TABLE

| VERSION | INSTALL | ITEM FIND NUMBER | REMOVE |
|---|---|---|---|
| -X0Z | W3 , W6 , W7 W27 | 14 | W1 , W2 , W4 , W5 , W8 , W9 , W28 |
| -X1Z | W2 , W5 , W9 , W27 | 14 | W1 , W3 , W4 , W6 – W8 , W28 |
| -X2Z | W2 , W5 , W8 , W27 | 14 | W1 , W3 , W4 , W6 , W7 , W9 , W28 |
| -X3Z | W1 , W4 , W7 , W27 | 14 | W2 , W3 , W5 , W6 , W8 , W9 , W28 |
| -X4Z | W3 , W6 , W7 , W28 | 14 | W1 , W2 , W4 , W5 , W8 , W9 , W27 |
| -X5Z | W2 , W5 , W9 , W28 | 14 | W1 , W3 , W4 , W6 – W8 , W27 |
| -X6Z | W2 , W5 , W8 , W28 | 14 | W1 , W3 , W4 , W6 , W7 , W9 , W27 |
| -X7Z | W1 , W4 , W7 , W28 | 14 | W2 , W3 , W5 , W6 , W8 , W9 , W27 |
| ALL | W18 , W24 , W29 , W32 , W33 , W51 , W53 | 13 | W10 – W17 , W20 , W21 , W25 , W26 , W30 , W31 , W34 , W35 , W52 , W54 – W56 |
| ALL | W22 , W23 | 14 | |

| SIZE | DR NO | |
|---|---|---|
| D | 980109405 | 000 |
| SCALE 1:1 | SHEET 3 OF 3 | |

BILL OF MATERIALS NO. 980109405-000

UNIT OF MEAS = EA: EACH, IN.: INCH, FT: FEET, BK: BULK, AR: AS REQ'D

| ITEM FIND NO | QUANTITY PER ASSEMBLY | UNIT OF MEAS | PART NUMBER/REFERENCE DOCUMENT | DESCRIPTION | REF DESIGNATOR |
|---|---|---|---|---|---|
| 1 | | REF | 870109405-001 | SCHEMATIC DIAGRAM | |
| 2 | | REF | 427109405-001 | TEST PROCEDURE | |
| 3 | | REF | 420109405-001 | TECHNICAL MANUAL | |
| 4 | | | - | | |
| 5 | | | - | | |
| 6 | | | - | | |
| 7 | | | - | | |
| 8 | 1 | EA | 551109405-002 | PC BOARD | |
| 9 | 2 | EA | 740003058-001 | CARD EJECTOR | |
| 10 | | | - | | |
| 11 | 73 | EA | 214102685-003 | SOCKET 16 POS | U1-U72, U79 |
| 12 | 43 | EA | 283101551-001 | W/W PIN | W10-17, 24-26, 29-35, 51-56 |
| 13 | 6 | EA | 214101550-001 | W/W JUMPER | NOTE 6. |
| 14 | 4 | EA | 601002749-001 | JUMPER, INSULATED | NOTE 6. |
| 15 | | | - | | |
| 16 | 3 | EA | 513107003-004 | DIP SWITCH 4 POS | S1, 3, 4 |
| 17 | 1 | EA | 513107003-010 | DIP SWITCH 10 POS | S2 |
| 18 | | | - | | |
| 19 | | | - | | |
| 20 | | | - | | |
| 21 | | | - | | |
| 22 | | | - | | |

| ENG CHG | | |
|---|---|---|
| REV | A | B |
| CHG NO | PCO 24158 | PCO 24161 |
| DATE | 8-25-1 | 10-2-1 |
| APPR | [illegible] | [illegible] |

NOTES:

TITLE: BLC 0512

PREPARED BY: DATE:
CHECKED BY: Mark Lainz DATE: 8-26-81
APPROVED BY: DATE:

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, Calif. 95051

SIZE A | BILL OF MATERIALS NO. 980109405-000 | SH 1 OF 5

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BILL OF MATERIALS NO. 980109405-000

UNIT OF MEAS = EA: EACH, IN.: INCH, FT: FEET, BK: BULK, AR: AS REQ'D

| ITEM FIND NO | QUANTITY PER ASSEMBLY | UNIT OF MEAS | PART NUMBER/REFERENCE DOCUMENT | DESCRIPTION | REF DESIGNATOR |
|---|---|---|---|---|---|
| 23 | | | - | | |
| 24 | 1 | EA | 482000311-001 | IC 74S139 | U73 |
| 25 | 3 | EA | 482000354-001 | IC 74LS00 | U74, 129, 131 |
| 26 | 3 | EA | 482100777-001 | IC 74S37 | U75, 128, 130 |
| 27 | 1 | EA | 611101027-200 | DELAY LINE 200NS | U76 |
| 28 | 2 | EA | 482100785-001 | IC 74LS04 | U77, 84 |
| 29 | 1 | EA | 482000180-001 | IC 74S04 | U78 |
| 30 | 1 | EA | 482102160-001 | IC 555 | U80 |
| 31 | 1 | EA | 482100365-001 | IC 74LS74 | U81 |
| 32 | 1 | EA | 482100840-001 | IC 74S132 | U82 |
| 33 | 1 | EA | 482000334-001 | IC 74S02 | U83 |
| 34 | 1 | EA | 482107006-001 | IC 3628 | U85 |
| 35 | 1 | EA | 482107018-001 | IC 74LS279 | U86 |
| 36 | 3 | EA | 482000079-001 | IC 74S00 | U87, 125, 126 |
| 37 | 2 | EA | 482001344-001 | IC 74S10 | U88, 95 |
| 38 | 1 | EA | 482100672-001 | IC 74S08 | U89 |
| 39 | 1 | EA | 482000283-001 | IC 8098 | U90 |
| 40 | 1 | EA | 482102639-001 | IC 74LS393 | U91 |
| 41 | 1 | EA | 482101837-001 | IC 74S374 | U92 |
| 42 | 1 | EA | 482000300-001 | IC 74S86 | U93 |
| 43 | 1 | EA | 482101026-001 | IC 74S32 | U94 |
| 44 | 3 | EA | 482102505-001 | IC 74S283 | U96, 110, 111 |

ENG CHG: REV | CHG NO: SEE SHEET 1 | DATE | APPR

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2900 Semiconductor Drive
Santa Clara, Calif. 95051

SIZE A | BILL OF MATERIALS NO. 980109405-000 | SH 2 OF 5

---

BILL OF MATERIALS NO. 980109405-000

UNIT OF MEAS = EA: EACH, IN: INCH, FT: FEET, BK: BULK, AR: AS REQ'D

| ITEM FIND NO | QUANTITY PER ASSEMBLY | UNIT OF MEAS | PART NUMBER/REFERENCE DOCUMENT | DESCRIPTION | REF DESIGNATOR |
|---|---|---|---|---|---|
| 45 | 1 | EA | 482101177-001 | IC 74S260 | U97 |
| 46 | 1 | EA | 482101381-001 | IC 74LS02 | U98 |
| 47 | 1 | EA | 482100778-001 | IC 74S38 | U99 |
| 48 | 1 | EA | 482000438-001 | IC 74S22 | U100 |
| 49 | 2 | EA | 482000342-001 | IC 74S280 | U101, 123 |
| 50 | 2 | EA | 482101172-001 | IC 74S257 | U102, 103 |
| 51 | 1 | EA | 482107045-001 | IC 74LS21 | U104 |
| 52 | 2 | EA | 482107063-001 | IC 74S85 | U105, 106 |
| 53 | 2 | EA | 482103984-001 | IC 74LS240 | U107, 112 |
| 54 | 1 | EA | 482000437-001 | IC 74S175 | U108 |
| 55 | 3 | EA | 482107061-001 | IC 74LS533 | U113, 116, 117 |
| 56 | 2 | EA | 482107046-001 | IC 74LS374 | U114, 115 |
| 57 | 2 | EA | 482103947-001 | IC 74LS373 | U118, 122 |
| 58 | 3 | EA | 482107062-001 | IC 74LS640 | U119, 120, 121 |
| 59 | 1 | EA | 482000302-001 | IC 74S157 | U124 |
| 60 | 1 | EA | 482103982-001 | IC 74LS244 | U127 |
| 61 | | | - | | |
| 62 | | | - | | |
| 63 | | | - | | |
| 64 | | | - | | |
| 65 | | | - | | |
| 66 | | | - | | |

ENG CHG: REV | CHG NO: SEE SHEET 1 | DATE | APPR

NOTES:

TITLE: BLC 0512

PREPARED BY: DATE:
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2900 Semiconductor Drive
Santa Clara, Calif. 95051

SIZE A | BILL OF MATERIALS NO. 980109405-000 | SH 3 OF 5

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BILL OF MATERIALS NO. 980109405-000

UNIT OF MEAS = EA: EACH, IN.: INCH, FT: FEET, BK: BULK, AR: AS REQ'D

| ITEM FIND NO | QUANTITY PER ASSEMBLY | UNIT OF MEAS | PART NUMBER/REFERENCE DOCUMENT | DESCRIPTION | REF DESIGNATOR |
|---|---|---|---|---|---|
| 67 | 4 | EA | 474107002-001 | RES. SIP 15Ω / 8 | RP1, 2, 8, 9 |
| 68 | 4 | EA | 474100806-041 | RES. SIP 1KΩ / 6 | RP3, 5, 6, 10 |
| 69 | 1 | EA | 474107036-102 | RES. SIP 1KΩ / 10 | RP4 |
| 70 | 1 | EA | 474100806-066 | RES. SIP 10KΩ / 6 | RP7 |
| 71 | 2 | EA | 470101134-047 | RES. CC. 220Ω | R1, 2 |
| 72 | 4 | EA | 470101134-039 | RES. CC. 100Ω | R4, 5, 10, 15 |
| 73 | 1 | EA | 470101134-077 | RES. CC. 3.9KΩ | R6 |
| 74 | 1 | EA | 470101134-073 | RES. CC. 2.7KΩ | R7 |
| 75 | 1 | EA | 470101134-025 | RES. CC. 27Ω | R8 |
| 76 | 2 | EA | 470101134-055 | RES. CC. 470Ω | R9, 16 |
| 77 | 1 | EA | 470101134-107 | RES. CC. 68KΩ | R11 |
| 78 | 1 | EA | 470101134-097 | RES. CC. 27KΩ | R12 |
| 79 | 3 | EA | 470101134-063 | RES. CC. 1KΩ | R13, 14, 17 |
| 80 | | | - | | |
| 81 | 27 | EA | 151104975-012 | CAP. CER .47UF | SEE BELOW 1 |
| 82 | 41 | EA | 151104975-007 | CAP. CER .1UF | SEE BELOW 2 |
| 83 | 2 | EA | 151101308-017 | CAP. CER 220 PF | C58, 59 |
| 84 | 6 | EA | 152107059-004 | CAP. ALUM 22 UF | C57, 61, 76-79, 81 |
| 85 | 3 | EA | 151101308-013 | CAP. CER 100 PF | C62, 66, 71 |
| 86 | 1 | EA | 151101308-009 | CAP. CER 47 PF | C65 |
| 87 | | | - | | |
| 88 | | | - | | |

ENG CHG: REV | CHG NO: SEE SHEET 1 | DATE | APPR

NOTES: ① C1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 51, 53,
② C2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 52, 54, 55, 60, 63, 67, 68, 69, 70, 72, 74, 75, 80, 82, 83, 84,

TITLE: BLC 0512

PREPARED BY: DATE:
CHECKED BY: DATE:
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National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, Calif. 95051

SIZE A | BILL OF MATERIALS NO. 980109405-000 | SH 4 OF 5

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BILL OF MATERIALS NO. 980109405-000

UNIT OF MEAS = EA: EACH, IN.: INCH, FT: FEET, BK: BULK, AR: AS REQ'D

| ITEM FIND NO | QUANTITY PER ASSEMBLY | UNIT OF MEAS | PART NUMBER/REFERENCE DOCUMENT | DESCRIPTION | REF DESIGNATOR |
|---|---|---|---|---|---|
| 89 | 0 | EA | 482107076-002 | 64KX1 DRAM, CER. 200 NS | NOTE 4,5 |
| 90 | | | - | 32KX1 DRAM, U, CER. 200 NS | NOTE 4,5 * |
| 91 | | | - | 32KX1 DRAM, L, CER. 200 NS | NOTE 4,5 * |
| 92 | | | - | 16KX1 DRAM, CER. 200 NS | NOTE 4,5 * |
| 93 | 0 | EA | 482107076-012 | 64KX1 DRAM, PLTIC. 200 NS | NOTE 4,5 |
| 94 | | | - | 32KX1 DRAM, U, PLTIC, 200 NS | NOTE 4,5 * |
| 95 | | | - | 32KX1 DRAM, L, PLTIC, 200 NS | NOTE 4,5 * |
| 96 | | | - | 16KX1 DRAM, PLTIC, 200NS | NOTE 4,5 * |
| 97 | | | - | | |
| 98 | | | - | | |
| 99 | | | - | | |
| 100 | | | - | | |
| 101 | | | - | | |
| 102 | | | - | | |
| 103 | | | - | | |
| 104 | | | - | | |
| 105 | | | - | | |
| 106 | | | - | | |
| 107 | | | - | | |
| 108 | | | - | | |
| 109 | | | - | | |
| 110 | | | - | | |

ENG CHG: REV | CHG NO: SEE SHEET 1 | DATE | APPR

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APPROVED BY: DATE:

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SIZE A | BILL OF MATERIALS NO. 980109405-000 | SH 5 OF 5