PRELIMINARY DATA: SEPTEMBER 1974

IMP-4A/521D MOS/LSI control and read only memory unit (CROM) for 4-bit microprocessors

general description

The IMP-4A/521D Control and Read Only Memory Unit (CROM) is a member of a new family of microprocessor devices, and is a monolithic MOS/LSI circuit utilizing standard P-channel, enhancement mode, silicon gate technology. It provides read only microprogram storage and control logic and is designed for use with the Register and Arithmetic Logic Unit (RALU) and the 4-Bit Interface Logic Unit (FILU). The CROM provides storage for 100 microinstructions of 23 bits each. Circuitry is also provided for program sequencing, subroutine execution, and translation of microinstructions into RALU commands. Multiple CROM's may be used to provide expanded capability.

The CROM operates on +5V and −12V supplies with 4-phase, non-overlapping clocks. Signals are MOS level.

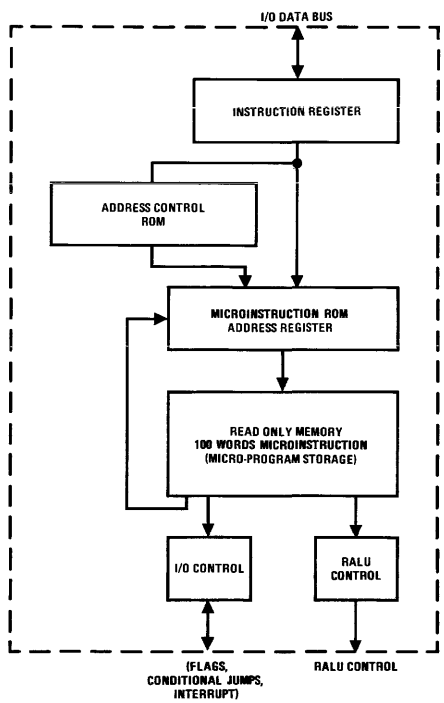
features

■ Standard supplies	+5V, −12V
■ Standard package	24 pin DIP
■ High speed	500 kHz
■ Microprogrammable	100 words
■ Subroutine capability	Return address register
■ Expandable	Up to 4 CROM's

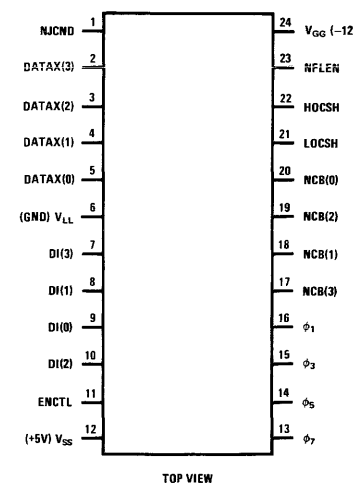
applications

- Standard 4-bit instruction set
- Expansion of standard instruction sets
- Custom instruction sets
- Custom application control programs

block and connection diagrams



Dual-In-Line Package



TOP VIEW

B15M94/Printed in U.S.A.

absolute maximum ratings (Note 1)

All Input or Output Voltages with Respect to Most Positive Supply Voltage (V_{SS})	+0.3V to −20V
Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1W Maximum at +25°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (T_A = 0°C to +70°C; V_{SS} = +5V ±5%; V_{GG} = −12V ±5%, V_{LL} = GND)

PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNITS
Logic "1" Input (MOS) ($V_{IN(1)}$)		V_{SS}−1.0			V
Logic "0" Input (MOS) ($V_{IN(0)}$) (Note 4)				V_{SS}−7.0	V
Input Leakage Current (MOS) (I_L)	V_{IN} = +5V to −12V			2.0	μA
Logic "1" Output (MOS) ($V_{OUT(1)}$)		V_{SS}−0.6			V
Logic "0" Output (MOS) ($V_{OUT(0)}$) (Note 5)				V_{SS}−8.0	V
DI(0) – DI(3) Input Capacitance (C_S) DATAX(0) – DATAX(3)	V_{IN} = V_{SS}, f_T = 500 kHz		5.0	10	pF
NJCND, ENCTL, LOCSH, HOCSH Input Capacitance	V_{IN} = V_{SS}, f_T = 500 kHz		11	14	pF
Clock Input Capacitance (C_C)	V_{IN} = V_{SS}, f_T = 500 kHz	30	40	60	pF
Clock "1" Level ($V_{\phi(1)}$) (Note 3)		V_{SS}−1.0		V_{SS}	V
Clock "0" Level ($V_{\phi(0)}$)		V_{GG}		V_{GG}+1.0	V
Load Capacitance for DI(0), (1), (2), (3) (C_L)				25	pF
HOCSH, LOCSH				22	pF
ENCTL, NFLEN				20	pF
NCB(0), (1), (2), (3)				50	pF
Power Dissipation (P_D) (T1 – T8 Equal Width)	f = 500 kHz		700	950	mW

Note 1: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

Note 2: Max. = most positive; Min. = most negative.

Note 3: Clamp diodes and series damping resistors may be required to prevent clock overshoot.

Note 4: V_{SS}−5.0 for DI(0) – (3), DATAX(0) – (3), and NJCND.

Note 5: V_{SS}−6.0 for DI(0) – (3).

FUNCTIONAL DESCRIPTION

A block diagram of the Control and Read Only Memory (CROM) chip is shown in *Figure 1.* The ROM provides storage for 100 23-bit microinstructions. This is sufficient to implement a macroinstruction set comparable to many mini-computers, or to provide a control program directly in microcode. In cases where larger programs are desired, up to four CROM chips may be used in a single processor.

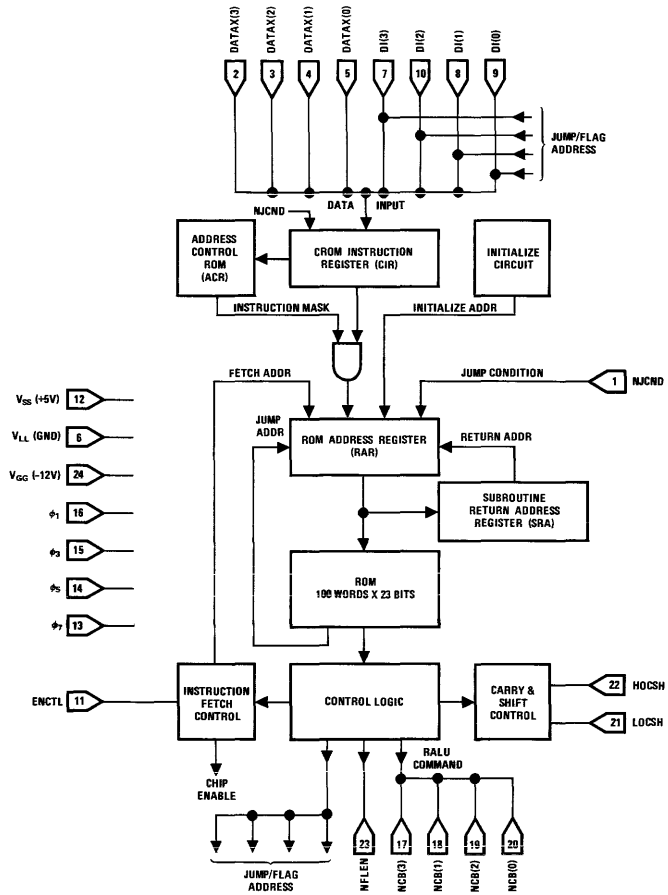
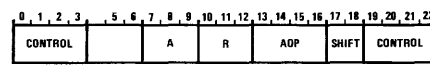


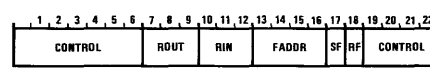
FIGURE 1. CROM Block Diagram

TABLE I. IMP Microinstruction Word Formats

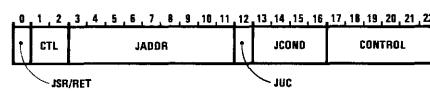
ARITHMETIC INSTRUCTIONS



I/O INSTRUCTIONS



JUMP INSTRUCTIONS



A simplified version of the ROM bit functions is indicated in Table I. For explanation purposes the functions have been divided into three classes. The class is specified by the control fields, which are also used for special functions. The arithmetic class allows specification of the registers to be loaded on the A and B-bus of the RALU, the ALU operation to be performed (AOP), a shift operation and the register to be loaded from the R-bus. The I/O class provides fields for addressing a register for data output and a register for data input as well as setting (SF) and/or resetting (RF) one of 16 control flags to indicate the type of I/O transfer. The microinstruction jump class provides a 9-bit address field, selection of up to 8 jump conditions (JCOND), an unconditional jump command (JUC) and specification of a subroutine jump or return (JSR/RET). (The jump condition and flag logic is provided off the chip to save pins.)

The ROM has 9 programmable address inputs which come from the ROM address register (RAR). The RAR is a 9-bit synchronous counter with parallel load inputs which normally counts sequentially through ROM addresses. When a program branch is desired the contents of the RAR may be altered by parallel loading from one of several sources. One possibility is to load an address specified by the microcode stored in the ROM. This may be either a conditional or unconditional branch. Conditional branches are controlled by the jump condition input (NJCND). An external jump condition multiplexer drives NJCND and may apply one of up to 16 conditions to the input. The condition applied is selected by the jump/flag address which is sent out over pins DI(0), (1), (2), and (3) at the beginning of each microinstruction cycle. The RAR may also be loaded from the subroutine address register (SRA). This register is loaded from the RAR if a jump to subroutine is specified by the microcode. The incremented SRA is loaded back into the RAR when a return from subroutine is executed. There are two programmable addresses which may be loaded into the RAR. These are the addresses of the instruction fetch routine, which will be loaded into the RAR when a new macroinstruction is to be "fetched" from the system memory, and the address of the initialize routine, which will be loaded when the power is turned on. The final method of loading the RAR is from the CROM instruction register (CIR). This register is loaded from external memory, or an I/O device, with a macroinstruction to be executed. The CIR is loaded into the RAR as commanded by the microprogrammed "fetch" routine. The CIR bits are masked by the outputs of the Address Control ROM (ACR) before being loaded into the RAR. The masking is used to set bits which are not part of the instruction opcode to zero. There are 12 masks available; the one used is selected by the current contents of the CIR (i.e., each instruction selects its own mask). The selection code and masks are both programmable.

The HOCSH and LOSCH (High and Low Order Carry/Shift) signals are used to implement carry and shift operations. LOCSH is used to provide a low order carry in for the ALU. This is useful for incrementing, two's complementing a number or emitting (serial) bit patterns to the ALU. During circular shift operations HOCSH and LOCSH are tied together by an internal transistor, allowing shifts to propagate between the most and least significant ALU bits. In the case of open shifts the HOCSH and LOCSH pins provide trailing zeroes to be shifted into the ALU.

Control information from the CROM to the RALU is sent over four time-multiplexed lines [NCB(0), (1), (2), and (3)]. Four 4-bit commands are sent each microinstruction cycle. These lines go to the RALU. The enable control pin (ENCTL) and the chip enable circuitry are used for systems having more than one CROM (for microprograms with more than 100 words).

Details of signal functions and timing are presented in the following sections. Positive true logic signals are used ("1" = more positive voltage, "0" = more negative voltage). Signal names beginning with N are complemented signals.

FUNCTIONAL DESCRIPTION OF SIGNALS

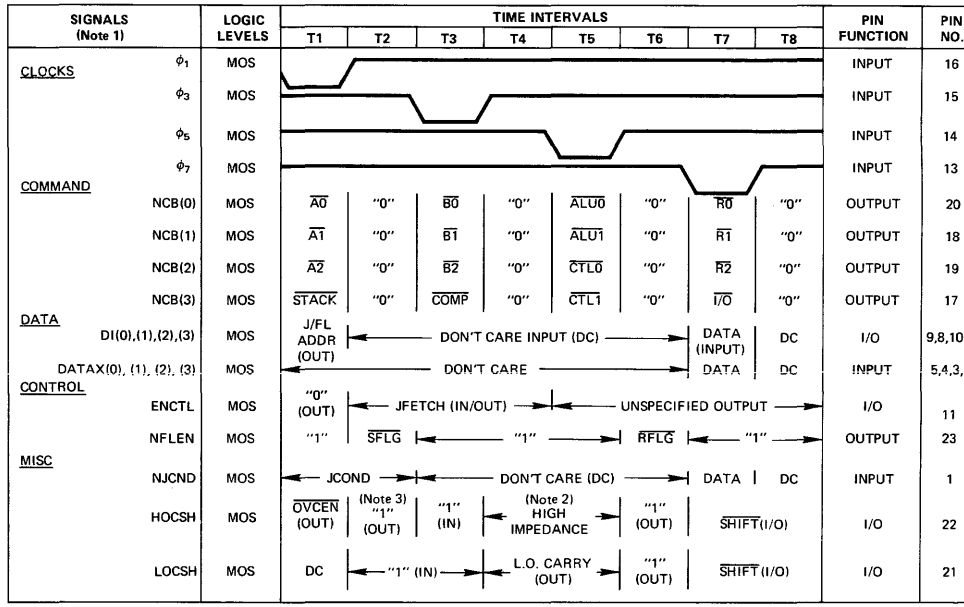
The timing diagram *(Figure 2)* is divided into 8 time intervals (T1 – T8) based on the 4-phase non-overlapping clocks. The clocks inputs have MOS levels of +5V and −12V and occur during the odd time intervals. Thus phase 1 is a logic "0" (−12V) during T1 and a logic "1" (+5V) during T2 – T8.

Commands

The command outputs to the RALU occur on pins 20, 18, 19, and 17 which correspond to command bits NCB(0), (1), (2), and (3). The command outputs are complemented MOS signals and are multiplexed over the 4 odd time intervals in each cycle (T1, T3, T5, T7). Outputs are driven negative to logic "0" during the even time intervals. The command functions for each bit are indicated in the diagram. During T1, the three least significant command bits specify the address of the register to be loaded onto the A-bus, Registers R1 – R7 are addressed by binary values of 1 – 7 respectively. A value of zero causes the A-bus to be set equal to zero. The fourth command bit is used to enable stack operations. If NCB(3) is at a logic "1" (most positive level) no stack operation occurs. If it is at a logic "0" stack operations are enabled, but will only occur if the A or R-bus address is zero. If the A-bus address is zero the stack will be pulled onto the A-bus. If the R-bus address is zero, the R-bus will be pushed onto the stack.

During T3 the three least significant bits specify the address of the register (R1 – R7) to be loaded on the B-bus. The most significant bit specifies that the A-bus is to be complemented when it is transferred to the IA-bus. During T5 NCB(1) and NCB(0) specify the ALU operation to be performed. while NCB(3) and NCB(2) are used to specify control functions.

During T7 the three least significant bits specify the address of the register (R1 – R7) to be loaded from the R-bus. The most significant bit specifies that the R-bus is to be set equal to the output of the I/O multiplexer rather than the shifter.



Note 1: A positive true logic convention is used for all signals except clocks. Signal names beginning with N are complemented signals.

Note 2: HOCSH at T4 and T5 is in the TRI-STATE high impedance output mode of CROM load drivers.

Note 3: "1" (OUT) means CROM is driving this node to the logic "1" level during the defined interval. For I/O lines the logic state is defined as "in" or "out." Input or output nodes are defined only as "1" or "0."

FIGURE 2. CROM Timing Diagram

Data

Instructions to the CROM are transferred over the data input lines [DI(0) – DI(3) and DATAX(0) – DATAX(3)] into bits 0 – 7 of the CIR. (Bit 8 of the CIR is loaded from the NJCND input.) Data input occurs at T7. Signal lines DI(0) – DI(3) are also used to output a 4-bit address to the control flags and jump conditions. This address output becomes valid during T1 and is stored by the FILU.

Control Signals

The enable control (ENCTL) is a "wired OR" signal line required for operation of multiple CROM's. It provides a logic "1" output at T2 – T4 whenever a branch to the instruction fetch routine occurs, and responds to a logic "1" input at T2 – T4 by executing a branch to the instruction fetch routine and disabling if the instruction has not been implemented in that particular CROM. The flag enable (NFLEN) control output is used to set or reset flags addressed by DI(0) – DI(3) at T1 of the current cycle. A logic "0" output at T2 specifies setting of the addressed flag while a logic "0" output at T6 specifies resetting.

Miscellaneous Signals

The jump condition input line (NJCND) is used to input conditional branch information at T1 and T2 as specified by the jump condition addressed by DI(0) – DI(3) at T1. If the input is a logic "0" and a conditional branch has been specified for the current cycle, a branch will occur. The NJCND input is also used to load data into CIR(8) at T7.

The high and low order carry/shift lines (HOCSH and LOCSH) are used to provide shift and carry information to the RALU. If a circular shift has been specified, HOCSH and LOCSH are connected together on the CROM during T7 and T8 by a low on-resistance MOS transistor switch. For the case of a circular left shift HOCSH serves as an input driven by the RALU and LOCSH serves as an output to the RALU and follows the voltage input at HOCSH. The direction of data transfer is reversed for circular right shift. In the case of open ended shifts the CROM output (LOCSH for left shift and HOCSH for right shift) provides a logic "1" to the RALU (since the shift data is complemented this will provide a trailing "0" for the shift operation) and ignores the shift input data from the RALU. The carry input to the RALU is provided by LOCSH at T4 and T5. The overflow and carry flags on the RALU are enabled by the output of HOCSH at T1. A logic "1" input is required to HOCSH at T3. This line is precharged to a logic "1" at T2. A logic "1" input is required for LOCSH at T2 and T3. The LOCSH input will be precharged to a logic "1" at T1 when connected to CSHO of the RALU.

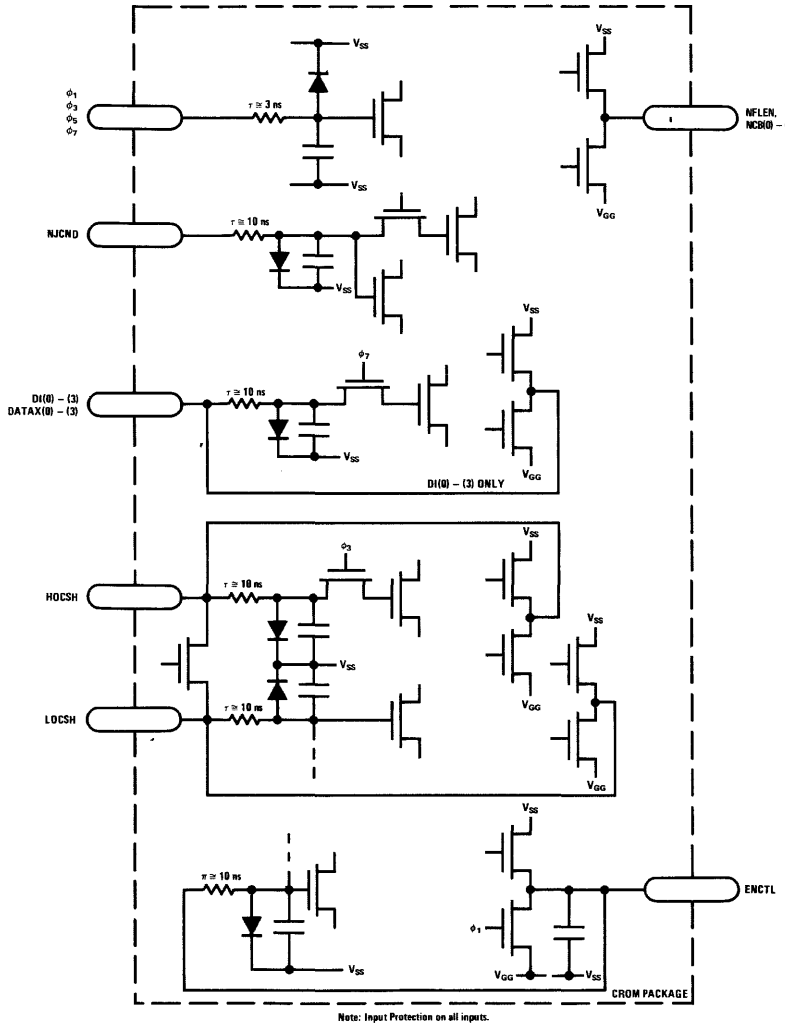
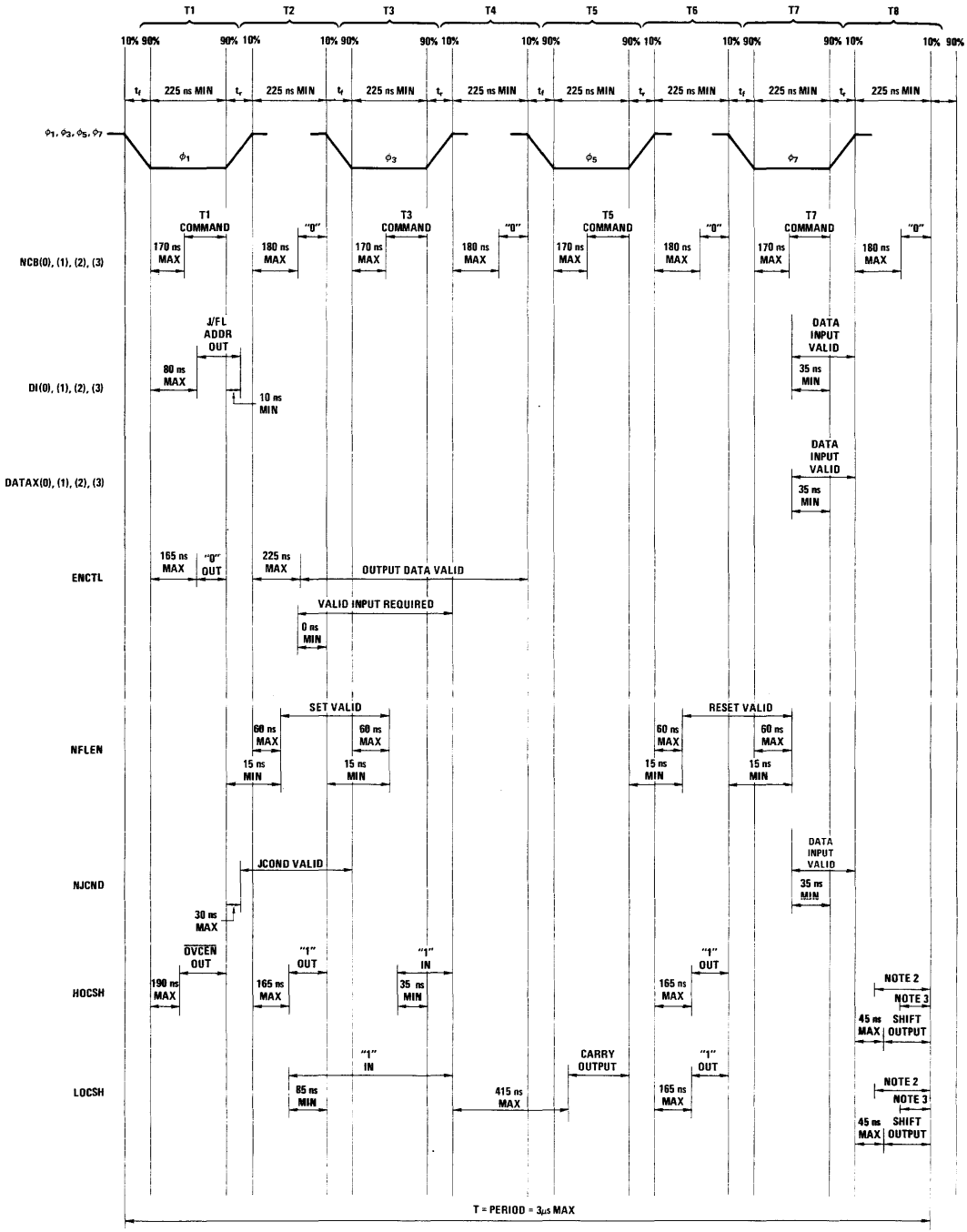


FIGURE 3. CROM Driver and Receiver Buffer

SIGNAL TIMING SPECIFICATIONS

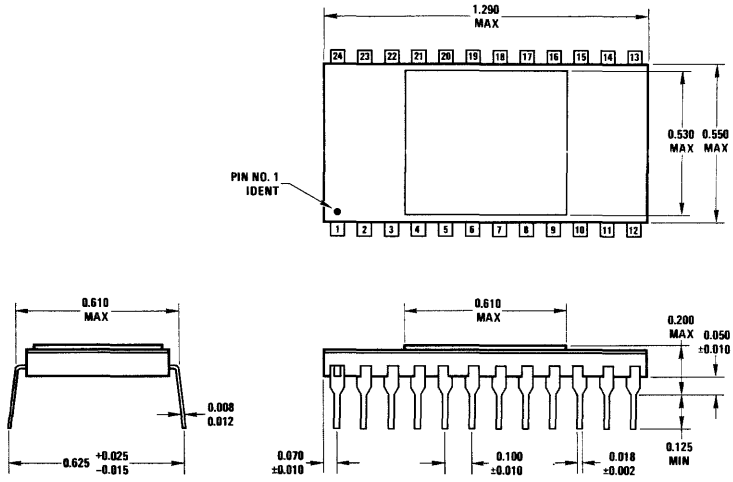
The timing specifications for all CROM signals are shown in *Figure 4.* These specifications apply over the complete range of recommended operating conditions. Time intervals are defined with respect to the 10% and 90% points of the four MOS clock inputs. The command outputs on the NCB bus become valid within the first 85 ns of the odd time intervals. These lines are driven to a logic zero within the first 85 ns of the even time intervals. The jump condition and flag address outputs on DI(0) – DI(3) become valid within the first 80 ns of T1 and remain valid for at least 10 ns after the 90% point at the end of T1. Data inputs to all DI lines must be valid for at least the last 35 ns of T7 and must remain valid until the 10% point at the start of T8. Timing for the remaining signals is similar. (Note that signals may not change state during "valid" time intervals.)



Note 1: t_r and t_f = 100 ns max.
Note 2: Rotate input valid 130 ns min.
Note 3: Rotate output valid 80 ns min.

FIGURE 4. CROM Signal Timing Specifications
(T_A = 0°C to +70°C, V_{SS} = +5V ±5%, V_{GG} = −12V ±5%, V_{LL} = GND)

physical dimensions



Cavity Dual-In-Line Package (D)

ordering information

The basic CROM device is available with a variety of different microcode masks to tailor it to different applications. The mask versions defined so far include:

IMP-16A/521D	16-Bit Standard Instruction Set
IMP-16A/522D	16-Bit Extended Instruction Set
IMP-8A/520D	8-Bit Standard Instruction Set
IMP-4A/521D	4-Bit Standard Instruction Set

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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