Design Guide for an Ethernet Adapter Using the DP83907 AT/LANTIC™ II

National Semiconductor
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About This Guide

This guide describes the DP83907 AT/LANTIC™ II Evaluation Board and the underlying hardware design considerations

1.0 INTRODUCTION

The DP83907 AT/LANTIC II Evaluation Board provides system designers a simple method of interfacing PC ISA (Industry Standard Architecture) bus based system to Ethernet. This Evaluation board provides complete 16-bit 10 Base-T, 10Base2 and 10Base5 Ethernet solutions in a half-size jumperless ISA adapter card. It is IEEE 802.3 compliant and NE2000/NE2000*Plus* I/O mode compatible.

Built into the DP83907 is an Ethernet Media Access Control unit, a Manchester Encoder/Decoder, Twisted Pair Transceiver, an AUI, ISA bus, EEPROM and SRAM interfaces. It uses the EEPROM to store the board's configuration and IEEE node address and two 8kx8 SRAMs to buffer transmit and receive packets. The 10Base2 network interface is implemented with the addition of a 1:1 pulse transformer, a DC-DC Converter and a DP8392 Coaxial Transceiver Interface (CTI). Refer to the block diagram in *Figure 1*.

2.0 EVALUATION BOARD FEATURES

- Designed with the DP83907.
- Jumper-less design.
- Half-size PC AT adapter card.
- NE2000 / NE2000Plus I/O mode compatible.
- 10Base2 connectivity.
- 16 kByte SRAM packet buffer.
- Serial EEPROM stores the board's configuration and IEEE node address.
- Serial EEPROM can be programmed in-situ.
- Boot ROM socket to allow disk-less boot from NetWare, Lan Manager and other network operating systems.
- 8 interrupts.
- Status LEDs for transmit, receive and collision.

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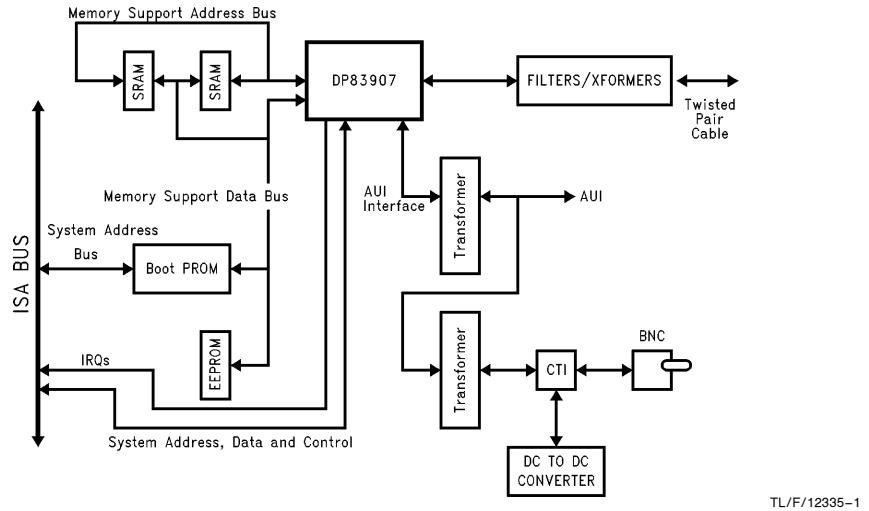

FIGURE 1. DP83907EB Block Diagram

3.0 HARDWARE DESIGN CONSIDERATIONS

This section describes the signal interfaces with the DP83907 in designing this Evaluation Board.

3.1 Crystal and Oscillator

The DP83907 has been designed to operate with either a crystal or an oscillator module. The Evaluation Board comes assembled with the crystal option. The crystal should conform to the following specifications.

AT cut parallel resonance crystal

Series resistance $\leq 40\Omega$

Specified load capacitance $\leq$ 20 pF

Accuracy: 50 ppm

Typical load: 50 μW–75 μW

Note, the X2 pin is not guaranteed to provide a TTL compatible logic output and should not be used to drive external logic.

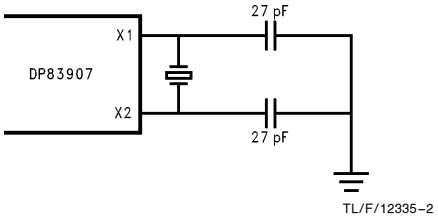

FIGURE 2. Crystal Circuit

If an oscillator module is used, its output should be connected directly to X1, while X2 is left unconnected. The load capacitors should not be used. The oscillator clock should be :

TTL or CMOS output with a 0.01% freq. tolerance
40%–60% duty cycle

3.2 ISA Bus Interface

The DP83907EB can be used in 8- or 16-bit ISA slots. 8- or 16-bit mode is determined by MSA9 at reset. For an adapter card this pin can be used to automatically detect if the card has been plugged into an 8- or 16- bit slot by connecting MSA9 via a 10 kΩ pull-up resistor to V_{CC}. When connected to a 16-bit slot MSA9 will be pulled high enabling 16-bit mode. When plugged into an 8-bit slot, MSA9 will be floating enabling 8-bit mode.

For applications requiring 8-bit only interface, MSA9, SD8-15, /IO16 should be left open.

3.3 Memory Support Interface

The Memory Support Interface is used by the DP83907's local DMA and auto-configuration. This includes the SRAMs and the EEPROM. *Figure 1* shows how the SRAMs and EEPROM are connected to the Memory Support Bus.

On power up, MSA10 must be pulled high to load the EEPROM contents to its internal registers and make them accessible by software. The two 8kx8 SRAMs are used as receive and transmit packet buffers during network data exchanges.

3.3.1 Buffer SRAM

The two SRAMs provide 8k words (16-bit) of memory for the DP83907 to buffer received and transmit packets. For an 8-bit-only interface, only one SRAM is needed with the data bus connected to MSD0-7.

For a standard ISA bus configuration, 100 ns SRAMs or faster should be used, Details of how to calculate SRAM speeds can be found in Ref. [3].

3.3.2 EEPROM

The DP83907 uses its EECS and MSD0-2 pins for accessing the serial EEPROM (NM93C06). MSD0-2 serve as DO, DI, and SK respectively.

The EEPROM is normally read automatically upon power-on reset. One can modify its content by software thereafter.

There is a possibility that a randomly programmed EEPROM may cause the host system to hang. If this happens, Jumper J2 can be installed (MSA10 pin pulled to GND). This will disable the EEPROM from loading and the DP83907 will initialize to the default settings. The EEPROM can then be correctly programmed by either of the two methods described in section 3.6.2.

3.4 Boot ROM

A boot ROM allows the PC to load the operating system from a server on the network without needing a disk drive on the PC (Diskless Workstation). Boot ROMs are available from network operating system vendors or from third parties.

The DP83907EB is supplied with an empty boot ROM socket. Boot ROM sizes of 8kB, 32kB and 64kB are supported. It can be located at particular addresses between C0000h and DFFFFh by programming configuration register C bits 0-3 ''BPS0-3''. For addresses refer to Reference [1].

The boot ROM address lines must be connected directly to the ISA Bus.

The boot ROM data lines are connected to the DP83907's MSD bus. When the system reads within the selected memory area, the DP83907 reads the data in through MSD0-7 and drives it onto the system data bus. The DP83907 supplies the chip select to the device. See *Figure 3*.

For a standard ISA bus configuration a 250nS ROM or faster should be used. Details of how to calculate boot ROM speeds can be found in Reference [3].

3.5 Interrupt and Status LEDs

There are eight interrupt request pins on the DP83907, namely IRQ3–5, IRQ9–12 and IRQ15. The operation of these outputs are determined by configuration register A. The DP83907 has only one Interrupt mode. Configuration Register A controls which one of the 8 interrupt lines will be driven, the others are TRI-STATED. The interrupt outputs should be connected to the following ISA interrupt lines, in the order given, to maintain NE2000 Architecture compatibility: 3, 4, 5, 9, 10, 11, 12 and 15.

Table I. Direct Drive Interrupt Assignment

DP83907	ISA Bus
IRQ3	IRQ3
IRQ4	IRQ4
IRQ5	IRQ5
IRQ9	IRQ9
IRQ10	IRQ10
IRQ11	IRQ11
IRQ12	IRQ12
IRQ15	IRQ15

The configuration register A is used for interrupt selection. Bits 3, 4, 5 are set in the following manner for different interrupt lines:

Table II. Output Interrupt Assignment

DP83907			ISA Bus
5	4	3	
INT2	INT1	INT0	IRQs
0	0	0	IRQ 3
0	0	1	IRQ 4
0	1	0	IRQ 5
0	1	1	IRQ 9
1	0	0	IRQ 10
1	0	1	IRQ 11
1	1	0	IRQ 12
1	1	1	IRQ 15

Status LEDs

These pins are open-drain, active low outputs and serve as $\overline{\text{ACT\_LED}}$, $\overline{\text{GDLNK\_LED}}$ and $\overline{\text{COL\_LED}}$ respectively. The maximum sinking current of these outputs are 24 mA. The current limiting resistors should be chosen so that this requirement is not violated. The LED circuit of the DP83907EB is shown in *Figure 5*.

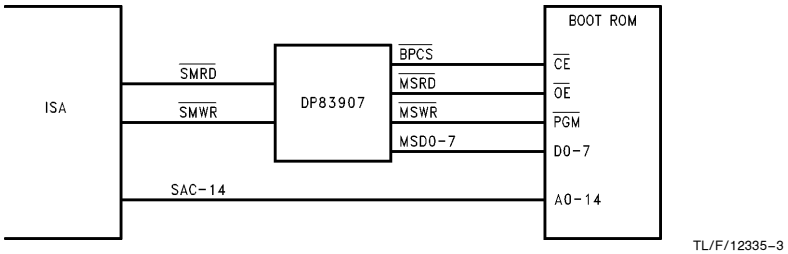

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FIGURE 3. Boot ROM Interface

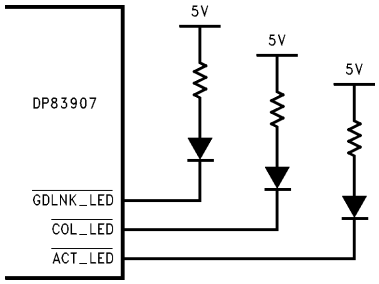

FIGURE 5. LED Circuit

3.6 Configuration

The DP83907 has three configuration registers A, B and C; one signature register and a PROM store register array. All these registers must be properly initialized before the DP83907 can be operational. Table 3–5 may assist you in this task. Note that a full description is given in Reference [1].

Table III. Configuration Registers

Config A Register

Bit	Symbol	Use
0–2	IOAD0–2	Select IO address
3–5	INT0–2	Interrupt
6	FRd/Wr	Fast read/write
7	RES	Reserved (must be zero)

Config B Register

Bit	Symbol	Use
0–1	PHYS0–PHYS1	Physical Layer Interface
2	GDLINK	GOOD LINK
3	IO16CON	IO16 bug fix enable
4	RES	Reserved (must be zero)
5	BE	Bus Error Status
6	BPWR	BOOT PROM Write
7	EELOAD	Enable Loading EEPROM

Config C Register

Bit	Symbol	Use
0–3	BPS0–3	Boot ROM addr and size
4	RES	Reserved (must be zero)
5	RES	Reserved (must be one)
6	RES	Reserved (must be zero)
7	SOFEN	Config Reg Access Disable

Table IV. Signature Register

Bit	Symbol	Use
0–3	REV0–3	DP83907 Identity (1000)
4	EEPR	Enable EEPROM In-situ Program
5–7	SIG5–7	Board Revision (Note 1)

Note 1. This reflects the trapping state of MSA11-13, which can be fixed by manufacturers for board revision identification.

3.6.1 Default Configuration

During power-on reset, the DP83907 loads configuration registers A, B and C and bits 5–7 of the signature register from the memory support bus. Subsequently, the DP83907 reads the first 7 words from the EEPROM and maps them into its PROM store. If in 16-bit mode (MSA9 sampled high on power-on reset), it also reads the next word in the EEPROM and appends this. If in 8-bit mode (MSA9 floating), it skips a word, then reads and appends the next word. Mapping from the EEPROM onto the PROM store is shown in the DP83907 data sheet. The EEPROM should be programmed according to Table 5 for NE2000*Plus* compatibility.

If the MSA10 pin is sensed high, the last two words of the EEPROM are also loaded. Configuration registers A, B and C are re-initialized with the EEPROM content. Hence, a jumper-less solution can be achieved. If the last byte read from EEPROM is 73H, programming in-situ is not allowed. Section 3.6.2 will elaborate more on this.

Table V. EEPROM CONTENTS (NM93C46/NM93C06)

	D15	D0
0FH 3FH (Note 1)	73H	Config Reg. C
0EH 3EH (Note 1)	Config Reg. B	Config Reg. A
09H–0DH	Not used	Not used
08H	42H	42H
07H	57H	57H
06H	Not used	SUM (Note 2)
05H	Driver ID (Note 3)	0DH
04H	H/W Feature (Note 4)	00H
03H	00H	00H
02H	E'net Addr 5	E'net Addr 4
01H	E'net Addr 3	E'net Addr 2
00H	E'net Addr 1	E'net Addr 0

Note 1. If an NM93C46 EEPROM is used then addresses 0FH and 0EH need to be changed to 3FH and 3EH respectively.

Note 2. This field contains the sum of the first 6 words (00H–05H).

Note 3. Novell Driver ID is 01H.

Note 4. This field contains the hardware features of the physical media. The bit 0, 1, 2 should be set respectively for the twisted-pair, thin Ethernet and thick Ethernet.

3.6.2 Configuration Modification

For an implementation using jumpers, one can change the jumper setting on the DP83907's memory support bus. This will effectively modify the DP83907's configuration upon power up.

For a jumper-less solution one can program the DP83907's configuration registers A, B and C. Special procedures must be followed as listed in Table 6.

Table VI. Config Registers Access

Configuration Registers	Read/Write Requirements	
	Read	Write
A	Page 0 of NIC's registers selected	Preceded by a read on Config A
B	Page 0 of NIC's registers selected	Preceded by a read on Config B
C	Page 0 of NIC's registers selected by 3rd consecutive read of Config A	Preceded by 3rd consecutive read of Config A

To make it a permanent change, one must write the new configuration into the EEPROM. It can be done by either of the two methods described below.

(1) Indirect Write to EEPROM

Three bytes of the EEPROM, storing configuration registers A, B and C values, can be modified by a special pseudo code. EELOAD acts as load enable and must be set to one. The DP83907 serializes the data and writes them into the EEPROM. The EELOAD bit (Bit 7 of configuration register B) will be reset by the DP83907 when it completes the load EEPROM operation. It has full control on all the interface signals EECS, DI and SK. Note that this algorithm does not change the configuration registers directly, i.e., the new state only appears on the next power up.

```
EEPROM-LOAD( )
    {       Disable Interrupts( );
            Value = Read(Config_B);
            Value = Value AND GDLINK
            Value = Value OR EELOAD
            Write(Config_B, Value)
            Read(Config_B)
            Write(Config_B, Config_for_A)
            Write(Config_B, Config_for_B)
            Write(Config_B, Config_for_C)
            While(Value AND EELOAD)
            {       Value = Read(Config_B)
                    Wait( );
            }
            Enable Interrupt( )
    }
```

In the pseudo code above, interrupt is disabled, GDLINK bit preserved, and the EELOAD bit of configuration B serves as load enable.

(2) In-situ EEPROM programming

If the uppermost byte of the EEPROM does not contain 73H, the EEPR bit of the signature register will be zero, and the entire content of the EEPROM can be modified.

One must first set the EELOAD bit (load enable), and subsequent writes to the data transfer port will have SD1-3 driven onto the EECS, SK and DI pins, allowing users to have full control on writing to the EEPROM.

Similar to the previous case, one must apply a power-on reset for the DP83907 to load the new configuration data from the EEPROM.

With in-situ programmability, manufacturers do not have to pre-program the EEPROM before board assembly. It also provides much more flexibility because the entire EEPROM content can be modified at will.

By programming 73H to the uppermost byte, the EEPROM is protected from further changes, except for configuration register A, B and C, which can still be changed with an Indirect write to the EEPROM.

3.6.3 IO16 mode

In some PCs using certain chip sets, the timing requirements in 16-bit I/O cycle cannot be achieved by the DP83907. As a consequence the host system does not recognize the CHRDY signal and does not insert wait states. The system executes a standard 16-bit cycle and deasserts $\overline{IORD}$ or $\overline{IOWR}$ even if the DP83907 is not ready. The DP83907 incorporates logic to detect this condition, Configuration register B bit 5 ''BE'' is set to ''1'' if the condition is detected. This can be used by software to warn the user that a fix is required.

By setting bit 3 of configuration register B, the DP83907 enters IO16 mode. It generates $\overline{IO16}$ after $\overline{IORD}$ or $\overline{IOWR}$. The offending chip sets are fooled into accepting 8-bit timing for CHRDY, while still transferring 16 bits correctly.

3.6.4 Jumperless Operation Support

One of the biggest problems in installing new adapters in a PC is not knowing the available resources within that machine. The DP83907 software configuration overcomes that problem. The conflicts possible in the I/O base selection can be overcome by a special mode for software configuration of the I/O base address. By using this mode, and by using the configuration storage capability of the EEPROM, a fully software configurable design on the ISA bus can be realized without address conflict problems.

This mode is invoked by having the DP83907 default to jumper-less software configuration option in the I/O base selection. This mode enables configuration register A to be mapped to address location 278H which is defined to be a printer port's data register. If software writes to this location four consecutive times, on the fourth write the DP83907 will load the data written into the I/O address bits of Configuration Register A. This data should set the I/O base address to a known conflict-free value. The DP83907 can now be configured and operated at the desired base I/O address. If desired, the configuration software could change the EEPROM content to the new values eliminating the need to reconfigure upon each power up. Alternately the software could leave the EEPROM alone and execute the configuration using the printer port's data register upon each power up. This configuration scheme will only work once after each power-up. Therefore the user can not enable the DP83907 from reserved mode, change it back into reserved mode and enable it again. A power-on reset must occur between the first time it is enabled from the reserved mode and the second.

3.7 Twisted Pair Interface (TPI)

The Twisted Pair interface is simple, it requires components external to the DP83907 which are pre-emphasis resistors, some capacitors and a transformer/filter module.

3.7.1 ON-CHIP Filters

The on-chip filters are enabled via an external pull-up resistors on MSD12 at configuration. Only an isolation transformer and a few impedance matching resistors are needed for the transmit and receive twisted pair interface.

3.7.2 RTX Resistor

In on-chip filter mode, the value of TPI VOD when measured dirving a 100Ω load may not meet the IEEE-802.3 specification over temperature and process without the use of a resistor of RTX. This does not adversely affect system performance.

An R9 resistor value of 82.5 kΩ (±1%) to V_{CC} is recommended.

- Increasing the valued of this resistor will lower the value of VOD.
- Decreasing the value of this resistor will increase the value of VOD.

3.7.3 Non Cat3 Cable

When using non-Cat3 cable such as type 9, 2 pair, 26AWG cable, the following modification is suggested to ensure optimum operating performance.

- Install a 2200 pF (±10%) capacitor across each 10.5Ω summing resistor, i.e., R11 and R13.
- Relmove any R9 resistor.
- Install a 24.3 kΩ (±1%) resistor from RTX to GND, i.e., R10.

3.8 Attachment Unit Interface (AUI)

The DP83907 can be used with external Medium Attachment Unit (MAU). The interface is via the 15-pin D-type connector and is a direct interface to the DP83907's ENDEC. The DP83907's ENDEC only requires 39.2Ω terminations on receive and collision inputs. The transmit outputs do not require any pull-down resistors.

3.9 UTP/STP Function

The TPI Transceiver supports both shielded (STP) and unshielded twisted pair (UTP) cable. UTP is the default but STP can be enabled during configuration by a pull-up resistor on MSA7 or by setting bit D6 high of configuration register C. In UTP mode TXO+ and TXOD+ are driven and TXO− and TXOD− are TRI-STATED. In STP mode TXO− and TXOD− are driven and TXO+ and TXOD+ are TRI-STATED.

3.10 AUTO-SWITCH Function

The auto-switch function can be enabled at configuration by pull-up resistor on MSA5 or by setting bit D4 high of the configuration register C. When auto-switch is enabled link integrity should also be enabled. It allows the transceiver to switch between TP and AUI outputs. If there is an absence of link pulses the transceiver will switch to AUI mode. Similarly when the transceiver starts detecting link pulses it will switch to TP mode. The switching between modes is done after the current packet has been transmitted or received. If the twisted pair output is jabbering and gets into link fail state then the switch to AUI mode is only done after the jabbering is done including the times it takes to unjab (unjab time). When auto-switching is enabled the THIN output is automatically generated if AUI is selected.

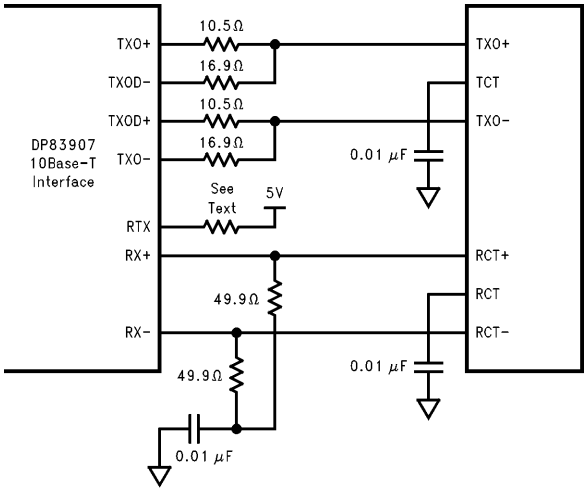

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FIGURE 6. Circuitry to connect the DP83907 to Twisted pair cable with internal filter.

4.0 SOFTWARE SUPPORT

4.1 Configuration and Diagnostics Software

If you are offering a jumper-less solution, the user will require configuration software. The DP83907EB-AT comes with configuration and diagnostics software, called AT5CFG.

AT5CFG will detect and list all the boards installed in the system. The I/O address and interrupt assignment will also be shown. A warning message will appear if there is any conflict in resource allocation.

There are 2 options of saving a changed configuration. Saving a configuration temporarily will render the EEPROM unmodified. Once the system is powered up again the configuration will default to the original settings. Saving the configuration to the EEPROM will permanently store the configuration until another modification is made. The software enable bit (bit 7 of the configuration register C) must be zero for changing configuration register A, B and C by software.

The adapter initialization option will check to see whether a configurable board is present. If so, its configuration parameters will be read and displayed. Otherwise, an error message will be displayed. If the board is non-configurable, the user will be alerted by a warning message. The diagnostic option will do a simple test on cache, interrupt and buffer memory.

The advanced network diagnostic, ''Ping Pong Test'', can be run only after the board is initialized and passes the diagnostic test described above. Two stations are needed, one master and one slave. In order to test both transmit and receive logic, each station should be tested as a master and slave.

4.2 EEPROM in-situ Programming

The software called EEPROM is used to program the Evaluation Board's EEPROM in-situ. There is also a data file holding previous programmed data to facilitate repeated programming. An error message will be prompted if there is no DP83907 present or the programming in-situ feature has been disabled.

4.3 Driver Software

The DP83907 can use all NE2000 drivers and NE2000plus drivers in I/O mode only.

5.0 REFERENCES

1. DP83907 Data Sheet, National Semiconductor
2. DP83905EB-AT AT/LANTIC Evaluation Board AN875, National Semiconductor
3. DP83905EB-AT AT/LANTIC Hardware Users' Guide AN897, National Semiconductor

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