The Design and Operation of a Low Cost, 8-Bit PC-XT® Compatible Ethernet Adapter Using the DP83902

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OVERVIEW

This 8-Bit Ethernet adapter board design is an inexpensive-low part count design that provides PC-XT and PC-AT® compatibles with Thick, Thin, and Twisted Pair Ethernet connectivity. This design provides an 8-bit interface that is compatible with Novell's 8-bit NE1000, while using the DP83902 (ST-NIC™) to interface to twisted pair Ethernet. The ST-NIC also has an AUI interface which allows interface to thick wire Ethernet, or thin wire Ethernet by the addition of the DP8392 Coaxial Transceiver Interface (CTI). The dual DMA (local and remote) capabilities of the ST-NIC, along with 8 kbytes of buffer RAM, and bus interface logic provide a high performance 8-bit interface. The I/O port architecture used in this design isolates the CPU from the network traffic, proves to be the simplest method to interface the DP83902 to a PC system bus.

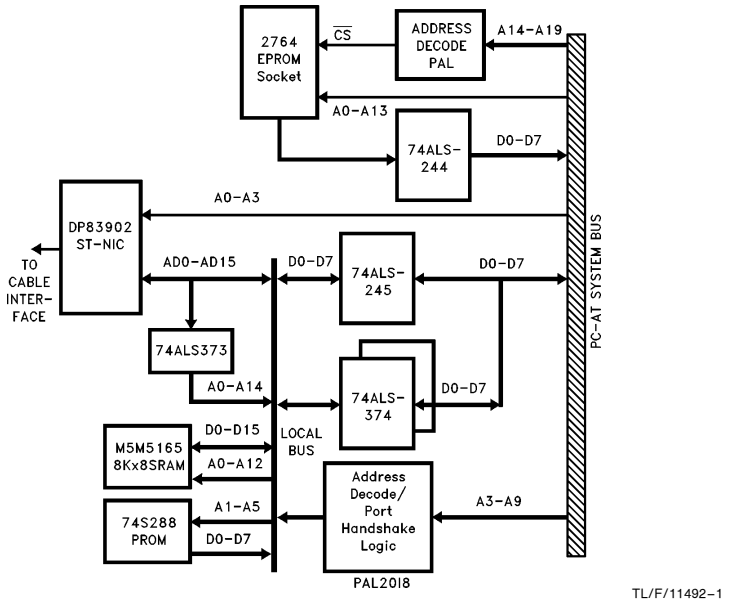
This paper describes the basic design and operation of this 8-bit adapter card, and then follows this with specific design information including the PAL equations and a detailed schematic of the design. For detailed information refer to the schematics at the end of this document.

HARDWARE FEATURES

- Fits in a half-size IBM XT form factor
- Utilizes DP83902 twisted pair network interface controller (ST-NIC)
- 8 kbyte on-board packet buffer
- Simple I/O port interface software compatible with Novell's NE1000 Ethernet adapter
- Interfaces to Thick (10BASE5), Thin (10BASE2), and Twisted Pair (10BASE-T) Ethernet
- Boot EPROM socket

BUS INTERFACE

The block diagram for this design is shown in *Figure 1*. The ST-NIC board as seen by the system appears only to be a block of I/O ports. With this architecture the ST-NIC board has its own local bus to access the board's memory. The system never has to intrude further than the I/O ports for any packet data operation. There are two register/memory maps that describe the card. The first is the I/O register map that describes how the PC's processor accesses the card. The second map is the one that describes how the ST-NIC accesses the on-card memory.



TL/F/11492–1

FIGURE 1. System Bus Block Diagram for 8-Bit Ethernet Card

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I/O Map

The ST-NIC board requires a 32 byte I/O space to allow for decoding the data port, the reset port, and the ST-NIC registers. This is shown in Table I. The first 16 bytes are the ST-NIC registers, the next 16 bytes address the data port and the reset port, which are aliased alternately as shown.

TABLE I. I/O Map in PC-AT

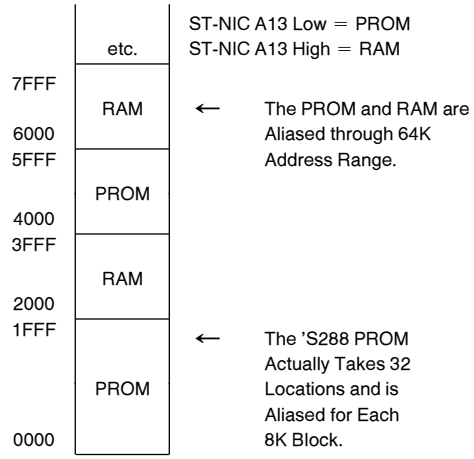
Address Offset	Device Accessed
00h–0Fh	ST-NIC Registers
10h–13h	Data I/O Port
14h–17h	Reset Port
18h–1Bh	Data I/O Port
1Ch–1Fh	Reset Port

Additionally there are three jumpers which define the base addresses for the address map shown in Table I. (See the Jumper Configuration section for details.)

On-Card Memory Map

There are only two items mapped into the local memory space. These two items being the 8k x 8 buffer RAM and the Ethernet ID address PROM. The buffer RAM is used for temporary storage of transmit and receive packets.

TABLE II. ST-NIC's Local Memory Map



The buffer RAM is used for temporary storage of network packet data that is either being transmitted or received. The ID address PROM (74S288 32 x 8) contains the physical address of the evaluation board. Each PROM holds its own unique physical address which is installed during its manufacture. Besides this address, the PROM also contains some identification bytes that can be checked by the driver software. At the initialization of the evaluation board the software commands the ST-NIC to transfer the PROM data to the I/O Port where it is read by the CPU. The CPU then loads the ST-NIC's physical address registers. The following table shows the contents of the PROM.

TABLE III. PROM Contents

PROM Location	Location Contents
00h	Ethernet Address 0 (Most Significant Byte)
01h	Ethernet Address 1
02h	Ethernet Address 2
03h	Ethernet Address 3
04h	Ethernet Address 4
05h	Ethernet Address 5
06h–0Dh	00h
0Eh, 0Fh	57h
10h–15h	Ethernet Address 0–5
16h–1Dh	Reserved
1Eh, 1Fh	42h

EPROM INTERFACE

An EPROM socket is provided so that the end user may add an EPROM to the system. This EPROM would normally contain a program and a driver to enable the PC-AT to be booted up (Operating System loaded) from a designated network server. The ICs necessary to interface the EPROM to a 16L8 (PAL), and a 74ALS244 (buffer). The PAL decodes SA14–SA19, along with system memory read, in order to generate the EPROM enable signal. The '244 provides buffering of the EPROM's data bus to the PC's bus.

General Bus Interface Operation

For receiving of packets, the ST-NIC first starts to receive a packet and checks the address of this packet. If the address corresponds to the address for this card, then the data is received by the ST-NIC. The ST-NIC utilizes it's Local DMA channel to buffer the packet into the next available area of the 8k buffer RAM. As each packet is received the ST-NIC's local DMA will buffer it to the next available location in memory. After each packet is buffered the ST-NIC will generate and interrupt to the CPU. If a packet that has an error is loaded into RAM, the ST-NIC will reject the packet and reclaim the memory space that the packet occupied.

Upon recognition of the receive interrupt the CPU should then program the ST-NIC's Remote DMA to read the packet into the I/O port consisting of the two back-to-back 74ALS374s (see *Figure 1*). As the ST-NIC's Remote DMA does this the CPU handshakes with the DMA to read each byte from the I/O Data Port and store it in the PC's main memory. This is repeated until the packet has been completely transferred.

For packet transmission, the system CPU first programs the ST-NIC's Remote DMA to receive a packet from the system into a predetermined area of the card's buffer RAM. The CPU and the ST-NIC then handshake while the data is sent through the I/O data port.

Once the transmit packet is completely assembled into the local card RAM, the ST-NIC is then programmed to transmit the packet out onto the network. The ST-NIC then reads the transmit data using its Local DMA channel, and then follows the CSMA/CD protocol to transmit the data. When the transmission is complete an interrupt is generated, and the CPU can check the status of the transmit to ensure proper transmission did occur.

NETWORK INTERFACE

The evaluation board supports three physical media interfaces options: Thick Ethernet, Thin Ethernet, and Twisted Pair. The block diagram for these interfaces can be seen in *Figure 2*. A single jumper selects between the ST-NIC's Attachment Unit Interface (AUI) and its 10BASE-T interface. When the AUI is selected a second jumper selects the Thin Interface or the AUI connector. This second jumper shorts/opens the power supply to the transceiver. The AUI interface provides connectivity to an external transceiver which typically connects to Thick Ethernet cable.

The ST-NIC has an integrated 10BASE-T interface so that all that needs to be added are the equalization resistors, and an integrated filter module such as the Valor FL1012.

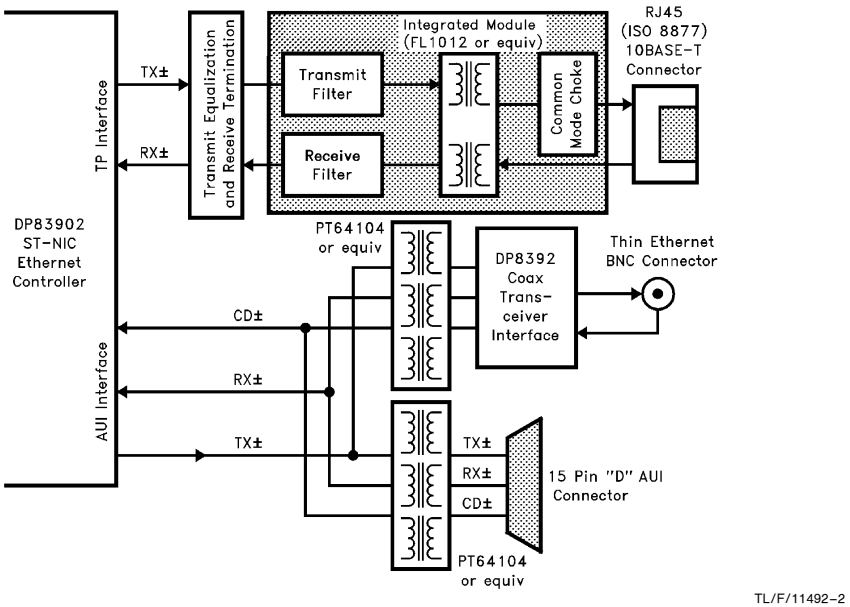
The Thin Ethernet interface is a little more complicated. This section includes a pulse transformer and a DC-DC Converter (Valor PM7102 or equivalent) to provide the required isolation, and the DP8392 Coax Interface and a few discrete components. The input power to the PM7102 is enabled via the jumper to enable disabling of this interface.

JUMPER CONFIGURATIONS

On the DP83902EB-AT ST-NIC AT board, there are nine jumpers as grouped in the one block in the component layout shown in *Figure 3*. The following pages will explain how to configure these jumpers, and what they do.

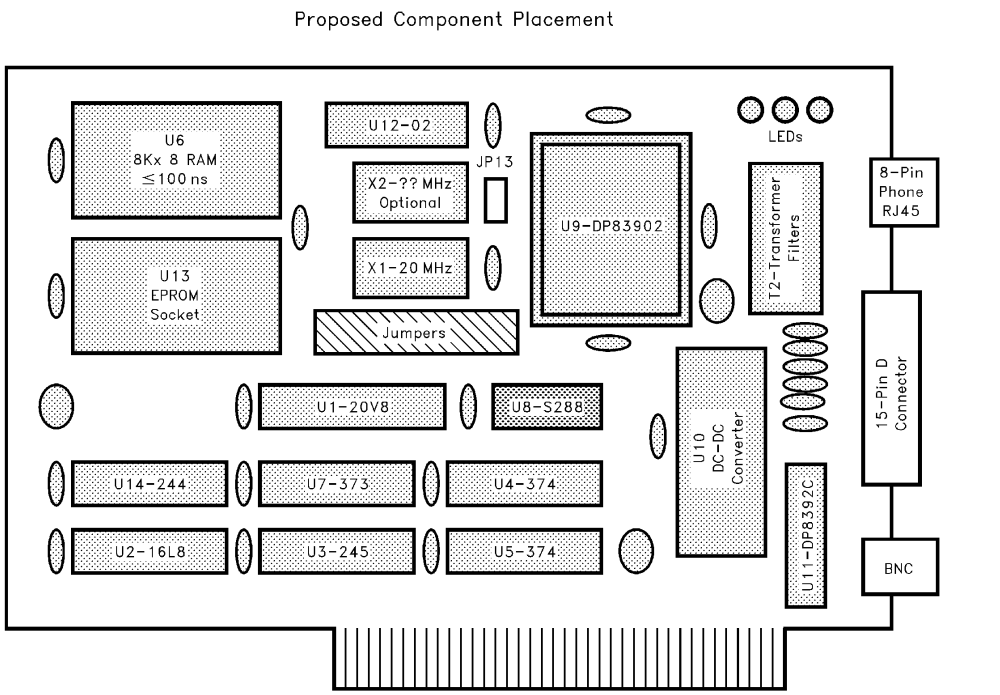
Physical Interface

There are a number of jumper options provided in this design to enable utilizing some of the ST-NIC's pin programmable options. Most of these are set for the normal default and should not have to be changed (in fact most are only provided for experimentation purposes). These jumpers are JP3, JP5, and JP6. JP4 is provided to enable experimentation with different bus clocks should a designer wish. This option is not useful for general operation and the default to use the 20 MHz network clock would normally be used.



TL/F/11492–2

FIGURE 2. Media Interface Block Diagram



TL/F/11492–3

FIGURE 3. Proposed Component Placement (Jumpers Located in Center of Board)

TABLE IV. ST-NIC Option Jumpers

Jumper	Position	Description	
JP3	OFF	IEEE Half Step AUI Mode	Default
	ON	Ethernet Full Step AUI Mode	
JP4	ON	Common Network-Bus Clocks	Default
	OFF	Separate Network-Bus Clocks	
JP5	ON	Link LED Off	
	OFF	LED Enabled	Default
JP6	OFF	10BASE-T Link Enabled	Default
	ON	10BASE-T Link Disabled	

Two jumpers select which physical media to use as shown in Table V.

TABLE V. Physical Media Selection

JP8	JP7	Description	
OFF	OFF	Thick Coax (10BASE5)	
OFF	ON	Twisted Pair (10BASE-T)	
ON	OFF	Thin Coax (10BASE2)	Default
ON	ON	Illegal	

For Table V, the selection default is Thin Ethernet, and any of the jumper options may be selected, except shorting both jumpers, JP7 and JP8. If this is done then the Thinnet transceiver is enabled, but the ST-NIC will use the twisted pair interface, since this does not make any sense the option is not useable.

I/O and EPROM Addresses

This design utilizes the same set of I/O address selections and EPROM address selections as NE1000, as shown in Table VI.

TABLE VI. I/O and EPROM Address Options

JP2	JP1	JP0	I/O Address	EPROM Address	
ON	ON	ON	300H	C800H	
ON	ON	OFF	300H	Disabled	Default
ON	OFF	ON	320H	CC00H	
ON	OFF	OFF	320H	Disabled	
OFF	ON	ON	340H	D000H	
OFF	ON	OFF	340H	Disabled	
OFF	OFF	ON	360H	D400H	
OFF	OFF	OFF	360H	Disabled	

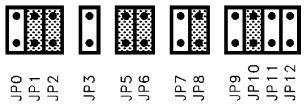
As can be seen JP0 actually is the enable for the EPROM, and JP1 and JP2 select the addresses for both the I/O and EPROM. Like the NE1000 the addressing of the I/O and EPROM cannot be set individually.

This design supports the same interrupt selection options as the NE1000, as shown in Table VII. Individual jumpers enable each interrupt to the bus interface. It is important that only one interrupt be selected at any one time.

TABLE VII. Interrupt Output Selection

JP12	JP11	JP10	JP9	Interrupt	
ON	OFF	OFF	OFF	IRQ6	
OFF	ON	OFF	OFF	IRQ4	
OFF	OFF	ON	OFF	IRQ3	Default
OFF	OFF	OFF	ON	IRQ9	
OFF	OFF	OFF	OFF	NONE	

All of these jumper options can be provided in a relatively easy grouping as shown below. (JP5) may not be grouped here as it is better to place it near the ST-NIC to try to minimize clock trace lengths.



TL/F/11492–4

FIGURE 4. Possible Jumper Configuration

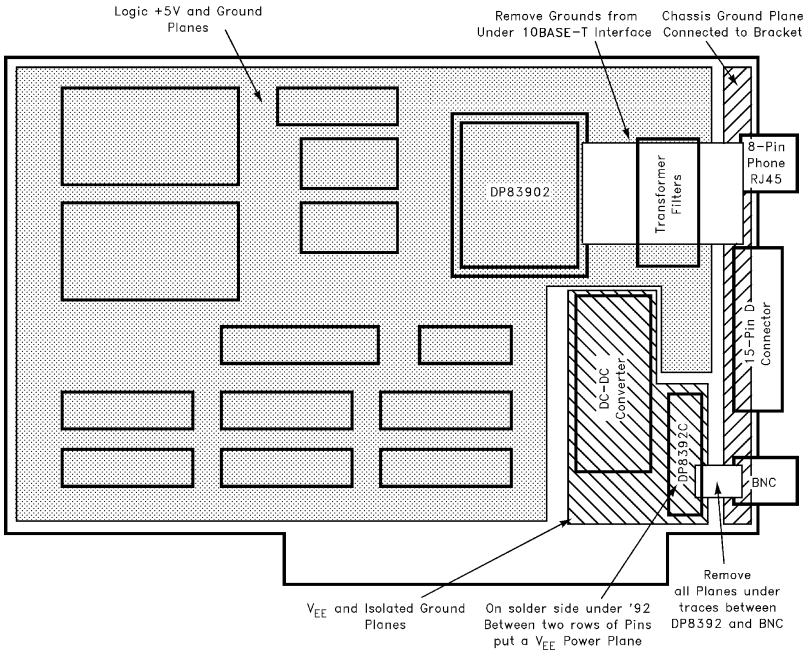
LAYOUT CONSIDERATIONS

The PCB layout for this design is very similar to most triple media interface designs (most of the layout considerations revolve around the media interfaces layout). The major component placement decisions are to place the ST-NIC's 10BASE-T port near the RJ45 Connector, and to place the DP8392 close to the BNC connector.

For the ST-NIC placement and layout, it is important to ensure that the power supply noise imparted from the board is minimized. To ensure this adequate decoupling around the 4 sides of the ST-NIC is important. There are two reasons for this. First the ST-NIC is a combined digital and analog function so to maximize the analog circuit performance, noise should be reduced. Secondly, the AUI and twisted pair outputs can conduct power supply noise out to the connectors. Thus power supply noise should be kept to a minimum to reduce RFI emissions. It is recommended that 0.1 μF low ESR decoupling capacitors be used along with a couple of 4.7 μF–10 μF tantalum capacitors.

On the ST-NIC's twisted pair interface, the layout should be compact, and all signal traces should be kept straight and short. It is preferable to have each of the signals in a particular differential pair matched to minimize differential skews (i.e., RX+ and RX− should be matched). Also, the power planes under the twisted pair interface components should be removed to prevent power supply noise from being injected into the twisted pair signals, again to minimize RFI.

For the DP8392 layout there are several considerations. First the CTI power planes must be isolated from the logic power planes by a PCB gap that can withstand 500V. The isolated power plane should be removed from under the signals that interface from the CTI to the BNC connector. This is required to reduce the capacitance as seen from the Thin net (RG58) cable. It is also advisable to add a small heatsink power plane to the solder side layer that encompasses the area between the two rows of pins of the DP8392 package (see datasheet for specific layout recommendations).



TL/F/11492–5

FIGURE 5. Ground/Power Planes and Layout Considerations

BILL OF MATERIALS July 8, 1991

CAPACITORS	
C1, C2, C6–C26, C31–C35	0.01 μF, 50V Monolythic
C3, C27, C28, C36	22 μF, 12V Tantalum 20%
C4	0.01 μF, 1 kV Ceramic
C5	0.01 μF, 50V Ceramic
C29, C30	0.01 μF, 50V Ceramic
RESISTORS (5% 1/8 Watt unless otherwise noted.)	
R1–R3	4.7k
R4, R5	270, 1/4W
R6–R9	39.2, 1%
R10–R13	1.5k
R14	1k, 1%
R15	150, 1%, 1/4W
R17	1M, 1/2W
R18	10k, 1%
R19, R20	50, 1%
R22, R23	66, 1%, 1/4W
R21, R24	271, 1%
R25	800, 1%
R26–R28	300
R29–R35	4.7k
DIODES	
D1	1N4150 (FDSO1201 SMT Version)
D2	Green LED 5mm Low Current
D3	Amber LED 5mm Low Current
D4	Green LED 5mm Low Current
CONNECTORS/SOCKETS	
J2	BNC Same as ATT
J3	RJ-45 AMP 520252 or Non-Keyed or Equivalent
J4	15-Pin D Conn Female, 747247-4 Slide Lock AMD MDA 51220-1
JP0–JP13	2 Pin Jumper, 0.1″ Pin Space

CONNECTORS/SOCKETS (Continued)	
S1	24-Pin 0.3″ Space Socket for U1
S2	20-Pin 0.3″ Space Socket for U2
S3	16-Pin 0.3″ Space Socket for U8
S4	24-Pin 0.3″ Space Socket for U13
SEMICONDUCTORS	
U1	GAL20V8-15 or PAL20L8 (Socketed)
U2	PAL16L8-15 (Socketed)
U3	74ALS245
U4, U5	74ALS374
U6	HM6264-85ns (May Use 100ns)
U7	74F373
U8	74S288
U9	DP83902
U11	DP8392C
U12	74ALS02
U13	27128 (Socket Installed Only)
U14	74ALS244
MISC	
SP1	0.75 pF, 1 kV, Spark Gap Mallory ASR75A or MEPCO/CENTRALAB S758X44000NAZAA
T1	Belfuse S553-1006-AE
T2	Supra1.1 10BASE-T Pulse Transformer/Filter
U10	PM7102 Valor DC-DC
X1	20 MHz, 0.01%, Oscillator 40/60% 10 TTL Drive Opt.
X2	25 MHz, 0.1%, Oscillator 40/60% (Not Installed) Opt.
	Bracket for Mounting in PC-AT Slot G44 Basic Blank, Stamped as DP839EB-ATS Board (Assy. #980550173) Screw: Bind Head Slotted 4—40 x 0.250, Steel, (90277A106) Washer: Lock Ext #4, Zinc/Steel, (91114A005) Washer: Flat #4, Zinc-CRS, (90126A005)

PAL EQUATIONS
PAL # 1 (U1)

```
module iodecode    flag '-r1'
title 'date: 7/5/91
functions: IO Address Decode, IO Port-NIC Handshake, Ready Generation'

u1 device 'P20L8';

"input pins:
BCLK, SA9, SA8, SA7, nJPEN          pin 1, 2, 3, 4, 5;
SA4, SA2, RSTD, nIOR, nIOW          pin 6, 7, 8, 9, 10;
PRQ, nAEN,  nACK                    pin 11, 14, 23;

"output pins:
nIORDY, nCSN, nWACK, nIOEN          pin 15, 17, 18, 19;
nNRST, NRST, nRACK                  pin 20, 21, 22;

"constants

    X, Z, H, L = .X.,.Z., 1, 0;
    ADDR2 = [SA9, SA8, SA7, X, X, SA4, X, SA2, X, X];

equations

nCSN =   !((!nAEN & !nJPEN & !SA4 & SA9 & SA8 & !SA7 & !nIOR)
          # (!nAEN & !nJPEN & !SA4 & SA9 & SA8 & !SA7 & !nIOW ));

nRACK =  !(!nAEN & !nJPEN & SA9 & SA8 & !SA7 & SA4 & !SA2 & !nIOR & PRQ);

nWACK =  !(!nAEN & !nJPEN & SA9 & SA8 & !SA7 & SA4 & !SA2 & PRQ & !nIOW);

nIOEN =  !((!nAEN & !nJPEN & !nIOR & SA9 & SA8 & !SA7 & SA4 & !SA2)  "Not Reset
         # (!nAEN & !nJPEN & !nIOW & SA9 & SA8 & !SA7 & SA4 & !SA2)
         # (!nAEN & !nJPEN & SA9 & SA8 & !SA7 & !SA4 & !nIOR)    "NIC Registers
         # (!nAEN & !nJPEN & SA9 & SA8 & !SA7 & !SA4 & !nIOW));

enable nIORDY = !nIOEN;
nIORDY = !(nACK & !nCSN
         # !PRQ & nCSN);

NRST = !(!nIOW # nNRST);
nNRST = !((!nIOR & !nAEN & !nJPEN & SA9 & SA8 & !SA7 & SA4 & SA2)
        # RSTD # NRST);


test_vectors ([ADDR2, nAEN,  nIOR, nIOW, nJPEN] -> [nCSN]);

" nCSN ASSERTION

"  A   nA nI nI nJP    nC
"  D    E  O  O  E      S
"  D    N  R  W  N      N

[^h310, L, L, L, L] -> [H]; " None
[^h310, L, H, H, L] -> [H]; " None
[^h300, H, L, L, H] -> [H]; " None
[^h300, L, L, L, H] -> [H]; " None
[^h300, L, L, L, L] -> [L]; " nCSN
[^h300, L, L, H, L] -> [L]; " nCSN
```

TL/F/11492–6

```
[^h308, L, H, L, L] -> [L]; " nCSN
[^h320, L, L, L, H] -> [H]; " None

test_vectors ([ADDR2, nAEN, nIOR, nIOW, nJPEN, PRQ] -> [nRACK, nWACK]);

"  A   nA nI nI nJP P     nR nW
"  D    E  O  O  E  R      C  C
"  D    N  R  W  N  Q      K  K

[^h310, L, L, H, L, H] -> [L, H]; " nRACK
[^h310, L, H, L, L, H] -> [H, L]; " nWACK
[^h310, H, L, H, H, H] -> [H, H]; " None
[^h310, L, L, H, H, H] -> [H, H]; " None
[^h310, H, L, L, L, H] -> [H, H]; " None
[^h310, H, L, L, H, H] -> [H, H]; " None
[^h300, L, L, L, H, H] -> [H, H]; " None
[^h314, L, L, L, H, L] -> [H, H]; " None
[^h318, L, L, H, L, H] -> [L, H]; " nRACK
[^h318, L, H, L, L, H] -> [H, L]; " nWACK

test_vectors ([ADDR2, nAEN, nIOR, nIOW, PRQ, nACK, nJPEN] -> [nIORDY]);

"  A   nA nI nI  P nA nJP    nI
"  D    E  O  O  R  C  E      R
"  D    N  R  W  Q  K  N      DY

[^h300, L, L, H, X, H, L] -> [L]; " NIC Read
[^h300, L, L, H, X, L, L] -> [H]; " NIC Read Ready
[^h300, L, H, L, X, H, L] -> [L]; " NIC Write
[^h300, L, H, L, X, L, L] -> [H]; " NIC Write Ready

[^h310, L, L, H, L, X, L] -> [L]; " IO Read
[^h310, L, L, H, H, X, L] -> [H]; " IO Read Ready
[^h310, L, H, L, L, X, L] -> [L]; " IO Write
[^h310, L, H, L, H, X, L] -> [H]; " IO Write Ready

test_vectors ([ADDR2, nAEN, nIOR, nIOW, RSTD, nJPEN] -> [nNRST, NRST]);

"  A   nA nI nI  R nJP    nN  N
"  D    E  O  O  S  E      R  R
"  D    N  R  W  T  N      T  T

[^h300, H, H, H, H, L] -> [L,  H]; " Hard Reset
[^h300, H, H, H, L, L] -> [L,  H]; " Reset Latched
[^h300, H, H, L, L, L] -> [H,  L]; " Un Reset
[^h314, L, L, H, L, L] -> [L,  H]; " Soft Reset
[^h314, L, H, H, L, L] -> [L,  H]; " Reset Latched
[^h300, H, H, L, L, L] -> [H,  L]; " Un Reset
[^h30C, L, L, H, L, L] -> [H,  L]; " Soft Reset
[^h30C, L, H, H, L, L] -> [H,  L]; " Reset Latched
[^h300, H, H, L, L, L] -> [H,  L]; " Un Reset

end iodecode;
```

TL/F/11492–7

PAL #2

```
module epdecode   flag '-r1';
title '
date:7/5/91
functions: EPROM DECODE, ID PROM DECODE, INTERRUPT BUFFER'

u2 device 'P16L8';

"input pins:
nAEN, nMEMR, SA19, SA18           pin 1, 2, 3, 4;
SA17, SA16, SA15, SA14            pin 5, 6, 7, 8;
SA13, A5, A6                      pin 9, 11, 13;
NINT, JP2, JP1, JP0               pin 14, 15, 16, 17;

"output pins:
INT, nJPEN, nCSEP                 pin 12, 18, 19;

"constants
  X, Z, H, L = .X.,.Z., 1, 0;
  ADDR = [SA19, SA18, SA17, SA16, SA15, SA14, SA13, X, X, X, X, X, X, , X, X];

equations
nCSEP =    !((!nAEN & !nMEMR & !JP2 & !JP1 & !JP0 & (ADDR == ^hC800))
           # (!nAEN & !nMEMR & !JP2 &  JP1 & !JP0 & (ADDR == ^hCC00))
           # (!nAEN & !nMEMR &  JP2 & !JP1 & !JP0 & (ADDR == ^hD000))
           # (!nAEN & !nMEMR &  JP2 &  JP1 & !JP0 & (ADDR == ^hD400)));

nJPEN =   !((!JP2 & !JP1 & !A5 & !A6)     " 300H
          # (!JP2 &  JP1 &  A5 & !A6)     " 320H
          # ( JP2 & !JP1 & !A5 &  A6)     " 340H
          # ( JP2 &  JP1 &  A5 &  A6));   " 360H

INT = !(!NINT);

test_vectors ([ADDR, nAEN, nMEMR, JP2, JP1, JP0] -> [nCSEP]);

"  A     A  M  J  J  J      C
"  D     E  M  P  P  P      S
"  D     N  R  2  1  0      EP

[^hC800, L, L, L, L, L] -> [L]; " Proper Decode
[^hCC00, L, L, L, H, L] -> [L]; "
[^hD000, L, L, H, L, L] -> [L]; "
[^hD400, L, L, H, H, L] -> [L]; "
[^hC800, L, L, L, L, H] -> [H]; " Jumper Disable
[^h0000, L, L, L, L, L] -> [H]; " No Address
[^hC800, L, H, L, L, L] -> [H]; " No MRD
[^hC800, H, L, L, L, L] -> [H]; " No AEN
[^hFF00, L, L, L, L, L] -> [H]; " No Address
[^hC800, L, L, H, L, L] -> [H]; " No JP2
[^hCC00, L, L, L, L, L] -> [H]; " No Address

test_vectors  ([JP2, JP1, A5, A6] -> [nJPEN])

" J  J  A  A      J
" P  P  5  6      P
" 2  1            EN

 [H, L, L, L] -> [H]; " No Enable
 [L, H, L, L] -> [H]; " No Enable
```

TL/F/11492–8

```
  [L, L, H, L] -> [H]; " No Enable
  [L, L, L, H] -> [H]; " No Enable
  [L, L, L, L] -> [L]; " Enable
  [H, L, L, H] -> [L]; " Enable
  [L, H, H, L] -> [L]; " Enable
  [H, H, H, H] -> [L]; " Enable

test_vectors ([NINT] -> [INT]);

[H] -> [H]; "Non Inverter
[L] -> [L];

end epdecode;
```

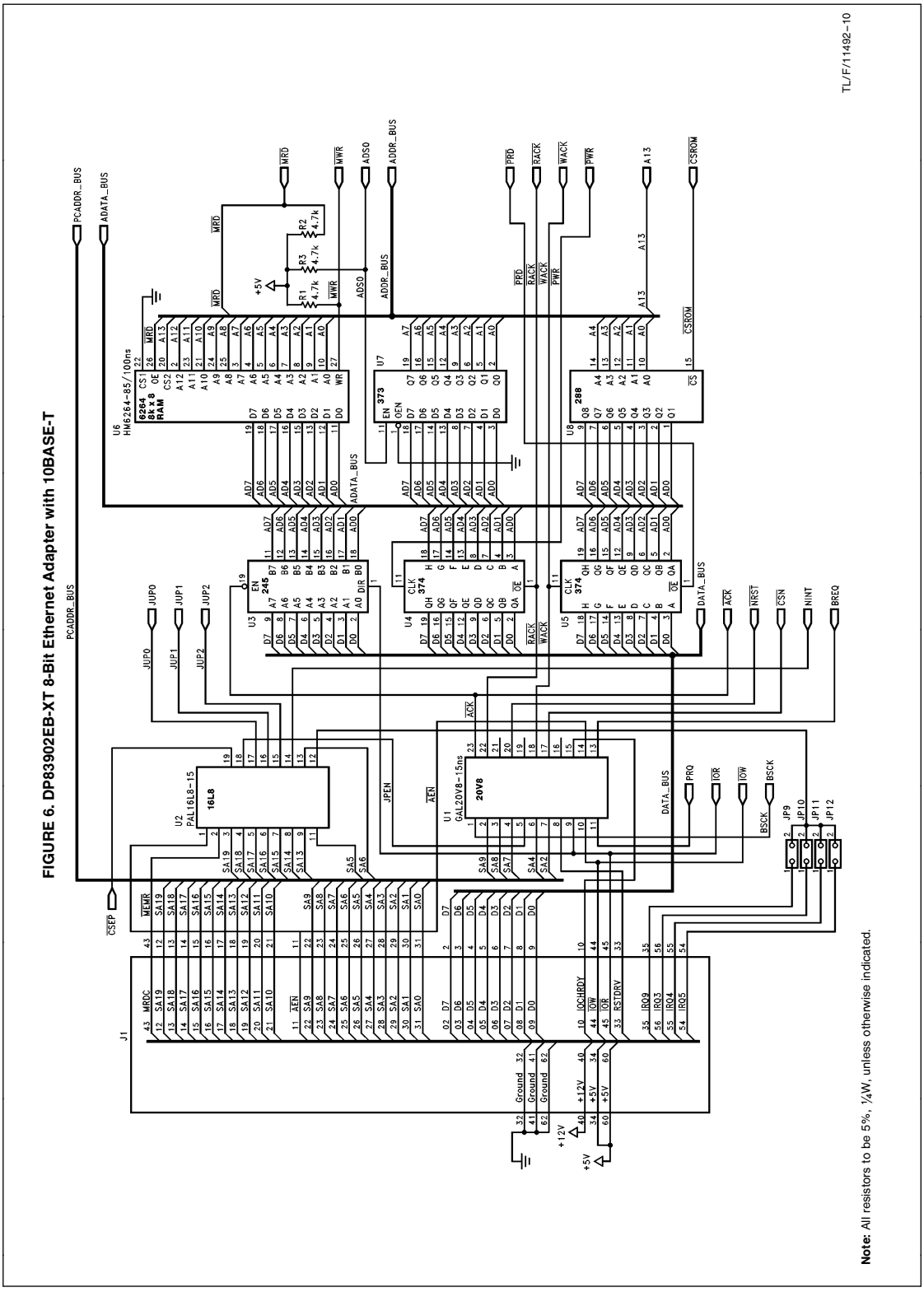
TL/F/11492–9

ETHERNET ADDRESS PROM CONTENTS

The ID PROM is 74S288 type. The content is as follows:

ADDR 00:	08	00	17	xx	yy	zz	00	00	00	00	00	00	00	00	57	57
ADDR 10:	08	00	17	xx	yy	zz	00	00	00	00	00	00	00	00	42	42

The ID address is 080017xxyyzz where 080017 is National's ID ''prefix''.

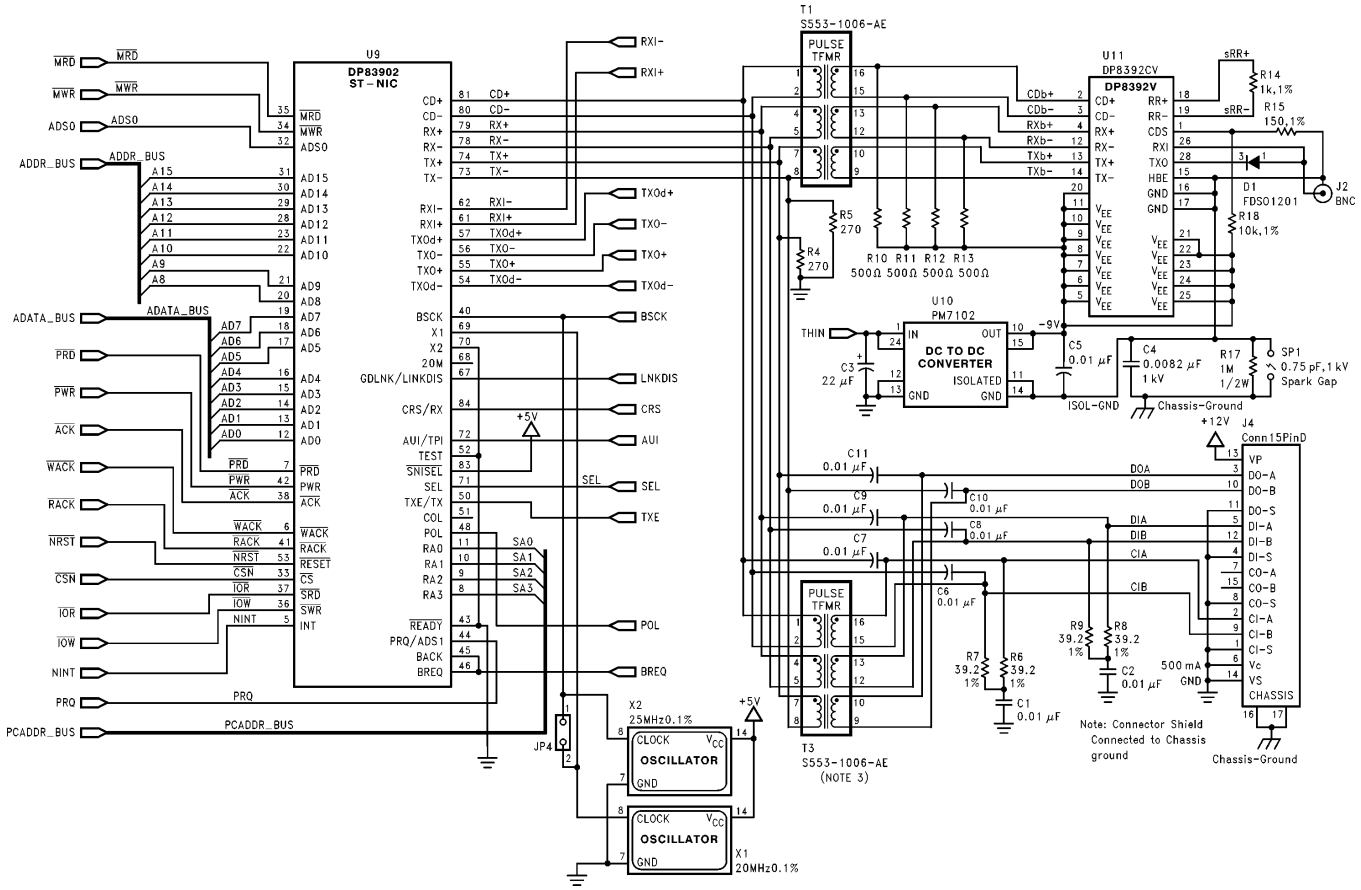


TL/F/11492–10

FIGURE 6. DP83902EB-XT 8-Bit Ethernet Adapter with 10BASE-T

Note: All resistors to be 5%, ¼W, unless otherwise indicated.

FIGURE 6. DP83902EB-XT 8-Bit Ethernet Adapter with 10BASE-T (Continued)



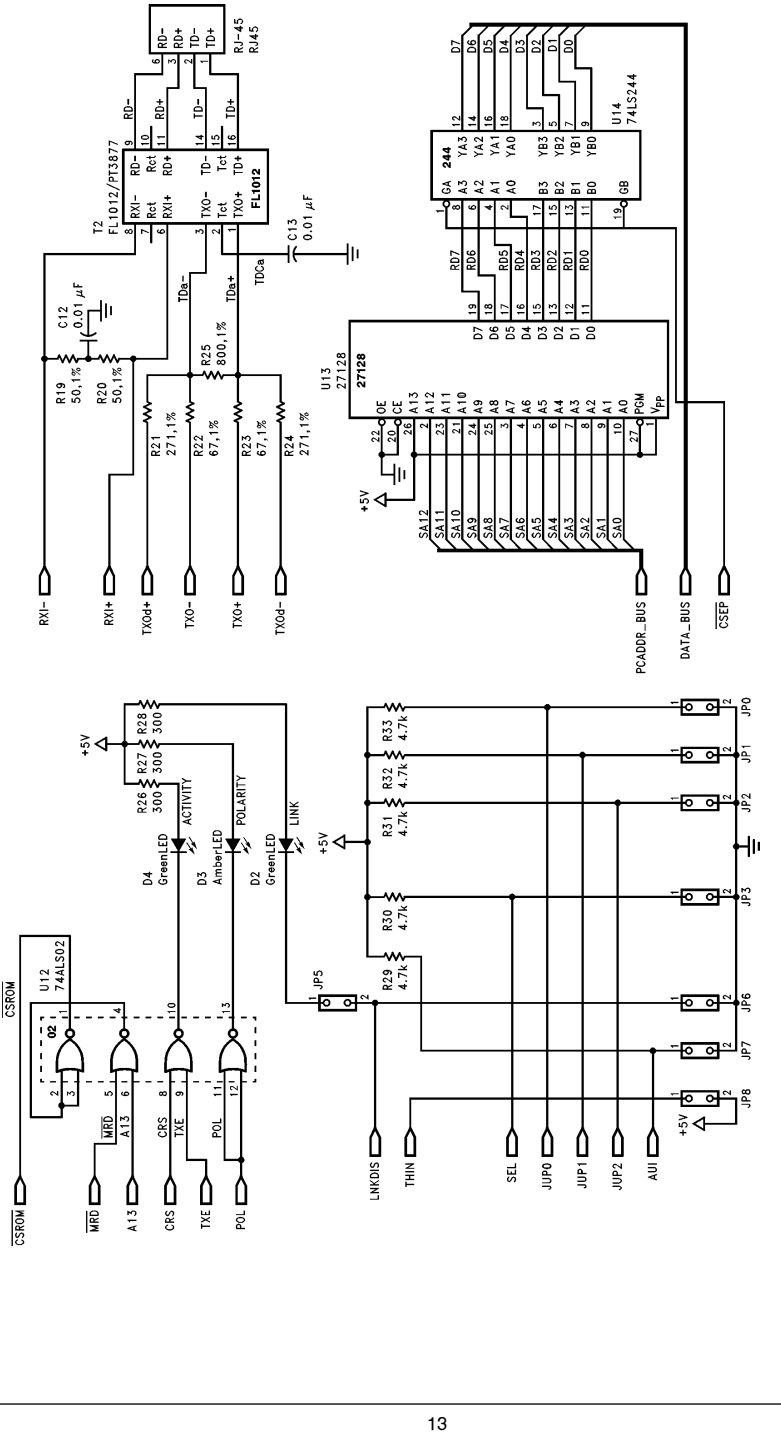
TL/F/11492–11

Note 1: All resistors to be 5%, ¼W, unless otherwise indicated.

Note 2: X2 is not populated but the location is provided to provide optional bus clock speeds.

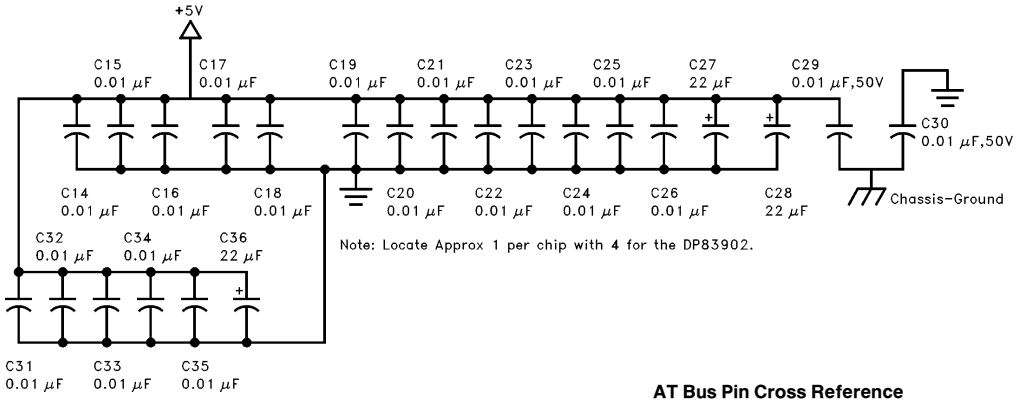
Note 3: T3 and C6–C11 are not populated simultaneously. Either T3 can be populated or the capacitors can be installed.

FIGURE 6. DP83902EB-XT 8-Bit Ethernet Adapter with 10BASE-T (Continued)



TL/F/11492–12

FIGURE 6. DP83902EB-XT 8 Bit Ethernet Adapter with 10BASE-T (Continued)



TL/F/11492–13

AT Bus Pin Cross Reference

AT Pins	SCH No.	AT Pins	SCH No.	AT Pins	SCH No.
A2	02	A23	23	B12	43
A3	03	A24	24	B13	44
A4	04	A25	25	B14	45
A5	05	A26	26	B15	46
A6	06	A27	27	B16	47
A7	07	A28	28	B17	48
A8	08	A29	29	B18	49
A9	09	A30	30	B19	50
A10	10	A31	31	B20	51
A11	11	B1	32	B21	52
A12	12	B2	33	B22	53
A13	13	B3	34	B23	54
A14	14	B4	35	B24	55
A15	15	B5	36	B25	56
A16	16	B6	37	B26	57
A17	17	B7	38	B27	58
A18	18	B8	39	B28	59
A19	19	B9	40	B29	60
A20	20	B10	41	B30	61
A21	21	B11	42	B31	62
A22	22				

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