Sound Effects for the COP800 Family

National Semiconductor
Application Note 663
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October 1989

This application note describes the creation of sound effects using National Semiconductor's COP800 family of microcontrollers. The following applications are described in detail:

1. Whistle
2. White Noise
3. Explosion
4. Bomb
5. Laser Gun

These applications were developed on a COP820C using a 10 MHz crystal and a 1 µs instruction cycle time. By making the appropriate changes to control registers within the routines, slower clock speeds may be used. Program flow diagrams and complete source codes are included in this document.

I. WHISTLE

The whistle routine utilizes the timer underflow interrupt and employs the TIO function on pin G3. Each timer underflow causes the TIO pin to toggle. This creates a tone whose frequency remains constant as long as the timer autoreload register value remains unchanged. In order to create a desending or ascending whistle tone, the autoreload register value is increased or decreased after every thirty-two timer interrupts (FCNTR register is used to count the interrupts). When the maximum or minimum frequency has been reached, the autoreload value must be reinitialized so that the whistle frequency does not exceed the desired range.

II. WHITE NOISE

White noise is generated by using a random number generating algorithm called a RING COUNTER. One random number is extracted periodically and placed into the MICROWIRE/PLUS™serial shift register. These bits are shifted onto the serial output (SO) pin which is wired to a transistor amplifier that drives a speaker. The serial input (SI) and serial output (SO) pins must be tied together.

The RING COUNTER is a pseudo-random number generator which operates on the principle of a linear feedback shift register (see *Figure 1*). This shift register is not to be confused with the MICROWIRE/PLUS serial shift register. Rather it is created using two bytes of data memory (RAM), and the carry flag. Each bit is called a "stage" with the carry flag being "stage 1" and bit 0 of the two byte data register being "stage 17". Using a seventeen stage shift register results in a clean tone with little distortion.

Implementation of the ring counter shift register is accomplished by a rotate right with carry instruction (RRC A). The linear feedback function is accomplished using an "exclusive or" on stages fourteen and seventeen. This particular choice of feedback stages results in a complete cycle of bit combinations, ($2^{17} - 1$), as long as the loop does not begin with zero in the RNGVAL register.

The "exclusive or" function is not explicit in that the XOR instruction is not used. Rather, stages seventeen and fourteen are tested in software using the principle that if only one of them is set then the result is a logic one, otherwise the result is logic zero. It turns out that since the rotate occurs prior to the test, the actual bits tested are the carry flag (stage 1) and bit 2 (stage 15).

A short example using four bits can be used to demonstrate how the ring counter works (see *Figure 2*). If you perform the "exclusive or" on stages three and four, then a complete cycle results. If instead, you use stages two and four, two cycles of six and one cycle of three results depending on the bit combination you begin with.

III. EXPLOSION

The explosion sound effect is generated by manipulating the white noise algorithm to begin with a high pitch and progress to a lower pitch. This is done by altering the rate (contained in the register LUPREG) at which the random numbers are extracted from the ring counter before being placed into the MICROWIRE/PLUS serial shift register (SIOR). If for example LUPREG initially contains the value 4, the white noise will be at a high pitch. By incrementing this number after every ten timer interrupts (using the register TCNTR) the white noise pitch will be reduced. Several other registers are used to provide control of strategic portions of sound within the routine. First and last tones are controlled with FIRSTR and LASTR. The value in EXITR is used to control the overall length of the explosion and the length of each tone is controlled by the register TCNTR. To vary the white noise pitch, the register LUPCNT is used. The value in LUPCNT is incremented each time the pitch of the white noise is decreased within the timer interrupt routine. Prior to entering the ring count loop, LUPCNT is loaded into LUPREG. The serial input (SI) pin must be tied to the serial output (SO) pin.

IV. BOMB

The bomb sound effect combines the descending whistle with an explosion at the end. The TIMER I/O (TIO) and serial input (SI) pins must be tied to the serial output (SO) pin. The explosion portion of this routine was altered slightly in that the first tone control register (FIRSTR) was removed. The first initialization of TCNTR, the tone control register, provides a means to control the first tone length. Subsequent tones are controlled (at label NF2 in the timer interrupt routine) where TCNTR is reinitialized. Both versions were retained for comparison and in the event that greater control of the first tone is needed.

V. LASER GUN

The laser gun sound effect combines the output from the white noise routine and the COP800 timer I/O (TIO) pin (tie TIO to SO). The SI pin is not tied to SO in this application and the ring counter uses only nine stages instead of seventeen.

The registers used for program control are EXITR, TCNTR, and the TIMER. By adjusting the value in EXITR the duration of the laser "shot" can be shortened or lengthened. (A value larger than 03F hex may create problems.) By adjusting the

TIMER values (TVALO, TVALHI) and the tone counter (TCNTR) value, interesting variations in the laser sound can be attained.

Note: This note applies to all routines that use both the timer interrupt and the ring counter: In order to return to the main program from which the subroutine was called, the stack pointer must be manually restored during the timer interrupt before executing the return (RET) instruction. The reason for this is that the timer interrupt is two levels below the main program. A simple return statement will only serve to return to the ring counter routine from the point at which the timer interrupt occurred. By adding two to the stack pointer (SP + 2), the return statement will force the address of the instruction following the JSR in MAIN into the program counter (PC) from which point execution will continue.

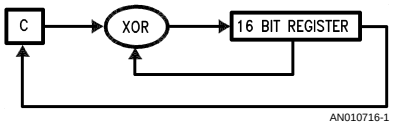

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FIGURE 1. 17 Stage Ring Counter

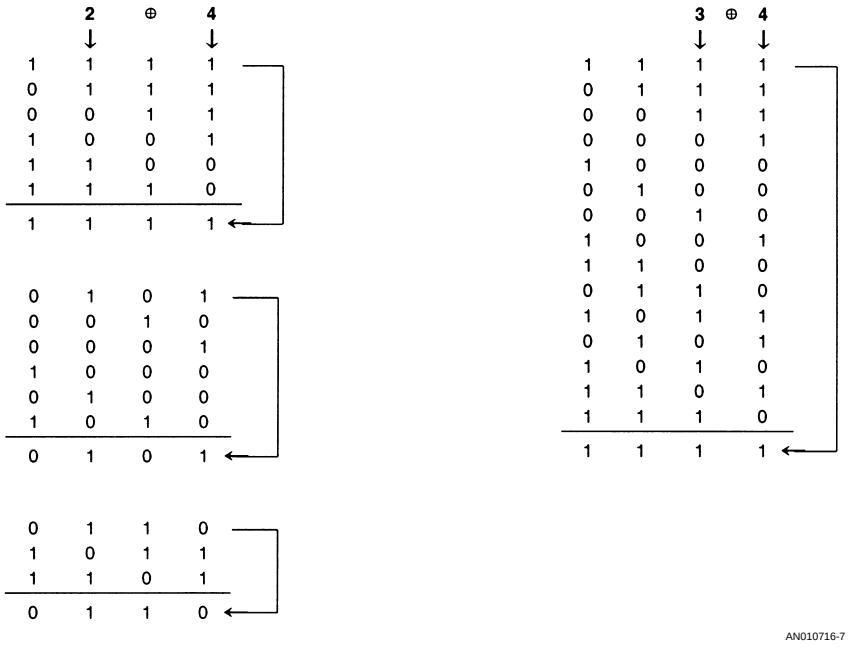

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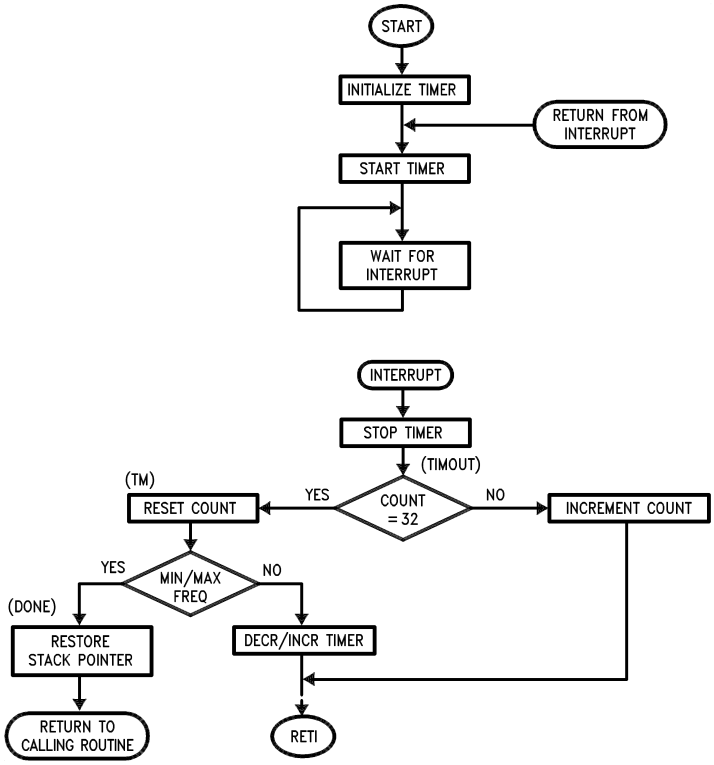
FIGURE 2. Example Showing Possible Cycles from a 4 Stage Ring Counter

Whistle Flow Diagram



Descending Whistle

```
 1 ;
 2 ;
 3 ; TIMER INTERRUPT IS USED.
 4 ; OUTPUT ON TIMER I/O (TIO) PIN.
 5 ; USE 20 MHz XTAL, 1 us INSTR CYCLE FOR THIS DEMO.
 6 ;
 7 ; WRITTEN BY: JERRY LEVENTER
 8 ; DATE: OCTOBER 4, 1989
 9 ;
10 .TITLE WHISTLE1
11 .CHIP 820
12 ;
13 00D5 PORTGC = 0D5 ; PORT G CONFIGURATION
14 00E9 SIOR = 0E9 ; SIO SHIFT REGISTER
15 00EA TMRLO = 0EA ; TIMER LOW BYTE
16 00EB TMRHI = 0EB ; TIMER HIGH BYTE
17 00EC TAULO = 0EC ; TIMER REGISTER LOW BYTE
18 00ED TAUHI = 0ED ; TIMER REGISTER HIGH BYTE
19 00EE CNTRL = 0EE ; CONTROL REGISTER
20 00EF PSW = 0EF ; PSW REGISTER
21 0004 TRUN = 4
22 0005 TPND = 5
23 0002 BUSY = 2
24 0000 GIE = 0
25 ;
26 ; **** SPECIAL REGISTERS AND CONSTANTS ****
27 ;
28 002F WSLO = 02F ; TIMER VALUES
29 0000 WSLHI = 000
30 00F0 FCNTR = 0F0 ; FREQUENCY COUNT REGISTER
31 0000 FCNT = 000
32 00FF MINFREQ = 0FF ; MIN FREQUENCY CONSTANT
33 ;
34 ; ********************************
35 ; **** BEGIN DEMO PROGRAM HERE ****
36 ; ********************************
37 ;
38 0000 DD2F MAIN: LD SP,#02F ; DEFAULT INITIALIZATION OF SP
38 0002 3005 JSR WHISTLE ; ***CALLING ROUTINE FOR DEMO***
40 0004 FF JP .
41 0005 BCD508 WHISTLE:LD PORTGC,#008 ; TIO PIN (G3) AS OUTPUT
42 0008 BCEEA2 LD CNTRL,#0A2 ; PWM WITH TIO TOGGLE, 8Tc
43 000B BCEA2F LD TMRLO,#WSLO ; WHISTLE VALUE FOR TIMER
44 000E BCEB00 LD TMRHI,#WSLHI
45 0011 BCEC2F LD TAULO,#WSLO
46 0014 BCED00 LD TAUHI,#WSLHI
47 0017 D000 LD FCNTR,#FCNT ; INIT FREQ COUNT
48 0019 BCEF11 LUP: LD PSW,#011 ; ENTI, GIE = 1, TPND = 0
49 001C BDEE7C SBIT TRUN,CNTRL ; START TIMER
50 001F FF JP . ; SELF LOOP TIL TIMER INTERRUPT
51 0020 F8 JP LUP ; RUN TIL LAST HISTLE FREQ
52 ;
53 ; **** INTERRUPT ROUTINE ****
54 ;
55 00FF .=0FF
56 00FF BDEF75 IFBIT TPND, PSW ; TEST TIMER PENDING FLAG
57 0102 01 JP TIMOUT
58 0103 FF JP . ; ERROR
59 0104 BDEE6C TIMOUT: RBIT TRUN,CNTRL ; STOP THE TIMER
60 0107 BDF075 IFBIT 5,FCNTR ; COUNT CYCLES
61 010A 06 JP TM
62 010B 9DF0 LD A,FCNTR ; INCREMENT COUNT
63 010D 8A INC A
64 010E 9CF0 X A,FCNTR
65 0110 8D RETSK
66 0111 D000 TM: LD FCNTR,#FCNT ; RESET COUNT
```

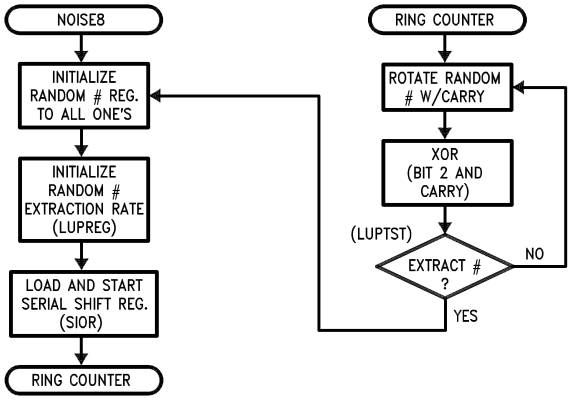
```
67 0113 DEEC LD B,#TAULO
68 0115 AE LD A,[B] ; CHANGE FREQUENCY
69 0116 92FF IFEQ A,#MINFREQ ; TIMER = MIN FREQ?
70 0118 03 JP DONE ; YES
71 0119 8A INC A
72 011A A6 X A,[B] ; STORE FREQ IN AUTO RELOAD
73 011B 8D RETSK
74 011C 9DFD DONE: LD A,SP ; *** RESTORE STACK POINTER ***
75 011E 9402 ADD A,#002 ; *** AND RETURN TO CALLING ***
76 0120 9CFD X A,SP ; *** ROUTINE.   ***
77 0122 8E RET
78 .END
```

Ascending Whistle

```
 1 ;
 2 ;
 3 ; OUTPUT ON TIMER I/O (TIO) PIN.
 4 ; USES TIMER INTERRUT.
 5 ; USE 20 MHz XTAL, 1 us INSTR CYCLE FOR THIS DEMO.
 6 ;
 7 ; WRITTEN BY: JERRY LEVENTER
 8 ; DATE: OCTOBER 4, 1989
 9 ;
10 ;
11 .TITLE WHISTLE2
12 .CHIP 820
13 ;
14 00D5 PORTGC = 0D5 ; PORT G CONFIGURATION
15 00EA TMRLO = 0EA ; TIMER LOW BYTE
16 00EB TMRHI = 0EB ; TIMER HIGH BYTE
17 00EC TAULO = 0EC ; TIMER REGISTER LOW BYTE
18 00ED TAUHI = 0ED ; TIMER REGISTER HIGH BYTE
19 00EE CNTRL = 0EE ; CONTROL REGISTER
20 00EF PSW = 0EF ; PSW REGISTER
21 0004 TRUN = 4
22 0005 TPND = 5
23 0002 BUSY = 2
24 0000 GIE = 0
25 ;
26 ; **** SPECIAL REGISTERS AND CONSTANTS ****
27 ;
28 00FF WSLO = 0FF ; TIMER VALUES
29 0001 WSLHI = 001
30 000A MAXFREQ = 00A ; LAST FREQUENCY CONSTANT
31 00F0 FCNTR = 0F0 ; TIMER COUNT REGISTER
32 0010 FCNT = 010 ; COUNTER CONSTANT
33 ;
34 ; ********************************
35 ; **** BEGIN PROGRAM HERE ****
36 ; ********************************
37 ;
38 0000 DD2F MAIN: LD SP,#02F ; DEFAULT INITIALIZATION OF SP
39 0002 3005 JSR WHISTLE2 ; *** CALLING ROUTINE FOR DEMO ***
40 0004 FF JP .
41 WHISTLE2:
42 0005 BCD508 LD PORTGC,#008 ; TIO PIN (G3) AS OUTPUT
43 0008 BCEEA0 LD CNTRL,#0A0 ; PWM WITH TIO TOGGLE,
44 000B BCEAFF LD TMRLO,#WSLO ; WHISTLE VALUE FOR TIMER
45 000E BCEB01 LD TMRHI,#WSLHI
46 0011 BCECFF LD TAULO#WSLO
47 0014 BCED01 LD TAUHI,#WSLHI
48 0017 D010 LD FCNTR,#FCNT ; INITIALIZE COUNTER
49 0019 BCEF11 LUP: LD PSW,#011 ; ENTI, GIE = 1, TPND = 0
50 001C BDEE7C SBIT TRUN,CNTRL ; START TIMER
51 001F FF JP . ; SELF LOOP UNTIL TIMER
52 0020 F8 JP LUP ; INTERRUPT
```

```
53 ;
54 ; **** INTERRUPT ROUTINE ****
55 ;
56 00FF .=0FF
57 00FF BDEF75 IFBIT TPND,PSW ; TEST TIMER PENDING FLAG
58 0102 01 JP TIMOUT
59 0103 FF JP .
60 0104 BDEE6C TIMOUT: RBIT TRUN,CNTRL ; STOP THE TIMER
61 0107 BDF075 IFBIT 5,FCNTR ; FREQUENCY TIMED OUT?
62 010A 06 JP TM ; YES, CHANGE FREQUENCY
63 010B 9DF0 LD A,FCNTR ; NO, KEEP GOING
64 010D 8A INC A ; INCREMENT COUNT
65 010E 9CF0 X A,FCNTR
66 0110 8D RETSK ; RETURN
67 0111 D010 TM: LD FCNTR,#FCNT ; RESET COUNTER
68 0113 9DEC LD A,TAULO ; CHANGE FREQUENCY
69 0115 920A IFEQ A,#MAXFREQ ; TIMER = MAX FREQUENCY ?
70 0117 05 JP DONE ; YES
71 0118 94FF ADD A,#0FF ; INCREMENT FREQUENCY
72 011A 9CEC X A,TAULO ; STORE FREQ IN AUTO RELOAD
73 011C 8D RETSK
74 011D 9DFD DONE: LD A,SP ; *** RESTORE STACK POINTER ***
75 011F 9402 ADD A,#002 ; *** AND RETURN TO CALLING ***
76 0121 9CFD X A,SP ; *** ROUTINE. ***
77 0123 8E RET
78 .END
```

White Noise

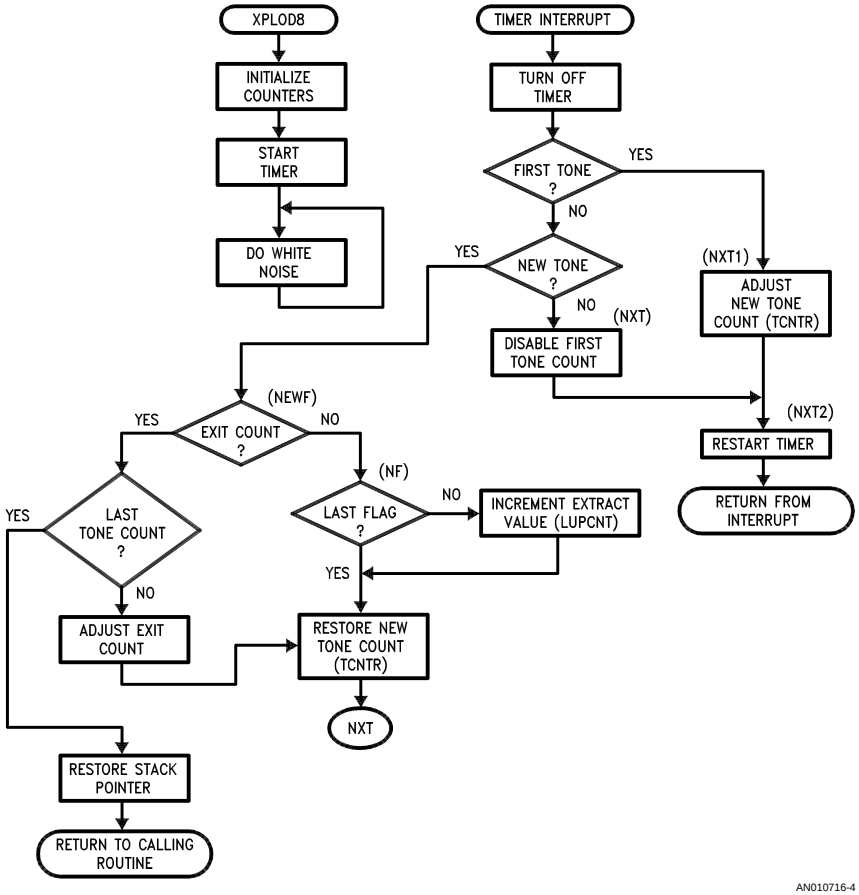


AN010716-3

```
 1 ;
 2 ;
 3 ;
 4 ;
 5 ; TIE SERIAL INPUT (SI)PIN TO SERIAL OUTPUT (SO) PIN.
 6 ; OUTPUT IS ON THE SERIAL OUTPUT (SO) PIN.
 7 ; NO INTERRUPT IS USED.
 8 ; USE 20 MHz XTAL, 1 us INSTR CYCLE FOR THIS DEMO.
 9 ;
10 ; WRITTEN BY: JERRY LEVENTER
11 ; DATE: OCTOBER 4, 1989
12 ;
13 .TITLE NOISE8
14 .CHIP 820
15 ;
16 00D5 PORTGC = 0D5 ; PORT G CONFIGURATION
17 00E9 SIOR = 0E9 ; SERIAL SHIFT REGISTER
18 00EA TMRLO = 0EA ; TIMER LOW BYTE
19 00EB TMRHI = 0EB ; TIMER HIGH BYTE
20 00EC TAULO = 0EC ; TIMER REGISTER LOW BYTE
21 00ED TAUHI = 0ED ; TIMER REGISTER HIGH BYTE
22 00EE CNTRL = 0EE ; CONTROL REGISTER
23 00EF PSW = 0EF ; PSW REGISTER
24 0002 BUSY = 2 ; BUSY BIT
25 ;
26 ; **** SPECIAL REGISTERS AND CONSTANTS ****
27 ;
28 0002 RNGVAL = 002 ; RANDOM NUMBER LOCATION
29 00FF LUPREG = 0FF ; EXTRACTION RATE REGISTER
30 0000 FLAG = 000 ; RANDOM NUMBER BYTE FLAG
31 0004 COUNT = 4 ; EXTRACTION RATE CONSTANT
32 ;
33 ; ********************************
34 ; **** BEGIN PROGRAM HERE ****
35 ; ***************************** ****
36 ;
37 0000 DD2F LD SP,#02F ; DEFAULT INITIALIZATION OF SP
38 0002 BCD530 NOISE: LD PORTGC,#030 ; SO AND SK AS OUTPUTS
39 0005 BCEE8B LD CNTRL,#08B ; SK = DIV BY 8, TIMER RELOAD
40 0008 A1 SC ; INIT STAGE 1
41 0009 5D LD B,#RNGVAL ; POINT TO RANDOM # LOCATION
42 000A 9AFF LD [B+],#0FF ; INIT RING VAL TO ONE'S
43 000C 9EFF LD [B],#0FF ; B POINTS TO UPPER BYTE
44 000E 9CE9 SHIFT: X A,SIOR ; PLACE # IN SIOR
45 0010 BDEF7A SBIT BUSY,PSW ; START SHIFTING
46 0013 DF04 LD LUPREG,#004 ; RESTORE EXTRACTION COUNT
47 ;
```

```
48 ; ******************************************
49 ; RING COUNTER (17 STAGE)
50 ; THIS IS A SEVENTEEN STAGE RING COUNTER (LINEAR
51 ; FEEDBACK SHIFT REGISTER) WITH THE RRC COMMAND.
52 ; THE COUNTER'S 14TH AND 17TH STAGES THROUGH AN
53 ; EXCLUSIVE-OR SERVE AS THE FEEDBACK FUNCTION.
54 ; THIS 14, 17 RING COUNTER BREAKS DOWN INTO
55 ; 1 CYCLE OF [(2 ** 17) - 1] COUNTS. SINCE THE EXCLUSIVE OR
56 ; OCCURS AFTER THE ROTATE, IT IS THE 15TH AND CARRY
57 ; STAGES THAT ARE XOR'D (BIT 2 AND CARRY).
58 ;
59 ; STAGE
60 ; _______________
61 ; BEFORE ROTATE: 14 17
62 ; AFTER ROTATE: 15 CARRY
63 ;
64 ; CARRY BIT = STAGE ONE
65 ; LOW ORDER BIT = STAGE 17
66 ; ******************************************
67 ;
68 0015 AE RING: LD A,[B] ; GET RANDOM #
69 0016 B0 RRC A ; ROTATE UPPER BYTE
70 0017 A3 X A,[B-]
71 0018 AE LD A,[B]
72 0019 B0 RRC A ; ROTATE LOWER BYTE
73 001A A6 X A,[B]
74 001B 9804 LD A,#004 ; PERFORM XOR
75 001D 85 AND A,[B]
76 001E 9200 IFEQ A,#000
77 0020 05 JP LUPTST
78 0021 88 IFC
79 0022 02 JP RC
80 0023 A1 SC
81 0024 01 JP LUPTST
82 0025 A0 RC: RC
83 0026 AA LUPTST: LD A,[B+] ; POINT TO UPPER BYTE
84 0027 CF DRSZ LUPREG ; EXTRACT THIS NUMBER ?
85 0028 EC JP RING ; NO, KEEP ROTATING
86 0029 E4 JP SHIFT ; YES, SEND IT
87 .END
```

Explosion

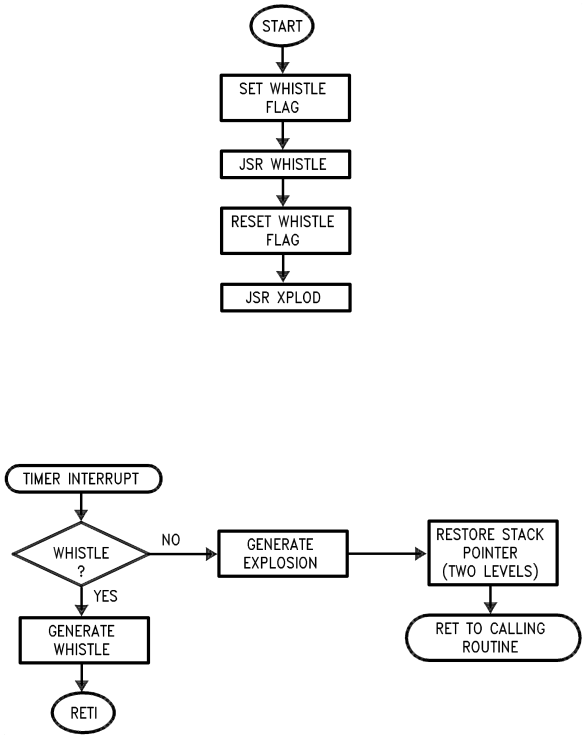

XPLOD8
INITIALIZE COUNTERS
START TIMER
DO WHITE NOISE
TIMER INTERRUPT
TURN OFF TIMER
FIRST TONE ?
YES
NO
NEW TONE ?
YES
NO
(NXT)
DISABLE FIRST TONE COUNT
(NXT1)
ADJUST NEW TONE COUNT (TCNTR)
(NXT2)
RESTART TIMER
RETURN FROM INTERRUPT
(NEWF)
EXIT COUNT ?
YES
NO
(NF)
LAST FLAG ?
NO
INCREMENT EXTRACT VALUE (LUPCNT)
YES
LAST TONE COUNT ?
YES
NO
ADJUST EXIT COUNT
RESTORE NEW TONE COUNT (TCNTR)
NXT
RESTORE STACK POINTER
RETURN TO CALLING ROUTINE
AN010716-4

```
1 ;
2 ;
3 ; TIMER INTERRUPT IS USED.
4 ; SI MUST BE TIED TO S0. OUTPUT ON S0.
5 ; USE 20 MHz XTAL, 1 us INSTR CYCLE FOR THIS DEMO.
6 ;
7 ; WRITTEN BY: JERRY LEVENTER
8 ; DATE: OCTOBER 4, 1989
9 ;
10 .TITLE XPLOD8
11 .CHIP 820
12 ;
13 00D5 PORTGC = 0D5 ; PORT G CONFIGURATION
14 00E9 SIOR = 0E9 ; SIO SHIFT REGISTER
15 00EA TMRLO = 0EA ; TIMER LOW BYTE
16 00EB TMRHI = 0EB ; TIMER HIGH BYTE
17 00EC TAULO = 0EC ; TIMER REGISTER LOW BYTE
18 00ED TAUHI = 0ED ; TIMER REGISTER HIGH BYTE
19 00EE CNTRL = 0EE ; CONTROL REGISTER
20 00EF PSW = 0EF ; PSW REGISTER
21 0004 TRUN = 4
22 0005 TPND = 5
23 0002 BUSY = 2
24 ;
25 ; **** SPECIAL REGISTERS AND CONSTANTS ****
26 ;
27 ; ANY REGISTER USED FOR THE DRSZ TEST MUST
28 ; BE INITIALIZED TO AT LEAST ”1”.
29 ;
30 00F5 FIRSTR = 0F5 ; FIRST TONE CONTROL REGISTER
31 0002 FIRST = 002 ; FIRST TONE CONSTANT
32 00F6 LASTR = 0F6 ; LAST TONE CONTROL REGISTER
33 0002 LAST = 002 ; LAST TONE CONSTANT
34 00F7 EXITR = 0F7 ; ROUTINE DURATION REGISTER
35 0010 EXIT = 010 ; EXIT CONSTANT
36 0002 RNGVAL = 002 ; HOLDS CURRENT RANDOM #
37 00F8 TCNTR = 0F8 ; TONE DURATION REGISTER
38 000A TCNT = 0A ; TONE CONSTANT
39 0020 TCNT1 = 020 ; ”FIRST” TONE CONSTANT
40 00F9 LUPREG = 0F9 ; EXTRACTION RATE REGISTER
41 0004 XTRCT = 004 ; EXTRACT CONSTANT
42 00FA LUPCNT = 0FA ; EXTRACTION VARIABLE REGISTER
43 0000 TEMP = 000 ; LAST TONE FLAG
44 00FF TVALO = 0FF ; TIMER VALUES
45 0010 TVALHI = 010
46 ;
47 ; *******************************
48 ; **** BEGIN PROGRAM HERE ****
49 ; *******************************
50 ;
51 0000 DD2F MAIN: LD SP,#02F ; DEFAULT INITIALIZATION OF SP
52 0002 3005 JSR XPLOD ; **** XPLOD CALLING ROUTNE ****
53 0004 FF JP . ; **** SELF LOOP FOR DEMO ****
54 0005 BCD530 XPLOD: LD PORTGC,#030
55 0008 BCEE8A LD CNTRL,#08A ; SK = DIV BY 8, PWM ON
56 000B BCEF11 LD PSW,#011 ; ENABLE TIMER INTERRUPT
57 000E BCEAFF LD TMRLO,#TVALO ; INITIALIZE TIMER
58 0011 BCEB10 LD TMRHI,#TVALHI
59 0014 BCECFF LD TAULO,#TVALO
60 0017 BCED10 LD TAUHI,#TVALHI
```

```
 61 001A D502 LD FIRSTR,#FIRST ; LENGTHEN FIRST TONE
 62 001C D602 LD LASTR,#LAST ; LENGTHEN LAST TONE
 63 001E D710 LD EXITR,#EXIT ; INITIALIZE EXIT COUNT
 64 0020 D80A LD TCNTR,#TCNT ; INITIALIZE TONE COUNT
 65 0022 DA04 LD LUPCNT,#XTRCT ; INITIALIZE EXTRACTION RATE
 66 0024 BD0068 RBIT 0,TEMP ; RESET LAST TONE FLAG
 67 0027 BDEE7C SBIT TRUN,CNTRL ; START TIMER
 68 002A A1 NOISE: SC ; INIT. STAGE 1
 69 002B 5D LD B,#RNGVAL ; POINT TO RANDOM NUMBER
 70 002C 9AFF LD [B+],#0FF ; INIT TO ALL ONE'S
 71 002E 9EFF LD [B],#0FF
 72 0030 9CE9 SHIFT: X A,SIOR ; LOAD AND START SIOR
 73 0032 BDEF7A SBIT BUSY,PSW
 74 0035 9DFA LD A,LUPCNT ; RESTORE EXTRACTION COUNT
 75 0037 9CF9 X A,LUPREG
 76 ;
 77 ; *********************************
 78 ; RING COUNTER (17 STAGE)
 79 ;
 80 ; THIS IS A SEVENTEEN STAGE RING COUNTER (LINEAR
 81 ; FEEDBACK SHIFT REGISTER) WITH THE RRC COMMAND.
 82 ; THE COUNTER'S 14th AND 17th STAGES THROUGH AN
 83 ; EXCLUSIVE-OR SERVE AS THE FEEDBACK FUNCTION.
 84 ; THIS 14, 17 RING COUNTER BREAKS DOWN INTO
 85 ; 1 CYCLE OF [(2 ** 17) - 1] COUNTS. SINCE THE EXCLUSIVE OR
 86 ; OCCURS AFTER THE ROTATE, IT IS THE 15th AND CARRY
 87 ; STAGES THAT ARE XOR'D (BIT 2 AND CARRY).
 88 ;
 89 ; STAGE
 90 ; _______________
 91 ; BEFORE ROTATE: 14 17
 92 ; AFTER ROTATE: 15 CARRY
 93 ;
 94 ; CARRY BIT = STAGE 1
 95 ; LOW ORDER BIT OF 16 BIT REGISTER = STAGE 17
 96 ; *********************************
 97 ;
 98 0039 AE RING: LD A,[B] ; GET RANDOM #
 99 003A B0 RRC A ; ROTATE UPPER BYTE
100 003B A3 X A,[B-]
101 003C AE LD A,[B]
102 003D B0 RRC A ; ROTATE LOWER BYTE
103 003E A6 X A,[B]
104 003F 9804 LD A,#004 ; PERFORM XOR
105 0041 85 AND A,[B]
106 0042 9200 IFEQ A,#000
107 0044 05 JP TSLUP
108 0045 88 IFC
109 0046 02 JP RC
110 0047 A1 SC
111 0048 01 JP TSTLUP
112 0049 A0 RC: RC
113 004A AA TSTLUP: LD A,[B+] ; POINT TO UPPER BYTE
114 004B C9 DRSZ LUPREG ; EXTRACT THIS # ?
115 004C EC JP RING ; NO, KEEP ROTATING
116 004D AE LD A,[B] ; YES
117 004E E1 JP SHIFT
```

```
118 ;
119 ; **** TIMER INTERRUPT ROUTINE ****
120 ;
121 00FF ; .= 0FF
122 00FF BDEF75 IFBIT TPND,PSW ; TEST TIMER PND FLAG
123 0102 02 JP TMOUT
124 0103 2005 JMP XPLOD
125 0105 BDEE6C TMOUT: RBIT TRUN,CNTRL ; STOP TIMER
126 0108 DEFA LD B,#LUPCNT
127 010A C5 DRSZ FIRSTR ; TEST FOR FIRST TONE
128 010B 213B JMP NXT1 ; AND ADJUST
129 010D C8 DRSZ TCNTR ; TEST FOR NEW TONE
130 010E 01 JP NXT ; NO
131 010F 0D JP NEWF
132 0110 D501 NXT: LD FIRSTR,#1 ; DISABLE FIRST TONE REG
133 0112 BDEF7C NXT2: SBIT 4,PSW ; ENABLE TIMER INTERRUPT
134 0115 BDEF6D RBIT 5,PSW ; RESET TPND FLAG
135 0118 5D LD B,#RNGVAL ; POINT TO RANDOM#
136 0119 BDEE7C SBIT TRUN,CNTRL ; RESTART TIMER
137 011C 8F RETI ; RETURN
138 011D C7 NEWF: DRSZ EXITR ; TEST EXIT COUNT
139 011E 10 JP NF ; NO
140 011F C6 DRSZ LASTR ; ENABLE LAST TONE
141 0120 01 JP LST
142 0121 06 JP NLST
143 0122 D709 LST: LD EXITR,#09 ; SET LAST TONE LENGTH
144 0124 BD0078 SBIT 0,TEMP ; SET LAST TONE FLAG
145 0127 0F JP NF2
146 0128 9DFD NLST: LD A,SP ; *** RESTORE STACK POINTER ***
147 012A 9402 ADD A,#002 ; *** FROM TIMER INTERRUPT ***
148 012C 9CFD X A,SP ; *** AND RETURN TO MAIN ***
149 012E 8E RET
150 012F BD0070 NF: IFBIT 0,TEMP ; LAST TONE ?
151 0132 04 JP NF2 ; YES
152 0133 AE LD A,[B] ; NEW TONE
153 0134 9404 NF4: ADD A,#04 ; INCR EXTRACTION VALUE
154 0136 A6 X A,[B]
155 0137 D80A NF2: LD TCNTR,#TCNT ; REINITIALIZE TONE TIME
156 0139 2110 JMP NXT
157 013B D820 NXT1: LD TCNTR,#TCNT1 ; ADJUST FIRST TONE LENGTH
158 013D 2112 JMP NXT2
159 .END
```

Bomb


START
SET WHISTLE FLAG
JSR WHISTLE
RESET WHISTLE FLAG
JSR XPLOD
TIMER INTERRUPT
WHISTLE ?
NO
YES
GENERATE EXPLOSION
RESTORE STACK POINTER (TWO LEVELS)
RET TO CALLING ROUTINE
GENERATE WHISTLE
RETI
AN010716-5

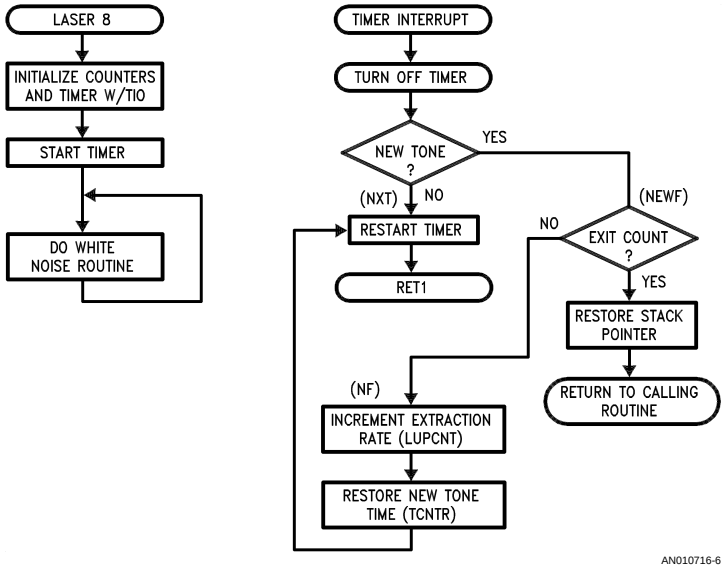
```
1 ;
2 ;
3 ; THE SERIAL INPUT (SI) AND TIMER I/O (TIO) PINS
4 ; MUST BE TIED TO THE SERIAL OUTPUT (SO) PIN.
5 ; OUTPUT IS ON SO.
6 ; USE 20 MHz XTAL, 1 us INSTR CYCLE FOR THIS DEMO.
7 ;
8 ; WRITTEN BY: JERRY LEVENTER
9 ; DATE: OCTOBER 4, 1989
10 ;
11 ;
12 .TITLE BOMB8
13 .CHIP 820
14 ;
15 00D5 PORTGC = 0D5 ; PORT G CONFIGURATION
16 00E9 SIOR = 0E9 ; SIO SHIFT REGISTER
17 00EA TMRLO = 0EA ; TIMER LOW BYTE
18 00EB TMRHI = 0EB ; TIMER HIGH BYTE
19 00EC TAULO = 0EC ; TIMER REGISTER LOW BYTE
20 00ED TAUHI = 0ED ; TIMER REGISTER HIGH BYTE
21 00EE CNTRL = 0EE ; CONTROL REGISTER
22 00EF PSW = 0EF ; PSW REGISTER
23 0004 TRUN = 4
24 0005 TPND = 5
25 0002 BUSY = 2
26 0000 GIE = 0
27 ;
28 ; **** EXPLOSION REGISTERS AND CONSTANTS ****
29 ;
30 ; SOME OF THE FOLLOWING REGISTERS USE THE DRSZ
31 ; TEST AND MUST THEREFORE BE INITIALIED TO AT
32 ; LEAST ”1”.
33 ;
34 00F6 LASTR = 0F6 ; CONTROL LAST TONE
35 0002 LAST = 002 ; LAST TONE CONSTANT
36 0004 LAST2 = 004 ; EXIT CONSTANT
37 00F7 EXITR = 0F7 ; TOTAL TIME TILL EXIT
38 0010 EXIT = 010 ; EXIT CONSTANT
39 00F3 RNGVAL = 0F3 ; HOLDS CURRENT RING VALUE
40 00F8 TCNTR = 0F8 ; TIME FOR EACH TONE FREQ
41 000A TCNT = 0A ; CONSTANT VALUE
42 00F9 LUPREG = 0F9 ; TONE COUNT INSIDE RING
43 00FA LUPCNT = 0FA ; TONE COUNT OUTSIDE RING (VARIABLE)
44 0000 FLAG = 000 ; FLAG REGISTER FOR SUBROUTINES
45 ;
46 00FF TVALO = 0FF
47 001A TVALHI = 01A
48 ;
49 ;**** WHISTLE REGISTERS AND CONSTANTS ****
50 ;
51 002F WSLO = 02F ; TIMER VALUES
52 0000 WSLHI = 000
53 00FF MINFQ = 0FF ; FINAL (LOW FREQ) TIMER VALUE
54 ;
55 00F0 FCNTR = 0F0 ; FREQUENCY COUNT REGISTER
56 0000 FCNT = 000
```

```
 57 ;
 58 ; ********************************
 59 MAIN:
 60 0000 DD2F LD SP,#02F ; DEFAULT INITIALIZATION OF SP
 61 0002 BD0078 SBIT 0,FLAG ; SET SUBROUTINE FLAG
 62 ; 1 = WHISTLE
 63 ; 0 = EXPLOSION
 64 0005 3157 JSR WHISTLE
 65 0007 BD0068 MAIN2: RBIT 0,FLAG
 66 000A 300D JSR BOMB
 67 000C FF JP . ; *** STOP HERE OR REPEAT ***
 68 ; ********************************
 69 ;
 70 000D BCD530 BOMB: LD PORTGC,#030 ; CONFIGURE "SO" AS OUTPUT
 71 0010 BCEE8A LD CNTRL,#08A ; SK = DIV BY 8, PWM ON
 72 0013 BCEF11 LD PSW,#011 ; ENABLE TIMER INTERRUPT
 73 0016 BCEAFF LD TMRLO,#TVALO ; INITIALIZE TIMER
 74 0019 BCEB1A LD TMRHI,#TVALHI
 75 001C BCECFF LD TAULO,#TVALO
 76 001F BCED1A LD TAUHI,#TVALHI
 77 0022 D602 LD LASTR,#LAST ; INITIALIZE LAST TONE FLAG
 78 0024 D710 LD EXITR,#EXIT ; INITIALIZE EXIT COUNT
 79 0026 D80A LD TCNTR,#TCNT ; INITIALIZE TONE COUNT
 80 0028 DA0A LD LUPCNT,#10 ; INITIALIZE FIRST TONE FREQUENCY
 81 002A BD0069 RBIT 1,FLAG ; RESET LAST TONE FLAG BIT
 82 ;
 83 002D A1 NOISE: SC ;
 84 002E DEF3 LD B,#RNGVAL ; POINT TO RING VALUE
 85 0030 9AFF LD [B+],#0FF ; INIT TO ALL ONE'S
 86 0032 9EFF LD [B],#0FF
 87 0034 BDEE7C SBIT TRUN,CNTRL ; START THE TIMER
 88 0037 BEF6A SHIFT: RBIT BUSY,PSW
 89 003A 9CE9 X A,SIOR ; RANDOM # TO SIO
 90 003C BDEF7A SBIT BUSY,PSW
 91 003F 9DFA LD A,LUPCNT ; RESTORE EXTRACTION COUNT
 92 0041 9CF9 X A,LUPREG
 93 ;
 94 ; ********************************
 95 ; RING COUNTER (17 STAGE)
 96 ;
 97 ; THIS IS A SEVENTEEN STAGE RING COUNTER (LINEAR
 98 ; FEEDBACK SHIFT REGISTER) WITH THE RRC COMMAND.
 99 ; THE COUNTER'S 14th AND 17th STAGES THROUGH AN
100 ; EXCLUSIVE-OR SERVE AS THE FEEDBACK FUNCTION.
101 ; THIS 14, 17 RING COUNTER BREAKS DOWN INTO
102 ; 1 CYCLE OF [(2 ** 17) - 1] COUNTS. SINCE THE EXCLUSIVE OR
103 ; OCCURS AFTER THE ROTATE, IT IS THE 15th AND CARRY
104 ; STAGES THAT ARE XOR'D (BIT 2 AND CARRY).
105 ;
106 ; BEFORE ROTATE: 14 17
107 ; AFTER ROTATE: 15 CARRY
108 ;
109 ; CARRY BIT = STAGE ONE
110 ; LOW ORDER BIT = STAGE 17
```

```
111 ; ************************************
112 0043 AE RING: LD A,[B] ; GET RANDOM #
113 0044 B0 RRC A ; ROTATE UPPER BYTE
114 0045 A3 X A,[B-]
115 0046 AE LD A,[B]
116 0047 B0 RRC A ; ROTATE LOWER BYTE
117 0048 A2 X A,[B+]
118 0049 9804 LD A,#004 ; PERFORM XOR
119 004B 85 AND A,[B]
120 004C 9200 IFEQ A,#000
121 004E 05 JP TSTLUP
122 004F 88 IFC
123 0050 02 JP RC
124 0051 A1 SC
125 0052 01 JP TSTLUP
126 0053 A0 RC: RC
127 0054 C9 TSLUP: DRSZ LUPREG ; POINT TO UPPER BYTE
128 0055 ED JP RING ; EXTRACT THIS # ?
129 0056 AE LD A,[B] ; NO, KEEP ROTATING
130 0057 2037 JMP SHIFT ; YES
131 ;
132 ; **** INTERRUPT ROUTINE ****
133 ;
134 00FF .= 0FF
135 00FF BDEF75 IFBIT TPND,PSW ; TEST FOR EXIT
136 0102 01 JP TMOUT
137 0103 FF JP . ; ERROR
138 ;
139 0104 BDEE6C TMOUT RBIT TRUN,CNTRL ; STOP TIMER
140 0107 BD0070 IFBIT 0,FLAG ; BRANCH TO ROUTINE
141 010A 213B JMP WSINT ; SET = WHISTLE, RESET = EXPLOSION
142 ;
143 010C DEFA LD B,#LUPCNT
144 010E C8 DRSZ TCNTR ; TEST FOR NEW TONE
145 010F 01 JP NXT ; NO, DON'T INCREMENT LUPCNT
146 0110 0C JP NEWF ; YES
147 0111 BDEF7C NXT: SBIT 4,PSW ; ENABLE TIMER INTRRUPT
148 0114 BDEF6D RBIT 5,PSW ; RESET TIMER PENDING FLAG
149 0117 DEF3 LD B,#RNGVAL ; POINT TO RANDOM #
150 0119 BDEE7C SBIT TRUN,CNTRL ; RESTART TIMER
151 011C 8F RETI ; RETURN TO RING COUNTER
152 011D C7 NEWF: DRSZ EXITR ; DO LAST TONE ?
153 011E 10 JP NF ; NO
154 011F C6 DRSZ LASTR ; IS LAST TONE DONE?
155 0120 01 JP LST ; NO
156 0121 06 JP NLST ; YES, RETURN TO MAIN
157 0122 D704 LST: LD EXITR,#LAST2 ; LENGTHEN THE LAST TONE
158 0124 BD0079 SBIT 1,FLAG ; SET LAST TONE FLAG
159 0127 0F JP NF2
160 0128 9DFD NLST: LD A,SP ; ** RESTORE STACK POINTER **
161 012A 9402 ADD A,#002 ; ** AND RETURN TO MAIN **
162 012C 9CFD X A,SP
163 012E 8E RET
164 ;
165 012F BD0071 NF: IFBIT 1,FLAG ; LAST TONE ?
166 0132 04 JP NF2 ; YES, DON'T INCREMENT LUPCNT
167 0133 AE LD A,[B] ; NEW TONE
168 0134 9404 ADD A,#04 ; INCR EXTRACT COUNT (LUPCNT)
169 0136 A6 X A,[B]
170 0137 D80A NF2: LD TCNTR,#TCNT ; REINITIALIZE TONE TIME
171 0139 2111 JMP NXT
```

```
172 ; ***********************************
173 013B BDF075 WSINT: IFBIT 5,FCNTR ; READY FOR NEW FREQUENCY ?
174 013E 06 JP TM ; YES
175 013F 9DF0 LD A,FCNTR ; NO, INCREMENT COUNT
176 0141 8A INC A
177 0142 9CF0 X A,FCNTR
178 0144 8D RETSK ; NO, RETURN TO WHISTLE
179 0145 D000 TM: LD FCNTR,#FCNT ; RESET NEW FREQUENCY COUNT
180 0147 DEEC LD B,#TAULO ; POINT TO AUTORELOAD REG
181 0149 AE LD A,[B] ; CHANGE FREQUENCY
182 014A 92FF IFEQ A,#MINFQ ; TIMER = MIN FREQ ?
183 014C 03 JP DONE
184 014D 8A INC A
185 014E A6 X A,[B] ; STORE FREQ IN AUTO RELOAD
186 014F 8D RETSK
187 0150 9DFD DONE: LD A,SP ; ** RESTORE STACK POINTER **
188 0152 9402 ADD A,#002 ; ** AND RETURN TO MAIN **
189 0154 9CFD X A,SP
190 0156 8E RET
191 ; *********************************
192 0157 BCD508 WHISTLE: LD PORTGC,#008 ; TIO PIN (G3) AS OUTPUT
193 015A BCEEA2 LD CNTRL,#0A2 ; PWM WITH TIO TIGGLE, 8Tc
194 015D D000 LD FCNTR,#FCNT ; INIT FREQ COUNTER
195 015F BCEA2F LD TMRLO,#WSLO ; WHISTLE VALUE FOR TIMER
196 0162 BCEB00 LD TMRHI,#WSLHI
197 0165 BCEC2F LD TAULO,#WSLO
198 0168 BCED00 LD TAUHI,#WSLHI
199 ;
200 016B BCEF11 BEGIN LD PSW,#011 ; ENTI, GIE = 1, TPND = 0
201 016E BDEE7C SBIT TRUN,CNTRL ; START TIMER
202 0171 FF JP . ; LOOP UNTIL TIMER INTERRUPT
203 0172 F8 JP BEGIN ; RETURN HERE FROM INTERRUPT
204 .END
```

Laser Gun


LASER 8
INITIALIZE COUNTERS AND TIMER W/TIO
START TIMER
DO WHITE NOISE ROUTINE
TIMER INTERRUPT
TURN OFF TIMER
NEW TONE ?
YES
(NXT)
NO
(NEWF)
RESTART TIMER
NO
EXIT COUNT ?
RET1
YES
RESTORE STACK POINTER
(NF)
RETURN TO CALLING ROUTINE
INCREMENT EXTRACTION RATE (LUPCNT)
RESTORE NEW TONE TIME (TCNTR)
AN010716-6

```
1 ;
2 ; TIMER INTERRUPT IS USED.
3 ; THE SERIAL OUTPUT PIN (SO) AND THE TIO PIN MUST BE
4 ; TIED TOGETHER.
5 ; OUTPUT IS ON SO AND TIO.
6 ;
7 ; TO ALTER THE DURATION OF THE LASER SHOT CHANGE THE
8 ; ″EXIT″ VALUE, HOWEVER, DO NOT EXCEED 03F HEX.
9 ; THE TIMER VALUES (TVALO, TVALHI) COMBINED WITH THE
10 ; TONE COUNT (TNCTR) CAN BE ADJUSTED TO ACHIEVE A
11 ; VARIETY OF SOUNDS.
12 ;
13 ; USE 20 MHz XTAL, 1 us INSTR CYCLE TIME FOR THIS DEMO.
14 ;
15 ;
16 ; WRITTEN BY: JERRY LEVENTER
17 ; DATE: OCTOBER 4, 1989
18 ;
19 ;
20 .TITLE LASER8
21 .CHIP 820
22 ;
23 00D5 PORTGC = 0D5 ; PORT G CONFIGURATION
24 00E9 SIOR = 0E9 ; SIO SHIFT REGISTER
25 00EA TMRLO = 0EA ; TIMER LOW BYTE
26 00EB TMRHI = 0EB ; TIMER HIGH BYTE
27 00EC TAULO = 0EC ; TIMER REGISTER LOW BYTE
28 00ED TAUHI = 0ED ; TIMER REGISTER HIGH BYTE
29 00EE CNTRL = 0EE ; CONTROL REGISTER
30 00EF PSW = 0EF ; PSW REGISTER
31 0004 TRUN = 4
32 0005 TPND = 5
33 0002 BUSY = 2
34 ;
35 ; **** SPECIAL REGISTERS AND COUNTERS ****
36 ; ANY REGISTER THAT IS USED FOR THE DRSZ TEST,
37 ; MUST BE INITIALIZED TO AT LEAST ″1″.
38 ;
39 00F7 EXITR = 0F7 ; ROUTINE DURATION REGISTER
40 003F EXIT = 03F ; EXIT CONSTANT
41 0002 RNGVAL = 002 ; HOLDS CURRENT RANDOM #
42 00F8 TCNTR = 0F8 ; TONE DURATION REGISTER
43 0020 TCNT = 020 ; TONE CONSTANT
44 00F9 LUPREG = 0F9 ; EXTRACTION RATE REGISTER
45 0003 XTRCT = 003 ; EXTRACT CONSTANT
46 00FA LUPCNT = 0FA ; EXTRACTON VARIABLE REGISTER
47 00FF TVAL0 = 0FF ; TIMER VALUES
48 0000 TVALHI = 000
49 ;
50 ;*******************************
51 ;**** BEGIN PROGRAM HERE ****
52 ;*******************************
53 ;
54 0000 MAIN: LD SP,#02F DD2F; DEFAULT INITIALIZATION OF SP
55 0002 LUP: LD EXITR,#EXIT D73F; INITIALIZE SHOT DURATION
56 0004 JSR LASER8 3018; *** LASER CALLING ROUTINE ***
57 0006 LD EXITR,#EXIT D73F
58 0083 JSR LASER8 3018
```

```
 59 000A D73F LD EXITR,#EXIT
 60 000C 3018 JSR LASER8
 61 000E D715 LD EXITR,#015 ; EXIT COUNT CAN BE INITIALIZED
 62 0010 3018 JSR LASER8 ; INSIDE PROGRAM IF SHOT RATE
 63 0012 D715 LD EXITR,#015 ; DOES NOT CHANGE.
 64 0014 3018 JSR LASER8
 65 0016 B8 NOP
 66 0017 EA JP LUP ; **** LOOP FOR DEMO ****
 67 ;
 68 0018 BCD530 LASER8: LD PORTGC,#030
 69 001B BCEEAA LD CNTRL,#0AA ; SK = DIV BY 8, PWM/TIO TIMER
 70 001E BCEF11 LD PSW,#011 ; ENABLE TIMER INTERRUPT
 71 0021 BCEAFF LD TMRLO,#TVALO ; INITIALIZE TIMER
 72 0024 BCEB00 LD TMRHI,#TVALHI
 73 0027 BCECFF LD TAULO,#TVALO
 74 002A BCED00 LD TAUHI,#TVALHI
 75 ; LD EXITR,#EXIT ; INITIALIZE EXIT COUNT
 76 002D D820 LD TCNTR,#TCNT ; INITIALIZE TONE COUNT
 77 002F DA03 LD LUPCNT,#XTRCT ; INITIALIZE EXTRACTION RATE
 78 0031 BDEE7C SBITTRUN,CNTRL ; START TIMER
 79 0034 A1 NOISE: SC ; INIT. STAGE 1
 80 0035 5D LD B,#RNGVAL ; POINT TO RANDOM NUMBER
 81 0036 9EFF LD [B],#0FF ; INIT RANDOM #
 82 0038 9CE9 SHIFT: X A,SIOR ; LOAD AND START SIOR
 83 003A BDEF7A SBIT BUSY,PSW
 84 003D 9DFA LD A,LUPCNT ; RESTORE EXTRACTION COUNT
 85 003F 9CF9 LD A,LUPREG
 86 ;
 87 ; *******************************
 88 ; RING COUNTER
 89 ;
 90 ; THIS IS A NINE STAGE RING COUNTER (LINEAR
 91 ; FEEDBACK SHIFT REGISTER) WITH THE RRC COMMAND.
 92 ; THE COUNTER'S 8th AND 9th STAGES, THROUGH AN
 93 ; EXCLUSIVE-OR SERVE AS THE FEEDBACK FUNCTION.
 94 ; SINCE THE EXCLUSIVE OR OCCURS AFTER THE ROTATE,
 95 ; IT IS THE 1st AND 9th STAGES THAT ARE XOR'D,
 96 ; (THE CARRY FLAG AND BIT 0).
 97 ;
 98 ; CARRY BIT = STAGE 1
 99 ; LOW ORDER BIT = STAGE 9
100 ; *******************************
101 0041 AE RING: LD A,[B] ; GET RANDOM #
102 0042 B0 RRC A ; ROTATE UPPER BYTE
103 0043 A6 X A,[B] ;
104 0044 9800 LD A,#000 ; PERFORM XOR
105 0046 85 AND A,[B]
106 0047 9200 IFEQ A,#000
107 0049 05 JP TSTLUP
108 004A 88 IFC
109 004B 02 JP RC
110 004C A1 SC
111 004D 01 JP TSTLUP
112 004E A0 RC: RC
```

```
113 004F C9 TSTLUP: DRSZ LUPREG ; EXTRACT THIS # ?
114 0050 F0 JP RING ; NO, KEEP ROTATING
115 0051 AE LD A,[B] ; YES
116 0052 E5 JP SHIFT
117 ;
118 ; **** TIMER INTERRUPT ROUTINE ****
119 ;
120 00FF .= 0FF
121 00FF BDEF75 IFBIT TPND,PSW ; TEST TIMER PND FLAG
122 0102 01 JP TMOUT
123 0103 FF JP . ; ERROR
124 ;
125 0104 BDEE6C TMOUT: RBIT TRUN,CNTRL ; STOP TIMER
126 0107 DEFA LD B,#LUPCNT
127 0109 C8 DRSZ TCNTR ; TEST FOR NEW TONE
128 010A 01 JP NXT ; NO
129 010B 0B JP NEWF
130 010C BDEF7C NXT: SBIT 4,PSW ; ENABLE TIMER INTERRUPT
131 010F BDEF6D RBIT 5,PSW ; RESET TPND FLAG
132 0112 5D LD B,#RNGVAL ; POINT TO RANDOM #
133 0113 BDEE7C SBIT TRUN,CNTRL ; RESTART TIMER
134 0116 8F RETI ; RETURN
135 0117 C7 NEWF: DRSZ EXITR ; EXIT COUNT = 0 ?
136 0118 07 JP NF ; NO
137 0119 9DFD NLST: LD A,SP ; *** RESTORE STACK POINTER ***
138 011B 9402 ADD A,#002 ; *** FROM TIMER INTERRUPT ***
139 011D 9CFD X A,SP ; *** AND RETURN TO MAIN ***
140 011F 8E RET
141 0120 AE NF: LD A,[B] ; NEW TONE
142 0121 9404 ADD A,#04 ; INCR EXTRACTION VALUE
143 0123 A6 X A,[B]
144 0124 D820 LD TCNTR,#TCNT ; REINITIALIZE TONE TIME
145 0126 E5 JP NXT
146 .END
```

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