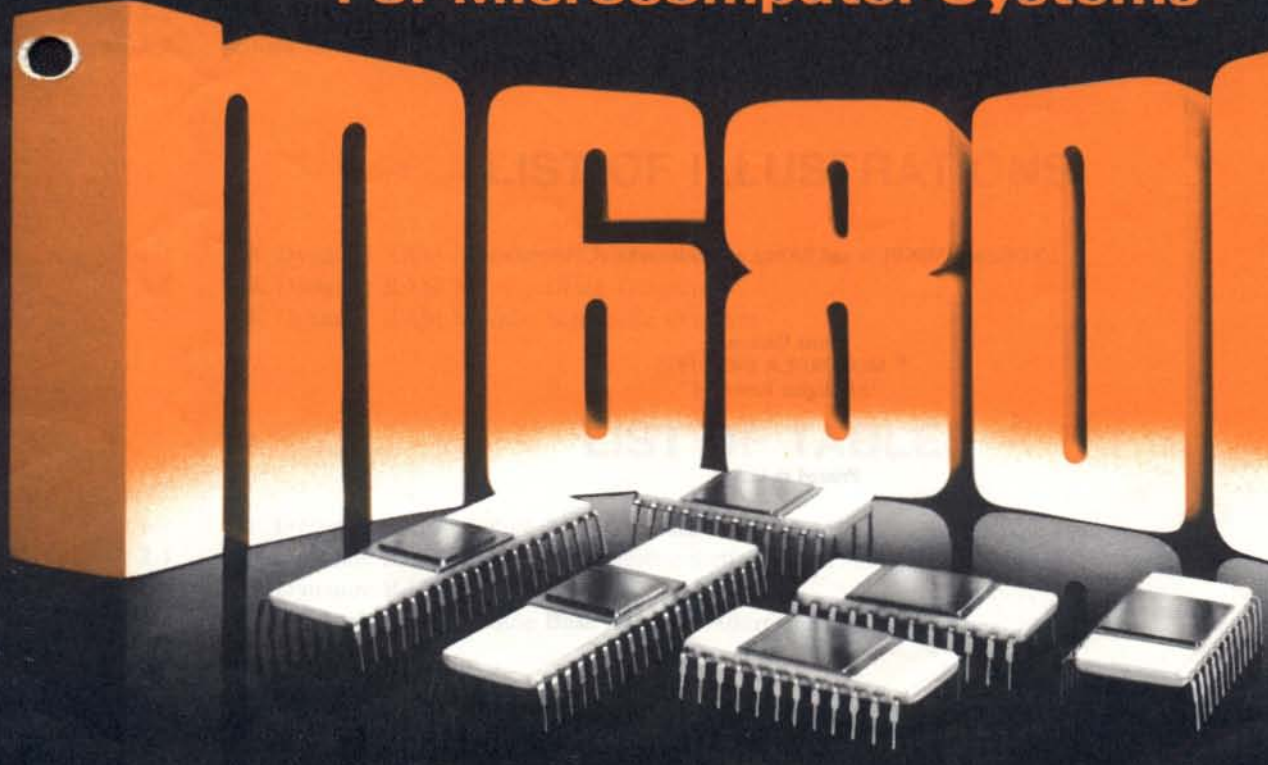
MOTOROLA

MEX6815-1 8K DYNAMIC RAM MODULE SUPPLEMENT

M6800 EXORciser User's Guide

Benchmark Family For Microcomputer Systems

M6800



by Support Products Group

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CHAPTER 1 GENERAL DESCRIPTION

1-1 DESCRIPTION

This manual is a supplement to the M6800 EXORciser User's Guide and provides general information, preparation for use, installation instructions, programming considerations, and theory of operation for the optional MEX6815-1 8K Dynamic RAM Module. A typical module is illustrated in Figure 1-1.

1-2 FEATURES

The features of the 8K Dynamic RAM Module include:

- TTL voltage compatible
- 8192 × 8 bits of dynamic MOS memory in two 4k byte arrays
- Switch selectable base location address for each RAM array
- Switch selectable RAM/ROM (inhibited memory write function) capability for each array
- Cycle stealing memory refresh operation
- Memory refresh capability during power-fail condition when using external power source.
- Bus driver capability

1-3 SPECIFICATIONS

The specifications for the MEX6815-1 8K Dynamic RAM Module are identified in Table 1-1.

1-4 GENERAL DESCRIPTION

The MEX6815-1 8K Dynamic RAM Module, consisting of sixteen MCM6605L-1 n-channel MOS memory circuits, provides the EXORciser with 8,192 bytes of dynamic random access memory. This memory is organized into two separate 4096 byte memory arrays. The module's base memory address switches permit the user to select the base memory address for each memory array in 4k byte increments (0000, 4096, 8192, etc.). The ROM/RAM switch for each memory array permits its respective memory array to be used as RAM or pseudo ROM (inhibiting the memory write function).

The 8K Dynamic RAM Module, using an external battery backup circuit, has the capability of refresh-

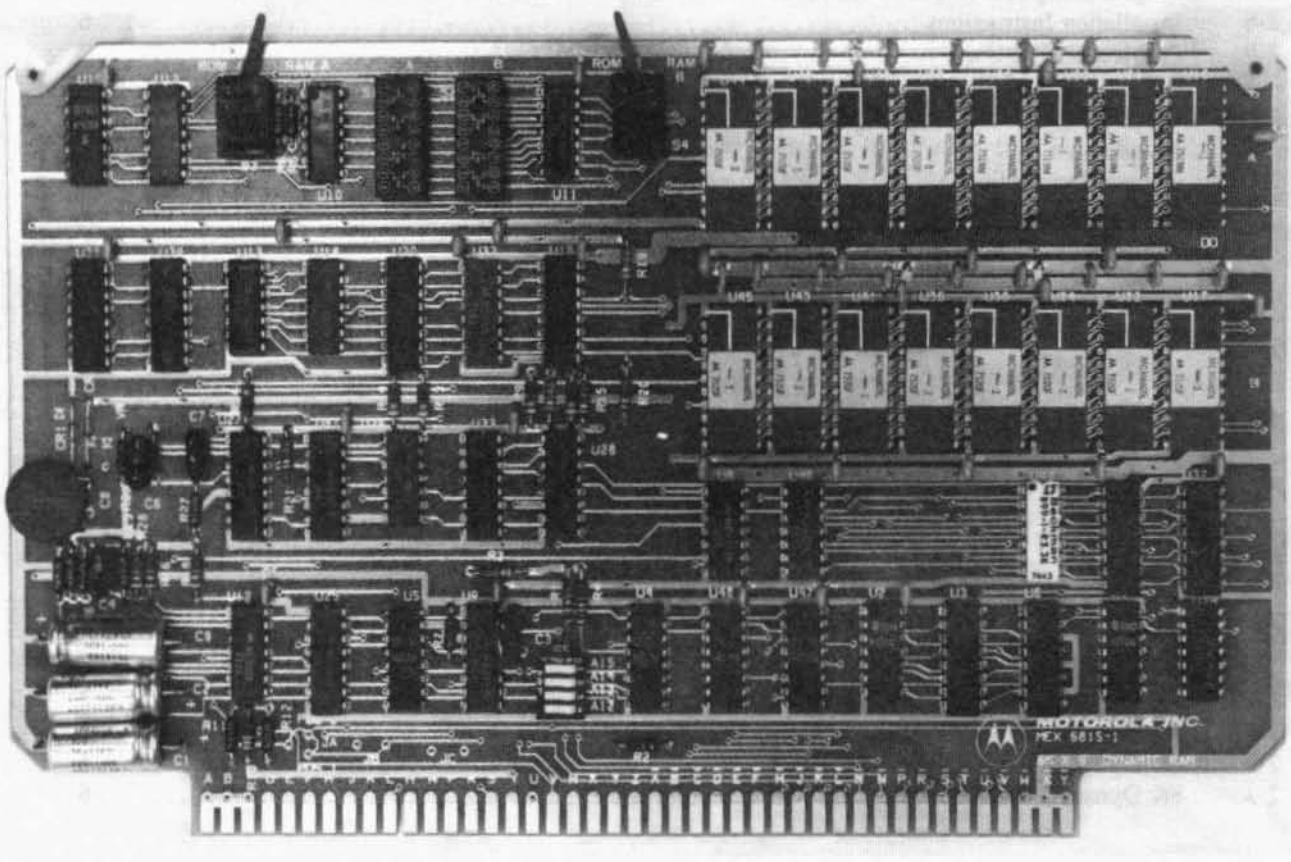

FIGURE 1-1. MEX6815-1 8K Dynamic RAM Module

ing itself while power is removed from the EXORciser power supply. This refresh capability enables the module to retain its stored data during the power loss.

1-5 EQUIPMENT SUPPLIED

The optional MEX6815-1 8K Dynamic RAM Module is shipped with its supplement to the EXORciser User's Guide.

TABLE 1-1. 8K Dynamic RAM Module Specifications

CHARACTERISTICS	SPECIFICATION
Type Memory	N-Channel MOS Dynamic RAM
Memory Organization	8192 × 8 bits organized into two 4096 × 8 bit arrays
Read Access Time	350 ns from memory clock
Cycle Time	750 ns
Input Signals	TTL voltage compatible
Data Bus	Three-state TTL voltage compatible
Dimensions	
Width	9.75 in.
Height	5.75 in.
Thickness	0.062 in.
Power Requirements Operating	+5 VDC @ 860 mA +12 VDC @ 300 mA*
Powerfail Refresh	+5 VDC — not used +12 VDC @ 25 mA

*Power consumption is dependent on the number of memory accesses of the module. In cases where multiple 8K Dynamic RAM Modules are being used, the +12 VDC power consumption will be less than the number of modules times 300 mA.

CHAPTER 2
INSTALLATION INSTRUCTIONS AND PROGRAMMING CONSIDERATIONS

2-1 INTRODUCTION

This chapter provides the unpacking, inspection, installation, and preparation for use instructions for the MEX6815-1 8K Dynamic RAM Module. This chapter also discusses the module's bus interconnection signals, the function of the module's switches, and the module's programming considerations.

2-2 UNPACKING INSTRUCTIONS

The user may receive the 8K Dynamic RAM Module as part of his M6800 EXORciser or as an individual unit. In the case where the 8K Dynamic RAM Module is shipped as part of the M6800 EXORciser, the unpacking instructions are discussed in the M6800 EXORciser User's Guide. If, on the other hand, the 8K Dynamic RAM Module was shipped as an individual unit, unpack in accordance with the following paragraph.

Unpack the 8K Dynamic RAM Module from its shipping carton and, referring to the packing list, verify that all the parts are present. Save the packing material for storing the module. If the shipping carton is damaged upon receipt, request that the carrier's agent be present while the module is being unpacked and inspected.

2-3 INSPECTION

The 8K Dynamic RAM Module should be inspected upon receipt and at periodic intervals. It is a good practice, however, to visually inspect the module whenever it is removed from the EXORciser. Inspect the module for broken, damaged, or missing parts and the printed circuit board for physical damage.

2-4 EXORciser BUS INTERCONNECTIONS

The 8K Dynamic RAM Module interconnects directly with the EXORciser's bus. The bus signals are identified in Table 2-1. This table lists each of the pin connections, the signal's mnemonics and the signals characteristics.

TABLE 2-1. 8K Dynamic RAM Module Bus Interconnections

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A	+5 VDC	+5 VDC used for the module's logic circuits
B	+5 VDC	+5 VDC used for the module's logic circuits
C	+5 VDC	+5 VDC used for the module's logic circuits
D	IRQ	Not used
E	NMI	Not used
F	VMA	Not used
H	± 12 V GND	Not used
J	Ø2	Not used
K	± 12 V GND	Not used
L	MEMCLK	MEMORY CLOCK (MEMCLK) — This is the basic clock signal used by the MPU Module to generate its $\phi 1$ and $\phi 2$ clock signals. The 8K dynamic RAM Module uses this signal to control its timing.
M	− 12 V	Not used
N		Not used
P		Not used
R		Not used
S	REF CLOCK	REFRESH CLOCK (REFCLOCK) — This line may be used as an input line or an output line depending on the jumper connections on the module. Refer to Paragraph 3.3 for details on this signal.
T	+ 12 V	Not used
U	BAT +12	BATTERY +12 VOLTS (BAT +12) — This line in normal EXORciser operation is +12 VDC from the EXORciser power supply. If the EXORciser is using battery backup and the power supply is turned off or a powerfail should occur, the power backup places +12 VDC on this line.
V	$\overline{\text{STDBY}}$	STANDBY ($\overline{\text{STDBY}}$) — This line is a low level during a powerfail condition and a high level during normal EXORciser operation.
W		Not used
X		Not used
Y		Not used
Z		Not used
$\overline{\text{A}}$		Not used
$\overline{\text{B}}$		Not used
$\overline{\text{C}}$		Not used
$\overline{\text{D}}$		Not used
$\overline{\text{E}}$		Not used
$\overline{\text{F}}$		Not used
$\overline{\text{H}}$	$\overline{\text{D3}}$	DATA BUS ($\overline{\text{D3}}$) — This bi-directional line, when enabled, provides a two-way data transfer between the M6800 MPU Module and the 8K Dynamic RAM Module. The data bus drivers and receivers on this module are in their off or high-impedance state except when the module is selected during a memory read or write operation.
$\overline{\text{J}}$	$\overline{\text{D7}}$	DATA BUS ($\overline{\text{D7}}$) — Same as $\overline{\text{D3}}$ on P1-$\overline{\text{H}}$
$\overline{\text{K}}$	$\overline{\text{D2}}$	DATA BUS ($\overline{\text{D2}}$) — Same as $\overline{\text{D3}}$ on P1-$\overline{\text{H}}$

TABLE 2-1 (continued)

$\overline{L}$	$\overline{D6}$	DATA BUS ($\overline{D6}$) — Same as $\overline{D3}$ on P1-$\overline{H}$
$\overline{M}$	A14	ADDRESS BUS (A14) — This address line, when enabled, transfers the MPU program counter output to the 8K Dynamic RAM Module.
$\overline{N}$	A13	ADDRESS BUS (A13) — Same as A14 on P1-$\overline{M}$
$\overline{P}$	A10	ADDRESS BUS (A10) — Same as A14 on P1-$\overline{M}$
$\overline{R}$	A9	ADDRESS BUS (A9) — Same as A14 on P1-$\overline{M}$
$\overline{S}$	A6	ADDRESS BUS (A6) — Same as A14 on P1-$\overline{M}$
$\overline{T}$	A5	ADDRESS BUS (A5) — Same as A14 on P1-$\overline{M}$
$\overline{U}$	A2	ADDRESS BUS (A2) — Same as A14 on P1-$\overline{M}$
$\overline{V}$	A1	ADDRESS BUS (A1) — Same as A14 on P1-$\overline{M}$
$\overline{W}$	GND	GROUND
$\overline{X}$	GND	GROUND
$\overline{Y}$	GND	GROUND
1	+5 VDC	+5 VDC used for the module's logic circuits
2	+5 VDC	+5 VDC used for the module's logic circuits
3	+5 VDC	+5 VDC used for the module's logic circuits
4		Not used
5	RESET	Not used
6	R/W	READ/WRITE (R/W) — This MPU output signal indicates to the 8K Dynamic RAM whether the MPU is performing a memory read (high) or write (low) operation. The normal standby state of this signal is read (high). Also, when the MPU is halted, this signal will be in the read state.
7		Not used
8	-12V	Not used
9	GND	Not used
10	VUA	VALID USER'S ADDRESS (VUA) — This signal indicates that the address on the address bus is valid and the EXORciser is not addressing its EXbug program.
11	-12V	Not used
12	$\overline{REFREQ}$	REFRESH REQUEST ($\overline{REFREQ}$) — This signal, when present, initiates a memory refresh cycle of the modules memory. Refer to Paragraph 3-3.
13	REFGRANT	REFRESH GRANT (REFGRANT) — This signal, when present, instructs the 8K Dynamic RAM Module to refresh its memory.
14		Not used
15		Not used
16	+12V	Not used
17	BAT +12	BATTERY +12 VOLTS (BAT +12) — This line in normal EXORciser operation is +12 VDC from the EXORciser power supply. If the EXORiser is using battery backup and the power supply is turned off or a powerfail should occur, the power backup places +12 VDC in this line.
18		Not used
19		Not used
20		Not used
21		Not used
22		Not used
23		Not used

TABLE 2-1 (continued)

24		Not used
25		Not used
26		Not used
27		Not used
28		Not used
29	$\overline{D1}$	DATA BUS ($\overline{D1}$) — Same as $\overline{D3}$ on $\overline{P1\text{-}H}$
30	$\overline{D5}$	DATA BUS ($\overline{D5}$) — Same as $\overline{D3}$ on $\overline{P1\text{-}H}$
31	$\overline{D0}$	DATA BUS ($\overline{D0}$) — Same as $\overline{D3}$ on $\overline{P1\text{-}H}$
32	$\overline{D4}$	DATA BUS ($\overline{D4}$) — Same as $\overline{D3}$ on $\overline{P1\text{-}H}$
33	A15	ADDRESS BUS (A15) — Same as A14 on P1-$\overline{M}$
34	A12	ADDRESS BUS (A12) — Same as A14 on P1-$\overline{M}$
35	A11	ADDRESS BUS (A11) — Same as A14 on P1-$\overline{M}$
36	A8	ADDRESS BUS (A8) — Same as A14 on P1-$\overline{M}$
37	A7	ADDRESS BUS (A7) — Same as A14 on P1-$\overline{M}$
38	A4	ADDRESS BUS (A4) — Same as A14 on P1-$\overline{M}$
39	A3	ADDRESS BUS (A3) — Same as A14 on P1-$\overline{M}$
40	A0	ADDRESS BUS (A0) — Same as A14 on P1-$\overline{M}$
41	GND	GROUND
42	GND	GROUND
43	GND	GROUND

2-5 MODULE SWITCH LOCATIONS

Figure 1-1 identifies the location of the switches on the 8K Dynamic RAM Module and Table 2-2 identifies the function of each of these switches.

2-6 MASTER/SLAVE 8K DYNAMIC RAM MODULE JUMPER CONNECTIONS

The EXORciser may be using one or multiple 8K Dynamic RAM Modules in a system configuration. If you are using only one 8K Dynamic RAM Modules in your system, configure it in accordance with Paragraph 2-6.1 and if you are using multiple modules, configure one module (master) in accordance with Paragraph 2-6.1 and the remaining modules (slaves) in accordance with Paragraph 2-6.2

2-6.1 MASTER JUMPER CONNECTIONS

The master 8K Dynamic RAM Module has the capability of refreshing itself on a MPU clock cycle stealing basis. In a system using multiple 8K Dynamic RAM

TABLE 2-2. 8K Dynamic RAM Module Switches

SWITCH (REF DES)	DESCRIPTION
MSB (S1)	The MSB hexadecimal switch selects from bits A12 through A15 and their complements the base memory address for memory block 1.
ROM/RAM (S3)	The ROM/RAM switch enables the user to use memory block 1 as RAM or ROM memory. This switch in its ROM position inhibits the module's capability of writing into this memory block.
ROM/RAM (S4)	The ROM/RAM switch enables the user to use memory block 2 as RAM or ROM memory. This switch in its ROM position inhibits the module's capability of writing into this memory block.
MSB (S2)	The MSB hexadecimal switch selects from bits A12 through A15 and their complements the base memory address for memory block 2.
A12-A15 (S5)	The address line select switches enable the user to simulate his system by enabling the address lines he uses in his system and disabling the address lines he is not using.

Modules, one module is set up as master to control the refresh of all of these modules.

Prepare the master module jumper connections as follows:

(a) Remove jumper JA position 2.

(b) Install jumpers JA position 1, JB, and JC.

2-6.2 SLAVE JUMPER CONNECTIONS

In a system using multiple 8K Dynamic RAM Modules, the slave module's memory refresh is controlled by the master module.

Prepare the slave module jumper connections as follows:

(a) Remove jumpers JA position 1, JB, and JC.

(b) Install jumper JA position 2.

2-7 PROGRAMMING CONSIDERATIONS

The programming considerations in this paragraph are a supplement to the M6800 EXORciser User's Guide and discuss only the specific programming considerations for this module.

2-7.1 MODULE PROGRAMMING CONSIDERATIONS

The 8K Dynamic RAM Module provides the EXORciser with 8192 bytes of random access memory arranged into two separate 4096 byte memory blocks. Switches S1 and S2 on the module allow the user to select the base memory address for the switches respective memory blocks. The ROM/RAM switches S3 and S4 determine whether their respective memory blocks, once loaded, are to be used as RAM or pseudo ROM (inhibiting the memory write capability) memory. Switch S5 allows the user to simulate systems not using all 16 lines by permitting the user to enable and disable these lines.

2-7.2 PROGRAMMING PROCEDURES

In preparing the program for his system the user sets up a memory map and assigns the base memory addresses for the memory and peripheral devices being used in the system. The user now configures his hardware and writes his programs around these memory assignments. Table 2-3 identifies each of the possible base memory address for the 8K Dynamic RAM Module memory blocks.

(a) Construct your memory map and assign the base memory address for each memory on the 8K Dynamic RAM Module.

(b) Set the base memory address switches to the assigned base memory addresses in accordance with Paragraph 2-9.

(c) Set the four address select switches of S5 to the address lines used in the planned user's system and disable the address lines not used.

2-8 INSTALLATION INSTRUCTIONS

Install the 8K Dynamic RAM Module as follows:

TABLE 2-3. 8K Dynamic RAM Module Base Memory Addresses

MEMORY ADDRESS LOCATIONS		SWITCHES
FROM	TO	S1/S2
0000	0FFF	0
1000	1FFF	1
2000	2FFF	2
3000	3FFF	3
4000	4FFF	4
5000	5FFF	5
6000	6FFF	6
7000	7FFF	7
8000	8FFF	8
9000	9FFF	9
A000	AFFF	A
B000	BFFF	B
C000	CFFF	C
D000	DFFF	D
E000	EFFF	E
F000*	FFFF*	F

*Addresses F000 through FFFF are reserved in the EXORciser for EXbug.

(a) If the EXORciser is not using battery backup, place a jumper between pins T and U. If, on the other hand, the EXORciser is using battery back, ensure that there is not a jumper between pins T and U.

(b) Turn the PWR keyswitch on the EXORciser to off.

> CAUTION
> INSERTING AN 8K DYNAMIC RAM MODULE WHILE POWER IS APPLIED TO THE EXORciser MAY RESULT IN DAMAGE TO THE COMPONENTS ON THE MODULE.

(c) Install the module in the selected card slot. This module may be installed in any of the 14 EXORciser card slots.

(d) Turn the PWR keyswitch on the EXORciser to on.

> NOTE
> If the EXORciser is using an external clock signal, this signal must be between 333.3 kHz and 1 MHz.

2-9 PREPARATION FOR USE

Prepare the 8K Dynamic RAM Module as follows:

(a) Refer to Table 2-3 and set the base memory address switch S1 to the selected base memory address for memory block 1.

(b) Refer to Table 2-3 and set the base memory address switch S2 to the selected base memory address for memory blocks.

(c) Prior to loading the user's program into these memory blocks, set the module's ROM/RAM switches S3 and S4 to RAM.

(d) If the data loaded into memory block 1 is to be protected, set its ROM/RAM switch S3 to ROM.

(e) If the data loaded into memory block 2 is to be protected, set its ROM/RAM switch S4 to ROM.

CHAPTER 3 THEORY OF OPERATION

3-1 INTRODUCTION

This chapter provides a block diagram description of the 8K Dynamic RAM Module. A block diagram of the module is illustrated in Figure 3-1 and the schematic diagram is illustrated in Figure 3-2.

3-2 GENERAL DESCRIPTION

The optional 8K Dynamic RAM Module, consisting of 16 MCM6605L-1 n-channel memory devices provides the EXORciser with 8192 bytes of dynamic random access memory. This memory is organized into two separate 4096 byte memory arrays. The module's base memory address switches permit the user to select the base memory address for each memory array in the 4k byte increments (0000, 4096, 8192, etc.). The ROM/RAM switch for each memory array permits its respective memory array to be used as RAM or as pseudo by ROM inhibiting the memory write function. The dynamic memory devices are refreshed on a cycle stealing basis. The module interfaces directly with the EXORciser bus.

The 8K Dynamic RAM Module, using an external battery backup circuit, has the capability of refreshing itself while power is removed from the EXORciser power supply. THIS REFRESH CAPABILITY ENABLES THE MODULE TO RETAIN ITS STORED DATA DURING A POWER LOSS.

3-3 BLOCK DIAGRAM DESCRIPTION

The optional 8K Dynamic RAM Module receives the 16 address lines A0 through A15, a MEMCLK (MEMory CLocK) timing signal, a VUA signal and the R/W (Read/Write) command during each memory operation. During a memory write operation, this module also receives the eight data bits $\overline{D0}$ through $\overline{D7}$. The module applies the address bits to the address bus interface and the MEMCLK, VUA, and R/W inputs to the control bus interface. The address bus interface, after buffering its inputs, applies the five address bits A0 through A4 to the refresh address multiplexer and the seven address bits A5 through A11 to the RAM1 and RAM2 memory arrays. Also incorporated in the address bus interface are the four switches of the address select switch S5. These switches are toggle switches and enable/disable address lines A12 through A15. Disabling individual address lines enables the user to simulate a system not using all of the 16 address lines. The address bus interface applies the resultant four address bits A12 through A15 with their complements from its switches and buffers to the RAM1 and RAM2 select circuits.

The control bus interface, after buffering its inputs, applies the MEMCLK signal to the powerfail circuit, the refresh circuit, and the control logic circuit. This circuit also applies the VUA signal to the RAM select circuits and the R/W command with its complement to the control logic.

The data bus interface provides a two-way data transfer between the RAM memory arrays and the EXORciser bus. The drivers and receiver circuits in the data bus interface are three-state logic devices whose operation is controlled by control logic. When the drivers and receivers are in their disabled or off state, they provide high impedance outputs to their respective busses.

Now, if the EXORciser is not in a power off condition, the powerfail circuit receives a high level $\overline{\text{STDBY}}$ (STanDBY) signal and the BAT +12 (BATtery +12 volt) input. With these inputs the powerfail circuit

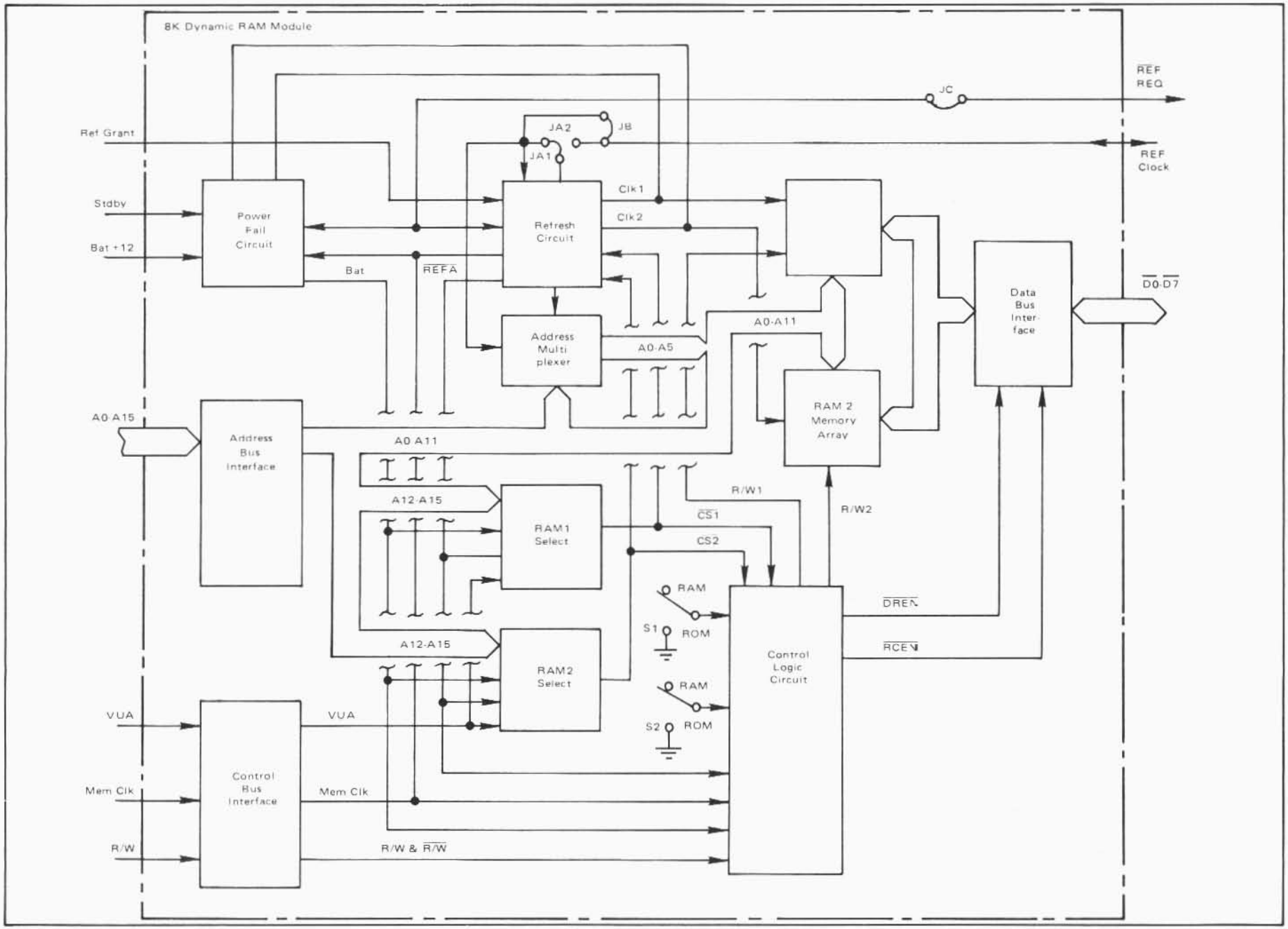

FIGURE 3-1. 8K Dynamic RAM Module Block Diagram

generates a low level BAT (BATtery) signal. This BAT signal enables the RAM select circuits and the control logic circuit to process their input signals. The two RAM select circuits decode their inputs bits and determine whether the MPU is addressing their respective memory arrays. Since the two RAM select circuits and the two RAM memory arrays are identical, only the RAM1 select circuit and the RAM1 memory array are discussed here. The RAM1 select circuit consists of a hexadecimal base memory address switch and a decoding circuit. The base memory address switch selects the base memory address (S1) for RAM1 memory array and the decoding circuit determines when its memory array is being addressed. The RAM1 select circuit, on determining that its memory is being addressed, generates a CS1 (Chip Select 1) signal and applies this signal to the RAM1 memory array. At this time the control logic circuit instructs the RAM1 memory array to perform a memory read or write function.

During a memory read operation the control bus interface circuit receives a high level R/W command and applies this command with its complement to the control logic. The control logic now transfers a high level R/W 1 (Read/Write 1) command to the RAM1 memory array and couples a DREN (DRiver ENable) control signal to the data bus interface. The high level R/W 1 command instructs the RAM1 memory array to perform a memory read operation and the DREN control signal instructs the data bus interface to transfer data from the memory to the EXORciser bus.

During a memory write operation the control bus interface receives a low level R/W command and applies this command with its complement to the control logic. The control logic now couples a $\overline{\text{RCEN}}$ (ReCeiver ENable) control signal to the data bus interface. This $\overline{\text{RCEN}}$ control signal instructs the data bus interface to transfer data from the EXORciser bus to the RAM memory arrays. After a 280 ns delay, the control logic reads the position of ROM/RAM switch S3 and determines whether the RAM1 memory segment is to be protected or to be written into. When this ROM/RAM switch is in the ROM position, this switch inhibits the control logic from initiating a memory write operation. In the RAM position, however, this switch enables the control logic to generate a low level R/W 1 command. This low level command instructs the RAM1 memory array to perform a memory write operation and to store the data it receives from the EXORciser bus via the bus interface circuit.

The RAM memory arrays consist of eight MCM6605L-1 memory devices. Each memory device is organized in 32 columns by 128 rows. Address bits A0 through A4 control the decoding of the 32 memory columns while address bits A5 through A11 select the 128 memory rows. These memory devices must be refreshed every 2 ms.

The 8K Dynamic RAM Module, through its jumper connections, may be used as the master or the slave in a memory refresh operation. All systems, whether they are using only one or several 8K Dynamic RAM Modules, must have one master module controlling the dynamic memory arrays refresh operation. In systems using more than one 8K Dynamic RAM Module, the other modules must be configured to function as slaves in the memory refresh operation. The reason for this approach is that only one module will initiate the memory refresh operation rather than each module initiating its own refresh operation and thus increase the efficiency of the refresh operation. In the refresh operation the master refresh module generates a $\overline{\text{REFREQ}}$ pulse approximately once every 60μs and the MPU Module responds with a REF GRANT. The master refresh module and slave refresh module, using the REF GRANT, refresh themselves and the master refresh module removes the $\overline{\text{REFREQ}}$ signal.

Using an external +12 volt power source, the 8K Dynamic RAM Module refreshs itself when power is removed from the EXORciser. At this time the module will receive a low level STDBY signal and the +12 volt BAT +12 input. The powerfail circuit now applies a high level BAT signal to RAM select circuits and the control logic circuit disabling these circuits from processing their inputs. The powerfail circuit now generates the CLK1 and CLK2 clock pulses during each memory refresh operation.

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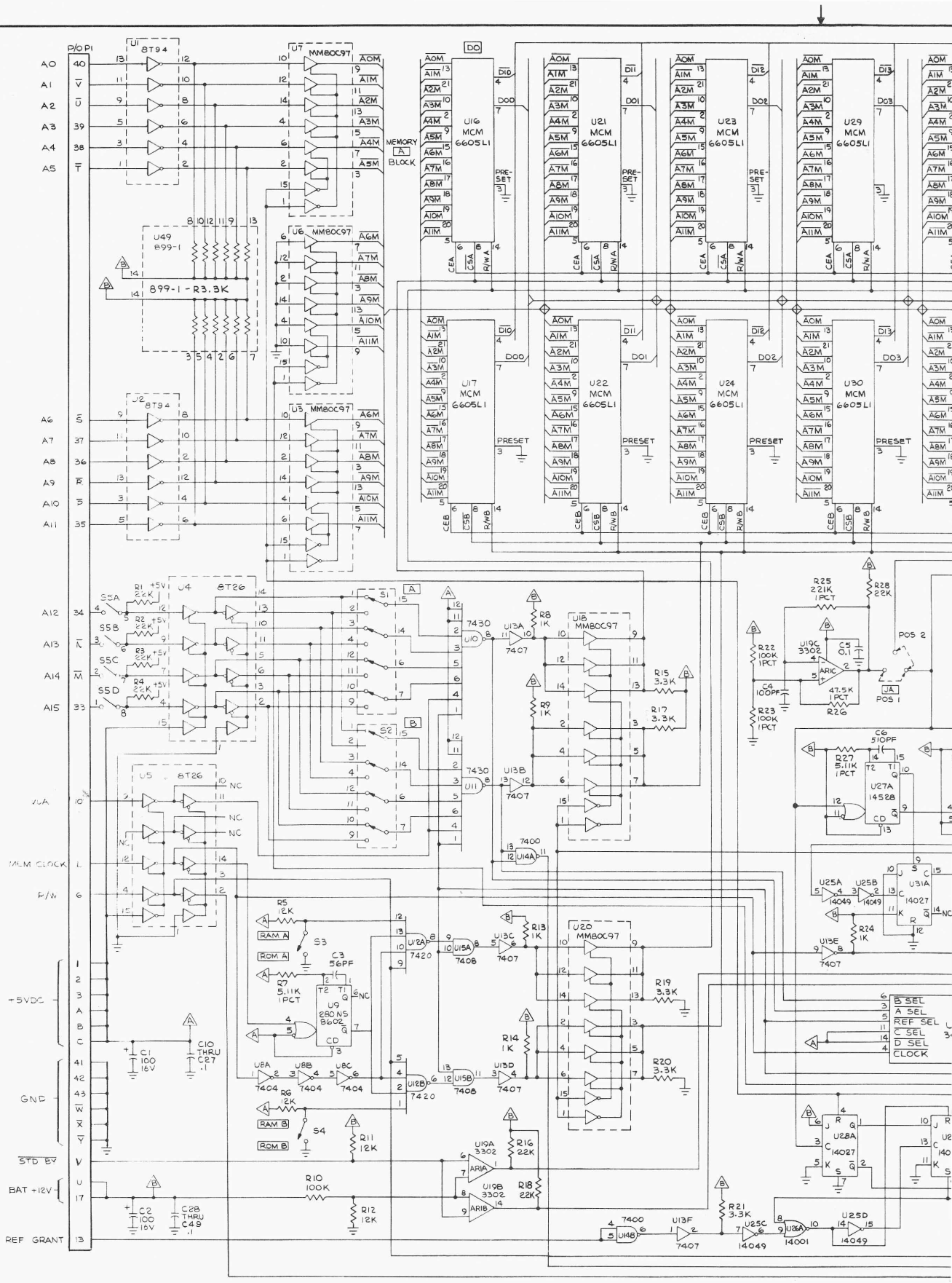


2. TERMINATIONS CODED WITH THE SAME LETTER ARE ELECTRICALLY CONNECTED.
1. ALL RESISTORS ARE IN OHMS, ± 10 PCT, 1/4W. ALL CAPACITORS ARE IN UF UNLESS OTHERWISE SPECIFIED

NOTES:

5. FOR VOLTAGE AND GROUND CONNECTIONS REFER TO TABLE.
4. ☐ DENOTES EQUIPMENT MARKING.
3. SWITCHES S1 AND S2 ARE ROTARY HEXADECIMAL SWITCHS SHOWN IN POSITION ZERO.

NOTES: CONTINUED

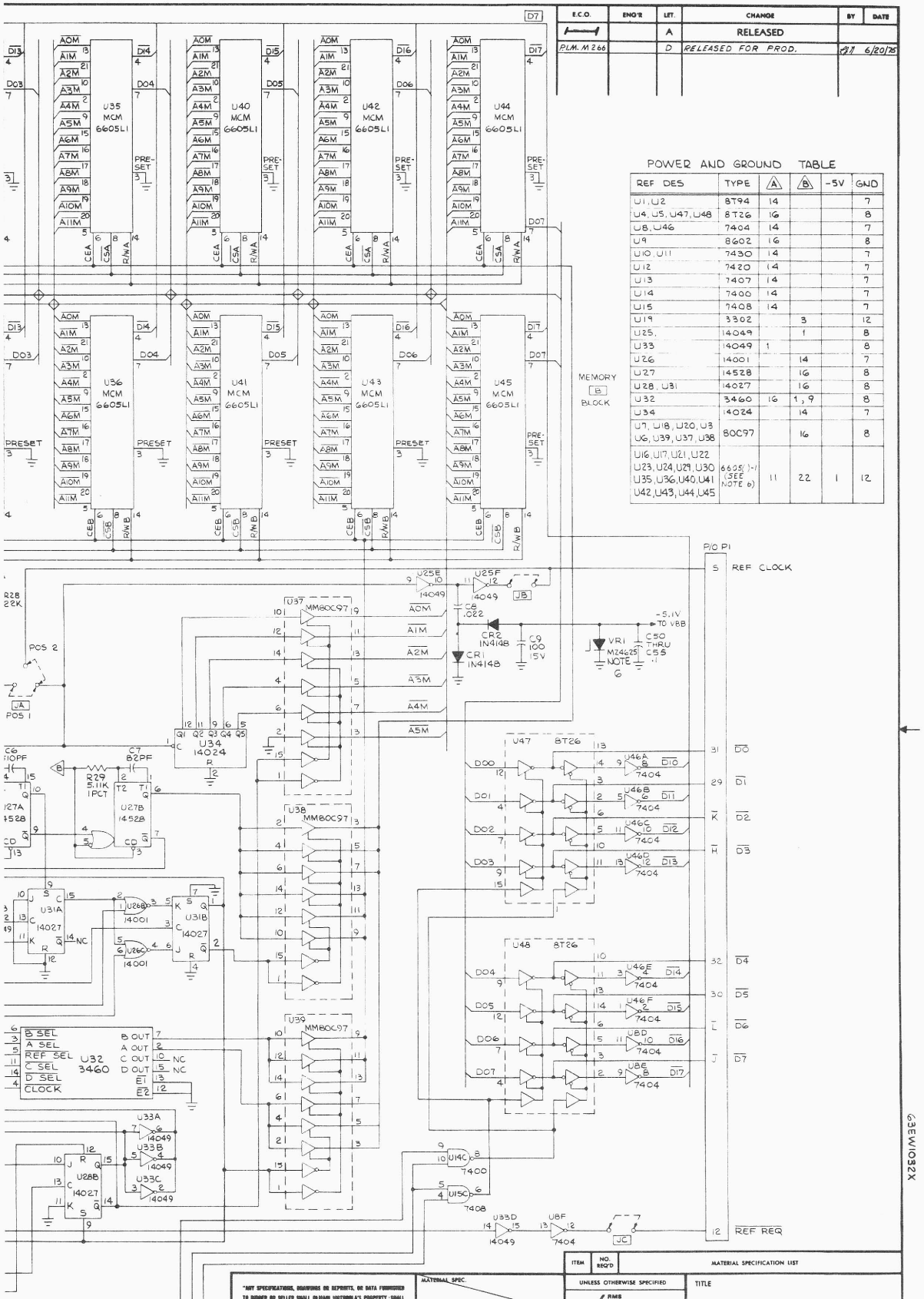
6. SELECT VR1 AS FOLLOWS:
FOR MCM6605L-1 MEMORYS USE MZ4625
FOR MCM6605E-1 MEMORYS USE MZ4625
FOR MCM6605V-1 MEMORYS USE MZ4627

NOTES: CONTINUED

HOLE	QUAN	DESCRIPTION	TRUE UN

HOLE LIST

FIGURE 3-2. MEX6815-1 8K Dynamic RAM Module Schematic Diagram



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		A	RELEASED		
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POWER AND GROUND TABLE

REF DES	TYPE	A	B	-5V	GND
U1, U2	8T94	14			7
U4, U5, U47, U48	8T26	16			8
U8, U46	7404	14			7
U9	8602	16			8
U10, U11	7430	14			7
U12	7420	14			7
U13	7407	14			7
U14	7400	14			7
U15	7408	14			7
U19	3302		3		12
U25,	14049		1		8
U33	14049	1			8
U26	14001		14		7
U27	14528		16		8
U28, U31	14027		16		8
U32	3460	16	1, 9		8
U34	14024		14		7
U7, U18, U20, U3 U6, U39, U37, U38	80C97		16		8
U16, U17, U21, U22 U23, U24, U29, U30 U35, U36, U40, U41 U42, U43, U44, U45	6605(-1 (SEE NOTE 6)	11	22	1	12

ITEM	NO. REQ'D	MATERIAL SPECIFICATION LIST

"ANY SPECIFICATIONS, DRAWINGS OR REPRINTS, OR DATA FURNISHED TO BIDDER OR SELLER SHALL REMAIN MOTOROLA'S PROPERTY, SHALL BE KEPT CONFIDENTIAL, SHALL BE USED FOR THE PURPOSE OF COMPLYING WITH MOTOROLA'S REQUESTS FOR QUOTATION OR WITH MOTOROLA PURCHASE ORDERS AND SHALL BE RETURNED AT MOTOROLA'S REQUEST. PATENT RIGHTS EMBODIED IN DESIGNS, TOOLS, PATTERNS, DRAWINGS, DEVICES, INFORMATION AND EQUIPMENT SUPPLIED BY MOTOROLA PURSUANT TO THIS REQUEST FOR QUOTATION OR PURCHASE ORDER AND EXCLUSIVE RIGHTS FOR THE USE IN REPRODUCTION THEREOF ARE RESERVED BY MOTOROLA."

MATERIAL SPEC.

HEAT TREAT

APPLIED FINISH

THIRD ANGLE PROJECTION

DRAWN BY DEA ENTERPRISES — DATE 5-10-75

CHECKED BY — DATE 6/19

SCALE NONE — REQ'D

UNLESS OTHERWISE SPECIFIED

RMS ALL MACHINED SURFACES

DEC. TOL. .XX ± .XXX ±

MM TOL. .X ± .XX ±

ANGULAR TOL. ±

FEATURE CONTROL SYMBOLS PER USASI Y14.5-1972 CURRENT REV.

BREAK ALL SHARP EDGES & CORNERS. REMOVE BURRS.

UNDERLINE DIMS NOT TO SCALE

TITLE

SCHEMATIC DIAGRAM
MEX6815-1 8K×8 DYNAMIC RAM
EXORciser™ PROGRAM

MOTOROLA INC.
Semiconductor Products Division
3009 EAST McDOWELL ROAD, PHOENIX, ARIZONA 85008

DWG. NO. 63EW1032X

ON — TRUE POSITION TOL. AT M.M.C. UNLESS OTHERWISE SPECIFIED — HOLE LIST

63EW1032X