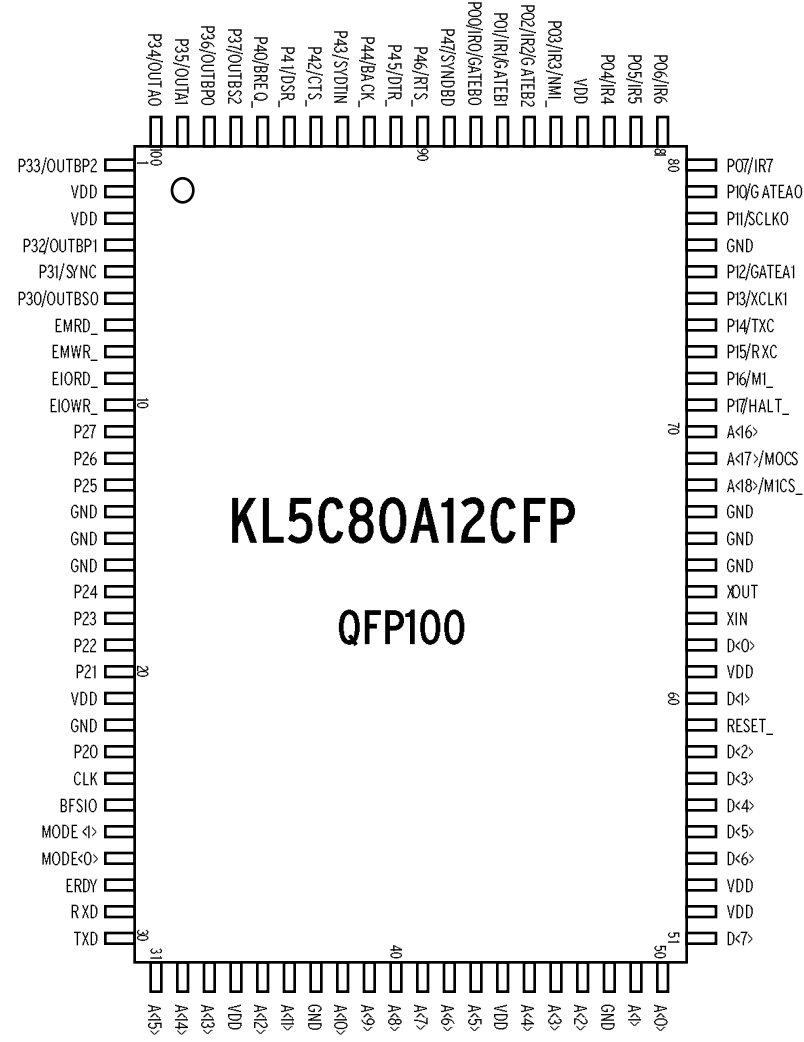# KL5C80A12CFP

■ PIN CONFIGURATION

Fig. 1   KL5C80A12CFP Pin Configuration

KL5C80A12CFP

■ BLOCK DIAGRAM

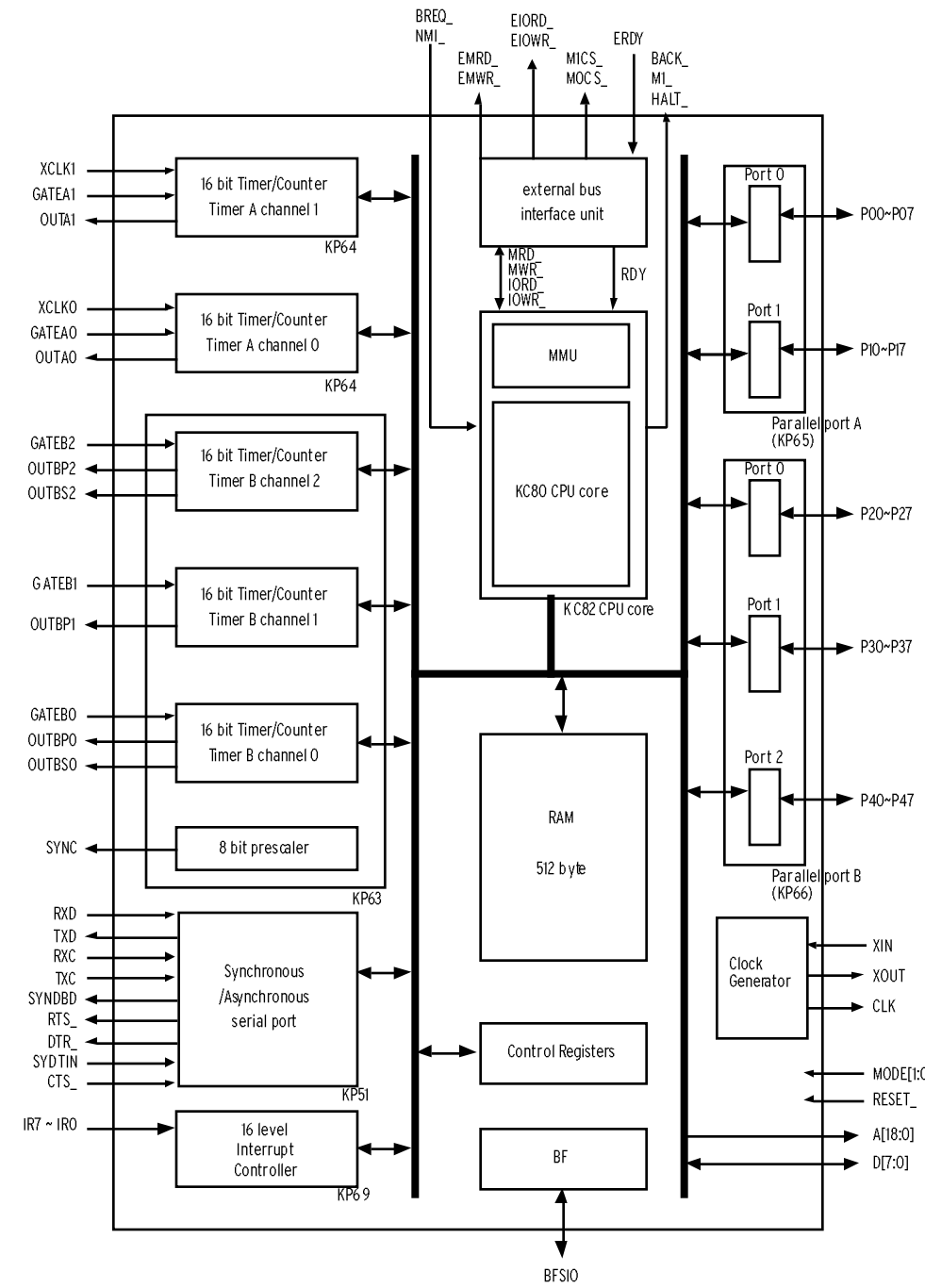Fig. 2   KL5C80A12CFP Block Diagram

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KL5C80A12CFP

■ FUNCTIONS

Address space	512 K byte
CPU registers	8 bit x 16 (general purpose), 16 bit x 4 and 8 bit x 2 (special purpose)
Machine cycle	Min. instruction execution time = 100 nsec.
Instruction set	Z80 fully compatible at binary level.
I/O ports	Total 40 bit (16; bit wise configurable in/out derection, 24; 4-bit wise configurable in/out derection, bit set/reset function for output ports)
Serial interface	Full-duplex USART x 1 channel, MAX baud rate 2Mbps
Timers	16 bit multifunctional timer/counter x 2 channels 16 bit timer/counter x 3 channels with 8 bit prescaler Event, interrupt and interval count, PWM, WDT operation modes
Interrupts	Maskable interrupts 16 inputs (8; external, 8; internal) Non-maskable interrupts 1 input (external), Mode2(vector) interrupt operation Supports multiple interruption
On chip memory	512 byte high speed synchronous RAM (no wait accessible)
Other functions	Clock generator, wait-state controller and embedded debug logic which cooperates with external 'Bug Finder™' system
Package	QFP 100 pin

■ DEBUG TOOLS

Bug Finder	Handy type debug tool from TANAKA Electric Co. (TW-001) and Unitek Electric Co. (UBR-820/830) Supports IBM PC/AT and compatibles as platform.
ADVICE™	ICE from Yokogawa Digital Computer Co.
Partner-ET80™	ROM-ICE from Kyoto Microcomputer Co.
iD 1600A™	ROM-ICE from Computex Co. Full support for KC82 MMU address extension.

■ COMPILERS

LSI-C80 Ver. 3.4	From LSI Japan Co. Linker (knil™) fully supports KC82 MMU address extension.
ICC Z80	From IRA Systems AB Supports KC82 MMU address extension.
HI-TECH C Ver. 7.4	From HI-TECH software Inc. Fully supports KC82 MMU address extension.