MB86601 & MB86602A
Data Sheet
(Timing Diagrams)

Provisional

First Edition

Fujitsu Microelectronics Inc.
Integrated Circuits Division

NO.	I/O	PIN NAME	NO.	I/O	PIN NAME	NO.	I/O	PIN NAME	NO.	I/O	PIN NAME
1	I	$\overline{WR}$	26	I	$\overline{IOWR}$	51	I	$\overline{DACK}$	76	I	A4
2	I	$\overline{RD}$	27	I	$\overline{IORD}$	52	O	DREQ	77	I	$\overline{CS0}$
3	PWR	VDD	28	PWR	VDD	53	PWR	VDD	78	PWR	VDD
4	PWR	VSS	29	PWR	VSS	54	PWR	VSS	79	PWR	VSS
5	I	CLK	30	I	DMA0	55	I	TP	80	I	$\overline{CS1}$
6	I	$\overline{RESET}$	31	I/O	LDMDP	56		(NC)	81	I/O	LDP
7	O	INT	32	I/O	DMD0	57	I	TEST2	82	I/O	D0
8	I	MODE	33	I/O	DMD1	58	I/O	$\overline{I/O}$	83	I/O	D1
9	I/O	$\overline{DBP}$	34	I/O	DMD2	59	PWR	VSS	84	I/O	D2
10	PWR	VSS	35	I/O	DMD3	60	I/O	$\overline{REQ}$	85	I/O	D3
11	I/O	$\overline{DB7}$	36	I/O	DMD4	61	I/O	$\overline{C/D}$	86	I/O	D4
12	I/O	$\overline{DB6}$	37	I/O	DMD5	62	I/O	$\overline{SEL}$	87	I/O	D5
13	I/O	$\overline{DB5}$	38	I/O	DMD6	63	I/O	$\overline{MSG}$	88	I/O	D6
14	PWR	VDD	39	I/O	DMD7	64	PWR	VDD	89	I/O	D7
15	PWR	VSS	40	PWR	VSS	65	PWR	VSS	90	PWR	VSS
16	PWR	VSS	41	I/O	DMD8	66	PWR	VSS	91	I/O	D8
17	I/O	$\overline{DB4}$	42	I/O	DMD9	67	I/O	$\overline{RST}$	92	I/O	D9
18	I/O	$\overline{DB3}$	43	I/O	DMD10	68	I/O	$\overline{ACK}$	93	I/O	D10
19	I/O	$\overline{DB2}$	44	I/O	DMD11	69	I/O	$\overline{BSY}$	94	I/O	D11
20	I/O	$\overline{DB1}$	45	I/O	DMD12	70	PWR	VSS	95	I/O	D12
21	PWR	VSS	46	I/O	DMD13	71	I/O	$\overline{ATN}$	96	I/O	D13
22	I/O	$\overline{DB0}$	47	I/O	DMD14	72	I	A0	97	I/O	D14
23	I	TEST1	48	I/O	DMD15	73	I	A1	98	I/O	D15
24		(NC)	49	I/O	UDMDP	74	I	A2	99	I/O	UDP
25		(NC)	50	I	$\overline{DMBHE}$	75	I	A3	100	I	$\overline{BHE}$

NO.	I/O	PIN NAME	NO.	I/O	PIN NAME	NO.	I/O	PIN NAME	NO.	I/O	PIN NAME
1	O	INIT	26	I	$\overline{IOWR}$	51	I	$\overline{DACK}$	76	I	$\overline{RD}$
2	O	TARG	27	I	$\overline{IORD}$	52	O	DREQ	77	I	$\overline{BHE}$
3	PWR	VDD	28	PWR	VDD	53	PWR	VDD	78	PWR	VDD
4	PWR	VSS	29	PWR	VSS	54	PWR	VSS	79	I	$\overline{CS0}$
5	I	CLK	30	I	DMA0	55	I	TP	80	I	$\overline{CS1}$
6	I	$\overline{RESET}$	31	I/O	LDMDP	56	I/O	LDP	81	I	A0
7	O	DBOEP	32	I/O	DMD0	57	I/O	D0	82	I	A1
8	I/O	DBP	33	I/O	DMD1	58	I/O	D1	83	I	A2
9	O	DBOE7	34	I/O	DMD2	59	I/O	D2	84	I	A3
10	I/O	DB7	35	I/O	DMD3	60	I/O	D3	85	I	A4
11	O	DBOE6	36	I/O	DMD4	61	I/O	D4	86	O	INT
12	I/O	DB6	37	I/O	DMD5	62	I/O	D5	87	I	MODE
13	O	DBOE5	38	I/O	DMD6	63	I/O	D6	88	I/O	ATN
14	I/O	DB5	39	I/O	DMD7	64	I/O	D7	89	I/O	ACK
15	PWR	VSS	40	PWR	VSS	65	PWR	VSS	90	PWR	VSS
16	O	DBOE4	41	I/O	DMD8	66	I/O	D8	91	I/O	REQ
17	I/O	DB4	42	I/O	DMD9	67	I/O	D9	92	I/O	MSG
18	O	DBOE3	43	I/O	DMD10	68	I/O	D10	93	I/O	C/D
19	I/O	DB3	44	I/O	DMD11	69	I/O	D11	94	I/O	I/O
20	O	DBOE2	45	I/O	DMD12	70	I/O	D12	95	I	BSYI
21	I/O	DB2	46	I/O	DMD13	71	I/O	D13	96	O	BSYO
22	O	DBOE1	47	I/O	DMD14	72	I/O	D14	97	I	SELI
23	I/O	DB1	48	I/O	DMD15	73	I/O	D15	98	O	SELO
24	O	DBOE0	49	I/O	UDMDP	74	I/O	UDP	99	I	RSTI
25	I/O	DB0	50	I	$\overline{DMBHE}$	75	I	$\overline{WR}$	100	O	RSTO

• Electrical Characteristics

1. Absolute Maximum Rating

Items	Symbols	Rating	U/M
Power source voltage	V_{DD}	Vss-0.5 ~ 6.0	V
Input voltage	V_I	Vss-0.5 ~ VDD + 0.5	
Output voltage	V_0	Vss-0.5 ~ VDD + 0.5	
Storage Temperature	T_{STG2}	-40 ~ +125	°C

Maximum rating is the limit that may not be exceeded even momentarily.

More specifically, operating within the maximum ratings guarantee that the device will not be permanently damaged. However, this does not guarantee normal logic operations.

2. Recommended Operational Conditions

Items	Symbols	Recommended Value		U/M
		Minimum	Maximum	
Power source voltage	V_{DD}	4.75	5.25	V
Input voltage	V_{IH}	2.2	------	
	V_{IL}	-----	0.8	
Operational temperature	T_A	0	70	°C

3. DC Characteristics
(V_{DD}= 5V ± 5%, V_{SS}=0V, T_A=0~70 degrees C)

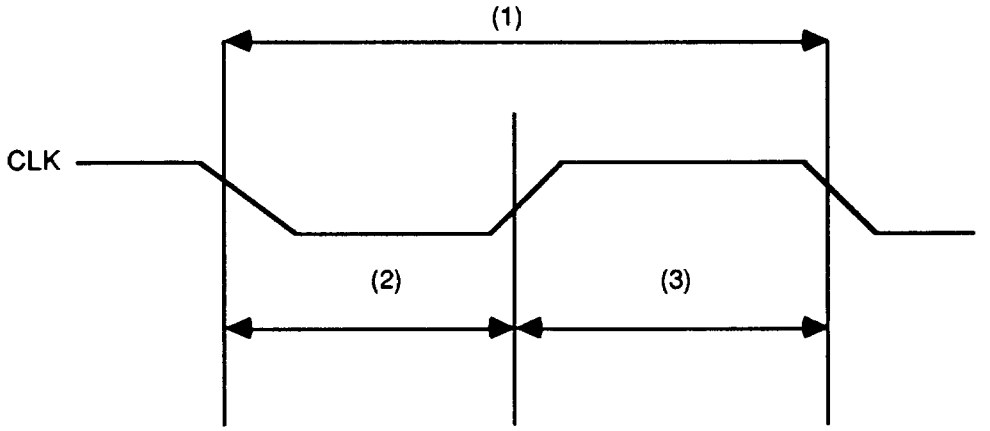
Items		Symbols	Require-ments	Rating		U/M
				Min.	Max.	
Input voltage	Non-SCSI pins	VIH	-----	2.2	----	V
		VIL	-----	----	0.8	
	SCSI pins (MB86601 only)	VIH	-----	2.0	----	
		VIL	-----	----	0.8	
SCSI pin input hysteresis		VHW	-----	0.2	----	
Output voltage	Non-SCSI pins	VOH	1 OH=-2.0mA	4.2	VDD	
		VOL	Iol= +3.2mA	Vss	0.4	
	SCSI pins (REQ/ACK pins only for MB86601)	VOH	ioh=-8.0mA	2.5	----	
		VOL	Iol=+48.0mA	----	0.5	
	SCSI pins (MB86601 only)	VOL	Iol=+48.0mA	----	0.5	
Current Leakage	Non-SCSI pins	ILI	Vin=0~VDD	-10	10	µA
		ILZ	Vin=0~VDD	-10	10	
	SCSI pins (MB86601 only)	ILI	Vin=0~VDD	-10	10	
		ILZ	Vin=0~VDD	-10	10	

Note 1) A SCSI pins consists of a total of 18-pins for DB7 ~ DBO, DBP, BSY, SEL, RST, ATN, REQ, ACK, MSG, C/D, and I/O.

Note 2) Current leakage denotes the following:
(1) current input at the input device
(2) current leakage during the output high impedance state for 3-state output devices
(3) current leakage during the output high impedance state (input state) for bi-directional bus devices.

- AC Characteristics

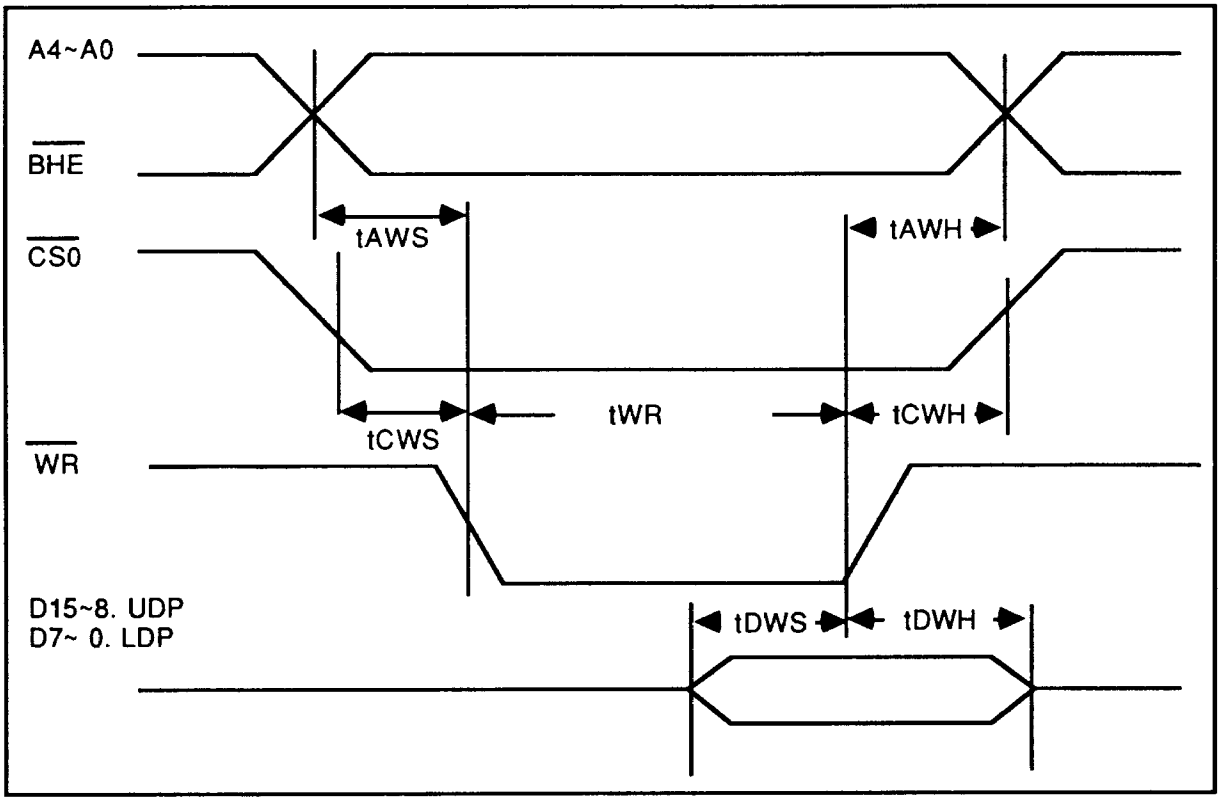
1. CLK Cycle



	Items	Rating			U/M
		MIN	TYP	MAX	
(1)	Clock cycle (tCLF)	31.25	——	125	ns
(2)	Clock Pulse Width (LOW)	10.0	——	——	
(3)	Clock Pulse Width (HIGH)Items	10.0	——	——	

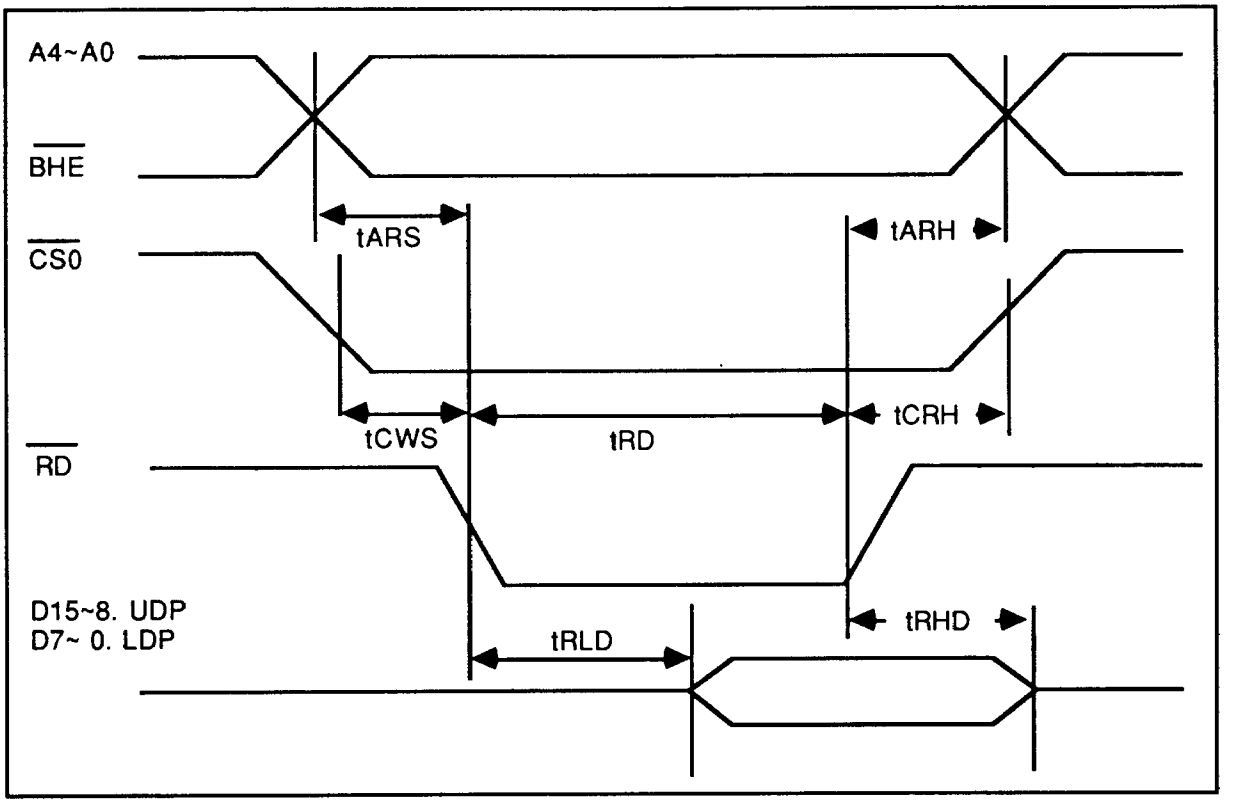
2-1-1. Writing in Register (80-Family)

Items	Symbols	Rating		U/M
		Min	Max	
Address Set-up	tAWS	40	------	ns
Address Hold	tAWH	20	------	
$\overline{\text{CSO}}$ Set-up	tCWS	20	------	
$\overline{\text{CSO}}$ Hold	tCWH	10	------	
Data Bus Set-up	tDWS	40	------	
Data Bus Hold	tDWH	20	------	
WR Pulse Width	tWR	70	------	



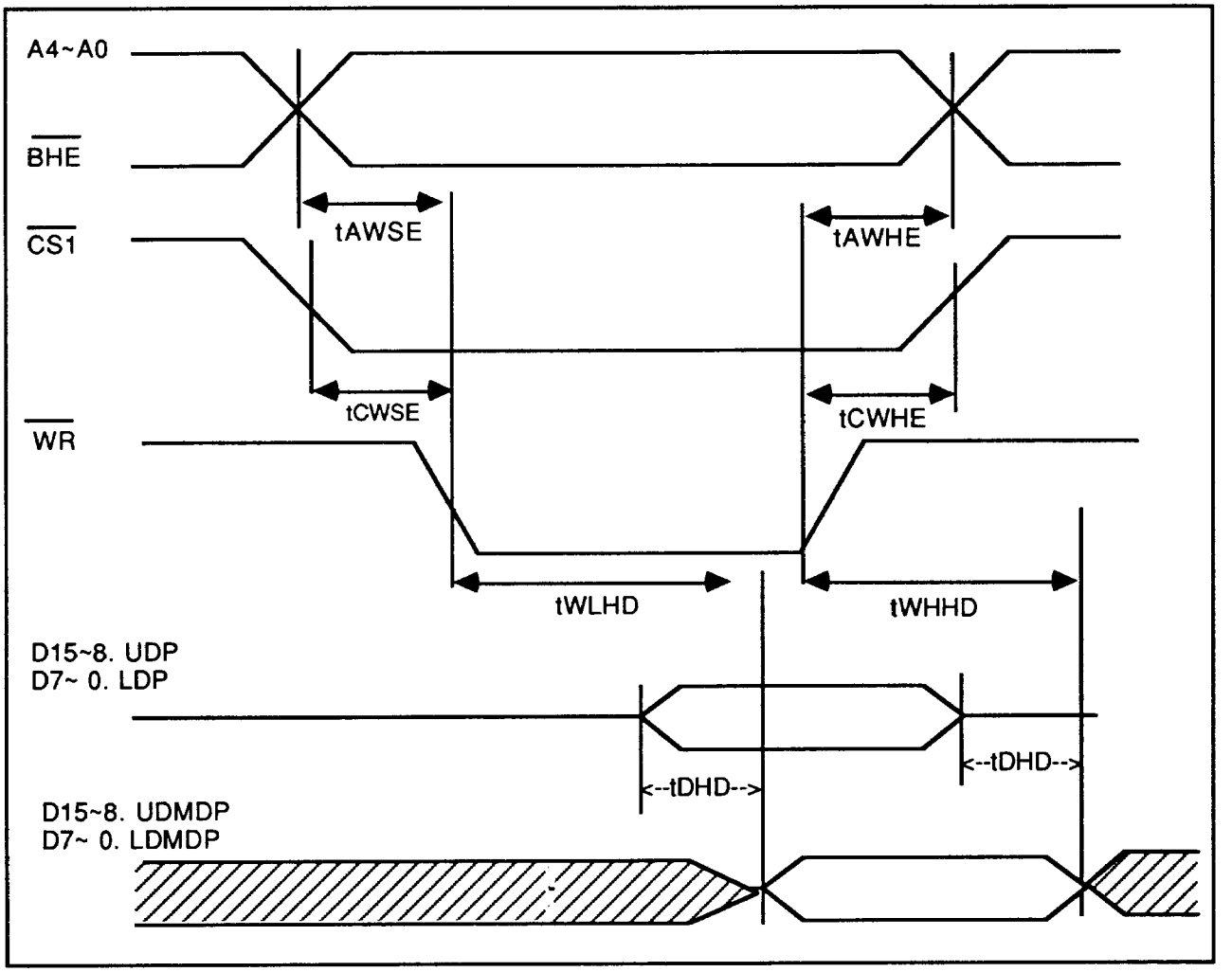
2-1-2. Reading Register (80-Family)

Items	Symbols	Rating		U/M
		Min	Max	
Address Set-up	tARS	40	----	ns
Address Hold	tARH	20	----	
$\overline{CS0}$ Set-up	tCRS	20	----	
$\overline{CS0}$ Hold	tCRH	10	----	
$\overline{RD}$ "L"->DATA Specified	tRLD	----	70	
$\overline{RD}$ "H"->DATA Un specified	tRHD	5	----	
$\overline{RD}$ Pulse Width	tRD	70	----	



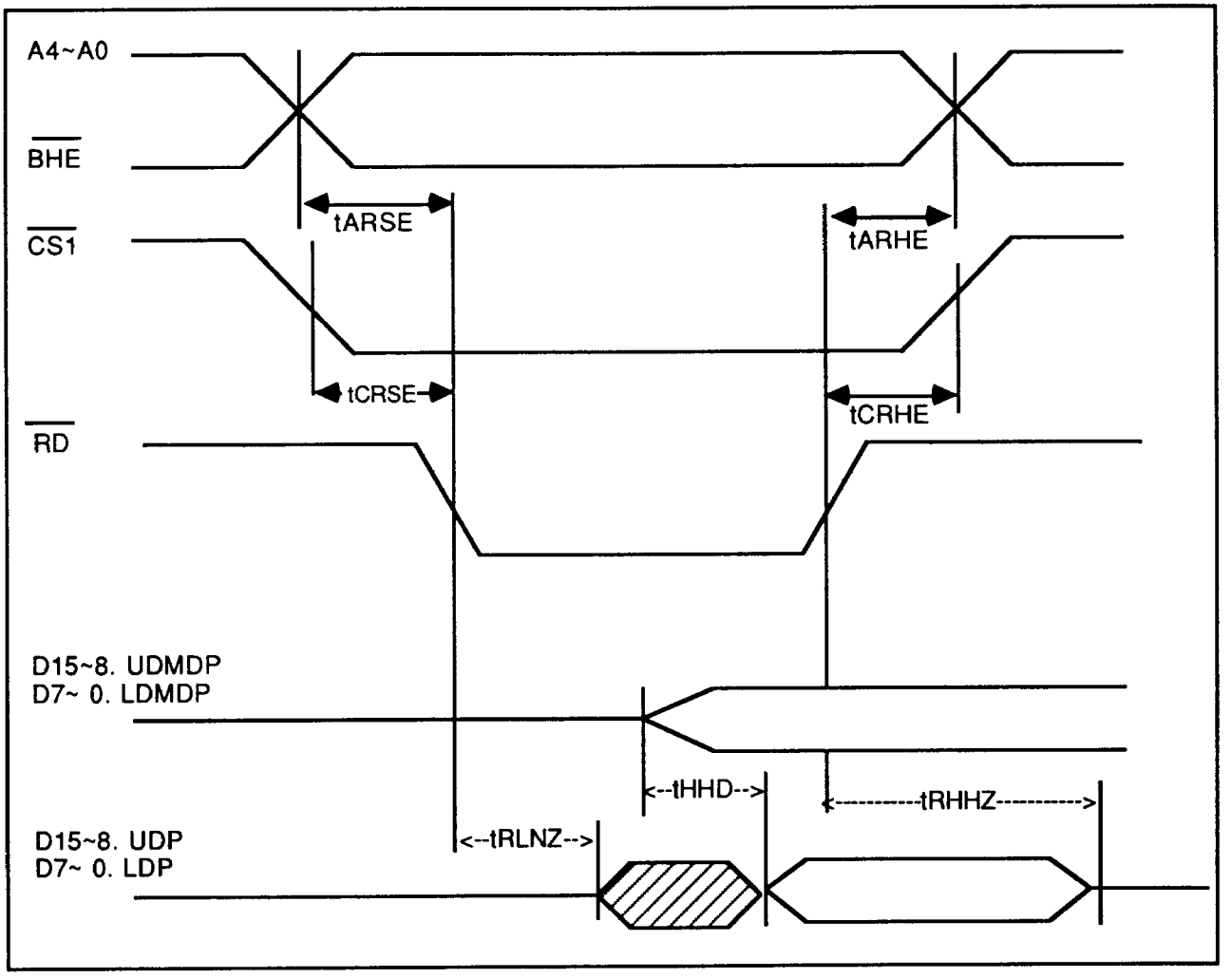
2-1-3. Writing to the Register (80-family; When Externally Accessed)

Items	Symbols	Rating		U/M
		Min	Max	
Address Set-up	tAWSE	40	——	ns
Address Hold	tAWHE	20	——	
$\overline{CS1}$ Set-up	tCWSE	20	——	
$\overline{CS1}$ Hold	tCWHE	10	——	
$\overline{WR}$ "L"->DATA Specified	tWLHD	——	70	
$\overline{WR}$ "H"->DATA unspecified	tWHHD	5	——	
MPU DATA BUS-> DMA BUS DELAY	tDHD	——	40	



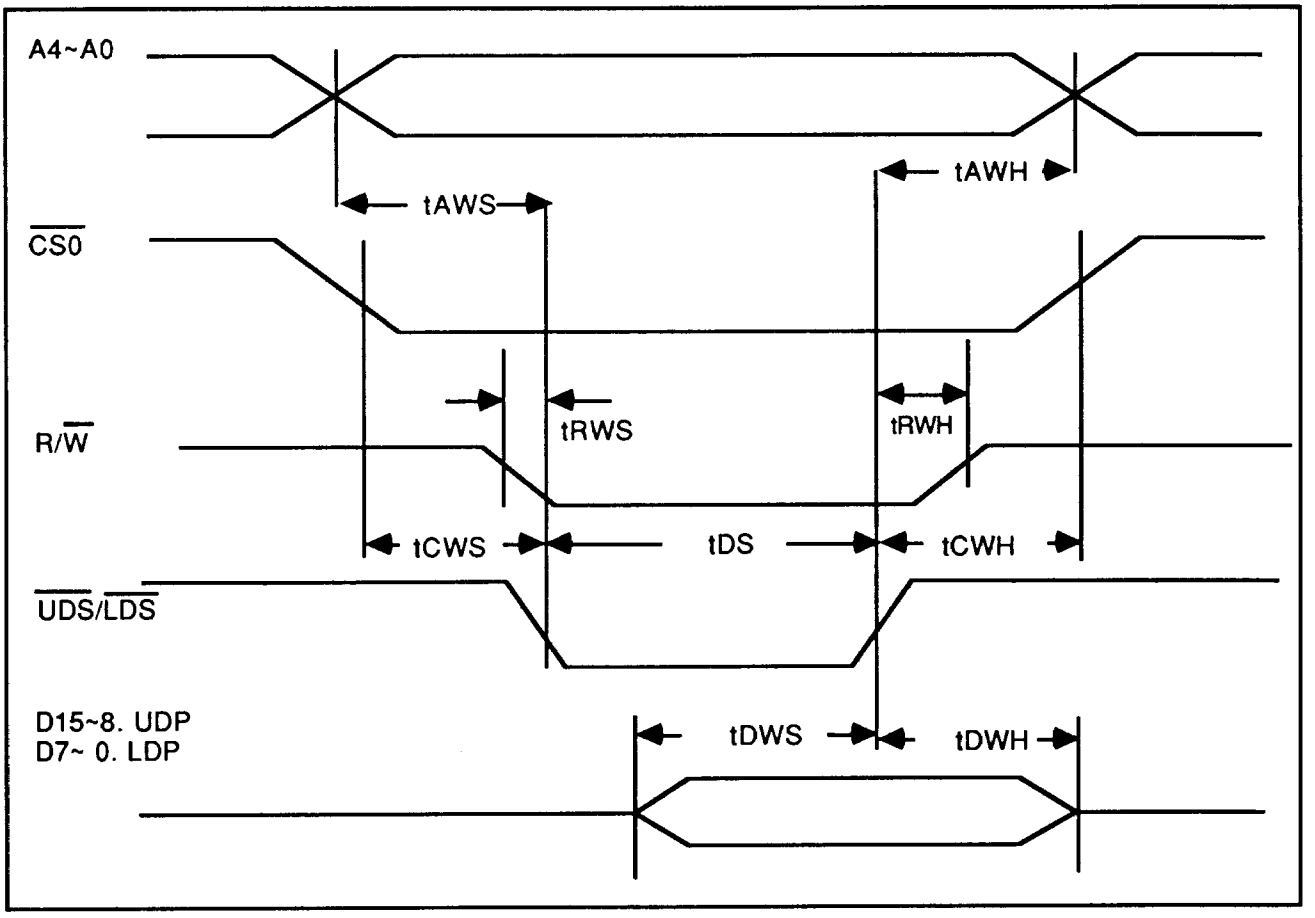
2-1-4. Reading Register (80-Family; When Externally Accessed)

Items	Symbols	Rating		U/M
		Min	Max	
Address Set-up	tARSE	40	----	ns
Address Hold	tARHE	20	----	
$\overline{CS1}$ Set-up	tCRSE	20	----	
$\overline{CS1}$ Hold	tCRHE	10	-----	
$\overline{RD}$ "L" ->DMA bus output	tRLNZ	----	70	
$\overline{RD}$ "H" ->DMA bus HIGH Z	tRHHZ	5	----	
MPU DATA BUS-> DMA BUS DELAY	tHHD	-----	40	



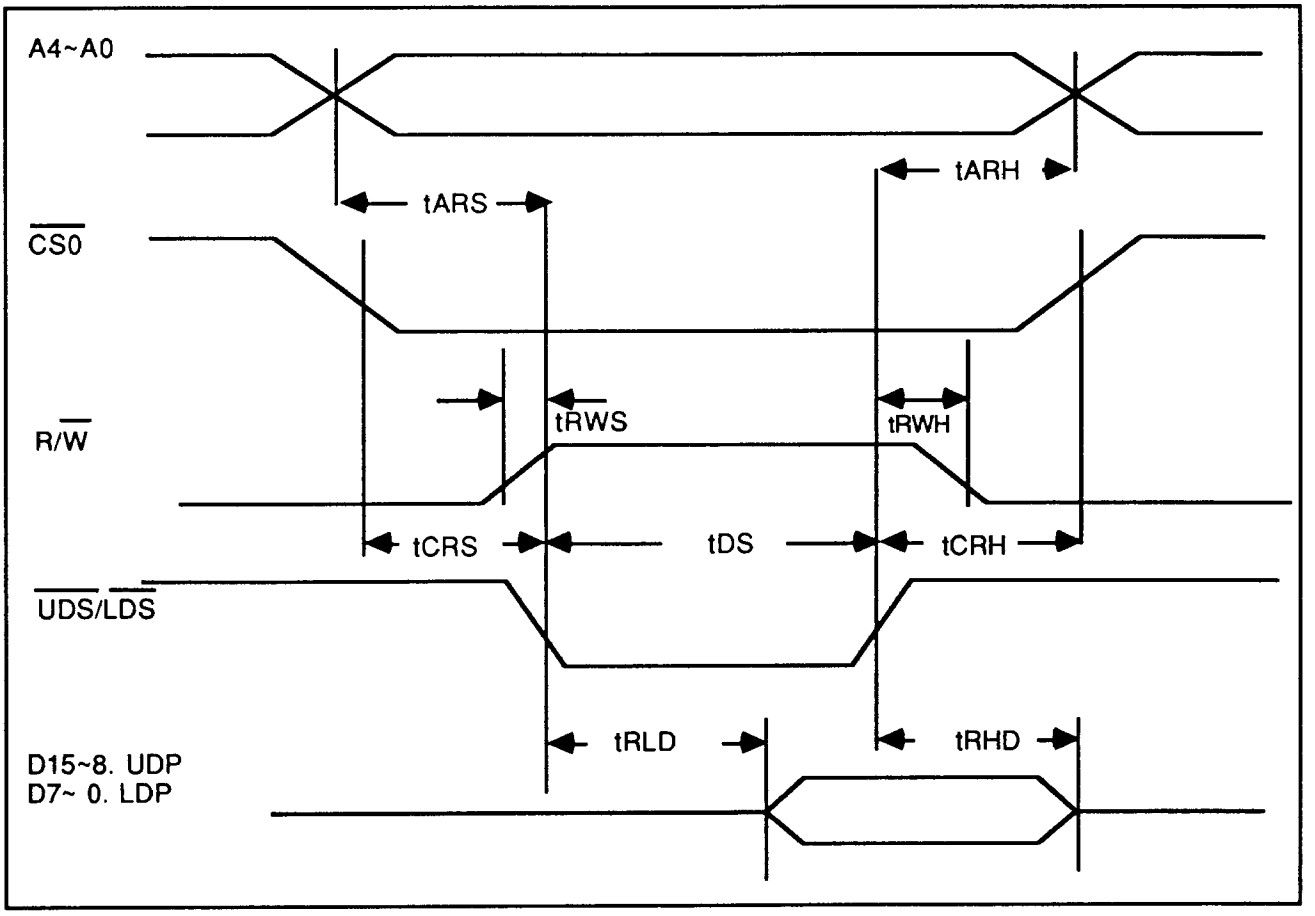
2-2-1. Writing to Register (68-Family)

Items	Symbols	Rating		U/M
		Min	Max	
Address Set-up	tAWS	40	----	ns
Address Hold	tAWH	20	----	
$\overline{CSO}$ Set-up	tCWS	20	----	
$\overline{CSO}$ Hold	tCWH	10	----	
DATA BUS Set Up	tDWS	40	----	
DATA BUS Hold	tDWH	20	----	
$\overline{UDS}/\overline{LDS}$ Pluse Width	tDS	70	----	
R/$\overline{W}$ Set-up	tRWS	20	----	
R/$\overline{W}$ Hold	tRWH	20	----	



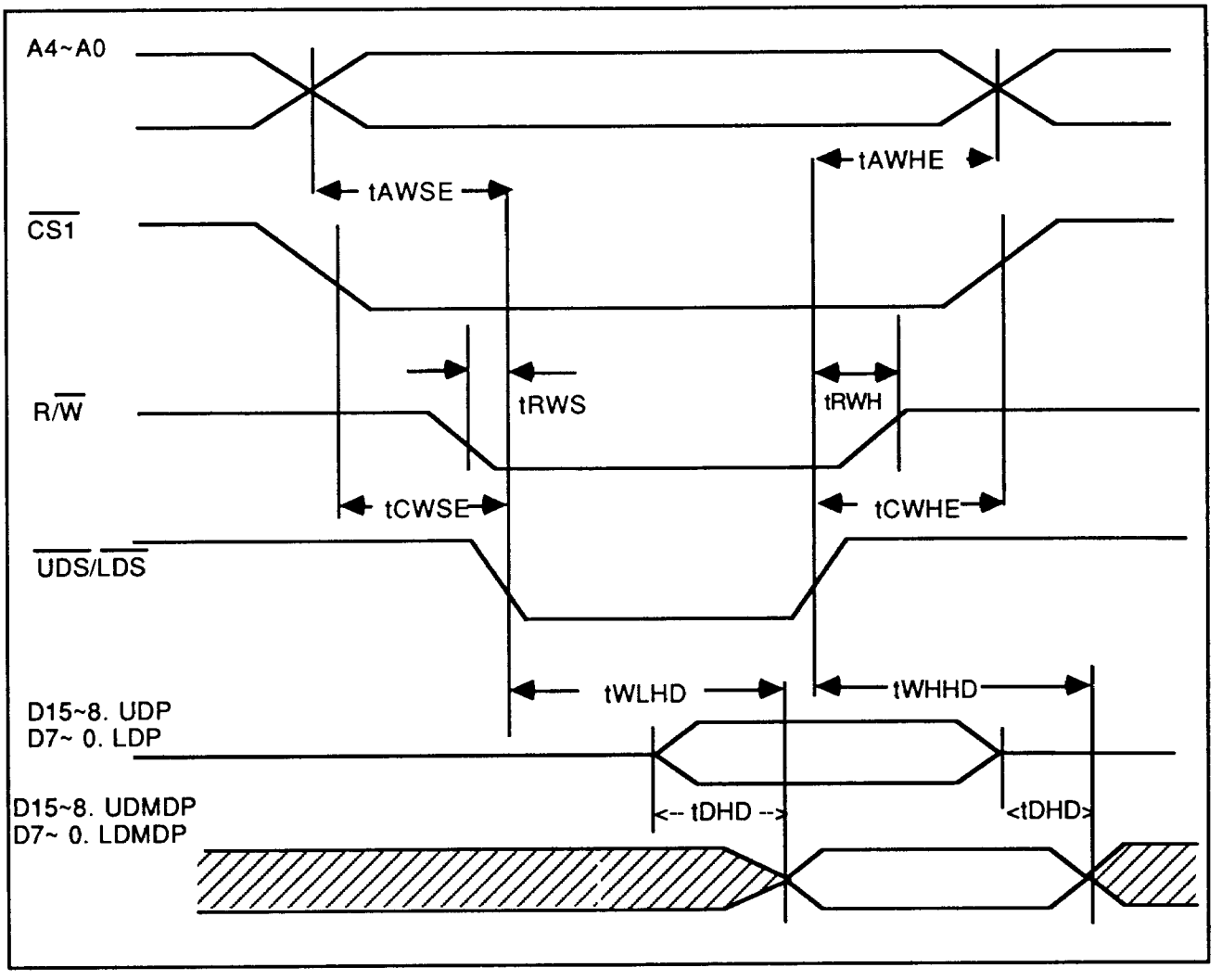
2-2-2. Register Reading (68-family)

Items	Symbols	Rating		U/M
		Min	Max	
Address Set-up	tARS	40	——	ns
Address Hold	tARH	20	——	
$\overline{CSO}$ Set-up	tCRS	20	——	
$\overline{CSO}$ Hold	tCRH	10	——	
$\overline{UDS}/\overline{LDS}$ "L"->DATA Specified	tRLD	——	70	
$\overline{UDS}/\overline{LDS}$ "H"->DATA Unspecified	tRHD	5	——	
$\overline{UDS}/\overline{LDS}$ Pluse Width	tDS	70	——	
R/$\overline{W}$ Set Up	tRWS	20	——	
R/$\overline{W}$ Hold	tRWH	20	——	



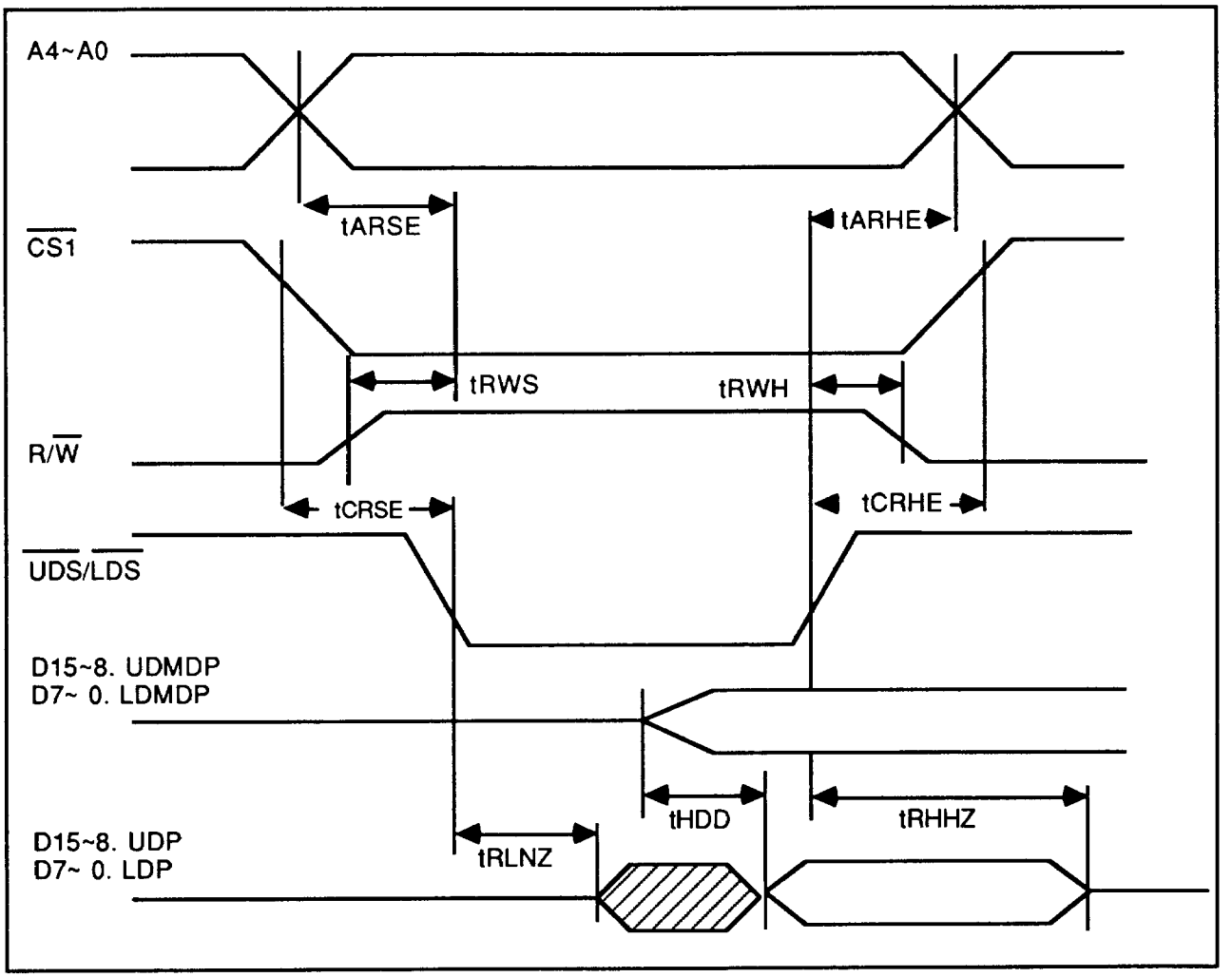
2-2-3. Writing in Register (68-Family; When Externally Accessed)

Items	Symbols	Rating		U/M
		Min	Max	
Address Set-up	tAWSE	40	----	ns
Address Hold	tAWHE	20	----	
$\overline{CS1}$ Set-up	tCWSE	20	----	
$\overline{CS1}$ Hold	tCWHE	10	-----	
$\overline{UDS}$/$\overline{LDS}$ "L"->DMA Output Specified	tWLHD	----	70	
$\overline{UDS}$/$\overline{LDS}$ "H"->DMA Output Unspecified	tWHHD	5	-----	
$\overline{UDS}$/$\overline{LDS}$ Pluse Width	tDHD	----	40	
R/$\overline{W}$ Set Up	tRWS	20	-----	
R/$\overline{W}$ Hold	tRWH	20	-----	



2-2-4. Register Reading (68-family Access Time)

Items	Symbols	Rating		U/M
		Min	Max	
Address Set-up	tARSE	40	----	ns
Address Hold	tARHE	20	----	
$\overline{CS1}$ Set-up	tCRSE	20	----	
$\overline{CS1}$ Hold	tCRHE	10	----	
$\overline{UDS}$/$\overline{LDS}$ "L"->DATA Output	tRLDZ	----	70	
$\overline{UDS}$/$\overline{LDS}$ "H"->DATA HIGH Z	tRHHZ	5	----	
DMA BUS->MPU DATA Delay	tHDD	----	40	
R/$\overline{W}$ Set Up	tRWS	20	----	
R/$\overline{W}$ Hold	tRWH	20	----	



3. DMA Interface

In terms of DMA access times, the timing rules that are specified in this section do not apply if:

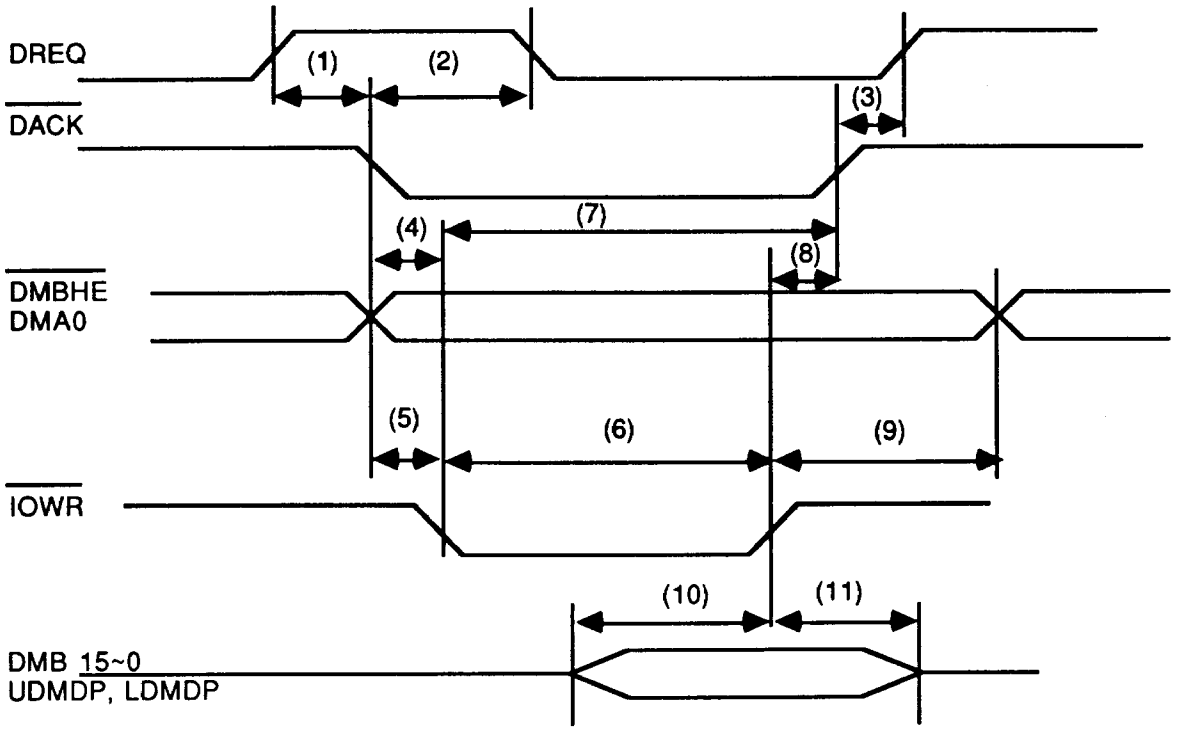
- The data buffer is empty, or holds 1 Byte, during an input operation via the SCSI

- The data buffer is full, or holds 31 Bytes, during an output operation via the SCSI

- Parity errors are detected (target)

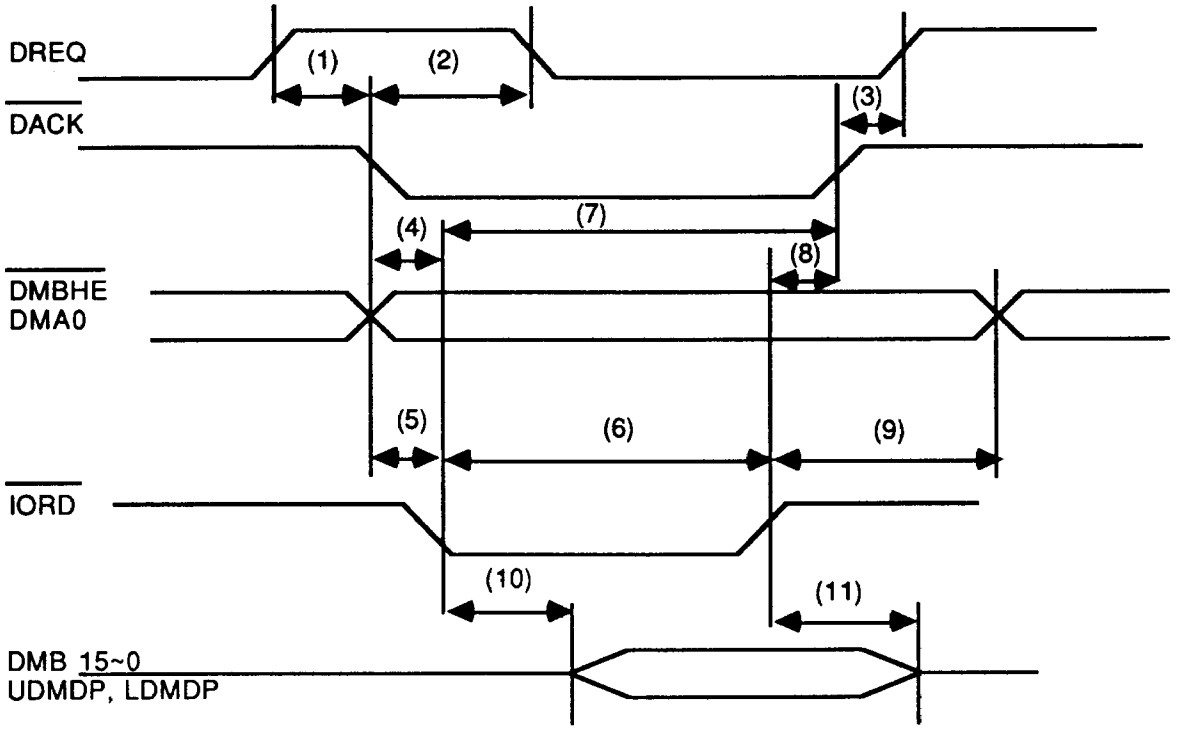
- An error has occurred to the terminate transfer via the SCSI interface.

3-1-1. 80- Family Hand Shake Mode (1) Writing:



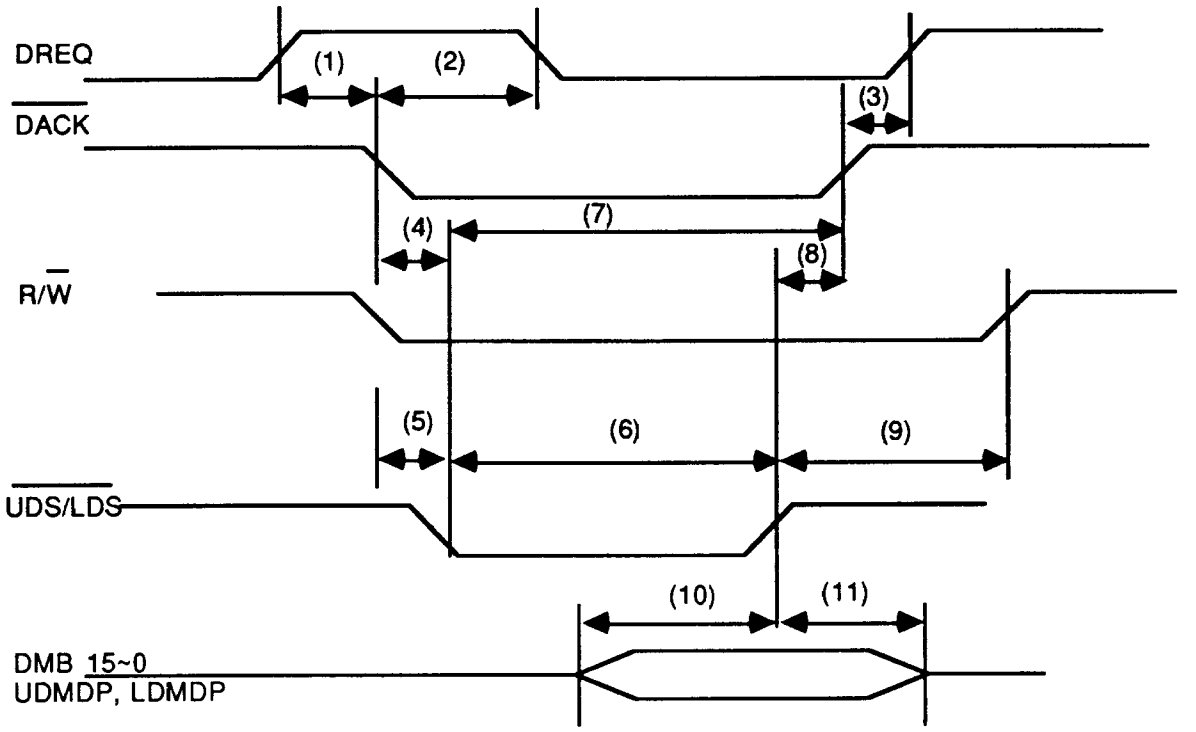
	Items	Rating		U/M
		Min	Max	
1	DREQ "H" -> DACK "L"	0	----	ns
2	DACK "L" -> DREQ "L"	-----	40	
3	DACK "H" -> DACK "H" (8 bit) (MB86601 only)	-----	50	
	DACK "H" -> DACK "H" (8 bit) (MB86602A only)		40	
	DACK "H" -> DACK "H" (16 bit)	-----	2tCLF + 40	
4	DACK "L" -> IOWR "L"	0	----	
5	DMBHE, DMAO SET-UP	20	----	
6	IOWR Pulse Width	40	----	
7	IOWR "L" -> DACK "H"	1tCLF	----	
8	IOWR "H" --> DACK "H"	0	----	
9	DMBHE, DMAO HOLD	20	----	
10	INPUT DATA SETUP	30	----	
11	INPUT DATA HOLD	10	----	

3-1-1. 80- Family Hand Shake Mode (2) Reading:



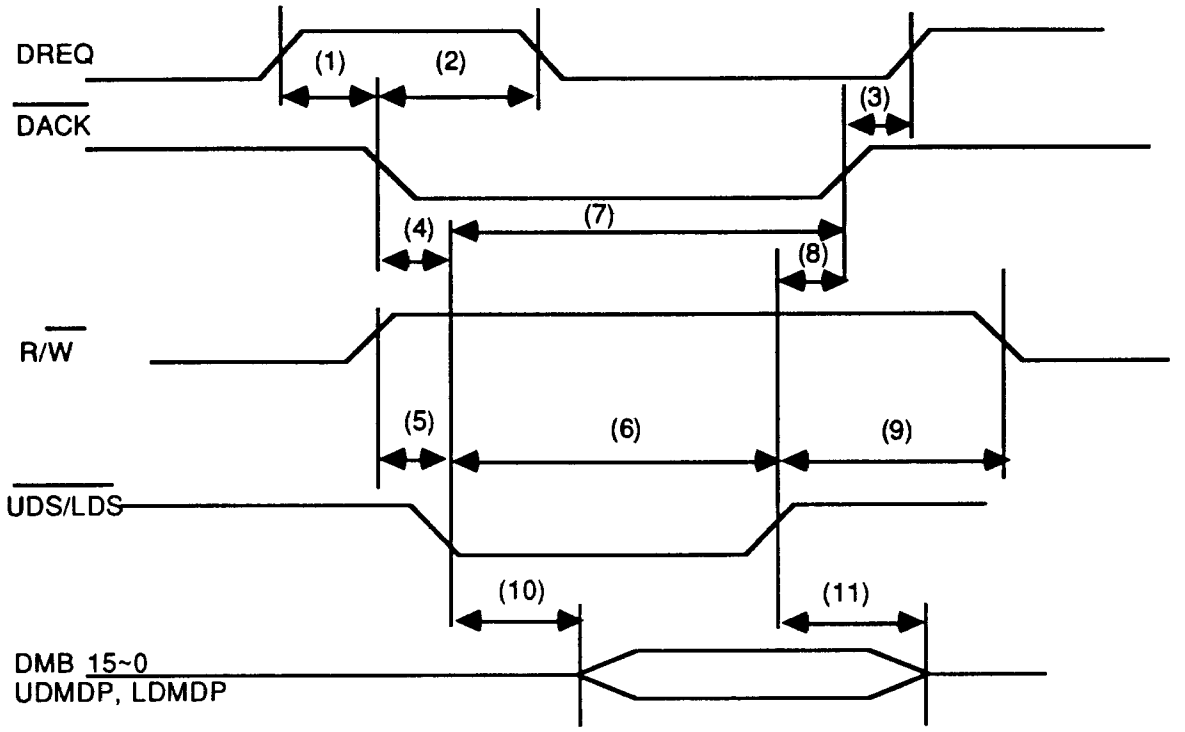
	Items	Rating		U/M
		Min	Max	
1	DREQ "H" -> $\overline{\text{DACK}}$ "L"	0	----	ns
2	$\overline{\text{DACK}}$ "L" -> DREQ "L"	----	40	
3	$\overline{\text{DACK}}$ "H" -> $\overline{\text{DACK}}$ "H" (8 bit) (MB86601 only)	----	50	
	$\overline{\text{DACK}}$ "H" -> $\overline{\text{DACK}}$ "H" (8 bit) (MB86602A only)	----	40	
	$\overline{\text{DACK}}$ "H" -> $\overline{\text{DACK}}$ "H" (16 bit)	----	2tCLF + 40	
4	$\overline{\text{DACK}}$ "L" -> IORD "L"	0	----	
5	$\overline{\text{DMBHE}}$, DMAO SET-UP	20	----	
6	$\overline{\text{IORD}}$ Pulse Width	40	----	
7	$\overline{\text{IORD}}$ "L" -> $\overline{\text{DACK}}$ "H"	1tCLF	----	
8	$\overline{\text{IORD}}$ "H" --> $\overline{\text{DACK}}$ "H"	0	----	
9	$\overline{\text{DMBHE}}$, DMAO HOLD	20	----	
10	OUTPUT DATA VALID	----	40	
11	OUTPUT DATA HOLD	5	----	

3-1-2. 68- Family Hand Shake Mode (1) Writing:



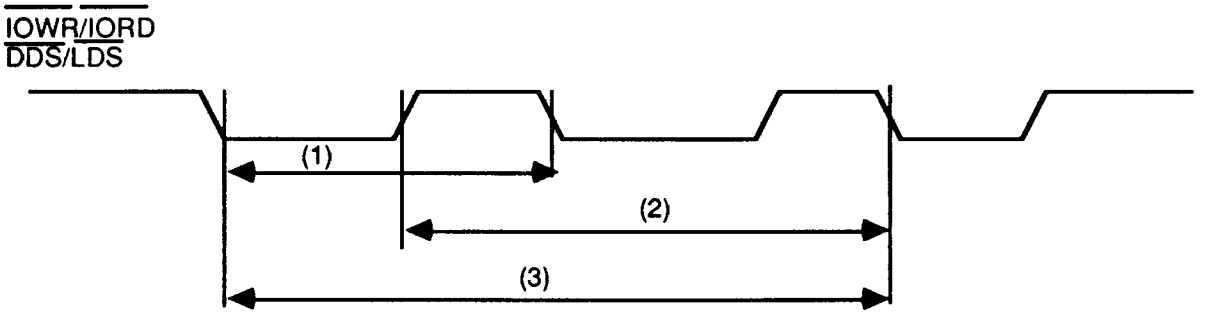
	Items	Rating		U/M
		Min	Max	
1	DREQ "H" -> $\overline{\text{DACK}}$ "L"	0	----	ns
2	$\overline{\text{DACK}}$ "L" -> DREQ "L"	----	40	
3	$\overline{\text{DACK}}$ "H" -> DREQ "H" (8 bit) (MB86601 only)	----	50	
	$\overline{\text{DACK}}$ "H" -> DREQ "H" (8 bit) (MB86602A only)	----	40	
	$\overline{\text{DACK}}$ "H" -> DREQ "H" (16 bit)	----	2tCLF + 40	
4	$\overline{\text{DACK}}$ "L" -> $\overline{\text{UDS}}$/$\overline{\text{LDS}}$ "L"	0	----	
5	R/$\overline{\text{W}}$ SET-UP	20	----	
6	$\overline{\text{UDS}}$/$\overline{\text{LDS}}$ Pulse Width	40	----	
7	$\overline{\text{UDS}}$/$\overline{\text{LDS}}$ "L" -> $\overline{\text{DACK}}$ "H"	1tCLF	----	
8	$\overline{\text{UDS}}$/$\overline{\text{LDS}}$ "H" --> $\overline{\text{DACK}}$ "H"	0	----	
9	R/$\overline{\text{W}}$ HOLD	20	----	
10	INPUT DATA SETUP	30	----	
11	INPUT DATA HOLD	10	----	

3-1-2. 68- Family Hand Shake Mode (2) Reading:



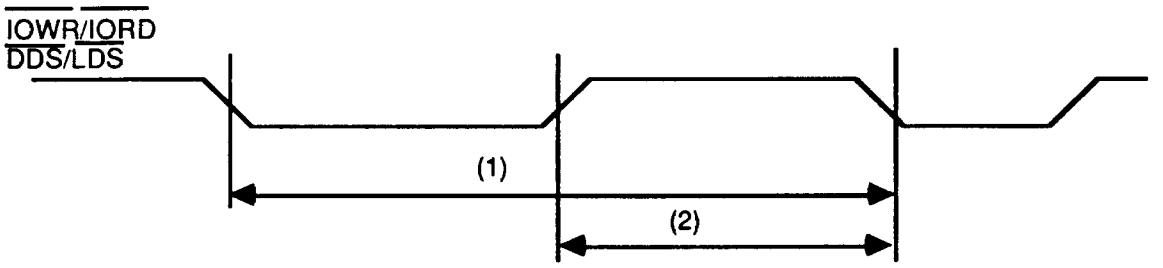
	Items	Rating		U/M
		Min	Max	
1	DREQ "H" -> $\overline{\text{DACK}}$ "L"	0	----	ns
2	$\overline{\text{DACK}}$ "L" -> DREQ "L"	----	40	
3	$\overline{\text{DACK}}$ "H" -> DREQ "H" (8 bit) (MB86601 only)	----	50	
	$\overline{\text{DACK}}$ "H" -> DREQ "H" (8 bit) (MB86602A only)	----	40	
	$\overline{\text{DACK}}$ "H" -> DREQ "H" (16 bit)	----	2tCLF + 40	
4	$\overline{\text{DACK}}$ "L" ->$\overline{\text{UDS}}$/$\overline{\text{LDS}}$ "L"	0	----	
5	R/$\overline{\text{W}}$ SET-UP	20	----	
6	$\overline{\text{UDS}}$/$\overline{\text{LDS}}$ Pulse Width	40	----	
7	$\overline{\text{UDS}}$/$\overline{\text{LDS}}$ "L" -> $\overline{\text{DACK}}$ "H"	1tCLF	----	
8	$\overline{\text{UDS}}$/$\overline{\text{LDS}}$ "H" --> $\overline{\text{DACK}}$ "H"	0	----	
9	R/$\overline{\text{W}}$ HOLD	20	----	
10	OUTPUT DATA VALID	----	40	
11	OUTPUT DATA HOLD	5	----	

3-2-1. Burst Mode: Access Cycle Time (1) 8 Bit



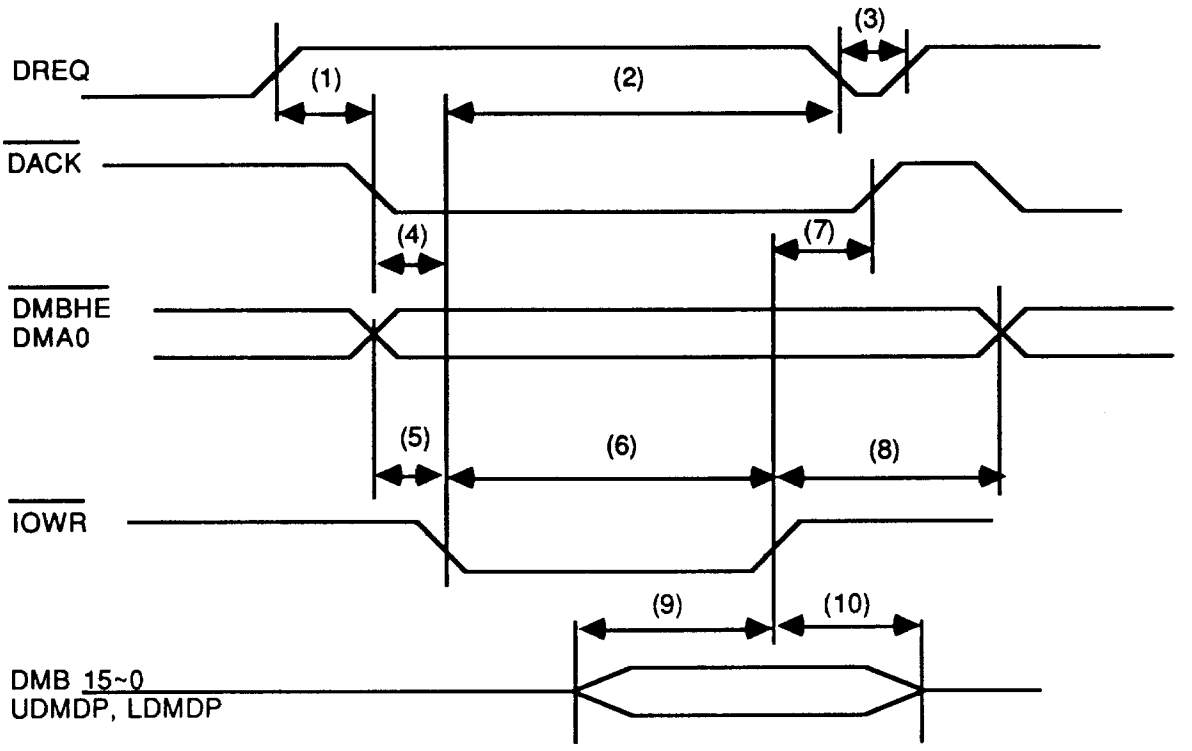
	Items	Rating		U/M
		Min	Max	
1	Access Cycle (1)	tCLF	-----	ns
2	Access Cycle (2)	3tCLF	-----	
3	Access Cycle (3)	4tCLF	-----	

3-2-1. Burst Mode: Access Cycle Time (2) 16 Bit



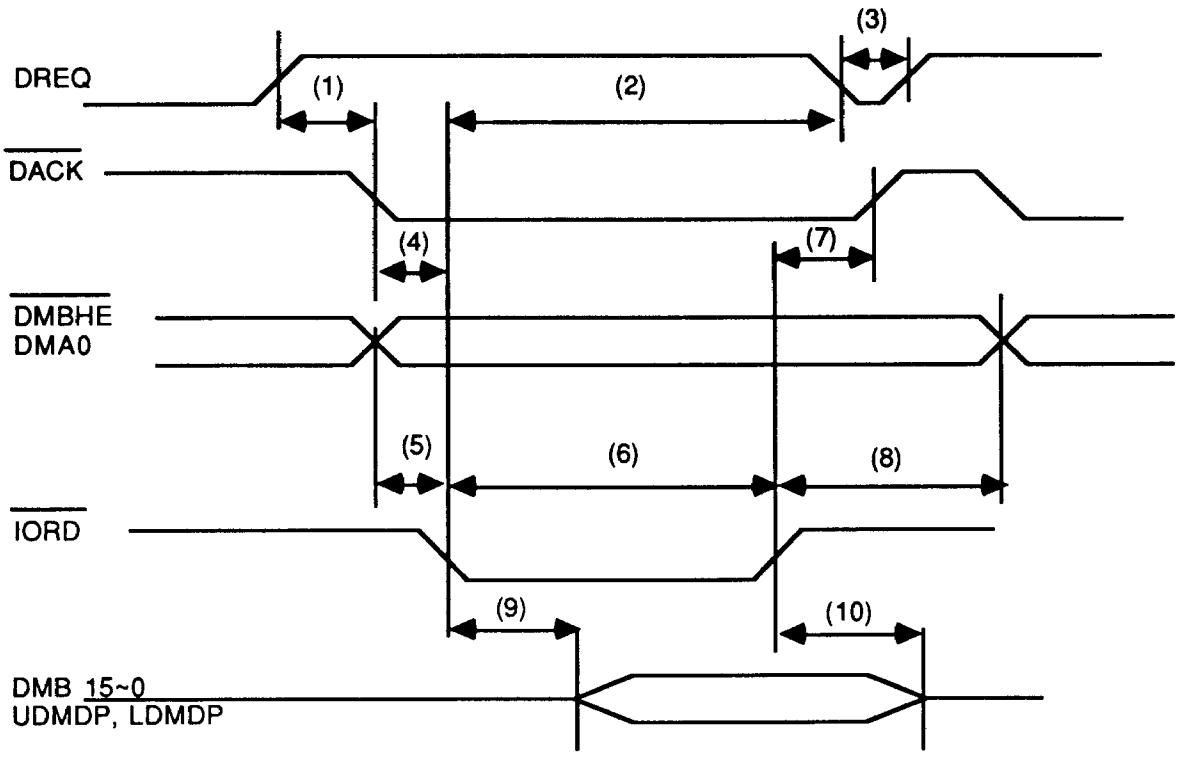
	Items	Rating		U/M
		Min	Max	
1	Access Cycle (1)	4tCLF	-----	ns
2	Access Cycle (2)	3tCLF	-----	

3-2-2. 80-Family Burst Mode (1) Writing



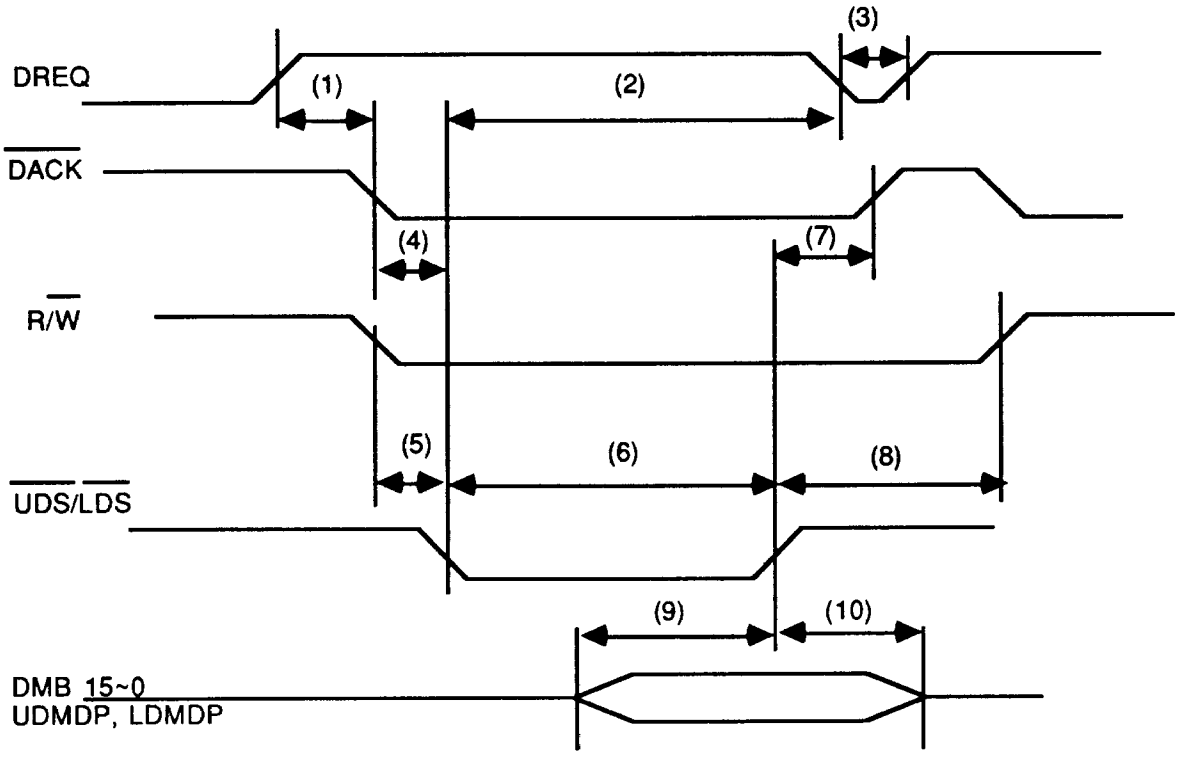
	Items	Rating		U/M
		Min	Max	
1	DREQ "H" -> $\overline{\text{DACK}}$ "L"	0	-----	ns
2	$\overline{\text{IOWR}}$ "L" -> DREQ "L"	-----	60	
3	DREQ "L" -> DREQ "H"	0	-----	
4	$\overline{\text{DACK}}$ "L" -> $\overline{\text{IOWR}}$ "L"	0	-----	
5	$\overline{\text{DMBHE}}$, DMAO SET-UP	20	-----	
6	$\overline{\text{IOWR}}$ Pulse Width	40	-----	
7	$\overline{\text{IOWR}}$ "H" -> $\overline{\text{DACK}}$ "H"	0	-----	
8	$\overline{\text{DMBHE}}$, DMAO HOLD	20	-----	
9	INPUT DATA SETUP	30	-----	
10	INPUT DATA HOLD	10	-----	

3-2-2. 80-Family Burst Mode (2) Reading



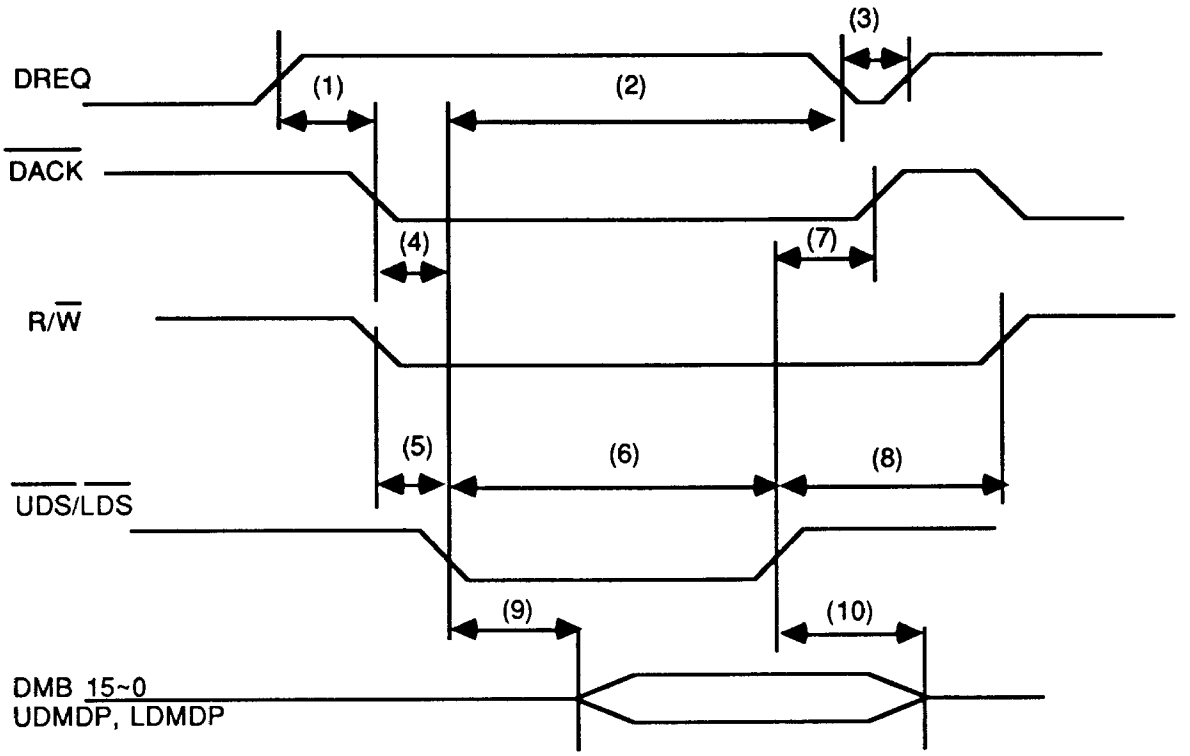
	Items	Rating		U/M
		Min	Max	
1	DREQ "H" -> $\overline{\text{DACK}}$ "L"	0	-----	ns
2	$\overline{\text{IORD}}$ "L" -> DREQ "L"	-----	60	
3	DREQ "L" -> DREQ "H"	0	-----	
4	$\overline{\text{DACK}}$ "L" -> $\overline{\text{IORD}}$ "L"	0	-----	
5	$\overline{\text{DMBHE}}$, DMAO SET-UP	20	-----	
6	$\overline{\text{IORD}}$ Pulse Width	40	-	
7	$\overline{\text{IORD}}$ "H" -> $\overline{\text{DACK}}$ "H"	0	-----	
8	$\overline{\text{DMBHE}}$, DMAO HOLD	20	-----	
9	OUTPUT DATA VALID	-----	40	
10	OUTPUT DATA HOLD	5	-	

3-2-3. 68-Family Burst Mode (1) Writing



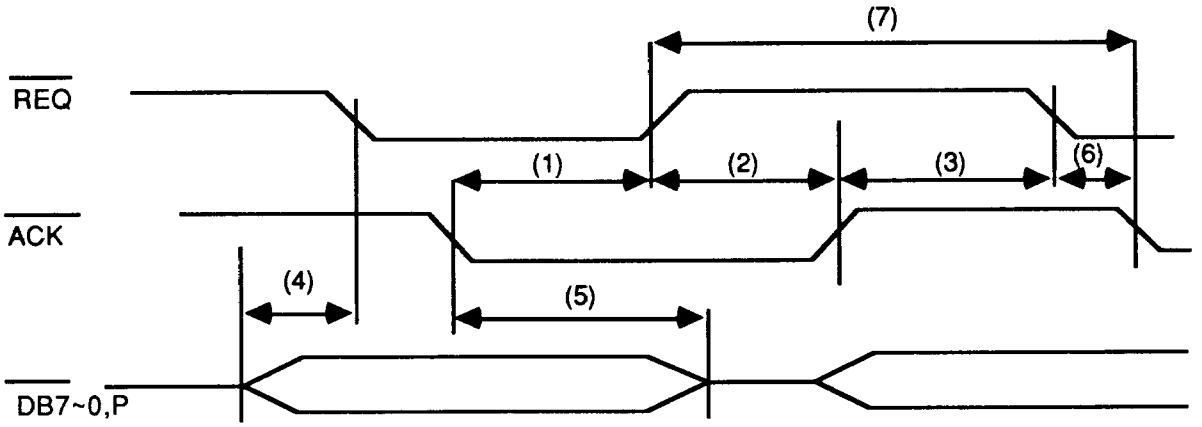
	Items	Rating		U/M
		Min	Max	
1	DREQ "H" -> $\overline{\text{DACK}}$ "L"	0	-----	ns
2	$\overline{\text{UDS}}/\overline{\text{LDS}}$ "L" -> DREQ "L"	-----	60	
3	DREQ "L" -> DREQ "H"	0	-----	
4	$\overline{\text{DACK}}$ "L" ->$\overline{\text{UDS}}/\overline{\text{LDS}}$ "L"	10	-----	
5	$\overline{\text{R/W}}$ Set Up	20	-----	
6	$\overline{\text{UDS}}/\overline{\text{LDS}}$ Pulse Width	40	-----	
7	$\overline{\text{UDS}}/\overline{\text{LDS}}$ "H" -> DACK "H"	0	-----	
8	R/$\overline{\text{W}}$ Hold	20	-----	
9	INPUT DATA SETUP	30	-----	
10	INPUT DATA HOLD	10	-----	

3-2-3. 68-Family Burst Mode (2) Reading



	Items	Rating		U/M
		Min	Max	
1	DREQ "H" -> $\overline{\text{DACK}}$ "L"	0	-----	ns
2	$\overline{\text{UDS}}/\overline{\text{LDS}}$ "L" -> DREQ "L"	-----	60	
3	DREQ "L" -> DREQ "H"	0	-----	
4	$\overline{\text{DACK}}$ "L" -> $\overline{\text{UDS}}/\overline{\text{LDS}}$ "L" (MB86601)	10	-----	
	$\overline{\text{DACK}}$ "L" -> $\overline{\text{UDS}}/\overline{\text{LDS}}$ "L" (MB86602A)	0	-----	
5	R/$\overline{\text{W}}$ Set Up	20	-----	
6	$\overline{\text{UDS}}/\overline{\text{LDS}}$ Pulse Width	40	-----	
7	$\overline{\text{UDS}}/\overline{\text{LDS}}$ "H" -> $\overline{\text{DACK}}$ "H"	0	-----	
8	R/$\overline{\text{W}}$ Hold	20	-----	
9	OUTPUT DATA VALID	-----	40	
10	OUTPUT DATA HOLD	5	-----	

4-1-1. Asynchronous Initiator (1) Input

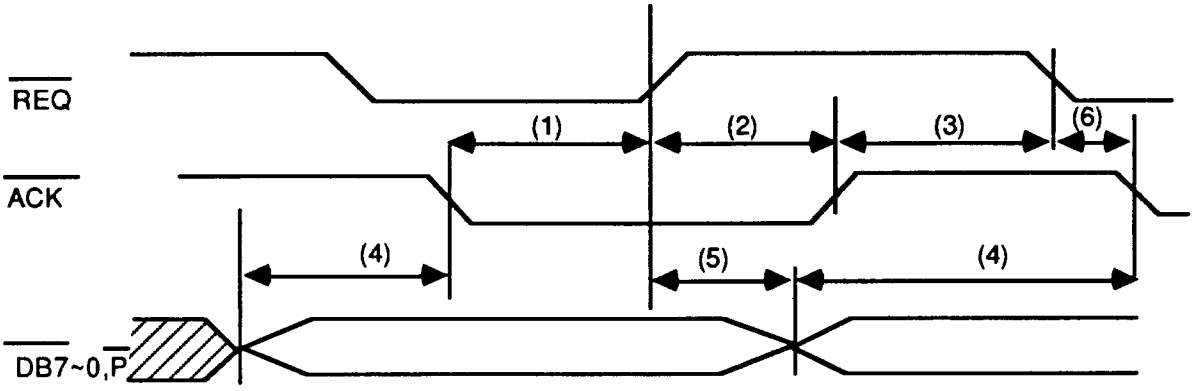


	Items	Rating		U/M
		Min	Max	
1	ACK "L" -> REQ "H" ->	0	----	ns
2	REQ "H" -> ACK "H"	----	60	
3	ACK "H" -> REQ "L"	0	----	
4	DATA BUS Specified -> REQ "L"	10	----	
5	ACK "L" -> DATA BUS Hold	10	----	
6	REQ "L" -> ACK "L"	20	40	
7	REQ "H" -> ACK "L"	----	3tCLF+40	

*1. Duration for REQ "H" -> ACK "L" is defined by the longer of [(2)+(3)+(6)] or (7).

*2. The definition of time as noted in this section does not apply when:
- the data register is full during data phase
- during last byte transferred

4-1-1. Asynchronous Initiator (2) Output



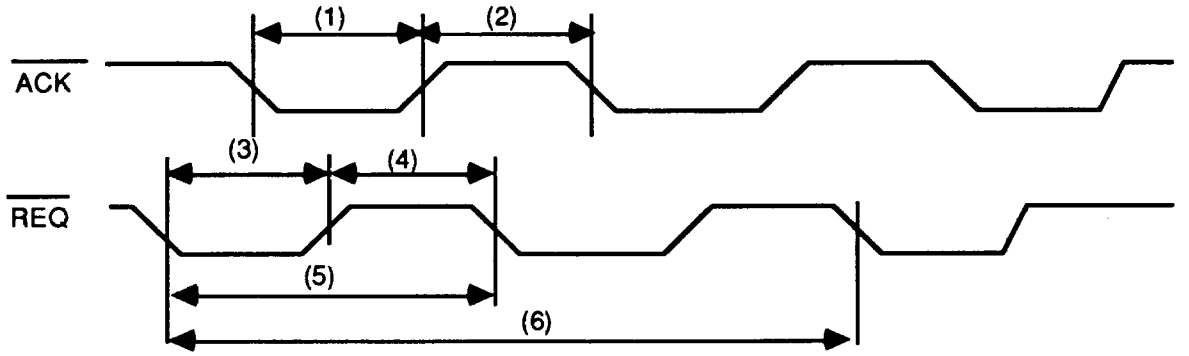
	Items	Rating		U/M
		Min	Max	
1	$\overline{ACK}$ "L" -> $\overline{REQ}$ "H" ->	0	-----	ns
2	$\overline{REQ}$ "H" -> $\overline{ACK}$ "H"	-----	60	
3	$\overline{ACK}$ "H" -> $\overline{REQ}$ "L"	10	----	
4	DATA BUS Specified -> $\overline{ACK}$ "L" (MB86601 only)	StCLF-10	-----	
	DATA BUS Specified -> $\overline{ACK}$ "L" (MB86602A only)	StCLF-20	StCLF-5	
5	$\overline{REQ}$ "H" -> DATA BUS Hold	2•tCLF	----	
6	$\overline{REQ}$ "L" -> $\overline{ACK}$ "L"	----	40	

*1. The duration of REQ "H" -> ACK "L" is based upon by the longer of either [(2) + (3) +(6)] or [(5) + (4)]

*2. The definition of time/duration as noted in this section does not apply when:
• the data register is empty during the data phase

*3. The value for "S" is based upon the asynchronous setup time register (Address 23) setting.

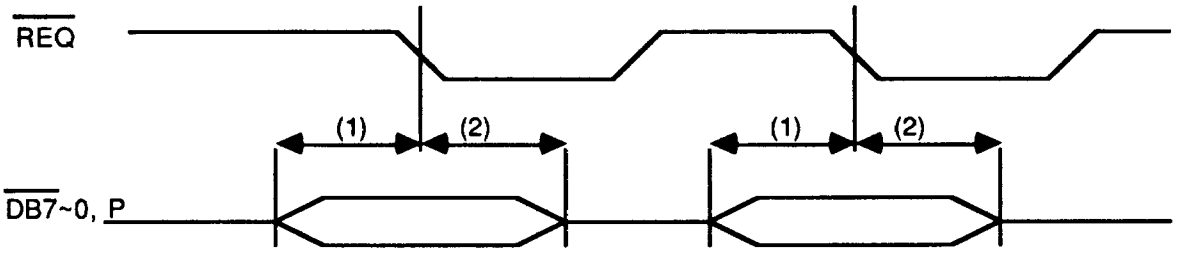
4-1-2. Synchronous Transfer Initiator (1) REQ/ACK Cycle



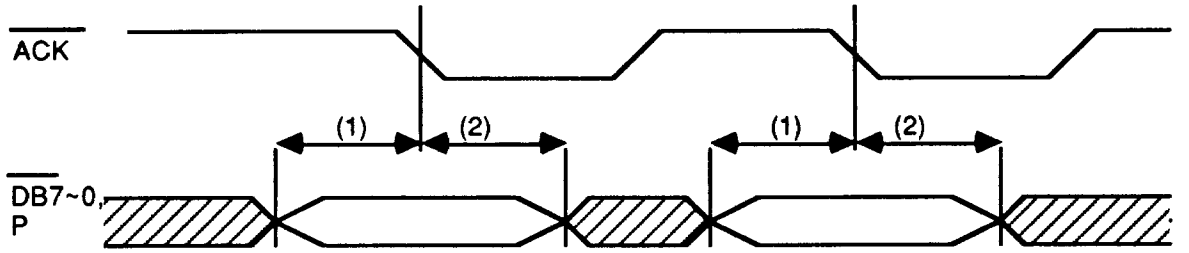
	Items	Rating		U/M
		Min	Max	
1	$\overline{ACK}$ Assertion Period (MB86601)	A•tCLF-5	----	ns
	$\overline{ACK}$ Assertion Period (MB86602A)	A•tCLF		
2	$\overline{ACK}$ Negation Period (MB86601)	N•tCLF-5	----	
	$\overline{ACK}$ Negation Period (MB86602A)	N•tCLF-10		
3	$\overline{REQ}$ Assertion Period	30	----	
4	$\overline{REQ}$ Negation Period	30	----	
5	$\overline{REQ}$ Input Cycle Time (1)	1tCLF	----	
6	$\overline{REQ}$ Input Cycle Time (2)	3tCLF	----	

*Values for 'A' and 'N' are based upon the setting of the transfer period register (Address 13).

4-1-2. Synchronous Transfer Initiator (2) Input



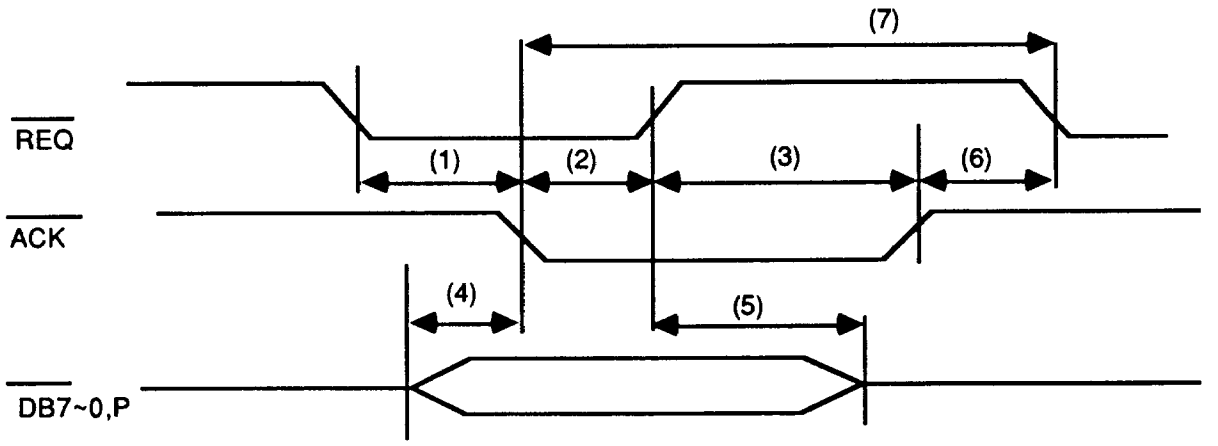
	Items	Rating		U/M
		Min	Max	
1	DATA BUS Specified -> REQ "H"	10	----	ns
2	REQ "L" -> DATA BUS Hold	20	----	



	Items	Rating		U/M
		Min	Max	
1	DATA BUS Specified ->$\overline{ACK}$-> "L" (MB86601 only)	N•tCLF-10	----	ns
	DATA BUS Specified ->$\overline{ACK}$-> "L" (MB86602A only)	N•tCLF-20		
2	$\overline{ACK}$ "L" -> DATA BUS Hold	A•tCLF	----	

* The value for A and N are based on the transfer period register (address 13) setting.

4-2-1. Asynchronous Target (1) Input



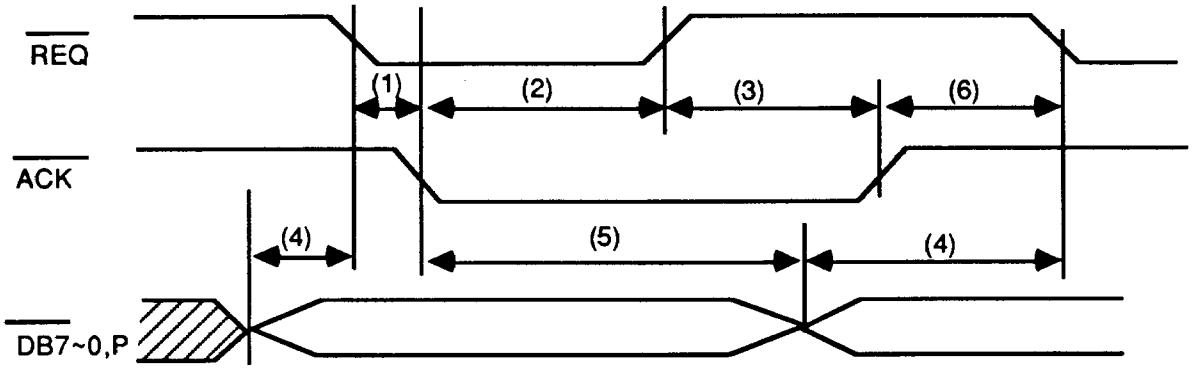
	Items	Rating		U/M
		Min	Max	
1	REQ "L" ->ACK "L"	0	----	ns
2	ACK "L" -> REQ "H"	----	60	
3	REQ "H" ->ACK "H"	0	----	
4	DATA BUS Specified -> ACK "L"	10	----	
5	REQ "H" -> DATA BUS Hold	20	----	
6	ACK "H" -> REQ "L"	----	40	
7	ACK "L" -> REQ "L"	----	3tCLF+40	

*1. The duration of ACK "L" ->REQ "L" is determined by the longer of either [(2) + (3) +(6)] or (7).

*2. The definition of time/duration as noted in this section does not apply when:

- the data register is full during the data phase

4-2-1. Asynchronous Target (2) Output



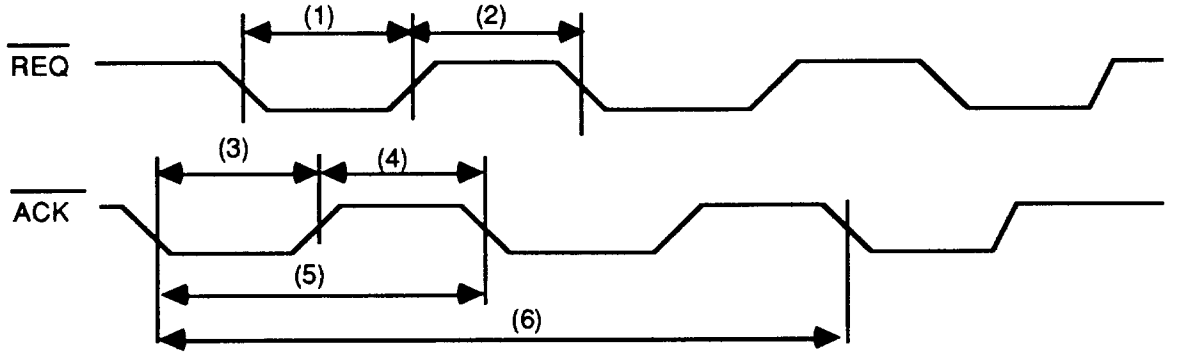
	Items	Rating		U/M
		Min	Max	
1	$\overline{REQ}$ "L" ->$\overline{ACK}$ "L"	0	-----	ns
2	$\overline{ACK}$ "L" -> $\overline{REQ}$ "H"	----	60	
3	$\overline{REQ}$ "H" ->$\overline{ACK}$ "H"	0	----	
4	DATA BUS OUTPUT (MB86601) Specified -> $\overline{REQ}$ "L"	S•tCLF-10	-----	
	DATA BUS OUTPUT (MB86602A) Specified -> $\overline{REQ}$ "L"	S•tCLF-20	S•tCLF-5	
5	$\overline{ACK}$ "L" -> DATA BUS Hold	2tCLF	-----	
6	$\overline{ACK}$ "H" -> $\overline{REQ}$ "L"	----	40	

*1. The Duration for ACK "L" --> REQ "L" is defined by longer of either [(2)+(3)+(6)] or (7).

*2. The definition of the time/duration as noted in this section does not apply when:
• the data register is empty during the data phase

*3. The value for S' is based upon the setting of the asynchronous setup time register (Address 23).

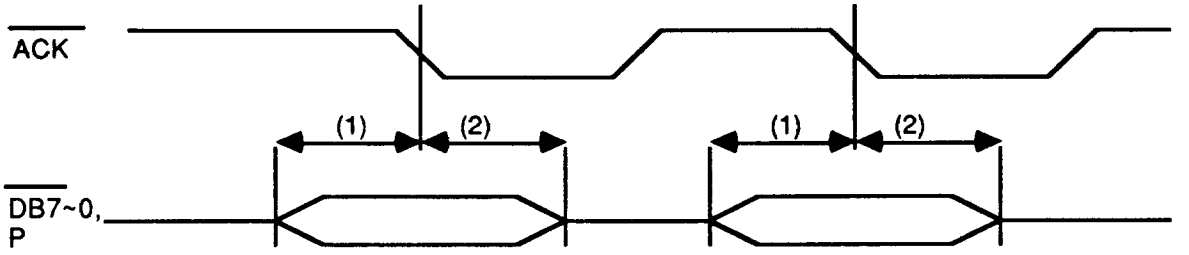
4-2-2. Synchronous Transfer Target (1) REQ/ACK Cycle



	Items	Rating		U/M
		Min	Max	
1	$\overline{REQ}$ Assertion Period (MB86601)	A•tCLF-5	----	ns
	$\overline{REQ}$ Assertion Period (MB86602A)	A•tCLF	----	
2	$\overline{REQ}$ Negation Period (MB86601)	N•tCLF-5	----	
	$\overline{REQ}$ Negation Period (MB86602A)	N•tCLF-10	----	
3	$\overline{ACK}$ Assertion Period	30	----	
4	$\overline{ACK}$ Negation Period	30	----	
5	$\overline{ACK}$ Input Cycle Time (1)	1tCLF	----	
6	$\overline{ACK}$ Input Cycle Time (2)	3tCLF	----	

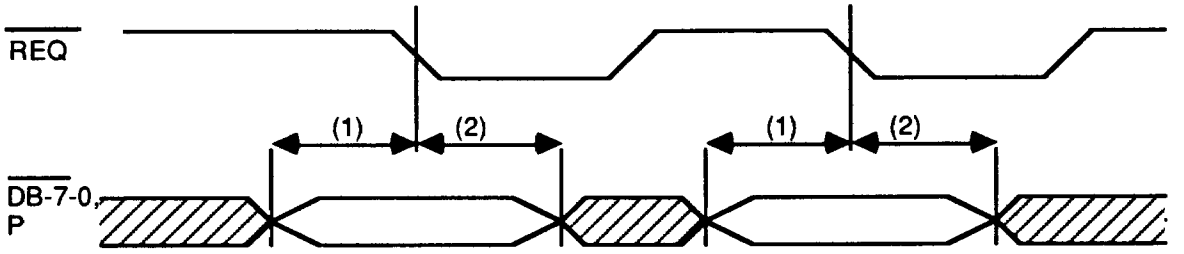
* The value for A and N are based on the setting of the transfer period register (address 13).

4-2-2. Synchronous Transfer Target (2) Input



	Items	Rating		U/M
		Min	Max	
1	DATA BUS Specified ->$\overline{ACK}$ "L"	10	----	ns
2	$\overline{ACK}$ "L" -> DATA BUS Hold	20	-----	

4-2-2. Synchronous Transfer Target (3) Output



	Items	Rating		U/M
		Min	Max	
1	DATA BUS Specified ->$\overline{REQ}$-> "L" (MB86601 only)	N•tCLF- 10	----	ns
	DATA BUS Specified ->$\overline{REQ}$-> "L" (MB86602A only)	N•tCLF- 20	----	
2	$\overline{REQ}$ "L" -> DATA BUS Hold	A•tCLF	----	

* The value for A and N are based on the setting of the transfer period register (address 13).

5. Table

(1) Transfer Period Register Setting and the Values of A and N

TP-REG					A	N	TP-REG					A	N
4	3	2	1	0			4	3	2	1	0		
0	0	0	0	1	(Unautho-rized)	(Unautho-rized)	1	0	0	0	1	9	8
0	0	0	1	0	1	1	1	0	0	1	0	9	9
0	0	0	1	1	2	1	1	0	0	1	1	10	9
0	0	1	0	0	2	2	1	0	1	0	0	10	10
0	0	1	0	1	3	2	1	0	1	0	1	11	10
0	0	1	1	0	3	3	1	0	1	1	0	11	11
0	0	1	1	1	4	3	1	0	1	1	1	12	11
0	1	0	0	0	4	4	1	1	0	0	0	12	12
0	1	0	0	1	5	4	1	1	0	0	1	13	12
0	1	0	1	0	5	5	1	1	0	1	0	13	13
0	1	0	1	1	6	5	1	1	0	1	1	14	13
0	1	1	0	0	6	6	1	1	1	0	0	14	14
0	1	1	0	1	7	6	1	1	1	0	1	15	14
0	1	1	1	0	7	7	1	1	1	1	0	15	15
0	1	1	1	1	8	7	1	1	1	1	1	16	15
1	0	0	0	0	8	8	0	0	0	0	0	16	16

(2) Asynchronous Setup Time Setting and the Value for S:

SUP-REG				S
3	2	1	0	
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15
0	0	0	0	16